Improved Silicon Quantum Dots Single Electron Transfer Operation with Hydrogen Silsesquioxane Resist Technology

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Hydrogen silsesquioxane (HSQ) is a high resolution electron beam resist that offers a high etch resistance and small line edge roughness [1-3]. In our previous work [4], we showed that by using this resist we can fabricate very high density double quantum dot (QD) single electron transistors on silicon-on-insulator (SOI) substrates for applications in quantum information processing. We observed that 80% of 144 fabricated devices had dimensional variations of ±5 nm with a standard deviation of 3.4 nm. Here, we report on the functionality of our Si QD devices through electrical measurements and further HSQ process optimisations, which improve the effective side gates control on single electron operation.

Fig. 1 shows a scanning electron micrograph (SEM) of the typical arrangement of a double quantum dot (DQD) transistors etched into a 50 nm thick SOI. A low electron concentration for conduction in the SOI is induced by the application of a top gate (not shown) bias. The devices are intrinsic silicon islands connected to the source (S) and drain (D) leads by narrow constrictions that act as tunnel junctions. A 4% HSQ resist (55 nm thick) process optimisation allowed for realisation of reproducible silicon islands of 50 nm and tunnel junctions of 25 nm. The constrictions along with the capacitively coupled side gates, which are ~60 nm away, allowed for formation and control of potential barriers that modulate electron tunnelling through the two QDs between the source and the drain. One of the two transistors here acts as an electrometer to detect changes in the charge configuration in the other, which is operated as a turnstile for electrons.

Electrical measurements of the drain current, I_{DS}, of the turnstile was performed as a function of varying drain voltage, V_{DS}, and top gate voltage, V_{TG}, at a base temperature of 80 mK. A plot (Fig. 2) of the absolute drain current $|I_{DS}|$ revealed diamond shaped coulomb blockade regions which indicate single electron transfer through the QDs. From this plot a charging energy of 5 meV was extracted signifying QD dimensions of 25 nm. This is dimensionally consistent with that expected from the fabrication process where a 10 nm thermal oxide was formed to reduce the QD dimensions. In Fig. 3 we present a plot of I_{DS} as a function of applied biases on side gates 1 and 3 with side gate 2 grounded and V_{DS} = 1 mV and V_{TG}= 3.87 V. An active control of coulomb oscillations was observed, which indicates a strongly coupled DQD system. However, due the weak decoupling effect from the bias on side gate 2 on these dots, we were unable to obtain the expected honeycomb shaped charge stability diagram [5].

For effective side gate control of single electrons in the DQD, we further attempted to fabricate devices with the side gates closer to the constrictions and QDs. A 2% HSQ resist (25 nm thick) process with extensive dose optimisation was performed to realise DQD transistors with side gate to QD separations less than 20 nm. Fig.4 shows an SEM of the improved DQD system etched into a 30 nm SOI substrate, where the side gates and transistors are as close as ~14 nm. A detailed fabrication process to achieve these extremely high density quantum devices along with electrical characteristics will also be presented.

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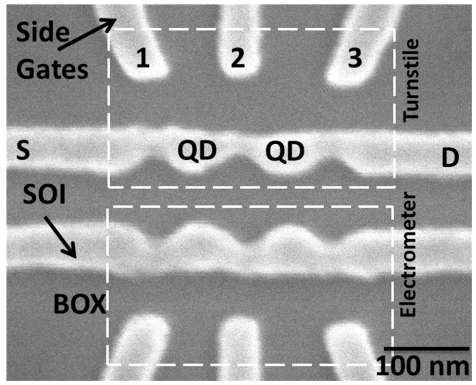

Fig. 1. SEM of a DQD device etched into 50 nm thick SOI and realised by using a 4% HSQ resist. Here the side gates (1-3) are ~60 nm away from the constrictions.

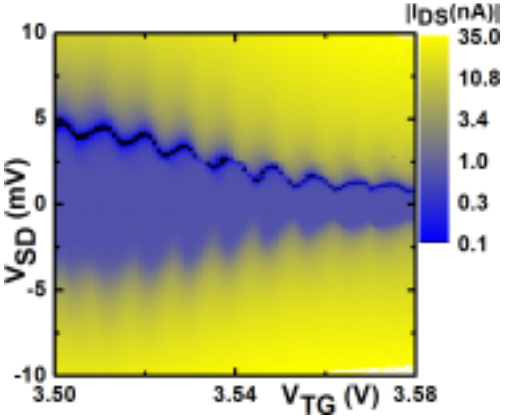

Fig. 2. A plot of a turnstile $|I_{DS}|$ as a function of V_{DS} and V_{TG} at a base temperature of 80 mK. All other electrodes were grounded.

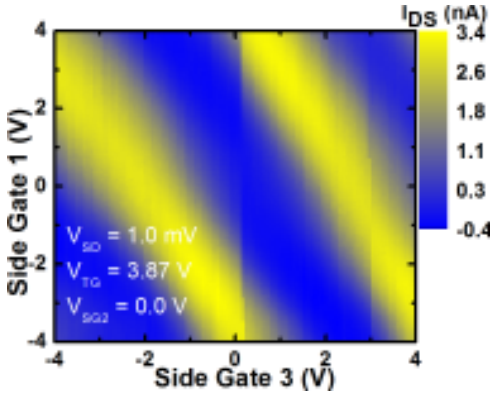

Fig. 3. A plot of a turnstile I_{DS} at 80 mK as a function of applied voltages on side gate 1 and side gate 3 with V_{DS}= 1 mV, V_{TG}= 3.87 V and all other electrodes grounded.

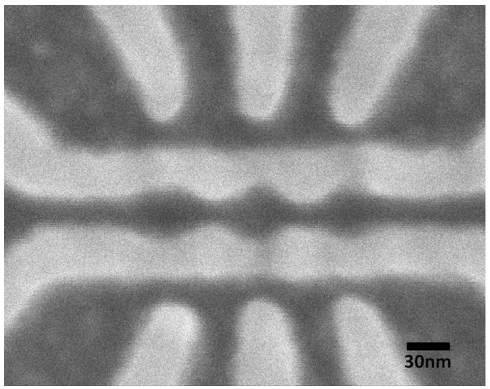

Fig. 4. SEM of DQD devices etched into 25 nm SOI and realised by using a 2% HSQ resist (25 nm thick) process. Here the side gates and transistors are as close as ~14 nm.