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Design and fabrication of densely integrated silicon quantum dots using a VLSI compatible hydrogen silsesquioxane electron beam lithography process

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ABSTRACT

Hydrogen silsesquioxane (HSQ) is a high resolution negative-tone electron beam resist allowing for direct transfer of nanostructures into silicon-on-insulator. Using this resist for electron beam lithography, we fabricate high density lithographically defined Silicon double quantum dot (QD) transistors. We show that our approach is compatible with very large scale integration, allowing for parallel fabrication of up to 144 scalable devices. HSQ process optimisation allowed for realisation of reproducible QD dimensions of 50 nm and tunnel junction down to 25 nm. We observed that 80% of the fabricated devices had dimensional variations of less than 5 nm. These are the smallest high density double QD transistors achieved to date. Single electron simulations combined with preliminary electrical characterisations justify the reliability of our device and process.

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1. Introduction

Hydrogen silsesquioxane (HSQ) is increasingly being used as the resist of choice for nano-scale electron beam lithography (EBL) capable of sub 10 nm [1] parallel line definition. As a negative resist, its small line edge roughness [2,3] is particularly useful for precise nano-scale patterning of quantum dots (QDs). This, coupled with its high etching resistance property after curing, allows for direct pattern transfer into silicon-on-insulator (SOI) for applications in quantum information technology [4]. This offers a competitive advantage over positive resist alternatives such as poly methylmethacrylate (PMMA) and ZEP520 where nanostructure fabrication requires an additional lift off process which often suffers from significant line edge roughness. In addition, HSQ can be directly imaged in a scanning electron microscope (SEM), allowing for faster process optimisation and device turnaround time. The few-nm scale resolution that HSQ offers is crucial in enabling true single electron occupancy in lithographically defined solid state QDs for use in a single electron transistor (SET) [5]. A SET comprises of a source and drain terminal weakly coupled via electron tunnel barriers to a nano-scale conduction island (the QD), whose number of occupied electrons can be individually controlled by electrostatically coupled gates [8].

In this work, we optimise the first very large scale integration (VLSI) compatible EBL process using HSQ resist for large scale parallel fabrication of up to 144 reproducible intrinsic silicon based QD transistors with potential for scalability in the quantum architecture and true single electron storage and manipulation in the QD. HSQ is used with an optimised E-Beam process for realisation of high density nano-scale double QD SETs (DSETs) [9] with near perfect pattern transfer after etching into SOI. The dimensions achieved with EBL pave a way towards precise control of QD occupations down to the single electron regime. Measurement results from electrical characterisations are combined with Monte Carlo-based single electron simulations of device design for an indication of the viability of our platform and process.

2. Design and simulations

Our device (Fig. 1a and b) is a pair of DSETs defined in the top 50 nm intrinsic-Si layer of an SOI substrate. Its ability to conduct is through the use of inversion carriers induced by a metal top gate [10]. This offers greater control over the electron concentration in a QD compared to heavily doped Si QDs [5,10], allowing for occupancies down to the few electron regime. The two QDs in each of our designed DSET ($QD_{1,2}$ and $QD_{a,b}$) are weakly coupled to each other and to their respective source and drain terminals via channel constrictions which form electron tunnel barriers. Each DSET has two side gates ($G_{1,2}$ and $G_{a,b}$) where applied voltages electrostatically control the discrete electron occupation of each of its two QDs. One of the two DSETs acts as an electrometer to detect changes in the charge configuration in the other, which is operated as a turnstile for electrons [7]. It is crucial to have a small distance d_1

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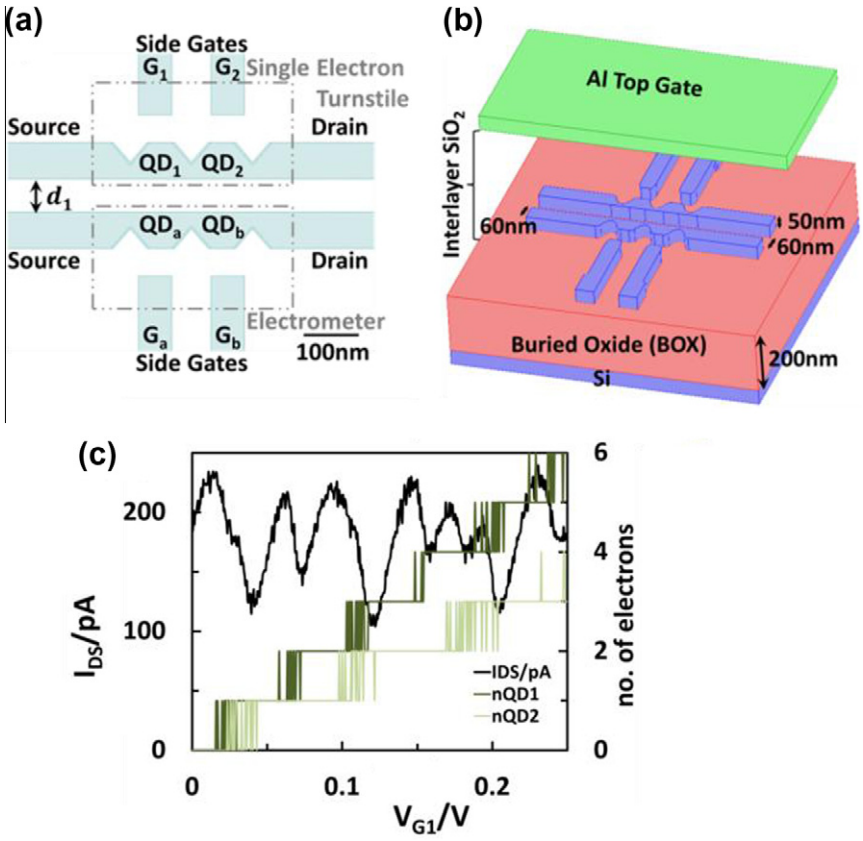

Fig. 1. (a) Schematic top down view of two DSETs defined in the top intrinsic-Si layer of the SOI. (b) The 3D structural model of the nanostructure used in COMSOL electrostatic simulations with an exception of the Al top gate which has been modified to allow visibility of the underlying QD structure. (c) Graph of the simulated I_{DS} (left axis), and the variation in electron occupation number (right axis), n_{QD1} and n_{QD2}, in QD_1 and QD_2 respectively as a function of an applied voltage V_{G1} on side gate G_1 with side gate G_2 grounded (in this figure a).

for sufficient coupling between the electrometer current and the turnstile's QDs during operation. Here we target d_1 of 60 nm and a side gate to QD gap of 50 nm. The introductory use of HSQ allows for ultra-small realisation of channel constrictions of just 25 nm and 50 nm QD structures – which can be further reduced in dimension to just ~25 nm by thermal oxidation. This design offers both scalability in the number of QDs present as well as doubling the yield in QD device fabrication since only one DSET is operated as a turnstile. The electrometer does not require perfect formation of a double QD (DQD) for good sensitivity as a charge detector; therefore, functionality can be interchanged between the two DSETs depending on fabrication results.

A 3D finite element based (FEM) COMSOL capacitance analysis is combined with Monte Carlo single-electron circuit simulations to model device operations during single electron detection. The 3D structural data (Fig. 1b) of the nanoscale DQD pair and multiple gate electrodes are precisely input into COMSOL's FEM-based electrostatics simulator. Capacitances between different device components are then extracted and fed into the well-tested single electron circuit simulator SETSPICE [11], based on the orthodox theory of single electron tunnelling [12]. For our target d_1 of 60 nm, simulation results (Fig. 1c) showed that as we sweep the voltage applied on gate G_1, V_{G1}, single electron tunnelling into the turnstile's two QDs should generate shifts in the electrometer current, I_{DS}, of tens of pA. This is well within the charge sensitivity of DQD electrometer [6] and consistent to the same order of magnitude with previous work in single electron detection [13]. In addition, the gate to QD capacitive coupling appear to be sufficient for the control of QD occupations down to the single electron limit, allowing for future manipulation of single electron spins in qubit research.

3. Experiment

3.1. Fabrication process

A schematic process flow diagram of our VLSI compatible fabrication process is outlined in Fig. 2. This process is designed to allow for large scale fabrication of integrated scalable QD systems. The thickness of an intrinsic-SOI's top Silicon layer is first thinned to 50 nm via wet thermal oxidation. A 2 μm wide square window of three layers of 33 nm thick SiO_2 is then deposited via plasma enhanced chemical vapour deposition (PECVD), defined optically and reactive ion etched (RIE) to be at the centre of each device. This multilayer deposition is used to minimise pinhole formation between SiO_2 layers, improving its function as a Phosphorus doping mask to protect an intrinsic Si region for the nanostructure. A 1 μm layer of Phosphorosilica film (P concentration of 5×10^{20} cm^{-3}) "spin-on-dopant" is used for Phosphorus doping and thermally activated and driven into the 50 nm Si layer at 925 °C for 15 min. 4-point probe Van-der-Pauw measurements then indicated the formation of a heavily doped Si layer of $n \sim 10^{19}$ cm^{-3}, which is adequate to ensure low device source and drain resistance.

After Phosphorosilica film removal with 20:1 buffered HF, 4% HSQ resist is spin coated on the sample at 5000 RPM and hot-plate baked at 80 °C for 4 min to produce a 55 nm thick layer. Device nanostructures were then written by using a JEOL JBX 9300 FS EBL system. A 1 nA beam current at 100 keV acceleration voltage was used with a 60 μm aperture which generated an estimated exposure spot size of 4 nm. Due to the dense nature of our nanostructure design, definition by EBL was seriously limited by proximity effects where electron scattering outside the desired exposure areas produces undesired resist cross linking. This

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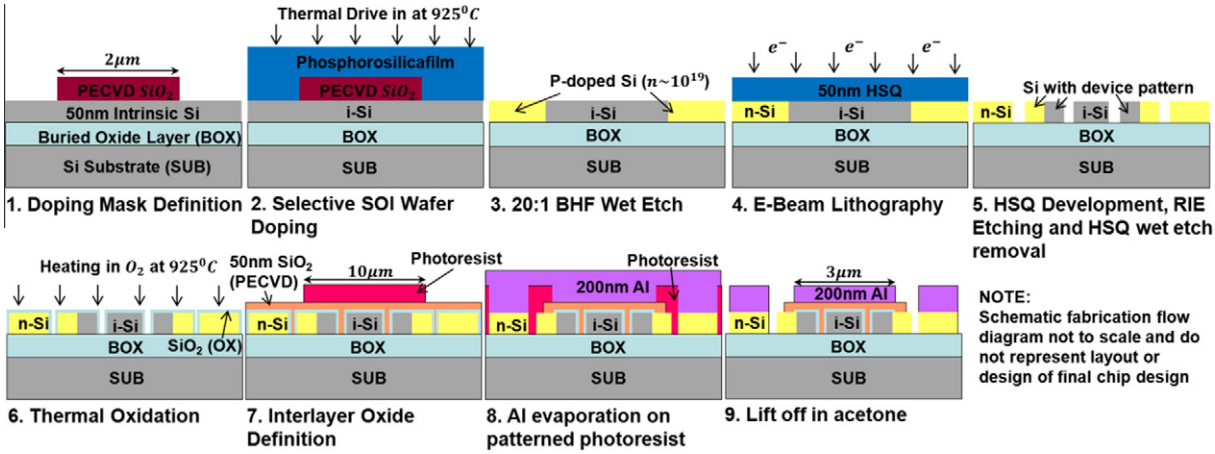

Fig. 2. Schematic VLSI compatible process flow diagram for fabrication of our high density quantum devices.

resulted in uneven nanowire sidewalls, causing unintentionally formed QDs as presented in an earlier work [10]. This is in addition to a more macroscopic effect of back-scattered electrons originating from the exposure of the micron scale contact pads which produced undesired resist cross-linking over the whole nanoscale structure region. As such, extensive dose optimisation was required in the immediate vicinity of the critical features to reduce these proximity effects. E-beam dose ranges of 1100–1250 μC/cm^2 was used to write the nanostructure, whereas the micron-size contact pads were exposed with doses of 550–625 μC/cm^2 to achieve the best repeatability. The exposed HSQ is then developed in 2.45% tetramethylammonium hydroxide for 1 m 40 s, rinsed in deionised water and cured on a hot-plate at 250 °C for 4 m 30 s to become a hard etching mask.

The resist patterns were transferred into the 50 nm Si via RIE with O_2/SF_6 chemistry and an etching selectivity of 1.3:1 to HSQ. The sample is then oxidised at 925 °C to form a ~17 nm SiO_2 layer around the device structure, helping to reduce charge traps, surface imperfections as well as reducing QD dimensions from 60 to ~25 nm. A 50 nm thick PECVD SiO_2 layer is then deposited on top and RIE etched into a 10 μm square window, optically aligned above the nanostructure region. This acts as an interlayer gate oxide, preventing leakage between the nanostructure and a 200 nm Al top gate which is evaporated on top and optically defined along with contact pads via a lift off process.

3.2. Characterisation

Fig. 3a below show an SEM image of a nanostructure patterned into HSQ on a SOI wafer. Fig. 3b shows an SEM image after a pattern is transferred by RIE into the SOI. The use of HSQ for EBL has allowed for high density QDs of smaller dimensions to that previously fabricated [5,10]. More importantly, we found the realised DSET structures to be well defined with over 80% of the

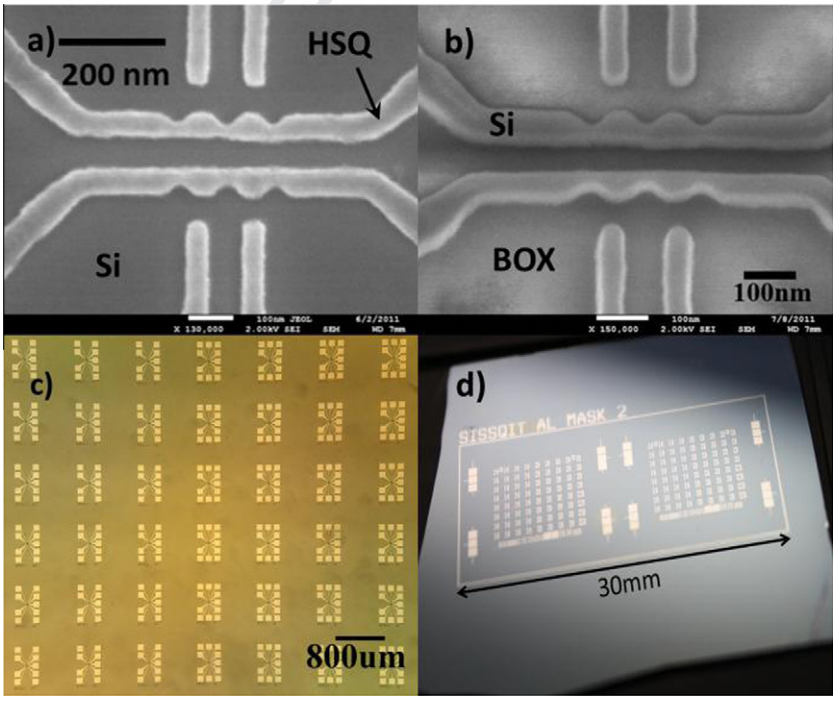

Fig. 3. (a) An SEM image of HSQ patterned with the device nanostructure and (b) the etched structure after transferring into SOI. (c) An optical photo of an array of devices. (d) Chip scale photo of the VLSI compatible fabrication result.

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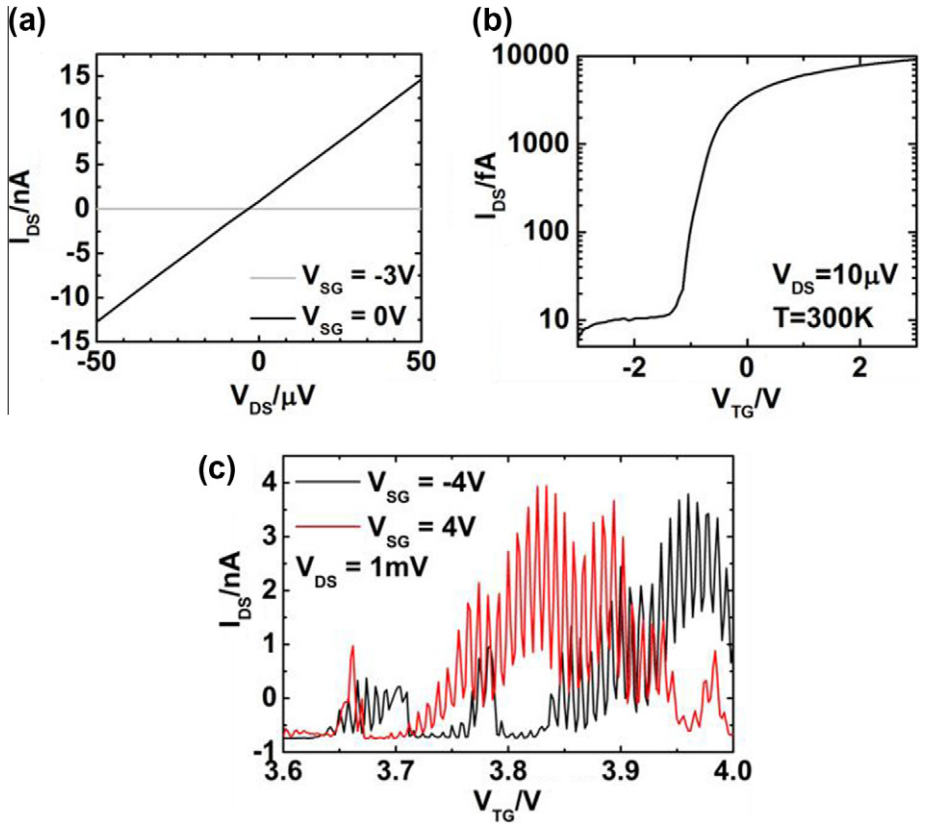

Fig. 4. (a) DSET source to drain current, I_{DS}, as a function of source to drain voltage, V_{DS}, with voltages V_{SG} = 0 V and −3 V applied to side gates. (b) I_{DS}, as a function of top gate voltage, V_{TG}, with all other gates grounded at V_{DS} = 10 μV. (c) The same measurement as b) except at a temperature of 80 mK with V_{SG} = 4 and −4 μV.

QDs in 64 devices fabricated in parallel having dimensional variations of less than ±5 nm compared to the design. Likewise, the etched nanostructures are observed to have clearly defined vertical sidewalls with <1% dimensional deviation from the resist pattern. The average realised QD dimension was 51 nm across 64 devices with a standard deviation of 3.4 nm. To our knowledge, this is the first successful attempt at obtaining such high density and high resolution lithographically defined quantum devices repeatedly on SOI using HSQ.

Fig. 3c and d shows chip scale photos of fabrication results, showing the potential for chip scale fabrication of 144 device in parallel – a key advantage of a VLSI compatible approach. Trials showed that a wide range of designs of similar dimensions can be accurately realised using our VLSI compatible approach.

The source to drain current–voltage characteristics of DSETs in each device at room temperature (Fig. 4a) showed a source to drain resistance of ~50 kΩ. A clear distinction can be seen when a single voltage was applied to all other gates at V_{SG} = −3 V and 0 V (i.e., MOSFET on/off). Preliminary electrical characterisation also showed minimal leakage current through the BOX (Fig. 1b) with an interlayer gate oxide breakdown voltage of >22 V, well above the operating voltage of the top gate.

Fig. 4b shows the electrical measurements of the room temperature DSET source to drain current I_{DS} as a function of the applied top gate voltage V_{TG} at the source to drain voltage, V_{DS} = 10 μV. Characteristic MOSFET behaviour was observed with all other gates grounded. Seven out of nine tested devices showed consistent top gate control over the DSETs' channel conductance. The behaviour is similar to previous work [10] where control of channel conductance has been performed using a Poly-Si top gate. A repeat of this measurement at a temperature of 80 mK with V_{DS} = 1 mV and V_{SG} = −4 and 4 V (Fig. 4c) showed the characteristic coulomb oscillations of SETs. This signifies single electron transfer through the QDs.

4. Conclusions

We have successfully implemented and optimised a VLSI compatible process allowing for the large scale parallel fabrication of up to 144 scalable Silicon based high density quantum dot systems using HSQ resist and electron beam lithography. The implementation of HSQ resist allows for lithographically defined SOI Si QDs of ~50 nm and nanowire channel constrictions of just ~25 nm – smaller dimensions than that in previous work [5,10] and results in the potential for true single electron QD occupation and manipulation. The resultant high density nanostructures are well-defined and within variations of less than ±5 nm from the design for over 80% of the 64 devices fabricated in parallel. The next step is to both further decrease the lithographically defined QD dimensions to just 30–40 nm and to explore the reproducibility of exposures for even higher density QD devices with >4 QDs. This can be achieved through more refined exposure strategies making use of proximity corrections and further optimisation of development procedures.

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