Realization of Al FinFET single electron turnstile co-integrated with a close proximity electrometer SET

Feras M. Alkhalil [a], Julia I Perez-Barraza [b], Muhammad K. Husain [a], Yun P. Lin [a], Nick Lambert [b], Harold M. H. Chong [a], Yoshishige Tsuchiya [a], David A. Williams [c], Andrew J. Ferguson [b] and Hiroshi Mizuta [a,d]

[a] School of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, UK
[b] Microelectronics Group, Cavendish Laboratory, University of Cambridge, Cambridge CB3 0HE, UK
[c] Hitachi Cambridge Laboratory, J. J. Thomson Avenue, Cambridge CB3 0HE, UK
[d] School of Material Science, JAIST, Nomi, Ishikawa 923-1292, Japan
e-mail: fma1g08@ecs.soton.ac.uk

In the past few years, spin qubits in Si quantum dots (QDs) have demonstrated great potential to fulfill the Loss DiVincenzo quantum computing criteria [1]. Although good controllability of single electron spins has been demonstrated for QDs defined on the two-dimensional electron gas (2DEG) formed at the GaAs/AlGaAs heterojunction by using top-down lithography [2], the coherence of electron spins deteriorates rapidly in GaAs due to rich nuclear spins in GaAs. Electron spins confined in silicon based QDs are expected to have longer coherence time thanks to the low nuclear spin density of silicon based materials, with coherence times as long as 6 seconds recently been demonstrated [3]. This has further asserted the advantage of using Si as a platform to realize spin qubits and several Si QD structures have been investigated in silicon on insulator (SOI) [4], [5] and Si (2DEG) [6]. In previous work, we have presented the design and simulation of a novel SOI-based spin qubit platform using Al FinFET gates and Si side gates. The simulations demonstrated the ability of this platform to transfer, confine and detect single electrons [7], [8]. In this letter, we report a novel fabrication process to realize high density silicon based QDs with close proximity Al and Si gates on ultrathin SOI for spin qubit applications.

Figure 1 shows an outline of the fabrication process. This challenging process, requiring precise lithography alignment and fully optimized dry etching and lift-off techniques, is made possible by employing deep etched alignment marks, a liquid source selective doping technique, and six electron beam lithography steps with alignment accuracy close to 15 nm. After the selective doping process (Fig. 1 (a)), two nanowire channels and Si plunger gates are patterned on the 30-nm-thick SOI (Fig. 1 (b)). Thermal oxidation (Fig. 1 (c)) is followed by the formation of the Al FinFET layer (Fig. 1 (d)) with our precision alignment technique. Finally the Al top gate is defined on the PECVD deposited gate oxide layer ((Fig. 1 (e) and (f)). This fabrication approach of using both Al and Si gates to form the QDs and to control their potential is compatible with conventional MOS technologies, shows good reproducibility and offers great flexibility to integrate more complex structures.

Figure 2 shows an SEM image of a fabricated device taken before the top gate oxide deposition. The QDs are defined by the FinFET gates separation (100 nm) and the SOI channel width (50 nm); the Al FinFET gates (gate width of 35 nm) surround the SOI nanowire channels to form electrically tunable potential barriers. The separation between the Si plunger gates and the QDs is 25 nm providing precise control of the QDs potential. The structure also has an Al top gate that covers the QDs region (not shown in Fig. 2) and is used to form a carrier inversion layer in the intrinsic SOI channel. The two identical formed QDs are 50 nm apart (QDs separation as small as 30nm is also being investigated); one is used as a single electron turnstile and the other as an electrometer.

Figure 3 shows coulomb oscillation characteristic for the source drain current (I_{SD}) of the top QD structure as a function of the voltages applied to the Al barrier gates and the Si plunger gate at a source-drain (V_{SD}) voltage of 1 mV and a top gate voltage (V_{TG}) of 2 V at 4 K. Low temperature measurements demonstrated the effectiveness of the top gate in forming the carrier inversion layer in the intrinsic SOI and the effect of the Al FinFET gates and the Si plunger gates proving that these gates are able to form the designed QDs and to control their potential. The bottom QD structure has also successfully demonstrated coulomb oscillation characteristics similar to the top structure characteristics shown in Fig. 3.

[1] D. Loss and D. DiVincenzo, Physical Review A, vol. 57, no. 1, pp. 120-126, Jan. 1998.
[2] J. R. Petta et al., Science (New York, N.Y.), vol. 309, no. 5744, pp. 2180-4, Sep. 2005.
[3] A. Morello et al., Nature, vol. 467, no. 7316, pp. 687-91, Oct. 2010.
[4] H. Liu, T. Fujisawa, H. Inokawa, Y. Ono, A. Fujiwara, and Y. Hirayama, Applied Physics Letters, vol. 92, no. 22, p. 222104, 2008.
[5] T. Kodera et al., Physics of semiconductors, ICPS-30 conference proceedings, pp. 331-332, 2011.
[6] W. H. Lim et al., Applied Physics Letters, vol. 95, no. 24, p. 242102, 2009.
[7] F. M. Alkhalil et al., ESSDERC/ESSCIRC Fringe, 2010.
[8] F. M. Alkhalil et al., Quantum Information Processing and Communication at ETH Zurich, 2011.

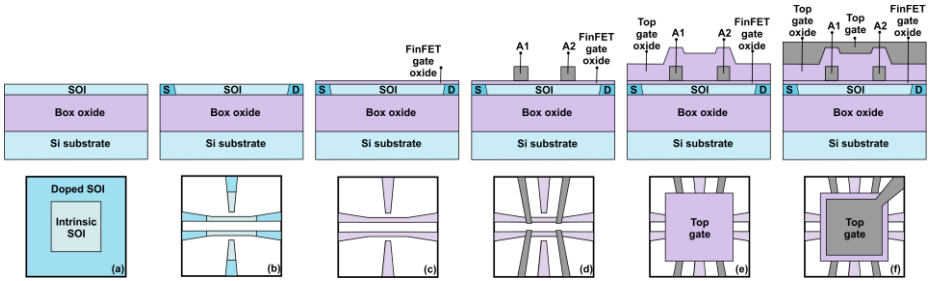

Figure 1. Schematic cross section and top view of the fabrication process, (a) selective liquid source doping, (b) definition of the SOI device layer, (c) thermal oxidation, (d) realization of the Al FinFET layer, (e) deposition of top gate oxide, and (f) top gate definition.

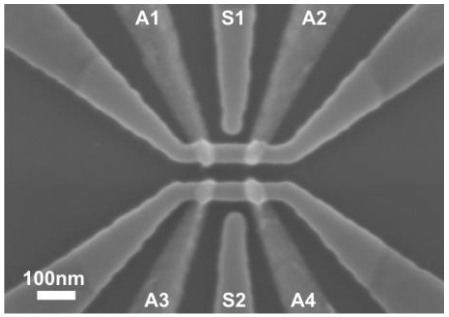

Figure 2. SEM image of the Al FinFET platform, the Al gates are 35 nm wide with a spacing of 100 nm, the Si plunger gates are 60 nm wide and 25 nm away from the SOI channel.

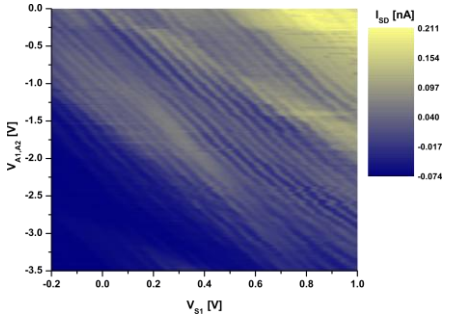

Figure 3. I_{SD} of the top QD transistor as a function of the Al barrier gates potential (V_{A1}, V_{A2}) and Si plunger gate potential (V_{S1}) with V_{SD} of 1 mV and V_{TG} of 2 V at 4 K with all other gates grounded.