Al FinFET single electron devices with close proximity Si plunger gates

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In the past few years, spin qubits in Si quantum dots (QDs) have demonstrated great potential to fulfill the Loss DiVincenzo quantum computing criteria. Although good controllability of single electron spins has been demonstrated for QDs defined on the two-dimensional electron gas (2DEG) formed at the GaAs/AlGaAs heterojunction by using top-down lithography [1], the coherence of electron spins deteriorates rapidly in GaAs due to rich nuclear spins in GaAs. Electron spins confined in silicon based QDs are expected to have longer coherence time thanks to the low nuclear spin density of silicon based materials, with coherence times as long as 6 seconds recently been demonstrated [2]. This has further asserted the advantage of using Si as a platform to realize spin qubits and several Si QD structures have been investigated in silicon on insulator (SOI) [3], [4] and Si (2DEG) [5]. In this letter, we report a novel fabrication process to realize high density silicon based QDs with close proximity Al and Si gates on ultrathin SOI for spin qubit applications.

The challenging process adopted here, requiring precise lithography alignment and fully optimized dry etching and lift-off techniques, is made possible by employing deep etched alignment marks, a liquid source selective doping technique, and six electron beam lithography steps with alignment accuracy close to 15 nm. Figure 1 shows SEM images of the fabricated devices. The QDs are defined by the Al FinFET gates separation (80 nm) and the SOI channel width (50 nm); the Al FinFET gates (gate width of 35 nm) surround the SOI nanowire channels to form electrically tunable potential barriers. The separation between the Si plunger gates and the QDs is 25 nm providing precise control of the QDs potential. The structure also has an Al top gate that covers the QDs region (not shown in Fig. 1) and is used to form a carrier inversion layer in the intrinsic SOI channel. The two identical QD transistors are 50 nm apart (separation as small as 30nm is also being investigated); one is used as a single electron turnstile and the other as an electrometer.

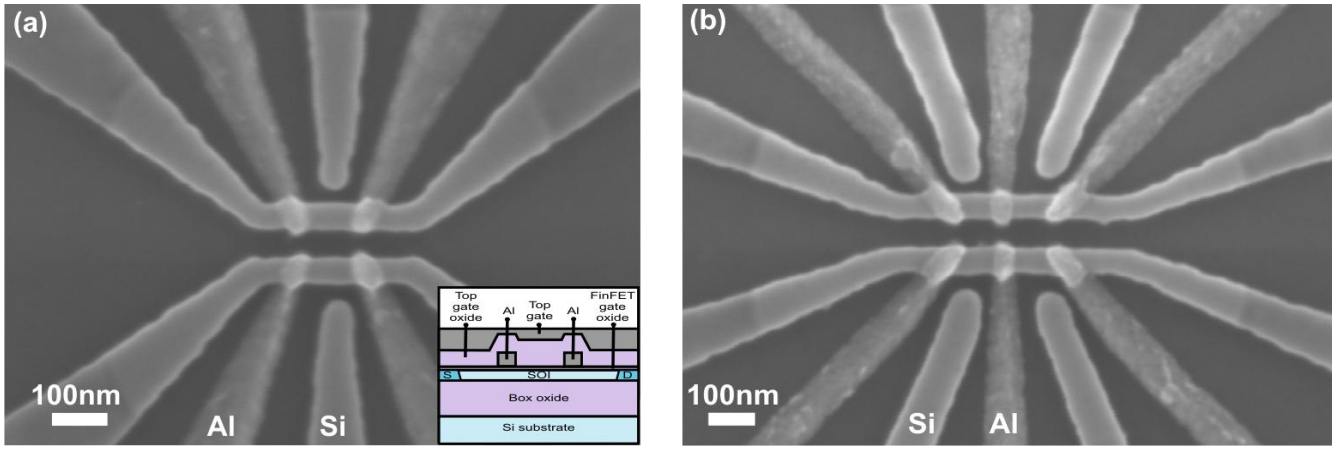

Fig. 1: SEM images of the Al FinFET turnstile and electrometer, (a) single QD turnstile and electrometer, inset figure shows a cross section schematic of the structure, (b) double QDs turnstile and electrometer.

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