University of Southampton
Electronics and Computer Science
Communications, Signal Processing and Control Research Group

Fault Tolerant Stochastic LDPC Decoders in Voltage Scaling Scenarios

Isaac Perez-Andrade, Xin Zuo, Robert G. Maunder,
Bashir M. Al-Hashimi and Lajos Hanzo

Presented by Robert G. Maunder
Email: {ip1g10,xz3g08,rm,bmah,lh}@ecs.soton.ac.uk

Shanghai, China
April - 2012

Outline

- Motivation
- Stochastic LDPC decoder
- Timing error analysis
- Error correction capability
- Modified stochastic LDPC decoder
- Performance comparison
- Processing energy consumption
- Conclusion

Motivation

- Low Density Parity Check (LDPC) codes can correct transmission errors.
- LDPC codes allow low transmission energies and/or high transmission throughputs.
- But, overall energy consumption may be limited by LDPC decoder energy consumption and overall throughput may be limited by processing throughput.
- Voltage and clock scaling techniques can be employed for reducing processing energy consumption and increasing processing throughput.
- These techniques might induce timing errors, but LDPC codes have an inherent error correction capability.
- In fixed-point LDPC decoders, timing errors affecting the most significant bit are catastrophic.
- In stochastic LDPC decoders, all bits have equal significance.
  $0.3 \rightarrow \ldots 00100100010 \ldots$

Stochastic LDPC decoder

- LDPC codes have two types of nodes: Check Nodes (CNs) and Variable Nodes (VNs).

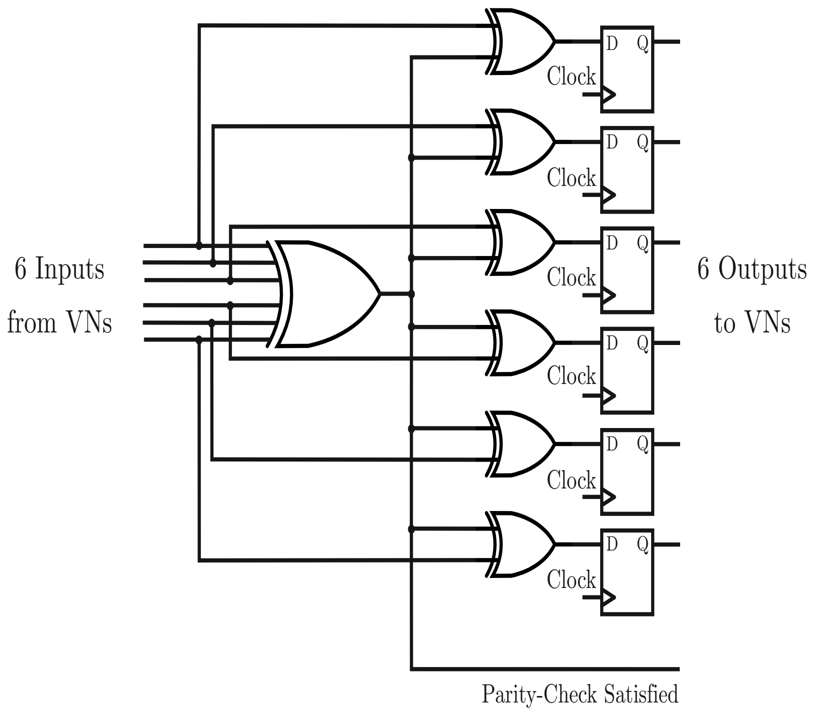

Figure 1: Stochastic CN degree 6.

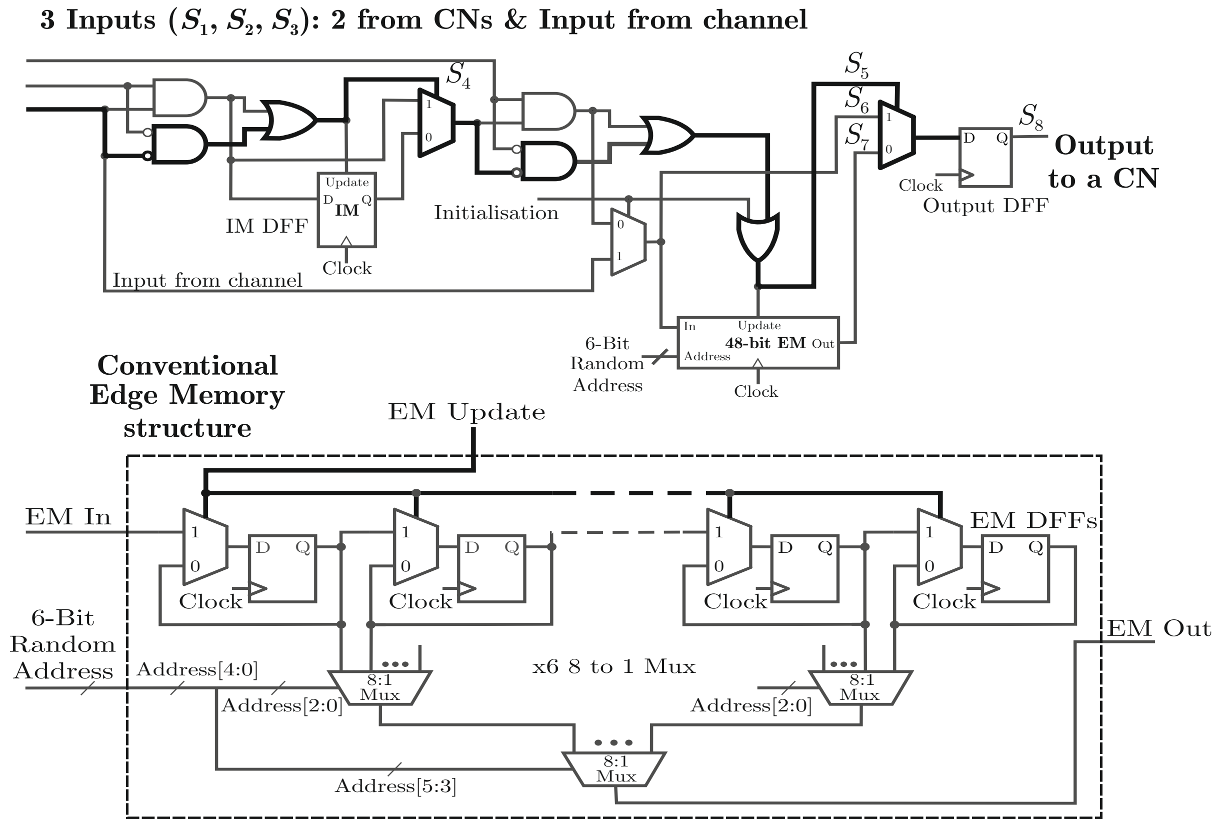

Figure 2: Stochastic VN degree 3.

Timing error analysis

- Timing errors occur when $t_p > T_{\mathrm{clk}}$
  - t_p is the propagation delay of the signal path p
  - T_{clk} is the clock period.
- Cause of timing errors:
  - Excessive propagation delays owing to noise reducing the supply voltage.
- Effect of timing errors:
  - Erroneous values are clocked into memories and/or output flip flops in VNs.

- Propagation delay t_p in different critical paths as a function of the supply voltage.

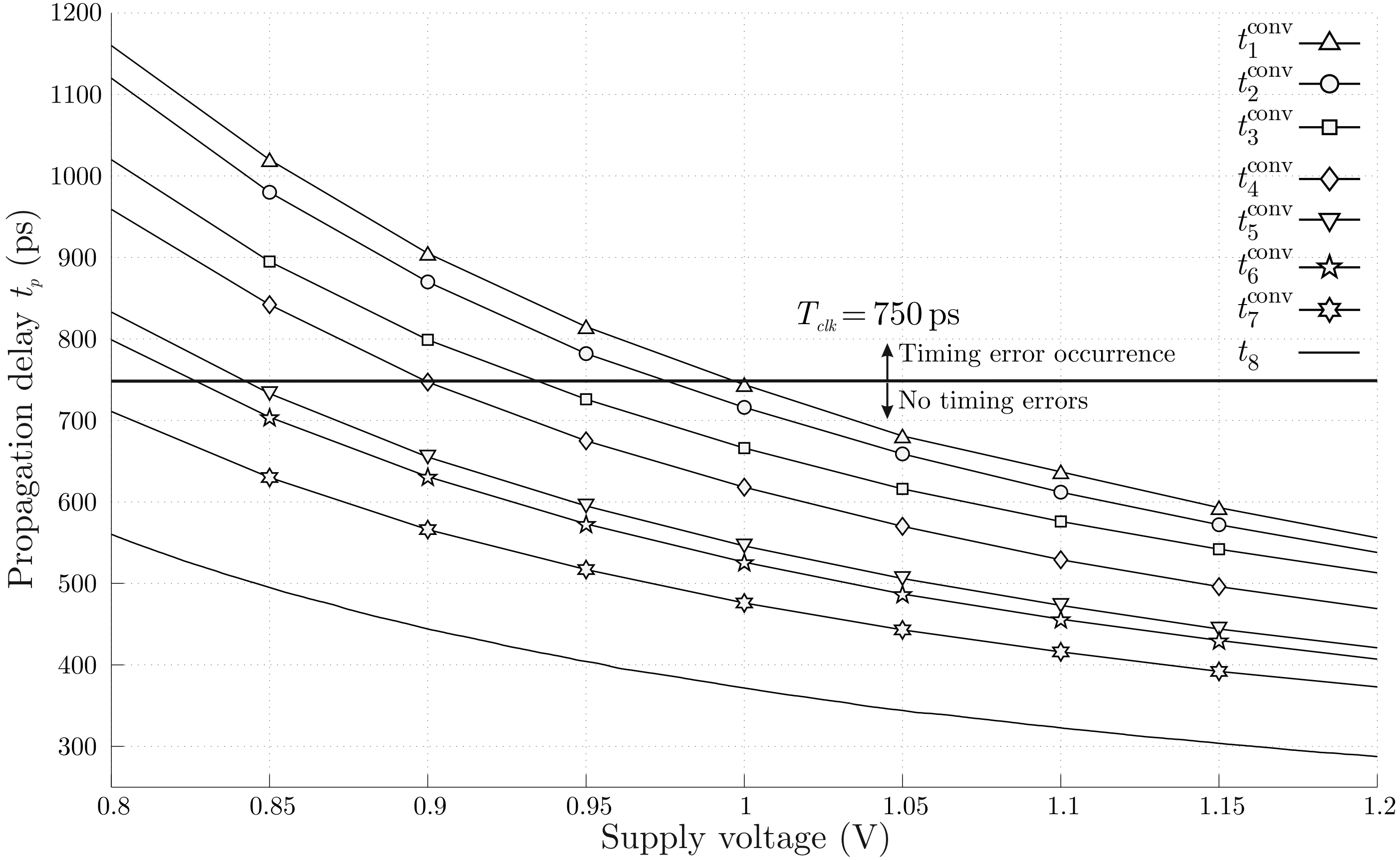

Figure 3: Propagation delays for stochastic LDPC decoders obtained using STMicroelectronics 90 nm technology.

Error correction capability

- (1056,528) WiMAX LDPC decoder, BPSK modulation over AWGN channel.

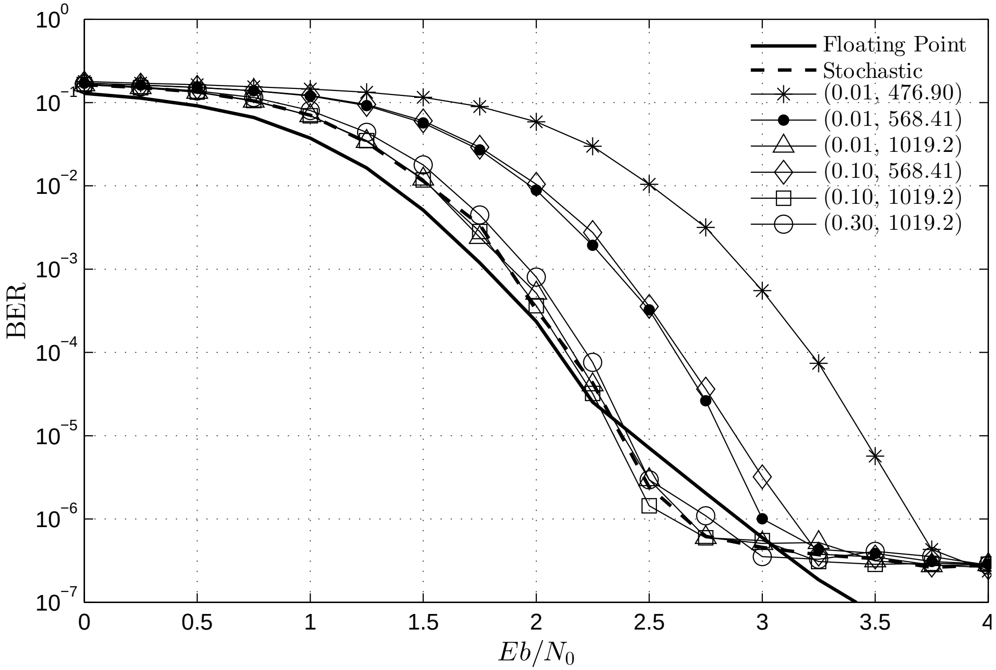

Figure 4: BER with $\mu = 1.0$ V

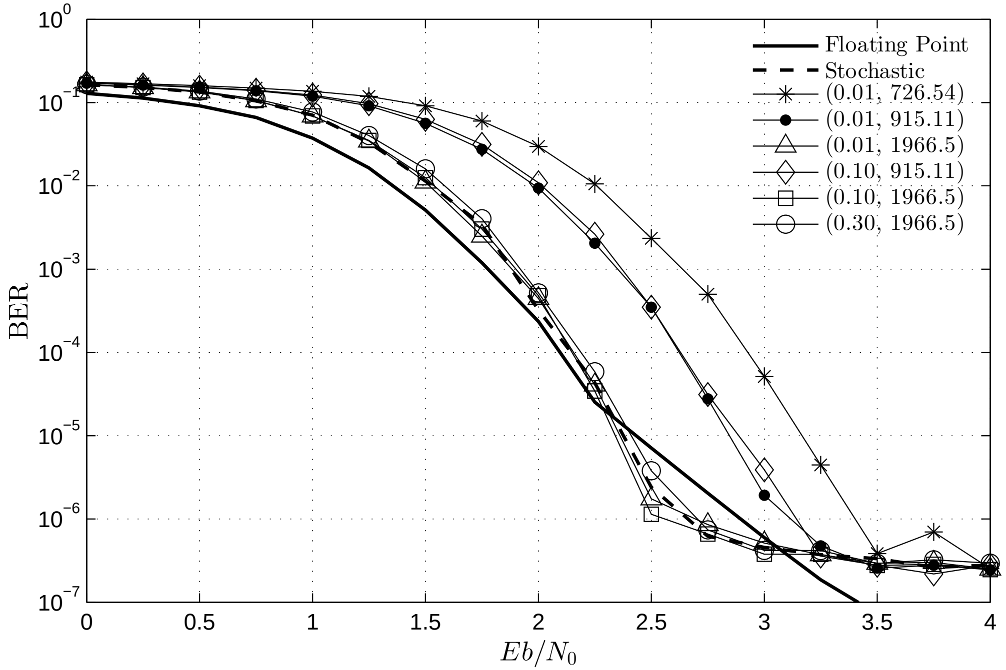

Figure 5: BER with $\mu = 0.8$ V

Modified stochastic LDPC decoder.

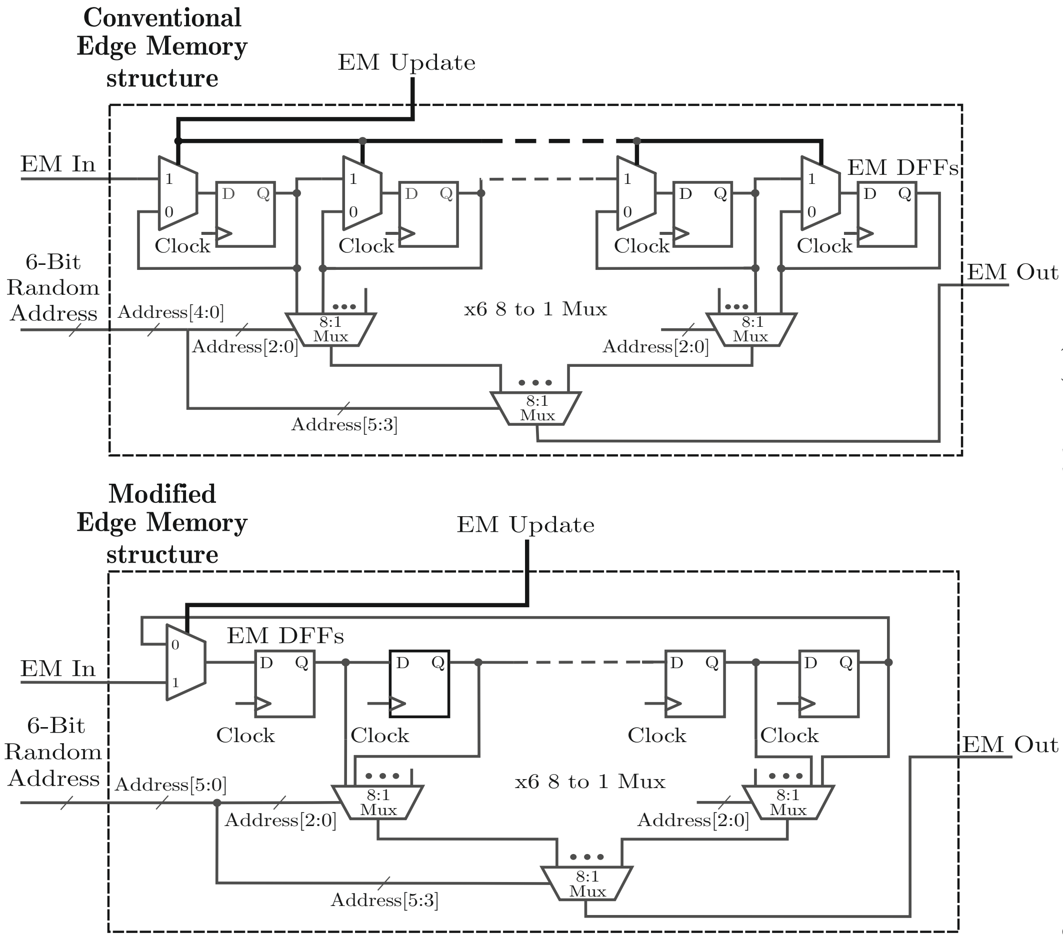

Figure 6: Conventional and Modified EM structures.

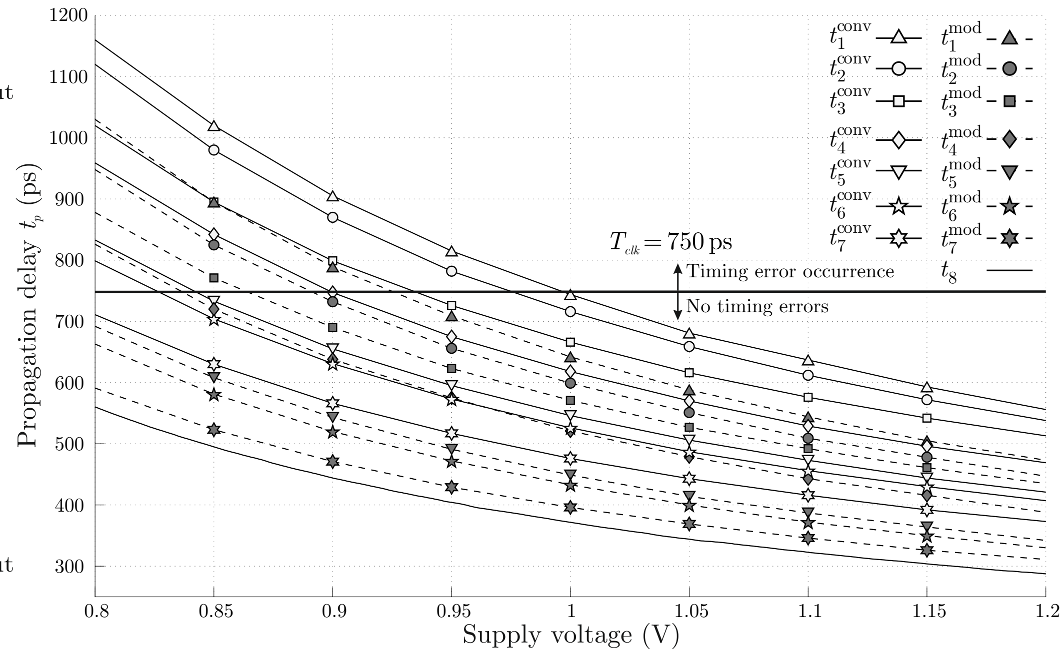

Figure 7: Propagation delays in modified stochastic LDPC decoders.

Error correction capability of the modified stochastic LDPC decoder.

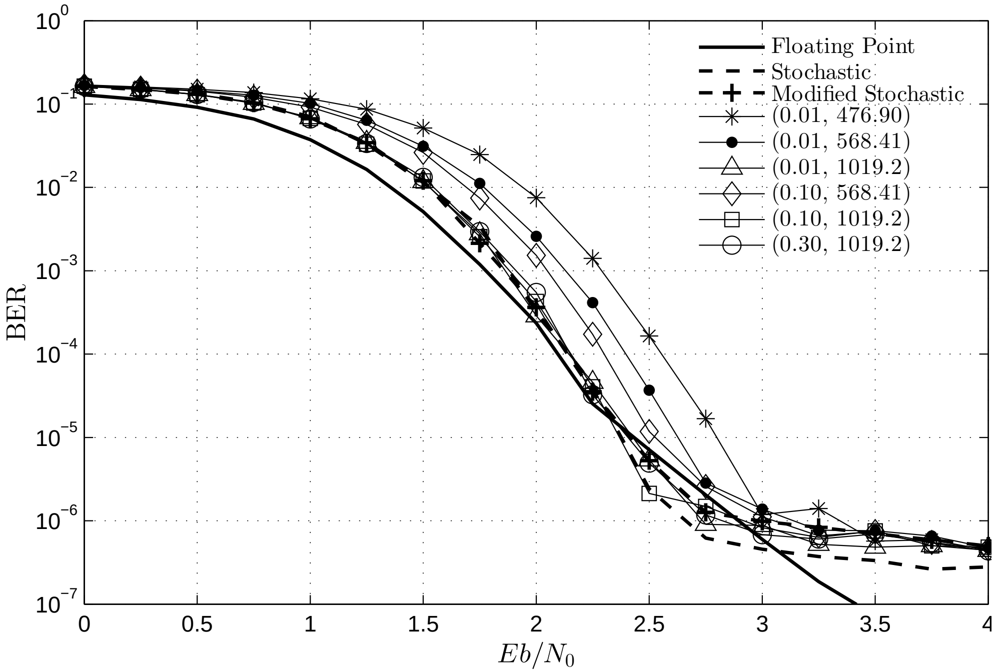

Figure 8: BER with $\mu = 1.0$ V

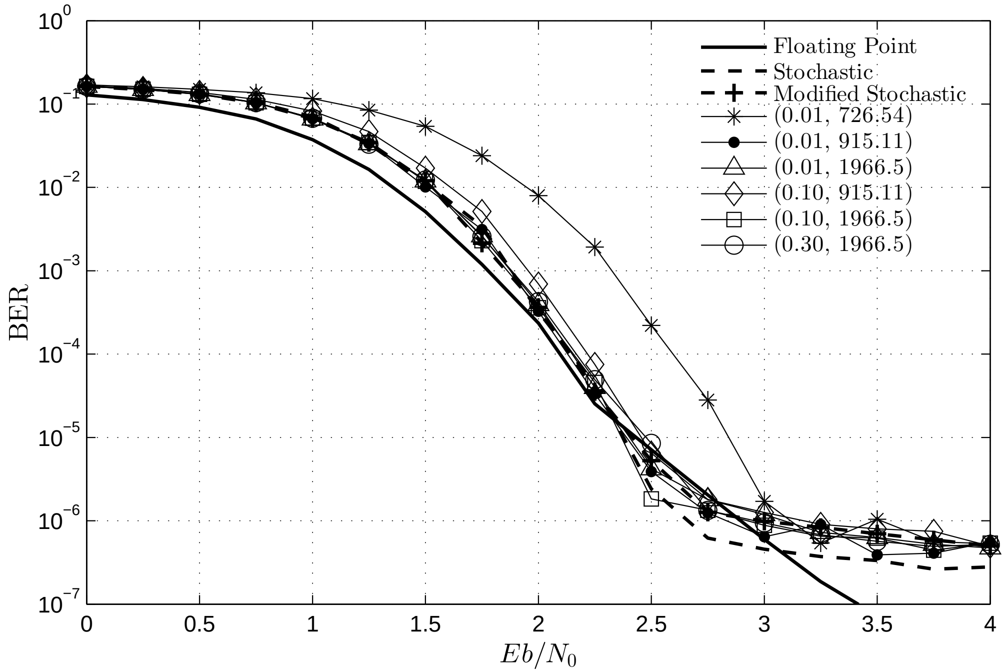

Figure 9: BER with $\mu = 0.8$ V

Performance comparison

- Similar error correction capabilities in the modified design at (V_{DD}, T_{clk})=(0.8 V, 915.11 ps) and the conventional decoder at (V_{DD}, T_{clk})=(1.0 V, 1019.2 ps).

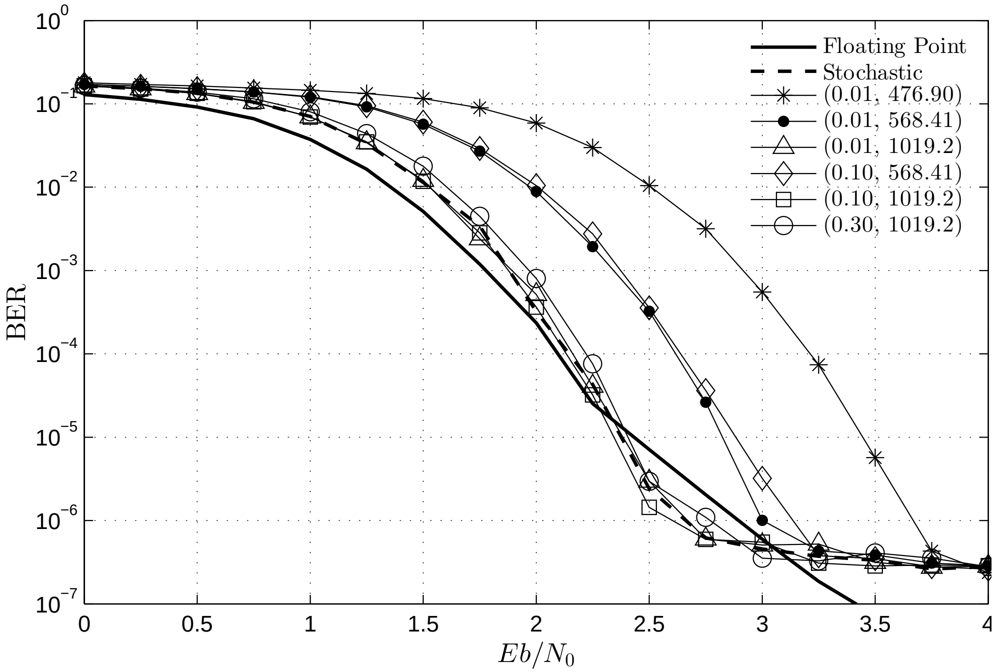

Figure 10: Nominal with $\mu = 1.0$ V

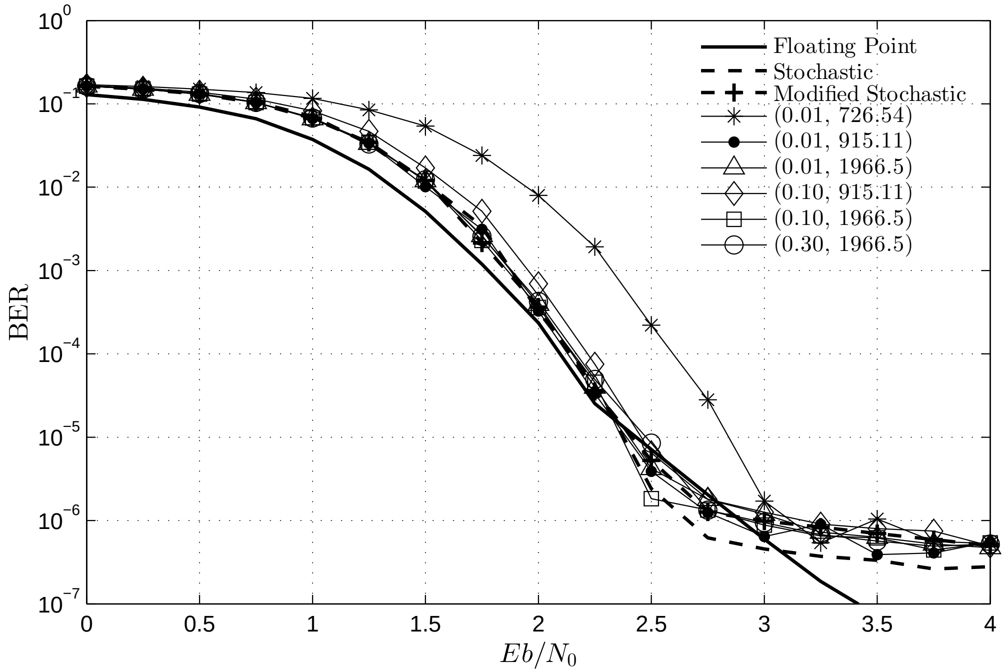

Figure 11: Modified with $\mu = 0.8$ V

Processing Energy Consumption

Table 1: Average energy consumption per decoding iteration with $\mu = 1.0$ V

	$T_{\text{clk}} = 476.90$ ps	$T_{\text{clk}} = 568.41$ ps	$T_{\text{clk}} = 1019.20$ ps
TOTAL$^{\text{conv}}$	3.93 nJ	3.69 nJ	**3.90 nJ**
TOTAL$^{\text{mod}}$	3.99 nJ	4.03 nJ	4.02 nJ

Table 2: Average energy consumption per decoding iteration with $\mu = 0.8$ V.

	$T_{\text{clk}} = 726.54$ ps	$T_{\text{clk}} = 915.11$ ps	$T_{\text{clk}} = 1966.5$ ps
TOTAL$^{\text{conv}}$	2.46 nJ	2.29 nJ	2.45 nJ
TOTAL$^{\text{mod}}$	2.48 nJ	**2.47 nJ**	2.50 nJ

Conclusions

- Voltage- and clock-scaled modified LDPC decoder presents a similar decoding performance of that of the conventional decoder at nominal operation conditions.
- This is translated into:
  - 20% reduction in supply voltage
  - 10.2% reduction in the clock period
  - 36.7% reduction in processing energy consumption
- Stochastic LDPC decoders have an inherent tolerance to correct not only transmission errors but also timing errors, when employing voltage and clock scaling.

Thank you !

LDPC decoder

- LDPC codes can be represented with factor graphs composed of VNs and CNs.

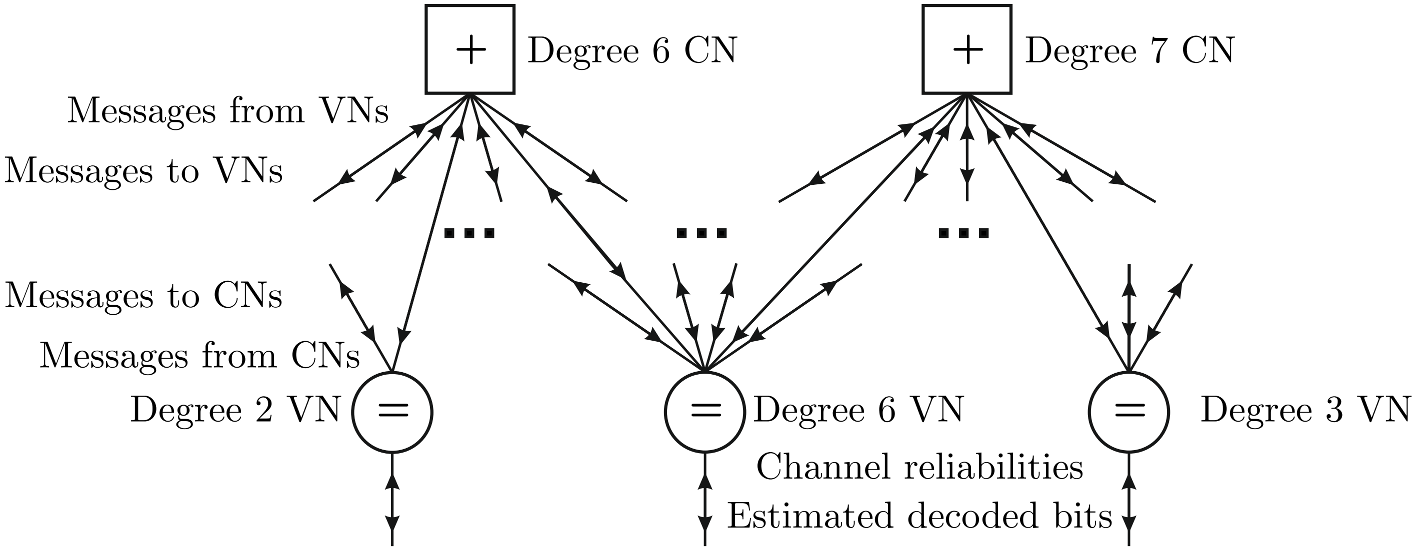

Figure 12: Fraction of a factor graph.

- Type I timing error.
  - Occurs when EM MUX selector signal has a constant value of 0.
  - Previous output value of EM Output signal is erroneously clocked into the output flip flop.
- Type II timing error.
  - Occurs when EM MUX selector signal toggles and arrive late, but EM Output signal arrives on time.
  - Wrong signal is clocked into Output flip flop.
- Type III timing error.
  - Occurs when both EM MUX selector signal and EM Output signal arrive late and EM MUX has been toggled.
  - Previous values of signals are clocked into Output flip flop.

- Occurrence of timing errors when voltage scaling is applied.

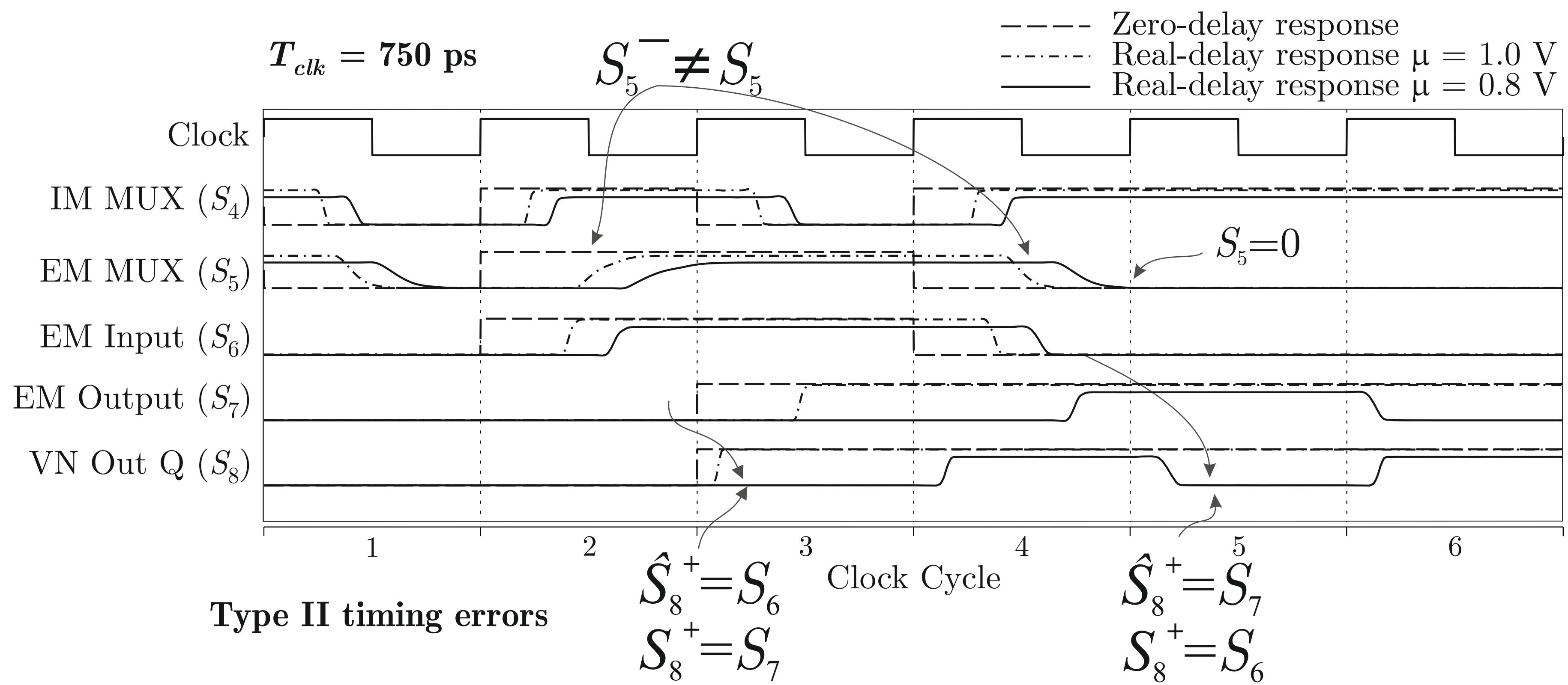

Figure 13: SPICE simulation demonstrating the occurrence of timing errors Type II in the conventional stochastic VN having a degree 3.

Table 3: Combinations of MUX selector signal values corresponding to each path p that is considered for timing analysis.

Path p	Node	Degree d	Affected D-type Flip Flops (DFFs)	MUX selector signal	
				Edge Memory (EM)	Internal Memory (IM)
1	VN	6	Output and EM	constant value $(0 \rightarrow 0)$	any
2		3	Output and EM	constant value $(0 \rightarrow 0)$	any
3		6	Output and EM	toggle value (any)	toggle at least one value (any)
4		2	Output and EM	constant value $(0 \rightarrow 0)$	N/A
5		6	Output and EM	toggle value (any)	constant values (at least one is $1 \rightarrow 1$)
6		6	Output and EM	toggle value $(0 \rightarrow 1)$	constant values (both are $0 \rightarrow 0$)
7		3	Output and EM	toggle value $(0 \rightarrow 1)$	toggle value (any)
8	CN	7	Output	N/A	N/A