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Electronics and Computer Science

Plasma enhanced chemical vapor deposition of nanocrystalline graphene and device fabrication development

by

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Supervisor: Dr. Harold M.H. Chong

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ABSTRACT

FACULTY OF PHYSICAL AND APPLIED SCIENCES
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Doctor of Philosophy

PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION OF NANOCRYSTALLINE GRAPHENE AND DEVICE FABRICATION DEVELOPMENT

by Marek Edward Schmidt

Large area growth of high quality graphene remains a challenge, and is currently dominated by chemical vapor deposition (CVD) on metal catalyst films. This method requires a transfer of the graphene onto an insulating substrate for electronic applications, and the graphene film quality and performance can vary with the transfer. A more attractive approach is plasma enhanced chemical vapor deposition (PECVD) of graphene and nanocrystalline graphene (NCG) directly on insulating substrates. The aim of this project was to explore the deposition process and microfabrication processes based on these NCG films.

A deposition process for nanocrystalline graphene was developed in this work based on parallel-plate PECVD. NCG with thicknesses between 3 and 35 nm were deposited directly on wet thermal oxidized silicon wafers with diameter of 150 mm, quartz glass and sapphire glass. High NCG thickness uniformities of 87% over full wafer were achieved. Surface roughness was measured by atomic force microscopy and shows root mean square (RMS) values of less than 0.23 nm for 3 nm thin films. NCG films deposited on quartz and sapphire show promising performance as transparent conductor with 13 k$\Omega/\square$ sheet resistance at 85% transparency.

Furthermore, the suitability of the developed PECVD NCG films for microfabrication was demonstrated. Microfabrication process development was focused on four device types. NCG membranes were fabricated based on through-wafer inductively coupled plasma etching from the back, and consecutive membrane release by HF vapor etching. The fabrication of suspended NCG strips, based on HF vapor release, shows promising results, but was not entirely successful due to insufficient thickness of the sacrificial oxide. Top gated NCG strips are successfully fabricated, and the increased modulation by the top gate is demonstrated. Finally, NCG nanowire fabrication is performed on 150 mm wafers. Experiments yielded an increased back gate modulation effect by a reduced NCG thickness, although no nanowire formation was observed.

A highly accurate focused ion beam (FIB) prototyping technique was developed and applied to exfoliated graphene in this work. This technique systematically avoids any exposure of the graphene to Ga^+-ions through the use of an alignment marker system, achieving alignment accuracies better than 250 nm. Contacts were deposited by FIB- or e-beam-assisted tungsten deposition, and FIB trench milling was used to confine conduction to a narrow channel. A channel passivation method based on e-beam-assisted insulator deposition has been demonstrated, and showed a reduction of ion damage to the graphene. Three fabricated transistor structures were electrically characterized.

To my wife, Akiko

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Declaration of Authorship

I, Marek Edward Schmidt , declare that the thesis entitled *Plasma enhanced chemical vapor deposition of nanocrystalline graphene and device fabrication development* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as: Journal [1] and presented at international conferences [2, 3]

Signed:.....

Date:.....

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Note: This version of the thesis contains several corrections and clarifications which are not present in the examined version. Please refer to page 167 for a list of differences.

Marek E. Schmidt, January 2013

Nomenclature

Symbol	Description
α	Optical absorption or fine structure constant
A	Area
$\mathbf{a}_1$, $\mathbf{a}_2$, $\mathbf{a}_3$	Primitive vectors
$\mathbf{b}_1$, $\mathbf{b}_2$, $\mathbf{b}_3$	Reciprocal primitive vectors
C_0, C_1	Scaling constants for calculation of $C(\lambda)$
$C(\lambda)$	Variable scaling coefficient
d_{NCG}	NCG thickness
d_{NCG}^{150}, d_{NCG}^{100}	Mean NCG thickness for 150 and 100 mm size
D_0	Reference dose
D_{line}	Line dose
D	Total electron dose
ϵ	Deposition per dose
E	Energy
E	Young's modulus
E_{F}	Fermi energy
e	Elementary electron charge
F	Gas flow rate (in sccm)
γ	Nearest neighbor hopping energy
h, $\hbar$	Planck constant, reduced
I_{2D}, $I(\mathrm{2D})$	Raman intensity of 2D peak
I_{D}, $I(\mathrm{D})$	Raman intensity of D peak
I_{D}	Drain current
I_{G}, $I(\mathrm{G})$	Raman intensity of G peak
I_{I}	Incident intensity
I_{Rfilm}	Reflected intensity of thin film
I_{Rsample}	Reflected intensity of sample
I_{Tfilm}	Transmitted intensity of thin film
I_{Tsample}	Transmitted intensity of sample
K, K′	Points in first *Brillouin zone*
k	Thermal conductivity
k	Wave vector
λ	Wavelength

ℓ	Length
L_a	Cluster diameter
LU, LV	*ELPHY Quantum* linear mode in U and V direction
M	Channel modulation
M	Point in first *Brillouin zone*
MA	*ELPHY Quantum* meander mode, automatic direction selection
M_BG, M_TG	Channel modulation for back gate (top gate)
$\mathrm{M_C}$	Molar mass of carbon
μ	Charge carrier mobility
NU	Non-uniformity
NU^{150}, NU^{150}	Non-uniformity for 150 and 100 mm size
NU_DG, NU_2DG	Non-uniformity of Raman $I(\mathrm{D})/I(\mathrm{G})$ and $I(\mathrm{2D})/I(\mathrm{G})$ ratio
μ	Carrier mobility
n	Electron or hole concentration
n	Number of atoms in primitive cell
n_A	Number of atoms in primitive unit cell
n_S	Number of faces of graphene sheet
R	Reflectance
$R_\square$	Sheet resistance
R_max, R_min	Maximum and minimum resistance
R_mean	Mean resistance
σ_xy	Hall conductivity
σ_max	Ultimate tensile strength
t_clean	Cleaning time
t_cool	Cooling time
t_dep	Deposition time
t_dwell	Dwell time
t_etch	Etch duration
t_heat	Heating time
ΔT	Temperature difference
T	Transmittance
T_dep	Deposition temperature
T_load	Loading temperature
U, V	Internal coordinates of *ELPHY Quantum*
U', V'	Internal coordinates of *ELPHY Quantum* used for mark milling
V_D	Drain voltage
V_G	Gate voltage
V_BG	Back gate voltage
V_TG	Top gate voltage
w	Width

Chapter 1

Introduction

Graphene, a one-atom thin carbon crystal, is an extraordinary material in many regards. It is a zero bandgap semiconductor with linear energy dispersion relation near the Dirac points, where conduction and valence band touch. Carriers are thus described as massless Dirac fermions, traveling at near relativistic speed. This provides a very high carrier mobility that is regarded as a possibility for improved transistor speed and reduced power consumption, and makes graphene a contestant as a possible successor of silicon in the post-Moore era. The bandgap changes when multiple graphene layers are stacked, and is further tunable by an applied electric field perpendicular to the graphene film. The mechanical strength of graphene is several times higher than the one of silicon or iron. The importance of graphene was honored very recently by the Nobel Prize committee. The Nobel Prize in Physics 2010 has been awarded to Prof. Andre Geim and Prof. Konstantin Novoselov, the researchers who were first to discover and isolate a monolayer of graphene [4].

The most common methods used for obtaining graphene for planar applications are mechanical exfoliation from highly oriented pyrolytic graphite (HOPG) [4], epitaxial growth on silicon carbide [5], and chemical vapor deposition (CVD) on transition metals [6, 7]. So far, exfoliated graphene offers the largest mono-crystalline and defect free domains. However, the random shape, size and location of exfoliated graphene, and the fact that it does not currently scale beyond 1 mm, makes it unsuitable for large area device fabrication. Graphene grown by epitaxy on SiC, on the other hand, offers high crystal quality over large areas, however, the recent progress is suffering from the inherent surface steps that form during growth, and the high cost of SiC substrates. The CVD deposition of graphene on metal substrates at high temperatures requires a consecutive transfer step onto an insulating surface for electronic device applications. This transfer process is constantly improved and has been demonstrated for areas of 30 inch in diameter [8]. Nevertheless, electric properties of such transferred films are worse than those of exfoliated graphene, partially due to the transfer step introducing defects.

None of these methods is currently good enough to allow wide commercial application of graphene. It is therefore necessary to develop deposition techniques that are able to

yield large area graphene directly on insulating substrates [9]. Plasma-enhanced chemical vapor deposition (PECVD), a method that has not yet seen a lot of attention in respect of graphene research, is identified as ideally suited for this task. The parallel plate PECVD system *Nanofab 1000 Agile*, which is configured for carbon nanotube (CNT) growth based on CH_4, is used for nanocrystalline graphene (NCG) deposition in collaboration with *Oxford Instruments*. The novel, large area PECVD deposition method of NCG developed in this work is, in contrast to CNT growth on metal nanoparticles, performed directly on SiO_2 thin films, quartz glass and sapphire.

A technique for rapid prototyping of electronic devices on exfoliated graphene by focused ion beam (FIB) and scanning electron microscopy (SEM) lithography was developed in this work, as well. As mentioned earlier, randomly distributed flakes with various numbers of layers and individual size are obtained in the process of mechanical exfoliation from HOPG. Therefore, rapid prototyping methods are employed for patterning and contacting such flakes. Direct electron beam lithography with a consecutive metal lift-off is already widely used [10], but it is resist based (a known contaminant) and requires samples with elaborate alignment structures. Graphene device fabrication using focused helium ion beam technology has also been investigated [11–13]. In this work, the third available rapid prototyping method was investigated: Focused gallium ion beam. The dual integration of the FIB with a high resolution SEM allows damage-free in-situ SEM examination of the graphene and individual milling or deposition of various materials through the use of a gas injection system (GIS). FIB technology is tested and well established, and benefits from a wide availability. The FIB/SEM prototyping technique developed in this work relies on alignment marks to strictly avoid any detrimental exposure of the graphene to ions, while achieving very high accuracy. Furthermore, a fabrication path towards structures which are entirely fabricated within the FIB/SEM microscope is proposed.

Structure of thesis

In the following Chapter 2 of this thesis, literature concerning graphene is reviewed. This includes methods used to obtain graphene, graphene applications and device fabrication based on graphene. Also, focused ion beam technology and its application to graphene is reviewed. The large area, metal-free PECVD deposition of NCG directly on silicon dioxide is explained in Chapter 3. NCG is deposited on 150 mm wafers and different aspects of these films are investigated. The performance of the developed films for transparent conductor applications is discussed as well. Extensive device fabrication process development based on the obtained NCG is then carried outs in Chapter 4. The compatibility of the developed NCG with planar microfabrication is demonstrated by the fabrication of membrane devices, suspended beams, top gated structures and nanowires. Electrical characterization of several devices is reported. In Chapter 5, the highly-accurate FIB prototyping technique is introduced, and the electrical characterization of three transistors is discussed. Finally, the thesis is concluded in Chapter 6 and suggestions for future work are provided.

Chapter 2

Literature review

Graphene is a one-atom thin carbon layer with a hexagonal honeycomb crystal structure. It is the building block of graphite, which is a stack of numerous graphene sheets. Furthermore, it can be used to construct carbon nanotubes (CNT) or fullerenes. This relation is illustrated in Figure 2.1. The carbon atoms in graphene are sp^2 hybridized, meaning that they have three in-plane σ bonds to neighbor atoms, and one free π orbital perpendicular to the sheet. The distance of each carbon atom to its three in-plane neighbors is 0.142 nm.

This Chapter is a review of the different aspects of this extraordinary material. Starting with the band structure and the electronic properties in Section 2.1, several other properties will be discussed in Section 2.2, such as mechanical strength, thermal conductivity, surface-to-mass ratio and optical properties. In Section 2.3, procedures used

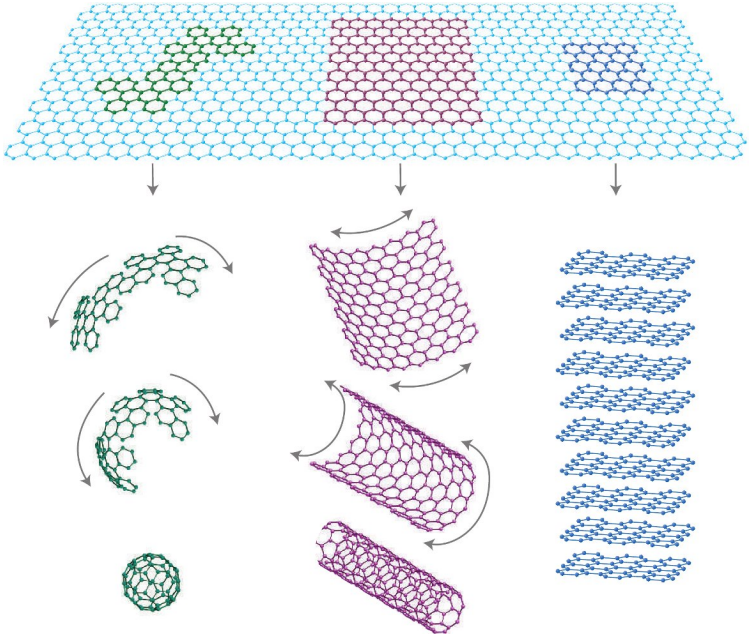


Figure 2.1: Relationship between graphene (top) and fullerene (left), CNT (middle) and graphite (right), respectively. Reproduced from [14].

to detect and characterize graphene will be discussed, which includes the optical contrast method and Raman spectroscopy. The scattering effects giving rise to the different Raman peaks are reviewed, as well. The various methods used to obtain graphene will then be discussed and compared in Section 2.4, with a focus on the question whether the obtained graphene is suitable for large area device fabrication. In Section 2.5 and Section 2.6, graphene applications and graphene related device fabrication processes, respectively, will be discussed. An introduction into focused ion beam (FIB) technology and its application to graphene device prototyping will then be discussed in Section 2.7. Finally, the Chapter will be summarized in Section 2.8.

2.1 Band structure and electronic properties of graphene

Many of the electronic phenomena of graphene, such as the room-temperature electron mobility of $100\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [15] (theoretical limit $\sim 200\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [16]) and the quantum Hall effect observable even at room temperature, can be explained with the band structure of graphene.

2.1.1 Calculation of first Brillouin zone

The band structure is conveniently described in the reciprocal lattice, also called momentum space or k-space. This momentum space is related to the crystal structure of a material. The graphene unit cell is defined by the three primitive vectors

$$\mathbf{a}_1 = \left(\sqrt{3}\mathrm{a}/2,\, \mathrm{a}/2,\, 0\right), \quad \mathbf{a}_2 = \left(\sqrt{3}\mathrm{a}/2,\, -\mathrm{a}/2,\, 0\right) \quad \text{and} \quad \mathbf{a}_3 = (0,\, 0,\, 1)\,,$$

where $\mathrm{a} = 0.246\,\mathrm{nm}$. Since graphene is a two-dimensional crystal, the third vector $\mathbf{a}_3$ is the perpendicular unit vector. The graphene crystal structure, together with the primitive vectors, is shown in Figure 2.2a. The alternative vectors $\mathbf{a}_1'$ and $\mathbf{a}_2'$ are only shown for completeness as they are also sometimes encountered in literature. The reciprocal primitive vectors are defined by the following relationship:

$$\mathbf{b}_1 = 2\pi\frac{\mathbf{a}_2 \times \mathbf{a}_3}{\mathbf{a}_1 \cdot (\mathbf{a}_2 \times \mathbf{a}_3)}, \quad \mathbf{b}_2 = 2\pi\frac{\mathbf{a}_3 \times \mathbf{a}_1}{\mathbf{a}_2 \cdot (\mathbf{a}_3 \times \mathbf{a}_1)} \quad \text{and} \quad \mathbf{b}_3 = 2\pi\frac{\mathbf{a}_1 \times \mathbf{a}_2}{\mathbf{a}_3 \cdot (\mathbf{a}_1 \times \mathbf{a}_2)}.$$

Using the above primitive vectors, we thus obtain

$$\mathbf{b}_1 = \left(2\pi/\sqrt{3}\mathrm{a},\, 2\pi/\mathrm{a},\, 0\right), \quad \mathbf{b}_2 = \left(2\pi/\sqrt{3}\mathrm{a},\, -2\pi/\mathrm{a},\, 0\right) \quad \text{and} \quad \mathbf{b}_2 = (0,\, 0,\, 2\pi)\,.$$

Figure 2.2b shows the reciprocal primitive vectors and first *Brillouin zone*.

The two points K and K′ at the corners of the graphene Brillouin zone are called Dirac points and are particularly important, as will be shown later.

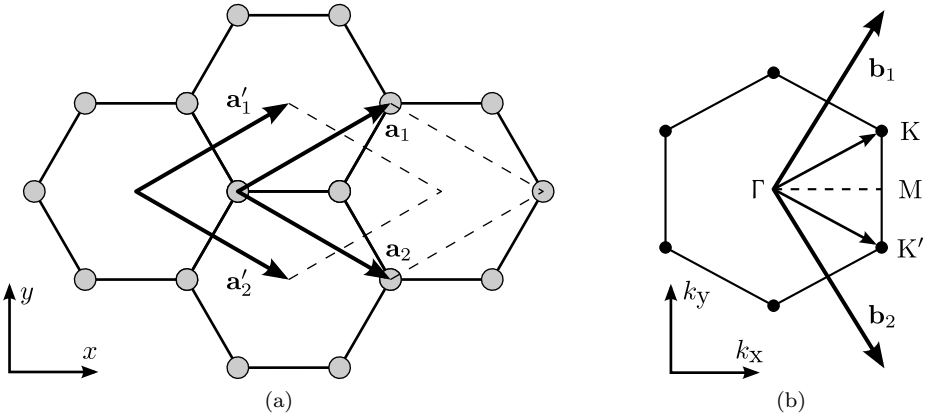


Figure 2.2: (a) Two possible ways of defining the elementary cell of graphene. (b) First *Brillouin zone* of graphene.

2.1.2 Tight-binding model

The band structure of graphene was first discussed by P. R. Wallace in 1947, with the aim to find an approximate model for the band structure of graphite [17]. By considering the interaction with the wave function of only two next neighbors (electrons can only hop to nearest- and next-nearest-neighbor), the tight binding model is calculated by

$$E(k_\mathrm{x}, k_\mathrm{y}) = \pm\gamma\sqrt{1 + 4\cos\left(\frac{\sqrt{3}k_\mathrm{x}\mathrm{a}}{2}\right)\cos\left(\frac{k_\mathrm{y}\mathrm{a}}{2}\right) + 4\cos^2\left(\frac{k_\mathrm{y}\mathrm{a}}{2}\right)} \tag{2.1}$$

where $\gamma = 2.7\,\mathrm{eV}$ is the nearest-neighbor hopping energy. A 3D model of this solution in the first *Brillouin zone* is shown in Figure 2.3.

2.1.3 Dispersion relation near K- and K′-point

The tight-binding model shows a very unique feature at the minima near the K- and K′-points of the reciprocal lattice, i.e. linear dispersion relation. For other crystals (including silicon), the region close to minima ($\vec{k} = 0$) can be approximated by the quadratic curve

$$E = \frac{\hbar^2\,\vec{k}^{\,2}}{2m_0}$$

with $\hbar$ the reduced Planck constant and m_0 the effective mass. In monolayer graphene, however, it was found that the effective mass of the charge carrier is zero. For the small region around the K- and K′-points, the tight-binding model can thus be reduced to [18]

$$E = \hbar v_\mathrm{F}\sqrt{k_\mathrm{x}^2 + k_\mathrm{y}^2} \tag{2.2}$$

with $v_\mathrm{F} = 10^6\,\mathrm{m/s}$ the Fermi velocity (speed of light $c = 300v_\mathrm{F}$). This unique linear dispersion relation with zero bandgap near the K-point is illustrated in Figure 2.4a-i, and the band shape is called Dirac cone.

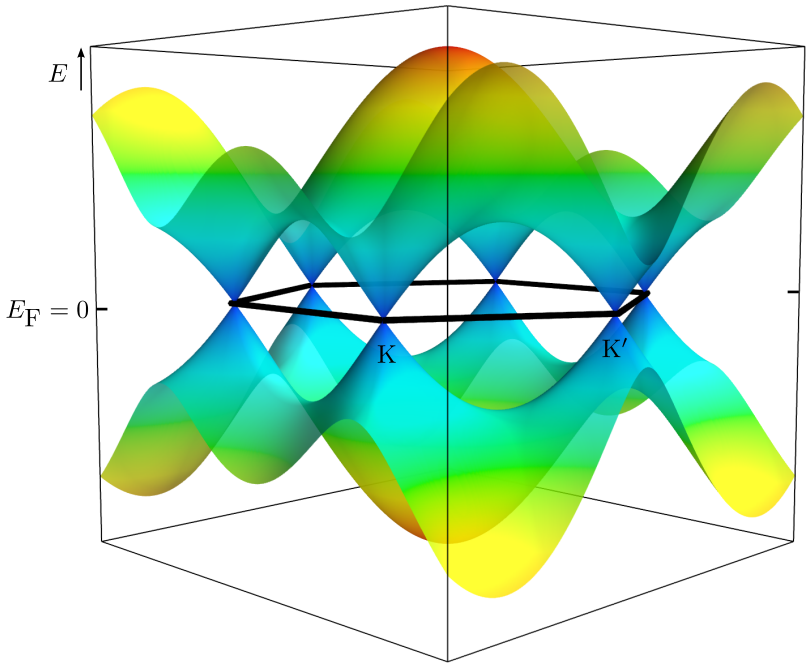


Figure 2.3: The two-dimensional tight binding energy surface of monolayer graphene. Dirac cones (linear dispersion) visible at K- and K′-points.

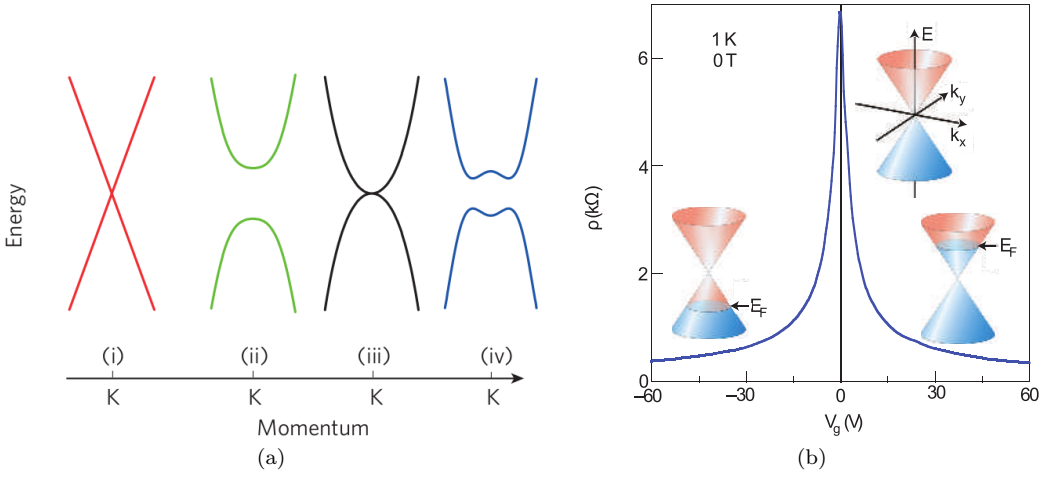


Figure 2.4: (a) Band structure of (i) monolayer graphene, (ii) graphene nanoribbons, (iii) bilayer graphene and (iv) bilayer graphene with a perpendicular electrical field applied. Reproduced from [19]. (b) Ambipolar electric field effect in single-layer graphene. Reproduced from [14].

Based on the assumption that monolayer graphene is a zero bandgap material as shown above, one would expect that for the Fermi level at the Dirac point, the resistivity would become infinite. This is, however, not the case, as shown in Figure 2.4b: For gate voltage $V_G = 0\,V$ a resistance of $7\,k\Omega$ is measured. The reason for this phenomenon is believed to be out of plane deformation of graphene. Graphene is assumed to be a perfect two-dimensional material; however, it has been shown that suspended graphene

develops out-of-plane ripples with amplitude of around 1 nm [14, 20, 21]. This out-of-plane ripple movement leads to scatter centers, and thus it is not possible to shut off conduction entirely.

It has been further shown by calculations and experiments that the band structure changes significantly with increasing number of graphene layers [22]. Bi-layer graphene, for example, has a parabolic band structure with slight band overlap, resulting in semi-metallic characteristics (see Figure 2.4a-iii).

2.1.4 Opening a bandgap in graphene

For transistor applications it is necessary for a material to exhibit a bandgap that is small enough to allow a significant amount of charge carriers to be readily excited, and large enough (more than 500 meV [23]) to permit depletion (and thus shutting off conduction) at ambient conditions. As explained above, monolayer graphene and bilayer graphene both have a bandgap of zero. Therefore, methods to open a bandgap in graphene are extensively investigated, which could eventually pave the way towards graphene-based logic circuits.

2.1.4.1 Biased bilayer graphene

When applying an electrical field perpendicular to bilayer graphene, a bandgap opens as illustrated in Figure 2.4a-vi. This particular parabolic band structure near the K-point with dent is sometimes called Mexican-hat shape [19]. The bandgap can be up to 250 meV at field strengths of 3×10^7 V/cm [24, 25]. However, since it disappears upon removal of the electrical field, this method to induce a bandgap is of little practical use, especially for low-power or battery-powered applications. To apply such a perpendicular electrical field, a sandwich structure with the graphene encapsulated between a top and bottom gate electrode is necessary [26]. A schematic cross section of such a structure is shown in Figure 2.25 (middle device) on page 29.

2.1.4.2 Graphene nanoribbons (GNR)

A honeycomb crystal can comprise two different edge structures, called armchair and zigzag, respectively [27] (see Figure 2.5a). Computations were done on migration of graphene zigzag edges [28], considering energetics and kinetics. The edge geometry has also influence on the band structure. It had been shown that zigzag graphene ribbons ([1 0] direction) are metallic, while armchair ribbons ([2 1] direction) exhibit a bandgap with a width dependent band gap [5, 29–32]. Calculations and experiments show that for a bandgap of 200 meV widths below 20 nm are necessary. To achieve this, electron beam lithography or mechanical derivation can be used. The band structure of such a nanoribbon is schematically illustrated in Figure 2.4a-ii.

The two distinct edge orientations manifest themselves also in exfoliated graphene and can be observed by optical microscopy [14], as illustrated in Figure 2.5b.

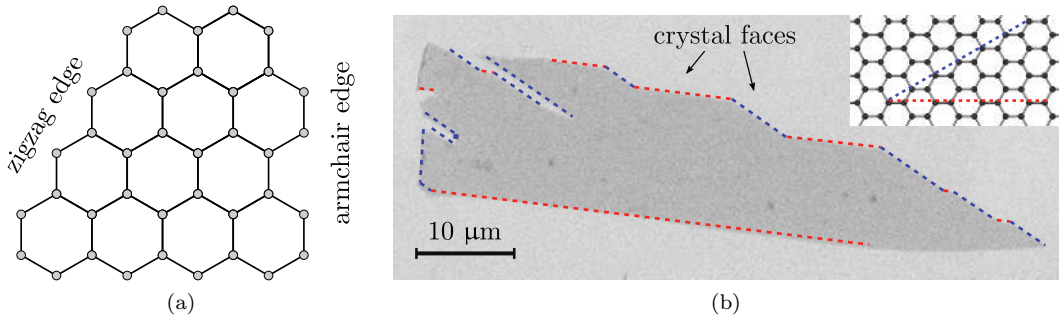


Figure 2.5: (a) The two possible edge geometries of planar hexagonal crystals: zigzag or armchair. (b) Optical detection of graphene crystal orientation. (b) reproduced from [14].

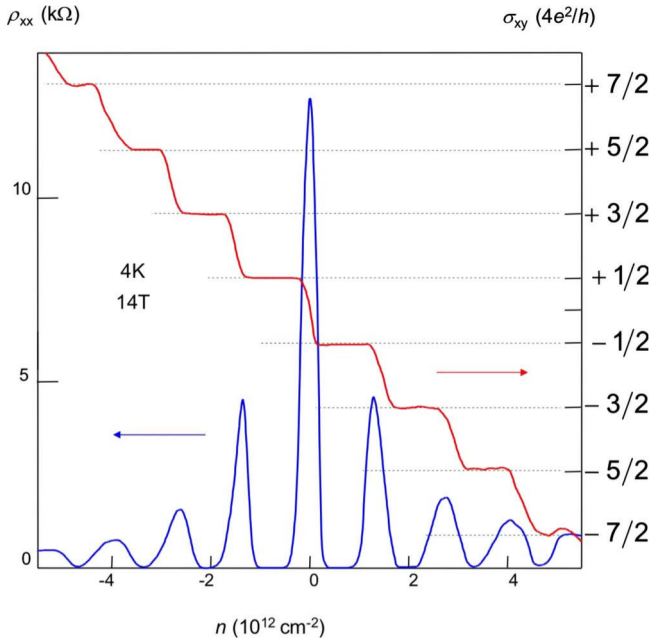


Figure 2.6: Quantum Hall effect in graphene as a function of charge-carrier concentration. Reprinted figure with permission from [27]. Copyright 2009 by the American Physical Society.

2.1.5 Quantum Hall effect at room temperature

The quantum Hall effect is the quantum-mechanical manifestation of the Hall effect. Typically, it can only be observed in two-dimensional electron systems at low temperatures and strong magnetic fields. The Hall conductivity σ_{xy} then takes on quantized values. In bilayer graphene, this effect of quantized conductivity can be observed even at room temperatures [33–36], and the plateaus of the hall conductivity $\sigma_{xy} = (4e^2/h)(N + 1/2)$ are shown in Figure 2.6. The position of the plateaus are shifted because the charge carrier in graphene mimic Dirac fermions [36].

Due to this remarkable property of graphene, exhibiting quantum-mechanical effects even at room temperature, the physics community benefits significantly from this material.

2.2 Other properties of graphene

The large interest in graphene is not exclusively due to its electronic properties. Graphene is also a material with excellent mechanical, thermal and optical properties. Furthermore, a single layer of graphene has a very high surface to mass ratio. In this Section, the current knowledge of non-electronic properties of graphene will be reviewed.

2.2.1 Mechanical strength

The strength, elasticity or hardness are very important information when working with materials. It allows the prediction of resonance frequencies, helps to determine necessary dimensions to withstand a given external force, or allows calculation of influence on electrical properties by mechanical stress. Standard methods to characterize thin film materials include *bulge testing*, *buckling*, wafer curvature, *nanoindentation*, measurement of resonance frequency and *microtensile testing* [37, 38].

Although graphene layer can be difficult to handle, mechanical properties have been extracted using several of these methods. An ultimate tensile strength of $\sigma_{\max} = 130\,\text{GPa}$ and *Young's modulus* of $E = 1.0\,\text{TPa}$ (∼5.5 times as high as silicon) were obtained from AFM nanoindentation experiments on suspended exfoliated graphene [39]. The suspended graphene structure and measurement method are schematically illustrated in Figure 2.7a. Nanobulge experiments, as illustrated in Figure 2.7b, where a cavity with a defined pressure is sealed using a monolayer graphene sheet, were used to extract an elastic constant of $390\pm20\,\text{N/m}$ [40]. However, no calculations were done to obtain E or $\sigma_{\max}$. This requires exact knowledge of the dimensions, as well as possible edge effects of the membrane. Other nanointendation measurements were done on suspended graphene ribbons that were epitaxially grown on SiC and later underetched [41]. The exact mechanical size was not reported, which makes a comparison difficult.

The nanobulge measurement, mentioned before, showed that monolayer graphene is furthermore impermeable for gases [42].

2.2.2 Thermal conductivity

Graphene was found to have a very high thermal conductivity k between 4.4 and $5.78 \times 10^3\,\text{W/mK}$ [43]. This is more than a factor of 10 higher than the thermal conductivity of gold, and opens wide possibilities for thermal management when used as material in electronic circuitry. This parameter was measured using Raman spectroscopy on exfoliated graphene flakes, placed over 2-5 µm wide trenches. Large graphitic pieces were attached to the edges of the sheets at a distance of ∼10 µm. The center of the suspended strip was then heated by incident laser light, while the position of the G-peak was monitored, as shown in Figure 2.7d. The position of this peak was found to have a strong temperature dependence [44]. The portion of the laser power dissipating in the graphene sheet was obtained through experiments on highly oriented graphite and

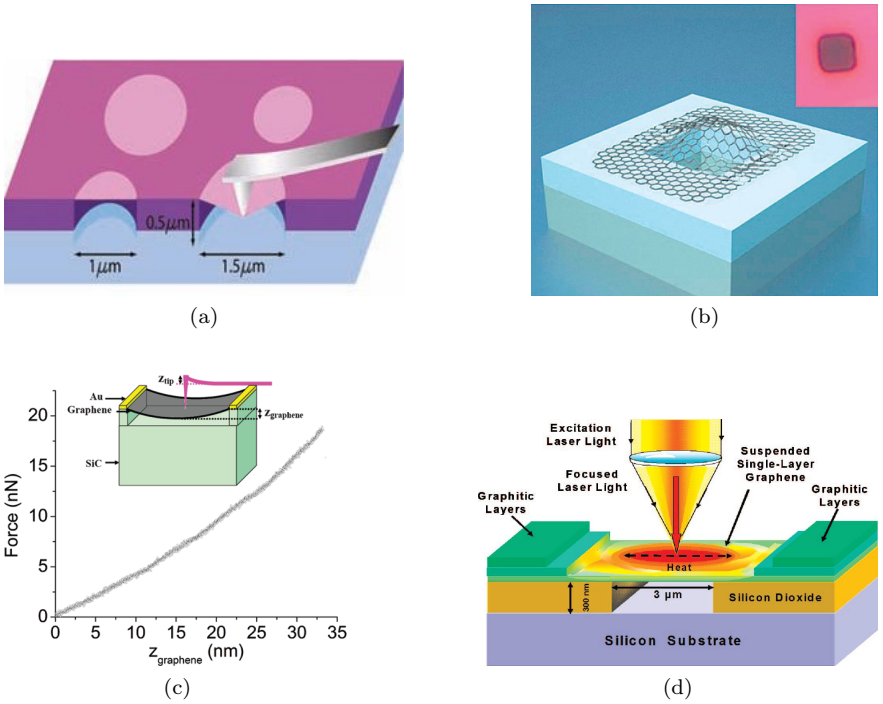


Figure 2.7: (a) Schematic depiction of nanoindentation measurements on suspended exfoliated graphene. From [39]. Reprinted with permission from AAAS. (b) Schematic depiction of graphene membrane used for bulge testing and permeability experiments. Inset top-right shows top view of membrane. Reprinted with permission from [40]. Copyright 2008 American Chemical Society. (c) Force-displacement curve obtained on suspended graphene ribbon epitaxially grown on SiC. Reprinted with permission from [41]. Copyright 2009 American Chemical Society. (d) Method for optical measurement of thermal conductivity of suspended graphene. Reprinted with permission from [43]. Copyright 2008 American Chemical Society.

calculations. This high thermal conductivity can be explained by the high electron (and also phonon) mobility.

2.2.3 Surface-to-mass ratio

In some applications, mainly catalytic reactions or gas sensing, large surface-to-mass ratios are of benefit. This value for monolayer graphene is very large, as the atoms are bound only in-plane. The unit cell of graphene contains two carbon atoms ($n_\mathrm{A} = 2$) and has an area $A = \sqrt{3}\mathrm{a}^2/2$ where $\mathrm{a} = 0.246\,\mathrm{nm}$. Considering the molar mass of carbon ($\mathrm{M_C} = 12\,\mathrm{g/mol}$) and the two sides ($n_\mathrm{S} = 2$) of a graphene sheet, the area to mass ratio can easily be calculated by

$$S_\mathrm{graphene} = \frac{\mathrm{N_A} n_\mathrm{S} A}{\mathrm{M_C} n_\mathrm{A}} = 2630\,\frac{\mathrm{m}^2}{\mathrm{g}}$$

with $\mathrm{N_A} = 6.022 \times 10^{23}\,\mathrm{mol}^{-1}$ the *Avogadro constant*.

2.2.4 Optical properties

The opacity of monolayer graphene is solely defined by the fine structure constant $\alpha = e^2/\hbar c \approx 1/137$ (c is speed of light) and absorbs $\pi\alpha = 2.3\%$ of incident white light [45]. This is a very low value for a one atom thin material.

The bilayer graphene bandgap can be tuned up to 250 meV (corresponding to a wavelength $\lambda = 5\,\mu m$), which allows electrical tuning of the optical properties. Therefore, graphene has wide application in ultrafast pulsed lasers [46]. It is also discussed whether graphene will find application in devices such as microwave saturable absorber, modulator, polarizer, microwave signal processing, and broad-band wireless access networks [47]. Some of the applications of this graphene property will be discussed in Section 2.5 on page 22.

2.3 How to detect and characterize graphene

It was shown above that defect-free graphene has very exceptional electrical properties, particularly in a single layer. However, it is first necessary to detect graphene and characterize its quality. The procedure to detect and locate graphene has been established and is used today by many researchers. However, before 2004 this was not the case. Whenever a graphite pencil is drawn across a piece of paper, among the micro- and nanometer sized debris forming the pencil trace, some monolayer graphene flakes could be found [27]. Nevertheless, it stayed undetected until recently.

2.3.1 Optical contrast method

Monolayer graphene can be made visible in an optical microscope by placing it on 300 nm of SiO_2 [4]. Different number of layers can be determined by an optical contrast method [48], taking advantage of transparency of graphene. A graphene flake with areas comprising different numbers of layers is shown in Figure 2.8.

2.3.2 Raman spectroscopy

Raman spectroscopy is a non-destructive technique to study vibrational, rotational, and other low-frequency modes of a material [49]. Raman spectroscopy had been extensively used in graphitic materials [50], and its usefulness for graphene has been demonstrated. From Raman spectra, the defect density can be obtained, and the number of graphene layers can be determined [51].

In Figure 2.9a, the Raman active modes of monolayer graphene are illustrated, and in Figure 2.9c, a Raman spectrum of defective monolayer graphene comprising these peaks is shown. The G-peak is a first-order Raman active scattering process (direct excitation without phonon), while the D-peak is a double resonance process. It involves one iTO-phonon (in-plane transversal optical) and one defect scattering. Due to the fact that a defect scattering effect is required for this process to manifest itself, this peak

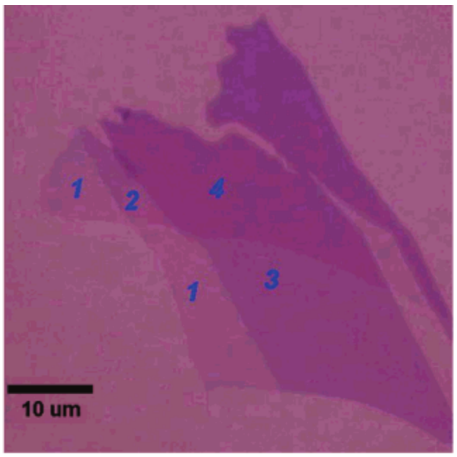


Figure 2.8: Optical microscope image of exfoliated graphene flake. The optical contrast method is used to determine the number or layers. Reprinted with permission from [48]. Copyright 2007 American Chemical Society.

is often referred to as the disorder peak. It only appears in regions where the perfect periodicity of graphene is broken, such as edges or crystal defects.

The 2D-peak[1] is the sum of two Raman active scattering processes. One double and one triple resonance, as shown in Figure 2.9a. While the double resonance occurs in bilayer graphene and graphite, the triple resonance is exclusive to monolayer graphene. It requires two iTO phonons, one scattering the excited electron and the other one the hole. Through this effect, the 2D-peak has a higher intensity than the G-peak in monolayer graphene, which is a very unique and distinct Raman signature.

The 2D-peak holds additional valuable information, namely the number of graphene layers. This can be explained by the scattering process and the modified band structure of two graphene layers in Bernal AB stacking (shown in Figure 2.9b). For a given excitation wavelength, two different excitation states are allowed, which can then scatter to one of the two bands. Thus in bilayer graphene, four peaks can be distinguished, as shown in Figure 2.9d. For larger numbers of layers the 2D-peak components change further, finally reaching the two component peak for HOPG.

This evolution of the Raman spectrum of defect-free graphene with the number of layers is illustrated in Figure 2.10.

2.3.3 Graphite or Graphene?

Since the stability of monolayer graphene at room temperature had been experimentally demonstrated [4], the research into carbon-based materials has gained momentum [54]. In the last eight years, the usage of the word *graphene* has been gradually extended. Initially, it was only used to describe one single layer of the honeycomb carbon film, but now it is also used in the context of *bilayer graphene* (BLG), *fewlayer graphene* (FLG)

[1] This peak is also sometimes referred to as G'-peak in literature.

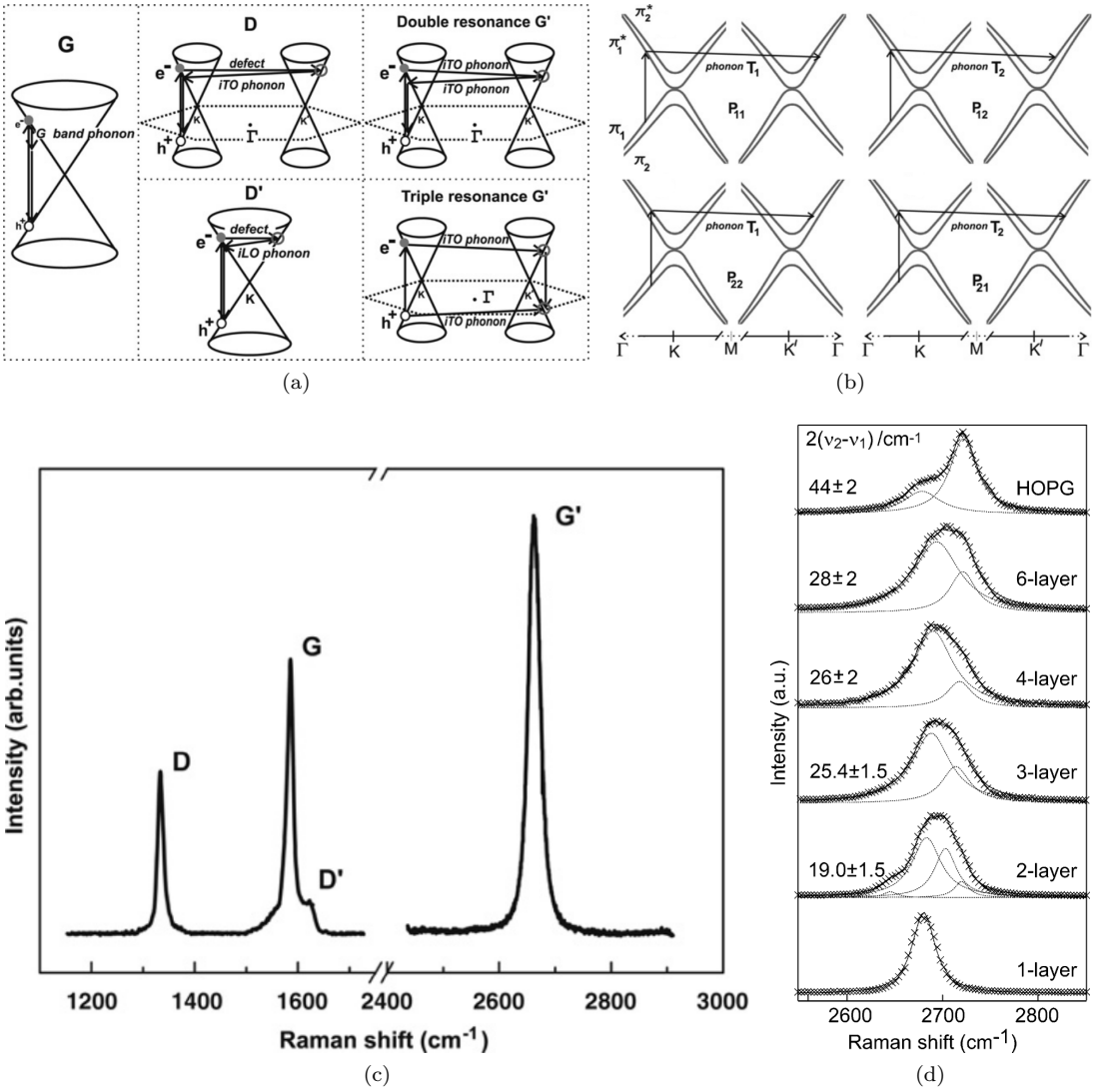


Figure 2.9: (a) First-order Raman and double resonance Raman scattering processes in graphene. G' (also referred to as 2D) is the sum of the double resonance and triple resonance scattering process. The latter only occurs in monolayer graphene. (b) Due to the modified band structure of graphene with more than 1 layer, four scattering processes with very similar Raman shift occur. (c) Full Raman spectrum of graphene edge. (a-c) reproduced from [51]. (d) Evolution of 2D peak shape and location with increasing number of layers. Reprinted with permission from [52]. Copyright 2007 American Chemical Society.

and even *multilayer graphene* (MLG) which can consist of more than one hundred layers [7], a material that would have been traditionally referred to as *graphite*. A similar shift of naming convention in the graphene research community occurred for nanocrystalline graphite, as described by Ferrari *et al.* [55]. Quite recently, films with Raman characteristics very similar to those described, have been called *nanographene* [56–58] or *nanocrystalline graphene* [59, 60]. Several researchers decided, however, to maintain the traditional naming convention and called their films *nanocrystalline graphite* [61]. Nevertheless, in order to be consistent with the scientific community, it was decided to

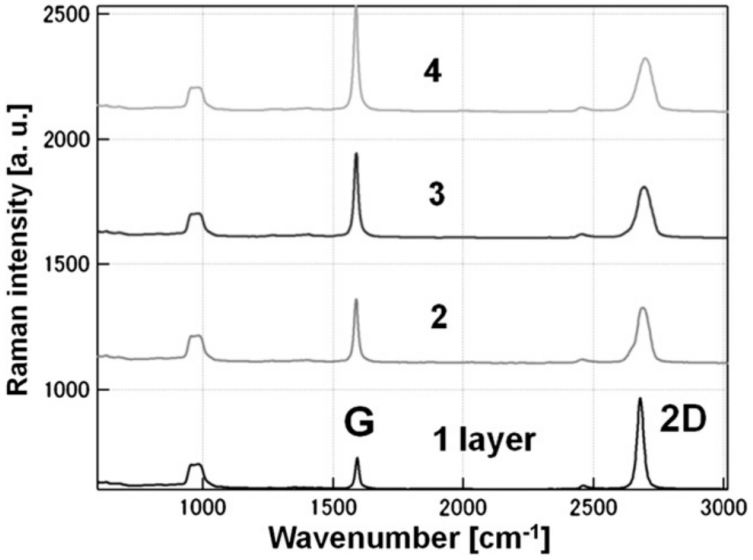


Figure 2.10: Raman spectra of exfoliated graphene with 1 to 4 layers. With increasing number of layers the 2D peak changes. Reproduced from [53].

adopt *nanocrystalline graphene* as the name for the films deposited by PECVD on SiO_2 in this work.

2.4 Methods to obtain graphene

In this Section, several growth/deposition methods used to obtain graphene will be reviewed, with a focus on whether these methods are suitable for large area growth. First, exfoliation from graphite will be discussed, followed by epitaxial growth on silicon carbide (SiC) and catalytic growth on metal by chemical vapor deposition (CVD). Then, substrate free CVD growth and plasma enhanced chemical vapor deposition (PECVD) is discussed (including this work). A visual summary of these methods will be given in Table 2.1.

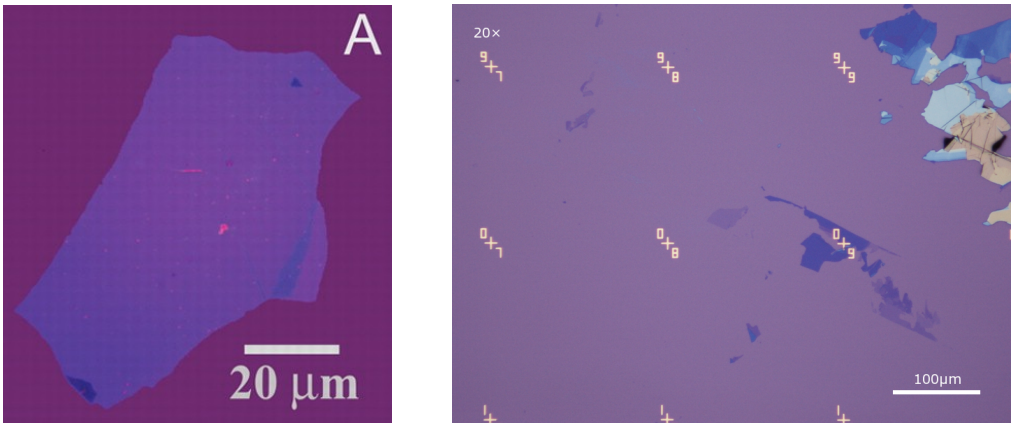
2.4.1 Exfoliation from graphite

Graphite is a stack of many graphene layers that are bonded together by weak van der Waals force. It has been shown that this weak force can be broken by applying a mechanical cleaving force, in the case of Novoselov and Geim by the use of an adhesive tape approach [4]. This method is a top–down method, meaning that the graphene is already present in the shape of graphite. Therefore, the quality of the graphite has immediate influence on the final graphene quality. The best quality graphite is highly ordered pyrolytic graphite (HOPG), which is commercially available in sizes of up to $20 \times 20\,mm^2$. The size of graphene flakes, obtained from HOPG and placed on 300 nm thick SiO_2 (Figure 2.11a) for visibility under white light microscopy, does not exceed 1 mm. A commercial graphene sample, comprising markers and flakes, is shown in Figure 2.11b. Nevertheless, exfoliation of HOPG is simple, does not require a lot of investment and

Method	**Description**	**Advantages**	**Disadvantages**
Exfoliation from graphite	Graphene peeled from HOPG using adhesive tape	• Highest quality • Simple	• Random (shape, size, location) • Does not scale
Epitaxial growth on SiC	SiC annealed (1200–1500 °C) → Si sublimation	• Good control over number of layers • Large domains	• Expensive substrates • High temperature • Surface steps
Catalytic growth on metal (CVD)	Catalyst film heated and hydrocarbon supplied (530–1000 °C)	• No limit of substrate size • Low temperature	• Requires transfer for electr. application • Metal
Metal-free PECVD (this work)	Insulator exposed to hydrocarbon plasma (parallel plate, 700–900 °C)	• No limit of substrate size • No transfer • Metal-free	• Small crystalline graphene grains

Table 2.1: Comparison chart of selected graphene growth/deposition methods.

offers the highest graphene quality of all methods so far. The disadvantages result from the nature of the method: The obtained flakes are random in shape, size and location, and, most importantly, the method does not scale. Certain advancements are expected, but direct mechanical exfoliation of graphene at wafer-scale remains doubtful.



(a) (b)

Figure 2.11: Exfoliated graphene sheet. (a) One of the first monolayer graphene sheets ever observed. Optical microscopy on 300 nm SiO_2. From [4]. Reprinted with permission from AAAS. (b) Commercially available exfoliated graphene flakes. Flakes are individually obtained and cataloged with respect to alignment marks. Reprinted with permission from [62].

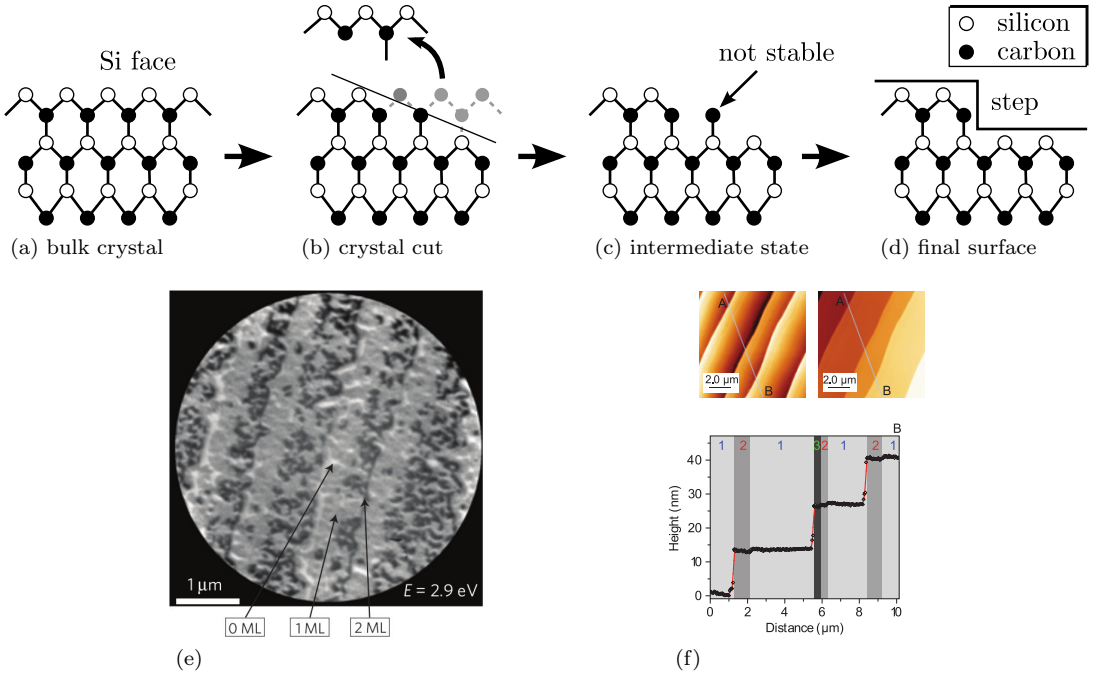


Figure 2.12: Schematic atom-scale explanation of surface steps formation on SiC during epitaxial growth. (a) The bulk crystal is (b) cut during wafer fabrication. Due to unavoidable misalignment, thermodynamically instable atoms remain (c). These detach resulting in (d) a stepped surface. (e) LEEM image of graphene on SiC and (f) AFM measurements showing surface steps of 15 nm. (e+f) reproduced from [65].

2.4.2 Epitaxial growth on SiC

A very popular method for graphene growth is the epitaxial growth on SiC. The Si is thermally decomposed and sublimates away, while the carbon rich surface layer crystallizes to graphene. One problem with SiC, however, is the inherent atomic surface steps formation, resulting from the inaccurate alignment of the SiC crystal and cutting orientation during wafer fabrication. This step formation process is schematically illustrated in Figure 2.12a to d, and the steps have a height of $\sim 2.52\,\text{nm}$ for 6H-SiC (hexagonal SiC with unit cell consisting of six Si-C bilayers). Epitaxial growth requires temperatures of more than 1200 °C and ultra high vacuum [63]. It has been found, however, that growth at ultra high vacuum results in a very rough surface [64]. This was partially resolved by Emtsev *et al.* [65], when they performed the epitaxial growth at atmospheric pressure and elevated temperature (1500 °C). The surface after growth is regular, but the surface steps become more pronounced with heights of 15 nm (in comparison, monolayer graphene has a thickness of only 0.335 nm). A low-energy electron microscopy (LEEM) micrograph and AFM results of the SiC surface after growth are shown in Figure 2.12e and f, respectively.

Nevertheless, epitaxial growth was shown to allow accurate control of the number of graphene layer by controlling the growth duration, and the obtained graphene has large,

high-quality crystalline graphene domains. Transistors with switching speed of 100 GHz were realized on such graphene films [66]. The disadvantages of this method are the high cost of SiC substrates, the very high temperature making specialized equipment necessary, and the inherent surface steps. Furthermore, wet and dry etching of SiC is very challenging and the transfer of the grown graphene remains difficult.

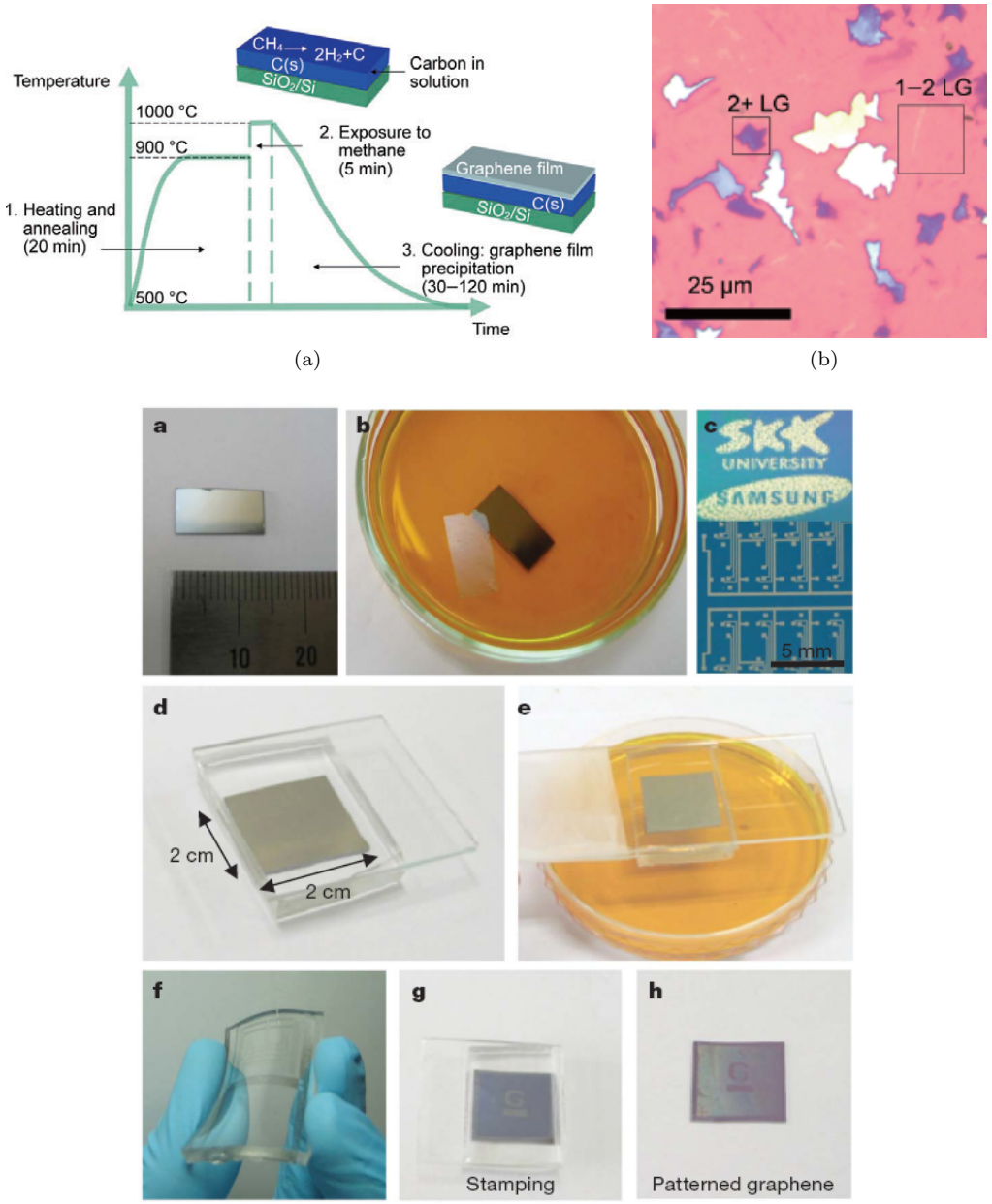
2.4.3 Chemical vapor deposition on metal

Chemical vapor deposition of graphene on metal thin films such as nickel [6, 67, 68], iron [7], copper [69, 70], ruthenium [71], or iridium [72] has been demonstrated. This method typically involves sputtering or e-beam evaporation of an initial thin metal film, followed by the exposure to a carbon rich atmosphere at high temperatures. This carbon source (methane (CH_4) or ethyne (C_2H_2)) is thermally decomposed and the carbon solves in the metal film. During cool-down, the solubility of the carbon in the metal decreases, resulting in crystallization of graphene on the surface. One reported growth cycle on Ni is illustrated schematically in Figure 2.13a [67]. After a pre-annealing of the Ni film at 900 °C, methane (CH_4) is introduced into the CVD chamber for 5 min at 1000 °C, followed by a slow cool-down to room temperature. A relatively low temperature CVD process was developed by Kondo *et al.* [7] and is performed below 650 °C on an iron substrate with ethyne.

Since metal thin films are generally amorphous or have small crystalline grains even after prolonged annealing, CVD-grown graphene shows alternating thicknesses and crystal lattice misalignments [6]. A microscope picture of a graphene film, grown using the annealing cycle on nickel, outlined in Figure 2.13a, and later transferred to a 300 nm SiO_2/Si substrate is shown in Figure 2.13b.

Many applications require a transfer of graphene onto insulating substrates. Two possible transfer methods were demonstrated with films grown using CVD on nickel [68], one in aqueous solution and the other one dry. In the first method, the graphene film detaches and floats in the aqueous solution after the wet etching of the nickel (this is illustrated in Figure 2.13c-b). After that, the film can be picked up and placed on any substrate. The dry method involves the deposition of a PDMS (polymer) film or stamp on top of the graphene (Figure 2.13c-d) and a subsequent nickel wet etch in $FeCl_3$ solution (Figure 2.13c-e). The graphene attached to the PDMS can then be placed on arbitrary substrates (Figure 2.13c-g), and the PDMS is dissolved using acetone to complete the transfer process (Figure 2.13c-h). Recently, a roll-to-roll process for transparent electrodes, as shown in Figure 2.14, was demonstrated [8]. Rectangular areas with diameter of 30 inch (76.2 cm) with very high crystal quality were successfully obtained.

In summary, CVD growth of graphene offers flexibility with respect to substrate size, and can be performed at relatively low temperatures. However, a transfer step is necessary for electronic applications, and the metal catalyst is problematic due to the required chemical etch, possible contamination, and economic considerations.



(a) (b)

(c)

Figure 2.13: CVD growth of graphene on metal substrates. (a) Heating profile and conditions used for graphene growth on amorphous nickel and (b) optical image of graphene film transferred to SiO_2/Si. (a+b) reproduced from [67]. (c) Various stages of graphene film transfer grown on Ni catalyst. After wet-etching of the Ni film, the floating graphene can be transferred to various substrates, or a PDMS stamp is used. Reproduced from [68].

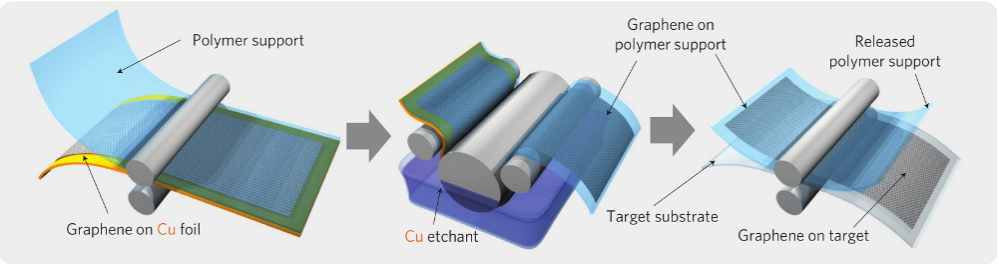


Figure 2.14: Roll-to-roll transfer process of graphene grown on copper foil. Reproduced from [8].

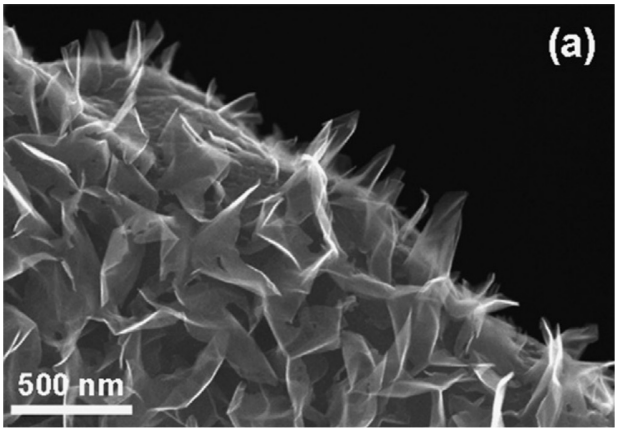


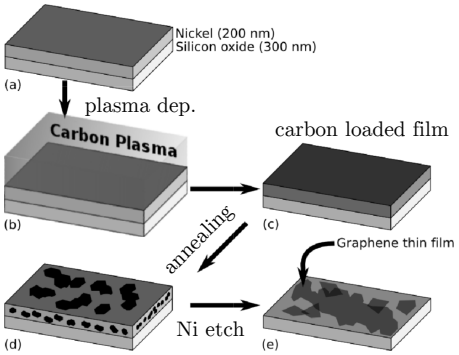
Figure 2.15: Cauliflower-like graphene obtained by PECVD. Reproduced from [160].

2.4.4 Plasma enhanced chemical vapor deposition

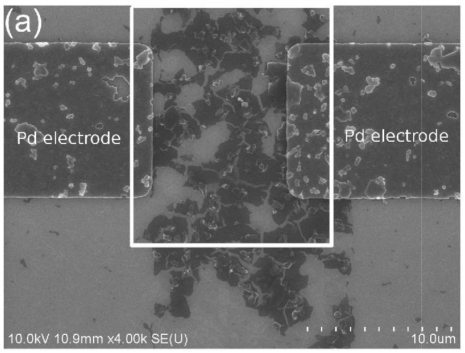
PECVD is a well established method for the deposition of oxide, nitride, doped or undoped amorphous and polycrystalline silicon, and other semiconducting materials. Also carbon nanotubes (CNT) have been deposited by PECVD [73]. The advantages of PECVD are the applicability to large substrates, lower vacuum requirements and high uniformity.

Experimental research on PECVD deposition of graphene was carried out as early as 2003 [74]. The graphene-like carbon obtained then and in several other experiments that followed [75–77, 160], however, was not planar. Figure 2.15 shows such graphene films that are believed to be vertical due to the electric field orientation. These films are consequently not suitable for planar microfabrication processes.

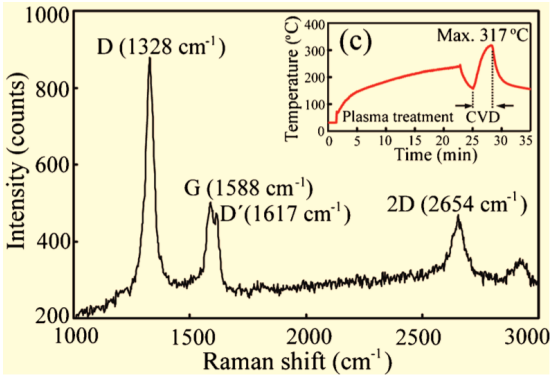
In more recent time, various methods making use of PECVD or other plasma-assisted processes to obtain planar graphene-like films were reported. Baraton *et al.* [78], for example, used a triode PECVD setup to supply carbon to a previously deposited nickel film. After annealing at 900 °C, the carbon segregates to the interface between nickel and SiO_2, and is exposed after nickel wet etching. The deposition process flow chart is illustrated in Figure 2.16a, and an SEM micrograph of the obtained graphene is shown in Figure 2.16b. The irregular coverage makes it, however, unsuitable for large area fabrication.



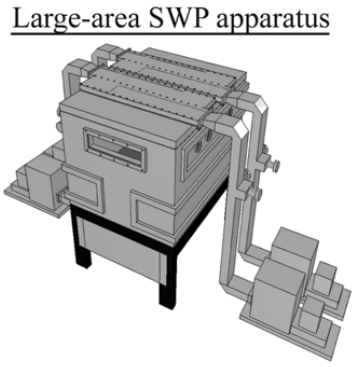
(a) From Baraton *et al.* [78]



(b) From Baraton *et al.* [78]



(c) From Kim *et al.* [79]



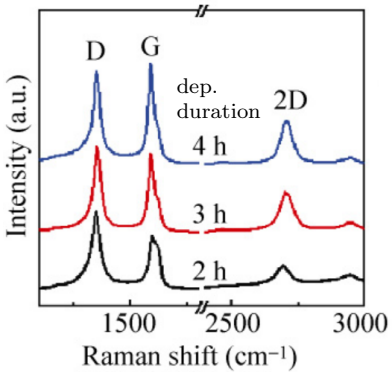
(d) From Kim *et al.* [161]

Figure 2.16: Review of plasma-assisted deposition methods for graphene and graphene-like films involving metal. (a+b) Deposition by triode PECVD on Nickel. After annealing at 900 °C and nickel etch, graphene is obtained on SiO_2 surface. Reproduced from [78]. (c) Raman spectrum of graphene-based film on aluminum deposited by surface wave PCVD. Reprinted with permission from [79]. Copyright 2011, American Institute of Physics. (d) 3D model of surface wave PECVD apparatus with four microwave sources. Reproduced from [161].

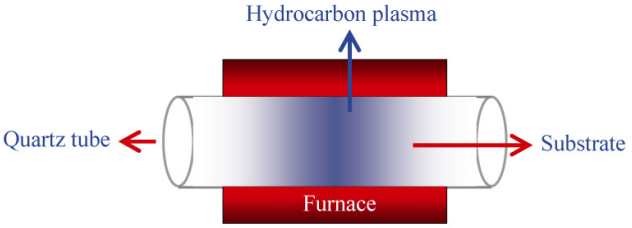
Surface wave plasma chemical vapor deposition (SWP-CVD) was used by Kim *et al.* [79] to deposit graphene-based films at 400 °C on copper or aluminum foils. This method is closely related to CVD growth, however, growth temperatures could be reduced significantly by using plasma activation. The Raman spectrum of such a film deposited on aluminum (Figure 2.16c) indicates strong disorder (D-peak).

Graphene growth by a remote PECVD system at relatively low substrate temperatures of 550 °C has been reported by Zhang *et al.* [56]. As the name suggests, the hydrocarbon source is decomposed in a plasma field away from the substrate, and the radicals are directed over the SiO_2 substrate, where planar graphene-like films are deposited. The Raman spectra of films deposited for 2, 3 and 4 h are shown in Figure 2.17a, again indicating disorder. The *r*-PECVD system is limited to 100 mm substrates. Although such films have smaller crystalline domains compared to exfoliated graphene, they benefit from large area coverage directly on insulating substrates.

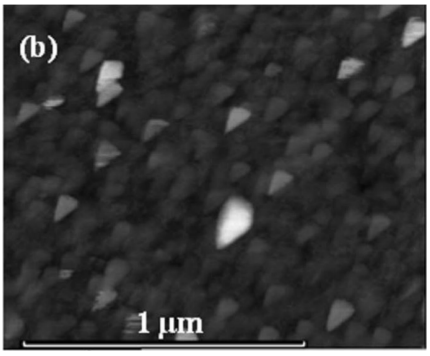
Another plasma enhanced method, reported to yield nanographene films, is microwave



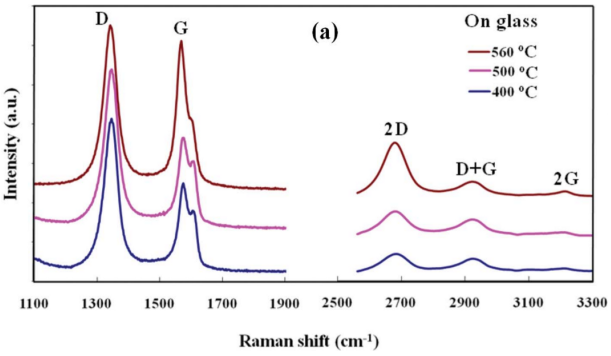
(a) From Zhang *et al.* [56]



(b) From Zhang *et al.* [56]



(c) From Kalita *et al.* [58]

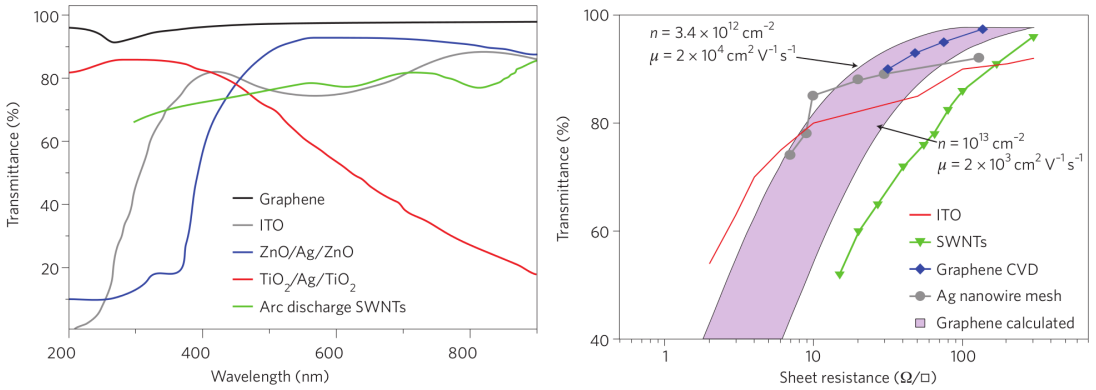


(d) From Kalita *et al.* [58]

Figure 2.17: Review of plasma-assisted deposition methods for graphene and graphene-like films on insulating substrates. (a) Raman spectra of graphene on SiO2 deposited by remote PECVD system schematically illustrated in (b). (a) reproduced from [56], (b) reproduced from electronic supplementary material of [56]. (c+d) AFM topography and Raman spectra of nanographene deposited on SiO_2 by microwave assisted surface wave plasma (MW-SWP) CVD. [58] – Reproduced by permission of The Royal Society of Chemistry.

assisted surface wave plasma (MW-SWP) CVD [58]. Kalita *et al.* successfully deposited films using this method with a very characteristic triangular topography on glass and silicon, respectively, at temperatures between 400 °C and 560 °C. An AFM image of the surface is shown in Figure 2.17c. Raman spectra of films deposited on glass are shown in Figure 2.17d.

In conclusion, some of the plasma enhanced CVD and other plasma-based processes reviewed here offer several advantages over mechanical exfoliation, epitaxial growth on SiC and CVD. These are large substrate sizes, metal-free deposition, and consequently there is no need for graphene transfer. The disadvantage of the PECVD methods is the apparent lower crystal quality of the graphene, as compared to exfoliated graphene. Nevertheless, it is a method with huge potential not yet fully developed.



(a) (b)

Figure 2.18: (a) Transparency of graphene, ITO and other transparent conductive films. (b) Transparency versus sheet resistance plots for different transparent conductive films, including CVD graphene and theoretical calculation of graphene. Reprinted by permission from Macmillan Publishers Ltd: Nature Photonics [81], copyright 2010.

2.5 Graphene applications

Graphene has several applications. Firstly, it is a very interesting material for the study and confirmation of fundamental principles in physics. An example of this is the observation of the quantum Hall effect at room temperature, as explained in Section 2.1.5 on page 8. But there are also a number of other applications which benefit from graphene. In this Section, these different application areas are divided into transparent conducting electrode, transistor, optical transducer, superconductor and gas sensor, and are discussed based on published work.

2.5.1 Transparent conducting electrodes

To date, the most practical application for graphene is as electrode in electronic and photonic devices. Integrating graphene offers a lot of flexibility to the device's design because of the excellent electrical, optical and mechanical properties of graphene. The large amount of graphene publications concerning transparent electrode applications [80] support this observation, and this was further confirmed at the *Graphene 2012* conference during the panel discussion concerning the graphene position paper [9]. Two drivers of this development are the increasing cost for indium tin oxide (ITO), the current industry standard, and the increasing demand for flexible transparent electrodes. As ITO is very brittle and shows fast deterioration upon repeated deformation [81], graphene has a realistic chance in this field. An additional advantage of graphene over ITO and other materials is its broadband transparency, as shown in Figure 2.18a.

2.5.1.1 Theoretical limit of graphene

In order to allow comparison of transparent electrode materials obtained by different researchers, it is common to report the transmittance at 550 nm wavelength and the

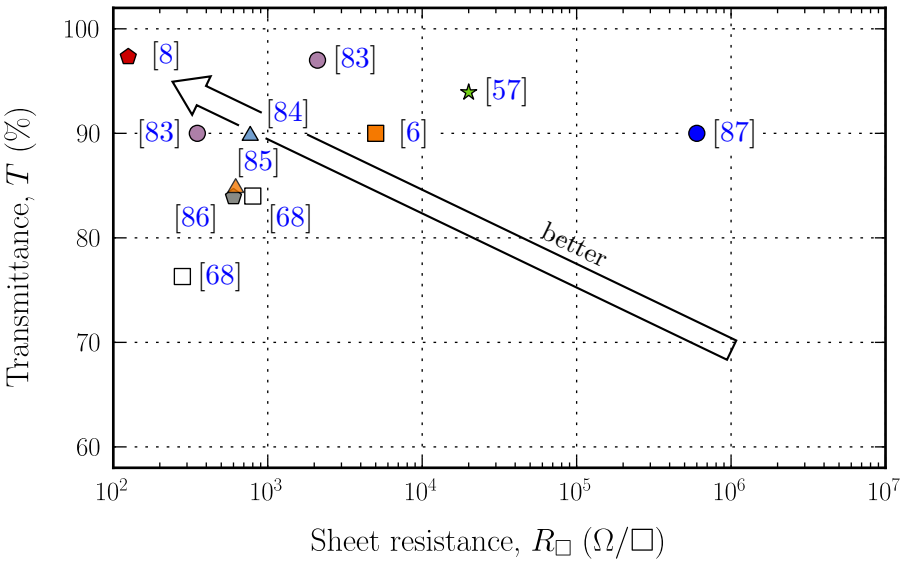


Figure 2.19: Comparison chart of reported transmittance T versus sheet resistance $R_\square$ values from literature.

corresponding sheet resistance $R_\square$. It has also been suggested to use the ratio of the electrical conductivity σ to the visible absorption coefficient α as a quantitative measure (figure of merit) of the performance of transparent conductors [80, 82], defined as

$$\sigma/\alpha = -\frac{1}{R_\square \ln(T+R)} \tag{2.3}$$

with T and R the transmission and reflectance, respectively, with a value between 0 and 1. This latter ratio, however, is not as prevalent in graphene literature as the separate values for transparency and sheet resistance. This is most probably due to the additionally required reflectance value, which is often not measured. Furthermore, when compared to other transparent electrode materials such as ITO with a figure of merit of 4 [82], the values for graphene films are much lower and do not allow intuitive comparison of results. The lower limit of transmittance for highly efficient commercial applications is 90% [9]. ITO has a sheet resistance of $10 - 30\,\Omega/\square$ at 90% transmittance. This is regarded as the benchmark value that has to be exceeded for any material to become a viable alternative to ITO. Calculations have shown that graphene has the potential to achieve this for transparencies above 85% (this applies to less than six layers of graphene) [81], as shown in Figure 2.18b.

2.5.1.2 Reported graphene performance values

In Figure 2.19, several transparent graphene electrode performance values from literature are compared. Most of these results were obtained graphene grown on metal substrates by CVD with consecutive transfer onto a transparent carrier. Nickel was used in Refs. [6, 68, 85, 86], while Refs. [8] and [83] used a copper catalyst layer. The results reported by Blake *et al.* [84] were obtained from exfoliated graphene, and Medina *et al.* [57] used

electron-cyclotron resonance CVD (ECR-CVD) to deposit graphene directly on quartz. The relatively high sheet resistance of 600 kΩ reported by Eda *et al.* [87] were obtained through reduction of deposited graphene oxide. Additional values can be found in review papers, such as [80, 81, 88].

2.5.2 Graphene transistor

Silicon transistors act as switches in logic circuitry, and by complementing p- and n-type metal oxide semiconductor field effect transistors (MOSFETs), low power consumption can be achieved. The performance of such integrated circuits constantly increases following Moore's law, but it is becoming increasingly difficult to maintain the development with silicon (gate oxide scaling and short channel effect are two issues). Therefore, extensive work is being done to evaluate the suitability of graphene as a silicon replacement. Currently, the main obstacle for graphene to replace silicon is the difficulty to engineer the bandgap, as explained in Section 2.1.4 on page 7.

There are two different types of semiconductor electronics: logic (digital) and radiofrequency devices. For the former, it is paramount to be able to completely shut off conductivity, which is not currently possible [19]. For the latter semiconductor device, a very fast response to the gate modulation is necessary. For this, a gate-controlled channel region with very small, but well defined thickness is necessary. Such a control over the number of layers in graphene has been demonstrated. Other properties of graphene, that are beneficial to radiofrequency devices, are the high carrier mobility and low series resistance.

The reported I_D–V_D results of a graphene transistor (schematic illustration shown in Figure 2.20A, graphene oxide (GO) used as gate insulator) are shown as inset in Figure 2.20B [89]. The characteristic is linear (metal-like), with a weak gate modulation effect. Due to the large mobility, the saturation region typically observed in silicon transistors is not reached. The drain current as a function of the gate voltage (see Figure 2.20B) has a minimum value. Figure 2.20C shows the temperature dependence of the channel resistance. Similar to metals, resistivity increases for decreasing temperatures.

A switching speed of 26 GHz was reported by Lin *et al.* [90] for a transistor fabricated from exfoliated graphene. A channel length of 150 nm and a 12 nm thin Al_2O_3 layer was used as gate oxide. The same group furthermore demonstrated switching speeds of up to 100 GHz for 240 nm channel lengths on wafer-scale epitaxial graphene on SiC [66]. These devices have relatively low on/off ratios.

A on/off ratio of 100 at room temperature for a transistor fabricated from exfoliated bilayer graphene was reported by Xia *et al.* [26]. As gate oxide, atomic layer deposited (ALD) hafnium oxide (HfO_2) was used, and a back gate voltage between -120 and 80 V allowed the modulation of the bandgap of the bilayer graphene.

The transistors mentioned so far have a straight channel, and the in-plane crystal orientation (and thus different band structure, see Section 2.1.4.2 on page 7) is not considered. A reported graphene transistor structure, fabricated by focused ion beam

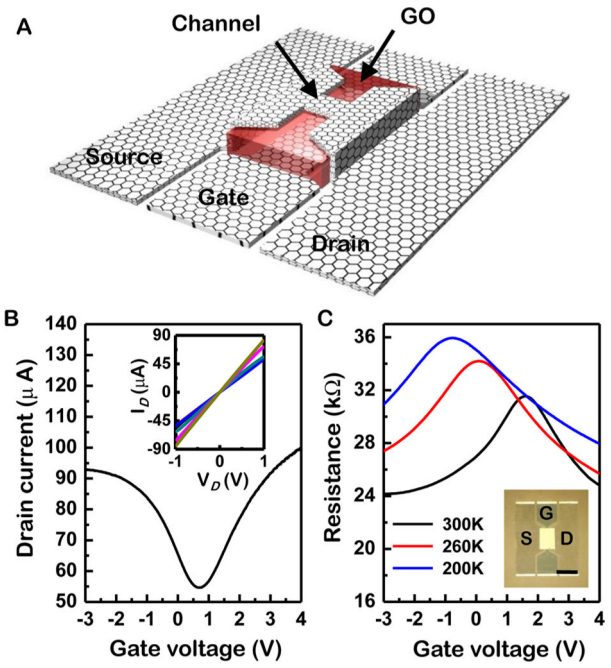


Figure 2.20: (a) Schematic illustration of all-graphene transistor with graphene oxide (GO) as gate oxide layer. (b) Drain current modulation by gate voltage and (c) temperature dependence of resistance. Reprinted with permission from [89]. Copyright 2012 American Chemical Society.

with an U-shaped channel, showed on/off ratios of 1×10^5 [23]. The exact operation principle of this 300 nm wide and 20 µm long graphene wire is not yet fully understood, but it is suggested that quantum-mechanical quasi-bound states at the corners play a role.

A different issue concerning graphene transistors was raised by Wu *et al.* [91]: The typically used SiO_2 substrates cause additional scattering in the graphene due to the large trap density, decreasing transistor performance. By transferring the graphene (grown by CVD on copper) onto diamond-like carbon instead, and fabricating gate lengths of only 40 nm, a cut-off frequency of 155 Ghz was observed. It was confirmed that the cut-off frequency for graphene transistors scales with the inverse of the gate length.

2.5.3 Optical transducer

Optical transducers are yet another application of graphene, which is currently in the focus of intense research. Sun *et al.* [92] demonstrated infrared photodetectors based on CVD-grown graphene. They combined the graphene with PbS quantum dots to achieve maximum responsivity of $\sim 1 \times 10^6$ A/W at an incident power of 30 pW, several orders of magnitude higher than traditional quantum dot IR detectors.

A self-powered photodetector based on a Schottky structure between CdSe and graphene was demonstrated by Jin *et al.* [93] (this relies on the work function difference of these two materials). A photosensitivity of around 3.5×10^5 and recovery times of 179 µs were achieved.

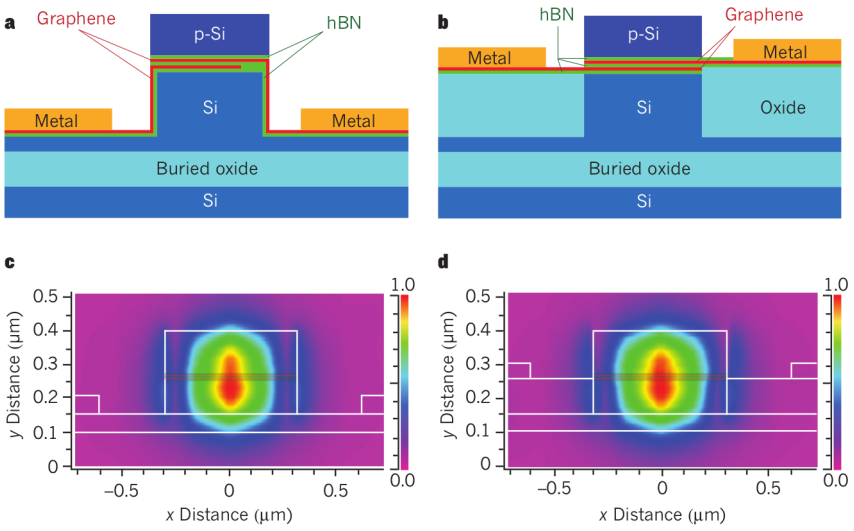


Figure 2.21: Proposed (a) ridge and (b) buried type optical modulator integrating graphene with silicon technology. The transverse electric mode profiles at a wavelength of 1.55 μm for the two types are shown in (c) and (d), respectively. Reproduced from [94].

Kim *et al.* [94] proposed the integration of graphene with silicon technology (rather than replacing silicon completely) to realize graphene-gated optical modulators. The two different fabrication approaches (ridge and buried type) are shown in Figure 2.21a and b, respectively, with the transverse electric mode profiles at a wavelength of 1.55 μm shown in Figure 2.21c and d. Suitability for 55 GHz modulation is predicted.

2.5.4 Superconductivity

The resistivity of graphene at room temperature of 1 μΩ cm is 35% less than that of copper. Despite this already extraordinary property, different routes are explored with the hope to modify graphene in such a way that superconductivity can be achieved at room temperature. Success would mean an immense advance of technology.

One method, proposed by Profeta *et al.* [95, 96], is phonon-mediated superconductivity. By depositing Li atoms onto monolayer graphene, as shown in Figure 2.22, the interlayer band can be modified so it crosses the Fermi level, enhancing the electron-phonon coupling, and inducing superconductivity.

A similar route was proposed by Nandkishore *et al.* [97]. The group found that, by carefully filling the π-band of graphene through calcium or potassium doping, chiral superconductivity could be realized.

2.5.5 Gas detection

In this Chapter we have seen that the band structure, and as a consequence the graphene resistance, depends on the material's vicinity. This can thus be exploited to use graphene for gas sensing.

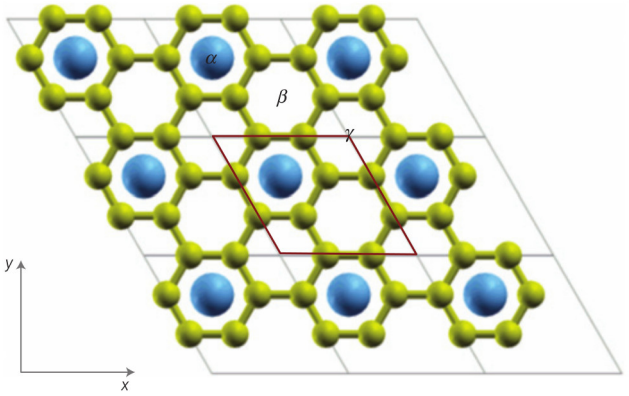


Figure 2.22: Crystal Structure of metal adatom covered graphene. The metal atoms (blue) sit on the hollow sites of the graphene. Reprinted by permission from Macmillan Publishers Ltd: Nature Physics [96], copyright 2012.

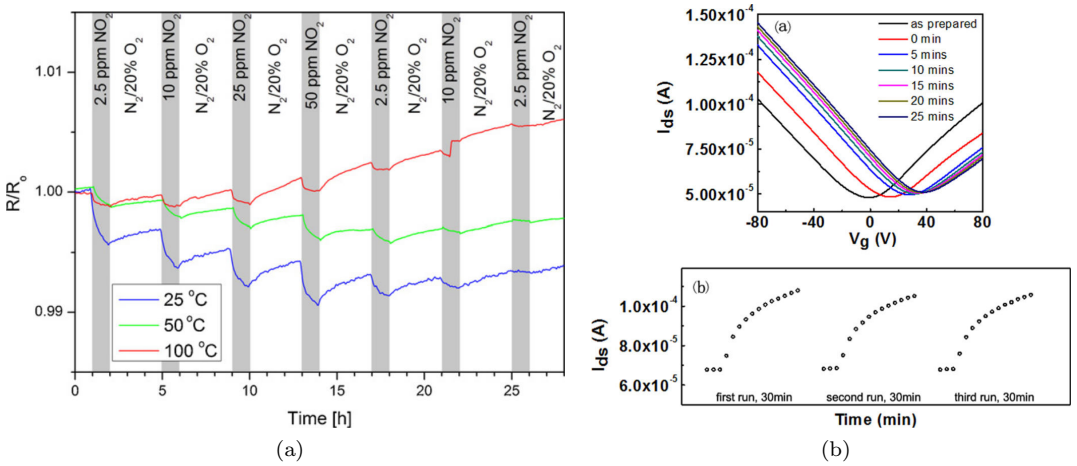


Figure 2.23: (a) Response of graphene on SiC to NO_2-gas exposure. Reproduced from [98]. (b) Response of monolayer graphene FET to SO_2-gas exposure. Reprinted with permission from [99]. Copyright 2012, American Institute of Physics.

Pearce *et al.* [98] have demonstrated an extremely sensitive NO_2 sensor based on monolayer graphene epitaxially grown on SiC. The sensing principle is a change of the graphene channel resistance in the presence of NO_2. The reported high sensitivity is due to the low carrier concentration stemming from the SiC substrate. In Figure 2.23a, a response diagram to different concentrations of NO_2 at different temperatures is shown.

A monolayer graphene FET, fabricated from CVD-grown graphene on copper and later transferred to SiO_2, was used by Ren *et al.* [99] for the detection of sulfur dioxide gas. It was demonstrated that the Dirac point shifts due to the temporary SO_2-induced p-doping (see Figure 2.23b). Furthermore, resistance reproducibly decreased by 60% at SO_2 concentrations of 50 ppm.

Other methods for sensing of CO, NH_3 and NO gas are zinc oxide (ZnO) decorated graphene sheets [100], inkjet-printed graphene oxide wireless gas sensors for NH_3 [101], and a sensor based on ozone treated graphene [102].

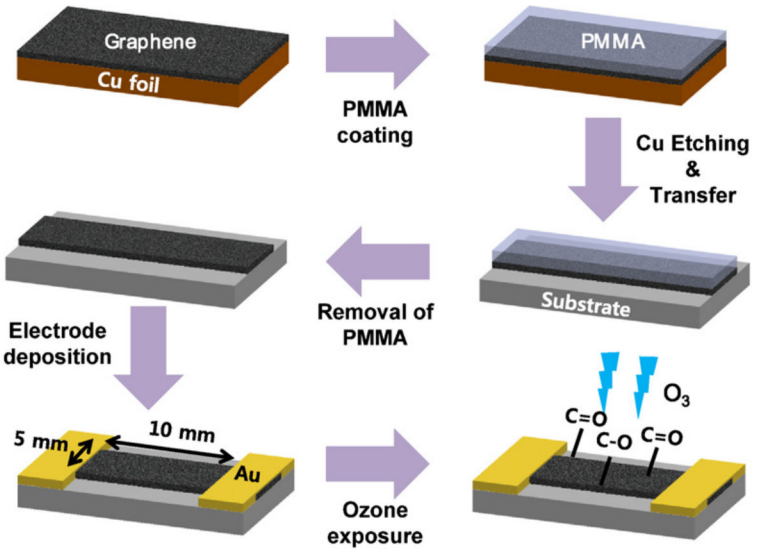


Figure 2.24: Schematic fabrication process chart for graphene-based gas sensor. Reproduced from [102].

2.6 Graphene device fabrication

In Section 2.4, several methods used to obtain graphene were discussed. Additionally, several graphene applications were introduced in Section 2.5. In all of these application cases, some additional processing was done, such as contacting or patterning. Therefore, in this Section, the different aspects of graphene device fabrication will be reviewed.

Device fabrication depends, to a certain extent, on the nature of the graphene: Is it a random exfoliated flake or a homogeneous, large area film? In the first mentioned cases it is necessary to fabricate individual structures that are adjusted from flake to flake, while large area films are more suitable for full-wafer, mask based processing similar to silicon technology.

In Figure 2.24, the fabrication process flow chart of a gas sensor, reported in Ref [102], is illustrated. The graphene film was grown by CVD and falls therefore under the category of large area growth. The next steps are (i) graphene transfer onto an insulating substrate (this process has been explained in Section 2.4.3 on page 17 and is shown in Figure 2.13c), (ii) Au contact deposition and (iii) exposure to ozone.

Three different graphene transistor fabrication approaches are illustrated in Figure 2.25 [19]. The first one requires only deposition of source and drain contacts (identical to the device shown in Figure 2.24). The middle and right device require additionally a top gate and gate electrode deposition.

An SEM cross section of a graphene transistor reported by Wu *et al.* [91] is shown in Figure 2.26b. The schematic 3D view of this device is shown Figure 2.26a. The Al_2O_3 gate insulator was deposited by ALD, followed by the top gate deposition. The top view of the device is shown in Figure 2.26c.

Due to the various device types and shapes, as shown with the examples above, it is difficult to categorize full fabrication processes. Instead, the different aspects of

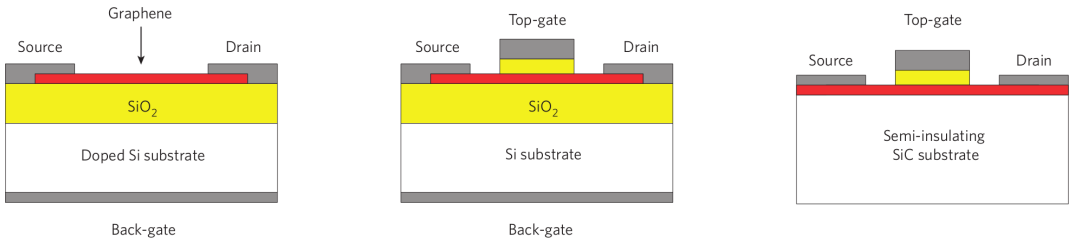
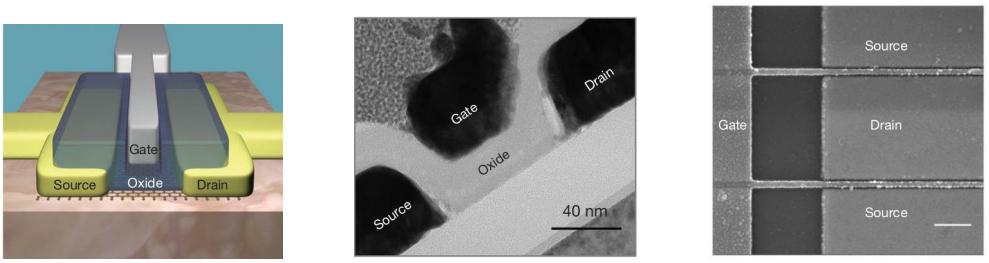


Figure 2.25: Graphene transistor fabrication approaches. Left: source and drain contacts are deposited on top, and the highly doped substrate is sued as back gate. Middle: same as left, but additionally a top gate is fabricated. Right: for graphene epitaxially grown on SiC, source/drain/gate are fabricated on top. Reproduced from [19].



(a) (b) (c)

Figure 2.26: Graphene transistor fabrication approach. (a) Schematic 3D model of transistor. (b) SEM micrographs showing cross section and (c) top view of fabricated device. Reproduced from [91].

graphene device fabrication are discussed separately, namely patterning, contacting, insulator deposition on top of graphene, suspending, and finally nanowire formation.

2.6.1 Patterning graphene

Graphene is readily etched by O_2 plasma etching, and this can thus be used, together with a masking material, to pattern graphene. The masking can be achieved by resist patterned by optical lithography (this work, for example fabrication Step 2 on page 74), e-beam resist or nano-imprint lithography (NIL) [103].

A very slow, and thus controllable, gas phase chemical etching process with etch rates of less than 1 nm/min was developed by Wang *et al.* [104]. By patterning e-beam resist or e-beam lithographically patterned aluminum, narrow graphene ribbons with widths down to 20 nm were achieved. The width was then further reduced by the gas phase etching, and 5 nm wide ribbons were achieved.

An etching method devised by Campos *et al.* [105] allows cutting of graphene with well-defined crystallographic edges. The principle is shown in Figure 2.27. Nickel nanoparticles are formed from $NiCl_2$ solution at 1000 °C which eat their way through the graphene, converting it to methane gas. There is no direct control over the cut location and direction, but cuts in monolayer graphene are not crossing, leading to nanoribbons with widths below 10 nm.

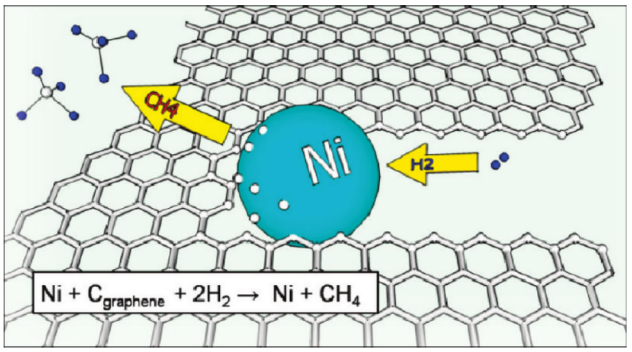


Figure 2.27: Illustration of graphene cutting method using Ni nanoparticle. The nanoparticle converts carbon into methane. Reprinted with permission from [105]. Copyright 2009 American Chemical Society.

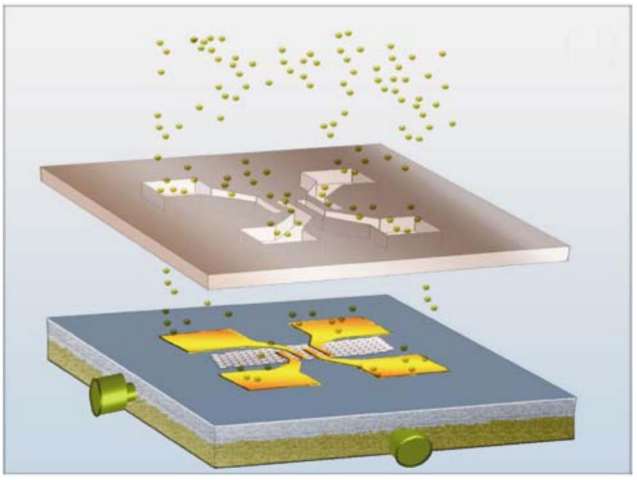


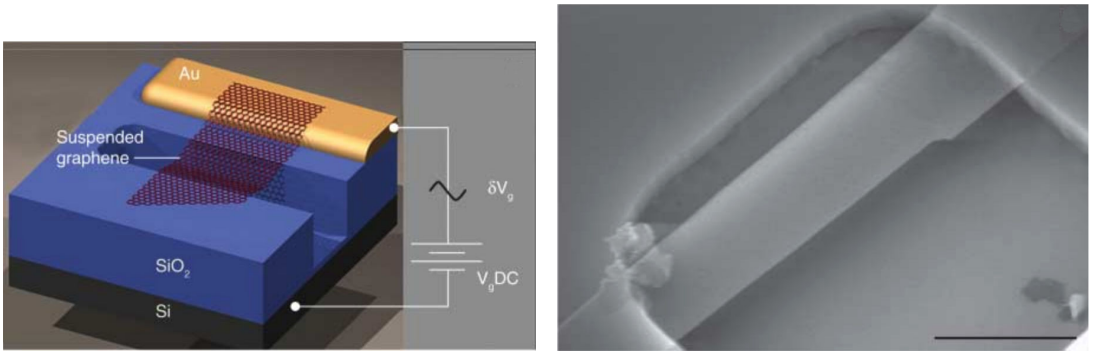
Figure 2.28: Schematic illustration of resist-free graphene contacting by metal evaporation through a shadow mask. Reproduced from [108].

Finally, graphene can be accurately cut by focused helium ion beams [11]. Due to the low sputter volume and small beam diameter, feature sizes in the sub-20 nm regime were demonstrated.

2.6.2 Contacting graphene

The most common method for electrical contacting of graphene is electron-beam evaporation of metal with consecutive lift-off. The lift-off resist is either patterned by normal optical lithography (this work, for example fabrication Step 5 on page 75) or e-beam lithography [90, 106, 107].

An alternative route, that avoids the use of polymer resists and has thus potential for higher carrier mobility, is the use of a shadow mask [108]. The pattern is pre-etched into a thinned silicon wafer, which is then positioned above the graphene sample during electron-beam evaporation. This process is schematically illustrated in Figure 2.28. The alignment can be challenging, but the reported carrier mobility of $120\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ from devices fabricated using this technique seems worth the effort.



(a) (b)

Figure 2.29: (a) 3D schematics of graphene resonator. (b) SEM micrograph showing fabricated resonator. (a+b) from [110]. Reprinted with permission from AAAS.

2.6.3 Dielectric deposition on top of graphene

For graphene structures with top gates (compare Figure 2.25 and Figure 2.25), a gate dielectric is required. The material to be used for this application has to be easily patterned on top of graphene, and should have sufficient adhesion to graphene to ensure long-time stability.

Materials found in literature are ALD-deposited Al_2O_3 [69, 109] and ALD-deposited HfO_2 on top of a polymer [26]. These ALD processes are very conformal and allow accurate thickness control.

The device schematically shown in Figure 2.20A comprises graphene oxide as dielectric [89]. Thus, an all-graphene based thin film transistor is possible.

2.6.4 Suspending graphene

The electronic properties of graphene deteriorate when being in contact with other materials such as SiO_2, thus steps were proposed to use other support materials instead [91]. A different possibility of improving graphene performance is to suspend it. Such suspended graphene has been used to obtain the fine structure constant and transparency [45], membranes were used to demonstrate that graphene is impermeable to gas [42], the thermal conductivity could be determined, as explained in Section 2.2.2 on page 9, as well as the mechanical strength (Section 2.2.1 on page 9). To suspend graphene, several methods are available depending on the graphene.

Exfoliation is a relatively simple method. Instead of exfoliation on top of flat SiO_2, a perforated substrate is used and by chance some of the graphene flakes will be suspended. A structure fabricated in this way is shown in Figure 2.29a and b [110].

A different method, used by Bolotin *et al.* [106], is to use buffered HF etching and critical point drying to etch the underlying SiO_2. The previously deposited Au electrodes act as etch mask. A similar approach was chosen by Shivaraman *et al.* [41]. To suspend graphene epitaxially grown on SiC, a photoelectrochemical etching procedure (aqueous potassium hydroxide solution together with UV illumination) was used. Again, Au

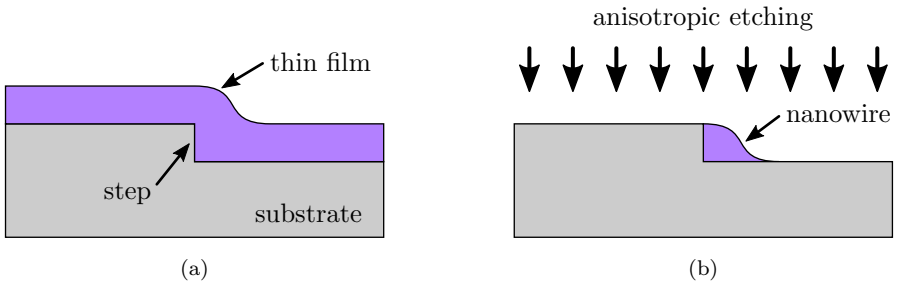


Figure 2.30: Schematic illustration of nanowire formation process. (a) A thin film is deposited on top of a sharp step, resulting in a larger vertical thickness at the step. (b) Nanowire is formed at step during anisotropic dry etching.

electrodes acted as etch mask. The same etching chemistry was used by Butz *et al.* [111] to etch through the SiC substrate from the back after graphene growth, thus fabricating membranes with diameter exceeding 10 µm.

2.6.5 Nanowire formation

Nanowires have a very large surface to volume ratio, offering very high conductance changes depending on the surface properties. This can be used for various sensing applications, such as gas sensing reviewed in Section 2.5.5 on page 26. By functionalization, sensitivity toward specific molecules or biological entities can be increased. To achieve fabrication of nanowires with dimensions far below the resolution limit of optical lithography, a novel technique had been developed [112, 113]. It does not require e-beam lithography and is thus potentially usable for disposable devices. The principle of this fabrication is illustrated in Figure 2.30. After deposition of the thin film over a predefined surface step, the larger vertical thickness at that step is exploited during anisotropic dry etching to form the nanowire. This fabrication process is applicable for thicker films, not for fewlayer graphene.

2.7 Graphene device prototyping by focused ion beam (FIB)

In the previous Section, a number of fabrication techniques applicable to graphene were reviewed. One method deliberately not mentioned was focused gallium ion beam milling and deposition. This was done for two reasons: Firstly, although FIB is a widely available and well established technology, very few work on mono- and bilayer graphene had been reported so far. Secondly, the author developed a highly-accurate prototyping technique in this PhD work based on FIB milling, FIB-assisted deposition and e-beam-assisted deposition (using scanning electron microscopy (SEM)). Therefore a more thorough and complete introduction is necessary to allow the reader to put the achievements presented in Chapter 5 on page 103 into context. This Section contains an explanation of FIB technology first, followed by a comparison with other fabrication methods, and finally a review of reported graphene structures fabricated by FIB.

2.7.1 FIB milling and deposition

Gallium ions (Ga^+) can be extracted from a liquid metal ion source, accelerated and focused using electrostatic lenses to form beams with diameters below 10 nm [114]. This beam, very similar to SEM technology, is scanned over the sample surface, while the synchronized secondary electron (SE) signal can be used to construct a raster image. In some special cases, the contrast of FIB imaging can be better than SEM due to the different detection mechanism involved (higher secondary electron yield). The high energy of the FIB beam can also be used for precise material removal (ion milling). Depths of several µm with a resolution below 35 nm can be achieved in conducting samples [115, 116], making this a widely used technology for maskless nanofabrication applications and rapid prototyping. Furthermore, cross sections can be prepared for the analysis of material stacks, or transmission electron microscopy (TEM) lamellae can be extracted. Metal, carbon or insulator films can be locally deposited through the use of a gas injection system (GIS). The GIS nozzle, positioned close to the surface, is used to inject special precursor gases which contain the desired species, surrounded by precursors that keep it volatile (e.g. $W(CO)_6$ for tungsten). After attaching to the surface, the bombardment with electrons or Ga^+ ions dissociates the precursor, resulting in the localized deposition of the desired species. However, for FIB this requires a very careful adjustment of the beam current, dwell time and spacing to achieve good deposition while minimizing the simultaneously competing milling process.

One limitation of FIB technology is related to the ion optics. As with any electron-optical system, it is very challenging to get a small beam diameter with high current. Effects such as astigmatism, beam divergence and depth of focus have to be controlled. The charged nature of the ions will additionally increase the convergence. Imaging resolutions of 5 nm for a beam current of 1 pA have been reported, with the limiting factor found to be the simultaneous milling [114, 117]. FIB beams have a Gaussian profile when measured across the beam diameter, which causes low ion exposure to areas even several beam diameters away.

Nanosized structures would be immediately damaged if Ga^+-ions were used for observation, making it necessary to integrate the FIB with an SEM. In this work a *Zeiss NVision 40 CrossBeam®* workstation is used. It combines a high-resolution *Gemini* SEM column with a FIB gun, aligned at an angle of 54 °. A schematic illustration of the gun configuration is shown in Figure 2.31a, and a picture taken with the camera inside the chamber is shown in Figure 2.31b. For FIB milling, the sample is positioned perpendicular to the FIB beam. In order to allow simultaneous observation of the sample using the SEM, the sample is placed in the point where the electron and focused ion beam coincide (called coincidental point), as indicated in Figure 2.31a. The GIS nozzle can be inserted on demand to a distance of 200-300 µm from the sample surface.

Once the beams are adjusted to the coincidental point, FIB milling can, in theory, be accurately directed based on SEM observation. Practice shows, however, that a time stable (> 1h) and accurate (sub-µm) coincidental alignment of SEM and FIB beam is

very challenging. The two main reasons are: (i) Due to the geometric configuration of the beams and the sample, temperature induced expansion or contraction will cause a misalignment of the coincidental point and (ii) possible electrical charging of the sample surface will have different effects on the electron and the FIB beam, respectively, making it necessary to constantly re-adjust the beam alignment. Therefore, samples are normally imaged by FIB if very accurate positioning is required. For the application of FIB to the prototyping of graphene devices, this would result in some serious implications. Any imaging of graphene using FIB, no matter how low a current is used, will introduce Ga^+-ion induced damage. Therefore, an approach is necessary to maintain high accuracy while avoiding any FIB imaging of the graphene at any stage. The approach chosen in this work is the utilization of an alignment marker system, which will be introduced in detail later in this Chapter.

The FIB/SEM microscope is equipped with a *Raith ELPHY Quantum* lithography attachment. This is in essence a pattern generator and an advanced lithography software, which can be used for accurate beam control (electron or ion beam), based on pattern files. It features accurate beam calibration procedures and alignment methods, and allows multiple exposures at predefined locations. The beam repositioning frequency is limited to 2.5 MHz, resulting in a minimum dwell time of 0.4 µs.

2.7.2 Comparison of prototyping methods for graphene

FIB technology is not the only method used for graphene device prototyping. The two other methods are e-beam lithography with consecutive metal lift-off and scanning helium ion microscopy (HIM). Both of these methods have been mentioned briefly before, in particular in Section 2.6.1 and Section 2.6.2 on pages 29 and 30, respectively.

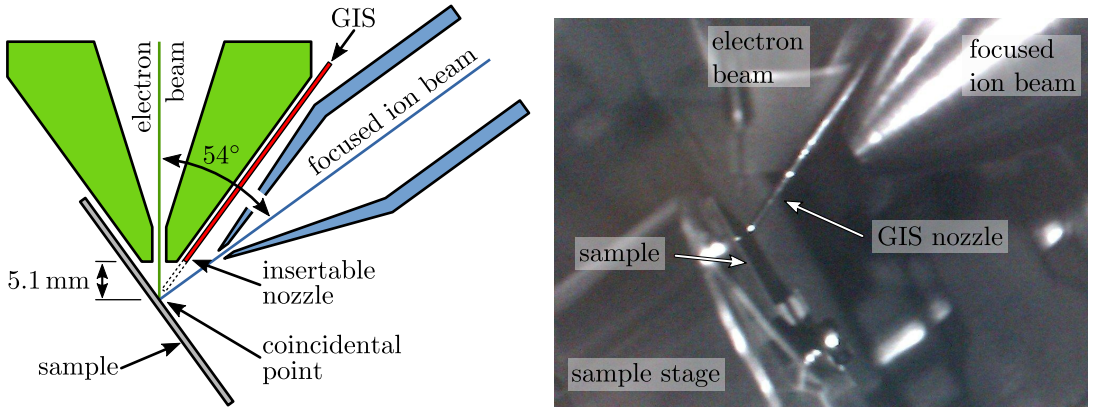


Figure 2.31: (a) Schematic illustration of electron and focused ion beam configuration of *Zeiss NVision 40* microscope. During FIB milling the sample is positioned in the coincidental point perpendicular to the FIB beam. The GIS nozzle can be inserted on demand and used for process gas introduction. (b) Photograph taken by chamber scope showing the gun configuration and the inserted GIS nozzle.

In e-beam lithography, an electron sensitive polymer film is spun onto the sample and patterned by localized exposure to electrons. After removal of the exposed polymer in a development step, a metal film is evaporated and consecutively patterned by lift-off. The resist mask is alternatively used for other processes. The general work flow is to prepare samples with alignment structures, exfoliate or otherwise transfer graphene onto these samples and design custom mask files based on the position and orientation of these graphene flakes relative to the alignment markers. This process is very well established, however, it has some inherent limitations. Polymer based resist used in electron beam lithography is very resilient, and it can be very difficult to remove all resist residues after the process. Thus it is assumed that resist changes the electronic properties of the graphene. In contrast, FIB-technology allows complete device fabrication without the use of any polymer based resists. It has been reported that carbon atoms can be removed from the graphene crystal by high energy electrons ($> 140\,\mathrm{kV}$) [118]. However, this is not an established procedure and outside the acceleration voltage range of commercial e-beam lithography systems.

Scanning helium ion microscopy is a technology which was established very recently, and is not yet widely deployed. The operation principle is the same as FIB, except for the different ion species used. While FIB uses heavy Ga^+-ions, HIM uses lighter He^+-ions. By doing so, a much higher imaging and milling resolution can be achieved than with SEM or FIB. This is due to the higher brightness of the ion source which allows the beam to be focused to a smaller spot, and the smaller excitation volume (a resolution of 0.24 nm has been reported [119]). Ga^+-ions, in contrast, have a very large excitation or sputter volume. Helium ion microscopes can be fitted with gas injection systems and thus used for imaging, milling and deposition. The HIM systems commercially available today are, in contrast to FIB, not integrated with an SEM. And although the surface damage due to HIM imaging is much lower than FIB, it is assumed that some damage is introduced into the graphene crystal upon imaging. With FIB/SEM technology, on the other hand, ion exposure can be avoided by using the SEM to identify graphene and control the FIB milling. The second disadvantage of HIM is the small excitation/sputter volume of He^+-ions, resulting in low deposition and milling rates. The problem of the low rates has been recently tackled by *Zeiss*, manufacturer of the *Orion*® microscope, through the unveiling of the *Orion*® *NanoFab* [120]. It comprises a switchable ion source (helium and neon) and is integrated with a gallium ion beam.

The author believes that HIM will eventually replace FIB for graphene device fabrication. Nevertheless, the low-damage prototyping technique developed in this thesis will also be applicable to HIM, if fitted with an appropriate pattern generator and a non-destructive imaging capability.

2.7.3 Review of FIB-patterned graphene devices

FIB technology can be used in various ways for graphene-related work. A trench has been FIB-milled into a sputtered tungsten film and multilayer graphene (MLG) was exfoliated

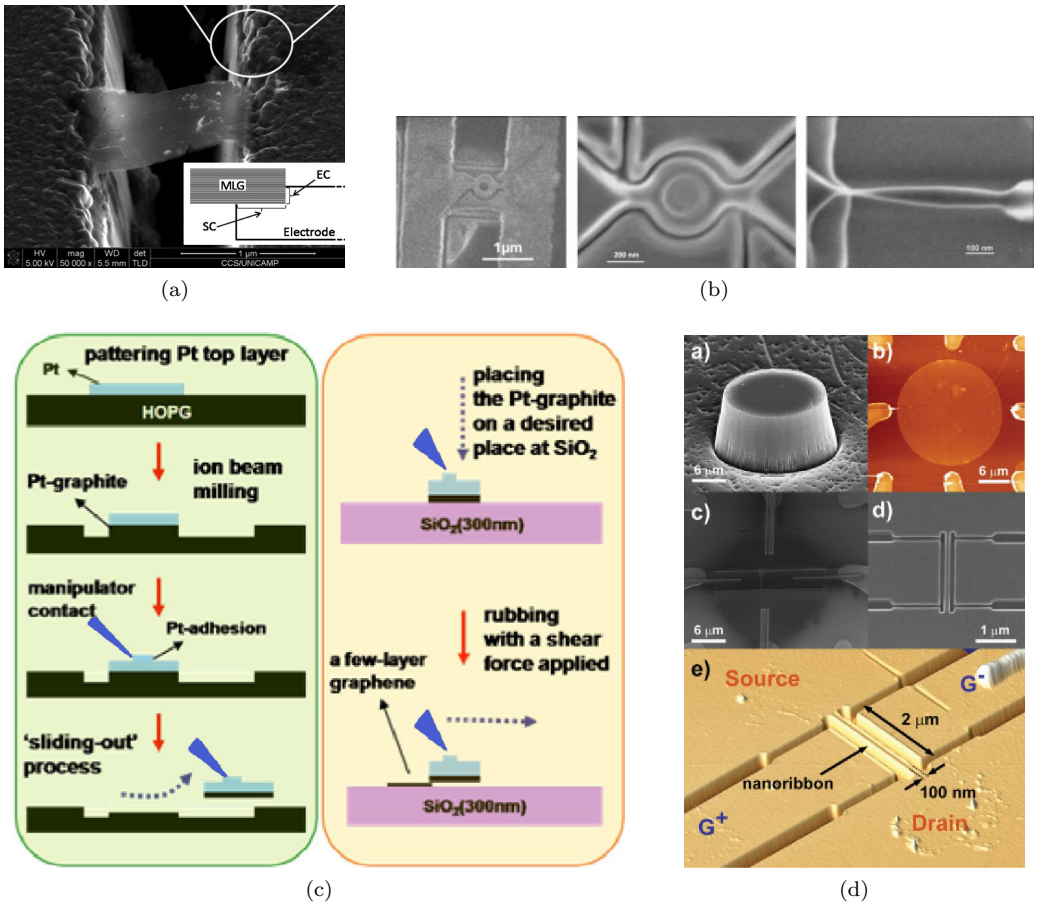


Figure 2.32: Review of FIB-fabricated graphene structures. (a) Graphene flake exfoliated across FIB-milled trench. Reprinted with permission from [121]. Copyright 2010, American Institute of Physics. (b) High precision milling of suspended graphene. Reproduced from [122]. (c) Localized graphene exfoliation using micro manipulator. Reproduced from [123]. (d) Side-gated graphene channel fabricated using FIB milling and platinum deposition. Reproduced from [124].

on top of a trench to obtain suspended graphene [121]. After annealing at 850 ° for 1 h, an ohmic contact was formed to the tungsten electrodes. A SEM micrograph of the bridging graphene flake is shown in Figure 2.32a. In a different work, in-situ micro manipulators were used to perform highly localized graphene exfoliation [123]. The process flow is illustrated in Figure 2.32c: using FIB induced deposition, the manipulator was glued to a larger piece of HOPG. The HOPG around the contact point was then FIB-milled and the extraction achieved. Subsequently, few-layer graphene was locally exfoliated using this "micro-stamp" technique.

In the two previous examples, FIB was not directly used to pattern graphene, but rather as a supporting tool. In contrast, Dayen *et al.* [124] used FIB milling as a primary tool. FIB-assisted platinum deposition was used to pattern interconnects between an exfoliated monolayer graphene disk on SiO_2 and larger metal pads (shown in Figure 2.32d). In a second step, accurate milling was used to form a 100 nm wide channel region with two side gates. It is reported that after the milling an amorphous zone is

observed around the 100 nm trenches, affecting the graphene quality in those areas. To avoid this effect, Lucot *et al.* [122] patterned graphene, suspended over 200 nm thick gold electrodes, with a custom built Ga^+ beam. A resolution of 10 nm was reported as illustrated in Figure 2.32b. This high resolution was achieved through the suspension of the graphene, thus eliminating back-scattering effects and ion implantation. Due to the high conductivity of graphene no detrimental charging occurred.

2.8 Summary

In this Chapter, different aspects of graphene were reviewed. The first Section contained an introduction into the band structure and electronic properties of graphene. The effect of graphene layer stacking, as well as techniques used to open a bandgap in this otherwise zero-bandgap material, were reviewed. In Section 2.2, mechanical strength, thermal conductivity, surface-to-mass ratio and optical properties were discussed. Two techniques to detect and characterize graphene were then discussed in Section 2.3, namely optical contrast method and Raman spectroscopy. In Section 2.4, the four prevalent methods used to obtain graphene for planar applications were reviewed, with a focus on the question whether these methods are suitable for large area deposition. These methods are mechanical exfoliation from HOPG, epitaxial growth on SiC, CVD growth on metal substrates and various plasma enhanced processes. The advantages and disadvantages of each method were discussed (see also Table 2.1), and it was concluded that there is still demand for further research before graphene can become a viable competitor for silicon. In Sections 2.5 and 2.6 practical applications of graphene (aside from being an extraordinary material for the study of fundamental physical principles) and graphene device fabrication aspects were reviewed. In the last Section 2.7 of this Chapter, the principle of focused ion beam technology was explained, and its application to graphene device prototyping was reviewed.

Chapter 3

Large area metal-free PECVD deposition of graphene-like films

This PhD is to develop a large area PECVD deposition technique for graphene. Parts of the results in this Chapter have been presented at the *Graphene2012* conference in Brussels, Belgium [3].

For graphene to have a commercial research and development appeal, exfoliated graphene is not suitable. The main reasons are the random nature of size and location, and the fact that graphene exfoliation does not scale. In Section 2.4 on page 14, several methods to obtain graphene were discussed, and it was concluded that PECVD is a promising candidate to achieve large area, metal-free deposition directly on insulating substrates.

In this Chapter, the development of a novel PECVD deposition process for nanocrystalline graphene is described. Starting with preliminary experiments on nickel films, the discovery and characterization of films deposited directly on SiO_2 are described in detail. Finally, the obtained films are evaluated for their suitability for transparent electrode applications.

3.1 PECVD deposition of carbon films

3.1.1 Reaction chemistry and chamber

For plasma-enhanced carbon deposition, a gaseous source material is required. This carbon source is then introduced into a plasma reactor and ionized through an applied electrical field typically at an RF frequency of 13.56 MHz. The two most common gases used as a carbon source are acetylene (C_2H_2, also called ethyne) and methane (CH_4). In this work only methane was available.

During ionization, the methane is decomposed into different hydrocarbons:

$$CH_4 \xrightarrow{\text{RF-plasma}} CH_x,\ C_2H_y,\ C_3H_z,\ H.$$

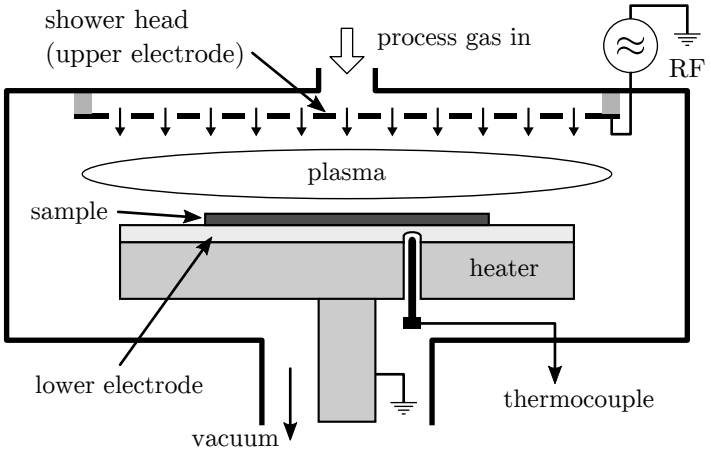


Figure 3.1: Schematic illustration of PECVD tool chamber.The process gas is introduced through the shower head into the evacuated chamber, and an applied RF voltage is used to generate a plasma between the upper and lower electrode. The sample or wafer, sitting on the heated lower electrode, is exposed to the plasma. Substrate temperature is controlled by an embedded thermocouple.

These volatile hydrocarbons then form atomic bonds with other atoms. Finally, hydrogen is desorbed and the carbon atoms are able to enter a bond with another hydrocarbon.

The deposition speed and the morphology of the final deposit greatly depend on the process conditions. The pressure of the plasma chamber influences the mean free path of molecules before collision with other molecules. Thus by reducing the pressure, molecules with higher kinetic energy are obtained, resulting in a better atomic bond when colliding with the surface. On the down side, reduced pressure reduces the deposition rate due to the lower concentration of hydrocarbons. The second important parameter is the target surface temperature. At high temperatures, hydrocarbons that have formed weaker bonds are more likely to be consecutively desorbed, resulting in a denser film but a lower deposition rate.

To allow the accurate control of all these parameters and ensure uniform plasma conditions (and thus deposition rates), PECVD chambers such as the one schematically illustrated in Figure 3.1 are used. This particular chamber has a parallel plate configuration. The process gas, which is controlled by mass flow controllers (MFCs) and can be a mix of more than one gas, is introduced into the evacuated chamber through small holes in the so called shower head. This ensures a uniform flow and concentration distribution over the deposition area. The shower head acts as the upper electrode, and is used together with the grounded sample stage to generate the required RF field. The plasma is thus localized between the upper and lower electrode, with the wafer sitting on the lower electrode. Situated underneath the lower electrode is an electrical heating element and a thermocouple, which is used to control the temperature of the sample.

In this work, a *Nanofab 1000 Agile* from *Oxford Instruments* [125] is used. It enables processing of wafer with a diameter of up to 200 mm, and the lower electrode (made of graphite) can be heated to up to 1000 °C. The chamber pressure is accurately controlled

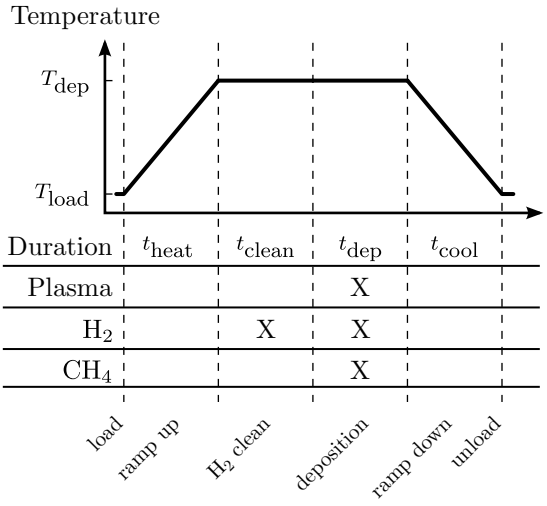


Figure 3.2: Illustration of PECVD process of nanocrystalline graphite. The wafer is loaded at T_{load} and heated to the deposition temperature T_{dep}. The sample is then hydrogen cleaned before the deposition is performed. Finally, the sample is cooled to T_{load} for unloading.

by a butterfly valve. A loading mechanism comprising a separately evacuated load lock and a stainless steel loading arm provide for high-throughput processing. The loading and unloading process is restricted to temperatures below 700 °C.

The sample temperature is measured from within the lower electrode assembly and can deviate from the real temperature on the top surface of the processed substrate depending on process conditions. This difference ΔT can be more than 100 °C at a temperature of 900 °C in vacuum ($\leq$ 1 mT). In this thesis, all deposition temperatures reported are the set value.

3.1.2 PECVD process

A relatively simple deposition process is used in this work, as illustrated in Figure 3.2. After loading the wafer into the chamber at the loading temperature T_{load}, the temperature is ramped up to the deposition temperature T_{dep} within the heat up time t_{heat}. As mentioned earlier, T_{load} has to be less than 700 °C due to machine limitations. In case T_{dep} is below 700 °C, the ramp up and ramp down steps are omitted. Next, hydrogen pre-cleaning is performed at the deposition temperature for the duration t_{clean}. Initially hydrogen plasma was used, but this led to pinhole formation in the used nickel films, as will be explained later. Hydrogen cleaning is commonly used, for example for metal films before CVD growth [67], cleaning of silicon carbide [126] or silicon [127], and is therefore used here as well. In the next step, the process gases (hydrogen and methane) are introduced into the chamber and the plasma is generated, resulting in deposition for the duration t_{dep}. After the deposition, the process gas supply and plasma are shut off, immediately halting the deposition, and the table temperature is again ramped down to the loading temperature. The ramp up and ramp down durations t_{heat} and t_{cool},

respectively, are identical. The maximum heating and cooling rates are limited to 15 or 30 °C/s, depending on temperature.

3.1.3 Deposition on Ni film

The initial strategy chosen in this work was to evaluate the feasibility of using PECVD to reproduce CVD growth on metal substrates, similar to the method by Baraton *et al.* [78] briefly mentioned in Section 2.4.4 on page 19. Nickel was chosen as catalyst layer since a large number of results had been published before (see Section 2.4.3 on page 17). Copper and iron were considered as well, however, copper is known to have high solubility in silicon and was therefore not available in the Southampton Nanofabrication Centre, as well as iron, which easily oxidizes to rust and is therefore difficult to handle.

A 150 mm silicon wafer (wafer specifications see Appendix C.1 on page 145) with 245 nm of wet thermal oxide (1000 °C, 48 min) was coated with 100 nm Ni by e-beam evaporation. This wafer was subsequently diced into $10 \times 10\,\mathrm{mm}^2$ samples. Since this process development could not rely on previous parameters, it was expected that a large number of experiments would have to be carried out. By using small samples, valuable machine time could be saved. For loading purposes, a 150 mm diameter molybdenum disc with a thickness of less than 250 µm was used. The molybdenum disc is used because it has a better thermal conductivity than a silicon handle wafer.

The PECVD deposition on nickel is schematically illustrated in Figure 3.3. After (1) nickel evaporation on the thermal oxide, it is expected that (2) graphene or graphene-like films will form on the surface through the plasma process. The formation process for CVD growth relies on the carbon solving in the nickel and carbon segregation upon cooling [67, 68, 128]. This formation has been shown to strongly depend on the cooling rate that is in the range of 5-20 °C/s [128, 129]. The heating table of the *Nanofab*, however, is not able to achieve such rates due to the large thermal mass. Therefore, an optional rapid thermal annealing (RTA) step (see Step 3 in Figure 3.3) was considered.

3.1.4 Initial evaluation of PECVD deposition and hydrogen cleaning

An initial set of nine experiments was performed on Ni samples. All except one were run at 500 °C. The first two runs involved 2 min hydrogen plasma cleaning (200 sccm, 1000 mT) followed by 5 min carbon deposition (40 sccm CH_4, 50 sccm H_2, 1500 mT). After unloading the samples from the *Nanofab*, spots were visible on all samples. These were identified as pinholes with diameter of several hundred microns. Raman spectroscopy was used to confirm carbon deposition on the nickel surface (weak D and G peak visible). However, before continuing to investigate the carbon deposit, it was decided that the pinhole formation on the nickel surface has to be investigated.

For this purpose, three samples were cleaned with different conditions as listed below plus one sample annealed without gas for reference. The results are:

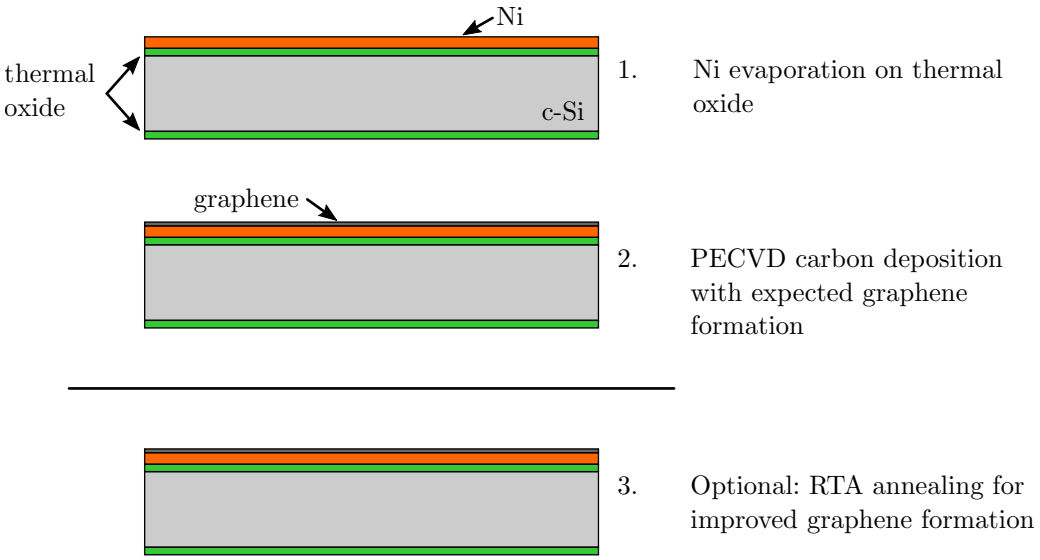


Figure 3.3: Schematic illustration of PECVD-assisted graphene growth on nickel. After electron beam evaporation of 100 nm Ni, PECVD carbon deposition is performed. In case the deposited carbon does not form graphene, an optional RTA annealing is performed.

1. Annealing without gas: 2 min, 500 °C, 0 mT
   ⇒ *Nickel surface undamaged*

2. H_2 cleaning: 2 min, 500 °C, 1000 mT, 200 sccm, 100 W LF power (50 kHz)
   ⇒ *High pinhole density on surface*

3. H_2 cleaning: 2 min, 500 °C, 1750 mT, 200 sccm, no plasma
   ⇒ *Low pinhole density on surface*

4. Ammonia (NH_3) cleaning: 2 min, 500 °C, 3000 mT, 200 sccm, no plasma
   ⇒ *High pinhole density on surface*

The result of experiment 1 (undamaged nickel surface) shows that the damage was indeed due to hydrogen. The other three experiments with hydrogen or ammonia show significant pinhole formation. Thus it became apparent that any hydrogen source at temperatures of 500 °C (with or without plasma activation) leads to pinhole formation in the nickel surface. Nickel is generally not etched by hydrogen and it is thus assumed that contaminants in the nickel film, possibly introduced during e-beam evaporation, are responsible for the observed pinhole formation. It was thus concluded that detailed investigation of the hydrogen cleaning process on the available nickel samples is of little benefit, and pure H_2 cleaning without plasma (compare experiment 3) was established as cleaning procedure for all further experiments.

Following this cleaning investigation, three more PECVD carbon depositions were carried out (four samples each):

1. Carbon deposition at 500 °C: cleaning 2 min, 1750 mT, 200 sccm H_2; deposition 5 min, 337 mT, 100 sccm CH_4, 8 sccm H_2
   ⇒ *Weak but dense pinholes, no visible carbon deposition*

2. Carbon deposition 500 °C: cleaning 2 min, 1750 mT, 200 sccm H_2; deposition 5 min, 337 mT, 100 sccm CH_4, 8 sccm NH_3
   ⇒ *Very weak pinhole formation, no visible carbon deposition*

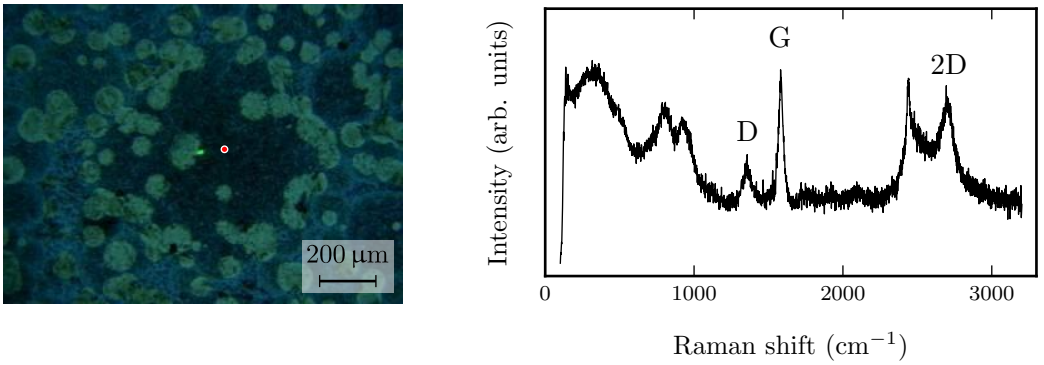
3. Carbon deposition 900 °C: cleaning 2 min, 1840 mT, 200 sccm H_2; deposition 5 min, 450 mT, 100 sccm CH_4, 8 sccm NH_3
   ⇒ *Nickel surface dark after deposition, visible surface damage*

Raman spectroscopy was then used to investigate the films, revealing very weak D and G peaks. It was decided to anneal samples from each of these runs using a *Jipelec Jetfirst 200C* rapid thermal annealer at 950 °C for 5 and 1 min, respectively. The cooling rate from 950 °C to below 600 °C was 25 °C/s. After investigating the annealed samples by Raman spectroscopy (inconclusive results), it became apparent that a more systematic approach was necessary for the investigation of cooling rates.

3.1.4.1 Investigation of cooling rates for graphene formation with amorphous carbon

The deposition process development explained in this chapter contains many variables for which no previous results were available. These can be divided into three main groups: (i) Sample preparation, (ii) PECVD carbon deposition and (iii) RTA annealing. The sample preparation should have a small influence, but the PECVD carbon deposition relies on parameters such as gas composition, gas flow rates, temperature, duration, pressure and plasma. The parameters for RTA annealing are heating/cooling rates, annealing temperature, duration and whether the anneal is performed in vacuum. It was thus decided to first investigate the RTA conditions. To do this, carbon films were deposited using an *Emitech SC7640* carbon coater (used for SEM sample coating). Ni samples with carbon thicknesses of 4.7, 52, 55 and 70 nm (measured by ellipsometry) were consecutively annealed by RTA.

A microscope picture of sample `Run2_26` is shown in Figure 3.4a. This sample with a 52 nm thick amorphous carbon film was annealed at 950 °C for 1 min in an argon atmosphere and cooled down at a rate of 15 °C/s. The surface is non-uniform with darker areas in the center and brighter, round features randomly distributed. The Raman spectrum acquired in the indicated location (red dot) is shown in Figure 3.4b (*Renishaw inVia* Raman spectrometer, excitation wavelength 532 nm, ×20 lens). It exhibits distinct D, G and 2D peaks with the 2D peak intensity larger than the D peak intensity, which indicates few layer graphene with slight crystal defects. The peak at around 2500 cm^{-1} might be the so called G* which appears due to double resonance Raman scattering processes [51]. However, the intensity of this peak in relation to the D, G and 2D peaks was found to be strongly dependent on the used optical lens.



(a) (b)

Figure 3.4: (a) Optical microscope image of Ni sample `Run2_26` after RTA annealing. (b) Raman spectrum acquired in the location indicated by red dot in (a).

Additionally, as will be shown later in this Chapter, this peak is visible even without any graphene films. It has been further confirmed that the peak is present in Raman spectra acquired on clean SiO_2. It is therefore concluded that this peak is a measurement artifact of the Raman spectrometer. The features at Raman shifts lower than 1000 cm^{-1} are due to the nickel film underneath the graphene.

Samples annealed with cooling rates of 15 °C/s and 25 °C/s had very similar Raman results. It was thus concluded that RTA annealing at 950 °C for 1 min and a cooling rate between 15 °C and 25 °C will yield graphene on nickel films with sufficient carbon supply. This is a very promising result and provides a reference for the process development using the *Nanofab*.

3.1.4.2 Experimental series

After experimentally obtaining RTA conditions that will yield graphene films on nickel, the focus was directed on the PECVD deposition using the *Nanofab*. For this purpose five runs were performed (`Run 16` to `Run 20`). The deposition conditions (see Table 3.1) are identical except for the deposition temperature, which is varied from 500 °C to 900 °C. The deposition duration t_{dep} was set to 15 min to ensure that any deposition that might occur can be reliably detected.

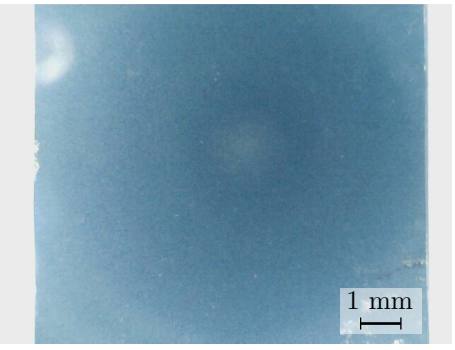
In each of these runs, four nickel samples and additionally four samples without nickel were processed. This was done out of curiosity to see if there would also be any effect on SiO_2 surfaces. After the deposition and before any additional RTA annealing, Raman spectroscopy was used to investigate these samples. The SiO_2 samples were very homogeneous while some of the nickel samples developed very rough surfaces. Images of nickel samples from `Run 17` to `Run 20` are shown in Figure 3.5. Raman spectra were taken in several locations on the samples using 532 nm excitation wavelength and ×20 lens, and the most distinct Raman spectrum for each sample is shown in Figure 3.6 on

Wafer	T_{dep} °C	t_{heat} min	t_{dep} min	t_{cool} min	$F[H_2]$ sccm	$F[CH_4]$ sccm
`Run 16`	500	15	15	15	75	60
`Run 17`	600	15	15	15	75	60
`Run 18`	700	15	15	15	75	60
`Run 19`	800	15	15	15	75	60
`Run 20`	900	15	15	15	75	60
`Run 22`	900	15	15	15	75	30
`Run 23`	900	15	15	15	100	15
`Run 26`	900	15	15	15	75	60

Table 3.1: Deposition conditions used for PECVD in `Run 16` to `Run 26`. See Figure 3.2 on page 41 for parameter explanation. Flow rates F are applied during the deposition step. Hydrogen flow during heat up and 10 min pre-clean is fixed at 100 sccm.

the left side. The Raman spectra taken on the SiO_2 samples (no nickel) are shown in Figure 3.6 on the right side.

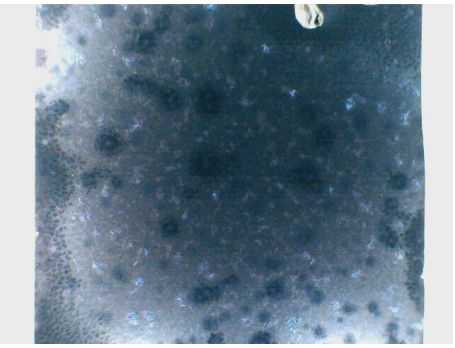
On the nickel samples, no distinct D and G peaks are visible below 700 °C deposition temperature. The sample from `Run 18`, however, has very distinct but broad D and G peaks and no indication of a 2D peak. This is characteristic for amorphous carbon



(a) `017-0_Ni`, 600 °C

(b) `018-0_Ni`, 700 °C

(c) `019-0_Ni`, 800 °C



(d) `020-0_Ni`, 900 °C

Figure 3.5: Optical images of Ni samples `017-0_Ni`, `018-0_Ni`, `019-0_Ni` and `020-0_Ni` after carbon PECVD.

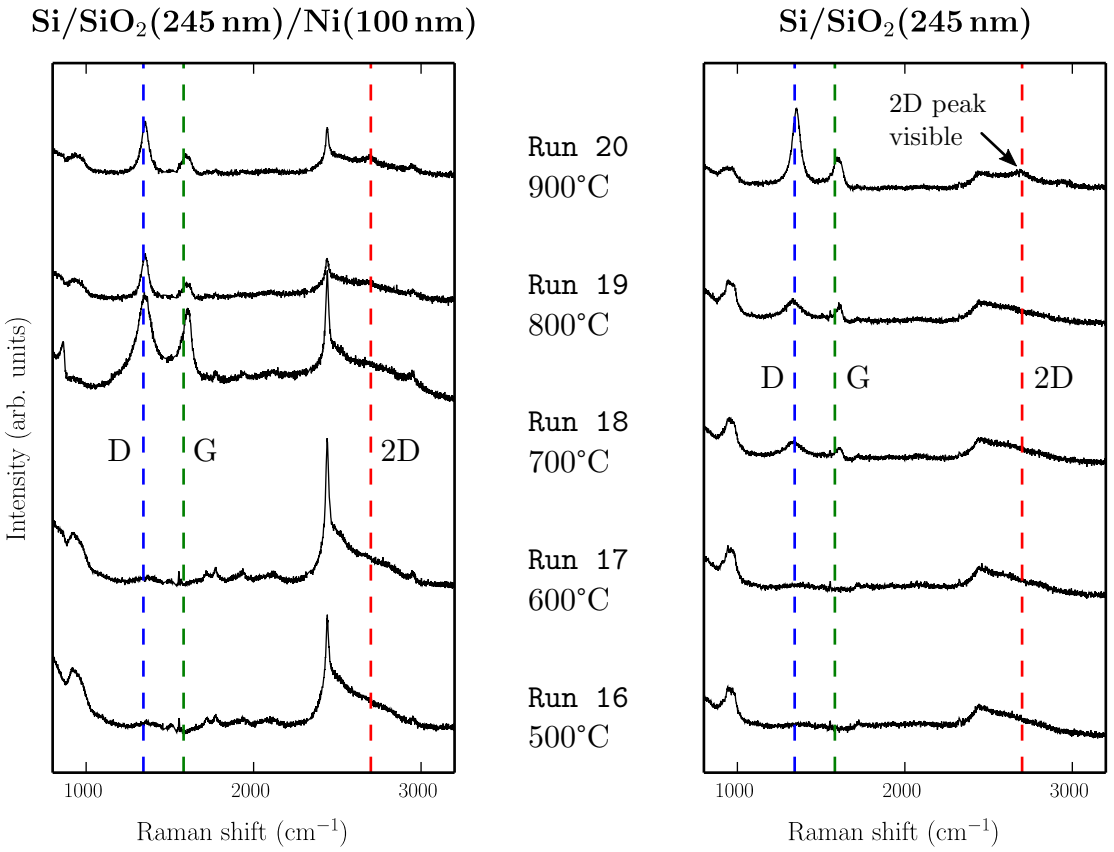


Figure 3.6: Raman spectra of films deposited by PECVD on nickel and SiO_2 between 500 °C and 900 °C. D, G and 2D peak formation on SiO_2 at 900 °C indicates disordered graphene formation.

[55, 130] and it appears that the plasma assisted decomposition of CH_4 starts between 600 °C and 700 °C. It should be also noted that the surface of the sample from `Run 18` is very homogeneous, as can be seen in Figure 3.5b, and the same Raman results are obtained independent of the location. This result stands out considerably from all the other deposition experiments performed on nickel which show D and G peak formation. The Raman spectra of the samples from `Run 19` and `20` have clearly defined 2D peaks, which are an indication for graphene formation. However, the D (disorder) peak is approximately double the intensity of the G peak suggesting that the films have a large crystal defect density. No further experiments were performed on the films deposited on nickel, as the focus of this work was drawn to other areas. The peaks visible at $\sim 2500\,\mathrm{cm}^{-1}$ are, as explained in Section 3.1.4.1 on page 44, measurement artifacts influenced by the used Raman optics.

In the author's opinion, the Raman spectra acquired on the SiO_2 samples are surprising. In line with the deposition results on nickel, D and G peaks appear at 700 °C and above. Additionally, a 2D peak is clearly visible for `Run 20`. This indicates that a graphene film, albeit with a large crystal defect density, was deposited directly on SiO_2 without the need of any metal catalyst.

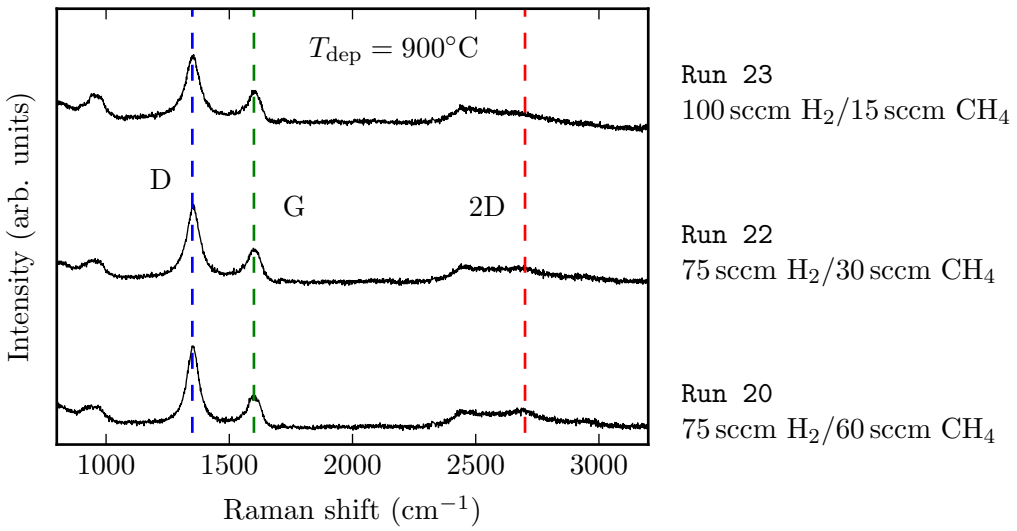


Figure 3.7: Raman spectra of NCG deposited on SiO_2 with different methane concentrations at 900 °C. Exact deposition conditions are listed in Table 3.1.

A second series of experiments was conducted to investigate the effect of the methane concentration on the resulting films. Starting from `Run 20`, the methane flow rate $F[CH_4]$ was reduced to 30 and 15 sccm. The chamber pressure of 1500 mT could not be maintained at the latter flow rate, and consequently the hydrogen flow rate was increased to 100 sccm. The deposition conditions are shown in Table 3.1. Bare SiO_2 samples and samples with 100 nm of nickel were used in the deposition, however only the former were thoroughly investigated. The Raman spectra obtained on these films are shown in Figure 3.7. Note that the spectrum for `Run 20` is the same as the one shown in Figure 3.6. The D and G peak positions and intensities are virtually unchanged. The 2D peak, however, has a decreasing intensity with lower methane concentrations. This could be partially due to the reduced thickness (not measured) resulting from the lower deposition rates at low methane concentrations.

Thermal decomposition of methane can occur at temperatures as low as 600 °C [131]. Thus it was necessary to confirm that the deposition observed on SiO_2 at 900 °C is indeed PECVD and not CVD. To do so, `Run 26` was performed on SiO_2 samples. The conditions are identical to `Run 20`, but no RF field is applied and consequently no plasma is ignited. Raman spectroscopy obtained on these samples after unloading did not exhibit any D, G or 2D peaks, confirming that the deposition was of plasma enhanced nature.

3.2 Nanocrystalline graphene (NCG) deposited directly on insulating substrates

The distinct Raman D peak of the films obtained by PECVD deposition using methane at 900 °C on SiO_2 indicate a strong disorder, and it must be assumed that the obtained films are not crystalline graphene. Raman fitting was used to obtain the intensity ratios $I(D)/I(G)$ and $I(2D)/I(G)$ of ~ 2 and ~ 0.18, respectively. Furthermore, it has been

confirmed that the D peak location ($\sim$ 1600 cm^{-1}) is independent of the excitation wavelength (532, 633 and 785 nm). The D, G and 2D Raman peaks are similar to the ones observed by Ferrari *et al.* [55] and attributed to nanocrystalline *graphite*. An explanation why these films are called nanocrystalline *graphene* in this work, is given in Section 2.3.3 on page 12.

3.2.1 Cluster size estimation from Raman results

The graphene films obtained through PECVD deposition on SiO_2 are nanocrystalline, and it is necessary to assess the film (or crystal) quality. One of the techniques is to estimate the cluster diameter (or crystalline grain size) from Raman peak intensities [132]. The cluster diameter of the nanocrystalline graphene L_a is thus

$$L_a = \frac{I(\mathrm{G}) \cdot C(\lambda)}{I(\mathrm{D})} \tag{3.1}$$

with $C(\lambda)$ a variable scaling coefficient which depends on the excitation wavelength. This coefficient can be calculated by the following equation [133]:

$$C(\lambda) = C_0 + \lambda \cdot C_1 \tag{3.2}$$

where $C_0 = -12.6$ nm and $C_1 = 0.033$ are constants. Note that this is an approximation only valid for excitation wavelengths $400 < \lambda < 700$ nm. With Equations 3.1 and 3.2, the cluster diameter for the films from `Run 20` can be calculated to $L_a \sim 2.5$ nm ($C(532\,\mathrm{nm}) \sim 4.95$ nm, $I(\mathrm{G})/I(\mathrm{D}) \sim 0.5$). Considering this small cluster diameter, the possibility of nanocrystalline cluster formation inside the plasma, and then settling onto the substrate, has to be considered. This can, however, be ruled out with satisfying confidence based on the mechanical stability of the film (no peeling observed in any experiments, including the fabrication process development in Chapter 4).

3.2.2 Thickness measurement by ellipsometry

In this work, two measurement methods are used to characterize the NCG thickness. The first one is based on ellipsometry which is non-destructive, and the whole measurement takes less than 1 min. However, the result strongly depends on the model that is used for fitting and the initial fitting values. The accuracy further decreases when the film is on top of a carrier material with very similar optical properties. The second method for thickness measurement is the use of atomic force microscopy. For this, a surface step has to be obtained, which involves a photolithographic step and a selective etching. This method is destructive, but more accurate as the physical thickness is measured. The AFM system used in these measurements only allows 10×10 mm^2 size sample, making it unsuitable for investigating thickness uniformity over 150 mm wafer.

A sample from `Run 20` (clearest Raman peaks) was used to investigate the accuracy of ellipsometry thickness measurement of NCG on top of wet thermal oxide. The results were then compared with AFM results obtained on a processed sample from the same run. An NCG thickness of $d_{\mathrm{NCG}} = 27.4\,\mathrm{nm}$ was measured by AFM at a surface step created by RIE oxide etching and positive resist mask (successful etch confirmed by Raman). The ellipsometer measurement was done using a *Woollam M-2000* with a spot size of 150 µm at angles of 65, 70 and 75°. The fitting model, including substrate and wet thermal oxide, is provided in Appendix C.5.1 on page 149. The NCG thickness obtained through ellipsometer measurement fitting for the sample from `Run 20` is $30.38 \pm 0.2\,\mathrm{nm}$. The two values show good agreement (difference 10.8%) and it has been demonstrated that ellipsometry offers accurate, non-destructive NCG thickness measurement. The error of the fitting procedure was found to be in the range of 0.05 to 0.2 nm for all measurements, independent of the absolute thickness. Therefore, error values are omitted for the remaining ellipsometry results in this Chapter.

3.2.3 Electric properties

A sheet resistance of $R_{\square} = 3.73\,\mathrm{k\Omega/\square}$ was measured using an *Accent HL5500 Hall System* on the 30.38 nm thick film obtained in `Run 20` on SiO_2. The charge carrier mobility μ of $2.49\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ was extracted as well, alongside with the sheet electron concentration of $n_{\mathrm{s}} = 6.73{\times}10^{14}\,\mathrm{cm^{-2}}$. This corresponds to a bulk electron concentration of $n = 2.22 \times 10^{20}\,\mathrm{cm^{-3}}$.

The sheet resistance and charge carrier mobility is in a very similar range as values reported for nanocrystalline graphene elsewhere. The films deposited by Kalita *et al.* [58] using surface wave plasma enhanced chemical vapor deposition have sheet resistances of $R_{\square} = 3$–$7\,\mathrm{k\Omega/\square}$. Charge carrier mobility and concentration were not reported. The ECR-CVD deposited films at 400 °C by Medina *et al.* [57] have sheet resistances in the range of 5–20 kΩ/□ without reporting the mobility or concentration of charge carrier. The charge carrier mobility of $\mu = 1\,\mathrm{cm^2/V^{-1}\,s^{-1}}$ as reported for molecular beam epitaxy (MBE) grown films on sapphire is slightly lower than the values reported here, however no sheet resistance is provided [61].

3.3 Large area deposition

The deposition achieved on $10 \times 10\,\mathrm{mm^2}$ samples has been a major breakthrough. However, the goal of this thesis is to develop a large area process, and therefore in the following Sections, the transfer of the previous results to full wafers is explained. The used *Nanofab* PECVD tool has the capability for 200 mm diameter wafer deposition. The standard size used in the Southampton Nanofabrication Centre, however, is 150 mm diameter. Therefore the latter size was used in this work.

Eight wafer were processed with the aim to investigate the feasibility of transferring the previous results to large areas, and assess the uniformity of the deposition process.

Wafer	T_{dep} °C	t_{heat} min	t_{dep} min	t_{cool} min	$F[H_2]$ sccm	$F[CH_4]$ sccm
`MSx12`	900	15	15	15	75	60
`MSx13`	900	15	15	15	75	30
`MSx14`	900	15	15	15	75	10
`MSx15`	900	15	5	15	75	60
`MSx16`	900	15	1	15	75	60
`MSx17`	850	12	5	12	75	60
`MSx18`	800	8	5	8	75	60
`MSx19`	750	5	5	5	75	60

Table 3.2: Conditions used for PECVD deposition of NCG on wafer `MSx12` to `MSx19`. See Figure 3.2 on page 41 for parameter explanation. Flow rates F are applied during the deposition step. Hydrogen flow during heat up and 10 min pre-clean is fixed at 100 sccm.

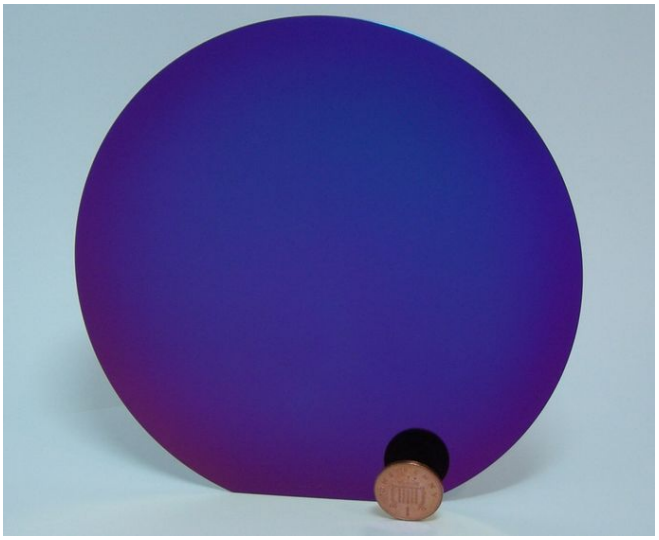
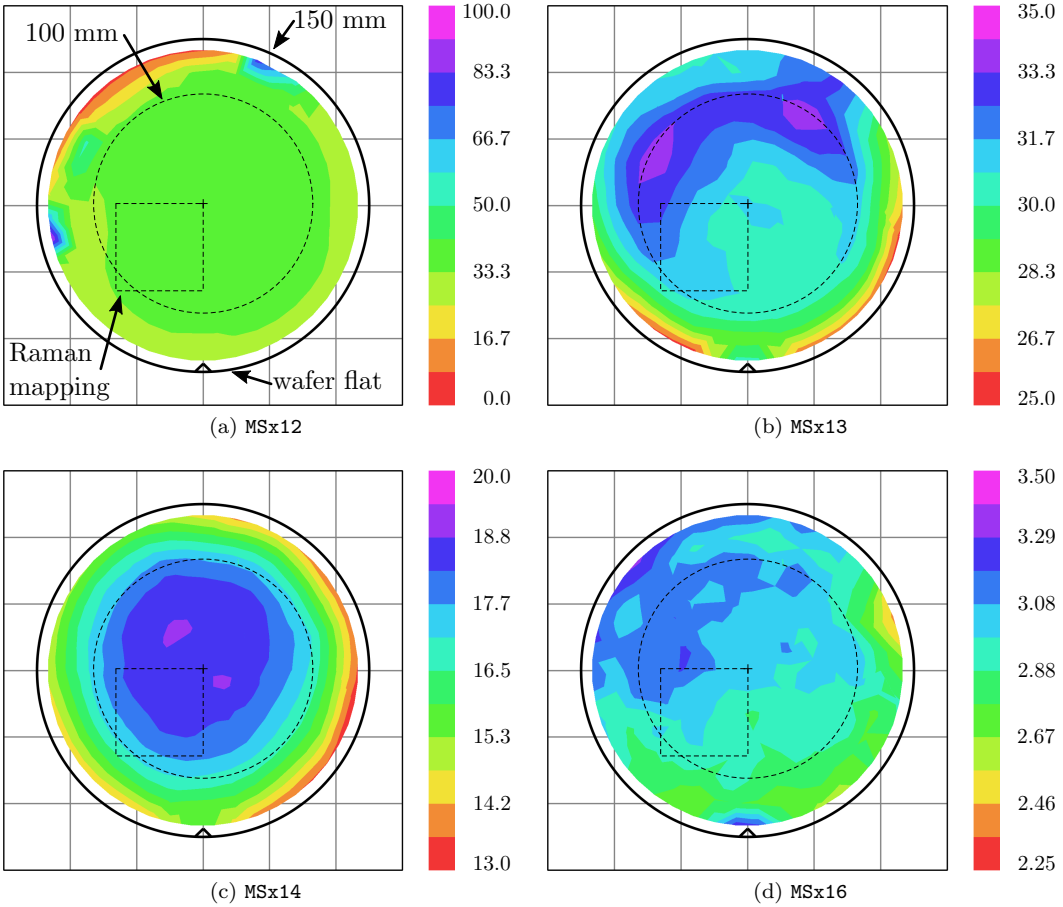


Figure 3.8: Photograph of a 150 mm wafer with deposited NCG film.

These wafers were later used for device fabrication, which is subject of Chapter 4 on page 67. The thermal oxidation and laser marking of these n-doped wafers is described in Section 4.2 on page 69. Deposition conditions used for these wafers (denoted `MSx12` to `MSx19`) are given in Table 3.2 and a picture of such a 150 mm wafer with NCG deposited by PECVD is shown in Figure 3.8.

3.3.1 NCG thickness uniformity

The thickness distribution of the as-deposited NCG was mapped by ellipsometry. The same fit model was used as described earlier in Section 3.2.2. On each of the 150 mm wafers, a total of 180 evenly spaced points were measured (distance from wafer edge 5 mm) and the NCG thickness was obtained through fitting. The results for `MSx12`, `MSx13`, `MSx14` and `MSx16` are shown in Figure 3.9. The physical outline is indicated by a solid circle, and the wafer flat location is at the bottom (small triangular mark).



(a) `MSx12` (b) `MSx13`

(c) `MSx14` (d) `MSx16`

Figure 3.9: NCG thicknesses on wafer `MSx12`, `MSx13`, `MSx14` and `MSx16` measured by ellipsometry. NCG thickness scale is in nm. The solid circle indicates the dimensions of the 150 nm wafer. Inner 100 mm size is indicated. Average thickness values and calculated non-uniformities are provided in Table 3.3. Additional ellipsometry results can be found in Figure C.5 on page 150

The ellipsometer results for the remaining four wafers can be found in Figure C.5 on page 150.

All wafers have an increased non-uniformity toward the edges, which is due to edge effects during deposition. These effects can include different temperature at the wafer edges, plasma non-uniformities or differences of plasma composition, and are typical for PECVD processes. The very strong non-uniformity on wafer `MSx12` (thickness between 0 and 100 nm), however, is unexpected and might be due to some contaminants on the wafer or the shower head. Nevertheless, the inner area has a uniform thickness similar to the other wafers.

Wafer	d^{150}_{mean} (nm)	NU^{150} (%)	d^{100}_{mean} (nm)	NU^{100} (%)	RMS (nm)	d^{100}_{mean}/RMS (–)
`MSx12`	33.8	92	35.5	7	2.04	17.4
`MSx13`	30.6	14	31.5	6	2.25	14.0
`MSx14`	16.6	18	18.0	7	1.17	15.4
`MSx15`	15.0	13	15.7	4	1.27	12.4
`MSx16`	3.0	15	3.0	7	0.227	13.3
`MSx17`	11.7	16	12.4	6	0.91	13.6
`MSx18`	8.0	34	8.9	11	0.559	16.0
`MSx19`	4.6	40	5.2	25	0.408	12.8

Table 3.3: Summary of NCG thicknesses measured by ellipsometry. d^{150}_{mean} is the mean thickness over the whole 150 mm wafer with the respective non-uniformity NU^{150}. The values d^{100}_{mean} and NU^{100} are the mean thickness and non-uniformity for the inner area with a diameter of 100 mm. RMS values were obtained from $1 \times 1\,\mu\text{m}^2$ contact mode AFM measurements close to the wafer center (see Section 3.3.3). The ratio d^{100}_{mean}/RMS is calculated to allow better comparison of RMS values.

To allow better comparison of different thickness distributions, it is common to calculate the non-uniformity NU. The general formula for non-uniformity is defined as[1]

$$NU = \frac{\max(X) - \min(X)}{\max(X) + \min(X)} \cdot 100\% \tag{3.3}$$

where X is the measured quantity. The NCG thickness non-uniformities over the whole 150 mm wafer, NU^{150}, were calculated for all eight wafers according to Equation 3.3 and are listed in Table 3.3. Additionally d^{150}_{mean}, the mean thicknesses (obtained through averaging all 180 points) have been calculated and are shown in Table 3.3, as well.

These calculated non-uniformities, especially for wafer `MSx12`, are very high owing to the extreme data points obtained in the edge regions. Also, as mentioned earlier, edge effects are very common for PECVD processes. Therefore, the average thicknesses and non-uniformities were calculated once more, considering only the inner 100 mm diameter of the wafer, as indicated by the dashed circle in Figure 3.9a. These values (NU^{100} and d^{100}_{mean}) are also provided in Table 3.3 and represent the results more accurately. This is important to allow quantitative comparison of different deposition conditions.

All wafers deposited at 900 °C (`MSx12` to `MSx16`) have very similar thickness non-uniformities in the inner 100 mm area (NU^{100} between 4 and 7%), which increases significantly for 800 °C (`MSx18`, $NU^{100} = 11\%$) and 750 °C (`MSx19`, $NU^{100} = 25\%$). The two films deposited below 850 °C are also relatively thin. Nevertheless, since wafer `MSx16` with only 3 nm NCG thickness has a very low non-uniformity, it is concluded that there is no correlation between non-uniformity and thickness at low temperatures.

[1] This definition is according to the *National Electrical Manufacturers Association* (NEMA), see for example [134, p. 276]. An alternative definition for non-uniformity is $(\max(X) - \min(X))/\text{average}(X)$ [135].

It should be noted that non-uniformities for PECVD-deposited SiO_2 and SiN are generally in the range of 1%. One reason for this non-uniformity could be related to the PECVD tool. The heated wafer stage is made of graphite and has a diameter of 200 mm. The used substrates, however, are only 150 mm in diameter. As a consequence, a ring of exposed graphite surrounds the wafer during deposition. To investigate whether this has an effect on the non-uniformities of the films, deposition on 200 mm substrates should be carried out for comparison. A graphite ring is surrounding the stage, however, it is at significantly lower temperatures than the lower electrode.

3.3.2 Raman mapping

In addition to the NCG thickness mapping by ellipsometry, Raman mapping was used to investigate the full-wafer deposition. This was done using a *Renishaw inVia* Raman spectrometer fitted with an automated xy sample stage with a range of approximately $70 \times 70\,\mathrm{mm}^2$. This is not sufficient to map an entire 150 mm wafer. Thus the wafers were diced into four $40 \times 40\,\mathrm{mm}^2$ samples (details can be found in Section 4.3.2 on page 70), and sample number `4` (e.g. sample `4` from wafer `MSx12` is called `MSx12_4`) was used for Raman mapping. The location of sample number `4` on each wafer is indicated by the dashed rectangle in the ellipsometer results in Figure 3.9.

Each of the eight samples was mapped (8×8 evenly spaced measurements) using 532 nm excitation wavelength. The laser spot diameter is approximately 1 µm ($\times 50$ lens), and the spacing between the measurement locations is 5 mm, with 2.5 mm offset from the edges. Peak fitting was then used to obtain the location and intensity of the D ($1350\,\mathrm{cm}^{-1}$, only present in disordered graphene), G ($1600\,\mathrm{cm}^{-1}$) and 2D ($2700\,\mathrm{cm}^{-1}$) peaks, respectively. The D and 2D peak are fitted by one Lorentzian[2] curve shape, while four Lorentzians are necessary for the G peak. The envelope of these four curves is then used to obtain the intensity and the location (point of highest intensity). The raw data and the fit results for one Raman spectrum of sample `MSx12_4` is shown in Figure 3.10.

The Raman intensities obtained through curve fitting were also used to calculate the intensity ratios $I(\mathrm{D})/I(\mathrm{G})$ and $I(\mathrm{2D})/I(\mathrm{G})$. The former can be used to estimate L_a, the cluster diameter of the nanocrystalline graphene, as explained in Section 3.2.1. L_a is plotted as a function of the NCG thickness in Figure 3.13. The maps of these calculated ratios are shown in Figures 3.11 and 3.12 for `MSx12_4`, `MSx13_4`, `MSx14_4` and `MSx16_4`, with the center of the wafer in the upper right corner of this $40 \times 40\,\mathrm{mm}^2$ representation. The average intensity ratios are also listed in Table 3.4, together with non-uniformity values NU_DG and NU_2DG calculated according to Equation 3.3.

The Raman maps of the $I(\mathrm{D})/I(\mathrm{G})$ and $I(\mathrm{2D})/I(\mathrm{G})$ ratios show good uniformity on all wafers, with non-uniformity values slightly lower than the ones of the ellipsometry results (compare Table 3.3). However, the increasing trend of the non-uniformities for 800 °C and 750 °C (wafers `MSx18` and `MSx19`) are observed in the Raman data as well. A

[2] Lorentzian is the preferred curve shape for fitting of Raman spectra of disordered graphite [132].

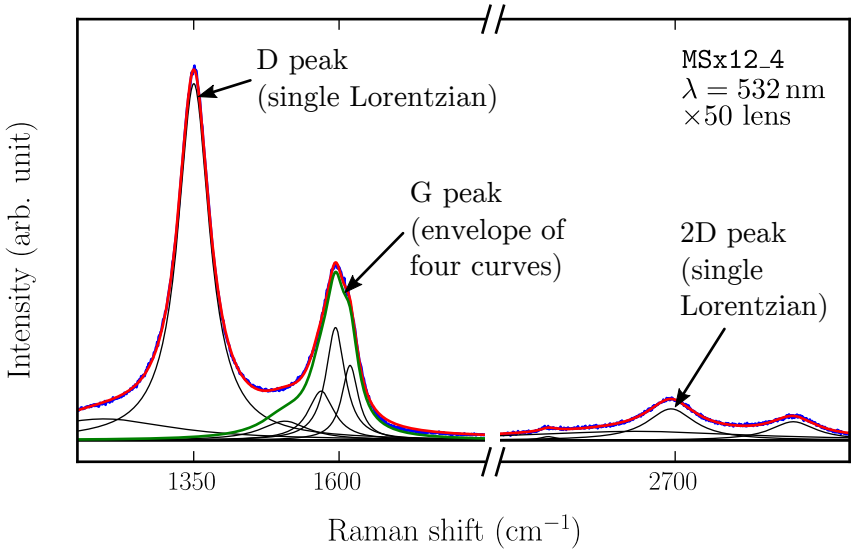


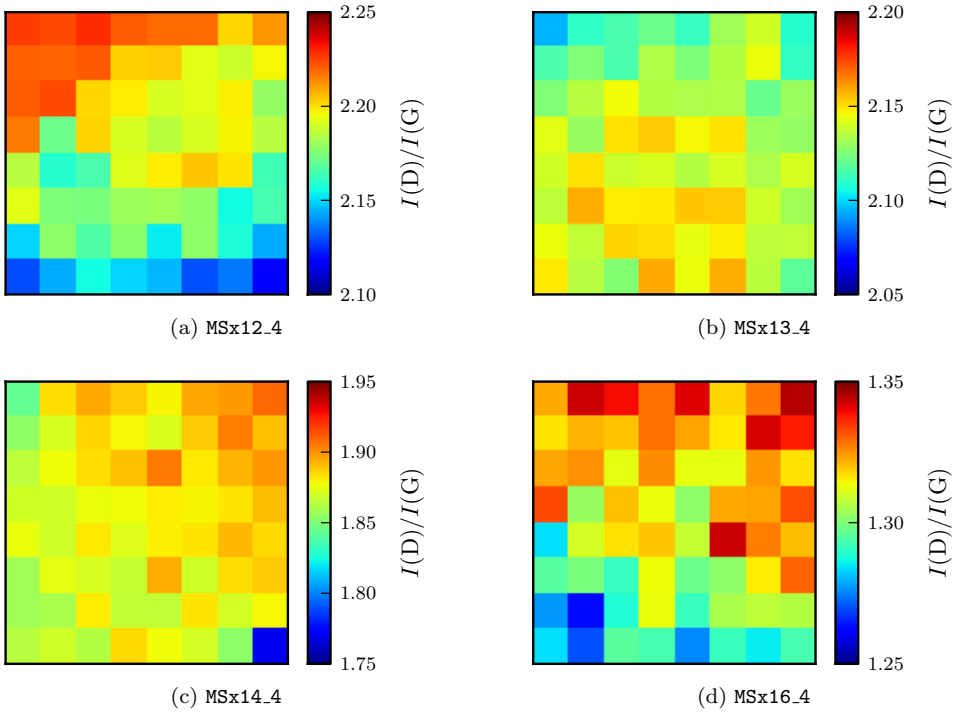
Figure 3.10: Illustration of fitting results. The Data is approximated by lorentzian curves. The D and 2D peak are approximated by one single Lorentzian. Four Lorentzians are used to approximate the G peak (sum of these Lorentzians shown in green).

Sample	T_{dep} (°C)	t_{dep} (min)	d^{100}_{mean} (nm)	$I(\mathrm{D})/I(\mathrm{G})$	NU_{DG} (%)	$I(\mathrm{2D})/I(\mathrm{G})$	NU_{2DG} (%)	L_{a} (nm)
MSx12_4	900	15	35.5	2.185	2.6	0.194	5.1	2.27
MSx13_4	900	15	31.5	2.136	1.5	0.148	6.0	2.32
MSx14_4	900	15	18.0	1.878	3.8	0.126	5.1	2.64
MSx15_4	900	15	15.7	2.051	3.5	0.105	4.2	2.41
MSx16_4	900	15	3.0	1.313	3.1	0.117	5.4	3.77
MSx17_4	850	12	12.4	2.028	1.1	0.092	4.9	2.44
MSx18_4	800	8	8.9	1.919	6.6	0.105	3.9	2.58
MSx19_4	750	5	5.2	1.633	6.7	0.089	6.5	3.03

Table 3.4: Fitting results of NCG Raman mapping. $I(\mathrm{D})/I(\mathrm{G})$ and $I(\mathrm{2D})/I(\mathrm{G})$ are the averages over all 64 data points. Deposition temperature, duration and NCG thickness is given for reference.

smaller $I(\mathrm{D})/I(\mathrm{G})$ value indicates a lower defect density in the NCG films, and a higher $I(\mathrm{2D})/I(\mathrm{G})$ value shows the presence of graphene.

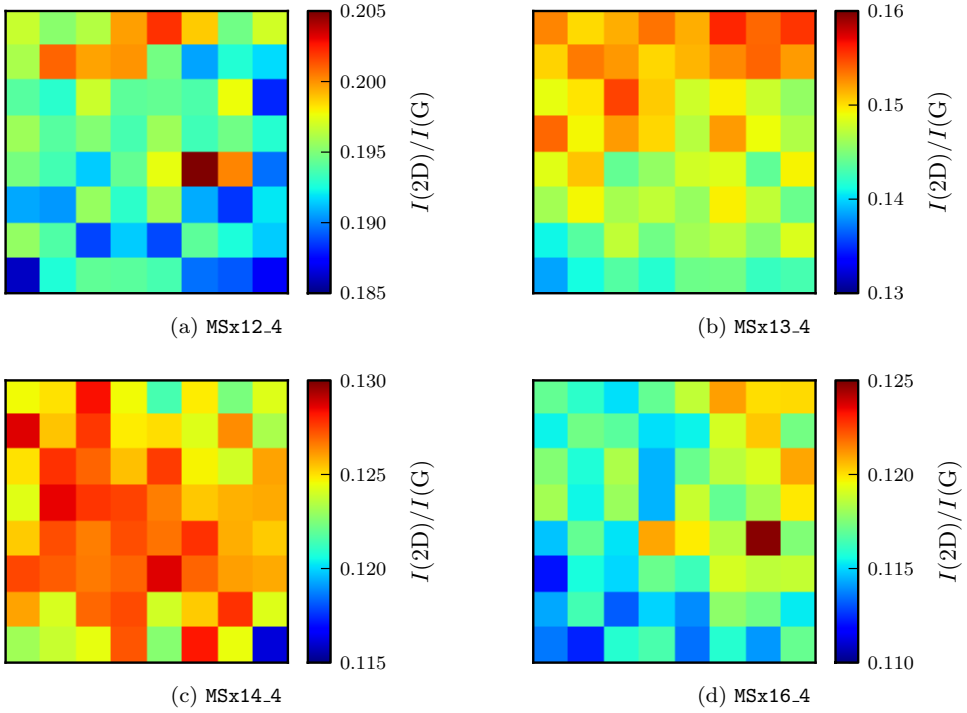
Two interesting trends are visible in the obtained data. The first one is the increasing cluster diameter L_{a} with decreasing NCG thickness d^{100}_{mean} (Figure 3.13). The resulting data was approximated using a linear fit and a power-law function. The variance of the linear and power-law fits are 0.1035 and 0.0077, respectively, quantifying the observation that the power-law fit matches the data points closer. The second observation is that, for 900 °C deposition temperature, a decrease of disorder is achieved by reduction of methane concentration (MSx12–MSx14). A similar trend has been observed for CVD growth of graphene on copper, where low concentrations of CH_4 favor the formation of



(a) MSx12_4 (b) MSx13_4

(c) MSx14_4 (d) MSx16_4

Figure 3.11: Raman $I(\mathrm{D})/I(\mathrm{G})$ mapping results for wafer MSx12, MSx13, MSx14 and MSx16. For location of the $40 \times 40\,\mathrm{mm}^2$ areas on the 150 mm wafers see Figure 3.9a.



(a) MSx12_4 (b) MSx13_4

(c) MSx14_4 (d) MSx16_4

Figure 3.12: Raman $I(\mathrm{2D})/I(\mathrm{G})$ mapping results for wafer MSx12, MSx13, MSx14 and MSx16. For location of the $40 \times 40\,\mathrm{mm}^2$ areas on the 150 mm wafers see Figure 3.9a.

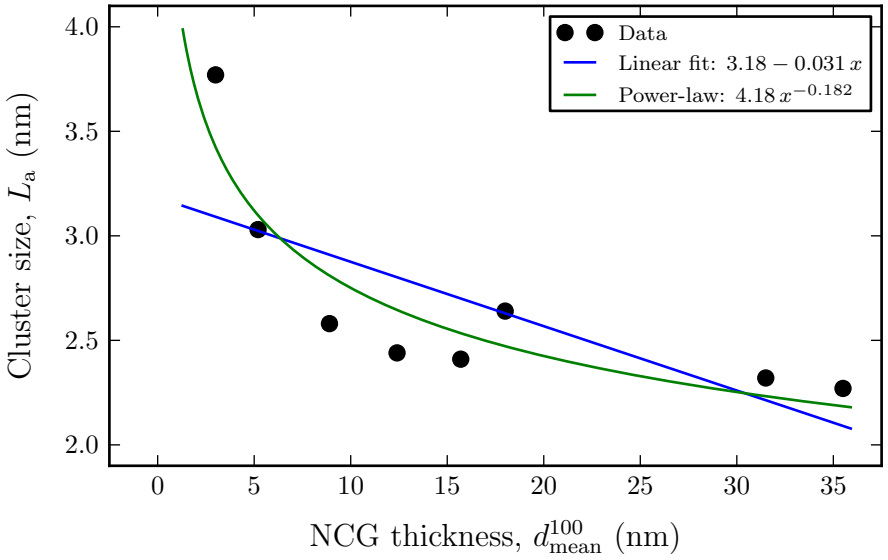


Figure 3.13: Cluster diameter L_a obtained from Raman fitting results versus NCG thickness obtained from ellipsometry. The cluster diameter increases with decreasing NCG thickness.

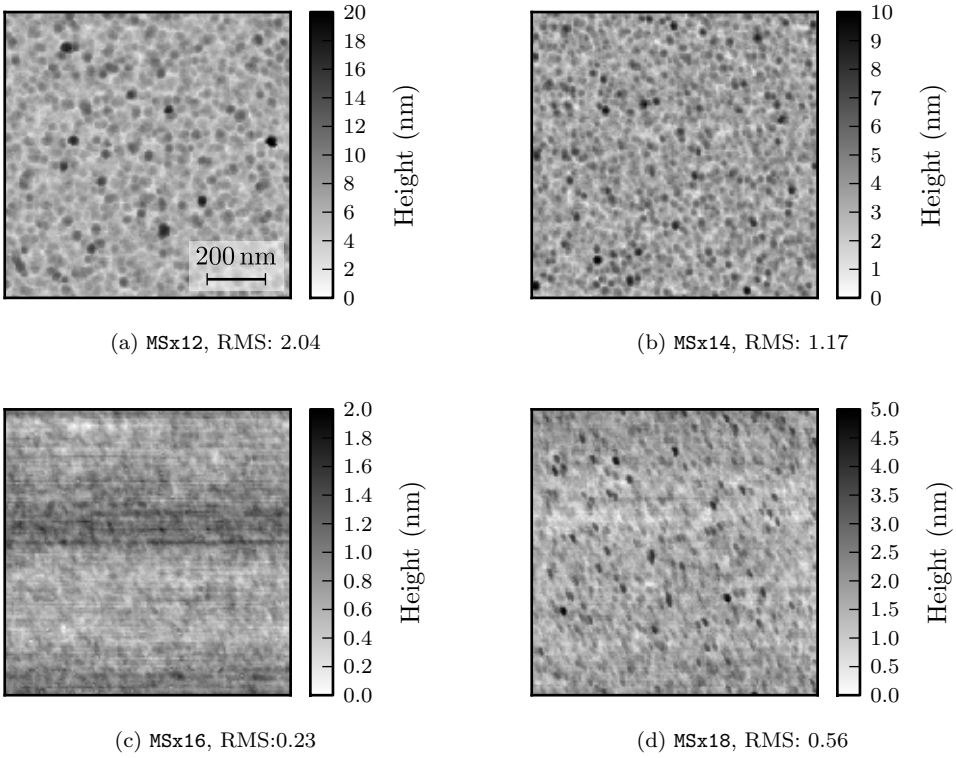
large area uniform monolayer graphene [136].

3.3.3 Surface roughness

From each of the $40 \times 40\,\mathrm{mm}^2$ samples used for Raman mapping, a $5 \times 5\,\mathrm{mm}^2$ piece was obtained by cleaving from the corner originally in the center of the wafer. This sample was consecutively used to measure the NCG surface roughness by AFM. An $1 \times 1\,\mu\mathrm{m}^2$ large area was scanned with a *Veeco Multimode V* AFM in contact mode with a spatial resolution of 256 by 256 points. The root mean square (RMS) roughnesses were calculated from these results and are listed in Table 3.3 on page 53. In order to allow better comparison between the RMS values, the ratio of the NCG thickness d^{100}_{mean} to RMS is calculated and is provided in Table 3.3. Compared to the Raman results, no significant variation of the d^{100}_{mean}/RMS ratio is observed, which suggests that the deposition conditions (see Table 3.2) have little influence on this quantity. The RMS value of 0.227 nm for `MSx16`, however, is less than the distance between graphene sheets in graphite of 0.335 nm [137].

3.3.4 Summary of large area deposition

It has been demonstrated in this Section that the metal-free PECVD deposition is suitable for large areas. A total of eight 150 mm wafers were deposited with variations in deposition temperature (750–900 °C), methane flow rate and deposition durations. The as-deposited films were then extensively analyzed by ellipsometry, Raman spectrometry and atomic force microscopy.



(a) `MSx12`, RMS: 2.04

(b) `MSx14`, RMS: 1.17

(c) `MSx16`, RMS:0.23

(d) `MSx18`, RMS: 0.56

Figure 3.14: NCG topography for wafers `MSx12`, `MSx14`, `MSx16` and `MSx18` acquired by contact mode AFM close to wafer center. RMS values for all eight wafers is given in Table 3.3 on page 53.

Thickness non-uniformities for all wafer deposited at 850 °C and 900 °C were below 7% (considering the inner 100 mm diameter). Raman mapping revealed furthermore a strong dependence of the cluster diameter L_a on the film thickness.

Further work should be carried out to reduce the concentration of CH_4 (possibly by adding argon) and evaluate the influence on cluster diameter L_a and the surface roughness. Furthermore, there is strong evidence that reduction of the film thickness has a very strong positive influence on the cluster diameter. Using highly diluted process gas will help keep the process time in controllable dimensions (> 1 min), as depositions with durations shorter than that are likely to suffer from effects such as plasma instability in the first seconds of the deposition. An important additional area deserving attention is the reduction of deposition temperature while maintaining the film quality. This will help increase compatibility with other fabrication processes.

Device fabrication process development based on the NCG films deposited on wafers `MSx12` to `MSx19` is explained in Chapter 4 on page 67.

3.4 Application of NCG as transparent electrode

In this Section, optical transparency of NCG was investigated, and the performance as transparent electrode is compared to ITO, exfoliated graphene and other reported values.

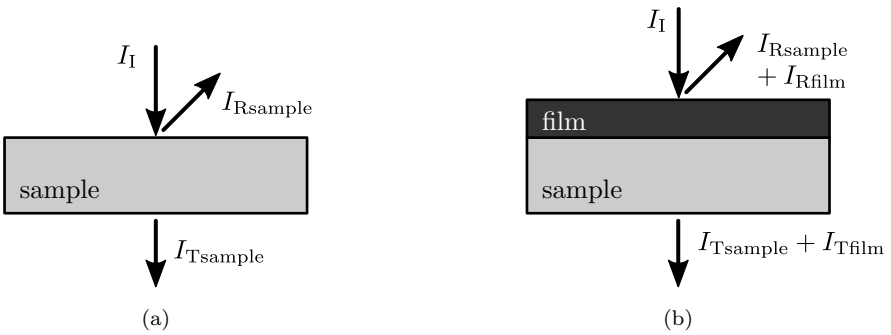


Figure 3.15: Model for optical characterization of (a) single material and (b) two material stack. Incident light with intensity I_I gets reflected (I_R), transmitted (I_T) or absorbed.

3.4.1 Optical measurement method

When a material is to be used as transparent conductive film, the most important information about its optical properties is the optical absorption α. It is the percentage of the light which gets absorbed on its way through the material. A larger value indicates a stronger absorption. Optical absorption cannot be measured directly, instead it is calculated from optical transmission and reflection measurements.

The setup for transmission measurements consists of a white light light source with a constant intensity which is directed onto a photodetector. When the optical path is free, the full light intensity reaches the sensor, providing a calibration reading. Then, the specimen under investigation is placed in the light path between the light source and the photodetector, and the output of the sensor is recorded. This value, together with the calibration reading mentioned before, allows the transmittance T to be calculated. The transmittance is the percentage of light that passes through the specimen and has a value between 0 and 100%.

The calculation of the optical absorption from the transmittance alone can introduce significant errors due to the possible reflectance of the specimen. This is illustrated in Figure 3.15a. Light with known intensity (I_I) is directed onto the sample, and the transmitted intensity (I_T) is detected to yield the transmittance T. Some light, however, is typically reflected (I_R), which has to be considered when calculating the absorption.

To measure the reflectance R, light (with constant intensity I_I) is directed onto a surface with full reflectivity, and the reflected intensity I_R is detected by a photodetector. This, again, is used as calibration reading. Following this, the reflective surface is replaced by the sample under investigation, and only the intensity of the reflected light I_R is measured.

The schematic model in Figure 3.15a shows that light that was neither reflected nor transmitted must have been absorbed by the material. Thus, the absorption α can be calculated by

$$\alpha = 1 - (T + R)\,. \tag{3.4}$$

Next, the absorption measurement of a film on top of a carrier substrate, as shown in Figure 3.15b, is considered. It is assumed that there is no interaction (e.g. Fresnel reflection) between the film and sample, and the results are a simple superposition of the optical properties of the two materials. For transmittance and reflectance, the contribution of the film can thus be calculated by

$$T_{\text{film}} = T + (1 - T_{\text{sample}}) \tag{3.5}$$

and

$$R_{\text{film}} = R - R_{\text{sample}} \tag{3.6}$$

where T and R are the measured transmittance and reflectance, respectively, of the specimen and T_{sample} and R_{sample} are the corresponding values of the sample. The absorption of the film alone is then

$$\alpha_{\text{film}} = 1 - (T_{\text{film}} + R_{\text{film}}). \tag{3.7}$$

By using a light source with adjustable output wavelength, the absorptions can be obtained as a function of wavelength. This information is particularly interesting when a material is to be used for optical device application at specific wavelengths. Additional explanations about the optical theory mentioned in this Subsection can be found in standard optics literature [138].

3.4.2 Measurement setup

All measurements were performed in a commercial system from *Bentham*, consisting of a *TMc300* monochromator and a *DTR6* integrating sphere fitted with a silicon photodiode as detection unit. A schematic cross-section of the integrating sphere is shown in Figure 3.16a. The incident light beam (red line) enters the integrating sphere through the transmittance port and is directed at the reflectance port. Specular reflections finally reach the SPIN/SPEX[3] port. The interior of the integrating sphere is coated with barium sulphate (a very good reflector) to include detection of diffused light as well. In the measurements here, the specular reflection is included by closing the SPIN/SPEX port. During calibration measurements, the reflectance port is closed using a highly reflective material with a reflectance of 1. The measured calibration curve is shown in Figure 3.16b illustrating the wavelength dependence of the silicon photodetector. The measurement software uses the calibration data to calculate the transmittance and reflectance in percentage.

Small samples are held in place perpendicular to the incident light beam with the help of a mounting frame and adhesives. Measurements are carried out for wavelengths ranging from 300 to 1100 nm, and take up to 15 min.

[3]SPIN stands for *specular included*, SPEX stands for *specular excluded*.

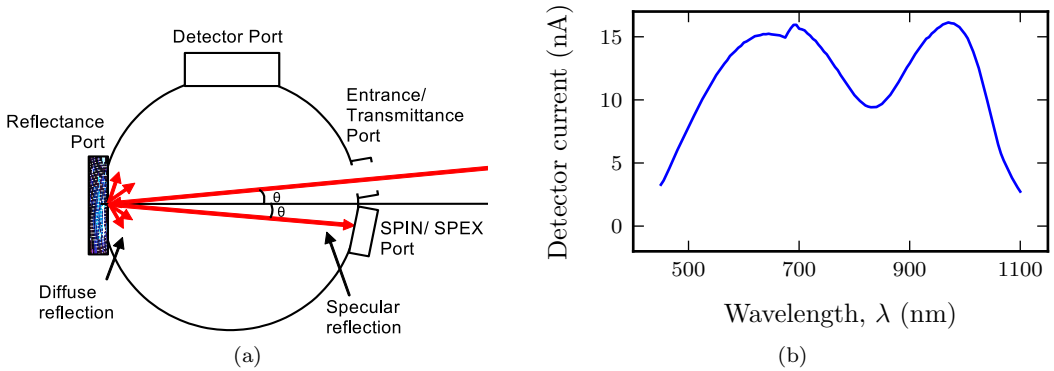


Figure 3.16: (a) Schematic cross section of *Bentham* integration sphere. Reproduced from www.bentham.com. (b) Typical calibration curve for silicon photodiode measured with the integrating sphere.

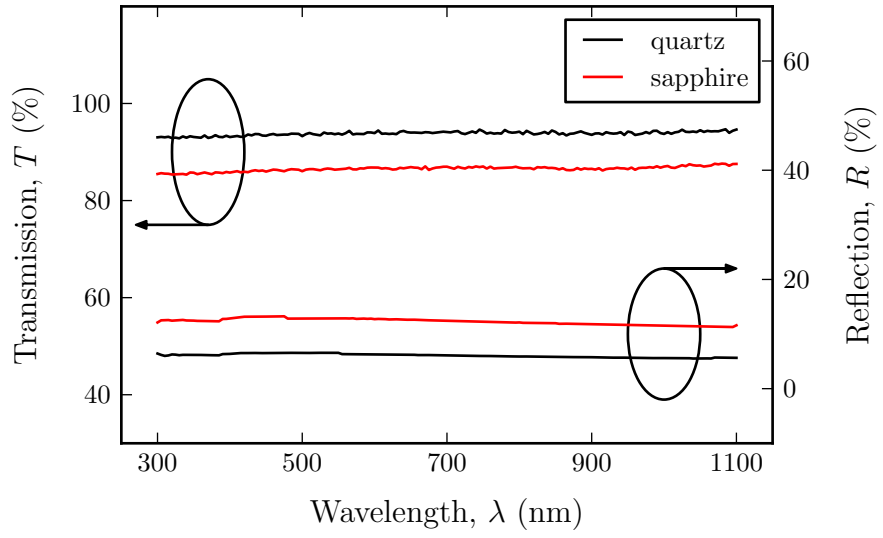
3.4.3 Absorption of quartz and sapphire glass

The absorption of clean 1 mm thick quartz glass and 375±20 µm thick sapphire glass was measured first. Figure 3.17a show the obtained transmittance and reflectance for quartz and sapphire, respectively. Figure 3.17b shows the sum of the measured transmittance and reflectance curves shown in Figure 3.17a. All sums are within a very narrow margin around 100%, showing that the optical absorption in the quartz and sapphire is very small and therefore can be neglected without introducing any significant error. Since the accuracy of the transmission and reflection measurements rely on the calibration measurement, variations of the light power or photodectector sensitivity (for example due to temperature change) can lead to sums larger than 100%. Sampling errors can add to these inaccuracies. Therefore, any result larger than 100% is treated as if 100% and it has been concluded that quartz glass has the lower absorption and is thus more suitable as substrate.

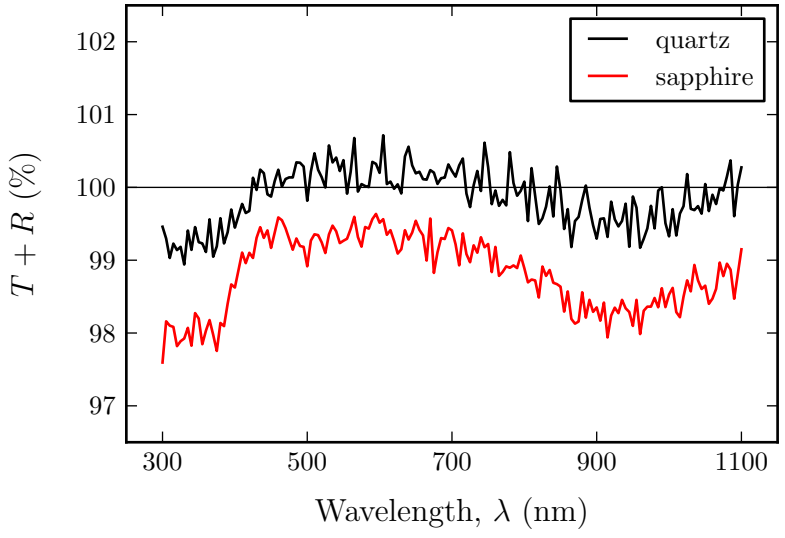
3.4.4 Absorption of NCG films on quartz and sapphire

Three NCG samples deposited at 900 °C for 15 min on 1 mm thick quartz and 375±20 µm thick sapphire are shown in Figure 3.18. The growth conditions are summarized in Table 3.5. The transmission and reflection of the NCG films were calculated according to Equations 3.5 and 3.6. These calculated values were then used to obtain the optical absorption of the films according to Equation 3.7, as shown in Figure 3.19a (black curves).

The procedure above requires two optical measurements, i.e. transmission and reflection. However, the reflectance for a single layer of exfoliated graphene was found to be $<0.1\%$ [45], and as a consequence it is common to only do transmission measurements for graphene. To evaluate whether this also applies to the NCG developed in this work, optical absorption is calculated once more according to Equation 3.7 with R neglected. The results are shown in Figure 3.19a as red curve.



(a)



(b)

Figure 3.17: (a) Measured transmission and reflection of 1 mm thick quartz and 375 ± 20 µm thick sapphire. (b) Sum of transmission and reflection from (a).

The differences between these two curves are shown in Figure 3.19b. In the visible range the difference is below 2%. Thus, it is concluded that for the optical characterization of the NCG films on quartz and sapphire it is sufficient to perform only transmittance measurement.

3.4.5 Performance of NCG as transparent electrode

Performance values of graphene-based transparent electrodes were reviewed in Section 2.5.1 on page 22. There is a consensus in literature that the transparency at 550 nm wavelength and the sheet resistance are compared. The measured transmittance

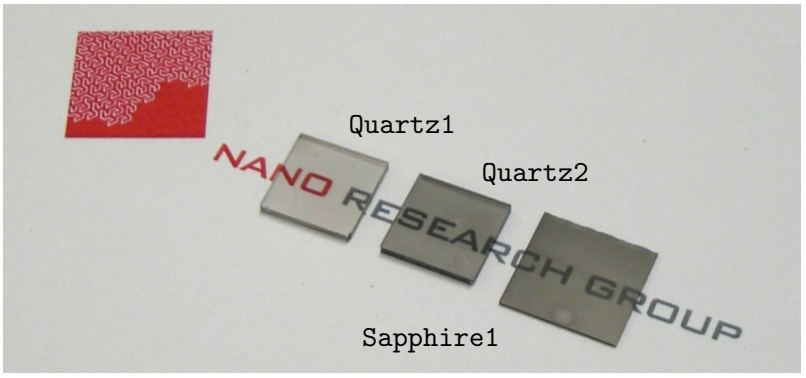


Figure 3.18: Picture showing NCG films deposited on quartz (left and middle, $10 \times 10\,\mathrm{mm}^2$) and sapphire (right) on top of *Nano Research Group* logo.

Sample ID	Carrier substrate	$F[H_2]$ (sccm)	$F[CH_4]$ (sccm)	d_{NCG} (nm)	$R_\square$ (k$\Omega/\square$)	Transp. (%)	σ/α (Ω^{-1})
`Quartz1`	quartz	60	75	5.5	13	85	0.47×10^{-3}
`Quartz2`	quartz	72	90	15	2.5	65	0.93×10^{-3}
`Sapphire1`	sapphire	72	90	15	7500	65	0.31×10^{-6}

Table 3.5: Description of samples with NCG deposited on transparent substrates. Deposition temperature T_{dep} and duration t_{dep} for all samples are 900 °C and 15 min, respectively. The sheet resistance $R_\square$ and transparency are measured at 550 nm wavelength.

(or transparency) at 550 nm wavelength and sheet resistances (measured using an *Accent HL5500 Hall System*) for the three samples fabricated in this work are given in Table 3.5. Additionally, the figure of merit values (compare Equation 2.3 on page 23) of the films are calculated and given in Table 3.5. In Figure 3.20, these three values are visually compared to literature values.

The result for `Sapphire1` is far away from other reported values. The large resistance of 7.5 MΩ on sapphire has not been further investigated, and it is not possible at this stage to say whether this is a reproducible value. The possibility of granular boundary passivation has to be considered. Samples `Quartz1` and `Quartz2`, however, are closer to other reported values, and `Quartz1` falls within the range attributed by Jo *et al.* [80] to chemically modified graphene. The value is also close to the value reported by Medina *et al.* [57], which is a metal-free deposition method.

Several methods exist to reduce the sheet resistance of graphene without influence on the transparency. One is by doping, using the polymer TFSA ($(CF_3SO_2)_2NH$), reported to reduce the sheet resistance by up to 70% [139]. Also nitrogen doping can increase the conductivity [140]. It is possible that the performance of NCG will increase by employing such doping methods, and results similar to the ones obtained on graphene grown by CVD on nickel with consecutive transfer will be achieved.

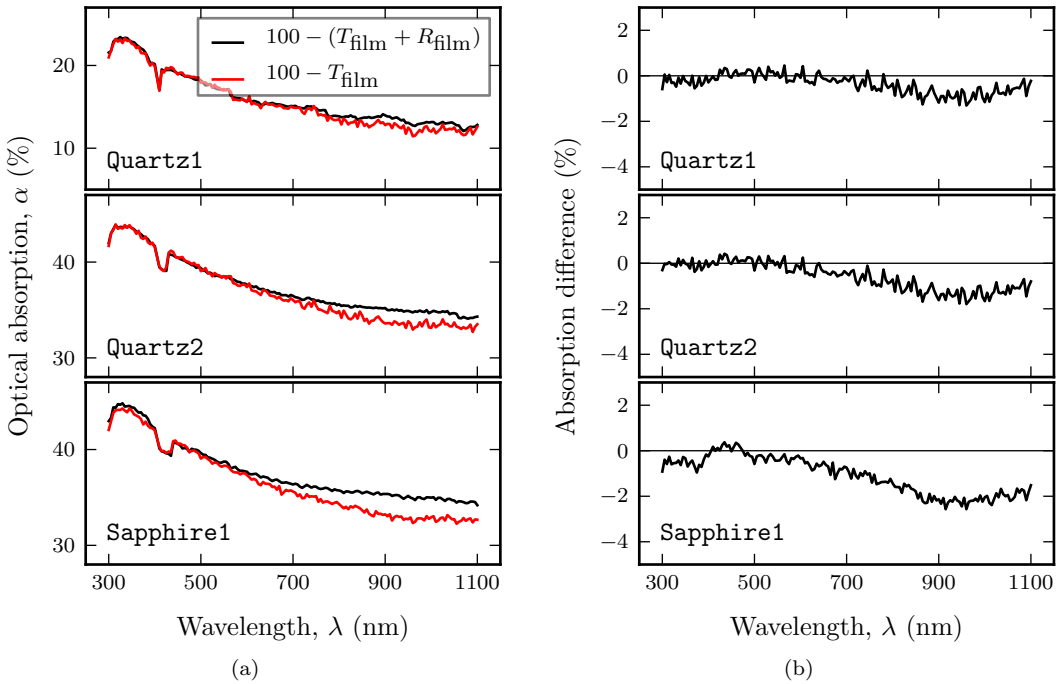


Figure 3.19: Comparison of NCG absorption calculation strategies. (a) Absorption calculated following Equations 3.7 with and without film reflectance. (b) Difference between the two calculation methods.

3.5 Summary

In this Chapter, the development of a large area, metal-free PECVD deposition process for nanocrystalline graphene has been developed. In the first part of the Chapter initial experiments, which were aimed at reproducing CVD growth on nickel by PECVD, were explained. Since CVD growth on nickel strongly depends on the cool-down rate, and the used PECVD machine does not allow accurate control, rapid thermal annealing was first used to crystallize graphene on top of nickel from evaporated amorphous carbon. With RTA conditions known to work, the next step was taken to deposit carbon on nickel samples by PECVD. In the course of these experiments, direct deposition of nanocrystalline graphene was achieved on SiO_2. Such a direct deposition on insulating substrates is favorable over deposition on nickel as it does not require any subsequent transfer step.

In the second part of this Chapter, the NCG deposition on SiO_2 was further investigated, and films were analyzed extensively. It has been shown that ellipsometry is a reliable method to determine the NCG thickness on SiO_2, and the cluster diameter was estimated from Raman results. Finally, four probe measurements were used to obtain sheet resistance and charge carrier mobility.

The subject of the third part of this Chapter was the evaluation of NCG deposited on 150 mm oxidized silicon wafers. In total eight wafers were deposited. The high thickness and cluster diameter uniformity was confirmed by ellipsometry and Raman spectrometry,

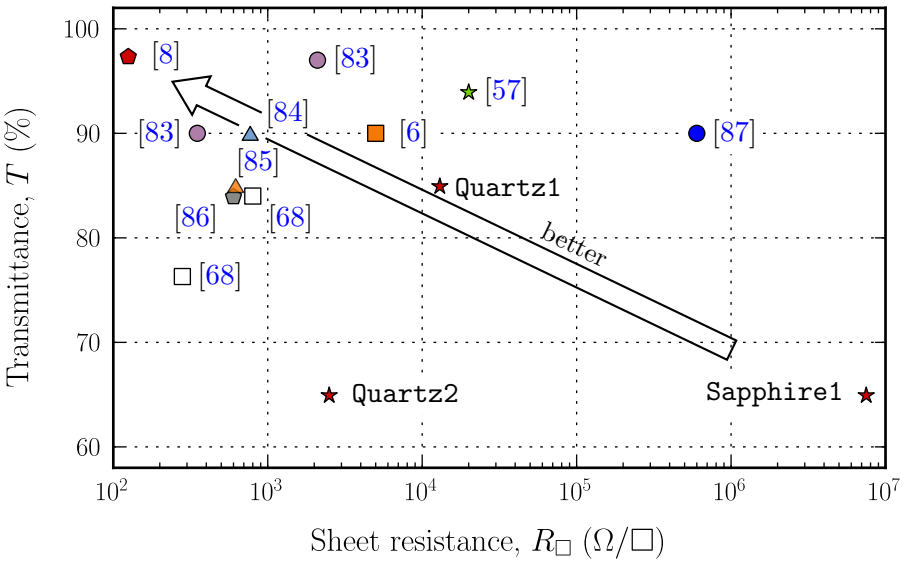


Figure 3.20: Comparison of transmittance T versus sheet resistance $R_\square$ values obtained in this work (`Quartz1`, `Quartz2` and `Sapphire1`) with reported values.

respectively. AFM measurements show low RMS roughness values, and strong evidence is presented suggesting that thinner NCG films have larger cluster diameter.

In the last part of this Chapter, the suitability of the NCG for transparent electrode applications was demonstrated. NCG is deposited on quartz and sapphire glass, and the optical absorption is extensively studied. The obtained films are finally compared to other reported values, showing promising results.

Chapter 4

Device fabrication and characterization

In the previous Chapter, a large area, metal-free PECVD deposition process for nanocrystalline graphene has been developed. The high uniformity of the films has been demonstrated. The primary aim of this Chapter is to develop new, or adapt existing, processes that are suitable for the fabrication of microfabricated structures based on the NCG film.

In Section 2.2.1 on page 9, it has been shown how graphene membranes and suspended graphene strips can be used to measure mechanical strength (see Section 2.2.1 on page 9) and thermal conductivity (see Section 2.2.2 on page 9). Furthermore, electronic properties of suspended graphene are closer to the theoretical values than graphene in contact with a substrate. Therefore, fabrication processes for membranes and suspended NCG strips are developed here.

Different aspects of graphene transistors were reviewed in Section 2.5.2 on page 24, and the three fundamental transistor fabrication designs are shown in Figure 2.25 on page 29. Fabrication of an NCG transistor comprising back gate is a subset of the suspended beam fabrication process, as will become clear in Section 4.5 of this Chapter. The transistor variation with top gate, however, requires a top gate to be deposited and patterned on top of the contacted NCG. Therefore, as the third fabrication process, a top gated transistor structure is developed comprising an SiO_2 gate dielectric.

Finally, a fabrication process for NCG nanowire is developed in Section 4.7 on page 91, following the technique reviewed in Section 2.6.5 on page 32.

4.1 Overview

To help illustrate the four fabrication processes and their relation between each other, the reader is referred to Figure 4.1. All silicon substrates used in this work were originally wet thermally oxidized together. This substrate preparation step is explained in Section 4.2. Section 4.3 then contains details of the NCG sample preparation. The as-deposited

samples are subsequently used for the fabrication of membranes, suspended beams and top-gated structures.

The fabrication of the membrane devices is explained in detail in Section 4.4. The membranes are realized by through-wafer inductively coupled plasma (ICP) etching of the samples from the back, with the thermal oxide below the NCG acting as etch stop. The membranes are finally released by HF vapor etching. The mask used for the ICP etch step comprises squares and circles with diameters between 1 and 100 µm. The fabrication could not be finished by the time of preparing this thesis.

The fabrication of suspended NCG beams, explained in Section 4.5, and the fabrication of top-gated structures, explained in Section 4.6, are related in several ways. They are based on the same lithography mask set and the same initial fabrication steps. After patterning the NCG film into 20 µm long strips with different widths, Ti/Au contacts are patterned by lift-off to form an electrical contact to these strips. In the case of the suspended beams, the fabrication is then finalized by etching the underlying SiO_2 film with HF, thus releasing the beams. The top-gated structures, on the other hand, require two more photolithographic patterning steps. First, a PECVD oxide is patterned to form the top gate passivation. Secondly, the top gate is realized by Ti/Au lift-off.

The NCG nanowire formation is achieved by patterning steps into the SiO_2 layer prior to the NCG deposition. During a subsequent anisotropic oxygen plasma etch, NCG remains at the steps due to the increased vertical film thickness. Finally, Ti/Au contacts are realized by lift-off.

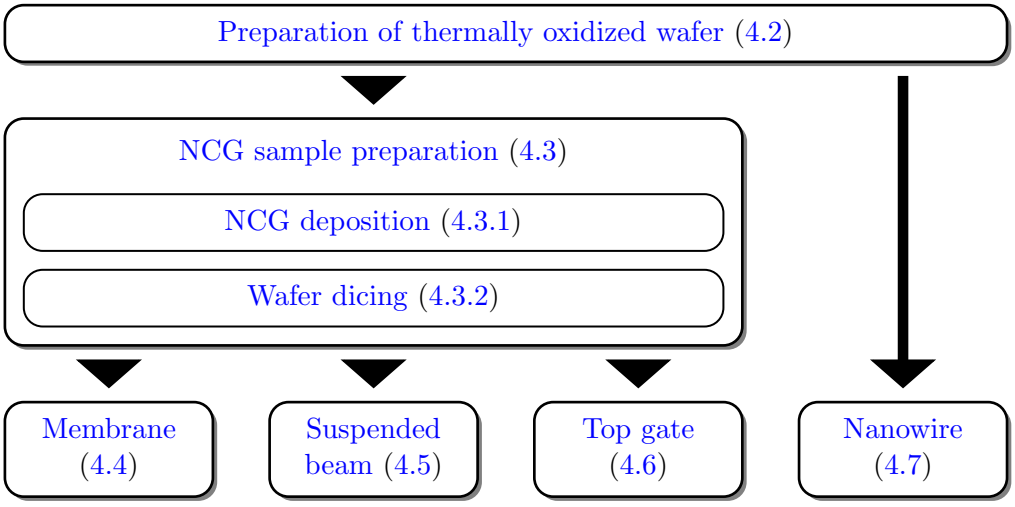


Figure 4.1: Flowchart illustrating the relation between the four fabrication processes represented by the four bottom squares.

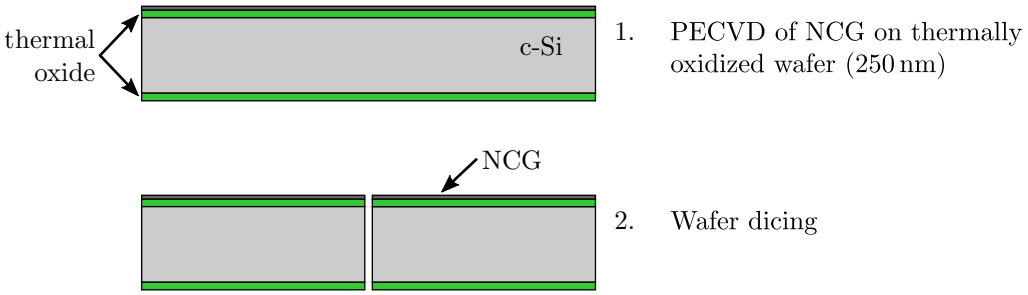


Figure 4.2: Fabrication process flow chart illustrating NCG growth and wafer dicing. After (1) NCG deposition, the wafer is (2) diced into smaller samples for further processing.

4.2 Wet thermal oxidation and laser marking

The silicon wafers used in this work are [100] n-doped single side polished with a diameter of 150 mm. The exact properties can be found in Appendix C.1 on page 145. The wafers were first cleaned in FNA (fuming nitric acid) for 15 min, rinsed and spin dried. Then, wet thermal oxidation was performed on all 25 wafers at 1000 °C for 48 minutes. The oxide thickness was measured on the second wafer in the boat by ellipsometry. The thickness was in the range of 242.5 to 246.5 nm, which correlates to a non-uniformity of 0.8%.

Identifiers were laser scribed into the back side of the wafers labeled as `MSx12` to `MSx19` (eight wafers) after the oxidation. This was done to ensure that diced wafer pieces do not get mixed, and fabricated devices can be unambiguously attributed to their respective NCG deposition conditions. Refer to Appendix C.2 on page 145 for details about the laser marking. The wafers were consecutively cleaned in deionized (DI) water and FNA to remove any particles potentially generated during the laser ablation method.

4.3 NCG sample preparation

As explained in the Overview at the beginning of this Chapter and illustrated in Figure 4.1, NCG samples were prepared together, and later processed into different devices. This has two reasons: firstly, device functionality can be better compared, since different devices are fabricated from identical NCG films. Secondly, one sample obtained from each NCG wafer is kept unprocessed and can be analyzed in detail, even by destructive analysis methods.

Figure 4.2 illustrates the process of this part of the fabrication. The first step is the PECVD deposition of NCG on the thermally oxidized 150 mm wafers, as explained in Section 4.2. Subsequently, the wafers are diced into smaller samples.

4.3.1 NCG deposition

Deposition was carried out as part of the large area deposition experiments described in Section 3.3 on page 50 (wafer `MSx12` to `MSx19`). The deposition conditions are listed in Table 3.2 on page 51. That Section also describes the thickness uniformity evaluation by ellipsometry, the Raman mapping and roughness measurement by AFM on these wafers.

4.3.2 Wafer dicing

Wafer dicing requires the substrate to be placed on an adhesive foil with a defined thickness. During dicing, the depth of the cut is controlled in such a way that it reaches into the dicing foil without damaging the underlying stage. The wafer can therefore be placed on the foil either with the top facing up (and thus be exposed to water and silicon dust) or facing down (in direct contact with the dicing foil). The second option is generally preferred, as the foil protects the active surface of the wafer from contamination. However, removing the foil after the dicing process can lead to peeling of the surface or other implications. Here, the NCG has good adhesion to the SiO_2 and is not damaged during peeling. Thus, the NCG film was diced facing the dicing foil.

The wafers were diced into $40 \times 40\,\mathrm{mm}^2$ samples, yielding four full samples from the center of the wafer. The dicing pattern is provided in Figure C.1 on page 146. A resin blade with a feed speed of 10 mm/s was used. The samples were blow dried after the dicing using N_2 gas and left on the dicing foil for storage and removed on demand.

4.4 NCG membranes

It has been shown that freestanding exfoliated graphene shows properties closer to the theoretical predictions than graphene in contact with, for example, SiO_2 [10, 106, 141]. To evaluate whether this also applies to the nanocrystalline graphene films developed in this work, a fabrication process for membranes without metal contacts was thus conceived. Membranes can also be used for nanoindentation measurements using AFM, providing mechanical properties [39, 41]. Also, Raman spectroscopy can be used to measure stress in graphene [142]. The aim is to compare the Raman spectra of the NCG before (stressed) and after (unstressed) membrane release, allowing estimation of the original film stress.

4.4.1 Fabrication summary

The fabrication process for the NCG membranes is illustrated in Figure 4.3, and a detailed process step listing is provided below. The back side oxide of the samples obtained from the preparation process, explained in Section 4.3, is first thickened by PECVD oxide deposition and subsequently patterned by reactive ion etching (RIE) to form the etch mask for the back side inductively coupled plasma (ICP) etching step. The wet thermal oxide of 245 nm alone would be too thin, making the PECVD oxide deposition

necessary. The samples are then diced into $10 \times 8\,\mathrm{mm}^2$ samples. This small sample size is necessary to fit into the *Veeco Multimode V* AFM and perform nanoindentation experiments. Dicing has to be done at this stage, as dicing of freestanding membranes would have a low yield. After ICP etching the membranes are released by HF vapor.

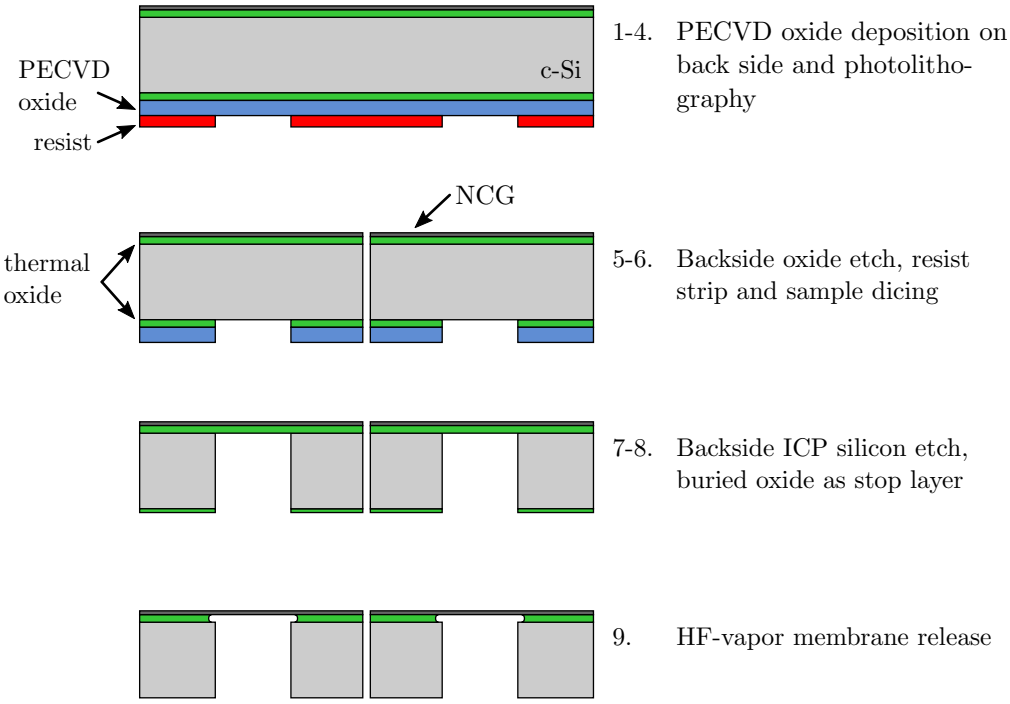


Figure 4.3: Fabrication process flow chart illustrating NCG membrane fabrication.

The full process involves one PECVD oxide deposition, one optical lithography, one RIE step, one ICP etch step and one HF vapor etch. Steps marked [B] are performed on the backside. Steps marked [*pending*] were not yet performed at the time of preparing this thesis.

	Step	***Details***
1.	**Cleaning**	Acetone/IPA
2.	**PECVD SiO_2 [B]**	Deposition conditions: • Substrate temperature: 350 °C • Gas flows and pressure: 4.2 sccm SiH_4, 80 sccm N_2, 350 sccm N_2O, 1000 mT • Plasma: 20 W RF power • Deposition duration: 51 min • Target thickness: 3000 nm
3.	**Cleaning**	Acetone/IPA

4. **Lithography [B]** — Thick positive resist AZ 9260:
   - Wafer dehydration: oven, 120 °C, 15 min
   - Spincoating: thickness of $\sim$ 5.1 µm measured by profilometer after development
   - Pre-exposure bake: hotplate, 110 °C, 2 min 30 s
   - Exposure: alignment to sample edges
   - Development: AZ726 MIF, 5 min
5. **RIE SiO_2 etch [B]** — Open PECVD and thermal SiO_2 ($\sim$ 3245 nm) until reaching bulk silicon
   - Gas flows and pressure: 38 sccm Ar, 12 sccm CHF_3, 30 mT
   - Plasma: 200 W RF power
   - Etch duration: 2 h 40 min
6. **RIE resist strip [B]** — Removal of residual resist (NCG on front not affected)
   - Gas flow and pressure: 100 sccm O_2, 200 mT
   - Plasma: 200 W RF power
   - Etch duration: 20 min
7. **Dicing** — Sample diced into $10 \times 8\,mm^2$ pieces (see Figure C.2 on page 146 for dicing pattern)
8. **Silicon ICP etch [B]** — Through-wafer etching using *Bosch process* until reaching buried thermal oxide [*pending*]
9. **HF vapor etching** — Membrane release [*pending*]

4.4.2 Fabrication details

Two fabrications steps require additional explanation. These are the through-wafer deep reactive ion etching (Step 8) and the HF vapor etching (Step 9).

4.4.2.1 Through-wafer inductively coupled plasma etching (Step 8)

The ICP silicon etch will likely suffer from microloading effects (different etch rates for different opening sizes). Alternatively, KOH etching from the back could be used in this process instead, since graphene is not etched by KOH solution [41]. The reason for choosing ICP etching was the availability of a suitable photolithographic mask.

4.4.2.2 HF vapor membrane release (Step 9)

In order to release the membranes, as shown in Figure 4.3, Step 9, the buried thermal oxide has to be selectively removed against carbon with minimal mechanical impact. This is achieved by vapor HF etching process [143]. This method does not require rinsing by DI and is thus expected to have a larger yield as compared to wet HF etching. The sample is exposed to HF vapor from the back side.

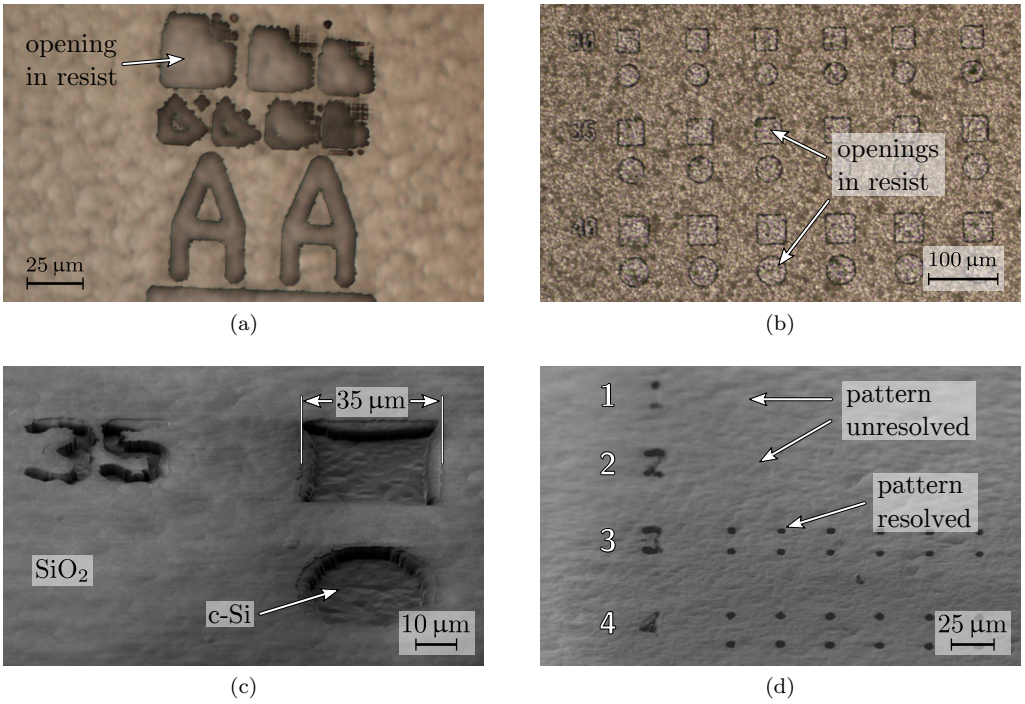


Figure 4.4: Microscope and SEM micrographs of resist and oxide mask patterned on unpolished backside. (a) Test pattern showing a lithography resolution of $\sim$ 3 µm. (b) Array of squares and circles with dimensions between 30 and 40 µm. (c) Square and circular pattern after RIE etching. (d) Square and circular pattern with diameter below 3 µm are not resolved.

Findings from the suspended beam process, which will be described in Section 4.5, show that HF vapor is able to penetrate NCG. Therefore, it should be also possible to carry out the HF vapor release step with the NCG facing towards the HF vapor. This could potentially minimize damage that might occur during sample unloading due to stiction.

4.4.3 Conclusion

At the time of preparing this thesis, the fabrication could not be completed due to the temporary unavailability of the *Bosch process* for the through-wafer etching. The backside hard mask was successfully patterned. A microscope image of the resolution test pattern of the resist mask on the unpolished back side is shown in Figure 4.4a. A resolution of 3 µm was achieved. The resist mask with regular square and circular pattern with diameters of 30, 35 and 40 µm before RIE etching is shown in Figure 4.4b. An SEM micrograph of a 35 µm large square and circle after successful RIE etching is shown in Figure 4.4c. In Figure 4.4d, the patterns with diameter of 1 to 4 µm after RIE etching are shown. Patterns down to 3 µm were resolved.

The AZ 9260 resist was peeling in some areas after development. This might be due to the unpolished backside surface of the silicon wafer available at that time. As a consequence, openings are not clearly defined after RIE etching (see Figure 4.4c). In

order to improve the resolution and the resist adhesion, double side polished wafers should be used.

4.5 Suspended Beam

As mentioned in Section 4.4, freestanding films are a great source of information. Mechanical properties can be extracted [39, 41], as well as thermal conductivity [43]. The latter is very interesting since the usage of graphene and graphene-like films in integrated circuits for thermal management is considered. Thus, in addition to the membrane fabrication mentioned in the previous Section 4.4, a fabrication process for suspended NCG beams is proposed. The electrically contacted NCG strips comprise also a back gate, allowing gate modulation experiments.

4.5.1 Fabrication summary

Figure 4.5 shows the schematic illustration of the suspended beam fabrication process. A detailed process step listing is provided below. First, the deposited NCG films are patterned into 20 µm long strips with widths of 6, 3 and 1 µm. Next, metal contacts and probe pads are aligned to the short edges of the strips and patterned by lift-off. Finally, HF vapor etching is used to remove the sacrificial oxide layer and suspending the strips.

The full process involves two optical lithography steps, one NCG plasma etching, one Ti/Au electron beam evaporation and one HF vapor etch. The optical Masks 1 and 2 used in this process are schematically illustrated in Figure 4.6. For the full mask design refer to Figure C.3 on page 148.

	Step	***Details***
1.	**Cleaning**	Acetone/IPA
2.	**Lithography 1**	Positive resist S1813: • Wafer dehydration: oven, 120 °C, 15 min • Spin coating: thickness ∼ 1.2 µm • Pre-exposure bake: hotplate, 90 °C, 2 min • Exposure: Mask 1, no alignment • Post-exposure bake: hotplate, 120 °C, 2 min • Development: MF319, 40 s
3.	**NCG oxygen plasma etch**	Remove exposed NCG • Gas flow and pressure: 20 sccm O_2, 20 mT • Plasma: 20 W RF power • Etch duration: see Table 4.1
4.	**NMP resist strip**	Remove residual resist, 1 h

5. **Lithography 2** — Negative resist AZ 2070:
   - Wafer dehydration: oven, 120 °C, 15 min
   - Spin coating: thickness ∼ 4.4 µm
   - Pre-exposure bake: hotplate, 110 °C, 1 min
   - Exposure: Mask 2, alignment to NCG pattern (Mask 1)
   - Post-exposure bake: 110 °C, 1 min
   - Development: AZ726, 1 min 20 s
6. **Metal evaporation** — Target material Ti/Au, target thickness 20/200 nm
7. **Lift-off process** — NMP
8. **RIE SiO_2 etch [B]** — Remove thermal SiO_2 (245 nm) to allow electrical contacting of substrate
   - Gas flows and pressure: 38 sccm Ar, 12 sccm CHF_3, 30 mT
   - Plasma: 200 W RF power
   - Etch duration: 20 min
9. **Contact annealing** — Improve contact between Ti/Au and NCG, 300 °C, 1 h

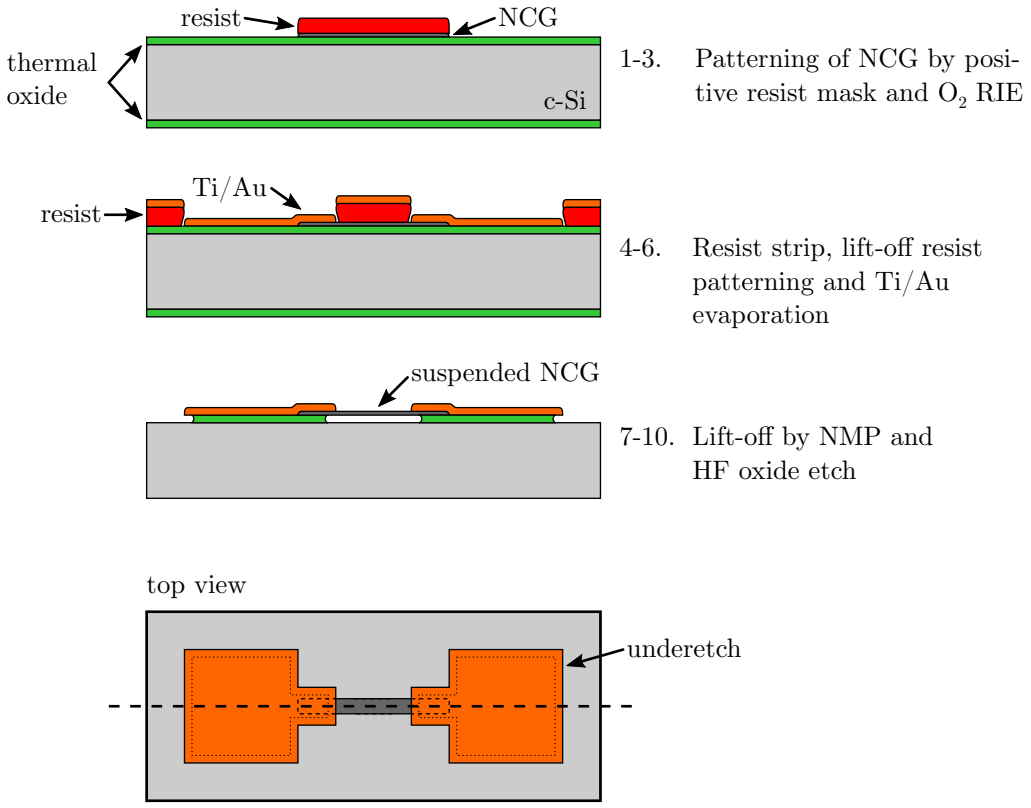
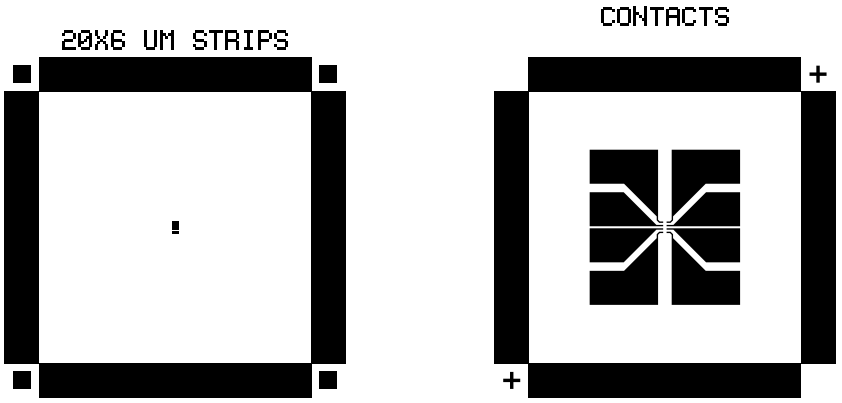


Figure 4.5: Fabrication process flow chart illustrating suspended NCG device fabrication. The NCG is patterned and contacted, and suspended by mask-less HF oxide etching. The amount of underetch is controlled by the etch duration.



(a) Mask 1 (b) Mask 2

Figure 4.6: Schematic illustration of mask used for suspended and top-gated structures. The full mask is shown in Figure C.3 on page 148. (a) Mask 1 provides four rectangles for patterning of NCG strips. (b) Mask 2 contains eight contact pads and contact leads matching the strips of Mask 1.

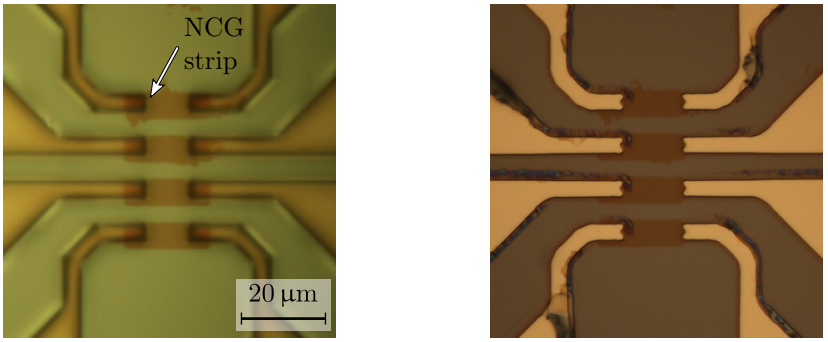
Sample	t_{etch} sec	d^{100}_{mean} nm
MSx12_3	600	35.5
MSx13_3	600	31.5
MSx14_3	400	18.0
MSx15_3	250	15.7
MSx16_3	50	3.0
MSx17_3	200	12.4
MSx18_3	200	8.9
MSx19_3	150	5.2

Table 4.1: Etch durations used in Step 3 of suspended NCG structures fabrication (Section 4.5) and Step 3 of top-gated structure fabrication (Section 4.6). The NCG thicknesses d^{100}_{mean} were obtained by ellipsometry as explained in Section 3.3.1 on page 51.

10. **HF vapor etching** Suspend NCG strip
    - substrate temperature: 40 °C
    - HF concentration: 48%
    - etch duration: 4 min

4.5.2 Fabrication details

Two fabrication steps will be described in more detail. These are the lithography for the Ti/Au lift-off (Step 5) and the HF vapor etching (Step 10).



(a) (b)

Figure 4.7: Contacting of NCG by Ti/Au lift-off. (a) After light-off lithography. (b) After Ti/Au evaporation and lift-off by NMP.

4.5.2.1 Lithography 2 (Step 5)

Negative resist (AZ 2070) is used because it gives a better retrograde resist edge profile compared to positive resist, which is necessary for successful lift-off. There were several issues during the lithography, and the lithography was performed three times before success. Four NCG strips ($20 \times 6\,\mu m$) are shown in Figure 4.7a after the lithography, and again in Figure 4.7b after the successful Ti/Au deposition and NMP lift-off.

A different issue during this lithography, but not related to resolution, was the lack of dedicated, pre-patterned alignment marks. The first lithography step (Step 2), used to pattern the NCG, is simultaneously used to pattern alignment marks. However, the NCG films on samples `MSx16_3` and `MSx19_3` were too faint to allow subsequent optical alignment, and could thus not be processed further than Step 4. To allow successful alignment of such thin films it would be necessary to perform an alignment mark patterning step before the NCG deposition. Due to the high NCG deposition temperatures, metal markers are not an option. Instead, patterning the thermal oxide by RIE is recommended.

4.5.2.2 HF vapor etching (Step 10)

A HF vapor phase etcher from *Idonus* [144] was used in this step. A trial vapor HF etch was performed on sample `MSx18_3`. `MSx18_3` was used because it has poor NCG–metal contact alignment and would thus be no big loss if unsuccessfully released.

Figure 4.8 shows a microscope image of an HF etched structure with $20 \times 6\,\mu m$ strips. It has a device identifier patterned above a frame, and comprises eight probe pads in the center (connected to the four NCG strips). Due to the mask design, a solid, 200 µm wide NCG strip is located on the left of the image. A small area of this solid NCG strip, which appears etched, is magnified for better visibility in the inset in Figure 4.8. A brighter area is present around five small Ti/Au particles which were deposited due to damage of the photolithographic mask. The SEM micrograph in the second inset of Figure 4.8 shows one of those Ti/Au particles. At the bottom of the micrograph a perforated

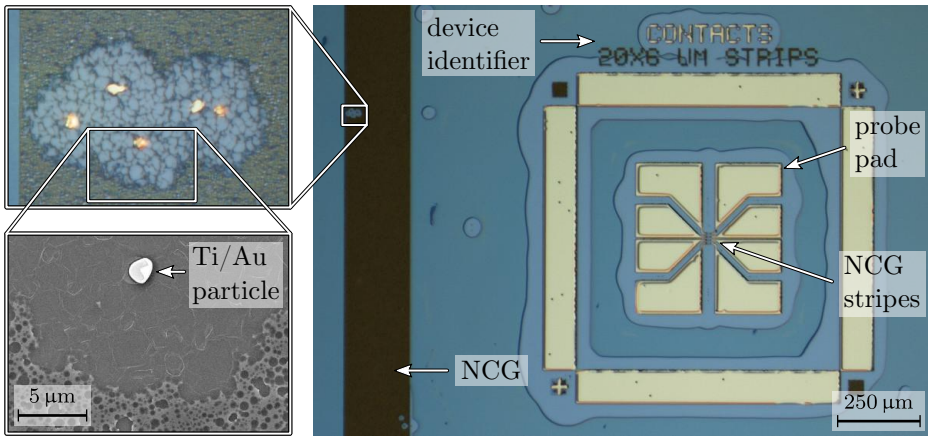


Figure 4.8: Results of HF vapor oxide etch of device `MSx18_3`. Optical microscope image of full device is shown on the right. A small part is magnified twice (see insets).

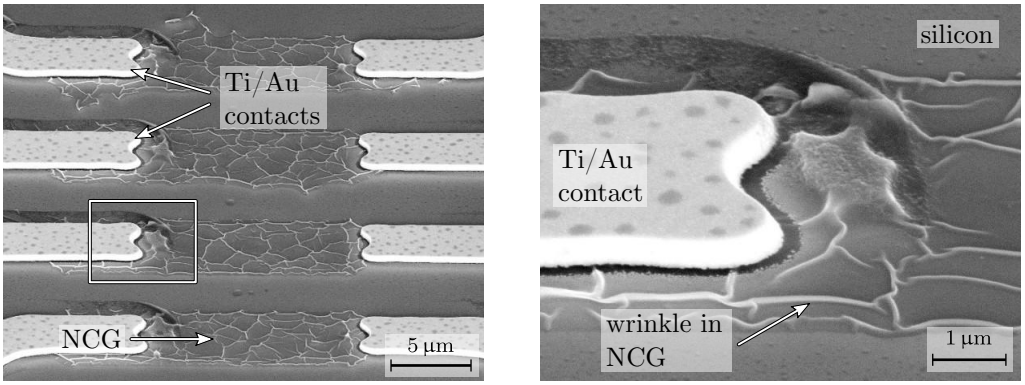
film is visible. This perforated film is the thermal oxide on which the NCG film was initially grown. Close to the Ti/Au particle the oxide had been etched completely. SEM investigation suggests that the oxide underneath the NCG was etched without damage to the NCG.

In the microscope image of the HF etched device shown in Figure 4.8, two different contrasts with clear, but irregular, borders are visible between the inner Ti/Au probe pads and the outer frame. This pattern does not correlate to any of the lithography steps used in this process. SEM and AFM investigation revealed that the areas closer to the Ti/Au are bare silicon (SiO_2 etched completely), while the areas further away ($> 50\,\mu m$) are not or only partially etched SiO_2. This indicates that the etch rate close to the Ti/Au structures was higher.

An SEM micrograph of the four NCG strips after the HF release is shown in Figure 4.9a, with the indicated area magnified in Figure 4.9b. It is clearly visible that the NCG strips exhibit wrinkles and are in direct contact with the silicon substrate. The Ti/Au contacts are also in direct contact; the gap of 245 nm is not present. A lack of vertical gap was further confirmed from the FIB cross section shown in Figure 4.10.

The fact that the NCG strips developed wrinkles after the release suggests that as-deposited NCG films on SiO_2 had compressive stress. The sacrificial oxide thickness is too small, and the structures stick down despite the use of HF vapor etching. Several wrinkles were analyzed by AFM and wrinkle heights between 50 and 170 nm were observed.

To determine the etch rate of the HF vapor etching, an FIB cross section was performed on the edge region of a $100 \times 100\,\mu m$ contact pad. An SEM micrograph of the cross section is shown in Figure 4.10. The inset clearly shows the unetched thermal oxide to the left, and partially etched oxide to the right. The perpendicular distance between the metal pad edge and this transition of the thermal oxide is $\sim 9.5\,\mu m$. The etch rate is thus $\sim 2.4\,\mu m/min$, which is much higher than previously reported etch



(a) (b)

Figure 4.9: SEM micrographs of suspended beam device `MSx18_3` after HF release. (a) Four contacted NCG strips and (b) closeup of area indicated in (a). The NCG sticks down onto the silicon substrates, and wrinkle formation in the NCG is visible.

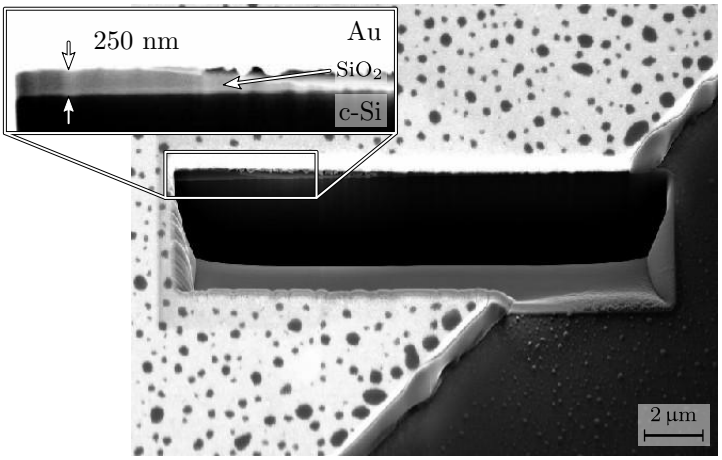


Figure 4.10: SEM micrograph of FIB cross section through Ti/Au probe pad illustrating the amount of underetch.

rates of 15 nm/min for thermal oxide [145] and 166-220 nm/min for tetraethyl orthosilicate (TEOS) [143, 145]. The effect which leads to the apparent higher etch rate close to the Ti/Au particles is not entirely understood. Two possibilities are considered: (i) The particles act as local heat sinks (the HF vapor etch rate increases with decreasing temperature) or (ii) a catalytic reaction occurred. However, reported titanium etch rates in HF are very slow [145] with no indication of a catalytic effect. These results are inconclusive and further work should be carried out to investigate the higher etch rates close to the metal.

4.5.2.3 Raman characterization of HF vapor etched NCG

Raman spectroscopy was performed on NCG strips after HF etching (sample `MSx18_3`) and compared to the results obtained on the unprocessed reference sample `MSx18_4`.

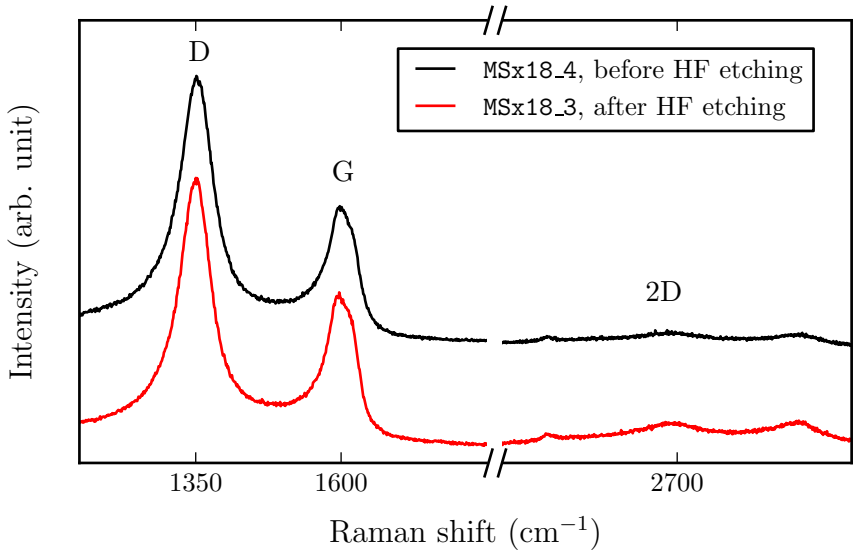


Figure 4.11: Raman spectra of NCG before HF vapor etching (`MSx18_4`) and after (`MSx18_3`). The latter was taken on the topmost NCG strip visible in Figure 4.9a.

Figure 4.11 shows these spectra for the relevant ranges. The peak intensity ratio I_D/I_G obtained through curve fitting is 1.91 and 1.68 for `MSx18_4` and `MSx18_3`, respectively. This is a decrease of 12%, while the I_{2D}/I_G ratio increased by 52% (from 0.089 to 0.135). This might be due to the stress release after the HF etching.

The curve fitting also provides the peak location, which has been demonstrated to change due to applied stress [142, 146–148]. The 2D peak of exfoliated graphene ($\sim 2700\,\mathrm{cm}^{-1}$) exhibits a red shift (reduction of Raman shift) on applied tensile stress. The G peak ($\sim 1580\,\mathrm{cm}^{-1}$) shows the same behavior with an additional split of the single peak into a G^+ and G^- peak. Here, the G peak shows a red shift of $5 \pm 2\,\mathrm{cm}^{-1}$ after HF vapor etching, which suggests that the as-deposited film had an initial blue shift due to compressive stress. However, the 2D peak exhibits an opposite trend. The peak shifted $10 \pm 4\,\mathrm{cm}^{-1}$ to the right after etching, which would mean that the as-deposited film had a tensile stress. Using the reported shift rate of $1.9 \pm 0.4\,\mathrm{cm}^{-1}/\mathrm{GPa}$ [142], the compressive stress of the NCG on wafer `MSx18` is $10.3 \pm 5.8\,\mathrm{GPa}$ based on the G peak.

It is expected that this inconclusive observation (G and 2D peak shift in opposite directions) can be better understood with further Raman results obtained on properly suspended films, without any stiction to the silicon substrate. Localized stress due to wrinkles is also likely to influence the Raman investigation. To achieve properly suspended structures, the oxide thickness should be increased.

4.5.3 Electrical characterization

The devices on sample `MSx08_3` were electrically characterized after the HF vapor etching even though the NCG strips were not suspended. The I_D–V_D results for one such device

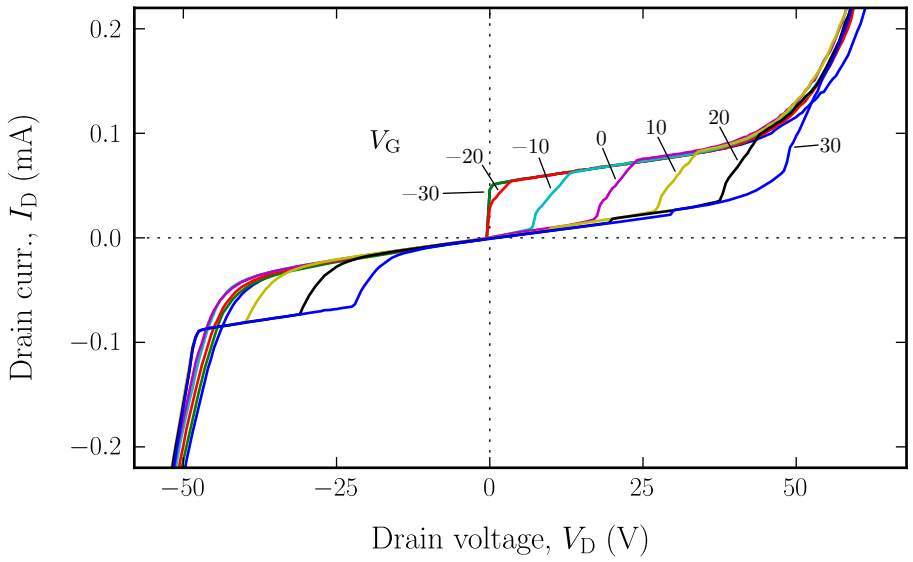


Figure 4.12: I_D–V_D measurements results of $20 \times 1\,\mu m^2$ strip (`MSx18_3`) after HF vapor etching. Back gate voltage V_G applied to the bulk sample.

are shown in Figure 4.12 with different back gate voltages V_G applied. These results are reproducible, and similar characteristics were observed for all other devices. These results strongly resemble Schottky diode characteristics. Two possible explanations are considered: (i) A Schottky contact is formed between the Ti/Au contacts and the NCG during the HF etching, or (ii) the Schottky contact exists between the Ti/Au contacts and the silicon substrate.

In Figure 4.9a it is visible that the entire contact area between the NCG and the Ti/Au is underetched. Furthermore, it has been concluded that NCG is permeable to HF vapor. As a consequence, it must be assumed that the whole contact area was affected by HF. It is unclear what effect exactly this might have on the NCG–Ti/Au interface, but formation of a Schottky contact has to be considered as one of the possibilities. To avoid this kind of complications, future device mask designs should be modified as schematically illustrated in Figure 4.13. The current design (see also Figure C.3 on page 148) was originally designed to allow contacting of FIB-fabricated structures. The design goal was to achieve a high device density, and as a consequence the contact area between the NCG and the Ti/Au is very small and readily underetched by HF vapor etching. An improved mask design would comprise sufficiently enlarged contact areas. This would solve two problems: (i) During HF vapor etching most of the contact area would stay unaffected due to the larger contact size, thus ensuring good contact, and (ii) the requirements on the optical mask alignment accuracy during lithography would be greatly reduced.

The second possible explanation for the Schottky contact characteristics is a contact between the silicon substrate and the Ti/Au contacts. As can be seen in Figure 4.10, the underetched Ti/Au bends down and is in contact with the silicon substrate. By

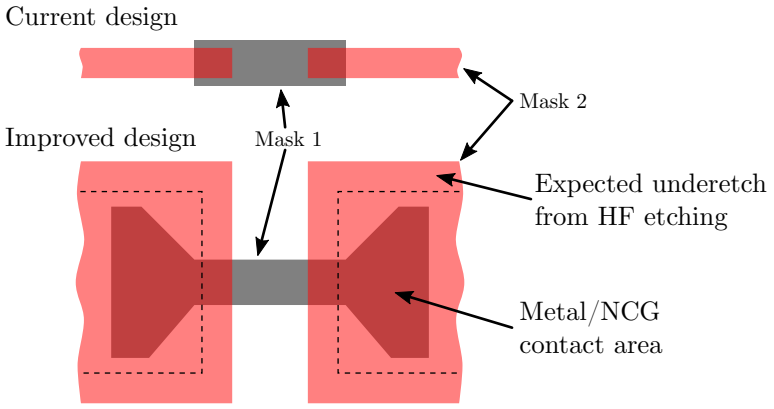


Figure 4.13: Schematic illustration of proposed improved mask design. The larger overlap between NCG and metal ensures good contact even after HF vapor etching.

increasing the oxide thickness, which was identified as necessity for successful device fabrication before, this contact can be avoided. Therefore, by fabricating structures with thick oxide ($\sim 3\,\mu m$) using both, the current (HF influence on contact area expected) and the improved mask design (contact area protected from HF), the origin of the Schottky contact characteristics could be identified.

4.5.4 Conclusion

The suspended beam fabrication described in this section was not entirely successful, as the NCG beams were not suspended but rather stuck down. The main reason for this is the very small sacrificial oxide thickness (245 nm). Nevertheless, valuable results were obtained. Firstly, it has been shown that NCG films are compressive, as evidenced by the wrinkle formation after the HF vapor oxide etch. Secondly, Raman spectra of the unstressed NCG after HF vapor release show lower disorder (D peak) and higher 2D peak intensities, as well as a red shift of the G peak. Finally, unexpectedly high HF etch rates of $\sim 2.4\,\mu m$/min were obtained close to Ti/Au, while oxide away from metal was etched much slower.

For a future revision of this fabrication process it is suggested to increase the sacrificial oxide thickness. Furthermore, an improved mask design (as proposed in Figure 4.13) should be considered. A larger range of beam lengths and widths should be implemented as well. It should be also evaluated whether liquid HF etching with consecutive critical point drying can be an option.

4.6 Top gated NCG

In the previous Section the fabrication and characterization of suspended beam devices was reported. These structures are basic TFT structures with NCG connecting the source and drain contacts and a gate realized by the handle wafer. They comprise a

gate oxide with a thickness of 245 nm and do not have a counter electrode on top. Thus, a weak gate voltage modulation of the source–drain voltage is possible due to the limited gate field penetration [149]. To investigate whether NCG devices indeed suffer from the described effect, structures were fabricated comprising an additional top gate with a 100 nm PECVD gate oxide.

4.6.1 Fabrication summary

The fabrication process flow chart is shown in Figure 4.14 and a detailed list of the fabrication steps is provided below. After NCG patterning and contacting by Ti/Au lift-off (Step 1-7, identical to the suspended beam process), a PECVD oxide is deposited and patterned to form the top gate oxide (Step 8-14). Finally, the top gate is realized by Ti/Au lift-off (Step 15-19). The full process involves four optical lithography steps, one NCG plasma etching, two Ti/Au electron beam evaporations, one PECVD oxide deposition and two RIE oxide etching. The optical masks used are schematically illustrated in Figure 4.6 on page 76 and in Figure 4.15. Details and the full mask layout can be found in Appendix C.4 on page 147.

	Step	***Details***
1.	**Cleaning**	Acetone/IPA
2.	**Lithography 1**	Positive resist S1813: • Wafer dehydration: oven, 120 °C, 15 min • Spincoating: thickness ∼ 1.2 µm • Pre-exposure bake: hotplate, 90 °C, 2 min • Exposure: Mask 1, no alignment • Post-exposure bake: hotplate, 120 °C, 2 min • Development: MF319, 40 s
3.	**NCG oxygen plasma etch**	Remove exposed NCG • Gas flow and pressure: 20 sccm O_2, 20 mT • Plasma: 20 W RF power • Etch duration: see Table 4.1 on page 76
4.	**NMP resist strip**	Remove residual resist, 1 h
5.	**Lithography 2**	Negative resist AZ 2070: • Wafer dehydration: oven, 120 °C, 15 min • Spincoating: thickness ∼ 4.4 µm • Pre-exposure bake: hotplate, 110 °C, 1 min • Exposure: Mask 2, alignment to NCG pattern (Mask 1) • Post-exposure bake: 110 °C, 1 min • Development: AZ 726, 1 min 20 s
6.	**Metal evaporation**	Target material Ti/Au, target thickness 20/200 nm
7.	**Lift-off process**	NMP

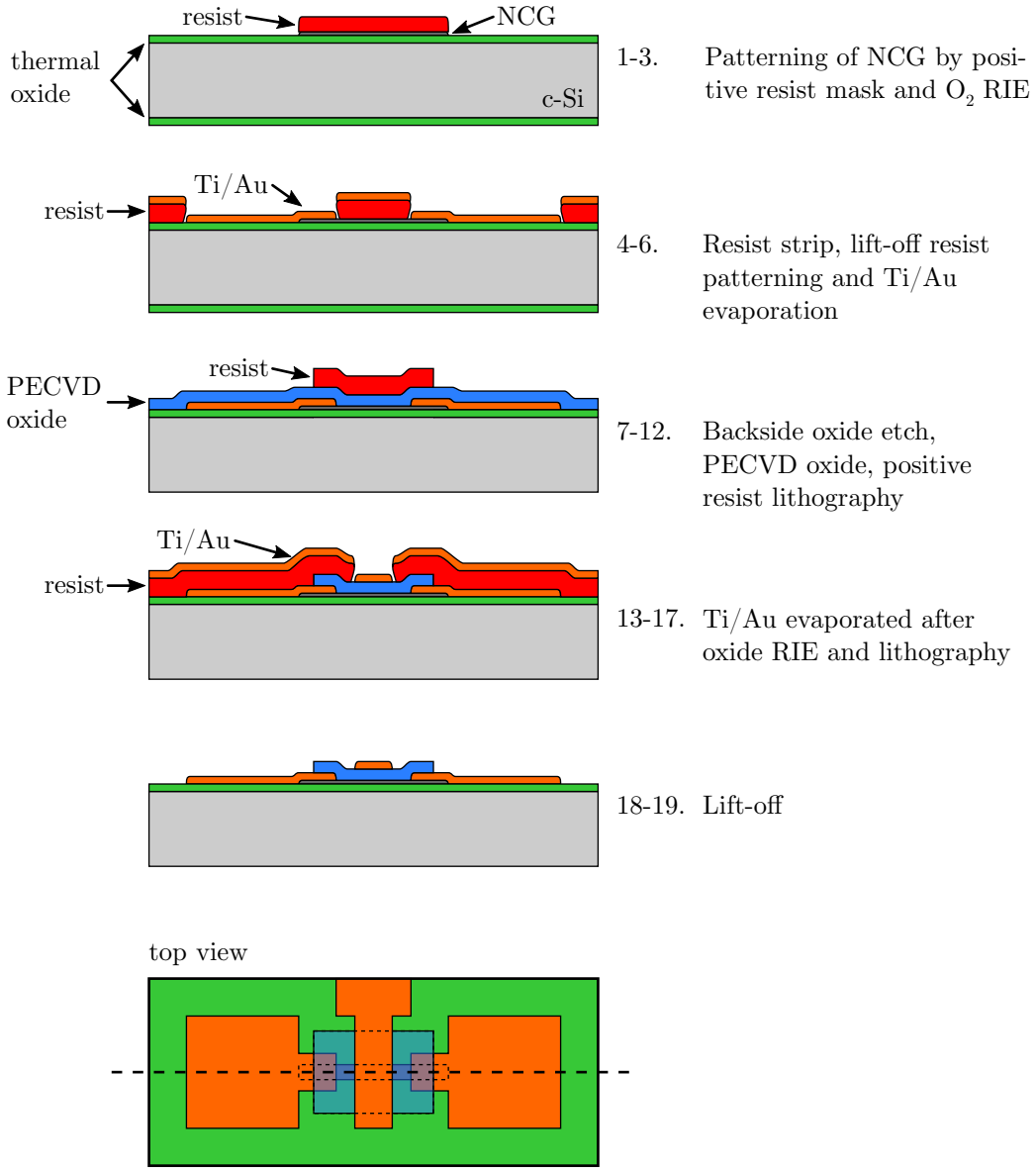
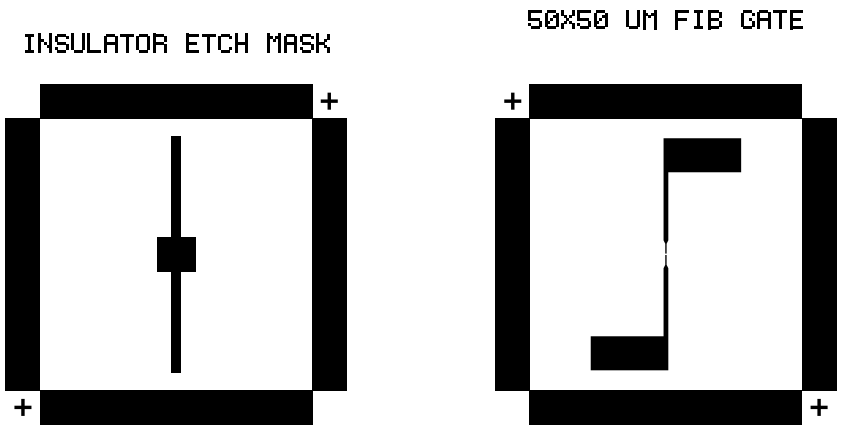


Figure 4.14: Fabrication process flow chart illustrating NCG top gate device fabrication. The NCG is patterned and contacted. After oxide passivation a Ti/Au top gate is deposited above the channel by lift-off. PECVD oxide is transparent in top view for clarity.

8. **RIE SiO_2 etch [B]** Remove thermal SiO_2 (245 nm) to allow electrical contacting of substrate
   - Gas flows and pressure: 38 sccm Ar, 12 sccm CHF_3, 30 mT
   - Plasma: 200 W RF power
   - Etch duration: 20 min
9. **Contact annealing 1** Improve contact between Ti/Au and NCG, 300 °C, 1 h



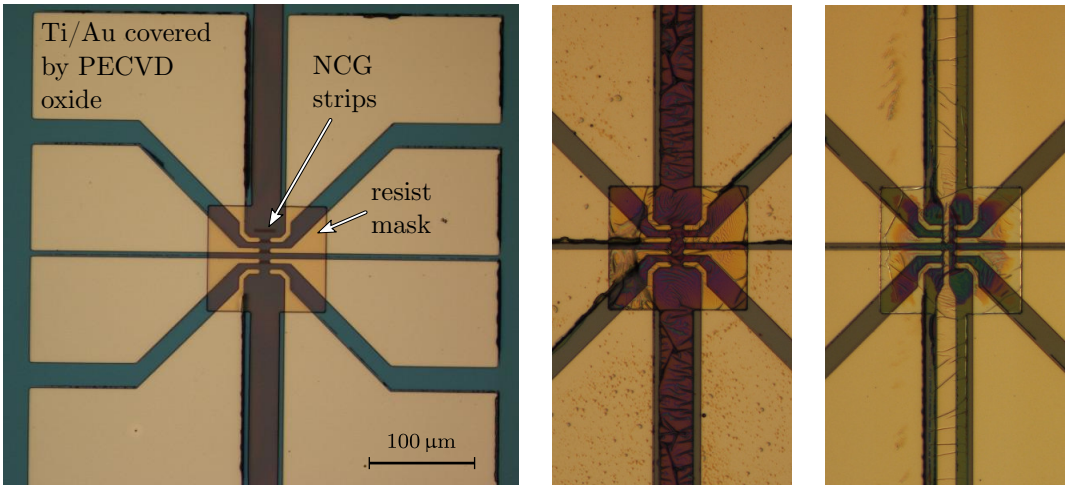
(a) Mask 3 (b) Mask 4

Figure 4.15: Illustration of masks used for top-gated structures in addition to the masks shown in Figure 4.6. (a) Mask 3 is used as etch mask to maintain protection of the NCG strips while opening the contact pads. (b) Mask 4 contains the top gate patterned by lift-off.

10.	**PECVD SiO_2**	Deposition conditions: • Substrate temperature: 350 °C • Gas flows and pressure: 4.2 sccm SiH_4, 80 sccm N_2, 350 sccm N_2O, 1000 mT • Plasma: 20 W RF power • Deposition duration: 2 min • Target thickness: 100 nm
11.	**Cleaning**	Acetone/IPA
12.	**Lithography 3**	Same as Step 2, Mask 3, alignment to existing structures
13.	**RIE SiO_2 etch**	Same as Step 8, etch duration 5 min
14.	**NMP resist strip**	Remove residual resist, 30 min
15.	**Cleaning**	Acetone/IPA
16.	**Lithography 4**	Same as Step 5, Mask 4, alignment to existing structures
17.	**Metal evaporation**	Target material Ti/Au, target thickness 20/200 nm
18.	**Lift-off process**	High purity acetone
19.	**Contact annealing 2**	Same as Step 9

4.6.2 Gate oxide deposition and patterning (Step 10-13)

Adhesion between silicon dioxide and noble metals is generally weak, making it necessary to use Cr or Ti as adhesion layer. In the fabrication process described in this Section, a



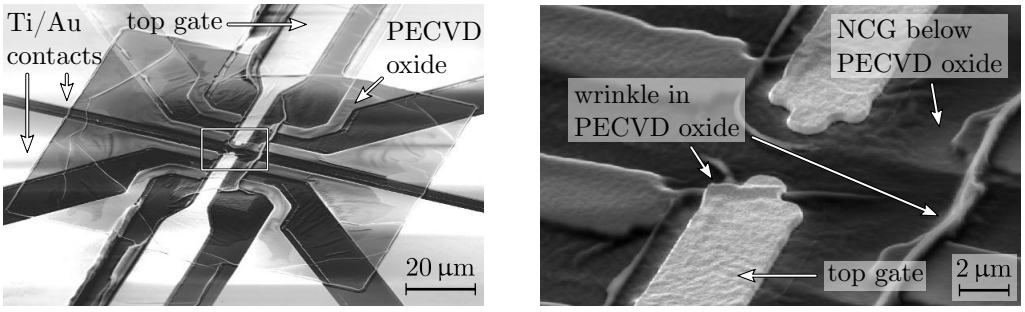
(a) (b) (c)

Figure 4.16: Optical microscope images showing the top gate fabrication steps. (a) A positive resist mask is patterned on top of the PEVCD oxide. (b) After RIE and resist strip cracking of the PECVDE oxide is visible. (c) The same device as (b) after top gate lift-off process.

100 nm thin PECVD oxide is deposited at 350 °C directly on top of the previously patterned Au structures. Gold areas (contact pads) larger than 100 µm have been covered. Thus, it was expected that peeling of the oxide might occur due to stress induced into the oxide/Au interface during the deposition.

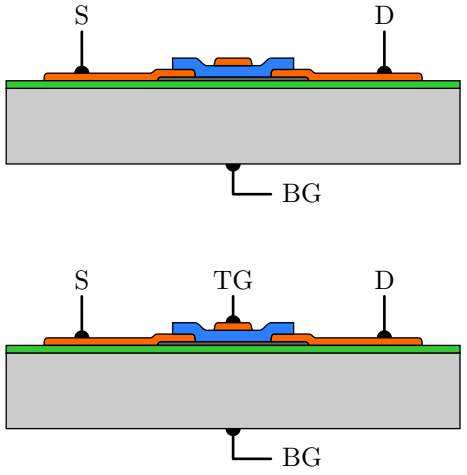
A device with the gate oxide deposited (Step 10) and the resist mask patterned (Step 12) is shown in Figure 4.16a. The oxide film is very uniform and no delamination is observed. The same structure is shown again after the RIE oxide etch (Step 13) and the NMP resist strip (Step 14) in Figure 4.16b. The oxide surface is not smooth and delamination of the PECVD oxide occurred. It is not clear at which stage this deterioration occurred, since no observation by microscopy was done until after the NMP strip. In case the damage to the oxide occurred during the NMP strip, an alternative resist removal process using acetone and IPA could be used. Using an oxygen plasma resist strip would be possible as well, since the NCG is protected by oxide. However, in Step 18 either acetone or NMP has to be used for the metal lift-off. Thus switching Step 14 to dry resist stripping would be of little merit.

The device fabrication was continued, and the Ti/Au top-gate was successfully patterned despite the wrinkles of the PECVD oxide. A microscope image of the channel region after successful fabrication is shown in Figure 4.16c. SEM micrographs of the patterned gate oxide after top gate patterning are shown in Figure 4.17a. The wrinkles of the PECVD oxide are clearly visible, however, no cracking of the oxide layer is observed. The Ti/Au top gate is continuous despite the wrinkles, and device fabrication is successful, as shown in the magnified micrograph in Figure 4.17b.



(a) (b)

Figure 4.17: SEM micrograph of fabricated top gated structures. (a) PECVD oxide covering channel area. (b) Closeup of the area indicated in (a). Wrinkles of the PECVD oxide are visible. V_{TG}



Strategy S1
Measurement: I_{D}–V_{D}
Variable: V_{BG}

Strategy S2
Measurement: I_{D}–V_{D}
Variable 1: V_{TG}
Variable 2: $V_{\mathrm{BG}} = \{-40, 0, +40\}$ V

Figure 4.18: I_{D}–V_{D} measurement strategies for top gated structures. For **Strategy S1** I_{D}–V_{D} is measured for different back gate voltages V_{BG} (top gate not used). **Strategy S2**: I_{D}–V_{D} measured as function of top gate voltage V_{TG} three times with back gate biased at -40, 0 and $+40$ V, respectively.

4.6.3 Electrical characterization

The successfully fabricated structures were electrically characterized using a probe station and an *Agilent B1500A Semiconductor Device Analyzer*. The fabricated structures were measured according to two measurement strategies, in order to determine whether there is any difference between the top and bottom gate biasing. These two strategies, henceforth called S1 and S2, are illustrated in Figure 4.18. First, the top gate is ignored for strategy S1, and I_{D}–V_{D} measurements with variable back gate biasing are carried out. For measurements according to strategy S2, the top gate is used for I_{D}–V_{D} modulation. This measurement is performed for three different back gate potentials V_{BG}.

Device		d_{NCG} (nm)	R (kΩ)	$R_\square$ (kΩ/□)	M_{BG} (%)	M_{TG} (%)
MSx12_1	Dev1	35.5	10.78	2.3 ± 0.2	0.14	1.73
	Dev2		10.58	2.3 ± 0.2	0.16	0.44
MSx13_1	Dev1	31.5	22.06	4.7 ± 0.5	0.37	1.22
	Dev2		22.79	4.9 ± 0.5	0.21	0.57
MSx15_1	Dev1	15.7	38.08	8.2 ± 0.8	0.49	1.39
	Dev2		37.88	8.1 ± 0.8	0.89	0.98
MSx17_1	Dev1	12.4	78.62	16.9 ± 1.7	0.74	2.76
	Dev2		84.22	18.1 ± 1.9	0.67	1.79

Table 4.2: Measured channel resistances R and calculated sheet resistances $R_\square$ of top gated structures. NCG strip dimensions obtained from SEM micrographs are 13 ± 0.25 and 3 ± 0.25 µm for length and width, respectively. M_{BG} and M_{TG} are the channel modulation for back and top gate, respectively. NCG thickness d_{NCG} as obtained from ellipsometry given for reference.

4.6.3.1 Results

Two NCG devices with 3 µm wide NCG strips were measured on each sample. These two devices are located next to each other and have a common top gate. Out of the six samples that were successfully fabricated (MSx12_1, MSx13_1, MSx14_1, MSx15_1, MSx17_1, MSx18_1), only four showed electrical conduction.

The source–drain current I_D was limited to ±30 µA in all measurements, and the drain voltage V_D is sweeped from −10 V to 10 V in steps of 50 mV. The I_D–V_D results of all devices show metallic characteristics without offset, and linear least square fitting was used to obtain channel resistances. The fitting results for all measured devices following strategy S1 with $V_{BG} = 0$ V are provided in Table 4.2. Dev1 and Dev2 refer to the measured NCG strips which are in the same location on all four samples. These two top gated NCG strips of sample MSx17_1 are visible in Figure 4.16a and Figure 4.17a; Dev1 is the top device, Dev2 is the second from top. Dev2 is also visible in Figure 4.17b (top device). The sheet resistances listed in Table 4.2 were calculated based on NCG strip dimensions obtained from SEM micrographs. Detailed electrical results of sample MSx12_1 and MSx17_1 are shown in Figure 4.19 and 4.20, respectively.

In addition, the influence of the NCG thickness on the gate modulation effect was investigated. For this purpose the channel modulation effect (in %) was calculated by

$$M = \frac{R_{max} - R_{min}}{R_{mean}} \times 100 \tag{4.1}$$

with R the channel resistance. The results are shown in Table 4.2 and visualized in Figure 4.21.

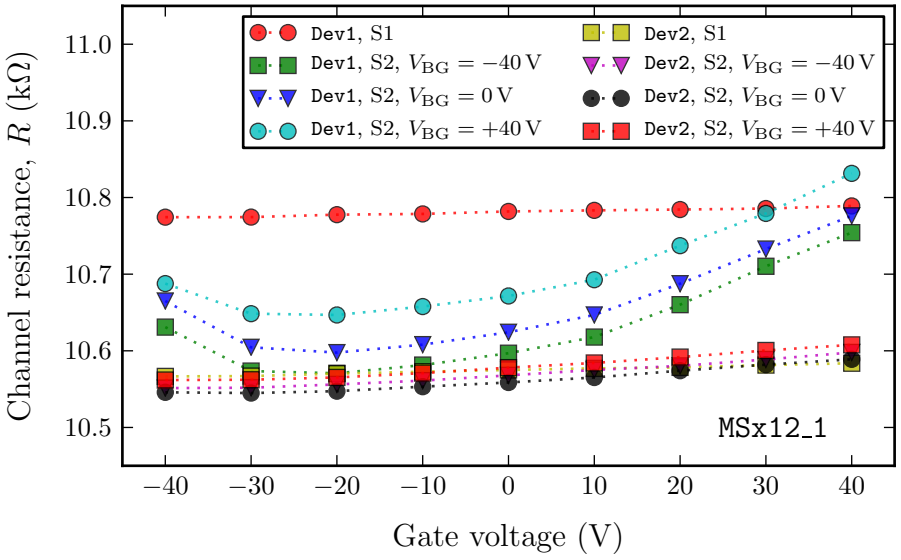


Figure 4.19: Channel resistance fit results for sample `MSx12_1`. The gate voltage is top gate or back gate, depending on the measurement. Example "`Dev1`, S2, $V_{BG} = -40$ V": gate voltage (x-axis) is applied to top gate (V_{TG}); the back gate voltage V_{BG} is fixed at -40 V.

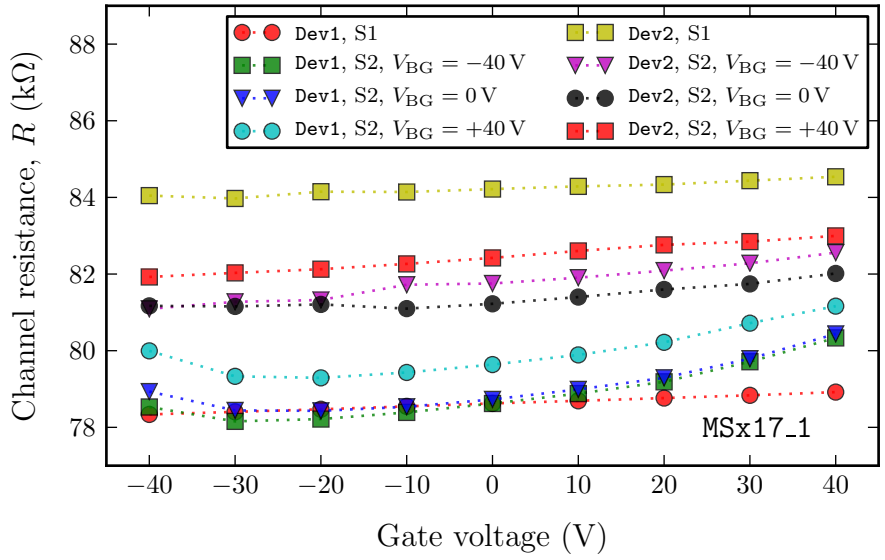


Figure 4.20: Channel resistance fit results for sample `MSx17_1`. The gate voltage is top gate or back gate, depending on the measurement. Example "`Dev1`, S2, $V_{BG} = -40$ V": gate voltage (x-axis) is applied to top gate (V_{TG}); the back gate voltage V_{BG} is fixed at -40 V.

4.6.3.2 Discussion

Several observations can be made regarding the obtained channel resistances shown in Figure 4.19 and 4.20.

1. The top gate modulation effect is stronger than the back gate modulation effect for all devices. This is especially apparent for `MSx12_1`, `Dev1` and `MSx17_1`, `Dev1`.

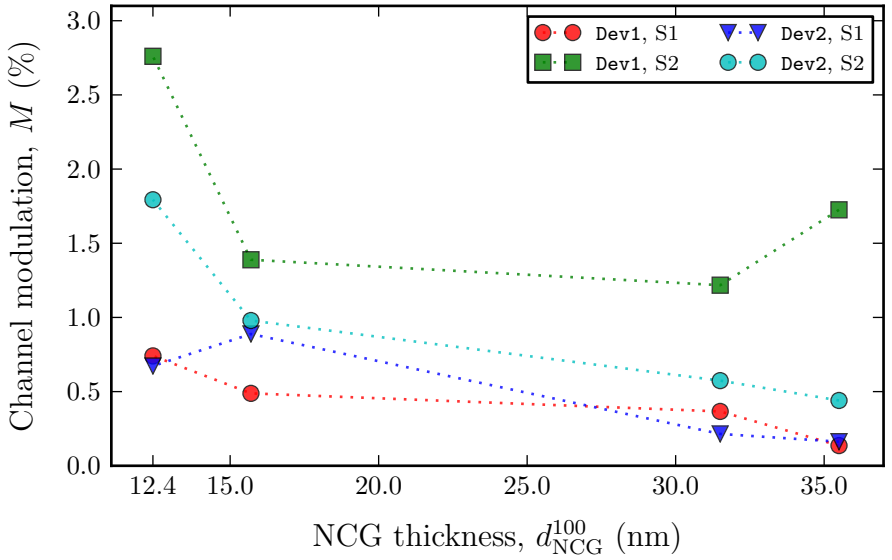


Figure 4.21: Calculated channel modulation for different NCG thicknesses and different measurement strategies. For strategy S2, the strongest modulation value of the three measurements is used. Modulation increases with decreasing NCG thickness.

2. The modulation effect is not linear for `Dev1` on both samples shown in Figure 4.19 and 4.20, respectively (increasing resistance for $V_{TG} = -40\,V$). This effect is also observed for the results of `Dev1` on sample `MSx13_1` and `MSx15_1` (not shown).

3. Discrepancy between strategy S1 and S2: The results obtained following strategy S2 with $V_{TG} = V_{BG} = 0\,V$ do not always match the results following strategy S1 with $V_{BG} = 0\,V$ (compare, for example, red circle and blue triangle in Figure 4.16a). This might be due to the undefined top gate potential during measurements following strategy S1.

4. Figure 4.21 shows that the channel modulation increases for decreasing NCG thicknesses.

5. The physical top gate geometry is different for `Dev1` and `Dev2`, respectively. For `Dev1` the top gate reaches completely over the channel, while for `Dev2` the top gate ends close to the edge of the NCG strip. See Figure 4.16c and Figure 4.16a.

These observations follow expected characteristics. Since the top gate has a thickness of 100 nm (compared to bottom gate thickness of 245 nm), a stronger modulation effect was expected. The positive Gaussian-like shape of the channel resistance modulation by a gate field for exfoliated graphene [4, 26, 106] was not observed for NCG. Possible explanations are the relative thick NCG films used here and the crystal structure of the NCG. Measurements were limited to $\pm 40\,V$ so the further trends of the channel resistances could not be investigated. As mentioned in Section 4.5.2.1 on page 77, the

samples with thinner films (e.g. `MSx_16` with 3 nm thin NCG) could not be used for fabrication due to the lack of dedicated alignment marks. The clear trend visible in Figure 4.21, however, suggests that thinner NCG thicknesses might exhibit characteristics closer to few layer graphene.

4.6.4 Conclusion

In this Section, the successful fabrication of top gated NCG structures was reported. The deposited PECVD top oxide developed wrinkles after patterning and resist strip, however, no cracking occurs and device functionality is not significantly affected. It has been shown that the top gate has a stronger modulation effect on the channel resistance than the back gate. The observed non-linear modulation for some devices is likely to be related to the top gate shape. Results indicate that a reduced NCG thickness results in a stronger gate modulation effect. Samples with NCG as thin as 3 nm were processed but could not be fabricated, due to the lack of dedicated alignment marks. Further work should be carried out to modify the fabrication process to include alignment structures and to optimize the top gate deposition process to avoid wrinkle formation. Devices with different dimensions (both NCG stip and top gate) would also provide additional insight.

4.7 NCG nanowire devices

In Section 2.6.5 on page 32, a method was introduced that allows nanowire to be formed with dimensions much smaller than the available lithography resolution. It was furthermore concluded that this kind of process is only feasible with thicker films. The NCG films developed in this work are thus suitable for such fabrication. A fabrication process for such nanowire devices, based on the NCG films developed in this work (and suitable for this kind of fabrication due to the large range of thicknesses possible), is proposed in this Section.

4.7.1 Fabrication summary

The fabrication process flow chart for this process is shown in Figure 4.22, and the detailed process step listing is provided below. First, trenches are etched into the top thermal oxide using RIE, followed by the full-wafer NCG deposition. Then, selected areas are covered by resist and the anisotropic NCG etch is carried out to form the nanowires. Finally, Ti/Au contacts are patterned using lift-off, and the oxide on the backside is removed. The optical mask set used for the fabrication was designed by Dr Kai Sun during his PhD work in Southampton [150]. The full process involves three optical lithography steps, one PECVD NCG deposition, one NCG plasma etching, one RIE oxide etching and one Ti/Au electron beam evaporation.

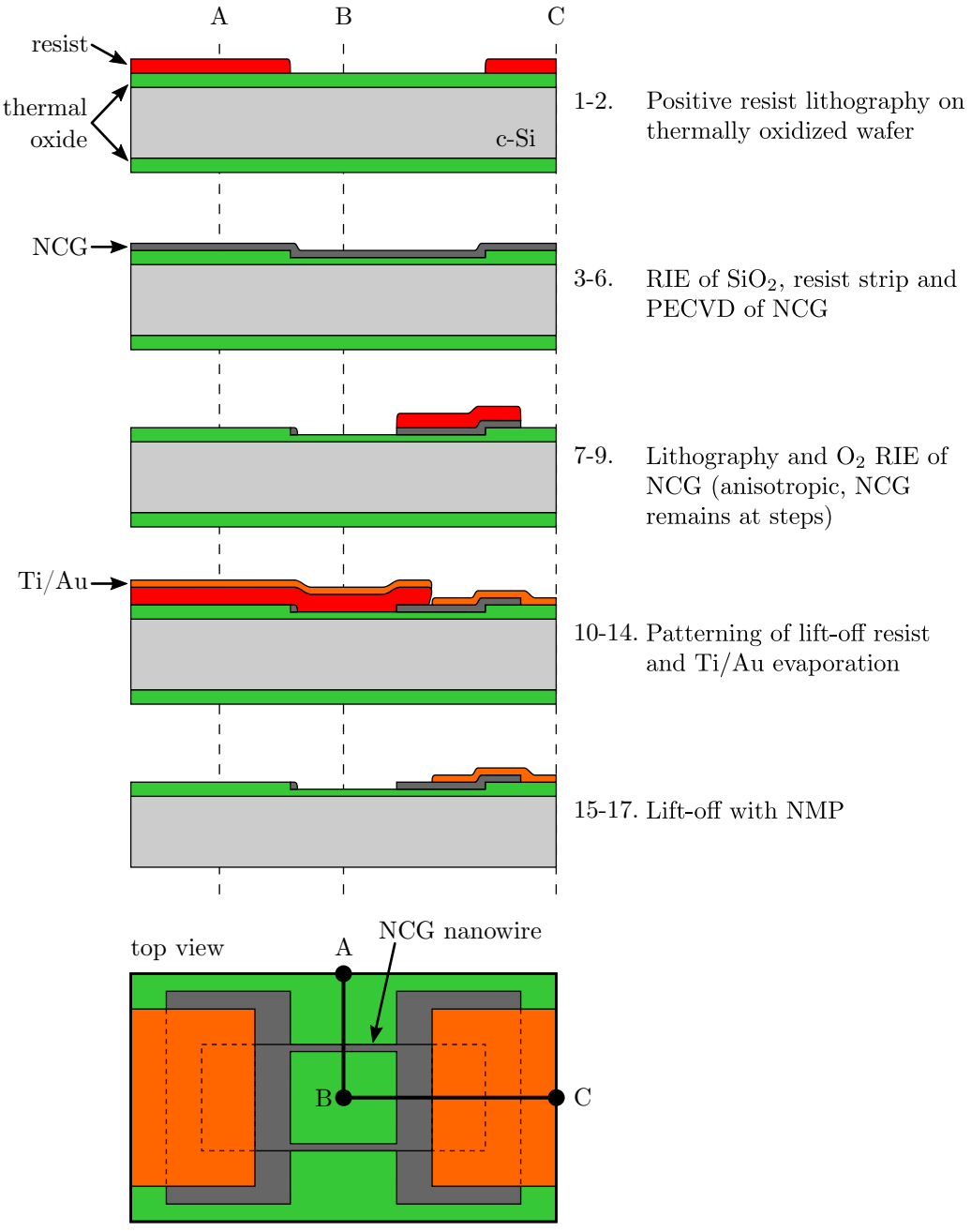


Figure 4.22: Fabrication process flow chart illustrating NCG nanowire device fabrication. The nanowires are formed in step 3, relying on the fact that the vertical thickness of the NCG is larger at steps. The top view shows the device of step 5.

Wafer	T_{dep} (°C)	t_{heat} (min)	t_{dep} (min)	t_{cool} (min)	$F[H_2]$ (sccm)	$F[CH_4]$ (sccm)	d_{NCG} (nm)	t_{etch} (s)
`MSx20`	900	15	15	15	75	60	37.5 ± 0.5	40
`MSx21`	900	15	15	15	75	30	28 ± 0	32
`MSx22`	850	12	15	12	75	60	16.75 ± 0.25	22
`MSx23`	800	8	15	8	75	60	30.5 ± 1.5	42

Table 4.3: Conditions used for nanowire devices fabrication. See Figure 3.2 on page 41 for parameter explanation concerning PECVD deposition of NCG. Flow rates F are applied during the deposition step. Hydrogen flow during heat-up and 10 min pre-clean is fixed at 100 sccm. NCG thicknesses were measured in three points (center, right, bottom) using ellipsometry. t_{etch} is the oxygen plasma etch duration applied in Step 9.

	Step	***Details***
1.	**Cleaning**	Fuming nitric acid, 15 min
2.	**Lithography 1**	Positive resist S1813: • Wafer dehydration: oven, 120 °C, 15 min • Spincoating: thickness ~ 1.2 µm • Pre-exposure bake: hotplate, 90 °C, 2 min • Exposure: alignment to wafer flat • Post-exposure bake: hotplate, 120 °C, 2 min • Development: MF319, 40 s
3.	**RIE SiO_2 etch**	Etch ~ 100 nm into thermal oxide • Gas flows and pressure: 38 sccm Ar, 12 sccm CHF_3, 30 mT • Plasma: 200 W RF power • Etch duration: 5 min
4.	**Oxygen plasma resist strip**	Removal of residual resist, 6 min
5.	**Cleaning**	Fuming nitric acid, 15 min
6.	**NCG PECVD**	Deposition conditions and resulting film thicknesses see Table 4.3
7.	**Cleaning**	Acetone/IPA
8.	**Lithography 2**	Same as Step 2
9.	**NCG oxygen plasma etch**	Etch NCG anisotropically, nanowires formed at oxide steps • Gas flow and pressure: 20 sccm O_2, 20 mT • Plasma: 300 W RF power • Etch duration: t_{etch}, see Table 4.3
10.	**NMP resist strip**	Remove residual resist, 5 min

11.	**Cleaning**	Acetone/IPA
12.	**Lithography 3**	Negative resist AZ 2070: • Wafer dehydration: oven, 120 °C, 15 min • Spincoating: thickness ∼ 4.4 µm • Pre-exposure bake: hotplate, 110 °C, 1 min • Exposure: alignment to NCG pattern • Post-exposure bake: 110 °C, 1 min • Development: AZ726, 1 min 20 s
13.	**O_2 descum etching**	Ensure resist is completely removed in opened areas while avoiding NCG removal • Gas flows and pressure: 20 sccm O_2, 20 mT • Plasma: 20 W RF power • Etch duration: 30 sec
14.	**Metal evaporation**	Target material Ti/Au, target thickness 20/200 nm
15.	**Lift-off process**	NMP
16.	**Contact annealing**	Improve contact between Ti/Au and NCG, 300 °C, 1 h
17.	**RIE SiO_2 etch [B]**	Remove thermal SiO_2 (245 nm) to allow electrical contacting of substrate • Gas flows and pressure: 38 sccm Ar, 12 sccm CHF_3, 30 mT • Plasma: 200 W RF power • Etch duration: 20 min

4.7.2 Fabrication details

The steps crucial for successful nanowire formation are the reactive ion etching of the oxide to form the surface steps (Step 3) and the NCG etching (Step 9). These two steps are explained in more details below. Additionally, some results of the metalization are provided.

4.7.2.1 Step formation in thermal oxide (Step 3)

The wet thermal oxide on the wafer surface has a thickness of 245 nm, as explained in Section 4.2 on page 69. To measure the etch depth ellipsometry was used. The trenches of the devices (width less than 6 µm) are too small for ellipsometry. However, by reducing the ellipsometry spot diameter through the use of focusing probes and measuring on the 300 µm wide frames around the samples, reliable top oxide thickness measurement is achieved. First wafer `MSx20` was etched for 2 min, with a resulting oxide thickness of 201 and 198 nm in the center and at the edge of the wafer, respectively. The etch rate in the center was thus 22 nm/min. After an additional etch of 3 min, the measured thicknesses

of 138 and 126 nm, respectively, indicated an etch rate of 21.4 nm/min. The remaining three wafers were then etched for 5 min each in one step. An oxide thickness of 140 and 124 nm for the center and at the edge, respectively, measured on wafer `MSx22` after the etch shows good reproducibility. The etch rate difference between center and edge was observed before with other samples and is due to plasma differences at the edges.

4.7.2.2 NCG dry etching (Step 9)

This step forms the nanowires, as schematically illustrated in Figure 2.30, and has to be as anisotropic as possible. High RF power and low pressure generally increases the directed etching for plasma processes. Without any previous results, wafer `MSx20` was etched for 30 sec with the given etch conditions. After this initial etch, NCG was still visible with the naked eye, and ellipsometry showed that 4.0 nm of NCG was present at the center of the wafer. The NCG thickness in the edge regions was higher (between 4.8 and 6.2 nm). The etch rate could thus be estimated to 1.04–1.12 nm/sec. Wafer `MSx20` was then etched a second time for 10 sec, which corresponds to an overetch of 7.2 and 4.2 nm in the center and at the edge, respectively. After the etching, NCG was still visible with the naked eye top-right, and weaker bottom-left from the center (wafer flat at bottom). This is due to the non-uniformity of the initial PECVD process (see thickness uniformity investigation in Section 3.3.1 on page 51). The remaining NCG areas are visible in Figure 4.23a, which is a photography of the full wafer after successful fabrication. The three remaining wafers were then etched for the duration t_{etch} as outlined in Table 9.

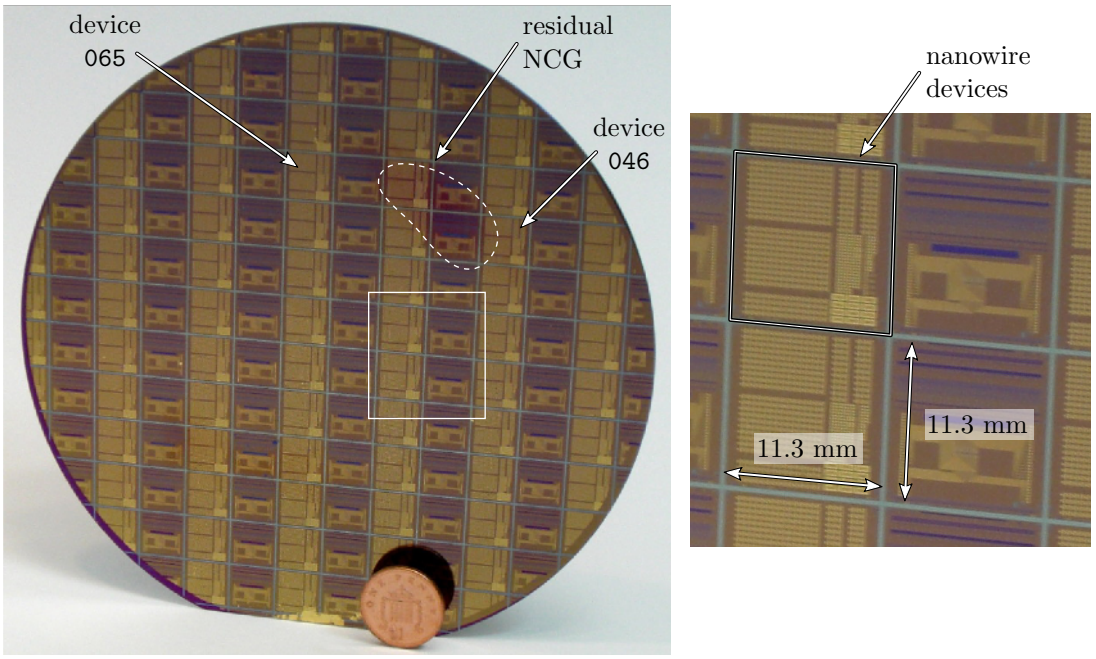
4.7.2.3 Metalization (Step 12–15)

An optical microscope image of the nanowire structures after successful lithography is shown in Figure 4.24a. The two orange/brown shaded areas are the NCG pads, and the brighter vertical structure is the etched trench. The nanowire location (left and right edge of the trench) is indicated.

A different structure after Ti/Au lift-off is shown in Figure 4.24b. The large contact area between the NCG and the Ti/Au ensures low resistivity. The contact reaching in from the left is not used in these structures.

4.7.3 Fabrication results

The fabrication of all four wafers was successfully concluded. Wafer `MSx20` is shown in Figure 4.23a. As mentioned earlier, the NCG has not been removed completely in all areas, resulting in residual NCG as indicated. In the transitional region between NCG and no NCG the etch progress can be observed. A closeup of two chips, each comprising many sets of nanowire devices, is shown in Figure 4.23b. Every second device type on the wafer (left and right of the nanowire devices) has not been used in this work.



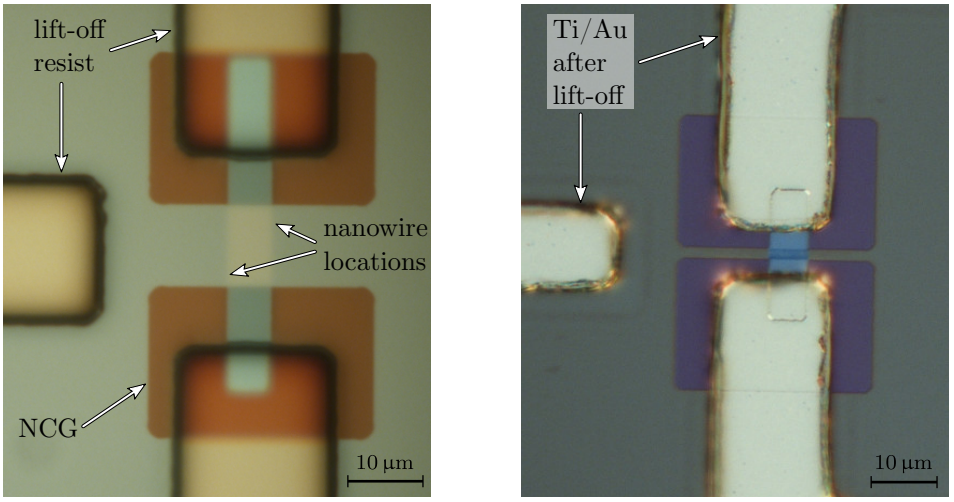
(a) (b)

Figure 4.23: (a) Picture of 150 mm wafer `MSx20` with fabricated nanowire devices. NCG residues in upper right part are indicated. Residues lower left are visible very faintly. British penny shown for size comparison. (b) Close up view of area marked by white rectangle in (a). Nanowire devices are located in the areas indicated.

The wafer design comprises nanowire devices in various variations. The fabricated devices shown in Figure 4.25a, for example, have four trenches and thus eight nanowires in parallel. Other devices comprise two very long nanowires (Figure 4.25b) or are solid NCG thin film (Figure 4.25c). The latter structures are also called thin film transistors (TFT) and will be used to compare the NCG properties between the different wafers.

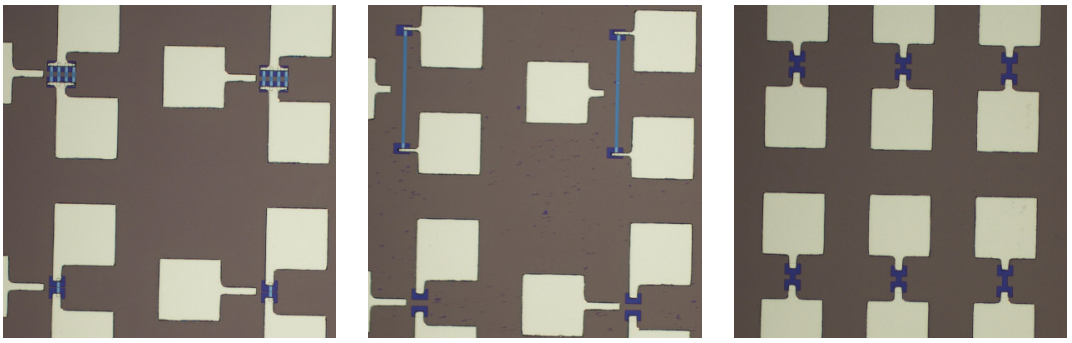
SEM micrographs of one fabricated device on wafer `MSx20` are shown in Figure 4.26, and the device is rotated by 90° in comparison to the device shown in Figure 4.24b. The SEM images are taken at a tilt angle of 40°, thus distorting vertical dimensions. The very high magnification micrograph (×100k) of the transition between the NCG and the oxide is shown as inset on the lower right. The SiO_2 step has a rough edge (roughness in the range of 50 nm) which is due to the lithography resolution and can not be avoided. The NCG has a slightly rough surface, as described in Section 3.3.3 on page 57. Even though electrical measurements, which will be discussed in detail later, show conduction of that particular device, no nanowire can be confirmed in the indicated locations.

Several more devices were examined by SEM in detail. The SEM micrograph in Figure 4.27a shows one of the nanowire locations of device `MSx20_046_1_J22`, with the unetched NCG on the left and right. Unfortunately, it appears that the NCG has not been etched sufficiently in Step 9, and partially etched NCG forms conducting paths. This partially etched NCG is interrupted by darker areas which are identified as the



(a) (b)

Figure 4.24: (a) Nanowire device after ligt-off resist patterning but before metal evaporation. (b) Different nanowire device after Ti/Au evaporation and lift-off by NMP.



(a) (b) (c)

Figure 4.25: Nanowire device variations. (a) Devices with eight (top) and two (bottom) nanowires in parallel. (b) Long nanowire devices. (c) Solid film devices.

SiO_2 that is below the NCG. Device `MSx20_046_1_J42`, which is shown in Figure 4.27b, is a structure without nanowire. Nevertheless, no distinct edge between the NCG and the inner area is visible. Thus, it must be assumed that also for this structure the NCG etch was not sufficient.

4.7.4 Electrical characterization

Only wafer `MSx20` was electrically characterized. The electrical characterization was done using a probe station and an *Agilent B1500A Semiconductor Device Analyzer*. Both nanowire and TFT structures were measured, and representative results are provided below for completeness.

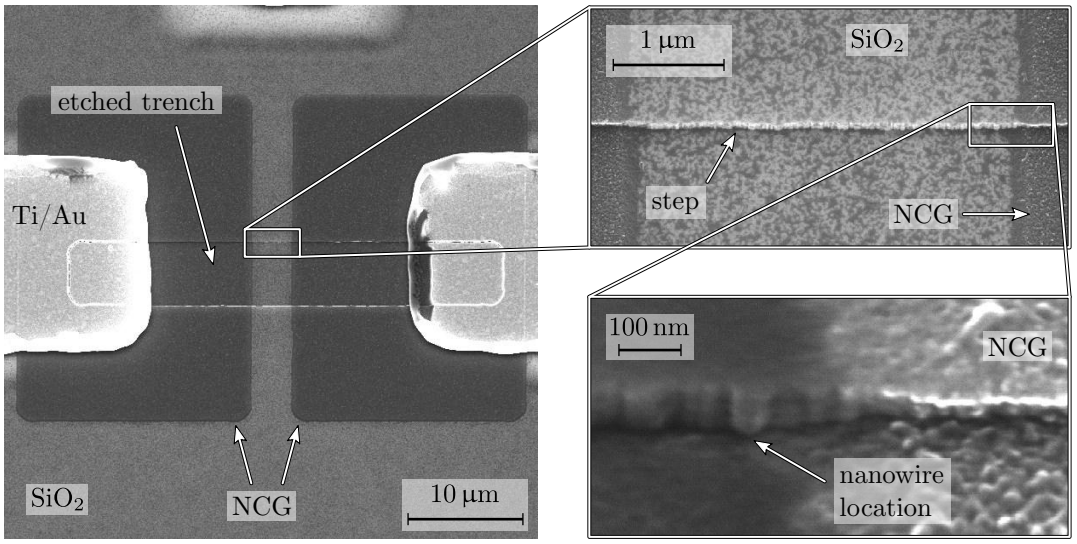
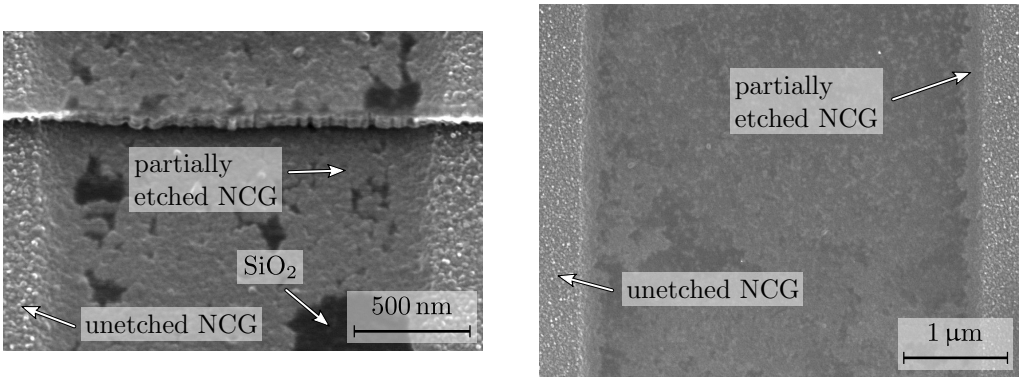


Figure 4.26: SEM micrographs of fabricated nanowire device `MSx20_046_1_J11`. The two NCG pads, Ti/Au contacts and the etched trench are visible. The inset upper right shows a closeup of one of the trench edges where the nanowire is expected. The right part is further magnified (inset lower right) showing the transition from NCG to SiO_2. The nanowire location is indicated. The device shows conduction, however the NCG at the step can not be identified from the SEM image.



(a) `W20_046_1_J22` (b) `W20_046_1_J42`

Figure 4.27: SEM micrographs of fabricated devices. (a) Nanowire device `MSx20_046_1_J22`, showing partially etched NCG present between electrodes. (b) Device `MSx20_046_1_J42` without nanowire. Partially etched NCG connects both electrodes.

4.7.4.1 Nanowire devices

Results The measurements were taken on sample `46`, which is close to the area with residual NCG (see Figure 4.23a). The electrical characterization results of device `MSx20_046_1_J22` are shown in Figure 4.28. Linear least square fitting to the results for small currents gives a resistance of $3.66 \pm 0.06\,\mathrm{M\Omega}$.

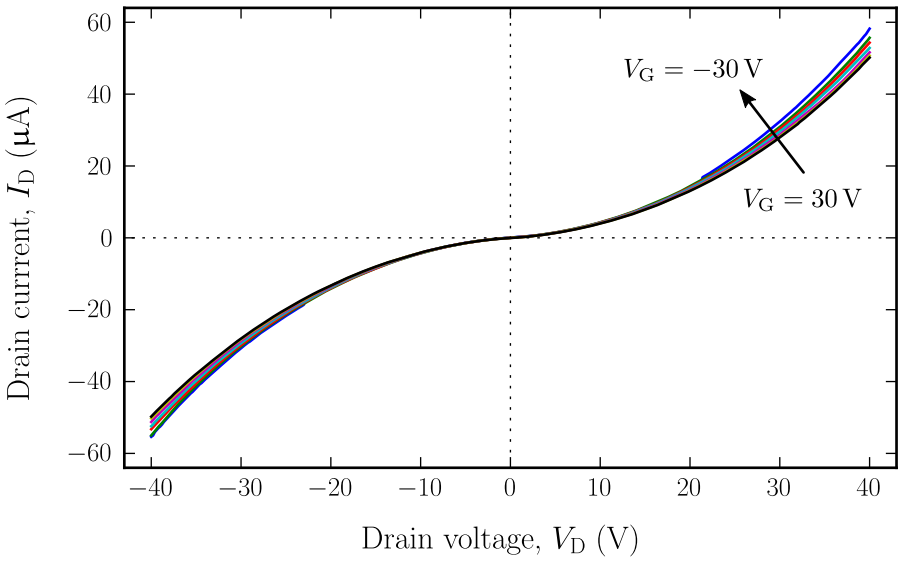


Figure 4.28: I_D–V_D results of nanowire device `MSx20_046_1_J22`. The back gate voltage V_G is varied from −30 V to 30 V in steps of 10 V.

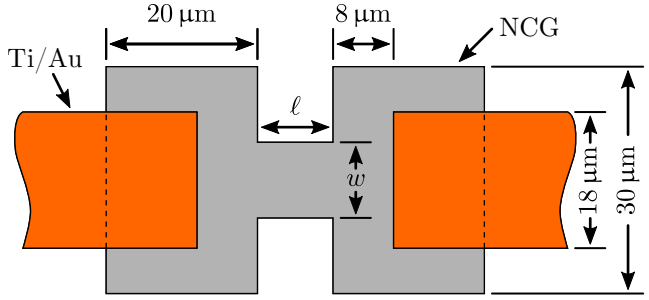
Discussion The devices `J22` exhibits significant back gate modulation. As mentioned earlier, NCG nanowire formation could not be confirmed using SEM on device `J11`. For device `J22` the case is even clearer. As visible in Figure 4.27a, there is partially etched NCG connecting both electrodes. Thus, it must be assumed that the conduction of this device is due to the remaining NCG. This assumption was further confirmed on device `MSx20_046_1_J42`. This device, shown in Figure 4.27b, does not comprise the trench necessary for nanowire formation. Consequently, this device should, if correctly fabricated, only exhibit a very small leakage current. However, a resistance of $\sim 1\,G\Omega$ was measured with a distinct back gate modulation effect.

4.7.4.2 Thin film transistor (TFT) devices

The mask design used for the fabrication comprises devices that result in solid NCG films of different dimension. Such devices are shown in Figure 4.25c.

Results In total 15 TFT devices with five different dimensions were measured on device chip `065` (see Figure 4.23a for device location). The TFT devices have dimensions as shown in Figure 4.29. The drain current was limited to 30 µA for the I_D–V_D measurements (V_D varied from −10 V to 10 V in steps of 50 mV) with variable back gate voltage V_{BG} (V_{BG} varied from −30 V to 30 V in steps of 10 V). All devices exhibited metallic behavior as expected, and linear least square fitting was used to obtain the channel resistances as a function of back gate.

The fitting results for devices `P31` to `P33` with inner dimensions of $20 \times 10\,\mu m^2$ are shown in Figure 4.30. Trend lines and their inclination m are also shown. The channel resistances of the remaining twelve measured devices for $V_{BG} = 0\,V$ are:



Device	ℓ	w
P11...P13	10	10
P21...P23	5	10
P31...P33	20	10
Q31...Q33	4	4
R31...R33	2	2

Figure 4.29: Schematic illustration of TFT devices. Device names are grid location of device. Inner length ℓ and width w according to table on the right (in µm).

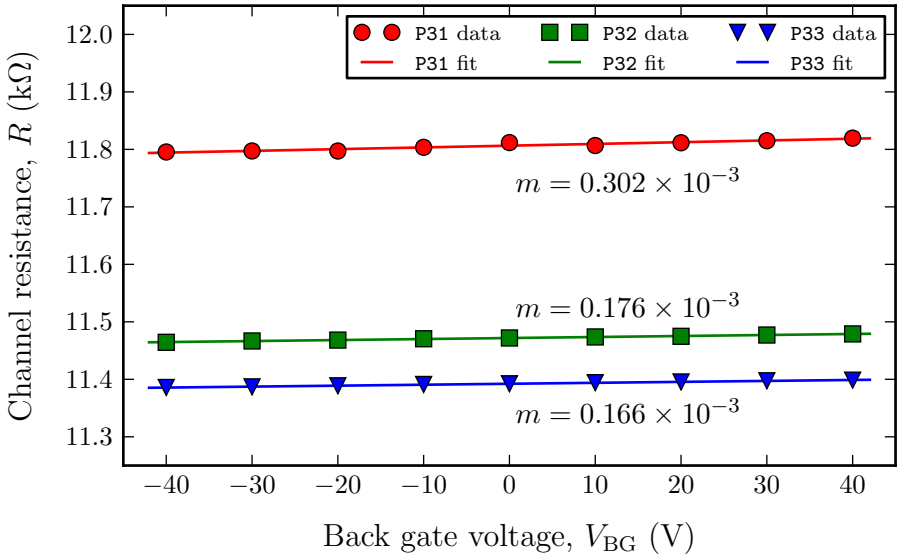


Figure 4.30: Fit results of TFT resistance for samples MSx10_065_6_P31, P32 and P33. Inclination of linear fit to results provided. Unit of m is kΩ/V.

- P11 to P13: 8.37, 8.05 and 10.49 kΩ.
- P21 to P23: 7.25, 14.13 and 11.75 kΩ.
- Q31 to Q33: 11.27, 9.27 and 10.47 kΩ.
- R31 to R33: 10.76, 11.31 and 12.79 kΩ.

Discussion The channel resistances obtained through fitting to I_D–V_D do not show any correlation with the inner dimensions ℓ and w. It is therefore difficult to estimate the sheet and contact resistance. Nevertheless, a positive back gate modulation effect is observed for all 15 measurements. It had been found from the measurements of the top gated structures (see Section 4.6.3) that a reduction of the NCG thickness increases the modulation effect. The NCG films on this measured wafer MSx20 is 37.5 ± 0.5 nm. The

top gated structures also exhibited very small modulation effects for NCG with similar thickness.

This would also help understand the measurement results of the nanowire device `MSx20_046_1_J22` (see Figures 4.28, respectively). From SEM images it was concluded that the NCG between the two electrodes had not been removed, but instead thinned. Consequently, these devices can also be treated as TFT devices. The channel resistance is more distinctively modulated by the back gate than the dedicated TFT devices, which is in line with the observation that thinner NCG films are more suitable for TFT applications.

4.7.5 Conclusion

In this Section, the wafer-scale fabrication of NCG nanowire devices was reported. Four 150 mm wafers were successfully processed. Electrical characterization and SEM investigation of devices in different areas of the wafer revealed, however, that the nanowire fabrication was not successful. In some areas the NCG film had been removed completely, while in other areas (presumably with thicker NCG due to deposition non-uniformities) partially etched films remained creating unwanted conduction paths. The electrical results of these devices have thus to be attributed to thin film conduction. A better process for the formation of the nanowires would be to use argon ion etching, therefore removing any chemical etch component. Furthermore, NCG thickness should be increased to guarantee reliable nanowire formation.

Thin film transistor devices on the same wafer showed weak back gate modulation. This is attributed to the relatively thick NCG films. Reduction of NCG thickness is not recommended, as this would impair successful nanowire fabrication. Instead, TFT device fabrication should be investigated separately since their requirements for NCG thickness contradict each other, i.e. thick NCG is required for nanowire fabrication and thin NCG is required for TFT devices.

4.8 Summary

The development of four different fabrication processes, based on the NCG films developed in this work, and the characterization of device obtained, were reported. In the first part of the Chapter, common sample preparation was described. The NCG film deposition and characterization (thickness, uniformity, surface roughness, Raman) of the eight 150 mm wafers had been described in Chapter 3. From each of these eight wafers, samples were used to fabricate different structures.

Fabrication of NCG membrane devices with dimensions between 1 and 100 µm was explained in the second Section. Based on deep reactive ion and HF vapor etching, a fabrication process was proposed. At the time of preparing this thesis, the fabrication had not been finished, thus no measurement results are reported. However, it became apparent that the usage of single side polished wafers significantly impaired the back side lithography.

The third part of this Chapter covers the fabrication of suspended NCG beam structures. NCG strips are patterned and contacted, and the underlying thermal oxide (thickness 245 nm) is removed by HF vapor etching to suspend the strips. Three major issues were encountered during the fabrication. First, due to the lack of dedicated alignment structures, NCG samples with thickness of less than 10 nm could not be processed. Secondly, the NCG strips were not suspended after the HF vapor etching, and some unexplained etch results were obtained. Lastly, NCG films developed wrinkles after the HF release. In the author's opinion it should be possible to solve the first and second issues by including a dedicated alignment mark patterning step and significantly increasing the sacrificial oxide layer thickness. A modified mask design is also suggested. The third issue of wrinkle formation in the NCG films shows that the films are compressive (supported by Raman investigation). A strong dependence on the deposition conditions is expected. By repeating the fabrication with the above mentioned improvements it should be possible to gain further insight into the mechanical stress of as-deposited NCG films. The electrical characterization of several devices showed Schottky-like behavior. The gold structures were found to be in direct contact with the underlying silicon substrate due to the insufficient sacrificial oxide thickness, consequently giving rise to the observed characteristics. An increase of oxide thickness, as mentioned earlier, would avoid this unwanted contact.

In the fourth part of this Chapter, the fabrication of top gated structures is reported. Contacted NCG strips are first covered by a PECVD oxide. Then, top gate electrodes are patterned. Besides the lack of dedicated alignment structures that made the processing of samples with NCG thicknesses of less than 10 nm thickness impossible, peeling and wrinkle formation of the top gate oxide were observed. Although not impairing successful device fabrication, further work should be carried out to improve this fabrication step. Electrical characterization was used to investigate the difference between the top and bottom gate modulation effect on the channel resistance. As expected, the top gate had a stronger modulation effect due to the reduced gate oxide. Furthermore, it has been shown that the modulation is positively influenced by reducing the NCG thickness. It would be thus beneficiary to device performance to reduce both, NCG and top gate oxide thickness.

The last part of this chapter covers the wafer-scale fabrication of NCG nanowire devices. By depositing NCG over predefined surface steps, the increased vertical thickness is exploited during the consecutive reactive ion etch to yield nanowires with a size far below the resolution limit of optical lithography. Four 150 nm wafers with different NCG thicknesses were successfully fabricated. Consecutive SEM and electrical characterization, however, showed that the nanowire formation was not successful. It became apparent that the reactive ion etching using oxygen is not suitable for the formation. It is thus concluded that thicker NCG thicknesses should be used and the anisotropic etching step should be performed using an ion miller instead. Electrical measurements of TFT devices show very weak back gate modulation, which is believed to be due to the relative large NCG film thicknesses.

Chapter 5

Low-damage, high-precision FIB/SEM prototyping technique

Focused ion beam (FIB) lithography has been identified as a rapid prototyping tool that can be used for the fabrication of electronic devices based on exfoliated graphene. The main reasons are, as mentioned in Section 2.7 on page 32, the high milling resolution, flexibility to accurately deposit insulator or conductor material in defined shapes and thicknesses, and the simultaneous observation using non-destructive SEM imaging. Here, the development of a low-damage, high-accuracy ($< 250\,\mathrm{nm}$) prototyping technique is demonstrated to overcome current issues arising when using FIB for graphene device prototyping.

First, a fabrication workflow for the FIB/SEM prototyping technique of graphene devices is proposed. The individual steps are described in detail, followed by the different contact pad metalization strategies. Furthermore, some process alternatives are explained. In Section 5.2, the application of the prototyping technique is demonstrated by fabricating three thin film transistor structures (similar to the ones reviewed in Section 2.6 on page 28 and shown in Figure 2.25). One based on FIB-assisted deposition, and two based on e-beam-assisted deposition. The electrical characterization of the obtained devices is discussed. Finally, a method for the fabrication of transistors with very short channels is proposed.

5.1 FIB/SEM prototyping technique

In this Section, the proposed FIB/SEM prototyping technique applicable to graphene is described. The main targets of this technique are manifold. One is to avoid FIB exposure of graphene as much as possible at any stage of the process. Also, the technique is intended to be of generic nature, therefore it is not limited to a specific material or structure. It allows material deposition by FIB and e-beam, as well as FIB trench milling.

The principal process flow is illustrated in Figure 5.1. First, alignment marks are milled which are necessary to achieve the high accuracy without direct FIB imaging.

Then, the pattern file is prepared and subsequently one or more deposition and milling steps are carried out. This can involve e-beam-assisted deposition, FIB-assisted deposition or FIB milling. Optionally, probe pads are metalized at the end of the fabrication, allowing contacting by probes or wire bonds. Each step is explained in detail below.

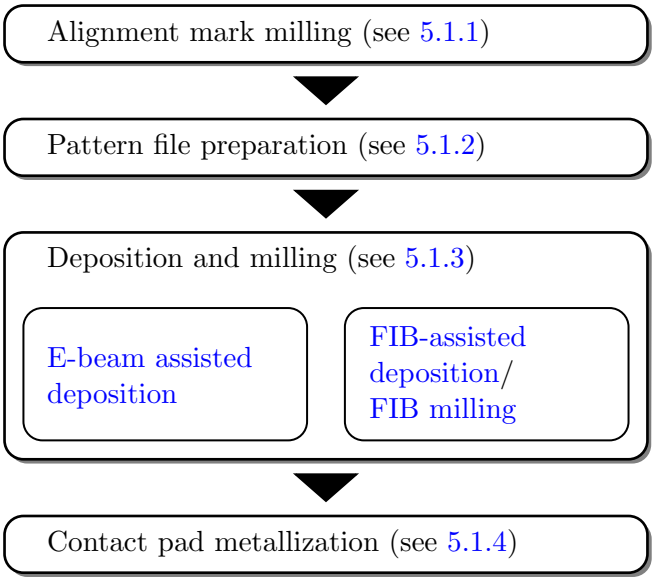


Figure 5.1: Flow chart illustrating the different steps of the FIB/SEM prototyping technique: Alignment mark milling, pattern file preparation, deposition/milling and probe pad metallization.

5.1.1 Alignment mark writing

As explained in Section 2.7.1 on page 33, the integrated SEM/FIB system does not allow a sufficiently stable alignment of the two beams in the coincidental point. Therefore, three or more alignment marks are first milled close to the graphene flake. To ensure accurate scaling, a write field[1] calibration using a commercial calibration sample with a $1 \times 1\,\mu m^2$ sized chess-like pattern is performed (Figure 5.2a). The sample is then positioned in the coincidental point, and the graphene flake is located using the SEM, followed by a translation of the sample. By doing so, the FIB write field is sufficiently far away from the graphene to avoid any unnecessary FIB exposure. In this location, dummy alignment marks are patterned by FIB based on a pattern file (shown in Figure 5.2b). Without moving the sample, the location of the alignment marks in the SEM view is recorded. Now, under SEM observation, the sample is moved until the graphene flake is in the center of the recorded alignment marks, and the FIB milling is repeated (Figure 5.2c). The sample is tilted perpendicular to the SEM after the alignment mark

[1] A write field is a predefined area in which pattern can be fabricated. It is linked to a fixed magnification value, available write field sizes are 100×100, 50×50, 20×20 and $10 \times 10\,\mu m^2$.

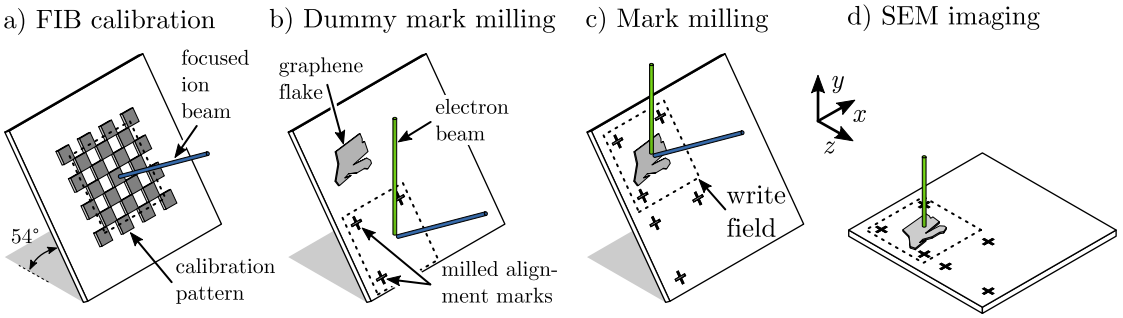


Figure 5.2: (a) The FIB or e-beam write field is calibrated using a commercial calibration sample. (b) Dummy marks are milled away from the graphene, and their positions are recorded in the SEM view. Next, the sample is repositioned, and alignment marks are accurately positioned and milled around the graphene (c). (d) Distortion free SEM micrograph acquired showing graphene and alignment marks.

milling, as shown in Figure 5.2d, and a distortion-free image is acquired by SEM showing the position of the graphene flake and the alignment marks, respectively.

5.1.2 Pattern file preparation

The next step is to generate a pattern file based on the previously acquired image. It has shown helpful to insert the image as background into a CAD software. This image is then scaled, rotated and translated until the marker visible in the image coincides with the alignment marks in the pattern file. Then, rectangles and lines are positioned for the deposition and milling steps, respectively. Note that since the drawn elements have to be perpendicular to the pattern file coordinate system to avoid stitching during fabrication, the alignment mark position in the pattern file might have to be changed (relative position of the alignment marks in respect to each other must remain unchanged). An alternative approach to generate the pattern file is to conduct geometric measurement of the alignment mark position in relation to the graphene flake. The patterns can then be constructed and generated.

5.1.3 Deposition and milling

The deposition and milling part of the proposed fabrication technique includes in fact three procedures, as illustrated in Figure 5.1. These are e-beam-assisted deposition of tungsten or insulator, FIB-assisted deposition of tungsten or insulator, and FIB milling. Each of these procedures can be carried out as often as necessary in random order. However, it is important to always avoid FIB imaging of the device and realign the write field between each step.

E-beam-assisted deposition (tungsten/insulator) The e-beam-assisted deposition is controlled by the *ELPHY Quantum* lithography attachment in this step. First, a mark alignment procedure is executed in the control software, which scans small areas

in predefined locations (the sample has to be positioned in such a way that the marks on the sample are within these typically $6 \times 6\,\mu m^2$ large scan areas) and requires user interaction to identify the exact location of the marks within these acquired raster images. This is shown in Figure 5.3a-1. Based on these correction values, the lithography attachment maps (rotation, scaling, translation) the SEM write field to the physical alignment marks. The inserted GIS nozzle (compare also Figure 2.31a) is then used to introduce precursor gases close to the sample, while the e-beam is used to dissociate these, resulting in deposition. In Figure 5.3a-2 the deposition of insulator passivation on top of previously deposited tungsten contacts is illustrated. Note that the only requirement for accurate positioning is the presence of alignment marks. Accuracy is not influenced by previous e-beam or FIB processes.

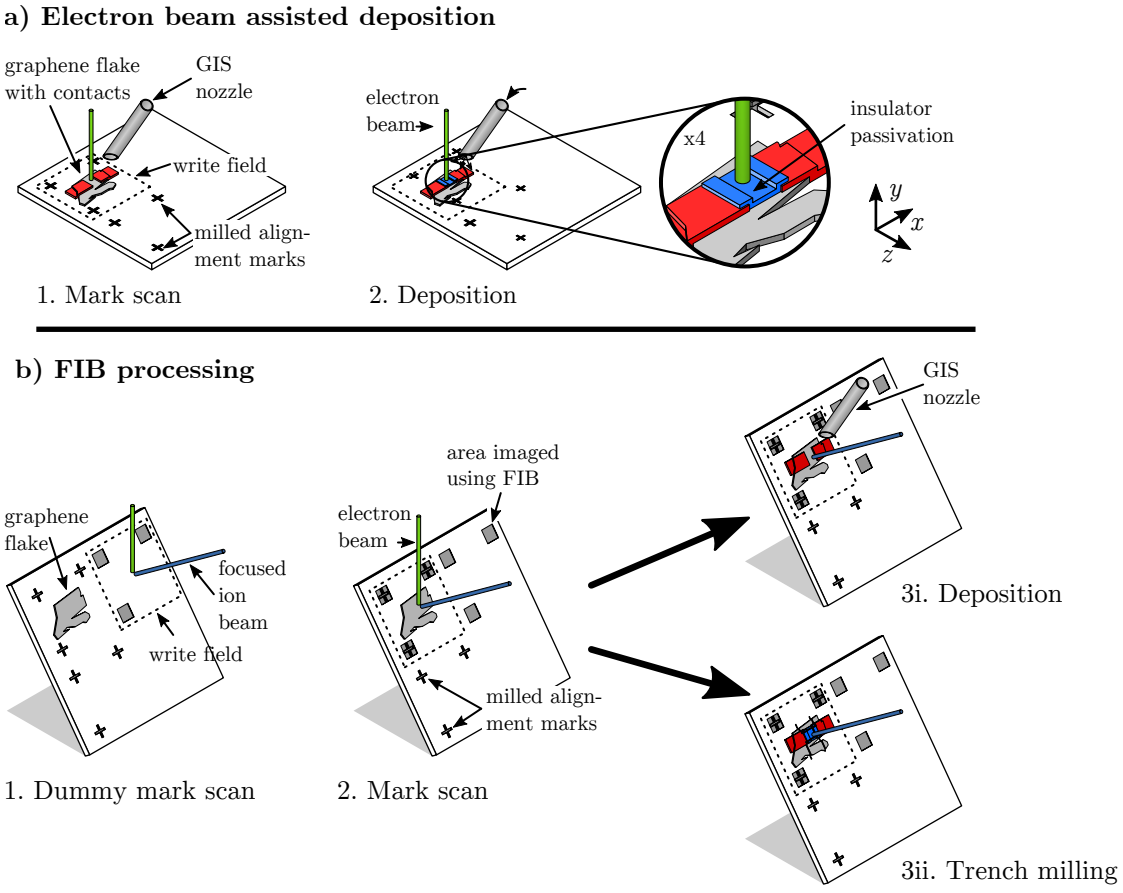


Figure 5.3: Schematic illustration of e-beam and FIB processing. (a) Electron beam assisted deposition: After mapping the write field to the alignment marks on the sample (1), e-beam-assisted deposition is executed (2). The callout shows insulator deposition in the channel region on top of previously deposited tungsten. (b) FIB processing: (1) A dummy mark scan away from the graphene flake is performed. The scan area is recorded in the SEM view followed by (2) the accurate sample re-positioning in the SEM view, and the execution of the mark scan procedure. FIB-assisted deposition (3i) or FIB trench milling (3ii) is then carried out.

FIB-assisted deposition (tungsten) For accurate FIB-assisted deposition, the FIB write field is mapped to the alignment marks. This is very similar to what is done for the e-beam mapping, however, an additional step has to be taken to avoid potential FIB exposure of the graphene. As illustrated in Figure 5.3b-1, after tilting the sample and positioning it in the coincidental point, the write field is positioned away from the graphene device. In this location a dummy mark scan is executed. As a result, the areas which are exposed by the FIB beam become visible in the SEM view and can be recorded. Now, the sample is moved so that the alignment marks, initially patterned on the sample, fall within the projected FIB scan area. As shown in Figure 5.3b-2, the mark scan procedure is then executed, resulting in the mapping of the FIB write field to the marks. Deposition is carried out through precursor gas introduction and simultaneous FIB exposure, as shown in Figure 5.3b-3i.

FIB trench milling Milled trenches are a crucial element in the device fabrication. They ensure current insulation to the channel region and define the channel width. As with FIB deposition, the write field is first mapped to the alignment marks on the sample (see Figure 5.3b-1 and 2). Then, trenches are milled according to the pattern file (see Figure 5.3b-3ii).

5.1.4 Contact pad metalization (FIB or lift-off)

In order to contact the device by probes or wire bonds, sufficiently large and thick contact pads are necessary. This can be achieved by FIB or e-beam-assisted deposition as explained above, however, deposition rates are relatively low, thus consuming large amounts of precursor gases. Also the used write field is too small to incorporate two pads with a size of at least $50 \times 25\,\mu m^2$. Depositing probe pads with the *ELPHY Quantum* lithography attachment is therefore more complicated than just adding two polygons to the pattern file. Instead, two methods are proposed: (i) Lift-off deposition of metal and (ii) FIB-assisted deposition of tungsten, with the former being the preferred method. Using lift-off deposition involves photoresist, which is a known contaminant. However, this prototyping technique allows the channel region of the device to be protected by an insulator layer. In addition, the alignment marks and patterned devices are sufficiently visible under optical microscopy commonly used in mask aligner, and can be readily aligned to a photolithographic mask.

The main advantage of the FIB-assisted contact pad deposition, on the other hand, is the ability to prepare a complete device within the SEM/FIB microscope without exposure to ambient conditions. Evaluation of deposition conditions based on the *ELPHY Quantum* system has shown much lower deposition rates as compared to the control software *Smart SEM*. The details of the conditions are given in the Appendix A on page 127. The disadvantage of using *SmartSEM*, however, is that it does not allow alignment to markers. To avoid exposure of the channel region to Ga^+-ions, the method found to be most convenient is the following: While imaging with a low FIB current,

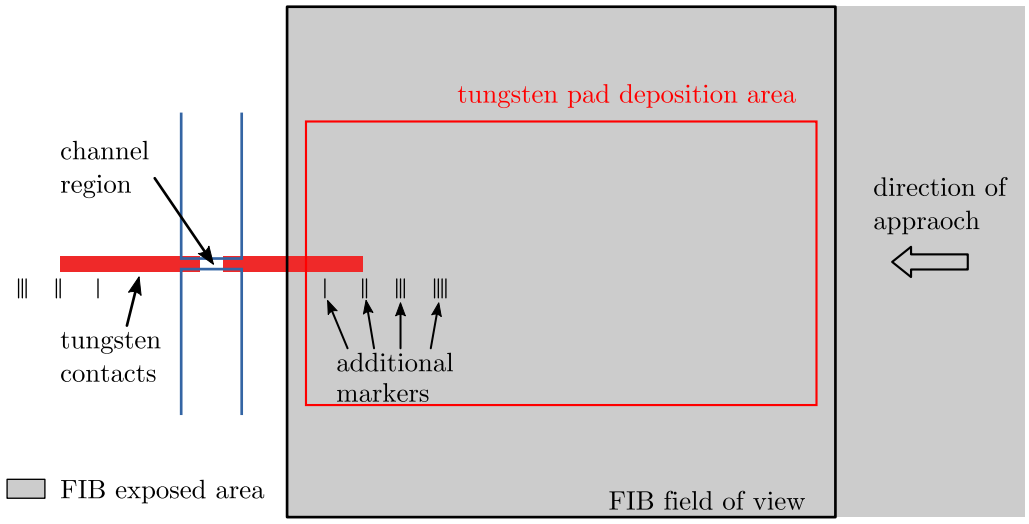


Figure 5.4: Schematic illustrating the FIB-assisted tungsten contact pad deposition procedure. Using FIB, the area right of the channel region is imaged and slowly moved left. Previously milled markers allow estimation of distance to the channel region without imaging it. Once the contact is visible, a large pad is deposited.

the device is slowly moved towards the FIB field of view until the extensions of the device are visible. Then the deposition with sufficient overlap can be achieved. This approach can be further facilitated by patterning small markers that help identify the intended position of the contact pads. Such an approach is illustrated in Figure 5.4. For illustration purposes a generic device comprising two tungsten contacts and milled trenches is shown.

5.2 Device fabrication and characterization based on the FIB/SEM prototyping technique

Before turning to fabrication results obtained by applying the proposed prototyping technique, the graphene exfoliation method used to obtain graphene samples is briefly explained. Then, fabrication and characterization of three graphene devices is presented. The first device, `264-384`[2], was fabricated using FIB beam only. The second and third device, `314-223` and `S2`, were fabricated using exclusively e-beam-assisted deposition, and comprise an insulator channel protection and FIB-milled trenches. For all three devices the lift-off probe pad metalization method was applied. This Section only provides exposure conditions used during fabrication of these particular devices. The extensive development of conditions for FIB-assisted deposition of tungsten, e-beam-assisted deposition of tungsten and insulator, and FIB trench milling is documented in Appendix A on page 127.

[2]Naming of devices is not systematic. Two numbers connected by a dash normally denote the unique number of the wafer marker closest to the device.

Toward the end of the Section, one test structure is documented which demonstrates the FIB-assisted pad deposition. The versatility of this accurate FIB technique is further demonstrated by applying it to devices of other researchers not based on graphene. These results are provided in Appendix B on page 141.

5.2.1 Graphene exfoliation

Mechanically exfoliated graphene was prepared by two different methods. In both cases numbered location markers are defined by e-beam lithography and realized by Cr/Au lift-off on the highly-doped p-Si wafer with a 300 nm thick SiO_2 surface layer. These are indispensable for catalogization of graphene and fast location under SEM. Next, the marked wafers are diced into smaller samples and used for exfoliation from HOPG purchased from *Agar Scientific*.

The first exfoliation method, henceforth called *sedimentation method*, was conducted by Zaharah Johari. Here, PMMA resist is spun onto the samples and used as a transfer medium for the HOPG. The substrate is then immersed into acetone inside a sedimentation dish, resulting in the dissolution of the PMMA layer. After the graphene settles on top of the substrate, any residual resist is removed by consecutive acetone and isopropyl alcohol (IPA) rinse.

The second exfoliation method, henceforth called *tape method*, was conducted by the author. Adhesive tape (Scotch® tape from 3M) is used to repeatedly peel HOPG, thus exfoliating graphene. The tape is then pressed onto the sample and peeled. The sample is cleaned in an ultrasonic acetone bath and rinsed in IPA to remove any adhesive residues and loosely attached graphene and graphite pieces.

The resulting graphene flakes are located using optical microscopy and cataloged together with the number of layers, as determined by micro Raman spectroscopy or by the optical contrast method.

5.2.2 Graphene device using FIB only (device `264-384`)

This device was fabricated on a graphene flake obtained through the sedimentation method. The results below have been presented as poster at the *37th International Conference on Micro and Nano Engineering* (MNE 2011) conference in Berlin [2] and have been published in the *Micro and Nano Engineering 2011 - Selected Papers* issue of the *Microelectronic Engineering (MEE) Journal* [1].

The fabrication steps are (for explanation see Figure 5.1): (i) alignment mark milling, (ii) pattern file preparation, (iii) FIB-assisted area deposition, (iv) FIB trench milling and (v) contact pad metalization by Ti/Au lift-off. The total FIB machine time including FIB write field calibration was under three hours.

The graphene sample allowed positioning of three channels on defect-free bilayer graphene (verified by Raman spectroscopy). Spacing and position of the devices were chosen as to allow alignment to an existing optical mask for probe pad metalization. The trench shape and location is individually adjusted for each channel. This is necessary

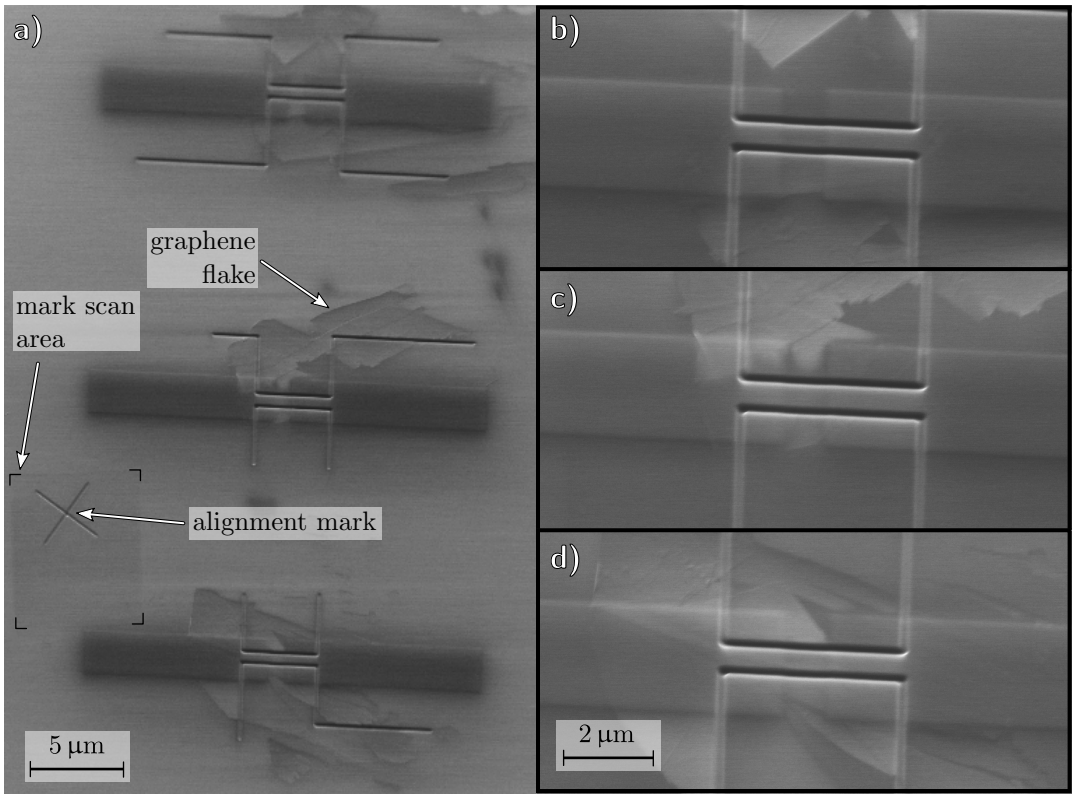


Figure 5.5: SEM micrographs showing FIB-fabricated graphene device `264-384`. Each of the three channels in (a) are shown enlarged on the right side in the same order. One alignment mark and the area scanned during write field mapping are visible. A closeup of the channel from (c) is shown in Figure 5.6.

as graphene has a random shape, and the conduction path from source to drain has to be isolated to the channel. An SEM micrograph of the full device before contact pad metalization, together with detailed views of the three channels, is shown in Figure 5.5. The conditions used for the three FIB fabrication steps are summarized in Table 5.1; the three devices were patterned simultaneously. In each FIB step more than one exposure loop was used. This is necessary to achieve sufficient milling without suffering from redeposition. Also, the deposition conditions had to be very carefully adjusted. Any change of dwell time t_{dwell} or spacing would lead to the reversal of the deposition into milling or the development of trenches along the pattern edges. The only way to adjust the deposition thickness is thus by means of adjusting the number of exposure loops. The chamber pressure during $W(CO)_6$ introduction for tungsten deposition was $1.8 \pm 0.1 \times 10^{-5}$ mbar (base pressure 1×10^{-6} mbar).

The exposure mode, as documented in Table 5.1, is also very important for the tungsten deposition and trench milling. Please refer to Figure A.2 on page 129 for detailed explanation of the acronyms. By choosing the linear exposure mode in V-direction (perpendicular to the channel direction), trenching at the edges facing the channel is avoided, while linear exposure mode in U-direction (parallel to channel) for trench milling ensures clearly defined edges.

Exposure step	t_{dwell}	**Spacing**	**Loops**	**Dose**	**Exp. mode**
Mark milling	0.2 ms	1 nm	40	0.8 µC/cm	MA
Tungsten deposition	0.4 µs	4 nm	150	1.5 nC/cm^2	LV
Trench milling	0.1 ms	1 nm	75	0.75 µC/cm	LU

Table 5.1: Milling and deposition conditions used for fabrication of device `264-384`. Legend for exposure modes: MA is meander mode with automatic direction selection, LV is line mode in V-direction, LU is line mode in U-direction. U and V are identical with the coordinates of the pattern file. See Figure A.2 on page 129 for detailed explanation.

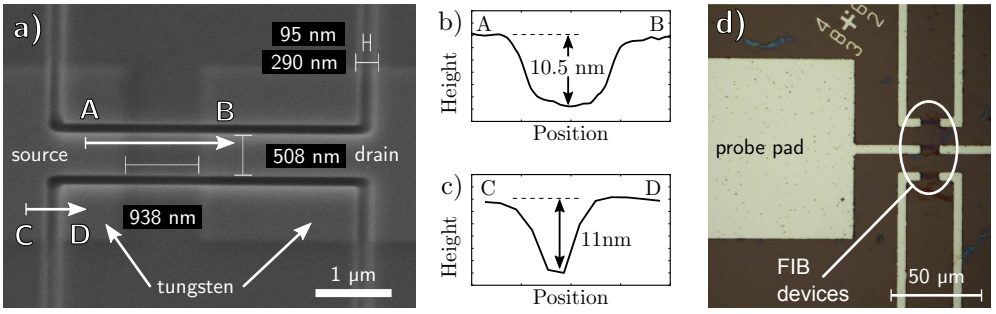


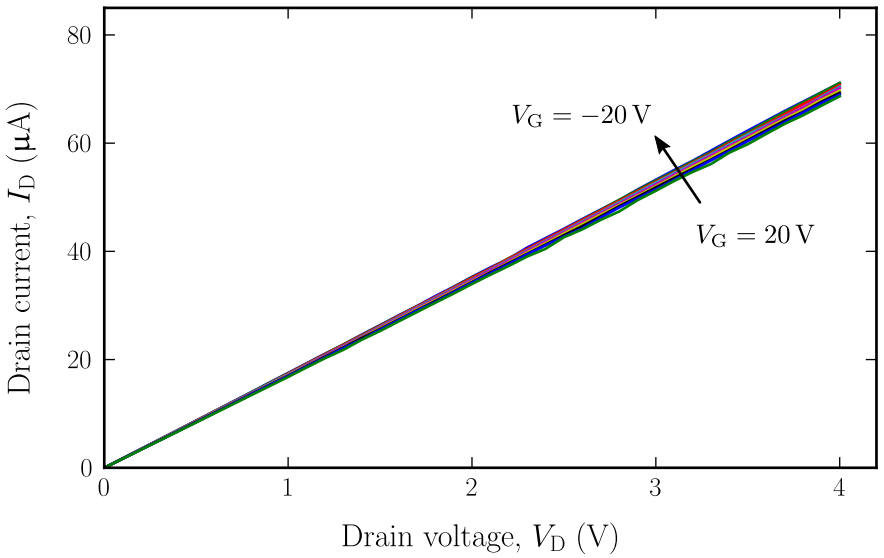
Figure 5.6: (a) High resolution SEM micrograph showing the channel region of the device depicted in Figure 5.5c. (b)+(c) Height profile extracted from AFM measurements along AB and CD. (d) Optical image of device after lift-off metalization. The leads are connected to their respective pads.

An SEM closeup of the middle channel is shown in Figure 5.6a. The AFM trace obtained along AB, as indicated in Figure 5.6a, is given in Figure 5.6b. It shows a tungsten contact thickness of 10.5 nm. Due to the geometric limitation of the probe tip, measurement of the trench depth by AFM is difficult. It is assumed to be significantly more than the 11 nm obtained from the CD profile (Figure 5.6c). The whole device after Ti/Au lift-off contacting is shown in Figure 5.6d.

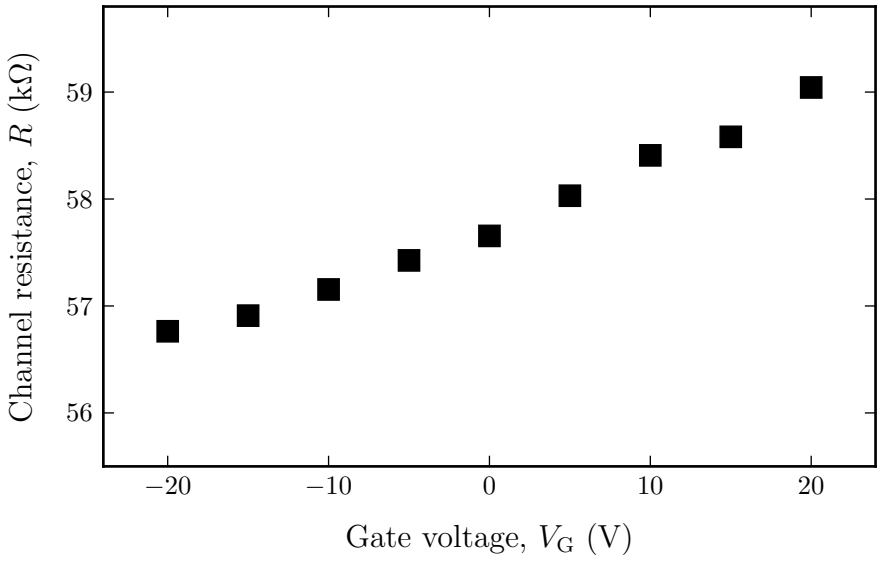
The channel length, as obtained from the SEM shown in Figure 5.6a, is 938 nm. However, the pattern file elements for the source and drain contacts had a separation of exactly 1 µm. The reason for this expected deviation between pattern file and fabricated structure dimensions is the beam diameter (∼60 nm for 10 pA beam current).

5.2.2.1 Electrical characterization

The backside of this particular sample had been metalized with a 300 nm Al layer before exfoliation. This was done to ensure good electrical contact with the measurement system's sample chuck. The sample is placed on the chuck which is connected as gate, and the source and drain are contacted by needle probes. Source/drain/gate biasing and current metering are done using an *Agilent 4155C Semiconductor Parameter Analyzer* with current and voltage measurement resolution of 10 fA and 0.2 µV, respectively. Out of the three channels fabricated, only the middle one (Figure 5.5c) exhibited any electrical conductance. The reason why the top and bottom channel did not show any



(a)



(b)

Figure 5.7: Electrical measurement of FIB-only fabricated device `264-384`. (a) The I_D–V_D characteristics shows a metallic-like response with a slight modulation by the back gate. (b) Channel resistance as a function of V_G.

conduction is not known. Contact annealing (300 °C for 30 min) in an inert atmosphere did not have any influence on the conductivity.

Figure 5.7a shows the I_D–V_D characteristics of that device. The response is metallic-like with a slight modulation by the applied back gate. The extracted channel resistance as a function of V_G is shown in Figure 5.7b. At $V_G = 0$ V, a reasonable channel resistance of $\sim 58\,\text{k}\Omega$ is achieved. This indicates ohmic contact between graphene and tungsten, and similar values have been observed before [124]. Next,the contribution of the tungsten contacts to the overall device resistance is calculated. To do this, a test sample was

prepared and used to measure the sheet resistance $R_\square = 89\,\Omega/\square$ for 10 nm thin FIB-deposited tungsten (the exact results and calculations are available in Appendix A.2 on page 131). From optical microscope pictures, the metal contact distance is estimated to be $10 \pm 1\,\mu m$. Further dimensions estimated from SEM micrographs are:

- 938 nm channel length
- 4 µm length of the milled trenches along the channel
- 508 nm tungsten width in the channel region
- 1.86 µm tungsten width away from the channel

The resistance of the tungsten is thus

$$R = R_\square \frac{\ell}{w} = R_\square \left(\frac{10 \pm 1 - 4}{1.86} + \frac{4 - 0.938}{0.508} \right) = 823 \pm 48\,\Omega$$

with ℓ the length and w the width of a rectangular conductor. This resistance is much smaller than the overall resistance of $\sim 58\,k\Omega$.

One also has to consider the possibility of device conduction due to tungsten deposited in the channel region by indirect/stray exposure. To rule this possibility out, a reference device with a 1 µm channel gap was fabricated on bare SiO_2 without graphene. This device did not show any detectable conduction. Thus, it can be concluded that the channel conductivity measured (Figure 5.7a) is due to the graphene.

5.2.3 Graphene device using e-beam-assisted deposition and FIB trench milling (device `314-223`)

The FIB-only fabricated device `264-384` had a low yield (one out of three channels showing conduction) and it lacked ambipolar characteristics (see Figure 5.7a). Therefore, in order to eliminate the possibility of Ga^+ doping or damage, a device was fabricated based on e-beam-assisted deposition which comprises an insulator channel protection. The motivation behind this is to have the electrodes and protective insulator deposited, before any FIB exposure is performed.

The fabrication procedure is a bit more complicated than for the previous device and will be explained in more detail (for explanation of the individual steps see Figure 5.1). The pattern file was prepared after the alignment mark milling. The final pattern file is shown in Figure 5.8 as overlay over the SEM micrograph, taken after the alignment mark milling[3]. Then, three consecutive e-beam-assisted depositions are carried out (5 kV acceleration voltage, 30 µm aperture size, 180 pA beam current). First e-beam-assisted tungsten deposition (, chamber pressure $1.8 \pm 0.1 \times 10^{-5}$ mbar, base pressure 1×10^{-6} mbar) of the inner contacts defining the channel length of 2 µm, followed by the

[3]Note that the coordinate system U/V of the prepared pattern is rotated by 26° in respect to the coordinate system U'/V', which was used to mill the alignment marks. This rotation was necessary due to the graphene flake shape.

Exposure step	t_{dwell}	Spacing	Loops	Dose	Exp. mode
Tungsten dep. 1 (E)	0.16 ms	4 nm	2	0.36 C/cm^2	LV
Insulator dep. (E)	0.16 ms	4 nm	1	0.18 C/cm^2	LV
Tungsten dep. 2 (E)	0.1 ms	2 nm	2	0.9 C/cm^2	LV
Trench milling (F)	0.2 ms	1 nm	60	1.2 µC/cm	LU

Table 5.2: Conditions used for device `314-223`. (E) indicates E-beam, (F) indicates FIB. Legend for exposure modes: LV is linear mode in V-direction, LU is linear mode in U direction. See Figure A.2 on page 129 for detailed explanation.

second e-beam-assisted deposition ( ). This second deposition forms an insulator channel protection overlapping the inner contacts (chamber pressure $2.25 \pm 0.1 \times 10^{-5}$ mbar, 1,3,5,7-Tetramethylcyclotetrasiloxane ($C_4H_{16}Si_4O_4$)). At this point, all critical depositions are finished and further processing is largely insensitive to drift. This even applies to the outstanding FIB trench milling step defining the channel width. Next, larger tungsten contacts are deposited by e-beam ( ), overlapping the inner contacts. These are necessary to allow optical alignment of the probe pads. Finally, FIB milling ( ) is used to define trenches which control the channel width of ~800 nm and cut off any alternative conduction paths between the two electrodes. The exact conditions for each of the three deposition steps and the FIB milling, respectively, are summarized in Table 5.2.

A SEM closeup of the device channel region is shown in Figure 5.9a. By comparing with Figure 5.8, the highly accurate positioning can be observed. The edges of the larger tungsten pads on the left side appear to be not perfectly defined. This could be due to drift during the relative long deposition step (40 min per exposure loop). However, since the inner electrodes had been defined before, no influence on the device operation

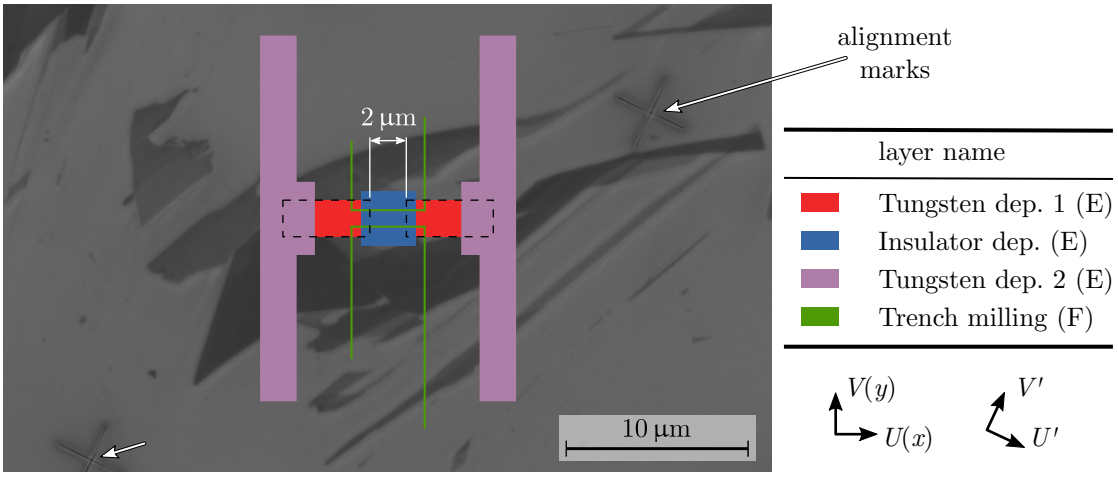


Figure 5.8: Mask design of graphene device `314-223` fabricated by e-beam-assisted deposition of tungsten (red and purple area) and insulator (blue), and FIB trench milling (green). U/V is rotated by 26° in respect to U'/V', which was used to mill the alignment marks.

is expected. The protective insulator layer covering the channel region ($3 \times 3\,\mu m$, $0.5\,\mu m$ overlap over electrodes) is visible only very faintly, and two corners are indicated by black lines. The device after lift-off metalization (50 nm Ti and 300 nm Au) is shown in Figure 5.9b.

AFM results are shown in Figure 5.10a. The structure is rotated by 45° counter clockwise compared to Figure 5.9a. From the extracted height profiles AB and CD (compare Figure 5.10b), all three deposition thicknesses can be estimated: the inner tungsten electrode thickness of ∼11 nm, the protective insulator film thickness of ∼19 nm and the outer tungsten electrode thickness of ∼40 nm.

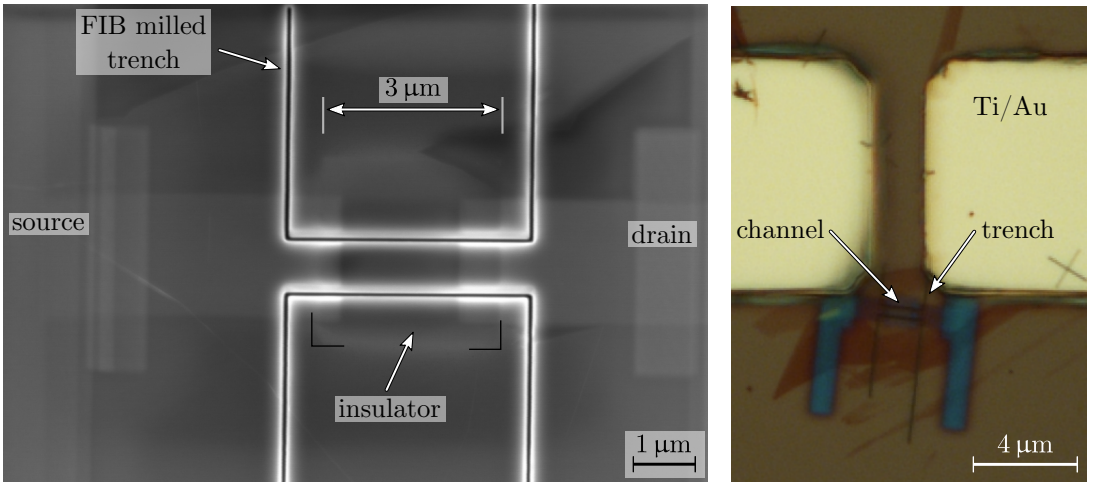
The trenches were milled as a last step. Although some charging is visible in the SEM (Figure 5.9a), the graphene underneath the insulator film is expected to be unaffected, and the AFM results support this assumption.

During electrical characterization, an over-current was applied (5 V drain voltage) before any results could be obtained.

5.2.4 Other devices using e-beam-assisted deposition (device S2)

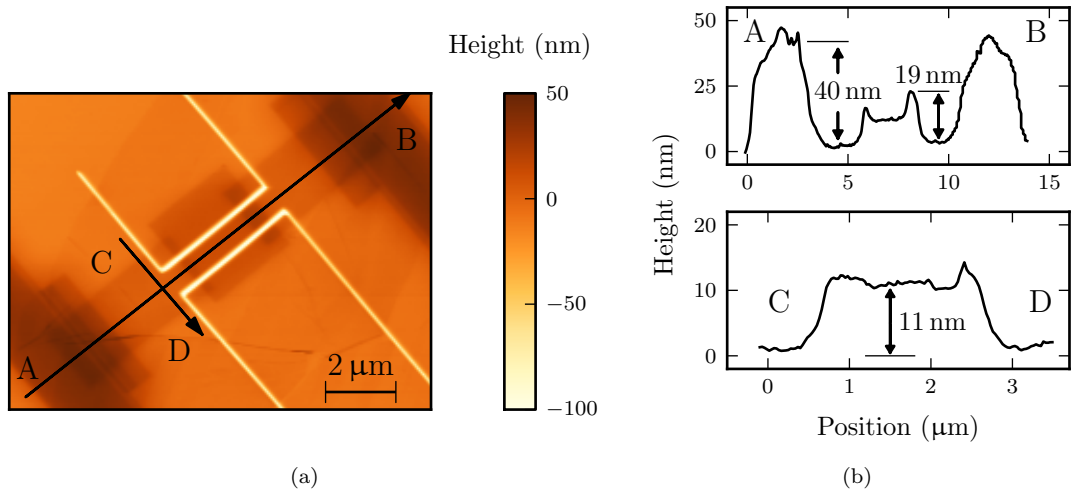
After damaging device `314-223` without obtaining any electrical data, two more devices (identified as `S1` and `S2`) were fabricated in a very similar manner. However, only `S2` could be electrically characterized. Therefore only `S2` is mentioned in this Subsection.

The pattern file was slightly modified as compared to device `314-223`, as can be seen in Figure 5.11a which shows the device after SEM/FIB fabrication. The larger tungsten leads now extend only in one direction. When preparing the pattern file for device `314-223`, the intention was to align the two Ti/Au pads from left and right. However, it



(a) (b)

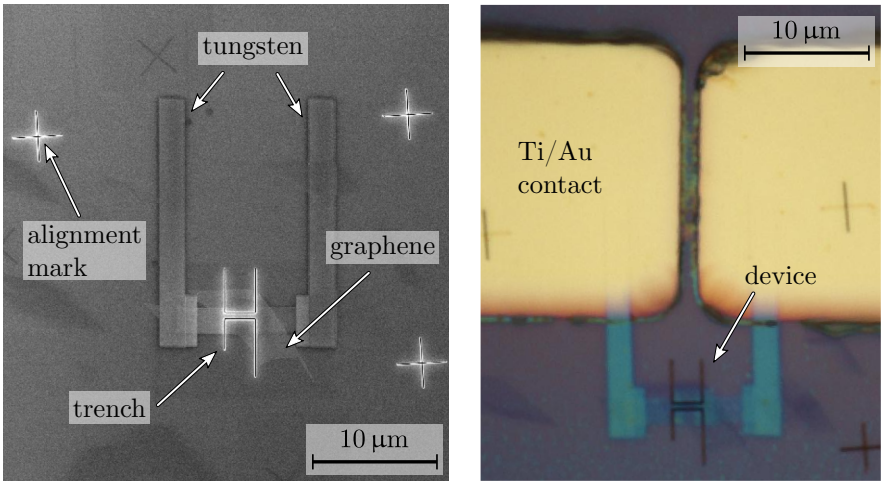
Figure 5.9: Fabrication results of device `314-223` based on e-beam-assisted deposition and FIB trench milling. (a) SEM micrograph showing the channel region. The insulator patch protecting the channel is indicated. (b) Optical micrograph showing the device after probe pad deposition.



(a) (b)

Figure 5.10: (a) AFM height data of channel region of fabricated device `314-223`. (b) AFM profiles as indicated in (a). AB shows the profile along the channel region. The indicated step of 19 nm corresponds to the deposited oxide thickness. The thickness of the inner electrodes is 11 nm, as obtained from the CD profile. The outer tungsten thickness of 40 nm is also obtained.

turned out that the alignment from top or bottom is easier (compare contacted device shown in Figure 5.11b). The inner contact and trench distances are 1 µm and 0.5 µm, respectively. The exposure conditions for the inner tungsten, insulator channel protection, outer tungsten and FIB trenches are listed in Table 5.3. In this device, an e-beam acceleration voltage of 10 kV with an aperture of 30 µm was used resulting in a current of 240 pA.



(a) (b)

Figure 5.11: (a) SEM micrograph showing device `S2` after FIB/SEM fabrication. The tungsten leads extend in only one direction. (b) Optical image of device after contacting by Ti/Au lift-off.

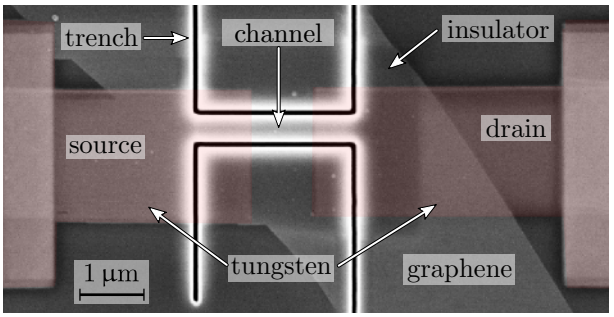


Figure 5.12: SEM micrograph showing closeup of channel region of device `S2`. Tungsten is shaded red for better visibility.

Exposure step	t_{dwell}	**Spacing**	**Loops**	**Dose**	**Exp. mode**
Tungsten dep. 1 (E)	0.16 ms	4 nm	2	0.48 C/cm^2	LV
Insulator dep. (E)	0.16 ms	4 nm	1	0.24 C/cm^2	LV
Tungsten dep. 2 (E)	0.1 ms	2 nm	2	1.2 C/cm^2	LV
Trench milling (F)	0.2 ms	1 nm	60	1.2 µC/cm	LU

Table 5.3: Conditions used for device `S2`. (E) indicates E-beam, (F) indicates FIB. Legend for exposure modes: LV is linear mode in V-direction, LU is linear mode in U direction. See Figure A.2 on page 129 for detailed explanation.

The device after probe pad metalization is shown in Figure 5.11b. The separation between the two contacts is not well defined (target distance 4 µm), however, measurements on dummy contacts showed no leakage current. The SEM micrograph in Figure 5.12 is a closeup of the channel region, with tungsten shaded red for better visibility. Note that the vertical shift of the FIB-milled trenches in respect to the tungsten contacts was deliberately introduced during pattern file preparation and is not due to drift. The outer tungsten contacts, however, are shifted by $\sim$ 420 nm to the right with respect to the other pattern features. The exact reason is unknown but most likely due to charging. The designed overlap of 1.25 µm between the two tungsten structures was fortunately sufficient. Based on this image, channel dimensions of $960 \times 390\,\mathrm{nm}^2$ were obtained.

Only drain/source resistance measurements were performed on the device. A channel resistance of 105 MΩ with metallic characteristics, which is considerably larger than the 58 kΩ for the FIB-only device (compare Figure 5.7a), was measured as shown in Figure 5.13. The higher channel resistance might be due to the low conductivity of e-beam deposited metals [151, 152] or a higher contact resistance between graphene and tungsten. An approach to fabricate devices with channel protection and FIB-assisted deposition of tungsten is proposed in Subsection 5.3 on page 118. That approach could potentially reduce the device resistance. When trying to measure the device's back gate modulation after several months, no conduction was observed. There was no further improvement even when the device was annealed at 300 °C for 30 minutes. The reason for the loss of conductivity was not further investigated.

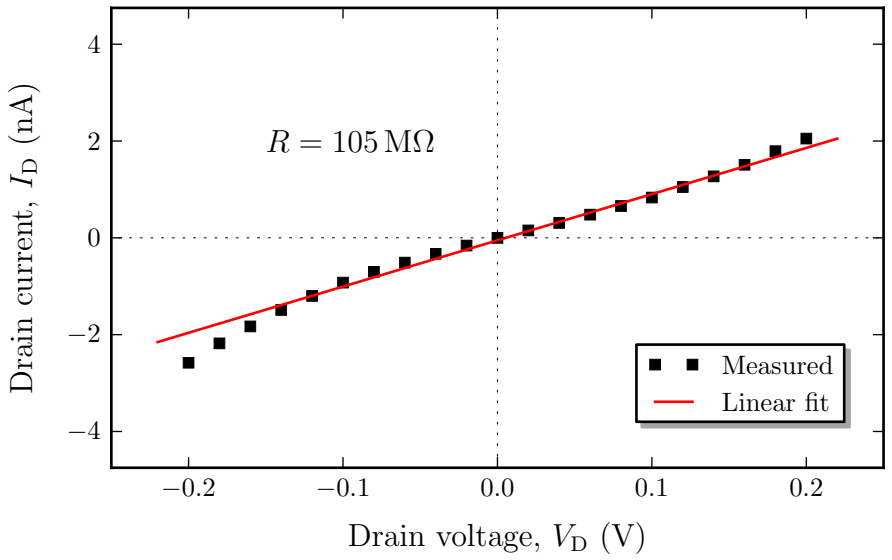


Figure 5.13: Electrical measurement results of FIB/SEM device `S2`. The resistance of 105 MΩ was obtained through linear fit (red line)

5.2.5 FIB-assisted probe pad metalization

The pads shown in Figure 5.14 have been deposited using *Smart SEM* following the procedure described in Subsection 5.1.4 on page 107 and illustrated in Figure 6.1 on page 126. The left pad was deposited with a current of 6.5 nA and has a thickness of 65 nm. The right pad, deposited using 3 nA, has a thickness of 35 nm. Although the step size was adjusted to the beam diameter, faint lines are visible on the right pad. One issue that has been observed but not analyzed is the possible Ga^+-ion contamination of the channel due to this pad deposition. A larger current has a larger halo effect, which is a possible reason for the glow visible around the left deposited pads, shown in Figure 5.14. This structure, which is on silicon carbide and has a solid tungsten strip connecting the two pads, was used to measure the resistivity of FIB-deposited tungsten. Details and results are available in Appendix A.2 on page 131.

5.3 Proposal for device fabrication with very short channel lengths

The prototyping technique outlined in this chapter opens some interesting possibilities. With the ability to do e-beam-assisted deposition, Ga^+-ion induced damage to the underlying graphene can be almost ruled out. However, one problem, which was discussed on page 117 concerning the resistance of device `S2`, is the fact that e-beam deposited metal has a resistivity up to three orders of magnitude larger than the same material deposited by FIB. However, FIB deposition also causes some stray exposure away from the pattern. So when reducing the channel length, most of the channel would be subjected to Ga^+-ions if unprotected.

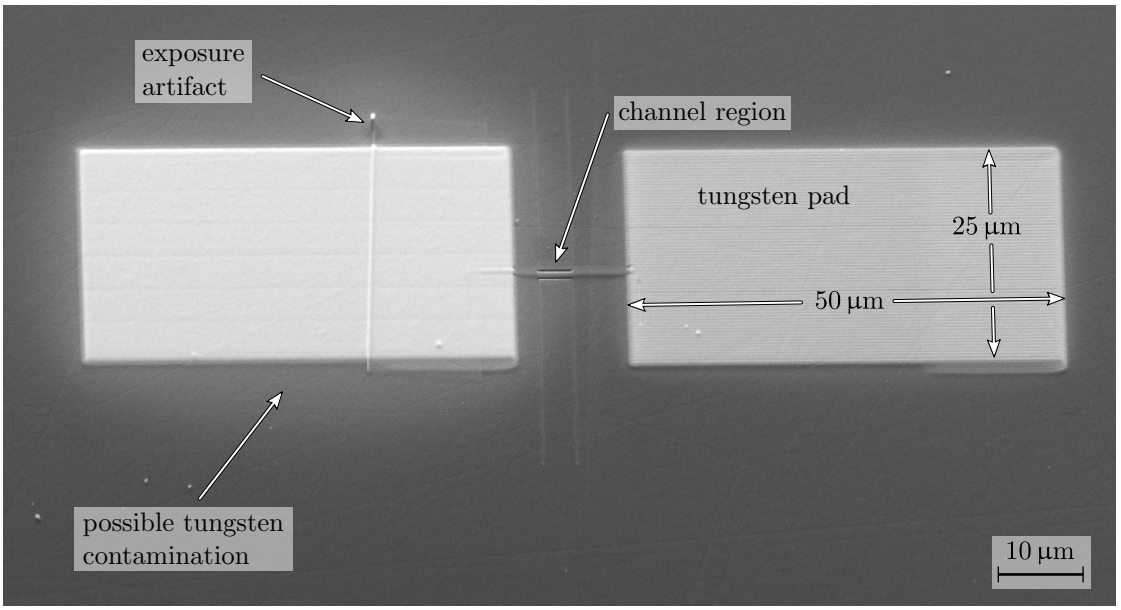


Figure 5.14: SEM micrograph showing two $50 \times 25\,\mu m^2$ large FIB-deposited probe pads. The two pads were exposed using different conditions. Left pad (65 nm thickness) shows glow, possibly originating from Ga^+-ion damage. The right pad is 35 nm thick.

To overcome this dilemma, a strategy entirely based on the above prototyping technique for very short channel lengths with FIB-deposited electrodes was proposed. It should be noted that this proposal has not been experimentally implemented, however, it is included as an example of the flexibility that the high alignment accuracy of the developed prototyping technique offers.

After milling of the alignment marks, an insulator film is deposited by e-beam in the channel region before the tungsten deposition. This film will define the final channel length and protect the graphene from subsequent Ga^+ doping or damage. For channel lengths of more than 500 nm, a process as shown in Figure 5.15a can be used, where the tungsten electrodes overlap the protective oxide area. In case a shorter channel than 500 nm is required, the strategy shown in Figure 5.15b could be successful, as an electrical separation of the two electrodes can otherwise not be guaranteed at that scale. The initially deposited insulator is completely covered by tungsten, followed by an FIB milling across the channel. This milling has to be very precise both in position and depth, in order to reliably separate the tungsten while not reaching the underlying graphene film. The penetration depth of Ga^+-ions through e-beam deposited insulator was not investigated, but this information would be necessary to determine the necessary thickness of the insulator protection.

Based on the results of e-beam-assisted insulator line deposition, which are described in detail in Appendix A.3.4 on page 138, insulator lines as narrow as 300 nm are feasible (compare profile 3 and 5 in Figure A.12 on page 138).

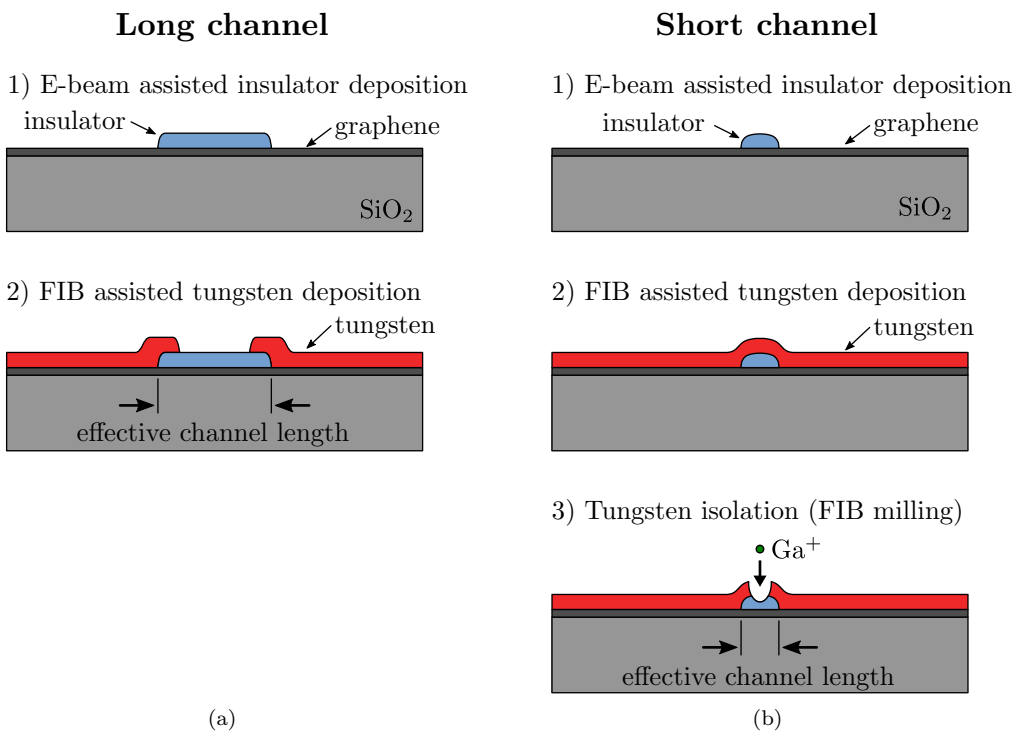


Figure 5.15: Illustration of methods for very short channel lengths based on e-beam-assisted insulator deposition and FIB-assisted tungsten deposition. The cross section is along the center of the channel. (a) Process chart for channel length of more than 500 nm. (b) Process chart for channel length of less than 500 nm.

5.4 Summary

In this Chapter, a prototyping technique based on FIB and SEM has been introduced. The focus of the technique is to enable graphene-device prototyping using FIB. The inherent problem, that any FIB imaging of graphene which is normally necessary for accurate alignment immediately causes significant damage, was solved by introducing a systematic high accuracy alignment procedure (< 250 nm) based on the capabilities of the *ELPHY Quantum* lithography attachment. Three graphene devices, fabricated following the technique, were described, and a channel resistances of 58 kΩ was achieved in line with published results. Two probe pad metalization approaches were introduced: the preferred resist-based metal lift-off approach, and the FIB-based approach. The latter opens the possibility to fabricate a fully functional device inside the FIB/SEM microscope. Deliberately exposing the contacted graphene to an FIB or electron beam while monitoring the transfer characteristics would help understand the damage formation of Ga^+-ions in graphene. Two proposals were presented based on the prototyping technique. One is for very short channel lengths with FIB-assisted tungsten deposition, the other one is alternative channel design. Additionally, the FIB technique was applied to the milling of grating structures in optical devices, where the dimensions and location of milled features have to match the used wavelength. Two such examples are presented in Appendix B on page 141, demonstrating the flexibility of the developed technique.

Chapter 6

Conclusions and future work

6.1 Conclusions

In this thesis, a novel large area, metal-free PECVD deposition of nanocrystalline graphene (NCG) has been reported and successfully demonstrated. By using a parallel plate PECVD tool, NCG films with thicknesses ranging from 3 to 35 nm were deposited on 150 mm wet thermal oxidized wafers at temperatures between 700 °C and 900 °C. Very high thickness uniformity (up to 96%) and low surface roughness (RMS down to 0.23 nm) were achieved. Raman mapping also showed the high cluster diameter (or grain size) uniformity of 98.9%. NCG films with a thickness of 30 nm show promising sheet resistances of 3.73 kΩ/□. In addition, NCG films deposited on quartz and sapphire glass were studied to evaluate their performance as transparent electrodes. The sheet resistances of 2.5 and 13 kΩ/□ at transparencies of 65% and 85%, respectively, are very promising.

The compatibility of the developed NCG films with surface microfabrication processes has been demonstrated through extensive fabrication process development. It has been shown that the NCG films are penetrated by HF vapor, allowing release of the underlying SiO_2 layer in large areas. The films are also readily patterned by oxygen RIE with a resolution better then 1 µm. Ohmic contacts form between the NCG films and Ti/Au. Raman investigations on underetched NCG films suggest that the as-deposited films have compressive stress. Devices with top-gated NCG strips show that thinner NCG films exhibit a stronger gate modulation. The fabrication of NCG nanowires has not been entirely successful. The oxygen RIE etching step used to form the nanowires has been found to be unsuitable and should be replaced by ion milling. Nevertheless, thin film transistors (TFT) were measured showing metal-like behavior with a weak back gate modulation, which can be improved by the use of a top gate or thinner gate oxide.

An SEM/FIB prototyping technique, specifically aimed at graphene work, has been developed. Through the consequent use of an alignment marker system, any detrimental exposure of graphene to Ga^+-ions is avoided. The technique allows the combination of e-beam and FIB based fabrication steps to increase the flexibility. Extensive work has been done on the development of conditions for e-beam-assisted deposition of tungsten and

insulator, and FIB-assisted deposition and milling. Several transistors were fabricated and measured, and a low channel resistance of $\sim 58\,\mathrm{k}\Omega$ was achieved for devices with FIB-deposited contacts. The application of the technique to non-graphene devices was demonstrated as well.

6.2 Future work

Recommendations for future work are split into two parts, according to the two different topics of this thesis.

6.2.1 Large area metal-free PECVD deposition of nanocrystalline graphene

Although a lot of work has been done in developing the PECVD deposition process and device fabrication processes based on these films, many aspects remain unexplored. In the author's opinion, further work should be carried out in the following fields:

1. **Optimization of current deposition process**
   Only eight full wafer depositions were evaluated in this work. It is therefore unlikely that the ideal deposition conditions have been found. Further investigation should focus on the following aspects:

   (a) **PECVD deposition at lower methane concentration** Reducing the methane concentration during plasma deposition decreases the growth rate, making the resulting thickness more controllable. This might help to increase the cluster diameter of the NCG films and further improve the deposition uniformity. As mass flow controllers have only a certain accuracy, it is advisable to increase the addition of hydrogen or argon, instead of simply reducing the methane flow rate.

   (b) **Optimize cluster diameter** The deposition conditions, including substrate pre-treatment, require additional investigation to see how they influence the cluster diameter L_a. It was shown in Figure 3.13 on page 57 that one parameter with positive effect on the cluster size is the NCG thickness. There might be, however, other parameters that have a significant influence on this important NCG property.

2. **Deposition on different materials**
   In this work, deposition of NCG on SiO_2, quartz glass and sapphire glass were investigated. It should be further investigated whether deposition is possible on additional carrier materials, such as Si_xN_y, Al_2O_3 (deposited by, for example, atomic layer deposition) or silicon. It would be of benefit to know if the NCG properties are affected by the underlying material, and whether the deposition rate varies.

3. **Device fabrication development**
   The purpose of the device fabrication development in Chapter 4 on page 67 was to demonstrate the suitability of the NCG for microfabrication. This work has not been concluded yet and requires additional attention. A second iteration of the different processes, based on the findings in this thesis, is highly recommended. In detail, the author makes the following recommendations:

   (a) **Membrane devices** Special attention should be paid to the suspension of NCG, as this would open a large range of applications. This includes better estimation of the mechanical stress of as-deposited films, and measurement of the mechanical properties by nanoindentation experiments. The current route using ICP etching should be further pursued. At the same time, it would be of benefit to attempt such membrane fabrication using KOH etching. This will require, however, modification of the photolithographic mask.

   (b) **Suspended beam** The fabrication process for suspended NCG beam structures reported here resulted in the NCG sticking down after HF vapor etching. It is therefore essential to do both, increase the sacrificial oxide thickness (currently 254 nm, recommended $> 2\,\mu m$) and prepare a modified mask design similar to the one proposed in Figure 4.13 on page 82. Furthermore, alignment marks have to be patterned in an additional process step to allow fabrication of structures with very thin NCG (Section 4.5.2.1 on page 77). The questionable result of the HF vapor etching, as mentioned in Section 4.5.2.2 on page 77, has to be further investigated.

   (c) **Top-gated structure** PECVD oxide delamination and wrinkle formation occurred at some point between the deposition and the NMP resist strip after lithography and patterning (Section 4.6.2 on page 85). Although device operation was not compromised, this is undesirable and should be addressed in future process development. The first attempt should be to use acetone and IPA for the resist strip instead of NMP. In case this does not solve the observed issues, HfO_2 or Al_2O_3 deposition should be used instead. Such materials had been successfully used by other researchers, as mentioned in Section 2.6.3 on page 31. A reduction of the gate dielectric thickness should be considered, in order to increase the top gate modulation effect.

   (d) **Nanowire** For nanowire formation, an oxygen RIE process was used. Although it was attempted to increase the anisotropy (low pressure, high power), nanowire formation could not be confirmed. Therefore, an inert ion milling process (e.g. Ar) and samples with very thick NCG ($> 50\,nm$) should be used first. Once nanowire formation was confirmed, further steps can be considered to improve the process. Depending on the uniformity of the NCG films and the ion milling process, overetching could be used to accurately tune the NCG nanowire dimensions. Additionally, e-beam lithography could help to

improve the edge roughness of the trench etched into the SiO_2 (roughness is visible, for esample, in Figure 4.26 and Figure 4.27a on page 98.

4. **Examine crystal structure of NCG**
   The cluster diameter of the NCG films was estimated from Raman peak fitting results. However, it does not offer a lot of information on the atomic crystal structure and alignment of the nanocrystalline graphene domains. Tunneling electron microscopy (TEM) would be very suitable for this, and the successful fabrication of the membrane devices would yield samples suitable for such investigation. Additionally, X-ray diffraction (XRD) should be used to measure crystal constants and orientation.

5. **Transparent electrode application of NCG**
   In Section 3.4 on page 58, preliminary results of NCG deposited on quartz and sapphire glass were reported. The sheet resistance is not competitive with ITO, and work should be done to improve this value. Different methods, such as doping, should be explored. The high resistivity of 7.5 MΩ on sapphire should be verified by an appropriate experimental investigation. Furthermore, for this method to be compatible with TFT screen fabrication, the deposition temperature has to be reduced to below 400 °C. Also, to be used in transparent electrodes, a transfer process to polymer-based substrates has to be developed, although not as a priority.

6. **Transparency measurement using reflectometry**
   The transparency of the NCG films was measured using a transmission measurement setup with integrating sphere. The values obtained this way are very accurate, however, other methods exist. One such method is spectroscopic ellipsometry. It is thus advisable to perform such measurements, compare them with the available values from the transmission measurements, and establish the accuracy of this method. This would allow measurement of transparency even on non-transparent substrates (such as silicon).

7. **Electric and electronic properties**
   The electric and electronic properties of the developed NCG films were touched upon only very superficially, as this was outside the main scope of this work. This aspect should be thus prioritized in future work. To do so, the successful fabrication of transistor devices based on the developed fabrication processes is necessary.

8. **Uniformity of NCG deposition process** Deposition should be carried out on 200 mm wafers to investigate possible improvement of the uniformity of the deposition process. This was discussed on page 54. In the author's opinion, this is not a high priority item.

6.2.2 FIB/SEM prototyping technique

The FIB technique proposed in this thesis has not been widely employed yet, and several areas for future work are identified below:

1. **Fabrication of full transistor within SEM/FIB microscope**
   The possibility of fabricating a fully functional graphene transistor on exfoliated graphene inside the SEM/FIB microscope has been proposed but not accomplished. It would be interesting to fabricate such a structure for two reasons. First, it would be possible to compare the electrical properties of the transistor before and after exposure to ambient conditions. Secondly, in-situ electrical measurement of the channel conduction, while subjecting the channel region to electron or ion irradiation, would allow to observe the effect of this radiation on the graphene.

2. **Fabrication of very short channel**
   In Section 5.3 on page 118, an approach to the fabrication of very short channel lengths by the prototyping technique was proposed. This kind of fabrication, illustrated in Figure 5.15 on page 120, heavily relies on the accuracy of the prototyping technique.

3. **Channel designs**
   The most basic channel shape was used in this work, i.e. straight shape. However, since this is a prototyping technique, the strength is the very flexible adjustment of every aspect of the process. One aspect, which only involves adjustment of the pattern file, is the modification of the channel shape. A U-shaped transistor, also fabricated by FIB, showed an extraordinarily high on/off ratio (see Section 2.5.2 on page 24). Transistor channel designs that can be easily implemented with the developed fabrication method are schematically illustrated in Figure 6.1. This includes U-shape, zigzag, multi-channel and tapered type.

   A strong effect on the device characteristics depending on the channel shape is expected. This is due to anisotropic in-plane electrical properties and the influence of the graphene edges. In the case of a multi-channel device, the relative influence of the edge effect is expected to increase, possibly allowing tuning of the electrical properties. Due to the very good alignment accuracy of the used methods, it is even possible to first fabricate a wide channel and later mill additional trenches to observe the evolution of the transfer characteristics. For the tapered structure, a separate contact for the top and bottom side-gate might yield additional insight into graphene properties.

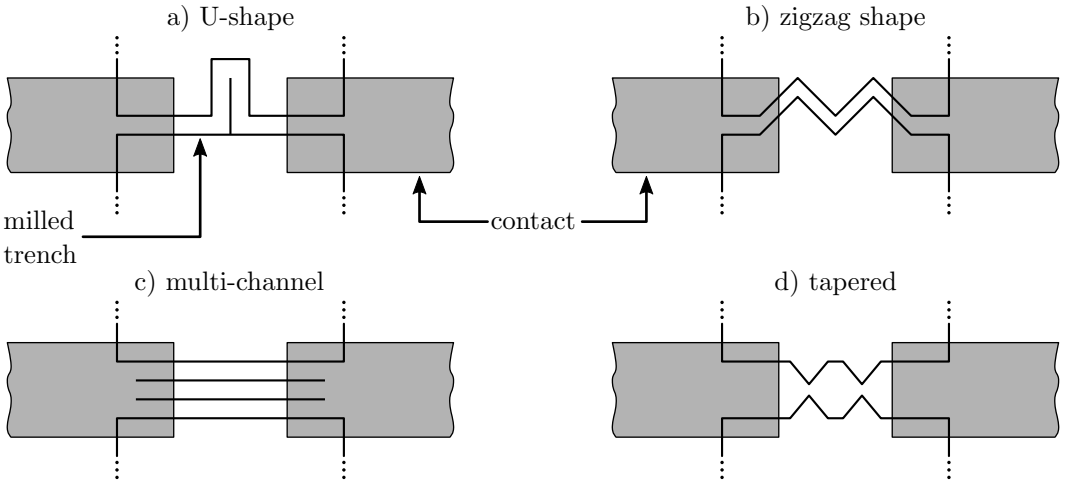


Figure 6.1: Alternative channel designs for graphene transistors fabricated following developed FIB technique. Gray areas represent the tungsten contacts, black lines represent the FIB trench milling.

Appendix A

FIB/SEM conditions (deposition and milling)

One big advantage of FIB technology is the possibility of performing milling and deposition of various materials with the same equipment. FIB-assisted deposition using the *Zeiss NVision 40* microscope is generally done using the control software, *SmartSEM*. Many of the parameters are not visible to the user, in order to facilitate quick and easy operation. However, as explained in Section 2.7.1, for the proposed rapid prototyping of graphene devices with highly accurate alignment, the complete fabrication has to be possible using the *ELPHY Quantum* lithography attachment. Since no recipes existed, extensive experimental evaluation was conducted. This appendix contains all the deposition conditions experimentally determined in this PhD work. The results where then, in turn, used to fabricate the devices, which are shown in Section 5.2 on page 108.

First, the results of FIB-assisted deposition of tungsten using the *ELPHY Quantum* lithography attachment is explained, followed by the measurement of the resistivity of that material. Then, results concerning e-beam-assisted deposition of tungsten and insulator, respectively, are given. This was evaluated for area and line depositions. Finally, results concerning FIB trench milling and FIB alignment mark milling are explained.

A.1 FIB-assisted deposition of tungsten

At first, it was attempted to reproduce the conditions that are used by *Smart SEM* for deposition. The recommended parameters by the manufacturer for tungsten deposition are 0.2 µs dwell time and a pixel fill factor (PFF) of 50%. The PFF gives a relation between beam diameter and step size, and indicates how many per cent of an area will be exposed by a certain beam and a certain step size. So increasing the current (and thus the beam size), while maintaining the step size, will increase the PFF. An increase of step size with a fixed current will result in a decrease of PFF. This concept has, however, some inaccuracies. Firstly, the beam diameter is not measured but taken from a calibration table instead. This table obviously does not reflect the current focus of the beam and might not be up to date. Secondly, step size is not defined but results from

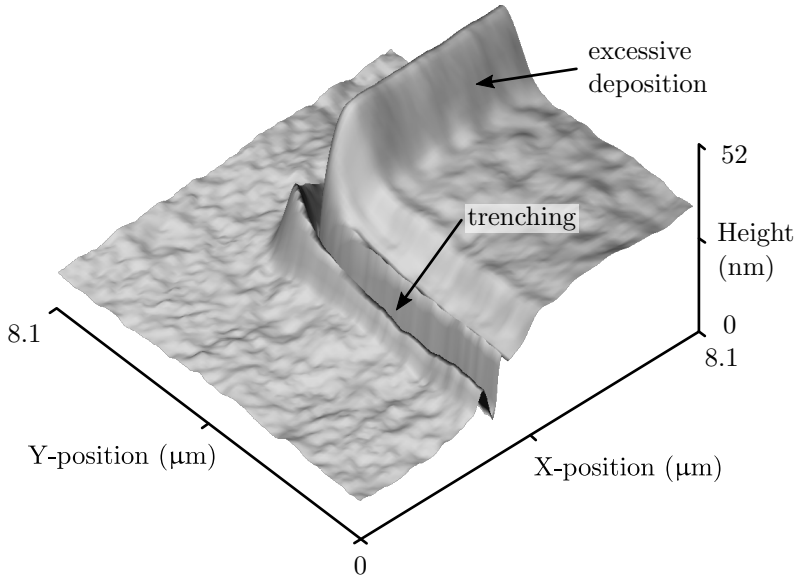


Figure A.1: 3D representation of cropped AFM data of FIB-deposited tungsten. Trenching and excessive deposition can be observed in the edge regions, caused by the prolonged exposure, as illustrated in Figure A.2.

scan resolution and zoom. The scan resolution can be set to different values[1] and defines the number of unique beam positions in the horizontal and vertical direction, which can be addressed. These unique positions are mapped onto the visible area (dependent on zoom level) and thus define the step size. Lower zoom level at fixed scan resolution will increase the step size and thus the physical resolution. As an example, if the horizontal visible size is 35 µm and a resolution of 1024 is set, the resulting step size is 35 000 nm/1024 = 34.2 nm. This, too, relies on calibration data that might not be accurate.

In addition to the difficulty of extracting the relevant value for step size, the *ELPHY Quantum* attachment is limited to a dwell time of 0.4 µs, as explained in Section 2.7.1 on page 34. This is four times as long as the fastest possible by *Smart SEM*.

First, deposition was attempted using 1.5 nA by *ELPHY Quantum*, step size of 100 nm and 0.4 µs dwell time. Although the process time for a 8×8 µm^2 square was 1 hour 40 min, the deposited thickness was less than 30 nm, and a strong trenching was observed. The 3D representation of the AFM data is shown in Figure A.1. At the upper edge, the deposition is higher than anywhere else, while a trench surrounds the structure reaching below the original surface. This is absolutely unacceptable for graphene device fabrication, since any milling of the original surface would automatically isolate the thin graphene film on the surface and hamper device operation.

The reason for the trenching in the edge regions is most easily explained by the way the beam is controlled by the *ELPHY Quantum* system. The scanning of the structure can be either meander-like or along lines in U or V direction. This is illustrated in Figure A.2 for the U-direction. In the areas where the meander turns or where the line

[1] Configured resolutions are 512 × 384, 1024 × 768, 2048 × 1536, 3072 × 2304 and 6144 × 4608.

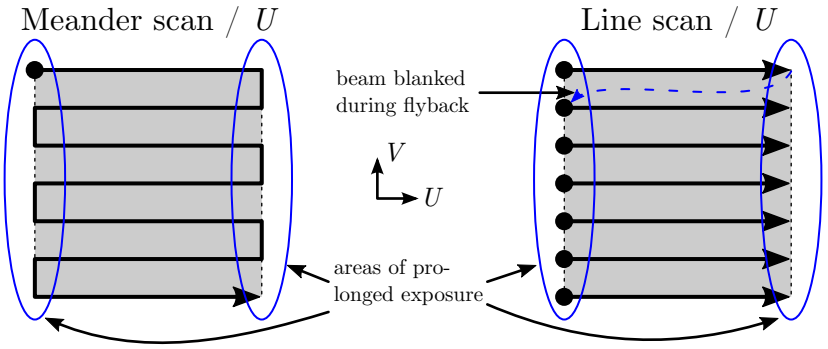


Figure A.2: Illustration of meander and line exposure mode of the *ELPHY Quantum* system in U direction. In meander mode the beam is continuously scanned over the sample, while for line mode the beam is blanked at the end of one line and jumps back (flyback). In both cases the indicated areas are subjected to a higher dose. This applies to the V direction (not shown) accordingly. Scan direction can be also set to auto, in which case U or V is automatically chosen by the lithography attachment.

scan starts/stops, the beam resides longer than the described dwell time. This additional settling time is necessary for accurate pattern writing, but can also lead to the observed trench milling effect around the pattern.

The next experimental evaluation consisted of 13 exposures using 80 pA. The dwell time was set to the minimum of 0.4 µs, while the step size was varied from 4 to 16 nm in 1 nm steps. The resulting ion dose thus varies from 0.2 to 0.013 mC/cm^2. Figure A.3 shows the deposition thickness as measured by AFM. The deposition thickness was additionally correlated to the ion dose and is also shown in Figure A.3. The negative thickness at 4 to 6 nm step size indicates that milling was predominant.

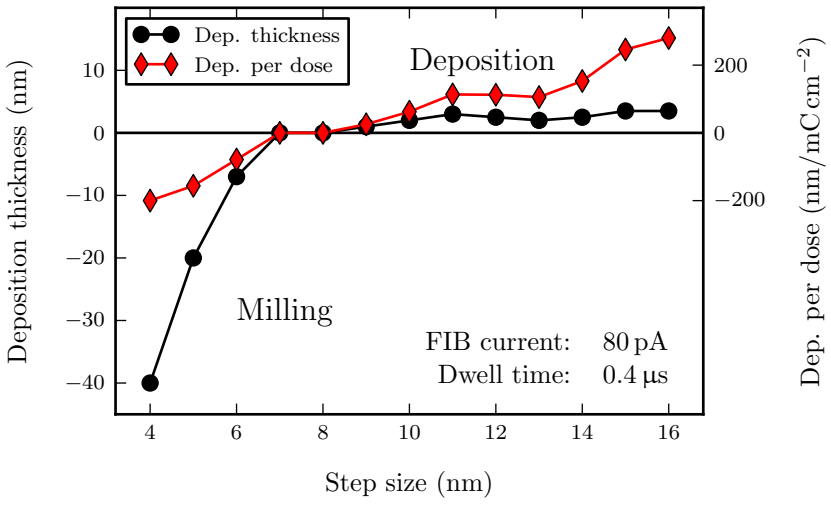
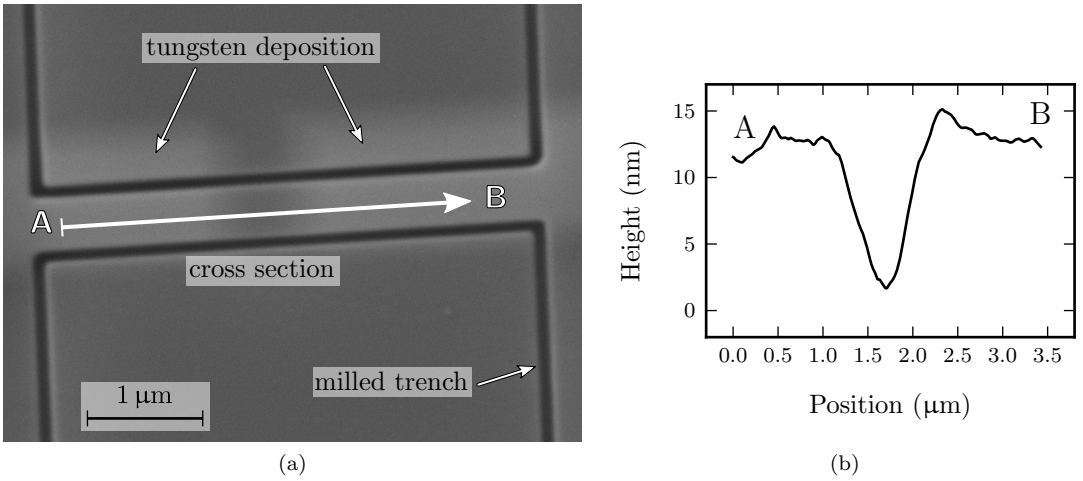


Figure A.3: Measured AFM thickness of FIB-assisted tungsten deposition and the calculated corresponding deposition thickness per dose. A negative thickness indicates that milling is predominant.

The deposition rate with 80 pA was found to be rather low, as shown, and additionally trenching along the pattern edges could be observed for all depositions. Therefore, the FIB current for deposition experiments was changed to 10 pA, with the hope of reducing the trenching effect. In Figure A.4a, an SEM micrograph of a two terminal device fabricated by FIB-assisted tungsten deposition and FIB milling using 10 pA is shown. The exact conditions for the two $9.2 \times 0.9\,\mu m^2$ large patterns in this case were 0.4 µs dwell time, 4 nm step size and 302 exposure loops in V-line mode, resulting in a total process time of 90 min and an area dose of $7.55\,mC/cm^2$. From the AFM data taken along the channel gap (compare Figure A.4b), a resulting tungsten thickness of ∼11 nm was measured without evidence of trenching. The deposition rate in relation to ion dose is merely $1.42\,nm/mC\,cm^{-2}$ (compare deposition thickness per dose values in Figure A.3 for 80 pA beam current), however, the fact that no trenching occures is deemed more important.

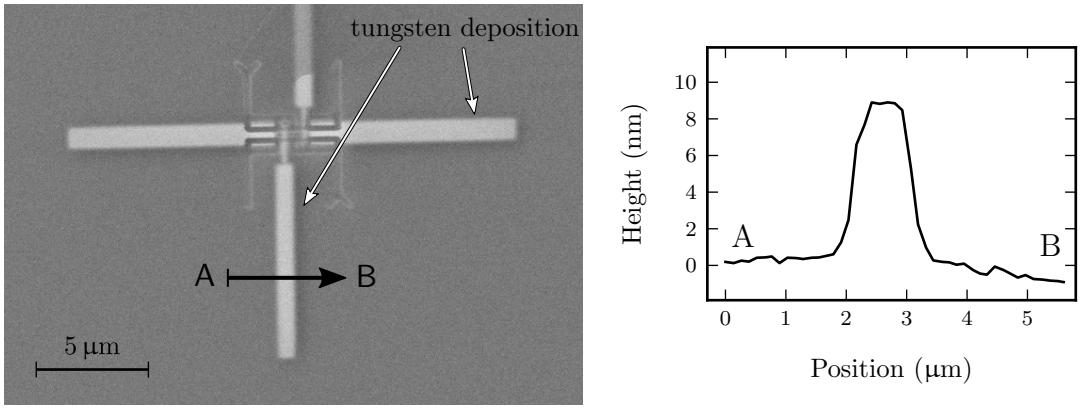
The structure shown in Figure A.5a was written with the same conditions but only 200 exposure loops (area dose $5\,mC/cm^2$). The thickness of the tungsten, as obtained from Figure A.5b, is ∼9 nm, with no detected trenching. The deposition thickness per exposure loop in the second case is 28 % larger, although all other deposition parameters are identical. The exact reason for this difference is not known, but the following could have an influence: The polygons exposed had different dimensions, meaning that the time it takes for the beam to finish one exposure loop is different. Therefore, the number of precursor atoms on the surface might be different, since there is more time for them to replenish. Furthermore, beam focus might not have been identical.

Since the deposition rate was acceptable and, most importantly, no trenching occured, these conditions (10 pA current, 0.4 µs dwell time, 4 nm step size) were used as default values for tungsten deposition by FIB.



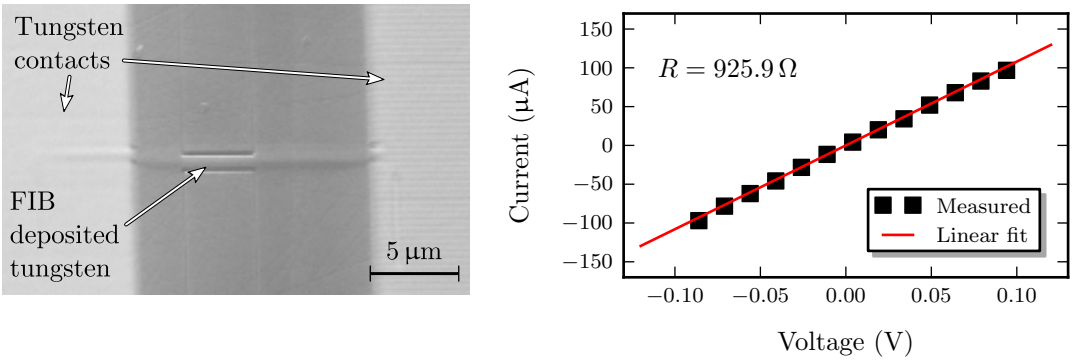
(a) (b)

Figure A.4: FIB-assisted tungsten deposition using 10 pA. (a) SEM micrograph showing two deposited contacts with a 500 nm gap in between. (b) Measured AFM cross section profile AB as indicated in (a). The deposition thickness is ∼11 nm, no trenching observed.



(a) (b)

Figure A.5: Structure comprising FIB-deposited tungsten using 10 pA. (a) SEM micrograph showing tungsten electrodes. (b) Measured AFM cross section profile AB as indicated in (a). The deposition thickness is ∼9 nm, no trenching observed.



(a) (b)

Figure A.6: (a) SEM micrograph of solid tungsten strip deposited by FIB on SiC and contacted by FIB-deposited tungsten pads. (b) Measured channel current as function of applied channel voltage. Resistance $R = 925.9\,\Omega$ obtained from linear fit.

A.2 Resistivity of FIB-deposited tungsten

Resistivity of FIB-deposited tungsten was measured on the reference structure shown in Figure A.6a (SEM of full device is additionally shown in Figure 5.14 on page 119), which was fabricated on SiC without channel gap. The structure was later contacted by FIB-deposited tungsten. Two-probe measurement of the structure resulted in the current readings, shown in Figure A.6b. The resistance $R = 925.9\,\Omega$ was obtained from a linear fit to the measured data. This includes the resistivity of the probe pads, the contact resistance between the pads and the probes, and the contact resistance between the tungsten strip and tungsten pads. Since only one such structure was fabricated and

measured, the individual contributions to the device resistance could not be extracted. The above mentioned contributions are thus ignored in the following calculations.

To calculate the resistivity ρ of the tungsten, the physical dimensions of the tungsten strip have to be known. The length $\ell = 13\,\mu\text{m}$, thickness $d = 10\,\text{nm}$ and width $w = 1.25\,\mu\text{m}$ were extracted from AFM data and SEM images. The contribution of the milled trench is neglected. With this information, the resistivity is calculated by

$$\rho = R\frac{d\,w}{\ell} = 925.9\,\frac{10\times10^{-7}\;1.25\times10^{-4}}{13\times10^{-4}}\,\Omega\text{cm} = 88\,\mu\Omega\text{cm}. \tag{A.1}$$

This value is close to the $218.3\,\mu\Omega$cm reported by Horváth *et al.* [153], and in the same order of magnitude as values published for FIB-deposited platinum [152]. The sheet resistance for this 10 nm thin layer can be also calculated by

$$R_\square = R\frac{w}{\ell} = 89\,\Omega/\square. \tag{A.2}$$

These values are valuable for the interpretation of electrical measurement results obtained from FIB-fabricated graphene devices. They allow more accurate extraction of the graphene properties.

Possible follow-up work would include a series of similar structures with a variable tungsten strip length, allowing the determination of the parasitic resistances.

A.3 E-beam-assisted deposition of tungsten and insulator

Deposition rates of e-beam-assisted tungsten and insulator deposition were experimentally evaluated by depositing adequate structures with varying conditions and measuring the resulting deposition thickness by AFM. Both squares and lines were deposited in order to detect any difference between area and line deposition. The precursor gases are tungsten hexacarbonyl ($W(CO)_6$) for tungsten and 1,3,5,7-Tetramethylcyclotetrasiloxane ($C_4H_{16}Si_4O_4$) for insulator, respectively.

The electron beam acceleration voltage was set to 10 kV with an aperture of 30 µm. This results in a beam current of 240 pA. It should be noted that increasing the aperture size to 120 µm increases the current to 2.64 nA, but the smaller aperture was chosen to achieve the highest resolution. The sample surface was positioned at a working distance of 5.1 mm. Smaller working distances are not possible for deposition due to the fixed GIS nozzle extension.

A.3.1 Area deposition

A preliminary experiment, where $2\times2\,\mu\text{m}^2$ large squares of tungsten had been exposed, was used to determine the minimum dwell time. Dwell times as low as 0.001 ms were tested, which led to results as shown in Figure A.7. The exposure mode is LV[2]. As can

[2]LV denotes linear exposure mode in V-direction. Compare Figure A.2.

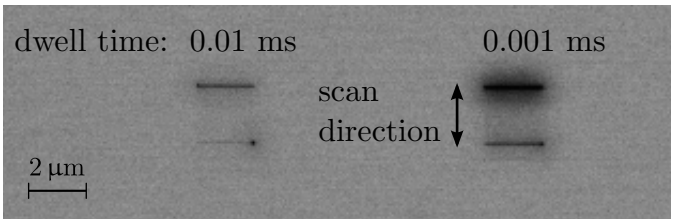


Figure A.7: SEM micrograph showing tungsten rectangles deposited using e-beam with dwell times of 0.01 and 0.001 ms, respectively. The deposition is not uniform.

Deposition 9 Dose: $0.4 \times D_0$ Dwell: 10.24 ms Spacing: 32 nm	Deposition 10 Dose: $0.4 \times D_0$ Dwell: 40.96 ms Spacing: 64 nm	Deposition 11 Dose: $0.4 \times D_0$ Dwell: 163.84 ms Spacing: 128 nm	Deposition 12 Dose: $0.4 \times D_0$ Dwell: 655.36 ms Spacing: 256 nm
Deposition 5 Dose: $0.4 \times D_0$ Dwell: 0.04 ms Spacing: 2 nm	Deposition 6 Dose: $0.4 \times D_0$ Dwell: 0.16 ms Spacing: 4 nm	Deposition 7 Dose: $0.4 \times D_0$ Dwell: 0.64 ms Spacing: 8 nm	Deposition 8 Dose: $0.4 \times D_0$ Dwell: 2.56 ms Spacing: 16 nm
Deposition 1 Dose: $1 \times D_0$ Dwell: 0.1 ms Spacing: 2 nm	Deposition 3 Dose: $1 \times D_0$ Dwell: 0.4 ms Spacing: 4 nm	Deposition 3 Dose: $1 \times D_0$ Dwell: 1.6 ms Spacing: 8 nm	Deposition 4 Dose: $1 \times D_0$ Dwell: 6.4 ms Spacing: 16 nm

Figure A.8: Exposure conditions for e-beam-assisted deposition evaluation. Twelve different conditions are used. The reference dose D_0 is $0.6\,\mathrm{C/cm^2}$. $0.4 \times D_0$ is thus $0.24\,\mathrm{C/cm^2}$. The duration value is the total time of the exposure which consists of exposure time, beam control and data processing overhead.

be seen, the rectangle was not correctly written. It appears that the beam positioning is not able to keep up with the desired stepping speed, or the exposure time is too short to dissociate the precursor gas. Nevertheless, 0.1 ms was identified as reasonable minimum value for the dwell time from these initial depositions.

Next, a series of twelve squares with a size of $2 \times 2\,\mu\mathrm{m}^2$ and a spacing of 10 µm was deposited with different conditions. The exact conditions and the geometric arrangement of the twelve rectangles are shown in Figure A.8. The conditions were chosen in a way which allows direct comparison. The spacing (or step size) of the four depositions at the bottom (1-4) is increased stepwise by a factor of 2 while decreasing the dwell time by a factor of 4. Thus the area dose $D_0 = 0.6\,\mathrm{C/cm^2}$ is identical for all the squares. The same is done for the eight conditions on top (5-12), where the area dose is chosen to be $0.4 \times D_0$, and the dwell time and spacing are modified in the same manner. The machine

time of the bottom depositions of 102 s is reduced to 42 s for the top deposition, which is in the same proportion as the area dose. This indicates that the given conditions require little process overhead.

The depositions were done on a $1 \times 1\,\mathrm{cm}^2$ sized sample (300 nm SiO_2 on Si) and the deposition thickness t was measured using a *Veeco Multimode V* AFM in contact mode with a height resolution better than 0.1 nm.

For quantiative comparison, the deposition per dose value ϵ is calculated by

$$\epsilon = \frac{d}{D},$$

where d is the measured thickness and D is the total electron area dose.

A.3.2 Tungsten area deposition

The obtained AFM image for tungsten area deposition is shown in Figure A.9a. Each of the deposited squares is labeled with a number which correlates to the conditions given in Figure A.8. Figure A.9b contains the corresponding profiles. The chamber pressure during deposition was 2.25×10^{-5} mbar (base pressure $\sim 1 \times 10^{-6}$ mbar).

Ripples can be observed in the cross-section data and the AFM image for sample 11 and 12. The reason for this is that the spacing is significantly larger than the beam diameter. Therefore, spacing should be kept below ~100 nm for smooth deposition. Furthermore, a clear decrease in height from deposition 1 to 4 is visible, although the dose was identical. The same trend is also observed for the 40 % dose deposition (profile 5 to 10). Table A.1 summarizes the measured thicknesses and deposition per dose rates.

A.3.3 Insulator area deposition

Measured AFM results for insulator area deposition are shown in Figure A.10a. Again the labels next to the squares refer to the conditions given in Figure A.8. Figure A.10b contains the corresponding profiles. The chamber pressure during deposition was 1.15×10^{-5} mbar (base pressure $\sim 1 \times 10^{-6}$ mbar).

As for tungsten, the AFM data reveals ripples for sample 11 and 12, which is due to the significantly larger step size as compared to the beam diameter. It should be noted that the insulator deposition is almost unaffected by the step size. Profiles 1 to 4 and 5 to 10 show identical deposition thicknesses, respectively. This is in clear contrast to the tungsten deposition, as shown in Figure A.9b. The measured thicknesses and deposition per dose rates are summarized in Table A.1.

Discussion of area deposition

Comparison of the obtained results for tungsten (see Figure A.9) and insulator (see Figure A.10) area deposition shows a significantly higher deposition per dose rate for the insulator. Ion and electron beam assisted deposition relies on many different factors, and a quantitative prediction of deposition rates is very difficult. A model for ion assisted

Table A.1: SEM **area** deposition thickness t and deposition per dose rate ϵ. Deposition numbers refer to the numbers in Figure A.9 and Figure A.10, respectively. The reference dose D_0 is $0.6\,\mathrm{C/cm^2}$. $0.4 \times D_0$ is thus $0.24\,\mathrm{C/cm^2}$.

Deposition		1	2	3	4	5	6	7	8	9	10	11	12
Dwell time (ms)		0.1	0.4	1.6	6.4	0.04	0.16	0.64	2.56	10.24	40.96	163.84	655.36
Spacing (nm)		2	4	8	16	2	4	8	16	32	64	128	256
Dose (D_0)		×1	×1	×1	×1	×0.4	×0.4	×0.4	×0.4	×0.4	×0.4	×0.4	×0.4
Tungsten	d (nm)	15.9	13.8	12.2	11.1	4.6	4.2	3.6	3.5	3.2	3.3	3.8†	6.7†
	ϵ (nm/C cm^{-2})	26.5	23.0	20.3	18.5	19.2	17.5	15.0	14.6	13.3	13.8	15.8	27.9
Insulator	d (nm)	48.7	48.1	48.2	48.1	18.7	18.2	17.8	17.6	18.2	18.7	21.7†	18.1†
	ϵ (nm/C cm^{-2})	81.2	80.167	80.3	80.2	77.9	75.8	74.2	73.3	75.8	76.5	90.4	75.4

† Surface not smooth. Thickness reading inaccurate.

Table A.2: SEM **line** deposition thickness t and deposition per dose rate ϵ obtained from SEM line deposition tests of tungsten and insulator. Deposition numbers refer to the numbers in Figure A.12. The reference dose D_0 is $12\,\mu\mathrm{C/cm}$.

Deposition		1	2	3	4	5	6	7
Dwell time (ms)		0.5	1	5	10	0.5	1	5
Spacing (nm)		10	10	10	10	1	1	1
Dose (D_0)		×0.01	×0.02	×0.1	×0.2	×0.1	×0.2	×1
Tungsten	d (nm)	0.3	0.6	1.1	1.6	1.2	1.3	8.8
	ϵ (nm/μC cm^{-1})	2.5	2.5	0.92	0.67	1.0	0.54	0.73
Insulator	d (nm)	0.2	0.5	3.0	7.1	3.2	6.9	44.4
	ϵ (nm/μC cm^{-1})	1.67	2.08	2.5	2.96	2.67	2.88	3.7

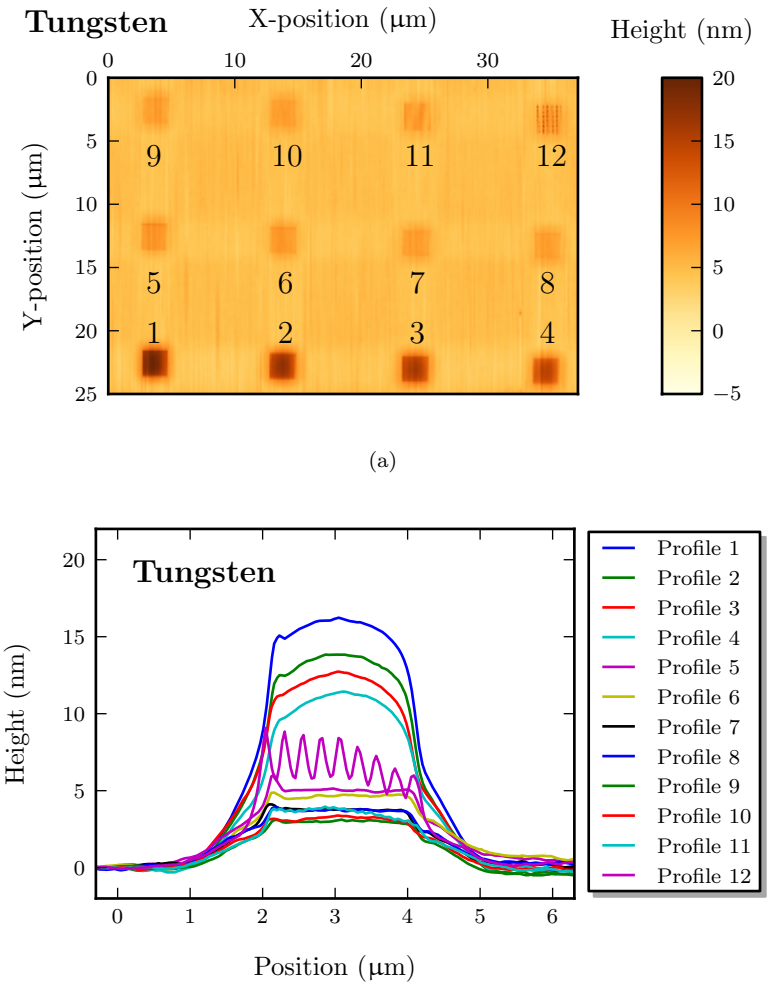
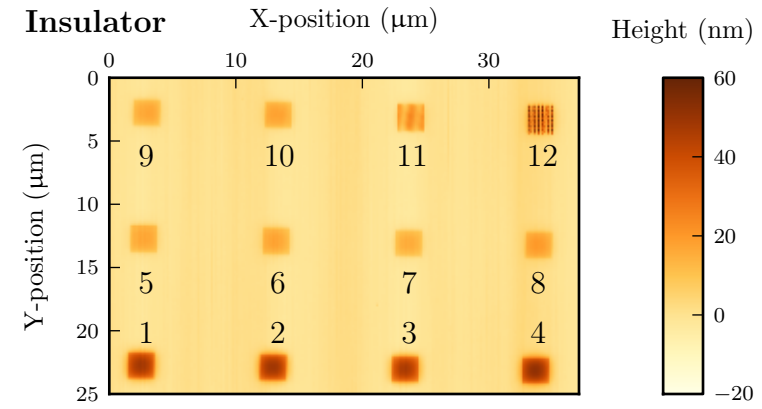


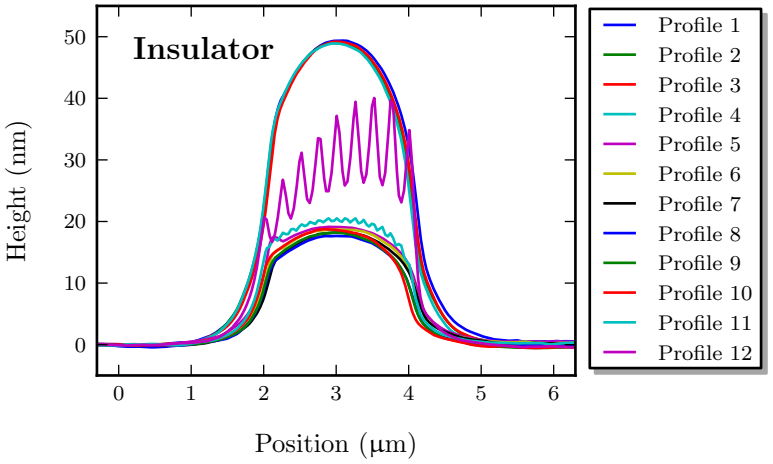
Figure A.9: Results of SEM tungsten deposition evaluation. (a) AFM image showing the test pattern deposited with tungsten. The numbers correlate to the exposure conditions shown in Figure A.8. (b) Cross-section profiles of the twelve depositions. Numbers correlate to (a). The deposition efficiency decreases with increasing dwell time.

deposition had been proposed, which takes into account the process of molecule ad- and desorption (this is dependent on molecule size, number of adsorption sites, gas flux, sticking coefficient and residence time) and the ion/electron beam conditions [154, 155]. Additionally, the number of relevant species per gas molecule (four Si compared to one W) has to be considered.

The observed decrease of the *deposition per dose rate* with increasing dwell time for tungsten, but not insulator, might be coupled to one or more of the factors mentioned above: A specific location on the sample is, as a result of the raster scanning, exposed several times for different durations and with varying periods between the exposures. Variation of each of these three factors will have an influence on the deposition rate. Therefore, no definitive explanation can be given, but the observed effect has to be considered when deciding on exposure conditions.



(a)



(b)

Figure A.10: Results of SEM insulator deposition evaluation. (a) AFM image showing the test pattern deposited with insulator. The numbers correlate to the exposure conditions shown in Figure A.8. (b) Cross-section profiles of the twelve depositions. Numbers correlate to (a). The deposition efficiency is not affected by dwell time.

Another property of the deposited material that has to be mentioned is the size difference between pattern and measured deposition. As can be seen from the AFM profiles (see Figure A.9b and Figure A.10b), material has been deposited as far as 1 µm away from the directly exposed area. This stray deposition effect is further illustrated in the SEM micrograph, shown in Figure A.11. Compared with FIB-assisted deposition, stray exposure with e-beam-assisted deposition appears to be stronger.

In conclusion, area deposition with a short dwell time and small spacing offers the largest deposition per dose rate (see deposition 1 in Table A.1). Spacing exceeding 100 nm should be avoided since it results in non-uniform deposition.

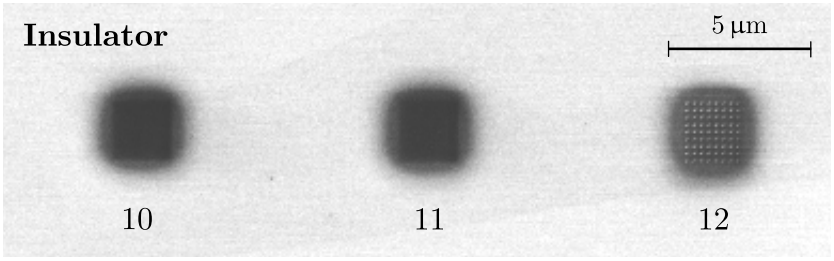


Figure A.11: SEM micrograph of e-beam deposited insulator. The numbers refer to the exposure conditions detailed in Figure A.8 and Table A.1. Deposition outside the $2 \times 2\,\mu m^2$ squares is visible.

A.3.4 Line deposition of tungsten and insulator

In some cases, it is necessary to deposit tungsten wires or very narrow strips of insulator. To achieve this, a line element is exposed. To evaluate the best conditions, seven lines with a length of 2 µm were exposed according to the conditions detailed in Table A.2. In an initial trial, the dwell time was varied in a quite large range from 0.01 ms to 10 ms, however, dwell times below 0.5 ms at a spacing of 1 nm did not yield any deposition that could be detected by AFM. This effect has been described at the beginning of this section on page 132 and shown in Figure A.7. The AFM profiles measured perpendicular to the lines are shown in Figure A.12, where the profile numbers correspond to the number listed in Table A.2.

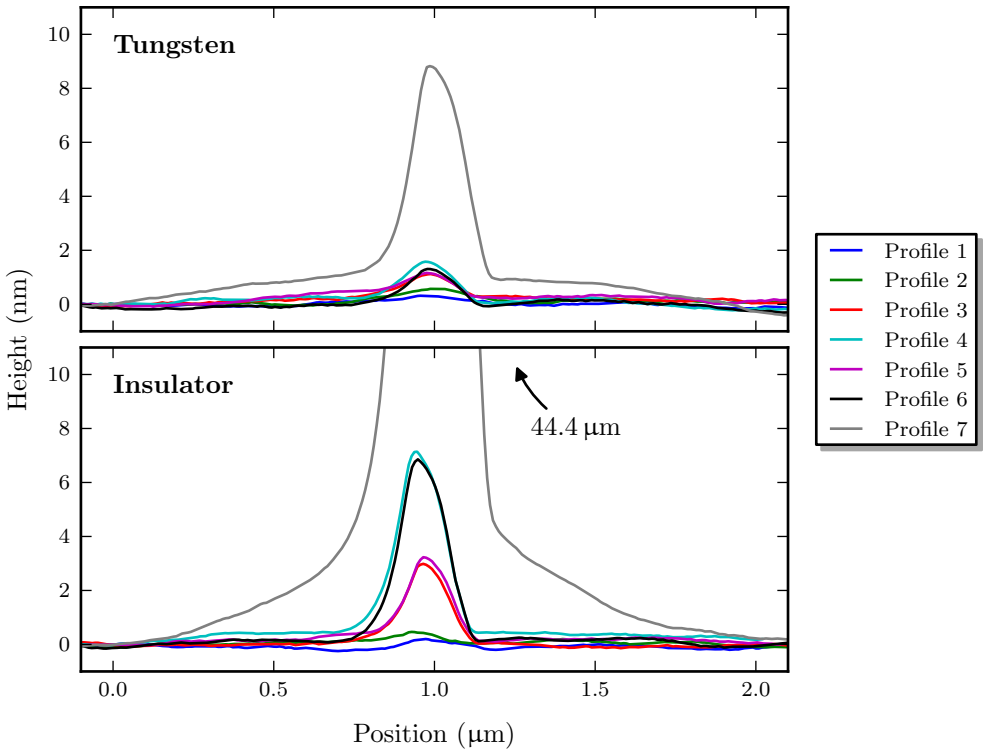


Figure A.12: Measured AFM profiles for e-beam-assisted line deposition of tungsten and insulator. The conditions for profile 1-7 are listed in Table A.2.

The measured (*Veeco Multimode V* AFM in contact mode) maximum deposition thicknesses are listed in Table A.2 for tungsten and insulator. Additionally, the calculated deposition per dose rate is provided. As with area deposition, the deposition rate of insulator is significantly larger (up to four times higher, see Profile 7). Although the e-beam was scanned only once, the deposition width is at least 200 nm for any dose. Insulator deposition appears to be insensitive to the exact spacing and dwell durations. Deposition 3/5 and 4/6 with relative dose of 10 and 20%, respectively, yield almost identical thicknesses. Also the thickness of insulator deposition 7 is ~ 5 times larger than that of 4/6, which correlates with the line dose. Tungsten deposition, on the other hand, is lower, as previously observed for area deposition, and less predictable.

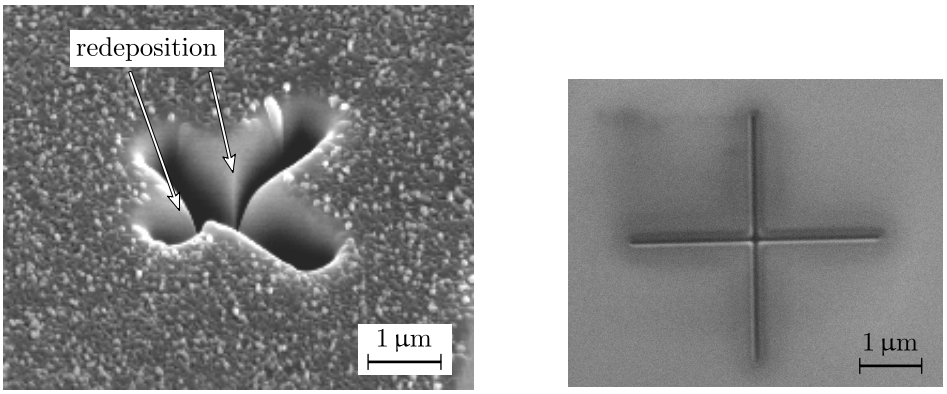
One more important observation is that the profiles are not symmetric around their maximum. In fact, it appears that the deposition on the right side tends to be larger. This can be explained by the precursor gas flow over the sample, since the GIS nozzle was located to the right of the scanned area. This effect is visible independent of the AFM scan direction.

A.4 FIB trench milling

The FIB fabrication technique, introduced in Chapter 5 on page 103, requires a trench milling step in order to define the channel region. This trench should, ideally, be as narrow as possible with absolutely vertical side walls. However, in reality this is not possible. Due to the Gaussian beam shape, the trench will have rounded trench edges, and the trench width depends on both beam current and focus. In any case, a line element in the pattern design will always yield the smallest possible trench width.

Acceleration voltage was kept constant at 30 keV for all milling. The first tests were performed using 300 pA beam current. The trenches were clearly defined, but had widths in the range of 350 nm. With improved settings (38 nm step size, 0.1 ms dwell time), trench widths of 200 nm could be achieved, which is still rather wide.

Reducing beam current and thus the beam diameter obviously reduces the trench width, however, some limitations exist. First, it becomes more and more difficult to accurately focus at lower currents ($\leq$1 pA). Secondly, every incident Ga^+-ion has a certain sputter volume that can be larger than the beam diameter [156]. This means that an incident Ga^+-ion creates damage in a much larger area than the ion diameter. Thus, reducing the beam diameter below the dimension of the damage radius has very little positive effect on the final trench width. On the contrary, reducing current further reduces the milling rate and thus increases the process time. A good compromise for the used FIB system is found at 10 pA beam current, 1 nm spacing, 0.1 ms dwell time (line dose $D_{\text{line}} = 10\,\text{nC/cm}$) and at least 30 exposure loops. This allows trench widths down to 80 ± 10 nm. Accurate measurement of the trench width from SEM micrographs, however, is difficult, as the Gaussian beam shape leads to blurred edges.



(a) (b)

Figure A.13: SEM micrograph of FIB-milled alignment marks. (a) Marks used as default for *Smart SEM* cross section milling. Due to single exposure with large current significant redeposition occurs. (b) Mark milled according to developed milling recipe. The low current of 10 pA and 40 exposure loops result in a uniform trench width of ∼80 nm and a clearly defined center point.

A.5 FIB alignment mark milling

Accurate re-alignment to predefined marks is absolutely crucial for the rapid prototyping technique, outlined in Chapter 5. This is only possible if these are clearly visible and well defined.

Alignment marks are commonly used with FIB, however, these are mostly milled with a very high current. This allows for a very quick writing (less than 10 s), but these alignment marks suffer from excessive redeposition. Such a mark is shown in Figure A.13a. The milling step from upper-left to lower-right was done last, resulting in a partial closing of the first trench. This and the large trench width of ∼1 µm makes the accurate location of the mark center difficult.

Therefore, several conditions for mark milling were evaluated in this work, with some overlap to the trench milling evaluation mentioned in section A.4 above. The obtained mark shown in Figure A.13b was milled using the *ELPHY Quantum* system. It is clearly visible under optical microscopy, SEM, and FIB imaging. Furthermore, it is well defined, and has an acceptable write time of less than 2 minutes. An FIB current of 10 pA is used. Dwell time and spacing are 0.2 ms and 1 nm, respectively. The mark is exposed 40 times (resulting line dose is 100 nC/cm). The trench depth was not measured but is estimated to be at least 80 nm.

Appendix B

Application of prototyping technique to non-graphene devices

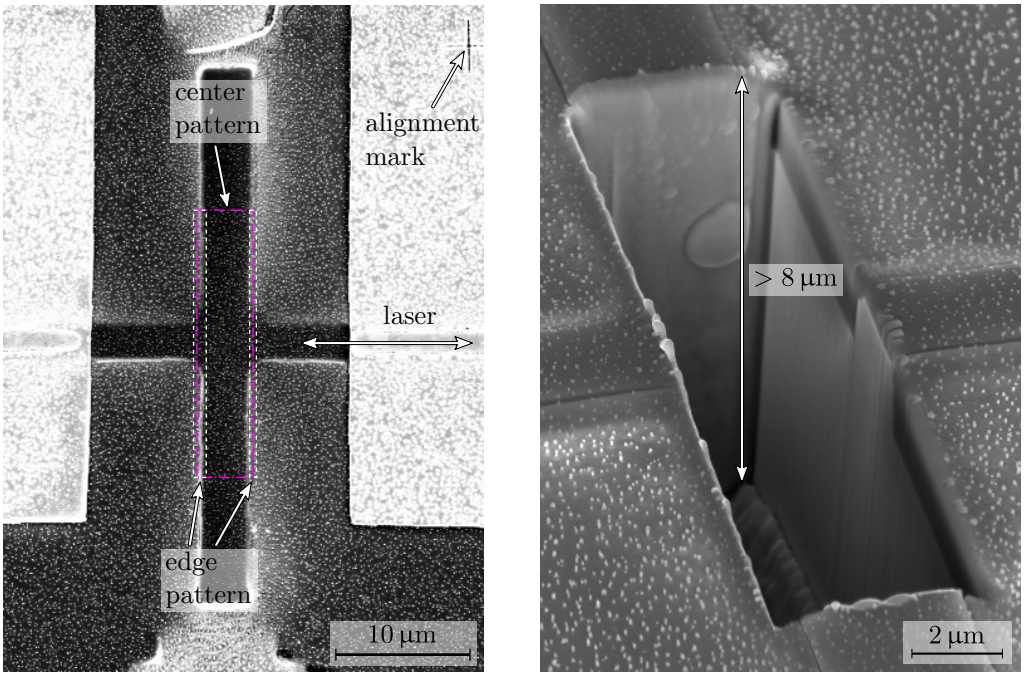
The development of this FIB/SEM prototyping technique, described in Chapter 5 on page 103, was motivated by the lack of reliable FIB-based prototyping of graphene devices. However, the technique can be applied to any application where highly accurate, low-damage FIB milling is necessary. One such field is optics, where often accurate dimensions are required to match the used wavelengths. In the following Sections, two examples of such applications are shown, which were carried out by the author. The device fabrication and consecutive evaluation was the work of other researchers.

B.1 Milling of deep trenches in lasing device

A lasing device, developed and fabricated at the University of Glasgow by Shahid Mahmood [157, 158], was not performing as expected. The reason was that one of the last steps of the lengthy and complicated fabrication process was unsuccessful. Thus, the required grating structures (trenches several µm deep) could not be realized. The devices were then transferred to Southampton where the author attempted to form the gratings by FIB. The reason for choosing the developed protoyping technique was to ensure accurate positioning and trenches perpendicular to the lasing direction.

One such device is partially shown in Figure B.1a. The vertical dark area is the desired location of the grating structure. The initial requirements were to mill two trenches at each such position with a center-to-center distance of 724 nm and a width of 362 nm. The target etch depth for these trenches was $\sim 2.5\,\mu m$ (vertical through the core) in order to increase the reflectivity.

The alignment mark milling and alignment did not pose any problems. However, it was difficult to mill these narrow trenches with such a high aspect ratio. In fact, for given conditions, the etch depth would not increase above a certain dose. This is due to



(a) (b)

Figure B.1: FIB milling of lasing device. (a) SEM micrograph of device before milling. Pattern file (dashed rectangles) shows location of high current milling in center and low current milling at the edges. (b) SEM micrograph showing side view of milled device. The trench is $\sim 4.2\,\mu m$ wide and more than $8\,\mu m$ deep.

the re-deposition of milled matter. Atoms removed at the bottom of the trench become increasingly likely to deposit on the side walls as the trench gets deeper. Finally, a depth of $> 3\,\mu m$ was achieved by using 1.5 nA beam current, 4 nm spacing, 0.01 ms dwell time and 40 exposure loops (line dose $60\,\mu C/cm$). The devices were then measured in Glasgow, however, the lasing capabilities of the devices had degraded significantly. The reason for this degradation was the non-vertical sidewalls of the trenches and resulting scattering.

The final solution was to mill a single trench with a width of $4.2\,\mu m$. This would still allow lasing while reducing the redeposition effect. Such a milled trench is shown in Figure B.1b. The depth is larger than $8\,\mu m$ and the width at the top and bottom are $4.76\,\mu m$ and $3.66\,\mu m$, respectively. This means that the side walls are not perfectly vertical. To estimate the width at the bottom of the core region, at a depth of around $2\,\mu m$, a linear inclination is assumed, resulting in a lasing-width of $\sim 4.2\,\mu m$. To achieve such vertical sidewalls, a two stage milling process (two different beam currents) was necessary, which would not have been possible without the accurate re-alignment capabilities of the FIB technique. The pattern file is indicated by dashed rectangels in Figure B.1a. The central $20 \times 4.2\,\mu m^2$ large pattern was first milled with a FIB current of 1.5 nA, 4 nm spacing, 0.01 ms dwell time and 15 exposure loops (area dose $1.4\,C/cm^2$, exposure mode meander in V direction). The sidewalls were bulged after this milling

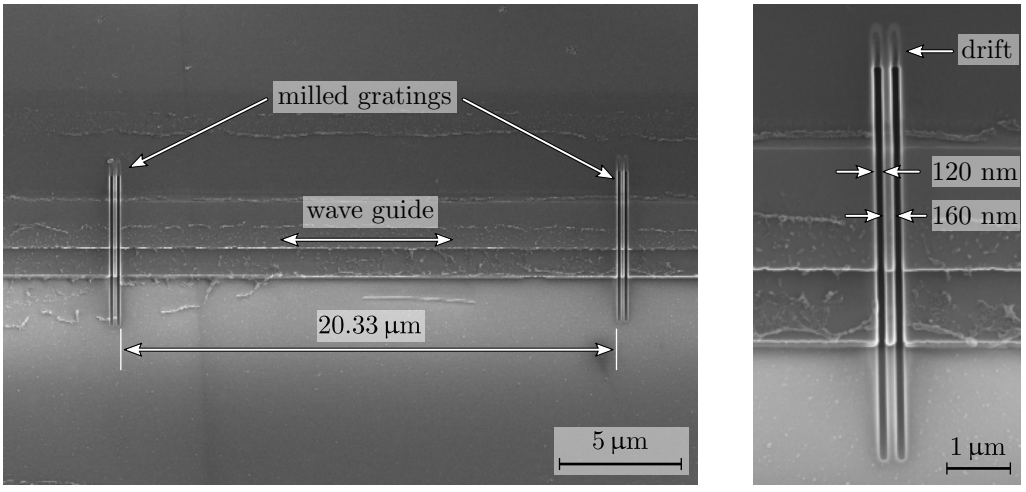
due to redeposition. Thus, in a second milling step, the edge patterns (compare Figure B.1a) were milled with a beam current of 80 pA, 4 nm spacing, 0.01 ms dwell time and 30 exposure loops (area dose 0.15 C/cm^2, exposure mode meander in V direction). The two edge patterns extend 250 nm to the outside of the center pattern, with a width of 950 and 500 nm for the left and right pattern, respectively. The increased width of the left pattern was necessary. With only 500 nm width, a lamella would remain at the bottom of the trench. The difference between the left and right side is due to the meander scan direction from left to right.

In total, more than ten devices were modified as mentioned above, with a yield of 100 % and without any alignment issues. The main challenge was instead to obtain optimal milling conditions.

B.2 Patterning of gratings in waveguide structure

A second non-graphene application for the protoyping technique was to accurately mill two double-gratings into a waveguide with a distance of 20 µm. The waveguide was developed and fabricated by Taha Ben Masaud from the University of Southampton [159]. Part of such a waveguide is shown in Figure B.2a, comprising the two milled double-gratings. The distance of the fabricated devices of 20.33 µm is just slightly larger than the target value. A closeup view of one such double-grating is shown in Figure B.2b. The trenches are 120 nm wide with a gap of 160 nm. The target width was 150 nm; however, it was decided to first measure the gratings obtained, before trying to further optimize the conditions. To achieve the clearly defined trenches, four narrow rectangles were defined in the pattern file ($6 \times 0.1\,\mu m^2$ with 170 nm distance). The exposure conditions were 10 pA beam current, 10 nm spacing, 0.1 ms dwell time and 100 exposure loops. The exposure mode was meander mode in V dirction, and the total exposure time for the four trenches was just below 10 minutes. During milling an initial drift effect was observed (see Figure B.2b), which might be due to surface charging. Luckily, the drift direction was exactly aligned with the V axis of the pattern file and was thus no problem.

After measuring the device it became evident that FIB-milled grating would not help to achieve the required device performance, no matter how accurately milled. The reason is that implanted Ga^+-ions result in significant optical absorption (similar to all metal ions). This route was thus not further pursued. Nevertheless, the obtained milling results demonstrate the high accuracy which can be achieved by the FIB technique. The full process, including milling conditions development, took less than 8 hours in total.



(a) (b)

Figure B.2: FIB milling of gratings into optical wave guide. (a) SEM micrograph of milled device. Two double-gratings were milled with a inner target distance of 20 µm. (b) Close-up of milled double grating. On top of the grating, evidence for drift is visible. The trenches are 120 nm wide with a 160 nm gap in between.

Appendix C

Supplementary information for PECVD growth and device fabrication

C.1 Silicon wafer specifications

The specifications of the crystalline silicon wafers used in the PECVD growth work are given below. All wafers used are from the same batch (received in the same sealed box).

Manufacturer:	IDB Technologies Ltd
Wafer material:	Si
Wafer type:	Prime, SSP
Orientation:	[110]
Diameter:	150 mm
Polished:	front side
Thickness:	640-675 µm
Doping:	n (P)
Resistivity:	1-20 Ωcm

C.2 NCG sample dicing pattern and sample marking

In Subsection 4.3.2 on page 70 it is mentioned that the 150 mm wafer were diced to obtain four $40 \times 40\,\mathrm{mm}^2$ samples. The dicing pattern to achieve this is shown in Figure C.1. The four full samples are obtained from the center of the wafer for highest film uniformity.

The numbers 1-12, visible in Figure C.1, represent the sample numbering. After the wet thermal oxidation but prior to the NCG depositon, identifiers were laser engraved into the back side of the samples. This greatly helps to track samples and avoid possible confusion. The identifiers are in the form `MSxYY_Z` where `YY` is a wafer number and `Z`

is a number from 1 to 12, as shown in Figure C.1. The sample upper left of the center (marked 1) on wafer 14 would thus become `MSx14_1`.

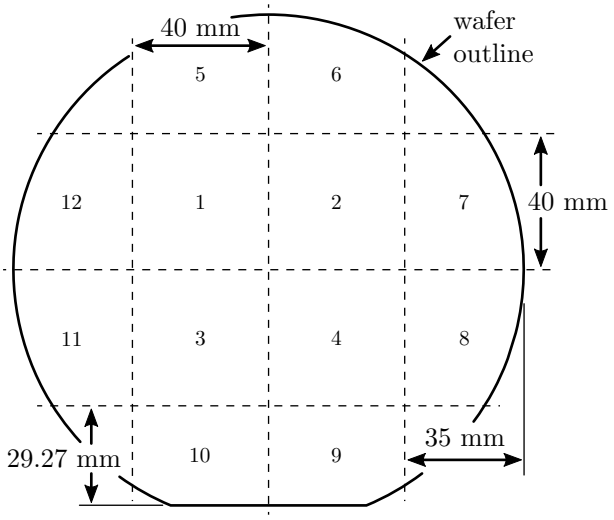


Figure C.1: Dicing pattern according to which 150 mm wafers are diced. Four complete $40 \times 40\,\mathrm{mm}^2$ samples are obtained. The numbers 1 to 12 refer to the identifiers which were laser engraved prior to NCG deposition. The orientation of the numbers is as seen from the back side of the wafer.

C.3 NCG membrane sample dicing pattern

As described in Section 4.4 on page 70, the $40 \times 40\,\mathrm{mm}^2$ samples are diced into 20 pieces with a size of $10 \times 8\,\mathrm{mm}^2$. Only half of the samples contain usable patterns. Figure C.2 contains the used dicing pattern together with a simplified pattern structure.

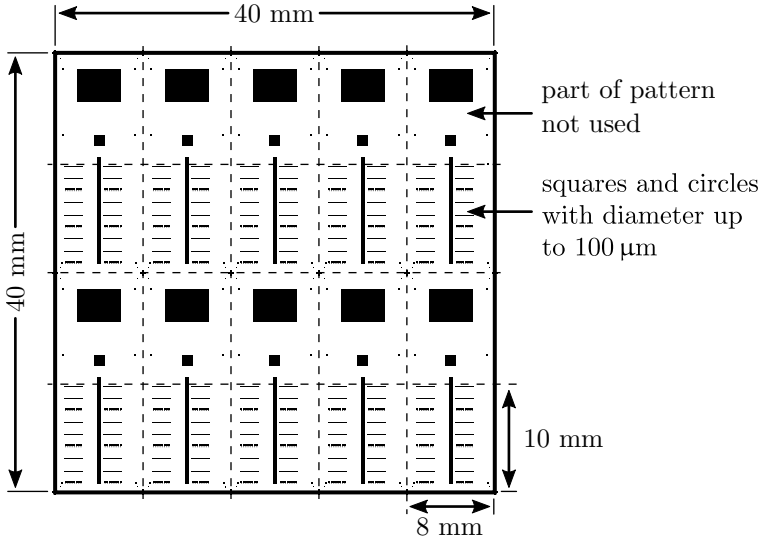


Figure C.2: Dicing pattern used for NCG membrane devices. A simplified pattern structure is shown for reference.

C.4 Lithography mask used for suspended beam and top gated structures

The lithography mask, used for the fabrication of the suspended beam and top gate structures, is shown in Figure C.3. It has total dimensions of $40 \times 40\,\mathrm{mm}^2$ and is located on a $7''$ chrome mask that contains patterns of different contributors.

The mask comprises elements in six columns and seven rows. By aligning different patterns onto the same spot on a sample, a multi-mask process is possible. The patterns labeled Mask 1 and Mask 2 were used for the suspended beam process (see Section 4.5 on page 74), and the respective patterns of Row 5 are shown in greater detail in Figure 4.6 on page 76. For the top gated structures, mentioned in Section 4.6 on page 82, additionally Mask 3 and Mask 4 were used. Detailed illustrations of the patterns from Row 2 are shown in Figure 4.15 on page 76.

The mask comprises additionally alignment marks at the top and bottom, which allow the mask to be shifted left or right by single or double column spacing. The resolution test patterns, located on top and bottom of the vertical beam, are used to assess process resolutions.

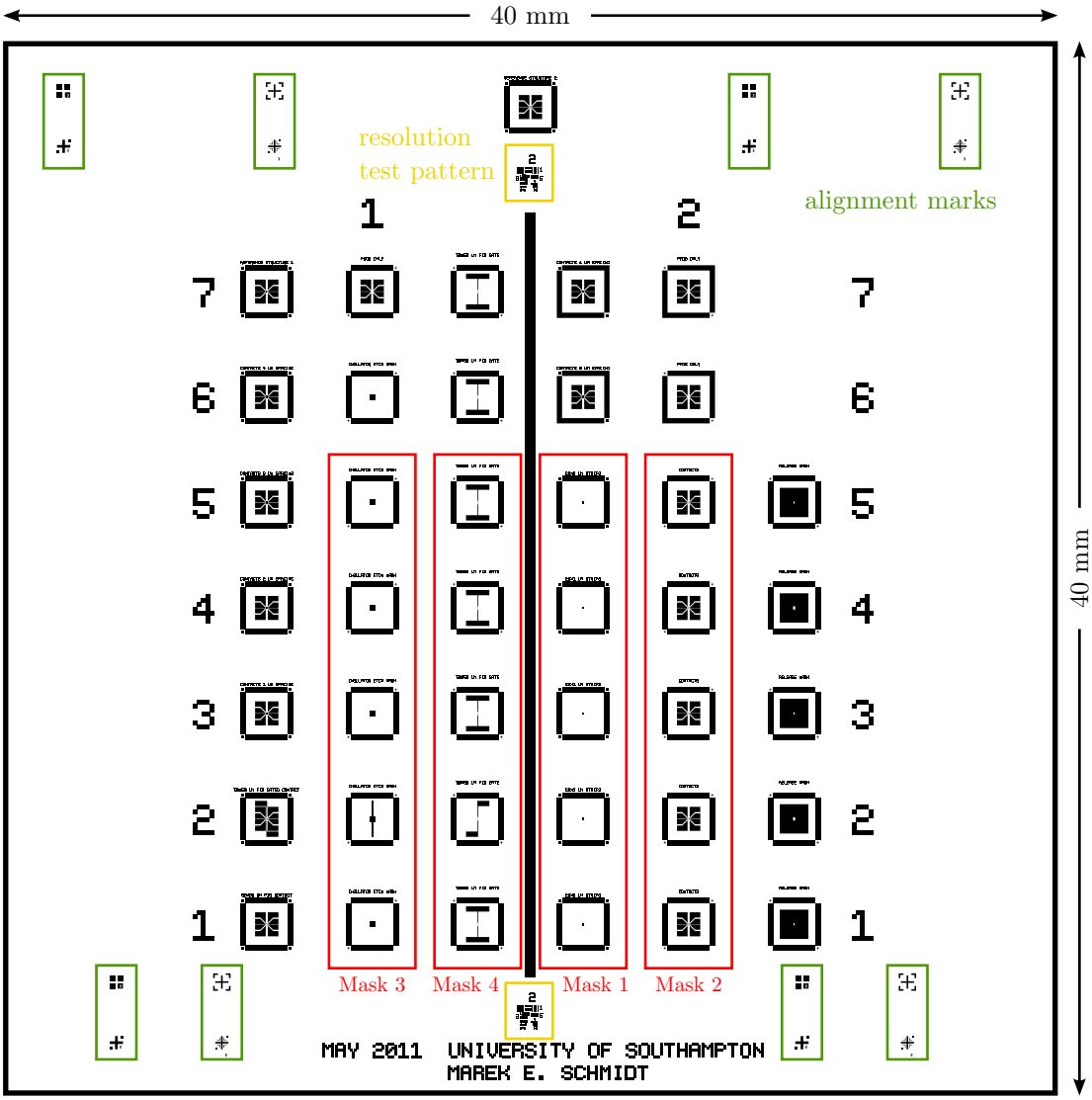


Figure C.3: Full optical chrome mask used for suspended beams (see Section 4.5 on page 74) and top gated devices (see Section 4.6 on page 82). Only the features labeled Mask 1–4, alignment marks and resolution test patterns are used.

C.5 Full-wafer NCG deposition results

C.5.1 Ellipsometry

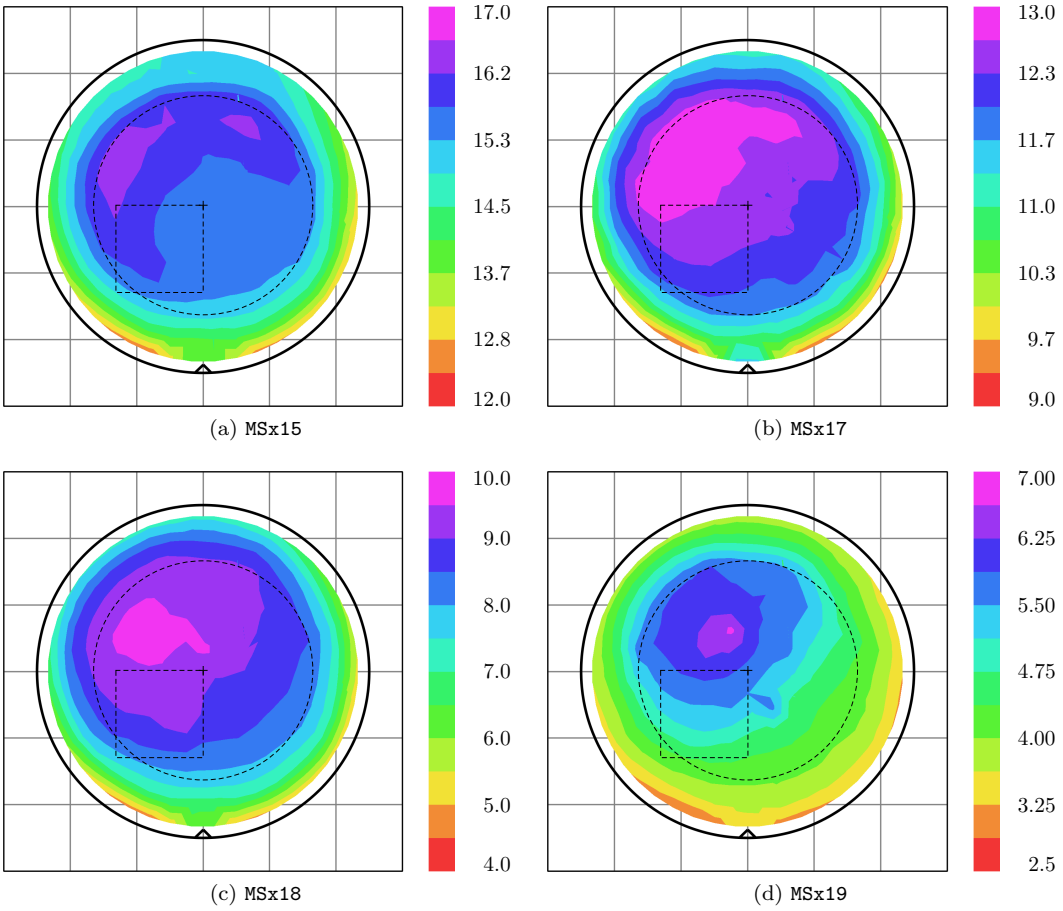
The ellipsometer results for wafers `MSx12`, `MSx13`, `MSx14` and `MSx16` had been discussed in Section 3.3.1 on page 51. The remaining four results for wafers `MSx15`, `MSx17`, `MSx18` and `MSx19` are shown in Figure C.5.

The NCG thickness was probed at 180 locations on the 150 nm wafer in a circular pattern with an offset of 5 mm from the wafer edge. This data was then fitted using the software *CompleteEASE* to a model consisting of three layers with two interfaces. The model and the relevant parameters are shown in Figure C.4.

3	built-in model: `B-Spline`
	model options: `Force E2 positive = ON`
	`Use KK mode = ON`
	fit parameters: `thickness`
	`E Inf`
	`IR Amp`
		NCG

2	built-in model: `SIO2_JAW` fit parameter: `thickness`	thermal oxide
1	built-in model: `Si_JAW`	silicon substrate

Figure C.4: Ellipsometer fitting model for NCG on thermal oxide used in *CompleteEASE*.



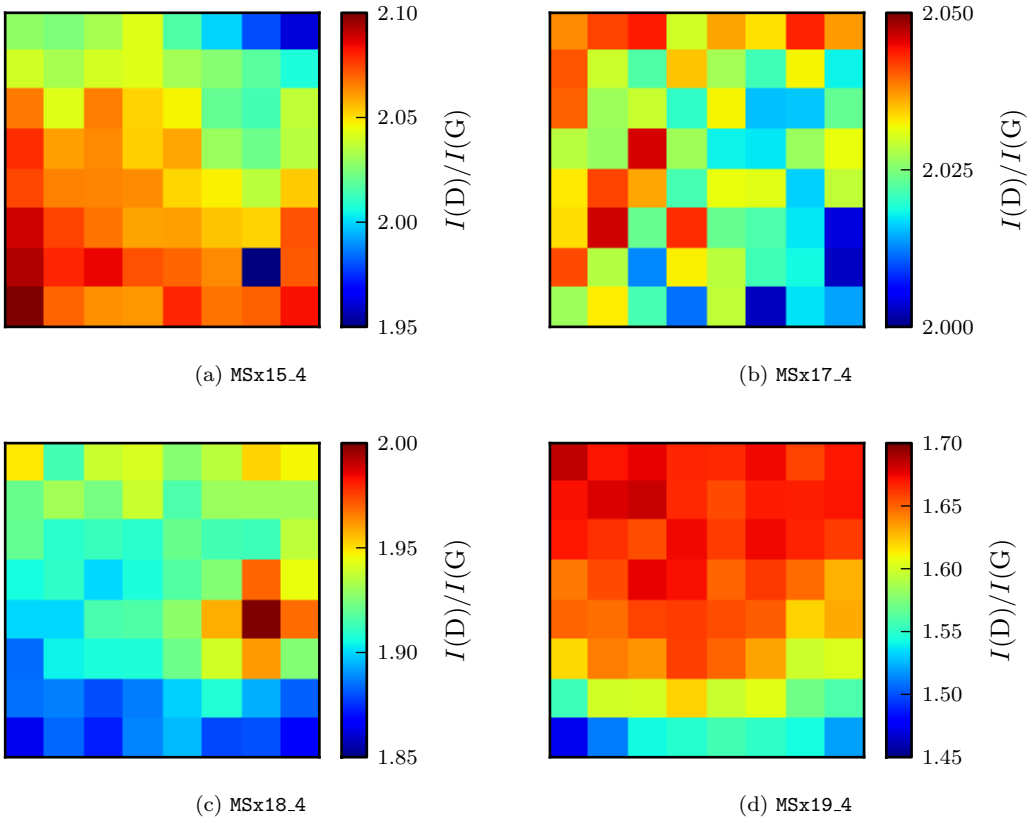
(a) `MSx15` (b) `MSx17`

(c) `MSx18` (d) `MSx19`

Figure C.5: NCG thickness on wafer `MSx15`, `MSx17`, `MSx18` and `MSx19` measured by ellipsometry. NCG thickness scale is in nm. The solid circle indicates the dimensions of the 150 nm wafer. Inner 100 mm size is indicated. Average NCG thickness values and calculated non-uniformities are provided in Table 3.3 on page 53.

C.5.2 Raman mapping results

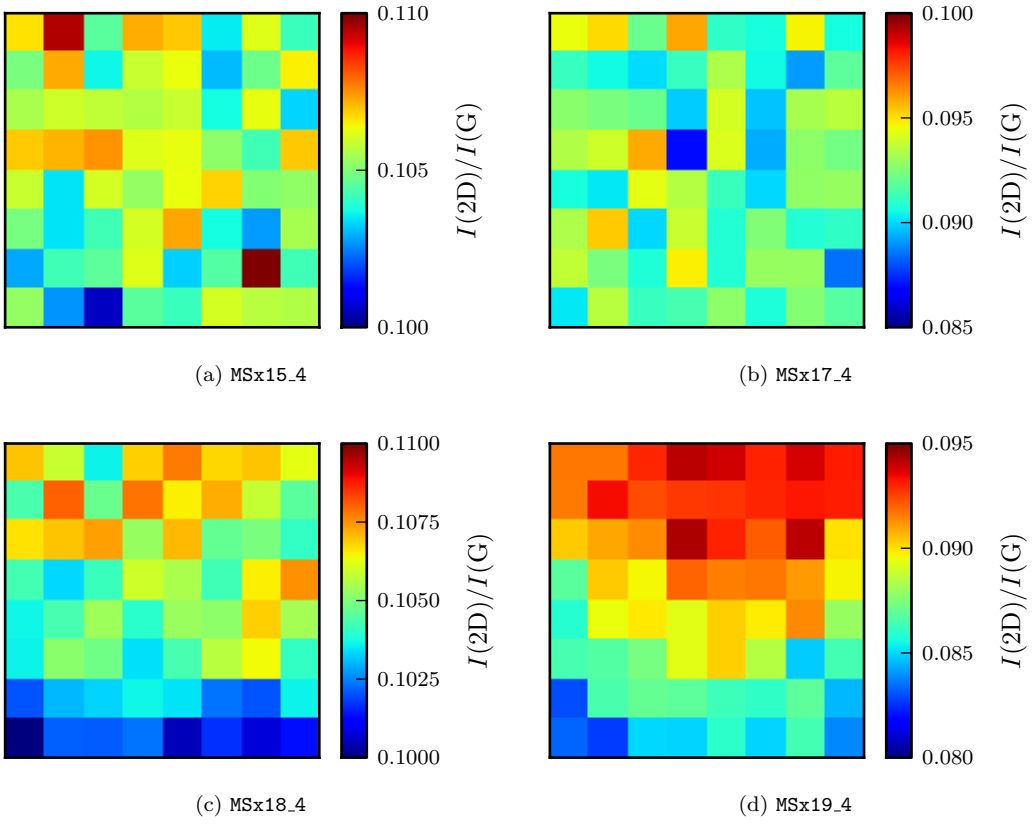
Raman mapping results for four wafers were discussed in Section 3.3.2 on page 54. Remaining results are shown below in Figure C.6 and C.7.



(a) `MSx15_4` (b) `MSx17_4`

(c) `MSx18_4` (d) `MSx19_4`

Figure C.6: Raman $I(\mathrm{D})/I(\mathrm{G})$ mapping results for wafer `MSx15`, `MSx17`, `MSx18` and `MSx19`. For location of the $40 \times 40\,\mathrm{mm}^2$ areas on the 150 mm wafers see Figure 3.9a.



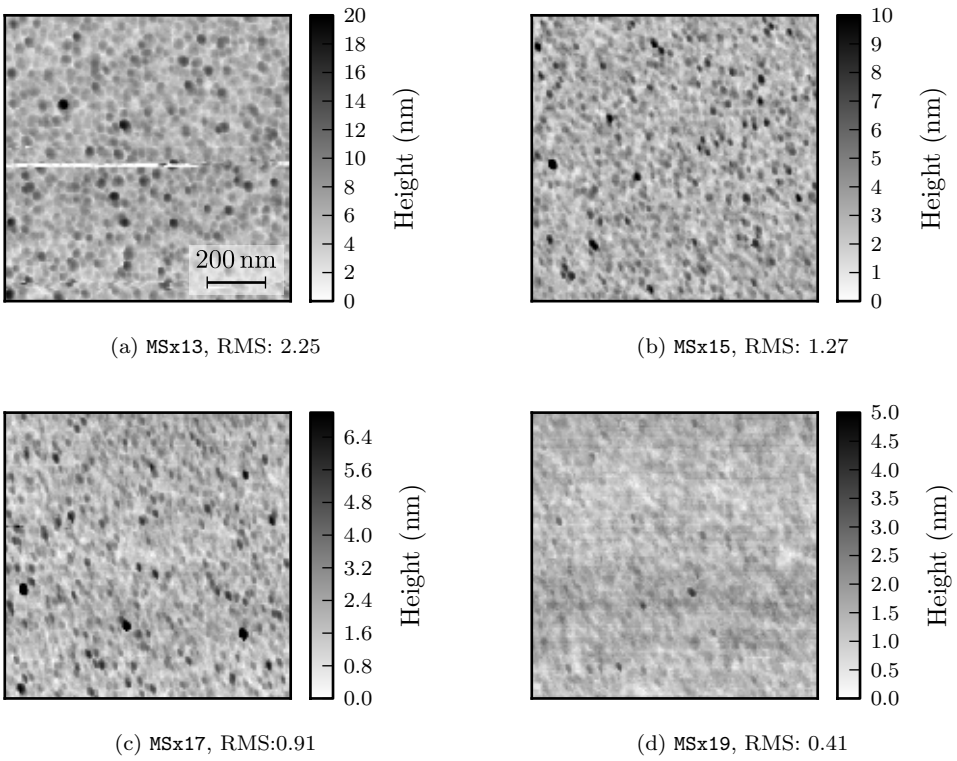
(a) `MSx15_4` (b) `MSx17_4`

(c) `MSx18_4` (d) `MSx19_4`

Figure C.7: Raman $I(2D)/I(G)$ mapping results for wafer `MSx15`, `MSx17`, `MSx18` and `MSx19`. For location of the $40 \times 40\,mm^2$ areas on the 150 mm wafers see Figure 3.9a.

C.5.3 AFM results

Results for four wafers were discussed in Section 3.3.3 on page 57. Remaining results are shown in Figure C.8 below.



(a) `MSx13`, RMS: 2.25

(b) `MSx15`, RMS: 1.27

(c) `MSx17`, RMS:0.91

(d) `MSx19`, RMS: 0.41

Figure C.8: NCG topography for wafers `MSx13`, `MSx15`, `MSx17` and `MSx19` acquired by contact mode AFM close to wafer center. RMS values are given in Table 3.3 on page 53.

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Differences of this version compared to examined version

Location	Correction/modification
p. 8, Figure 2.5	Clarified that Figure 2.5a is own original figure and Figure 2.5b was reproduced from [14].
p. 8, Figure 2.6	Modified copyright notice and reference to meet request by copyright holder.
p. 10, Figure 2.7a	Modified copyright notice to meet request by copyright holder.
p. 10, Figure 2.7b	Modified copyright notice to meet request by copyright holder.
p. 10, Figure 2.7c	Modified copyright notice to meet request by copyright holder.
p. 10, Figure 2.7d	Modified copyright notice to meet request by copyright holder.
p. 12, Figure 2.8	Modified copyright notice to meet request by copyright holder.
p. 13, Figure 2.9d	Modified copyright notice to meet request by copyright holder.
p. 15, Figure 2.11a	Modified copyright notice to meet request by copyright holder.
p. 15, Figure 2.11b	Modified copyright notice to meet request by copyright holder.
p. 18, Figure 2.13	Reference for Figure 2.13a and Figure 2.13b corrected. Now [67], was [6].
p. 19, Figure 2.15	Added correct reference for Figure 2.15. Now [160] (not included previously), was [75].
p. 20, Figure 2.16c	Modified copyright notice to meet request by copyright holder.
p. 20, Figure 2.16d	Added correct reference for Figure 2.16d. Now [161] (not included previously), was [79].
p. 21, Figure 2.17	Clarified origin of Figure 2.17a and b.
p. 21, Figure 2.17c and 2.17d	Modified copyright notice and reference to meet request by copyright holder.
p. 22, Figure 2.18	Modified copyright notice to meet request by copyright holder.
p. 25, Figure 2.20	Modified copyright notice to meet request by copyright holder.

p. 27, Figure 2.22	Replaced figure and citation, modified copyright notice to meet request by copyright holder. Figure previously taken from [95] which is not peer-reviewed. Now [96].
p. 27, Figure 2.23b	Modified copyright notice to meet request by copyright holder.
p. 30, Figure 2.27	Modified copyright notice to meet request by copyright holder.
p. 31, Figure 2.29	Modified copyright notice to meet request by copyright holder.
p. 36, Figure 2.32a	Modified copyright notice to meet request by copyright holder.
Bibliography entry for [8]	Added missing Ö to co-author name.
Bibliography entry for [52]	Fixed typo: raman → Raman.
Bibliography entry for [56]	Fixed date of publication. Was December 2010.
Bibliography entry for [58]	Added DOI link to meet request by copyright holder of Figure 2.17c and 2.17d.
Bibliography entry for [62]	Added URL.
Bibliography entry for [78]	Fixed publication title.
Bibliography entry for [102]	Added dash.
Bibliography entry for [123]	Added DOI link to meet request by copyright holder of Figure 2.32c.