Multi-Voltage Aware Resistive Open Fault Model

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***Abstract*—Resistive open faults (ROFs) represent common interconnect manufacturing defects in VLSI designs and their behavior exhibits major dependencies on the supply voltage and test patterns. The widespread utilization of multiple supply voltages in contemporary VLSI designs poses a critical concern as to whether conventional models for resistive opens would still be effective. This is because conventional models do not explicitly model the V_{DD} effect on fault behavior and detectability. Based on experimental analysis of ROFs in multi-V_{DD} environment, we propose a voltage-aware model which divides the full range of open resistances (RO) into continuous *behavioral intervals* and three *detectability ranges*. The division of the behavior into intervals is based on monitoring the behavior change versus voltage across the resistance continuum, whereas the detectability ranges are based on finding minimum resistance for small and gross delay faults. It is highlighted that the detectable open resistance range is having a decreased trend with new technologies. Additionally it is shown that the observability of the unique increasing delay behavior with V_{DD} for resistive open is reduced in new technologies. This poses reliability concerns and motivates the use of small delay testing for new technologies.**

***Index Terms*—Voltage Aware Modeling, Resistive Open Faults, Small Delay Faults, Open Resistance Intervals**

I. Introduction

RESISTIVE opens are common manufacturing failures that induce delay faults of different degrees and cause potential reliability risks due to their partial break-like nature [1], [2], [3], [4]. Therefore screening for such faults is important to reduce test escapes, infant mortality failures and reject rates. To optimize the screening and detection of resistive open faults (ROFs), testing methods employing multiple supply voltages have been investigated and proved to give good results [5], [6], [7], [8]. With the emergence of low power designs which utilize multiple supply voltage levels [9], multi-V_{DD}-based methods are ow of critical concern for effective testing and diagnosis [10], [11], [12], [13], [14].

However, the behavior and detectability of resistive open faults depend on the electrical characteristics of driving and driven gates and how the fault is sensitized (i.e. test patterns), as well as the supply voltage [15], [16], [17], [13]. Given such dependencies, characterization and prediction of the behavior and thus the detectability with respect to voltage becomes difficult. Previous models [18], [19], [20], [21], [22] for resistive open faults did not explicitly account for V_{DD}. Therefore for efficient multi-V_{DD} fault detection and diagnosis, a voltage aware model which considers these dependencies has to be developed.

Therefore, the aim of this paper is to present a parametric, voltage-aware resistive open fault model, including both the behavior and detection information. Additionally we explain a methodology to determine the various behavioral and detectability parameters of the model. That is, for every fault location and test pattern, the methodology identifies the resistance detection ranges for small and gross delay faults. We identify a small number of resistance intervals that have similar delay behavior with respect to V_{DD}. The model assumes a limited number of V_{DD} values. The behavioral information revealed by this model assists in defining the right test pattern-V_{DD} pair that can be used to excite distinguishable faulty behavior. The detection information helps to identify which test pattern-V_{DD} pair has the best fault coverage (i.e. the greatest resistive range coverage). Hence, this model improves the test pattern generation and fault detection algorithms.

A preliminary version of this work has been accepted at ETS12. The work presented in this paper brings the following extensions: Preliminary experimental verifications on benchmark circuits, computation of the critical resistance for behavior intervals, and algorithm for identifying the behavior parameters for each fault and test pattern. The organization of the paper is as follows: Background and prior work are given in Section II. In Section III, the motivation for developing the voltage-aware model based on delay-voltage dependencies of resistive opens is explained. An illustration of the model followed by a methodology used to identify the behavior intervals and detection ranges is discussed in Section IV. Experimental results on benchmark circuits using different technology models are discussed and analyzed in Section VI. Concluding remarks are given in Section VII.

II. Background

A resistive open fault is a parametric model representing partial-open failures, in which the size of the open (break) is represented by a resistance. In previous work, the resistances of opens (RO) have been experimentally characterized for an aluminum process and it was reported that for resistive open faults, RO can vary in the range of a Ohms to Megohms [2]. The distribution of resistance values can be used statistically to compute the fault coverage [23]. According to the resistance of the partial-open fault (RO) and the relative length of the sensitized faulty path to the longest path, a ROF can cause extra delays over several orders of magnitude. A *gross delay fault* is defined to have a cumulative propagation delay exceeding the longest path delay, other faults are is defined as *small delay faults* [3]. Gross delay faults are detected by at-speed transition delay fault testing, whereas small delay faults

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are tested using faster-than-at-speed testing. Generally delay faults due to ROF show some sensitivity to test patterns and V_{DD}, as will be discussed later in this section.

Kruseman and Heiligers, [16], conducted an inductive fault analysis for resistive opens on several standard cells using a wide range of technologies. They highlighted different voltage-delay dependencies with different fault locations and test patterns. In that work, the additional delay caused by resistive open faults was characterized and several delay behaviors were identified. An "increasing" delay pattern corresponds to an increase in delay for reduced voltage; a "constant" delay pattern means an almost constant delay for high voltages, but an increase in delay with smaller voltages; and a "constant inverse" delay means a decrease in delay for reduced voltage.

Arumi *et al.* in [24] assessed the behavior (delay) of ROFs at a single V_{DD} using an experimental chip and reported that high resistance values and low resistance values have different timing responses and have to be modeled differently. This is attributed to the ON resistance of MOS transistors driving a faulty node as well as the capacitance of the driven gates [24]. This shows that the range of open resistances can exhibit different behaviors with V_{DD} according to the relative value of RO with respect to the transistor ON resistance (R_{ON}).

Other factors affecting the behavior include: the location of a ROF within the interconnect [24]; the threshold voltage [7]; capacitance of driven gates [25]; and the technology used [17]. Each of the named factors affects the delay differently, therefore the delay-voltage dependency is likely to vary across fault locations and so questions whether assuming a fixed behavior for a fault is correct.

Li *et al.*, [15], demonstrated that resistive opens in wire delay-dominant (WDD) paths are better detected at the highest V_{DD}. On the other hand, for gate delay dominant (GDD) paths, a low V_{DD} gives better detection. It may be noted that WDD paths have a high wire resistance, while GDD paths have a small wire resistance. This implies that the delay-voltage dependency can be different for different RO values.

It can be concluded that the delay behavior due to ROF differs with V_{DD} and also depends on the fault location and the applied test pattern, as well as the actual resistance. On the other hand, the intrinsic delay of a fault free path decreases with V_{DD} and its magnitude depends on the length of the path [26], [9]. Consequently this makes prediction of the observable behavior of a faulty path difficult. This in turn could cause different fault detectability at different V_{DD} values. Therefore, two hypotheses can be proposed. First, if the behavior of a resistive open fault is a function of the resistance, then the ROF behavior can be modeled by dividing the range of open resistance values (RO) into intervals, each having its own observable fault behavior. Second, if the detectable resistance range varies with the supply voltage, the ROF detectability can be modeled by identifying the minimum detectable resistance value at each V_{DD}. In the next section, these hypotheses are tested using a set of benchmark circuits.

III. Prior Work

Recently, we investigated the delay behavior of paths affected by ROFs with respect to V_{DD} [14]. The experimental results showed that up to 3 resistance ranges per fault location and test pattern can exhibit different faulty behaviors. This is because the resistance of the fault determines the strength of the faulty behavior. Since the transistor delay and fault delay have different behaviors, the observable path delay depends on the relative strength of the fault to the transistor delay. This results in different observable behaviors with different ranges of the fault resistance. Additionally, we investigated, [13], the ROF detectability with respect to V_{DD} in multiple V_{DD} environments for different fault locations and test patterns. The experimental results showed that the detectability with respect to V_{DD} varies across test patterns, designs and technologies. This means that each ROF could have a different detectable resistance range coverage with V_{DD} and this implies a difference in the resistance detection threshold at each V_{DD}.

In the next section, the experimental setup and results from [14] and [13] will be discussed, followed by an experiment on an inverter chain design.

A. Benchmark Designs Experiments

Experiments on benchmark circuits [27], [28], [29] were performed to determine the identifiable number of behaviors per fault for each circuit. Additionally, the average detectable resistance range per V_{DD} for a large number of fault locations was computed for each circuit. Spice-level simulations were used. The delays of faulty paths were calculated at the different V_{DD} values. If two ROFs at the same V_{DD} had the largest delay value, then they were grouped. To verify the detectability at different V_{DD}s the detectable resistance ranges for all faults and test patterns were computed at each V_{DD}.

The experiments were conducted on different transistor technology models, namely a commercial 130nm technology, and the bulk 65nm, the 32nm and 16nm Hi-K metal gate strained Si technologies from the Berkeley Predictive Technology Models (BPTM) [30]. Three V_{DD} values were used in each experiment: a nominal, high V_{DD} value denoted by V_{DDH}, a middle V_{DD} value chosen to be in between the high and the low V_{DD}, denoted by V_{DDM}, and low V_{DD} which is twice the threshold voltage and denoted by V_{DDL}. Table I shows the V_{DD} values used in the simulation for each technology.

TABLE I
Technology models and V_{DD}/V_t settings used in simulation, High V_t and Standard V_t are from the technology models

Tech	V_{DD}			Standard V_t		High V_t	
	H	M	L	$\|Vtn\|$	$\|Vtp\|$	$\|Vtn\|$	$\|Vtp\|$
130nm	1.20	1.00	0.80	0.28	0.27	0.39	0.41
65nm	1.00	0.85	0.70	0.42	0.37	-	-
32nm	0.90	0.80	0.70	0.51	0.37	0.63	0.58
16nm	0.70	0.65	0.59	0.48	0.43	0.68	0.69

A list of faults is generated from the output nodes of each standard cell in each design. Discrete samples are chosen for RO so that they approximately represent a typical logarithmic distribution of open resistances [2]. In this work, eight to ten

TABLE II
RESISTANCE INTERVALS ON DIFFERENT BENCHMARK CIRCUITS

Ckt	Max at			$\frac{\#Intrv}{ROF}$
	V_L (%)	V_M (%)	V_H (%)	
c17	50.0%	0.0%	50.0%	**2.00**
s27	66.0%	2.1%	31.9%	**1.96**
b01	57.0%	1.0%	42.0%	**2.33**
c432	70.5%	0.0%	29.5%	**1.97**
c499	52.2%	0.0%	47.8%	**1.92**
c880	51.5%	0.0%	48.5%	**1.94**
c1355	52.7%	0.2%	47.1%	**1.90**
c1908	52.7%	0.0%	47.3%	**1.90**

values for open resistances were typically used and similar results were observed for all cases. Transition test patterns were obtained by a conventional stuck-at fault based Automatic Test Pattern Generator (ATPG) [31]. During the pattern generation process, each fault site is translated into stuck-at-0 and stuck-at-1 inputs for the ATPG. For detecting gross delay faults, the longest path delay at each V_{DD} is used as the test clock period (TCP), whereas for detecting small delay faults the 50^{th} path delay percentile is used instead. For the latter case, any test patterns that sensitize paths longer than the 50^{th} path delay percentile are not considered and therefore, the number of detectable faults will be reduced.

Table II reports the percentage of intervals identified at V_{DDH}, V_{DDM} and V_{DDL}, and the average intervals per ROF observed. Despite the fact that all resistive opens are injected at inter-gates locations and sensitized using the same falling transitions, Table II shows that distinct ROF intervals can be observed. On average all ROFs exhibit two to three behaviors per fault location as highlighted in the last column. This can be attributed to the contribution of delays due to faults compared to the delays contributed by the path. That is, the delays due to opens are a function of the fault size (open resistance). For small values of open resistance (RO), the fault contribution in the total path delay is low, therefore resulting in the dominance of intrinsic delay behavior of the fault free path. However, when the open resistance becomes large the faulty path delay behavior gets dominated by the behavior of opens. For intermediate values of RO the behavior might exhibit more complex behaviors which would increase the types of behavior to more than two per fault.

On the other hand, Table III reports the detectability results versus V_{DD} in different circuits (column 1) and different number of faults (columns 2 and 6) for the detection of gross delay faults (columns 3, 4 and 5) and small delay faults (columns 7, 8 and 9). The metric used in evaluating the detectability is the resistive open coverage (ROC). Table III shows that the average detection coverage generally varies with V_{DD}. Additionally, it shows that the detectable resistance range for small delay faults is more than gross delay faults. This is because the test clock period is shorter in testing small delay faults which enables detection of more subtle delays and therefore resistance ranges.

B. Inverter Chain Design Experiment

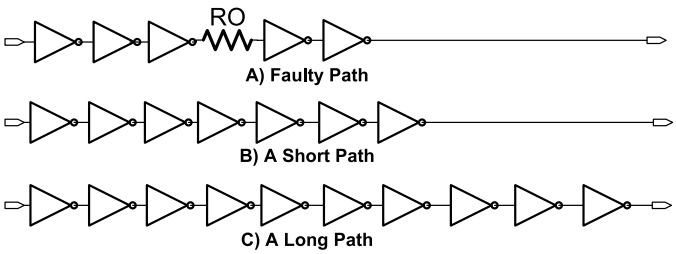


Fig. 1. Inverter Chain Example

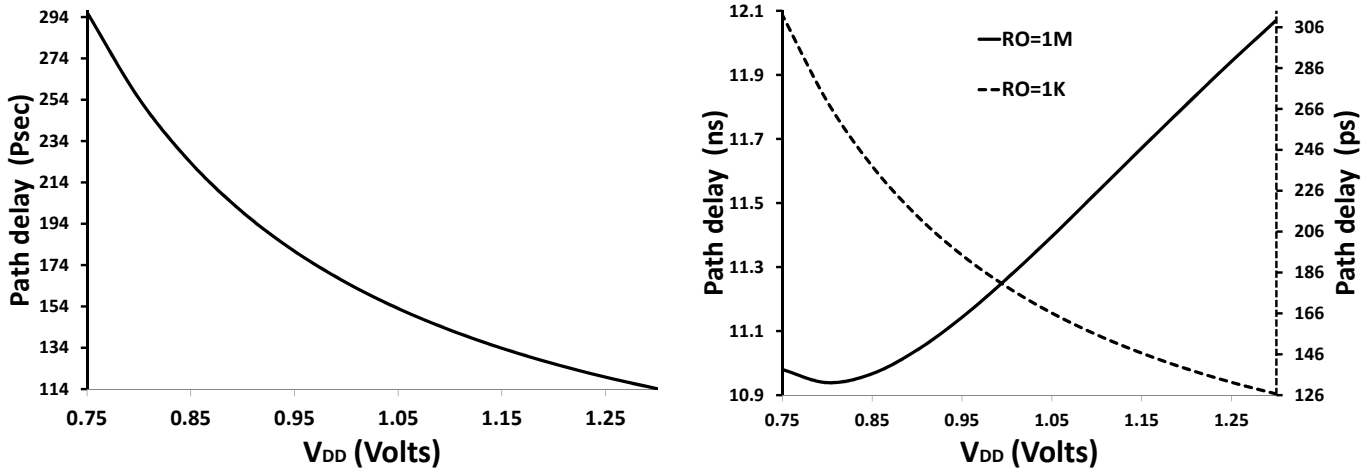
The aim of this experiment is to visualize the various parameters required to fully represent the detectability and behavior of a ROF with respect to V_{DD}. In this experiment, three inverter chains are considered, as shown in Fig. 1. The circuit has three paths, a faulty path where the fault resides, a short path and a long path. This is to enable simple observation of the behavior and to evaluate the fault detectability in at-speed testing and faster than at-speed testing methods. In order to examine the faulty behavior, two values of open resistances (denoted as RO in Fig. 1) are injected: $1k\Omega$ and $1M\Omega$. These values are selected to observe faulty behavior for small and large open resistances. Two consecutive vectors are applied to set the faulty node to 1 and 0 respectively causing a falling transition at the driving node of fault. The delays of the fault-free and faulty path are measured and shown in Fig. 2a and Fig. 2b, respectively.

Fig. 2b shows that for $RO = 1M\Omega$, the propagation delay increases as the supply voltage increases, whereas $RO = 1k\Omega$ produces an inverse relationship. To explain these differences, recall that the observable behavior of the faulty path comprises two components: the fault-free path behavior and the additional behavior of the open resistance. The delay of the fault-free circuit decreases with increasing voltage as in Fig. 2a. On the other hand, the delay due to the resistive open increases with voltage as described in [16]. However, the delay strength (magnitude) is low for $1k\Omega$ and high for $1M\Omega$. This consequently results in different total delays with voltage for the faulty path. It would be expected that the behavior of a range of resistance values around $1k\Omega$ will be similar to that at $1k\Omega$. We would expect a change in behavior when the fault effect has an equal delay strength to the that of the fault-free path. Then the behavior for another range of resistances would be similar to that at $1M\Omega$. The behavior identified for the full range of ROF using large number of resistances is illustrated in Fig. 3.

Fig. 3 shows that the resistance intervals $[50\Omega, 64k\Omega]$ and $[345\Omega, 10M\Omega]$ have decreasing and increasing delay behaviors, respectively. Additionally, the resistance interval $[97.6\Omega, 226.4k\Omega]$ has a "mid-bump" behavior, marked as "others" in the figure. In this "mid-bump" range, neither the intrinsic fault behavior nor the intrinsic fault-free path behavior dominates. The size of such intervals is expected to vary according to the path length where the fault resides. From this experiment, a key observation is that the behavior for a particular fault location and test pattern is dependent on

TABLE III
VERIFICATION OF THE DETECTABILITY VS V_{DD} ON DIFFERENT BENCHMARK CIRCUITS

Ckt	Gross Delay Faults				Small Delay Faults			
	#ROF	V_{DDL}	V_{DDM}	V_{DDH}	#ROF	V_{DDL}	V_{DDM}	V_{DDH}
c17	**9**	45.2%	47.3%	47.6%	**4**	58.7%	58.7%	58.7%
s27	**14**	43.8%	45.2%	45.8%	**6**	52.4%	56.6%	56.6%
b01	**40**	42.9%	44.6%	45.5%	**19**	50.1%	50.9%	51.3%
c432	**184**	29.4%	31.1%	36.5%	**92**	48.5%	51.0%	54.6%
c499	**124**	36.6%	39.4%	39.4%	**60**	41.8%	41.8%	66.7%
c880	**343**	31.4%	37.6%	39.8%	**172**	43.0%	44.1%	45.0%
c1355	**291**	33.7%	34.0%	39.5%	**143**	28.8%	40.7%	40.8%
c1908	**804**	26.0%	30.9%	37.6%	**401**	44.5%	45.6%	48.5%



(a) (b)

Fig. 2. Propagation delay for inverter design using failing transition pattern, (a) Fault free case, (b) Faulty case, dash line (RO=1kΩ) and solid line (RO=1MΩ)

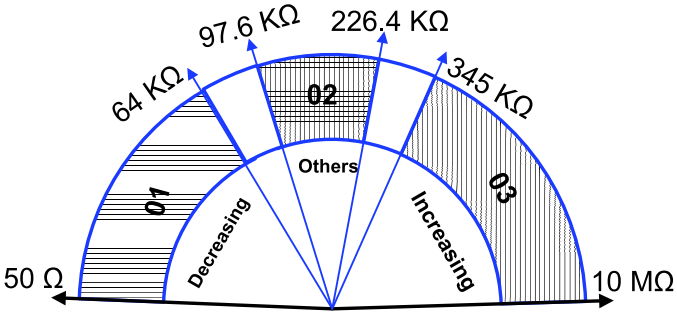
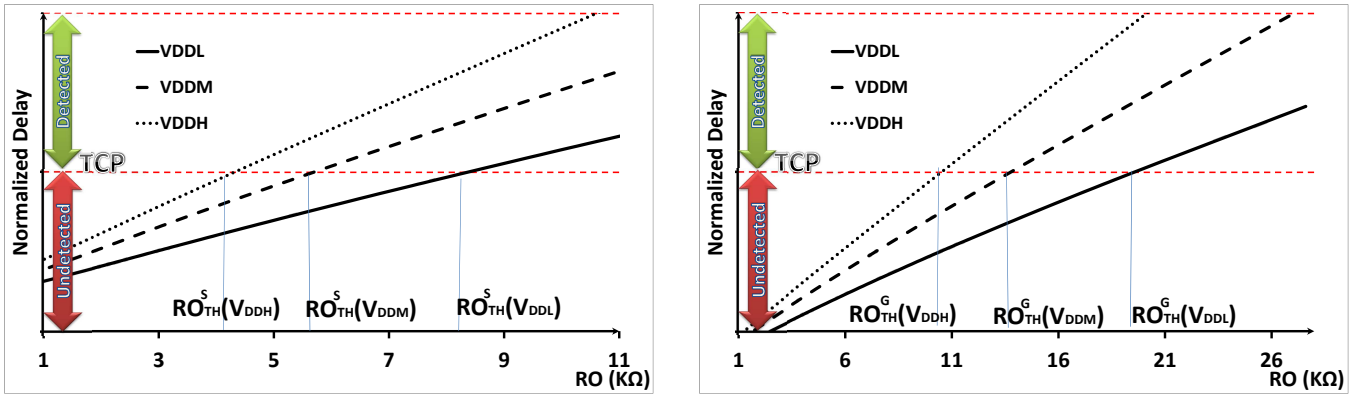


Fig. 3. Identified Behaviors

the open resistance value itself, i.e. it is interval dependent. This effectively allows the full domain of open resistances in sub-intervals which have similar delay behavior to be treated as a function of V_{DD}. The intermediate resistance value at which the delay-V_{DD} behavior changes is defined as the critical resistance (RO_{cr}). For two consecutive intervals i and j showing distinct behavior, the critical resistance is denoted as RO_{cr}^{i-j}.

The fault detectability was evaluated at three V_{DD} values (V_{DDL}=0.8V, V_{DDM}=1.0V and V_{DDH}=1.2V). The V_{DD} values were selected to be in the range of $2 \times V_t$ to the nominal V_{DD}. Transition test patterns causing falling transitions at the faulty node were applied. The selection of the specified values for V_{DD} along with the falling transition test pattern allows the fault to manifest inverse behavior compared to the fault free path [16]. To emulate detectability in at-speed and faster-than-at-speed testing scenarios, the captured delay values for a large number of resistance values at each V_{DD} are normalized to the delays of the long and short paths respectively. The detectability of the ROFs is shown in Fig. 4. The figures show the normalized faulty delay on the vertical axis and the corresponding RO values on the horizontal axis for three V_{DD} values. The behavior for small delay faults is shown in Fig. 4a, while that for gross delay faults is shown in Fig. 4b. For both cases, the normalized delay fault is detected when it exceeds the test clock period (TCP). The resistance at which the propagated delay is equal to the TCP is called the open resistance detection threshold (RO_{TH}). From Fig. 4a and Fig. 4b, it can be shown that detection threshold RO_{TH} is different for the three V_{DD} values for both small and gross delay fault detection. That is, the detection thresholds at V_{DDL}, V_{DDM} and V_{DDH} are $RO_{TH}^{S}(V_{DDL})$, $RO_{TH}^{S}(V_{DDM})$ and $RO_{TH}^{S}(V_{DDH})$, respectively, for small delay faults and



(a) (b)

Fig. 4. Resistance Detection Thresholds Using Falling Transition Pattern Considering (a) Small Delay Fault (b) Gross Delay Fault

$RO^G_{TH}(V_{DDL})$, $RO^G_{TH}(V_{DDM})$ and $RO^G_{TH}(V_{DDH})$, respectively, for gross delay faults. A key observation is that the detectable resistance range can vary with the voltage used in testing. This knowledge helps in selection of optimum test patterns and V_{DD} especially for dynamic voltage scaling-aware designs. For example, for the delay fault scenarios in Fig. 4a and Fig. 4b, V_{DDH} should be selected for test, since the detection threshold (RO_{TH}) is minimum and thus maximum resistance range can be detected.

The rest of the paper describes the various parameters of the proposed model and how they can be obtained.

IV. The Proposed Voltage Aware Model

In previous section, it is shown that the full resistance continuum of resistive open faults can potentially exhibit various behaviors and detection thresholds in voltage aware environment. In this section, by exploiting multi-V_{DD} operating environment, a model representing the behavior and detectability of ROF per test pattern is explained. That is, the full resistance continuum of ROF is divided into intervals and ranges representing distinct delay behaviors and detection thresholds. Though, the concept of dividing the whole resistance continuum into resistance intervals is not new as being practised in [11], [21]. However, in this work the intervalization concept relies on the combined observation of the delay behavior and detectability of the open resistance as far as the supply voltage is concerned. That is, the resistance continuum can be divided to N behavior intervals and three detectability ranges.

As far as the behavior is concerned, it is observed that all ROF behaviors reported in [16], can be represented by one of the four behaviors shown in Fig. 5. That is, considering three V_{DD} values, the delay behavior Bhv can only be a) maximum at V_{DDL} and minimum V_{DDH} resulting in "dec" behavior, or b) maximum at V_{DDH} and minimum V_{DDL} resulting in "inc" behavior, or c) minimum at V_{DDM} resulting in "mid-bump" behavior, or d) maximum at V_{DDM} resulting in "mid-bump-inv" behavior. Therefore, it can be generally found for the full resistance domain $[RO_{min}, RO_{Full}]$ of ROF sensitized using a test pattern TP, different resistance intervals, $i \in \{01, 02, 03, ..., N\}$, exhibiting behaviors $\{Bhv\,(01)\,, Bhv\,(02)\,, ..., Bhv\,(N)\}$, whereby, $Bhv(i-1) \neq Bhv(i), \forall i \in (02, 03, ..., N)$. That is, the model represent those behavior intervals by the critical resistance RO_{cr}^{i-1-i} separating any consecutive intervals $i-1$ and i, whereby $N \geq i > 1$.

As far as detectability is concerned, the resistance continuum can exhibit three detectability ranges (i.e. gross delay faults, small delay faults and undetectable delay faults). The proposed model represents those detectability ranges by the resistance detection threshold for gross delay faults (considering at-speed testing) and small delay faults (considering faster-than-at-speed testing). The minimum detected resistance when targeting gross delay faults is referred as RO^G_{TH}, whereas, for small delay faults is referred as RO^S_{TH}. Since each V_{DD} has its own RO^G_{TH} and RO^S_{TH}, the $RO^G_{TH}(V_{DD})$ and $RO^S_{TH}(V_{DD})$ notations are used in the model. That is, the gross delay fault range is $RO^G_{TH}(V_{DD}) > RO \leq RO_{Full}$, the detectable small delay fault range is $RO^S_{TH}(V_{DD}) > RO \leq RO^G_{TH}(V_{DD})$ and the undetectable range is $RO_{min} > RO \leq RO^S_{TH}(V_{DD})$.

A general graphical illustration for the proposed model is shown in Fig. 6. In this model, the full range of ROF resistance domain is depicted on the circular axis ranging from RO_{min} to RO_{Full}. On the circular axis of RO, different continuous RO intervals are depicted on the circular segments (01 ,02 , ..., N) having behaviors (Bhv(01), Bhv(02), ..., Bhv(N)) respectively. As example, the first identified resistance interval is shown at the most left circular section and denoted by 01. This 01 interval covers the resistances all the way from RO_{min} up to RO_{cr}^{01-02} which has a behavior $Bhv(01) \in \{dec, inc, mid-bump, mid-bump-inv\}$. RO_{cr}^{01-02} is the critical RO value at which the delay behavior observability changes. For detection use, the model also identifies the RO^S_{TH} and RO^G_{TH} resistances at each V_{DD}, indicating the detection regions for small and gross delay faults assuming faster than at-speed and at-speed testing scenarios respectively.

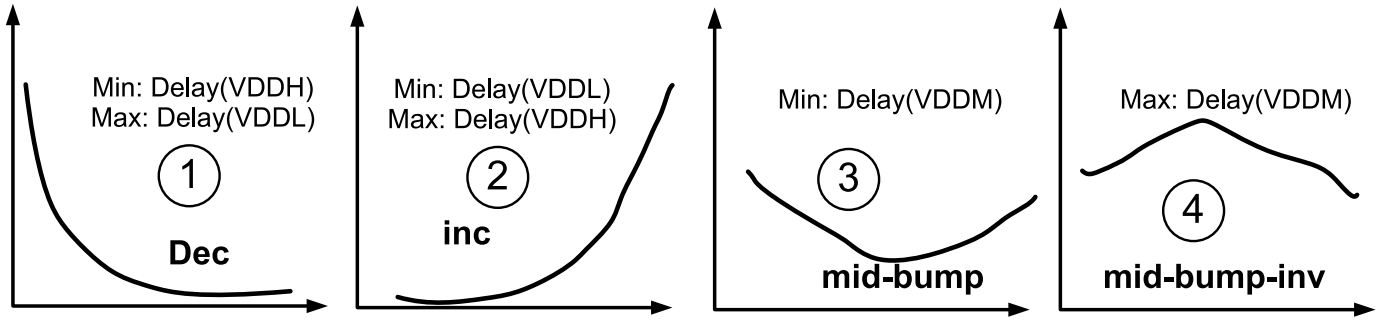


Fig. 5. behaviors Considered in the Proposed Voltage Aware Resistive Open Fault Model

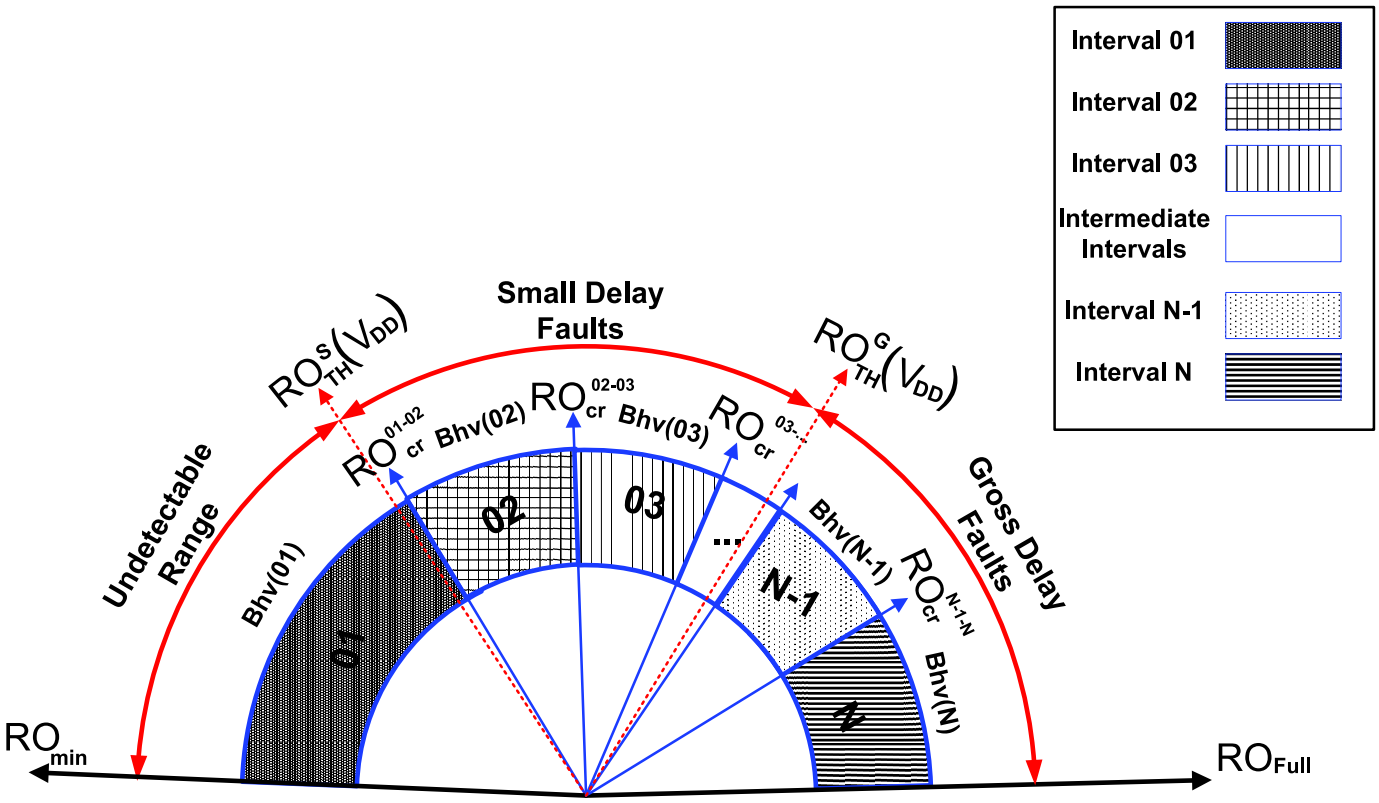


Fig. 6. Graphical Illustration of the Proposed Voltage Aware Resistive Open Fault Model

V. Behavior Intervals and Detection Ranges Identification Method

It is previously shown that, the behavior and detection of a ROF sensitized by a test pattern (TP), can be modelled by identifying the behaviors of each interval ($Bhv(i)$), the critical resistances separating the intervals (RO_{cr}^{i-i+1}), and the detection thresholds of small and gross delay faults ($RO_{TH}^{S}(V_{DD})$ and $RO_{TH}^{G}(V_{DD})$ respectively). The challenge though is that, determining the exact values of these parameters would excessively require time demanding circuit level simulations, thus prohibitively incurring high costs especially for large designs. Therefore, we proposed parameter identification method based on parametric SPECTRE simulations combined by SPLINE cubic interpolation to achieve reasonable trade-offs between accuracy and simulation time. The procedure used to identify the model parameters for every fault site/test pattern is described in Fig. 7 and Fig. 8. The proposed method identifies for a synthesized circuit netlist, operating at the V_{DD} settings (VDDs), the model parameters ($Bhv(i)$, RO_{cr}^{i-i+1} ($\forall i \in (1..N-1)$), $RO_{TH}^{S}(V_{DD})$ and $RO_{TH}^{G}(V_{DD})$) for each ROF and corresponding test patterns (TPs^{G} and TPs^{S}). The proposed method is broken in two main parts: a prior SPECTRE simulation part shown in Fig. 7 and the parameter identification part in Fig. 8. The aim of the SPECTRE simulation part is to obtain the path delay information for all faults/test patterns. Whereas the aim of the second part is to evaluate the model parameters.

As for the algorithm inputs in Fig. 7, the $ROFs$ fault list can be generated exhaustively for comprehensive fault coverage or selectively using layout-aware methodology for realistic fault locations. If the $Netlist$ corresponds to a multi-voltage design, its operating V_{DD} levels can be passed as the $VDDs$ to be used in this algorithm. However, when considering a multi-voltage design with large number of V_{DD} levels (i.e.

Input: Netlist, VDDs, ROFs, TPs^G, TPs^S
Output: PD(VDDs, ROFs, $TPs^G||TPs^S$,RO)

1: Select discrete values for ROs
2: //SPECTRE simulation()
3: **for all** $ROF \in ROFs$ **do**
4: **for all** $TP \in (TPs^G(ROF) \cup TPs^S(ROF))$ **do**
5: **for all** $VDD \in VDDs$ **do**
6: **for all** $RO \in (0 \cup ROs)$ **do**
7: SPECTREsimulate(Netlist,ROF,TP,VDD,RO)
8: Capture $PD(ROF)(TP)(VDD)(RO)$
9: **end for**
10: **if** $TP \in TPs^G$ **then**
11: $PDs^G(VDD) \leftarrow PD(ROF)(TP)(VDD)(0)$
12: **end if**
13: **if** $TP \in TPs^S$ **then**
14: $PDs^S(VDD) \leftarrow PD(ROF)(TP)(VDD)(0)$
15: **end if**
16: **end for**
17: **end for**
18: **end for**
19: **for all** $VDD \in VDDs$ **do**
20: $LPD^G(VDD) := max(PDs^G(VDD))$
21: $LPD^S(VDD) := max(PDs^S(VDD))$
22: **end for**

Fig. 7. Prior SPECTRE Simulation Step for the VA ROF Modelling

hundreds), it is proposed that only three V_{DD} levels to be used (the highest, middle and lowest). While $ROFs$, TPs^G, TPs^S, $VDDs$ are passed to the algorithm as input, the set of open resistances, ROs, is generated locally to obtain discrete representation for the ROF delay. Typically, eight and ten resistance values representing a logarithmic distribution are used in the simulation and reasonable results were observed for both cases. Two test patterns are considered in this method, the first one (TPs^G) for at-speed testing (detection of gross delay faults), whereas the other one (TPs^S) for faster-than-at-speed testing (detection of small delay faults). Those test patterns can be obtained using dedicated path delay aware Automatic Test Pattern Generation engines (ATPG).

After generating the discrete open resistance set (line 1), the procedure starts in the first part by fault simulating all fault locations ($ROFs$), test patterns (TPs) using V_{DD} settings ($VDDs$) and open resistance values (ROs) to obtain the path delay information (PD) as shown in lines (3-18). Once the delay values (PD) for fault free paths ($\forall RO = 0$) and faulty paths ($\forall RO \in ROs$) are obtained, the longest path delays at each VDD of long paths ($LPD^G(VDD)$) considering ($TP \in TPs^G$) and of short paths ($LPD^S(VDD)$) considering ($TP \in TPs^S$) are identified using the fault free path delay data PD ($\forall RO = 0$) as shown in line 19-22. Once the delays of the faulty paths and the delays of the longest paths versus VDD are obtained, then it is possible to determine the model parameters. It is important to note that this method in fault simulation is time consuming and is not suitable for large circuits. But since accuracy is very crucial to this work, we have employed it as it is. We are considering some optimization methods in a future work.

Input: PD(VDDs, ROFs, TPs^G,TPs^S,RO)
Output: $RO^G_{TH}(VDD)$, $RO^S_{TH}(VDD)$, RO_{cr}^{i-i+1}, $Bhv(i)$

1: **for all** $ROF \in ROFs$ **do**
2: **for all** $TP \in (TPs^G(ROF) \cup TPs^S(ROF))$ **do**
3: //Identifying: RO^G_{TH}, RO^S_{TH}
4: **for all** $VDD \in VDDs$ **do**
5: $RO^G_{TH}(VDD) := Intrp(LPD^G(VDD), PDs(ROF)(TP)(VDD))$
6: $RO^S_{TH}(VDD) := Intrp(LPD^S(VDD), PDs(ROF)(TP)(VDD))$
7: **end for**
8: //Identifying: RO_{cr}^{i-i+1}, $Bhv(i)$
9: $i := 1$, $PrevRO := \phi$
10: **for all** $RO \in ROs$ **do**
11: **if** $ROBhv(PrevRO) = ROBhv(RO)$ **then**
12: $PrevRO := RO$, $Bhv(i) := ROBhv(RO)$
13: **else**
14: $RO^L_{cr} := PrevRO$,$RO^H_{cr} := RO$
15: RO_{cr}^{i-i+1}:=avg(RO^L_{cr},RO^H_{cr})
16: **for** $iter = 1 \rightarrow MAX$ **do**
17: **if** ROBhv(RO^L_{cr}) = ROBhv(RO_{cr}^{i-i+1}) **then**
18: $RO^L_{cr} := RO_{cr}^{i-i+1}$
19: **else**
20: $RO^H_{cr} := RO_{cr}^{i-i+1}$
21: **end if**
22: RO_{cr}^{i-i+1}:=avg(RO^L_{cr},RO^H_{cr})
23: **end for**
24: $i := i + 1$
25: **end if**
26: **end for**
27: **end for**
28: **end for**

Fig. 8. The Proposed Method to Obtain the Parameters of the Voltage Aware ROF Model

By taking the SPECTRE-simulation output of Fig. 7, the detection thresholds and the intervals' behaviors and critical resistances are obtained. The open resistances detection threshold (i.e. RO^S_{TH} and RO^G_{TH}) for each ROF and TP is computed by employing cubic SPLINE interpolation to find the resistances corresponding to $LPD^G(VDD)$ and $LPD^S(VDD)$ given the faulty path delays and the corresponding open resistance (ROs) as shown in lines 1-7. Subsequently, the algorithm continues to identify the various possible resistance intervals (i) and their respective behaviors ($Bhv(i)$) and critical resistances (RO_{cr}^{i-i+1}). To identify the behavior, a function $ROBhv(RO)$ is used to check the behavior of that RO value. The possible behaviors are "inc", "dec", "mid-bump" and "mid-bump-inv" which were explained in previous section. The behavior is being checked $\forall RO \in ROs$, once the behavior changes (i.e. $ROBhv(RO) \neq ROBhv(PrevRO)$) then a critical resistance (RO_{cr}^{i-i+1}) between $PrevRO$ and RO can be identified. The algorithm searches for more accu-

rate value by successively narrowing the range of the solution by reducing the upper limit RO_{cr}^{H} or increasing the lower limit RO_{cr}^{L} as shown in the remainder of the algorithm. The range is narrowed at each iteration for MAX number of times. Typically, MAX was arbitrarily set to 10 and 15 and showed almost similar results (difference in order of ten Ω), therefore, 10 is used in obtaining the results shown in the rest of the paper. Following the explained procedure, the behavior and corresponding critical resistances along with the detection threshold are obtained for all fault locations and respective test patterns. The rest of the paper analyses the experimental results of the modelling procedure and the possible implications and projections considering the observability of behavior and fault detectability across technologies.

VI. Experimental Analysis on VA ROF model

Experiments were carried out on several benchmark circuits to verify the effectiveness of the proposed methodology in modelling the behavior and detectability characteristics of ROF with V_{DD}. The experimental setup and procedures followed to obtain the circuit netlist, fault list, V_{DD} setting, test patterns for at-speed and faster-than-at-speed testing were as explained in Section III-A. The results of the obtained model parameters for different benchmark circuits are reported in this section, however for space limit, results are analysed in detail for c17 circuit only.

Different test patterns were investigated in c17 circuit experiment. As rising test patterns resulted in single behavior for all faults, only results for falling transition test patterns which induce more behaviors and imply more challenging modelling scenario were reported in Table IV. Table IV shows the identified behavior parameters (i.e. resistance intervals and corresponding behavior) in column 2, 3 and 4, and the resistance detection threshold for small and gross delay faults per V_{DD} ($RO_{TH}^{S}(V_{DD})$,$RO_{TH}^{G}(V_{DD})$) in columns 5-10 for each fault in column 1. For example, the first two rows entry in the table shows for ROF number 1, two distinct resistance intervals were identified. The first identified behavior with voltage is a decreasing delay behavior "dec" which is manifested by resistances from 50 Ω (minimum used open resistance : σ or RO_{min}) up to 460 KΩ, whereas, for resistances from 460 KΩ to 10 MΩ (Maximum open resistance used: RO_{Full}) an increasing delay behavior "inc" is detected. Having a "dec" behavior for small range of RO was observed for faults in all circuits due to the dominance of fault free path delay behavior for that range and the length of that interval increases with the path length. For example, for fault location number 3 which is sensitized along a long path, the change in behavior from "dec" to "inc" occurs around 2 MΩ, and for fault location 8 sensitized along middle-length path, the change occurs around 700 KΩ, whereas for fault location sensitized along a short path the change is approximately at 400 KΩ. It is also observed that ROFs especially those sensitized via long paths (e.g. faults no. 3, 4 and 6), undergo transient "mid-bump" behavior when changing from "dec" behavior (for small RO) to "inc" behavior (for large RO). However for other faults especially those sensitized via shorter paths (e.g. faults no. 1, 2 and 8), this transient "mid-bump" behavior interval is reduced or not detected. This is again, can be attributed to the different strength (delay magnitude and variance with respect to V_{DD}) of the fault free path delay contribution which is dependent on the path length. Another interesting observation is that, for some fault location, a change in fault behavior when approaching the full open range (RO=10MΩ) is detected. As there is no apparent reason for such behavior changes, one possibility can be that the finding reported in [24] where it is stated that large open resistances behave differently from small open resistances.

An important note from this table is that, assuming fixed (such as "inc" behavior) for ROF is not always realistic and could be misleading especially if the transition test pattern/ fault locations are carefully not considered. In fact for rising transition test pattern encountering "inc" behavior is very rare or can almost be negligible.

Additionally, ROF detectability with V_{DD} is presented in Table IV columns 5-10. The open resistance detection threshold is presented for small delays in columns 5-7 and gross delay faults in columns 8-10. It can be observed that for the detection threshold for each fault varies with V_{DD}. This has a significant implication in testing. That is, selecting the best V_{DD} and test patterns for test among different test patterns/V_{DD} depends on the maximum fault coverage can be obtained. In this result, the maximum fault coverage can be denoted by the minimum resistance detection threshold which are boldfaced in Table IV. Considering gross delay faults, it can be observed that for fault no 3, minimum RO_{TH} (or σ) is obtained for all V_{DD}. This is because, the fault in this case was propagated along the longest path, therefore, any resistance value exceeds 0 Ω would ideally be detected. For other faults, it is observed that minimum RO_{TH} can be found at V_{DDH} which substantiates the observations/expectations in [16], [10], [13]. Considering small delay faults, it can be observed that, results are only reported for half of the faults. This is because, the same test patterns used to sensitize gross delay faults however only test patterns sensitizing short paths were considered. This results in achieving lower detection threshold (i.e. $RO_{TH}^{S} < RO_{TH}^{G}$ for each V_{DD}) as shown in the table. An interesting observation though is that, the minimum RO_{TH} is not always achieved at V_{DDH} as for fault no 5, the minimum threshold is found at V_{DDL}. This highlights some challenges in selecting the optimal test pattern/V_{DD} for test, especially when considering multi-voltage designs.

More circuits were considered and the VA ROF model parameters were obtained with the procedure/ experimental setup discussed in Section III-A. Figure 9 shows the behavior intervals statistics from different benchmark circuits based on 130 nm technology library using falling transition test patterns. In the figure, the resistance interval for each behavior found in each circuit is represented stacked bars. The last stacked bar at the most right represents the average behavior identified as proportion of the resistance domain. The figure shows that the dominance of the "dec" behavior over all the other behaviors even though only "falling transitions" were used. In average, the probability of encountering "dec" behavior is 5 times more than the probability of encountering "inc" behavior. This is

TABLE IV
ROF VAMODEL BEHAVIORAL AND DETECTABILITY PARAMETERS FOR C17 CIRCUIT (σ=RO_{min}= 50Ω)

#	Behavior Intervals			Detection Thresholds (KΩ)					
	Interval (KΩ)		Behavior	RO^S_{TH}			RO^G_{TH}		
	Lower	Upper		V_L	V_M	V_H	V_L	V_M	V_M
1	σ	460	**dec**	1.3	0.8	**0.6**	28.5	19.6	**15.3**
	460	10000	**inc**						
2	σ	442	**dec**	1.9	1.2	**0.8**	29.0	20.2	**15.7**
	442	10000	**inc**						
3	σ	517	**dec**	-	-	-	$\boldsymbol{\sigma}$	$\boldsymbol{\sigma}$	$\boldsymbol{\sigma}$
	517	2141	**mid-bump**						
	2141	9997	**inc**						
	9997	10000	**mid-bump**						
4	σ	280	**dec**	-	-	-	1.1	1.1	**1.0**
	280	1193	**mid-bump**						
	1193	8321	**inc**						
	8321	10000	**mid-bump**						
5	σ	355	**dec**	**0.4**	0.6	0.6	21.2	16.5	**13.9**
	355	1243	**mid-bump**						
	1243	10000	**inc**						
6	σ	384	**dec**	-	-	-	19.5	15.0	**12.5**
	384	1492	**mid-bump**						
	1492	10000	**inc**						
7	σ	515	**dec**	-	-	-	15.3	12.3	**10.6**
	515	1906	**mid-bump**						
	1906	9349	**inc**						
	9349	10000	**mid-bump**						
8	σ	178	**dec**	$\boldsymbol{\sigma}$	$\boldsymbol{\sigma}$	$\boldsymbol{\sigma}$	12.0	9.2	**7.6**
	178	708	**mid-bump**						
	708	9124	**inc**						
	9124	10000	**mid-bump**						
9	σ	50	**dec**	-	-	-	13.6	9.5	**7.5**
	50	176	**mid-bump**						
	176	10000	**inc**						

because, a logarithmic distribution probability is assumed for RO. Since the "dec" behavior is dominant for small RO values, this results in high global occurrence for "dec" when considering the logarithmic distribution. An implication from this figure is that, the methods used to distinguish ROF from other types of faults exploiting the "inc" behavior of such fault can potentially miss significant range of fault. Therefore, to enhance the distinguishing methodology, exploiting the "mid-bump" behavior -in addition to the "inc" behavior- is promising and could duplicate the distinguishing effectiveness.

The average detectability (i.e. resistance detection threshold) for small delay faults (SDF) and gross delay faults (GDF) versus V_{DD} in a number of benchmark circuits is depicted in Fig. 10. The vertical axis in this figure represent the open resistance value in KΩ, whereas the horizontal axis represents the circuit being considered in the analysis. For each circuit, the RO_{TH} is shown at each V_{DD} for SDF as (SDF(VDDL), SDF(VDDM) and SDF(VDDH)) and for GDF as (GDF(VDDL), GDF(VDDM) and GDF(VDDH)). The average detection thresholds for all considered circuit is illustrated at the most right of the figure. A general observation from the results of the individual circuits and that of the average is that, the minimum average detection threshold for both SDF and GDF is always achieved at the highest V_{DD} i.e. VDDH. That is, an implication of that in test generation could be that testing at the highest V_{DD} is most effective single voltage test strategy. However, for optimum fault detection, an individual consideration for faults has to be made to avoid test escapes for faults such as the one reported in Table IV (fault number 5).

The effect of the transition test patterns on the observability of the fault behavior and detectability is addressed and illustrated in Fig. 11 and Fig. 12 respectively. For each circuit, rising transitions (R) and falling transitions (F) were

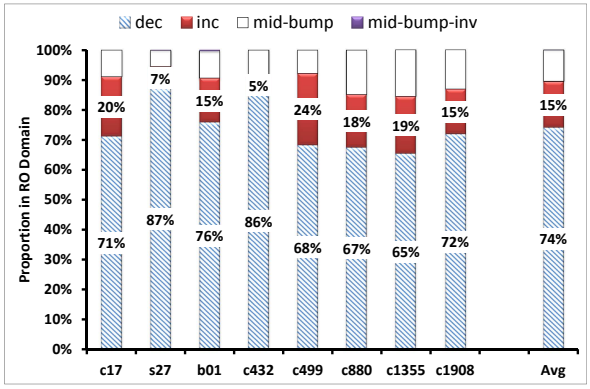


Fig. 9. ROF behaviors' Proportions for Different Benchmark Circuits

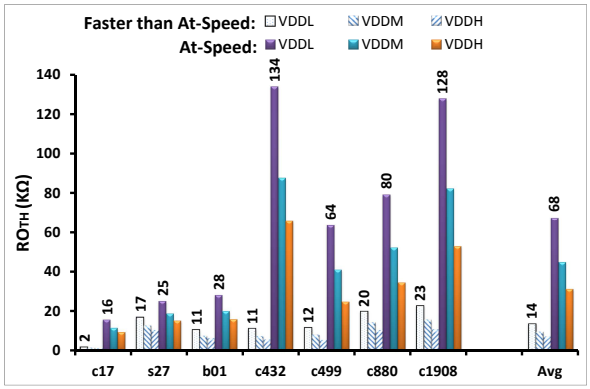


Fig. 10. Average ROF Detection Thresholds for Different Benchmark Circuits

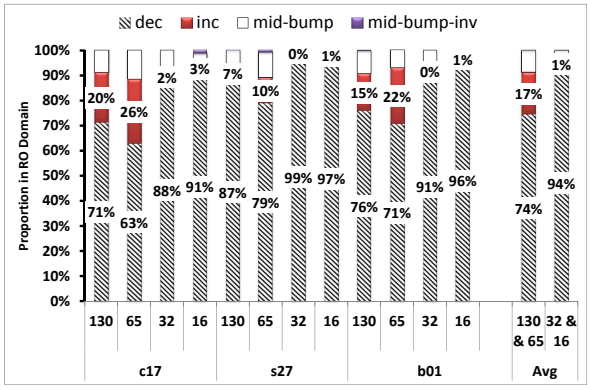


Fig. 11. ROF behavior Analysis for Different Transition Test Patterns

applied for all fault location. Fig. 11 shows the proportion of the identified behavior intervals in the resistance domain considering falling (F) and rising (R) transitions. Interestingly, Fig. 11 shows that the observability of different behaviors is significantly reduced when using rising transition test patterns compared to falling transitions. This is because, while the intrinsic fault free path delay behavior is almost insensitive to the transition type, the intrinsic fault behavior exhibits different patterns ("inc" and "constant" behaviors) when considering falling and rising transitions. This leads to significant reduction on the observable "inc" behavior in faulty paths.

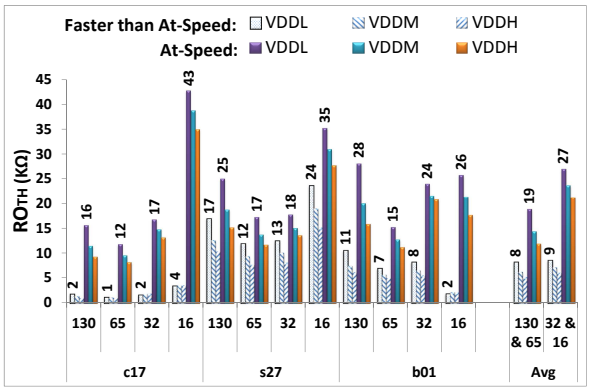


Fig. 12. ROF Detection Threshold Analysis for Different Transition Test Patterns

As for the ROF detectability with V_{DD} illustrated in Fig. 12, it is observed that for some circuits (e.g. c17, s27 and b01) falling transitions result in lower detection thresholds whereas in other circuits (e.g. c432) lower thresholds are achieved by rising transitions. The results show that, generally different test patterns and particularly transition patterns induce different fault behaviors and detectability. This highlights the significance in selecting the proper test pattern for exciting the required fault behavior in distinguishing the source of fault. Additionally it shows that, for optimizing the detection coverage, the suitable test pattern transition has to be used.

To investigate the fault behavior and detectability across technologies, different technology models: silterra 130nm (130), and BPTM technology models (65, 32, and 16) nm were considered and reported in Fig. 13 and Fig. 14.

In this experiment, falling transitions were used to sensitize more behaviors per fault. The results presented in Fig. 13 shows the behavior for different technologies whereas the ROF detectability for the same circuits and technology models are depicted in Fig. 14. As far as the behavior is concerned, it can be noted that, the observability of different behaviors (especially the "inc" behavior) is reduced for small nanometric technologies (32nm and 16nm) technologies compared to larger nanometric technologies (130nm and 65nm). On the other hand when considering the detectability, it can be observed in Fig. 14, that 32nm and 16nm technologies has larger detection thresholds. That is, in smaller nanometric technologies, the detectable resistance range is reduced.

Generally the different results for new technologies reported in Fig. 13 and Fig. 14 can be attributed to the difference in the electrical characteristics of the SPECTRE models in new technologies (e.g. due to metal gates, strained Si and

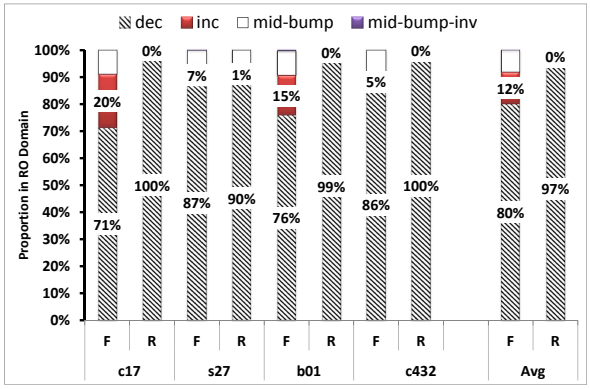


Fig. 13. ROF behavior Analysis for Different Technologies

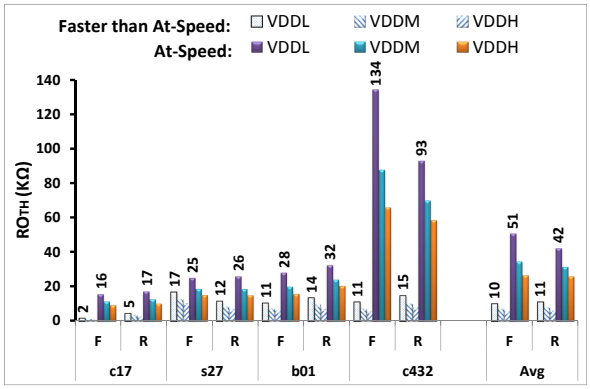


Fig. 14. ROF Detection Threshold Analysis for Different Technologies

hi-K dielectric insulator). A possible implication from the results is that, the reduced observability trend is likely to limit the effectiveness of fault distinguishing methodologies and therefore a concerned is raised on how to distinguish and screen faults with such non-unique behaviors. Additionally, the reduction in the detectable resistance range trend in new technologies, raises the importance of detecting more resistance range by means of small delay fault testing in newer and future technologies. This is because, undetectable resistive open faults are likely to cause infant mortality failures and thus posing potential reliability risks.

In summary, the results shown in this paper show the effectiveness of the proposed model which can be further exploited for test generation, fault simulators, distinguishing and localization techniques for resistive open faults. For multi-voltage designs, the use of this model is necessary to obtain accurate fault related work.

VII. Conclusion

With the increasing employment of multiple supply voltages in low power design, considering the effect of supply voltage on fault behaviour and detectability is necessary to optimize testing and diagnosis of manufacturing defects. Resistive open faults, which represent frequent manufacturing failures and cause delay violations and potential reliability risks, were considered in this work. The behaviour and detectability of resistive open fault were experimentally analysed as a function of a discrete set of the supply voltage. The experiments showed that the behaviour of a resistive open fault is open resistance-interval based and its detectable resistance range varies with V_{DD}. This observation was exploited and thus a general voltage aware model which fully represents the possible behaviour and detection is presented. It is demonstrated that the full resistance continuum of open faults can potentially be treated as sub set of continuous intervals representing the behaviours and three detection ranges. The methodology of identifying the model parameters utilizing exhaustive SPECTRE simulations, searching and interpolation is thoroughly explained. Considering the proposed model, it is believed that the work associated with fault simulation, test generation, fault screening and fault diagnosis of resistive open faults in voltage variant environment can be effectively enhanced.

Exploiting the proposed model, it is highlighted that the detectability of resistive opens is having a decreased trend with new technologies. This raises the importance and need of small delay testing to detect more open resistance range. Additionally it is shown that the observability of the unique increasing delay behaviour with V_{DD} for resistive open is reduced in new technologies. This poses a concern on whether screening methods which relies on that unique behaviour of resistive opens would still be effective for future technologies.

Considering the process variation in this model is our future focus.

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