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A MICROMACHINED ZIPPING VARIABLE CAPACITOR

by

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Abstract

Micro-electro-mechanical systems (MEMS) have become ubiquitous in recent years and are found in a wide range of consumer products. At present, MEMS technology for radio-frequency (RF) applications is maturing steadily, and significant improvements have been demonstrated over solid-state components.

A wide range of RF MEMS varactors have been fabricated in the last fifteen years. Despite demonstrating tuning ranges and quality factors that far surpass solid-state varactors, certain challenges remain. Firstly, it is difficult to scale up capacitance values while preserving a small device footprint. Secondly, many highly-tunable MEMS varactors include complex designs or process flows.

In this dissertation, a new micromachined zipping variable capacitor suitable for application at 0.1 to 5 GHz is reported. The varactor features a tapered cantilever that zips incrementally onto a dielectric surface when actuated electrostatically by a pull-down electrode. Shaping the cantilever using a width function allows stable actuation and continuous capacitance tuning. Compared to existing MEMS varactors, this device has a simple design that can be implemented using a straightforward process flow. In addition, the zipping varactor is particularly suited for incorporating a high-permittivity dielectric, allowing the capacitance values and tuning range to be scaled up. This is important for portable consumer electronics where a small device footprint is attractive.

Three different modelling approaches have been developed for zipping varactor design. A repeatable fabrication process has also been developed for varactors with a silicon dioxide dielectric. In proof-of-concept devices, the highest continuous tuning range is 400% (24 to 121 fF) and the measured quality factors are 123 and 69 (0.1 and 0.7 pF capacitance, respectively) at 2 GHz. The varactors have a compact design and fit within an area of 500 by 100 μm.

Declaration

The results reported in Section 3.3.2 consist of joint work with Andrew J. Laister from the University of Leeds. All other results reported in this thesis are primarily due to the author, except for background results, which are clearly referenced. Some of the results in Chapters 3 to 5 have been published elsewhere [104, 122, 134].

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To my parents

"For the LORD is good; his steadfast love endures forever, and his faithfulness to all generations." (Psalm 100:5)

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Nomenclature

$'$	Prime denotes parameter values per unit distance in Chapter 3
$'$	Prime denotes derivative with respect to time in Chapter 4
$\sim$	Tilde denotes trial function (with the exception of the biaxial modulus)
α_i	Parabolic fitting curve parameters ($i = 1$ to 3)
δ_x	Electrode offset
ε	Permittivity of dielectric material
ε_0	Permittivity of free space
ε_c	Biaxial contraction strain
ε_r	Relative permittivity (i.e. dielectric constant)
ϕ	Angle between connecting rod and horizontal reference
κ	Curvature due to bending
λ	Wavelength of RF signal
ν	Poisson's ratio
ν_1	Poisson's ratio of gold
ν_2	Poisson's ratio of chromium/copper
Π	Total elastic potential energy
θ	Angle between crank position and horizontal reference
σ	Conductivity
σ_2	Biaxial stress in chromium/copper
$\sigma_{1,r}$	Biaxial stress in gold after relaxation
$\sigma_{2,r}$	Biaxial stress in chromium/copper after relaxation
ω	Angular frequency
a, c, m	Trial function parameters for displaced cantilever axial profile
A	Area
b	Cantilever width
b_e	Electrode width
B	Radius of crank
c_i	Capacitance parameters for TRANS126 element ($i = 0$ to 4)
C	Capacitance

C_1	Lowest capacitance in continuously tunable range
C_2	Highest capacitance in continuously tunable range
C_r	Capacitance ratio
C_s	Series capacitance in varactor circuit model
C_{max}	Maximum capacitance
C_{min}	Minimum capacitance
d_1	Distance from bottom surface of bi-layered cantilever to neutral axis
d_2	Distance from top surface of bi-layered cantilever to neutral axis
D	Flexural rigidity of plate in bending
D_1	Flexural rigidity of gold layer
D_2	Flexural rigidity of chromium/copper layer
E	Young's modulus
E_1	Young's modulus of gold
E_2	Young's modulus of chromium/copper
E_d	Young's modulus of dielectric
E_m	Young's modulus function of cantilever in ANSYS model
$\tilde{E}$	Biaxial modulus
f	Frequency of RF signal
f_e	Electrostatic force per unit length
f_r	Electrical self-resonance frequency
F_s	External surface force
F_b	External body force
g	Plate separation in parallel-plate capacitor
G	Conductance
h	Cantilever total thickness
h_1	Thickness of gold layer in cantilever
h_2	Thickness of chromium/copper layer in cantilever
h_m	Cantilever thickness in ANSYS model
I_1	Area moment of inertia of gold layer about the neutral axis
I_2	Area moment of inertia of chromium/copper layer about the neutral axis
I_m	Area moment of inertia of cantilever in ANSYS model
K_c	Stress intensity factor
k_n	Normal stiffness of TRANS126 element after closure to minimum gap
l	Cantilever length

L	Inductance
L_s	Series inductance
M	Bending moment
M_m	Bending moment of cantilever in ANSYS model
P	Length of connecting rod
q	Electric charge
Q	Quality factor
R	Resistance
R_s	Series resistance
s	Gap between signal and ground conductors of CPW
s_d	Axial profile of cantilever under electrostatic load
s_r	Initial axial profile of cantilever due to residual stress
S	Surface of elastic body
t	Time
t_d	Thickness of dielectric
t_e	Equivalent air thickness of dielectric
TR	Tuning range
u	Displacement of elastic body
u_y	Stoke (vertical displacement) of TRANS126 element
U_e	External work due to electrostatic force
v	Vertical displacement of cantilever under electrostatic load
V	Volume of elastic body
V_e	Electrical potential difference
V_b	Bias voltage
w	Width of signal conductor in CPW
W	Strain energy
W_m	Internal elastic potential energy
x, y, z	Cartesian coordinates
Z_0	Characteristic impedance of transmission line
Z_a	Line element representing device anchor in varactor circuit model
Z_e	Line element representing the fixed electrode in varactor circuit model
Z_l	Line element representing CPW in varactor circuit model

Abbreviations

APDL	ANSYS Parametric Design Language
BCB	Benzocyclobutene
BEM	Boundary Element Method
CMOS	Complementary Metal-Oxide-Semiconductor
CMU	Carnegie Mellon University
CPW	Coplanar Waveguide
CU Boulder	University of Colorado at Boulder
C-V	Capacitance-Voltage
DC	Direct Current
DI	Deionised
DRIE	Deep Reactive Ion Etch
EPFL	Swiss Federal Institute of Technology at Lausanne
FEM	Finite Element Method
FM	Frequency Modulation
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HARPSS	High Aspect-Ratio combined Poly- and Single-crystal Silicon
IC	Integrated Circuit
IPA	Isopropyl Alcohol
KAIST	Korea Advanced Institute of Science and Technology
KU Leuven	Catholic University of Leuven
LAN	Local Area Network
MEMS	Micro-Electro-Mechanical Systems
MIT	Massachusetts Institute of Technology
MOS	Metal-Oxide-Semiconductor
MU	University of Missouri
MUMPs	Multi-User MEMS Processes
NJIT	New Jersey Institute of Technology
PSU	Power Supply Unit

PTFE	Polytetrafluoroethene
PZT	Lead Zirconate Titanate
RF	Radio-Frequency
RIE	Reactive Ion Etch
RMS	Root Mean Square
RSC	Rockwell Science Center
SEM	Scanning Electron Microscope
SIMIT	Shanghai Institute of Microsystem and Information Technology
SOLT	Short-Open-Load-Through
TEM	Transverse Electromagnetic
UC Berkeley	University of California at Berkeley
UCLA	University of California at Los Angeles
UIUC	University of Illinois at Urbana-Champaign
UoM	University of Michigan
U of S	University of Saskatchewan
USC	University of Southern California
UW	University of Waterloo
UV	Ultraviolet
VCO	Voltage-Controlled Oscillator

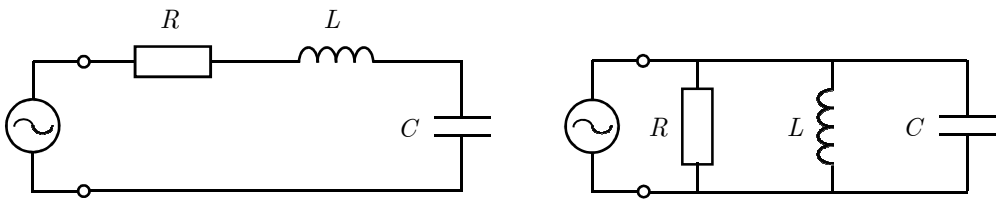
Chapter 1

Introduction

In electrical circuits, capacitors and inductors function as the energy storage elements with the former storing electrical energy and the latter storing magnetic energy [1]. When combined in series or in parallel, capacitors and inductors can be used to implement resonators that are integral to radio communication systems. An RLC circuit consisting of a resistor, an inductor and a capacitor can be connected either in series or in parallel to form a resonant circuit (see Figure 1.1). For both the series and the parallel circuits, the resonance frequency, in radians per second, is given by

$$\omega = \frac{1}{\sqrt{LC}} \tag{1.1}$$

where L and C are the circuit inductance and capacitance, respectively. By tuning either the capacitance or the inductance, the resonant frequency of the circuit can be tuned accordingly.



(a) (b)

Figure 1.1: Resonant circuits: (a) series RLC resonator; (b) parallel RLC resonator.

Figure 1.2 shows the geometry of a simple parallel-plate capacitor consisting of two conductor plates separated by an insulating region known as the dielectric. If the charge that exists on the two plates is $+q$ on one plate and $-q$ on the other, the capacitance is defined as the constant of proportionality relating the potential difference, V_e to the charge, q i.e.

$$C \equiv \frac{q}{V_e} \tag{1.2}$$

This relationship is true in general for any two conductors. For the case of the parallel-plate capacitor, the relationship between capacitance and the device geometry can be expressed as [2]

$$C = \frac{A\varepsilon}{g} \tag{1.3}$$

where A is the overlap area of the plates, g is the plate separation and ε is the permittivity of the dielectric. Equation (1.3) is valid provided the area is large relative to the plate separation [3].

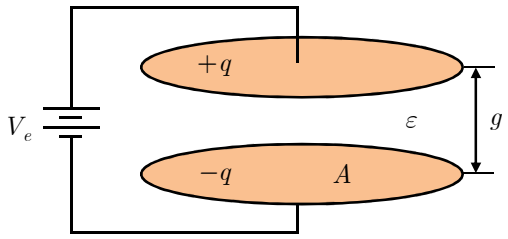


Figure 1.2: Parallel-plate capacitor.

Variable or tunable capacitors are designed with a variety of capacitance ranges and are packaged into different sizes depending on the application. By varying the capacitance area, the plate separation distance or the dielectric permittivity, the device capacitance can be tuned. An air variable capacitor used in amateur radio communication equipment is shown in Figure 1.3. In this design, turning the tuning shaft varies the amount of overlap area between capacitor stator and rotor plates, resulting in a change in capacitance.

The focus of this dissertation is on the development of a new continuously tunable, micromachined capacitor suitable for applications in the 0.1 to 5 GHz frequency range.

An introduction to the context of this work, the research objectives and a brief description of the thesis organisation is given in the following sections.

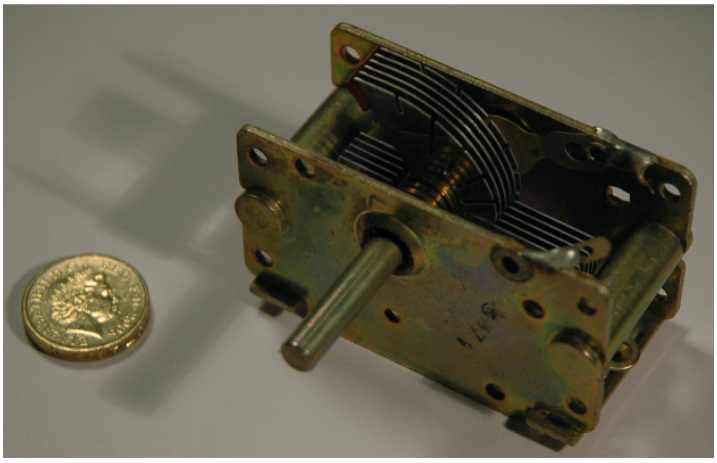


Figure 1.3: Amateur radio air variable capacitor (100 pF maximum capacitance).

1.1 RF MEMS Variable Capacitors

Micro-electro-mechanical systems (MEMS), also known as microsystems, encompass a broad range of miniaturised components fabricated using batch processing techniques derived from the microelectronics industry [4]. From its early beginnings in the 1970's, the MEMS industry has grown tremendously and a recent market study by iSuppli Corp predicts that the global MEMS market will expand to $8.8 billion by 2012 [5]. Typical MEMS applications include automotive motion sensors, actuators for digital light processing, and ink-jet printer heads, while newer growth areas are fuelled by motion sensors for consumer electronics. Two well-known products employing MEMS technology are the Nintendo Wii game console and the Apple iPhone mobile handset (see Figure 1.4) [6].

The development of the MEMS industry opened new possibilities for implementing tunable radio-frequency (RF) circuit components with enhanced performance [7-11]. Improvements in performance are due, in part, to the development of new materials and the novel use of surface- and bulk-micromachining techniques [12]. On the other hand, MEMS technology opened the possibility of incorporating mechanical motion in integrated-circuit (IC) components. The first MEMS switch was reported by Petersen of IBM in 1979 [13]. Subsequently, Larson et al. from Hughes Research Laboratories demonstrated a rotating MEMS switch for microwave applications in 1991 [14]. Since then many high-quality RF MEMS components have been demonstrated, including

switches [15-17], tunable capacitors [18, 19], inductors [20, 21], resonators [22, 23] and their associated application circuits [24-27].

(a) (b)

Figure 1.4: Popular consumer products with MEMS components: (a) Apple iPhone 3GS; (b) Nintendo Wii remote controller.

Reconfigurable microwave circuits traditionally employ solid-state varactors to provide variable capacitance. The word 'varactor' comes from the term 'variable reactor', i.e. the device capacitive reactance is changed by tuning its capacitance [28]. Varactors in common RF applications include p-n junction diodes [29, 30], Schottky diodes [31, 32] and metal-oxide-semiconductor (MOS) capacitors [33, 34]. The main advantages of MEMS varactors over these traditional solid-state varactors include a higher quality factor (Q-factor), larger tuning range, lower power consumption (with electrostatic actuation), lower temperature sensitivity and high linearity with respect to RF power.

The Q-factors of semiconductor varactors are typically less than 50 for frequencies greater than 1 GHz [8] whereas Q-factors larger than 100 are relatively easy to obtain in MEMS varactors [35]. A physical model of a p-n junction varactor is shown in Figure 1.5, where the device consists of n- and p-type semiconductors sandwiched between metal ohmic contacts. The majority charge carriers in the n- and p-regions are electrons and holes, respectively. A 'depletion layer', characterised by an absence of charge carriers, exists in the middle of the device. Hence, the depletion layer is analogous to the dielectric in a parallel-plate capacitor. When a reverse bias is applied (see Figure 1.5(b)), the width of the depletion layer increases, leading to a decrease in capacitance [36]. Since the varactor series resistance includes the bulk resistance of the

semiconductors [28], the Q-factor of a p-n junction varactor is relatively low. In contrast, MEMS varactors can be designed with electrodes that are made using high-conductivity metals such as aluminium or gold.

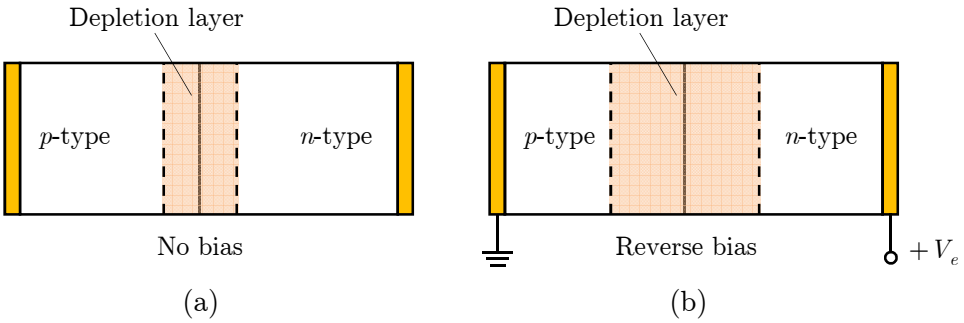


Figure 1.5: p-n junction varactor model.

In addition, MEMS varactors have demonstrated tuning ranges greater than 3000% [19] while semiconductor varactors are limited to tuning ranges of 500% or less. The negligible power consumption of electrostatically-actuated MEMS varactors is also particularly attractive for portable consumer electronics since the battery life can be extended. Finally, the linearity of MEMS varactors with respect to RF power is a strong selling point since signal distortion can be reduced in the presence of voltage swings [35]. An example of a MEMS varactor is shown in Figure 1.6 where the device capacitance can be tuned by changing the overlap area between interdigitated structures using a comb-drive actuator.

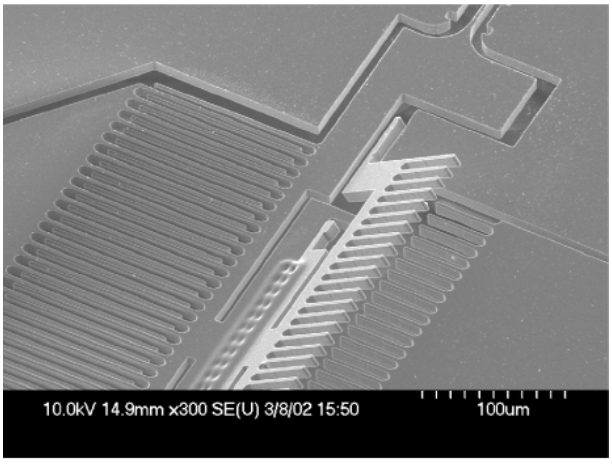


Figure 1.6: A micromachined MEMS varactor [37].

Other variable capacitors are also available such as ferroelectric varactors [38-40], heterostructure barrier varactors [41, 42] and liquid crystal varactors [43] among others

[35, 44]. However, at present only MEMS varactors are able to provide the combination of a high Q-factor (i.e. low-loss), large tuning range, low power consumption, low temperature sensitivity and linearity with RF power.

The disadvantages of the MEMS approach to implementing varactors are in some ways similar to the disadvantages associated with MEMS switches [8, 35, 44-47]. For one, MEMS varactors have a greater sensitivity to external vibration due to the use of mechanically compliant parts. Hence, careful design is required to ensure that the varactor will be robust enough for the intended application. In addition, reliability is a concern since a design with moving parts introduces numerous modes of failure such as fracture and creep deformation. Where contact between the moving and fixed parts of a varactor occurs, additional failure modes such as stiction and surface wear can also occur. The problem of moisture- or contaminant-induced stiction can be reduced by encapsulating the varactor within a hermetic package. This increases overall system complexity and cost, and thus the selection of a suitable packaging must be done with careful consideration. Stiction can also be caused by dielectric charging and hence designers may have to select appropriate material combinations or alter certain design features [48] to avoid device failure.

Another disadvantage of MEMS varactors is the slower tuning speed relative to solid-state varactors. Typical tuning speeds for MEMS varactors are on the order of microseconds while tuning speeds for solid-state varactors are in the region of nanoseconds. Nevertheless, this is sufficient for most RF applications except certain communication and radar components that require extreme frequency agility [49]. One way of increasing mechanical response speed is by increasing the stiffness of the compliant suspensions with the trade-off being a higher DC actuation voltage. However, using stiffer mechanical parts will help to reduce the problem of stiction since the mechanical restoring forces are increased. It is also often stated that the high actuation voltages of MEMS components pose difficulties for portable consumer electronics since the supply voltage is usually around 5 V or less. In reality, it is not difficult to scale these voltages to the level required by MEMS components (up to 50 V) through the use of high efficiency DC-DC converters such as charge pumps [46]. The drawback of such an approach would be the increase in system cost.

1.2 Research Objectives

Relative to established RF technologies based on III-V compound semiconductors (GaAs, GaN, InP, InSb) and silicon semiconductors (SiC, SiGe, CMOS, i.e. complementary metal-oxide-semiconductor), RF MEMS is in a relatively early stage of development. Nevertheless, reliability issues are actively being addressed and reasonable actuation cycles (greater than 100 billion) have been achieved for MEMS switches [35, 50]. Research effort into MEMS varactors has only recently picked up momentum and it is expected that similar levels of reliability can be achieved since MEMS varactors share many similar design characteristics with MEMS switches. Once the teething problems are ironed out, it is expected that RF MEMS will become commonplace in the near future, with switches paving the way for other components. Suitable application areas for MEMS varactors include tunable LC-tanks of voltage-controlled oscillators (VCO), impedance matching, tunable filters and loaded-line phase shifters.

In this thesis, the design, simulation, fabrication and experimental characterisation of a novel MEMS varactor is reported. After the switch, the varactor is arguably the next most important component in RF systems. Hence, the goal of this work is to provide a strong design candidate for future commercialisation of MEMS varactors. The primary design challenges include realising a large (greater than 300%), continuous tuning range and a high Q-factor (above 100) in order to maximise the versatility of the device in terms of application.

The intended deployment for the new MEMS varactor is in mobile communications, where there is an increasing amount of industry interest in MEMS varactors [8, 46, 47]. The nature of consumer demands for mobile phones is such that an ever increasing level of functionality is required within a smaller and lighter handset. Furthermore, modern mobile phones are required to provide clearer reception and yet demonstrate increased battery life. It is also not uncommon for a modern handset to provide reception over a large number of frequency bands such as GSM (4 bands), wireless LAN, GPS, Bluetooth, FM radio and imminently, mobile television. A low-loss MEMS varactor with a large tuning range is well-placed to meet such requirements and hence the proposed varactor will be aimed for application at the 0.1 to 5 GHz range.

Due to the benefits associated with a more compact varactor in mobile applications, a key specification for the proposed varactor is a small device footprint. To this end,

the possibility of integrating a dielectric with very high-permittivity, such as lead zirconate titanate (PZT), is explored. By increasing the dielectric permittivity, the size of the varactor can be reduced for a given capacitance. In addition, it is difficult to achieve large capacitances in MEMS varactors [48] with standard dielectric materials (e.g. silicon dioxide or silicon nitride). Although the capacitance of a device with a low-permittivity dielectric can be increased by reducing the dielectric thickness, there are practical limitations such as excessive surface roughness, dielectric breakdown and pinhole defects. Therefore, using high-permittivity dielectrics may be the only practical way of providing larger capacitances (greater than 20 pF) for low frequency applications (less than 0.5 GHz).

1.3 Thesis Structure

The remainder of this thesis is organised into five chapters. In the next chapter, a comprehensive review of MEMS varactors in the open literature is given. The review provides a classification of varactors based on their design features and a varactor library is compiled as a design resource for RF engineers. A new varactor design is proposed in Chapter 3 and detailed electromechanical simulation results are presented. RF simulation results for the varactor Q-factor are also reported. Chapter 4 provides a fabrication method developed for the varactor prototypes, with discussion on the process issues and the steps taken to overcome certain developmental challenges. Subsequently, experimental characterisation results for the varactors are reported in Chapter 5. The conclusions arising from the research in this dissertation, and recommendations for future work are summarised in Chapter 6.

Chapter 2

MEMS Varactors: A Literature Survey

This chapter is a review of the state of the art in RF MEMS varactor technology. The advantages and disadvantages of various varactor designs are highlighted relative to key figures of merit. The main focus of this literature survey is on *analog* MEMS varactors, where continuous tuning is possible over a range of capacitances. Another method of achieving variable capacitance is by implementing an array of capacitive switches. Such varactors, also known as *digital* MEMS varactors, are also included in the review. From this literature survey, a library of micromachined varactors is compiled as a resource for RF design engineers.

The first MEMS varactor was fabricated at the University of California at Berkeley by Young and Boser [18]. Since then, the MEMS research community has been actively pursuing a high-Q, low-loss tunable capacitor with large tuning range. MEMS varactor designs can be broadly categorised into gap-tuned devices, in which the gap between the capacitor electrodes is varied to achieve tuning, and area-tuned devices, where the electrode overlap area is varied instead. The majority of these varactors employ electrostatic actuation for its relative ease of implementation compared to other actuation methods. In addition, electrostatic actuators consume very little power and hence the device power consumption can be kept low.

2.1 Figures of Merit

In the literature, two parameters are often quoted as an indication of a varactor's capacitance range, namely the capacitance ratio and the tuning range. The capacitance ratio (C_r) is defined as

$$C_r = \frac{C_{\max}}{C_{\min}} \tag{2.1}$$

where $C_{\max}$ is the maximum capacitance and $C_{\min}$ is the minimum capacitance. A related parameter known as the tuning ratio is given by

$$\text{tuning ratio} = \frac{C_{\max} - C_{\min}}{C_{\min}} = C_r - 1 \tag{2.2}$$

Although the capacitance and tuning ratios give an indication of the absolute capacitance range of a varactor, they do not provide any information on the presence of discontinuity in the capacitance-voltage (C-V) characteristic. Both are functions of the extreme values of capacitance and hence a varactor with a large tuning ratio may not necessarily have a smooth C-V characteristic. Furthermore, the term capacitance ratio is also used to describe bistable capacitive switches operating at two discrete capacitance values. Hence, it can be misleading to use the term capacitance (or tuning) ratio to describe the continuous tuning of varactors. The tuning *range* (TR) of a varactor, expressed as a percentage, can be defined as

$$TR = \frac{C_2 - C_1}{C_1} \times 100\% \tag{2.3}$$

provided the device capacitance can be tuned continuously between C_1 and C_2 ($C_2 > C_1$). For certain designs, the value of C_1 corresponds to the minimum capacitance although this is not the case for some MEMS varactors that have discontinuous C-V characteristics.

Apart from specifying a varactor's tuning range, the specific value of C_1 (or C_2) is required to determine its application frequency. For frequencies between 30 and 600 MHz, capacitance values of around 5 to 50 pF are required [48]. Correspondingly, lower capacitance values of around 0.1 pF are required for applications up to 12 GHz [51]. In MEMS varactors, the capacitance value in the unactuated state is sometimes termed the nominal capacitance.

To minimise the loss attributed to a varactor in an RF circuit, its Q-factor at the frequency of operation must be maximised [9]. If a varactor is modelled as a capacitance, a resistance and an inductance in series, the Q-factor is given by [48]

$$Q = \frac{1}{2\pi f C R_s} \tag{2.4}$$

where f is the frequency of operation, C is the device capacitance and R_s is the series resistance. This equation is valid provided the frequency is much less than the electrical self-resonance which is defined as

$$f_r = \frac{1}{2\pi\sqrt{L_s C}} \tag{2.5}$$

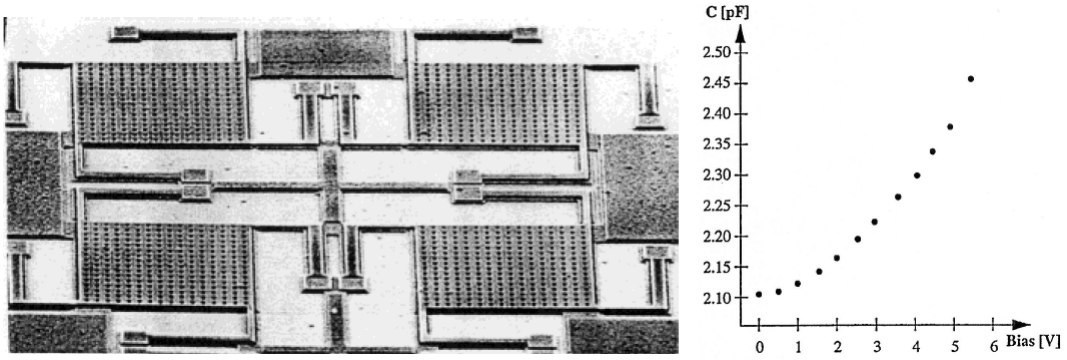
where L_s is the series inductance. At the self-resonant frequency, the device Q-factor becomes zero. Therefore, for a varactor to be useful as a tuning component, its intended application frequency must be well below its electrical self-resonance.

The following two sections review gap- and area-tuned varactors, respectively. Section 2.4 introduces *zipping* varactors: devices with parts that zip together to provide capacitance tuning. Digital MEMS varactors are reviewed in Section 2.5 and finally, certain unique varactor designs that are less widely explored are presented in Section 2.6. The performance parameters of MEMS varactors in this review are summarised in a MEMS varactor library in Section 2.7.

2.2 Gap-Tuned Varactors

The first successful implementation of a MEMS varactor was Young and Boser's gap-tuned device [18]. In this design, a movable aluminium top plate is suspended by four folded beams over a fixed aluminium bottom electrode. The aluminium electrodes ensure a low series resistance and are important for achieving a high Q-factor. Capacitance is tuned by varying the bias voltage between the two electrodes. An increase in the bias voltage leads to an increase in the electrostatic force of attraction between the electrodes, and hence, a decrease in the gap separating them. In such a configuration, the maximum displacement of the top plate is a third of the gap at zero bias due to the electrostatic pull-in instability [4]. This corresponds to a theoretical maximum tuning range of only 50%. To obtain the required capacitance, four micromachined varactors were connected in parallel, resulting in a capacitance range of

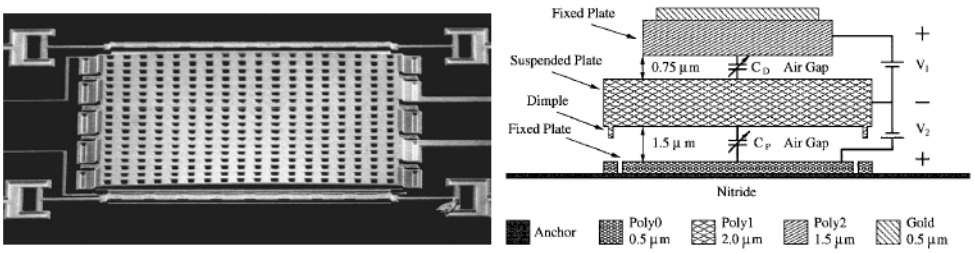
2.11 to 2.46 pF (16% TR). Although the demonstrated tuning range was far lower than expected due to parasitic capacitances, the reported Q-factor of 62 at 1 GHz was much better than typical solid-state varactors. Figure 2.1 shows a scanning electron microscope (SEM) image of this varactor and its C-V characteristic.



(a) (b)

Figure 2.1: UC Berkeley gap-tuned parallel-plate varactor: (a) SEM image; (b) C-V characteristic [18].

Subsequently, Dec and Suyama [52] at Columbia University implemented a gap-tuned varactor using the Cronos/MEMSCAP MUMPs process [53]. With a polysilicon fixed electrode and a gold-coated polysilicon movable electrode, they achieved a TR of approximately 50% ($C_1 = 2.05$ pF). In order to extend the tuning range even further, a three-plate varactor design was also reported where a movable electrode is suspended equidistant between two fixed electrodes. By separately biasing the movable plate and either of the two fixed plates, the range of travel can be extended. A TR of 87% was demonstrated out of a theoretical maximum of 100%. However, due to the high resistivity of polysilicon relative to metals such as aluminium and gold, the measured Q-factors were low: 20 and 15 at 1 GHz for the two-plate and three-plate designs, respectively.

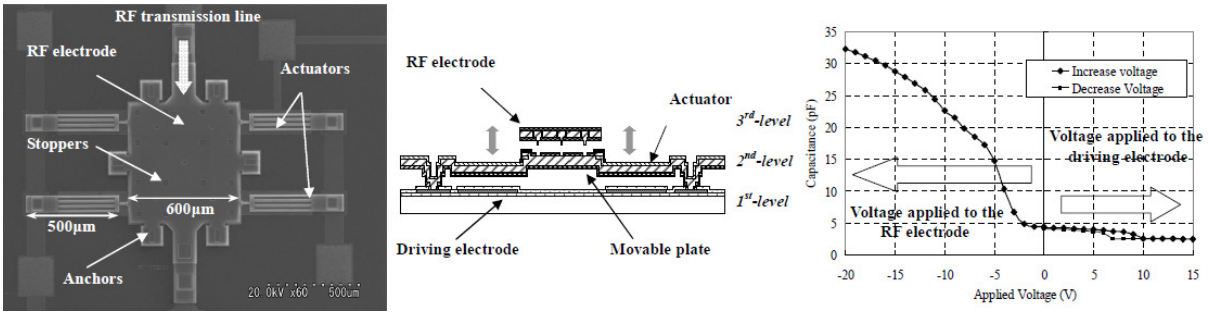


(a) (b)

Figure 2.2: Columbia three-plate varactor: (a) SEM image; (b) schematic cross-section [52].

The need for suspensions of sufficient mechanical compliance also contributes to increasing device series resistance. Figure 2.2 shows an SEM image and a schematic of the Columbia three-plate varactor.

Recently, two new designs for three-plate varactors have been reported [54, 55]. Unlike the design in [52], these varactors were not designed for bi-directional actuation. Conversely, only one of the fixed electrodes is used for actuation while the other fixed electrode forms the RF varactor together with the movable plate. In addition, the zero-voltage varactor state corresponds to a minimum gap in the RF varactor. When actuated, the gap of the varactor increases, resulting in a decrease in capacitance. The three-plate varactor fabricated by Konishi et al. at Nikon Corporation demonstrated a TR of 1180% along with a relatively large $C_{\max}$ of 32 pF [54]. They were able to achieve such a large maximum capacitance by using the built-in stress of the movable plate to deform it towards the fixed electrode, achieving a small minimum gap. Electrode shorting is prevented by rigid stoppers that also define the initial gap size. Figure 2.3 shows the Nikon three plate varactor design. Leidich et al. [55] demonstrated a three-plate design with a high Q-factor (larger than 100 up to 2 GHz) although the TR was comparatively low at 167% ($C_1 = 1.5$ pF).



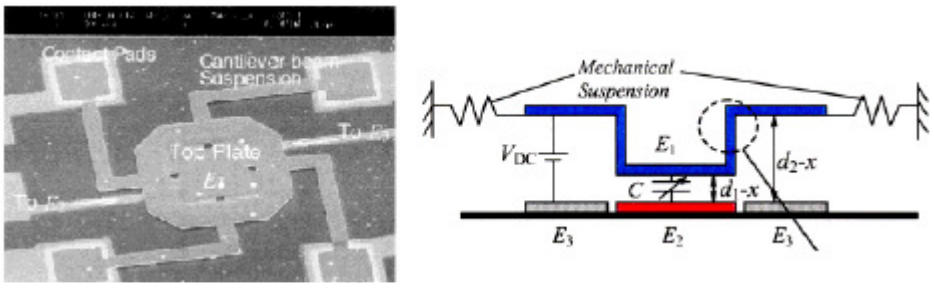
(a) (b) (c)

Figure 2.3: Nikon three-plate varactor: (a) SEM image; (b) schematic cross-section; (c) C-V characteristic [54].

2.2.1 Dual-Gap Varactors

To achieve an extended tuning range with parallel-plate, electrostatically-actuated varactors, Zou et al. [56, 57] from the University of Illinois at Urbana-Champaign (UIUC) implemented a varactor with a stepped profile in the movable plate. This allows the use of a different gap size for the actuation electrodes and the RF varactor (see Figure 2.4). By designing the gap of the actuation electrode to be more than three

times the gap of the RF varactor, the travel range of the varactor is no longer limited by the pull-in instability.



(a) (b)

Figure 2.4: UIUC dual-gap varactor (a) SEM image; (b) schematic cross-section [57].

However, tuning will still be limited by the lack of perfect planarity (e.g. due to stress-induced warpage) and excessive surface roughness in the electrodes. The need to maintain insulation between the varactor electrodes also imply that in practice a dielectric layer must be present (or a sufficient air gap must be maintained). A TR of 70% and a Q-factor of 30 at 5 GHz was reported for the UIUC dual-gap varactor.

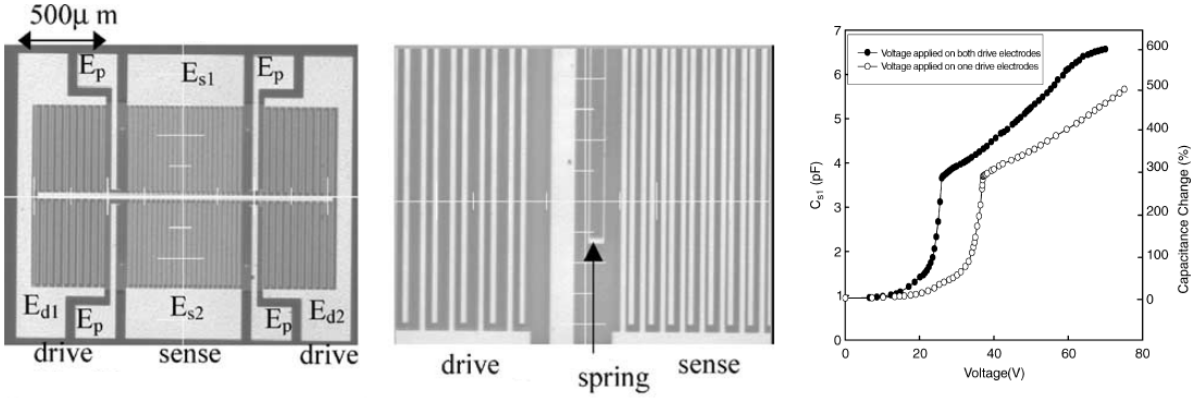
A variety of other dual-gap varactors have been reported [58-65]. These varactors, implemented using both non-standard and commercial foundry processes, have achieved tuning ranges of up to 520% [64]. Varactors with high Q-factors that are suitable for application at Ka-band (26 to 40 GHz) operation have also been demonstrated [59, 61, 64].

2.2.2 Interdigital Gap-Tuned Varactors

Several researchers have reported gap-tuned varactor designs where the RF capacitor consists of interdigitated comb structures [66-68]. The gap between these comb fingers is varied using electrostatic actuation. Unlike the previous designs where the electrode motion is out-of-plane, these comb structures have in-plane actuation.

Xiao et al. from the New Jersey Institute of Technology (NJIT) reported gap-tuned interdigital varactors fabricated using a deep reactive ion etching (DRIE) process [66]. The silicon varactor electrodes are capped with aluminium for lower series resistance. A TR of 595% (0.945 to 6.57 pF) was demonstrated although the Q-factor was only 100 at 1 MHz. The authors attributed the low Q-factor to the lossy silicon substrate. It is also possible that the series inductance of the device is very high due to the

suspension design, limiting the use of this varactor at low frequencies. Figure 2.5 shows an image of one of the NJIT varactors and its C-V characteristic.

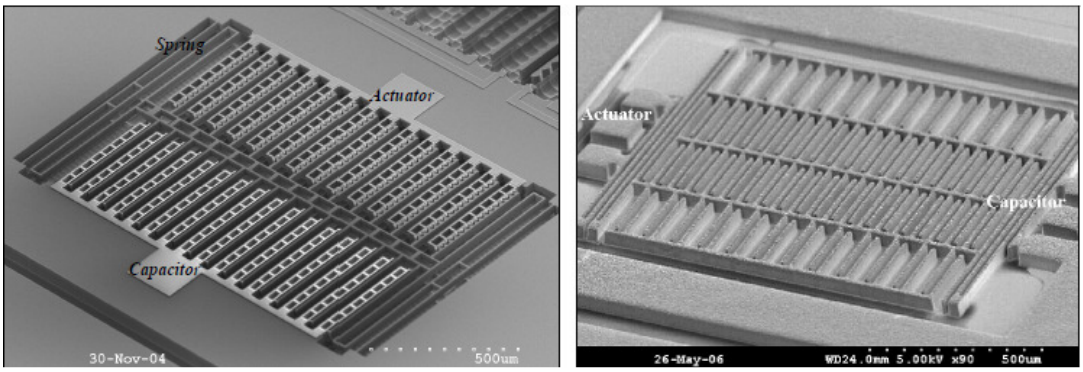


(a) (b) (c)

Figure 2.5: NJIT interdigital varactor: (a) microscope image; (b) close-up view of drive and sense electrodes; (c) C-V characteristic [66].

Subsequently, Monajemi and Ayazi from Georgia Institute of Technology reported a gap-tuned interdigital varactor suitable for applications at higher frequency (1 GHz) [67]. The varactors were implemented using high aspect-ratio combined poly- and single-crystal silicon (HARPSS) technology. Using low-inductance suspensions and an additional gold layer above the silicon comb fingers, a Q-factor of 49 at 1 GHz was obtained for a C_1 value of 2.5 pF. The reported TR of 100% was modest but on the other hand, the actuation voltage required was only 2 V. A different interdigital varactor with high aspect-ratio, electroplated silver electrodes was reported by Rais-Zadeh and Ayazi [68]. In this design, a high Q-factor greater than 200 at 1 GHz was obtained through the use of highly-conductive silver electrodes and a low-loss polymer substrate. The device was fabricated on a silicon substrate coated with a 20 μm thick Avatrel polymer (based on polynorbornene, see [69]) and the backside silicon beneath the varactor was removed to reduce substrate loss. This varactor can be tuned for capacitances between 0.68 to 1.56 pF (129% TR). Figure 2.6 shows SEM images of the Georgia Tech varactors.

The main advantage of interdigital varactors is that the shape of the varactor comb structure can be lithographically defined in one mask step. Hence, the fabrication process of such varactors is considerably straightforward relative to parallel-plate designs.

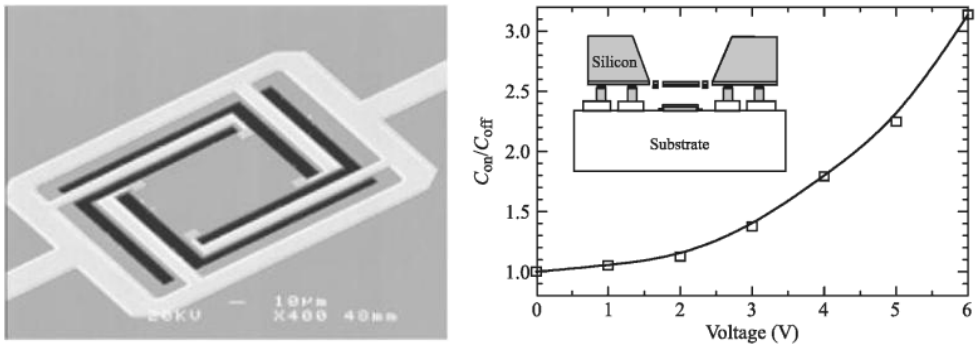


(a) (b)

Figure 2.6: Georgia Tech interdigital varactors: (a) HARPSS varactor [67]; (b) high aspect-ratio silver varactor [68].

2.2.3 Varactors with Piezoelectric Actuation

As an alternative to electrostatic actuation, parallel-plate varactors with piezoelectric actuation have been proposed by various research groups [70-73]. The advantages of using piezoelectric actuators include a larger stable displacement range, low voltage operation (less than 10 V), bi-directionality and the absence of dielectric charging effects.



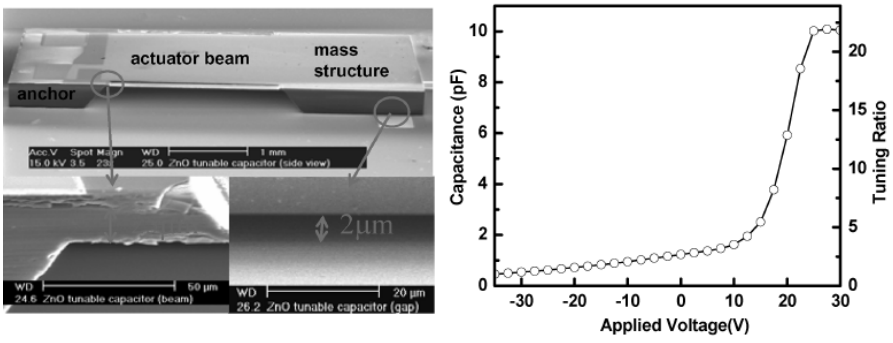
(a) (b)

Figure 2.7: LG Electronics piezoelectric varactor: (a) SEM image of movable plate and actuators; (b) plot of C_r versus voltage and device schematic [70] (figures reproduced from [48]).

Park et al. from LG Electronics demonstrated the first varactors employing piezoelectric actuators in 2001 [70]. Each unimorph actuator consists of a 380 nm thick layer of PZT sandwiched between platinum and ruthenium oxide electrodes. The varactor achieved a TR of 210% (around 0.1 to 0.3 pF) at a low actuation voltage of

6 V. A Q-factor of 210 at 1 GHz was reported. Due to the high processing temperatures (up to 650 °C) required to anneal the PZT, the actuators and movable plate of the device were first fabricated on a silicon substrate and then flip-chip bonded onto the final device substrate. The silicon substrate was then removed in the device region via backside etching. Figure 2.7 shows the LG Electronics varactor design and its tuning characteristics.

To improve compatibility with standard microelectronic fabrication, Lee and Kim from the University of Southern California (USC) implemented a varactor with zinc oxide (ZnO) actuators [71]. The device was fabricated on silicon using a combination of surface and bulk micromachining and then transferred onto a glass substrate. The actuator has a unimorph design, consisting of a 350 nm thick layer of ZnO sandwiched between aluminium electrodes. As the maximum process temperature was 300 °C, it is more compatible with standard IC fabrication technology. A very large TR of 2000% (0.46 to 10.02 pF) was achieved through the use of bi-directional actuation. However, the maximum actuation voltage of 35 V was high for a piezoelectric varactor (see Figure 2.8). This could be due to the lower piezoelectric constant of ZnO (relative to PZT) as well as excessive stiffness in the varactor beam. The measured Q-factor of the device was around 10 at 2 GHz which is comparatively low.

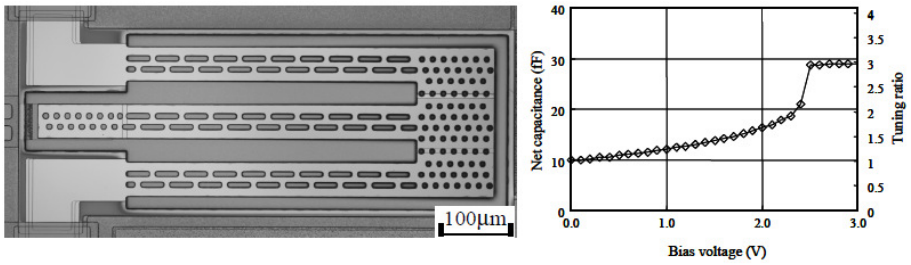


(a) (b)

Figure 2.8: USC piezoelectric varactor: (a) SEM image; (b) C-V characteristic [71].

A third varactor with piezoelectric actuation has been reported by Kawakubo et al. from Toshiba Corporation [73]. This varactor uses actuators with a bimorph design, where there are two layers of aluminium nitride each sandwiched between aluminium electrodes. By applying an opposite electric field to the two layers, one layer contracts while the other expands resulting in vertical displacement. A very low actuation voltage of 3 V was used and a TR of 100% was reported (10 to 20 fF). Although

varactors with TR values greater than 900% were reported by the same authors [72], this was due to the movable varactor plate coming into contact with the silicon nitride insulation over the fixed electrode, resulting in a large jump in capacitance. Like the USC varactor, this device was also designed to be CMOS compatible.

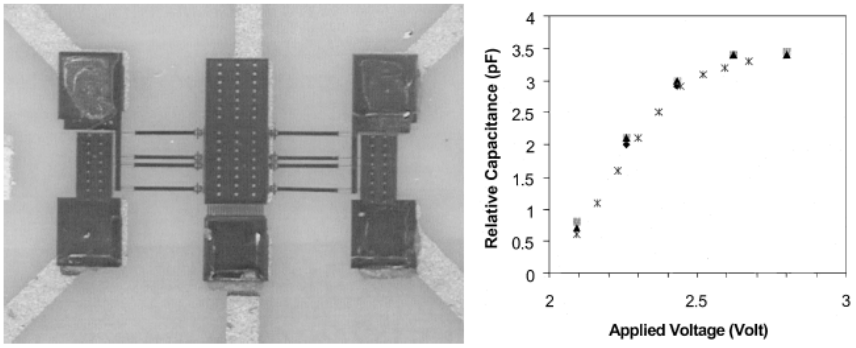


(a) (b)

Figure 2.9: Toshiba piezoelectric varactor: (a) optical image; (b) C-V characteristic [73].

2.2.4 Gap-Tuned Varactors with Thermal Actuation

Apart from using electrostatic and piezoelectric actuation, parallel-plate varactors with thermal actuation have also been demonstrated. Thermal actuators translate differential expansion of *hot* and *cold* arms into vertical motion in the movable plate of a varactor, changing the gap and hence capacitance. Harsh et al. from the University of Colorado at Boulder (CU Boulder) reported a flip-chip integrated MEMS varactor that is tuned using polysilicon thermal actuators [74, 75]. The actuators and the movable plate were fabricated using the commercial MUMPs process and subsequently transferred onto a ceramic substrate. A large TR of 600% (0.5 to 3.5 pF) was demonstrated along with a measured Q-factor of 100 at 10 GHz.



(a) (b)

Figure 2.10: CU Boulder thermally-actuated varactor: (a) optical image; (b) C-V characteristic [75].

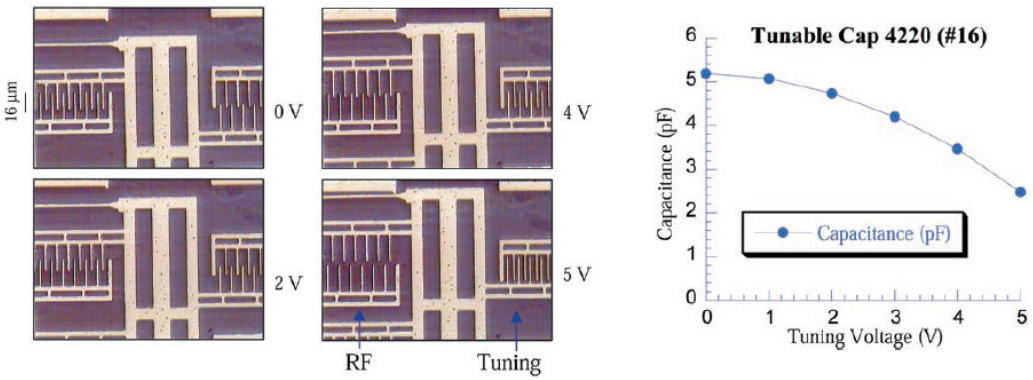
However, thermal actuators consume much more power relative to electrostatic or piezoelectric actuators due to the current that is required to heat up the actuator arms. In addition, thermal actuators have longer response times relative to electrostatic actuators and hence tuning speeds are correspondingly lower. An optical image of the CU Boulder varactor and its tuning characteristics is shown in Figure 2.10. A summary of gap-tuned varactors is given in

Table 2.1 of Section 2.7. Some varactors that were not explicitly reviewed have also been included here for the purpose of comparison [76-78].

2.3 Area-Tuned Varactors

The second method of tuning MEMS varactors is by actuating a change in the overlap area between the varactor electrodes. Larson et al. from Hughes Research Laboratories presented a conceptual micromachined area-tuned varactor in 1991 [14]. Using interdigital electrodes, a change in capacitance was demonstrated by manually moving the electrodes to vary the overlap area. Subsequently, Yao et al. from the Rockwell Science Center (RSC) reported the first area-tuned MEMS varactors [51, 79]. These varactors feature a suspended array of interdigitated comb fingers that is mechanically linked to a comb-drive actuator. The actuator varies the amount of overlap area in the interdigital varactor when biased. Several designs were fabricated with tuning ranges of around 100 to 200% and maximum actuation voltages as low as 5 V. The interdigitated comb-finger array was formed in deep-etched silicon and subsequently covered with an aluminium thin-film to reduce device series resistance. A Q-factor of 34 at 500 MHz was measured in a 5.19 pF device. Figure 2.11 shows the same varactor in different stages of tuning and its corresponding C-V characteristic.

One of the main advantages of the RSC varactors is the ease of fabrication: like the interdigital gap-tuned designs, only one or two masks are required. In addition, the actuators are isolated from the variable capacitor and hence do not affect the RF performance. The device capacitance values are also easily scalable and can be designed to either decrease or increase with actuator bias voltage. In a subsequent design, the RSC group reported another interdigital area-tuned varactor with a TR of 740% and a Q-factor greater than 100 (at 500 MHz) [80, 81]. The capacitance of this device varied from 1.4 to 11.9 pF with a maximum bias of 8 V.

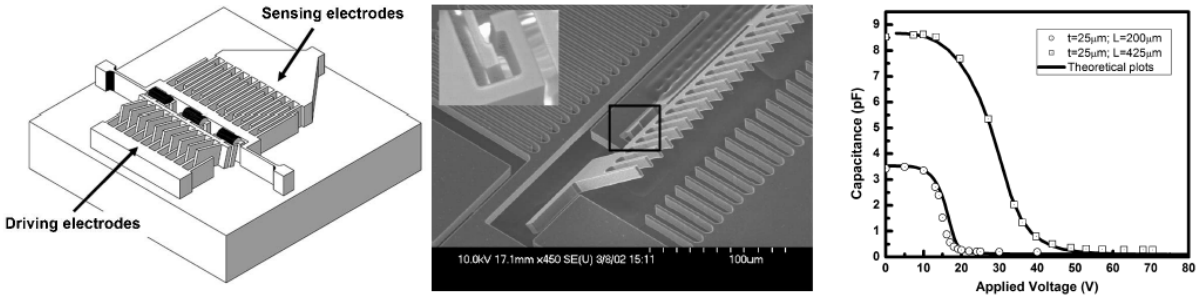


(a) (b)

Figure 2.11: RSC area-tuned interdigital varactor: (a) optical images showing change in finger overlap area with bias voltage; (b) *C*-*V* characteristic [51].

2.3.1 Rotational Varactors

Interdigital area-tuned varactors with lateral actuation share the same disadvantage as the interdigital gap-tuned varactors, i.e. they tend to have a larger device footprint. In order to obtain a large tuning range while keeping the device compact, Nguyen et al. from the University of California at Los Angeles (UCLA) implemented an area-tuned interdigital varactor with electrodes that rotate out-of-plane [19, 37]. The device consists of actuator and RF comb fingers connected via benzocyclobutene (BCB) hinges (see Figure 2.12). A surface tension self-assembly technique using BCB reflow creates an initial offset angle in the driving electrode, while the RF electrode has maximum overlap area at zero bias. When the driving electrode is actuated, the RF electrode rotates upwards, leading to a decrease in capacitance.



(a) (b) (c)

Figure 2.12: UCLA interdigital rotational varactor: (a) device schematic; (b) SEM image of drive and sense electrodes; (c) *C*-*V* characteristics of devices with different finger lengths [19].

A very large TR of 3085% (0.27 to 8.6 pF) was reported with a maximum actuation voltage of 50 V. By coating the silicon comb fingers with aluminium, a high Q-factor of 273 at 1 GHz was measured.

Recently, Gu and Li from the Shanghai Institute of Microsystem and Information Technology (SIMIT) reported an interdigital varactor with in-plane rotational actuation (see Figure 2.13) [82]. By designing the stiffness of the varactor in the radial direction to be much greater than the stiffness in the tangential direction, a key advantage of this design is its insensitivity to low frequency vibration. Although its sensitivity to vibration-induced noise has not been measured, simulated acceleration loads suggest that this design could be useful for reducing mechanical noise when implemented into a tunable circuit. The device is fabricated using a post-CMOS process and the comb electrodes are made of nickel and gold (10 μm and 200 nm respectively). A TR of 108% (0.13 to 0.27 pF) was measured for actuation voltages up to 12 V. The measured Q-factor is 51.3 at 1 GHz due to high parasitic inductance in the folded-beam suspension.

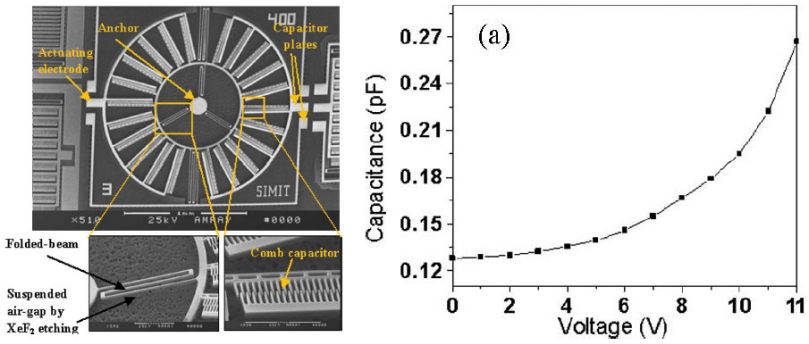
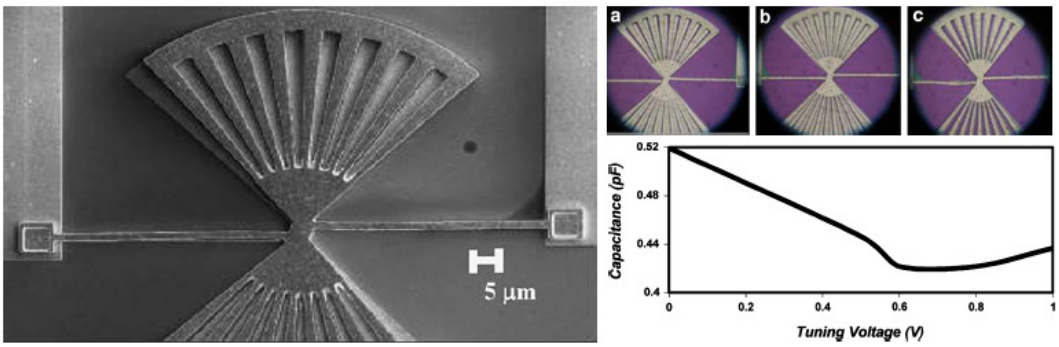


Figure 2.13: SIMIT rotational varactor: (a) SEM image; (b) C-V characteristic [82].

Another rotational varactor design has been proposed by Mehdaoui et al. from the Swiss Federal Institute of Technology at Lausanne (EPFL) [83]. Instead of interdigitated comb fingers, the movable and fixed electrodes consist of segmented regions that form an overlap area. Thermal actuators were used create an angular rotation, changing the capacitance area. Due to the mechanical design of the actuators, the TR was limited to only 30% as buckling occurred during testing. A similar varactor design was first proposed in [84] but no experimental results were reported in that paper. Figure 2.14 shows the thermally actuated rotational varactor in different stages of actuation.

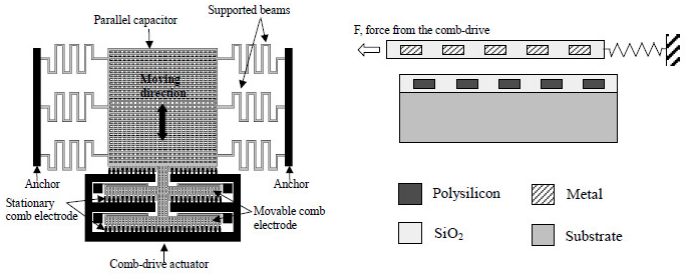


(a) (b)

Figure 2.14: EPFL segmented rotational varactor: (a) SEM image; (b) optical images showing various states of actuation (above), and C-V characteristic (below) [83].

2.3.2 Other Area-Tuned Varactors

A laterally-actuated varactor with segmented electrodes was reported by Dai et al. [85]. Using an electrostatic comb-drive actuator, a TR of 50% was measured. The low TR was probably due to the effect of fringing capacitances in each electrode segment. For this method of tuning to be effective, the varactor gap needs to be much smaller than the width of each segment and this may be difficult to implement. Figure 2.15 shows the design and tuning principle of this varactor.

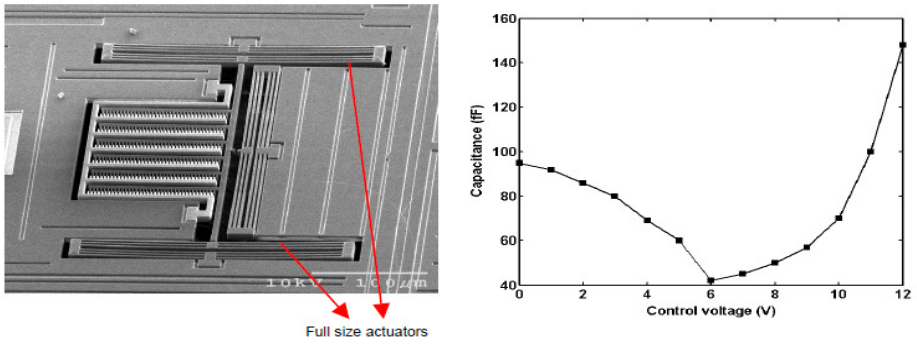


(a) (b)

Figure 2.15: Lateral segmented varactor: (a) varactor design; (b) tuning principle [85].

The first MEMS varactors fabricated using commercial CMOS processes were reported by Oz and Fedder from the Carnegie Mellon University (CMU) [86, 87]. Several thermally-actuated, area-tuned interdigital varactors were implemented. The best measured TR was 252% (0.042 to 0.148 pF) with a Q-factor of 52 at 1.5 GHz. A latching mechanism was included in the design as a means of reducing operating power requirements. However, the design of the latch only allows one capacitance value to be

held and hence a more complex latching mechanism is required for a continuously tunable varactor. Figure 2.16 shows the CMU varactor and its tuning characteristics.



(a) (b)

Figure 2.16: CMU thermally-actuated interdigital varactor: (a) SEM image [87]; (b) C-V characteristic [86].

Other area-tuned varactors with designs similar to the RSC varactor have also been reported [88, 89]. A summary of the performance parameters and design features of area-tuned varactors is given in Table 2.2.

2.4 Zipping Varactors

Electrostatic 'zipping' structures have been previously employed as actuators in a variety of applications [90-93]. These actuators, also known as 'touch-mode' actuators, usually feature a movable membrane or cantilever that generates a force and displacement. A larger displacement is possible relative to parallel-plate electrostatic actuators and hence they are attractive for implementing MEMS varactors with a large tuning range.

Zipping varactors were first reported by Hung and Senturia from the Massachusetts Institute of Technology (MIT) [94, 95]. In this design, a straight polysilicon cantilever is pulled down towards the bottom electrode by applying a bias voltage greater than the pull-in voltage. Upon contact, the geometry of this device resembles an 'S'-shaped fixed-fixed beam, with zipping occurring towards the anchor when the bias is increased (see Figure 2.17).

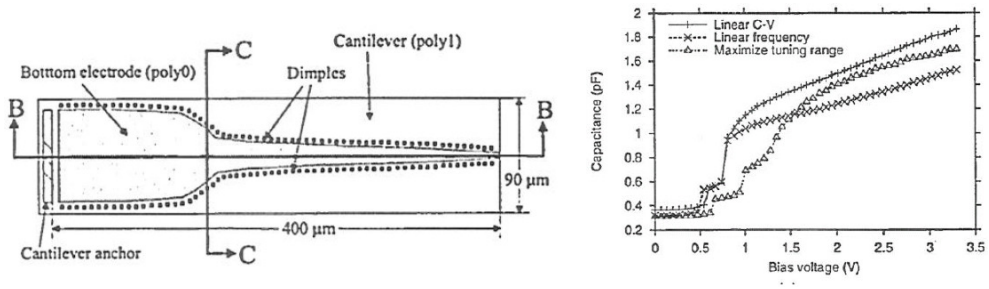
Since the effective beam length becomes shorter as it zips, the beam stiffness increases and stable zipping can be achieved with increasing bias voltage. To obtain linear C-V response, the width of the bottom fixed electrode is shaped using an

optimisation routine, resulting in a width function that increases the local electrostatic force towards the anchor.

(a) (b) (c)

Figure 2.17: MIT zipping varactor operation: (a) initial beam displacement; (b) cantilever pull-in; (c) zipping regime [94].

Figure 2.18 shows a bottom electrode with an optimised shape and the tuning performance of three zipping varactors. To eliminate stiction, no dielectric layer is present apart from air and contact between the beam and the bottom electrode is prevented by rigid dimples underneath the beam. These varactor prototypes were not optimised for RF performance and hence, only DC characterisation was performed. A TR of 77% (0.56 to 0.99 pF) was demonstrated in a device with eight zipping varactors connected in parallel.

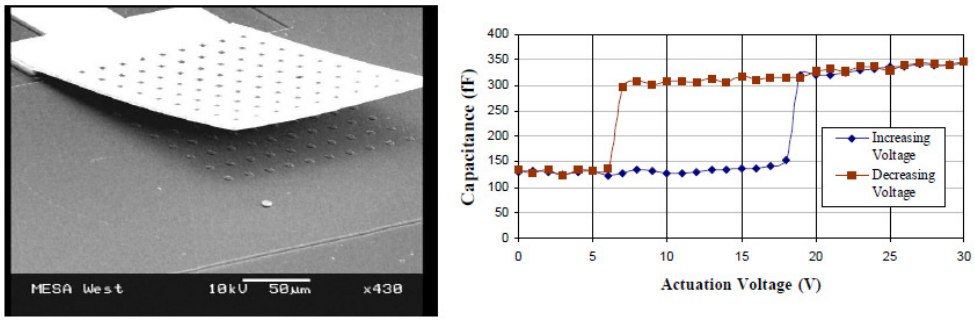


(a) (b)

Figure 2.18: MIT varactor: (a) optimised bottom electrode shape; (b) C-V characteristics of three different zipping varactors [94].

Other zipping varactors with a similar design to that in [94] have been fabricated [96-99]. Ionis et al. from Columbia University adapted the MIT zipping varactor design for a VCO operating at 1.5 GHz [96]. Both the MIT and the Columbia zipping varactors were fabricated using the MUMPs process, but the latter design has an additional gold layer on top of the cantilevers. However, the measured Q-factor of the Columbia device was only 6.5 at 1.5 GHz ($C_1 = 3.1$ pF) and its TR was 46%. In [97], a similar zipping cantilever was mounted over a spiral inductor to implement a tunable

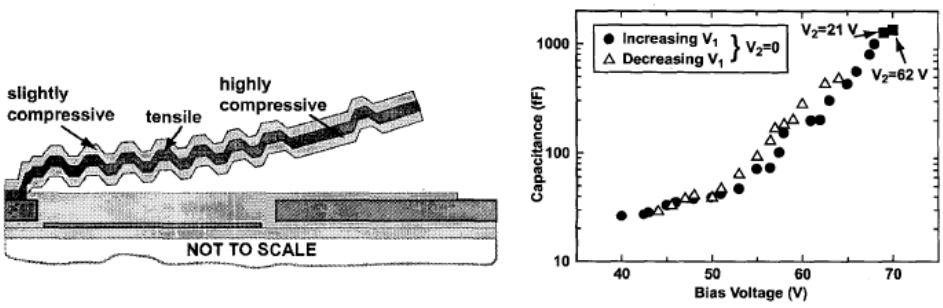
resonator. Subsequently, Nordquist et al. from Sandia National Laboratories reported a zipping varactor with a TR of 21% (0.29 to 0.35 pF) [98]. Using gold electrodes and a gallium arsenide substrate, a Q-factor greater than 100 was measured at 10 GHz. Nevertheless, due to the lack of optimised electrode shapes, this varactor had a large discontinuity in its C-V characteristic (see Figure 2.19) and was later implemented as a switched capacitor in a coplanar strip filter [99].



(a) (b)

Figure 2.19: Sandia varactor: (a) SEM image; (b) C-V characteristic [98].

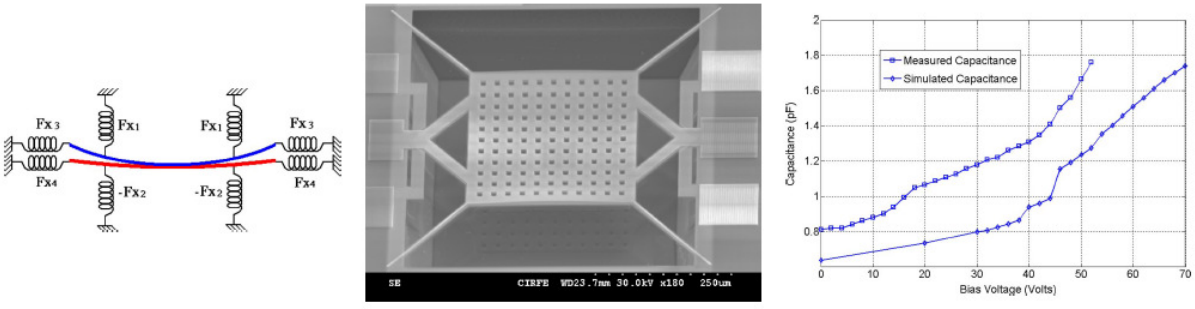
A zipping varactor with a curved cantilever electrode was reported by Muldavin et al. from MIT Lincoln Laboratory [100]. The device operates by zipping outwards, away from the cantilever anchor, unlike the above-mentioned zipping varactors (see Figure 2.20). Curvature in the top electrode was obtained using a stress-controlled tri-layer (SiO_2/Al/SiO_2) structure for the cantilever. Although a working TR of 600% (30 to 210 fF) was reported, no Q-factor measurement was available. For actuation, a bipolar square-wave signal was used to bias the varactor, possibly as a means of minimising stiction due to dielectric charging. This caused some modulation in the varactor, leading the authors to implement the varactors in a multi-bit configuration.



(a) (b)

Figure 2.20: Lincoln Lab varactor: (a) device schematic; (b) C-V characteristic [100].

Bakri-Kassem et al. from the University of Waterloo (UW) proposed a varactor design that consists of two movable plates [101]. The gold-coated nickel top plate resembles a conventional parallel-plate electrode suspended on suspension springs while the bottom plate is a polysilicon membrane with silicon nitride insulation. When a pull-in voltage is applied, the two plates collapse onto each other and then zip further as the bias is increased. Due to the initial instability, a large jump in capacitance occurs during pull-in. Subsequently, the authors reported an improved dual-zipping varactor where there is no initial gap between the two varactor plates and hence a smoother tuning characteristic [102]. This varactor consists of two curled plates (see Figure 2.21) suspended above an etched cavity in the silicon substrate. The varactor is fabricated using a commercial CMOS process and the device is released using a mask-less post-processing technique. The curvature of the top plate is designed to be larger than the bottom plate, allowing zipping to occur when a bias is applied. Tuning was demonstrated between 0.81 and 1.74 pF (115% TR) along with a Q-factor above 300 at 1.5 GHz. A third varactor design with two movable plates was reported by the same authors [103]. This varactor achieved a nearly linear, continuous C-V response with a TR of 500% (0.68 to 3.4 pF).



(a) (b) (c)

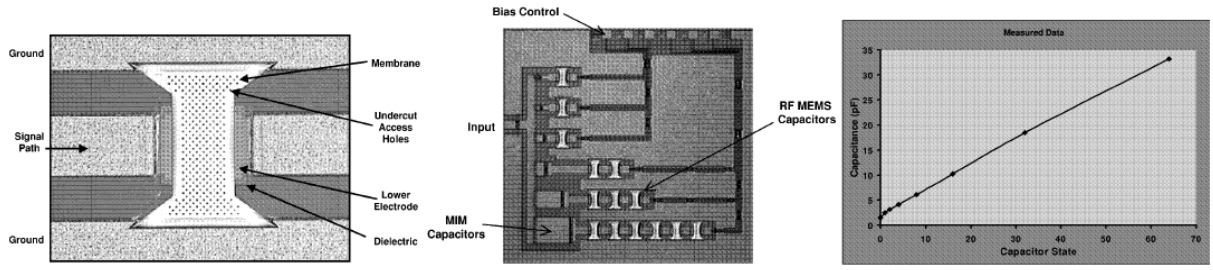
Figure 2.21: UW dual-zipping varactor: (a) device schematic; (b) SEM image; (c) model and prototype C-V characteristics [102].

The performance parameters and design features of zipping varactors are summarised in Table 2.3. For the purpose of comparison, the zipping varactor which forms the main subject of this thesis [104] is also included in the table. Varactors with a zipping cantilever [94, 96, 98, 100] are attractive for implementing high-TR varactors in a compact configuration. However, these zipping varactors need to be connected in parallel in order to scale up the device capacitance. Hence, the advantage of having a compact design is eliminated if larger capacitances are required. This is also true in

general for most MEMS varactors. By incorporating a high-permittivity dielectric into a zipping varactor, the capacitance of a zipping varactor can be scaled up without increasing the device footprint significantly. Further discussion on integrating a high-permittivity dielectric into a zipping varactor will be given in the subsequent chapters of this thesis. Another disadvantage of existing zipping varactor designs is that they are relatively complex [100-103], requiring many device layers in their process flow.

2.5 Digital MEMS Varactors

MEMS capacitive switches can be used as tunable capacitors by implementing a switched capacitor bank with several switches connected in parallel. These two-state switches can be addressed in suitable combinations to obtain different capacitances. Due to the step change in capacitance, such switch-array varactors are termed digital varactors. Goldsmith et al. from Raytheon Systems demonstrated a multi-bit varactor with a C_r of 22 (1.5 to 33.2 pF) using fourteen membrane switches [105]. Although the Q-factor of this varactor was only 20 at 1 GHz, the authors believe that this value could be significantly improved by optimising transmission line lengths and thicknesses. The Raytheon switched varactor and its tuning characteristic is shown in Figure 2.22.



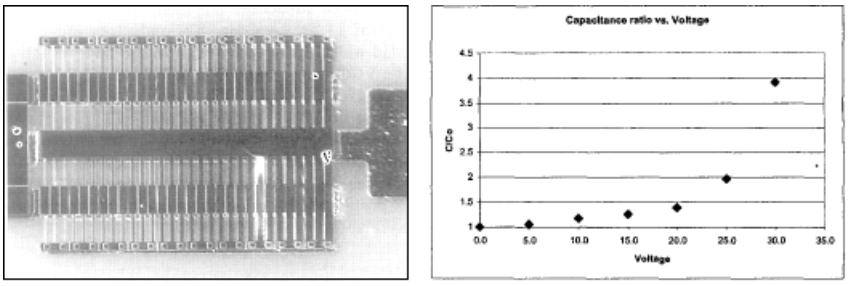
(a) (b) (c)

Figure 2.22: Raytheon digital MEMS varactor: (a) individual switch; (b) switch array topology; (c) discrete capacitance values [105].

The main advantage of using digital varactors is that it is highly scalable and can be designed for almost any required range of capacitances. However, the drawback is that it increases the device footprint, system complexity and could be more expensive to implement. In addition, only a finite number of capacitance values can be accessed as opposed to the entire range of values between the minimum and maximum

capacitance. Nevertheless, RF MEMS switch technology is more mature compared to micromachined varactors and could be a reliable means of implementing variable capacitors. Other digital varactors implemented using switch arrays have also been reported [100, 106-108].

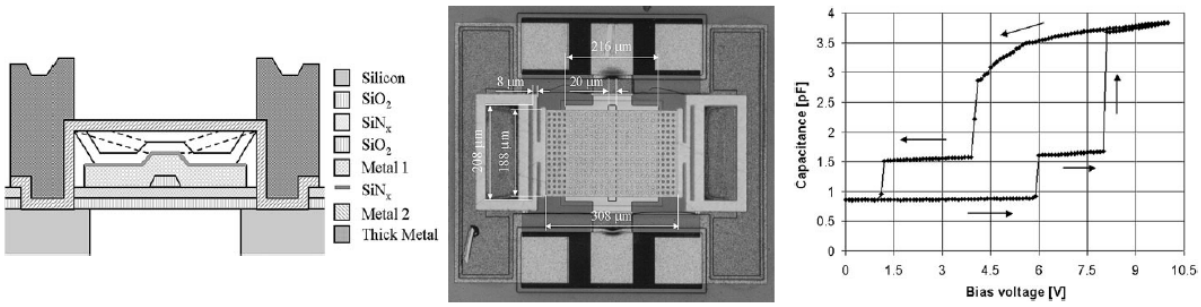
Apart from using individually addressed switches, certain digital varactor designs consist of switches that are biased simultaneously [109-111]. Each switch has a different mechanical stiffness and hence as the bias is ramped up, the switches are activated in a cascading manner. Such designs provide the advantage of a simpler and more compact layout. Hence, relative to switch arrays, less effort is needed for design optimisation in order to ensure a high varactor Q-factor. Figure 2.23 shows a cascading-switch varactor implemented by Hoivik et al. from CU Boulder along with its C-V characteristic [109]. A Q-factor of 140 at 750 MHz was reported for this device with tuning between 1 and 4 pF.



(a) (b)

Figure 2.23: CU Boulder cascading-switch varactor: (a) optical image; (b) C-V characteristic [109].

The third subset of digital varactors consists of individual devices with multiple stable capacitance states [58, 59, 100, 102, 112]. Such multi-state varactors could replace bi-stable switches in a switch array, extending tuning flexibility at the cost of increased device complexity. Nieminen et al. from Nokia Research Center reported a three-state varactor as shown in Figure 2.24 [58]. The first state is the capacitance when the varactor is unbiased (0.86 pF). The capacitances of the second and third states are 1.61 and 3.68 pF, respectively. By using gold electrodes and removing the substrate beneath the device, a high Q-factor of 94 at 2 GHz was measured for this device.



(a) (b) (c)

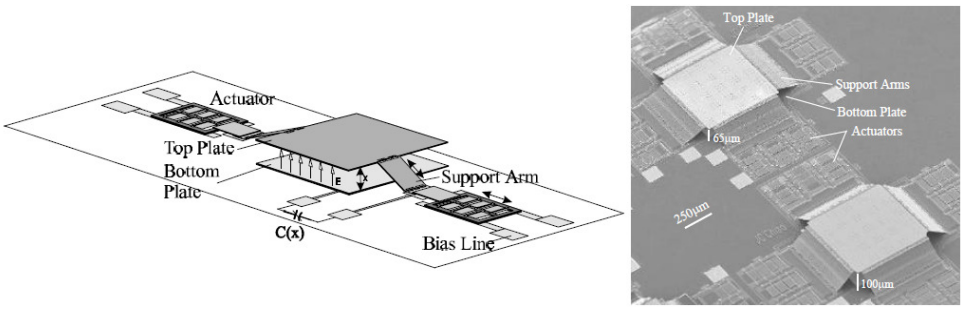
Figure 2.24: Nokia three-state varactor: (a) schematic cross-section; (b) fabricated device; (c) C-V characteristic [58].

A summary of digital varactor designs is given in Table 2.4 of the varactor library.

2.6 Other Micromachined Varactors

Several other MEMS varactor designs have been reported in the literature. These varactors introduce interesting design concepts that are less widely pursued but could be useful for future implementations of MEMS varactors. These varactors are briefly reviewed in this section.

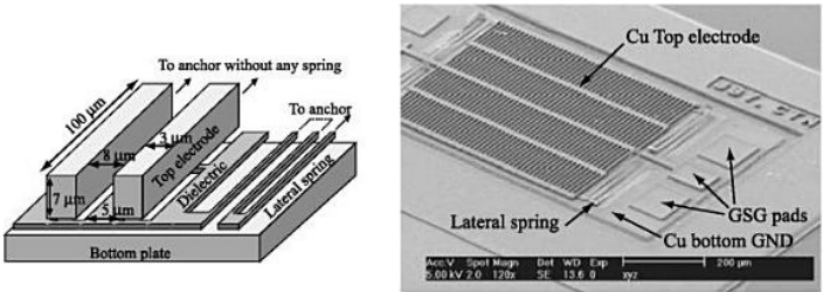
Chiao et al. introduced a novel gap-tuned varactor actuated by electrostatic scratch drives [84, 113]. The movable plate is connected to the actuators using a support mechanism that converts the lateral motion of the actuators into vertical motion in the varactor plate (see Figure 2.25). The support mechanism also allows large vertical displacements and potentially a very large tuning range. However, no RF measurements were reported.



(a) (b)

Figure 2.25: Scratch-drive actuated varactor: (a) operating principle; (b) SEM image [113].

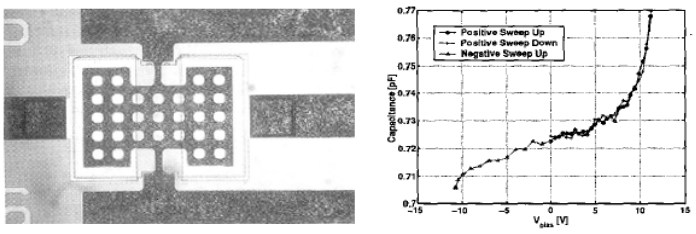
Yoon and Nguyen from the University of Michigan (UoM) introduced a varactor where the dielectric is movable instead of the capacitor electrode [114]. A silicon nitride dielectric is suspended on springs and electrostatically actuated to move between two electrodes (see Figure 2.26). This results in a change in the effective dielectric constant of the capacitor. Since the fixed electrodes do not need to be mechanically compliant, a thick copper layer is used in both the top and bottom electrodes (7 and 5 μm, respectively), yielding a very high device Q-factor. The measured Q-factor was 291 at 1 GHz for a nominal capacitance of 1.21 pF. However, the TR for this design is very low at only 8%, probably for the same reasons as the design in [85].



(a) (b)

Figure 2.26: UoM varactor with movable dielectric: (a) operating principle; (b) SEM image [114].

A varactor prototype where the movable electrode is suspended on torsion beams has been reported by De Coster et al. from the Catholic University of Leuven (KU Leuven) [115]. As shown in Figure 2.27, the varactor consists of two actuation electrodes on either side of a pair of torsion beams. The dual actuation allows an extended TR relative to the limit of 50% in the original parallel-plate design [18].

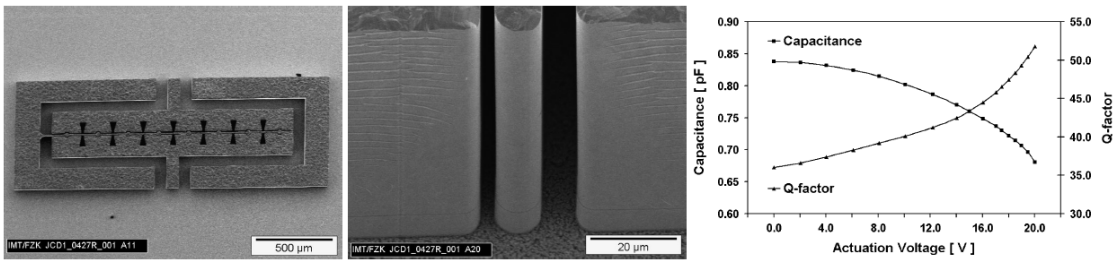


(a) (b)

Figure 2.27: KU Leuven torsion beam varactor: (a) microscope image; (b) C-V characteristic [115].

Another varactor based on this concept has been recently reported, achieving a TR of 147% [116].

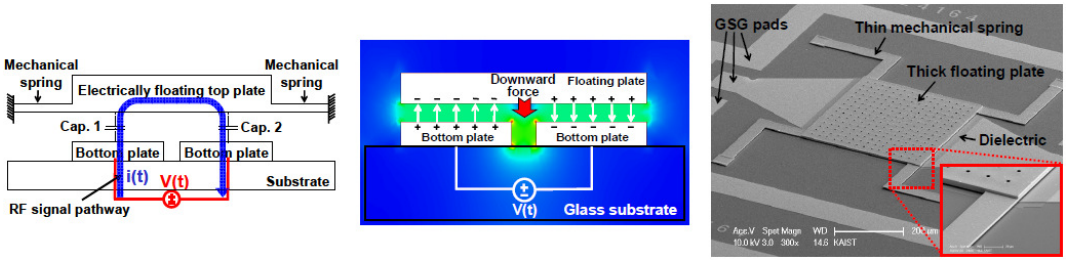
Klymyshyn and Haluzan from the University of Saskatchewan (U of S) fabricated a vertical cantilever varactor using high-aspect-ratio electroplated nickel structures [117]. The electroplating mould was defined using deep X-ray lithography and the fabricated varactor has a height of 100 μm with an air gap of 2.5 μm. This is the only lateral gap-tuned varactor that does not incorporate interdigital comb structures. However, the Q-factor of the device (51.8 at 4 GHz) is probably limited by the skin effect at higher frequencies. Hence, the use of very thick metal structures does not provide a significant advantage. Figure 2.28 shows the fabricated device, its C-V characteristic and the measured Q-factor.



(a) (b) (c)

Figure 2.28: U of S vertical varactor: (a) top view of fabricated device; (b) close-up view of cantilever tip; (c) measured C-V characteristic and Q-factor at 4 GHz [117].

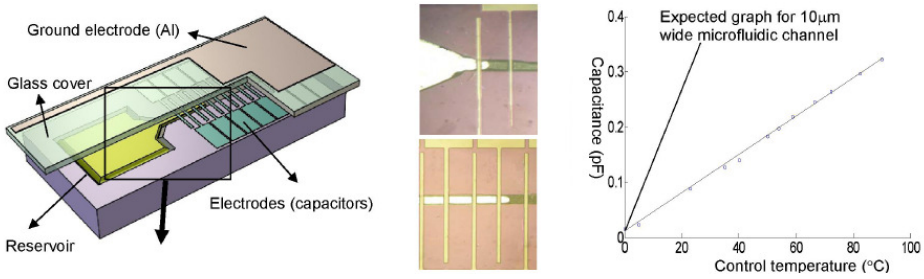
Recently, Lee et al. from Korea Advanced Institute of Science and Technology (KAIST) proposed a parallel-plate varactor design where there are two fixed electrodes and a movable top electrode plate (see Figure 2.29) [118]. Each fixed electrode forms a variable capacitor with the electrically floating top plate and hence the RF signal travels from one electrode to the other via the two capacitors in series. The device is actuated by applying a bias across the two bottom electrodes, leading to opposite induced charges in the regions of the movable plate directly above each electrode. Since the mechanical suspensions do not act as RF signal pathways, they can be designed to be thin and compliant while thicker layers are used for the floating plate and the bottom electrodes. Hence, this compact varactor design uses low actuation voltages while preserving a reasonable Q-factor value. A measured Q-factor of 34.9 at 5 GHz ($C_{\min} = 0.3$ pF) was reported along with a maximum bias voltage of 5.5 V. This design concept can potentially be combined with the dual-gap design to improve its tuning range (41% at present).



(a) (b) (c)

Figure 2.29: KAIST varactor with electrically floating plate: (a) device schematic; (b) simulated electrostatic field; (c) SEM image [118].

Pottigari and Kwon from the University of Missouri (MU) reported a unique microfluidic varactor [119]. The bottom electrode consists of liquid mercury that electrically connects an increasing number of capacitor plates as it flows through a micro-channel in the silicon substrate (see Figure 2.30). The mercury is initially stored within a reservoir and the varactor operates in a way similar to conventional liquid thermometers. Heating or cooling the reservoir moves the mercury in the channel one direction or the other. A glass cover with the patterned capacitor plates (titanium) seals the mercury in the reservoir and micro-channel. The cover also acts as the varactor dielectric and aluminium is deposited on top of the cover to form the top electrode. A very linear, digital-type capacitance-temperature characteristic was obtained in preliminary measurements and the device capacitance increased from 15 to 322 fF as the reservoir is heated from 0 to 90 °C. However, the tuning speed of this design is most likely orders of magnitude lower than electrostatically-actuated varactors. In addition, a mechanism for heating or cooling the reservoir must be integrated in the design before it can be used for practical purposes.



(a) (b) (c)

Figure 2.30: MU microfluidic varactor: (a) device schematic; (b) actual device showing mercury flow in the micro-channel; (c) capacitance-temperature characteristic [119].

2.7 RF MEMS Varactor Library

A review of the state of the art in MEMS varactor technology has been given in the preceding sections. The large variety of designs reported along with their associated advantages and disadvantages serves as a guide for choosing the right varactor in a given application. In the following tables, a summary of key design features and figures of merit from the varactors in this review is provided. The varactors are categorised according to their method of tuning and then listed chronologically in each table. Where possible, the data in the tables are reproduced directly from the references cited in the first column of each table. However, some data have been derived based on the information given by the authors. For example, the size of all the varactors includes the variable capacitor itself and its associated mechanical suspensions, actuators and anchors. It is less meaningful to quote the device footprint using the area of the capacitor alone as the actuating mechanisms are integral to the device performance and characteristics. In comparing Q-factor values from one varactor to another, it is important to bear in mind that the values are likely to have been reported for different capacitance values and operating frequencies. Therefore, it is better to convert the values into an equivalent series resistance before a crude comparison can be made. A dash (-) in the table indicates that the information is not available in the references.

Table 2.1: Gap-tuned MEMS varactors.

Varactor	Actuation	V_{max} [V]	Size [μm^2]	Electrode Geometry	C_1 [pF]	TR [%]	Dielectric	Movable Electrode	Stationary Electrode	Q-Factor	f_r [GHz]
Young [18], 1996	Electrostatic	5.5	690 x 690	Parallel-Plate	2.11	16	Air	Al	Al	62 (1 GHz)	-
Dec [52], 1998	Electrostatic	4.0	410 x 290	Parallel-Plate	2.05	50	Air	Au/Poly-Si	Poly-Si	20 (1 GHz)	> 6
Dec [52], 1998	Electrostatic	4.4	500 x 500	Three-Plate	3.4	87	Air	Poly-Si	Au/Poly-Si	15 (1 GHz)	6
Zou [56], 2000	Electrostatic	18	480 x 480	Dual-Gap	0.048	70	Air	Ni-Fe	Au	30 (5 GHz)	> 5
Harsh [75], 2000	Thermal	2.8	-	Parallel-Plate	0.5	600	Air	Au/Poly-Si	Au	100 (10 GHz)	> 14
Park [70], 2001	Piezoelectric	6	250 x 250	Parallel-Plate	0.1	210	Air	Au	Au	210 (1 GHz)	-
Nieminen [58], 2002	Electrostatic	17.7	610 x 310	Dual-Gap	1.58	125	Air	Au	Au	53 (2 GHz)	-
Dussopt [59], 2002	Electrostatic	25	400 x 400	Dual-Gap	0.082	46	Air	Au	Au	95 (34 GHz)	83
Tsang [60], 2003	Electrostatic	10	750 x 410	Dual-Gap	0.6	433	Air	Au/Poly-Si	Poly-Si	25–90 (2.4 GHz)	-
Peroulis [61], 2003	Electrostatic	22.5	1170 x 300	Dual-Gap	0.042	300	Air	Au	Au	> 80 (40 GHz)	>100
Xiao [66], 2003	Electrostatic	70	1900 x 1600	Interdigital	0.945	595	Air	Al/Si	Al/Si	100 (1 MHz)	-
Rijks [62], 2006	Electrostatic	30	500 x 500	Dual-Gap	0.23	350	Air	Al	Al	> 100 (4 GHz)	-
Fritschi [63], 2004	Electrostatic	8	725 x 325	Dual-Gap	3.5	190	Air	Al-1% Si	Al-1% Si	-	-
Kim [76], 2005	Electrostatic	37	600 x 400	Parallel Plate	0.030	33	Air	Au/Si	Au	-	-
Monajemi [67], 2005	Electrostatic	2	1500 x 1000	Interdigital	2.5	100	Air	Au/Si	Au/Poly-Si	49 (1 GHz)	> 10
McFeetors [64], 2006	Electrostatic	45	-	Dual-Gap	0.310	520	Air	Al-Mo	Au	50 (30 GHz)	-
Elshurafa [78], 2006	Electrostatic	9	1200 x 1200	Dual-Gap	3.56	240	Air	Au/Poly-Si	Poly-Si	3 (1 GHz)	4
Lee [71], 2006	Piezoelectric	35	3000 x 2100	Parallel-Plate	0.46	2080	Air	Al/Si	Al	10 (2 GHz)	-
Kawakubo [73], 2006	Piezoelectric	3	640 x 270	Parallel-Plate	0.010	100	Air	Al	W/Si	< 10 (2 GHz)	18
Dai [65], 2007	Electrostatic	21	400 x 400	Dual-Gap	1.38	85	Air	Al	Al	40 (0.1 GHz)	-
Konishi [54], 2007	Electrostatic	20	1720 x 1080	Three-Plate	2.5	1180	Air	Al	Al	-	-
Rais-Zadeh [68], 2007	Electrostatic	54	1000 x 900	Interdigital	0.68	129	Air	Ag	Ag	> 200 (1 GHz)	> 6
Fang [77], 2007	Electrostatic	12.8	970 x 610	Parallel-Plate	0.759	31	Air	Ni	Ni	51.6 (1 GHz)	> 10
Leidich [55], 2008	Electrostatic	100	1700 x 1700	Three-Plate	1.5	167	Air	Al/Si	Al	>100 (< 2 GHz)	4

Table 2.2: Area-tuned MEMS varactors.

Varactor	Actuation	V_{max} [V]	Size [μm^2]	Electrode Geometry	C_1 [pF]	TR [%]	Dielectric	Movable Electrode	Stationary Electrode	Q-Factor	f_r [GHz]
Yao [51, 79], 1998	Electrostatic	5	1800 x 1000	Interdigital	2.48	109	Air	Al/Si	Al/Si	34 (0.5 GHz)	5
Seok [88], 2002	Electrostatic	8	1130 x 1130	Interdigital	1.27	10	Air	Au/Si	Au/Si	4 (2 GHz)	> 4
Borwick [80, 81], 2003	Electrostatic	8	-	Interdigital	1.4	740	Air	Al/Si	Al/Si	> 100 (0.5 GHz)	> 3
Yalcinkaya [89], 2003	Electrostatic	3.15	1100 x 700	Interdigital	1	100	Air	Au/Si	Au/Si	10 (1 GHz)	4.1
Oz [86, 87], 2003	Thermal	12	250 x 228	Interdigital	0.042	252	Air	Al	Al	52 (1.5 GHz)	-
Nguyen [19], 2004	Electrostatic	50	1400 x 650	Interdigital	0.27	3085	Air	Al/Si	Al/Si	273 (1 GHz)	-
Dai [85], 2005	Electrostatic	20	900 x 730	Segmented	0.34	50	Air	Al/W	Poly-Si	-	-
Mehdaoui [83], 2007	Thermal	1.2	460 x 390	Segmented	0.42	30	Air	Al-4% Si	Al-1% Si	-	-
Gu [82], 2008	Electrostatic	12	1500 x 1500	Interdigital	0.13	108	Air	Ni/Au	Ni/Au	51.3 (1 GHz)	9.5

Table 2.3: Zipping varactors.

Varactor	Actuation	V_{max} [V]	Size [μm^2]	Electrode Geometry	C_1 [pF]	TR [%]	Dielectric	Movable Electrode	Stationary Electrode	Q-Factor	f_r [GHz]
Hung [94], 1998	Electrostatic	35	920 x 400	Cantilever	0.56	77	Air	Poly-Si	Poly-Si	-	-
Ionis [96], 2001	Electrostatic	35	1600 x 600	Cantilever	3.1	46	Air	Au/Poly-Si	Poly-Si	6.5 (1.5 GHz)	-
Nordquist [98], 2003	Electrostatic	30	360 x 300	Cantilever	0.29	21	Air/Si_2N_2O	Au	Au	> 100 (10 GHz)	> 50
Muldavin [100], 2004	Electrostatic	62	200 x 180	Curved Cantilever	0.03	600	Air/SiO_2	Al	Al	-	-
B.-Kassem [101], 2004	Electrostatic	39	1720 x 500	Dual-Zip	4.6	117	Air/Si_3N_4	Poly-Si	Ni/Au*	8.8 (1 GHz)	4.35
B.-Kassem [102], 2008	Electrostatic	70	820 x 820	Dual-Zip	0.81	115	Air/SiO_2	Al	Al*	300 (1.5 GHz)	> 20
B.-Kassem [103], 2009	Electrostatic	60	650 x 300	Dual-Zip	0.68	500	Air/Al_2O_3	Au/Poly-Si	Poly-Si*	29 (1 GHz)	20
Pu [104], 2009	Electrostatic	46	500 x 100	Curved Cantilever	0.092	400	Air/SiO_2	Au	Au	123–69 (2 GHz)	-

* Bottom electrode movable in these designs.

Table 2.4: Digital MEMS varactors.

Varactor	Actuation	V_{max} [V]	Size [μm^2]	Topology	C_1 [pF]	C_r	Dielectric	Movable Electrode	Stationary Electrode	Q-Factor	f_r [GHz]
Goldsmith [105], 1999	Electrostatic	55	2800 x 2800	Switch Array	1.5	22	Air/Si_3N_4	Al	W	20 (1 GHz)	∼4.4–1.9
Hoivik [109], 2001	Electrostatic	30	1000 x 500	Cascading Switches	1	4	Air/-	Au/Poly-Si	Au	140 (0.75 GHz)	-
Nieminen [58], 2002	Electrostatic	8.1	550 x 210	Multi-State Device	0.86	4.3	Air/Si_3N_4	Au	Au	94 (2 GHz)	-
Rizk [106], 2002	Electrostatic	30	1170 x 500	Switch Array	0.32	3.6	Air/Si_3N_4	Au	Au	-	> 3
Dussopt [59], 2002	Electrostatic	40	-	Multi-State Device	0.094	1.87	Air	Au	Au	-	-
Dussopt [107], 2003	Electrostatic	15	640 x 370	Switch Array	0.146	2.95	Air	Au	Au	10 (10 GHz)	36–25
Muldavin [100], 2004	Electrostatic	-	540 x 260	Switch Array	0.02	225	Air/SiO_2	Al	Al	-	-
Muldavin [100], 2004	Electrostatic	-	200 x 180	Multi-State Device	0.009	115	Air/SiO_2	Al	Al	-	-
Kannan [110], 2004	Electrostatic	35	750 x 500	Cascading Switches	0.62	15	Air/Si_3N_4	Au	Au/Ag	144 (1 GHz)	> 10
Luo [111], 2006	Electrostatic	25	390 x 210	Cascading Switches	1	1.7	Air/HfO_2	Ni	Al	-	-
Nishiyama [108], 2007	Electrostatic	56	3000 x 2700	Switch Array	0.2	37	Air/Si_3N_4	Al	Al	-	-
Han [112], 2007	Electrostatic	25	2800 x 1600	Multi-State Device	2.38	1.76	Air	Au/Si	Au/Si	24 (1 GHz)	-
B.-Kassem [102], 2008	Electrostatic	70	500 x 500	Multi-State Device	0.29	5.6	Air/SiO_2	Al	Al	300 (1.5 GHz)	20

Table 2.5: Other micromachined varactors.

Varactor	Actuation	V_{max} [V]	Size [μm^2]	Design Features	C_1 [pF]	TR [%]	Dielectric	Movable Electrode	Stationary Electrode	Q-Factor	f_r [GHz]
Chiao [84, 113], 1999	Electrostatic	-	3200 x 3200	Scratch-Drive Actuated	0.5	-	Air	Au/Poly-Si	Poly-Si	-	-
Yoon [114], 2000	Electrostatic	10	620 x 480	Movable Dielectric	1.21	8	Air/Si_3N_4	Cu[#]	Cu	291 (1 GHz)	19
De Coster [115], 2003	Electrostatic	12.4	440 x 140	Torsion Suspension	0.1	61	Air	Al	Al	-	-
Klymyshyn [117], 2007	Electrostatic	20	2000 x 700	Vertical Cantilever	0.68	24	Air	Ni	Ni	51.8 (4 GHz)	-
Lee [118], 2008	Electrostatic	5.5	780 x 780	Electrically Floating Plate	0.3	41	Air	Cu	Cu	34.9 (5 GHz)	> 10
Pottigari [119], 2008	Thermal	-	5600 x 3200	Microfluidic	0.015	2047	Glass	Ti/Hg	Al	-	-
Farinelli [116], 2008	Electrostatic	38	640 x 320	Torsion Suspension	0.314	147	Air	Au	-	-	-

[#] Both electrodes stationary

Chapter 3

Design and Simulation

The design considerations and modelled characteristics of a new micromachined zipping varactor are reported in this chapter. Zipping varactors offer the potential for achieving large tuning ranges in a compact design. Such varactors will be important for applications such as transceivers in mobile handsets, where a small device footprint is highly desirable. In addition, the incremental contact of the movable electrode with the dielectric when a zipping device is actuated makes it attractive for integration with high-permittivity dielectric materials.

Non-contact gap-tuned varactor designs, where a finite air gap exists between the dielectric and the movable electrode, cannot take advantage of high-permittivity materials unless the air gap is very small. In practice, this may be difficult to achieve since the air gap has to be on the order of the equivalent air thickness of the dielectric (defined as the dielectric thickness divided by the dielectric constant). As an example, if a conventional dual-gap varactor design (see [56]) is modified to include a dielectric with a relative permittivity of 100 and a thickness of 500 nm, its air gap needs to be tuned down to 5 nm otherwise the device capacitance will be dominated by the low-permittivity air gap. In addition, an extremely small electrode separation may also introduce dielectric breakdown issues if the electric field exceeds the dielectric strength.

The disadvantage of a zipping design with dielectric contact is that the long-term reliability may be reduced. A possible mode of failure could occur where the movable electrode becomes permanently attached to the dielectric surface and cannot be restored to its initial unbiased state. Such stiction induced failure could be caused by factors such as moisture adsorption, leading to hydrogen bridging; friction induced

electrostatic charging (tribocharging), among others [120, 121]. In the long term, these could be resolved by appropriate material selection and the use of hermetic packaging.

Other disadvantages include the possibility of dielectric charging (from the DC bias), resulting in hysteresis and tuning errors in the varactor. However, this could be resolved by using a bi-polar actuation voltage at the cost of increased device complexity. Reducing the bias voltage will also alleviate the problem of dielectric charging. Finally, the roughness of the contact surfaces will have an adverse effect on the device capacitance and tuning range since it would hinder the closure of the air gap. The effect of surface roughness on the on/off capacitance ratios of RF switches have been modelled in [48], and it was shown that if the dielectric permittivity is very high, a large capacitance ratio can still be obtained. Furthermore, rough surfaces are less susceptible to stiction and hence, a trade-off could be achieved between device performance and reliability.

In the following three sections, the concept of a new zipping varactor, its modelled electromechanical characteristics and RF performance will be presented.

3.1 Zipping Varactor Concept

Figure 3.1 shows an illustration of the proposed zipping varactor, which consists of a curved cantilever electrode and a fixed bottom electrode that is covered by an insulating dielectric. For controllable capacitance tuning, the cantilever is tapered such that its width increases linearly along its length [122]. This has the effect of increasing the local stiffness of the cantilever from the anchor towards the free end. When a bias voltage is applied, the region near to the anchor first comes into contact with the dielectric. The capacitance is then further tuned by increasing the bias voltage and allowing the cantilever to zip incrementally onto the dielectric surface. Conversely, if both the fixed and movable electrodes are of constant width, then the device will have a switch characteristic due to the pull-in instability [99, 123]. If the cantilever is not tapered, the curvature alone is insufficient to provide stable zipping and the entire cantilever is pulled down once the bias exceeds the pull-in voltage.

Gray et al. from Georgia Tech demonstrated zipping actuators where the electromechanical behaviour of the device was tailored by patterning the stressed layer of their bi-layered cantilever [124, 125]. Although the extended stable displacement of the movable electrode was demonstrated, their devices were designed as actuators

rather than varactors. As such, only DC capacitance measurements were performed and no RF experimental results were reported. The Lincoln Lab analog varactor uses two pull-down electrodes for tuning [100], whereas the proposed zipping varactor adopts a simple design with fewer device layers and only one actuating electrode.

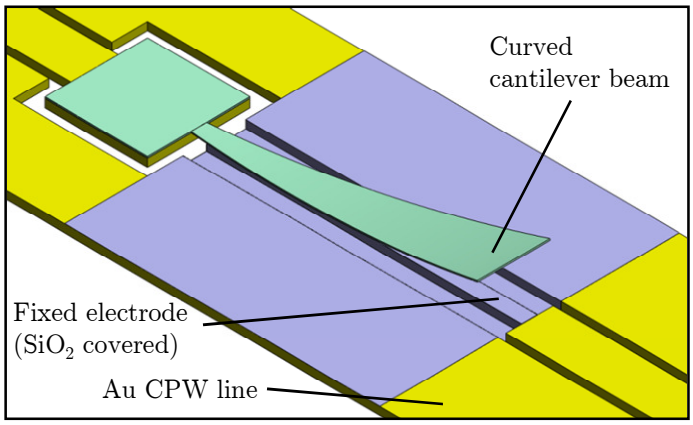


Figure 3.1: Zipping varactor illustration.

The length of the varactor (l) is between 200 to 400 μm and the minimum feature size of the device layout is 10 μm, i.e. the gap of the coplanar waveguide (CPW) transmission lines. A standard surface micromachining process can be adopted to fabricate the varactor prototypes and the details are described in the following chapter. To obtain the curvature in the cantilever, a composite structure is adopted consisting of chromium, copper and gold layers. The Cr/Cu layered is sputtered with residual tensile stress [126], while the relatively thicker gold layer has negligible stress. Upon release, the tensile stress creates a bending moment in the cantilever and curves it upwards. A schematic cross-section of the zipping varactor is given in Figure 3.2.

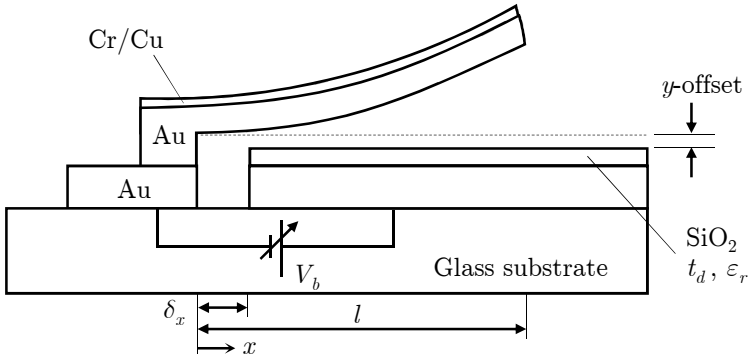


Figure 3.2: Schematic cross-section of device.

3.2 Electromechanical Modelling

Three electromechanical models have been constructed to predict the C-V characteristics of the proposed zipping varactor. The first model is a three-dimensional numerical model implemented in Coventor. Due to the excessive amount of time required to obtain solutions from the 3D model, alternative models are also proposed. The modelling results for a 400 μm long zipping varactor are discussed in detail in the following sub-sections.

3.2.1 3D FEM/BEM Model

The CoSolveEM module of Coventor 2008 allows coupled electromechanical modelling of MEMS structures. Figure 3.3 shows the 3D model of the zipping varactor, including the cantilever, the bottom electrode and dielectric. By exploiting the symmetry of the structure (in the z-plane, i.e. $z = 0$), the model complexity can be reduced and this shortens the simulation time. The cantilever is modelled as a bi-layered structure where the mechanical properties of the Cr/Cu (layer 2) is specified using a thickness-weighted average of the individual layers. A partition is made in the cantilever so that the designated contact surface is restricted to only the region that overlaps with the dielectric. This significantly reduces the computation time and results in a more efficient model. The detailed model parameters for the varactor are summarised in Table 3.1.

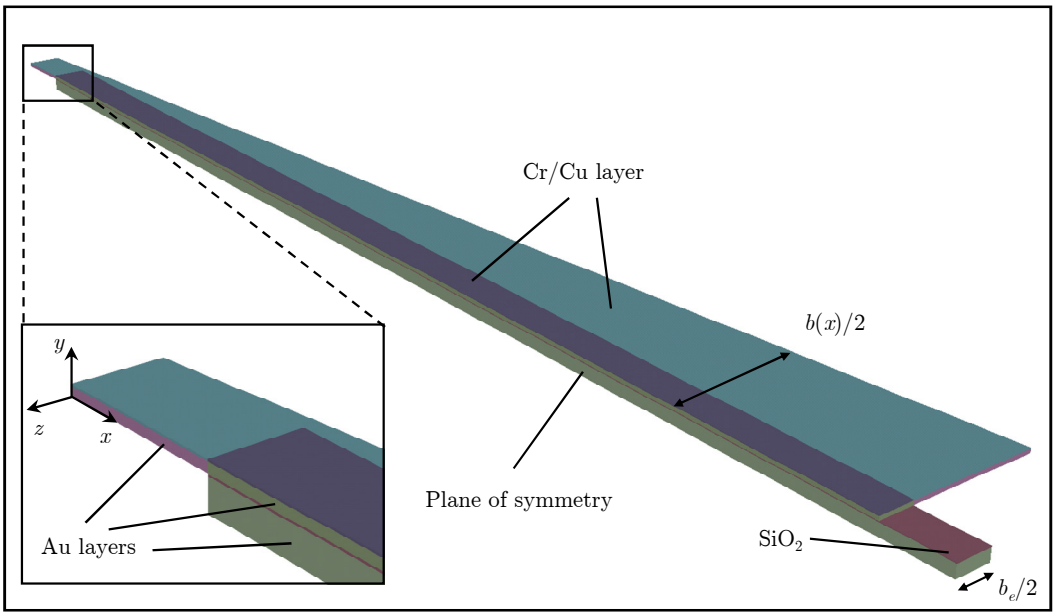


Figure 3.3: Coventor 3D varactor model with symmetry about the z-plane.

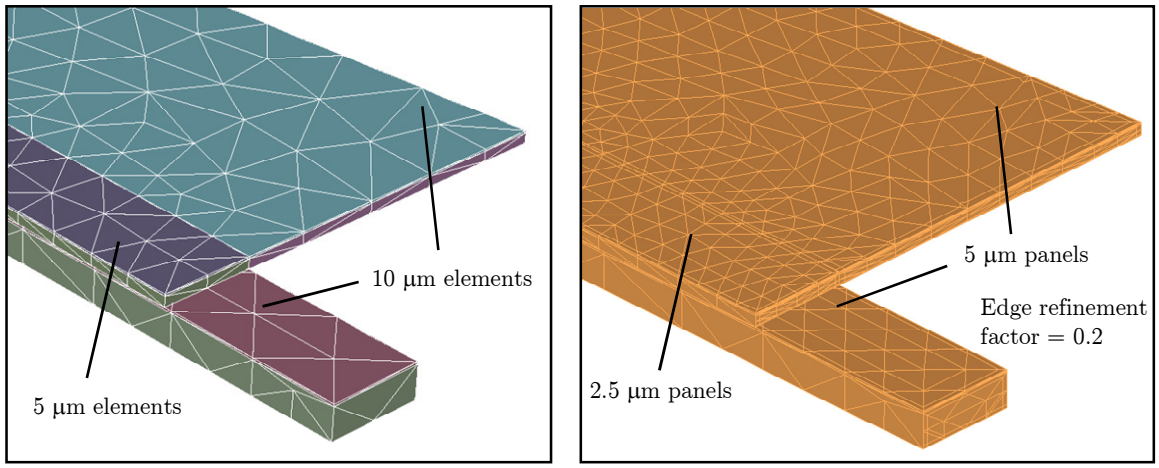
To simulate the voltage-controlled deflection of the varactor cantilever, a DC potential difference is applied across the cantilever and bottom electrode. The solver then determines the charge distribution and calculates the resulting electrostatic force on the cantilever. Next, the solution from the electrical domain is used to load the cantilever in the mechanical domain. With the cantilever anchor, bottom electrode and dielectric mechanically fixed, the solver determines the displaced profile of the cantilever due to the applied bias voltage. A number of iterations between the two domains are required before solution convergence is obtained. Convergence occurs when the change in nodal charge and displacement in two successive iterations is less than the pre-defined tolerance [127]. The convergence tolerance for this model is set at 0.001 pC and 0.001 μm for the electrical and mechanical domains, respectively. Once the solution for a particular voltage load is converged, the CoSolveEM solver moves to the next voltage value according to a specified trajectory.

Coventor's mechanical module uses the finite element method (FEM) to solve for the model's displacements. A tensile (positive) biaxial stress, σ_2 is applied in the Cr/Cu layer of the cantilever in the x- and z-directions. In the first load step, the solver determines the initial profile of the cantilever with no bias applied. Subsequently, a voltage is applied incrementally and the corresponding cantilever displacement (and capacitance) is calculated for each load step. Contact surfaces are also defined so that the displacement of the cantilever is constrained by the dielectric surface. The mechanical FEM mesh for the varactor is shown in Figure 3.4(a), where the tetrahedral elements have a second order quadratic shape function [128].

Table 3.1: Varactor model parameters.

Parameter	Value	Parameter	Value
Length, l	400 μm	Cantilever Au thickness, h_1	1.1 μm
Cantilever width, $b(x)$	$0.18x + 20$ μm	Cantilever Cr/Cu thickness, h_2	0.2 μm
Electrode width, b_e	20 μm	Young's modulus of Au, E_1	80 GPa
Electrode offset, δ_x	20 μm	Young's modulus of Cr/Cu, E_2	145 GPa
Thickness of SiO_2, t_d	0.23 μm	Poisson's ratio of Au, ν_1	0.42
SiO_2 permittivity, ε_r	4	Poisson's ratio of Cr/Cu, ν_2	0.325
Au conductivity, σ	4.1×10^{13} pS/μm	Initial biaxial stress in Cr/Cu, σ_2	167 MPa

For the electrical domain, the boundary element method (BEM) is used to solve for the charge distribution. Since the method requires only a surface mesh, the surfaces of the mechanical volume mesh are converted into panels for the electrical domain. A further refinement of the panels is applied at the model edges to account for charge accumulation at edges and corners [127]. The resulting BEM mesh is shown in Figure 3.4(b). For this model, the dielectric is lossless silicon dioxide with a relative permittivity of 4. The conductivity of the entire composite cantilever is defined using the conductivity of gold.



(a) (b)

Figure 3.4: Coventor mesh: (a) mechanical domain FEM mesh; (b) electrical domain BEM mesh.

Mesh convergence studies were performed to determine if the number of elements is sufficient for good accuracy. For the mechanical domain, the convergence criteria used were the initial maximum displacement (at zero bias) and the first resonant frequency of the cantilever. The FEM mesh convergence of the model is plotted in Figure 3.5, indicating that an element size of 20 µm is sufficiently refined for modelling the cantilever mechanics. Relative to the solution using 5 µm elements, the solution using 20 µm elements is within 0.3% and 1.6% for the initial maximum displacement and first resonant frequency, respectively. Note that for a given element size setting, the length of the element edges vary depending on location. This is due to the mesher algorithm and the constraints of the model geometry.

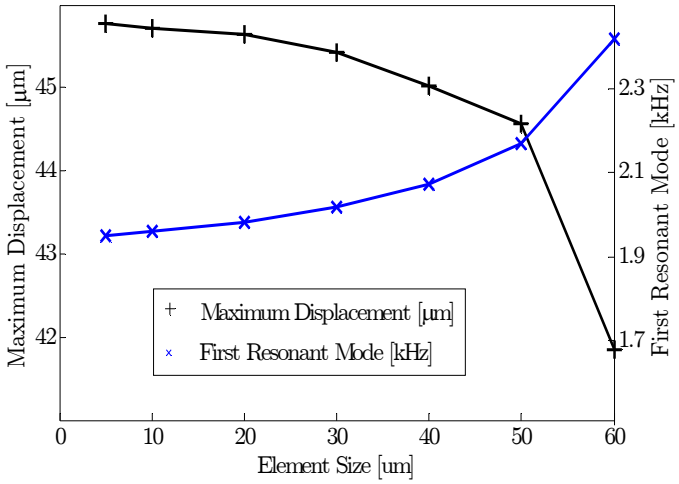
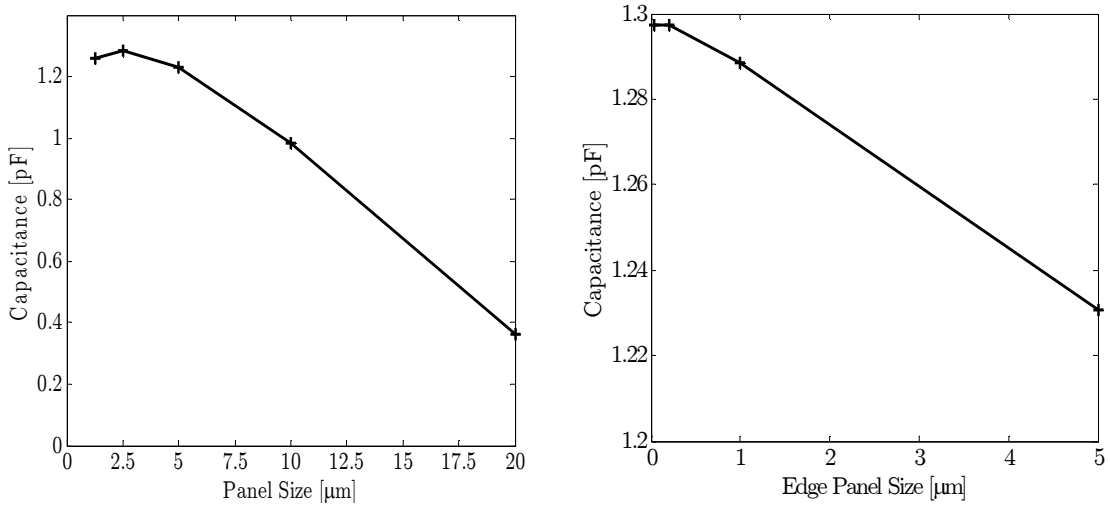


Figure 3.5: FEM mesh convergence.

For the electrical domain, a similar mesh trial was performed using a test model with capacitance being the convergence criterion. As shown in Figure 3.6(a), a panel size of 5 µm provides a solution that is within 2.3% of the solution obtained with a panel size of 1.25 µm. Additionally, the effect of refining the panels at the edges while keeping the global mesh size constant (5 µm) is shown in Figure 3.6(b). The computational cost of refining the edge elements by a factor of 0.2 (i.e. the edge panel size is one fifth the size of the global panels) is negligible but improves the solution accuracy further.



(a) (b)

Figure 3.6: BEM mesh convergence: (a) capacitance versus global panel size; (b) capacitance versus edge panel size (5 µm global panel size).

A preliminary electromechanical simulation using a 20 μm volume element size and a 5 μm panel size (with an edge refinement of 0.2) revealed that while the meshes were good for their respective domains, the coupled results were still inaccurate. This was deduced from the inconsistent and irregular C-V characteristic obtained. Further tests resulted in an optimised mesh for the coupled simulation where the mechanical elements are nominally 5 μm in the electrode overlap region and 10 μm elsewhere (see Figure 3.4). In the electrical domain, a refinement factor of 0.5 was applied resulting in a panel size of 2.5 μm in the electrode overlap region and 5 μm elsewhere. The solution irregularities were then eliminated and an accurate varactor C-V characteristic was obtained. The simulation results from this 3D model will be discussed in sub-section 3.2.4 along with the results from the 2D models.

3.2.2 2D Semi-Analytical Model

Although the 3D model is useful for providing an accurate simulation of varactor tuning behaviour, it is computationally expensive and extremely time consuming. Hence, it is difficult to make use of this model to rapidly evaluate different design variants. It would be useful if a simplified 2D model can be developed, providing reasonably accurate solutions but at a fraction of the time required for the 3D model solutions. In addition, if a closed form analytical expression for the deformed profile of the varactor can be found, further insight into the dependence of varactor tuning on various parameters is possible.

Initial Curvature of Cantilever

We begin by finding an expression for the curvature of the bi-layered cantilever due to the biaxial stress in the top layer. Figure 3.7 shows a cross-section of the cantilever, where layer 1 corresponds to the stress-free Au layer and layer 2 is the Cr/Cu layer with residual tension. Since the thickness of the cantilever is small relative to the other two dimensions, the cantilever is in a state of plane stress and the y-component of stresses is negligible.

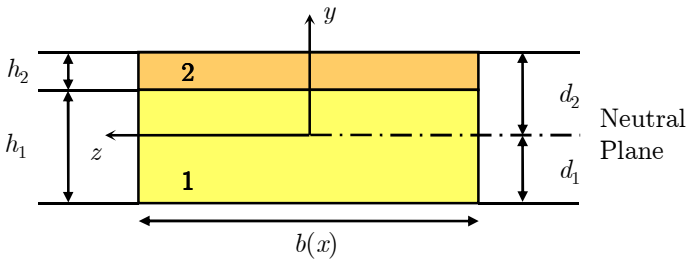


Figure 3.7: Cantilever cross-section at arbitrary x-location.

Using plate theory [129], the moment-curvature relationship for the composite cantilever can expressed as

$$\kappa = \frac{M}{\tilde{E}_1 I_1 + \tilde{E}_2 I_2} \tag{3.1}$$

where M is the bending moment acting in the x- and z-directions. $\tilde{E} = E\,/\,(1-\nu)$ is the biaxial modulus and I is the area moment of inertia about the neutral axis. The subscripts 1 and 2 correspond to the bottom and top layers, respectively. Since the thickness of the top layer is significant relative to the bottom layer, the exact position of the neutral plane (zero strain) is calculated using the following geometry parameters

$$\begin{aligned} d_1 &= \frac{E_1 {h_1}^2 + 2E_2 h_1 h_2 + E_2 {h_2}^2}{2\left(E_1 h_1 + E_2 h_2\right)} \\ d_2 &= h_1 + h_2 - d_1 \\ &= \frac{E_1 {h_1}^2 + 2E_1 h_1 h_2 + E_2 {h_2}^2}{2\left(E_1 h_1 + E_2 h_2\right)} \end{aligned} \tag{3.2}$$

The area moments of inertia about the neutral axis can then be expressed as

$$\begin{aligned} I_1 &= b\left(\frac{{h_1}^3}{3} - {h_1}^2 d_1 + h_1 {d_1}^2\right) = bI_1{}' \\ I_2 &= b\left(\frac{{h_2}^3}{3} - {h_2}^2 d_2 + h_2 {d_2}^2\right) = bI_2{}' \end{aligned} \tag{3.3}$$

where the primes denote the area moments of inertia per unit width.

Figure 3.8(a) shows the approximate stress distribution of the cantilever after fabrication and before release, where the tensile stress in layer 2 is assumed to be uniform across its thickness. After release, the net effect of biaxial relaxation can be estimated by satisfying the force balance condition of equilibrium. This is equivalent to imposing the condition that the average stress in the cantilever is zero.

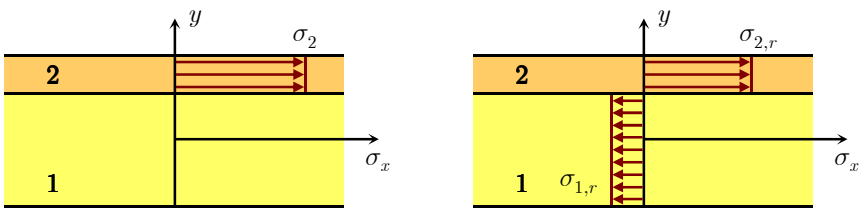


Figure 3.8: Cantilever stress in x-direction: (a) as deposited; (b) after relaxation but before bending.

The average biaxial contraction strain is then given by

$$\varepsilon_c = \frac{\sigma_2 h_2}{\tilde{E}_1 h_1 + \tilde{E}_2 h_2} \tag{3.4}$$

After relaxation, the stress in the bottom and top layers are

$$\begin{aligned} \sigma_{1,r} &= -\frac{\sigma_2 \tilde{E}_1 h_2}{\tilde{E}_1 h_1 + \tilde{E}_2 h_2} \\ \sigma_{2,r} &= \frac{\sigma_2 \tilde{E}_1 h_1}{\tilde{E}_1 h_1 + \tilde{E}_2 h_2} \end{aligned} \tag{3.5}$$

where the stress distribution is taken to be uniform in each of the layers (as shown in Figure 3.8(b)). Next, the effect of bending is accounted for in order to satisfy the moment balance condition of equilibrium. The bending moment can be calculated from

$$\begin{aligned} M &= \int_{-d_1}^{d_2-h_2} \sigma_{1,r} b y \, dy + \int_{d_2-h_2}^{d_2} \sigma_{2,r} b y \, dy \\ &= \frac{1}{2}\sigma_{1,r} b h_1 \left(d_2 - d_1 - h_2 \right) + \frac{1}{2}\sigma_{2,r} b h_2 \left(2d_2 - h_2 \right) \end{aligned} \tag{3.6}$$

If the initial contraction is neglected, then $\sigma_{1,r} \approx 0$, $\sigma_{2,r} \approx \sigma_2$ and the bending moment simplifies to

$$M = \frac{1}{2}\sigma_2 b h_2 \left(2d_2 - h_2 \right) \tag{3.7}$$

For small displacements, the bending equation of the cantilever can expressed as

$$\frac{\partial^2 s_r}{\partial x^2} \approx \kappa \tag{3.8}$$

where s_r is the displacement in the y-direction. Hence, the initial profile of the cantilever due to the stressed layer can be obtained by integrating (3.8) twice with respect to x and substituting the following boundary conditions for the built-in anchor

$$\begin{aligned} s_r(0) &= 0 \\ \left.\frac{\partial s_r}{\partial x}\right|_{x=0} &= 0 \end{aligned} \tag{3.9}$$

Neglecting the small initial contraction upon release, the released cantilever profile is then given by

$$s_r(x) = \frac{1}{2}\kappa x^2 = \frac{\sigma_2 h_2\left(2d_2 - h_2\right)}{4(\tilde{E}_1 I_1{}' + \tilde{E}_2 I_2{}')} x^2 \tag{3.10}$$

Electrostatic Loading

The electromechanical behaviour of the cantilever under an electrostatic load, can be modelled using an energy method based on the Principle of Virtual Work. For an elastic body, the principle states that under quasi-static equilibrium conditions, the sum of the work done by external forces on the body is equal to the increase in internal strain energy stored in the body in its deformed state [130, 131]. The principle can be expressed mathematically as follows

$$\int_S F_s \delta u \, dS + \int_V F_b \delta u \, dV = \int_V \delta W \, dV \tag{3.11}$$

where F_s and F_b are the external surface and body forces, respectively and δW represents the change in internal strain energy. δu is the virtual displacement field associated with the deformed state of the body, i.e. any small displacement satisfying the conditions of continuity for the material as well as the boundary conditions. The integral of the surface forces is taken over the surface S of the elastic body, while the integrals of the body forces and the strain energy are taken over its volume V. Additionally, the external forces are considered constant over a virtual displacement, and hence (3.11) can be re-written as

$$\delta\left[\int_V W \, dV - \int_S F_s u \, dS - \int_V F_b u \, dV\right] = 0 \tag{3.12}$$

where the terms in the brackets represent the total potential energy of the elastic system. From (3.12), we see that for a given set of external forces, the total potential

energy is stationary with respect to neighbouring admissible virtual displacements. In addition, it can be shown [131] that the total potential energy is a local minimum.

Figure 3.9 shows a schematic of the varactor cantilever in its original released state and two admissible trial functions for the cantilever profile when it is electrostatically actuated. Due to the offset between the cantilever anchor and the bottom electrode (δ_x), there is an initial gap between the cantilever and the dielectric. At low bias voltages, the cantilever deflects downwards without zipping onto the dielectric. Since the initial profile of the cantilever is parabolic, it is reasonable to use a parabolic trial function satisfying the boundary conditions (3.9). At higher bias voltages, the cantilever is in the zipping regime and a portion of the cantilever ($\delta_x \leqslant x \leqslant a$) is in contact with the dielectric. The remaining unzipped portion is modelled as a parabola. Hence, the trial functions for the deflected cantilever profile are

$$\tilde{s}_d(x) = mx^2 \tag{3.13}$$

when there is no zipping, and

$$\tilde{s}_d(x) = \begin{cases} 0 & 0 \leqslant x \leqslant a \\ c\big(x-a\big)^2 & a \leqslant x \leqslant l \end{cases} \tag{3.14}$$

when there is zipping.

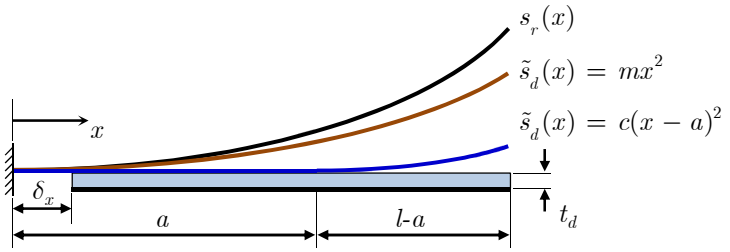


Figure 3.9: Cantilever profile after release and when deflected electrostatically.

The trial function for the displacement of the cantilever is then defined as

$$\tilde{v}(x) = s_r - \tilde{s}_d \tag{3.15}$$

Neglecting the effect of body forces, the total potential energy of the elastic system is given by

$$\begin{aligned} \Pi &= \int_V W\,dV - \int_S F_s u\,dS \\ &= W_m - U_e \end{aligned} \tag{3.16}$$

where W_m is the internal potential energy stored due to the cantilever deformation and U_e is the external work done by the electrostatic force. To determine the internal potential energy stored, we consider the strain energy of a plate in bending

$$W_m = \int\int \frac{1}{2} D \left\{ \left[\frac{\partial^2 \tilde{v}}{\partial x^2} \right]^2 + \left[\frac{\partial^2 \tilde{v}}{\partial z^2} \right]^2 + 2\nu \frac{\partial^2 \tilde{v}}{\partial x^2} \frac{\partial^2 \tilde{v}}{\partial z^2} \right\} dx\, dz \tag{3.17}$$

where

$$D = \frac{Eh^3}{12\left(1-\nu^2\right)} \tag{3.18}$$

is the flexural rigidity of the plate. For simplicity, the bi-layered structure of the cantilever is simplified into a single layered cantilever by using thickness-weighted average values for the Young's modulus and Poisson's ratio, i.e.

$$\begin{aligned} h &= h_1 + h_2 \\ E &= \frac{E_1 h_1 + E_2 h_2}{h} \\ \nu &= \frac{\nu_1 h_1 + \nu_2 h_2}{h} \end{aligned} \tag{3.19}$$

Using (3.17), the strain energy of the cantilever can then be expressed as

$$\begin{aligned} W_m &\approx \frac{1}{2} D \int_0^l \int_0^b \left[\frac{\partial^2 \tilde{v}}{\partial x^2} \right]^2 dx\, dz \\ &= \frac{Eh^3}{24\left(1-\nu^2\right)} \int_0^l b(x) \left[\frac{d^2 (s_r - \tilde{s}_d)}{dx^2} \right]^2 dx \end{aligned} \tag{3.20}$$

where the change in z-curvature under the electrostatic load is not taken into account. Hence, this expression neglects the contribution to the strain energy due to the change in curvature in the z-direction when a bias voltage is applied. The effect of dropping the z-terms will be discussed in the results section. In addition, the shear strain energy of bending has also been neglected since the cantilever is long and thin, i.e. shear strains are small relative to direct strains.

To find the external work done by the electrostatic force, we consider the force per unit length along the cantilever for a given bias voltage V_b and virtual displacement v

$$
\begin{aligned}
f_e(x) &= \frac{\varepsilon_0 b_e V_b^{\,2}}{2\left(t_e + s_d\right)^2} \\
&= \frac{\varepsilon_0 b_e V_b^{\,2}}{2\left(t_e + s_r - v\right)^2}
\end{aligned}
\tag{3.21}
$$

where b_e is the width of the actuating electrode, ε_0 is the permittivity of free space and t_e is the equivalent air thickness of the dielectric given by $t_e = t_d \,/\, \varepsilon_r$. This expression neglects the fringing electric fields. The external work done is then given by

$$
\begin{aligned}
U_e &= \int_{\delta_x}^{l} \int_0^{\tilde{v}} f_e \, dv \, dx \\
&= \int_{\delta_x}^{l} \frac{\varepsilon_0 b_e V_b^{\,2}}{2\left(t_e + \tilde{s}_d\right)} dx
\end{aligned}
\tag{3.22}
$$

where the surface integral is taken along the x-direction instead of along the cantilever curvature since the deflection is assumed to be small. This is consistent with the assumptions for classical plate theory.

Given that the total potential energy is stationary for a given bias voltage, the derivatives with respect to the cantilever profile parameters m, or a and c, are zero. Hence, we can solve for the deflected profile of the cantilever using

$$
\frac{d\Pi}{dm} = 0 \tag{3.23}
$$

when there is no zipping and using

$$
\frac{\partial \Pi}{\partial a} = 0 \quad \text{and} \quad \frac{\partial \Pi}{\partial c} = 0 \tag{3.24}
$$

when zipping has occurred. For the trial functions chosen, the resulting expressions were highly non-linear and hence no closed-form analytical solutions have been found. With the aid of the optimisation function **fsolve** in MATLAB R2007a (see Appendix A), the profile of the deflected cantilever is obtained and the capacitance is calculated as follows

$$C = \begin{cases} \displaystyle\int_{\delta_x}^{l} \frac{\varepsilon_0 b_e}{t_e + \frac{1}{2}\kappa x^2}\, dx & V_b = 0 \\ \displaystyle\int_{\delta_x}^{l} \frac{\varepsilon_0 b_e}{t_e + m x^2}\, dx & V_b > 0 \text{ , no zipping} \\ \displaystyle\frac{\left(a - \delta_x\right)\varepsilon_0 b_e}{t_e} + \int_{a}^{l} \frac{\varepsilon_0 b_e}{t_e + c\left(x - a\right)^2}\, dx & V_b > 0 \text{ , zipping} \end{cases} \tag{3.25}$$

This semi-analytical model provides a much faster tool for simulating the electromechanical behaviour of the zipping varactor. Relative to the 3D model, only a fraction of the time is required and hence it is useful for design purposes. The accuracy of the results depend in part on the choice of trial functions as well as the validity of assumptions such as the small deflection criterion and the negligible strain energy contribution of bending in the z-direction. In addition, the model is insensitive to the presence of instability in the C-V characteristic.

3.2.3 2D FEM Model with Equivalent Elastic Modulus

The third modelling approach is a hybrid finite element model that reduces the 3D geometry into 2D, by specifying an equivalent Young's modulus corresponding to the cantilever width at any axial position. The bending equations for the composite cantilever are

$$\begin{aligned} M_x{}' &= D_1\left[\kappa_x + \nu_1\kappa_z\right] + D_2\left[\kappa_x + \nu_2\kappa_z\right] \\ M_z{}' &= D_1\left[\kappa_z + \nu_1\kappa_x\right] + D_2\left[\kappa_z + \nu_2\kappa_x\right] \end{aligned} \tag{3.26}$$

where $M_x{}'$ and $M_z{}'$ are the bending moments per unit width in the x- and z-directions, respectively. κ_x and κ_z are the curvatures (due to electrostatic loading) in the two directions, and D_1 and D_2 are the flexural rigidities of the respective layers given by

$$\begin{aligned} D_1 &= \frac{E_1 I_1{}'}{1 - \nu_1{}^2} \\ D_2 &= \frac{E_2 I_2{}'}{1 - \nu_2{}^2} \end{aligned} \tag{3.27}$$

Dropping the z-terms from (3.26), we can then express the moment-curvature relationship for the cantilever as

$$\kappa_x \approx \frac{M_x}{b(x)\left(D_1 + D_2\right)} \tag{3.28}$$

We now consider a single-layered cantilever of unit width with a Young's modulus function $E_m(x)$. The moment-curvature relationship for this model cantilever is given by

$$\kappa_m = \frac{M_m}{E_m(x) I_m} = \frac{12 M_x}{E_m(x) {h_m}^3 b_e} \tag{3.29}$$

where h_m and I_m are the thickness and area moment of inertia of the model cantilever, respectively. The bending moment of the model is given by $M_m = M_x \,/\, b_e$, where the actual bending moment has been scaled using the width of the bottom electrode.

The requirement for the model is that for a given bending moment, its curvature must be the same as the actual bi-layered cantilever. When the varactor is actuated, the bending moment is due to the distributed electrostatic force between the cantilever and bottom electrode, and this force distribution is a function of the curvature. Hence, by equating (3.28) and (3.29) and imposing M_x to be identical for both cases, we can obtain an expression for $E_m(x)$

$$E_m(x) = \frac{12 b(x)\left(D_1 + D_2\right)}{{h_m}^3 b_e} \tag{3.30}$$

For simplicity, we take $h_m = h_1 + h_2$ although it is possible to use other values when implementing the finite element model. Figure 3.10 shows the model varactor geometry as implemented in ANSYS 11. The initial curved profile of the cantilever is estimated using equation (3.10) and the 2D structure is meshed using second order quadrilateral elements (PLANE183). The air gap, dielectric and electrostatic loading are modelled using 1D electro-mechanical transducer elements (TRANS126).

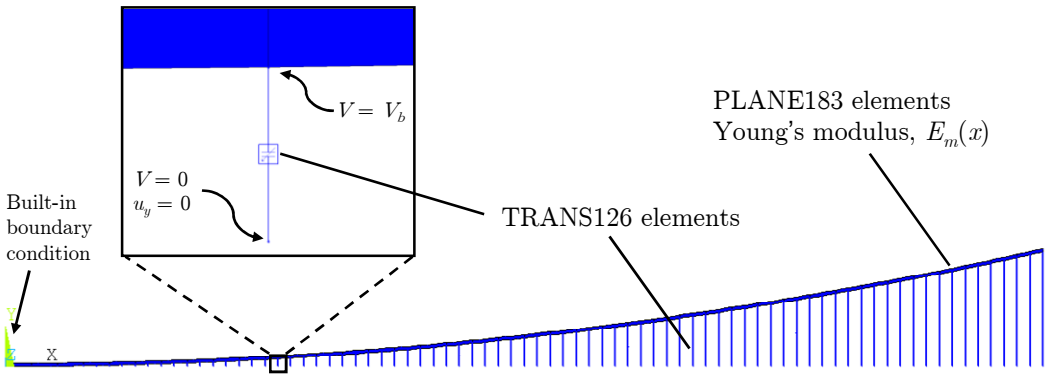


Figure 3.10: ANSYS 2D varactor model.

Each TRANS126 element has two nodes and two degrees of freedom at each node, namely voltage and vertical displacement [132]. The element behaves like a parallel-plate electrostatic actuator with its capacitive area, A determined by the structural elements that it is attached to. When a voltage is applied across the transducer elements, the electrical boundary condition is translated into a nodal force distribution on the cantilever. Figure 3.11 shows the force and capacitance of a TRANS126 element as a function of its stroke, u_y. The capacitance for each element is calculated from the function

$$c = \frac{c_0}{u_y} = \frac{A\varepsilon_0}{u_y} \tag{3.31}$$

and the remaining parameters c_1 to c_4 are 0.

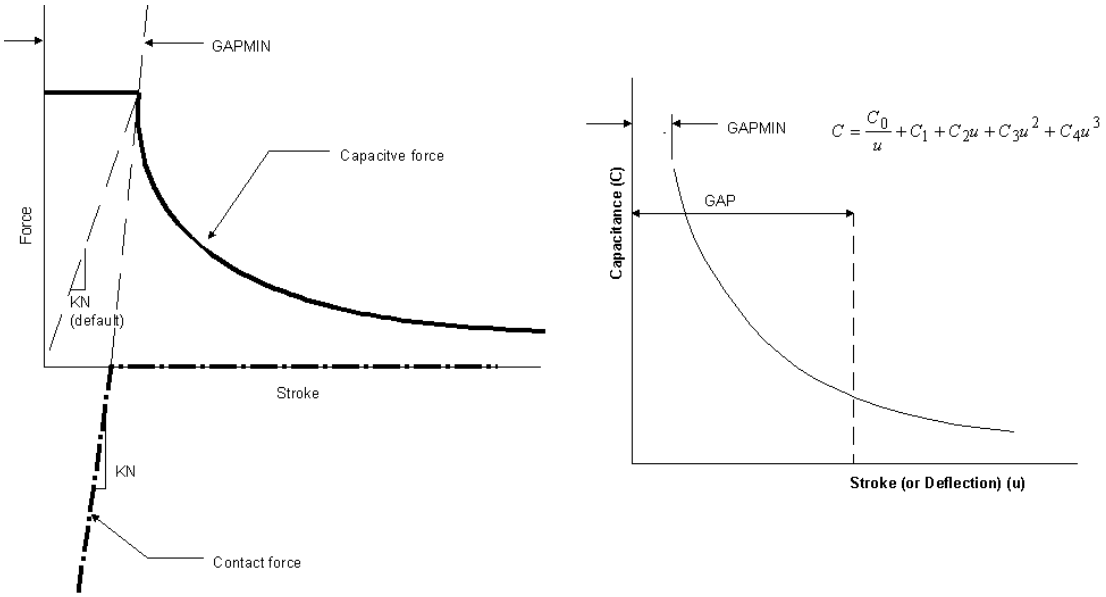
To prevent the capacitance, c from becoming infinite as the air gap closes, a minimum gap, equal to the equivalent air thickness of the SiO_2 dielectric, is defined for each TRANS126 element. When the element gap closes to t_e , it behaves like a contact surface and a normal contact stiffness specified using

$$k_n = \frac{E_d A}{t_d} \tag{3.32}$$

where E_d is the Young's modulus of the SiO_2 dielectric (70 GPa). Using TRANS126 elements result in a physically thinner dielectric and a slightly larger air gap. However, the error introduced is expected to be small since the average air gap is much larger than the dielectric thickness in an actual device. A convergence study revealed that a mesh with 160 structural elements along the length of a 400 μm cantilever (i.e. 2.5 μm

element size) is sufficiently refined. Only one element is required across the thickness of the cantilever.

In comparison with the Coventor model, the solution procedure for this hybrid model is straightforward since there is no need to iterate between the mechanical and electrical domains. Hence, it is easier for the solver to find a converged solution. In addition, the total number of degrees of freedom is substantially lower than the 3D model, yielding faster solution times. The ANSYS Parametric Design Language (APDL) code for this model is listed in Appendix B.



(a) (b)

Figure 3.11: ANSYS TRANS126 element properties: (a) force versus stroke; (b) capacitance versus stroke [133].

3.2.4 Simulation Results

Electromechanical Modelling

The simulated C-V characteristic of the zipping varactor listed in Table 3.1 is shown in Figure 3.12. For the purpose of comparison, the Coventor model is taken to be the most accurate solution. Results from the 3D model show that between 0 and 10.5 V, the capacitance increases only slightly from 33 to 39 fF. At 11 V, there is instability in the varactor tuning, and the capacitance jumps to 451 fF. This instability is due to the initial gap separating the cantilever and the dielectric surface and a step change in capacitance occurs when the cantilever first comes into contact with the dielectric.

Thereafter, the varactor operates in the zipping mode and the capacitance increases in a continuous manner as the contact area of the cantilever and the dielectric increases. Beyond 13 V, the capacitance continues to increase but with a much smaller gradient. When the bias voltage is subsequently reduced, there is little or no tuning hysteresis in the stable region (13 to 18 V). In addition, the continuous tuning range is larger and the capacitance can be tuned from 1000 fF down to 149 fF between 18 and 8.5 V.

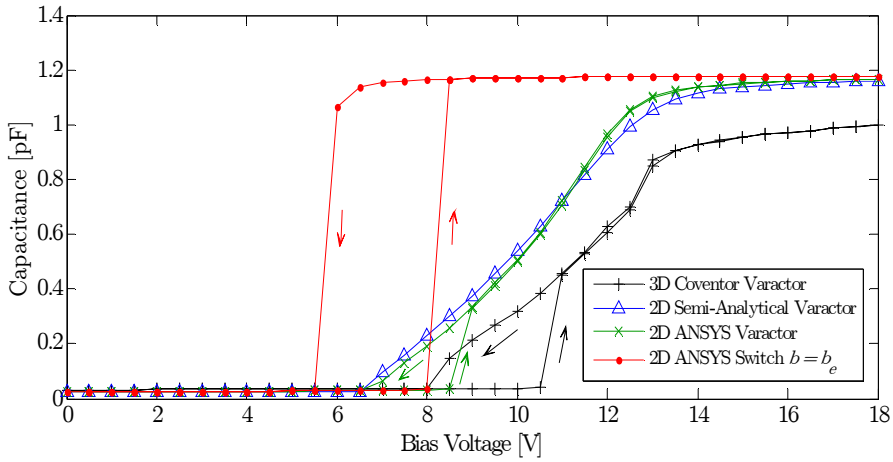


Figure 3.12: Zipping varactor simulation results.

The Coventor results show that this zipping varactor design has the potential for achieving a very large and continuous tuning range. Provided the cantilever is not unloaded fully and is kept in the zipping regime, the capacitance can tuned continuously between 8.5 and 18 V. This is confirmed by running an additional 3D simulation where the bias is first decreased from 11 to 8.5 V and then subsequently increased to 11 V. The simulation demonstrated repeatable capacitance for any given bias voltage, indicating stable zipping behaviour. This shows that the tuning hysteresis only occurs because of the initial pull-in instability and can be avoided by using the varactor in its stable operating range. In practice, some hysteresis will be present even in the stable zipping regime due to stiction, and some design optimisation may be required to address this.

The results from the two 2D models demonstrate good agreement and the ANSYS model shows a similar tuning behaviour relative to the Coventor model. However, the instability in the ANSYS model occurs at a lower voltage of 9 V indicating that the model stiffness is underestimated. The solution for the semi-analytical model depends largely on the choice of trial functions for the deflected cantilever profile. Between 7 and 9 V, the zipping trial function for the cantilever profile is used instead of the non-

zipping one. Hence, the solution coincides with the ANSYS model for decreasing bias voltages. This also indicates that the choice of parabolic trial functions is appropriate.

The lower stiffness in the 2D models is a consequence of dropping the z-components of the bending moment and curvature in favour of model simplicity. Differences in tuning behaviour relative to the 3D model could also be a result of neglecting the fringing fields in the 2D models. Another effect of modelling the varactor in 2D is that the device capacitance is overestimated as the models assume perfect contact between the cantilever and dielectric. The 3D model preserves the effect of the z-curvature due to the biaxial stress in the top layer of the cantilever, resulting in a lower capacitance. All three models show that tailoring the stiffness of the cantilever using a linear width function enables stable zipping and a large tuning range. In contrast, the C-V characteristic of a device with uniform width is modelled in ANSYS and plotted in Figure 3.12, demonstrating switching behaviour.

The main advantage of the 2D models is that they allow rapid evaluation of design alternatives since their computational requirements are significantly lower than the 3D model. Table 3.2 summarises the model complexity and time required to obtain the results shown in Figure 3.12. All of the simulations were performed on standard personal computers and the mesh for the Coventor and ANSYS models compared here are the optimum meshes in terms of solution accuracy and computational cost.

Table 3.2: Model complexity and solution time.

Model	Mesh	Solution Time
Coventor 3D	5687 10-node FEM elements, 14310 BEM panels	$>$ 26 hours
Semi-Analytical 2D	1 or 2 trial function parameters	$<$ 1 minute
ANSYS 2D	160 8-node FEM elements, 305 TRANS126 elements	$<$ 10 minutes

To improve the accuracy of the 2D models, the effect of the transverse curvature on the capacitance can be estimated using an effective dielectric constant. The capacitance of the semi-analytical and ANSYS models at 18 V is larger than the Coventor value by a factor of 1.15. Hence, by using a dielectric constant of 3.5 instead of 4, the results from the 2D models are then in better agreement with the 3D solution (see Figure 3.13). In the design process, an efficient strategy would be to obtain accurate 3D solutions at a few voltage points and then work out an effective dielectric constant value based on corresponding 2D solutions at the same voltage points.

Finally, either of the 2D models can then be used to evaluate the tuning characteristics of various design options. When a particular design has been chosen, the 3D model can be used to obtain accurate C-V results, and hence verify that the device provides the required tuning behaviour.

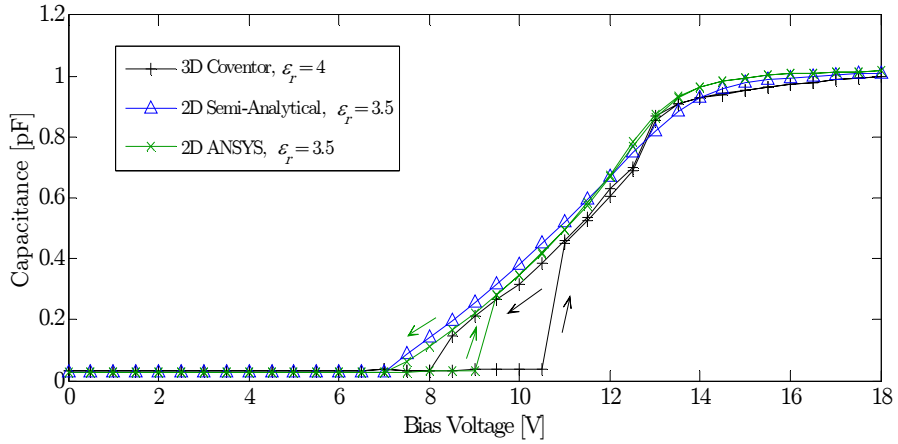


Figure 3.13: Simulation results using an effective ε_r for the 2D models.

The deflected profile of the cantilever has been extracted from the 3D model using data points on the bottom surface of the cantilever. The x-y (axial) profiles are shown in Figure 3.14 at several bias voltages. After release, the initial end height of the cantilever at 0 V is 47.1 μm. In comparison, the end height is 44.0 μm using the plate theory equation (3.10). It can be observed from the axial profile plot that when the bias was increased between 0 and 10 V, the cantilever deflects downwards slightly without zipping. This corresponds to the small increase in capacitance for this bias range. At 13 V, the cantilever is approximately fully zipped in the x-direction. Hence, the subsequent increase in capacitance is mainly due to zipping in the z-direction.

When the bias voltage is subsequently decreased, a larger range of zipping profiles is now accessible as shown by the plots for 9 and 10 V. The y-z (transverse) profiles for the cantilever at $x = l/2$ are shown in Figure 3.15 (increasing bias). By fitting a parabolic function of the form $y = \alpha_1(z + \alpha_2)^2 + \alpha_3$, the z-curvature of the cantilever can be compared for different bias values using the parameter α_1. The value of α_1 is listed in Table 3.3 for different bias voltages. It is observed that as the cantilever unfolds downwards in the x-direction from 0 to 13 V, its curvature increases upwards in the z-direction (at $x = l/2$). Once the cantilever is approximately fully-zipped in the x-direction, it begins to bend downwards in the z-direction. This additional zipping in the z-direction between 13 and 18 V contributes to a further increase in capacitance.

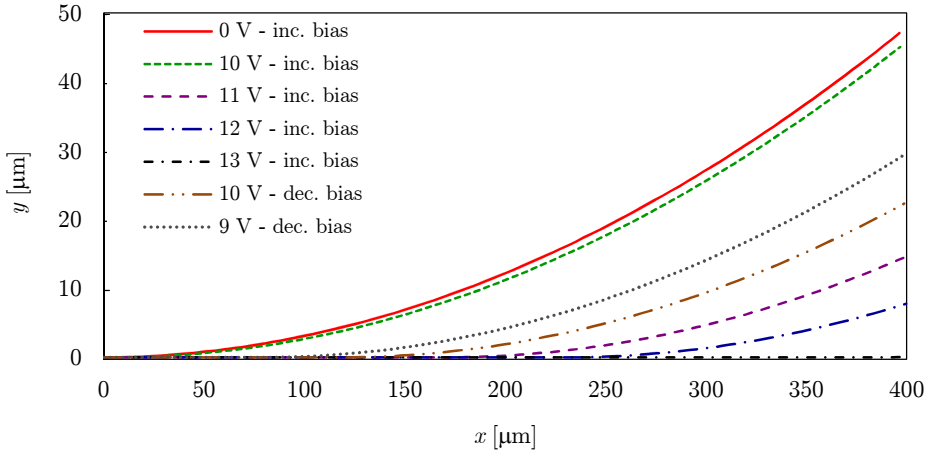


Figure 3.14: Cantilever axial profile in the plane of symmetry ($z = 0$).

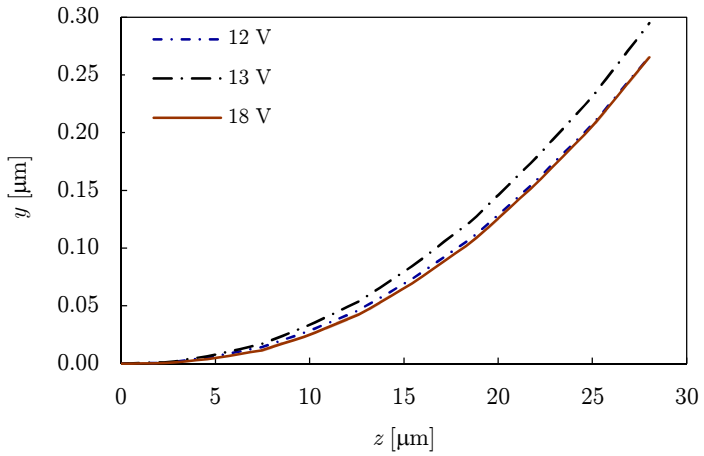
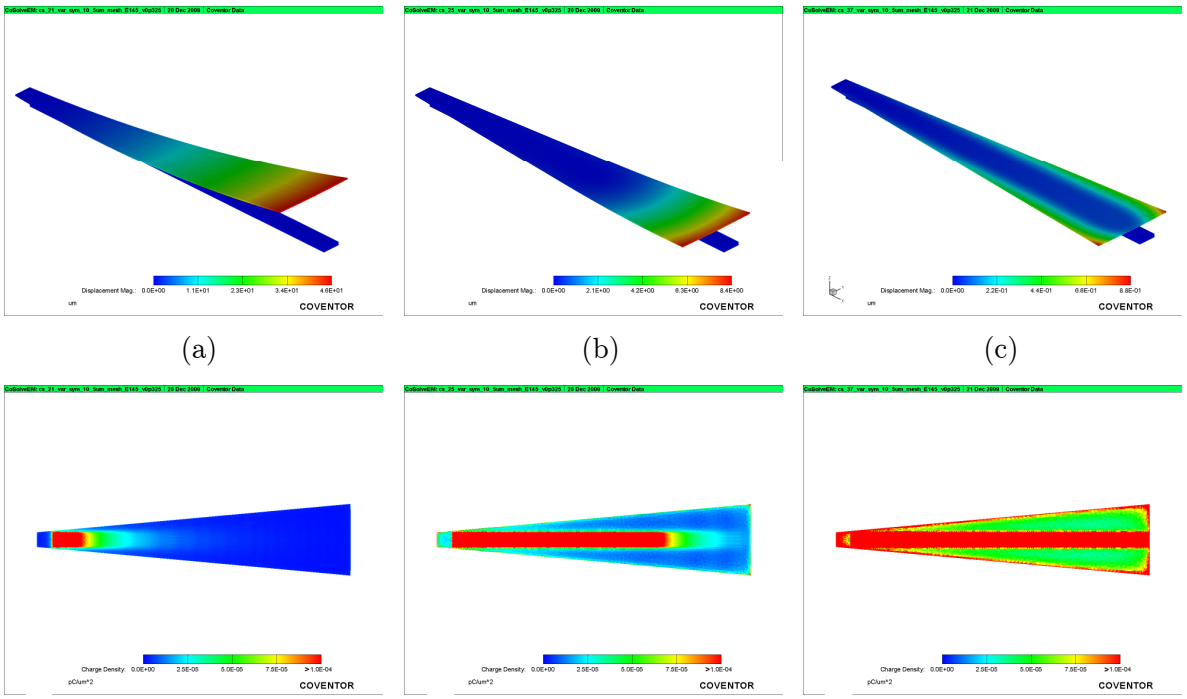


Figure 3.15: Cantilever transverse profile at $x = l/2$ for increasing bias.

Table 3.3: Variation of z-curvature with bias voltage.

Bias Voltage [V]	α_1 [µm^{-1}]
0	2.87×10^{-4}
10	2.88×10^{-4}
11	3.06×10^{-4}
12	3.77×10^{-4}
13	4.03×10^{-4}
18	3.97×10^{-4}

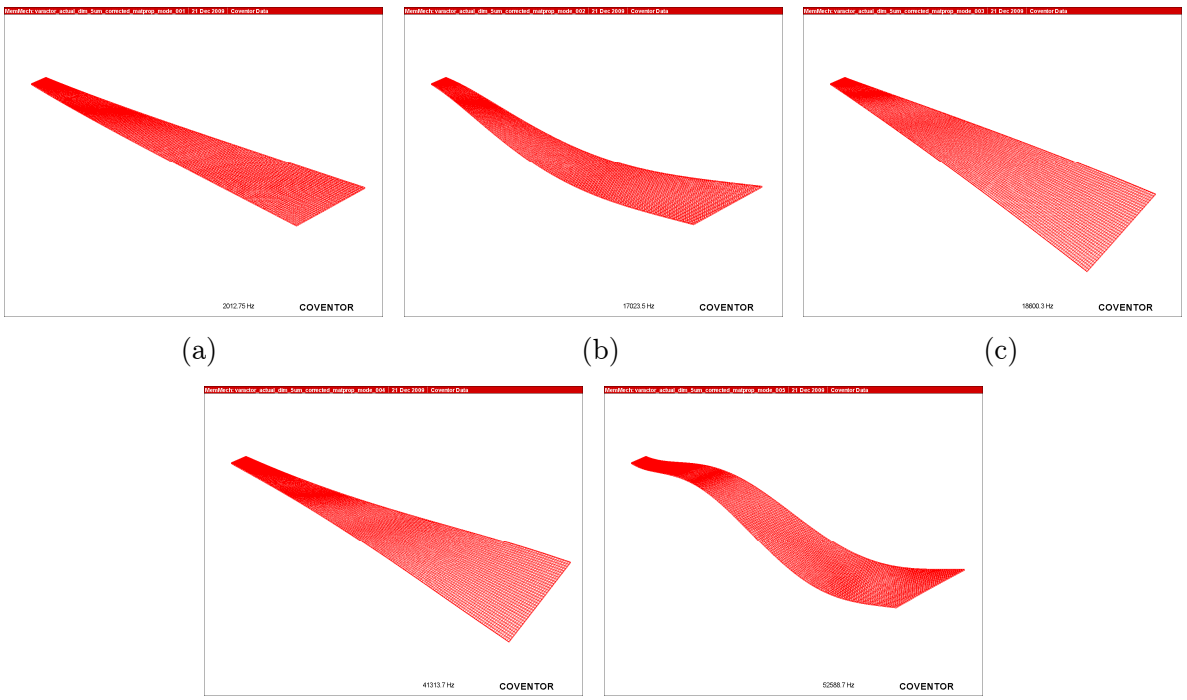
The deflection of the zipping varactor and the corresponding charge density on the cantilever is shown in Figure 3.16 for 10, 12 and 18 V when the bias is increased.



(a) (b) (c)

(d) (e) (f)

Figure 3.16: Cantilever deflection (top) and charge density (bottom) for 10 V (a, d), 12 V (b, e) and 18 V (c, f) when the bias is increased.



(a) (b) (c)

(d) (e)

Figure 3.17: First five vibration modes for varactor cantilever: (a) 2.0 kHz; (b) 17.0 kHz; (c) 18.6 kHz; (d) 41.3 kHz; (e) 52.6 kHz.

Vibration Response

The vibration response of the cantilever has been simulated in Coventor using the 3D model. Figure 3.17 shows the mode shapes of the cantilever at the first five natural frequencies.

3.2.5 Parametric Studies

The influence of various varactor design parameters on the tuning characteristics have been studied using the ANSYS model. The four parameters of interest are the thickness of the cantilever bottom layer h_1, the tensile stress in the cantilever top layer σ_2, the dielectric relative permittivity ε_r and the initial gap between the cantilever and dielectric. All other parameter values are the same as that in Table 3.1. The results from the parametric studies are plotted in Figure 3.18.

The bending stiffness of the cantilever can be adjusted, by changing the thickness of the stress-free layer, hence altering the varactor tuning characteristics. Figure 3.18(a) shows that the stiffest ($h_1 = 3$ μm) cantilever gives the lowest tuning voltages and the smallest initial jump in capacitance due to instability. Since the stress and thickness of the top layer is kept constant, the thickest cantilever has the least initial curvature (and gap) and consequently its zipping voltages are the lowest. In contrast, the varactor with the thinnest cantilever suffers ($h_1 = 0.55$ μm) from large jumps in the capacitance for both increasing and decreasing bias. As a result, its useful tuning range is lower than the stiffer zipping varactors.

When the tensile stress of the top layer in the cantilever is varied, the effect of different initial curvatures on the tuning behaviour can be studied. Using a lower stress reduces the initial curvature and also reduces the initial jump in capacitance when the cantilever is pulled into contact with the dielectric (see Figure 3.18(b)). Naturally, varactors with larger initial curvatures require higher tuning voltages. Nevertheless, the plot for the varactor with the highest stress ($\sigma_2 = 300$ MPa) shows that once the varactor is in the stable zipping mode, a substantial amount of continuous tuning is still possible (12 to 18 V).

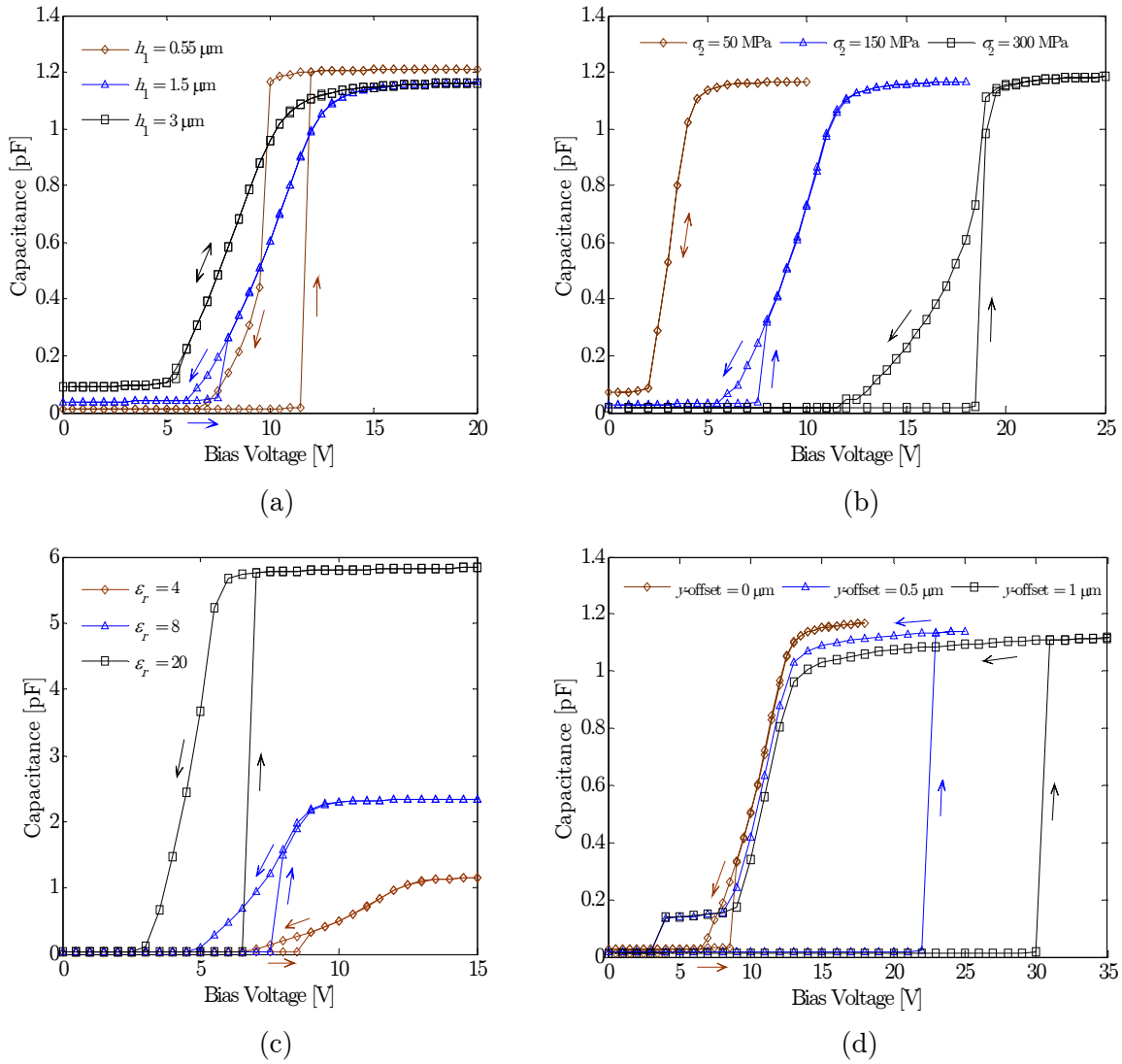


Figure 3.18: Effect of zipping varactor design parameters on tuning characteristics: (a) thickness of cantilever bottom layer; (b) tensile stress in cantilever top layer; (c) dielectric constant; (d) additional gap between cantilever and dielectric.

The influence of the dielectric permittivity on varactor tuning is shown in Figure 3.18(c). Three dielectric constant values have been simulated, corresponding to the materials SiO_2 ($\varepsilon_r = 4$), Si_3N_4 ($\varepsilon_r = 8$) and HfO_2 ($\varepsilon_r = 20$). Using a dielectric with a higher permittivity increases the initial jump in capacitance when the bias is increased. However, continuous tunability is preserved as shown by the C-V characteristics when the bias is subsequently decreased. The maximum capacitance of the varactor also scales directly with the dielectric constant. Hence, a varactor with a higher dielectric constant will give a higher maximum capacitance and larger tuning range for a given device footprint. In addition, the tuning voltages are lowered as the dielectric constant

is increased due to the increased electrostatic loading on the cantilever. However, the gradient of the C-V plot in the stable operating region is also the highest for $\varepsilon_r = 20$, indicating that a higher precision in the voltage control is required for accurate tuning.

In realising an actual device prototype, it is anticipated that an initial gap between the cantilever and the dielectric will be present. A typical process flow requires some separation between the dielectric and cantilever (e.g. the thickness of the sacrificial layer). After the cantilever is released, the presence of the initial gap results in an effective y-offset for the cantilever (see Figure 3.2), whereas in the ideal models no initial gap has been added. The presence of this y-offset has been modelled and the results are plotted in Figure 3.18(d). The results show that a y-offset of 0.5 μm increases the initial pull-in from 9 to 23 V. With a y-offset of 1 μm, the initial pull-in increases further to 31 V. Despite the high initial pull-in voltage introduced by the y-offset, the subsequent tuning behaviour of the three modelled varactors is similar between 8 and 13 V. This implies that if there is a substantial y-offset in a varactor, a large initial pull-in voltage may be required to pull the cantilever into contact with the dielectric. Subsequently, the varactor can then be operated at lower actuation voltages for continuous tuning provided the cantilever is not fully released.

3.3 RF Design

The design considerations for obtaining good RF performance are presented in this section. In particular, the influence of material selection on varactor quality factor is highlighted. Electromagnetic simulations are used to confirm the choice for the conductor in order to ensure low series resistance and a high Q-factor in the zipping varactor. Finally, the design of CPW feed lines for the varactor is discussed.

3.3.1 Quality Factor

In microwave circuits, the quality factor is used as a measure of loss. If the varactor is modelled as a series RLC model as shown in Figure 3.19, the input impedance can be expressed as

$$Z = R_s + j\left(\omega L_s - \frac{1}{\omega C}\right) \tag{3.33}$$

The quality factor is then defined as [48]

$$\begin{aligned} Q &= \frac{\left|\mathrm{Im}(Z)\right|}{\mathrm{Re}(Z)} \\ &= \frac{\left|\omega^2 L_s C - 1\right|}{\omega R_s C} \end{aligned} \tag{3.34}$$

For frequencies much smaller than the self-resonant frequency, the expression for the Q-factor simplifies to

$$Q \approx \frac{1}{\omega R_s C} \quad \text{for } \omega \ll \frac{1}{\sqrt{L_s C}} \tag{3.35}$$

Therefore, to increase the Q-factor of a varactor and hence improve its loss performance, its series resistance must be minimised. In addition, the device series inductance must also be kept reasonably low.

For a given varactor design, it is advantageous to use high-conductivity materials for the electrodes in order to lower the series resistance. In the proposed zipping varactor, the chosen material for both the movable and fixed electrodes is gold. Au is ideal for this application due to its excellent conductivity and resistance to oxidation. Another advantage of using Au is the relative ease of bonding connecting wires for electrical testing or integration into application circuits.

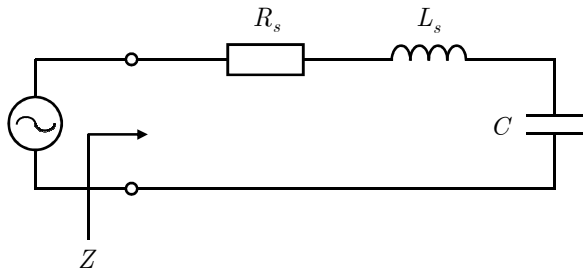


Figure 3.19: Series RLC model of a capacitor.

3.3.2 Electromagnetic Simulation

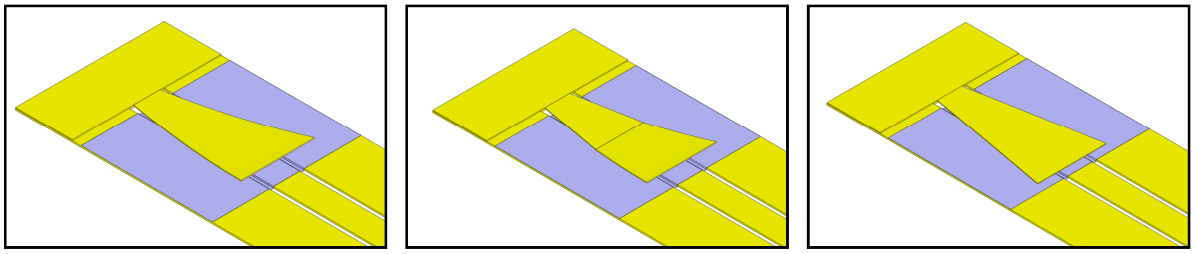
A full-wave simulation of the zipping varactor has been performed in HFSS 10 [134] using a 3D finite element model. In the model, the effect of conductive losses has been accounted for while the dielectrics are taken to be lossless. Hence, if the model reveals an unacceptably low Q-factor at operating frequencies, it is an indication that the series resistance of the varactor is too high. The varactor is modelled with a 100 μm

glass substrate and the relative permeabilities of all materials are taken to be 1. The cantilever is modelled as a 1.65 μm layer of Au while the pull-down electrode is 3.5 μm of Au. The rest of the parameters for the simulated varactor are listed in Table 3.4.

Three different tuning states have been modelled, namely when the varactor is unbiased; when the zipped portion is half the length of the cantilever; and when the cantilever is fully zipped. Figure 3.20 shows the three modelled states of the device. The z-curvature of the cantilever has not been modelled, i.e. the zipped portions are flat and have perfect contact with the dielectric. The cantilever end height for the unbiased model is 28 μm.

Table 3.4: Varactor parameters for HFSS model.

Parameter	Value	Parameter	Value
Length, l	300 μm	Substrate thickness, H	100 μm
Cantilever width, $b(x)$	$0.36x + 60$ μm	Substrate permittivity, $\varepsilon_{r,glass}$	5.5
Electrode width, b_e	60 μm	Au conductivity, σ	4.1×10^{13} pS/μm
Electrode offset, δ_x	20 μm	Cantilever Au thickness, h_m	1.65 μm
Thickness of SiO_2, t_d	0.3 μm	Electrode Au thickness, h_e	3.5 μm
SiO_2 permittivity, ε_r	4	Initial curvature, κ	6×10^{-4} μm^{-1}



(a) (b) (c)

Figure 3.20: Tuning states for zipping varactor HFSS model: (a) unbiased; (b) half-zipped; (c) fully-zipped.

The simulated capacitance and Q-factor between 1 and 10 GHz are plotted in Figure 3.21. At 2 GHz, the varactor capacitances are 0.066, 0.966 and 2.013 pF with corresponding Q-factors of 132, 98 and 91, respectively. The simulation indicates that a zipping varactor design with Au electrodes on an insulating glass substrate gives a device with high Q-factor. In an actual prototype, the presence of additional metal

layers and the effect of dielectric and substrate losses may degrade the actual Q-factor. However, it is expected that the RF performance of the zipping varactor will be sufficient for most applications. Note also that a thinner substrate (100 μm) has been modelled relative to the actual device substrate (500 μm) to improve modelling efficiency.

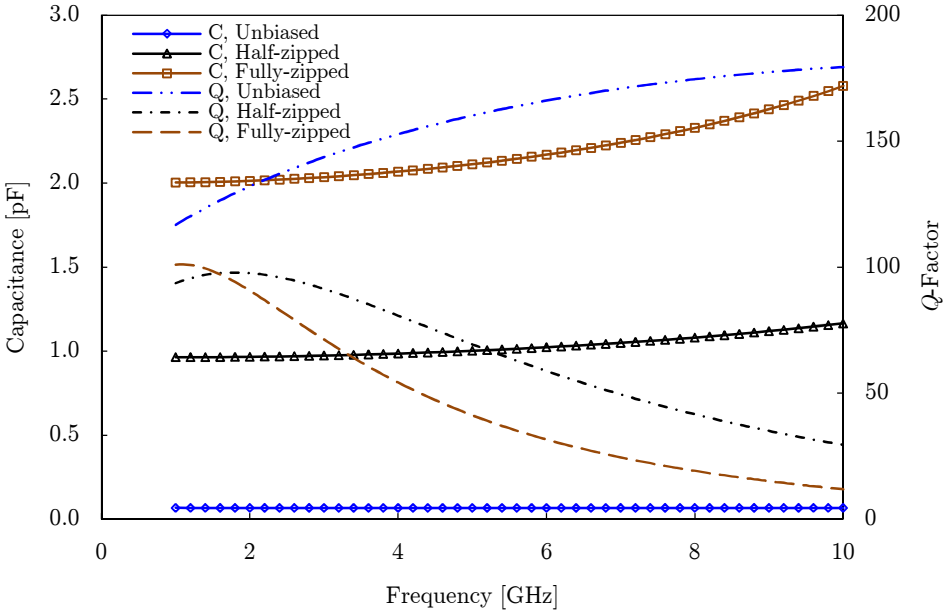


Figure 3.21: HFSS electromagnetic simulation results.

3.3.3 Coplanar Waveguide Design

For compatibility with the available 50 Ω RF testing equipment, CPW [135] feed lines have been integrated with the zipping varactors on a glass substrate. The width of the CPW signal conductor (w) is 60 μm with 150 μm wide ground conductors on the two adjacent sides. The gap between the signal and ground conductors (s) is 10 μm, and the thickness of the lines are 3.5 μm. An infinitesimal length of transmission length is often modelled using lumped elements as shown in Figure 3.22. The element R' is the series resistance per unit length while the element G' represents the shunt conductance per unit length. L' is the series inductance per unit length and C' is the shunt capacitance per unit length.

The CPW line is modelled using a quasi-TEM (transverse electromagnetic) analytical approach [136]. This model is valid provided the wavelength does not fall short of ten times the characteristic waveguide dimensions, i.e. $\lambda/10 \geqslant w + 2s$,

otherwise non-TEM modes will introduce significant inaccuracies. Given that the above condition holds, the variation of C' with frequency is negligible and has a value of 1.26×10^{-4} pF/μm. Since the CPW is approximately lossless, the characteristic impedance is then given by

$$Z_0 = \sqrt{\frac{L'}{C'}} \tag{3.36}$$

The dependence of R' and Z_0 with frequency are plotted in Figure 3.23. The plots demonstrate the effect of the skin depth on R' and L'. Note also that the skin depth of gold is 3.5 μm at 0.5 GHz and 1.8 μm at 2 GHz. From Figure 3.23(b), we see that the characteristic impedance Z_0 is around 50 Ω in the frequency range of interest (0.1 to 5 GHz).

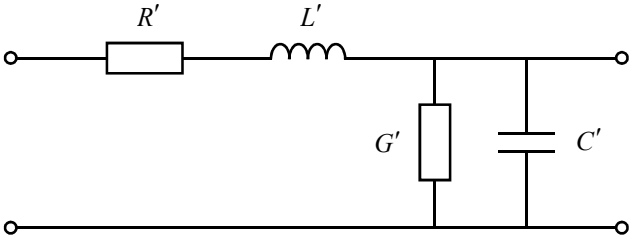
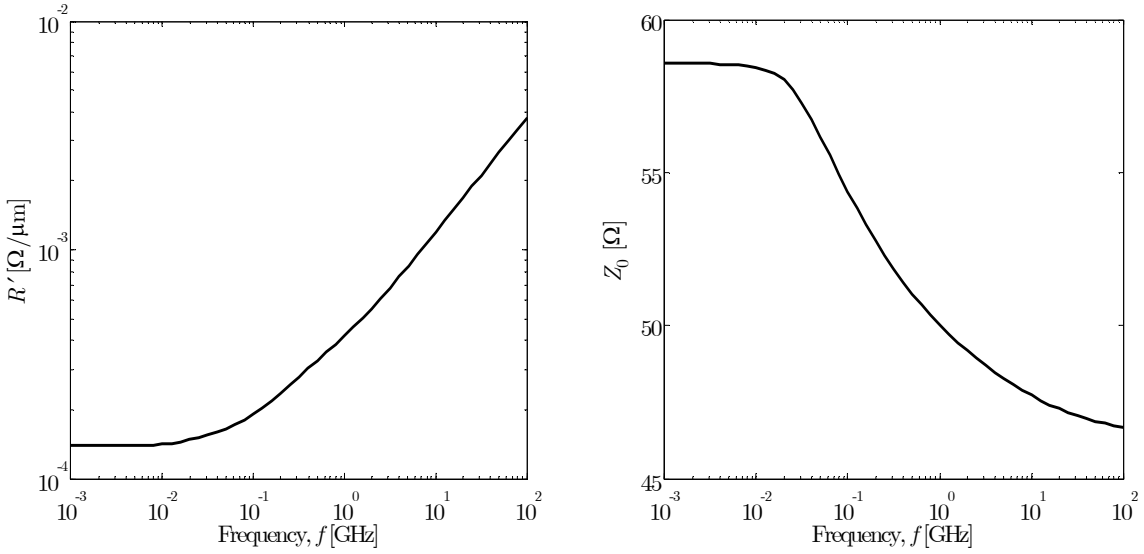


Figure 3.22: Transmission line equivalent circuit model.



(a) (b)

Figure 3.23: CPW lumped element model: (a) series resistance per unit length; (b) lossless characteristic impedance.

Based on the modelling results obtained from the models described in this chapter, zipping varactors incorporating a SiO_2 dielectric have been designed. In order to verify the predicted performance, varactor prototypes have been implemented and characterised. The following two chapters describe the fabrication and testing, respectively of these varactor prototypes.

Chapter 4

Fabrication

This chapter describes the fabrication method developed for the zipping varactors. A summary of the key fabrication steps is given, and subsequently, the issues associated with prototype development are discussed. The complete process flow for a zipping varactor incorporating silicon dioxide as the dielectric material is listed in Appendix C, and detailed parameters are specified for each step.

4.1 Process Flow

The zipping varactor fabrication is based on surface-micromachining techniques [12]. In order to facilitate the integration of a high-permittivity dielectric at a later stage, the process is divided into two separate wafers: a *bottom* wafer with the fixed electrode, CPW transmission lines and dielectric; and a *top* wafer with the bi-layered cantilever. Each wafer requires two photolithographic masks and the smallest feature size is 10 μm. Upon process completion, the wafers are diced up and the zipping varactors are assembled using dies from the bottom and top wafers. Due to the lack of in-house facilities for wafer-level assembly, a die-level assembly method has been adopted for the varactor prototypes.

4.1.1 Bottom Wafer Process

Figure 4.1 shows the fabrication steps for the bottom wafer. The device is fabricated on a 500 μm thick, 4-inch soda lime glass wafer. Using a glass wafer instead of high-

resistivity silicon reduces substrate losses and improves the varactor Q-factor. First off, the wafer is sputter-coated with 20 nm of chromium and 190 nm of copper (Figure 4.1(a)). The copper is used as a seed layer in subsequent electroplating steps while the chromium layer improves adhesion between the copper and the glass. For optimum adhesion, the glass substrate is pre-cleaned by performing a short sputter-etch prior to metal deposition. The sputter cleaning and chromium/copper deposition is completed in one vacuum cycle in a Nordiko RF sputtering system (NM-2000-T8-SE1).

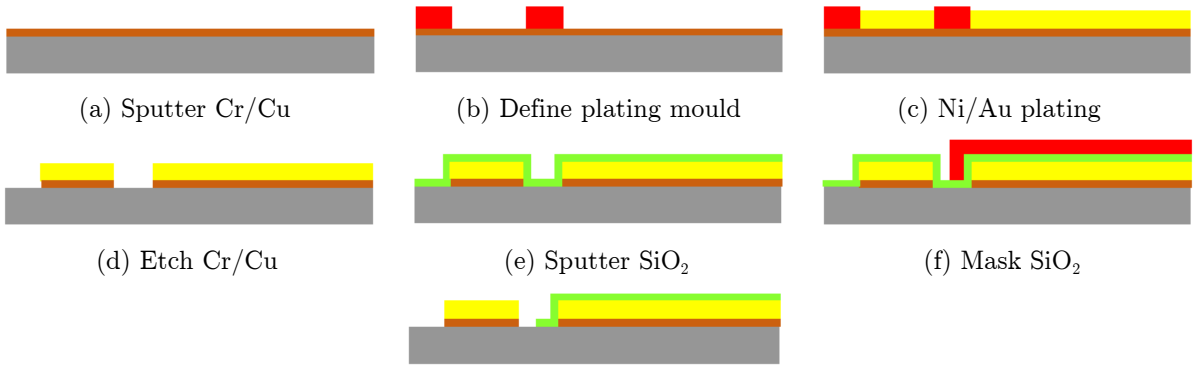


Figure 4.1: Bottom wafer fabrication steps.

Next, a 4.4 μm thick layer of Shipley S1828 positive resist is spin-coated onto the copper layer. For best adhesion, the resist is spun immediately after sputter deposition. This reduces the amount of surface contamination through moisture adsorption and copper oxidation. After spin-coating, the fresh resist is soft baked in a 90 °C convection oven for 30 minutes to remove the bulk of its solvent. During baking, the wafer is mounted vertically using a quartz wafer carrier rather than rested on the oven rack. This prevents non-uniform heat transfer across the wafer which can occur if the wafer is placed in direct contact with the steel rack.

For resist exposure, a Quintel Q4000 mask aligner equipped with a broadband mercury arc lamp is used to provide the required UV energy (65 s exposure). To achieve greater consistency in the lithography, setting the wafer aside for at least two hours after the pre-exposure bake ensures that the exposure and development time variability is reduced. In addition, the intensity of the UV exposure is ideally 7 ± 1 mW/cm^2 at 405 nm wavelength (measured at the mask plane). As the lamp power output drops over its lifetime, the exposure time must also be adjusted accordingly.

The wafer is then developed in Shipley MF-319 developer, and the exposed areas are removed, thus defining the electroplating mould (see Figure 4.1(b)). A short, low-power descum in oxygen plasma cleans the exposed copper surface of any remnant resist material and finally, a post-exposure hard bake at 110 °C makes the resist mould resistant to attack by the electroplating baths.

Before the wafer is electroplated, it is immersed briefly in dilute sulphuric acid to remove oxidised copper and improve seed layer conductance. A thin nickel diffusion barrier (approximately 60 nm) is then plated onto the copper using a Schloetter Nickel Sulphamate MS bath. After a thorough rinse in deionised (DI) water, the wafer is promptly plated with soft gold using Metalor's ECF 64D ammonium gold sulphite solution (Figure 4.1(c)). The main gold conductor for the fixed varactor electrode and the CPW feed lines is approximately 3.1 μm thick. With the presence of the nickel barrier layer, copper diffusion into gold is greatly reduced. This prevents the formation of intermetallic compounds, hence improving device reliability [137].

After the required conductor thickness has been obtained, the resist mould is stripped using acetone and isopropyl alcohol (IPA). With the electroplated layers acting as a mask, the copper seed layer is selectively etched away with 6% ammonium persulphate solution. The chromium adhesion layer is then etched away using a potassium ferricyanide etchant (Figure 4.1(d)).

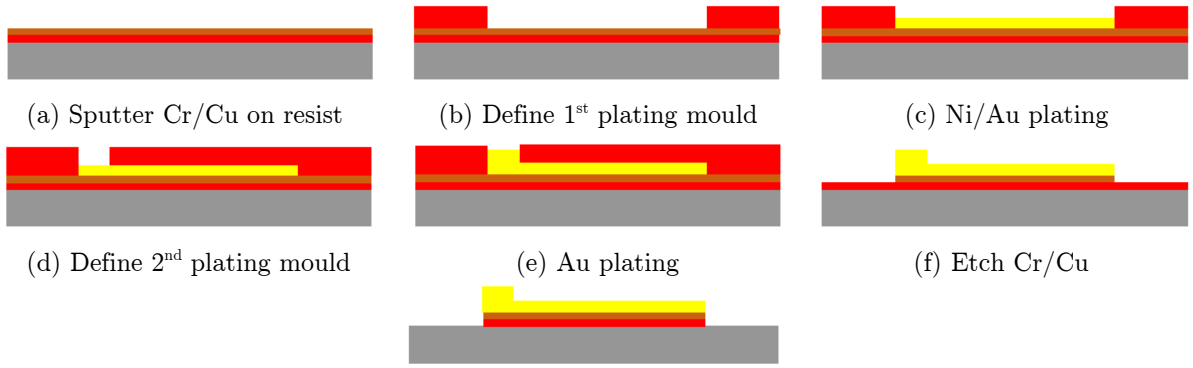
The varactor dielectric consists of 230 nm of silicon dioxide. This SiO_2 layer is sputtered over the entire wafer, and then masked with S1828 resist (Figure 4.1(e), (f)). For the resist mask, a soft bake is performed in a 90 °C oven but hard baking is not required. The exposed oxide is etched away in a CHF_3/Ar plasma in an Oxford Instruments Plasmalab80Plus reactive ion etch (RIE) process. Due to prolonged plasma exposure, the resist mask becomes resistant to typical solvents. Therefore, the most chemically resistant, surface layer is first removed using oxygen plasma in an ashing step. Subsequently, the remaining resist is removed using a 1-methyl-2-pyrrolidone resist stripper (Shipley 1165) heated to 80 °C.

4.1.2 Top Wafer Process

Figure 4.2 shows the fabrication steps for the top wafer. A soda lime glass wafer is chosen as the carrier substrate so that the process can be easily modified for a fused

silica substrate. This allows the option of using a laser-driven batch transfer process developed in the group [138, 139] which requires a UV-transparent substrate.

The first step in the top wafer process is to spin a 500 nm thick layer of Shipley S1813 resist for the sacrificial layer. This resist layer is soft baked at 90 °C and then hard baked at 130 °C in an oven so that it can withstand the subsequent processing steps. Next, 50 nm of chromium and 150 nm of copper are sputtered onto the sacrificial layer (see Figure 4.2(a)). The thickness and deposition parameters of the chromium and copper layers are adjusted to obtain an adequate amount of tensile stress, such that the cantilever curves upwards after assembly and release. As for the bottom wafer, the copper layer also functions as the electroplating seed layer.



(a) Sputter Cr/Cu on resist (b) Define 1st plating mould (c) Ni/Au plating

(d) Define 2nd plating mould (e) Au plating (f) Etch Cr/Cu

(g) Etch sacrificial resist

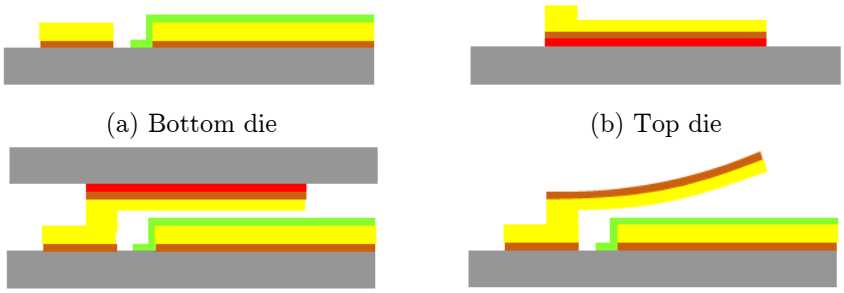
Figure 4.2: Top wafer fabrication steps.

Using identical process parameters to the bottom wafer CPW electroplating, the gold cantilever is plated (Figure 4.2(b), (c)) to a thickness of 1.1 μm. The first resist mould is then stripped by flood exposure followed by development in MF-319 solution. A second plating mould is then defined (Figure 4.2(d)), and the anchor region is plated with an additional 0.5 μm of gold (Figure 4.2(e)). After stripping the second resist mould, the copper and chromium layers are wet etched using the same etchants as the corresponding steps in the bottom wafer. Finally, the exposed sacrificial resist is dry etched with O_2 plasma RIE.

4.2 Device Assembly

Once the fabrication for the top and bottom varactor parts is completed, the respective wafers are cut into dies using a dicing saw. A layer of protective resist protects the dies

from contamination during the dicing process. For the top wafer, this protective resist is flood exposed prior to wafer dicing. After the wafers have been cut into dies, the protective resist and mounting adhesive (Crystalbond 555) are stripped using Shipley 1165 solution and MF-319 developer for the bottom and top dies, respectively. A final oxygen plasma cleaning step ensures that the gold surfaces are clean and free of organic material in order to improve bonding success (see Figure 4.3(a), (b)).



(a) Bottom die (b) Top die

(c) Alignment and bonding (d) Release and freeze drying

Figure 4.3: Wafer dicing, device assembly and release.

The dies are then assembled using a purpose-built aligner bonder [139, 140] as shown in Figure 4.4. The bottom die is clamped in place on the bonding stage, which is then heated to approximately 180 °C. The top die is held by a tungsten carbide bonding tool with a vacuum chuck, and this tool is attached to a UTHE ultrasonic transducer horn. Using the tilt adjustment screws for the stage, the dies are adjusted for parallelism using a laser alignment system. Next, the top and bottom varactor parts are aligned and the top die is brought into contact with the bottom die. A pressure of 120 MPa (12 kg-force/mm^2) is applied and the dies are thermosonically bonded together with 18 W of ultrasonic power and a bond time of 200 ms (Figure 4.3(c)). Apart from the device anchors, additional support bumps have been included in the die design to improve the mechanical robustness of the bonded dies.

After bonding, the top die substrates are removed by dissolving the sacrificial resist in hot 1165 resist stripper. Finally, the device is released using a freeze-dry process with a 9:1 water/methanol mixture (Figure 4.3(d)). If the wet solvent or rinse water is allowed to evaporate from the varactor directly, the cantilever becomes irreversibly stuck on the dielectric (stiction) due to surface tension forces. In the freeze-dry process, the frozen solvent matrix sublimates from the varactor gaps, leaving the free standing structures intact. The device dies are also inverted during free-drying (facing

downwards) to minimise the accumulation of remnant residue due to impurities in the solvent mixture.

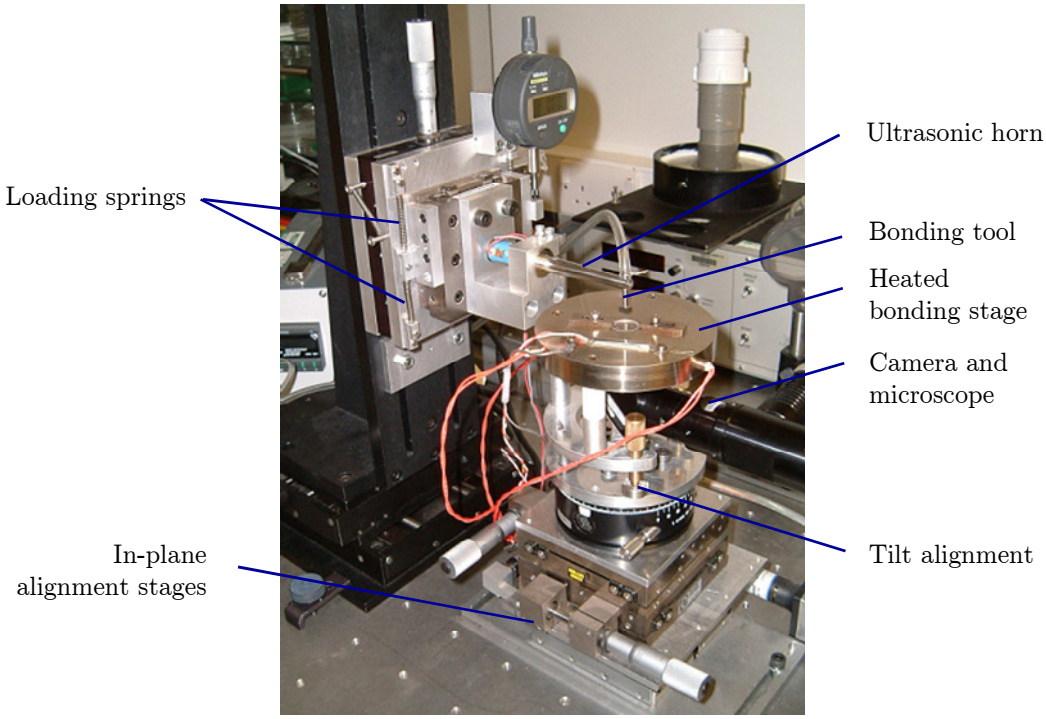


Figure 4.4: Aligner-bonder for die-level thermosonic bonding.

4.3 Process Optimisation

The main challenges encountered in developing the fabrication process and the steps taken to overcome them are described in this section.

4.3.1 Lithography

Early in the process development, a thorough post-exposure hard bake was found to be essential for resist compatibility with the gold plating process. If the resist is not hard-baked before the gold plating step, drastic degradation of the resist mould occurs when the wafer is exposed to the gold plating solution. A large amount of under-plating occurs at the resist/seed layer interface, leading to crack formation and resist lift-off. Voids and bubbles may also appear in the resist layer, suggesting a possible reaction with the gold solution.

For preliminary trials, the S1828 resist mould was soft-baked in an oven at 90 °C for 30 minutes and then hard-baked at 110 °C for 40 minutes after exposure and development. However, under-plating was not eliminated although the bulk of the resist layer appeared chemically resistant to the gold solution. Figure 4.5 shows the extent of gold under-plating resulting from an insufficiently hard-baked resist mould. Increasing the hard baking time to 60 minutes produced a resist mould that is fully compatible with the gold plating process. As shown in Figure 4.6, the gold under-plating could then be fully eliminated.

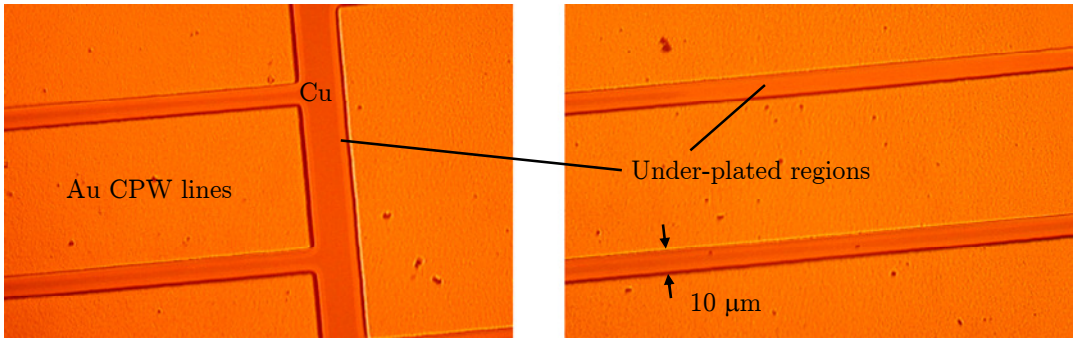


Figure 4.5: Gold under-plating leading to transmission line shorts.

The second issue encountered in resist processing is the difficulty in stripping plating moulds and etch masks after the resist has been exposed to various processing steps. When stripping the mask for oxide etching using Shipley 1165, a thin film of material remains over the device dielectric as shown in Figure 4.7(a). Studies by various groups suggest that this persistent layer could be due to the deposition of fluorocarbon polymers [141] or cross-linking of the resist mask due to photon irradiation and overheating [142]. Even after a prolonged immersion in hot 1165 solution (1 hour), the film of material is not removed. Adding ultrasonic agitation to the solvent did eventually result in complete mask removal. However, this caused the edges of the gold transmission lines to deform slightly, due to a lack of mechanical support caused by seed layer over-etch. One strategy adopted to clean device surfaces after exposure to fluorocarbon plasmas is to use a dry ashing step followed by a wet resist strip [143, 144] and this was sufficient to remove the resist mask cleanly (see Figure 4.7(b)).

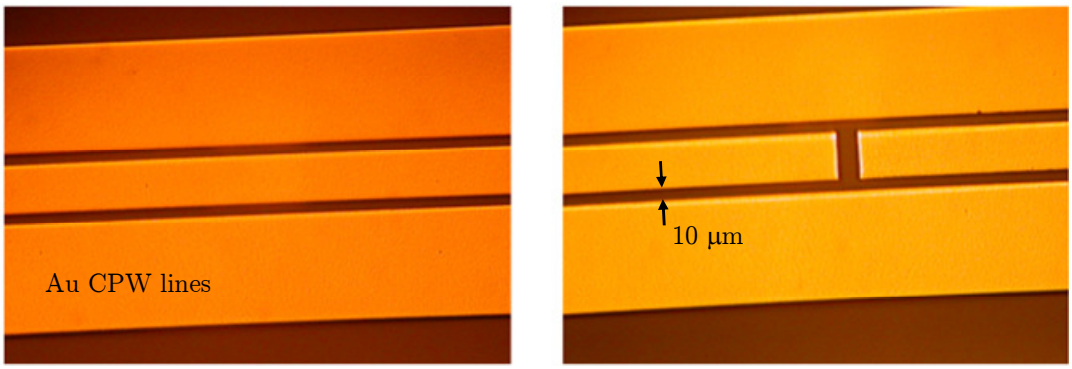
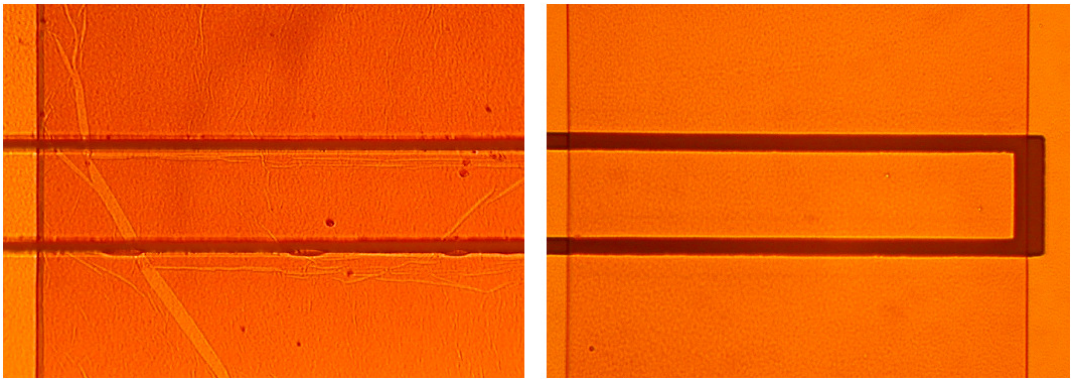


Figure 4.6: CPW lines with under-plating completely eliminated.

Stripping electroplating moulds using flood exposure and development for the top wafer was also more challenging compared to using acetone. In order to preserve the integrity of the sacrificial resist, the use of acetone was avoided initially. Instead, the electroplating moulds for the top wafer were removed by flood exposing the wafer (300 s) and then stripping the resist in MF-319 developer (10 to 15 minutes). However, it was observed that the resist moulds do not strip cleanly even after prolonged development. A test revealed that the resist mould could be stripped using acetone even for the top wafer. Due to the higher resist solubility in acetone, a short immersion (1 to 2 minutes) was sufficient and the sacrificial layer remains intact. Very slight peeling occurs in the seed layer at wafer edges but the bulk of the sacrificial resist beneath the varactors is protected by the seed layer.



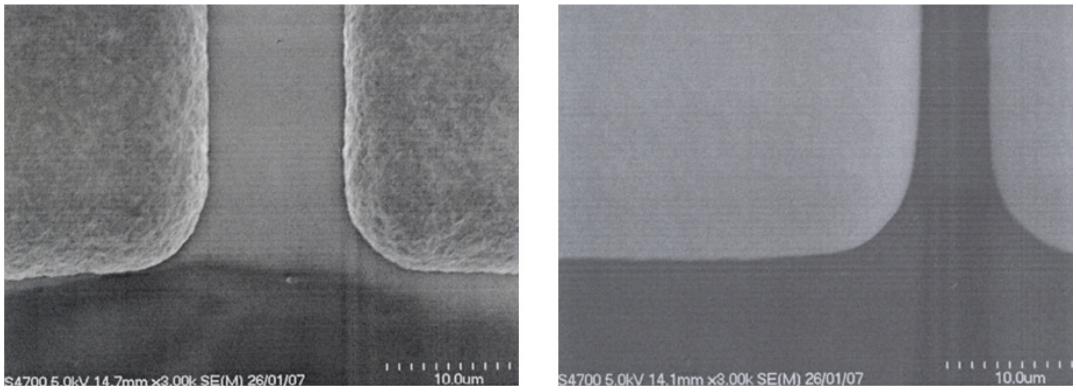
(a) (b)

Figure 4.7: Post-RIE resist strip: (a) without ashing step; (b) with ashing step.

4.3.2 Gold Plating

The main issues encountered in the gold electroplating steps were related to stress and roughness control. Plating solutions based on the gold (I) sulphite complex provide

better resist compatibility than bath chemistries based on the gold (I) cyanide complex [145, 146], hence an ammonium gold sulphite plating solution (Metalor ECF64) was selected for varactor fabrication. According to the supplier, this solution is used for plating soft, bondable gold deposits with low stress and a bright surface finish. In addition, the solution chemistry does not contain brighteners such as arsenic or thallium which increase the gold hardness, making bonding more difficult. The absence of cyanide and harmful brighteners is also attractive from a health and safety perspective. Figure 4.8 shows supplier SEM images of gold deposits plated using the ECF64 solution and another potassium gold sulphite solution (Metalor ECF60). The surface finish of gold plated using the ECF64 solution showed a much lower surface roughness.



(a) (b)

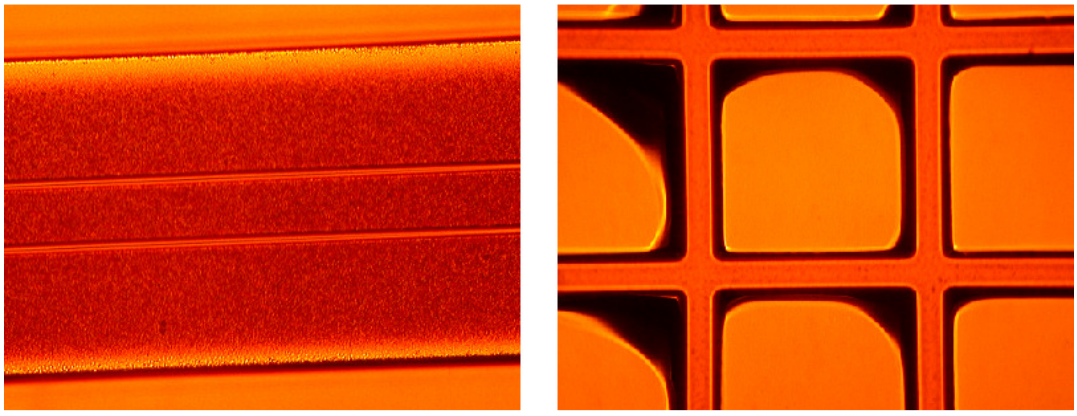
Figure 4.8: Gold plating surface finish: (a) ECF60; (b) ECF64 (photos courtesy of Mike Wild, Metalor Technologies UK).

Table 4.1: ECF64 supplier operating conditions.

Parameter	Range	Optimum
Gold Concentration [g/l]	12 – 18	15
Current Density [mA/cm^2]	1 – 5	3
Temperature [°C]	40 – 60	50
Cathode Agitation [m/s]	0.05 – 0.12	0.08
pH	8.5 – 9.5	9.1

Initial plating trials with the ECF64 gold solution revealed that careful process control was required in order to achieve the best results. The recommended operating conditions for an ECF64 bath are shown in Table 4.1. For the initial trials, the

optimum bath conditions were used except that the bath temperature was lowered to 35 °C and there was no cathode agitation. The low plating temperature was adopted to reduce the problems associated with the resist mould (i.e. under-plating, poor adhesion etc.). However, this resulted in gold deposits that were extremely rough, with a dark appearance ranging from orange to dark brown. When the quality of the resist mould was improved, the bath temperature was increased to 50 °C, but the quality of the plated gold remained inconsistent. This is in contrast to the ECF60 solution which gives gold deposits with a matt yellow appearance even when plated at 35 °C, despite having the same recommended temperature range. Figure 4.9(a) shows a very rough surface finish in ECF64 gold. Since the varactor dielectric is sputtered as a conformal coating over the plated gold, a high degree of gold roughness will result in a high degree of oxide roughness. This will reduce the effective dielectric constant of the SiO_2, and lower the device capacitance. Roughness in the plated gold for the cantilever will also have a similar effect.



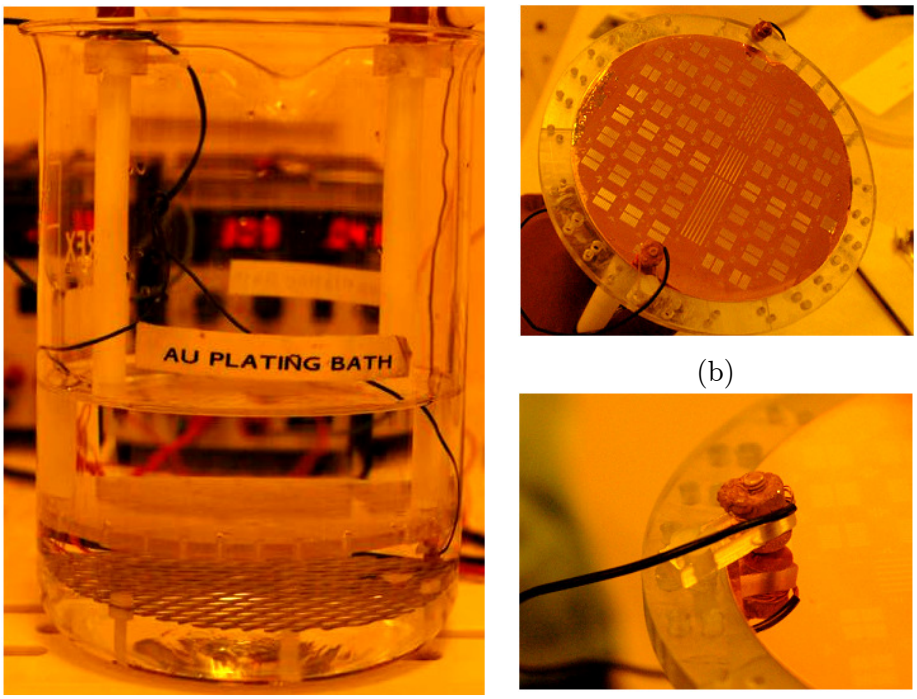
(a) (b)

Figure 4.9: ECF64 gold plating issues: (a) high surface roughness; (b) film delamination due to excessive stress.

Under non-ideal plating conditions, the gold stress could also become excessively high, leading to delamination (see Figure 4.9(b)). For the cantilever, it is also important to develop a process that gives low stress in the gold layer. A stress gradient in the gold could potentially give rise to an opposite bending moment to that obtained from the tensile seed layers, leading to a lack of upward curvature in the cantilever.

Several problems were identified in the gold plating setup which contributed to the inconsistent plating results. Figure 4.10 shows the gold plating setup that was used in the initial stages of process development. Firstly, the setup does not allow cathode

agitation which is recommended by the supplier. Some solution agitation is possible by incorporating a magnetic stirrer. However, this is less effective in promoting ion transport relative to moving the wafer (cathode) side to side in the solution. Secondly, the electrical contact to the wafer is exposed to the plating solution, and hence it is also plated with gold. Although the additional area introduced by the contact could be roughly estimated, it adds a degree of uncertainty to plating area. In addition, the contact has a slightly higher potential than the wafer surface since there is a potential drop due to contact resistance. The consequence is that the actual current density and plating rate becomes unreliable from wafer to wafer. Thirdly, the horizontal configuration of the wafer holder makes it difficult to eliminate bubbles when immersing the wafer into the solution.



(a) (b) (c)

Figure 4.10: Horizontal gold plating setup: (a) wafer holder and platinised titanium mesh in gold solution; (b) wafer holder with exposed contacts; (c) close-up view of exposed contact.

To overcome these issues, a new gold plating setup was designed and implemented. As shown in Figure 4.11, a vertical plating configuration is adopted in order to minimise bubble entrapment. The wafer holder is mounted on a slider-crank mechanism and hence a suitable amount of cathode agitation can be selected during plating. The main purpose of applying cathode agitation is to facilitate ion transport

and prevent a large departure from the optimum plating chemistry in the vicinity of the wafer. This is beneficial to all forms of electroplating in general and the agitation rig can be used for small-scale plating of other materials as well, such as copper, tin, silver etc. The linear velocity of the slider (and hence wafer) can be derived as (see Figure 4.11) [147]

$$x' = (\theta' + \phi')B\sin(\theta' t) \tag{4.1}$$

where θ' and ϕ' are the angular velocities of the crank and connecting rod, respectively, and B is the radius of the crank. The angular velocity of the connecting rod is given by

$$\phi' = \theta' \frac{(B\ /\ P)\cos(\theta' t)}{\left[1 - (B\ /\ P)^2 \sin^2(\theta' t)\right]^{1/2}} \tag{4.2}$$

and P is the length of the connecting rod.

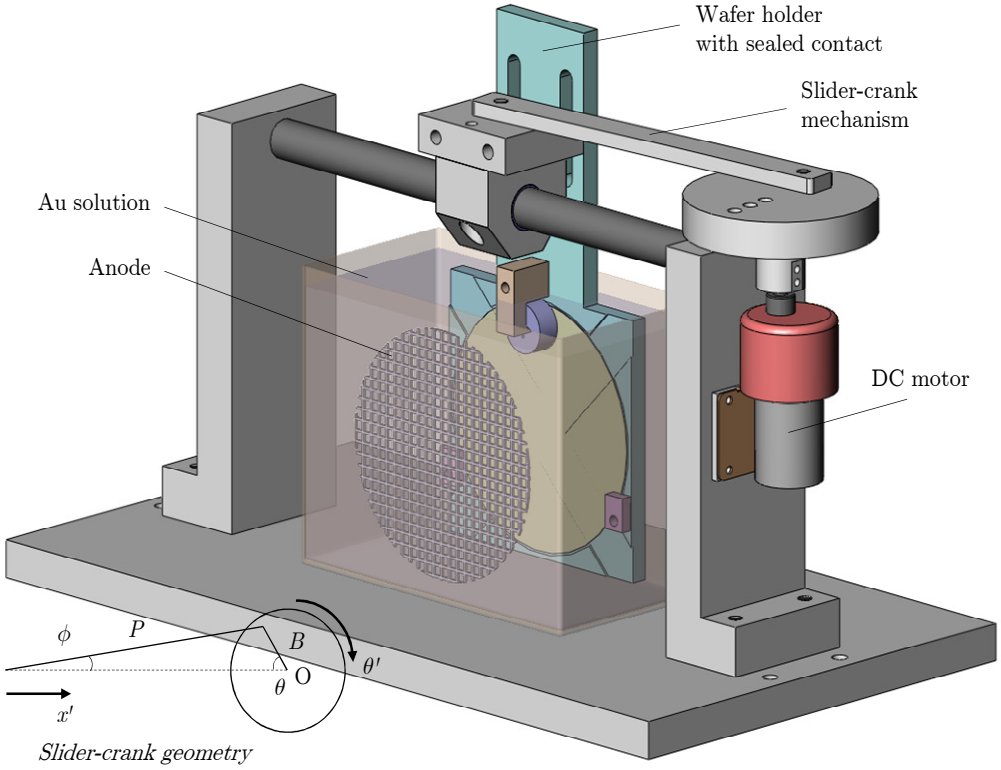


Figure 4.11: New gold plating setup with vertical plating configuration and cathode agitation.

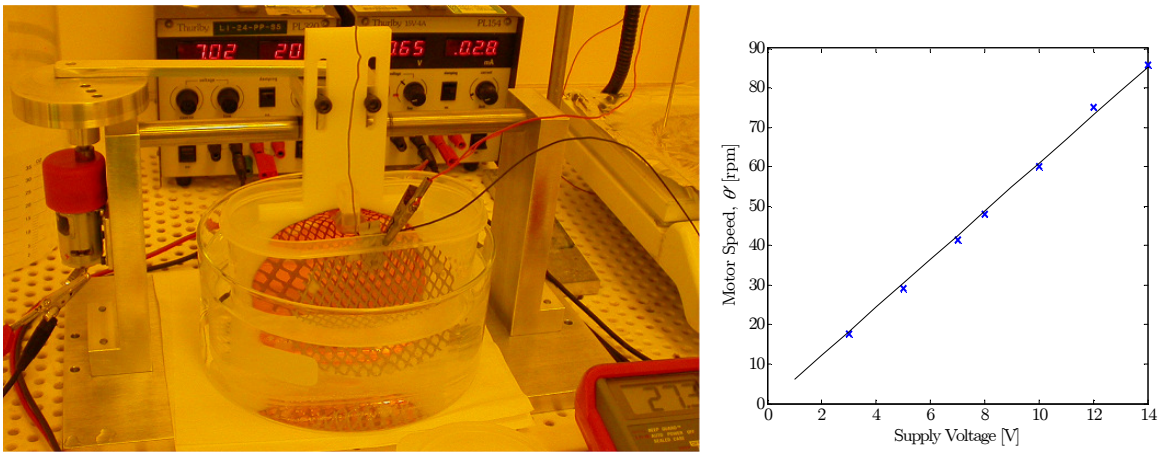
The length of the connecting rod is 160 mm and radius of the crank is adjustable between 10 and 30 mm. Provided $(B/P)^2 \ll 1$, then it can be shown from (4.2) that $\phi' \ll \theta'$ and the slider linear velocity can be approximated as

$$x' \approx B\theta' \sin(\theta' t) \tag{4.3}$$

with a corresponding root mean square (RMS) velocity given by

$$x'_{rms} \approx \frac{B\theta'}{\sqrt{2}} \tag{4.4}$$

Hence, a motor speed of 30 rpm (5 V supply voltage) gives an RMS linear velocity of 0.03 m/s ($B = 15$ mm). For most wafers, this was sufficient to produce good quality gold deposits. By changing the crank radius, the peak to peak displacement and the linear velocity for a given motor speed can be adjusted. Figure 4.12 shows the actual gold plating setup and the calibration of the DC motor speed against its supply voltage.



(a) (b)

Figure 4.12: Actual gold plating setup: (a) plating a 4-inch wafer; (b) motor speed versus supply voltage.

To allow more precise estimation of the plating area and hence select an appropriate current density, a sealed contact was designed for the wafer holder. When clamped into place, a silicone seal prevents the contact from exposure to plating solution. In addition, the contact has a soft spring which reduces contact resistance. This improved contact design allows better control of the plating process and it was observed that the repeatability of the plating rate and the quality of the deposits improved substantially.

As shown in Figure 4.12(a), the container for the gold solution is immersed in a water bath to increase the overall heat capacity. During electroplating, the pre-heated solution and water bath is removed from the hotplate and transferred to the agitation

rig. Inevitably, temperature drops during plating but this is acceptable if the plating time is reasonably short. If necessary, the entire setup including the agitation rig can be mounted on a temperature-controlled hotplate and the temperature variation can be reduced. The rig can withstand operating temperatures of up to 60 °C.

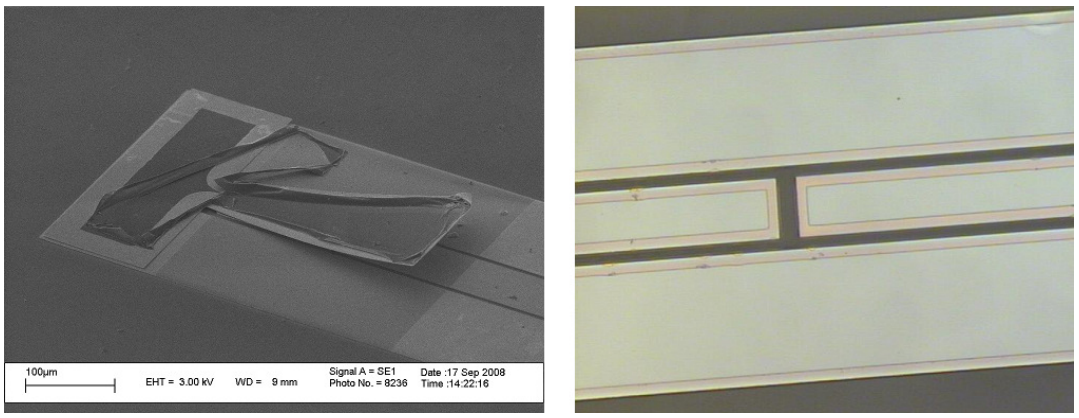
In summary, the recommended operating parameters for ECF64 gold plating using the new setup are as follows: a current density between 1 and 3 mA/cm^2; plating temperatures greater than 40 °C, with an ideal range from 45 to 55 °C; agitation speeds of 0.03 to 0.07 m/s. These plating conditions and the corresponding resist mould processing are also fully compatible with the ECF60 gold solution. The gold concentration of a plating solution is also monitored by keeping track of gold usage although this can difficult due to drag-out losses. Solution evaporation also affects the gold concentration and when necessary, the solution is topped up with DI water. Although the pH of the solution remains reasonably stable, periodic checking is necessary as a pH of 7 or less will lead to colloidal gold formation and rapid bath deterioration. To raise the pH of the solution, 30% ammonium hydroxide solution can be added (approximately 13 ml for one litre of gold solution increased the pH from 8 to 9). Under optimised plating conditions, bright gold deposits with low stress and low roughness can be plated consistently (see Figure 4.6). The typical plating rate for a current density of 3 mA/cm^2 is around 0.18 μm/min.

4.3.3 Wet Etching

The third issue encountered in varactor fabrication relates to seed layer etch control. In wet etching the copper and chromium layers on the wafers, etch control can be challenging since etch rates are typically different across the entire wafer. Sputter etching typically results in less over-etch and the facilities are available in the research group's cleanroom. However, additional masking over the electroplated gold is required as sputter etching is non-selective. Wet chemical etching provides the required selectivity but the etch rates must be optimised to prevent over-etching. Figure 4.13 shows examples of over-etching in the seed layers.

For chromium etching, a potassium ferricyanide etchant (NaOH, $K_3[Fe(CN)_6]$, H_2O in the proportion 1 g : 2 g : 80 ml) [148] was used to give good etch selectivity with respect to the other metals present. Two copper etchants, 6% ammonium persulphate solution (by weight percentage of $(NH_4)S_2O_8$) and a phosphoric acid based etchant

(85% H_3PO_4, 99% CH_3COOH, 70% HNO_3, H_2O in the volume proportion 4 : 4 : 1 : 1) [148] were tested for ease of etch control. The problem of etch control was narrowed down to copper etching rather than chromium etching since the copper etch rate was much higher. Typical chromium etch rates were between 13 to 27 nm/min using the potassium ferricyanide etchant, while copper etch rates were between 84 to 175 nm/min for the 6% ammonium persulphate solution and between 380 to 760 nm/min for the phosphoric acid etchant. Since the copper layer is etched before the chromium layer, an over-etched copper layer reduces the effectiveness of the etch mask (electroplated features) and promotes over-etching in the chromium layer. From Figure 4.13(a), it can be observed that the copper has been severely over-etched causing the chromium to peel off after device assembly and release.



(a) (b)

Figure 4.13: Seed layer over-etch: (a) copper over-etch causing chromium peeling in assembled device; (b) underside view of over-etched chromium and copper underneath CPW lines.

The first method of improving etch control is by etching the device dies individually as opposed to etching the entire wafer. It is difficult to obtain uniform etch rates across a 4-inch wafer, and by etching individual dies, the etch time can be controlled more precisely. This is not a feasible solution in the long term since it is time consuming and removes the advantages of batch processing. Nevertheless, since a die-level assembly step has been adopted for the varactor prototypes, the dies could be etched after wafer dicing with relatively good etching control. However, only the top wafer can be etched at the die level since the seed layer etch is the last step. For the bottom wafer, the seed layers have to be removed before sputtering the silicon dioxide.

To improve etch control at the wafer level, some preliminary tests were performed with the ammonium persulphate etchant at various concentration levels. Table 4.2 shows the etch times for 170 nm thick copper films on 7.1 by 7.1 mm dies. For solutions with ammonium persulphate concentrations between 2.1 to 6.0%, the etch time was apparently invariant at 30 s. However, due to the short etch times, and the difficulty in determining the exact point of etch completion, it was difficult to measure the etch time accurately. When the concentration was decreased to 1.6%, the etch time increased to 75 s and a further dilution to 1.3% concentration produced an etch time of 90 s.

Table 4.2: Etch time for 170 nm thick Cu film on 7.1 mm by 7.1 mm dies.

Ammonium Persulphate Conc. [% mass]	Etch Time [s]
6.0	30
4.1	30
3.1	30
2.1	30
1.6	75
1.3	90

Further work is required to confirm the above experimental results for copper etch rates with respect to ammonium persulphate concentration. Nevertheless, the diluted etchant, at 1.3% concentration, was found to be better for more precise etch control compared to the original etchant with 6% concentration. A combination of die-level copper etching and using the more dilute 1.3% ammonium persulphate solution reduced the problem of seed layer over-etching.

4.3.4 RF Sputtering

Sputtering the copper and chromium layers for the top wafer was particularly challenging due to the presence of the sacrificial resist layer. Problems such as film delamination, cracking or bubble formation can arise due to resist overheating. The cause of bubble formation was narrowed down to an insufficient hard-baking time for

the sacrificial resist. Even if a good seed layer is obtained by using the right sputter parameters, the presence of remnant solvent in the sacrificial resist can still result in bubble formation during subsequent processing. Figure 4.14(a) shows bubble formation in the sacrificial layer when hard-baking the first electroplating mould. The bubbles completely destroy the wafer features and no further processing is possible. By baking the sacrificial resist for an hour in the oven at 130 °C prior to sputtering the seed layer, the issue of resist bubbling was eliminated.

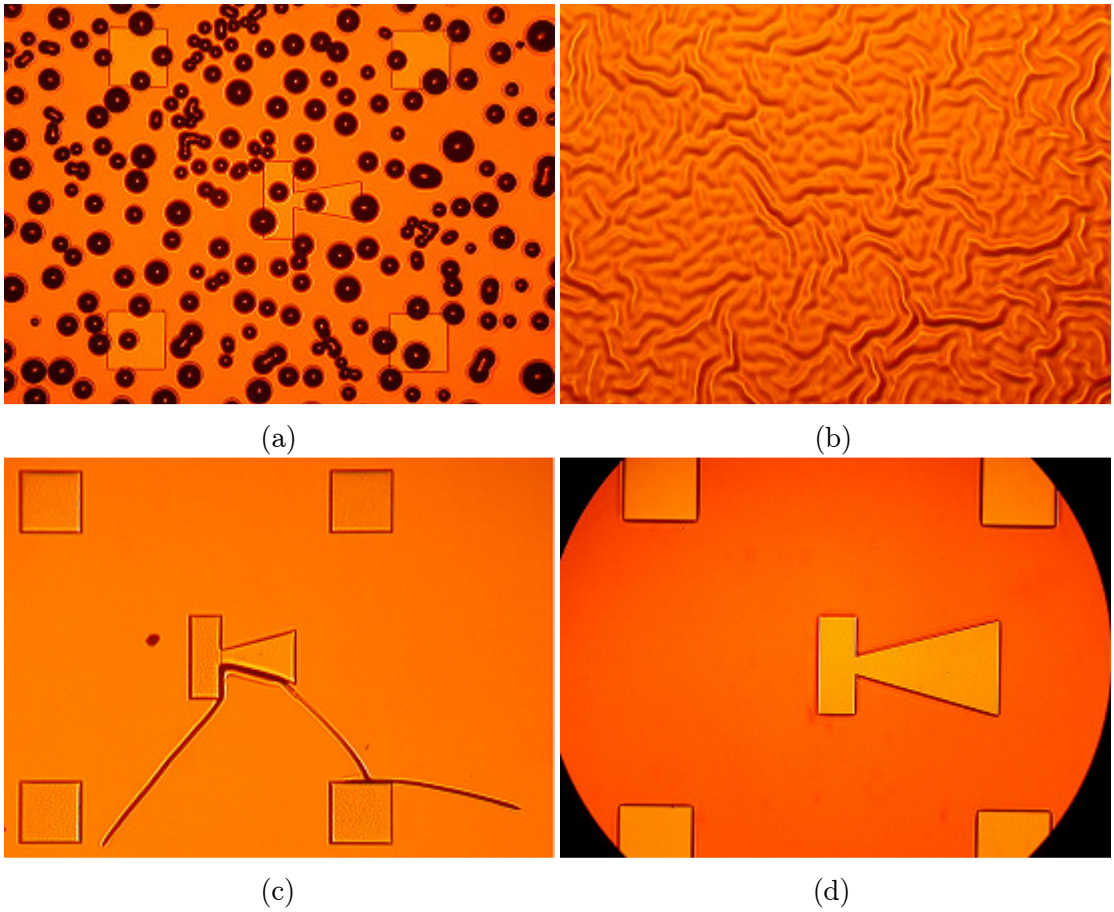


Figure 4.14: Cr/Cu sputtering issues: (a) bubbling in sacrificial layer; (b) delamination due to overheating; (c) cracking in seed and sacrificial layers; (d) good top wafer structures.

For sacrificial resist that has been thoroughly hard baked, film delamination can occur during sputtering if the wafer is overheated (see Figure 4.14(b)). In order to prevent overheating, an intermediate cooling step is included for both the chromium and copper deposition. Instead of sputtering continuously for 8 minutes at 400 W RF power, the wafer is exposed to 4 minutes of deposition and then shielded using a substrate shutter for 5 minutes. This allows the water-cooled substrate to cool down

before sputtering the wafer for a further 4 minutes to obtain the required film thickness. The same sputtering method is used for both the chromium and copper layers. Based on experimental investigation, the continuous sputtering time should not exceed 4 minutes as delamination occurred in some glass wafers that were sputtered with 5-minute deposition steps. Since there is no straightforward method for measuring the wafer surface temperature in real time, it was not possible to record the thermal history of the wafers in relation to various sputtering recipes. Another possible method for reducing the heat evolved during sputtering would be to reduce the RF power. However, this would require a longer deposition time for a given film thickness.

Another process issue to overcome was stress control in the sputtered copper and chromium layers of the top wafer. This is critical for achieving a specified amount of curvature in the cantilever. Since the required stress is tensile, cracking can occur when the stress exceeds a critical level. The initial wafer with only the sacrificial resist and the sputtered layers is relatively resistant to cracking. However, once the device features are added, cracks can initiate from regions of high stress concentration (e.g. at sharp corners) as shown in Figure 4.14(c)). To overcome the problem of film cracking, it was necessary to either reduce the film stress or to increase the overall fracture toughness, thereby increasing the critical fracture stress. A combination of both strategies was adopted. The film stress was reduced slightly by shortening the deposition time. To increase the fracture toughness of the thin film stack, the thickness of the sacrificial layer was reduced from 1.7 μm to 0.5 μm. Linear elastic fracture mechanics predicts that the critical stress intensity factor, K_c, at which crack propagation occurs is dependent of the specimen thickness [149]. For thin films in the plane stress regime, K_c increases with decreasing film thickness and hence it is advantageous to have a thinner sacrificial layer. Film cracking was successfully eliminated after modifying the fabrication parameters and crack-free processing was possible, as shown in Figure 4.14(d), using a 0.5 μm thick sacrificial resist.

To provide a quantitative measure of the stress levels in the sputtered film, a custom made device for measuring film stress was employed to provide an estimation of the film stress magnitude. The device consists of two polytetrafluoroethene (PTFE) clamps with a 22 by 22 by 0.1 mm borosilicate glass cover slip held in place (see Figure 4.15). Before film deposition, one side of the cover slip is clamped and its end height is measured using a digital dial indicator attached to a high magnification microscope. Care was taken to ensure that there is some initial end height and the

initial curvature of the cover slip is positive (i.e. curved upwards) otherwise the measured increase in end height would be inaccurate. Next, the free end is clamped down using a second clamp to ensure good contact with the aluminium base plate. When sputtering the chromium and copper onto the top wafer, the device is loaded alongside the wafer on the substrate platen. After deposition, the second clamp is released and the end height of the cover slip is measured again. The increase in the end height after film deposition is used to estimate the tensile stress of the film.

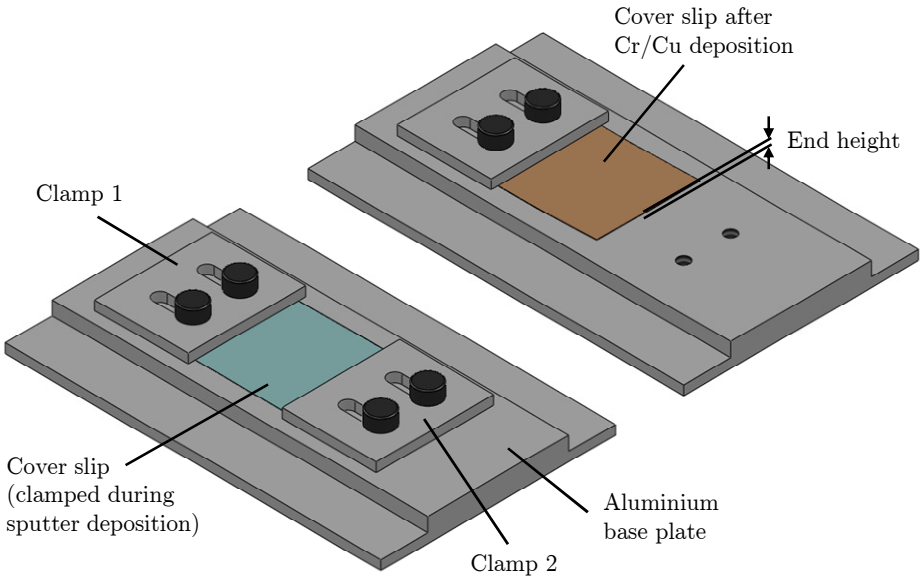


Figure 4.15: Device for measuring stress in sputtered films.

Although the stress measured by the tool will be different to the actual film stress on the wafer due to differences in substrate thermal conductance, the measurements are useful for process development. By changing deposition times, the change in stress can be monitored indirectly. The repeatability of the stress magnitudes obtained can also be tested from run to run when the deposition parameters are kept constant. Achieving process consistency is particularly challenging in a research environment where the sputter coater is used to deposit and etch a variety of metals and dielectrics. In addition, various polymers are also frequently used as deposition substrates and hence chamber contamination could be an issue. To improve consistency, a conditioning sputter run with an empty substrate platen is performed before the actual deposition. Subsequently, the chamber is vented and then loaded with the device wafer for the actual sputter deposition.

The measured stress for three different runs with identical deposition parameters are shown in Table 4.3. For each of these wafers, the chromium and copper layers are deposited in two steps of 4 minutes with 5 minutes of cooling in between (400 W RF power). The conditioning runs consisted of a 5-minute deposition on the shutter followed by a 5-minute deposition on the empty substrate platen for both copper and chromium.

Table 4.3: Stress in sputtered Cr/Cu layers.

Wafer Number	Initial End Height [μm]	Final End Height [μm]	Displacement [μm]	Stress [MPa]
WTG-18	300	370	70	180
WTG-19	280	380	100	250
WTG-20	225	300	75	190

4.4 Assembly Optimisation

Apart from process related challenges, several problems were also encountered at the assembly stage. Issues such as poor bonding success rate, bonding-induced damage and a lack of mechanical reliability in the assembled dies each affected the varactor yield to some degree.

4.4.1 Thermosonic Bonding

One of the main reasons for low bonding success was due to sliding between the top die and the vacuum chuck of the bonding tool. A schematic cross-section of the bonding tool is shown in Figure 4.16. Due to the lack of mechanical constraints, slipping can occur when the ultrasonic energy is applied especially if the vacuum suction on the die is weak. To improve the efficacy of the vacuum chuck, a more powerful pump was introduced and leaks in the pumping line were eliminated. In order to increase the bonding success further, a new tungsten carbide bonding tool has been introduced. As shown in Figure 4.16, a recess on the vacuum chuck provides a rigid hold on the top die and hence the coupling of the ultrasonic energy will be significantly better. This bonding tool will be used for future device assembly.

The second difficulty associated with the bonding process is that there is a trade-off between the requirement for sufficient die clearance (see Figure 4.3(c)) and the need to minimise the initial gap (i.e. y-offset) for lower actuation voltages. For example, bump heights in flip-chip applications are on the order of 100 μm while the additional height at the varactor anchor (and stabilising bumps) is only 0.5 μm. Although it is particularly challenging to find the optimum bump height in this application, preliminary results indicate that bonding success with an anchor thickness of 0.5 μm relative to the cantilever thickness, and a dielectric thickness of 0.2 μm (i.e. a y-offset clearance of 0.3 μm) was possible.

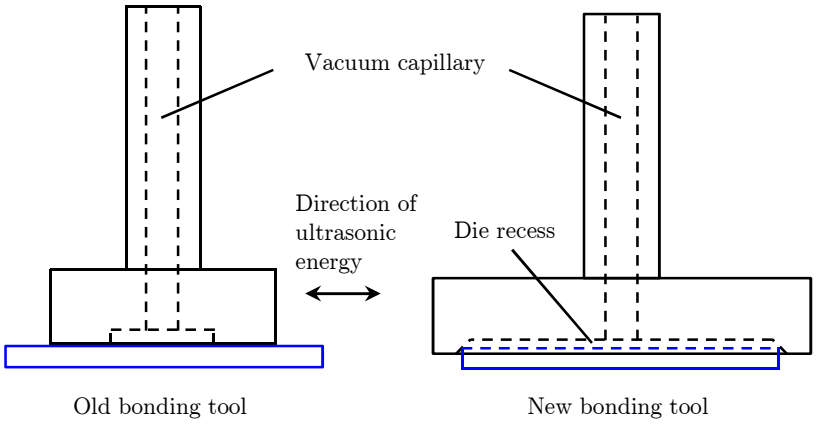


Figure 4.16: Tungten carbide bonding tools.

4.4.2 Mechanical Reliability of Assembled Dies

Despite the improvements to the bonder, assembly-related damage in the varactors remained prevalent. Figure 4.17 shows an example of a varactor that is damaged at the anchor. Re-evaluation of the die design revealed that the number of bumps was inadequate to support the mass of the top die during subsequent handling. In addition, the location of the bumps was also non-ideal and the mass of the top die impose a large load on the device.

Figure 4.18(a) shows the old version of the device dies, each consisting of a single device bump and four 250 by 250 μm supporting bumps. The four bumps were located within an area 1.5 by 1.5 mm and the anchor of the varactor is at the centre of the dies. Since the top die is 7.1 by 7.1 by 0.5 mm, the assembled device is vulnerable to handling damage when transferring the dies to the solvent bath for device release.

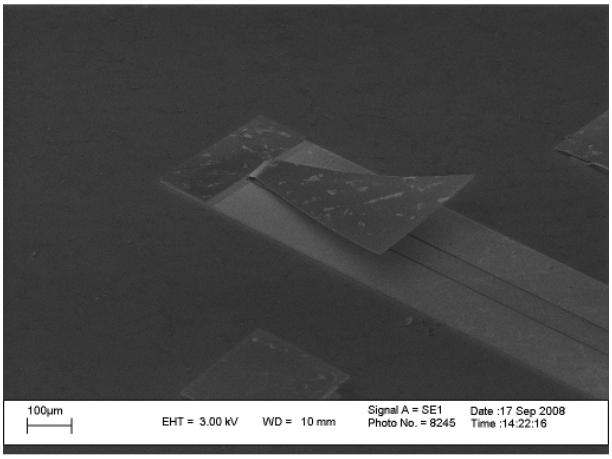


Figure 4.17: Varactor anchor damaged during assembly.

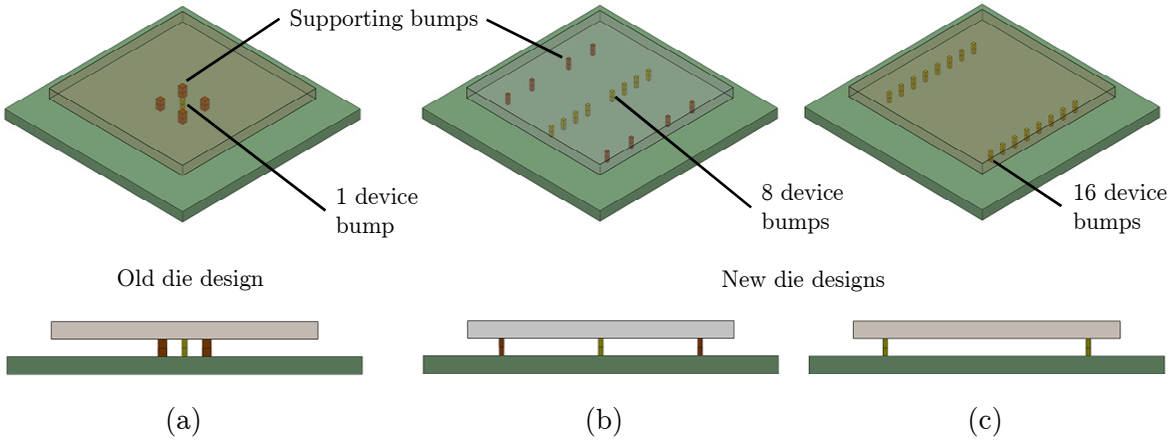


Figure 4.18: Varactor die designs showing isometric and front views: (a) old version with one device and four supporting bumps; (b) new series varactor die with 16 bumps (8 devices); (c) new shunt varactor die with 16 bumps (all devices).

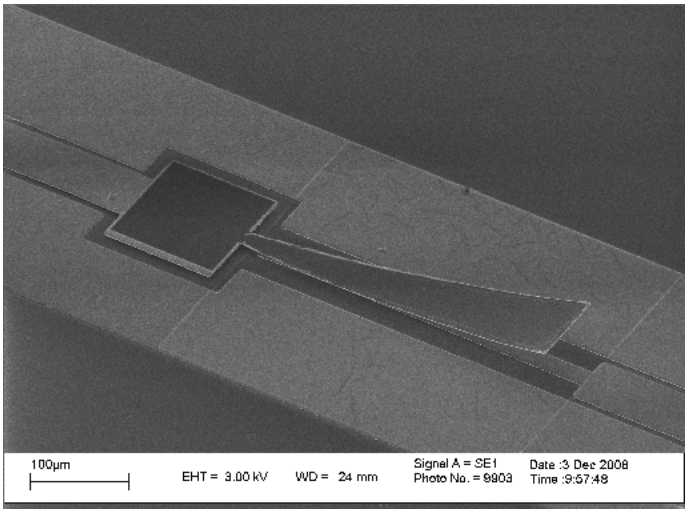
To improve device yield, the position of the bumps were adjusted as shown in Figure 4.18(b), (c). For the zipping varactor prototypes, both shunt-mounted and series-mounted devices have been included in the same mask set. For the shunt-mounted devices, the variable capacitance is from the signal line to ground, whereas in the series-mounted devices, the variable capacitance is along the signal line.

All dies for the new versions have sixteen 130 by 130 µm bumps spread over a much larger area, i.e. 5.84 by 4.89 mm and 5.72 by 5.59 mm for shunt and series device versions, respectively. Although the total bump area is slightly smaller in the newer design, the bumps are located nearer to the edge of the top die, making the assembled dies mechanically more robust. The total bond area was designed to be 0.27 mm^2 so that the load on the bonding stage does not exceed 3.5 kg-force. In

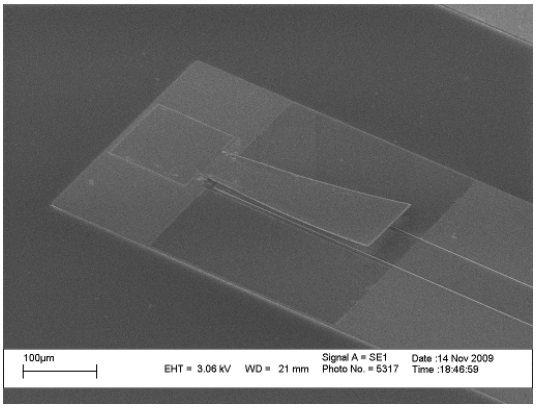
addition, the new dies have either eight series or sixteen shunt varactors and this significantly improved device yield.

4.5 Summary

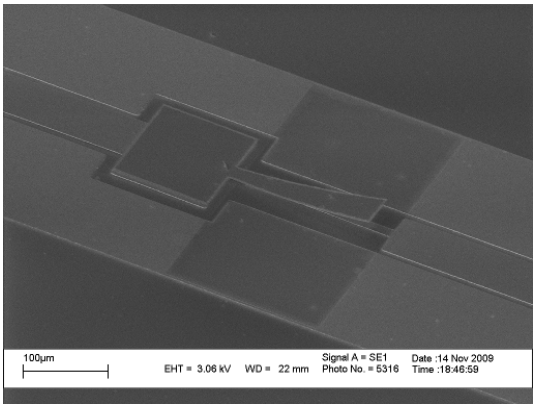
A repeatable fabrication and assembly process has been developed for zipping varactor prototypes. Examples of working devices are shown in Figure 4.19 below. The experimental characterisation and performance of these varactors will be reported in the next chapter.



(a)



(b)



(c)

Figure 4.19: Zipping varactor prototypes: (a) series device ($l = 400$ µm); (b) shunt device ($l = 300$ µm); (c) series device ($l = 200$ µm).

The varactor fabrication process is still being optimised and further improvements will be made in the future. A two wafer process was adopted so that in the next stage of varactor development, the bottom wafer can include a high-permittivity dielectric material while the top parts of the varactor can be fabricated using the existing process. Therefore, although a decrease in yield is inevitable in the assembly process, splitting the fabrication across two wafers simplifies the process for each wafer and decreases development time.

Due to the low yield associated with the thermosonic bonding step, a solder assembly method is being developed to improve fabrication yield in the short term. The existing process can be modified to include solder bumps at the anchor and the top and bottom device parts can be assembled via solder reflow. In the long term, a monolithic process can be developed for fabricating the zipping varactors. An application specific, integrated process would be a good way of improving device yield.

Another improvement to the current process flow would be to use a dry release method via laser ablation of the sacrificial resist. After device assembly, the cantilever can be released by firing a krypton fluoride laser (248 nm wavelength) through the top carrier die. The top wafer process, which was initially developed using soda lime glass substrates, has been successfully adapted to a UV-transparent fused silica substrate. By using a laser release process, the wet release and freeze-drying steps can be excluded.

To improve thermal and mechanical reliability, the cantilever structure can be modified to use a single material instead of multiple materials. At present, the cantilever consists of chromium (50 nm), copper (150 nm), nickel (60 nm) and gold (around 1 μm). Curved cantilever structures made purely of gold have been reported [150]. By controlling the stress in two separate layers of electroplated gold, a suitable curvature can be achieved. Another alternative would be to use a sputtered or evaporated gold seed layer with residual compression [151] and electroplate relatively stress-free gold as the upper layer of the cantilever. The chromium and copper stressed layers were chosen essentially for prototyping convenience since the chromium and copper etchants have good selectivity over gold.

Chapter 5

Varactor Characterisation

The experimental characterisation of the fabricated zipping varactor prototypes is reported in this chapter. Possible reasons for the differences between measured and modelled C-V characteristics are discussed. Finally, the measured Q-factor of a zipping varactor prototype is discussed and compared with predicted results from simulation.

5.1 RF Measurements

To evaluate the RF performance of the zipping varactors, the S-parameters of the varactors have been measured between 0.1 and 8.5 GHz. The results from a varactor identical to that listed in Table 3.1 are presented in detail.

5.1.1 Experimental Setup

Figure 5.1 shows a schematic of the measurement setup where the device under test (DUT) is a zipping varactor with its CPW feed lines. The S-parameters were measured using an Agilent E5071B vector network analyser and a Cascade Microtech Summit 9000 probe station fitted with 100-µm-pitch ground-signal-ground probes. A two-port short-open-load-through (SOLT) calibration [152] was performed prior to taking measurements. The short, load and through measurements were obtained from an impedance standard substrate (Cascade Microtech 101-190B) and the open measurement was taken with the probes in air [153].

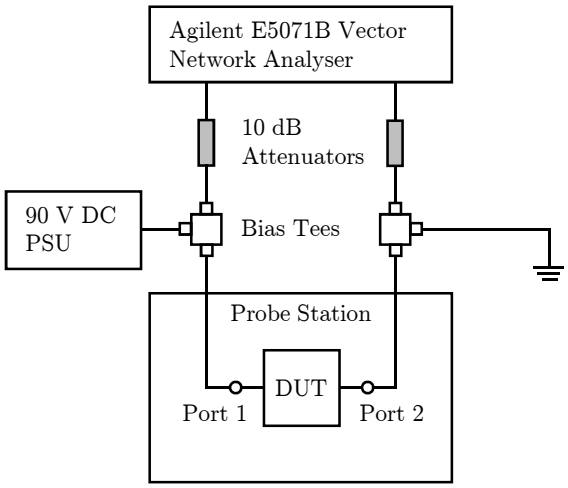


Figure 5.1: RF characterisation setup.

The varactors were actuated by applying a DC bias through the RF probes using bias-tees. Three 30 V DC power supply units (PSU) were connected in series to provide bias voltages up to 90 V. To protect the network analyzer from any high-voltage transients, 10 dB attenuators were connected between the RF ports and the network analyzer.

CPW test structures have been fabricated on the same wafer as the zipping varactors and characterised for the purpose of de-embedding the varactor feed lines. The CPW feed lines are 2 mm long and the test structures are of an equal length. The measured S_{21} magnitude for a 400 µm long series varactor (including CPW feed lines) is shown in Figure 5.2, where the bias was increased from 0 to 46 V.

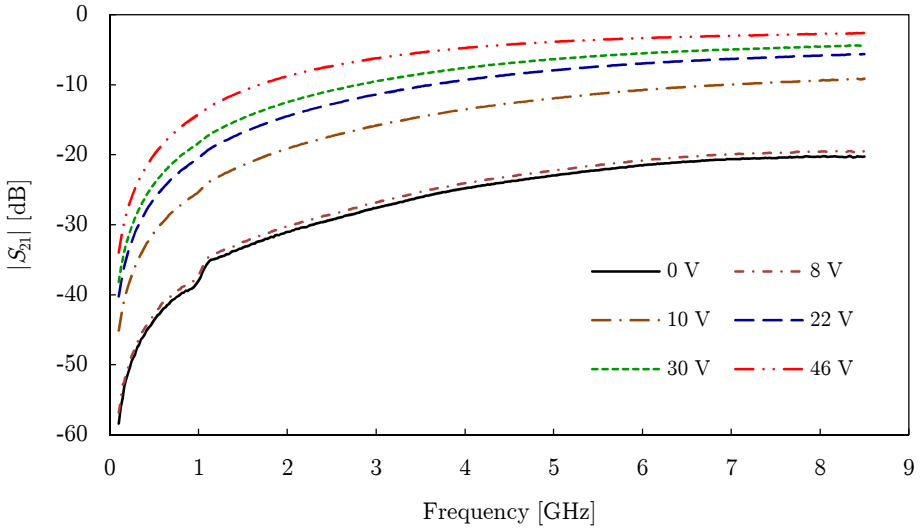


Figure 5.2: Measured $|S_{21}|$ for 400 µm series varactor (including CPW lines).

5.1.2 Equivalent Circuit Model

To extract the intrinsic device capacitance, an equivalent circuit model has been constructed using Microwave Office 2006 and fitted to the measured *S*-parameters. The equivalent circuit model is shown in Figure 5.3, consisting of both lumped elements and distributed transmission line elements. The elements Z_l represent the lossy CPW feed lines between Port 1 and reference plane **A**, and between Port 2 and reference plane **B**. The properties of Z_l were fitted to the *S*-parameters measured from the CPW test structures (60 μm signal width and 10 μm gap). Z_a represents the anchor region of the varactor modelled as a CPW element with a signal width of 130 μm and a gap of 20 μm. The actuation electrode is modelled with element Z_e, representing a CPW with a signal width of 20 μm and a gap of 30 μm.

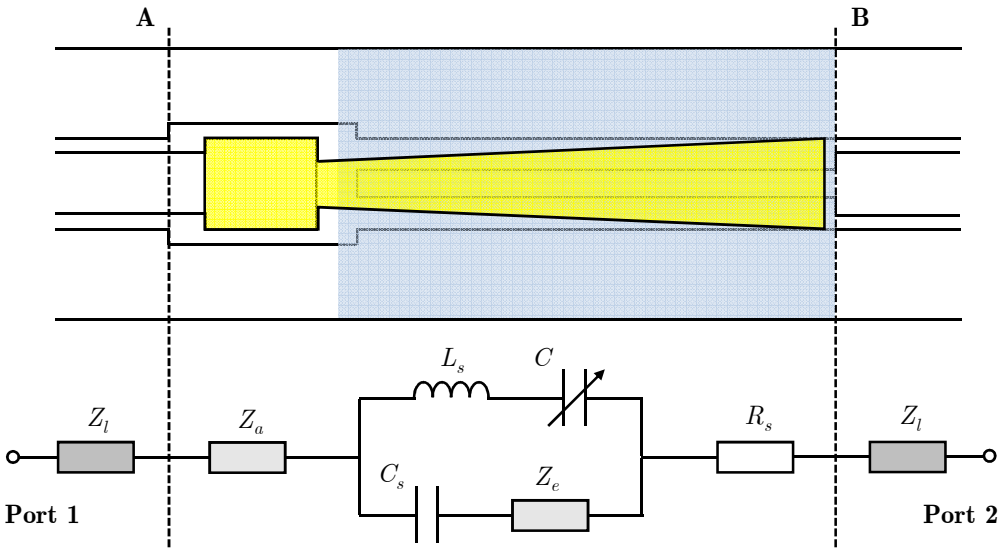


Figure 5.3: Series varactor layout and its equivalent circuit model.

The element C_s, with a value of 5 fF, represents the small series capacitance introduced by the break in the signal line between the anchor and fixed electrode. L_s is the inductance of the cantilever and has a value of 0.2 nH, and R_s is a series resistance with a value of 0.1 Ω. These values are obtained by manually fitting the *S*-parameters of the model to the measured data. The parameter-extracted capacitance of the varactor is then obtained from the value of C at each bias value. Figures 5.4 and 5.5 show the fitted *S*-parameter magnitude and phase, respectively (at the minimum and maximum bias values).

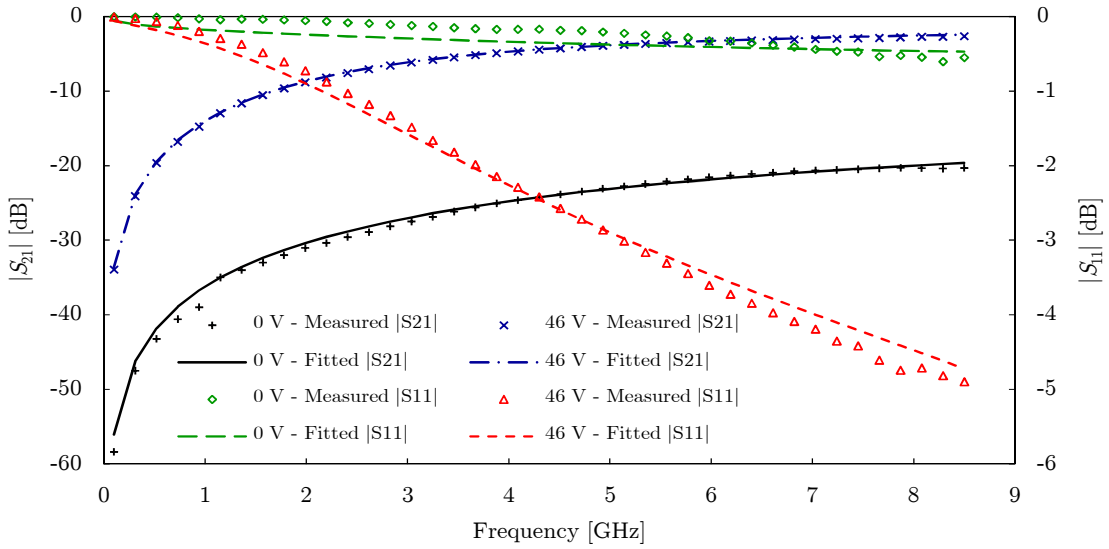


Figure 5.4: Measured and fitted *S*-parameter magnitude at extreme bias values.

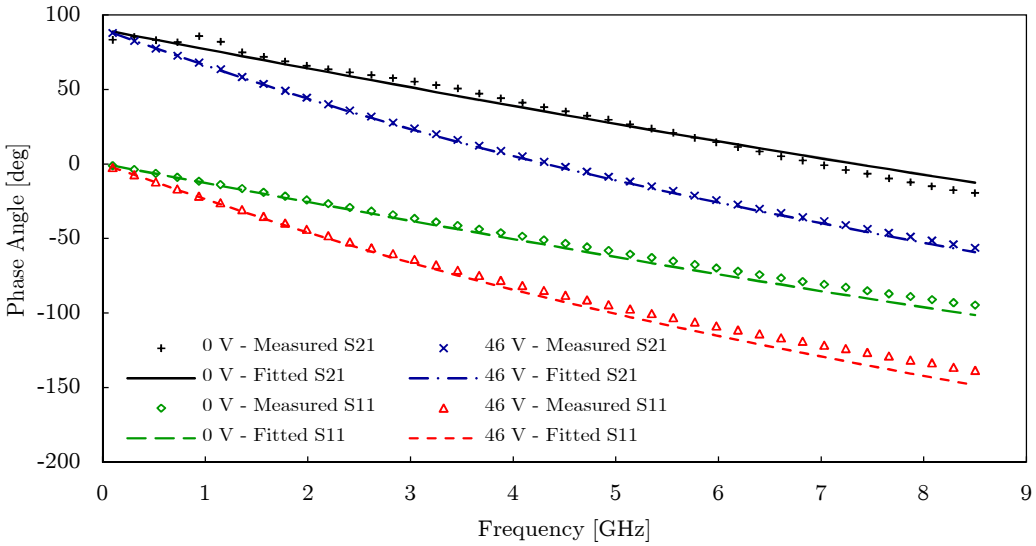


Figure 5.5: Measured and fitted *S*-parameter phase at extreme bias values.

5.1.3 Results

The parameter-extracted *C*-*V* characteristic of the zipping varactor is plotted in Figure 5.6. Capacitance values ranging from 20 to 329 fF were measured for bias voltages between 0 and 46 V, corresponding to a capacitance ratio of 16.5. When increasing the bias, the varactor exhibits tuning instability at 10 V as the cantilever touches the dielectric. This was predicted in the electromechanical modelling results. However, there is a second unexpected instability in the *C*-*V* characteristic between 30 to 32 V, where there is another unstable jump in capacitance.

Between 0 and 8 V, the varactor capacitance increases 15% (20 to 23 fF) as the cantilever is deflected downwards without zipping. Continuous tuning from 10 to 30 V, resulted in a capacitance increase from 92 to 207 fF (a TR of 125%). From 32 to 46 V, further tuning was obtained with an increase in capacitance from 297 to 329 fF (a TR of 11%).

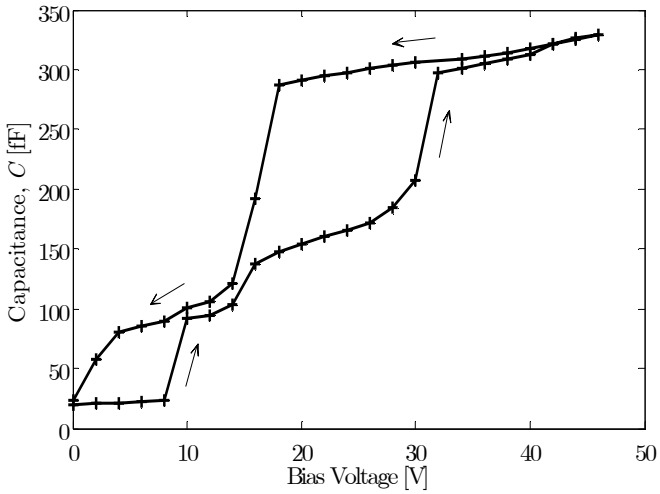


Figure 5.6: Measured C-V characteristic of zipping varactor prototype.

When the bias is decreased, the capacitance decreases continuously from 329 to 287 fF (15% TR) between 46 and 18 V. From 18 to 14 V, the capacitance decreases sharply from 287 to 121 fF and thereafter the capacitance decreases continuously to 24 fF when the bias voltage is reduced to zero. From 14 to 0 V, the best measured tuning range of the zipping varactor was obtained at 400%. The presence of an unexpected tuning instability resulted in added hysteresis in the C-V characteristic in a biasing cycle. Relative to the 3D varactor model, the bias voltages required for tuning are higher by a factor greater than 2. In addition, the maximum capacitance of 0.329 pF is lower than the Coventor model by a factor of 3.2.

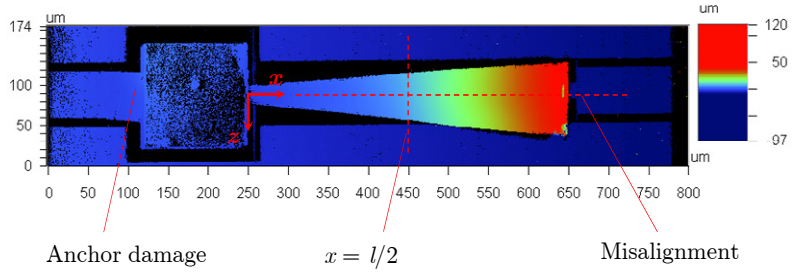
5.2 Discussion

The measured C-V characteristic of the zipping varactor shows that a large tuning range is possible as predicted by the modelling results. However, the tuning characteristics of these first generation varactors are still less than ideal. The differences between the measured and modelled varactor characteristics are due to the

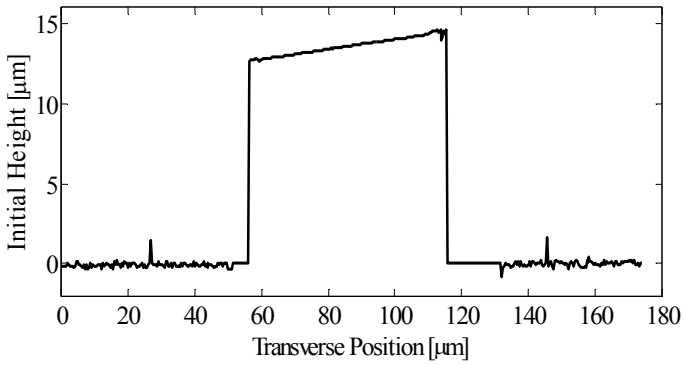
differences in device geometry arising from the fabrication process. In this section, the specific reasons for the higher bias voltages, lower capacitance and additional tuning instabilities are discussed. Subsequently, a modified 3D model is presented, taking into account some of the differences in model and prototype geometry.

5.2.1 Deviation from Idealised Geometry

An optical scan of the tested varactor revealed the presence of device imperfections arising from the fabrication and assembly process. Figure 5.7 shows the device contour obtained from a Wyko NT9100 white light interferometer. In the anchor region, the device has lifted off the substrate and is laterally displaced, leading to a z-offset misalignment in the cantilever relative to the actuation electrode. In addition, the assembly damage resulted in a 1.9° tilt in the cantilever, as shown in the transverse profile plot (see Figure 5.7(b)) for the varactor at zero bias.



(a)



(b)

Figure 5.7: Wyko scan of varactor: (a) misalignment in cantilever; (b) transverse profile at $x = l/2$.

Closer examination of the fixed electrode using scanning electron microscopy showed that the actuation electrode is also partially lifted-off from the substrate. Figure 5.8 shows an SEM image of the varactor where a slight arch is visible in the bottom electrode. This electrode lift-off could be a result of over-etching in the seed layers as well as the high electrostatic load arising from the DC biasing. The combination of the cantilever offset and tilting, together with the bottom electrode lift-off could be the reason in the additional tuning instability in the varactor.

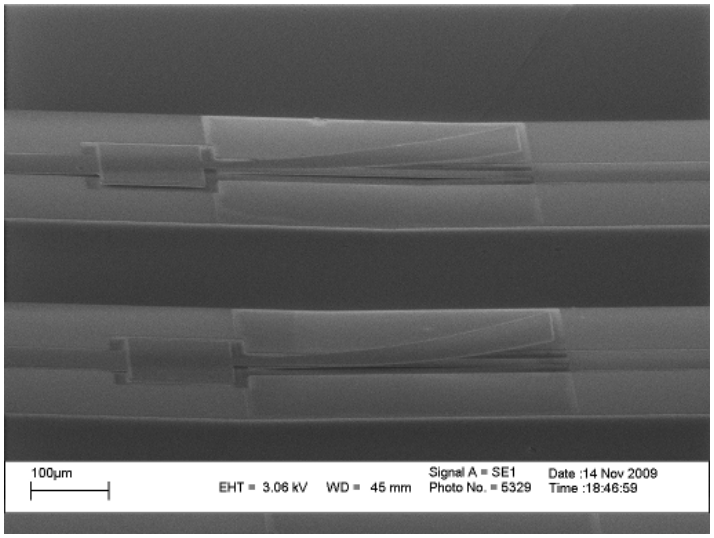


Figure 5.8: SEM image of tested varactors showing electrode lift-off from substrate.

The high bias voltages required for tuning the varactor could be due to a larger overall gap size between the cantilever and actuating electrode. However, the initial pull-in at 10 V is close to the simulated value of 11 V. This may be a result of the upward arch in the actuating electrode, reducing the local gap in that area. Nevertheless, the overall range of bias voltages required to tune the varactor fully (0 to 46 V) is much higher than the simulated values (0 to 18 V). By optimising parameters such as the anchor thickness, the curvature of the top electrode and the thickness of the cantilever, the bias voltage can be reduced.

A lower than expected capacitance in the varactor prototype could be due to a combination of roughness in the oxide and gold, and a lack of planarity in the dielectric contact surface. In addition, the density of the sputtered SiO_2 dielectric could also be lower than ideal. These factors result in a reduced effective dielectric constant and hence a lower varactor capacitance.

5.2.2 Modified 3D Model

To account for the effect of surface roughness and curvature in the bottom electrode, the Coventor model has been modified to include a curved surface in the actuating electrode. Figure 5.9 shows a cross-section of a dielectric-covered bottom electrode obtained from a Wyko scan. The profile of the original 3D model is also plotted where the dielectric surface was flat. In the actual device, the Au plating process results in a convex curvature in the electrode. When the SiO_2 dielectric is subsequently deposited, the layer conforms to the convex profile of the Au surface. Hence, this additional curvature results in a smaller device capacitance.

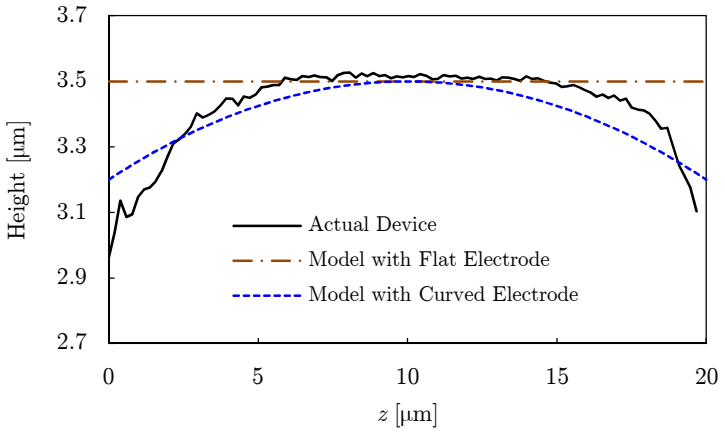


Figure 5.9: Cross-section of dielectric-covered bottom electrode.

In the modified Coventor model a parabolic bottom electrode curvature is introduced (see Figure 5.9), where the average height relative to the substrate is equal to the actual device (3.4 μm). The SiO_2 thickness is the same in the original model, device prototype and modified model (0.23 μm). From preliminary simulation results of the modified model, the effect of introducing a bottom curvature reduces the maximum capacitance from 1.00 pF to 0.52 pF, which is still a factor of 1.57 larger than the maximum capacitance of the prototype device. The reason for the lower capacitance in the actual device is the additional effect of roughness in the Au and SiO_2 contact surfaces. Furthermore, the effective dielectric constant of the SiO_2 could also be lower if there are defects or pores in the oxide film, resulting in a lower overall density.

By lowering the effective dielectric constant of the modified model from 4 to 2, the effects of surface roughness and reduced oxide permittivity can be accounted for and the maximum device capacitance is now similar to the measured device. The C-V characteristic of the modified model is plotted against the measured data in Figure

5.10. The remaining discrepancy between the model and prototype tuning behaviour is probably due to the assembly damage of the varactor (as discussed in sub-section 5.2.1) which has not been included in this model.

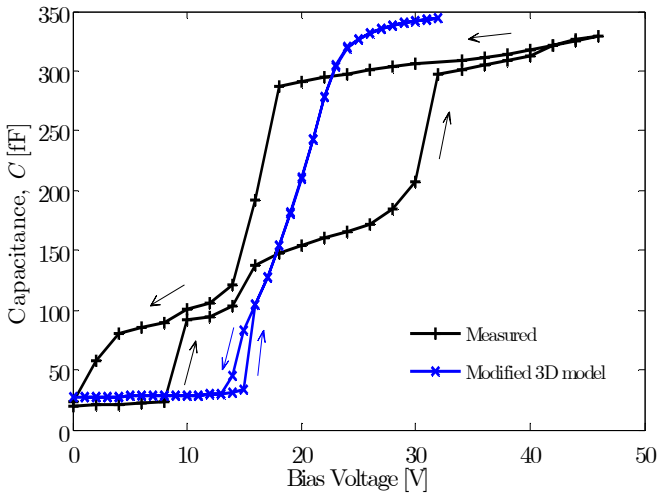


Figure 5.10: *C-V* characteristic of modified 3D model and varactor prototype.

5.3 *Q*-factor Measurement

Q-factor measurements were obtained from a varactor similar to the HFSS model listed in Table 3.4. This device was mounted in a shunt configuration as shown in Figure 5.11 and characterised using one port measurements. The differences in the actual varactor relative to the model include a thinner dielectric layer of 0.23 μm and a cantilever with multiple device layers, namely Au, Ni, Cu and Cr with respective thicknesses of 1.1, 0.06, 0.15 and 0.05 μm. The dielectric thickness in the HFSS model is 0.3 μm and the cantilever is a single 1.65 μm layer of Au.

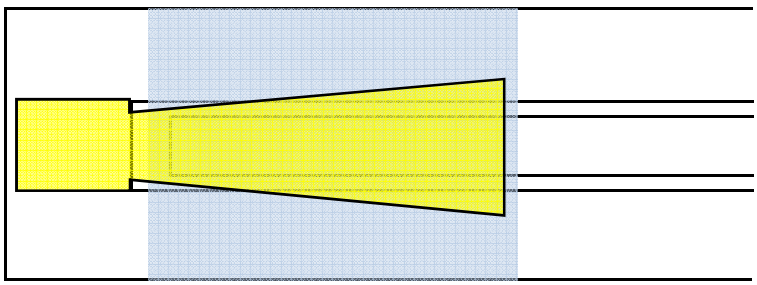


Figure 5.11: Shunt varactor layout.

To extract the varactor Q-factor, a series RC model is fitted to the measured S_{11} (excluding feed line). The Q-factor is then obtained from equation (3.35) for frequencies far below the electrical self-resonance. Figure 5.12 shows the Q-factor plotted against frequency when the device capacitance is 0.1 and 0.7 pF, respectively. For the unbiased varactor ($C = 0.1$ pF), the Q-factor at 2 GHz is 123. When the device capacitance is tuned to 0.7 pF, the Q-factor at 2 GHz is 69. The measured quality factors show reasonably good agreement with the HFSS results, where the simulated Q-factors at 2 GHz were 132 ($C = 0.07$ pF) and 98 ($C = 0.97$ pF). The slightly lower Q values in the actual device could be due to a higher cantilever series resistance, and dielectric (oxide and substrate) losses which were not accounted for in the model. Nevertheless, the measured values confirm that the zipping varactor design is capable of delivering low loss performance sufficient for most applications. The Q-factor plot in Figure 5.12(b) also shows that the first electrical self-resonance for this device is at 5.7 GHz when the capacitance is 0.7 pF.

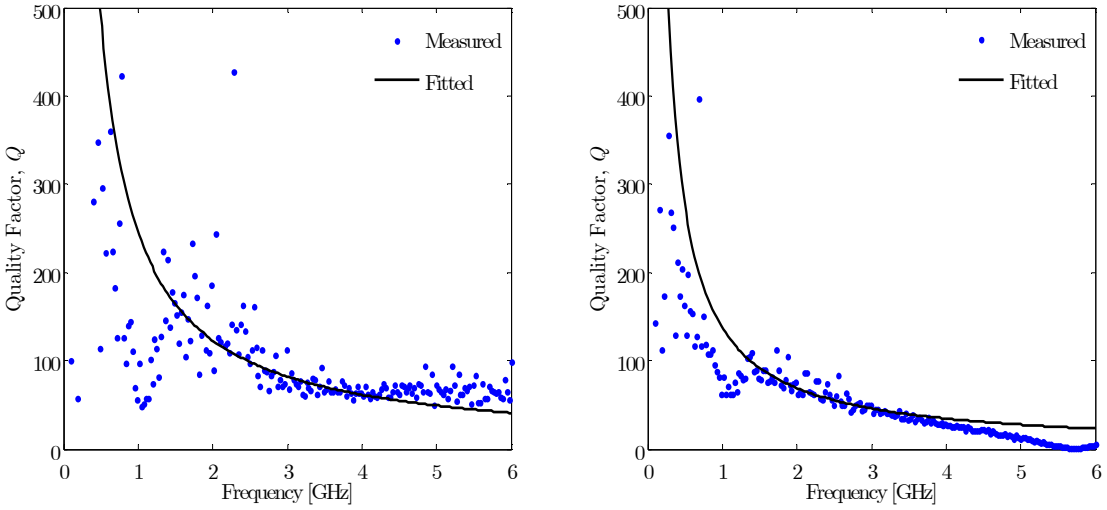


Figure 5.12: Zipping varactor quality factor: (a) 0.1 pF device capacitance; (b) 0.7 pF device capacitance.

The reported performance of the zipping varactors will be compared against other MEMS varactors in the concluding chapter. Based on the progress achieved in this work, future research directions are proposed.

Chapter 6

Conclusions

A novel micromachined zipping variable capacitor has been reported in this thesis. By using a tapered cantilever design to tailor the movable electrode's local stiffness, electrostatically-stable tuning has been demonstrated. The varactor has the potential of providing a large tuning range by allowing the cantilever to zip incrementally onto the dielectric surface. Gold electrodes with low series resistance are incorporated into the design and hence high Q-factors have been demonstrated. In addition, the varactor design is suitable for integrating a high-permittivity dielectric in order to achieve a greater tuning range within a small device footprint.

In Chapter 2, a detailed review of MEMS varactors has been presented. The advantages and disadvantages of different varactor designs have been weighed against various performance criteria, providing an objective summary of the state of the art. A varactor library was compiled from the literature survey to serve as a reference for selecting appropriate designs based on application requirements.

The design and electromechanical simulation of the proposed zipping varactor has been reported in Chapter 3. Three different models have been developed for the purpose of varactor design. An accurate 3D FEM/BEM model was employed to provide a reference solution for the varactor C-V characteristic. Two faster 2D models have been developed to supplement the computationally intensive 3D model for the purpose of rapid design analysis. The first 2D model is an approximate analytical model based on the method of total potential energy. The second 2D model combines an analytical approach with an FEM model, reducing the 3D geometry into 2D using an equivalent elastic modulus function.

Electromagnetic simulation results have also been presented in Chapter 3 in order to estimate the varactor Q-factor. The simulation results indicate that a high Q-factor can be achieved in the zipping varactor design with gold electrodes and an insulating glass substrate.

In Chapter 4, a process flow for varactor fabrication was reported. The process is based on surface-micromachining and is suitable for rapid-prototyping. Process repeatability has been established by addressing issues relating to photolithography, gold plating, wet etching of metals, metal sputtering and device assembly. Working varactors incorporating silicon dioxide as the dielectric layer have been successfully fabricated.

The experimental characterisation of zipping varactors was reported in Chapter 5. RF measurements were performed between 0.1 and 8.5 GHz and the capacitance of the varactor was parametrically extracted using an equivalent circuit model. For bias voltages between 0 and 46 V, the measurements show that the varactor has capacitance values between 20 and 329 fF. However, due to device defects arising from the fabrication, an additional tuning instability was introduced, leading to increased hysteresis in the C-V characteristic. Despite this, a proof-of-concept has been achieved and the potential for a large tuning range demonstrated. By modifying the 3D electromechanical model to account for curvature in the dielectric surface, and using an equivalent relative permittivity to account for roughness and dielectric imperfections, the accuracy of the simulation results can be further improved.

6.1 Zipping Varactor Performance

Relative to other zipping varactors, the varactor in this dissertation has a compact design comparable with [98], [100] and [103]. Although the measured TR of 400% is less than the varactors in [100] and [103] (600% and 500%, respectively), the simulation results in Figure 5.10 indicate that an improved TR of 660% (45.2 to 343.8 fF) is possible with the current design if the fabrication process is further optimised. In addition, the tuning range can be improved with the inclusion of a high-permittivity dielectric (see the simulation results in Figure 3.18(c)). Such a varactor could provide a tuning range exceeding current MEMS varactors, as well as a larger capacitance for a given device footprint.

The measured Q-factor (greater than 69 at 2 GHz) of this zipping varactor design is comparable with the state-of-the-art MEMS varactors. However, further improvement to the Q-factor can be obtained by increasing the thickness of the cantilever. Based on modelling results (see Figure 3.18(a)), it is possible to increase the cantilever thickness without adverse effects to the varactor's electromechanical performance. This will improve the loss performance of the varactor significantly.

Finally, one of the main advantages of this varactor is its non-complex design which is relatively easy to implement in a process flow. In addition, shaping a zipping cantilever in order to tailor its stiffness, and hence its C-V characteristic, has been demonstrated for the first time in an RF MEMS varactor. This design approach can be used to complement the shaping of the bottom electrode [94] in order to obtain desired tuning characteristics.

6.2 Future Work

At present, work is well in progress to integrate a high-permittivity PZT dielectric with the zipping varactor design. The process flows for both the top and bottom wafers have been successfully adapted to include the PZT dielectric and varactors will be assembled in the near future. The glass substrates have been replaced with fused silica to allow PZT annealing at around 500 °C (for the bottom wafer) and to open the option of using a dry laser release for the assembled device. In addition, the assembly method is being improved with the use of a new thermosonic bonding tool to increase assembly yield. An alternative method of device assembly using solder reflow is also being developed in parallel.

To improve the design process for the zipping varactors, the set of simulation tools can be further refined. For example, although no analytical solutions were obtained for the parabolic trial functions in the 2D semi-analytical electromechanical model, other trial functions could be used. It would be interesting to explore if a closed form solution could be obtained using a trial function in the form of an infinite series [129]. Such a solution may prove invaluable in terms quantifying the effect of various design parameters such as the cantilever's initial curvature, thickness, elastic modulus and the dielectric permittivity on the varactor C-V response. If a specific C-V characteristic is desired, e.g. a linear response, an optimisation algorithm can be employed to define the width function of the movable cantilever, or alternatively, the fixed electrode (see [95]).

Further work to develop a model for the zipping varactor's dynamic response with squeeze-film damping effects would be useful in predicting varactor tuning speeds at the design stage. The existing varactor prototypes could also be characterised experimentally to obtain a value for their damped natural frequency. If the same measurement is then performed in vacuum, the effect of vacuum sealing the varactor in a hermetic package can also be estimated.

In the longer term, the reliability of the zipping varactors has to be characterised and suitable design rules implemented to ensure an adequate device lifetime. In this area, the zipping varactor can benefit from the wealth of research already conducted for MEMS switches [50, 154] as well as touch mode actuators [155]. With additional attention, it is likely that the lifetimes of varactors with zipping designs can be extended to equal that of established MEMS switch designs.

With regard to the integration of zipping varactors in an application circuit, more detailed electromagnetic simulations would be required. In particular, the current varactor design has not been optimised for the highest possible Q-factor and it is anticipated that better performance can be expected with more detailed considerations to the varactor structure and layout. Furthermore, the varactor has to be simulated together with the surrounding RF passive elements and packaging (if applicable) to determine the overall performance. The capacitance values for individual varactors will also have to be scaled according to the application requirements.

At a more advanced stage of development, it would be beneficial to develop a monolithic process for the zipping varactors. Since the varactor has a simple structure, it is anticipated that adopting a monolithic process will be relatively straightforward. This will also improve the device yield which is necessary for reliable manufacturing. Finally, to improve thermal stability, an all-gold bi-layered cantilever structure can be adopted in future designs.

6.3 List of Publications

The following conference and journal papers are due in part to the work in this dissertation:

1. S. H. Pu, A. S. Holmes, E. M. Yeatman, C. Papavassiliou, and S. Lucyszyn, "Stable zipping RF MEMS varactors," Journal of Micromechanics and Microengineering, vol. 20, 035030, 2010.

2. S. H. Pu, A. J. Laister, A. S. Holmes, E. M. Yeatman, R. E. Miles, I. D. Robertson, and G. Dou, "High-Q continuously tunable zipping varactors with a large tuning range," in Proc. Asia-Pacific Microwave Conference, Hong Kong and Macau, China, 16-19 Dec, 2008.
3. S. H. Pu, A. S. Holmes, and E. M. Yeatman, "Design and simulation of zipping variable capacitors," in Proc. Micro Mechanics Europe Workshop, Guimaraes, Portugal, 16-18 Sep, pp. 147-150, 2007.

Appendix A

MATLAB Code for Semi-Analytical Varactor Model

```
% Model for varactor electromechanical behaviour. Based on the method of total
% potential energy. Implemented in MATLAB 7.4.0 (R2007a): requires symbolic math and
% optimization toolboxes.

% © Suan Hui Pu, Optical and Semiconductor Devices, Imperial College London
% Last modified: 23 Nov 2009

% Lower case for symbolic variables and upper case for device values

clear all;
tic                          % start timer

% Define symbolic math variables
syms x p q a c m k be d eps0 v te e h l;

b=p*x+q; % cantilever width function
sr=k*x^2/2;
cap0=be*eps0*int(1/(te+sr),x,d,l);

% Case 1: Deflected cantilever expressions when zipping has occurred (i.e. A > D)

sd1=c*(x-a)^2;
cap1=(a-d)*be*eps0/te + be*eps0*int(1/(te+sd1),x,a,l);
um1=int(1/24*e*b*h^3*(diff(diff(sr,x),x))^2,x,0,a)+...
    int(1/24*e*b*h^3*(diff(diff(sr-sd1,x),x))^2,x,a,l);
ue1=1/2*(a-d)*be*eps0*v^2/te + 1/2*be*eps0*v^2*int(1/(te+sd1),x,a,l);
pi1=um1-ue1;
dpi1_da=diff(pi1,a);
dpi1_dc=diff(pi1,c);
```

```
% Case 2: Deflected cantilever expressions when there is no zipping (i.e. A < D)

sd2=m*x^2;
cap2 = be*eps0*int(1/(te+sd2),x,d,l);
um2=int(1/24*e*b*h^3*(diff(diff(sr-sd2,x),x))^2,x,0,l);
ue2=1/2*be*eps0*v^2*int(1/(te+sd2),x,d,l);
pi2=um2-ue2;
dpi2_dm=diff(pi2,m);

% Substitute actual varactor values

S2=167;                     % Tensile stress in top layer [MPa]
L=400;                      % Length [um]
P=0.18;                     % Cantilever width parameter: linear gradient
Q=20;                       % Cantilever width parameter: width at x = 0
D=20;                       % Delta, offset for bottom electrode [um]

TD=0.23;                    % Actual dielectric layer thickness [um]
ER=4;                       % Dielectric relative permittivity - SiO2
TE=TD/ER;                   % Equivalent air thickness of the dielectric layer
EPS0=8.854e-6;              % Free space permittivity [pF/um]
BE=20;                      % Bottom electrode width, BE = Q

H1=1.1;                     % Thickness of bottom layer [um]
H2_CR=0.05;
H2_CU=0.15;
H2=H2_CR+H2_CU;             % Thickness of top layer [um]
H=H1+H2;                    % Total cantilever thickness

E1=80000;                   % Elastic modulus of bottom layer [MPa] - Au
NU1=0.42;                   % Poisson's ratio of bottom layer - Au
E2_CR=250000;
NU2_CR=0.22;
E2_CU=110000;
NU2_CU=0.36;
E2=(E2_CR*H2_CR+E2_CU*H2_CU)/H2;       % Elastic modulus of top layer [MPa] - Cr/Cu
NU2=(NU2_CR*H2_CR+NU2_CU*H2_CU)/H2;    % Poisson's ratio of top layer - Cr/Cu
EB1=E1/(1-NU1);             % Biaxial modulus of bottom layer [MPa]
EB2=E2/(1-NU2);             % Biaxial modulus of top layer [MPa]

D1=0.5*(E1*H1^2+2*E2*H1*H2+E2*H2^2)/(E1*H1+E2*H2);
D2=(H1+H2)-D1;
I1=H1^3/3-H1^2*D1+H1*D1^2;   % Moment of inertia per unit width [um^3]
I2=H2^3/3-H2^2*D2+H2*D2^2;
K=S2*(H2*D2-0.5*H2^2)/(EB1*I1+EB2*I2); % Cantilever curvature

NU=(NU1*H1+NU2*H2)/H;        % Poisson's ratio (thickness-weighted average)
E=(E1*H1+E2*H2)/H/(1-NU^2)   % Young's modulus (average) / (1-NU^2)

CAP0 = subs(cap0,{k,be,eps0,te,l,d},{K,BE,EPS0,TE,L,D});
results(1,1)=0;
```

```
results(1,2)=CAP0;
results(1,5)=K/2;

% Find stationary total potential energy by varying parameters a and c, or m

a0=L/10;                    % Initial values for optimisation algorithm
c0=K;
m0=K;

j=2;
for i = [0.5:0.5:18]        % Solve from 0-18 V
    V=i;
dpi1_da_V=subs(dpi1_da,{e,h,p,q,k,be,eps0,te,l,v,d},{E,H,P,Q,K,BE,EPS0,TE,L,V,D});
dpi1_dc_V=subs(dpi1_dc,{e,h,p,q,k,be,eps0,te,l,v,d},{E,H,P,Q,K,BE,EPS0,TE,L,V,D});

    % Code to write the two nonlinear equations in a and c to function eqns.m
    fid = fopen('eqns_tmp.m', 'wt');
    fprintf(fid, '%s\n', 'function dpi1 = eqns(g)');
    fprintf(fid, '%s', '% V = ');
    fprintf(fid, '%1.1f\n', V);
    fprintf(fid, '%s\n', 'a=g(1);');
    fprintf(fid, '%s\n', 'c=g(2);');
    fprintf(fid, '%s', 'dpi1 = [');
    fprintf(fid, '%s', char(dpi1_da_V));
    fprintf(fid, '%s', ';');
    fprintf(fid, '%s', char(dpi1_dc_V));
    fprintf(fid, '%s', '];');
    fclose(fid);
    copyfile('eqns_tmp.m','eqns.m'); % Tweak for fsolve to read the function file

options=optimset('Display','iter','MaxFunEvals',10000,'MaxIter',10000,'TolFun',1e-8);
    g0 = [a0;c0];           % Make a starting guess at the solution
    % Default fsolve algorithm is the "Trust-region dogleg" algorithm
    [g,fval,exitflag] = fsolve(@eqns,g0,options);
    A=g(1);
    C=g(2);

    if A < D
        disp('A is less than D, i.e. no zipping');

dpi2_dm_V=subs(dpi2_dm,{e,h,p,q,k,be,eps0,te,l,v,d},{E,H,P,Q,K,BE,EPS0,TE,L,V,D});
        % Code to write the nonlinear equation in m to function eqns2.m
        fid = fopen('eqns2_tmp.m', 'wt');
        fprintf(fid, '%s\n', 'function dpi2 = eqns(g)');
        fprintf(fid, '%s', '% V = ');
        fprintf(fid, '%1.1f\n', V);
        fprintf(fid, '%s\n', 'm=g(1);');
        fprintf(fid, '%s', 'dpi2 = ');
        fprintf(fid, '%s', char(dpi2_dm_V));
        fprintf(fid, '%s', ';');
        fclose(fid);
```

```
    copyfile('eqns2_tmp.m','eqns2.m');
    [g,fval,exitflag] = fsolve(@eqns2,m0,options);
    M=g;
    % Check that the potential energy function is a minimum at the stationary pt
    d2pi2_dm2=diff(dpi2_dm,m);
    pi2mm = double(subs(d2pi2_dm2,{m,e,h,p,q,k,be,eps0,te,l,v,d},...
        {M,E,H,P,Q,K,BE,EPS0,TE,L,V,D})); % Sub values, convert into number
    if pi2mm > 0
       disp('');
       N=0;
    else
       disp('Local minimum check failed; internal consistency error');
       N=1;
    end
    V
    CAP = subs(cap2,{m,be,eps0,te,l,d},{M,BE,EPS0,TE,L,D})
elseif A > D
    M=0;
    disp('A is greater D, i.e. there is zipping');
    % Check that the potential energy function is a minimum at the stationary pt
    d2pi1_da2=diff(dpi1_da,a);
    d2pi1_dc2=diff(dpi1_dc,c);
    d2pi1_dadc=diff(dpi1_da,c);
    pi1aa = double(subs(d2pi1_da2,{a,c,e,h,p,q,k,be,eps0,te,l,v,d},...
        {A,C,E,H,P,Q,K,BE,EPS0,TE,L,V,D})); % Sub values, convert into number
    pi1cc = double(subs(d2pi1_dc2,{a,c,e,h,p,q,k,be,eps0,te,l,v,d},...
        {A,C,E,H,P,Q,K,BE,EPS0,TE,L,V,D}));
    pi1ac = double(subs(d2pi1_dadc,{a,c,e,h,p,q,k,be,eps0,te,l,v,d},...
        {A,C,E,H,P,Q,K,BE,EPS0,TE,L,V,D}));
    if ((pi1aa > 0) && (pi1cc > 0) && (pi1ac^2 < pi1aa*pi1cc))
       disp('');
       N=0;
    else
       disp('Local minimum check failed; internal consistency error');
       N=1;
    end
    V
    CAP = subs(cap1,{a,c,be,eps0,te,l,d},{A,C,BE,EPS0,TE,L,D})
end
results(j,1)=V;
results(j,2)=CAP;
results(j,3)=A;
results(j,4)=C;
results(j,5)=M;
results(j,6)=N;

j=j+1;
a0=A;                    % Update initial values for faster convergence
c0=C;
m0=M;
```

```
    clear eqns;              % Clear current eqns function from memory
    clear eqns2;
end
toc                          % Display elapsed time
results

for i = 1:length(results)
    result_vb(i) = results(i,1);
    result_cap(i) = results(i,2);
end
figure;
plot(result_vb, result_cap, 'b+-');

% NB need to change formatting if CAP is value > 9.99..pF (e.g high-k deveice)
fid = fopen('results.csv', 'wt');
fprintf(fid, '%s\n', 'V,CAP [pF],A [um],C [um-1],M [um-1],N');
fprintf(fid, '%2.2f,%1.7f,%4.2f,%1.9f,%1.9f,%1f\n', results');
fclose(fid);
```

Appendix B

ANSYS Code for 2D FEM Varactor Model

```
! APDL script for 2D finite element model of zipping varactor with tapered cantilever
! Model elastic modulus, Em(x) corresponds to width function b(x)
! Implemented in ANSYS 11
! © Suan Hui Pu, Optical and Semiconductor Devices, Imperial College London
! Last modified: 15 Dec 2009

finish
/clear,start

/filname,2d_varactor_model
/num,1

! Geometry and material parameters
! Cantilever width function b(x)=px+q for x [0,l]

s2=167                          ! Tensile stress of top layer (MPa)
l=400                           ! Length (um)
be=20                           ! Bottom electrode width (um)
p=0.18                          ! Cantilever width parameter
q=be                            ! Cantilever width parameter
delta=20                        ! Offset between cantilever anchor and electrode (um)

td=0.23                         ! Dielectric layer thickness (um)
er=4                            ! Dielectric relative permittivity - SiO2
vmin=0.5                        ! Lowest voltage bias
vmax=18                         ! Highest voltage bias
vstep=0.5                       ! Voltage step size

h1=1.1                          ! Thickness of cantilever bottom layer (um)
h2_cr=0.05
```

```
h2_cu=0.15
h2=h2_cr+h2_cu               ! Thickness of cantilever top (tensile) layer (um)

E2_cr=250000
nu2_cr=0.22
E2_cu=110000
nu2_cu=0.36

E2=(E2_cr*h2_cr+E2_cu*h2_cu)/h2        ! Elastic modulus of top layer (MPa) - Cr/Cu
nu2=(nu2_cr*h2_cr+nu2_cu*h2_cu)/h2     ! Poisson's ratio of top layer - Cr/Cu

E1=80000                     ! Elastic modulus of bottom layer (MPa) - Au
nu1=0.42                     ! Poisson's ratio of bottom layer - Au

Eb1=E1/(1-nu1)               ! Biaxial modulus of bottom layer (MPa)
Eb2=E2/(1-nu2)               ! Biaxial modulus of top layer (MPa)

d1=0.5*(E1*h1**2+2*E2*h1*h2+E2*h2**2)/(E1*h1+E2*h2)
d2=(h1+h2)-d1
i1=h1**3/3-h1**2*d1+h1*d1**2 ! Moment of inertia per unit width (um^3)
i2=h2**3/3-h2**2*d2+h2*d2**2

! Geometry parameters of simplified 2D model

hm=h1+h2                     ! Model cantilever thickness
nu=(nu1*h1+nu2*h2)/hm        ! Model Poisson's ratio, thickness-weighted average

ne=160                       ! Number of element divisions along length
nt=1                         ! Number of elements across thickness

! Element size along length (choose esz to be a common factor of l and delta)
esz=l/ne
nk=4+2*(ne-1)                ! Number of keypoints used to define cantilever

*dim,sr,array,2*ne+1,2       ! Initial released profile of cantilever
*dim,bnode,array,2*ne+1,2    ! Bottom surface node x-coord and node numbers
*dim,emvalues,array,ne,2     ! Element x-coord and its equivalent modulus

! TRANS126(EMT) element parameters

eps0=8.854e-6                ! Free space permittivity (pF/um) - emtgen default value
airgap=0                     ! Initial air gap (um)
te=td/er                     ! Equivalent air thickness of the dielectric layer
gap=airgap+te                ! Initial dielectric gap
Ed=70000                     ! Elastic modulus of SiO2 dielectric (MPa)
knf=1                        ! Stiffness factor (1 = actual dielectric stiffness)

! Sketch cantilever geometry

/prep7
seltol,1e-08                 ! Set tighter tolerance for selection tool
```

```
kappa=s2*(h2*d2-0.5*h2**2)/(Eb1*i1+Eb2*i2)   ! Initial cantilever curvature

! Odd values of sr are keypoint locations, even values are for mid-pt nodes
j=1
*do,i,0,l,esz
  sr(2*j-1,1)=i              ! Store x-position in 1st column, profile in 2nd column
  sr(2*j-1,2)=kappa/2*i**2
  k,,i,sr(2*j-1,2)           ! Define keypoints for a parabolic cantilever profile
  k,,i,sr(2*j-1,2)+hm
  j=j+1
*enddo

j=1                          ! Coordinates of mid-pt nodes on bottom surface
*do,i,0,l-esz,esz
  sr(2*j,1)=i+esz/2
  sr(2*j,2)=(sr(2*j-1,2)+sr(2*j+1,2))/2
  j=j+1
*enddo

*do,i,1,nk-2                 ! Draw lines using keypoints
  lstr,i,i+2
*enddo
*do,i,1,nk-1,2
  lstr,i,i+1
*enddo

j=1                          ! Draw areas using lines.
*do,i,1,ne*2-1,2
  al,i,i+1,i+(2*ne-(j-1)),i+(2*ne-(j-1)+1)
  j=j+1
*enddo
aglue,all

! Meshing

et,1,183                     ! Plane stress quadratic element (ie unit thickness)

lsel,none                    ! Assign no of elem divisions lengthwise
*do,i,1,ne*2
  lsel,a,line,,i
  lesize,all,,,1
*enddo

lsel,none                    ! Assign no of elem divisions across thickness
*do,i,ne*2+1,ne*3+1
  lsel,a,line,,i
  lesize,all,,,nt
*enddo

mshape,0,2
```

```
j=1
*do,i,0,l-esz,esz
  bx=p*(i+esz/2)+q
  Em=12*bx*(E1/(1-nu1**2)*i1+E2/(1-nu2**2)*i2)/(hm**3*be)
  mp,ex,j,Em
  mp,nuxy,j,nu
  asel,s,loc,x,i+esz/2
  aatt,j,,1                  ! Assign Em(x) and element type 1 to all elements
  emvalues(j,1)=i+esz/2
  emvalues(j,2)=Em
  j=j+1
*enddo

allsel
amesh,all

! Mesh trans126 elements for air and dielectric region

mat,1000
*abbr,*uilist,/replot        ! To disable listing of _emtgen.out file

j=2*delta/esz+1
*do,i,delta,l,esz/2
  nsel,s,loc,x,i
  nsel,r,loc,y,sr(j,2)
  cm,node%i%,node            ! Bottom surface node component for emtgen (single node)
  bnode(j,1)=i               ! Store bottom surface node x-location
  *get,bnode(j,2),node,0,num,min    ! Store node number
  emtgen,'node%i%',,,'uy',-(sr(j,2)+gap),te,knf,eps0
  j=j+1
*enddo

*abbr,*uilist

j=2*delta/esz+1
nsel,none
*do,i,delta,l,esz/2
  nsel,a,node,,bnode(j,2)    ! Select all bottom surface nodes
  j=j+1
*enddo
cm,bnodecomp,node            ! Component for all bottom surface nodes

! Emtgen drops the real constants c0 and kn for trans126 elements when surface
! node component consists of only 1 node. Select bottom surface nodes only when using
! arnode() function.

j=2*delta/esz+1
area=0
*do,i,1,2*ne+1-2*delta/esz   ! Real constants 1 to 2*ne+1-2*delta/esz for trans126
  ndarea=arnode(bnode(j,2))
```

```
  c0=ndarea*eps0
  rmodif,i,7,c0
  kn=knf*Ed*ndarea/td
  rmodif,i,5,kn              ! Trans126 contact stiffness
  j=j+1
area=area+ndarea             ! Total area (unit width) of transducer elements
*enddo

*do,i,2,2*ne+2-2*delta/esz   ! Element types 2*ne+2-2*delta/esz are trans126
  keyopt,i,6,1               ! Use augmented stiffness option to aid convergence
  keyopt,i,4,1               ! Constrained DC voltage option
*enddo

save,meshed_model_ne%ne%_nt%nt%,db
finish

/solu
/title,b(x)=%p%x+%q%,S2=%S2%MPa,L=%l%,hm=%hm%um

eqslv,sparse
nlgeom,on
autots,on
neqit,1000
outres,all,all

cnvtol,f,,0.0001
cnvtol,u,,0.0001

! Boundary conditions

lsel,s,loc,x,0
dl,all,,ux,0
dl,all,,uy,0

nsel,s,loc,y,-gap
d,all,volt,0
d,all,uy,0

vb=0.0001                    ! Apply minute voltage for estimating C(0V)
cmsel,s,bnodecomp            ! C calculated indirectly from energy of trans126
d,all,volt,vb
allsel
keyw,pr_sgui,1               ! Turn-off 'Solution is done!' pop-up
solve

*do,vb,vmin,vmax,vstep       ! Solve for zipping - inc bias
  cmsel,s,bnodecomp
  d,all,volt,vb
  allsel
  solve
  *if,vb,eq,vmax-vstep,then
```

```
    keyw,pr_sgui,0
  *endif
*enddo

keyw,pr_sgui,1
*do,vb,vmax-vstep,vmin,-vstep    ! Solve for zipping - dec bias
  cmsel,s,bnodecomp
  d,all,volt,vb
  allsel
  solve
  *if,vb,eq,vmin+vstep,then
    keyw,pr_sgui,0
  *endif
*enddo
finish
save

! Post-process Results

/post1
*get,nsets,active,0,set,nset

! Calculate capacitance

*dim,results,table,nsets,2   ! Array for voltage and capacitance
nsel,s,loc,x,l
nsel,r,loc,y,sr(2*ne+1,2)
*get,vnode,node,0,num,max    ! Use voltage value at cantilever tip

esel,s,ename,,126
etable,sene,smisc,3          ! Element table for electrostatic energy stored in
trans126

*do,i,1,nsets                ! Store results for each substep
  set,i
  etable,refl                ! Refill element table with energies from this substep
  ssum
  *get,energy,ssum,,item,sene
  v=volt(vnode)
  results(i,1)=v
  results(i,2)=2*energy/(v*v)*be    ! Varactor capacitance
*enddo

*cfopen,results,csv
  *cfwrite,V,C
  *vwrite,results(1,1),results(1,2)
  (F8.4,',',F10.8)
*cfclos

/axlab,x,Voltage
/axlab,y,Capacitance
```

```
/gmarker,1,3,1
*vplot,results(1,1),results(1,2)
allsel

! Extract cantilever x-y profile

*dim,disp,array,2*ne+1,nsets*2  ! Displacements
*dim,sd,array,2*ne+1,nsets*2    ! Deflected profile

path,bsurf,2*ne+1,6,1           ! Results path along bottom surface
j=1
*do,i,0,l,esz/2
  ppath,j,,i,sr(j,2)
  j=j+1
*enddo

*cfopen,deflection,csv
*do,i,1,nsets
  set,i
  pdef,ux,u,x
  pdef,uy,u,y
  paget,pathres%i%,table

  j=1
  *do,k,0,l,esz/2
    disp(j,2*i-1)=pathres%i%(j,5)      ! x-displacement, ux
    disp(j,2*i)=pathres%i%(j,6)        ! y-displacement, uy
    sd(j,2*i-1)=sr(j,1)+disp(j,2*i-1)  ! x-coord of deformed profile, sdx=srx+ux
    sd(j,2*i)=sr(j,2)+disp(j,2*i)      ! y-coord of deformed profile, sdy=sry+uy
    j=j+1
  *enddo

  v=volt(vnode)
  *cfwrite,'%v%V'
  *cfwrite,srx,sry,ux,uy,sdx,sdy
  *vwrite,sr(1,1),sr(1,2),disp(1,2*i-1),disp(1,2*i),sd(1,2*i-1),sd(1,2*i)
  (F12.5,',',F8.4,',',F8.4,',',F8.4,',',F12.5,',',F8.4)
*enddo
*cfclos
finish
save
```

Appendix C

Process Parameters

C.1 Bottom Wafer (Soda Lime Glass)

Fabrication Step	**Sub-steps**	**Parameters**
Sputter Seed Layer	Substrate clean	200W, 2min, P_{Ar}=4x10^{-3}mbar, 0.45kV
	Sputter 20 nm Cr	400W, 3min, P_{Ar}=4x10^{-3}mbar, 0.90kV
	Sputter 190 nm Cu	400W, 10min, P_{Ar}=4x10^{-3}mbar, 0.95kV
Lithography	Spin 4.4 μm S1828 resist	500rpm, 10s; 1000rpm, 40s (closed spin)
	Soft bake	90°C oven, 30min (set aside >2hr)
	Resist exposure (Mask B1)	65s; 7 ± 1 mW/cm^2 at λ=405nm
	Develop	MF319, 1–2min; gentle agitation; rinse
	Descum	RIE: 60sccm O_2, 100W, 50mTorr, 1min
	Hard bake	110°C oven, 60min
Measure Resist Thickness	Dektak	
Ni Plating	Etch surface copper oxide	10% H_2SO_4 immersion, 10–15s; rinse
	Plate 60 nm Ni	3mA/cm^2, 50°C, 1min; rinse
	Immerse in DI water	Proceed with Au plating w/o drying
Au Plating (CPW)	Plate 3.1 μm Au	[ECF64D] 3mA/cm^2, 50°C, 17.5min, 0.03 m/s agitation; rinse
Measure Ni/Au Thickness	Dektak	

Fabrication Step	**Sub-steps**	**Parameters**
Remove Resist Mould	Strip resist	Acetone immersion, 1–2min; rinse with IPA, then DI water
	Oxygen plasma clean	RIE: 60sccm O_2, 100W, 50mTorr, 1min
Etch Seed Layer	Etch Cu	6% ammonium persulfate (diluted 1 part to 4 parts H_2O), ∼3–5min; rinse
	Etch Cr	$K_3[Fe(CN)_6]$ etchant, ∼45–60s; rinse
	Oxygen plasma clean	RIE: 60sccm O_2, 100W, 50mTorr, 10min
Sputter SiO_2	Sputter 230 nm SiO_2	300W, 25min, cool 5min, 25min, P_{Ar}=4x10^{-3}mbar, P_{O2}=2x10^{-5}mbar
Lithography	Spin 4.4 μm S1828 resist	500rpm, 10s; 1000rpm, 40s (closed spin); resist covering oxide is ∼2.8μm
	Soft bake	90°C oven, 30min (set aside >2hr)
	Resist exposure (Mask B2)	75s; 7 ± 1 mW/cm^2 at λ=405nm
	Develop	MF319, 1–2min; gentle agitation; rinse
Etch SiO_2	Descum	RIE: 60sccm O_2, 100W, 50mTorr, 1min
	Etch oxide	RIE: 25/25/2sccm CHF_3/Ar/O_2, 200W, 30mTorr, 15min (DC bias >150V)
Remove Resist Mask	Oxygen plasma ash	RIE: 60sccm O_2, 200W, 50mTorr, 10min
	Strip resist	1165 solvent, 80°C, 30min; rinse
	Oxygen plasma clean	RIE: 60sccm O_2, 100W, 50mTorr, 1min
Measure SiO_2 Thickness	Dektak	
Spin Protective Resist	Spin S1828 resist	500rpm, 10s; 1000rpm, 40s (closed spin)
	Soft bake	60°C hotplate, 3min; ramp to 90°C 3min
Wafer Dicing	Mount wafer on backing	Heat backing gently (<90°C) and bond wafer using Crystalbond 555 adhesive.
	Dice wafer	Standard settings; speed 3 or 4 (fastest)
Die Cleaning	Strip resist and adhesive	[Individual dies] 1165 solvent, 80°C, 10min; rinse
	Oxygen plasma clean	RIE: 60sccm O_2, 100W, 50mTorr, 5min

C.2 Top Wafer (Soda Lime Glass/Fused Silica)

Fabrication Step	Sub-steps	Parameters
Wafer Preparation	Dehydration bake	150°C oven, 30min (allow to cool briefly)
Spin Sacrificial Resist	Spin 0.5 μm S1813 resist	500rpm, 10s; 4000rpm, 40s (closed spin)
	Soft bake	90°C oven, 30min
	Hard bake	130°C oven, 60min
Sputter Preparation	Chamber pre-conditioning	[No sample loaded] 400W, 5min shutter + 5min substrate platen for both Cr and Cu
Sputter Seed Layer	Sputter 50nm Cr	400W, 4min, cool 5min, 4min, P_{Ar}=4x10^{-3}mbar, 0.90kV
	Sputter 150nm Cu	400W, 4min, cool 5min, 4min, P_{Ar}=4x10^{-3}mbar, 0.95kV
Lithography	Spin 4.4 μm S1828 resist	500rpm, 10s; 1000rpm, 40s (closed spin)
	Soft bake	90°C oven, 30min (set aside >2hr)
	Resist exposure (Mask T1)	65s; 7 ± 1 mW/cm^2 at λ=405nm
	Develop	MF319, 1–2min; gentle agitation; rinse
	Descum	RIE: 60sccm O_2, 100W, 50mTorr, 1min
	Hard bake	110°C oven, 60min
Measure Resist Thickness	Dektak	
Ni Plating	Etch surface copper oxide	10% H_2SO_4 immersion, 10–15s; rinse
	Plate 60nm Ni	3mA/cm^2, 50°C, 1min; rinse
	Immerse in DI water	Proceed with Au plating w/o drying
Au Plating (Cantilever)	Plate 1.1 μm Au	[ECF64D] 3mA/cm^2, 50°C, 7.5min, 0.03 m/s agitation; rinse
Measure Ni/Au Thickness	Dektak	
Remove Resist Mould	Strip resist	Acetone immersion, 1–2min; rinse with IPA, then DI water
	Oxygen plasma clean	RIE: 60sccm O_2, 100W, 50mTorr, 1min
Lithography	Dehydration bake	90°C hotplate, 10min (cool briefly)
	Spin 4.4 μm S1828 resist	500rpm, 10s; 1000rpm, 40s (closed spin); mould depth at anchor is 3.3μm
	Soft bake	90°C oven, 30min (set aside >2hr)
	Resist exposure (Mask T2)	65s; 7 ± 1 mW/cm^2 at λ=405nm
	Develop	MF319, 1–2min; gentle agitation; rinse

Fabrication Step	Sub-steps	Parameters
	Descum	RIE: 60sccm O_2, 100W, 50mTorr, 1min
	Hard bake	110°C oven, 60min
Measure Resist Thickness	Dektak	
Au Plating (Anchor)	Plate 0.5 μm Au	[ECF64D] 3mA/cm^2, 50°C, 2.75min, 0.03 m/s agitation; rinse
Measure Anchor Thickness	Dektak	
Remove Resist Mould	Strip resist	Acetone immersion, 1–2min; rinse with IPA, then DI water
	Oxygen plasma clean	RIE: 60sccm O_2, 100W, 50mTorr, 1min
Etch Seed Layer	Etch Cu	6% ammonium persulfate (diluted 1 part to 4 parts H_2O), ∼2–4min; rinse
	Etch Cr	$K_3[Fe(CN)_6]$ etchant, ∼1.5–2min; rinse
Etch Sacrificial Resist	Oxygen plasma ash	RIE: 60sccm O_2, 200W, 50mTorr, 10min
Spin Protective Resist	Dehydration bake	90°C hotplate, 10min (cool briefly)
	Spin S1828 resist	500rpm, 10s; 1000rpm, 40s (closed spin)
	Soft bake	90°C oven, 30min (set aside >2hr)
	Flood exposure	300s
Wafer Dicing	Mount wafer on backing	Heat backing gently (<90°C) and bond wafer using Crystalbond 555 adhesive.
	Dice wafer	Standard settings; speed 3 or 4 (fastest)
Die Cleaning	Strip resist and adhesive	[Individual dies] MF319, 10–15min; rinse
	Oxygen plasma clean	RIE: 60sccm O_2, 100W, 50mTorr, 5min

C.3 Die-Level Assembly

Fabrication Step	Sub-steps	Parameters
Thermosonic Bonding	Heat bonder stage	180°C (actual temp. at die ∼160°C)
	Mount dies	Clamp bottom die on bonder stage; mount top die on bonder tool vacuum chuck
	Parallelism adjustment	Makes dies parallel using laser aligner
	Align and apply pressure	120 MPa (12 kgf/mm^2)
	Apply ultrasonic energy	18W; 200ms
Device Release	Remove sacrificial resist	1165 solvent, 80°C, 30min

Fabrication Step	**Sub-steps**	**Parameters**
	Immerse in DI water	Rinse very gently in DI water bath, then transfer to clean DI water bath
Freeze-Drying	Mount dies on spacers	
	Rinse in freeze-dry mixture	Use 9:1 distilled water to methanol mixture; Baths 1, 2 for rinsing and bath 3 for freeze-drying; invert dies to minimise drying residue
	Pump overnight	Pump/chill mixture gradually until frozen and leave to pump overnight.
Final Device Clean	Oxygen plasma clean	RIE: 60sccm O_2, 200W, 50mTorr, 10min

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