UNIVERSITY OF SOUTHAMPTON

An Analogue Approach for the Processing of Biomedical Signals

by

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A thesis submitted in partial fulfillment for the degree of Doctor of Philosophy

in the

Faculty of Engineering, Science and Mathematics

School of Electronics and Computer Science

March 2012

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

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SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

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Constant device scaling has significantly boosted electronic systems design in the digital domain enabling incorporation of more functionality within small silicon area and at the same time allows high-speed computation. This trend has been exploited for developing high-performance miniaturised systems in a number of application areas like communication, sensor network, main frame computers, biomedical information processing etc. Although successful, the associated cost comes in the form of high leakage power dissipation and systems reliability. With the increase of customer demands for smarter and faster technologies and with the advent of pervasive information processing, these issues may prove to be limiting factors for application of traditional digital design techniques. Furthermore, as the limit of device scaling is nearing, performance enhancement for the conventional digital system design methodology cannot be achieved any further unless innovations in new materials and new transistor design are made. To this end, an alternative design methodology that may enable performance enhancement without depending on device scaling is much sought today.

Analogue design technique is one of these alternative techniques that have recently gained considerable interests. Although it is well understood that there are several roadblocks still to be overcome for making analogue-based system design for information processing as the main-stream design technique (e. g., lack of automated design tool, noise performance, efficient passive components implementation on silicon etc.), it may offer a faster way of realising a system with very few components and therefore may have a positive implication on systems performance enhancement. The main aim of this thesis is to explore possible ways of information processing using analogue design techniques in particular in the field of biomedical systems.

The first such effort has been made for controlling a prosthetic hand using a novel Analogue Arithmetic Unit which can concurrently perform mathematical operations like addition, subtraction and multiplication using very few components. Novel control algorithms have been developed for controlling the prosthetic hand that have been implemented in analogue domain resulting an efficient system that enables the prosthetic hand to behave closely to a real hand.

Continuing our effort, new algorithm and analogue-based implementation have been carried out for detection of heart-beat anomaly. The designed algorithm allows the detection of heart electrical activity and can identify four heart beat anomalies as ventricular premature beats, ventricular tachycardia, atrial fibrillation and atrioventricular blocks. Such methodology can be implemented for non-invasive heart beat monitoring allowing the monitoring for home health care and ambulatory.

Subsequently, the characteristics of non-linear oscillators have been studied and modified for a new method of signal processing. Such methodology incorporates inherent dynamic plasticity and can perform frequency and amplitude extraction of external signals with only a few electronic components. The very first circuit implementation of these new models of non-linear oscillators have been implemented showing the advantages that these systems can provide in real-life signal analysis.

The present work demonstrates the feasibility of implementing efficient information processing systems in the analogue domain and at the same time shows that the system can be implemented with very few components; e.g., signal processing blocks as multipliers can be designed in the analogue domain with a total amount of $10 - 16$ transistors, while a 6 bit digital multiplier requires at least 42 full adders with carry in and carry out signals with a total of approximately 840 transistors. Therefore it may result into less silicon area and less operational power.

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Nomenclature

A_i	Extracted amplitude of the input sinusoid
C_{ox}	Gate oxide capacitance per unit area
f_{osc}	Frequency of the ring oscillator
I_{SS}	Current source
K	Gain
L	Transistor length
N	Number of inverters
R	Resistor
V_{GS}	Gate-source voltage
$V_{out,ECG}$	Processed ECG signal
$V_{TH,n}$	Threshold voltage for NMOS transistor
$V_{TH,p}$	Threshold voltage for PMOS transistor
W	Transistor width
β	Transistor current gain
Δ	Voltage difference between two inputs
θ	Phase shift
μ_n	Charge-carrier effective mobility, amplitude of oscillation
τ	Time delay derived by an inverter
ω	Angular frequency
ω_i	Intrinsic frequency component of an external perturbation
ω_0	Frequency component of an external perturbation

Glossary

AC	Alternating Current
ADC	Analogue to Digital Converter
AF	Atrial Fibrillation
ALU	Arithmetic Logic Unit
ASIC	Application-Specific Integrated Circuit
ASP	Analogue Signal Processor
AV	Atrio-Ventricular
BIOCAS	Biomedical Circuits and Systems
CAD	Computer Aided Design
CAB	Computational Analogue Block
CI	Cochlear Implant
CIS	Continuous Interleaved Sampling
CMOS	Complementary Metal-OxideSemiconductor
CPG	Central Pattern Generator
DAC	Digital to Analogue Converter
DBS	Deep Brain Stimulation
DC	Direct Current
DSP	Digital Signal Processing
DTL	Dynamic Translinear
ECG	Electrocardiogram/Electrocardiography
EEG	Electroencephalogram
EMG	Electromyography
FF	Flip-Flop
FFT	Fast Fourier Transform
FPAA	Field Programmable Analogue Array
FPGA	Field Programmable Gate Array

HDL	Hardware Description Language
IC	Integrated Circuit
LPAF	Low Power Analogue Front-end
MIPS	Million of Instructions Per Second
MOSFET	MetalOxideSemiconductor Field-Effect Transistor
NMOS	n-channel MOSFET
NN	Neural Network
OEL	Optimum Electrode Location
OTA	Operational Transconductance Amplifier
PLD	Programmable Logic Device
PMOS	p-channel MOSFET
RASP	Reconfigurable Analogue Signal Processor
RC	Resistor-Capacitor
RF	Radio Frequency
SA	Sino-Atrial
SDR	Software-Defined Radio
SNR	Signal to Noise Ratio
SPIC	Simulation Program with Integrated Circuit Emphasis
STFT	Short Time Fourier Transform
TI	Texas Instruments
TSMC	Taiwan Semiconductor Manufacturing Company
VHDL	Very high-speed integrated circuit Hardware Description Language
VLSI	Very Large Scale Implementation
VPB	Ventricular Premature Beat
VT	Ventricular Tachycardia
WGN	White Gaussian Noise
WT	Wavelet Transform

Acknowledgements

I would like to thank my supervisor Dr Koushik Maharatna for the privilege of working under his supervision. The teaching and time that I have spent with him have been precious not only for my career but also in life. I also deeply thank him for his time and his availability that he has towards everyone. I also gratefully acknowledge Dr. Peter Wilson for his useful comments during my Ph.D transfer and all the lecturers in the ECS department with whom I have had precious lectures which have helped me in all my work.

I would also like to thank all my friends and fellow mates Dave, Dirk, Anton, Evans, Hamed, Amit and Li for living these last few years together and helping each other by sharing ideas. And I deeply thank all my family for listening to me, encouraging me during the hard times and sharing a smile with me during the good times.

To all my family...

Chapter 1

Introduction

Transistors are rapidly scaling down, leading to an increase in the number of components within a chip. These continuous advances in digital electronics also involve several disadvantages for low power design systems where the reduction of the power supply interferes with the drive current of the transistors resulting in slower speeds [1] in addition to the complexity required for testing and manufacturing [2] [3].
In the last few decades a different approach for the design of electronic systems has been investigating alternative methods in the analogue domain, showing the advantages which derive by the mathematical interaction between electronic components to create systems of high complexity. Such mathematical properties obtained in the analogue domain can result in a lower area and power consumption [4] and can therefore be implemented in different areas such as medical devices for new retina implants, cochlear implants, electrocardiogram (ECG) monitoring devices and sensor devices where such parameters as power and area are more critical. Additionally, the demand for smaller circuits and lower power consumption has drastically increased in the area of medical care for remote health care monitoring.
Several research works in different fields have already proven the advantages of analogue signal processing: in 1988 a successful design presented by [5] showed how a set of electronic programmable cells, made of basic analogue components, could interact with each other in the field of visual computing to visualize images, detect edges and identify differences between images (as in boolean logic). Different models of cochlear implants has also been designed in the analogue domain showing how a configuration based on real biological cochlear configurations can be extremely efficient [6]; while, analogue Wavelet Transforms (WTs) have been designed for the detection and monitoring of electrocardiogram (ECG) signals [7].

1.1 Research Motivation

For the last three decades digital electronics has evolved very rapidly by scaling down the transistor dimensions down to the nano scale and therefore providing higher levels of processing. The design of portable and autonomous sensors systems is becoming more critical as these require a certain amount of computational power that necessitate to stay within a power budget limit. Gene Frantz, analogue electronic expert engineer at Texas Instruments (TI), declared that with the decrease of transistor sizes the computational efficiency (Operation Vs. Power) doubles roughly every eighteen months [8]. Furthermore, Mead [9] affirmed that analogue computation can provide a higher level of efficiency if compared to custom digital design; while, Sarpeskar [10] asserted that the cost of digital systems will be more expensive than analogue systems for low to moderate signal to noise ratio (SNR) levels. Furthermore, digital electronics is now reaching the limits set by the Moore's Law, and the increase of number of transistors is dramatically increasing the power consumption within devices; while, the level of signal processing in analogue electronics design is attributed by the physics laws which control the voltage and current flowing through each of the transistors and the interactions between components (as previously explained, the configuration of an analogue multiplier would only requires $10 - 14$ transistors against the 840 transistors for a digital 6 bit multiplier). Consequently, it is possible to affirm that analogue signal processing has been considered quite lately and is now better implementable with newer technologies and layout techniques. Furthermore, recent research and conferences such as the BIOCAS (Biomedical Circuits and Systems) and the Biennial Analog Signal Processing Conference (ASP) have shown a high increase of analogue design replacing some of the digital architectures for faster computation and more compact design. Therefore, for the reasons mentioned above, a number of applications (finalized to medical devices) will be explored in the analogue electronics domain showing the level of complex signal processing that can be obtained with a much lower number of components (when compared to digital electronics design). Hence, this work concentrates on developing different platforms for medical devices such as prosthetic hands, automated heart monitoring devices, and new analogue signal processing techniques which may be applied to medical signal processing along with other generic signal processing applications.

1.2 Contribution

The main contribution of this work is to provide more evidence against traditional modern electronics constraints which result in large silicon area, large computational power and processing speed. Therefore it will be demonstrated how the complexity of a system can dramatically be reduced (while maintaining the same computational power) when designed in the analogue domain.

Furthermore, additional contributions relate to different methodologies in the area of different medical devices as for the analysis and controlling of prosthetic hands, a new methodology for detecting and differentiating heart beat anomalies which can be incorporated into non-invasive portable devices and finally, two new methodologies for signal processing which can also be applied to biomedical signals and other applications (e.g. communications).
The following peer-reviewed publications have been generated from the research work carried out in this thesis:

Ahmadi, A., Mangieri, E., Maharatna, K., Dasmahapatra, S. and Zwolinski, M. (2011) On the VLSI Implementation of Adaptive-Frequency Hopf Oscillator. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMSI: REGULAR PAPERS, 58 (7).

Ahmadi, A., Mangieri, E., Maharatna, K. and Zwolinski, M. (2009) Physical Realizable Circuit Structure For Adaptive Frequency Hopf Oscillator. In: NEWCAS-TAISA'09, 28 June-1July 2009, Toulouse, France.

Maharatna, K., Ahmadi, A. and Mangieri, E. (2009) Biologically inspired analogue signal processing: some results towards developing next generation signal analysers. In: International Symposium on Integrated Circuits (ISIC2009), Singapore.

Mangieri, E., Ahmadi, A., Maharatna, K., Ahmad, S. and Chappell, P. (2008) A novel analogue circuit for controlling prosthetic hands. In: IEEE Biomedical Circuits and Systems Conference , November 2008, USA. pp. 81-84.

1.3 Thesis Outline

Chapter 2 provides an overview of the advantages and disadvantages provided by analogue and digital electronics systems. Furthermore, a background to the technology used in medical devices is also introduced.

Chapter 3 contains the implementation of an analogue fabric which has been defined as an analogue arithmetic logic unit (ALU). Such implementation, which can concurrently perform multiplication, addition and subtraction, has allowed us to improve the signal processing techniques used in the following chapters.

Chapter 4 describes two new approaches for controlling prosthetic hands; these involve the understanding of biomedical signals constraints that are due to the level of arm amputation and the type of hand postures required by the user. Hence, the first methodology considers a very high level of amputation on the upper arm onto which only a single electrode can be placed to capture a biomedical signal to alter the motion of a prosthetic hand; while, the second methodology describes a new system for detecting real time fingers motion for prosthetic hands with only two electrodes.

Chapter 5 includes a new analysis and methodology for the detection and monitoring of heart beat irregularities within the ECG. This applies to ventricular premature beats, ventricular tachycardia, atrial fibrillation and atrioventricular blocks. Such methodology allows an extremely compact and simple configuration when compared to the latest digital equivalent circuits and can therefore be applied to non-invasive portable heart beat monitoring devices.

Chapter 6 explores different topologies of non-linear oscillators which will be modified to perform signal processing operations for frequency and amplitude extraction of external signals. Furthermore, the very first VLSI implementation for non-linear oscillators with dynamic plasticity - an essential ingredient for signal processing - has been designed and tested.

Chapter 7 takes into consideration the signal processing performance of the work presented in chapter 6 and creates an improved model of non-linear oscillator which is designed to improve frequency and amplitude extraction of external inputs. Such oscillator is also developed in the analogue domain and tested with a large range of different types of mixed signals (including biomedical signals).

Chapter 8 presents a summary of the thesis along with future and worthy research areas to improve proposed techniques in the area of analogue signal processing for biomedical signals.

Chapter 2

Background

This chapter presents an overview of state of the art electronics differentiating between digital and analogue signal processing. Furthermore, different biomedical devices are taken into consideration and explored to see the differences and disadvantages between a digital and analogue electronics design approach.

2.1 Digital Signal Processing

A signal that can be processed can be considered as a variable that carries or contains some kind of information which can also be conveyed, manipulated and displayed [11,12]. Signals that are of interest can vary in a large range of applications such as:

- sounds and music - which are used in everyday media players.
- speech - including telephony and radio.
- communication signals - transferring/receiving data
- biomedical signals - electroencephalograms (EEG - brain waves), electrocardiograms (ECG - heart beat waves) and electromyograms (EMG - the electroactivity present on the muscular tissue).

The majority of signals in nature are actually obtainable in an analogue form, meaning that they often vary in time. The signals used in most digital signal processors (DSP) come from an analogue signal which has been sampled at regular intervals and then transformed into a digital form for further processing.
DSP is therefore used in many areas for applications and analysis where analogue electronics design has been difficult to use or implement [11].
Additionally, the following advantages lay on DSPs [11, 13]:

- Guaranteed accuracy - accuracy is chosen according to the number of bits that are used.
- Perfect reproducibility - easy identical performance, sets of data can be easily transferred without distortion or alteration.
- Bit values or signal processing is not altered by external parameters as temperature or age.
- With the scaling down of transistor sizes the increase of operations and number of processing components can be added within the chip.
- Flexibility - DSP processors can be repetitively programmed to perform different operations according to the applications.
- Performance - highly complex algorithms can be implemented by using DSP techniques.

While the disadvantages that rely on DSP techniques are the following:

- Speed and cost - depending on the speed and large bandwidths required.
- Design time - DSP techniques can be very time consuming and hard to implement.
- Finite word length - in real-time situations, depending on the economic budget, algorithm implementations use a limited number of bits which may drastically reduce the system performance.

2.2 Analogue Signal Processing

Since the early 1980s electronics engineers predicted the demise of analogue circuits [14]. The performance achieved by digital electronics was becoming more powerful with the advances of technology and integrated-circuits (IC). DSPs were therefore becoming more compact and efficient replacing analogue components. Consequently, many functions, that were previously performed in the analogue domain, were then performed in the digital domain, also suggesting that with the advance of technology the whole signal processing would be performed digitally [14].
Considering that naturally occurring signals are received in the analogue domain, DSPs still require additional hardware to manipulate and transform the analogue raw signals into digital bits [15]. Therefore, the importance and complexity given by the operations required to convert raw analogue signals into digital signals still could not be avoided.
Nowadays, more than 80% of the microelectronics industry is dedicated to digital circuits including microprocessors, static and dynamic memories, and DSPs [15]. The remaining

20% of the analogue industry focuses mainly on different types of analogue-to-digital converters (ADCs) as flash ADCs, two-steps ADCs and pipeline ADCs [16]; operational amplifiers (op-amps) as instrumentation op-amps, programmable gain op-amps, isolation op-amps, audio op-amps, buffer op-amps, video op-amps, communication op-amps and bio-sensing op-amps [17–20].
Additionally to ADCs interfaces, and specific op-amps, there is also a variety of applications, researched and implemented in both academia and industry, where the signal processing is kept in the analogue domain; this includes analogue signal processors (ASPs). Modern analogue signal processors (ASPs) have the ability of being programmable and therefore allow the implementation of different mathematical functions. Such flexibility is given by their internal arrangement which is based on an array structure, as in field programmable gate arrays (FPGAs) in digital systems [21] and are capable of complex computation as modern FPGAs [22], Consequently, ASPs are also referred to as field programmable analog arrays (FPAAs) or reconfigurable analogue signal processors (RASPs) [22].
As shown in Fig. 2.1, the array in a FPAA is designed by computational analog blocks (CABs), where each CAB contains a mixture of analogue components as transistors, capacitors, operational transconductance amplifiers (OTAs) with programmable bias currents, programmable band pass elements, and analogue multipliers (depending on the application and type of FPAA) for a higher level processing [22].
The advantages of FPAAs, (which will be discussed in more details in Section 2.3), are given by a dramatic reduction of power consumption and a larger bandwidth of operation allowing the performance of operation at very high frequency where ordinary DSPs cannot operate due to insufficient speed and accuracy of modern ADCs.

A different variety of analogue designs involve more specific applications showing the ability and advantages that are obtained in the analogue domain. An example of such specific areas involve analogue systems for position sensing which can achieve great resolution and linearity of the sensor allowing reliability, small size, wide temperature range and insensitivity to moisture and dust [23].
While, other specific applications of analogue computation are related to realization of mathematical functions such as log-domain and hyperbolic sine ($sinh$) for high performance integrated circuits [24, 25].

2.3 Comparison of Analogue Vs Digital Design

Analogue and digital electronics have drastically changed and improved human life. During the last 3 decades digital signal processing has overtaken analogue signal processing for most of our current day activities showing the level of obtainable resolution and processing power [15]. This was due to the reduction of design complexity that digital

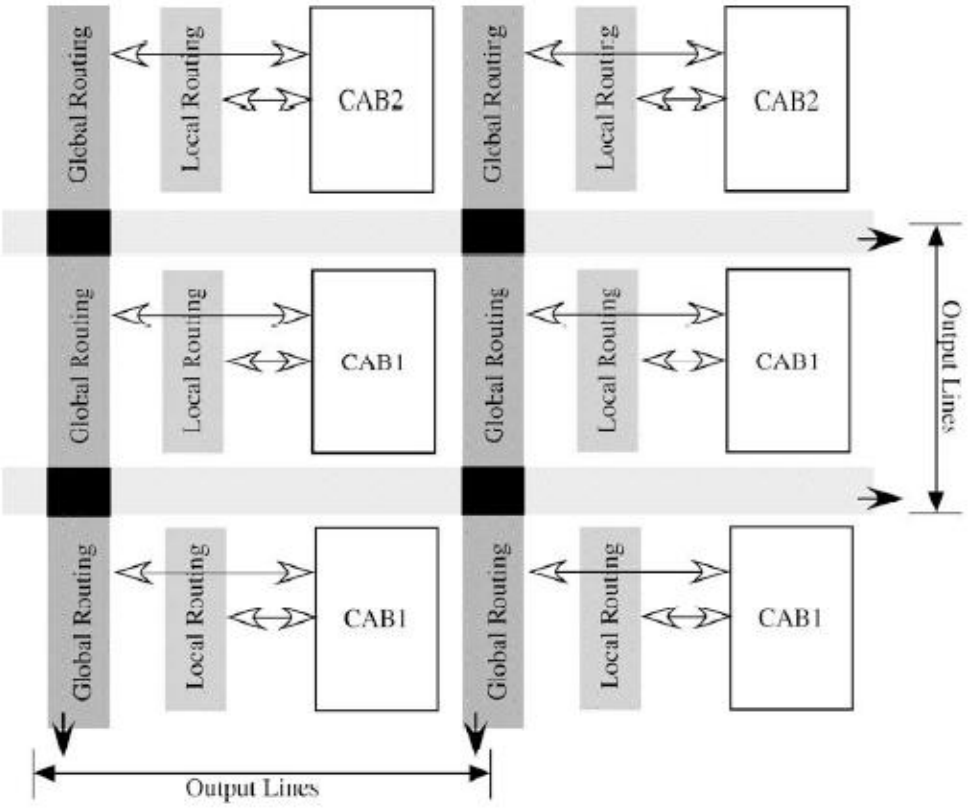

FIGURE 2.1: Block diagram of a field programmable array (FPAA) [22].

electronics could offer against analogue electronics [11,13]. Moreover, new digital design techniques are provided with hardware description languages (HDL), computer aided design (CAD), and embedded software devices for the implementation of complex systems. Consequently, these tools decrease the number of design steps as described in the block diagram of Fig. 2.2 where it is also possible to see a comparison between analogue and digital system design. Furthermore, analogue electronics design requires a larger number of design reiterations and layout simulations to compensate for manufacturing imperfections. Such simulation techniques can be associated to four corner simulations (which have also been used in the works presented in the following chapters). Additionally, with the introduction of new programmable devices as field programmable analogue arrays (FPAAs) and reconfigurable analogue signal processors (RASPs) it is possible to anticipate the arrival of HDL CAD tools for analogue circuit design which will decrease the design complexity.

The power available in small portable devices is very limited, thus low power implementations of signal processing algorithms is necessary, considering that batteries have doubled their capacity only every $5 - 20$ years [26]. Indeed, it has been shown that wireless applications for EEG monitoring in the digital domain require compression or data reduction due to the small power budget of approximately a few hundred microwatts [27]. [28] investigated the most appropriate hardware/software co-design implementations of a lossey EEG compression algorithm which manages to compress the data

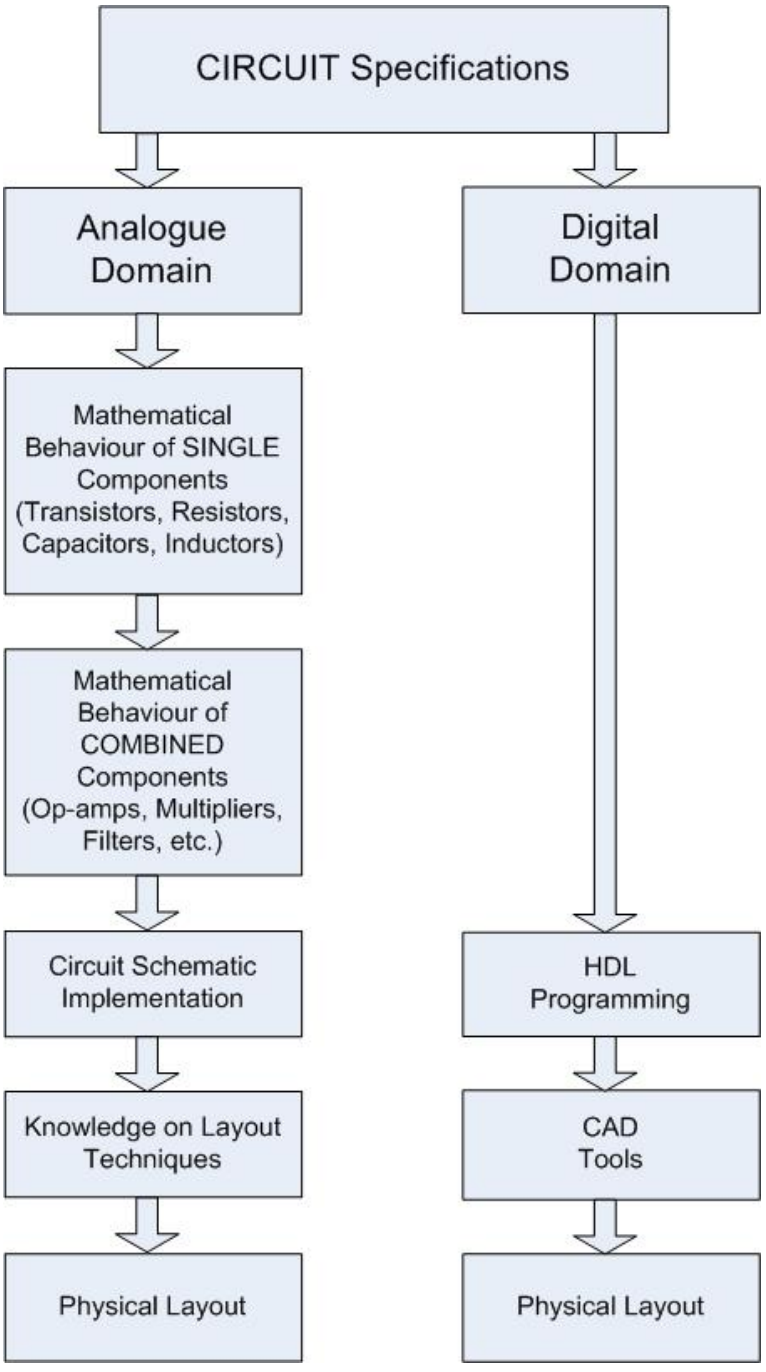

FIGURE 2.2: Comparison of analogue Vs digital electronics design.

by 98%. However, the lowest power consumption for these data compression algorithms require at least 72 mW demonstrating that the implementation of low power data compression algorithms is not a trivial task [29].

Interestingly, [29] designed a very simple algorithm for online data reduction in wireless EEG for epilepsy diagnosis presented by [30], and investigates the best implementation for this simple algorithm considering that the power budget is $96\mu W$. The two implementations investigated by [29] are firstly in the software domain using off-the-shelf processor solutions; and secondly, a full custom design in the analogue domain. It is

found that an implementation in the hardware digital domain is also feasible, whilst, only 24% of the available power supply budget would be necessary in the implementation of the algorithm in the analogue domain.
The algorithm under investigation is shown in Fig. 2.3. The aim of this simple algorithm is to reduce the power consumption of the system by recording only interictal (inter-seizure) epileptic events avoiding background signals [29].

It was calculated in [29] that a digital microprocessor would require approximately

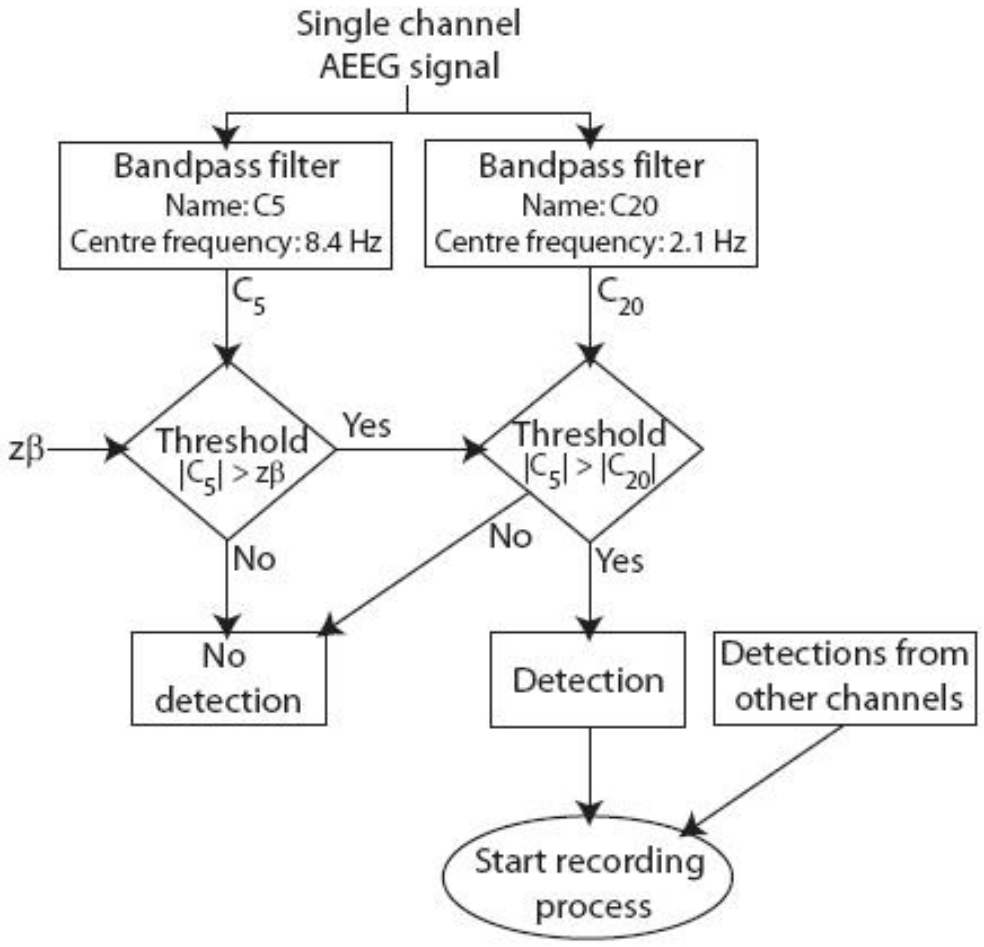

FIGURE 2.3: High level overview of the algorithm investigated by [29].

422400 instructions per second in order to perform the algorithm shown in Fig. 2.3. Modern Intel processors, which are obviously designed for computers rather than portable devices, consume 10nJ of energy per instruction [31] leading to an overall power consumption of 4.2 mW (which is well above the available power budget of $96\mu W$). A more suitable microprocessor for portable devices is the ARM7 processor which consumes 3.3 mW/MIPS (Millions of Instructions per second) on a $0.35\mu m$, 3.2 V process [32]. A more advanced ARM processor is the ARM cortex-M3 processor which stated to be 70% more efficient [33] but still require more than the power budget available of $96\mu W$. A final comparison is given by the TI MSP430 microprocessor which is designed for biomedical applications [34], Table 2.1 shows its typical power consumption per operation. It is

TABLE 2.1: Active Mode Power Consumption for a TI MSP430 Microprocessor With 2.2 V Supply [34]

Clock speed / kHz	**Current Supply /μA**	**Power Consumption / μW**
1000	270	594
100	60	132
4	5	11

possible to notice that operations at lower power can be achieved by reducing the clock speed, although this strategy would require the clock to run below 100 kHz and therefore not allowing an enough number of clock cycles to perform the 422400 operations per second required for this basic algorithm [29].

A better improvement in power consumption can be achieved with custom DSPs and application-specific integrated circuits (ASICs) which give an approximate power consumption of 0.5 μW/MIPS and 1 μW/MIPS respectively [35]; concluding, a specific DSP or ASIC design is needed for the implementation of ultra low power signal processors.

The power consumption of an analogue implementation is given by the power consumed by typical components. Generally, analogue components can have an approximate dynamic range of 45 dB (between 7 and 8 bits). Such range is considered to be lower than standard recommendations for EEG resolution [36]. However, "a typical diagnosis made by a human from a digital EEG is performed with 16 channels on a screen with 1024 vertical pixels giving just 6 bits of resolution" [37]. Hence, this dynamic range is sufficient for the algorithm operations, and it is also confirmed by recent results proved by [29]. Furthermore, [38] and [39] have shown in Fig. 2.4 the fundamental limits in power consumption for signal processing in the analogue and digital domain; concluding, the total power consumption for the algorithm of Fig. 2.3 in the analogue domain is estimated to be 23 μW, which is 24% of the available power budget.

[40] described a new approach to satellite tracking applications in the analogue domain with a comparison to digital implementations. This algorithm implemented in the analogue domain eliminates a large amount of components which can not be avoided in the digital domain, allowing a significant reduction of power consumption, system cost and system integration complexity.

The control algorithm in a typical beamforming algorithm for satellite tracking applications is designed in the digital domain and require a large number of components and processing power to operate at very high frequencies as 10-12 GHz. While, for instance, the control algorithm in the analogue domain in [40] saves approximately 34 digital-to-analogue converters (DACs) and associated multiplexing hardware. Additionally, in typical digital algorithms, the components which communicate with the DACs affect the speed of the algorithm and require the use of expensive high-speed digital components and DSPs [40].

[41] implemented a 65 nm CMOS circuit design of a sampled analogue signal processor

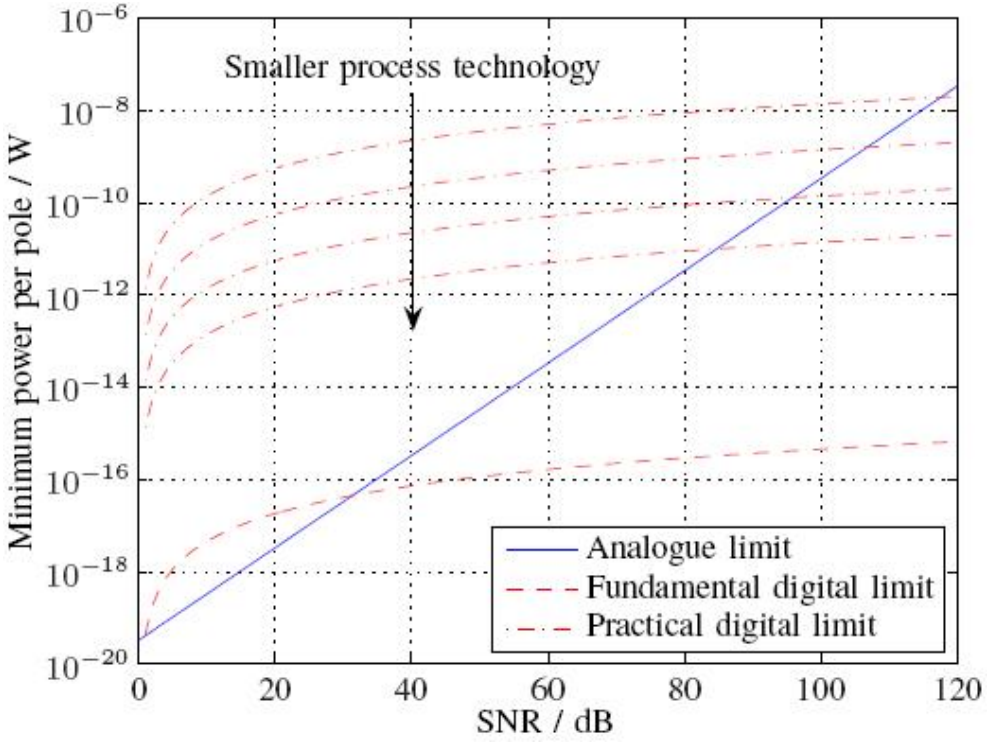

FIGURE 2.4: The fundamental limits on the power requirements of analogue and digital signal processing versus dynamic range. From [38] and [39].

dedicated to radio frequency (RF) applications. [41] also discuss the limitations of digital design, showing that digital software-defined radios (SDRs) systems imply analogue to digital A/D conversions close to the antenna, which are not feasible in the case of a mobile terminal [42, 43]. Therefore, the analogue signal processor designed by [41] process RF signals in order to select and convert into digital signals only the desired RF signal envelope allowing a more compact design with a lower power consumption.
[22] introduces one of the first large-scale field-programmable analogue arrays (FPAAs) as previously mentioned in section 2.2. Such FPAA is composed of 56 computational analogue blocks (CABs) containing over 50,000 programmable analogue elements where bias currents can be programmed to a minimum of 100 pA to a maximum of 3 μA. Fig. 2.5 shows a basic block diagram of the CABs inside the FPAA presented by [22].

Previous FPAA implementations [44–47] did not have the same capabilities as in [22] and they could be compared to early digital programmable logic devices (PLDs); and, the analogue computer proposed by [48] is composed of 16 macroblocks (similar to the CABs in FPAAs) and is also capable of performing complex tasks similar to FPAAs. Moreover, the new FPAA implemented by [22] has the same computational and signal processing power obtainable in modern FPGAs with the advantages of preserving the power efficiency benefits of analogue systems while providing reconfigurability and programmability (as in FPGAs). Additionally, a wide range of signal processing functions could be implemented in [22] and compared to equivalent DSPs to observe the overall

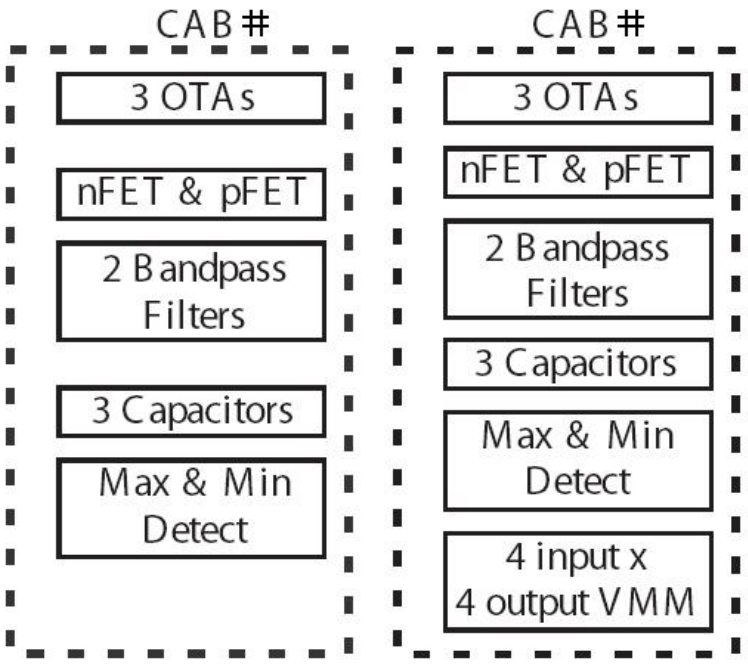

FIGURE 2.5: Block diagram of the inside components within a CAB.

power consumption. Furthermore, as discussed in [49–51] analogue design allows a potential power savings factor of up to 1000 over digital equivalents.

Also, other applications as signal processing for small portable loud-speakers, has recently found the advantages of analogue signal processing over digital approaches. [21] demonstrated how a typical algorithm from psychoacoustic, which is traditionally implemented on DSPs for commercial products [52], is implemented in the analogue domain to extend the bandwidth of auditory signals and allow a better quality of sound for low frequencies as the bass in small portable devices [53]. The resulting algorithm was implemented on a floating-gate based field programmable analogue array FPAA [54] and allowed a far less power consumption than ordinary all-digital designs.

The importance of smaller and lower power devices is one of the key parameters for medical devices. [55] described the basic concepts as continuous interleaved sampling (CIS) combined with novel current-mode, and micropower analog techniques for the implementation of very low power medical circuits for cochlear implants. Similarly, [56] designed simple analogue electronic spiking neuron circuits in order to create hardware models of biological neural systems, emulating the neuron behaviour of ventral cochlear nucleus. The purpose of [56] was to overcome the problems which arise with complex digital device operations which are becoming more intensive and memory demanding.

The work proposed by [57] on biomorphic circuits and systems for the control of robotic and prosthetic limbs puts under comparison two different implementations (analogue and digital) for central pattern generators (CPGs). Both designs are very similar, and consist of neuron circuits and programmable synapses; the only advantage of the digital version is given by the rapid prototyping of multi-neuron networks at the price of a relatively low number of neurons; while, the advantages on the analogue counterpart lies

on shorter synapses allowing a larger number of neuron and synapses. Table 2.2 summarizes the features and advantages of both the analogue and digital implementations.

TABLE 2.2: Comparison between analogue and digital silicon CPG implementations [57]

	Analogue Version	**Digital Version**
Neurons	24	10
Synapses	888, analogue	220, digital
Area (mm^2)	3×3	3.3×2.2
Power (mW)	<1	8.3
External Inputs	12	4 analogue + 4 digital
Spike Frequency Adaptation	On-Chip	External + Analogue Inputs
Value post-SHDN	Retained	Not retained
Synaptic Weight Storage	Analogue	Digital

2.4 Technology in Biomedical Signals

With the improve of technology and bio-compatible materials, electronics has found new applications in the field of health care and biomedical signals analysis allowing better studies, and implantable devices to improve the quality of life and health care [58].
The capturing of biomedical signals such as electroencephalogram (EEG), electrocardiogram (ECG) and electromyogram (EMG) signals is performed in the analogue domain; while, most of the signal processing is kept in the digital domain allowing most of the advantages and motivations discussed in section 2.1.

2.4.1 Electronic Systems for ECG Signals

The main issues in DSP technologies is given by the complexity of the algorithms that DSPs have to perform, the chip area which involve a dramatic amount of space for ADCs, and power consumption which does not allow the devices to last for sustained operations.
In order to improve these issues, a number of implementations can be performed in the analogue domain. [59] proposed a wireless ECG detection system with low power (453 nW) analogue front-end (LPAF) circuit and bio-processing Zigbee firmware where the LPAF is designed in 0.18μ TSMC CMOS technology; the combination of the LPAF with the BioZigbee firmware aimed to reduce the power consumption, and improve the signal acquisition, processing and communication. Fig. 2.6 shows a block diagram of the circuit structure proposed in [59].
[60] presented a portable three-channel compact and low power analogue processor fabricated in TSMC 0.35μ mixed-mode CMOS technology for the monitoring of ECG.

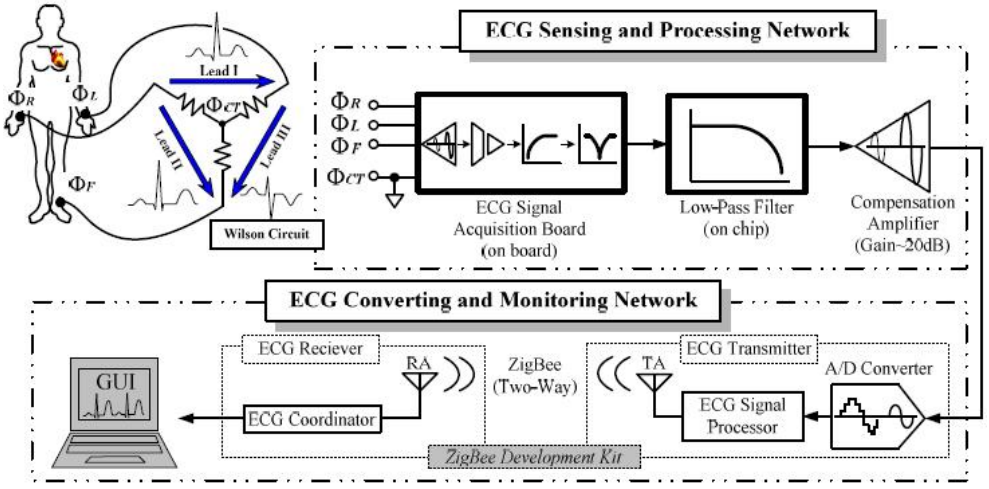

FIGURE 2.6: Wireless ECG detection system for portable ECG detection devices [59].

The analogue processor contains first order low-pass filters as well as programmable high-pass filters; and it shows how instrumentation amplifiers based on current balancing technique allow the implementation of more analogue signal conditioning functions at instrumentation amplifiers. Each of the channels draws 22μA from a 3.3V battery satisfying the requirements for portable ECG monitoring devices. The main aim highlighted by [60] is given by the importance of the analogue signal processing components extracting, amplifying and filtering signals in very noisy environments.

[61] focused on an optimised design of the front-end analogue high-pass filter for a diagnostic quality ECG monitoring system. In their methodology [61, 62] discuss the importance of designing more improved high-pass filters for a more faithful capturing and monitoring of the ECG signal, considering that the filters incorporated in a capturing system can distort the properties of the ECG signal [63–65].

The models and methodologies presented in [59–61, 66] are mainly dedicated to the capturing of ECG signals showing and proving the quality of different analogue signal processing techniques, while DSPs are still used for other processing functions as the detection of heart beat, heart beat rate and heart beat anomalies.

Back in the 1990s, the wavelet transform (WT) was finally considered for its more accurate abilities in signal analysis of biomedical signals, this was due to its ability of localizing signals information in a time-frequency plane, making WT very suitable for non-stationary signals as biomedical signals [67]. Early implementation of WT in electronics showed the advantages of the transform in a digital manner or purely mathematically [67–70]; while the first analogue implementations of WT for biomedical signals, and in particular for the detection of ECG signals, was presented by [71], demonstrating on simulation the abilities of scaling and shifting in time and frequency by simply controlling the capacitance and the control current values. Furthermore, [71] presented an improved and lower power implementation of analogue WT for ECGs in [7], where the first derivative Gaussian Wavelet function is implemented by means of dynamic translinear (DTL) circuits consuming 55nW.

Following the results and advantages produced in [71] and [7], other analogue implementations were introduced by [72–77] for general signal processing with WTs; while, [78] described a novel method based on balanced log-domain (WT) circuit for the detection of ECG complexes for implantable pacemaker applications.

2.4.2 Electronic Systems for Cochlear Implants

Cochlear Implants (CIs) are prosthetic devices which are used to restore hearing functions in deep deaf patients by bypassing the damaged parts of the inner ear and stimulating the remaining functioning auditory nerve fibers in the cochlea by means of electrical impulses [79].
CIs can be classified as low power wide-dynamic-range systems, which makes them extremely hard to design and implement [80] considering the size, adjustments and power consumption requirements that have to be respected [55]. Additionally, depending on the age and exterior preference, CIs users request the size to be as small as possible [55].
The dynamic range of a CI is determined by the ratio of the intensities of the largest and smallest inputs to the system which is typically measured in logarithmic units of decibel (dB) [80]. The biological human cochlea can cope with a dynamic range of 120dB and several octaves of bandwidth [81, 82] Moreover, the largest input that a system can support is limited by nonlinearities that can produce distortion or failure of the output; whilst, the smallest input that a CI can process is limited by the system's input-referred noise floor [80].
Traditionally, CI processors divide the frequency band of the speech into sub-bands and extract the envelope of each sub-band in order to stimulate the nerve fibers [79, 83]. Additionally, in order to implement a spectral analysis in an analogue speech processor, 2^{nd} order band-pass filters in the form of log-domain [55, 84] and $G_m - C$ filters [85] in CMOS technology have successfully shown the improvements in terms of power consumption but still not allowing the same performance at high frequency which is achieved by the biological cochlea [83] [86].

2.4.3 Electronic Systems for Electromyography (EMG) Signals

An electromyography (EMG) signal is represented by the electrical activity required to activate biological muscles and can be easily captured by applying electrodes on the skin surface [87] as shown in Fig. 2.7.
The main aim of EMG signals is to control the motion of prosthetic limbs [88–91] and therefore emulate real biological hands.
The capturing of EMG signals is achieved in the analogue domain (considering the raw nature of the signal), while the filtering and identification of the EMG features (such as frequency and amplitude) are achieved with ordinary DSPs [92, 93].

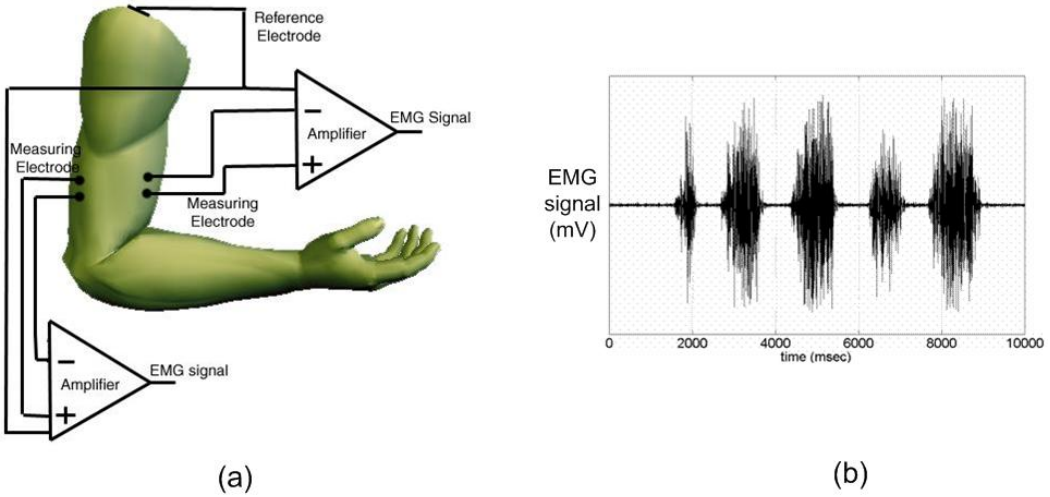

FIGURE 2.7: (a) Basic detection system for surface electromyography (EMG) signals; (b) electrical response of a captured EMG.

Other modern approaches, have shown the ability of neural networks (NNs) in identifying different hand postures [94,95]. Such systems can adapt to different patients and can be trained (as neural networks) to identify a number of postures, although NNs have certain limitations which are given by the large number of required electrodes and therefore available muscular tissue [88].Unfortunately, the amount of muscular tissue depends on the level of amputation which constantly varies from patient to patient.

2.4.4 Electronic Systems for Electroencephalography (EEG) Signals

The Electroencephalography (EEG) signal represents the recorded electrical activity along the scalp generated by firing neurons within the brain [96] with additional signal processing techniques (e.g., filetering, amplification) as shown in Fig. 2.8.
Studies on EEG are mainly academical and they are still at an early stage; this is confirmed by the difficulties which involve the capturing of EEG signals within the different regions of the brain [97]. More accurate and internal analysis of EEG activity can be achieved with deep brain stimulation (DBS) techniques which show the capability of capturing and interacting with inner parts of the brain. This is achieved by implanting internal brain pacemaker in the brain in order to interfere with the electrical activity of a particular part of the brain which causes disorders which might lead to certain deceases as epilepsies.

Diversely, most of the EEG devices concentrate specifically on the capturing, filtering and amplification of the surface EEG signals other than on differentiating different EEG waves as in DBS techniques. Therefore, most of the EEG devices involve only monitoring and wireless communication systems for portable EEG devices [98–100], considering that due to first implementations on EEG portable devices and early understanding of EEG signals, most of the EEG devices are mainly DSP [18], FPGA [101] or computer

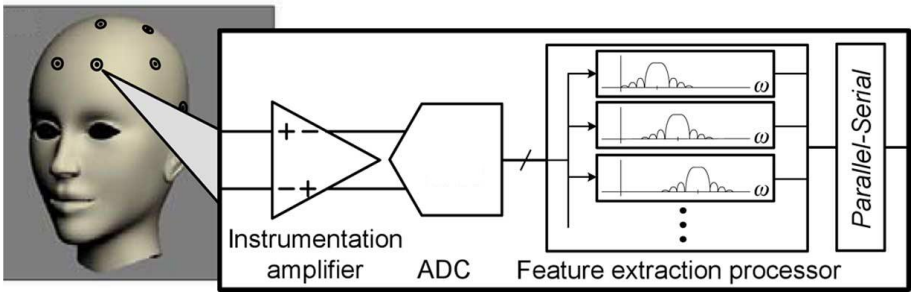

FIGURE 2.8: Basic detection system for electroencephalography (EEG) signals [18].

software based.
Furthermore, different techniques for capturing EEG signals involve a variety of materials as dry electrodes for better performances [102].

2.5 Conclusion

Nowadays, electronics has an extremely important role, which facilitates all our needs, from smart traffic light controls to communications and biomedical devices. The level of intelligence improves annually with the customers demand of smarter gadgets able to perform multi-tasks, at higher speed and resolution [21]. Digital electronics, has shown its advantages in resolution, storage and tools for fast implementations for the last 3 decades. Nowadays demand requires smarter, faster, more compact and longer lasting-life devices for a large number of applications which have been mentioned in section 2.2 and 2.4.
Consequently, due to the advance of technology and improved manufacturing techniques, analogue electronics has proved greater performances in terms of speed, area and power consumption. The design of analogue systems still requires a large background knowledge as internal circuit parameters (such as capacitors, resistors and transistor sizes) have to be calculated by the designer; while digital electronics designers are provided with design tools as HDL coding, synthesizers and layout softwares for a ready to manufacture product. Therefore, with the arrival of new designing tools for analogue design as FPAAs and specific analogue integrated circuits (ICs), analogue systems will occupy a much larger percentage in our everyday's products.

Chapter 3

Design of an Analogue ALU

Most of digital systems require a dedicated core to perform mathematical operations. Such cores usually contain an adder that can be programmed to perform summation and subtraction; furthermore, depending on the complexity of operations that need to be performed a multiplier and a divider can be added into the ALU core. Consequently, an analogue arithmetic unit, which was called "analogue ALU" (as in analogue arithmetic logic unit), was designed as a general core to perform mathematical operations in the presented works in the following chapters.
An analogue ALU has never been designed or implemented before; this was due to the mathematical complexity required to design such a unit in contrast to a digital ALU design.
The advantages of implementing an ALU in the analogue domain are given by the dramatic reduction of hardware (e.g. A/D converters and number of transistors depending on the bit resolution), sotware/hardware memory accesses and processing time (considering that an analogue ALU would not be dependent on controlling signals such as clocks in digital systems). After evaluating the types of operations required in the work presented in the following chapters, the analogue ALU was only required to perform such mathematical operations as addition, subtraction and multiplication.
The implementation of an analogue adder or subtractor could be easily achieved with ordinary operational amplifiers (op-amps) although, the amplification achieved by op-amps does not follow the arithmetical multiplication rules given by the positive and negative signs of the operands. For these reasons the designed analogue ALU was made of four different components: a multiplier core, an addition and a subtraction component, and a current subtracting circuit. These components have been meshed together to concurrently perform mathematical operations, as shown in Fig. 3.1 and Eq. 3.1, and to provide a more compact circuit.

$$out = A \times B + C - D \tag{3.1}$$

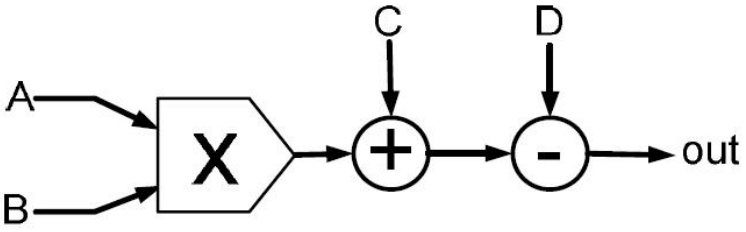

FIGURE 3.1: Analogue ALU block diagram.

The implementation of addition and subtraction in the analogue domain can be respectively achieved by applying Kirchhoff's law (as the summation of currents on a single node) and with the use of an ordinary current subtraction circuit. On the other hand, a circuit which would follow the multiplication rules (as for the multiplication of two signed integers) requires a more complex implementation; therefore, extra care was taken to choose the most appropriate analogue multiplier configuration.

3.1 Related Works

Analogue multipliers are very important components and vital building blocks in many analogue processing applications such as frequency mixers, modulators filtering, frequency translation, waveform generation etc [103].
Different techniques has been adopted to design analogue multipliers exploring different device technologies as Bipolar, CMOS [104] and Bi-CMOS [105]. According to the type of application, analogue multipliers can be classified into three categories, depending on which channel region the transistors are operating: weak-inverted, triode-biased and saturation region. The weak-inverted MOSFET inversion region is typically preferred for low frequency signals [106]; while, the triode-biased MOSFETs give better response for intermediate frequencies [107]; and multipliers with MOSFETs operating in their saturation region, are mostly used for higher frequencies (megahertz range). Additionally, three different topologies are possible for analogue multipliers [108] as: variable transconductance, square-law characteristics of MOSFET design and linear region current-voltage characteristics. The first approach is very frequently used in bipolar and CMOS devices where the variable transconductance in the Gilberts translinear circuit [104] is utilized. The second technique involves the square-law characteristics of MOSFET transistors which are biased in the saturation region [109]; while the last method uses the current voltage characteristics of transistors in the linear region [110]. From an application perspective, it is very important to provide compact multipliers which can work at low power, high input range and high bandwidth. However, with the scaling down of transistor sizes and due to the reduction of supply voltage the devices

become more prone to nonlinear effects [111]. To compensate these effects the reduction of input voltage/current variation range is necessary [16] [112].

3.2 The Implementation of the Multiplier Core

The implementation of the multiplier core has been improved several times to provide better performance in terms of input voltage range, output linearity and area. Such improvements have been summarized in the following subsections and have been used in the circuits designed in the following chapters.

3.2.1 The Gilbert Cell as Multiplier Core

The first implementation for the multiplier core was chosen to be the Gilbert cell [113] which is a simple and effective configuration which allows a four quadrant multiplication. Fig. 3.2 shows the transistor schematic of the Gilbert cell which consists of three source coupled pairs and a current tail [114]; whilst, Table 3.1 shows the transistor dimensions for a possible implementation on a 130 nm CMOS Technology.

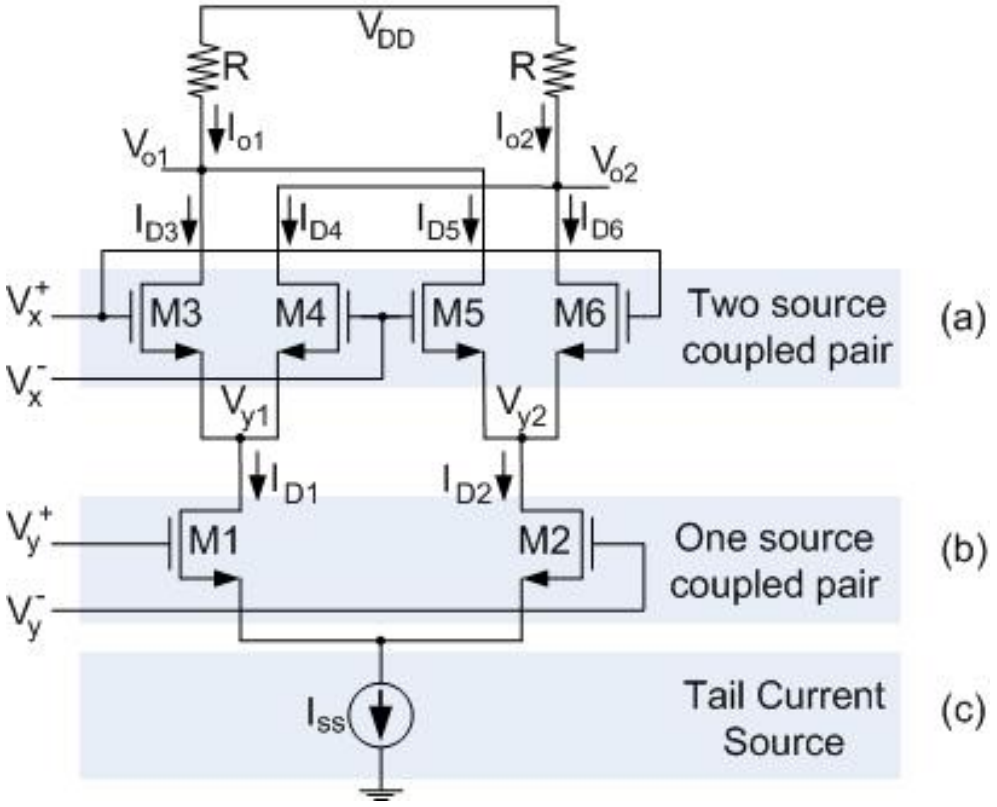

FIGURE 3.2: Schematic of the Gilbert cell; (a) two source-coupled pairs; (b) one source-coupled pair; (c) current tail.

TABLE 3.1: Transistor dimensions for the Gilbert multiplier of Fig. 3.2; 130nm CMOS technology with 0.2V threshold voltage

Transistor	**W/L**	**W(μm)**
M1-M2	3.8	0.5
M3-M6	30	4

Eq. 3.2 describes the response of the MOS differential pair.

$$I_{D1} - I_{D2} \simeq \beta\Delta\sqrt{(\frac{2I_{SS}}{\beta} - \Delta^2)} \tag{3.2}$$

where $\beta = \mu_n C_{ox}(W/L)$, $\Delta = V_y{}^+ - V_y{}^-$ (where $V_y{}^+$ and $V_y{}^-$ are respectively the input voltage and its inverted version).

The differential pair of Fig. 3.2 (b-c) with the four cross coupled transistors of Fig. 3.2 (a) are responsible for the multiplication algorithm and Eq. 3.3-3.6 describe the current behaviour of the square law components [115]:

$$I_{D3} = \frac{\beta}{2}(V_x^+ - V_{y1} - V_{TH,n})^2 \tag{3.3}$$

$$I_{D4} = \frac{\beta}{2}(V_x^- - V_{y1} - V_{TH,n})^2 \tag{3.4}$$

$$I_{D5} = \frac{\beta}{2}(V_x^- - V_{y2} - V_{TH,n})^2 \tag{3.5}$$

$$I_{D6} = \frac{\beta}{2}(V_x^+ - V_{y2} - V_{TH,n})^2 \tag{3.6}$$

where $V_{TH,n}$ is the threshold voltage of NMOS transistors, and V_x^+ and V_x^- represent the input voltage and its inverted version.
Therefore, the output voltage of the multiplier can be expressed in Eq. 3.7 [114]:

$$\begin{aligned} V_{o1} - V_{o2} &= ((I_{D6} + I_{D4}) - (I_{D3} + I_{D5}))R \\ &= \beta R(V_x^+ - V_x^-)(V_y^+ - V_y^-) \end{aligned} \tag{3.7}$$

Fig. 3.3 shows an example of analogue multiplication achieved by the multiplier of Fig. 3.2 when multiplying two different sinusoidal waveforms with amplitude $100mV$ and frequency 1 kHz and 30 kHz respectively.

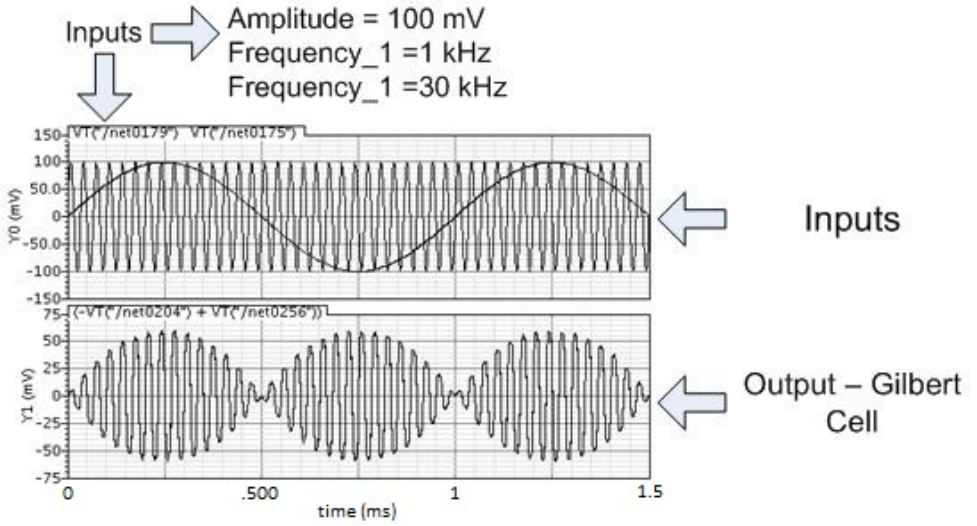

FIGURE 3.3: Simulation result of the multiplier of Fig. 3.2.

3.2.2 An Improved Gilbert Cell

The multiplier structure described in section 3.2.1 allows the multiplication of two analogue signals, although the output voltage linearity of this multiplier structure is limited by the amplitude voltage range of the two inputs. Consequently an improved version of the Gilbert cell of Fig. 3.2 is designed to increase the output voltage linearity for a larger input voltage range (see Fig. 3.4).
The source-coupled differential pair shown in Fig. 3.2 exhibits a non-linear voltage to current relationship which is due to the square law behaviour of the MOS transistors in saturation.
Therefore, the elimination of the tail current source linearizes the transconductor over a larger range of input voltages as illustrated in the graphs of Fig. 3.5 (a) and (b) where Eq. 3.2 and 3.8 regulate the current flowing through transistors M1 and M2 for the models in Fig. 3.5 (a) and (b) respectively.

Table 3.2 shows the transistor dimensions of the multiplier of Fig. 3.4. These parameters show different values if compared to the transistor sizes of Table 3.1 as the current tail has been removed and the transistors still need to be re-sized to remain in their saturation regions.

TABLE 3.2: Transistor dimensions for the Gilbert multiplier of Fig. 3.4; 130nm CMOS technology with 0.2V threshold voltage

Transistor	**W/L**	**W(μm)**
M1-M2	1.15	0.15
M3-M6	3	0.4

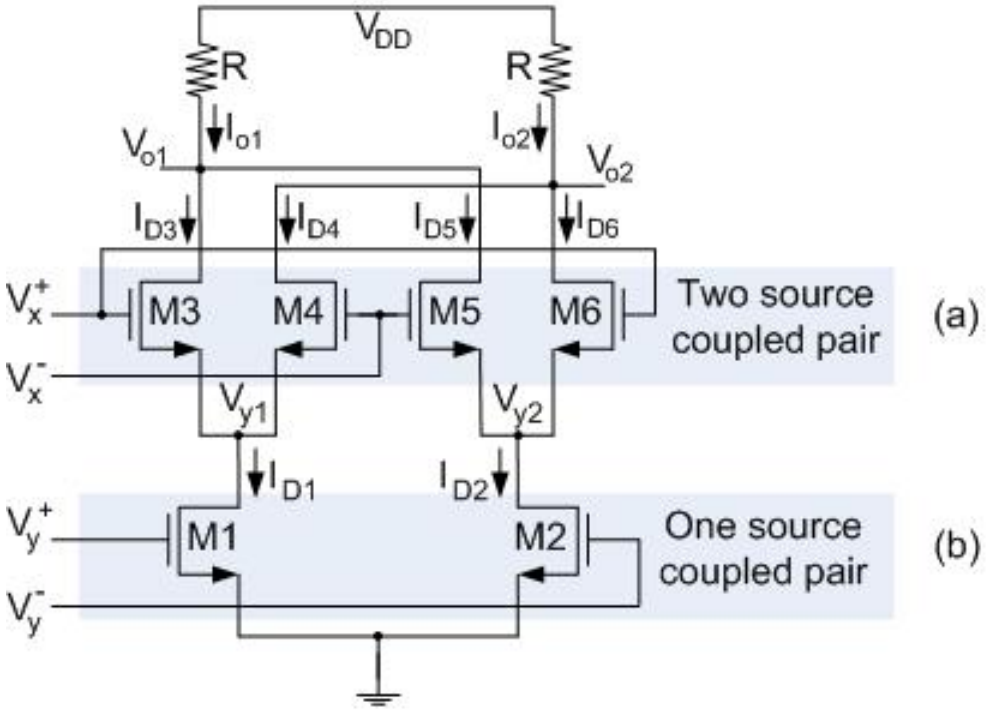

FIGURE 3.4: Schematic of the new Gilbert cell without the current tail.

$$I_{D1} - I_{D2} = 2\beta\Delta(-V_{SS} - V_{TH,n}) \tag{3.8}$$

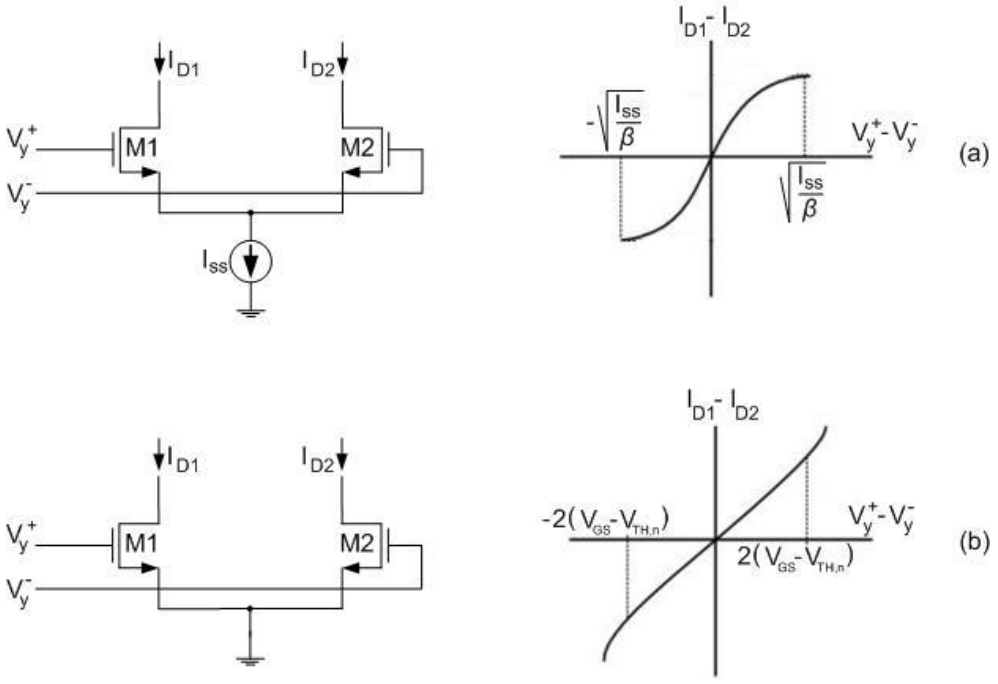

FIGURE 3.5: CMOS transconductors; (a) non-linear; (b) linear.

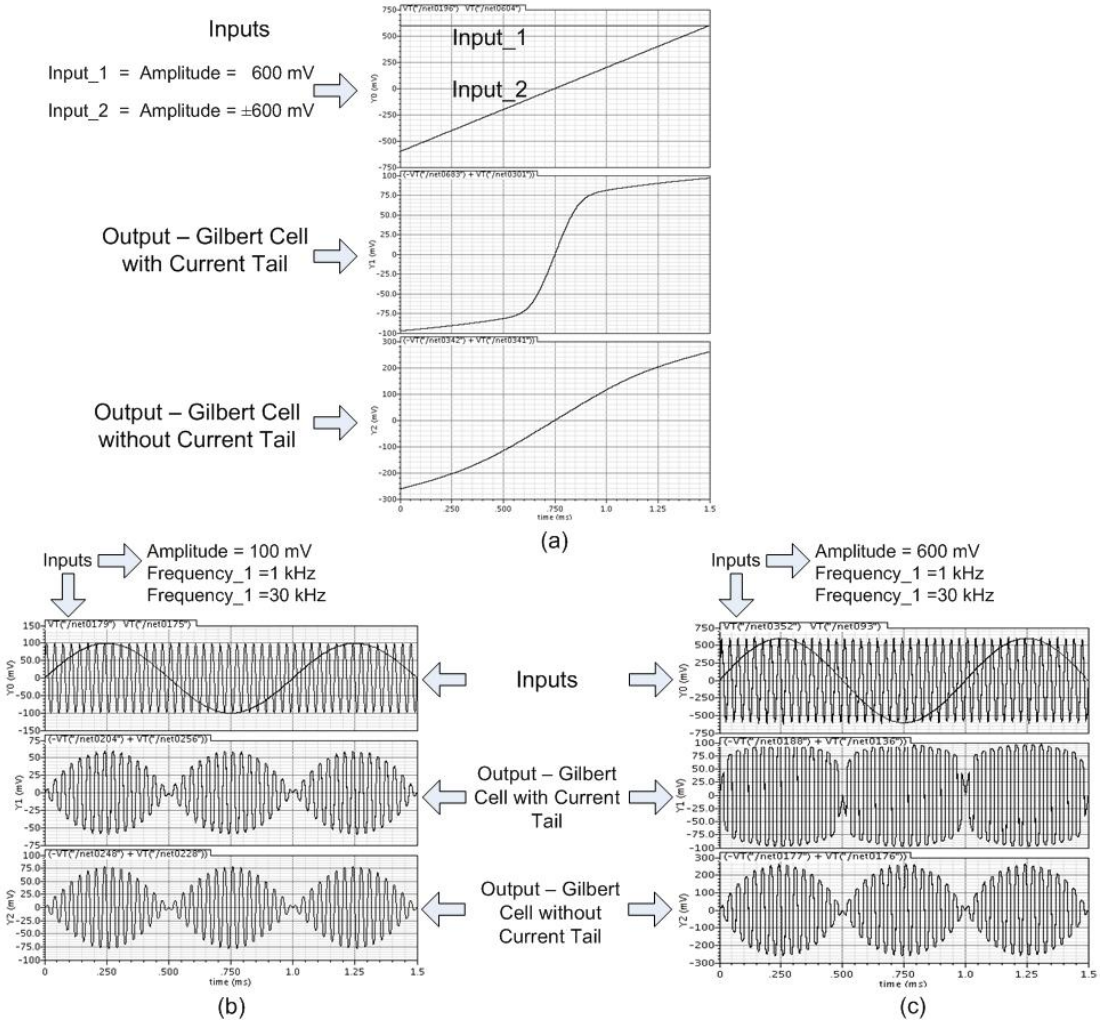

FIGURE 3.6: Output responses of two Gilbert cells with current tail and without current tail; (a) output voltage response; (b-c) multiplication of two sinusoids. Notice in (c) The Gilbert cell with current tail saturates fairly quickly.

Furthermore, the output responses of the Gilbert cells designed in section 3.2.1 and 3.2.2 are shown in the results obtained in Fig. 3.6. These were obtained from a simulation on Cadence Spectre where Fig. 3.6 (a) shows the output linearity of both the multipliers when "$input_1$" is kept constant and "$input_2$" is increased from $-V_{SS}$ to V_{DD} ; while the results shown in Fig. 3.6 (b-c) illustrate the output result when multiplying two sinusoids with $\pm V_{DD}$ voltage range.

From the results obtained in Fig. 3.6 (a) it is possible to observe how the output of the Gilbert cell of Fig. 3.2 saturates for small input voltages, while the output of the Gilbert cell shown in Fig. 3.4 allows a much larger input range $\pm V_{DD}$. Furthermore, Fig. 3.6 (b-c) shows another example of output voltage comparison between the two Gilbert cell configurations when two sinusoids are applied to the multipliers.

3.3 Implementation of the Addition and Subtraction Components

In order to implement a more compact design able to concurrently perform different arithmetical operations, such as multiplication, addition and subtraction, the internal components of the analogue ALU required to be meshed together. Therefore, considering Eq. 3.9 [114] for the output voltage of the multiplier core, it is possible to inject the addition and subtraction components into the multiplier core by adding the currents I_{D7} and I_{D8} as shown in Eq. 3.10:

$$V_{o1} - V_{o2} = ((I_{D6} + I_{D4}) - (I_{D3} + I_{D5}))R \tag{3.9}$$

$$V_{o1} - V_{o2} = ((I_{D6} + I_{D4} + I_{D8}) - (I_{D3} + I_{D5} + I_{D7}))R \tag{3.10}$$

while, Fig. 3.7 illustrates how the currents I_{D7} and I_{D8} can be implemented into the multiplier core of Fig. 3.4.

As the output voltage of the analogue ALU is given by the difference of nodes V_{o1}

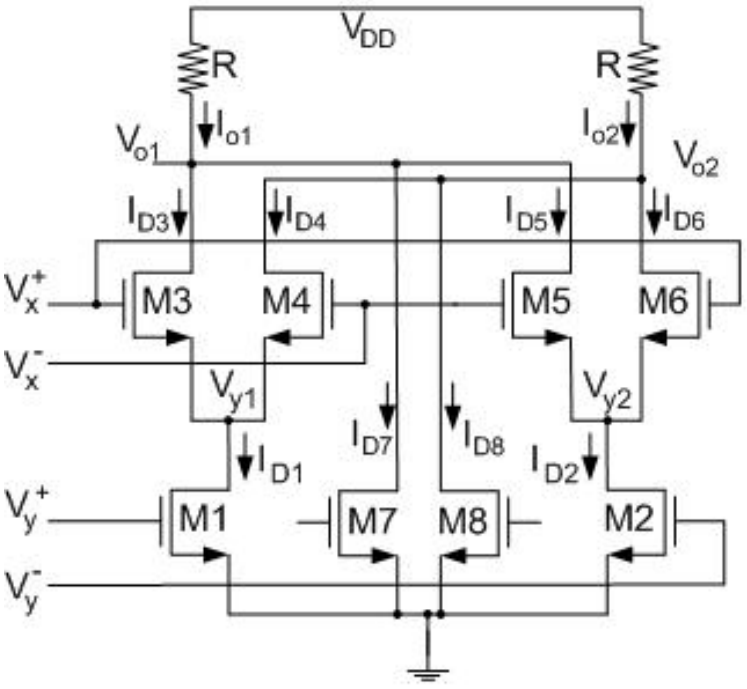

FIGURE 3.7: Schematic of the new multiplier with addition and subtraction components.

and V_{o2}, it is possible to use a current subtracting circuit which outputs a single output given by the difference in currents at nodes V_{o1} and V_{o2} as illustrated in Fig. 3.8. Furthermore, Fig. 3.9 shows three different examples of mathematical functions (e.g., multiplication, multiplication with addition and multiplication with subtraction) concurrently performed by the analogue ALU while Table 3.3 gives the transistor dimensions

of the complete ALU of Fig. 3.8.

The output noise response was also simulated on Cadence Spectre by varying an AC

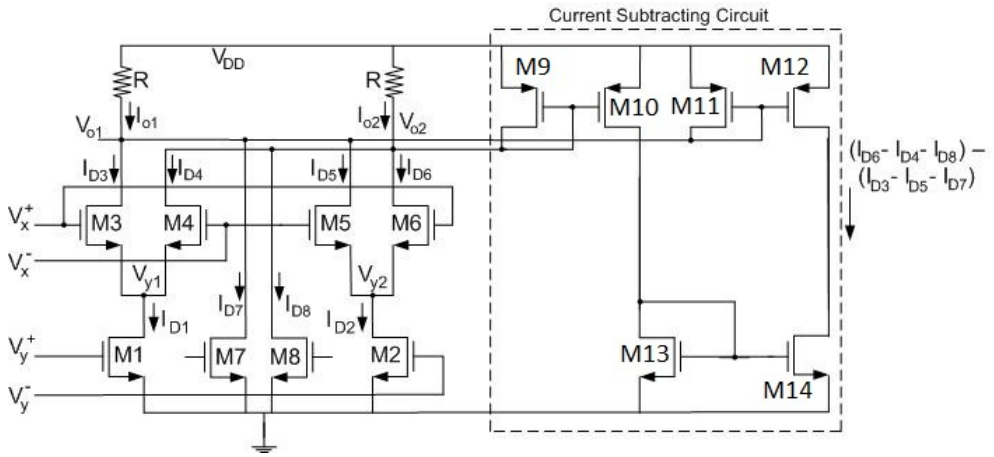

FIGURE 3.8: Schematic of the complete analogue ALU with multiplying, adding and subtracting components and current subtracting circuit.

TABLE 3.3: Transistor dimensions of the complete analogue ALU of Fig. 3.8; 130nm CMOS technology with 0.2V threshold voltage

Transistor	**W/L**	**W(μm)**
M1-M2	1.15	0.15
M3-M6	3	0.4
M7-M8	1.15	0.15
M9-M12	2.3	0.3
M13-M14	1.15	0.15

input signal from a frequency of 100Hz to 1GHz, as shown in Fig. 3.10.

3.4 Conclusion

Different configurations have been considered during the development of an analogue ALU. Such unit was the result of four different components meshed together: a multiplier core, an adding and subtracting component, and a current subtracting circuit.

The main advantage of this analogue ALU is given by the very low number of required transistors (14 transistors and 2 resistors on a 130nm CMOS Technology) and the ability to concurrently perform mathematical operations. Furthermore, different multiplier core configurations were selected to improve the output linearity and to increase the input voltage range. Simulations on Cadence Spectre have also shown the capabilities to contemporarily perform the mathematical operations in the desired manner.

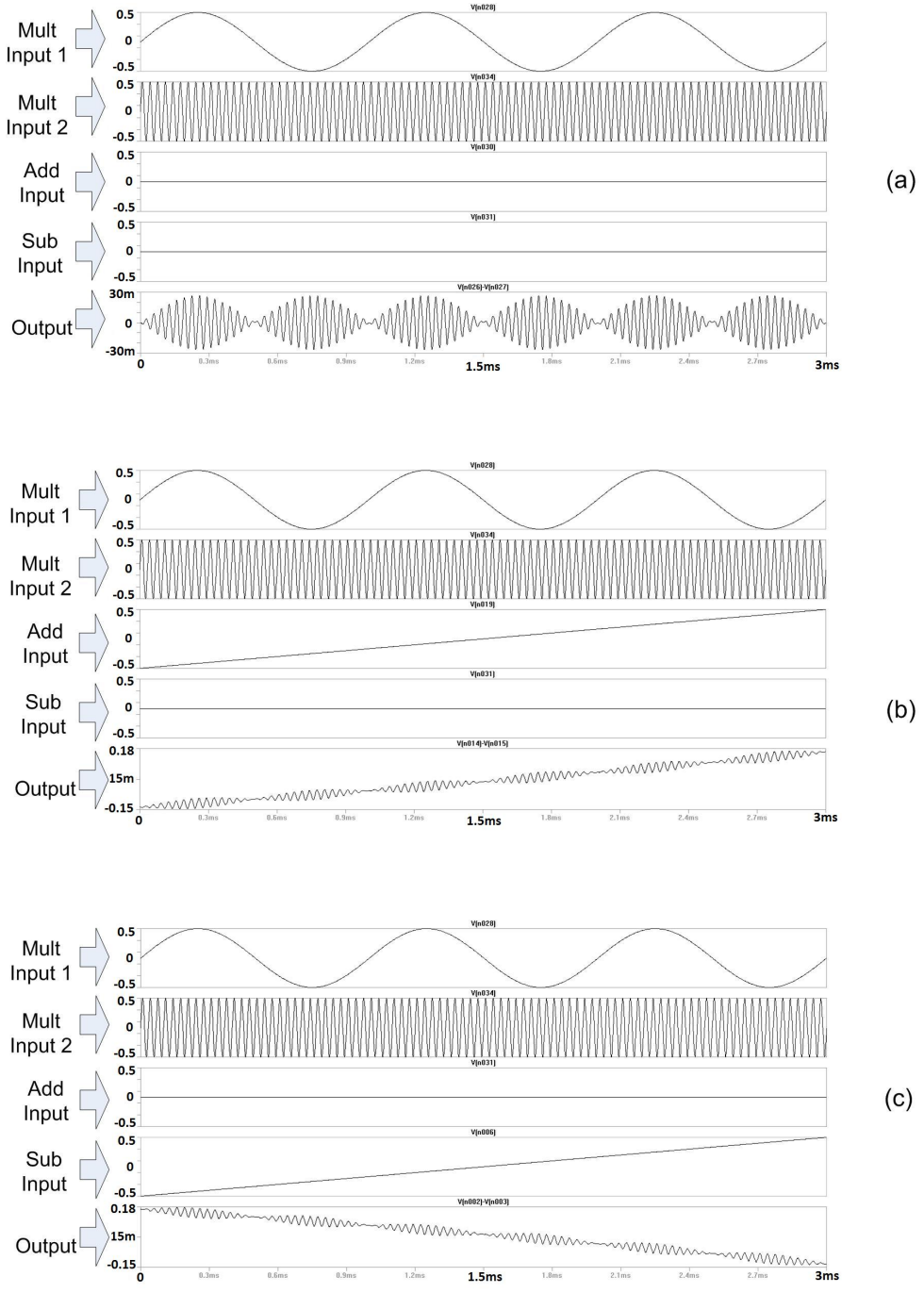

FIGURE 3.9: Simulation results of the analogue ALU while concurrently performing multiplication, addition and subtraction; (a) multiplication with no input variation of the adding and subtracting inputs; (b)multiplication with variation of the adding input; (c) multiplication with variation of the subtracting input.

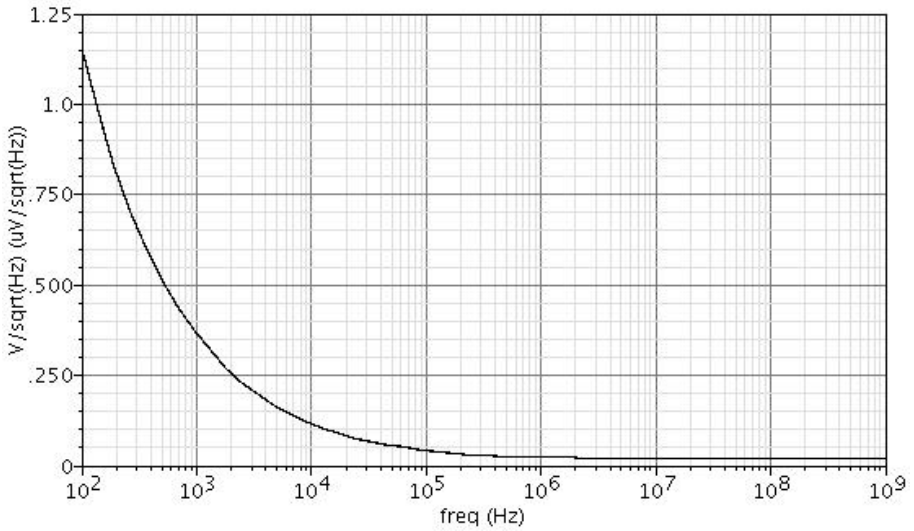

FIGURE 3.10: Output noise response of the analogue ALU.

Chapter 4

Analogue Processing Methodology for Controlling a Prosthetic Hand

One of the first medical applications that was of our interest was the control of prosthetic hands. As described in section 2.4.3, the analysis of EMG signals is performed in the digital domain with DSPs [92, 93] and with neural networks [94, 95]. The disadvantage of these two methods is given by the large amount of data required to identify the different movements for each finger of a prosthetic hand. Furthermore, these techniques have a dramatic disadvantage of being dependent on the level of amputation of the upper limb. Indeed, in case of high levels of amputations, prosthetics with DSPs and neural networks cannot be applied as they cannot acquire enough information to control the prosthetic hand. Therefore, considering these limitations, two new methodologies in the analogue domain for the control of prosthetic hands have been designed. The first method considers very high level of amputations where a single electrode can be applied to the amputated limb, limiting the capturing of a single EMG signal. While the second methodology uses only two electrodes (to capture two EMG signals) to identify individual finger movements. The results obtained by these two new methodologies were comparable to the performances obtained by the state of the art for prosthetic hands control systems.

4.1 Electromyography (EMG) Signal

The muscles are stimulated by electro-stimuli coming from the nervous system. Such electro-stimuli expand over the muscles in order to generate a muscle contraction. The electro-activity which reaches the outer part of the muscles (and therefore of the body) is defined as electromyography (EMG) signal, and this can be captured and analysed to

evaluate the type of movements and postures for the hand that each person wants to adopt [116].

4.2 Prosthetic Hands

Prosthetic hands are designed to help people who have a partial upper limb amputation. Their main aim is to mimic the activities of a biological hand, e.g. user intended finger movements to change grips and grab an object as closely as possible. One of the main difficulties for prosthetic hand designers is given by the fact that the movements adopted by an actual hand are directly controlled by neuronal signals [117] while prosthetic hands have to analyze EMG signals which are then limited by the level of amputation; thus, the larger the level of amputation the less EMG signals are available to decipher the type of hand movements.
Fig. 4.1 shows an illustration which relates the level of amputation of the upper limb to the available muscle tissue in the case of different levels of amputations.
Consequently, different studies and approaches vary according to the number of avail-

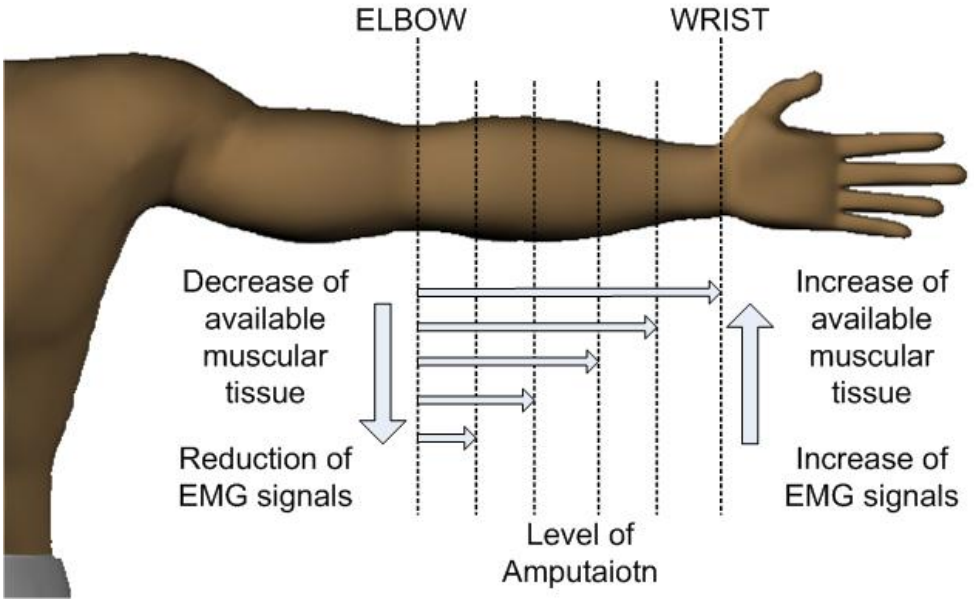

FIGURE 4.1: Upper limb and level of amputations.

able signals which are limited by the level of amputation.

4.3 The Southampton Hand

As described in section 4.2, one of the limitations and important factors for prosthetic hands is given by the level of processing the amount of raw signals captured by the electrodes on the surface of the remaining amputated upper limb. Furthermore, it is

also important to increase the performance of the prosthetic hands in terms of grabbing and holding objects of different weight and shape, without causing accidents as dropping or compressing too tightly the objects. Therefore, at the University of Southampton, a prosthetic hand was designed and manufactured with additional features such as slip and pressure sensors on the finger tips [118]. Fig. 4.2 shows the mechanical structure of the Southampton hand where the mechanics of the fingers has been designed to achieve a similar flexibility to the movements of real biological fingers. Fig. 4.3 (a) and (b) show a 3D graphic image of the mechanical structure of the fingers of the Southampton hand and the layout of the sensors which are placed in the fingertips of the prosthetic hand. More details regarding the mechanics of the Southampton hand can be found in [118].

FIGURE 4.2: External image of the Southampton prosthetic hand.

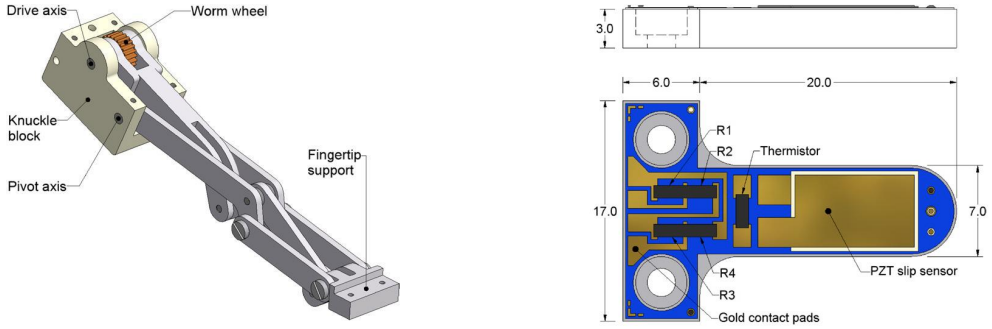

FIGURE 4.3: (a) mechanical structure of a finger of the Southampton hand; (b) fingertip sensors.

4.4 Related Works

Different approaches have been proposed to process the available EMG signals for controlling the motion of the fingers in a prosthetic hand [92, 119–125]. The difference within the available approaches in the literature are given by the way the EMG signals are processed, and the level of muscle tissue which allows the capturing of multiple EMG

signals. In general, the processing is performed in the digital domain [126] [122] [123] and with the use of neural networks [119–121, 124, 125]. The main limitations to these approaches is given by the need of large areas of muscle tissue in the upper arm causing these methodologies not to be suitable for users with high levels of amputations. Consequently the extractions of useful information which can be achieved in the digital domain requires complex filtering systems and the formulation of complex algorithms. While, the use of neural networks require a large amount of time to firstly train the neural network to identify the incoming EMG signals, and also additional time for the user who will have to train him/herself to achieve a good level of prosthetic hands movements.

4.5 A New Approach for the Analysis and Processing of EMG signals

EMG signals are a wide spectrum analogue signal and their actual shape and amplitude can vary considerably over time and from person to person [127] [128]. Thus in order to reduce the number of processes (e.g. signal digitization, memory accesses, etc.) it appears to be more pragmatic to process these signals in the analogue domain rather than in the digital domain. Additionally, recent research shows that processing naturally occurring signals in the analogue domain may result in a significant computational advantage compared to processing them in digital domain as part of the signals can be lost or distorted during A/D and D/A conversions [129] [130].
Consequently, a novel analogue circuit has been designed for an efficient control of prosthetic hands using a single EMG signal with a simple and effective methodology. Additionally the circuit has the capability of controlling the grips more efficiently by processing the feedback signals from the slip and pressure sensors on the finger tips of the prosthetic hand in combination with the input EMG signal.

4.5.1 Single EMG System Overview

A general block diagram of the proposed system is shown in Fig. 4.4. It is composed of a standard electrode, an EMG signal analyzer, a state machine, a signal processing unit and a prosthetic hand with embedded sensors for the detection of slip and pressure activity. The functionalities of each of these units are described in this section.

Using a single EMG signal for controlling different possible postures of a prosthetic hand leads to a one to many mapping problem and is extremely difficult to resolve. Even considering binary value of the EMG signal (1 = presence of EMG signal, 0 = no EMG signal) only two postures can be controlled. Therefore, in order to overcome this problem and acquire multiple postures for the prosthetic hand, each of the postures have been associated to a state, where each state is controlled by the number of EMG pulses that the user is sending when contracting the muscle. As an example, if three

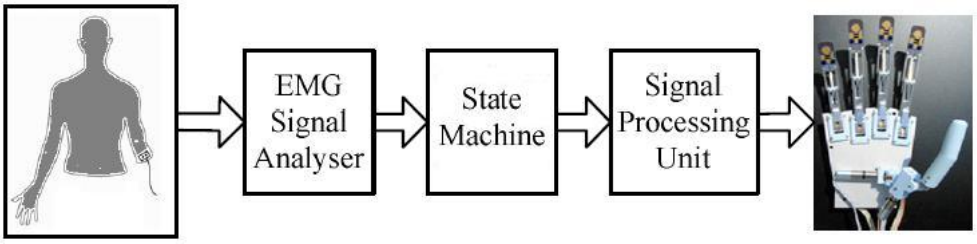

FIGURE 4.4: Block diagram of the proposed system for controlling prosthetic hands in case of high level of amputation.

postures for the prosthetic hand are available, the user has to send (stimulate) a single EMG signal to the amputated arm for the first posture, twice for the second posture and three times for the third posture. Each time the state machine receives an EMG signal it generates a time interval (T, of about 0.5 seconds) during which if a successive EMG signal is received, the state machine will pass to the following state (posture) otherwise it will adapt to the posture of the last number of incoming EMG signals. This process is described in Fig. 4.5, where three different hand postures are used as an example. The time window T was chosen to be of approximately 0.5 seconds as it would allow enough time for the user to send a successive EMG signal. Table 4.1 gives an example of each posture associated to individual states. The proposed methodology is scalable and can be adopted to incorporate more postures in the system, although here only three postures have been considered.

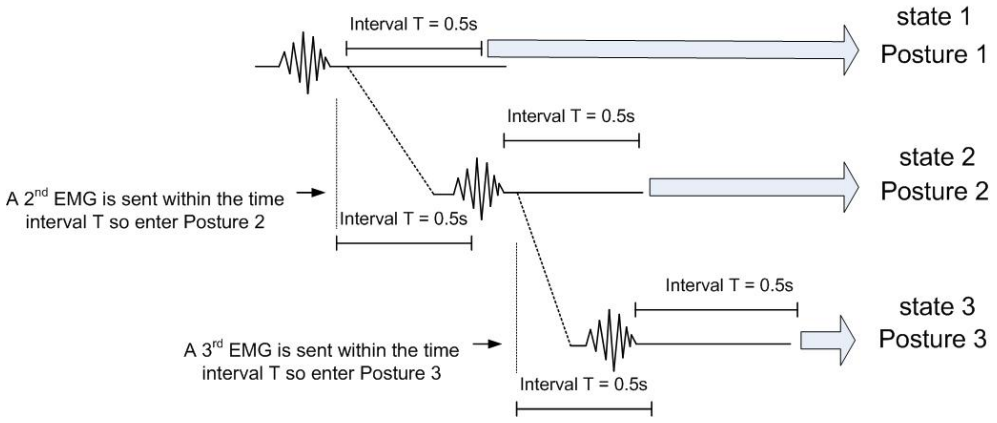

FIGURE 4.5: State diagram for controlling different hand postures using single EMG signal.

TABLE 4.1: Example hand postures and number of related EMG signals.

State	**(Posture)**	**No. of EMG Stimuli**
Posture 1	Open Hand	1
Posture 2	Lateral Grip	2
Posture 3	Spherical Grip	3

Unfortunately, the shape of the EMG signal does not lend itself as a suitable candidate for the above mentioned methodology. Thus, each EMG signal is converted to a square

wave by a thresholding technique, as shown in Fig. 4.6 where a real life EMG signal has been used. This operation is done using the EMG signal analyzer circuit. Therefore, the number of generated pulses can be considered as instructions which are read by the state machine to choose a particular posture as described earlier.

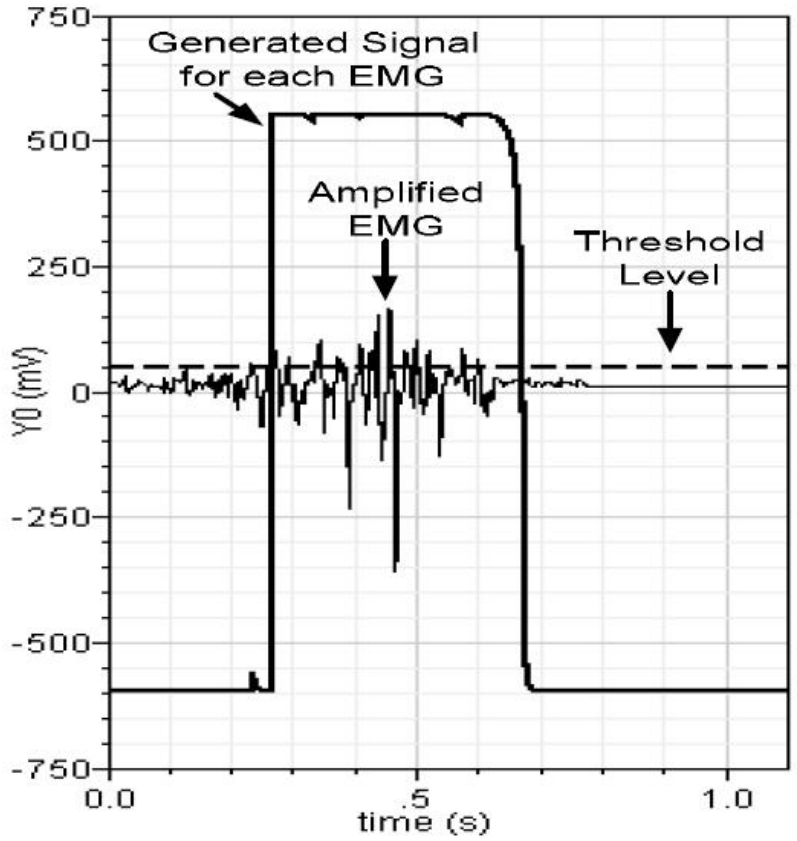

FIGURE 4.6: Amplified EMG signal and generated square wave.

Each time a posture has been selected within the state machine, corresponding signals are sent to a signal processing unit (the analogue ALU of Fig. 3.1) to control the prosthetic hand and process the feedback signals coming from the prosthetic hand (as slip and pressure sensor signals). More accurately, the signal generated by the slip sensor is summed to the signals controlling the prosthetic hand in order to increase the force of the prosthetic hand grip in case of slippery, while, the pressure signal is subtracted to avoid the breaking of eventual delicate objects.

4.5.2 Circuit Implementation

The presented work is designed on a 130nm CMOS Technology and dual ended supply with value ±0.6 V. A detailed explanation of the system sub-circuits, see Fig. 4.4, are presented in the following sub-sections.

4.5.2.1 EMG Signal Analyzer

Fig. 4.7 shows a block diagram and shape of the signal under processing at different nodes of the EMG signal analyzer. The captured EMG signal shows amplitude of 200 μV (peak to peak). The signal is amplified 1000× for ease of processing. The amplified signal has a low value (≈0 V) when a muscle is relaxed and a maximum value in the range of 150mV-200mV when contracted. Therefore, a comparator (C1 in Fig. 4.7) with a reference voltage of 50 mV is used to determine when the muscle is contracted (thresholding operation as mentioned in the previous section). The output of the comparator C1 is clamped by using a transistor configured as diode and a 50 pF capacitor. The clamped signal is compared to a reference voltage of 100mV using the comparator C2 for creating the desired square pulse which is used by the state machine. The choice of choosing a higher reference voltage (100mV) for the comparator C2 is given by the fact that small glitches can be generated by C1 each time the amplified EMG signal is near the reference voltage (50 mV) of C1.

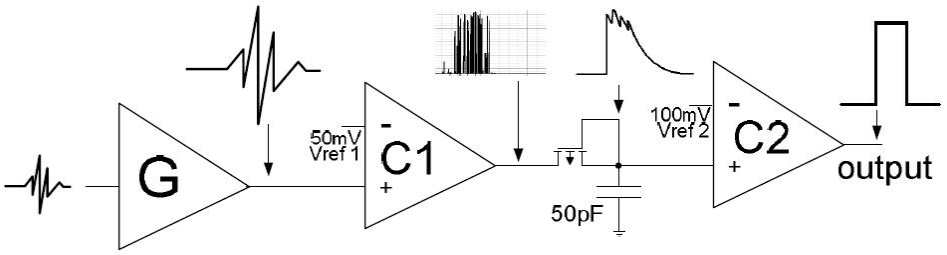

FIGURE 4.7: EMG signal analyzer block diagram.

4.5.2.2 The State Machine

Once the EMG signal is analyzed and transformed into a square pulse as shown in Fig. 4.6, each pulse is sent to the state machine shown in Fig. 4.8, to process the number of incoming pulses (EMG signals). Flip flops FF1 and FF2 are used as a 2-bit counter to keep track of the number of incoming EMG signals; while the operational amplifier OP1 with the transistor M1 (set as a diode) and the capacitor Cap1 are configured as a peak detector. This peak detector configuration can hold the output voltage for an amount of time equal to 0.5s (exactly 556ms, the time window T mentioned in subsection 4.5.1).

Comparators C3 and C4 are set to give a high signal at their output each time the clamped signal crosses the reference voltages. The rising edge of the outputs of C3 and C4 are nearly concurrent, whereas their falling edges take 556 ms and 750 ms respectively. The output of C3 is used to store the values of the 2-bit counter into FF3 and FF4; while the output of C4 resets the counter (FF1 and FF2). The control switch block shown in Fig. 4.8, is used to decode the signals stored in FF3 and FF4 to control the signals that control the motors of each finger depending on the type of posture. It is possible to notice how the inputs of the state machine are processed in the analogue domain while

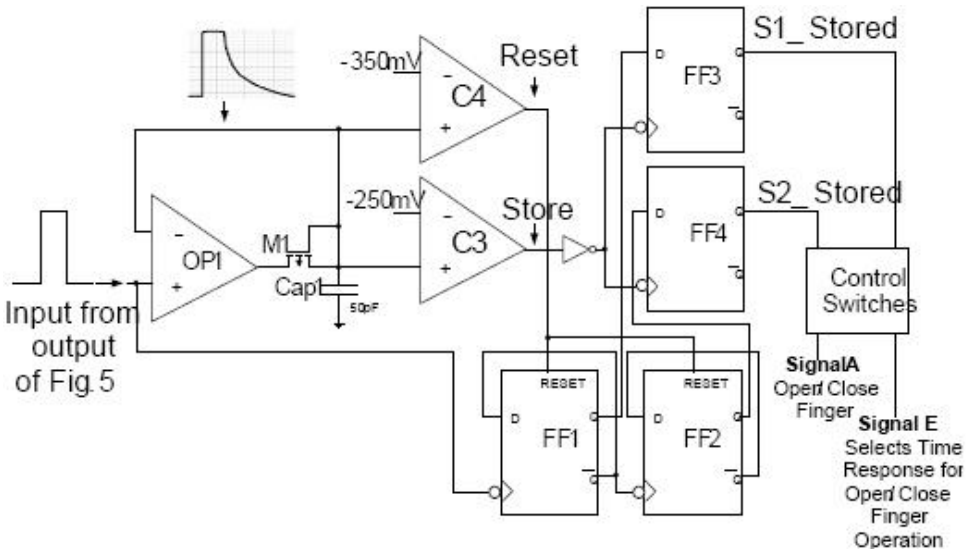

FIGURE 4.8: The block diagram of the state machine.

the counting of each incoming pulse and the storing of each state are held in the digital domain for simplicity purposes.

4.5.2.3 The Signal Processing Unit

The signal processing unit is represented by the analogue ALU described in chapter 3 with the addition of a current to voltage amplifier, as shown in the transistor schematic in Fig. 4.9, which can be used to increase the gain of the output voltage .
In order to control each of the five fingers on the prosthetic hand, five of such units are employed in the presented design. Input A in Fig. 4.9 is used to control the motor of the fingers of the hand; while the input B can be configured as a gain voltage. Inputs C and D are used for the addition and subtraction of the feedback signals respectively coming from the slip and pressure sensors embedded in the finger tips of the prosthetic hand.

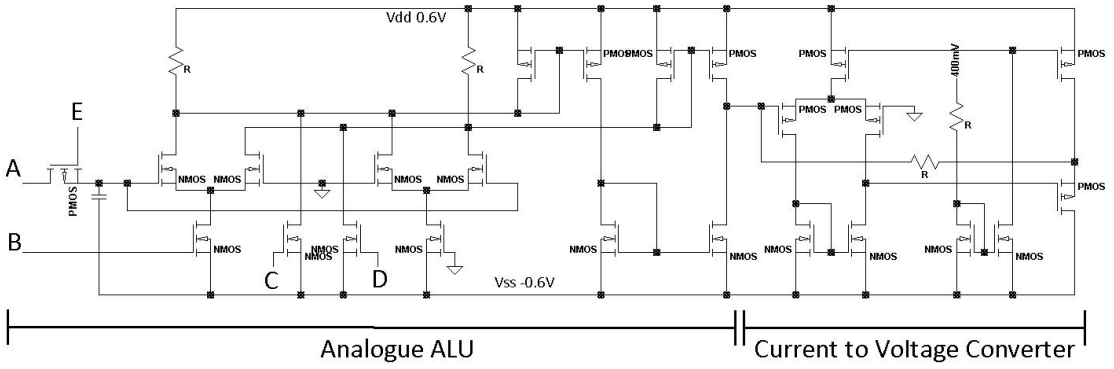

FIGURE 4.9: Transistor schematic of the signal processing unit.

4.5.3 Simulation Results

In order to demonstrate the system performance, real EMG signals have been used during experiments on Cadence Spectre. Fig. 4.10 shows the captured EMG signal, the clamped signal and the corresponding square pulse generated in the EMG signal analyzer circuit (explained in subsection 4.5.2.1 and shown in Fig. 4.7).

Fig. 4.11 shows the circuit response of the state machine when a set of EMG signals

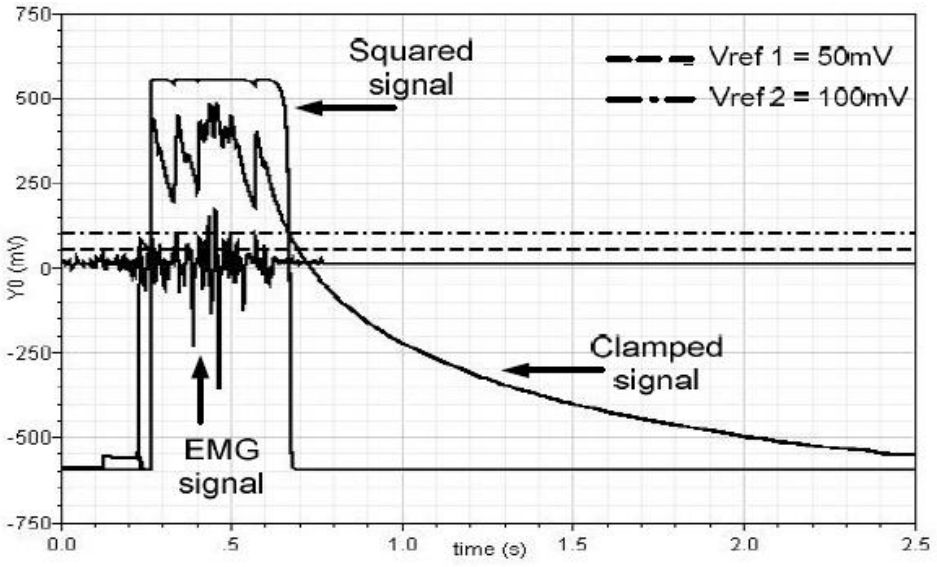

FIGURE 4.10: Simulated internal signals of the EMG signal analyzer.

is applied to the system. Fig. 4.11 (a) shows the square pulses generated by the EMG signal analyzer which are used as inputs to the state machine. Fig. 4.11 (b) illustrates how the state machine can hold the count and store the number of EMG pulses each time the interval between the successive EMG pulses exceed the predefined time interval T of 556 ms.

Furthermore, with the addition of an active RC component at the input A of Fig. 4.9 it is possible to control the velocity of reaction of each finger movement by varying the bias voltage E; such feature can be used to implement different postures where different fingers are activated at different times. An example of different finger motions is shown in Fig. 4.12.

4.6 A New Method for a Direct Differentiation of Finger Movements for Prosthetic Hands

Section 4.5 presented a novel design for an analogue control unit for the implementation of multiple postures by using a single EMG signal. As described in subsection 4.5.1 and 4.5.2.2 the system would identify each of the postures according to the number of

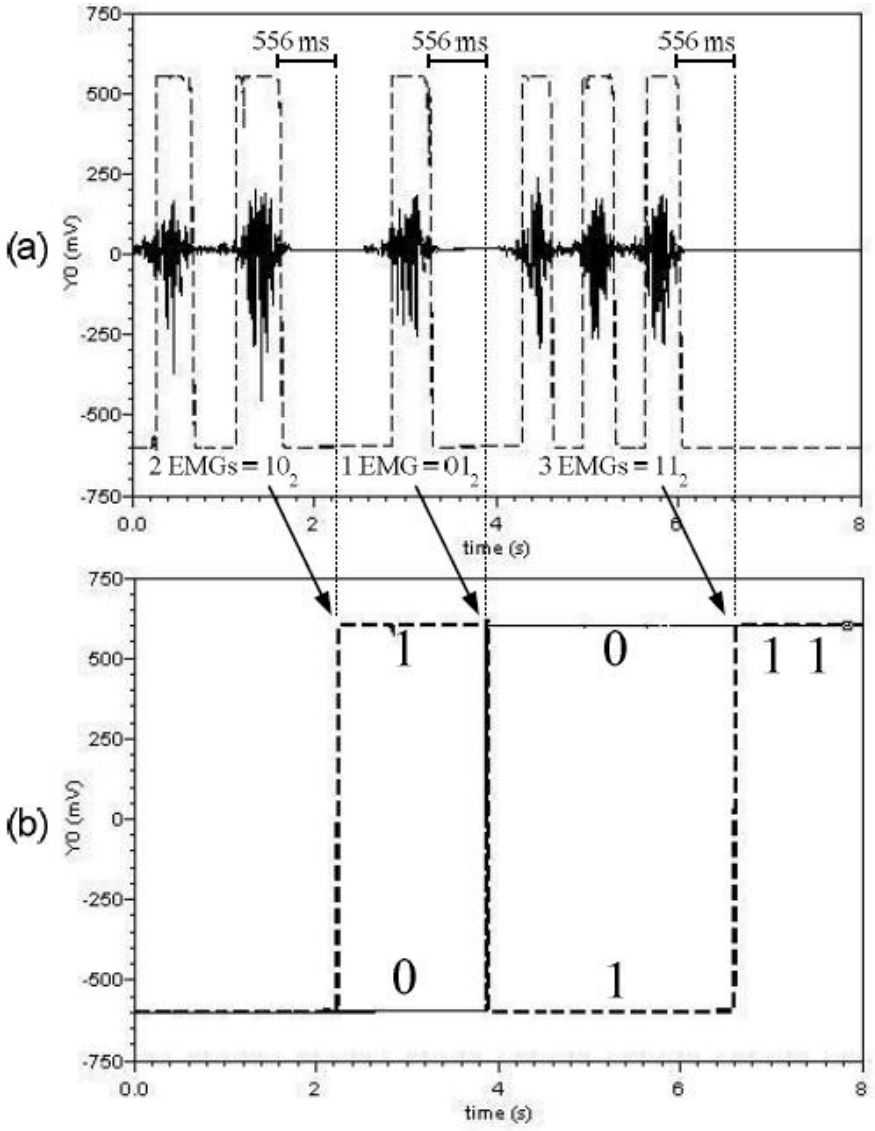

FIGURE 4.11: Simulated internal signals of the EMG signal analyzer.

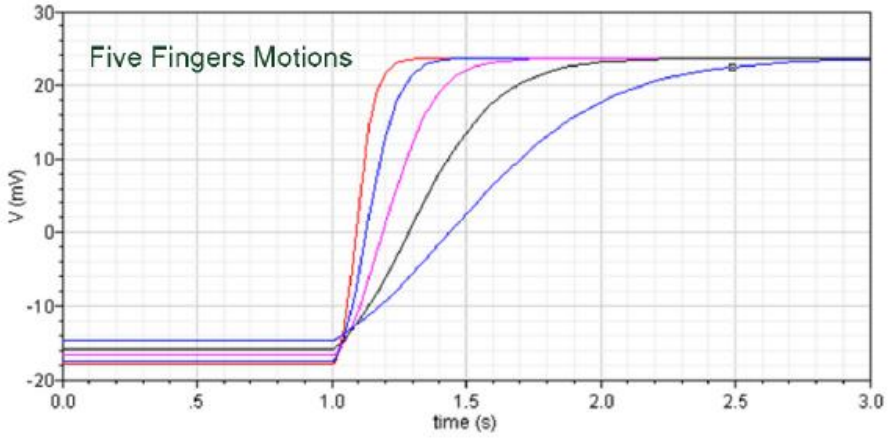

FIGURE 4.12: Simulated responses for different fingers varying the RC constant (signal "E" of Fig. 4.9).

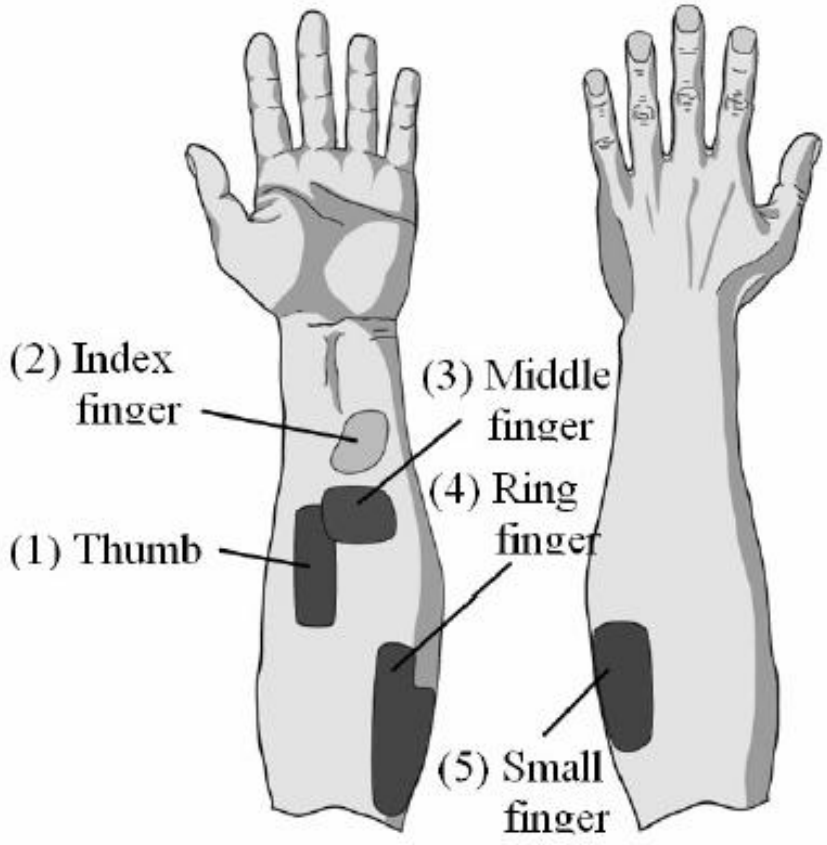

FIGURE 4.13: Specified positions related to the maximum intensity of EMG signals.

incoming EMG stimuli that the user would generate.

As described in section 4.4, [119–121, 124, 125] have shown how a neural network can be trained to identify different postures for a prosthetic hand by using a high number of electrodes (>> 6); additionally, to be considered that the main postures identified by neural networks are only represented by the motion of only the index, middle and ring finger.

Furthermore, studies conducted by [131] have identified the maximum intensity of EMG signals for each of the finger movements, pointing out where the electrodes of a prosthetic hand should be applied (other than randomly as in neural network approaches, trying to cover as much area as possible). Fig. 4.13 illustrates the region of maximum EMG activity for individual finger movements as proved by [131]. As described in section 4.4 the level of amputation determines the residual muscular tissue from which it is possible to capture EMG signals. Consequently, most of the regions shown in Fig. 4.13 can not be used for the identification of individual finger movements in case of a high or medium level of amputation.

Additional studies on the anatomy of the human muscular and nerves structure have been used to find an alternative approach for the identification of individual finger movements in case of high level of amputations. Fig. 4.14 (a) and (b) illustrate the internal

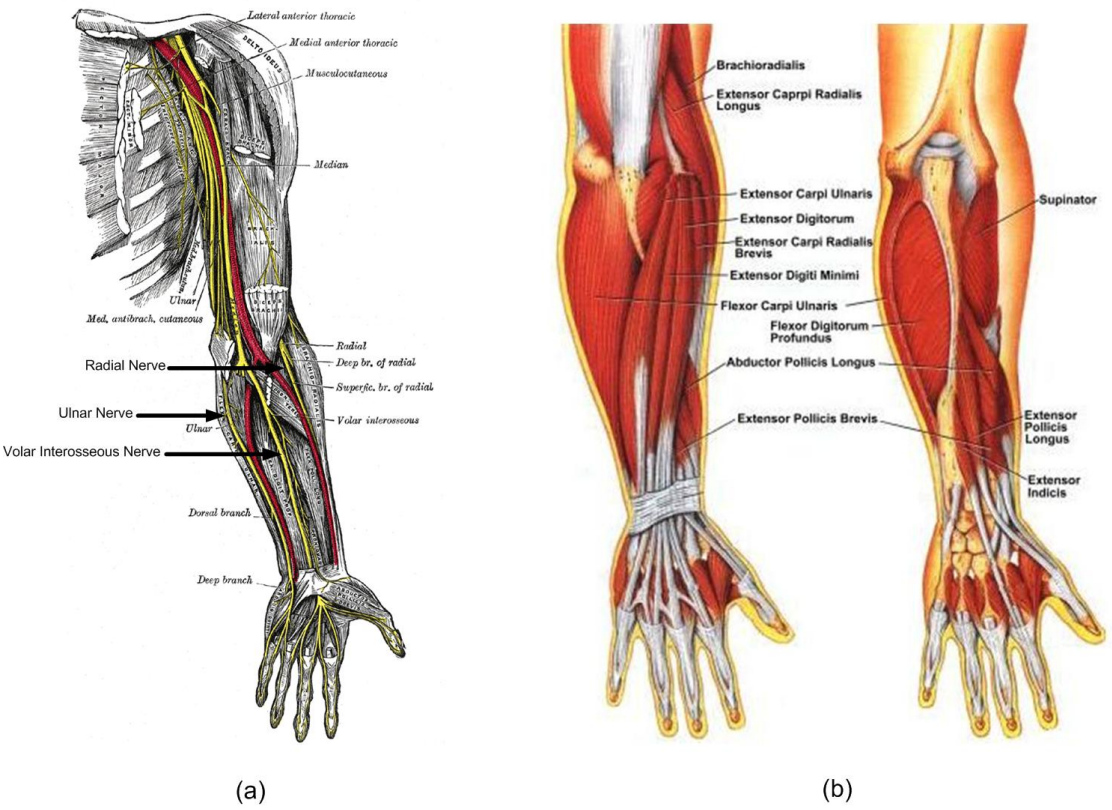

FIGURE 4.14: (a)Upper limb nerve system; (b) muscular structure [132].

human nerve system and muscular structure of the upper limb respectively. The principal nerves leading the coordination of the upper limbs are given by the radial, ulnar and volar interosseous nerves; while, the larger muscles involved in the movements of the fingers are the flexor carpi ulnaris and the flexor digitorum profundus.

Two electrodes have therefore been applied on the arm of 7 different users in the manner shown in Fig. 4.15. It is possible to observe that the electrodes are very close to the elbow, allowing the capturing of signals for high levels of amputations. The two electrodes do not present cross talk interference and this is due to the placement of electrodes which are placed on different muscles which do not interfere with each other.

Fig. 4.16 shows the EMG signal captured on both the electrodes ("Channel 1" and "Channel 2") of Fig. 4.15. During these experiments, the motion of the index followed by the middle and the ring finger has been captured showing the different amplitudes of EMG signals which allow us to create a simple control unit for the differentiation of individual fingers. It is possible to notice in Fig. 4.16 that the EMG signals generated by the motion of the middle finger are lower than the signals generated by the index and ring finger; this is due to the reason that the motion of the index and the ring finger is given by the flexor carpi ulnaris and the flexor digitorum profundus muscles respectively, while the motion of the middle finger is given by a smaller contraction of both these two muscles (as shown in Fig. 4.16).

The overall circuit is shown in Fig. 4.17. OP1 and OP2 are two op-amps used for the

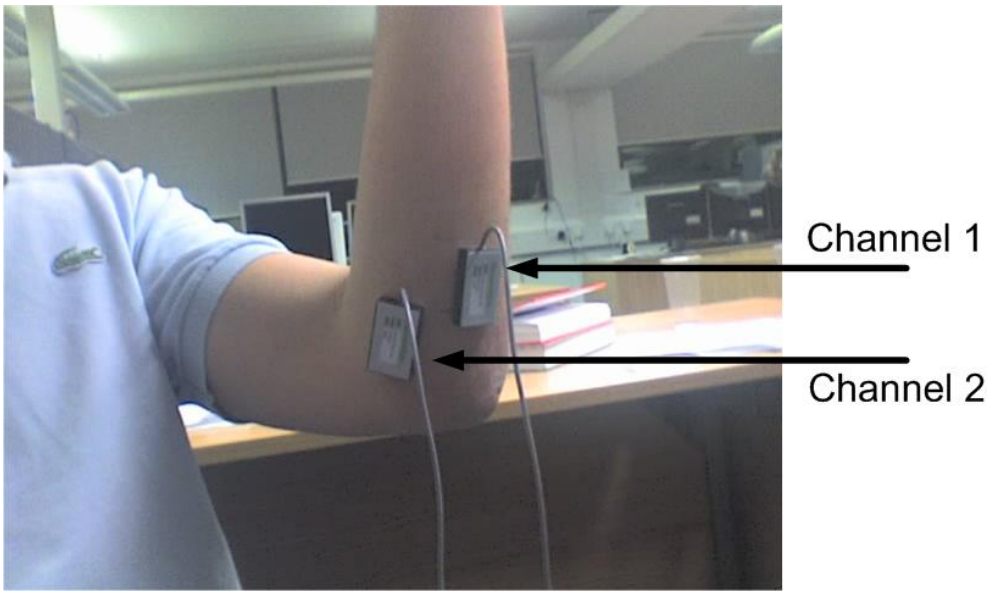

FIGURE 4.15: Position of the electrodes on the upper limb forearm.

amplification of the EMG signals. Interestingly, OP1 and OP2 have different gains, and this is due to the difference in muscle size and therefore different electrical amplitudes required for the stimulation of the muscles.

The amplified EMG signals are then clamped by transistors M1 and the following capacitors. Consequently the inverters (given by M2 and M3) are used as buffer and to provide a high value output voltage each time the clamped EMG signal is high enough to trigger the inverters M2 and M3. While the op-amp OP3 is used as a comparator for the detection of EMG activity and the identification of the middle finger (as described below). The reference voltage used on the negative node of OP3 is chosen to be equal to $35mV$ as this was observed to be on experimental results the minimum voltage required to identify the presence of EMG activity.

Fig. 4.18 shows the output simulation of the system shown in Fig. 4.17 when two EMG signals are captured during the sequential motion of the index, middle and ring finger. Fig. 4.18 (a) and (b) show the captured EMG signals of "Channel 1" and "Channel 2"; Fig. 4.18 (c) and (d) represent the two signals "Clamped 1" and "Clamped 2" of Fig. 4.17, after clamping the signals; Fig. 4.18 (e) and (f) show the output signals (A and B of the circuit in Fig. 4.17) which identify the movement of the index and ring finger; while Fig. 4.18 (g) illustrates the signal provided for the detection of EMG activity which is used for the detection of middle finger movements as the signals "A" and "B" remain low, and this is because the inputs captured at "Channel 1" and"Channel 2" are not high enough to trigger the inverters (M2-M3), but high enough to trigger the comparator OP3 which has a very low reference voltage (35 mV). Therefore, from the combination of the signals shown in Table 4.2 and Fig. 4.18 (e-f-g) it is possible to identify the motion of the index, middle and ring finger. Consequently, these signals can be used to drive the finger motors of the prosthetic hands.

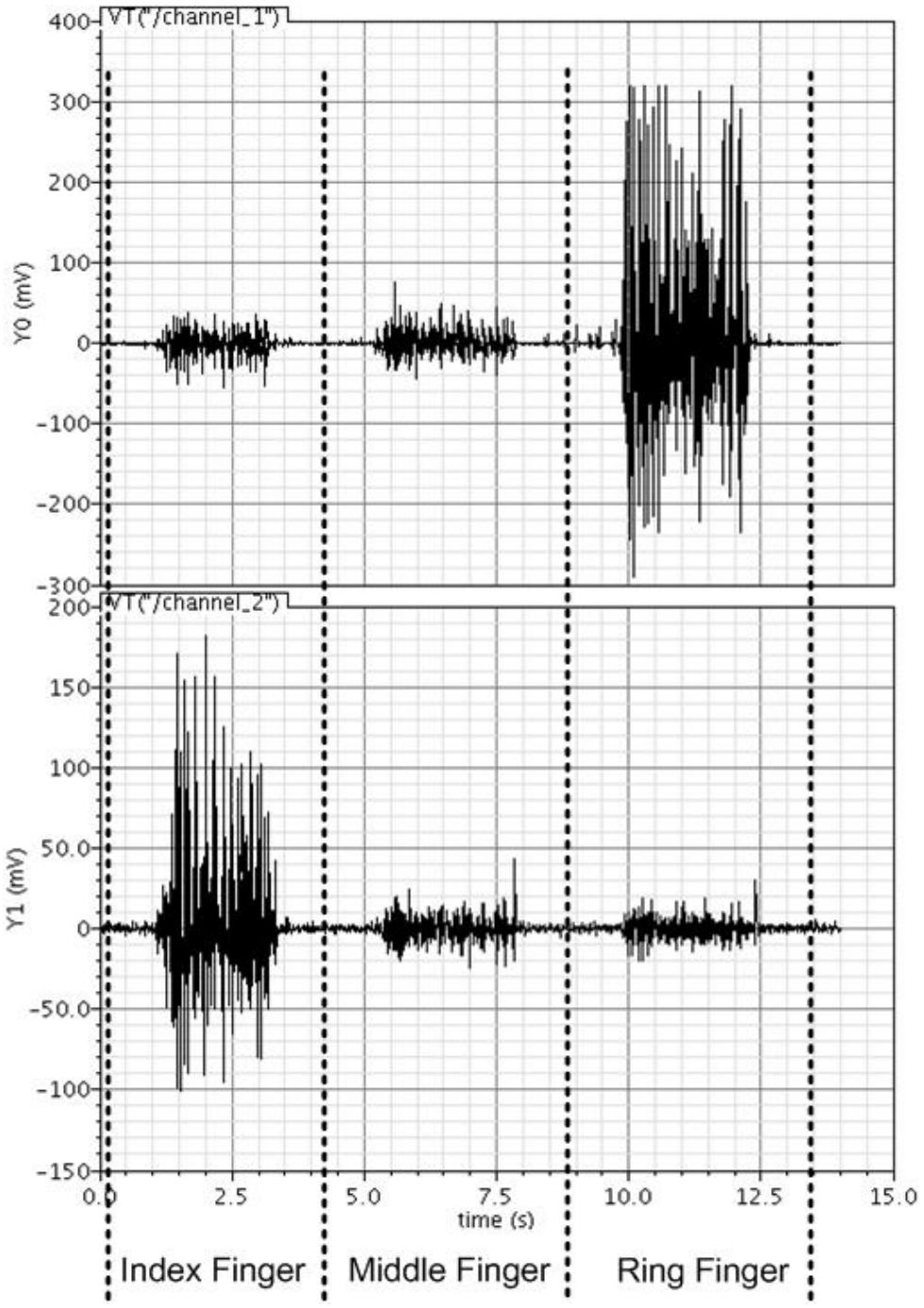

FIGURE 4.16: EMG detection captured on channel 1 and channel 2 for the movements of the index, middle and ring finger.

4.7 Conclusion

In this chapter two analogue approaches for the controlling of prosthetic hands with single and dual EMG signals have been presented. Furthermore the feedback signals

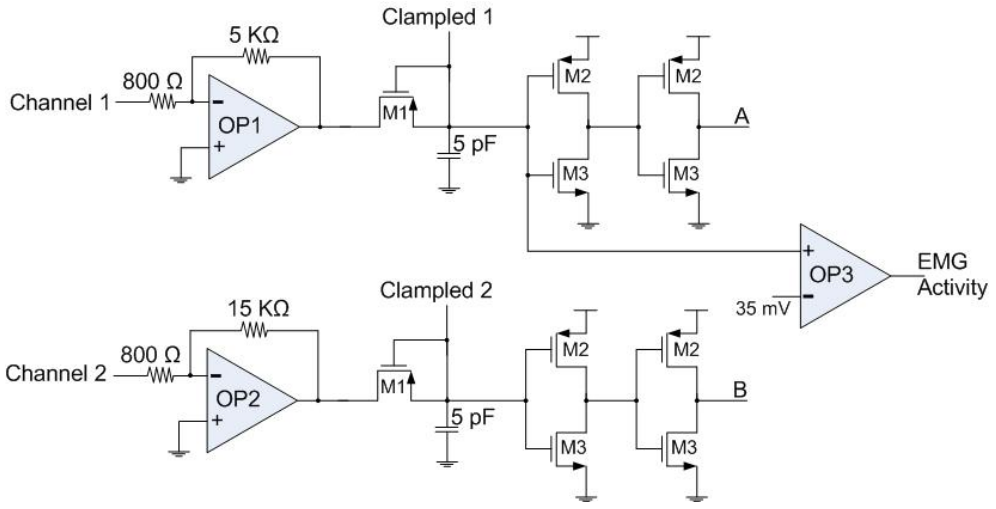

FIGURE 4.17: Schematic of the control unit for the differentiation of individual fingers movements.

TABLE 4.2: Combination of output signals generated by the motion of index, middle and ring finger

	A	**B**	**EMG Activity**
Index Finger	0	1	1
Middle Finger	0	0	1
Ring Finger	1	0	1

from slip and pressure sensors, which are embedded in the prosthetic hand, have also been considered to improve the gripping abilities of the prosthetic hand.

In the first methodology different postures for the prosthetic hand were selected by using a single EMG electrode and by associating the number of incoming EMG stimuli with each posture. This allowed the controlling of prosthetic hands for people with high level of upper limb amputations.

The second methodology involved the use of two electrodes for the capturing of EMG signals where the positioning of the electrodes was dictated by the muscle anatomy which control the finger movements. The novelty of this approach is given by the ability of controlling the index, middle and ring finger in the same manner as in real biological hands.

Real surface EMG signals have been used to validate the performance of the system showing the identification of different postures of the prosthetic hand for both the system presented in sections 4.5 and 4.6.

Furthermore, the system shown in Fig. 4.17 is dramatically simpler than any DSP and NN described in [92, 119–125] and can achieve the same performance when identifying finger movements for prosthetic hands.

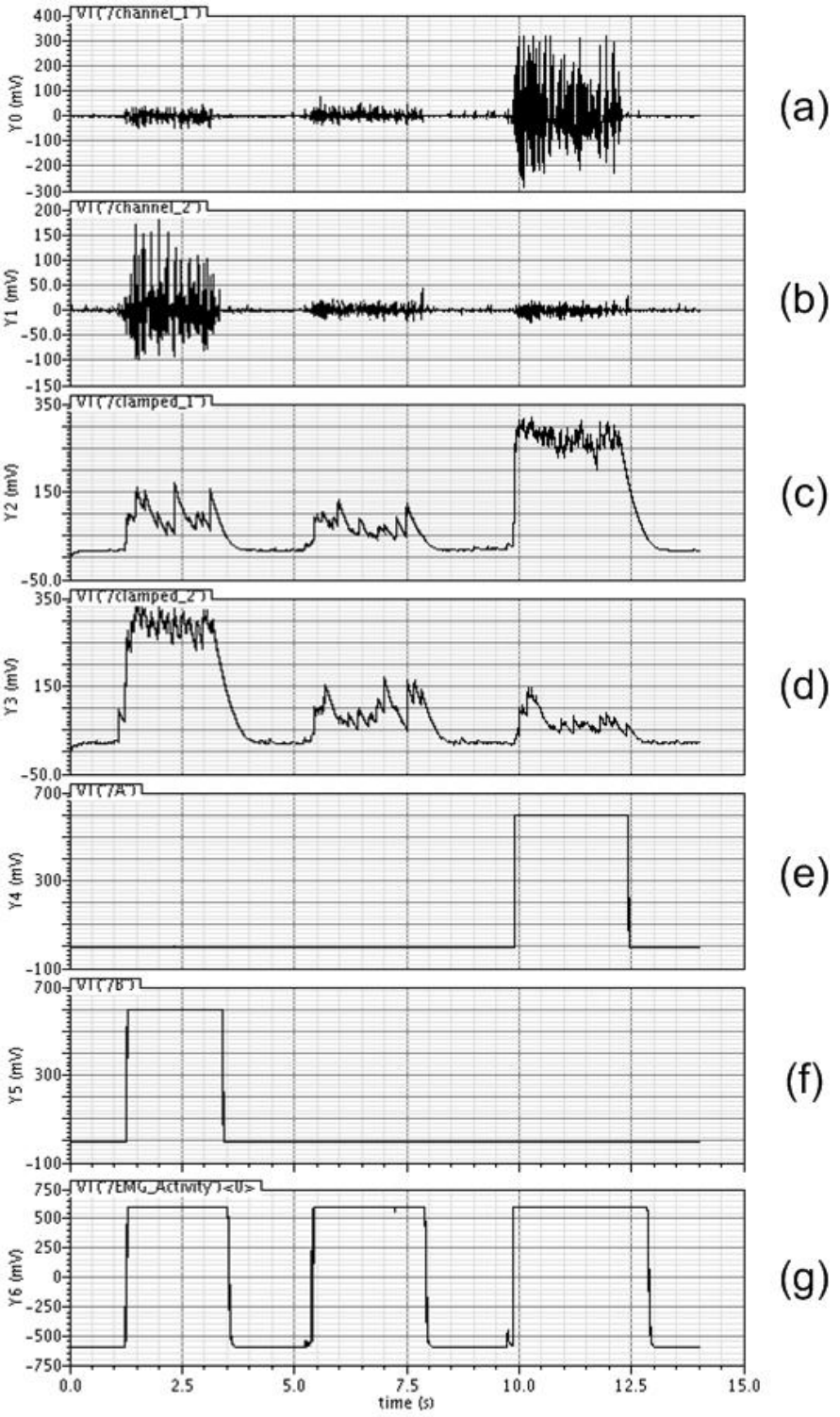

FIGURE 4.18: (a) EMG captured on Channel 1; (b) EMG captured on Channel 2; (c) clamped EMG signal from Channel 1; (d) clamped EMG signal from Channel 2; (e) identification of the index finger; (f) identification of the ring finger; (g) EMG activity which also allows the identification of the middle finger.

Chapter 5

Heart Beat Anomaly Detection

In this chapter a new model of analogue signal processing for an automated detection of heart beat anomalies is presented. The novelty of this work is given by the capabilities of the mathematical algorithm which is implemented in the analogue domain. The analogue ALU described in Chapter 3 with other analogue components allow a very compact circuit implementation and the detection of four different diseases (ventricular premature beats, ventricular tachycardia, atrial fibrillation and atrioventricular blocks). Such system aims to improve the heart monitoring in non-invasive devices allowing a larger number of patients to be monitored and for longer periods of time at a lower cost. Such analogue system is designed in 130nm CMOS technology allowing a very compact design reducing the complexity, the number of processes (e.g. A/D Conversions, software/hardware memory accesses, loop operations for the performance of mathematical calculations, etc.) and can easily be adapted to different users with different ECG characteristics.

5.1 Fundamentals of the Electrocardiogram (ECG)

The electrocardiogram (ECG, also referred to as EKG) is a transthoracic interpretation of the electrical activity of the heart over time which is captured over the skin with the use of electrodes. The ECG is used by cardiologists to check and provide evidence to support a diagnosis as this provides a wealth of information about the status of the heart [133]. Therefore, it is important to consider the ECG as a tool rather than an end [134].

5.1.1 The Electrical Activity of the Heart

A human heart is divided into four chambers as shown in Fig. 5.1: right atrium, left atrium, right ventricle and left ventricle. The electroactivity of the heart synchronizes

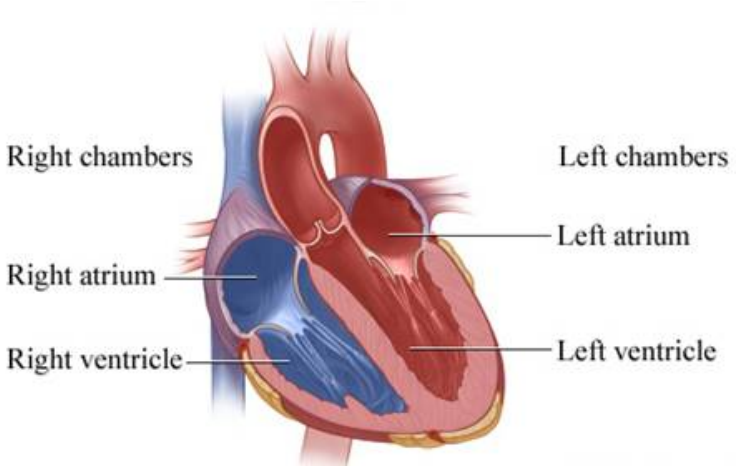

FIGURE 5.1: Internal structure of the heart, showing the four chambers of the heart [135].

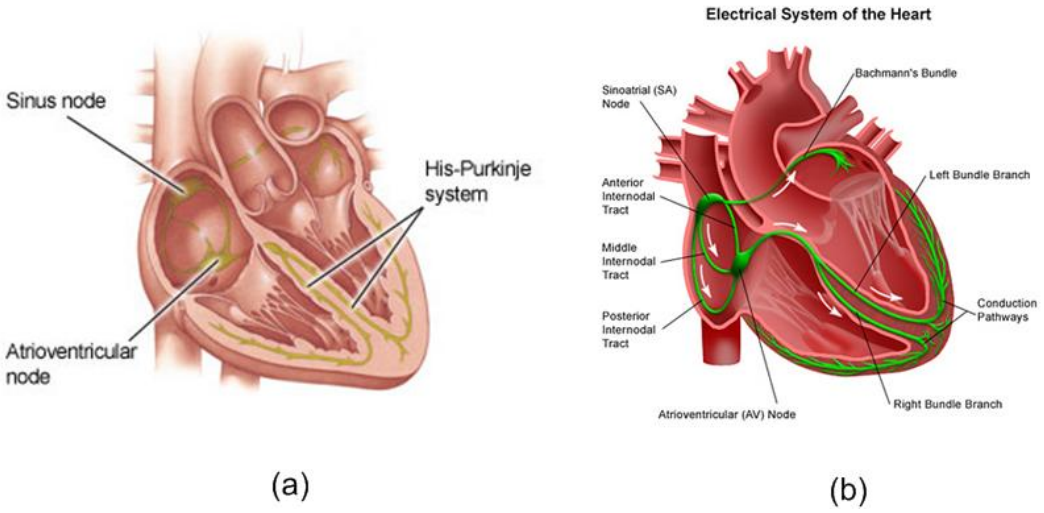

FIGURE 5.2: (a) nerve nodes of the heart where the electrical signals circulate in order to activate the heart; (b) electrical path of the ECG signal in the heart [135].

the movements of the heart in order to pump the blood into circulation.

The contraction of the muscles of the heart can be associated with changes in electrical potential which can be referred to as depolarisation. Such depolarisation activities can also be caused by other muscle activities as for chest and arm movements [134], thus, it is important to distinguish the ECG signals from other artifacts.

The cardiac electrical cycle of the heart normally starts from an area of the atrium called sino-atrial (SA) node, as shown in Fig. 5.2 (a); the depolarisation consequently spreads through the muscle fibres of the atria down to another area of the right atrium called atrioventricular (AV) node. Subsequently, the electrical signal travels down to the ventriculi through two specialized branches called "left bundle of His" and "right bundle of His" or simply "left bundle branch" and "right bundle branch" (see Fig. 5.2 (b)). Fig. 5.2 (b) shows the internal electrical path presented in the heart.

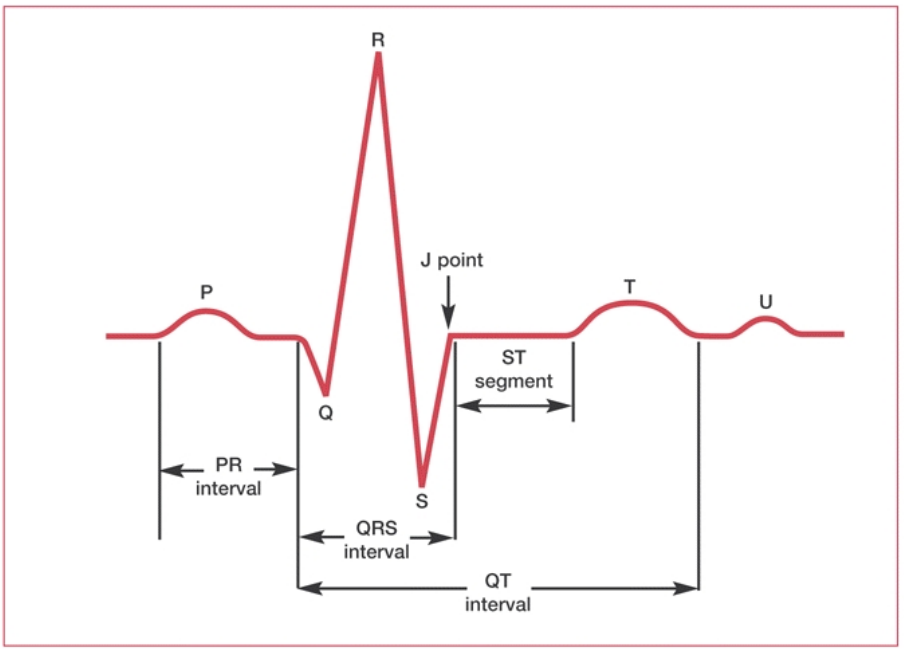

FIGURE 5.3: Shape of a normal ECG, including a U wave.

5.1.2 The Different Parts of the ECG

From Fig. 5.1 it is possible to observe that the mass muscle of the two atria is smaller compared to the two ventriculi. Hence, the electrical activity which controls the contraction of the atria is smaller than the one contracting the ventriculi. The contraction of the atria is referred to as "P-wave" on an ECG, as shown in Fig. 5.3; while, the depolarisation of the ventriculi is referred to as "QRS complex" and the "T-wave" is associated to the return of the resting state of the ventriculi [134, 135]. In some ECGs an extra wave, the "U-wave", is also present; the origin of such wave are quite uncertain though it can be associated to eventual re-polarization of some of the cardiac muscle tissues [134]. Additionally, the contraction of the left and right ventricles are not entirely concurrent, and this is verified in the "QRS complex" where the "R-wave" represents the contraction of the left ventricle whilst the "S-wave" represents the contraction of the right ventricle.

5.1.3 ECG Leads

The word "lead" is often confused with the hardware association of "wire" which connects the patient to the recorder; instead, refers to the electrical activity captured by a set of electrodes. Different types of recorders (electrocardiogram machines) are presented with a number of electrodes (> 2) and are applied around the chest area to capture ECG activity, allowing the doctors to examine different parts of the heart. Fig. 5.4 shows an example of a six electrodes cardiogram. The six V leads ($V_1 - V6$) look at the heart from a horizontal plane (from the front and the left side of the chest). Leads

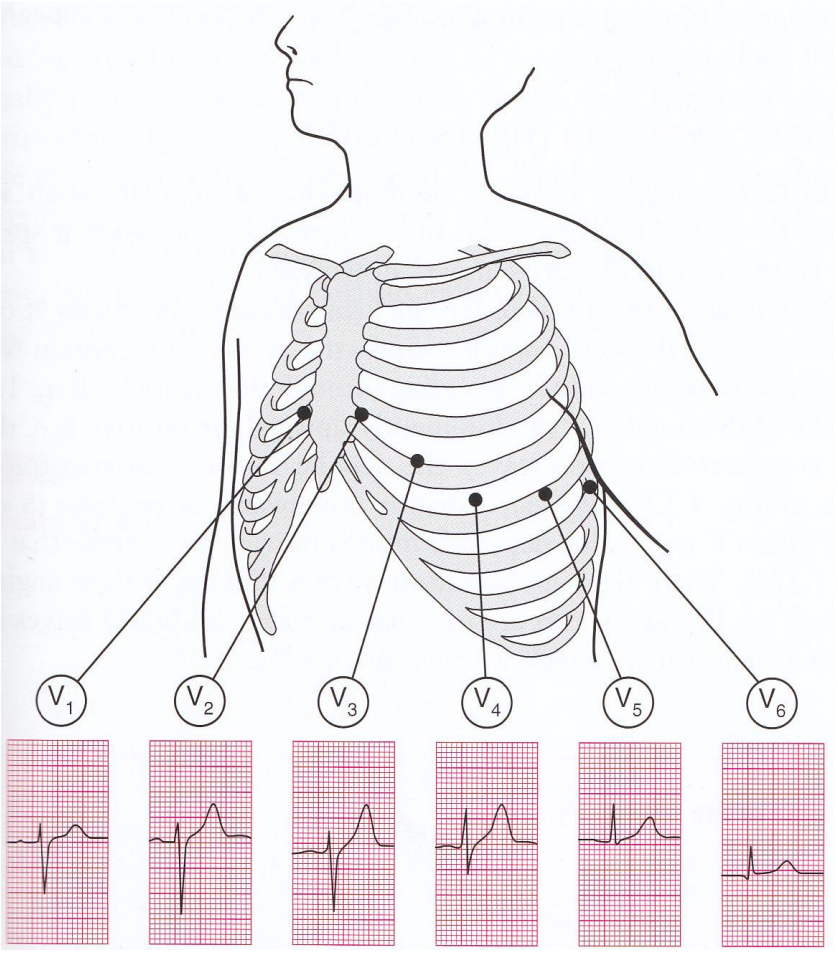

FIGURE 5.4: Visualization of the electrical activity captured on different leads [135].

V_1 and V_2 show the right ventricle, V_3 and V_4 look at the septum between the ventriculi and the anterior wall of the left ventricle [135]; while V_5 and V_6 show the anterior and lateral walls of the left ventricle of the heart [134].
In the work presented in this chapter, only the lead given in the area of the electrodes V_5 and V_6 were considered and processed as these leads allow a general visualization of both the atria and the ventriculi which allows sufficient information for the algorithm to detect heart beat anomalies.

5.1.4 Isoelectric Artifacts

The isoelectric line of an ECG is identified by the baseline of an ECG as shown in Fig. 5.5. The isoelectric line can vary its baseline position depending on chest and arm movements which alter the distance between the electrodes attached to the patients' chest. Such variations in the baseline are identified as isoelectric artifacts and an example is shown in Fig. 5.6.

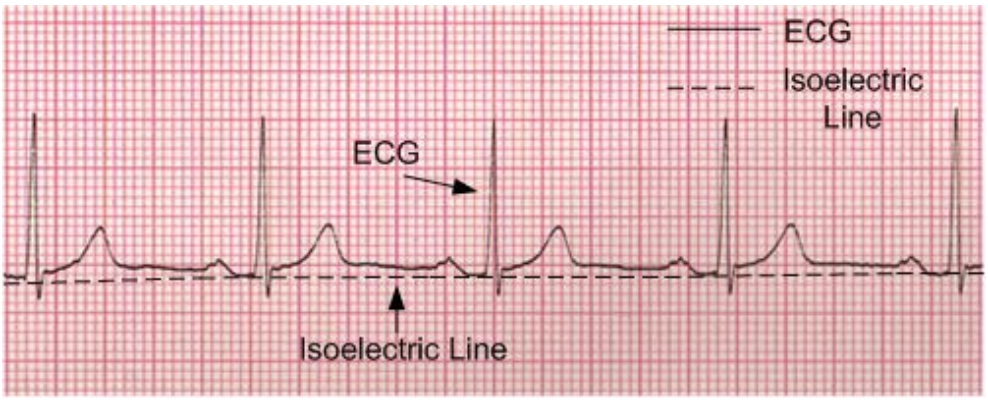

FIGURE 5.5: ECG and identification of the isoelectric line.

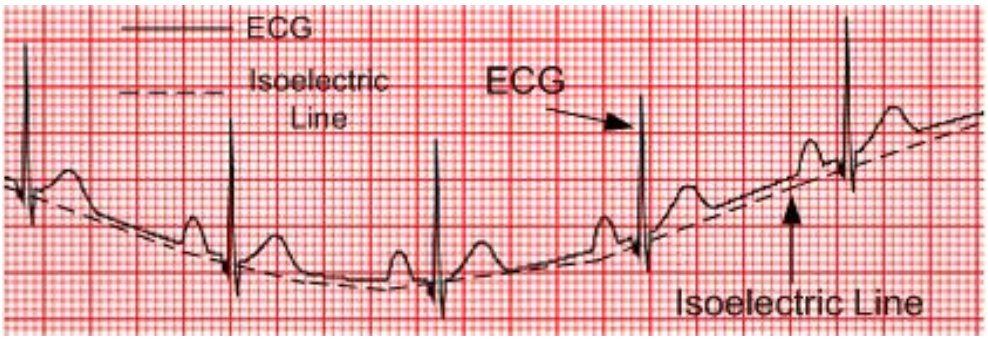

FIGURE 5.6: Example of isoelectric artifact.

5.2 Heart Diseases

The flowing of the blood within the body and the movements of the heart are dictated by the electrical activity of the heart which stimulates the heart in a predefined pattern as described in sections 5.1.1 and 5.1.2. Depending on age and daily habits (such as sport, food, smoking, etc.) the electrical activity can degenerate producing abnormal behaviors and irregularities in the heart activity. Consequently, such abnormalities can deteriorate even further producing physical pain and a regression of the physical abilities of the individual (e.g., the activity of the heart not being able to keep up with the external daily physical activities), and in the long term these can also lead to heart failure causing death.
Therefore, monitoring of the heart activity is extremely important as most of the heart beat irregularities can be used as indicator of the state of the heart. The most important heart beat irregularities (which are targeted for detection by the system) are described in the following subsections.

5.2.1 Ventricular Premature Beats

Ventricular Premature Beats (VPBs) can be common even on healthy individuals and they are usually asymptomatic and benign. A VPB randomly occurs when an ectopic

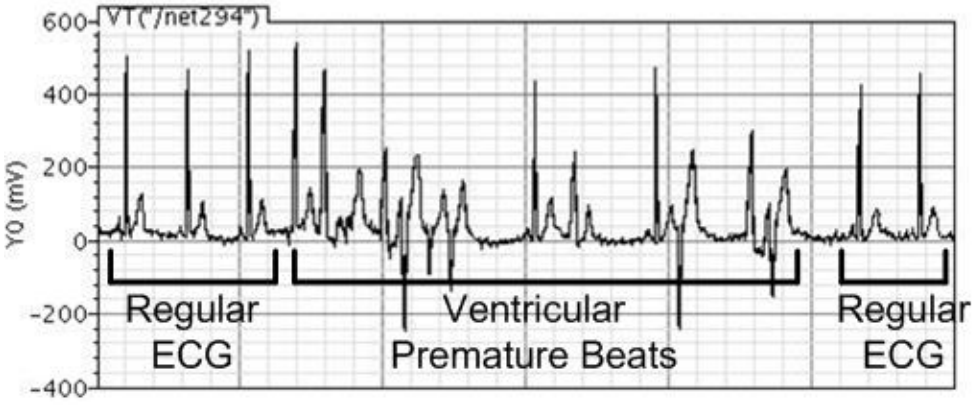

FIGURE 5.7: Example of ventricular premature beat.

ventricular focus fires an action potential [133] without following the regular ECG complex where a ventricular beat should be proceeded by a P-wave and followed by a T-wave. It is possible to recognise a VPB as they randomly appear on an ECG, as shown in Fig. 5.7. VPBs are not dangerous for people without any heart disease, although they are very important in patients who have a structural heart disease as they may lead to an increase in risks of ventricular tachycardia (explained in the following paragraph) or fibrillation [133]. Furthermore, when VPBs occur quite frequently or appear in couplets (two in a row) or triplets (three in a row) they can lead to a high risk of mortality [134].

5.2.2 Ventricular Tachycardia

A ventricular tachycardia (VT) is defined as a series of three or more VPBs in a row as shown in Fig . 5.8. A VT can be classified into two different categories: if the VT persists for more than 30 seconds it is called "sustained VT" otherwise it is referred to as "non-sustained VT". Additionally if the QRS complexes which appear during the VT appear the same and at a regular rate, they are called "monomorphic VT" and it can be due to an old infarction which the heart might have experienced in the past; vice versa, when the shape of the QRS complexes in the VT vary in time the VT is referred to as "polymorphic VT" [133].
In most cases the symptoms provoked by VT depend on the duration of the tachycardia, the rate, and the condition of the heart and can be manifested by the patients with hypotension and loss of consciousness [133]. Therefore, symptomatic of sustained VTs can be dangerous as they can deteriorate into a fatal ventricular fibrillation. Treatments involve implanted electrical defibrillator with additional antiarrhythmic drugs for chronic suppression [133].

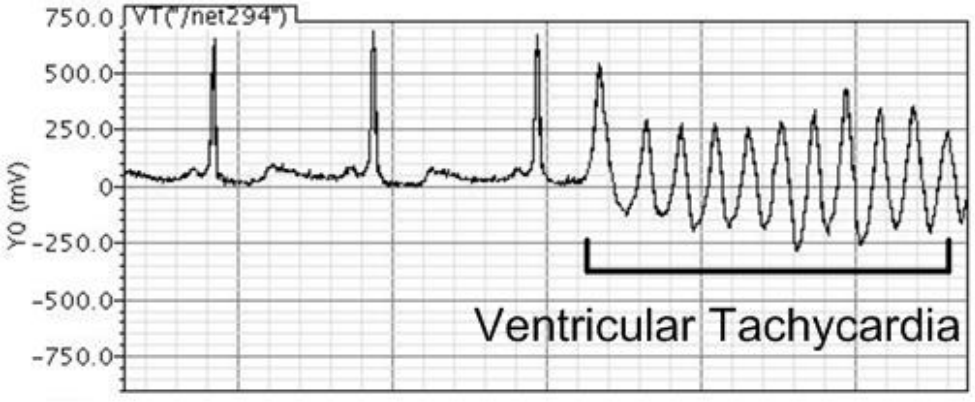

FIGURE 5.8: Example of ventricular tachycardia.

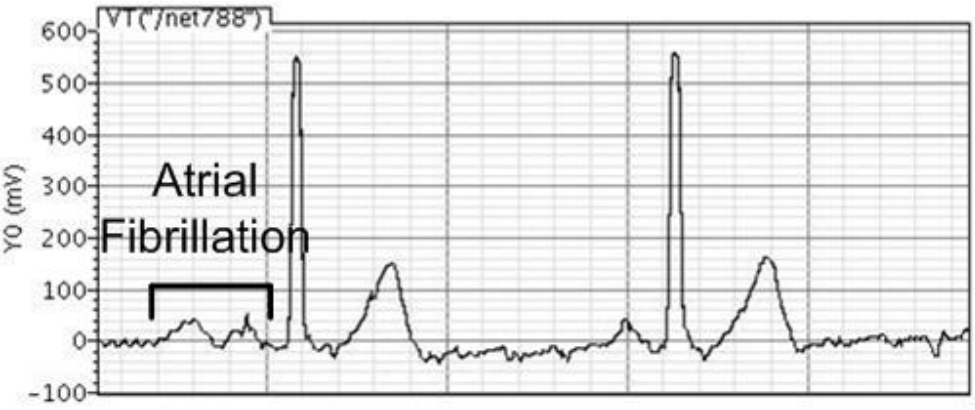

FIGURE 5.9: Example of atrial fibrillation.

5.2.3 Atrial Fibrillation

Atrial fibrillation (AF) is a chaotic rhythm with an atrial rate which can reach 350-600 contractions per minute [133]. Such irregularities of the atria are visible on the ECG through the P-wave, as also shown in the example of Fig. 5.9 where multiple P-waves can appear to generate AF. AF is usually common in patients who suffer from hypertension, coronary artery disease, alcohol intoxication, thyrotoxicosis, pulmonary diseases and also people who were subject to cardiothoracic surgery.
This type of heart beat anomaly can be classified as potentially dangerous since AF can increase the ventricular rates causing hypotension and pulmonary congestion. Additionally, the large number of AF can promote blood stasis in the atria and therefore increase the risk of thrombi which might lead to stroke. Usually, AF is treated with strong antiarrhythmic drugs which can also cause serious and sometime lethal side effects [133].

5.2.4 Atrioventricular Blocks

Atrioventricular blocks (AV blocks) involve the interruption of the ECG complex after the generation of the P-wave as shown in Fig. 5.10. More moderate episodes of AV blocks

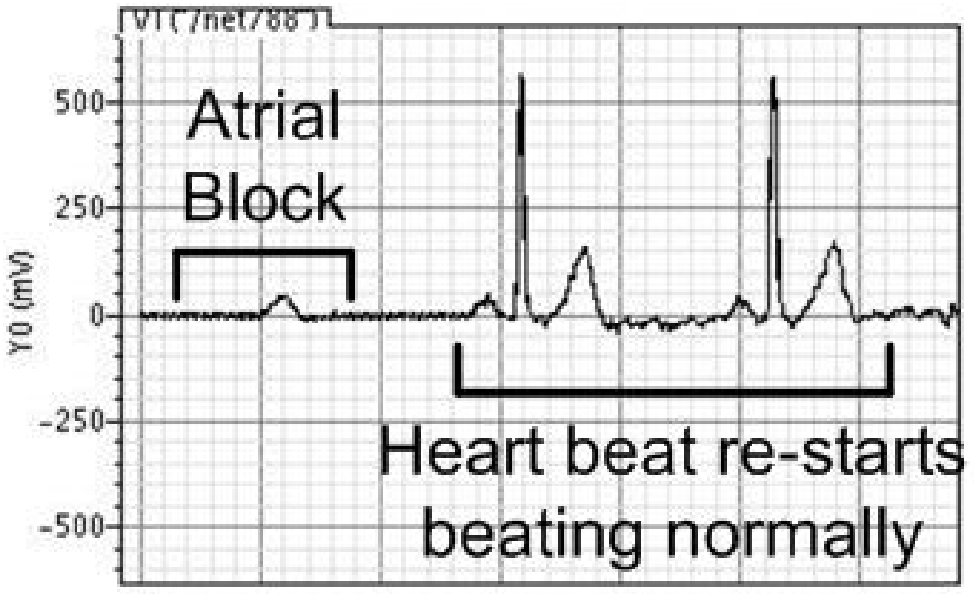

FIGURE 5.10: Example of atrioventricular block.

(often referred to as first degree AV blocks) simply involve a larger interval between the P-wave and the QRS complex without actually blocking the ECG characteristics; usually, this degree of AV block is benign which does not require any form of treatment although the gravity of the AV block might increase in time. For higher degrees of AV blocks (second and high degree of AV blocks) the ventricles do not reach enough potential to start a QRS complex and therefore a number of P-waves are shown on the ECG.

5.3 Related Works and Similar Systems

Nowadays, heart monitoring is divided into two different categories: invasive and non-invasive. Both these methods are chosen regarding the gravity of the patients' heart conditions, the data which have to be provided to the doctors and the sort of device which might re-stabilize the heart activity.
Three main devices can be used for such purposes: (a) the Holter device which has the feature of being non-invasive but with the constraint of recording ECGs for periods of 24-48 hours [136]; (b) the Loop Recorder, an invasive device which can operate for periods of 6-12 months to capture less frequent heart pathologies [137]. Additionally, such device is also presented with a remote control device, provided to the user, to store into memory recorded loops of ECGs when the user presents chest pains, fainting, etc. And (c), the Pacemaker which is another invasive device capable of monitoring and intervening during the heart activity to correct the heart beat rhythms [136, 138].
One other main constraint given by (b) and (c) is the applicability of these devices to only patients with a severe heart status. This is due to the costs of the implantable materials which need to be compatible with the human tissues and the corrosive liquids

of the body plus electronics, and days of hospitalization for eventual technical problems, infections or internal hematomas. Therefore, these constraints lead to a reduced number of patients who could be monitored for a long period of time both inside or outside hospitals.

5.3.1 Aims and Contributions

The aim of this work is to provide a new non-invasive compact mobile device for monitoring and automatically detecting ECG irregularities which will allow a larger number of patients to be monitored at a lower cost. Such method for automatic detection of ECG irregularities allows the selection of ECG traces when only heart beat anomalies are detected, in this way the device can save memory space and last for longer periods of time.
To be noted that the presented work does not concentrate on designing a new capturing circuit for ECG signals but on a new signal processor which can be used for the analysis of ECG signals and automatic detection of heart beat irregularities.
It will be shown in the following sections how the presented system can automatically eliminate isoelectric artifacts and identify heart beat anomalies as ventricular premature beats, ventricular tachycardia, atrial fibrillation and atrioventricular blocks. Additionally, the developed algorithm can be suitable for the detection of other heart beat alterations such as ST elevation and QT prolongation.
Such system is designed in the analogue domain to allow a very compact circuit which can easily perform mathematical operations (e.g. multiplication, integrations, etc.) and reduce the number of processes required in digital systems. Fig. 5.11, represents an example of how the signal processor could be connected to any general ECG capturing circuitry to analyse the captured ECG signal for eventual heart beat irregularities. Further implementations could also be used to send the detected ECG anomalies to a predefined hospital via computer or mobile phone as shown in Fig. 5.11.

5.4 Methodology for Heart Beat Anomaly Detection

The identification of heart beat irregularities can be achieved by formulating a mathematical algorithm which gives a different output response for different ECG irregularities such as ventricular premature beats (VPBs), ventricular tachycardia (VT), atrial fibrillation (AF) and atrioventricular blocks (AV blocks). Such algorithm must have the ability of differentiating each of these heart beat anomalies and also regular ECGs into different bands allowing the recognition of each ECG irregularity.
The implementation of such methodology was inspired by the fact that humans can simply recognize a “pattern” by observing an ECG lead; therefore, in order to let a

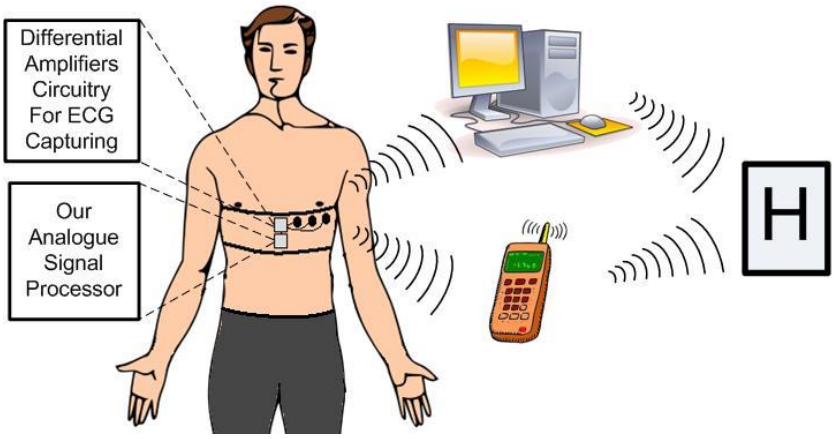

FIGURE 5.11: System example.

machine understand the different patterns generated by the different case scenarios, a mathematical integration of an ECG lead (calculation of the area under each ECG complex, see Eq. 5.1) can generate different output responses and consequently differentiate regular and unhealthy ECGs.

$$V_{out,ECG} = \int_{t_0}^{t_1} K \cdot V_{in} dt \tag{5.1}$$

V_{in} in Eq. 5.1 represents the captured ECG signal, K can be used as an adjustable gain, while t_0 and t_1 represent the beginning and end of each cardiac activity. Therefore, the integration of the incoming ECG is initiated with the start of ECG activity (e.g. with a P-wave) and it stops integrating only when the ECG electrical activity disappears. Such methodology allows the classification of different heart diseases where the heart beat has different time durations.

In order to validate the algorithm described in Eq. 5.1 and the capability of differentiating regular and different ECG irregularities, the Physionet ECG Database has been used to test over 90 different real ECGs including healthy and unhealthy patients which presented VPB, VT, AF, and AV blocks. Eq. 5.2 shows the different ECG databases for each heart beat anomaly within the Physionet ECG database. Such ECGs also required a pre-calibration process (as offset removal and amplitude re-adjustment which was processed on MatLab) as these signals have been captured with different ECG portable devices.

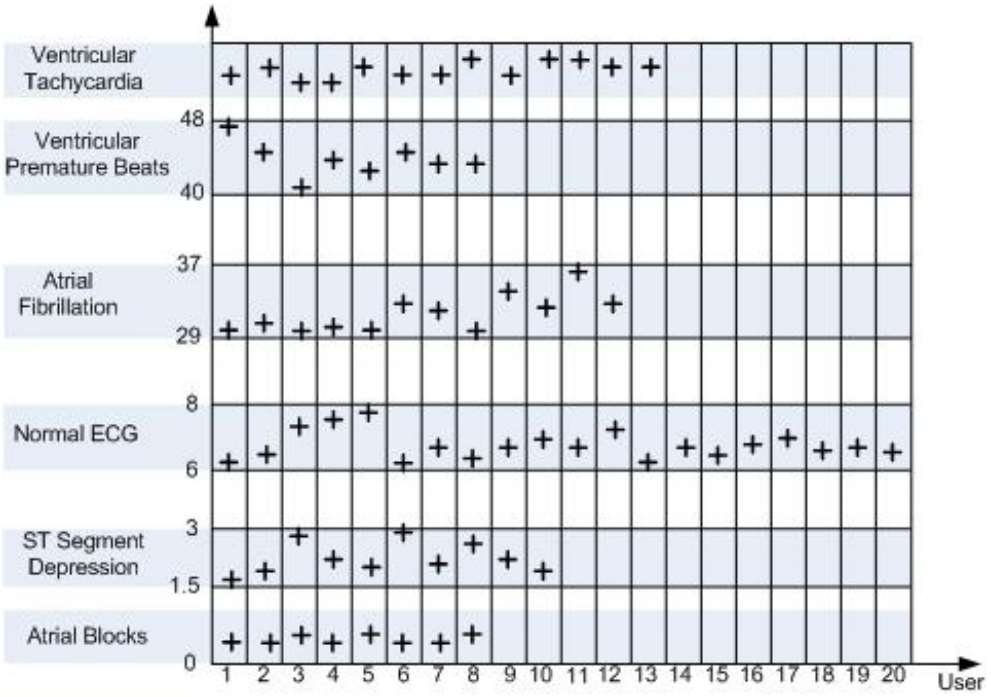

FIGURE 5.12: Statistical analysis of Normal ECG and different heart beat anomalies.

$$\begin{cases} VentricularTachycardia, & \text{The Creighton University Ventricular Tachyarrhythmia Database} \\ VentricularPrematureBeats, & \text{The Sudden Cardiac Death Holter Database and The Creighton University Ventricular Tachyarrhythmia Database} \\ AtrialFibrillation, & \text{Intracardiac Atrial Fibrillation Database} \\ NormalECG, & \text{The PTB Diagnostic ECG Database} \\ STSegmentDepression, & \text{The MIT-BIH ST Change Database} \end{cases} \tag{5.2}$$

Fig. 5.12 shows the different results which were obtained on MatLab when applying Eq. 5.1 to different patients with different ECG irregularities. Also to be noted, in the graph of Fig. 5.12, it is shown the integration result of ST segment depression, which it is not been considered in this work as this is a heart anomaly which is generated by different pharmaceutical drugs other than a natural ECG irregularity.

As it is possible to see in the graph of Fig. 5.12, the regular and irregular ECGs can be categorized into different bands which are also described in Eq. 5.3.

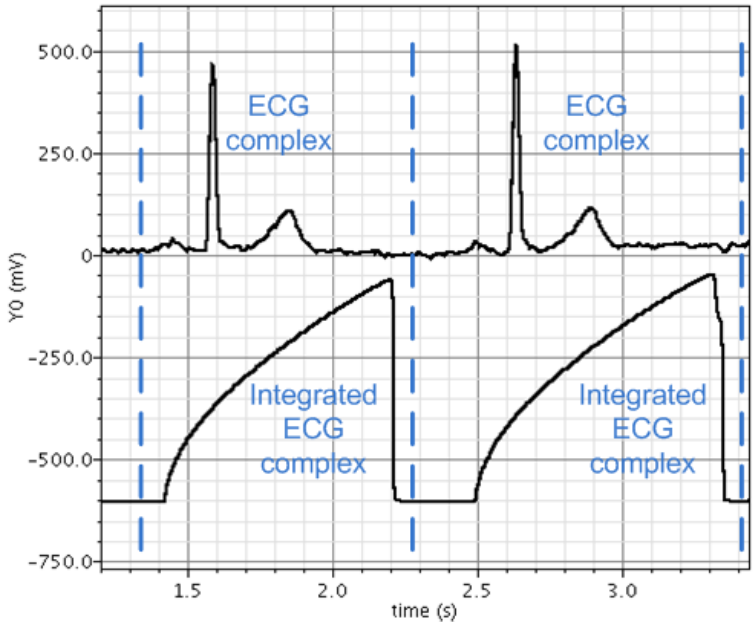

FIGURE 5.13: Example of ECG complexes and their resulting integration value.

$$\begin{cases} 0 < V_{out,ECG} < 1.3, & \text{Atrioventricular Blocks (AV blocks)} \\ 1.5 < V_{out,ECG} < 3, & \text{ST Segment Depression} \\ 6 < V_{out,ECG} < 8, & \text{Normal ECG} \\ 29 < V_{out,ECG} < 37, & \text{Atrial Fibrillation (AF)} \\ 40 < V_{out,ECG} < 48, & \text{Ventricular Premature Beats (VPBs} \\ 50 < V_{out,ECG}, & \text{Ventricular Tachycardia} \end{cases} \tag{5.3}$$

Consequently, from a hardware level description, it is possible to obtain the same information by integrating the input signal as shown in Fig. 5.13 and use a set of comparators to distinguish regular and irregular ECGs as shown in Fig. 5.14. The block diagram of Fig. 5.15 illustrates the different stages and operations which need to be performed, from a hardware point of view, to integrate incoming ECG complexes and identify irregularities within the ECG.

The removal of isoelectric artifacts (shown in the first block in Fig. 5.15) is usually necessary as such artifacts are often present in the ECG leads since most of the filtering processes, which are performed during the capturing of the ECG, aim to delete higher frequency components such as electromyography (EMG) artifacts and other artifacts which can be caused by the user (including noise produced by the skin/electrodes, sweating, or even caused by the user scratching around the electrodes area).

The second stage within the pre-processing block in Fig. 5.15 provides further filtering and amplification. This filtering operation is given by a simple first order low pass filter which aims to delete any residual noise; whereas, the amplification is importantly required to increase the amplitude voltage of the P-wave and the T-wave in each ECG

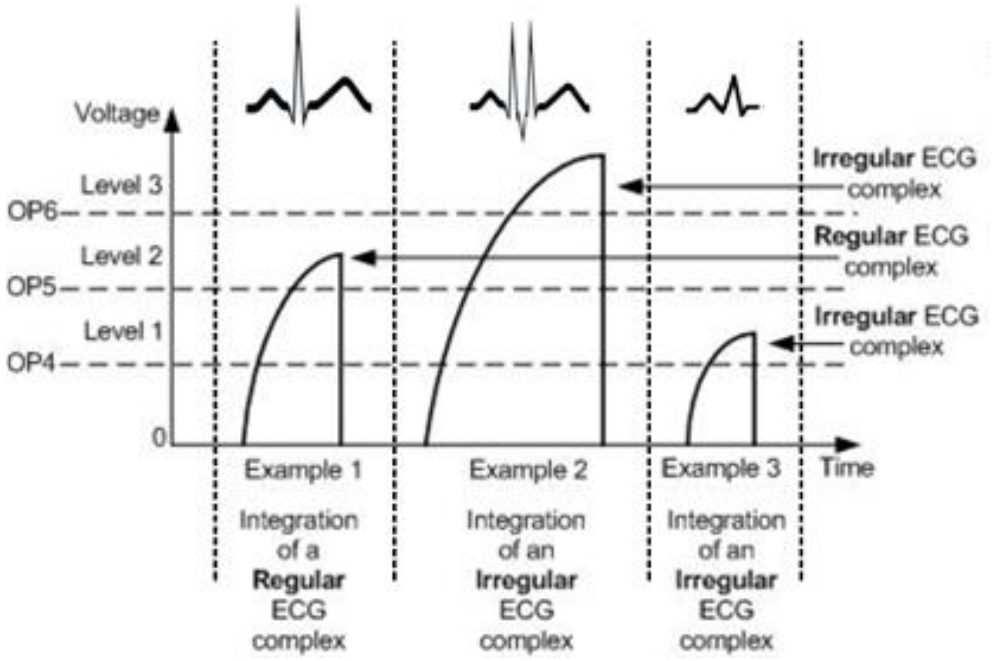

FIGURE 5.14: Examples of different integrated ECG complexes (ECG signatures).

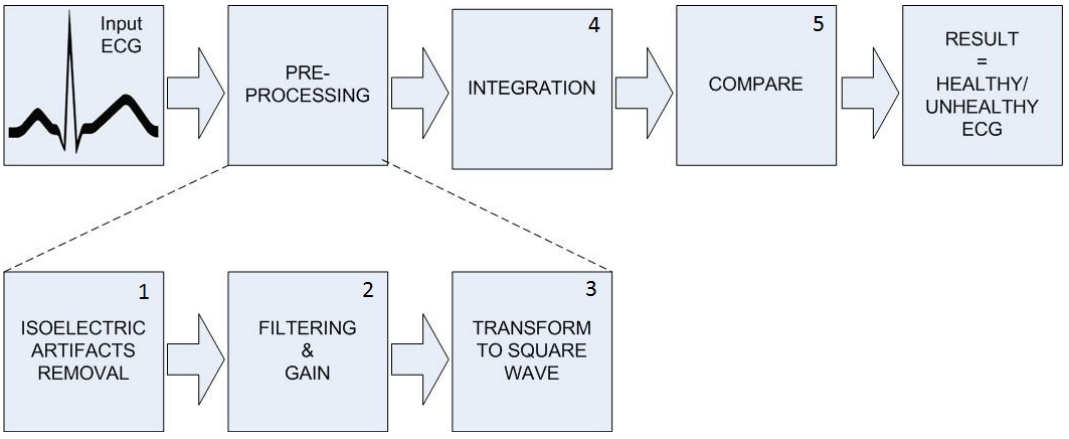

FIGURE 5.15: Block diagram of the operations performed by the proposed analogue signal processing unit.

complex (since these two waves are considerably smaller than the QRS complex, see Fig. 5.3). The amplification of each ECG complex is performed to more easily transform each ECG complex into a square wave (stage 3 in Fig. 5.15) which can then be integrated and classified (with comparators) in stages 4 and 5 respectively to verify whether a regular or an irregular ECG complex has occurred.

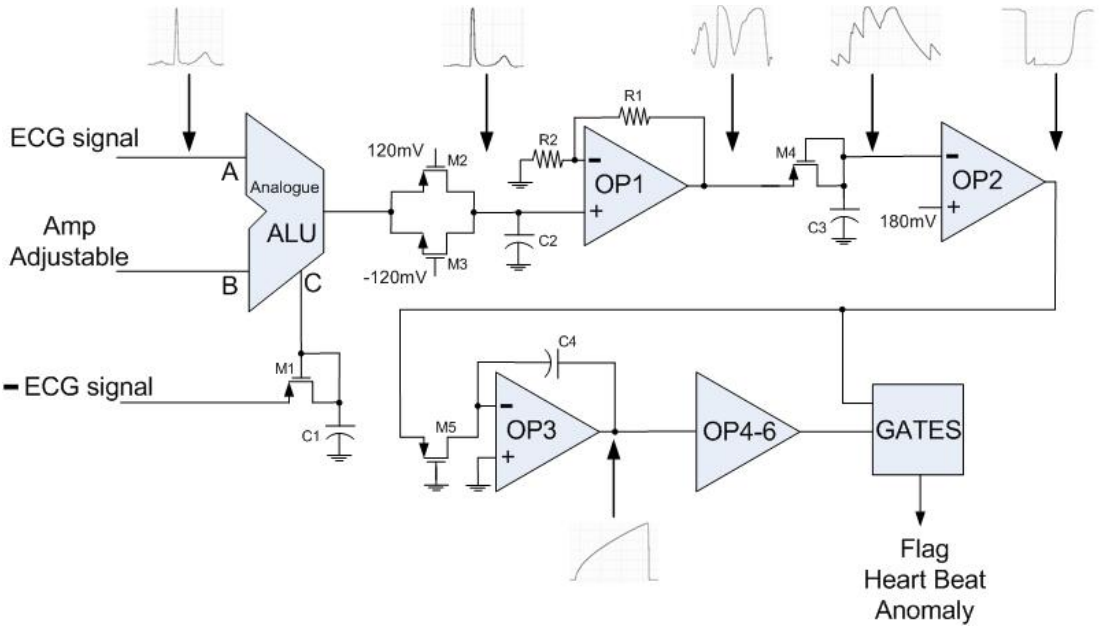

FIGURE 5.16: Schematic of the proposed analogue signal processing unit.

5.5 Circuit Implementation

The different stages described in Fig. 5.15 can be implemented with the circuit schematic of Fig. 5.16. Each of the components are designed and implemented on 130nm CMOS Technology with a dual power supply (±0.6V); a detailed explanation of each of the components is given in the following sections.

5.5.1 Analogue ALU, Filtering and Amplification System

The analogue ALU uses the schematic and mathematical properties described in chapter 3 and it is used to eliminate isoelectric artifacts.
Input A of the analogue ALU in Fig. 5.16 is connected to the incoming ECG signal while input B can be used as a gain as the parameter K in Eq. 5.1. Input C, is used to eliminate isoelectric artifacts and set the isoelectric line of the ECG back to zero (voltage level). The elimination of isoelectric artifacts can be easily achieved in the analogue domain by summing the incoming ECG signal and the resulting amplitude modulated signal of the inverted form of the incoming ECG signal. The amplitude modulated signal of an ECG signal can be generated by inputting an inverted form of the ECG into a peak detector with a predefined time constant. Hence, depending on the RC characteristics of the peak detector configuration it is possible to set the output of the peak detector to follow the isoelectric line as shown in the simulated result of Fig. 5.17. Such peak detector configuration is given by the diode-connected device M1 and capacitor C1 of Fig. 5.16. Capacitor C1 has a capacitance equal to 1 pF while transistor M1 (W=0.15μm; L=4μm) is set as a diode.

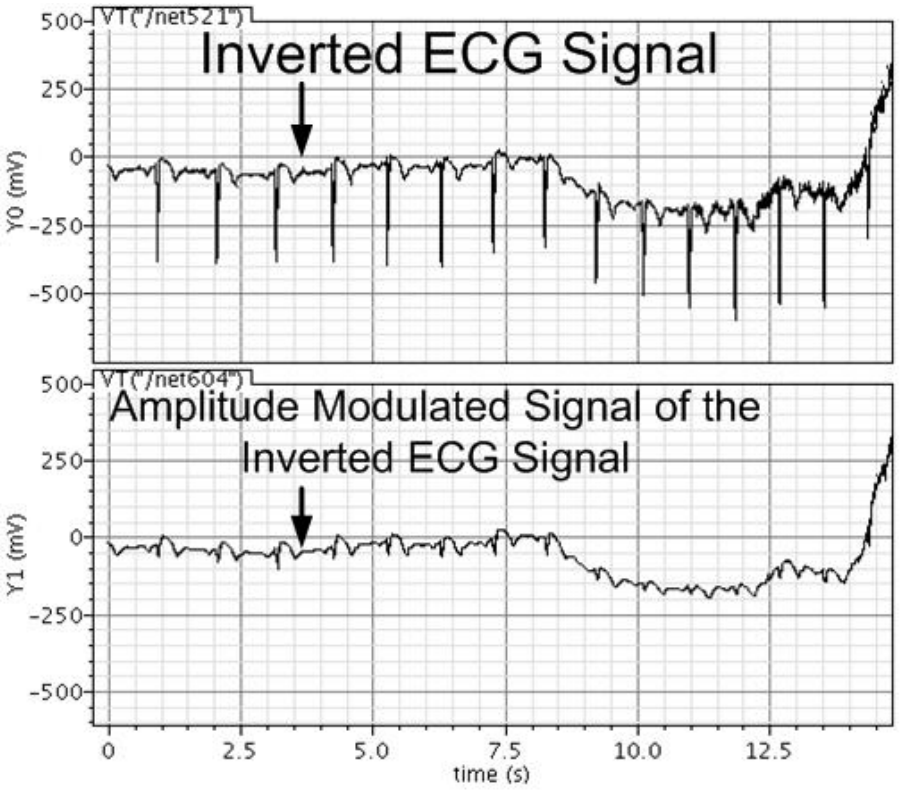

FIGURE 5.17: Inverted form of the incoming ECG signal and its amplitude modulated signal representing the isoelectric line of the incoming ECG.

Transistors M2-M3 with capacitor C2 of Fig. 5.16 are used as a first order low pass filter to eliminate any residual noise present in the ECG. The implementation of this low pass filter is based on the assumption that different ECG capturing systems have different characteristics and can therefore present more noisy output ECG signals. Consequently such low pass filter allows a higher compatibility to different ECG capturing circuits. Transistors M2-M3 are biased to allow a very low leakage current in order to increase the RC constant and obtain a very low pass filter which would only allow frequencies in the range of the ECG complex (e.g. ≈3-12Hz). This results in an RC time constant (τ) equal to 11.5 ms which allows a cut-off frequency of 13.8 Hz with C2 equal to 5 pF.
As previously mentioned, the amplification of the ECG signal is performed to increase the amplitude voltage of the P-wave and the T-wave. Fig. 5.18 (a) and (b) show the incoming ECG complex and the output of the amplified ECG complex at the output of OP1 (see Fig. 5.16). To be noted that the amplification of the QRS complex is limited by the power supply voltage level.

5.5.2 Peak Detector and Comparator

The configuration given by the diode-connected device M4 (W=0.15μm; L=1μm) with the capacitor C3 (5 pF) is set as a peak detector (see Fig. 5.16). Such configuration is used to hold the voltage across the capacitor C3 during cardiac electrical activity.

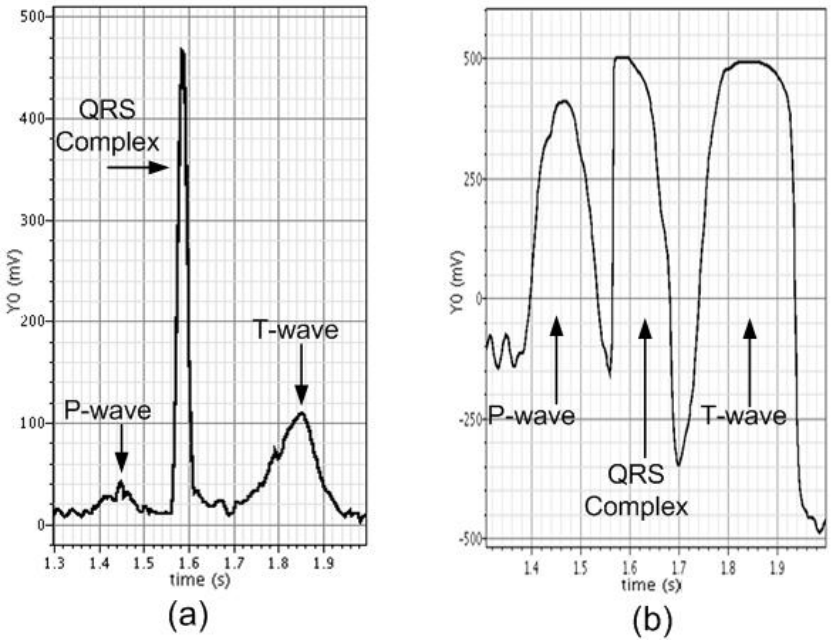

FIGURE 5.18: Amplification of the ECG complex. (a) incoming input A; (b) amplified ECG at the output of the amplifier OP1 (see Fig. 5.16)

Op-amp OP2 is used as a comparator to give a high output voltage each time the input at the negative input node is lower than the reference voltage at its positive input node (see Fig. 5.16).
Fig. 5.19 shows the voltage at three different stages of the block diagram of Fig. 5.16. Fig. 5.19 (a) illustrates the amplified ECG signal from OP1; the output of OP1 is then inputted into the peak detector configuration (set by M4-C3) to give the output voltage illustrated in Fig. 5.19 (b); while Fig. 5.19 (c) shows the output of the comparator OP2 which is controlled by the reference voltage set on the positive input node and the voltage across capacitor C3 on the negative input node.

5.5.3 Integrator

The mathematical integration of each ECG complex is achieved by the integrator OP3 (see Fig. 5.16) after performing the operations described in sections 5.5.1 and 5.5.2.
Fig. 5.13 shows an example of incoming ECG complexes and their associated signatures generated by the integrator OP3.
Such integration [104] is given by op-amp OP3, capacitor C4 (5 pF) and the PMOS transistor M5 (W=0.15μm; L=0.8μm) of Fig. 5.16.

5.5.4 Heart Beat Anomaly Detection

The integration of each ECG complex needs comparisons to evaluate whether each ECG complex presented any irregularity. Such operation is carried out in the final processing

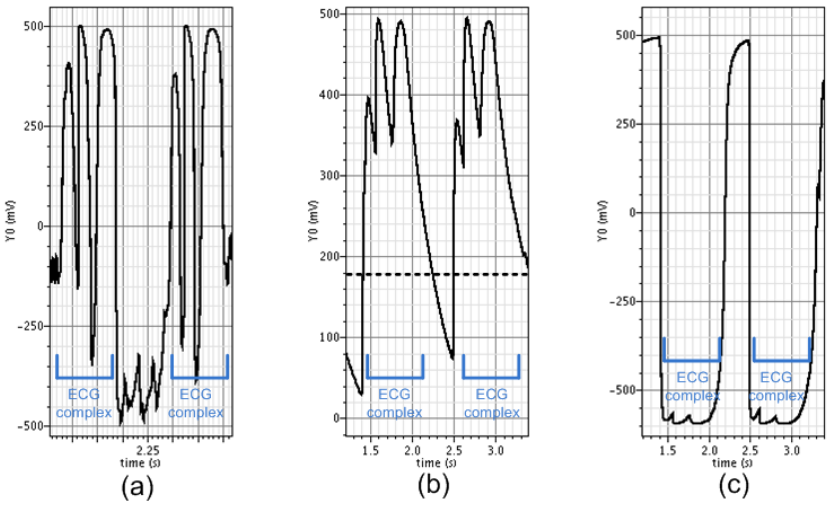

FIGURE 5.19: reference to Fig. 5.16 - (a) represents amplified ECG complex of output OP1; (b) output of the peak detector M4-C3; (c) output of the comparator OP2 Fig.5.16.

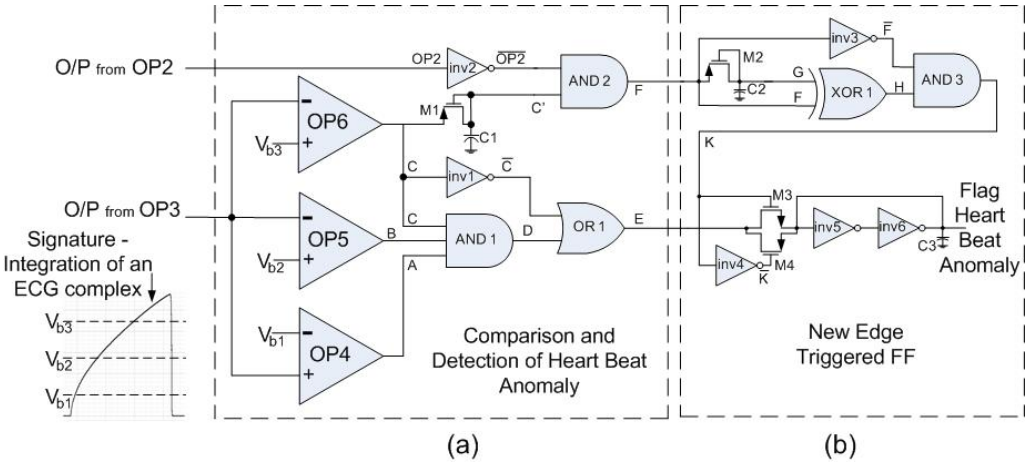

FIGURE 5.20: Level comparators given by Op4-OP6 and the logic to flag and store the heart beat anomaly.

block (labeled as GATES) in the block diagram of Fig. 5.16; while Fig. 5.20 shows a detailed view of the internal components of this processing block.

From Fig. 5.20 it is possible to observe both analogue and digital components; where, op-amps OP4-OP6 represent three level comparators which are used to compare the maximum amplitude voltages given by the integrator OP3 to determine whether an irregularity has occurred (as shown in the example of Fig. 5.14). While the digital components are used to evaluate the output signals of the level comparators OP4-OP6 and flag eventual heart beat anomalies.

Furthermore, the circuitry shown in Fig. 5.20 can be divided into two different parts: a circuit for the comparison and evaluation of heart beat anomalies (Fig. 5.20(a)), and a new model of an edge triggered flip flop (Fig. 5.20(b)) to flag the presence of occurring heart beat irregularities.

The inverter (inv1), the AND gate (AND1) and the OR gate (OR1) of Fig. 5.20(a), are

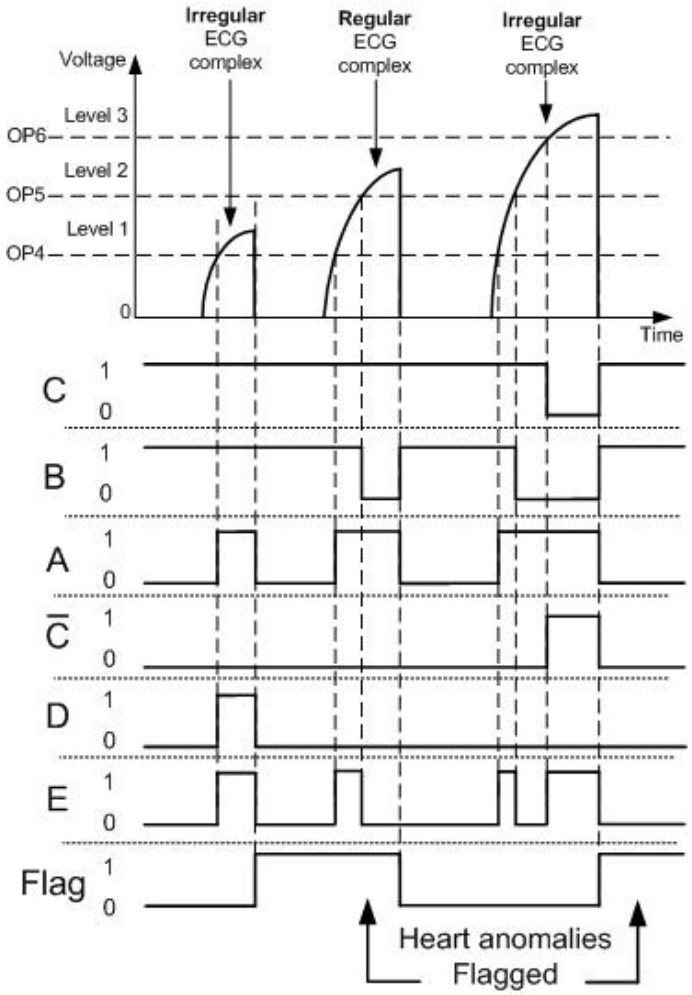

FIGURE 5.21: Time diagram.

configured to interact with the outputs of each level comparator (OP4-OP6) (as shown in the time diagram example of Fig. 5.21) to obtain a high amplitude voltage each time an anomaly in the heart beat has been detected. The output value of the gate OR1 is then stored into the edge triggered flip flop of Fig. 5.20(b) which is clocked at each falling edge of the output of the gate AND2. From Fig. 5.20 it is possible to observe that the gate AND2 is triggered by the output of the level comparator OP6, and by the inverted form of the output of the level comparator OP2 (refer to Fig. 5.16). The configuration given by transistor M2 (W=0.15μm; L=0.4μm), capacitor C2 (150 fF), the inverter (inv3), the XOR gate (XOR1) and the AND gate (AND3) is set to generate a pulse for every incoming falling edge (given at the input F) which is used to set the output node (labeled as Flag in Fig. 5.20) equal to the incoming input of node E. Fig. 5.22 shows a simulated example of how this new model of flip flop works. Furthermore, the width of the generated pulse (on the node K, also see Fig. 5.22) can be modified by changing the time constant generated by the values of transistor M2 and the capacitor C2.

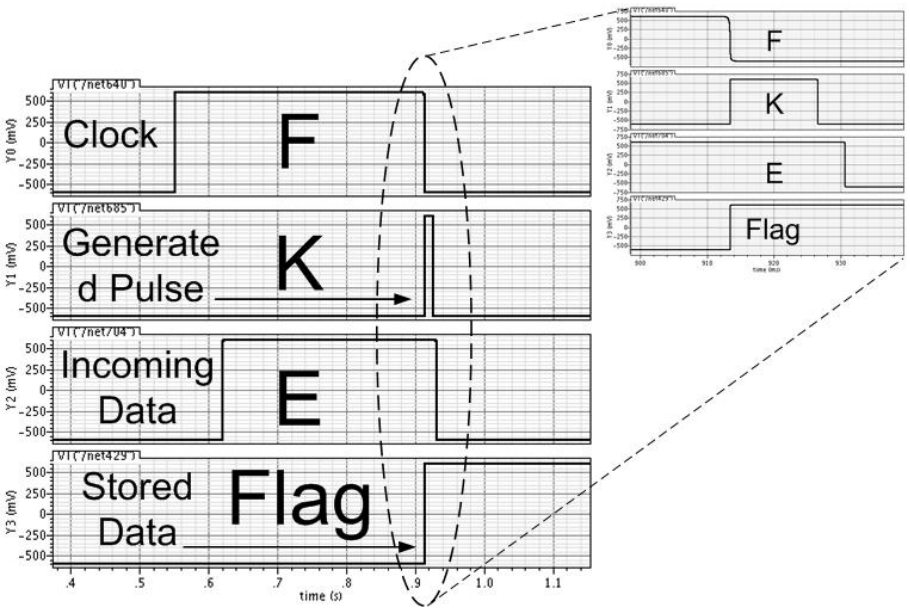

FIGURE 5.22: Example of simulated time diagram of the new model of negative edge triggered flip-flop.

5.6 Simulation Results

In order to validate the system for the detection of heart beat irregularities a large number of simulations, based on Cadence tools such as Spectre, have been performed using real electrocardiograms from the MIT-BIH database. Such ECGs belonged to different users and showed that the system can be adopted for the monitoring and detection of heart beat anomalies on different users. Therefore, real heart beat irregularities such as ventricular premature beats, ventricular tachycardia, atrial fibrillation and atrioventricular blocks have been used to validate the system and algorithm. Such heart beat pathologies were suggested by cardiologists from the Hospital of Rome as the most frequent and severe.

The first operation performed by the system, as shown in the block diagram in Fig. 5.15, is the elimination of isoelectric artifacts. Such operation is performed by the analogue ALU and by transistor M1 and C1 (see Fig. 5.16) as explained in section 5.5.1. Fig. 5.23 shows an experimental result where it is possible to observe the elimination of the isoelectric artifacts.

As previously explained, the ECG complex is always initiated in the order shown in Fig. 5.3: a P-wave followed by the QRS complex and a T-wave. Therefore, when this order is not maintained and the QRS complex appears in a more chaotic order, this creates the heart beat irregularity known as ventricular premature beat [136] which was previously described in subsection 5.2.1. Fig. 5.24(a) illustrates a trace of electrocardiogram with the presence of ventricular premature beats as indicated in the figure; whereas, Fig. 5.24(b) illustrates the final output of the system detecting the premature ventricular heart beats. Furthermore, it can be observed in Fig. 5.24(b) how the flag signal is set

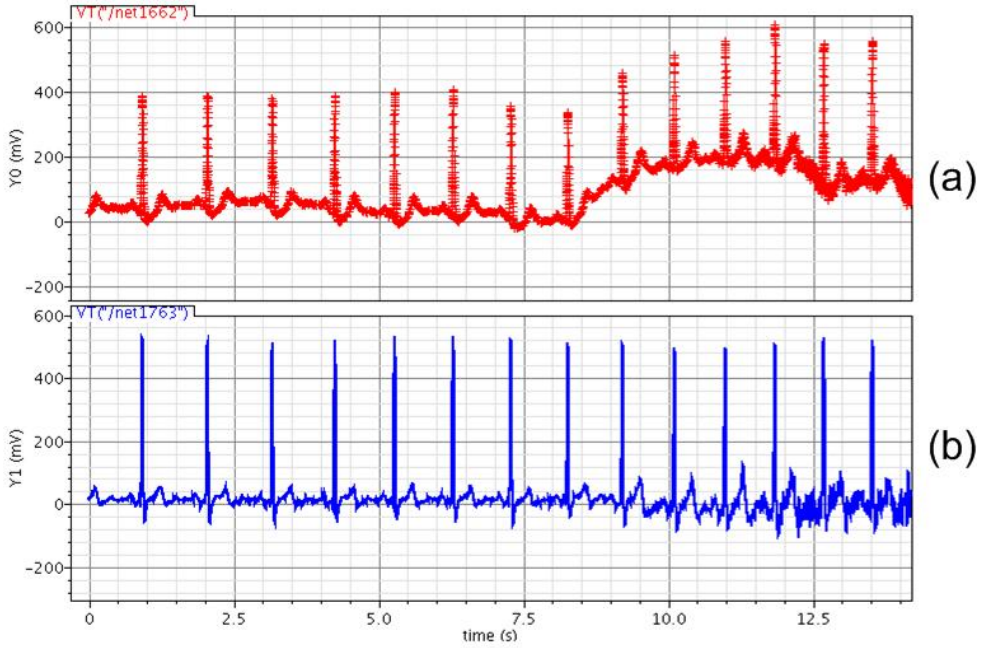

FIGURE 5.23: Removal of the isoelectric artifact. (a) Incoming ECG with isoelectric artifacts; (b) Same ECG after removing isoelectric artifacts.

back to zero when the heart beat re-starts beating normally.

As mentioned in subsection 5.2.2, ventricular tachycardia originates in one of the ventricles of the heart and is a very life threatening arrythmia which might lead to ventricular fibrillation and sudden death [136]. Fig. 5.25(a) illustrates an ECG trace with an occurring ventricular tachycardia while Fig. 5.25(b) shows the output of the signal processor detecting the hear beat irregularity.

The repetition of P-waves is also one of the most common cardiac arrhythmia as explained in subsection 5.2.3 [136]. Fig. 5.26(a) shows an example of atrial fibrillation as noted on the figure, while Fig. 5.26(b) illustrates the final output of the system detecting the atrial fibrillation and also the re-stabilization of the heart beat.
Additionally, from Fig. 5.26(a) and Fig. 5.26(b) it is possible to observe in more details how the detection of heart beat anomalies is achieved at the end of each ECG complex showing that each ECG complex is individually analysed.

Atrioventricular blocks can be classified as partial or complete interruptions of the signal transmission from the atria to the ventricles of the heart [136]. Fig. 5.27(a) shows the incoming ECG signal while Fig. 5.27(b) shows the detection of the atrioventricular block.

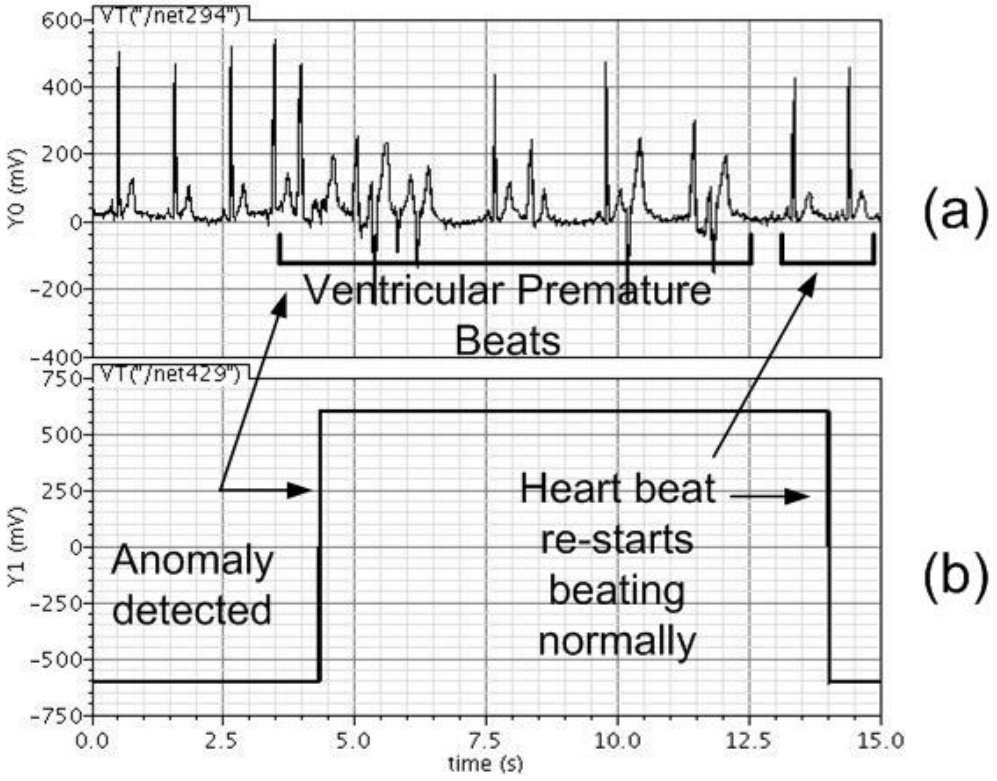

FIGURE 5.24: (a) incoming ECG signal showing ventricular premature beats; (b) detection of the ventricular premature beats by the system

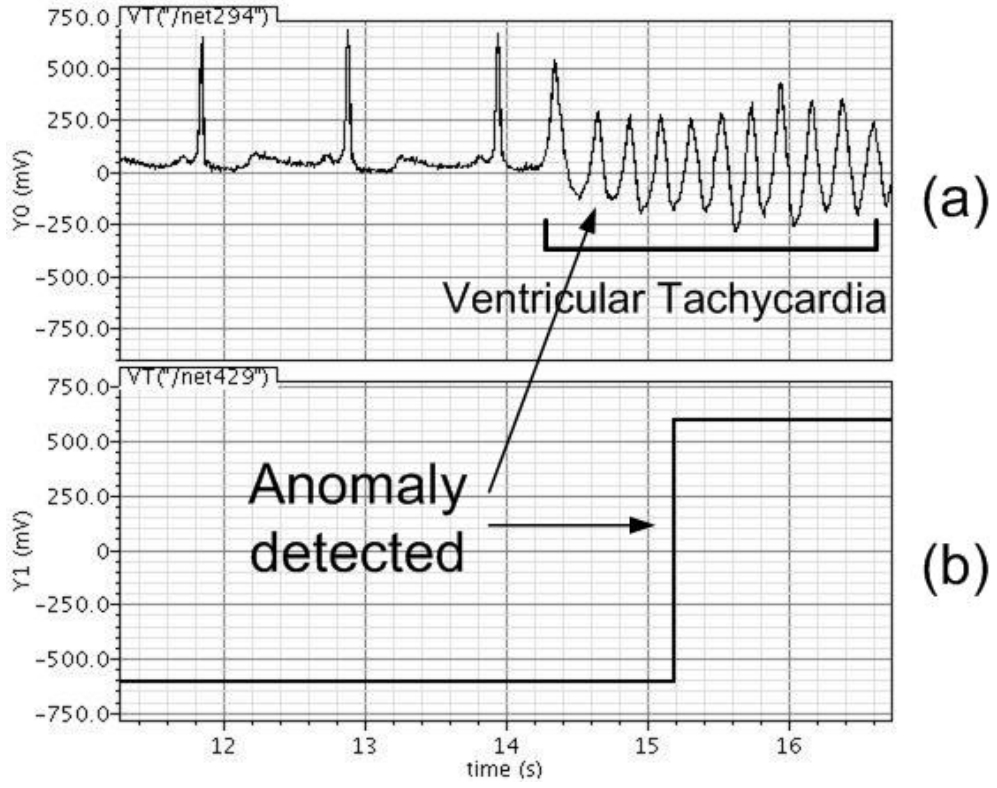

FIGURE 5.25: (a) incoming ECG signal showing a case of ventricular tachycardia; (b) detection of the ventricular tachycardia by the system.

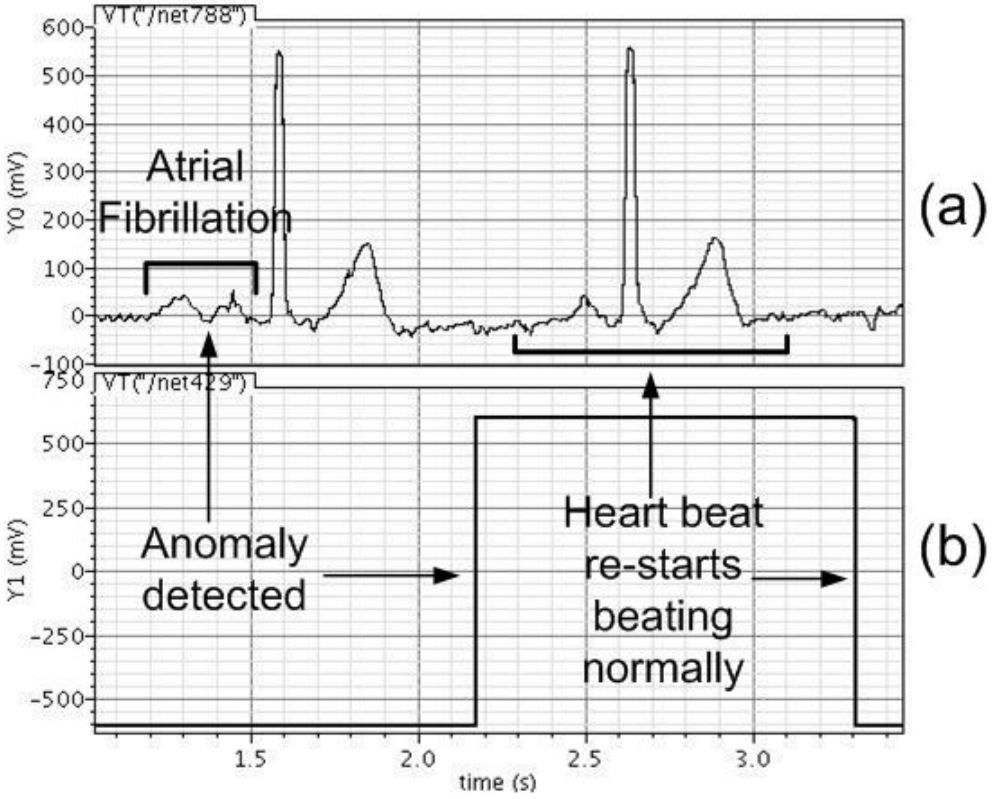

FIGURE 5.26: (a) incoming ECG signal showing a case of atrial fibrillation; (b) detection of the atrial fibrillation by the system.

5.7 Conclusion

In this chapter the physiology of the heart and its electrical characteristics, which are used by doctors (cardiologists) to determine whether the heart is functioning correctly, was studied. The most fundamental ECG anomalies such as ventricular premature beats, ventricular tachycardia, atrial fibrillation and atrioventricular blocks have been studied to analyze the existing heart monitoring devices and create a new methodology for the automatic detection of ECG anomalies with a non-invasive device. Consequently, such methodology has been tested on Matlab with over 90 ECGs with different irregularities. The results obtained showed the ability of the algorithm to differentiate between heart beat anomalies. Furthermore, such methodology has been implemented at circuit level and successfully tested with real ECG signals to verify that the system could automatically identify heart beat anomalies. The system was designed in the analogue domain on a 130nm CMOS Technology with capacitors in the range of a few pico Farad which allowed a dramatic reduction of hardware.

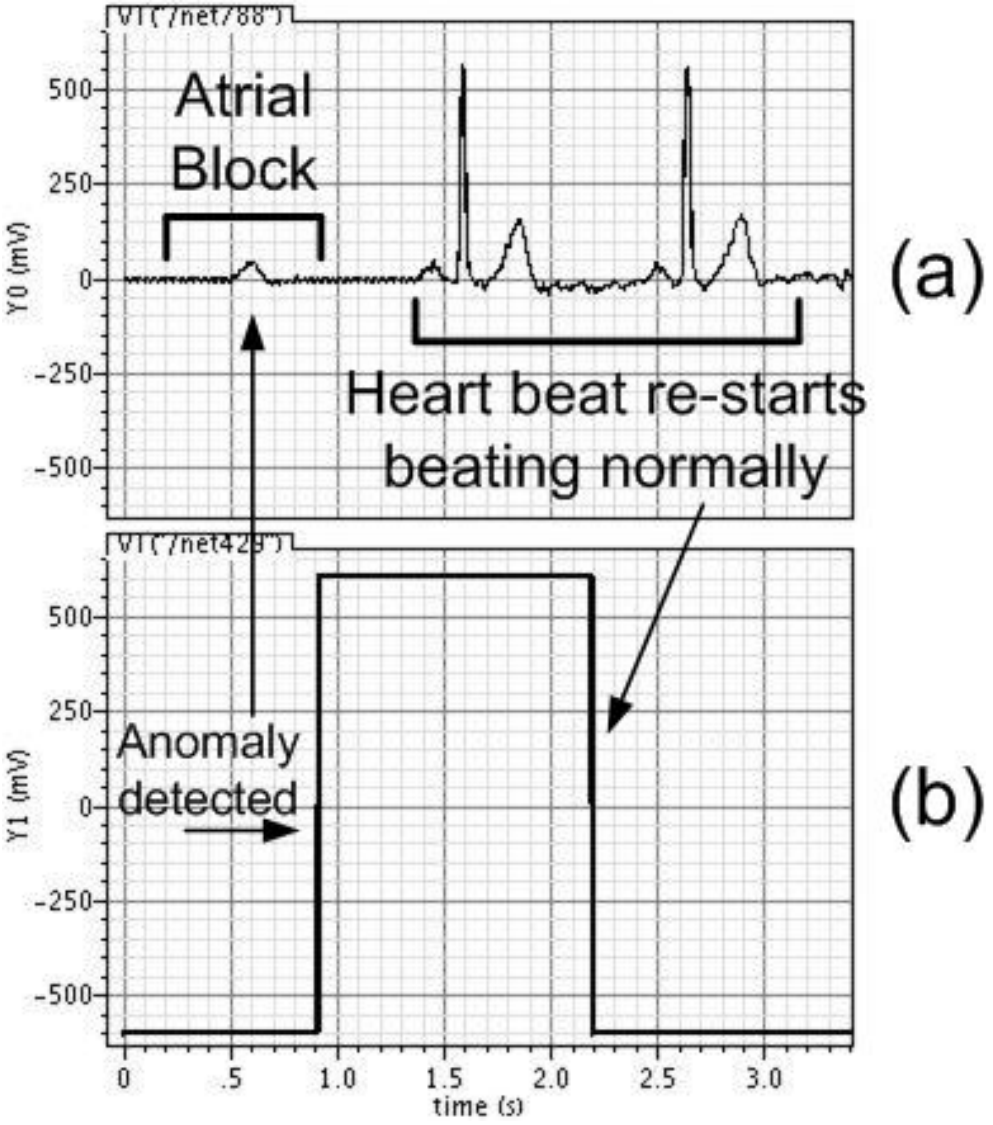

FIGURE 5.27: (a) incoming ECG signal showing a case of atrial block; (b) detection of the atrial block by the presented system.

Chapter 6

Hopf Oscillator with Dynamic Plasticity: New Approach to Signals Analysis

During the development of the works presented in the previous chapters, the significance of signal processing for the extraction of amplitude and frequency components was realised . Consequently, it became of interest to develop an alternative methodology which would present novel advantages for the signal processing of such biomedical signals as EMG and ECG signals as presented in the previous chapters.
Hence, this chapter presents a new methodology based on non-linear oscillators with dynamic plasticity for signal analysis. The concept of dynamic plasticity allows a system to vary its properties and adapt its frequency and amplitude components according to the incoming input. Consequently, it is possible to use this behaviour for the extraction of such parameters as frequency and amplitude components of incoming inputs. Furthermore, the choice of using oscillators is based on the fact that most of the signals in nature present oscillatory behaviours.
This chapter introduces the most relevant non-linear oscillators and describes the modifications required to incorporate dynamic plasticity and implement these models into a compact analogue system.
A large number of experiments with single and mixed signals have been performed to prove the functionality and advantages that this systems can provide.

6.1 Introduction to Non-Linear Oscillators

The theory of nonlinear oscillators has been used for decades to model diverse natural phenomena such as neuronal signaling [139], central pattern generation (CPG) [140,141],

associative memory [142,143] and beat perception [144,145], to engineering applications such as universal machines [146, 147], image processing [148], logic computation, [149] and robotics [150] [151]. This wide range of applications and capability has made non-linear oscillatory networks a likely ingredient in future system design in electronics [152]. Unfortunately because of the mathematical complexity inherent to such systems, hardware realization is a serious challenge, preventing their application in real-life VLSI systems. Additionally nonlinear oscillators find limited application in the field of signal processing, mainly because of their lack of plasticity (ability to adapt to external signals), as they have a fixed intrinsic frequency and cannot dynamically adapt their parameters to external signals.
Typically there are four main mathematical models of non-linear oscillators which have been used for modeling and analysis of physical and biological systems: the Van Der Pol oscillator, the Rayleigh oscillator, the Fitzhugh-Nagumo oscillator and the Hopf oscillator.

6.1.1 Fundamentals of the Van Der Pol Oscillator

The Van Der Pol oscillator was originally proposed by the Dutch electrical engineer and physicist Balthasar Van Der Pol when he was working at Philips and while he was designing stable oscillators with the use of vacuum tubes in 1926. Van Der Pol noticed that when his models of oscillators were driven towards the limit cycles these became entrained (i.e. the driving current of the external signal would pull the current of his oscillator along with it). Such behavioural model is then being used in certain phenomena in both physics and biology. The mathematical model of the Van Der Pol oscillator is described in Eq. 6.1 and can be considered depicting a self sustaining oscillation.

$$\ddot{x} - \mu(1 - x^2)\dot{x} + \omega^2 x = 0 \tag{6.1}$$

Where x represents the position coordinate, μ is the scalar parameter indicating the non-linearity and ω is the angular frequency of the oscillator ($2\pi f$). Fig. 6.1 shows the behaviour of the Van Der Pol model as the amplitude parameter μ increases. It is possible to notice how the limit cycle starts as a circle for small values of μ and changes its shape with the increase of μ. Such behaviour has often been utilized for CPGs since the variation of the internal parameters (e.g. μ and ω) can vary the shape of the oscillation waveform [153].

6.1.2 Fundamentals of the Rayleigh Oscillator

The Rayleigh oscillator also shares the same mathematical properties of the Van Der Pol oscillator, described in Eq. 6.1, which can be used for CPGs as in [154]. The main

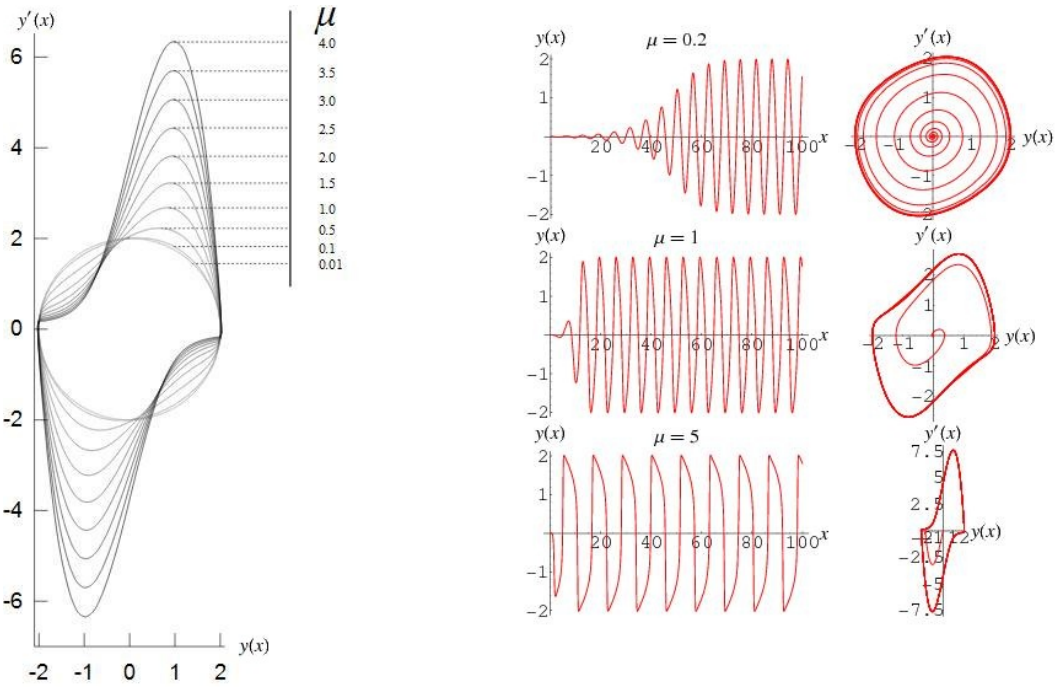

FIGURE 6.1: Evolution of the limit cycle of the Van Der Pol Oscillator.

difference between the Van Der Pol and and Rayleigh oscillator is given by the fact that the Van Der Pol model increases its frequency with ω while the Rayleigh model increases its amplitude. Fig. 6.2 shows an example of phase plot of the Van Der Pol and the Rayleigh oscillator which has been used for CPGs applications.

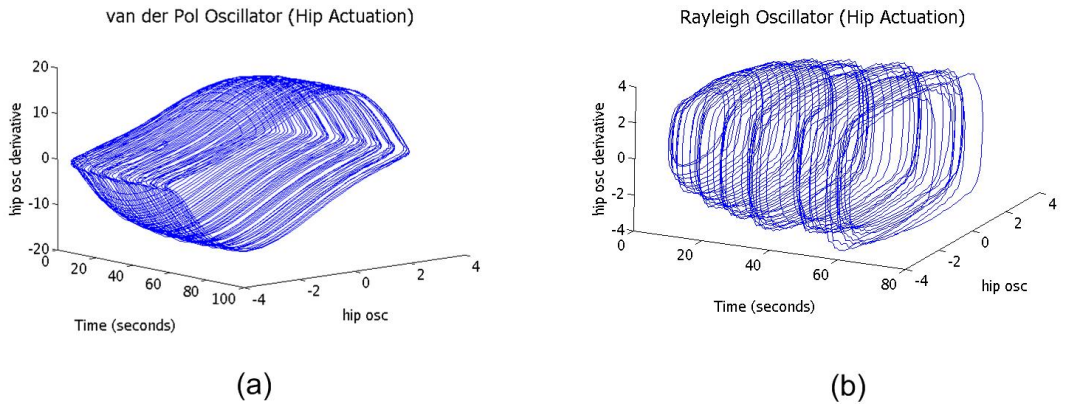

FIGURE 6.2: Phase plot of the (a) Van Der Pol and (b) Rayleigh oscillator [154].

6.1.3 Fundamentals of the Fitzhugh-Nagumo Oscillator

Fitzhugh-Nagumo oscillators are mainly used to model neural networks and partially CPGs [153]. Such preference is given by the parameters within the Fitzhugh-Nagumo model (shown in Eq. 6.2) which allow a more suitable variation of the parameters for

frequency, amplitude, and threshold values for the firing potentials of the neurons [155].

$$\frac{d\nu}{dt} = a(-\nu(\nu-1)(\nu-b)) - \omega + I \qquad (6.2)$$
$$\frac{d\omega}{dt} = \nu - c\omega$$

In Eq. 6.2 ν is the membrane potential, ω is the recovery variable, a and c are scaling parameters, I is the stimulus current, and b is a threshold parameter [153]. Additionally, the mathematical model described in Eq. 6.3 represents the Fitzhugh-Nagumo oscillator used to adapt the frequency of the oscillator to external input signals in case of an adaptive CPG [156]; while, Fig. 6.3 shows an example of frequency adaptation mechanism to an external stimulus.

$$\begin{aligned} \dot{x} &= x(x-a)(1-x) - y + KF \\ \dot{y} &= \omega(x - by) \\ \dot{\omega} &= -KF\frac{y}{\sqrt{x^2+y^2}} \end{aligned} \qquad (6.3)$$

In Eq. 6.3 the parameters a and b define the amplitude of the oscillator, while K and F represent the gain and the external stimulus respectively.

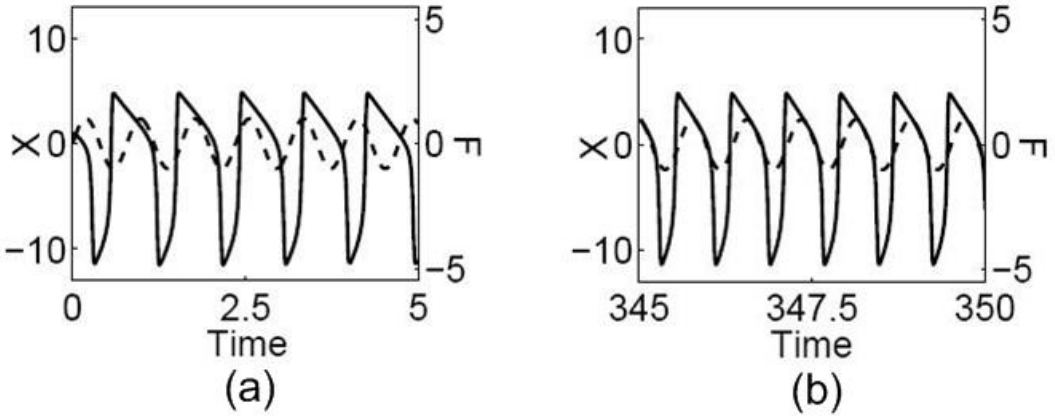

FIGURE 6.3: Oscillatory response of the Fitzhugh-Nagumo adaptive oscillator to an external stimulus (dashed line); (a) the oscillator (solid line) has not adapted/synchronised to the external stimulus (dashed line); (b) the oscillator has adapted/synchronised to the external stimulus [156].

6.1.4 Fundamentals of the Hopf Oscillator

The dynamics of the Hopf oscillator can be described by the following ordinary differential equations [157]:

$$\begin{aligned} \dot{x} &= (\mu^2 - (x^2+y^2))x + \omega y \\ \dot{y} &= (\mu^2 - (x^2+y^2))y - \omega x \end{aligned} \qquad (6.4)$$

where $\mu^2 > 0$ and determines the amplitude of the oscillator [158], x and y are the states of the oscillator, and ω is the angular frequency ($2\pi f$) [158].
The main advantage of the Hopf oscillator is given by the fact that, unlike the Van Der Pol and Rayleigh oscillators, the parameters which control the frequency (ω) and the amplitude (μ) do not depend on each other.

6.2 Choice of Non-Linear Oscillator

After considering and evaluating different topologies and mathematical characteristics given by the Van Der Pol oscillator, the Rayleigh oscillator, the Fitzhugh-Nagumo oscillator and the Hopf oscillator, it appeared that the Hopf oscillator is the most suitable for the frequency and amplitude analysis of an external input signal. This is due to the Hopf oscillator mathematical model and internal parameter characteristics defined by ω and μ as these do not depend on each other. Indeed, the frequency of the Hopf oscillator does not vary with amplitude as in the Van Der Pol model; and the amplitude of the oscillator does not change with frequency (ω) as in the Rayleigh model [153]; while, the Fitzhugh-Nagumo model with its frequency, amplitude and threshold parameters, appears to be more suitable for neural network analysis as also described in Table 6.1.

The only constraint given by the Hopf oscillator is that such oscillator does not pro-

TABLE 6.1: Comparison of non-linear oscillators main characteristics.

	Van Der Pol	**Rayleigh**	**Fitzhugh-Nagumo**	**Hopf**
Amplitude and Frequency Dependency	yes	yes	no	no
Threshold Parameters	no	no	yes	no

vide an inherent dynamic plasticity and therefore can not be used for signal processing. Hence, new modified models of the Hopf oscillator have to be developed for signal processing applications.

6.3 Related Works

Recently, [151] and [159], Buchli et al. introduced a new learning rule in the Hopf oscillator [157], according to which the intrinsic frequency of the system evolves towards the frequency of an external perturbation and thus incorporates dynamic plasticity in the oscillator itself. Therefore, in the case of an external additive perturbation $I(t)$ the system equation of a Hopf oscillator can be written as shown in Eq. 6.5 [159].

$$\begin{aligned}\dot{x} &= (\mu^2 - (x^2 + y^2))x + \omega y + KI(t) \\ \dot{y} &= (\mu^2 - (x^2 + x^2))y - \omega x \\ \dot{\omega} &= KI(t)\frac{y}{\sqrt{x^2 + y^2}}\end{aligned} \tag{6.5}$$

where $K > 0$ is a coupling constant.

Fig. 6.4 illustrates an example of frequency adaptation of the Hopf oscillator to an external perturbation.

However, a straight forward hardware implementation of Eq. 6.5 is extremely difficult

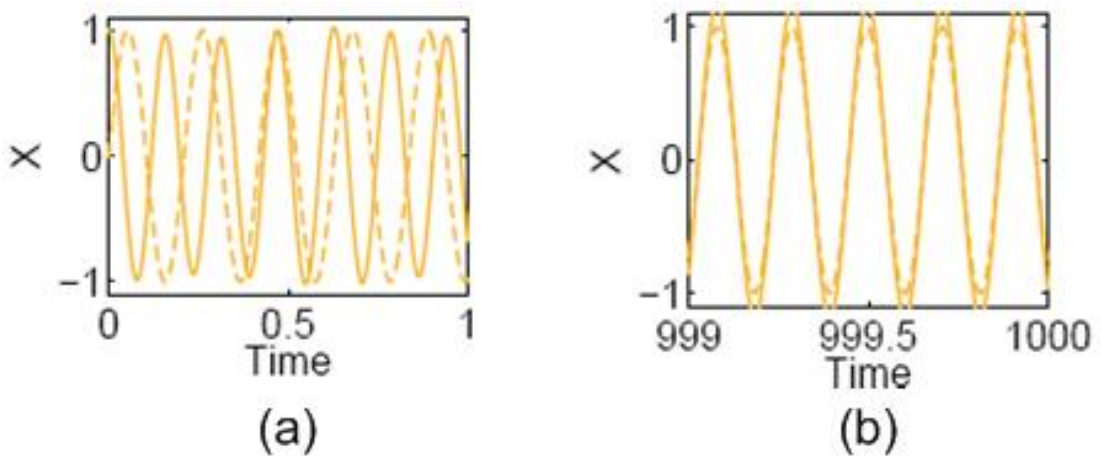

FIGURE 6.4: (a) The Hopf oscillator has not adapted to the external perturbation (dashed line); (b) the Hopf oscillator has adapted to the external perturbation [160].

because of the following reasons:

1. The learning time utilizes terms like $\frac{y}{\sqrt{x^2+y^2}}$ and $x^2 + y^2$ which would require a complex and large computational power from a hardware level point of view.

2. In an analog circuit domain, the frequency ω should be realized as a capacitance voltage. In practice, this linear dependence of ω on a capacitor voltage restricts its range of adaptation to only a few volts (or equivalently to a few Hertz, therefore a small oscillation-frequency basin).

3. The frequency convergence/learning time of this oscillator is very high (several thousand seconds in some cases). In a practical application this delay is not acceptable.

4. Although the oscillator proposed in [159] can learn the frequency of the external signal, the extraction of its amplitude requires a large number of coupled oscillators (1000) which is very costly in terms of real hardware particularly for a signal with a wide frequency spectrum.

These practical problems have inspired the development of a novel and simple analogue VLSI implementation of the Hopf oscillator with dynamic plasticity while staying within the framework proposed in [159]. In the following sections a new mathematical model has been formulated showing the changes and improvements that have been carried out to [159] in terms of learning time (when adapting to the external signals) and also for a more suitable VLSI implementation. Additionally, a generic circuit implementation has been designed and tested to validate the capabilities to extract frequency and also amplitude of external signals. This studies have also been reported in the publication [161].

6.3.1 Dynamics of the Hopf Oscillator

As previously mentioned in section 6.1.4, the dynamics of the Hopf oscillator can be described by Eq. 6.4; and results in stable periodic solutions, known as limit cycles [157]. Its limit cycles behaviour can be quantified by first applying the transformation shown in Eq. 6.6 and then using it to Eq. 6.4.

$$\begin{aligned} x &= \mu sin(\omega t + \theta_0) \\ y &= \mu cos(\omega t + \theta_0) \end{aligned} \tag{6.6}$$

Where θ_0 is determined by the initial conditions. This solution represents a circle of the form $x^2+y^2 = \mu^2$, around the origin of the state space as shown in Fig. 6.5. In the Hopf oscillator the oscillation radius is fixed and independent of the oscillation frequency. Under the new learning rule proposed by [160] (see Eq. 6.5) when perturbed by an external signal $I(t)$, the perpendicular component of the perturbation force is damped out in the long term leaving the tangential component of the perturbation (typically termed as the teaching force) to tune the limit cycle frequency to one of its frequency components [160]. Mathematically this teaching force can be represented by the term $sin(\phi)\frac{y}{\sqrt{x^2+y^2}}$ in the state space at the point $(x(t), y(t))$ as shown in Fig. 6.5.

Under this teaching force the oscillator will have a tendency to accelerate or decelerate, in the state space, which on average results in an oscillation at a frequency of the $I(t)$ (in case of a monotone signal). This behaviour, in frequency domain, is manifested as a ripple around the converged frequency. If $I(t)$ comprises different frequencies with different amplitudes, depending on the initial values of the state variables, the oscillator tunes itself to the frequency component having the highest amplitude.

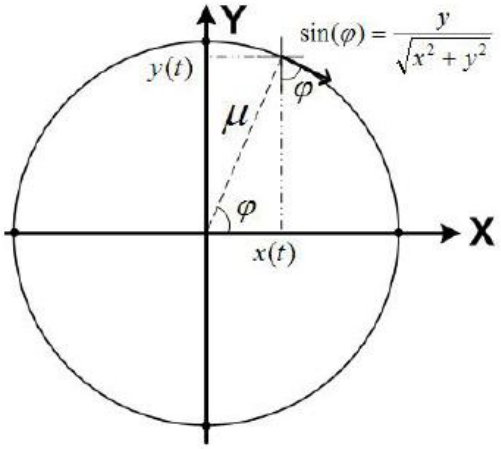

FIGURE 6.5: State space representation of the oscillation characteristics of the oscillator [159].

6.4 A New Model of Hopf Oscillator with dynamic plasticity

6.4.1 Mathematical Modification of the Hopf Oscillator for Low Complexity Implementation

The parameters described in Eq. 6.4 are responsible for generating an oscillatory behavior at a determined frequency (ω), and limiting the amplitude to the defined parameter μ^2. Furthermore, it is possible to note that the frequency behavior of such an oscillatory system depends only on the sign of $\dot{x}$ and $\dot{y}$ and the relative values of x and y to μ. From this understanding of the system behavior the first parts of both equations in Eq. 6.4 can be modified as in Eq. 6.7:

$$\begin{aligned} \dot{x} &= (\mu - (|x| + |y|))sgn(x) + \omega y \\ \dot{y} &= (\mu - (|x| + |y|))sgn(y) - \omega x \end{aligned} \tag{6.7}$$

where $|x| + |y|$ is the new measure of the oscillation amplitude and $sgn(\cdot)$ is the sign value of x and y. The state space representation of Eq. 6.7 is shown in Fig. 6.6. It can be seen that in this representation the circular function in Eq. 6.4 and Fig. 6.5 is replaced by a square shaped function $|x| + |y| = \mu$ which is easily realizable in the analogue domain.

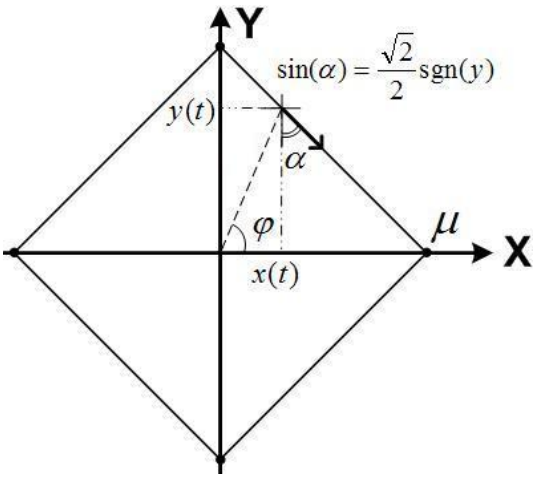

FIGURE 6.6: State space representation of the proposed oscillator.

6.4.2 Stability and Limit Cycle Behavior of The Modified Oscillator

The stability of the proposed modified Hopf oscillator system can be determined using the Lyapunov second method with the energy function as in Eq. 6.8 [162]:

$$V(x, y) = \frac{1}{2}(x^2 + y^2) \tag{6.8}$$

where by differentiating V and replacing x and y from Eq. 6.7, we get:

$$\dot{V} = x\dot{x} + y\dot{y} = (\mu - (|x| + |y|))(|x| + |y|) \tag{6.9}$$

resulting in:

$$\begin{cases} \dot{V} > 0, & |x| + |y| < \mu \\ \dot{V} = 0, & |x| + |y| = \mu \\ \dot{V} < 0, & |x| + |y| > \mu \end{cases} \tag{6.10}$$

which means that the system has a stable limit cycle for:

$$|x| + |y| = \mu \tag{6.11}$$

The inequalities in Eq. 6.10 apply to the applications in which initial values are always bounded and therefore, the system is guided to a limit cycle state.
Consequently, to derive the oscillation behavior of the system, by transforming Eq. 6.7 to the polar coordinates ($x = rcos(\phi)$ and $y = rsin(\phi)$) we get:

$$\begin{aligned} \dot{r} &= (\mu - r(|cos\phi + |sin\phi|))(sin\phi + cos\phi) \\ \dot{\phi} &= \omega + \frac{1}{r}(\mu - r(|sin\phi| + |cos\phi|) \times (sgn(sin\phi)cos\phi - sgn(cos\phi)sin\phi)) \end{aligned} \tag{6.12}$$

Applying the steady state criterion with: $\dot{r} = 0$:

$$\begin{cases} r = \frac{\mu}{|sin\phi|+|cos\phi|}, \\ \dot{\phi} = \omega, \end{cases} \tag{6.13}$$

Thus the steady state oscillation can be described as:

$$x_{ss}(t) = \frac{\mu sin(\omega t)}{|sin(\omega t)| + |cos(\omega t)|} \tag{6.14}$$

assuming $\phi(0) = 0$. The nature of the oscillation described in Eq. 6.14 is depicted in Fig. 6.7 comparing with $\mu sin(\omega t)$ (as in the original Hopf oscillator).

From Fig. 6.7 it is important to notice that the shape of the oscillation waveform resem-

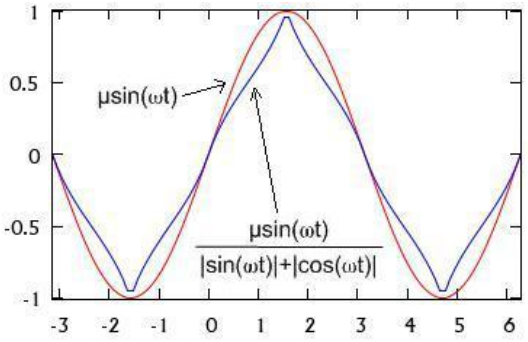

FIGURE 6.7: Output signal of the modified oscillator comparing with monotone sinusoidal oscillation.

bles a triangular wave rather than a pure sinusoid. However the frequency characteristic and amplitude value of the waveform are exactly similar to that of the reference sinusoid which is in conformation of the state space representation of the proposed oscillator as shown in Fig. 6.6

6.4.3 New Adaptive Frequency Hopf Oscillator

The most important implication of the modification proposed above is given by the change in the frequency adaptation equation in Eq. 6.5. From a geometrical point of view, as shown in Fig. 6.6, in order to create the limit cycle behavior of the system, in the proposed model, the circular function $x^2 + y^2 = \mu^2$ is replaced with the square shaped function $|x| + |y| = \mu$. Thus referring to Fig. 6.6, noting that the gradient of each side of the square is 45°, under an additive perturbation the tangential component of the teaching force can simply be defined as $sin(\alpha) = \frac{\sqrt{2}}{2} \cdot sgn(y)$.

Therefore the modifications carried out to Eq. 6.5 can be described below in Eq. 6.15:

$$\begin{aligned} \dot{x} &= (\mu - (|x| + |y|))sgn(x) + \omega y + KI(t) \\ \dot{y} &= (\mu - (|x| + |y|))sgn(y) - \omega x \\ \dot{\omega} &= KI(t) \cdot sgn(y) \end{aligned} \tag{6.15}$$

Knowing that $sgn(y) = \frac{y}{|y|}$ for $y \neq 0$ and $|y| = \sqrt{y^2}$, the adaptation equation can be rewritten as:

$$\dot{\omega} = KI(t) \cdot sgn(y) = KI(t) \cdot \frac{y}{\sqrt{y^2}} \tag{6.16}$$

Comparing with the adaptation equation in Eq. 6.5, it is possible to observe:

$$sgn(y) = \frac{y}{\sqrt{y^2}} \geq \frac{y}{\sqrt{x^2 + y^2}} \tag{6.17}$$

Using this basic inequality to compare the third equations in Eq. 6.15 and 6.5, which are responsible for the frequency adaptation mechanism of the oscillators; it is evident that the rate of change of ω in the proposed oscillator is larger than the rate of change of ω in the original Hopf oscillator. This results in a faster learning dynamics in the modified oscillator.

6.4.4 Computing the Relative Amplitude of the Frequency Component

Considering the Fourier expansion of the input perturbation $I(t) = \sum_{i=0}^{N}(a_i sin\omega_i t + b_i cos\omega_i t) = \sum_{i=0}^{N} A_i sin(\omega_i t + \theta_i)$, analyzing frequency spectrum of the input also requires information about the magnitude of each of the frequency components (A_i). Recalling the basic mathematical methods for computing the Fourier series, theoretically, the amplitude A_i of the frequency component ω_i can be calculated as:

$$A_i = \frac{2}{T} \int_0^T sin(\frac{2\pi i}{T}\tau) I(\tau) d\tau \tag{6.18}$$

where T is the period of the first harmonic [163, 164].
After the oscillator learning time, by which it converges to a single frequency of the input perturbation ($lim_{t \to \infty} x(t) \to \mu sin(\omega_i t)$), using the above equation, it is possible to conclude that:

$$A_i \propto \frac{1}{T} \int_0^T x(\tau) I(\tau) d\tau \tag{6.19}$$

where the right hand side of the equation represents averaging operation over time T. This proportionality means that after the oscillator's convergence to a frequency component of $I(t)$ (ω_i for instance) the amplitude will be proportional to the time-average of $x(\tau) \cdot I(\tau)$. In terms of system dynamics, this relationship can be represented as:

$$\dot{A} = K_A I(t) \cdot x \tag{6.20}$$

This equation results in a linear relationship between A_i and the integration time, creating an ever-increasing signal in the circuit. However, in practise it is possible to extract the slope of the integration result within a limited time (i.e. after the oscillator's convergence) and stop the integration thereafter. The slope thus computed represents the amplitude (relative) of the frequency component at which the oscillator has converged.

6.4.5 The Complete Oscillator and System Level Simulation

VHDL-AMS [165] and Mentor Graphics Advance MS tools were used to investigate the functional behaviour of the proposed oscillator. Concurrently, the oscillator proposed in [159] was also implemented and compared with the presented model.
Three issues were investigated, the rate of frequency convergence of the proposed oscillator, effect of the gain factor K on the frequency convergence rate and the tuning property of an array of oscillators having different intrinsic frequencies to their nearby frequencies.

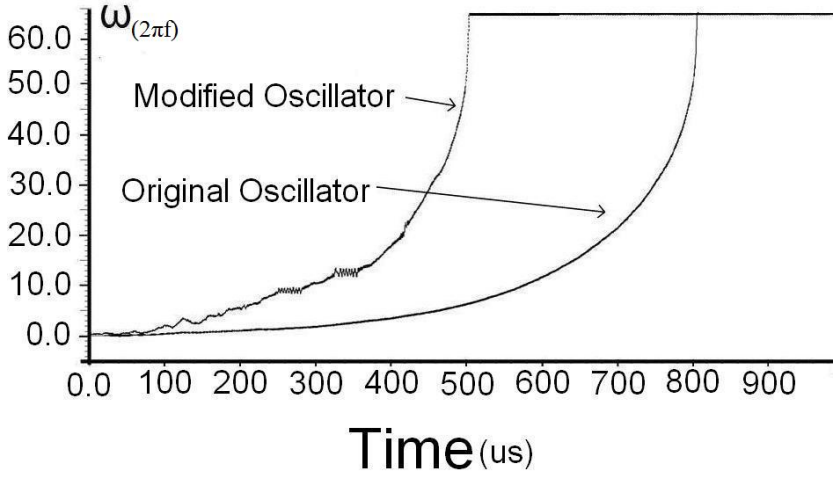

FIGURE 6.8: Frequency convergence comparison between the oscillator in [159] and the model shown in equations 6.15.

Fig. 6.8 shows the convergence characteristic of the proposed oscillator along with the oscillator proposed in [159] for a single sinusoid with 10 Hz frequency (f=10, which is represented by the value $62.8 = 2\pi f = 2\pi 10$ in Fig. 6.8) when the gain parameter K is set to a value of 10.
It can be clearly seen that the proposed oscillator converges to the desired frequency faster than that proposed in [159].
Fig. 6.9 shows the frequency convergence characteristics of the proposed oscillator for different values of K. It is evident that with increasing values of K the oscillator converges to the desired frequency at a faster rate.
Fig. 6.10 shows the oscillator response to different input frequencies, while Fig. 6.11 illustrates the frequency adaptation behavior of the oscillator under a non-stationary

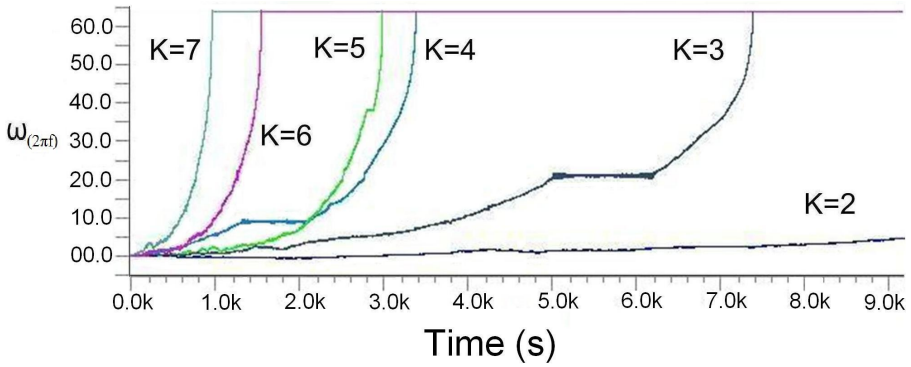

FIGURE 6.9: Frequency convergence characteristics for different values of K (f=20π, K=2-7).

external perturbation. From Fig. 6.11 it is possible to observe how the oscillator adapts to different frequencies depending on the input which varies in time. This characteristic can be employed to perform a time-frequency analysis of a non-stationary input signal by using an array of oscillators operating at different time zones (equivalent to the Wavelet transform).

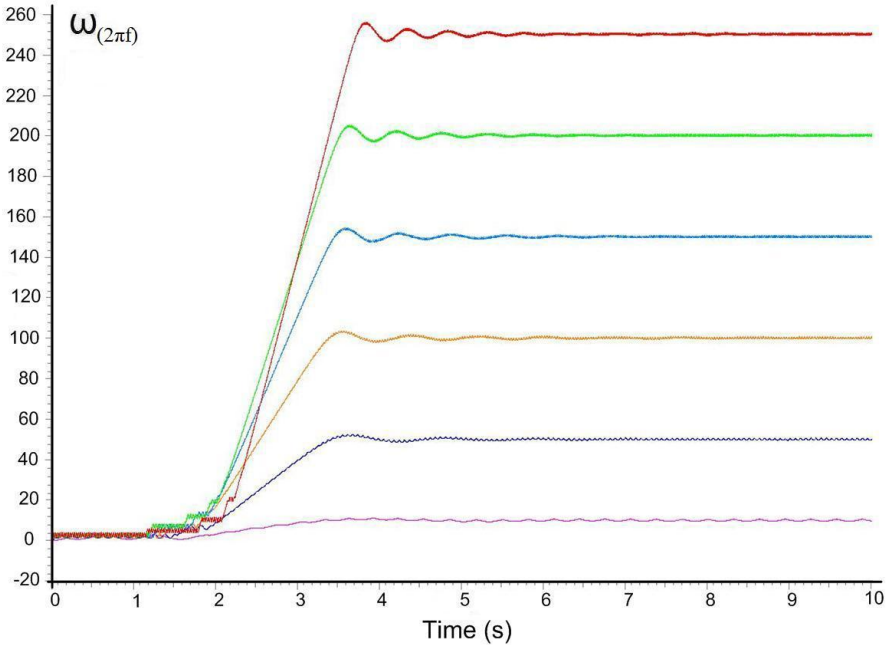

FIGURE 6.10: Frequency convergence characteristics for different input frequencies.

To demonstrate the behavior of the proposed oscillator in separating different frequency components present in a particular signal, an input signal composed of three frequencies (50, 30 and 10 Hz) and different amplitudes, has been used. Identical oscillators have been employed with different initial state values of $\dot{\omega}$. The result is shown in Fig. 6.12. In this case, each of these oscillators converged to its nearest frequency value and kept

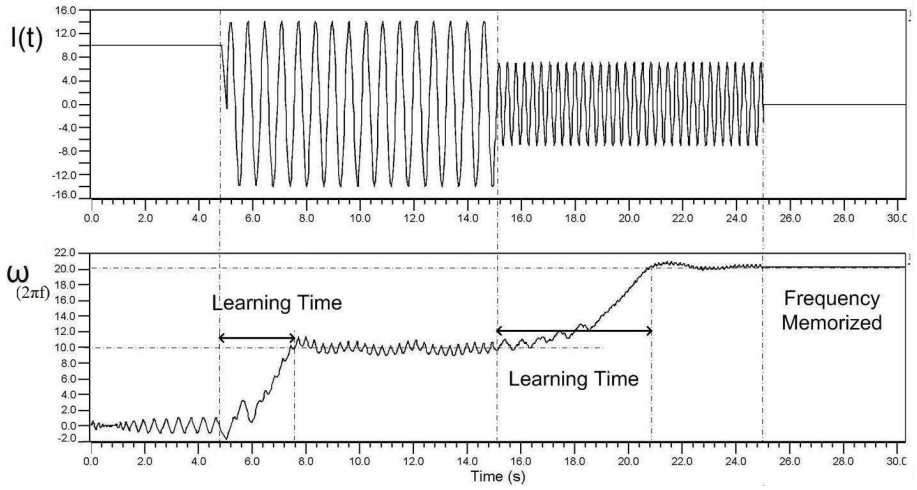

FIGURE 6.11: Oscillator response to a non-stationary input signal.

oscillating at that frequency when the input signal was withdrawn.

The frequency adaptation characteristic of the proposed adaptive oscillator is further

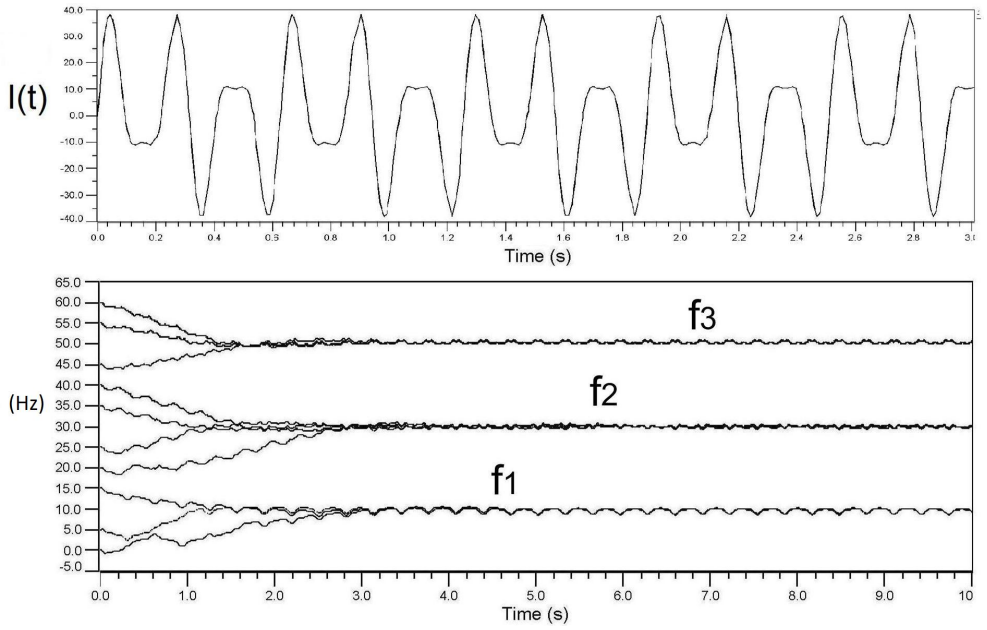

FIGURE 6.12: An array of similar oscillators with different initial values. Each oscillator converges to a frequency components of the $I(t)$ depending on its initial ω, $I(t) = 12sin(50t) + 27sin(30t) + 5sin(10t)$.

studied using a real-life EMG signal captured from a human subject. The result is shown in Fig. 6.13 where the captured EMG signal is shown at the upper left side of Fig. 6.13. The frequency content of the EMG signal is analyzed by performing 256-point FFT in Matlab as shown on the upper right side of Fig. 6.13. It is evident from the Fourier spectrum that the dominant frequency component present in this case is approximately 40 Hz. In this simulation only one oscillator was employed and thereby expect it to get tuned with this dominant frequency component only. The frequency adaptation characteristic of the proposed oscillator is shown in the lower part of Fig. 6.13. It is

clearly evident that the behavior of the oscillator is exactly as expected.

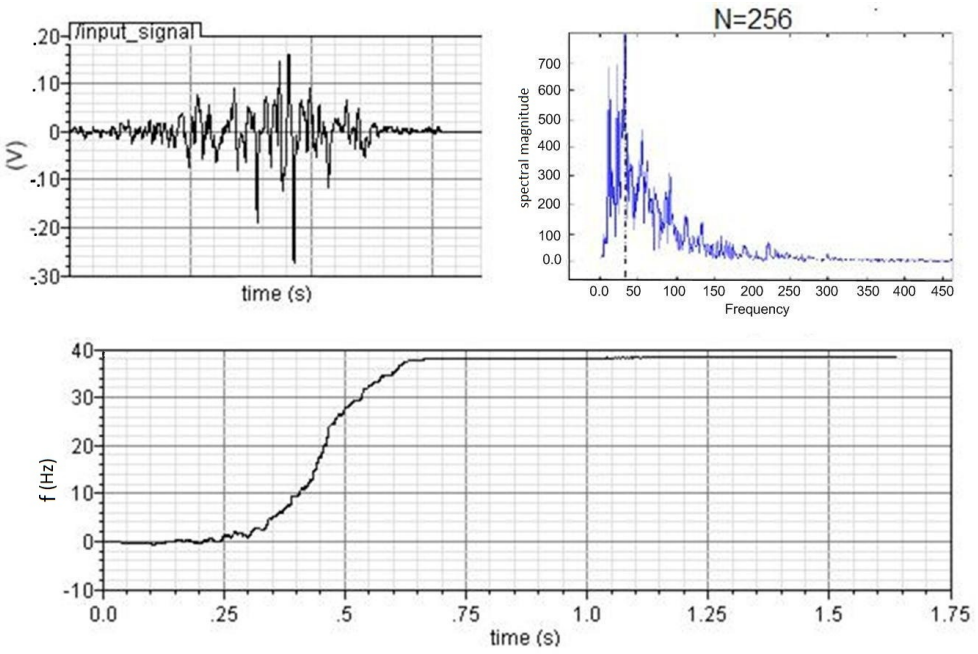

FIGURE 6.13: Oscillator response to an EMG signal.

As explained in section 6.4.4, the amplitude A_i of an external input signal can be extracted after the oscillator has adapted to the frequency of the external perturbation; consequently Fig. 6.14 shows the simulation results of different monotone signals with the same frequency but with different amplitudes.

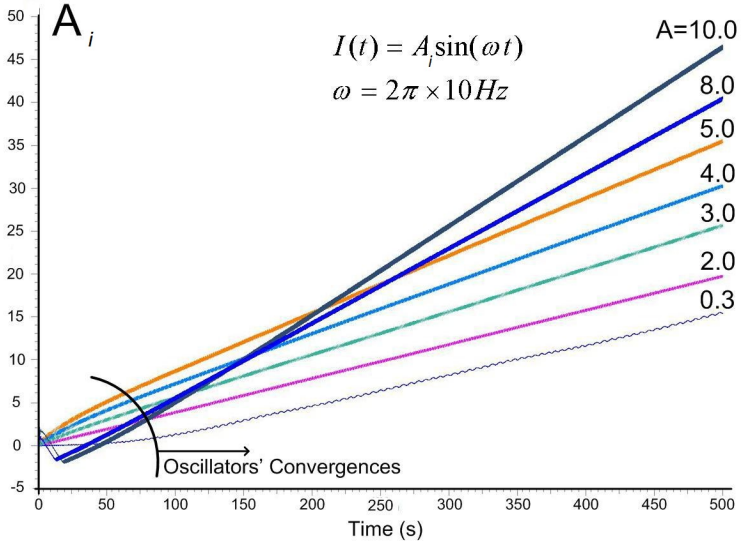

FIGURE 6.14: Slopes for different amplitude inputs after frequency convergence of the oscillator.

It is evident that signals having different amplitudes result in distinctly different slopes which as shown in Eq. 6.19 are proportional to the actual amplitude of the frequency components the oscillator has converged to. Therefore, these slopes can be used as a measure of amplitudes of different frequency components.

6.5 Circuit Realization

The circuit realization of a non-linear oscillator requires the consideration of other physical parameters which are given by physical limitations: e.g. the parameter μ, which defines the amplitude of oscillation in Eq. 6.15 and the parameters x and y which define the state variables, can have a maximum amplitude which is dependent of the power supply of the circuit. Hence, the parameters which define the oscillator of Eq. 6.15 will be changed as shown in Table 6.2 to distinguish the theoretical model from the analogue VLSI implementation.

Mathematical Notation		**Analogue VLSI Notation**		
μ	$\Leftrightarrow$	μ	$\Leftrightarrow$	power supply
x	$\Leftrightarrow$	V_x	$\Leftrightarrow$	state variable x
y	$\Leftrightarrow$	V_y	$\Leftrightarrow$	state variable y
ω	$\Leftrightarrow$	V_ω	$\Leftrightarrow$	voltage controlling the intrinsic frequency

TABLE 6.2: Mathematical and analogue VLSI terms notations.

Consequently, the first two equations of Eq. 6.15 can be rewritten as follow:

$$\begin{aligned} \dot{V_x} &= \overbrace{(\mu - (|V_x| + |V_y|))sgn(V_x) + V_\omega V_y}^{\text{Conventional Oscillator}} + KI(t) \\ \dot{V_y} &= \underbrace{(\mu - (|V_x| + |V_y|))sgn(V_y) - V_\omega V_x}_{\text{Conventional Oscillator}} \end{aligned} \tag{6.21}$$

where the first part of the equation can be considered as a conventional oscillator with an intrinsic frequency ω_0. Depending on the circuit design parameters, the range of ω_0 varies in the range $\omega_{min} \leq \omega_0 \leq \omega_{max}$ and thus creating a frequency basin within which the oscillator will perform frequency and amplitude analysis. A simple implementation of such an oscillator can be given by a ring oscillator with a controllable loop delay [166] [161] as shown in Fig. 6.15.

It is possible to observe that the frequency of the oscillator is tuned by the transmission gates between each inverter (which acts as controllable time constants) and the variable V_ω which defines the voltage required to tune the transmission gates according to the intrinsic frequency ω_0.

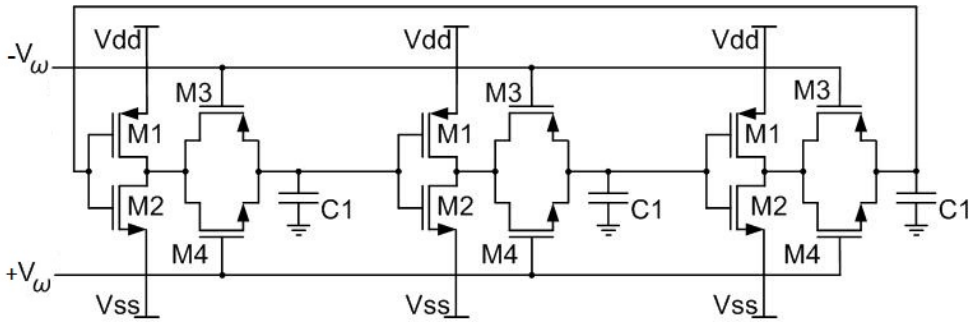

FIGURE 6.15: Ring oscillator with controllable loop delay.

The transistor sizes and the capacitors $C1$ can be modified according to the desired frequency range considering that the frequency basin of this ring oscillator ($\omega_{min} \leq \omega_0 \leq \omega_{max}$) is mainly given by the time constant produced by the transmission gates, which act as linear variable resistors, and the capacitors $C1$ which is charged by the current flowing through the transmission gates.
Furthermore, the frequency (f_{osc}) of the oscillator can be described in Eq. 6.22:

$$f_{osc} = \frac{1}{2 \cdot N \cdot \tau} \tag{6.22}$$

where N represents the odd number of inverter stages, τ the delay of each inverter stage provided by the relation given in Eq. 6.23:

$$\tau = \frac{V_{osc} \cdot C_p}{I_{ctrl}} \tag{6.23}$$

where V_{osc} represents the oscillation amplitude; while, C_p is given by the capacitor $C1$ and the corresponding capacitance of each inverter and I_{ctrl} is the current flowing through the transmission gates. Consequently, substituting Eq. 6.23 into Eq. 6.22 yields to Eq. 6.24 [167]:

$$f_{osc} = \frac{I_{Cctrl}}{2 \cdot N \cdot V_{osc} \cdot C_p} \tag{6.24}$$

The external perturbation $KI(t)$ can be added into the ring oscillator by connecting the perturbation signal to one of the inputs of the inverters; although, this implementation would require the external perturbation to be higher than the threshold voltage of each of the inverters. Therefore, in order to perform operations with an external perturbation in the range $V_{SS} \leq KI(t) \leq V_{DD}$, the analogue ALU (described in chapter 3) has been used to substitute one of the inverters as shown in Fig. 6.16 while satisfying the mathematical model of Eq. 6.21.

In order to derive the value of V_ω,which controls the frequency of the ring oscillators by varying the bias voltage on the gates of the transmission gates, the model proposed in Eq. 6.15 and 6.21 requires the use of a multiplication algorithm between the oscillator and the input $I(t)$; therefore, the analogue multiplier designed in section 3.2.2 can be

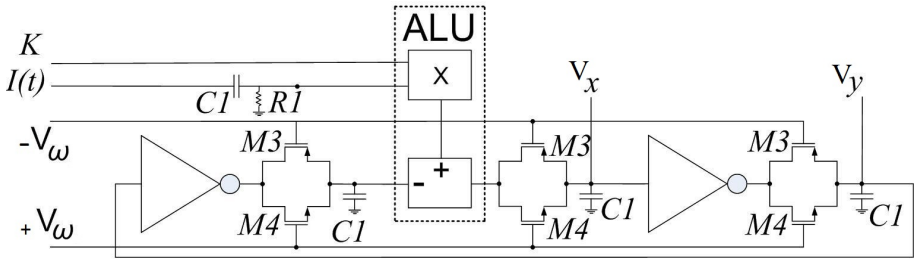

FIGURE 6.16: Modified ring oscillator with analogue ALU to allow the injection of input values in the range $V_{SS} \leq KI(t) \leq V_{DD}$.

employed for this purpose. Such multiplier necessitates a positive and a negative version of the incoming inputs (V_y and $I(t)$); hence, in order to create an inverted version of the output of the ring oscillator of Fig. 6.16, an extra inverter was added at the output of the ring oscillator in the configuration shown in Fig. 6.17 (a). It is possible to observe from the graph of Fig. 6.17 (b), obtained with a SPICE simulation, that the two signals are practically in a 180° phase difference; this is achieved by connecting the input of the second inverter between the output of the first inverter and its transmission gate.

Consequently, the value of V_ω is given by the multiplication between the signals V_y (coming from the ring oscillator) and the incoming perturbation $I(t)$. Additionally, as the transmission gates are designed with both NMOS and PMOS transistors, an inverted version of V_ω has to be provided so that V_ω will bias the NMOS transistors while $-V_\omega$ will bias the PMOS transistors of the transmission gates. This can simply be achieved by firstly using the multiplier (shown in Fig. 3.8) with two current subtractors where the input currents of the two current subtractors are respectively inverted to generate the two inverted signals V_ω and $-V_\omega$ as described in Eq. 6.25 and 6.26 and in Fig. 6.18.

$$V_{\omega,n} = (I_1 - I_2) \tag{6.25}$$

$$V_{\omega,p} = (I_2 - I_1) \tag{6.26}$$

Secondly, the voltage values $V_{\omega,n}$ and $V_{\omega,p}$, at this stage, are still oscillating signals which are not suitable for representing the gate voltages V_ω and $-V_\omega$ of the ring oscillator of Fig. 6.16; therefore, the circuits in Fig. 6.19 can be used to transform the signals $V_{\omega,n}$ and $V_{\omega,p}$ into the respective DC values V_ω and $-V_\omega$.

The reference voltage V_{ref} in Figure 6.19 (a) and (b) are set very low to keep the transistors $M_{\omega,n}$ and $M_{\omega,p}$ in the cut-off region and therefore creating a high resistance that will allow the implementation of a smaller capacitor (C_ω) which will be charged when the transistors $M_{\omega,n}$ and $M_{\omega,p}$ are forward biased; while, they will act as diodes

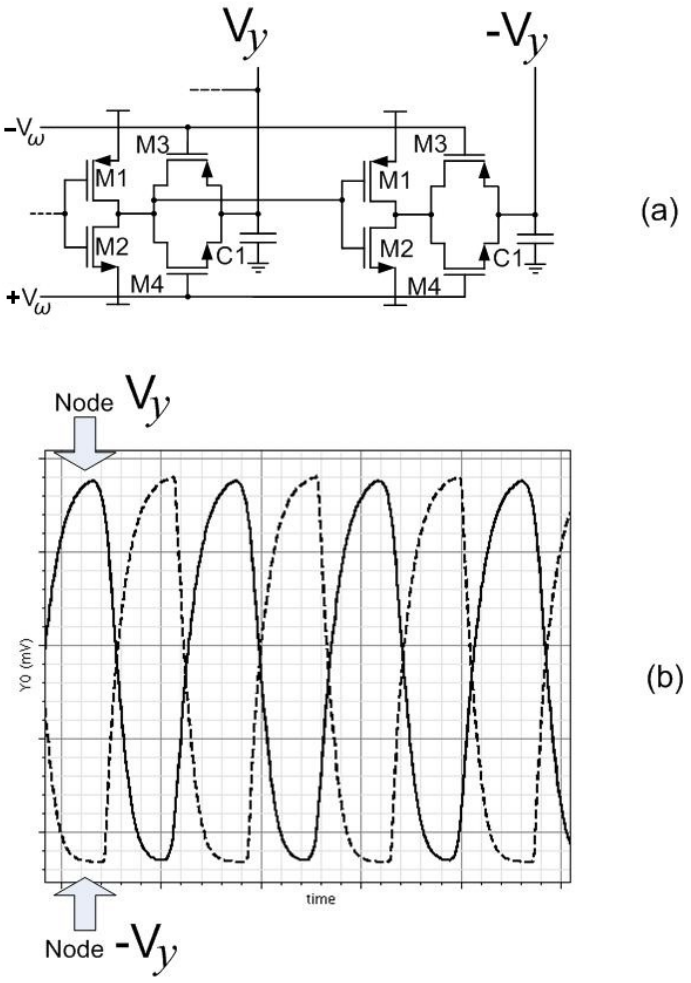

FIGURE 6.17: (a) transistor schematic used to generate two inverted signals (Node A and Node B); (b) output of the

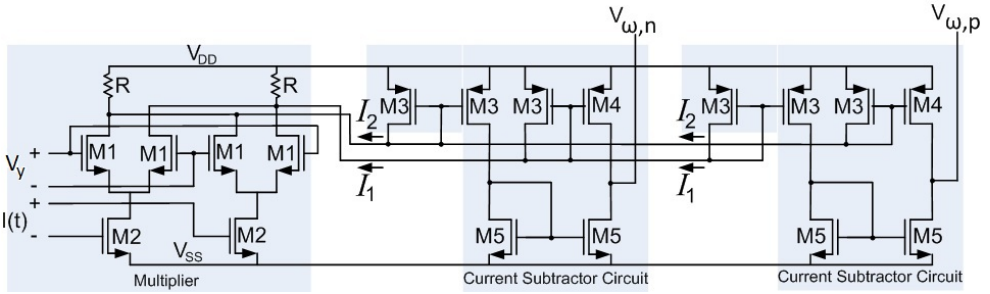

FIGURE 6.18: (a) Block diagram of the analogue multiplier and formulation of $V_{\omega,n}$ and $V_{\omega,p}$ with the use of two current subtracting circuits; (b) transistor schematic.

when reverse biased.

Consequently, the amplitude of V_ω and $-V_\omega$ varies according to the multiplied signals $V_{\omega,n}$ and $V_{\omega,p}$ and can be calculated by combining Eq. 6.27 [15] with Eq. 6.28 (which has been derived directly through experimental method by observing the internal signals at the nodes $V_{\omega,n,max}$ and $V_{\omega,p,max}$) as shown in Eq. 6.29:

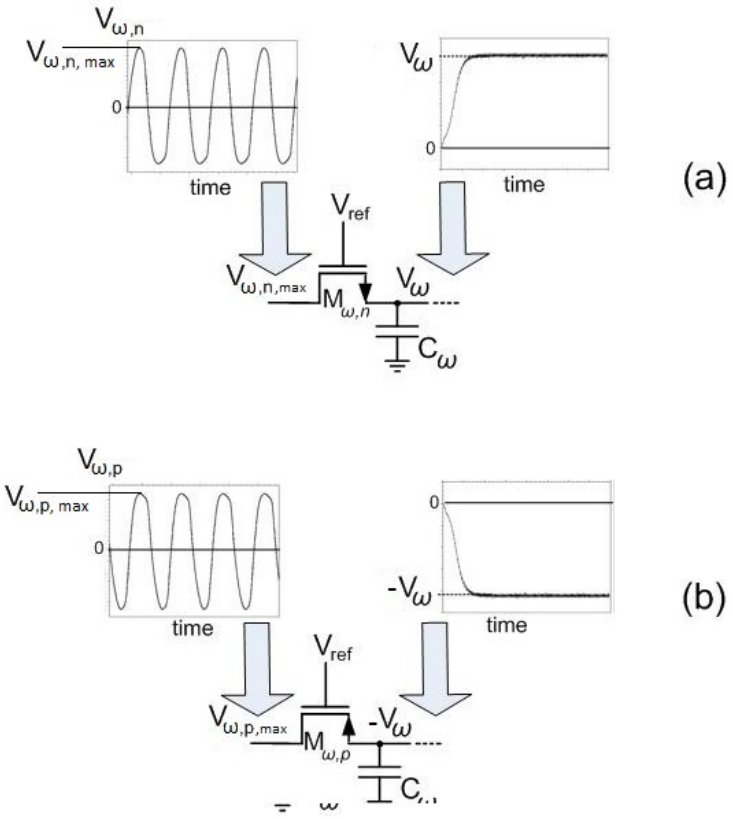

FIGURE 6.19: Transistor schematics for the DC conversion of the multiplied signals $V_{osc,n}$ and $V_{osc,n}$.

$$\begin{cases} V_\omega = V_{\omega,n,max} - V_{\omega,n,max} \cdot sin(\omega_0), \\ -V_\omega = V_{\omega,p,max} - V_{\omega,p,max} \cdot sin(\omega_0), \end{cases} \tag{6.27}$$

$$sin\omega = sin(\omega_0) \cdot sin(\omega_0 + \theta) \tag{6.28}$$

$$\begin{cases} V_\omega = V_{\omega,n,max} - V_{\omega,n,max} \cdot (sin(\omega_0) \cdot sin(\omega_0 + \theta)), \\ -V_\omega = V_{\omega,p,max} - V_{\omega,p,max} \cdot (sin(\omega_0) \cdot sin(\omega_0 + \theta)), \end{cases} \tag{6.29}$$

Where $V_{\omega,n,max}$ and $V_{\omega,p,max}$ represent the maximum voltage at the node before transistors $M_{\omega,n}$ and $M_{\omega,p}$; while ω_0 represents the intrinsic frequency (in Hz), while the phase difference θ in Eq. 6.28 and 6.29 is generated by the physical delay that is generated between the input signal $I(t)$ and the node V_y from the ring oscillator (Fig. 6.16).

The configuration given by $M_{\omega,n}$ and $M_{\omega,p}$ with the capacitor C_ω acts similarly to a rectifier, and it is possible to calculate the amount of ripple by following either Eq. 6.30 or 6.31 [15]:

$$V_{Ripple} \approx \frac{V_{\omega,n} - V_{TH,on}}{R_L \cdot C_\omega \cdot f_{in}} \tag{6.30}$$

$$V_{Ripple} = \frac{I_L}{C_\omega \cdot f_{in}} \tag{6.31}$$

Where f_{in} is the frequency of the input, $V_{TH,on}$ is the threshold voltage of the transistor ($M_{\omega,n}$), R_L, in Eq. 6.30, is given by the resistance generated by transistors $M_{\omega,n}$ and $M_{\omega,p}$ when reverse biased; whilst, I_L, in Eq. 6.31, is the current flowing through $M_{\omega,n}$ and $M_{\omega,p}$ when reverse biased.
The learning time of the oscillator can either be set by adjusting the value of the gain parameter K (see Eq. 6.15 and Fig. 6.16), and by varying the dimensions of the capacitor C_ω. To be considered that the reduction of the capacitor C_ω would allow a faster learning time, but also an increase in the ripple of V_ω. Consequently, the circuits of Fig. 6.19 can be replicated twice in series as shown in the example in Fig. 6.20 to reduce the voltage ripple described in Eq. 6.30 and 6.31.

Fig. 6.21 (a) and (b) show a block diagram and a more detailed transistor schematic

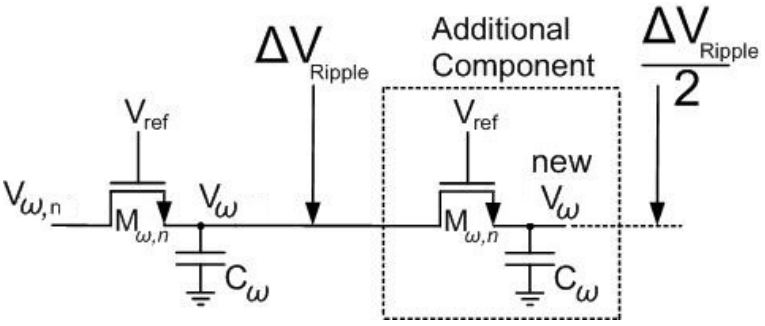

FIGURE 6.20: Circuit to reduce the ripple on V_ω.

of the model described in Eq. 6.15 and 6.21.

6.6 Simulation Results

The following subsections present a full set of simulations which was performed on Cadence Spectre to evaluate the circuit performance.

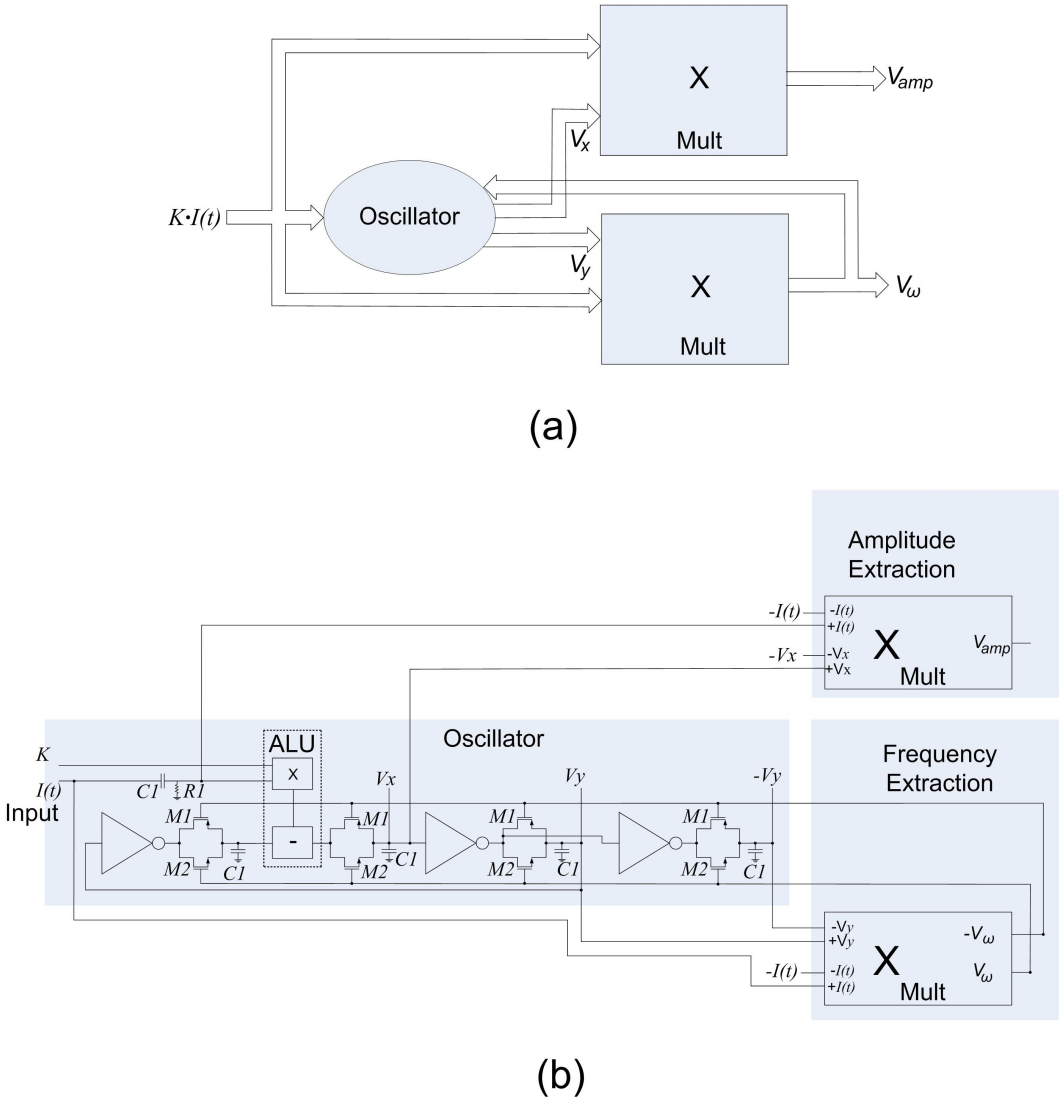

FIGURE 6.21: (a) Block diagram and (b) transistor schematic based on the new model presented in Eq. 6.15.

6.6.1 Adaptation to Monotone and Multiple-Frequency Signals

Fig. 6.22 shows the response of the circuit to a monotone sinusoidal input. It can be observed that the circuit level behavior of the oscillator is consistent with the system level simulation (shown in Fig. 6.10). As previously discussed, there is a frequency basin which indicates the range of the frequencies that can be adapted by the oscillator. In this particular case the frequency basin ranges from 7 MHz to 45 MHz (to be noted, this high frequency basin was randomly chosen also to demonstrate that such system can operate even at high frequency ranges).

As previously explained in section 6.5 the value of V_ω can be calculated by following Eq. 6.29. Therefore, by taking Fig. 6.22 as an example and proof of concept, it is possible to observe that V_ω is approx 160 mV for an input frequency of 7 MHz, and

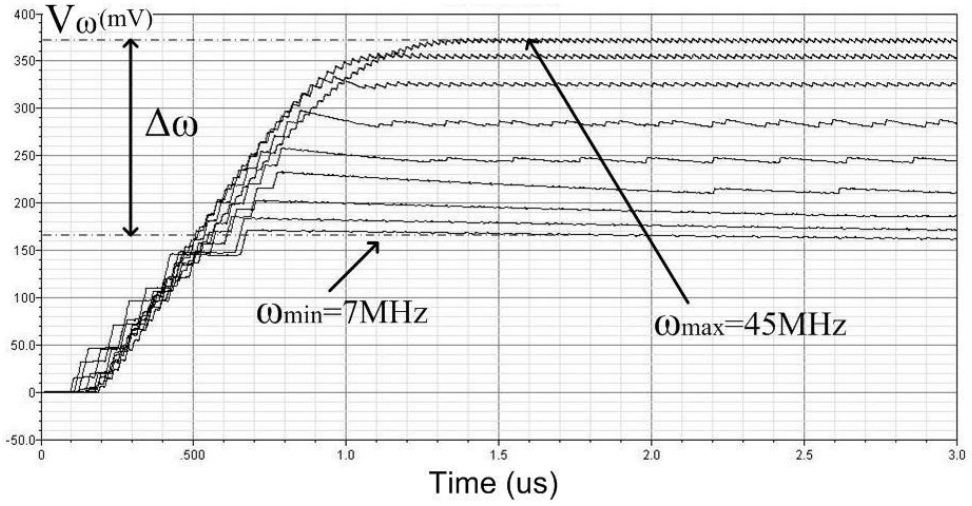

FIGURE 6.22: Circuit response to different input frequencies over the frequency catchment range ($[\omega_{min}, \omega_{max}]$).

approximately 370 mV when the input frequency is 45 MHz. Therefore, substituting the values $V_{\omega,n,max} = 0.35(V)$ and $\theta_0 = 120$ (measured on SPICE simulations) into Eq. 6.29, the resulting values of V_ω can be shown in Table 6.3:

TABLE 6.3: Comparison of the mathematical derivation of V_ω in Eq. 6.29 with the experimental results in Fig. 6.22

ω_0 **(MHz)**	V_ω **(V) (from Eq. 6.29)**	V_ω **(V) (from Fig. 6.22)**
7	0.15	0.155
45	0.38	0.37

It is possible to observe that the numerical values of V_ω displayed in table 6.3 match with the values of V_ω obtained in Fig. 6.22.

It can be observed from Fig. 6.22 that the mapping of the detected frequencies to this range is not linear. This non-linearity is quite prominent at the lower and upper ends of the frequency basin while maintaining linear mapping around the middle range. This non-linear mapping effect is attributed to the saturation effect of the transistor components.

Fig. 6.23 shows the result of a simulation where a mixed input signal is applied to the oscillator; it can be noted that after a certain learning time the oscillator adapts to the input frequency component having the largest amplitude.

Additionally, in both results of Fig. 6.22 and 6.23, a small ripple in the value of V_ω is present and this can be calculated using Eq. 6.30. To be considered that this small amount of ripple does not interfere with the dynamic plasticity property of the oscillator.

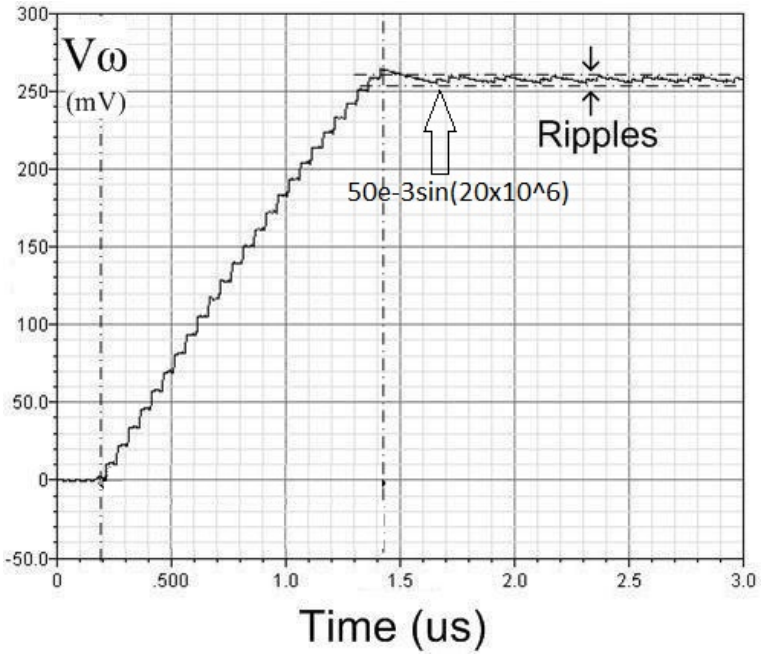

FIGURE 6.23: Oscillator response to $I(t) = 10e-3sin(1\times10^6)+50e-3sin(20\times10^6)+10e-3sin(10\times10^6)$ mV. The oscillator is adapting to the signal with higher amplitude $(50e-3sin(20\times10^6))$.

6.6.2 Non-Stationary Signals

The response of the oscillator to a non-stationary input is depicted in Fig. 6.24 where the input signal is composed of different frequencies at different times instants. As can be observed, the oscillator adapts its frequency to the new input frequency in each period of time as expected from the mathematical property of the adaptive oscillator. It is to be noted that unlike system level simulations the learning times at the circuit level are very short and even negligible in most of the cases.

6.6.3 Amplitude Detection

The simulation characteristic of the proposed adaptive oscillator for detecting amplitudes of different frequency components is shown in Fig. 6.25. In this simulation several inputs with different amplitudes, and same frequencies are applied to the circuit. It is clearly evident from Fig. 6.25 that there exists a one-to-one relationship of the amplitude of the applied frequency components and the corresponding output voltage. However, as in the case of frequency adaptation, there exists some nonlinearity in this relationship around the edge of the frequency basin.

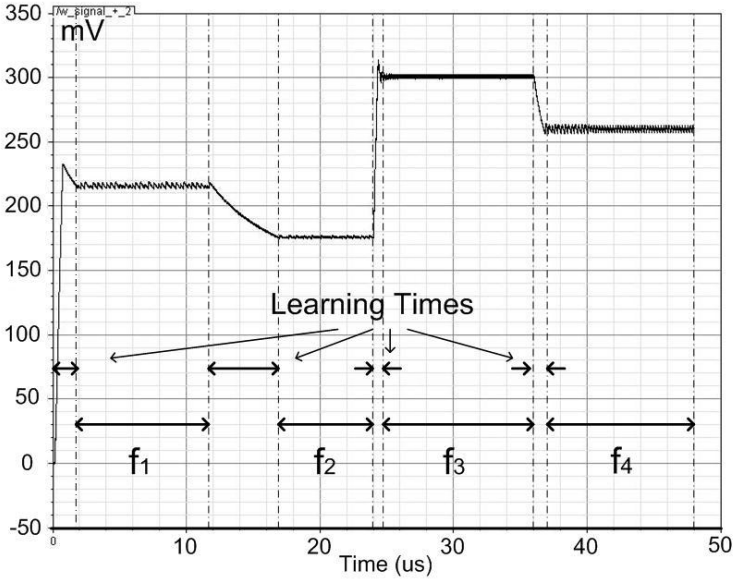

FIGURE 6.24: Behaviour of the oscillator under non-stationary monotones.

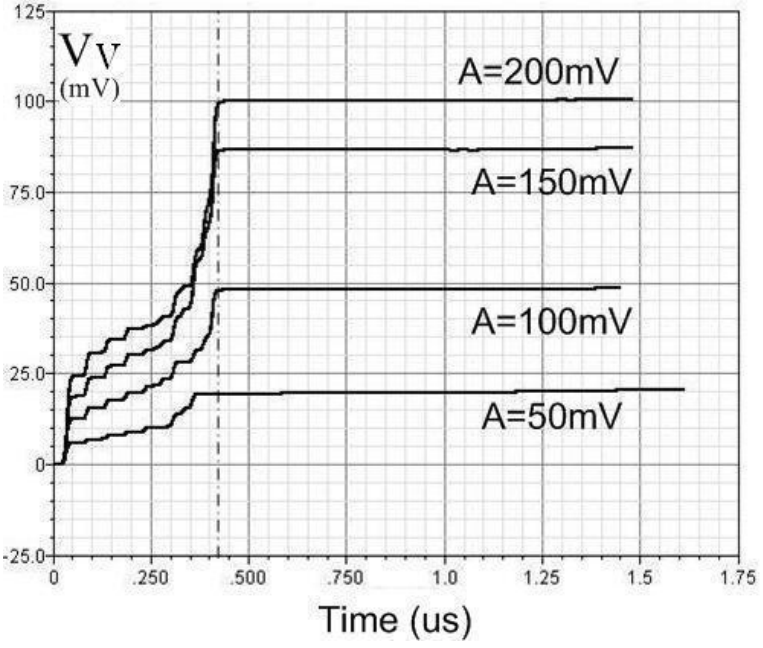

FIGURE 6.25: Simulated characteristics of the amplitude detection circuit.

6.7 Conclusion

The mathematical models of non-linear oscillators have been explored showing the potentials that these models have to offer in signal processing applications. Hence, it was evaluated that the model of Hopf oscillator would provide better performances in the field of signal processing; consequently, it was considered a modified model of Hopf oscillator with inherent dynamic plasticity and its characteristics were improved to more easily implement it in hardware. The circuit has been developed on a 130nm CMOS

Technology, with a total of 87 transistors, with a maximum length and width of 130nm and 400nm respectively. Cadence Spectre has been used for experimental simulations when the circuit was used to extract frequency and amplitude components of external inputs such as single sinusoids, mixed sinusoids, stationary and non-stationary signals. The results obtained showed the potential that this new approach has to offer in the field of signal processing. Consequently this could be further optimized for biomedical and communication applications.

Chapter 7

A New Model of Coupled Non-Linear Oscillators for Signal Processing

In this chapter an improved methodology for signal processing based on the work described in chapter 6 is presented. Such methodology was inspired by the performances obtained by the modified Hopf oscillator and its limitations. Indeed, the new model of oscillator (presented in this chapter) allows better performance when extracting frequency and amplitude of mixed signals where the noise is much greater than the signal of interest.
The proposed methodology is designed in 130nm CMOS Technology in the analogue domain allowing a compact design which can be adapted to different applications such as medical devices and communication.

7.1 Performance and Limitations of the Work Presented in Chapter 6

The model of Hopf oscillator described in Eq. 6.5 showed that this could be used for frequency and amplitude analysis when inherent dynamic plasticity was introduced. Consequently, the modified model shown in Eq. 6.15 provided a new configuration for a non-linear oscillator with inherent dynamic plasticity which would allow an easier implementation in the analogue VLSI environment. The results obtained by the latter proved that the designed oscillator could adapt to external input signals for the extraction of frequency and amplitude components (as in Fourier and Wavelet transforms), although this presented the following limitations:

1. if two or more signals are applied to the oscillator (e.g. input $I(t)$ and noise), the oscillator is able to extract the frequency and amplitude components of $I(t)$ until the noise does not become much greater than the input $I(t)$.

2. The oscillator can not extract the frequency and amplitude components when a large number of mixed signals (e.g. > 3) are applied to the oscillator.

Therefore, the above points can limit the outcome of the frequency and amplitude analysis of external signals which are presented in a more realistic environment where the number and randomness of mixed signals can constantly vary.

7.2 A New Model for Signal Processing based on Coupled Non-Linear Oscillators with Inherent Dynamic Plasticity

Both the models described in Eq. 6.5 by [159] and the new modified non-linear Hopf oscillator presented in Eq. 6.15 determined the frequency adaptation of the oscillator by multiplying the input perturbation $I(t)$ by the terms x and y depending on [159] and the model in Eq. 6.15 respectively. Accordingly, the value of $\dot{\omega}$ (which defines the frequency value of the oscillator) can generate a large amount of ripple when the input perturbation is given by a complex summation of signals. Consequently, the produced ripple would corrupt the understanding of which frequency components are present at the input $I(t)$ (as it will be shown in the comparison section 7.4.5).
Therefore, the ripple in the value of $\dot{\omega}$ can drastically be reduced by changing the adaptation algorithm and the formulation of $\dot{\omega}$, while keeping the amplitude extraction algorithm described in Eq. 6.20.
The new proposed model uses two coupled non-linear oscillators where the value of $\dot{\omega}$ is defined by the interaction of the two oscillators as shown in the block diagram of Fig. 7.1. From Fig. 7.1 it is possible to see how the input $I(t)$ interacts with "Oscillator 1" which then influences "Oscillator 2". Consequently, the evaluation of $\dot{\omega}$ is no longer performed by multiplying the input signal $I(t)$ with $\dot{y}$ as in the previous models, but it is calculated by multiplying the interaction between the two oscillators. The dynamics of the model is formulated in Eq. 7.1.

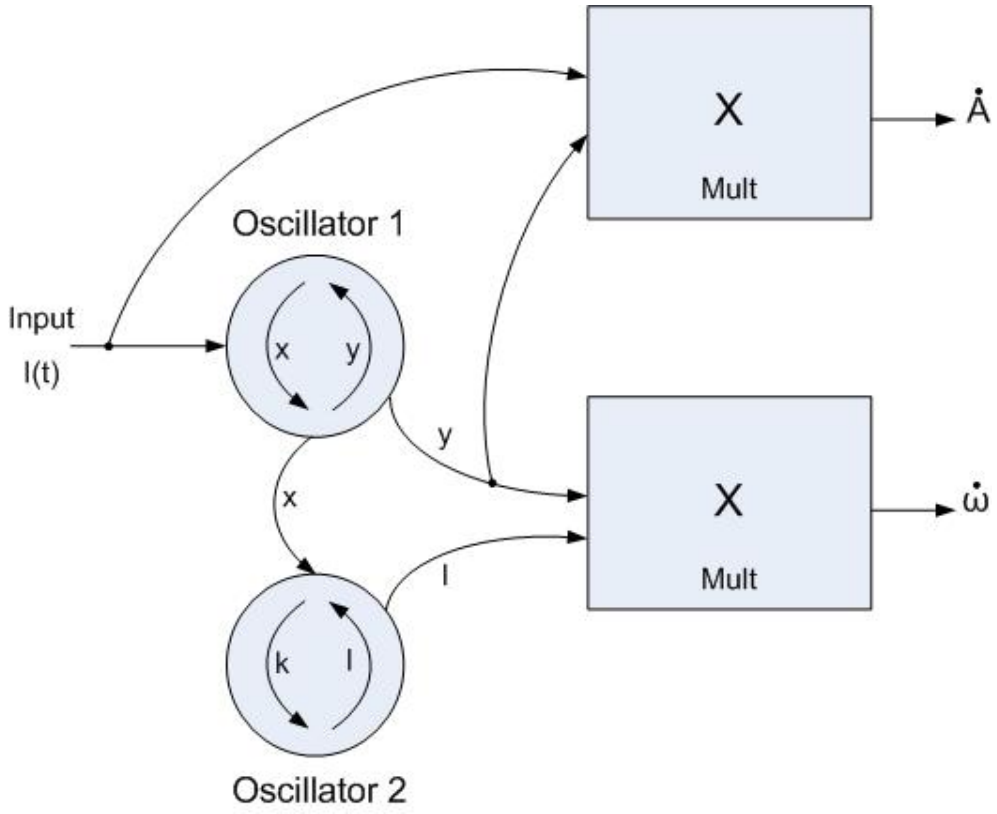

FIGURE 7.1: Block diagram of the new model for signal processing based on coupled non-linear oscillators.

$$\begin{aligned}
\dot{x} &= (\mu - (|x| + |y|))sgn(x) + \omega y + KI(t) \\
\dot{y} &= (\mu - (|x| + |y|))sgn(y) - \omega x \\
\dot{k} &= (\mu - (|k| + |l|))sgn(k) + \omega l + \omega x \\
\dot{l} &= (\mu - (|k| + |l|))sgn(l) - \omega k \\
\dot{\omega} &= y \cdot l
\end{aligned} \tag{7.1}$$

Where the first oscillator is defined by the state variables x and y and the second oscillator is defined by the state variables k and l. The coupling parameter between the two oscillators is given by injecting the node ωx of the first oscillator into the second oscillator. Consequently the estimation of $\dot{\omega}$ is given by the multiplication of y and l.

7.3 Circuit Implementation

The circuit implementation for the model described in Eq. 7.1 follows the same notations described in Table 6.2.

As described in the block diagram of Fig. 7.1, two oscillators and two multipliers are

required for this model. Both of these circuits use the same structure shown in Fig. 6.16 and 3.8 as for the model described in Eq. 6.15. Additionally, the values of V_ω and $-V_\omega$ are designed in the same manner as described in Fig. 6.19 and Eq. 6.29.
Fig. 7.2 shows the circuit schematic of the entire model described in Eq. 7.1.

It is possible to notice in Fig. 7.2 the presence of an additional inverter (named

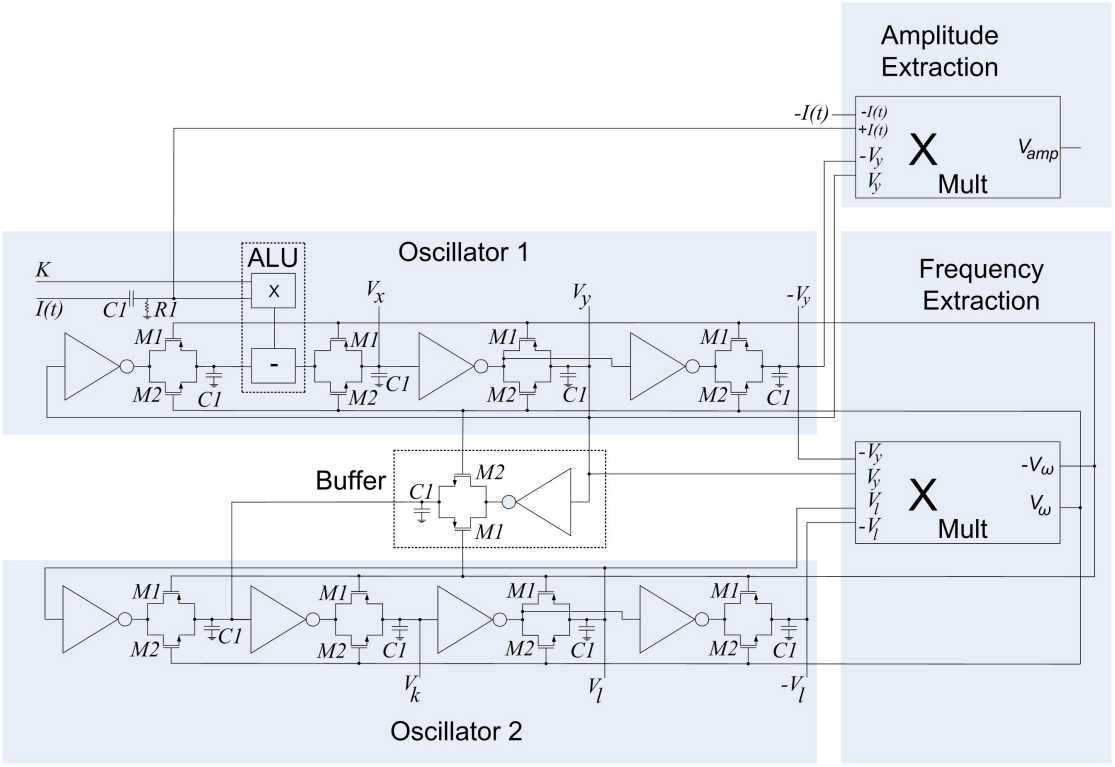

FIGURE 7.2: Transistor schematic of the model presented in Eq. 7.1.

"Buffer"); this indeed is used as a buffer between the two oscillators, so that only "Oscillator 1" will affect the frequency of "Oscillator 2" and not vice versa. The transistors in the circuit schematic of Fig. 7.2 are designed in 130nm CMOS Technology with a maximum length and width of 130nm and 400nm respectively, and 11 capacitors in the pico Farad range.

7.4 Simulation Results

A full set of simulations was performed using Cadence Spectre to evaluate the circuit performance. Single and mixed signals (including real biomedical signals such as EMG and ECG signals) have been used to validate the system.

7.4.1 Single Sinusoid

The first experiment involved the frequency and amplitude extraction of a single external sinusoid $I(t)$.
Fig. 7.3 and 7.4 show the frequency and amplitude extraction of the external signal $I(t)$ respectively.

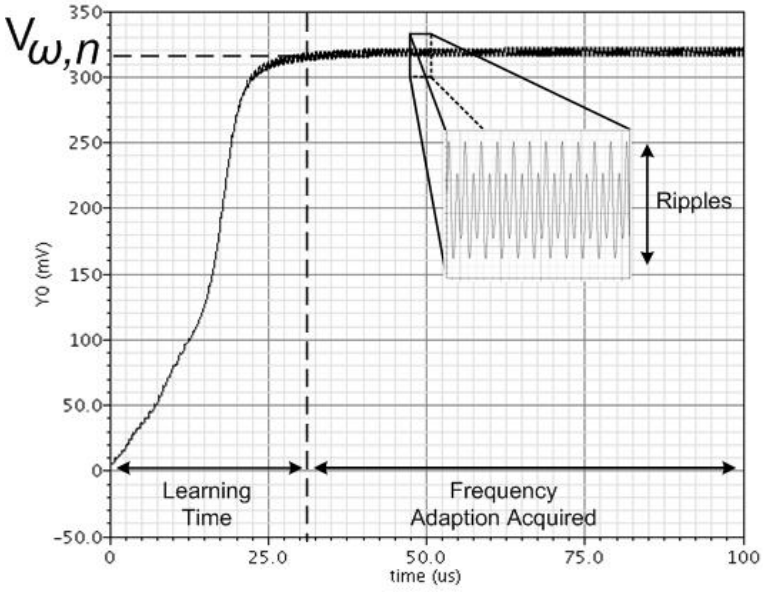

FIGURE 7.3: Frequency adaptation to the external signal $I(t) = 200{\cdot}10^{-3}{\cdot}sin(2{\cdot}\pi{\cdot}3{\cdot}10^{6})$.

Moreover, Fig. 7.3 also shows a zoomed part of the ripple present in V_ω; although this does not interfere with the outcome of the frequency extraction.
Fig. 7.5 illustrates an example of the frequency adaptation of the oscillator for different external signals within the oscillators basin. It is possible to observe how the value of V_ω presents less ripple than the values of V_ω shown in Fig. 6.22 for the previous model described in Eq. 6.15.

7.4.2 Mixture of Stationary Sinusoids

As previously explained, one of the abilities of non-linear oscillators is given by the extraction of frequency and amplitude components of complex mixed signals. Therefore, by setting a cluster of oscillators with different basins, it is possible to extract each of the signals present in a set of mixed signals as shown in Fig. 7.6.

Fig. 7.7 illustrates the simulation results when the mixed signal $I(t) = A{\cdot}sin(\omega_1+)A{\cdot}sin(\omega_2)+ A{\cdot}sin(\omega_3) + A{\cdot}sin(\omega_4)$ is inputted into a cluster of oscillators with different basins, as shown in Fig. 7.6. It is possible to see how the cluster of oscillators can clearly extract all the frequency and amplitude components.

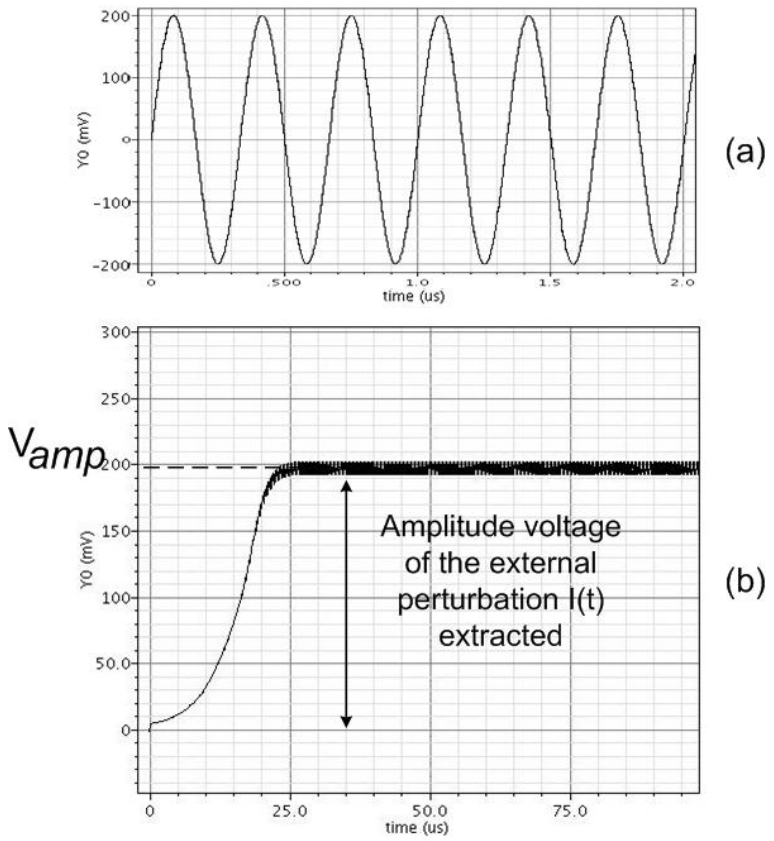

FIGURE 7.4: Amplitude voltage extraction. (a) the external signal $I(t) = 200{\cdot}10^{-3}{\cdot}sin(\omega)$; (b) amplitude voltage extracted

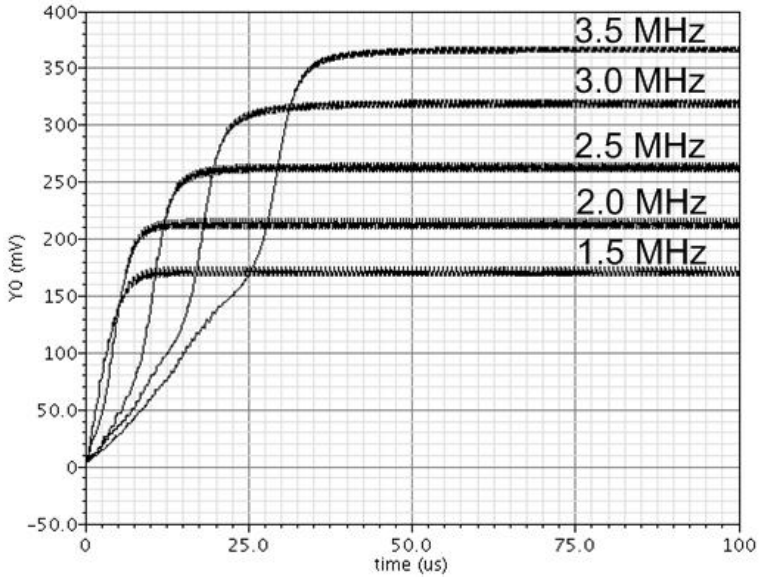

FIGURE 7.5: Frequency adaptation to different external perturbation within the oscillators basin.

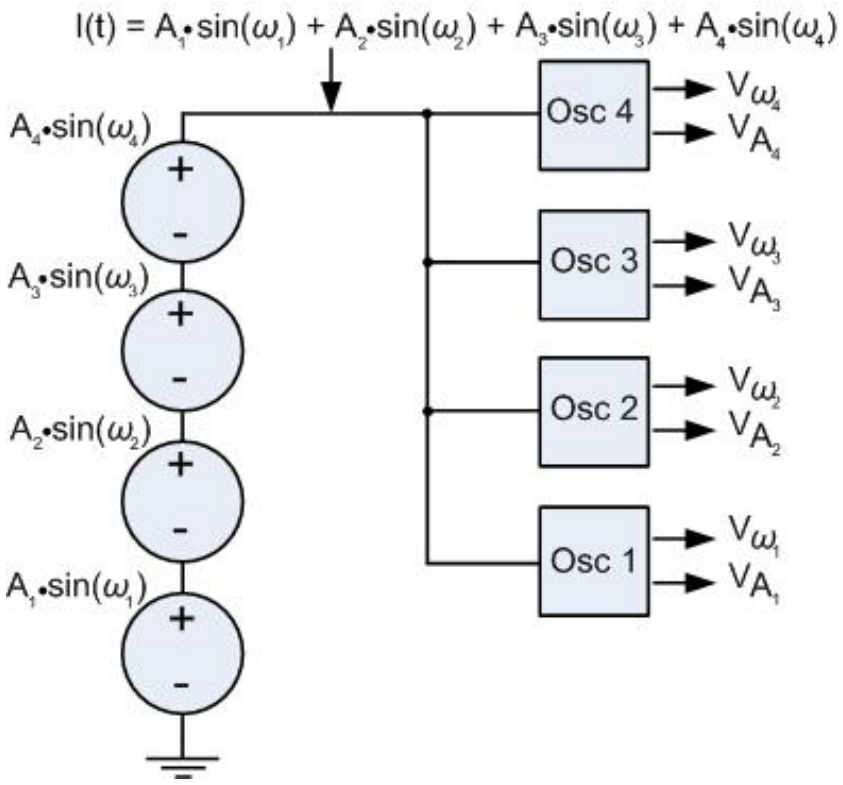

FIGURE 7.6: Schematic of a possible bank of oscillators for the extraction of signals within a set of mixed signals.

7.4.3 Single Non-Stationary Sinusoid

The ability of learning and therefore adapting to new incoming signals allows the tracking and extraction of non-stationary signals. Fig. 7.8 (a) shows an example of frequency extraction of a single non-stationary signal, while Fig. 7.8 (b) shows the ability of the oscillator to track a non-stationary signal within a complex mixed signal as described in the block diagram in Fig. 7.9. However, in this case the ripple on V_ω increases slightly.

7.4.4 Noise Performance

In this set of experiments an external signal composed of white gaussian noise was added to the input $I(t)$ to verify wether the proposed model could still extract the input $I(t)$. Fig. 7.10 illustrates the inputs used for these experiments: (a) White Gaussian Noise (WGN); (b) the input sinusoid $I(t) = A{\cdot}sin(\omega)$; and (c) the mixed signal $I(t) = A{\cdot}sin(\omega) + WGN$. Fig. 7.11 (a) shows the extracted output voltage V_ω when only the input signal $I(t) = A{\cdot}sin(\omega)$ is inputted to the oscillator; while, Fig. 7.11 (b-f) shows the output voltage V_ω when the white gaussian noise is gradually increased and added to $I(t)$.

From Fig. 7.11 (b-f) it is possible to observe that V_ω slightly deteriorates as the SNR value decreases, but still the oscillator can accurately extract the input signal

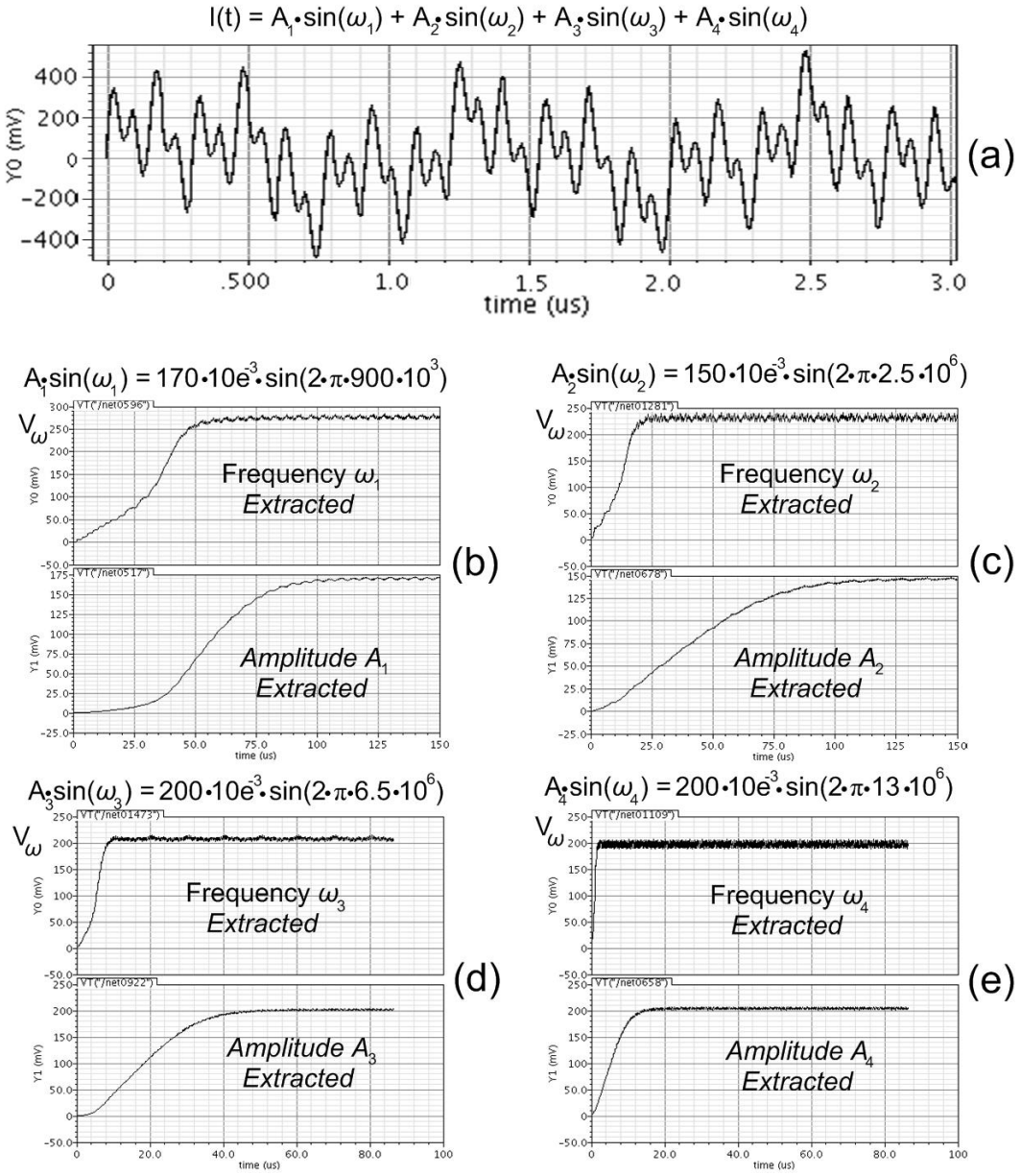

FIGURE 7.7: Simulation results for frequency and amplitude extraction of individual signals within a set of mixed signals. (a) mixed input signal $I(t) = A{\cdot}sin(\omega_1) + A{\cdot}sin(\omega_2) + A{\cdot}sin(\omega_3) + A{\cdot}sin(\omega_4)$; (b) frequency and amplitude extraction of $A{\cdot}sin(\omega_1)$; (c) frequency and amplitude extraction of $A{\cdot}sin(\omega_2)$; (d) frequency and amplitude extraction of $A{\cdot}sin(\omega_3)$; (e) frequency and amplitude extraction of $A{\cdot}sin(\omega_4)$.

$I(t) = A{\cdot}sin(\omega)$ even when the $SNR_{dB} = -5.26$ dB.

In order to quantify the dynamic power supply noise sensitivity, different experiments have been performed by adding an external tone $B{\cdot}sin{\cdot}(\omega_N)$ (50Hz mains) to the power supply V_{DD} while the oscillator was extracting the frequency of a monotone signal.
In usual experimental cases the amplitude noise is considered to be 4% of V_{DD} [168]; while, the new presented model of oscillator can still perform signal analysis when the

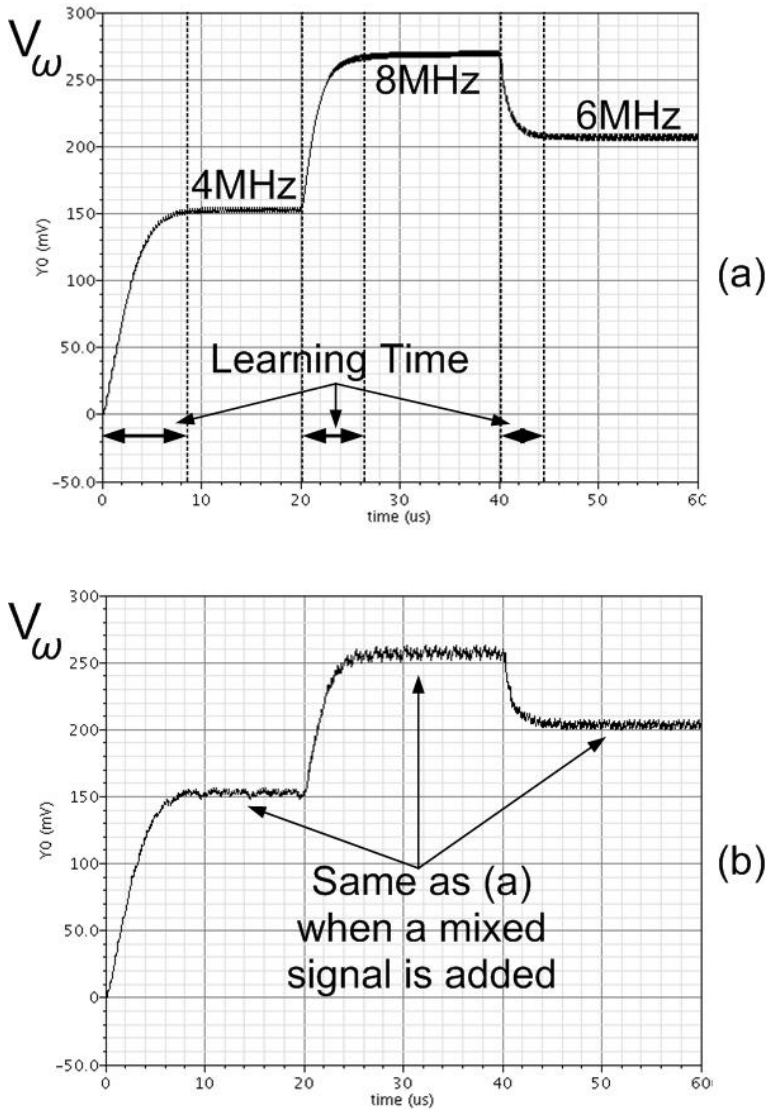

FIGURE 7.8: (a) frequency extraction of a non stationary sinusoid; (b) frequency extraction of a non-stationary signal inside a set of mixed signals.

noise reaches up to 17% of V_{DD}. Fig. 7.12 shows the increase of ripple voltage (V_{Ripple}) presented on the value V_ω against the increase of noised power supply. The noise signal is increased from 0 (0%), to 50mV (4% of V_{DD}), to 100mV (8% of V_{DD}), to 150mV (12.5% of V_{DD}) and to 200mV (17% of V_{DD}).

From Fig. 7.12 it is possible to observe that the ripple V_{Ripple} in V_ω varies only for large amplitude noise close to 17% of V_{DD}. Therefore, it is possible to conclude that the model presented in Eq. 7.1 could also be used in noisy environments.

7.4.5 Comparison with The Previous Model

In this section, a comparison of the new model of Eq. 7.1 with the previous model presented in Eq. 6.15 is evaluated. As previously explained, the main improvement of

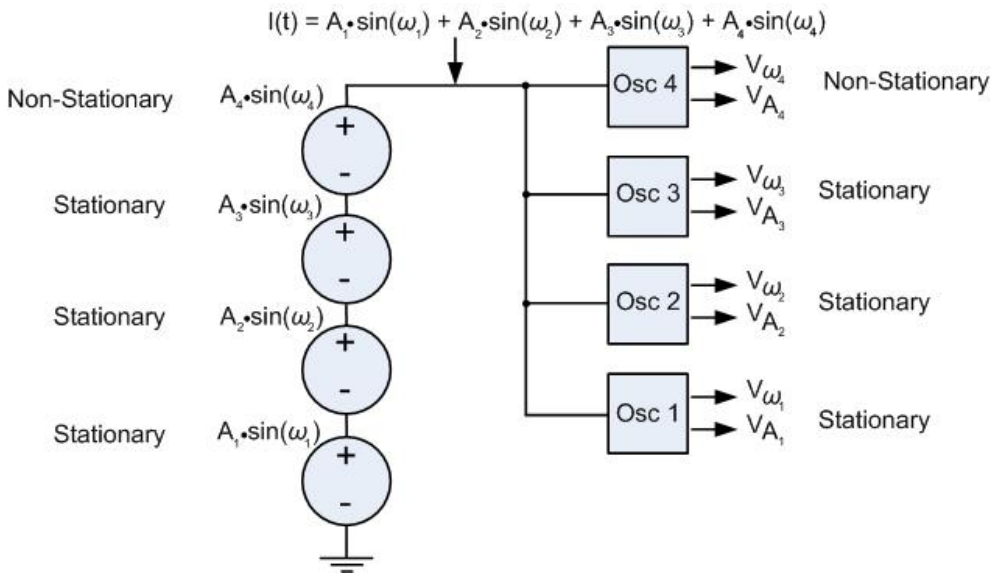

FIGURE 7.9: Schematic of a bank of oscillators for the extraction of a non-stationary signal within a set of mixed signals.

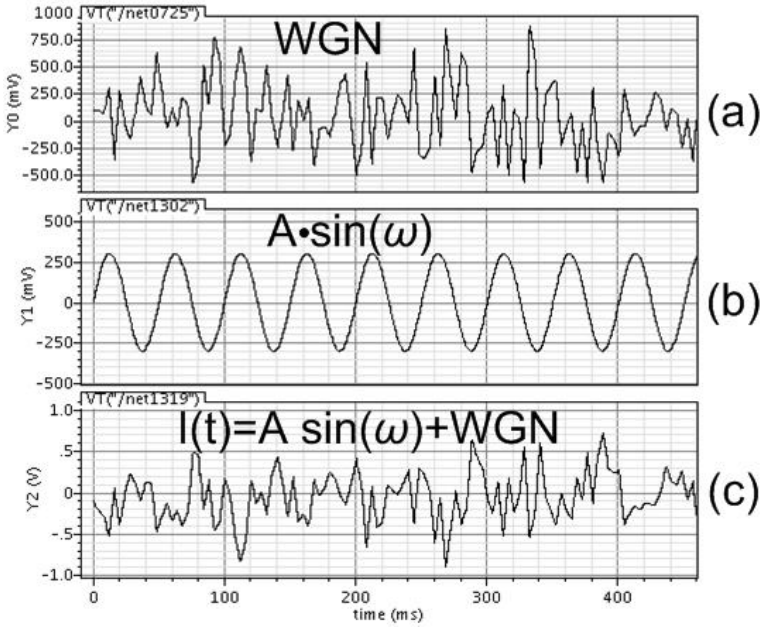

FIGURE 7.10: (a) White Gaussian Noise (WGN); (b) sinusoid $A{\cdot}sin(\omega)$; (c) mixed signal input $I(t) = A{\cdot}sin(\omega) + WGN$.

this new model is given by its ability to extract signals in worst case scenarios, this may include the extraction of a signal within a set of large mixed signals, or when an external noise is added to the signal or to the power supply.

In order to compare the previous model of Eq. 6.15 with the new model presented in Eq. 7.1 a mixed signal of two sinusoids ($A{\cdot}sin{\cdot}(\omega_0) + A{\cdot}sin{\cdot}(\omega_1)$) is inputted into both the oscillator presented in Eq. 6.15 and the oscillator represented by Eq. 7.1. $A{\cdot}sin{\cdot}(\omega_0)$ is set to be part of the frequency basin of each of the oscillators while $A{\cdot}sin{\cdot}(\omega_1)$ represents a sinusoid external to the oscillator basin (and therefore it could be considered as noise).

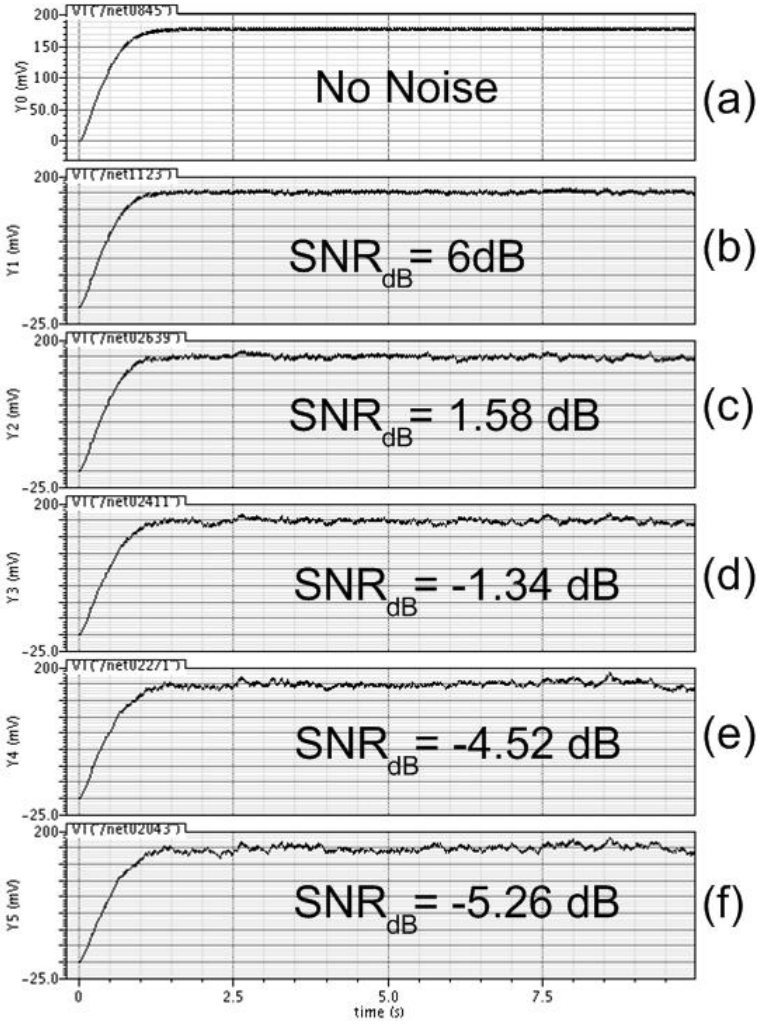

FIGURE 7.11: (a) frequency extraction V_ω with input $I(t) = A{\cdot}sin(\omega)$; (b) frequency extraction V_ω with input $I(t) = A{\cdot}sin(\omega) + WGN$.

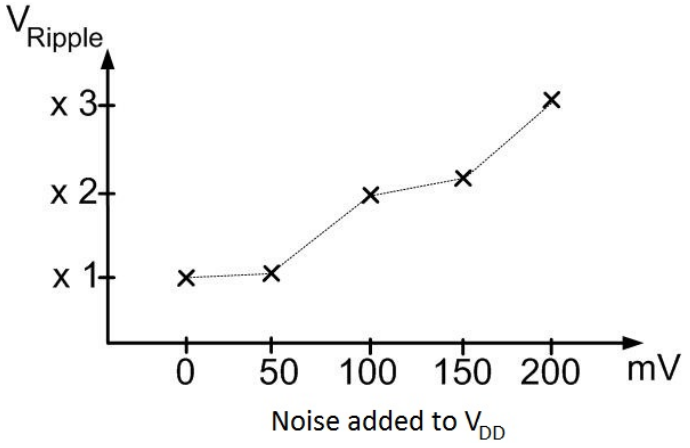

FIGURE 7.12: Different responds of V_{Ripple} (in the value of V_ω) for amplitudes noise up to 200mV.

Fig. 7.13 (a) shows the experimental result when only $A{\cdot}sin{\cdot}(\omega_0)$ is applied to both the oscillators; while, Fig. 7.13 (b), (c), (d) and (e) illustrate how the output voltage V_ω

degrades when the external signal $A{\cdot}sin{\cdot}(\omega_1)$ increases in amplitude. To be noted that the values of V_ω are different for the two models in Fig. 7.13 as the value of V_ω generated by the model in Eq. 6.15 and Eq. 7.1 have different internal parameters (e.g. the value of θ (from Eq. 6.29) is approx ≈ 120 for the model of Eq. 6.15 while the value of θ for the new model in Eq. 7.1 is ≈ 100, also, to be considered that the value of θ can also vary within the basin of each oscillator).

It is possible to observe that the new model presented in Eq. 7.1 shows a slight increase in the ripple of V_ω when the amplitude of $A{\cdot}sin{\cdot}(\omega_1)$ is increased; whilst the value of V_ω for the model previously proposed in Eq. 6.15 becomes unstable for large amplitudes of $A{\cdot}sin{\cdot}(\omega_1)$ and cannot adapt to the external perturbation $I(t)$.

7.4.6 Real Life Biomedical Signals: Electromyography (EMG) Signal

In this section, a real biomedical signal such as the electromyography (EMG) signal is used to observe whether the presented model can extract one of the frequency and amplitude components present in the EMG signal.

Fig. 7.14 (a) shows the frequency spectrum of the EMG signal shown in Fig. 7.14 (b); while Fig. 7.14 (c) and (d) illustrate the output response of the oscillator for frequency and amplitude extraction.

The frequency basin of the oscillator is chosen to capture frequencies in the range $33 - 66$ Hz and the frequency extracted by the oscillator in Fig. 7.14 (c) corresponds to $\approx$48Hz. Furthermore if considering Eq. 6.29 for the calculation of V_ω and substitute $V_{\omega,n,max} = 0.35$, $\theta = 100$ and $\omega_0 = 48$ then the value of V_ω is $\approx$0.26(V) which is in accordance with result shown in Fig. 7.14 (c). Furthermore, in order to verify whether the extracted amplitude, shown in Fig. 7.14 (d), matches with the amplitude of the real 48 Hz frequency component, the 2nd order band pass filter illustrated in Fig. 7.15 was used to extract the signal of interest (as shown in Fig. 7.14 (e)) and also to show the envelope of the amplitude as a comparison between Fig. 7.14 (d) and (f). Consequently it is possible to affirm that the two waveforms appear to be very similar, proving the functionality of the new model in extracting frequency and also amplitude components for such complex biomedical signals as the EMG.

7.4.7 Real Life Biomedical Signals: Electrocardiography (ECG) Signal

The electrocardiography signal is a very complex mixed signal given by the superimposition of multiple sine waves with frequencies of up to 250 Hz [169]. Therefore, in order to see the boundaries and limitations of this new model of oscillator, an ECG signal was applied to the oscillator. The frequency basin of the oscillator was designed to be 6-11 Hz.

Fig. 7.16 (a) shows the input signal (ECG), while Fig. 7.16 (b) and Fig. 7.16 (c) illustrate the frequency and amplitude response of the oscillator.

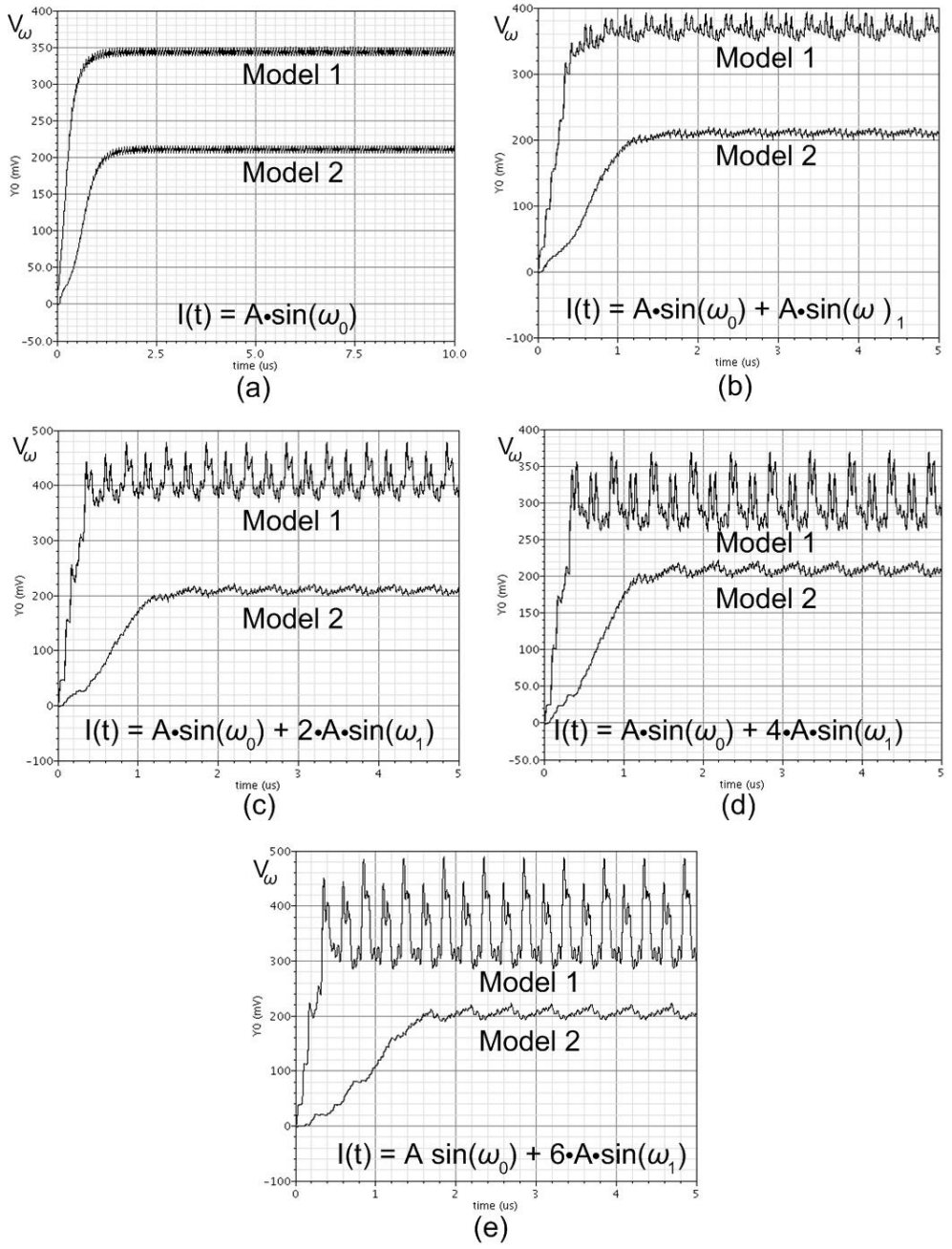

FIGURE 7.13: Comparisons of the previous model of Eq. 6.15 (Model 2 in the figure) and the new presented model of Eq. 7.1 (Model 1 in the figure). (a) V_ω responses when a single sinusoid $A{\cdot}sin{\cdot}(\omega_0)$ is applied; (b) two sinusoids $A{\cdot}sin{\cdot}(\omega_0) + A{\cdot}sin{\cdot}(\omega_1)$ with identical amplitude voltage and different frequencies are applied; (c) two sinusoids $A{\cdot}sin{\cdot}(\omega_0) + 2{\cdot}A{\cdot}sin{\cdot}(\omega_1)$ where the added signal has a larger amplitude voltage $(2{\cdot}A)$; (d) two sinusoids $A{\cdot}sin{\cdot}(\omega_0) + 4{\cdot}A{\cdot}sin{\cdot}(\omega_1)$ where the added signal has a larger amplitude voltage $(4{\cdot}A)$; (e) two sinusoids $A{\cdot}sin{\cdot}(\omega_0) + 6{\cdot}A{\cdot}sin{\cdot}(\omega_1)$ where the added signal has a larger amplitude voltage $(6{\cdot}A)$.

From Fig. 7.16 (b) and (c) it is possible to observe that the frequency varies during the ECG complex showing where the higher frequencies are present within each ECG complex. Furthermore, the extracted amplitude also responds correctly to the incoming ECG.

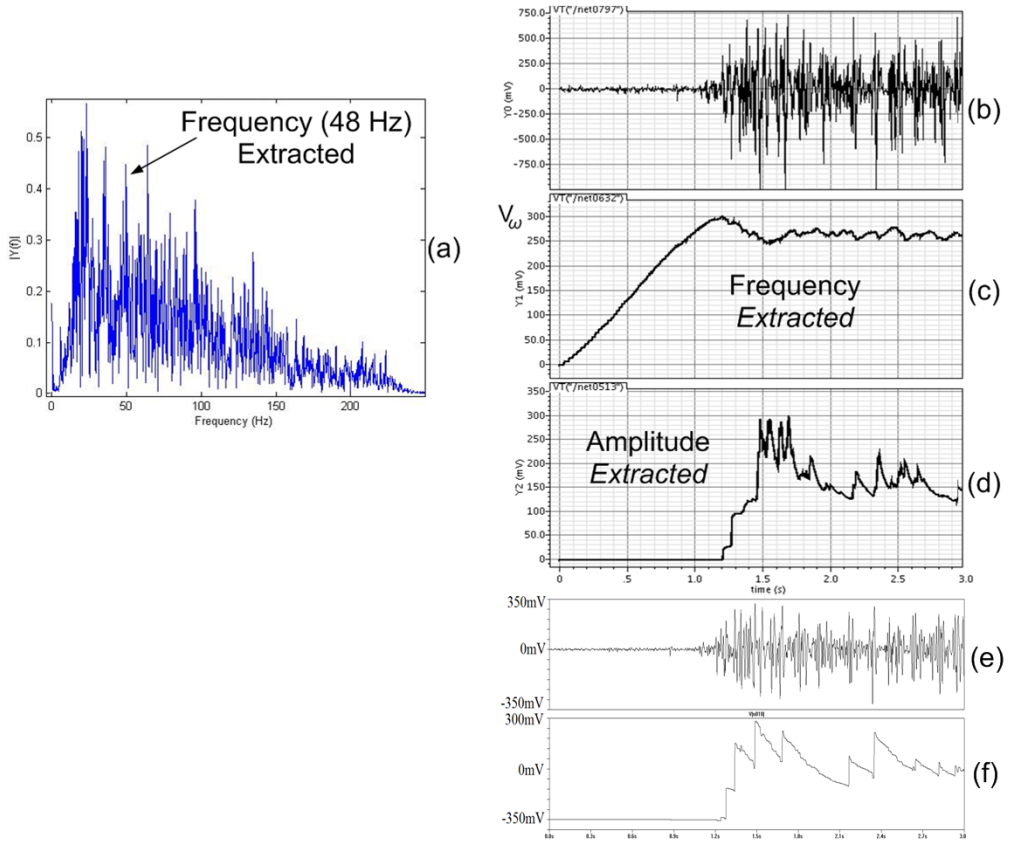

FIGURE 7.14: Frequency and amplitude analysis of a real EMG signal.

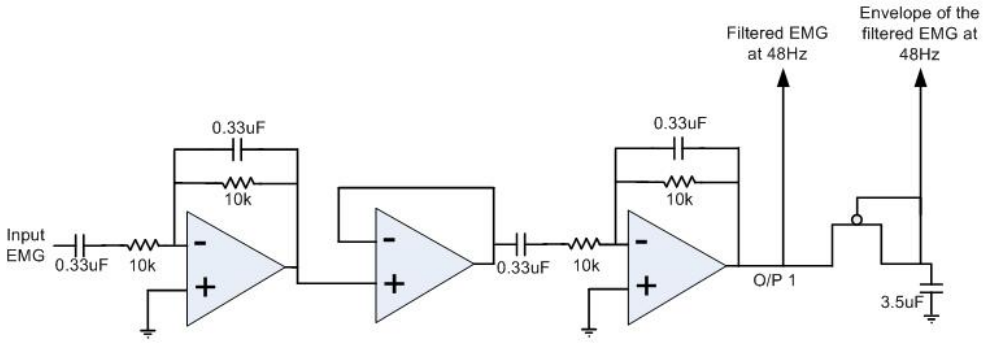

FIGURE 7.15: Circuit schematic of the filter used to extract the 48Hz frequency component within the EMG signal shown in 7.14 (b).

7.5 Conclusion

A new model of non-linear coupled oscillators, based on the model in Eq. 6.15, has been introduced showing the advantages and performances in signal analysis. Furthermore a simple VLSI implementation (on 130nm CMOS technology) has been described and tested with simulation results (on Cadence Spectre). The main advantage of the proposed model is given by the ability of extracting frequencies and amplitudes in very

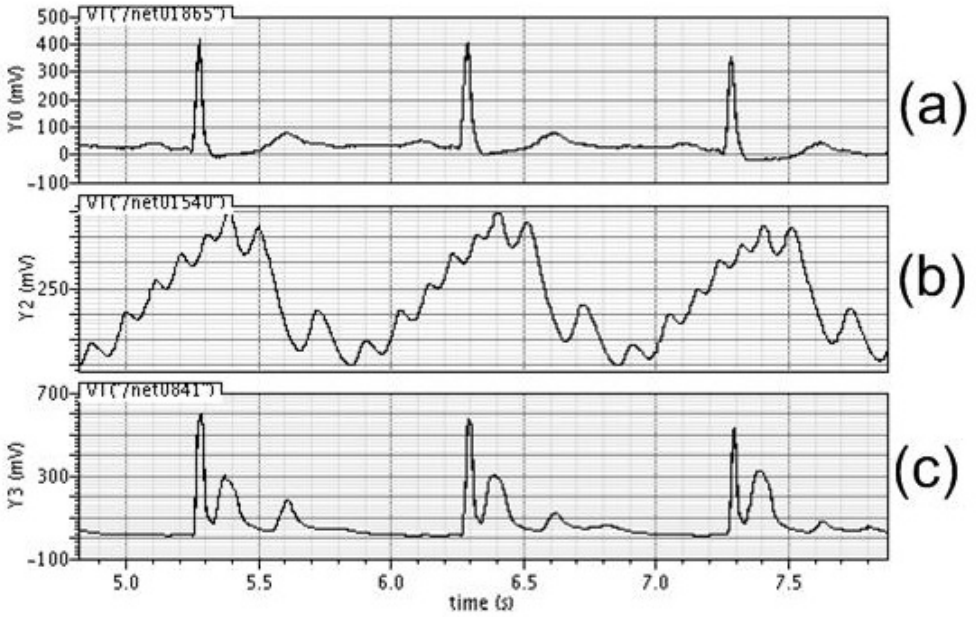

FIGURE 7.16: Frequency and amplitude analysis of a real ECG signal.

complex mixed signals, noisy environments and biomedical signals such as electromyography (EMG) and electrocardiography (ECG) signals. Therefore, such methodology can be used in many real-life applications as in biomedical and communications devices.

Chapter 8

Conclusions and Future Work

The overall aim of this research is to explore the potential advantages of analogue signal processing for real-time applications. In order to achieve this task different methodologies in the field of biomedical signals analysis, which are also applicable to generic signal processing system development, have been formulated and mapped to hardware demonstrating the possibility of analogue signal processing based high-performance system design.
The first step for the achievement of the presented work was to design an analogue ALU to perform the basic mathematical operations required for the performance of the algorithms for signal processing analysis. The first systems that were designed in the analogue domain and used the analogue ALU were two new approaches to control prosthetic hands for high level of upper limb amputation. Successively, a new methodology for the automated detection of heart beat anomalies has been developed and tested for four main heart beat diseases. Additionally, two implementations for signal processing of biomedical signals based on non-linear oscillators have been developed. Such implementations proved the potential of analogue signal processing for biomedical signals, such as EMG and ECG signals, which can be achieved with very few components (approximately less than 100 transistors, in contrast to thousands of transistors in ordinary DSP processors). Synthetic and real biomedical signals have also been used to validate the presented work.

8.1 Summary and Research Contributions

The work achieved during this research has provided a number of different designs in the analogue domain in the field of medical devices and signal analysis. Furthermore, the following contributions have been made:

The implementation of an analogue ALU was needed to perform basic mathematical operations within the presented algorithms, and required studies on different circuit topologies to perform multiplication, addition and subtraction. A Gilbert cell was selected and designed to be the multiplier within the presented analogue ALU. Secondly an improved version of Gilbert cell was provided to allow better performance in terms of output linearity and less number of transistors. Consequently the multiplier circuit was modified to incorporate addition and subtraction. Such modification allowed the analogue ALU to concurrently perform multiplication, addition and subtraction.

Two new methodologies in the field of prosthetic hands have been provided. This involved studies on the human nerve and muscle anatomy of the upper limb and the limitations of other control systems to control prosthetic hands. We studied how the level of amputation could affect the control system to choose the posture of the prosthetic hand and therefore we formulated two new methodologies to control prosthetic hands. In the first methodology, the highest level of upper limb amputation (just below the elbow) was considered, in this scenario the level of amputation allows only the positioning of a single electrode and therefore the capturing of a single EMG signal. Consequently a method for the user to acquire different postures for the prosthetic hand was developed. Such methodology was based on associating each different posture of the hand with a predefined number of EMG stimuli generated by the user. An analogue circuit was then designed and tested with real biomedical signals.

The second methodology that was developed, involved the use of two electrodes (therefore two EMG signals). The positioning of the electrodes was determined by the human muscle anatomy, and the signal captured by these two electrodes allowed us to generate a simple circuit which would allow the user to instantly choose which finger of the prosthetic hand to move as in real biological hands. Consequently, the circuit was tested and validated with real biomedical signals.

A new methodology for the detection of heart beat anomalies was developed. This has required studies on the human heart and ECG characteristics. Consequently, individual heart beat anomalies/diseases such as ventricular premature beats, ventricular tachycardia, atrial fibrillation and atrioventricular blocks were studied and taken into consideration. Hence, an algorithm which could differentiate each of the mentioned heart beat irregularities and also normal heart beats was developed. This was then implemented and tested on MatLab, with 90 real ECG signals which presented the mentioned irregularities, showing the ability of the algorithm to differentiate each heart beat irregularity. Hence, a simple circuit was designed to perform the algorithm in the analogue domain. The circuit was also tested with real ECG signals showing the ability to detect all the mentioned ECG irregularities.

Two new models for signal processing based on non-linear oscillators have been presented for the analysis of biomedical signals. Four models of non-linear oscillators were firstly introduced and the most suitable model for signal processing was selected. the chosen model of oscillator was studied in concurrence with its modified version, presented in the literature, which incorporates inherent dynamic plasticity to adapt its frequency to external signals. Following, the original oscillator was modified to obtain a simpler mathematical model which would then be easier to implement in a hardware environment. The implemented circuit was then tested with synthetic signals showing the ability to perform frequency and amplitude analysis.
Secondly, the limitations of the designed oscillator were considered and a new type of oscillator with a new model of inherent dynamic plasticity was formulated. This new model was also implemented into hardware and tested with synthetic and real biomedical signals such as EMG and ECG. The results obtained showed how the new model could successfully perform frequency and amplitude analysis in a noisy environment, and extract the frequency and amplitude components of very noisy input signals.

8.2 Future Research Directions

As part of future research, a number of worthy and interesting research challenges were identified:

1. The increase of automated postures for prosthetic hands with a single EMG signal.
2. Studies on ECG signals for the prevention of heart diseases.
3. Patient monitoring with non-linear oscillators.

The different aspects of these future research directions are described next.

8.2.1 The increase of automated postures for prosthetic hands with a single EMG signal

In section 4.6 we developed a new way of instantly controlling the postures of prosthetic hands with the use of dual EMG signals captured on the upper limb of the user. Consequently, the next challenge would consider the analysis of a single EMG for the "instant" control of prosthetic hands. Additionally, further studies could be conducted on capturing and analyzing EMG signals on higher levels of the upper limb to allow people with even higher level of amputations to be able to use prosthetic hands.

8.2.2 Studies on ECG signals for the prevention of heart diseases

In chapter 5 we presented a new methodology which was implemented in the analogue domain for the detection of heart beat anomalies. An interesting future research topic would involve further studies and analysis of ECG signals for the prevention of future heart beat diseases. Further mathematical algorithms could be implemented to observe whether there are different characteristics in ECG frequency and amplitude components which would allow doctors to predict heart beat anomalies.

8.2.3 Patient monitoring with non-linear oscillators

Biomedical signals such as respiratory movements, ECG, EMG and EEG signals are oscillatory signals which give information of the status of the user/patient. Therefore, it would be of interest to create a platform based on non-linear oscillators which would adapt to individual users/patients to collect their medical status.

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