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High Resistivity Czochralski-Silicon Using Deep Level Dopant Compensation For RF Passive Devices

by

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ABSTRACT

FACULTY OF PHYSICAL AND APPLIED SCIENCES

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HIGH RESISTIVITY CZOCHRALSKI-SILICON USING DEEP LEVEL DOPANT COMPENSATION FOR RF PASSIVE DEVICES

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Combinations of analytical and experimental results indicate that deep level doping of Czochralski grown silicon wafers is capable of providing very high resistivity wafers suitable for silicon-on-insulator (SOI), integrated passive devices (IPD) and 3D integration configurations.

Deep level doping involves adding trace elements to silicon that compensate for background free carriers introduced by impurities in the silicon and pin the Fermi level near the mid bandgap intrinsic level. Starting from n-type Czochralski-silicon wafers with a nominal resistivity of 50 Ωcm, gold ion implantation and subsequent annealing were used to increase the resistivity of silicon wafers by up to 3 orders of magnitude, to values as high as 93 kΩcm.

Hall measurements performed over a large temperature range show that the increase in resistivity is solely due to a decrease in carrier concentration and not a decrease in mobility. The carrier concentration is only one order of magnitude larger than that of intrinsic silicon over a temperature range of 200-360 K. Hall results also show that the resistivity of the compensated material remains up to two orders of magnitude larger than that of the uncompensated material at near operating temperatures.

High frequency attenuation measurements in the 1-67 GHz range for coplanar waveguides show attenuation reductions of up to 76% from 0.76 dB/mm to 0.18 dB/mm at 10 GHz for those fabricated on uncompensated and compensated silicon respectively. Spiral inductors fabricated on both compensated and uncompensated silicon show up to a factor of 10 increase in the maximum quality factor from 0.3 to 3.1 for inductors on uncompensated and compensated silicon respectively. A 70% increase in maximum quality factor from 9 to 15.2 is exhibited by inductors commercially fabricated on compensated silicon when compared to those on float-zone silicon.

The coplanar waveguide and spiral inductor results provide clear evidence that deep level dopant compensation is effective in improving the performance of passive devices in the GHz frequency range.

Contents

Declaration of Authorship

I, Ahmed Abuelgasim, declare that the thesis entitled 'High Resistivity Czochralski-Silicon Using Deep Level Dopant Compensation For RF Passive Devices', and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research.

I confirm that:

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List of Publications

A. Abuelgasim, K. Mallik, K. De Groot, P. Ashburn, D. M. Jordan, and P. R. Wilshaw, "High resistivity Czochralski-silicon using Deep Level Doping Compensation," in *2010 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, 2010.

K. Mallik, A. Abuelgasim, P. Ashburn, and K. De Groot, "Deep level dopant compensated Czochralski silicon substrates for MMICs," in *ARMMS RF & Microwave Society Conference*, 2010.

A. Abuelgasim, K. Mallik, P. Ashburn, D. M. Jordan, P. R. Wilshaw, R. J. Falster, and C. H. de Groot, "Reduced microwave attenuation in coplanar waveguides using deep level impurity compensated Czochralski-silicon substrates," *Semiconductor Science and Technology*, vol. 26, no. 7, Jul. 2011.

K. Mallik, A. Abuelgasim, P. Ashburn, C. H. de Groot, and P. R. Wilshaw, "Deep level impurity engineered semi-insulating CZ-silicon as microwave substrates," in *Microwave Integrated European Circuits Conference (EuMIC),* 2011, pp. 394-397.

A. Abuelgasim, K. Mallik, C. H. de Groot, and P. Ashburn, "Gold-doped high resistivity Czochralski-silicon for integrated passive devices and 3D integration," in *Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, 2011, pp. 363-366.

A. Abuelgasim, K. Mallik, P. Ashburn, and C. H. de Groot, "High resistivity Czochralski-silicon using a deep level dopant compensation process," in *International Conference on Micro and Nano Engineering (MNE)*, 2011.

A. Abuelgasim, K. Mallik, P. R. Wilshaw, P. Ashburn, and C. H. de Groot, "High resistivity Czochralski-silicon using a deep level dopant compensation process," in *Europe's Semiconductor Conference, Innovation in Advanced Manufacturing Processes (S2K)*, 2011.

A. Abuelgasim, K. Mallik, P. Ashburn, and C. H. De Groot, "Fabrication of low loss coplanar waveguides on gold-doped Czochralski-silicon," in *Society of Photo-Optical Instrumentation Engineers (SPIE) Conference Series*, 2011, vol. 8068, pp. 806811-806811-12.

A. Abuelgasim, K. Mallik, P. Ashburn, and C. H. de Groot, "High resistivity Czochralski-silicon using deep level dopant compensation," in *International Conference on Nanosciences & Nanotechnologies (NN12)*, 2012.

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Thank you all so much….

Ahmed Abuelgasim

And now the science…

Chapter 1

Introduction

The availability of low cost semiconductor technology is a necessity for the demanding modern cellular and wireless markets. The realisation of connectivity systems in a few integrated circuits with low external component count is the subject of a great deal of research academically and in industry. Typical GSM circuits are designed with a single radio frequency integrated circuit (RFIC) that includes most of the necessary sub-systems such as low-noise amplifiers, voltage controlled oscillators, mixers and low power transmit drivers [1]. A major problem associated with these ICs fabricated in silicon (Si) is the undesirable characteristics of the material operated at radio frequency (RF). Passive devices, in particular, fabricated on Si suffer from decreased performance and efficiency due to absorption of microwave power by background free carriers in the substrate, substrate coupling as well as cross-talk and transmission line loss. Passive components are known to greatly outnumber active devices on integrated circuits (ICs) and account for over a third of the cost, particularly in RFICs [2], so it is essential to address any factors affecting their performance on Si, before it can be accepted as a suitable substrate material for RFIC fabrication.

Solutions to these problems have in the past included the use of gallium-arsenide (GaAs) as an alternative to Si, due to its higher electron mobility and hence faster switching speeds. Si however is still preferred to GaAs as it is cheaper and has a native oxide. Other solutions

involving Si lie in the manipulation of Si substrates to reduce the background free carrier absorption. One such solution is the creation of high resistivity Si through a method known as deep level dopant compensation, which has been shown to greatly increase the resistivity of Si substrates thereby increasing the efficiency of passive devices fabricated on them.

In this work deep level doping is investigated as a method of increasing the resistivity of Si, and gold (Au) was found to be a great choice of material to achieve this. Deep level doping with Au was used to create high resistivity Si wafers, the properties of which were investigated using four-point probe, spreading resistance profiling and secondary ion mass spectroscopy techniques. Hall effect measurements were used to investigate the effects of deep level doping on the concentration and mobility of background carriers in the Si.

Coplanar waveguides and spiral inductors were chosen as the passive devices to be fabricated on the enhanced wafers in order to investigate any efficiency improvements brought about by the increased Si resistivity. ANSYS HFSS finite element simulations of spiral inductors were performed by Dr. Kanad Mallik, the results of which underpinned some of the decisions made in this work. These simulations, however, have not been included in this thesis. Passives were then fabricated and their RF performance on virgin and high resistivity Si (HRS) substrates were measured and compared. A number of iterations in the design and fabrication of these passives were performed particularly in relation to the development of the spiral inductors which proved to be a lengthy process due to the lack of ideal equipment in the Southampton Nanofabrication Centre where the devices were made. The methods and results of only the devices resulting from the iterations which gave the best results are hence reported.

The first chapter of this thesis covers deep level dopant compensation. Basic resistivity principles and measurement techniques are first explained before a critical review of various techniques that increase Si resistivity, as reported in literature, is given. The concept of deep level dopant compensation is then explained in detail including the use of Au as a deep level dopant. The methods used in this work to create HRS are next described before the results of this process are discussed.

The next chapter focuses on coplanar waveguides and their associated substrate related losses. General information about coplanar waveguide structure and attenuation related losses are given before a review of various methods of reducing attenuation as reported in literature. The design process is next explained before the fabrication process is detailed. The measured RF attenuation results are next included and discussed.

Chapter 4 begins with a basic description of spiral inductor geometry and a description of the major RF loss mechanisms. Inductor quality factor or efficiency is explained and then derived using several spiral inductor models, before different methods of increasing it are compared and critically reviewed. The design considerations of spiral inductors are then discussed after which quality factor frequency sweeps obtained from simulations are given. The fabrication process is finally detailed and RF measurements made are shown and discussed with reference to the simulated results.

Chapter 2

Increasing Silicon Resistivity Using Deep Level Dopant Compensation

Silicon grown by the Czochralski method is considered an excellent material for the fabrication of integrated circuits and the point has now been reached where devices based on this technology are capable of operating at frequencies approaching those of many III-V devices. A major remaining obstacle preventing the use of Czochralski-Silicon (Cz-Si) for RF applications lies in the fact that the performance of passive components fabricated on such substrates degrades when operated at RF due to absorption. This absorption is due to background free carriers in the Si and is therefore directly proportional to the conductivity of the substrate [3]; a fact that highlights the dependence of RFIC performance on substrate resistivity.

It is hence clear that high resistivity substrates are required for acceptable operation of passive RF integrated components to ensure device isolation thereby minimising undesirable effects. For these reasons the main aim of this work is the creation of high resistivity Si substrates through deep level dopant compensation. It is therefore important to first establish an understanding of the basic principles of resistivity and how it is measured.

2.1 Basic Principles of Resistivity

The resistance of a wire increases as the length of the wire increases and decreases as the cross-sectional area decreases, and depends on the material from which the wire is made. This dependence is known as the resistivity of the material and is the reciprocal of conductivity. In the context of a uniformly doped semiconductor bar, such as that shown in Figure 2.1, the resistance will increase if the length increases and decrease if the cross-sectional area increases. The resistance is also dependent upon the resistivity ρ of the semiconductor and can therefore be expressed as

$$R = \frac{\rho l}{A} \tag{2.1}$$

If an electric field E is applied to the semiconductor bar as shown in Figure 2.1 the electrons begin to move at a velocity known as the electron drift velocity v_n. This is the average velocity of the electron due to the field and depends on the electron mobility μ_n or the ease at which electrons can move through the material, and can hence be expressed as [4]

$$v_n = -\mu_n E \tag{2.2}$$

Similarly, using the hole mobility μ_p, the hole drift velocity can be obtained as

$$v_p = \mu_p E \tag{2.3}$$

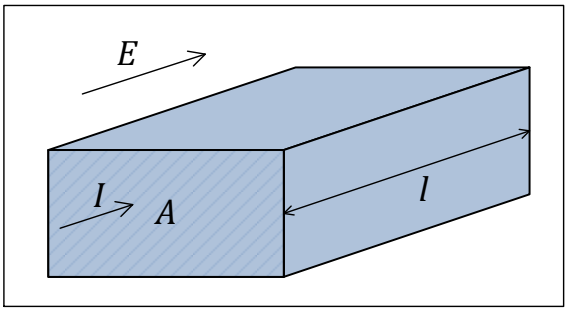

Figure 2.1 – A uniformly doped semiconductor bar of length l and cross-sectional area A with current I passing through it.

These drift velocities give rise to a drift current through the semiconductor bar. The electron current density of this drift current is the product of the electron drift velocity and the charge $-q$ of each electron and is given by [4]

$$J_n = \frac{I_n}{A} = -qnv_n = qn\mu_n E \tag{2.4}$$

The hole current density can similarly be calculated by

$$J_p = qp\mu_p E \tag{2.5}$$

where n and p are the electron and hole concentrations respectively. The total current density due to the applied force is the sum of the electron and hole current densities giving

$$J = J_n + J_p = q\left(n\mu_n + p\mu_p\right)E \tag{2.6}$$

however it is more commonly expressed using the conductivity of the material σ as [5]

$$J = \sigma E \tag{2.7}$$

The resistivity ρ of a semiconductor is the reciprocal of the conductivity and using equations (2.6) and (2.7) can be therefore be expressed as

$$\rho = \frac{1}{q\left(n\mu_n + p\mu_p\right)} \tag{2.8}$$

In extrinsic semiconductors there is a large difference between the concentrations of electrons and holes and one component dominates equation (2.8). For n-type semiconductors n is significantly larger than p and therefore equation (2.8) can be simplified to

$$\rho = \frac{1}{qn\mu_n} \tag{2.9}$$

and for a p-type semiconductor $p >> n$, therefore

$$\rho = \frac{1}{qp\mu_p} \tag{2.10}$$

2.2 Resistivity Measurement Techniques

A simple and common method of measuring resistivity is the four-point probe technique in which four equally spaced in-line probes are used. A small current is passed through the outer two probes while the voltage between the two inner probes is measured. The current and voltage values are then used to calculate the resistance of the surface of the material, or sheet resistance, which can be multiplied by the sample thickness to obtain the resistivity.

Another method of measuring resistivity is spreading resistance profiling (SRP) [6], where a small voltage is applied across two small probes on the surface of the material and used to measure the resistance and thus determine the resistivity. The probe to material resistance is negligible as there is a good contact between the two. The main benefit of SRP is that it can be used to determine the resistivity depth profile of semiconductor materials by beveling the sample and stepping the probes down the angled face.

Hall effect measurements can also be used to determine the resistivity of a material. The Hall effect is a consequence of the forces exerted on moving charges by electric and magnetic fields and is used to determine the type of majority carrier in a semiconductor, as well as to determine the majority carrier concentration and mobility. Using these values and equation (2.9) or (2.10) the resistivity can be calculated, depending on the type of majority carrier. The Hall effect relies on the fact that a charged particle moving in a magnetic field will experience a force perpendicular to both the direction of motion and that of the magnetic field.

This force, known as the Lorentz force, is a cross product of the magnetic field B and drift velocity vectors, and is given by [7]

$$F_y = q(v_x B_z) \tag{2.11}$$

The steady state behaviour of an n-type semiconductor sample with a voltage applied across the x-axis and a magnetic field applied across the z-axis is shown in Figure 2.2. The Lorentz force, acting in the y-direction, will cause electrons travelling in the x-direction to move and accumulate at the right hand side of sample. This in turn leads to an electric field E_y known as the Hall field directed towards the right hand side of the sample, which produces a force on the electrons that eventually balances out the Lorentz force. At this point no net force acts upon the electrons in the y-direction and this relationship, using $F = qE$ [8] and equation (2.11), can be expressed as

$$qE_y = q(v_x B_z) \tag{2.12}$$

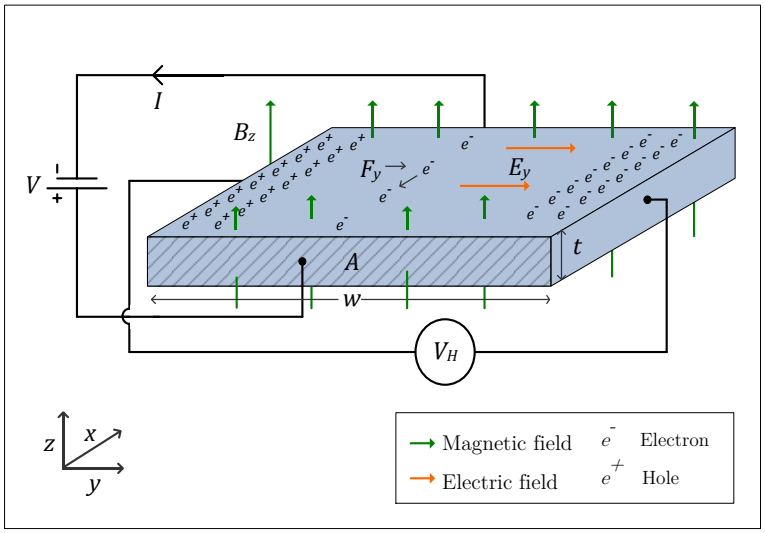

Figure 2.2 -–Steady state behaviour of an n-type semiconductor in a magnetic field B_z with applied voltage V, illustrating the Hall effect.

Using equations (2.4) and (2.12) the Hall field can be expressed as

$$E_y = -\frac{J_n B_z}{qn} \tag{2.13}$$

It is the establishment of the Hall field that is termed the Hall effect and leads to a Hall voltage in the y-direction which, using width w and $V = -Ed$ [9] where d is the distance between the two opposite charges, can be derived as

$$V_H = -E_y w \tag{2.14}$$

In equation (2.13) $-1/qn$ is termed the Hall coefficient and for p-type semiconductors it is $1/qp$. The Hall coefficient is used to determine the type of majority carrier as it is negative and positive for n-type and p-type semiconductors respectively. Using equations (2.13) and (2.14) the majority carrier concentration of n-type semiconductors can also be obtained as

$$n = \frac{J_n B_z w}{q(V_H)} = \frac{(I/A)B_z w}{qV_H} = \frac{IB_z}{qV_H t} \tag{2.15}$$

in which A and t are the cross-sectional area and sample thickness respectively as previously shown in Figure 2.2. Similarly the carrier concentration of p-type semiconductors can be expressed as

$$p = \frac{IB_z}{qV_H t} \tag{2.16}$$

When performing Hall effect measurements on thin samples, I and B_z are set while V_H is measured using a technique known as the van der Pauw method [10]. This involves setting up contacts as illustrated in Figure 2.3 (a), where I is fed from contact 3 to contact 4, while V_H is measured across contacts 1 and 2. When performing van der Pauw measurements the best results are obtained with ohmic contacts, achieved by creating metal contacts atop the semiconductor. The van der Pauw method can also be used to measure the sheet resistance of the semiconductor, which can be used to calculate the resistivity. To achieve this, current is fed through two adjacent contacts such as from contact 2 to contact 3, while the voltage drop

across the other two contacts is measured, as shown in Figure 2.3 (b). The resulting resistance can then be calculated using Ohm's law to give $R_{41,23} = V_{41}/I_{23}$. The same is repeated but with the current flowing between contacts 1 and 3, and the voltage measured across contacts 2 and 4, as in Figure 2.3 (c), to give resistance $R_{24,13}$. These voltages and currents are then used to calculate the resistivity using [11]

$$\rho = \frac{\pi t\left(R_{24,13} + R_{41,23}\right) f}{2 \ln 2} \tag{2.17}$$

where f depends on the ratio $R_{24,13}/R_{41,23}$. The mobility of the majority carriers can be obtained using this calculated resistivity and equation (2.9) or (2.10) depending on the type of majority carrier.

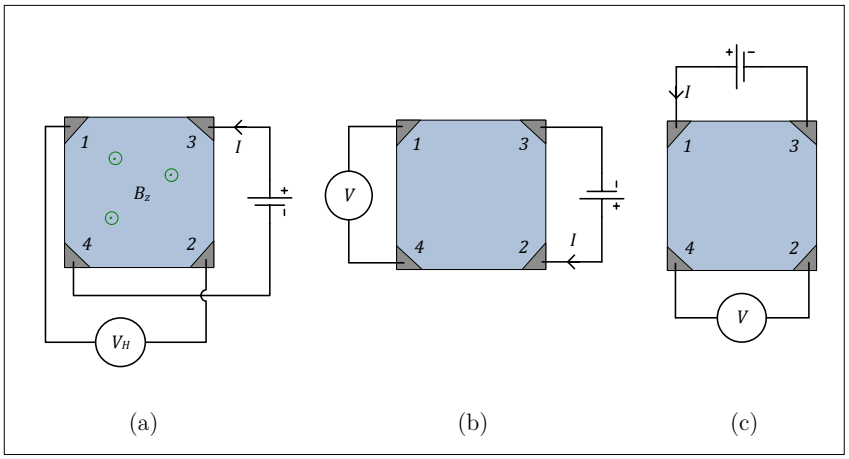

Figure 2.3 - The van der Pauw technique as it is used to measure (a) the Hall coefficient and (b) and (c) the resistivity of a small, thin semiconductor sample.

2.3 Increasing the Resistivity of Czochralski-Silicon

In III-V semiconductors, such as GaAs, high resistivity substrates can be easily produced because of the wide band-gap which makes it an ideal material for RF passive device operation. Thermal stability of these substrates however is a problem which, coupled with the lack of a native oxide, are reasons why Si is still considered a superior alternative [3].

Pure Si with no impurities is known as intrinsic Si and has the highest achievable Si resistivity of 500 kΩcm [12]. The most common crystal growth technique is the Czochralski method which involves melting Si in a boron nitride or quartz crucible before specific concentrations of boron (B) or phosphorus (P) are added to dope the Si giving it a desired resistivity. The crucible thus becomes contaminated with B and P, among other impurities, which make it extremely difficult to produce Si with a background, free carrier concentration below 10^{13} cm^{-3}. This concentration is equivalent to resistivities of approximately 400 Ωcm for n-type and 1 kΩcm for p-type Si at room temperature and is very low when compared to the intrinsic resistivity of Si. Therefore standard Cz-Si wafers are normally only produced with resistivities less than 100 Ωcm, with typical values of 10 Ωcm [13]. For this reason there has been a great deal of research into different methods of producing high resistivity Si substrates.

The development of wafer bonding techniques and the emergence of silicon-on-insulator (SOI) technology provide opportunities to create high resistivity substrates beneath the active Si wafer with an insulation layer, typically Silicon-dioxide (SiO_2), in between. Examples include the silicon-on-anything (SOA) approach which is capable of producing high resistivity substrates by bonding a thin, active Si wafer to a substrate of any material such as quartz or glass. However, the physical and thermal properties of such materials are responsible for a high thermal resistance leading to self-heating and thermal runaway of devices fabricated on these wafers [14]. Silicon-on-sapphire is one example that can be created at low temperatures, but due to the lattice mismatch crystallographic defects are a major problem. IC processing can also degrade material quality further as the thermal expansion coefficient of sapphire is much greater than that of Si, which makes this solution unsuitable for RFIC fabrication [15].

Due to these disadvantages there is a large interest in increasing the resistivity of Cz-Si substrates to improve the performance of passive devices fabricated on them.

For operation of Cz-Si substrates indistinguishable from GaAs substrates, it has been shown that a resistivity of at least 5 kΩcm is required for low absorption loss at frequencies greater than a few hundred MHz [16]. These resistivities can be realised using a high purity alternative to Cz-Si known as float-zone. Float-zone Si (FZ-Si) substrates with resistivities as high as 10 kΩcm have been created in the past [17]. HiRes™ is another form of high purity Si developed by Topsil Semiconductor Materials that can achieve resistivities of up to 30 kΩcm [18]. Nevertheless the main disadvantage of FZ-Si and HiRes substrates is the price as well as the fact that the maximum diameter is limited to 8 inches due to surface tension limitations during growth [18–20]. Hence this process is unsuitable for modern VLSI technology where the standard wafer diameter is 12 inches.

An alternate way of reducing substrate absorption is to remove parts of the substrate itself from under the passives in a process known as micromachining. In one such technique the Si under the passive devices is removed by bonding the wafer, top down, to a glass substrate and removing Si by a wet etch process [21]. Wet etches have also been used to selectively remove Si under the passives, leading to localised reduction of substrate losses [22], [23]. These solutions however lead to increased fabrication complexity as well as an increased cost, and have yet to prove process compatibility and yieldability [13]. For these reason increasing the resistivity of Cz-Si is of greater benefit. A large amount of research has been undertaken in this area and a few examples are mentioned as follows, with details summarised in Table 2.1.

A method for creating a HRS layer was patented by Aoki *et al.* in which an oxygen or nitrogen ion beam is implanted into amorphous, polycrystalline or single crystal Si [24]. The ions are implanted with an energy of 200 keV and doses of 3-7x10^{17} cm^{-2} before the substrate is annealed to activate the ions which increase the resistivity of the substrate to between 10^{7} Ωcm and 10^{11} Ωcm. A similar technique was used by Dehan *et al.* in which high resistivity polycrystalline Si (SIPOS) films were created by the pyrolysis of disilane and nitrous oxide in a

LPCVD chamber [25]. Resistivities of 10^9 - 10^{13} Ωcm can be achieved depending on the oxygen concentration. However, large negative substrate bias voltages produce intense electric fields inside the SIPOS film that induce the emission of free electrons, and in turn increase the conductivity of the material [26]. Similarly a high resistivity silicon-on-defect layer was produced by implanting protons into n-type Cz-Si samples, of initial resistivity 8 Ωcm, with an energy of 180 keV and a dose of 2.5×10^{16} cm^{-2} [27]. The samples were then annealed in a N_2 atmosphere by a rapid thermal anneal (RTA) at 900°C for 10 seconds, followed by furnace annealing at 1180°C for 1 hour. During the first anneal the protons form gas "bubbles" causing structural defects around them thereby forming a buried defect layer in Si that effectively traps free carriers and increases the resistivity up to 1 kΩcm.

Proton implantation was used in another instance to achieve a resistivity of 0.1 MΩcm [28]. In this case the wafers were implanted with a fixed dose of 10^{15} cm^{-2} at an energy of 17.4 MeV in six steps by changing the thickness of an aluminium (Al) absorber in order to provide a uniform proton profile throughout the entire depth of the Si substrate. Wu *et al.* also used proton implantation as well as As^+ ion implantation to increase the resistivity of conventional Si and Si-on-quartz (SOQ) substrates, respectively [29]. The implantation was performed with a dose of 10^{16} cm^{-2} and proton implantation energy of 10 MeV was required to give an implantation depth of 698 μm and hence penetrate the entire Si wafer. The resistivity was increased from 10 Ωcm to values as high as 36 kΩcm using As^+ ions and 1.6 MΩcm using protons. In another instance HRS was created also using proton implantation on p-type Si wafers, to increase the resistivity to 1 MΩcm [30]. The hydrogen ions were implanted with 30 MeV and doses 1×10^{16} cm^{-2} through 8 stacked 4 inch wafers. In a similar approach Si_{28} ions were systematically implanted into conventional low resistivity Si substrates, in a multi-implantation approach, to damage the lattice structure and form an amorphous layer on the surface of Si leading to improved microwave performance [31]. The disadvantage of these implantation techniques lies in the fact that they rely on creating defects in Si which make the material unsuitable for devices that require single crystal Si, rendering the techniques incompatible with modern VLSI technology. Some of the implantation methods also require multi-implantations, wafer stacking arrangements or very high energies to create thick high

resistivity layers; requirements that add to the complexity and cost of VLSI processes. For these reasons there is a need to develop other methods of increasing the resistivity of Si.

An alternative method is to create HRS using a technique known as deep level dopant compensation in which the effects of background free carriers are compensated for by implanted dopant atoms, reducing the carrier concentration thus increasing the resistivity of Cz-Si. This technique was used to implant manganese into Cz-Si with a dose of 10^{14} cm^{-2} at 100 keV, followed by a RTA at 800°C for 36 seconds, and enhanced the resistivity of Cz-Si from 600 Ωcm to 10 kΩcm [16]. As mentioned this resistivity is high enough to give RF behaviour indistinguishable from that of GaAs. Deep level doping was also used by Wang *et al.* to create HRS by diffusing Au into Cz-Si [15]. In this example Au was introduced into the Si wafer by diffusion from an evaporated Au layer during an anneal in an inert ambient. A subsequent RTA provided a high temperature step used to activate the Au and increase the resistivity to a value as high as 100 kΩcm. The research however does not address the effect of this increased resistivity on RF passive devices. It is clear from this research that deep level dopant compensation is a very promising technique that can be used to increase the resistivity of Cz-Si in a process that is in theory compatible with modern VLSI techniques, and therefore a study of the theory behind deep level dopant compensation follows.

TABLE 2.1
A summary of various techniques for creating high resistivity Si, as reported in literature, highlighting the resulting resistivities.

Description	Materials used	Implantation		Anneal	Initial Resistivity (Ωcm)	Enhanced Resistivity (Ωcm)
		Dose (cm^{-2})	Energy (eV)			
Implantation of oxygen or nitrogen ions before annealing in furnace [24]	O^+ or N^+	3-7x10^{17}	200 k	-	-	10^7 - 10^{11}
Pyrolysis of Si_2H_6 and N_2O by LPCVD to form doped high resistivity poly-Si [25]	Si_2H_6 and N_2O	-	-	-	-	10^9 - 10^{13}
Proton implantation before rapid thermal and furnace anneals [27]	H^+	2.5x10^{16}	180 k	910°C, 10s; 1180°C, 1hr	8	10^3
Proton implantation (6 steps) [28]	H^+	10^{15}	17.4 M	-	10	10^5
Proton implantation in Si and As^+ implantation in Si-on-quartz [29]	H^+	10^{16}	10 M	-	10	10^6
	As^+		-			36 k
Proton implantation for local high resistivity region [30]	H^+	10^{16}	30 M	-	1	10^6
Si_{28} ion multi-implantation [31]	Si_{28}^+	3x$10^9$$cm^{-3}$	200 k	-	5 - 10	-
Deep level doping by Mn implantation before RTA [16]	Mn	10^{14}	100 k	800°C, 36s	600	10^4
Deep level doping by Au diffusion using two step anneal [15]	Au	-	-	1000°C (RTA)	-	10^5 (5k @ 80°C)

2.4 Deep Level Dopant Compensation

Impurities introduced during the Czochralski crystal growth process often present themselves as dopant atoms which, depending on the impurity, act as donors, acceptors or both. Dopant atoms that introduce electrons are known as donors, those introducing holes are acceptors, while codopants introduce both. Given sufficient energy an electron from an introduced donor atom can break its bond and "jump" into the conduction band to become electrically active or ionised, rendering the material n-type. The same is true for holes jumping into the valence band rendering the intrinsic material p-type. Ionised electrons and holes are free to travel through the lattice thus contributing to the background free carrier concentration and reducing the resistivity. The energy required to ionise electrons or holes of a dopant material is known as the ionisation energy and varies from one dopant to another as can be seen in Figure 2.4. For the purposes of simplicity from this point onwards impurity dopants will be referred to as impurities and the compensating material as dopants.

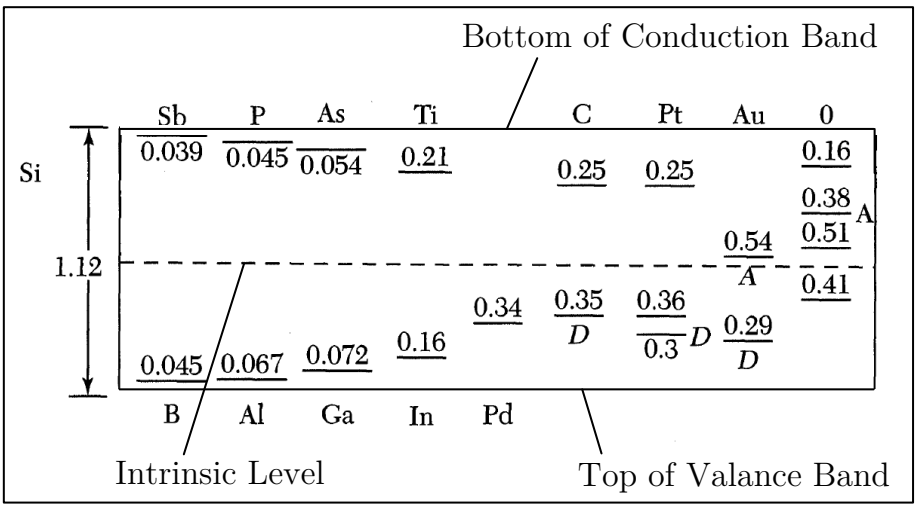

Figure 2.4 - Ionisation energy levels (in eV) of elements in Si at room temperature. Levels above the intrinsic level are measured from the bottom of the conduction band and are donor levels unless indicated by *A*. Those below the intrinsic level are measured from the top of the valence band and are acceptor levels unless indicated by *D*. [32]

The resistivity reducing effects of impurities can be compensated for by deliberately adding donors or acceptors to the Si thus increasing the resistivity to its intrinsic maximum value. This resistivity increasing process is known as dopant compensation.

The resistivity of a Si sample resulting from the introduction of a specific concentration of dopant used to compensate for a known impurity concentration can be determined using the energy levels of the dopants and the methods used by Mallik *et al.* [3]. This technique can be applied to both p-type and n-type Si and involves solving the charge neutrality equation [32]

$$p + \sum_i N_{D_i}^+ - n - \sum_j N_{A_j}^- = 0 \tag{2.18}$$

in which $N_{D_i}^+$ and $N_{A_j}^-$ are the ith and jth ionised donor and acceptor concentrations respectively, resulting from all impurities and compensating dopants. These are given by [3]

$$N_{D_i}^+ = N_{D_i}\left(1 + 2e^{\left(E_F - E_{D_i}\right)/kT}\right)^{-1} \tag{2.19}$$

and

$$N_{A_j}^- = N_{A_j}\left(1 + 4e^{\left(E_{A_j} - E_F\right)/kT}\right)^{-1} \tag{2.20}$$

where $E_{D_i}$and E_{A_j} are the ith and jth donor and acceptor ionisation energy levels respectively, k is the Boltzmann constant and T is the temperature in Kelvin. E_F represents the energy level at which the probability of occupation by an electron is ½ and is known as the Fermi energy level. For intrinsic Si at room temperature almost all the electrons sit in the valence band so the probability of finding an electron is almost unity. This means that the energy level at which the probability of finding an electron is ½ is at the middle of the bandgap, which is known as the intrinsic energy level. Therefore the Fermi level of intrinsic Si is at the mid-bandgap level and its resistivity is the maximum achievable for Si as there are almost no free electrons in the conduction band. Dopant donors make the Si extrinsic by introducing

electrons at the ionisation energy levels of the doping material in Si. This increases the probability of finding an electron near the conduction band and in turn shifts the Fermi level away from the mid-bandgap level and closer to the conduction band. Similarly dopant acceptors shift the Fermi level closer to the valence band.

In equation (2.18) the free electron and hole concentrations are represented by n and p respectively and are given by [32]

$$n = N_C e^{-(E_C - E_F)/kT} \tag{2.21}$$

and

$$p = N_V e^{-(E_F - E_V)/kT} \tag{2.22}$$

where E_C and E_V are the energy levels of the conduction and valance bands respectively. The absolute energy level values are not important as the dopant ionisation energy levels are given as values relative to the two bands. Therefore setting E_V to 0 eV gives E_C a value equal to the bandgap of Si, which is 1.12 eV at room temperature. The effective density of states of the conduction and valence bands are represented by N_C and N_V respectively, which for Si are $2.8\text{x}10^{19}$ cm^{-3} and $1.04\text{x}10^{19}$ cm^{-3} at room temperature [33]. It is clear from equations (2.19) - (2.22) that E_F is a factor in all the components in the charge neutrality equation. Therefore in order to solve it, E_F is iteratively varied until the equation is balanced. Once solved the values for n and p are used to obtain the resistivity ρ of the compensated Si using equation (2.8).

This technique was used to calculate the resistivity at room temperature of B-doped p-type Si as a function of compensating donor concentration, for donors with ionisation energy positions below the conduction band in the range of 0.045 eV - 1 eV. The resulting plot is included in Figure 2.5 shows that the resistivity increases as the dopant concentration increases. Increasing the dopant concentration increases the concentration of ionised donors which begin to compensate for the background B thus increasing the resistivity until a maximum is reached when the ionised donor concentration exactly matches the B concentration. At this point the Fermi level is at the mid-bandgap position and the Si is intrinsic.

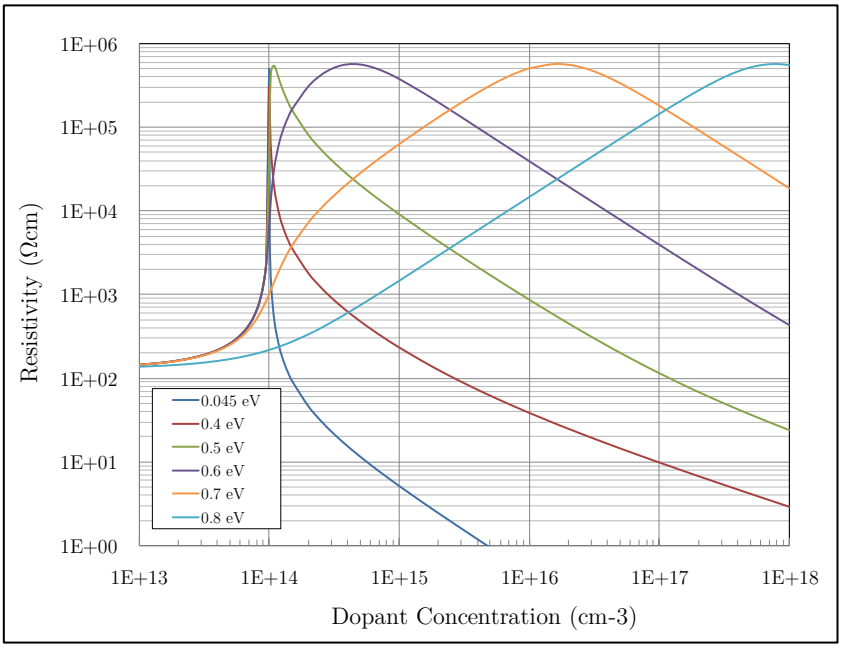

Figure 2.5 - Calculated resistivity of p-type Si with a B concentration of 10^{14} cm^{-3}, doped with generic donors with different ionisation energy levels, as a function of generic dopant concentration.

Increasing the donor concentration further, however, leads to a reduction in the resistivity due to over-compensation as the excess ionised donors render the material n-type. This is the basic principle of dopant compensation and holds true for n-type samples with dopant acceptors. Dopants with low ionisation energies introduce electrons or holes loosely bound to their host atoms, so at room temperature only a small amount of energy is required to ionise them. These types of dopants are known as shallow level dopants owing to the "depth" of their energy levels in the Si bandgap. The shallower the dopant, the higher the concentration of ionised donors at room temperature.

This explains why the peak resistivity ranges for shallower dopants in Figure 2.5, is much narrower than those for deeper dopants since more donors are ionised and contribute in the compensation process. In theory dopant compensation is possible with shallow level dopants but only with concentrations very close to the impurity concentration. The shallow level dopant concentration must therefore be tightly controlled to an extent that is not practically

possible, which rules out the use of shallow dopants P and B to compensate n-type and p-type Si respectively. Conversely for deep level dopants only a small fraction of donors or acceptors are ionised at room temperature and take part in the compensation. Therefore the increase in ionised donor concentration is gradual with increasing dopant concentration as is the resistivity change, leading to a larger peak resistivity range. Doping Si with deep level dopants to increase resistivity is known as deep level dopant compensation and is a much more practical and achievable option as there is no need to tightly control the dopant concentrations. Doping with deep level acceptors has another vital advantage over shallow level doping in that deep level doped materials are resistant to the effects of thermal donors which are oxygen precipitate related, shallow level impurities in Cz-Si. Thermal donors reduce the resistivity of n-type Cz-Si drastically after short anneals around 500°C [34]. Deep level acceptors can therefore compensate for the effects of P in n-type Si and thermal donors.

A drawback with deep level doping, however, is that relatively large concentrations are required to reach the resistivity peak, which can only be achieved when the solubility of the dopant in Si is high. Also although the effects are much more severe for shallow dopants, over-compensation is a problem still faced by deep dopants. This limits the usefulness of materials that introduce only deep donors or deep acceptors. There exist, however, materials that introduce pairs of donors and acceptors into Si and it has been shown that doping with large concentrations of these materials does not lead to overcompensation [3]. Au has been found to introduce an equal concentration of deep donors and acceptors at energy levels close the intrinsic level [35] as can be seen in Figure 2.4. Au also has a very high solubility in Si and its diffusive and electrical properties in Si are well studied [36–38]. These properties make Au an excellent candidate for deep level doping of Cz-Si, and for these reasons the compensating behaviour of Au in Si is discussed as follows.

2.5 Gold as a Deep Level Dopant

Au introduces both a donor and an acceptor level in Si with deep ionisation energies making it a deep level codopant as can be seen in Figure 2.4. For codopants that introduce a single pair of energy levels the ionised donor and acceptor concentrations are given by [3]

$$N_D^+ = N_D\left(1 + 2e^{(E_F - E_D)/kT} + e^{(2E_F - E_A - E_D)/kT}\right)^{-1} \tag{2.23}$$

and

$$N_A^- = N_A\left(1 + 2e^{(E_A - E_F)/kT} + e^{(E_A + E_D - 2E_F)/kT}\right)^{-1} \tag{2.24}$$

It has been reported that the position of the Fermi level in Si determines the type of active levels, i.e. only the acceptor level is active in n-type material and only the donor level in p-type material [36]. For this reason Au can compensate for both electrons and holes and can therefore be used for p-type and n-type Si which is a major advantage over dopants that only introduce either donors or acceptors. To confirm this, the resistivity at room temperature of p-type and n-type Si doped with Au as a function of Au concentration was calculated and the results are plotted in Figure 2.6 and Figure 2.7 respectively. It is clear from these graphs that not only can Au compensate for both n-type and p-type Si but for both types of Si it is not necessary to tightly control the concentration as it does not lead to overcompensation. It is also evident that for n-type compensation a much smaller Au concentration is required to achieve maximum resistivity.

Au atoms introduced into a Si substrate must take up substitutional sites in the lattice in order to contribute to any resistivity increase. Au diffusion in Si is known to occur by the kick-out mechanism in which each Au atom diffuses rapidly by interstitial diffusion through the lattice interstitials towards the edges of the substrate until it 'kicks out' a Si atom from its lattice site and takes its position as a substitutional atom, leading to a Si self-interstitial [39].

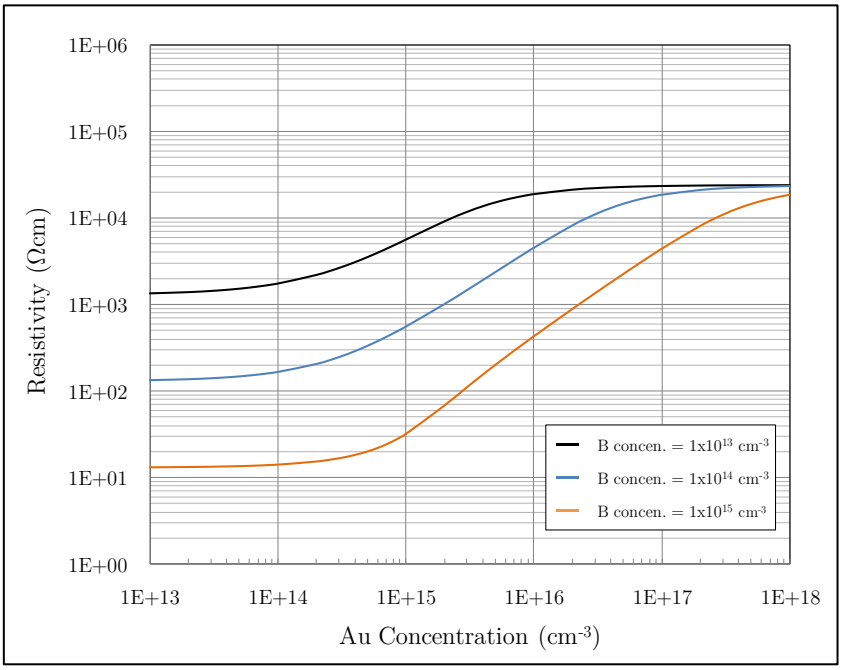

Figure 2.6 - Calculated resistivity of p-type Si with different B concentrations at room temperature as a function of Au concentration.

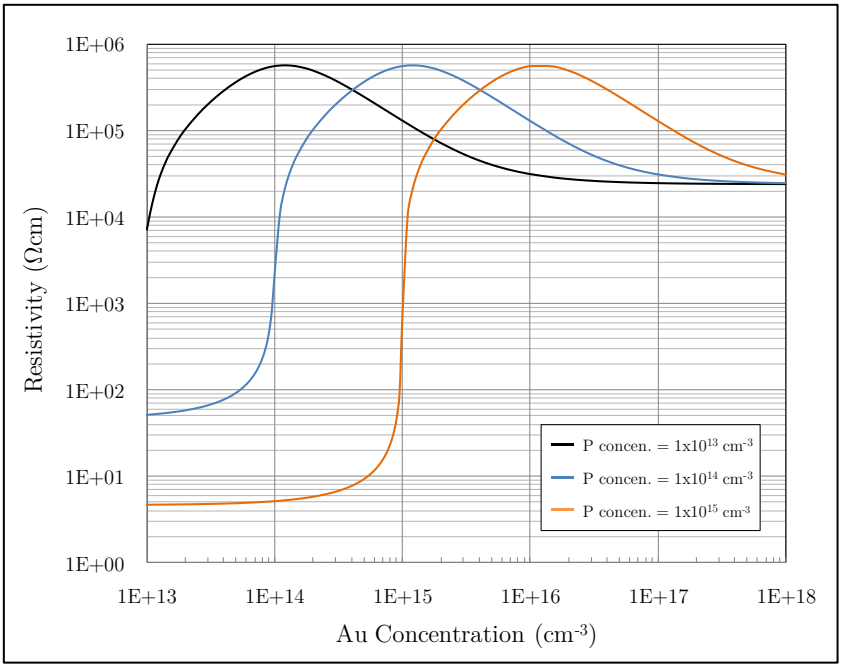

Figure 2.7 - Calculated resistivity of n-type Si with different P concentrations at room temperature as a function of Au concentration.

Due to the initial rapid interstitial diffusion the Au surface concentration is much higher than that in the bulk leading to a U-shaped Au concentration depth profile as can be seen in Figure 2.8 [40]. This translates to a U-shaped resistivity profile with maximum resistivity at the edges of the substrate. At higher temperatures the Au atoms have more energy thus the rate of exchange between interstitial and substitutional states of Au atoms increases and the solubility of Au in Si therefore increases with increasing temperature. The solubility of Au in Si has been calculated using thermodynamic data and a Au/Si phase diagram, in [40], and the results are shown in Figure 2.9. This graph was used to calculate the temperature the Si wafer must reach to introduce a required concentration of Au. One problem with using Au in Si is that Au is known as a device killer and would prevent the operation of active devices fabricated in the material. The U-shaped resistivity profile of Au-doped Si allows for implantation of Au into the handle wafer of SOI wafers through the back which would lead to the highest resistivity along the edges of the handle wafer and therefore directly below the active wafer, provided that the buried oxide prevents Au from diffusing into the active wafer.

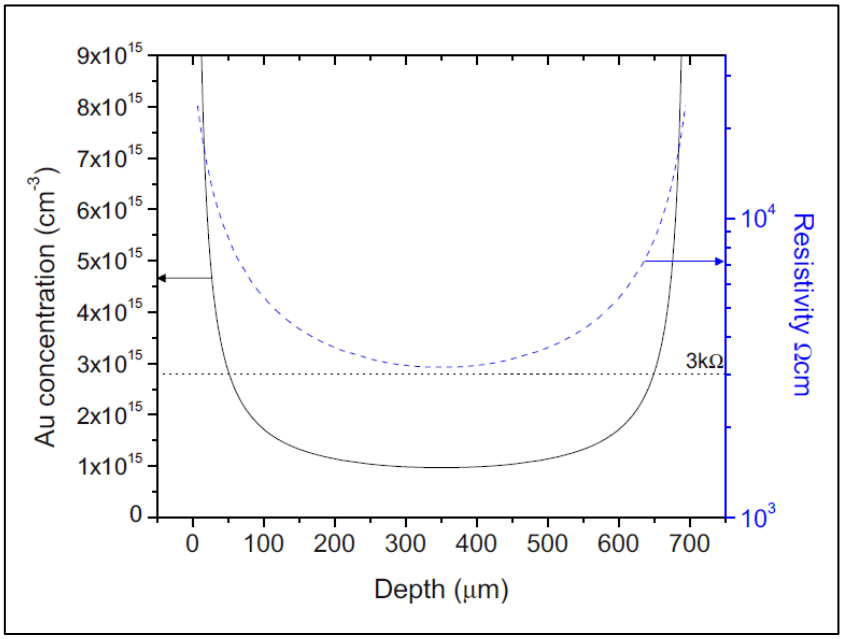

Figure 2.8 - Calculated Au concentration and resistivity as a function of depth, after a 40 minute anneal at 1050°C of a p-type Cz-Si wafer, illustrating U-shaped Au concentration and resistivity profiles [40].

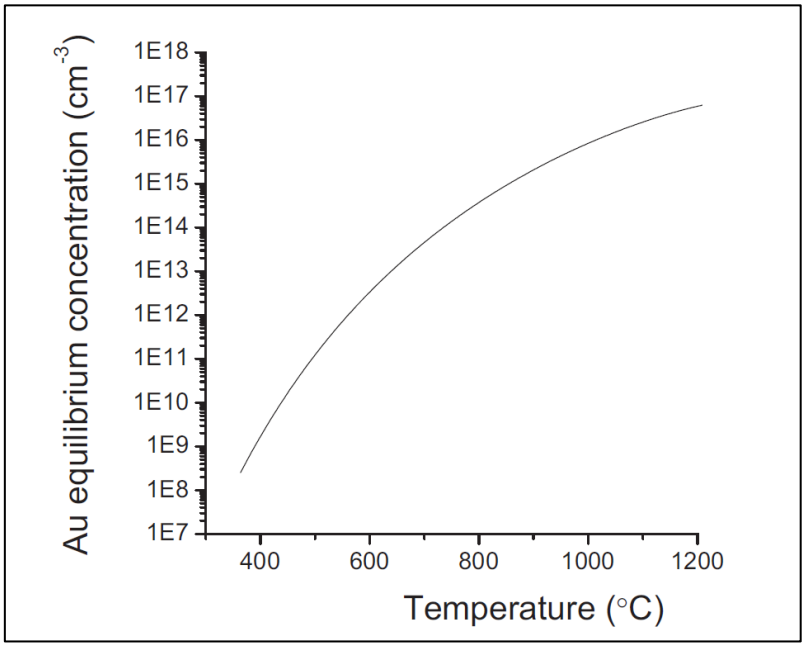

Figure 2.9 - Solubility of Au in Si as a function of temperature, calculated using thermodynamic data and a Au/Si phase diagram [40].

This ensures that any passives fabricated on the active wafer benefit from a high resistivity substrate underneath. The same principle can be applied with integrated passive device (IPD) and 3D integration technologies. In 3D integration, highly integrated systems can be created by vertically stacking various materials, technologies and functional components and making connection using Si vias. Using these technologies the passive device substrate does not come in direct contact with any active devices and fear of contamination is alleviated. It is hence possible to make use of deep level dopant compensation with Au to improve passive device characteristics and combine this with the advantages of minimizing size and reducing wiring.

For these reason Au was used as the material of choice for increasing the resistivity of Si through deep level dopant compensation in this work. Unlike with previous attempts [15] in this work Au was introduced into wafers by ion implantation as it is more practical than diffusion and allows greater control over concentration. The implanted Cz-Si wafers were then subjected to different temperature anneals that allow Au atoms to take up substitutional sites, leading to a resistivity increase. Coplanar waveguides and spiral inductors were then

fabricated onto these wafers and their microwave performance measured to investigate the effects that an increased resistivity has on passives devices. It was therefore important to develop an understanding of these devices and studies of both follow in the next chapters.

2.6 Creating High Resistivity Silicon through Gold Doping

The starting wafers chosen were 6 inch, P-doped, n-type <100> Cz-Si wafers, with an average thickness of 625 μm from MEMC Electronic Materials Inc. An average wafer resistivity of 56 Ωcm was calculated by measuring the sheet resistance at multiple points on the wafer surface using a Jandel RM3-AR four-point prober and then multiplying the average sheet resistance by the thickness. The wafers were chosen as n-type to investigate if the detrimental effects that thermal donors have on the resistivity of such wafers can be avoided by using deep level doping. As mentioned earlier, thermal donors can cause the resistivity of n-type Cz-Si to decrease at temperatures above 500°C. Since they can be considered n-type shallow donors they should theoretically be compensated for by deep level dopants. After a one hour anneal at 550°C, the resistivity of a sample of the wafers decreased from 56 Ωcm to 26 Ωcm, as measured using a four-point probe (FPP) technique, which amounts to a decrease of almost 50%. This is the temperature at which back-end alloy anneals are typically performed so for deep level doping to be compatible with VLSI fabrication techniques, the concentration of deep level dopants introduced into n-type Cz-Si must be sufficient enough to compensate for the background P concentration as well as any thermal donors introduced during back-end processing. In other words the enhanced resistivity of the Cz-Si must at least be higher than 5 kΩcm after the effects of thermal donors for RF performance indistinguishable from that of GaAs substrates [16].

To investigate this requirement the resistivity of n-type Si at room temperature was calculated as a function of P and thermal donor concentrations for Au doping concentrations of $1x10^{14}$ cm^{-3}, $2x10^{14}$ cm^{-3}, $4x10^{14}$ cm^{-3} and $8x10^{14}$ cm^{-3}, using the methods described in the work of Mallik *et al.* [3]. Figure 2.10 shows the results of these calculations including the measured

resistivity of the Si sample before and after the thermal donor anneal. The blue band represents the effects the thermal donors have on the resistivity of a Cz-Si wafer with an initial resistivity of 54 Ωcm, as mentioned earlier. For deep level compensation to be resistant to thermal donor effects the enhanced Si resistivity must remain higher than 5 kΩcm even after the increase in n-type dopants caused by thermal donor activation, i.e. the resistivity must not decrease below this value within the blue band. It is therefore clear from this graph that for Au concentrations above $2x10^{14}$ cm^{-3} the resistivity should be relatively stable at values greater than 10 kΩcm, even after the degrading effects of the thermal donors.

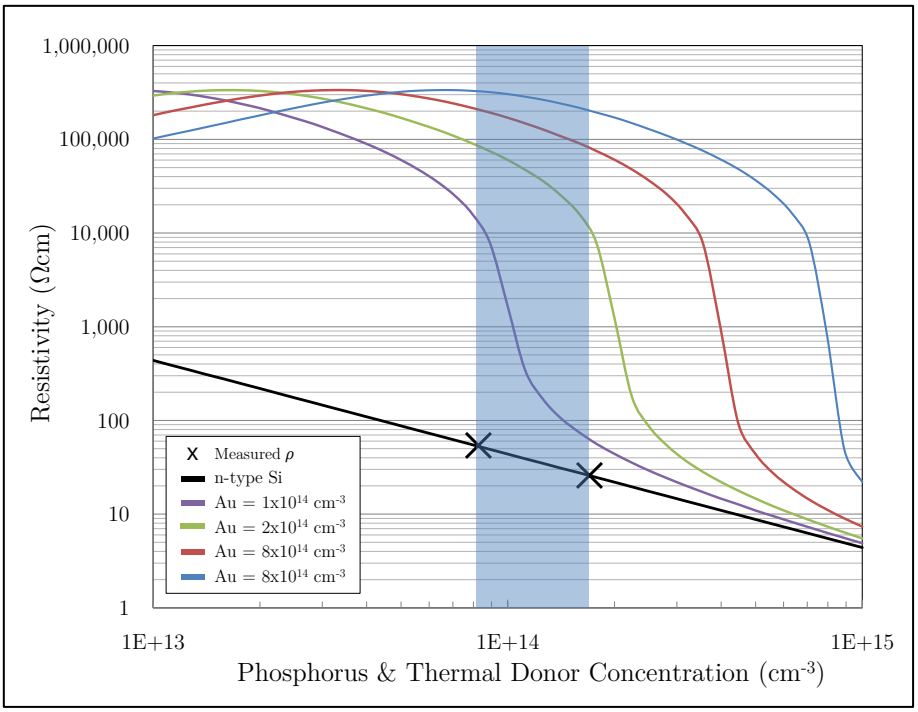

Figure 2.10 - Si resistivity as a function of phosphorous and thermal donor concentration, with different Au concentrations. Measured resistivities of a Si sample before and after a 550^{O}C anneal are also displayed (crosses). The blue band represents the drop in resistivity caused by thermal donors.

Ion implantation was chosen as the preferred method for introducing Au into the Si wafers as greater control over the dopant concentration is achievable in comparison to diffusion methods such as those used in [15] and [40]. Using the results in Figure 2.10, Au concentrations of $2x10^{14}$ cm^{-3}, $4x10^{14}$ cm^{-3} and $8x10^{14}$ cm^{-3} were chosen for implantation into the wafers, which correspond to implantation doses of approximately $1x10^{13}$ cm^{-2}, $2x10^{13}$ cm^{-2} and $4x10^{13}$ cm^{-2} respectively. As mentioned earlier for the implanted Au atoms to take part in the compensation they must take up substitutional sites through the kick-out mechanism and the Si must be annealed to achieve this. Using the Au solubility graph in Figure 2.9 in section 2.5, it is clear that in order to introduce Au with concentrations in the 10^{14} cm^{-3} range an anneal temperature of at least 800°C is required. For this reason temperatures of 900°C, 950°C and 1000°C were chosen for these activation anneals.

To begin with the wafers were cleaned for 15 minutes in fuming nitric acid (FNA) before a 20 nm thermal oxide was grown by dry oxidation in a Tempress furnace at 950°C for 28 minutes. This oxide was used as a sacrificial layer to protect the wafer from implantation damage and as a layer to prevent out diffusion of Au during subsequent anneals. The wafers were then divided into batches to be implanted with an energy of 100 keV and an implantation dose of $1x10^{13}$ cm^{-2}, $2x10^{13}$ cm^{-2} or $4x10^{13}$ cm^{-2} at the EPSRC ion implantation facility at Surrey University. The wafers were implanted through the front (polished) and back (unpolished) sides. The wafers were then divided into further batches to be annealed in another Tempress furnace at 900°C, 950°C or 1000°C in argon for 1 hour. The sacrificial oxide was then stripped by a wet-etch in buffered hydrofluoric (HF) acid solution (20:1) until hydrophobic.

2.7 Resistivity Measurements of Gold Doped Silicon

The Au-doped, HRS wafers were examined using a variety of techniques that include sheet resistance measurements using the four-point probe (FPP) technique; resistivity measurements through spreading resistance profiling (SRP) and Hall measurements; and Au concentration measurements using secondary ion mass spectroscopy (SIMS). All measurements with the exception of the Hall measurements were performed on both the front (polished) and back (unpolished) sides of the wafers or samples, for different implantation doses and activation anneal temperatures.

2.7.1 Four-point Probe Measurements

A Jandel RM3-AR four-point prober was used to measure the sheet resistance of the front and back sides of the wafers before and after Au implantation, as well as after anneals at 900°C, 950°C or 1000°C. The RM3-AR is essentially a combined constant current source and a digital voltmeter designed to make sheet resistance measurements that can be converted into resistivity by multiplying by the thickness of the wafer.

The sacrificial oxide was removed immediately before the measurements to ensure a good contact between the probe and the Si. Sheet resistance measurements were performed on full wafers at five points on either side with forward and reverse biased current and then averaged to give a mean sheet resistance for each side of the wafer. This was performed for wafers implanted with all three doses and annealed at all three temperatures. The measured sheet resistances were converted to resistivities by multiplying by the average thickness of the wafers of 675 μm. The as-implanted and post-anneal resistivities are displayed in Table 2.2, for the front and back sides as well as the average of the two. Figure 2.11 shows a plot of the averaged post-anneal resistivities from Table 2.2.

TABLE 2.2
As-implanted and post-anneal resistivities of Au-doped wafers, measured using a four-point probe technique.

Au Dose [cm^{-2}]	Front Side [Ωcm]				Back Side [Ωcm]			Averaged [Ωcm]		
	Anneal Temp. [°C]				*Anneal Temp.* [°C]			*Anneal Temp.* [°C]		
	-	*900*	*950*	*1000*	*900*	*950*	*1000*	*900*	*950*	*1000*
$1x10^{13}$	49.8	637	4.2k	3.7k	529	4k	3.7k	583	4.1k	3.7k
$2x10^{13}$	51.4	7.3k	9.1k	7k	7k	10k	7k	7.1k	9.5k	7k
$4x10^{13}$	51.3	6k	15k	12k	6.8k	18k	15k	6.4k	16k	14k

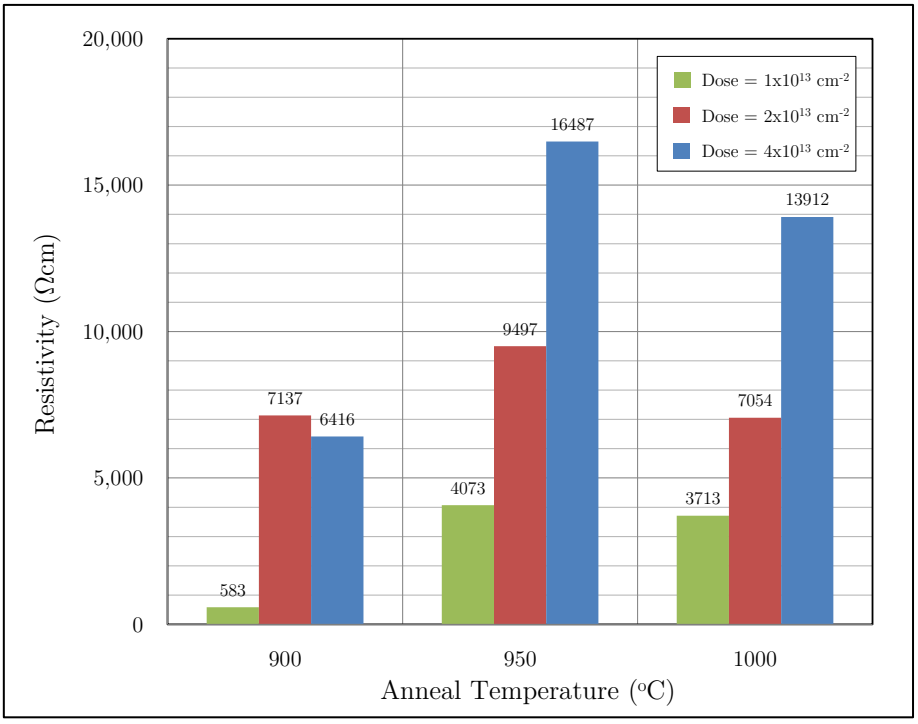

Figure 2.11 – The averaged resistivities of Au-doped Si wafers implanted with different Au doses and annealed at different temperatures, measured using a four-point probe technique.

These results show a large increase in resistivity of Cz-Si after Au implantation and subsequent annealing proving the effectiveness of deep level dopant compensation. The results also confirm that the resistivities of the front and back sides are very similar suggesting a U-shaped Au concentration profile. It is also clear that the resistivity increases with dose and hence concentration of the implanted Au for all anneals, with the highest values measured for the largest dose, with the exception of the 900°C anneal. The as-implanted resistivity values match those before the implant as an insignificant amount of Au is active and hence confirm the necessity of annealing, with all three temperatures leading to an increase in resistivity. It is interesting to note that for all three doses, the highest resistivity values were obtained after an activation anneal at 950°C, but this is not as expected since theoretically an activation anneal at 1000°C should result in a higher resistivity due to the higher solubility.

The average measured resistivity values of the wafers annealed at 950°C were plotted with the theoretical resistivity profiles for different Au concentrations in Figure 2.10, as shown in Figure 2.12. It is clear from this that although the measured resistivity values agree qualitatively with the theoretical profiles, the actual values fall short by just over one order of magnitude. To investigate these discrepancies SIMS and SRP measurements were performed, the results of which are reported in the following section.

The resistivity of the wafer implanted through the back side was also measured and found to be in close comparison to those implanted with the same dose through the front side. Both wafers received an implantation dose of $4x10^{13}$ cm^{-2} and were subsequently annealed at 950°C, and their measured resistivities are shown in Table 2.3. These results suggest that there is not much of a difference between the two implantation methods, both producing very similar resistivities, indicating that either can be used to successfully create HRS, allowing for the implantation of Au through the back of SOI wafers to increase the resistivity of the handle wafer directly beneath the active wafer. It is also clearly noticeable from Table 2.2 and Table 2.3 that the back sides of the wafers generally have a slightly higher resistivity than the front sides. This could be due to the different surface conditions as the polished nature of the front sides may provide less resistive contacts for the FPP probes.

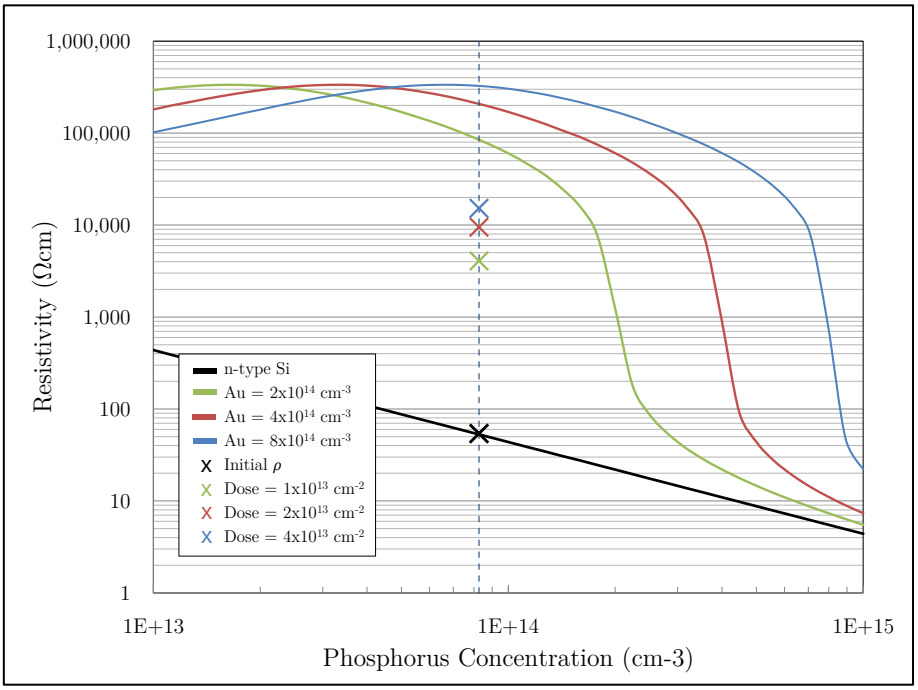

Figure 2.12 – Si resistivity as a function of P concentration, with different Au concentrations and measured averaged resistivity values of wafers annealed at 950°C along with the initial resistivity of 54 Ωcm. Crosses and curves are measured and calculated values respectively.

TABLE 2.3

Measured resistivities of front and back implanted wafers, with doses of $4x10^{13}$ cm^{-2} and annealed at 950°C.

	Resistivity [kΩcm]	
	Front Implant	*Back Implant*
Front Side	15	13
Back Side	18	18

2.7.2 SIMS and SRP Measurements

SIMS measurements were performed at Loughborough Surface Science Ltd on 1 cm^2 samples of wafers annealed at all temperatures, for all three Au doses. The integrated dose of the as-implanted samples agreed with the nominal dose to within 1% providing evidence of the good calibration of the SIMS measurements. It must be noted that the resolution limit of the SIMS measurement is approximately $1x10^{14}$ cm^{-3} and therefore the lower limit of the graphs have been set to this value.

The results for samples annealed at 900°C, 950°C and 1000°C are given in Figure 2.13, Figure 2.14 and Figure 2.15, and show that the post-anneal Au concentration is generally highest at the edges of the wafer decreasing with depth. These results also point to a U-shaped Au concentration profile, although SIMS measurements only detect a small section of it.

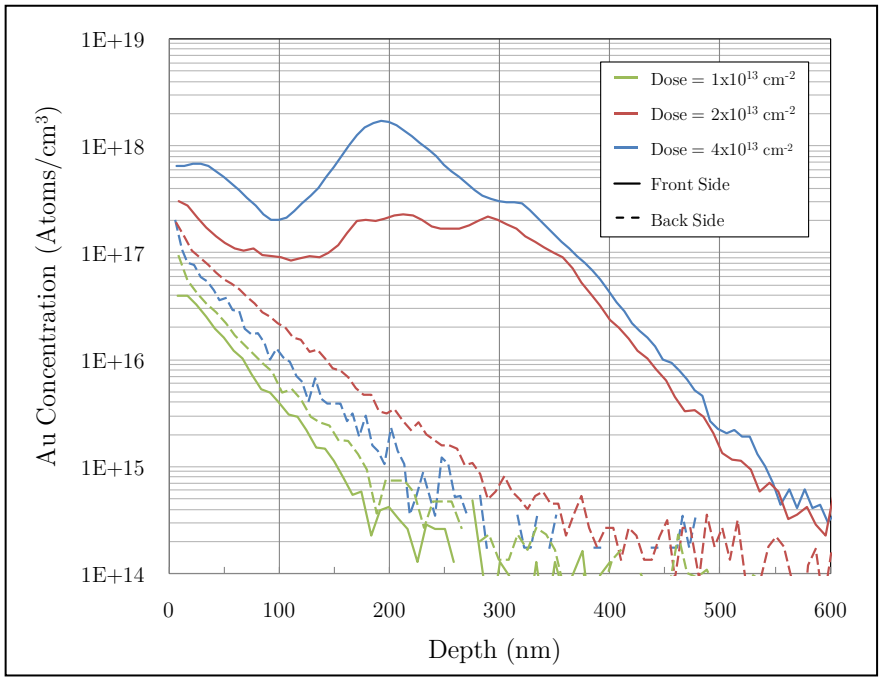

Figure 2.13 – SIMS profiles of Au-doped Si with different implantation doses after a 900°C anneal. Solid and dashed lines represent the profiles of the front side and back side of the wafers respectively.

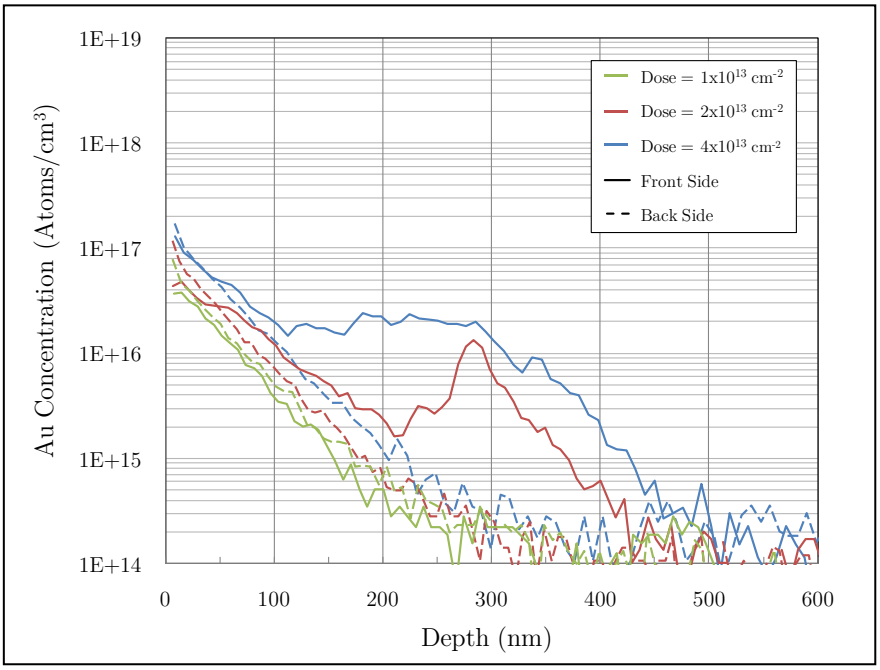

Figure 2.14 – SIMS profiles of Au-doped Si with different implantation doses after a 950°C anneal. Solid and dashed lines represent the profiles of the front side and back side of the wafers respectively.

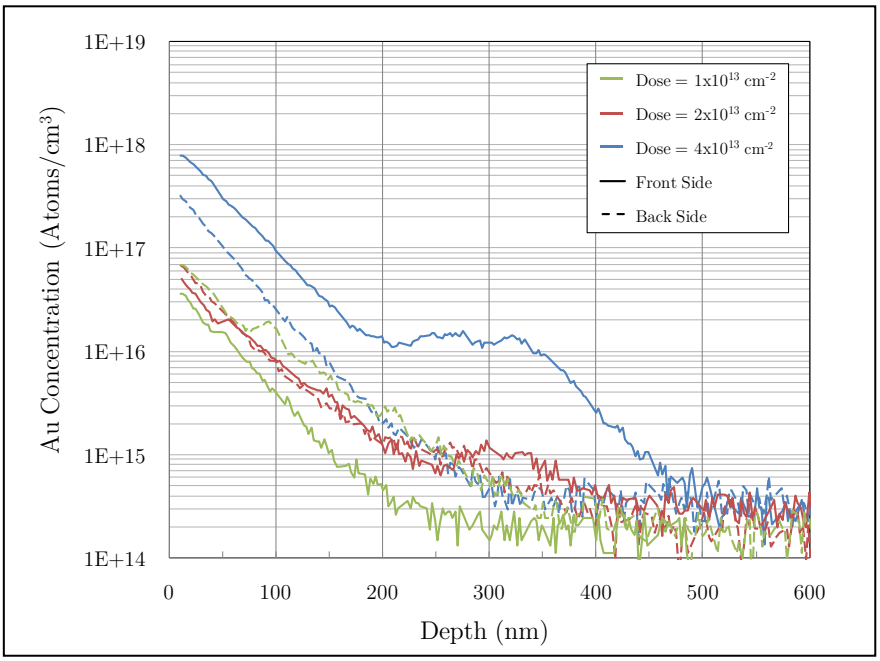

Figure 2.15 – SIMS profiles of Au-doped Si with different implantation doses after a 1000°C anneal. Solid and dashed lines represent the profiles of the front side and back side of the wafers respectively.

For the higher two doses the SIMS profiles of the front sides of the samples show a large amount of Au around a depth of 300 nm that is not present in the back side of the wafer. It is also clear that this Au concentration decreases with anneal temperature suggesting that a substantial amount of implanted Au is trapped at the front side of the wafer. This Au is believed to be electrically inactive because of the lower than expected resistivities measured and the fact that Au must be electrically active, or in substitutional lattice sites, to contribute to the compensation process. The trapped Au may be due to many factors of which agglomeration, or clustering, is the most likely.

SRP measurements were performed on the front and back sides of small samples of the wafers with areas of 1 cm^2, for all implantation doses and anneal temperatures, at the Semiconductor Assessment Services Laboratory. The resistivity depth profiles obtained from these measurements are given in Figure 2.16 and clearly confirm that Au-doped Si has a U-shaped, steeply varying, graded resistivity profile and that the front and back sides of the wafers are very symmetric for all cases. These results coupled with the SIMS profiles link the presence of Au atoms to the high resistivity values measured.

The absolute levels of resistivity were found to be within a factor of 1.5 of the FPP results, but in view of the complicated scaling methods applied to obtain SRP resistivities from measured resistances the discrepancy is not serious [41]. It is however clear that the resistivity at the edges is much lower than the peak value even though the SIMS profiles show that the maximum Au concentration is at the edges. This indicates that most of the Au at the surface is electrically inactive and does not contribute to the resistivity increase, since SIMS results do not distinguish between the different possible states of the Au atoms. These results therefore suggest the existence of a thin inactive Au layer on the wafer surfaces most likely formed by Au atoms pushed out of the substrate during the rapid interstitial diffusion phase. This Au layer would reduce the surface sheet resistance measured by the FPP and does not contribute to the compensation and could be the reason for the lower than expected resistivity values.

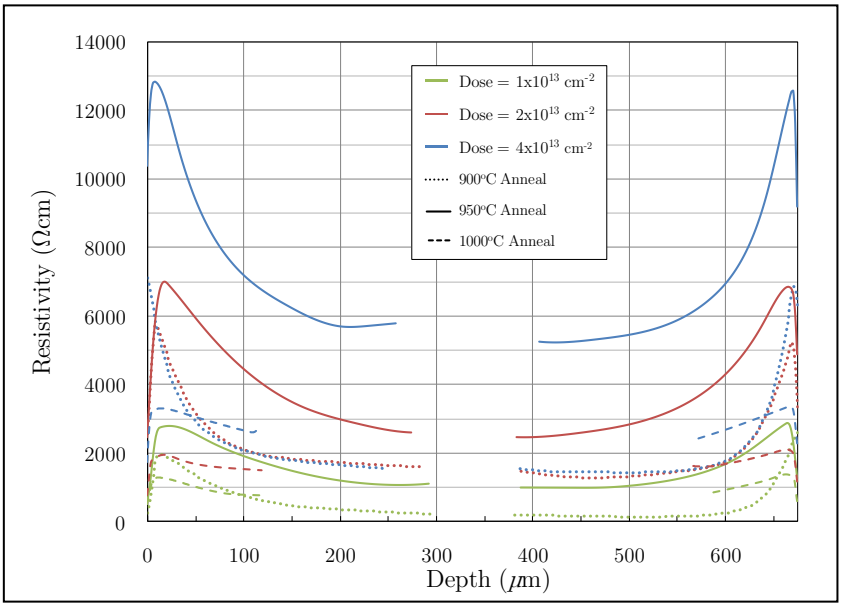

Figure 2.16 – Spreading resistance profiling results of Au-doped Si samples with different implantation dose. Dotted, solid and dashed lines represent anneal temperatures of 900°C, 950°C and 1000°C respectively.

2.7.3 Gold Surface Layer

To determine if a Au surface layer exists the wafers were given a 1 minute dip in an iodine-based Au etchant before being re-measured using the four-point prober. The resistivities after the Au etch are shown in Table 2.4 and in Figure 2.17 along with the pre-etch resistivities. It is clear from these results that the Au etch leads to an increased resistivity indicating the removal of a surface Au layer. The 950°C anneals however still produce the highest resistivities, with the exception of the highest dose. Since the surface Au layer is most likely formed by Au atoms being pushed out of the bulk towards the surfaces during annealing, a larger amount of Au would theoretically be pushed to the surface at higher anneals and could explain why 1000°C anneals result in lower resistivities.

TABLE 2.4

Four-point probe measured, average resistivities of Au-doped wafers annealed at different temperatures, before and after Au etching.

Au Dose [cm^{-2}]	Pre-Au Etch Average ρ [Ωcm]			Post-Au Etch Average ρ [Ωcm]		
	Anneal Temp. [°C]			*Anneal Temp.* [°C]		
	900	*950*	*1000*	*900*	*950*	*1000*
$1x10^{13}$	583	4.1k	3.7k	545	8.6 k	8 k
$2x10^{13}$	7.1k	9.5k	7k	9.6 k	35.5 k	32.4 k
$4x10^{13}$	6.4k	16k	14k	7.3 k	70 k	93.2 k

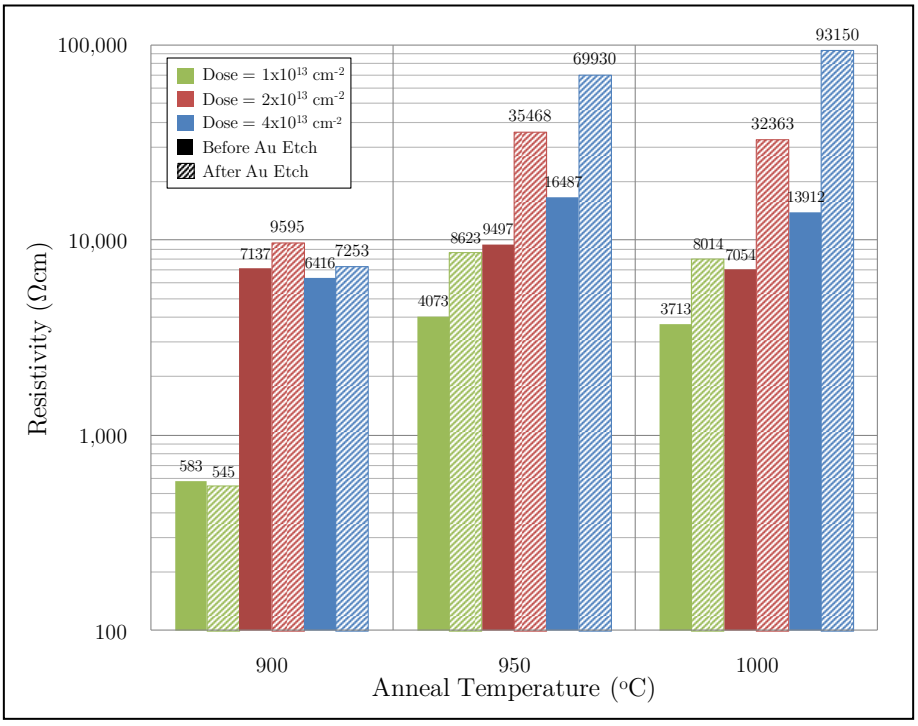

Figure 2.17 – Four-point probe measured resistivities of Au-doped wafers implanted with different Au doses and annealed at different temperatures, before and after a Au etch.

The average resistivity values for wafers annealed at 950°C that received the Au etch are plotted in Figure 2.18 and it can be seen that although there is still a significant difference between these and the theoretical values, this difference falls to within one order of magnitude. The inactive Au atoms forming the surface Au layer do not compensate for free carriers in the Si which explains why the resistivity is lower than expected since the actual active Au concentration is lower than that implanted.

Another possible reason for the lower than expected resistivities may be the agglomeration of Au atoms leading to cluster formation inside the bulk [37], and since these atoms do not take up substitutional sites they do not contribute to the compensation process. It is also suspected that oxygen precipitates or clusters resulting from oxygen introduced into the wafers during the crystal pulling process, may prevent Au atoms from taking up substitutional sites [42].

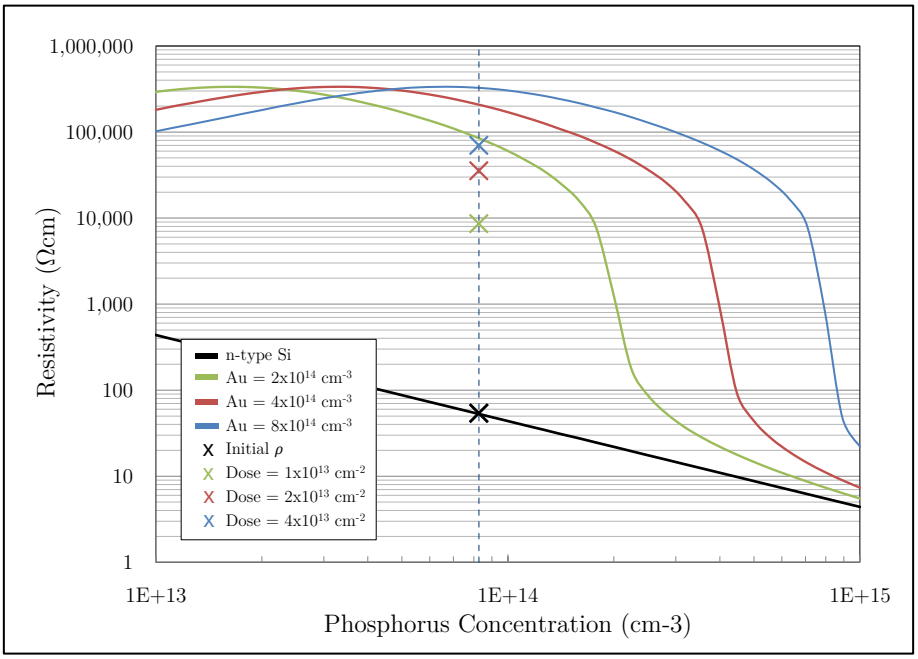

Figure 2.18 –Si resistivity as a function of P concentration, with different Au concentrations and measured average resistivity values of wafers annealed at 950°C that received a Au etch. Crosses and curves are measured and calculated values respectively.

As mentioned earlier for operation of Cz-Si indistinguishable from GaAs a resistivity of at least 5 kΩcm is required [16]. The results clearly show that after Au etching all wafers annealed at 950°C and 1000°C possess resistivities greater than 5 kΩcm regardless of implantation dose, and can therefore be used as alternatives to GaAs despite the lower than expected resistivity values. It is also clear from these results that the 950°C anneal produces the largest resistivity values with the exception of the largest dose. Although the increase from 70 kΩcm for 950°C to 93 kΩcm for 1000°C is significant, it is not worth the increased thermal budget. For these reason the remaining analysis was carried out on samples annealed at 950°C.

2.7.4 Hall Measurements

From equation (2.8) it is clear that the resistivity of a material can be increased by reducing either the carrier concentration or the mobility. To determine which of these is more significantly reduced by deep level dopant compensation Hall measurements were carried out over a large temperature range to obtain the resistivity, and electron mobility and concentration values for uncompensated and Au-doped samples. Hall measurements were made using the van der Pauw configuration which requires ohmic contacts. These were prepared by evaporating 500 nm thick Al contacts onto the corners of square samples of the wafers with areas of 1 cm^2, as illustrated in Figure 2.3. The measurements were then performed using a Nanometrics HL550LN2 cryostat system, on samples implanted with all three doses and annealed at 950°C.

Temperature dependant resistivity measurements were first performed on an uncompensated and three compensated Si samples, the results of which are included in Figure 2.19. These results show that at room temperature the resistivity was increased by up to three orders of magnitude. The room temperature resistivities for samples with doses $1x10^{13}$, $2x10^{13}$ and $4x10^{13}$ are 7.8 kΩcm, 25.3 kΩcm and 61 kΩcm, respectively. The results fall within a factor of two of the four-point probe resistivities of the Au-etched samples in Table 2.4 and the difference is hence not significant.

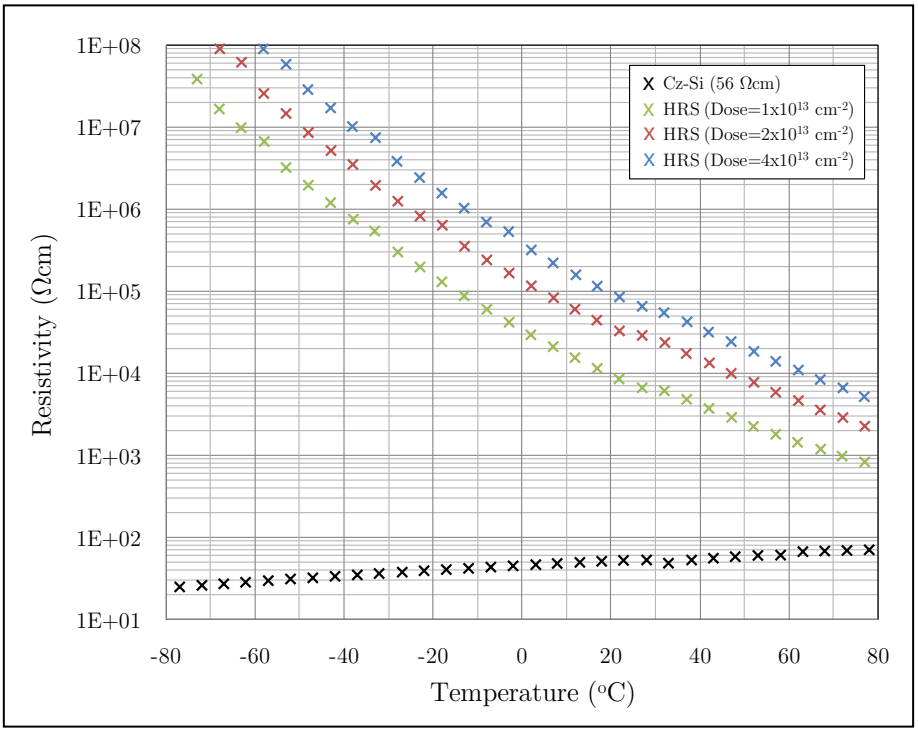

Figure 2.19 – Temperature dependence of resistivity for an uncompensated and three compensated Si samples annealed at 950°C obtained by Hall measurements.

It is also clear that at near operating temperatures of 80°C the resistivity of the compensated samples remain up to two orders of magnitude higher than that of the uncompensated sample. For the highest dose the resistivity is just over 5 kΩcm at 80°C which confirms that during operation the material will retain a high enough resistivity to compete with GaAs.

The electron concentrations of the samples were then measured and the results were used to create an Arrhenius plot using the Arrhenius equation, which relates the rate constant y of a chemical reaction to the temperature in Kelvin T and the activation energy E_a, or the minimum energy particles must possess for the reaction to take place. The Arrhenius equation can be expressed as

$$y = Ae^{-\left(\frac{E_a}{kT}\right)} \tag{2.25}$$

where k = 8.617x10^{-5} (eV)/K, and A is the pre-exponential factor [43]. An Arrhenius plot can be created by plotting the logarithm of y against $1/T$ giving a line with A as the y-intercept. With respect to semiconductor physics and particularly for n-type Si, the Arrhenius equation relates the concentration of electrons possessing enough energy to "jump" into the conduction band to the temperature and donor energy level in the Si bandgap. In other words y and E_a are the free carrier concentration and the donor energy level within the bandgap respectively.

The logarithm values of the free carrier concentrations were plotted against $1000/T$ to create an Arrhenius plot of electron concentrations as functions of temperature for Au-doped samples annealed at 950°C as shown in Figure 2.20. The plot also shows the electron concentration of an uncompensated sample as well as the calculated intrinsic Si and P doped Si behaviours.

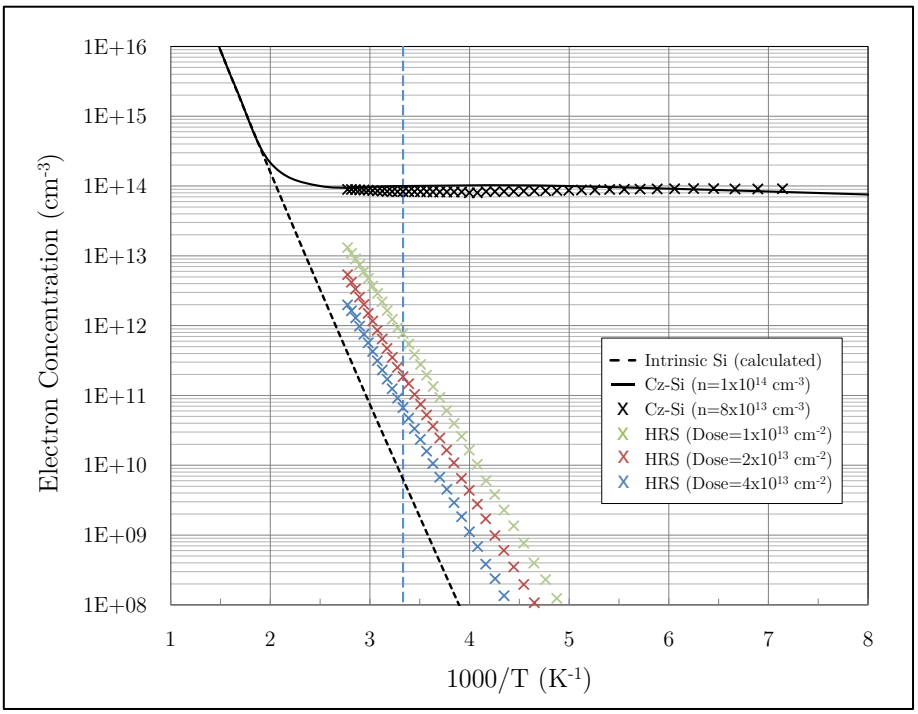

Figure 2.20 – Arrhenius plot of carrier concentration for an uncompensated and compensated samples, as well as theoretic behaviour of intrinsic and extrinsic Si. Lines and crosses represent calculated and measured values respectively. The blue dashed line represents room temperature.

It is clear that the carrier concentrations in the Au-doped samples are less than two orders of magnitude larger than the intrinsic carrier concentration of Si and the temperature dependence follows the intrinsic behaviour. This indicates that deep level dopant compensation greatly reduces free carrier concentration to values close to intrinsic Si.

Lines of best fit were plotted for the results of the Au-doped samples, as shown in Figure 2.21. The equation of the line of best fit for the results of the sample with the highest Au dose was obtained as

$$y = (5 \times 10^{19})e^{-6.113x} \tag{2.26}$$

where $x = 1000/T$. The donor energy level E_a for this sample can hence be extracted from the Arrhenius plot by relating equations (2.25) and (2.26) as follows

$$-\left(\frac{E_a}{kT}\right) = -\frac{6.113 \times 1000}{T}$$

therefore $E_a = 6113 \times (8.62 \times 10^{-5}) = 0.53$ eV. The lines of best fit for the remaining two samples with the lower two doses were found to have equations $y = (4 \times 10^{19})e^{-5.545x}$ and $y = (7 \times 10^{19})e^{-5.757x}$. These equations were used to obtain donor energy levels of 0.48 eV and 0.50 eV, which result in an approximate average energy level of 0.51±0.03 eV. From this analysis it is clear that the donor energy level extracted from the Arrhenius plot is very close to the reported value of Au in Si of 0.54 eV as shown in the energy band diagram in Figure 2.4. It is hence clear that only the donor level takes part in the compensation of n-type Si and the acceptor level is not of relevance. The value is also very close to the Si mid-bandgap energy level of 0.56 eV which proves that deep level dopant compensation pins the Fermi level near the mid-bandgap, intrinsic level.

The electron mobility temperature dependence was also measured and is shown in Figure 2.22, from which it is clear that the mobility values of the compensated samples do not vary much from those of uncompensated Cz-Si over the measured temperature range.

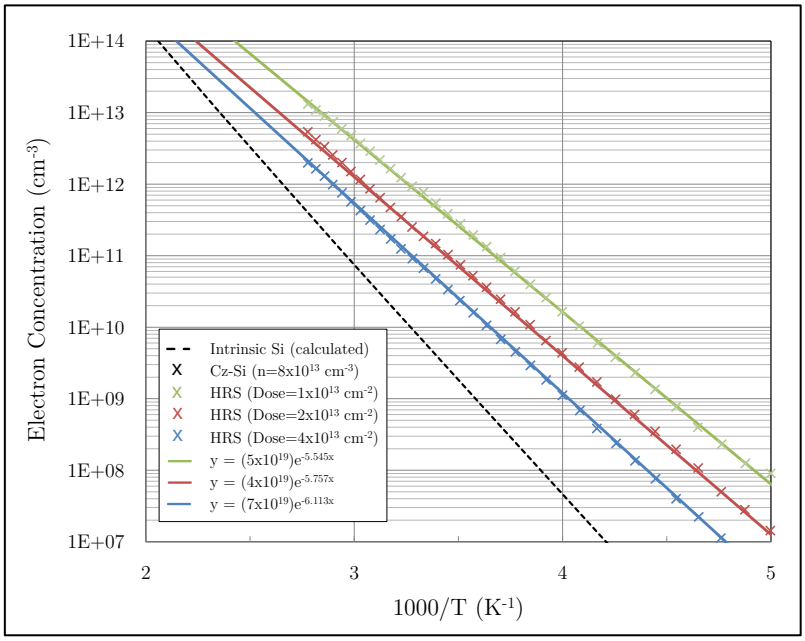

Figure 2.21 – Arrhenius plot of carrier concentration of compensated samples plotted with lines of best fit and the equations of these lines. The dashed line represents the behaviour of intrinsic Si.

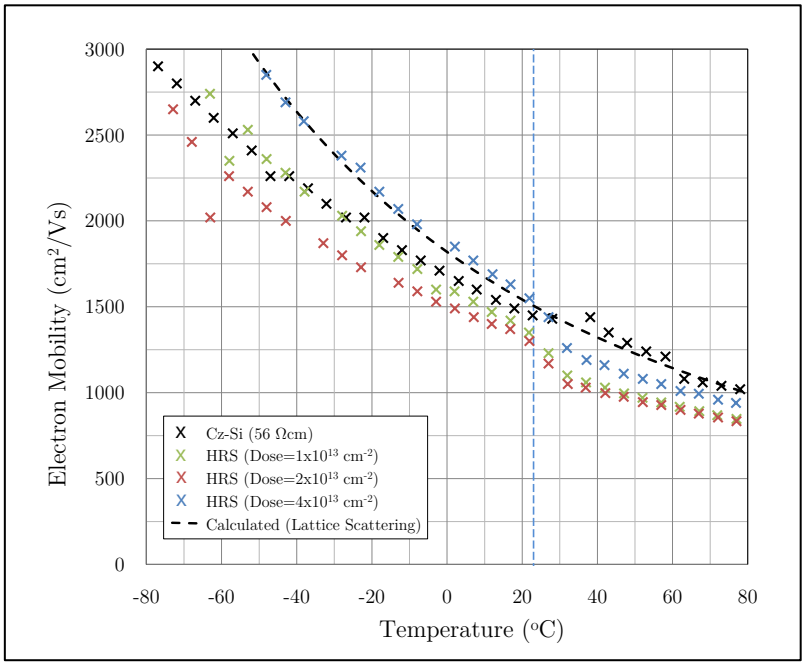

Figure 2.22 – Temperature dependence of mobility of uncompensated and compensated samples annealed at 950°C. The blue and black lines represent room temperature and the theoretical curve calculated using the Arora formula [44].

The room temperature electron mobility of all the samples is very close to the typical value for Si of 1400 $cm^{-2}/(Vs)$ [4]. The theoretical mobility temperature dependence due to lattice scattering was calculated using a formula reported by Arora *et al.* as $\mu_n = (8.56 \times 10^8)T^{-2.33}$, where T is the temperature in Kelvin, and was plotted in Figure 2.22 [44]. The results show that the measured mobilities do not vary much from the theoretical curve. It is hence clear from these results that the increase in resistivity in Au-doped Si is caused mainly by a reduction in the free carrier concentration.

The results discussed so far prove that deep level doping is highly effective in reducing the carrier concentration to near intrinsic values. The technology has also been shown to increase Si resistivity to values that make its performance indistinguishable from GaAs, even at operating temperatures. In order to determine if the technology is capable of improving the RF performance of passive devices, CPW attenuation and spiral inductor Q-factor were measured for devices on undoped and Au-doped wafers.

Chapter 3

Reducing Coplanar Waveguide Attenuation using Deep Level Doped Silicon

A coplanar waveguide (CPW) is an electromagnetic transmission structure used to transfer RF signals. Signal degradation through a CPW is mainly due to substrate absorption and can be easily measured. Therefore the performance of CPWs on deep level doped Si can give a clear indication of how effective deep level doping is at reducing absorption at RF.

3.1 Structure and Attenuation Loses of Coplanar Waveguides

CPWs were first introduced by Wen [45] in 1969 and consist of three in-plane conducting tracks, which include a signal track and a grounding track running in parallel on either side. Figure 3.1 shows a typical CPW structure and design parameters w and s representing the signal track width and the spacing between it and the ground tracks on either side respectively. CPWs offer several advantages over microstrip line technology, including low cost fabrication and flexibility in circuit design, as they remove the need for via holes and allow for easy surface mounting of shunt and parallel passive elements. CPWs also provide reduced crosstalk between transmission lines due to the electric shielding provided by surrounding ground tracks [46].

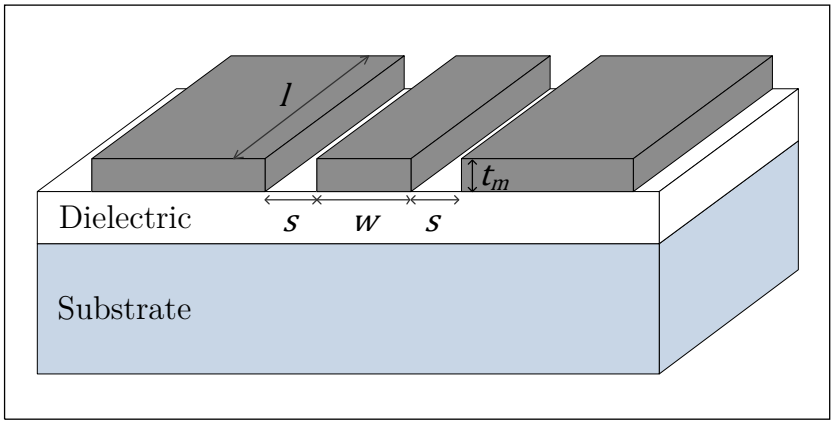

Figure 3.1 - Cross-sectional view of a coplanar waveguide structure showing important dimensions and design parameters.

Signal attenuation is a major issue in all transmission lines which must be minimised to ensure maximum signal transmission. Attenuation at microwave frequencies in a CPW is mainly due to three loss mechanisms; conductor losses in the metal tracks, losses due to absorption in the substrate, and losses caused by charge carriers and interface traps at the interface between the dielectric and the substrate [47], [48]. Therefore fabricating CPWs directly on Si removes the interface contribution to the losses leading to a total attenuation, in dB/unit length, of

$$\alpha = \alpha_c + \alpha_d \tag{3.1}$$

also known as the attenuation constant in which α_c and α_d are the conductor losses and the dielectric losses respectively. In this case the dielectric loss is that of the Si substrate which is due to background free carriers. The frequency dependent conductor losses are mainly due to ohmic losses in the metal tracks and are given, in dB/unit length, by [47]

$$\alpha_c = \frac{8.68\, R_S \sqrt{\varepsilon_{r,eff}}}{240\, \pi\, K(k) K(k') (1 - k^2)} [\Phi(w) + \Phi(w + 2s)] \tag{3.2}$$

where $\varepsilon_{r,eff}$ is the effective relative permittivity, which is an average of the dielectric under the CPW and the air above it since approximately half of the electromagnetic waves

emanating from the waveguide propagate through each of the two media and therefore $\varepsilon_{r,eff} = (1 + \varepsilon_r)/2$, where ε_r is the relative permittivity of the dielectric. $K(x)$ is the complete elliptic integral of the first kind of x, while variables k and k' are related to the layout of the CPW and given as [49]

$$k = \frac{w}{(w + 2s)} \tag{3.3}$$

and

$$k' = \sqrt{1 - k^2} \tag{3.4}$$

The series resistance of the metal track is represented by R_S which can be expressed as

$$R_S = \sqrt{\pi f \mu_0 \rho_m} \tag{3.5}$$

in which f is the frequency, μ_0 is the permeability of free space (4πx10^{-7} H/m) and ρ_m is the metal resistivity. The function Φ is given by

$$\Phi(x) = \frac{1}{x}\left[\pi + ln\left(4\pi \frac{x(1-k)}{t_m(1+k)}\right)\right] \tag{3.6}$$

where t_m is the metal track thickness. The substrate loss α_d can be expressed in dB/unit length using [49]

$$\alpha_d = 27.3 \frac{\varepsilon_r}{\sqrt{\varepsilon_{r,eff}}} . \frac{\varepsilon_{r,eff} - 1}{\varepsilon_r - 1} . \frac{\tan\delta}{\lambda_0} \tag{3.7}$$

in which λ_0 is the free space wavelength, and $tan\,\delta$ is the dielectric loss tangent, given by [50]

$$tan\,\delta = \frac{\omega\varepsilon'' + \sigma}{\omega\varepsilon'} \tag{3.8}$$

where ω is the frequency in radians, σ is the substrate conductivity, and ε' and ε'' are the real and imaginary parts of the complex permittivity of the substrate respectively. This loss tangent is a combination of the polarization losses due to the intrinsic Si substrate $\omega\varepsilon''/\omega\varepsilon'$, and extrinsic losses resulting from the resistivity of the substrate $\sigma/\omega\varepsilon'$ since resistivity $\rho = 1/\sigma$ [51]. The intrinsic loss is however very small and cannot be estimated exactly and can therefore be neglected [47]. Neglecting the intrinsic part of the loss, assuming the substrate thickness is much larger than the CPW dimensions and given that ε_0 is the permittivity of free space ($8.85\text{x}10^{-12}$ F/m) the substrate losses in dB/unit length can be simplified to [49]

$$\alpha_d = \frac{2.17}{\rho}\sqrt{\frac{\mu_0}{\varepsilon_0 \varepsilon_{r,eff}}} \tag{3.9}$$

Figure 3.2 shows a calculated plot of equation (3.2), highlighting the frequency dependence of the conductor losses for an Al CPW fabricated on a Si substrate, with dimensions $w = 50$ μm, $s = 35$ μm and $t_m = 0.5$ μm. The total losses for the same CPW were also calculated using equations (3.1), (3.2) and (3.9) and are shown in Figure 3.3 along with the conductor losses. It can be clearly seen from this graph that as the resistivity of the substrate increases the total attenuation is reduced until it equals the conductor losses.

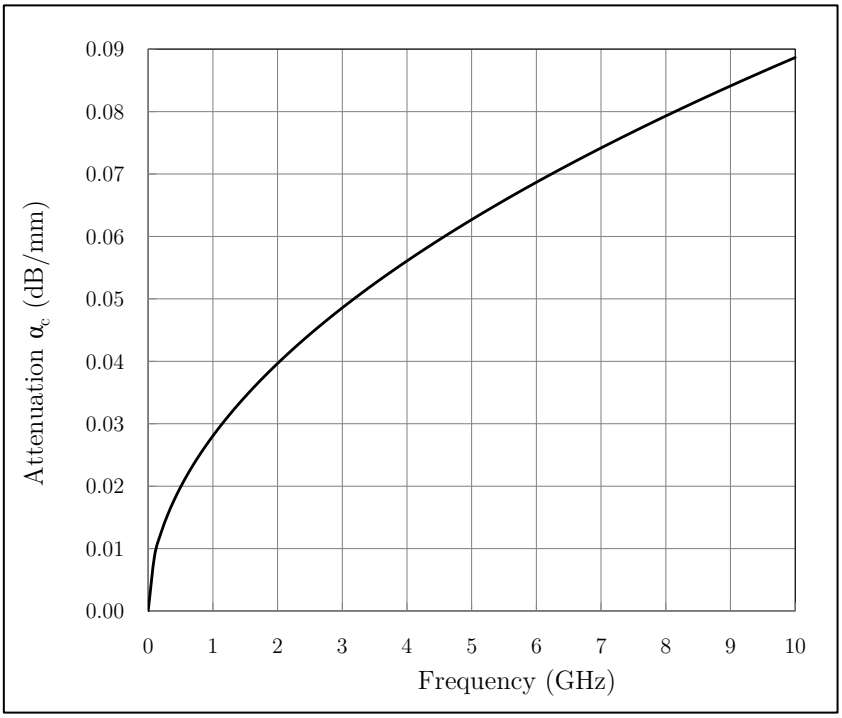

Figure 3.2 - Conductor losses of an Al CPW on Si calculated using equation (3.2), with $w = 50$ μm, $s = 35$ μm and $t_m = 0.5$ μm.

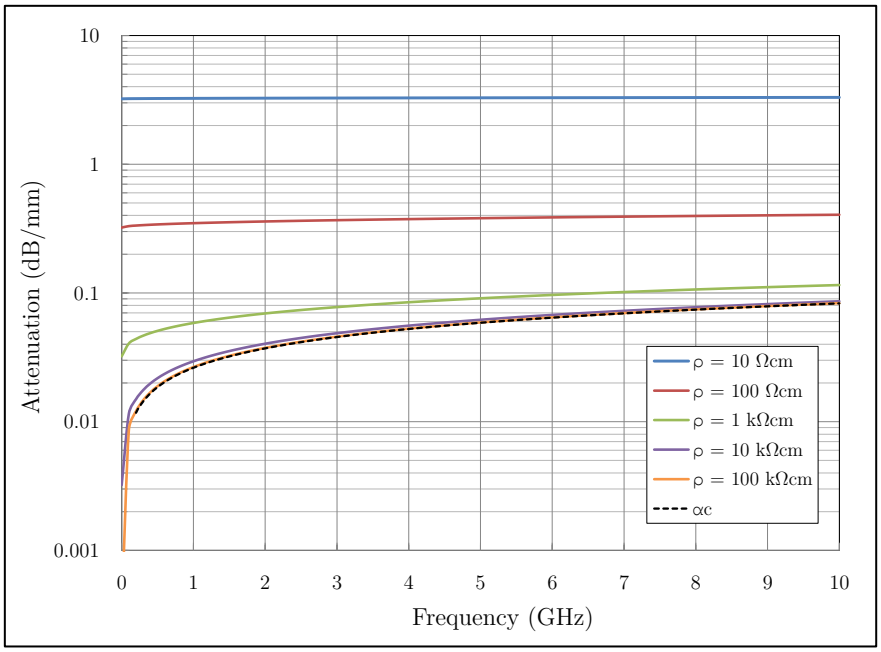

Figure 3.3 - Total attenuation of an Al CPW on Si with different resistivities, calculated using equation (3.1), with w=50 μm, s=35 μm, and t_m=0.5 μm. Conductor losses are represented by the dashed line.

3.2 Measuring Coplanar Waveguide Attenuation

Different proportions of an RF signal incident on one port of a network are either reflected out of the port, transmitted through the network and exit through another port, or lost as heat, radiation or absorption. These proportions can be obtained by measuring the scattering parameters or S-parameters, which are voltage ratios that describe the electrical behaviour of linear electrical networks. Many electrical properties of networks can be easily expressed using S-parameters, such as gain, reflection coefficient and attenuation.

Wave reflection at the ports of a network and transmission through the network are measured and can be represented in a matrix known as a scattering matrix. The directly measureable quantities are the magnitudes and phase angles of the waves reflected or scattered and are measured using a vector network analyser (VNA) [52]. S-parameters can be measured for networks with multiple ports but since CPWs and spiral inductors have only two ports, only the S-parameters of 2-port networks are described.

The S-parameters for a 2-port network at a given frequency and characteristic impedance can be expressed as [53]

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{3.10}$$

The voltages incident on and reflected from port 1 are a_1 and b_1 respectively, while the same is the case for a_2, b_2 and port 2. The matrix containing the S_{xy} elements is the scattering matrix and for these elements the first number in the subscript refers to the exit port, while the second refers to the incident port, i.e. S_{21} represents the voltage ratio of the signal received at port 2 to the signal transmitted at port 1 and hence the ratio of the voltage transmitted from port 1 to port 2. The scattering matrix elements can be converted into power or intensity ratios by taking the square of their magnitudes, i.e. $|S_{21}|^2$ represents the fraction of the power transmitted through the system. As mentioned earlier, fractions of the power of a

signal launched into port 1 of a CPW are either transmitted through the CPW to port 2 ($|S_{21}|^2$), reflected out of port 1 ($|S_{11}|^2$), or absorbed by the substrate.

The attenuation α of the system is related to the intensities of the different proportions of a signal applied to port 1 by the Beer-Lambert law as [54]

$$\frac{I_l}{I_0} = 10^{-\alpha l} \tag{3.11}$$

in which l is the length of the CPW and I_l and I_0 are the intensities or powers transmitted through the system and launched into the system respectively. This can be rewritten as

$$\frac{I_l}{I_0} = \frac{T}{I-R} = \frac{T/I}{1-R/I} = 10^{-\alpha l} \tag{3.12}$$

where I is the total power from the VNA and R and T are the powers reflected at port 1 and transmitted to port 2 respectively. The ratio T/I is the ratio of the power transmitted through the system and is therefore equal to $|S_{21}|^2$, while R/I is the ratio of the power reflected at port 1 and can be expressed as $|S_{11}|^2$. The attenuation coefficient can then be expressed in terms of S-parameters in dB per length l as

$$\alpha = -\frac{10}{l} log_{10}\left[\frac{|S_{21}|^2}{1-|S_{11}|^2}\right]. \tag{3.13}$$

Therefore to determine α of a CPW first the S-parameters are measured using a VNA after which α is calculated using (3.13) and the known length of the waveguide l. RF characteristics including S-parameters are usually measured using a ground-signal-ground (GSG) configuration in which a signal probe is in between two ground probes. The ground probes provide the same effect as the ground tracks in a CPW in that they help to shield the signal probe reducing noise.

3.3 Reducing Coplanar Waveguide Attenuation

As shown earlier the attenuation of microwave signals transmitted through CPWs on Si substrates is predominately due to absorption caused by background free carriers in the Si. There have therefore been many attempts to reduce absorption in Si substrates, examples of which are reviewed as follows and summarised in Table 3.1.

One way of reducing substrate absorption is to use micromachining techniques to remove the Si from beneath the CPWs. These techniques were used by Herrick *et al.* to create Al CPWs on Si substrates and then remove the Si in between the signal and ground tracks by an anisotropic etch to produce a V-shaped groove [55]. The attenuation constant α was reported for CPWs on both standard and micromachined substrates as 0.14 dB/mm and 0.075 dB/mm respectively, at a frequency of 10 GHz. A similar approach was used by Yang *et al.* to fabricate Al CPWs on Si, of resistivity 10 kΩcm, and then isotropically etch a trench between the signal and ground tracks [56]. Microwave attenuation of these CPWs was measured giving an attenuation constant of 0.1 dB/mm at 10 GHz. Although these results show a great reduction in attenuation, micromachining increases the process steps, the cost, and the complexity of the circuit design. For these reasons there exists a great deal of research into using substrates or layers of low loss materials instead of Si, as an alternative method of reducing attenuation.

There have been many instances where CPW attenuation has been reduced using FZ-Si or non-Si substrates. Al CPWs have been fabricated on 50 Ωcm Si and 1 kΩcm FZ-Si with α values measured at 10 GHz of 0.62 dB/mm and 0.3 dB/mm respectively [47]. Microwave measurements performed by Heinrich *et al.* [57], also show reduced attenuation of 1 μm thick Al CPWs on FZ-Si substrates, when compared to the same CPWs on low resistivity Si, and even lower values for 3 μm Au CPWs on GaAs. The resistivities of the substrates were reported as 50 Ωcm, 3 kΩcm and 10 MΩcm for the Si, FZ-Si and GaAs substrates respectively. Measured α at 10 GHz was found to be 0.6 dB/mm, 0.275 dB/mm and 0.15 dB/mm for Cz-Si, FZ-Si and GaAs substrates respectively. Attenuation constants of CPWs on Si and GaAs

were also measured as approximately 0.15 dB/mm and 0.015 dB/mm, respectively at 10 GHz, which is a one order of magnitude decrease [58]. These results suggest that the attenuation constant decreases with increasing resistivity due to the reduced substrate absorption. Taub *et al.* fabricated Au CPWs on a diamond substrate and measured an α of 0.03 dB/mm at 10 GHz [59]. Silicon-On-Quartz was used by Wu *et al.* as a low loss substrate material which led to an α for Al CPWs of 0.35 dB/mm at 10 GHz [60]. However FZ-Si and non-Si substrates are not ideal solutions for reducing CPW attenuation as they are not without their disadvantages, discussed earlier, as well as the fact that Cz-Si substrates are preferred.

Surface passivation is another technique used to increase the resistivity of 3 kΩcm FZ-Si by amorphising the top 300 nm through the implantation of Ar with a dose of 10^{15} cm^{-2} [61]. A 300 nm thick layer of amorphous Si was also deposited onto another FZ-Si wafer, and CPWs were fabricated on all the substrates. At 10 GHz the measured CPW α's were found to be approximately 0.7 dB/mm, 0.15 dB/mm, and 0.1 dB/mm for the FZ-Si and the Ar implanted substrates, and the substrate with the deposited amorphous Si layer respectively. Proton implantation is another variant of this method by which the resistivity of conventional Si was increased from 10 Ωcm to 1.6 MΩcm; a value close to the resistivity of intrinsic Si and GaAs. The measured α was found to be approximately 0.25 dB/mm at 10 GHz, which is lower than that of identical CPWs fabricated on the Silicon-On-Quartz substrate. Despite the effectiveness of these techniques they cause damage to the crystal lattice preventing the operation of many active devices. Another similar idea is to use a passivation layer on top of the Si substrate. In such an instance 10 μm [62] and 20 μm [63] layers of polyimide were deposited in-between Al CPWs and a HRS substrate, and Au CPWs and a low resistivity substrate. At 10 GHz α's of 0.29 dB/mm and 0.1 dB/mm are reported for the low and high resistivity substrates respectively.

A graph showing the theoretically calculated α per unit length of CPWs with $w = 50$ μm, $s = 3.5$ μm, and varying substrate resistivity is displayed in Figure 3.4, along with values from Table 3.1 taken from literature. This plot indicates that the values of α reported in literature are in very close agreement with the theory. It must also be noted that different CPW

geometries would lead to changes in α which would explain the slight deviation of some of the literature α values from the theoretical curve. Although all the techniques mentioned in this section lead to reduced microwave absorption and hence lower CPW attenuation, they all have their own sets of disadvantages, the most significant of which is that most are not compatible with conventional VLSI technology as they increase the complexity and cost of fabrication, and some have yet to prove process compatibility, maturity and yieldability. The use of deep level doped Si as a handle wafer in a SOI configuration or coupled with IPD and 3D integration technologies, on the other hand, are VLSI compatible techniques to achieve reduced signal attenuation.

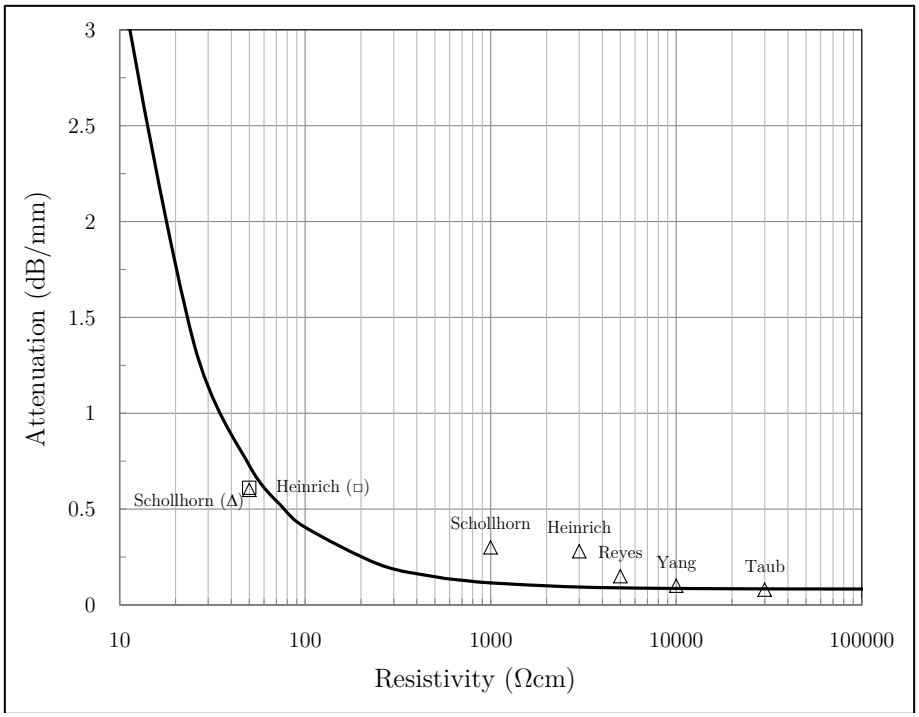

Figure 3.4 – Theoretically calculated attenuation per unit length of a coplanar waveguide ($w = 50$ μm, $s = 3.5$ μm, $t_m = 0.5$ μm) with varying substrate resistivity, along with experimental values from Table 3.1, at 10 GHz.

TABLE 3.1
A summary of attenuation constants of CPWs at 10 GHz reported in literature, highlighting technological and geometric parameters used.

Researchers	Description	Metal	Substrate	t_m (µm)	w (µm)	s (µm)	t_{sub} (µm)	ρ_{sub} (Ωcm)	α (dB/mm)
Herrick *et al.* [55]	Anisotropic micromachining (V-groove etch)	Cr/Au	[SiO_2-Si_3N_4-SiO_2] / HRS	1.75	20	45	1.5 / 500	(HRS)	0.14
								Air	0.08
Yang *et al.* [56]	Isotropic micromachining (trench etch)	Al	Si	1.46	70	40	650	10k	0.10
Scholhorn *et al.* [47]	α measured with -1V bias	Al	Si	1	20	15	-	> 50	0.61
			FZ-Si					> 1k	0.30
Heinrich *et al.* [57]	-	Al	SiO_2 / Si	1	20	15	-	50	0.60
			FZ-Si					3 k	0.28
		Au	GaAs	3				10 M	0.15
Reyes *et al.* [58]	Insulating layer atop Si and GaAs substrates	Au	[SiO_2-Si_3N_4-SiO_2] / Si	2.5	10	30	2 / 400	3k-7k	0.15
			[SiO_2-Si_3N_4-SiO_2] / GaAs				2 / 625	10M-40M	0.015
Taub *et al.* [59]	Au CPWs on FZ-Si and Diamond	Au	FZ-Si	2.5	50	25	200	30k	0.08
			Diamond	2.4	125	25	350	> 10^{11}	0.03
Wu *et al.* [60]	HRS created by implanting protons	Al	Si-on-Quartz	1	30	10	0.2 / 350	Quartz	0.35
			Proton implanted Si				350	1.2M	0.25
Rong *et al.* [61]	Amorphisation of FZ-Si by Ar implantation	-	FZ-Si	4	50	25	0.3 / -	3k	0.7
			Amorphised FZ-Si						0.15
			αSi / FZ-Si						0.10
Ko *et al.* [62]	10μm polyimide layer on Si	Al	Polyimide / Si	3.8	20	10	10 / 635	- / 20	0.29
Ponchak *et al.* [63]	20μm polyimide layer on low-resistivity Si	Au	Polyimide / Si	1.5	50	35	20 / 385	- / 1	0.1

3.4 Coplanar Waveguide Design

To maximise power transfer between components the output impedance of a source is designed to equal the input impedance of a load connected to it in a practice known as impedance matching. For the same reason the characteristic impedance of a CPW must also be matched to the source and load. In the context of this work the source and load are ports of an Agilent Technologies VNA that have a commonly used characteristic impedance of 50 Ω.

There exist many formulae that express the characteristic impedance Z_0 of a CPW as a function of its dimensions and the permittivity of the material under it, an example of which is given by Wen et al. [45] as

$$Z_0 = \frac{1}{C v_{ph}} \tag{3.14}$$

where C is the capacitance of a rectangle, formed by conformal mapping, and calculated using

$$C = 2(\varepsilon_r + 1)\varepsilon_0 \frac{K(k)}{K(k')} \tag{3.15}$$

The phase velocity is represented by v_{ph} which can be expressed as

$$v_{ph} = \frac{c}{\sqrt{\varepsilon_{r,eff}}} \tag{3.16}$$

in which c is the speed of light. Wen's formula can also be simplified to provide another expression for Z_0 as [49]

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{r,eff}}} . \frac{K(k')}{K(k)} \tag{3.17}$$

Another formula for the characteristic impedance stated as more accurate for values of $k > 0.6$ is given as [64]

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{r,eff}}} \cdot \frac{\ln 1/k}{0.665\left[1.5 - exp\left[-0.4\left(\frac{1}{k} - 1\right)\right]\right]} \tag{3.18}$$

When designing CPWs a value of k that sets Z_0 to the required value is obtained iteratively using equation (3.14), (3.17), (3.18) or any other relevant formula, and the permittivity of the dielectric used. This value of k is then used to obtain w and s by setting one to a desired value and calculating the other using equation (3.3).

The CPWs in this work were to be fabricated directly onto Si wafers without an oxide in between to eliminate the interface losses caused by charge carriers at the interface between the oxide and the Si. Given the relative permittivities of Si and air, of 11.9 and 1 respectively, $\varepsilon_{r,eff}$ can be calculated as 6.45. The probes available for measurements were Cascade Microtech GSG probes and the size of the central signal probe makes it difficult to measure contacts smaller than 50 μm x 50 μm, hence the signal track width w was set to 50 μm. Using these values for w and $\varepsilon_{r,eff}$, the spacing s was iteratively varied until the average of equations (3.14), (3.17) and (3.18) gave a characteristic impedance of 50 Ω. This lead to a value of 30 μm for s. The width of the ground planes is typically set to a value much larger than the signal track width and therefore a value of 250 μm was chosen to enable microwave measurements to be made using probes with a variety of pitches, or distances between probe tips. The CPWs were designed with lengths of 0.8 mm, 1.6 mm, 3.2 mm and 6.4 mm. The 6.4 mm waveguide was designed to ensure that a waveguide with a measureable attenuation was included as CPW attenuation is directly proportional to length. A photolithography mask used to fabricate the CPWs was designed using these dimensions and Tanner EDA's L-Edit IC design software, a section of which is shown in Figure 3.5.

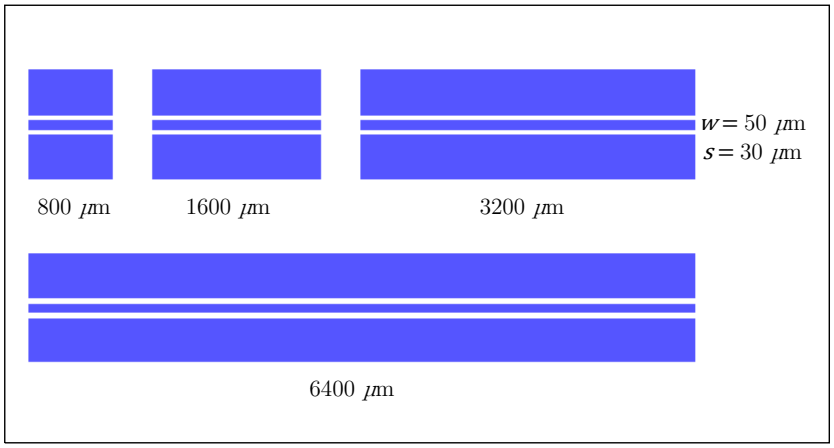

Figure 3.5 - Sample of the photolithography mask designed in L-Edit and used to fabricate CPWs with w = 50 μm, s = 30 μm, and l lengths of 0.8 mm, 1.6 mm, 3.2 mm and 6.4 mm.

3.5 Fabrication of Coplanar Waveguides

Device fabrication was performed in the Southampton Nanofabrication Centre at the University of Southampton. Al was typically used as a metallisation layer in IC fabrication, and due to its availability in the Southampton Nanofabrication Centre it was selected as the metal of choice for the fabrication of the passive devices in this work. Al CPWs with w = 50 μm, s = 30 μm, and l values of 0.8 mm, 1.6 mm, 3.2 mm and 6.4 mm were fabricated directly onto wafers that were implanted with Au with doses of 1x10^{13} cm^{-2}, 2x10^{13} cm^{-2} or 4x10^{13} cm^{-2} and annealed at 950°C before an oxide strip and Au etch, as well as an unimplanted wafer with a relatively low resistivity of 56 Ωcm.

The wafers were first cleaned in FNA for 15 minutes before a 500 nm thick Al layer was deposited using a Leybold Optics BAK600 e-beam evaporator at a rate of 0.25 nm/s. The Al layer was then patterned with the photolithography mask designed and an EV Group EVG620T contact mask aligner using optical lithography. First a Microposit positive photo-resist S1813 was spun atop the wafer using a Brewer Cee200 spinner, before soft baking using a Sawatec HP-401-Z hotplate at 95°C for 60 seconds. The resist was then exposed to light through the mask for 1.9 seconds in the mask aligner. The exposed resist was developed by a

35 second dip in Microposit MF-319 developer solution removing the exposed resist. The remaining protective resist was hard baked at 50°C for 20 minutes using the Sawatec hotplate. All uncovered Al was removed using an OM Group Al chemical wet etchant, comprised of 1-5% nitric acid that oxidises the Al, 65-70% phosphoric acid that etches the Al oxide, and 5-10% acetic acid for wetting and buffering. The etch rate was found to be approximately 360 nm per minute at 40°C, so for the 500 nm track a 2 minute etch was used to ensure all the Al was removed. Finally the protective resist was removed by a 10 second dip in FNA. Figure 3.6 shows an image, obtained from an optical microscope, of some of the fabricated CPWs.

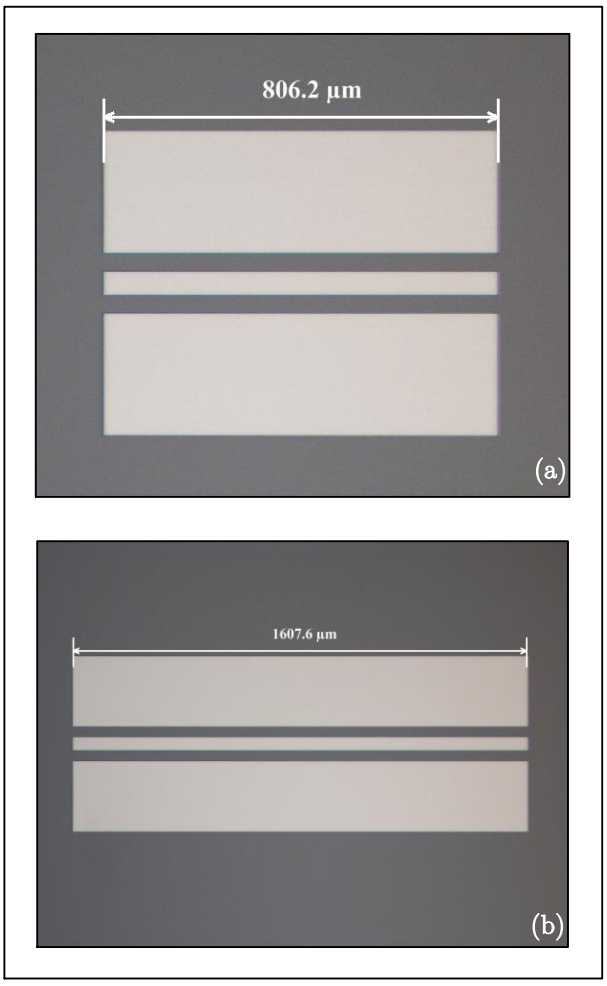

Figure 3.6 – Images of fabricated CPWs of length (a) 800 μm and (b) 1600 μm, as they appear on the wafer surface, taken using an optical microscope.

3.6 Coplanar Waveguide Attenuation Measurements

To assess the RF performance of CPWs on HRS, the S-parameters of the waveguides were measured using a VNA from which the attenuation was calculated using equation (3.13) as discussed earlier. The Agilent Technologies E8691A VNA used was first calibrated using an impedance standard substrate (ISS) containing Au S-O-L-T (Short-Open-Load-Through) calibration structures and CPWs on an alumina substrate, with a resistivity of $1x10^{14}$ Ωcm. The CPWs on the ISS were of similar dimensions to the ones designed in this work, with w = 50 μm, s = 34 μm and a characteristic impedance of 50 Ω. S-parameters were measured for CPWs fabricated on the uncompensated wafer and on wafers implanted with all three Au doses and annealed at 950°C, as well as for CPWs on the ISS. The measurements were made using probes with a GSG configuration, a Cascade Microtech Summit 12000B-AP semi-automatic probe station, and a VNA. Figure 3.7 shows an image of a CPW being measured, taken using an optical microscope.

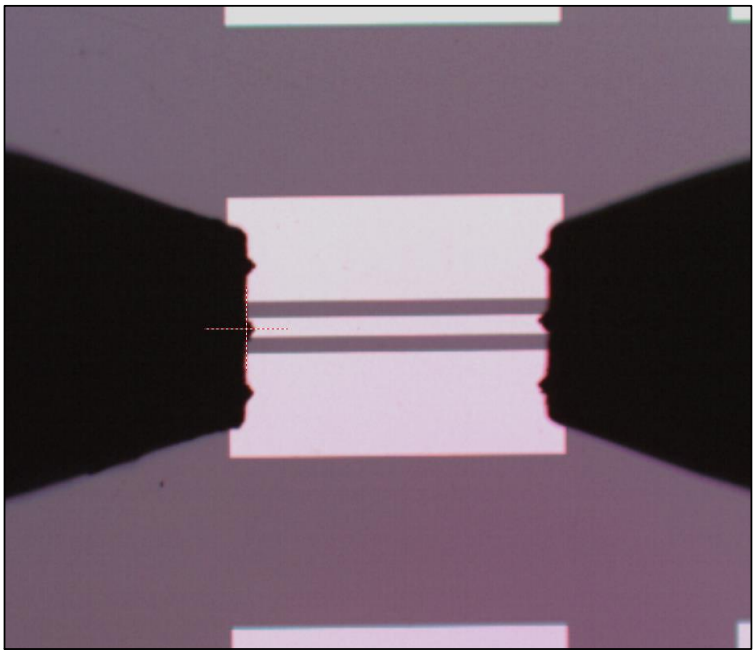

Figure 3.7 – Magnified image of a CPW with l = 0.8 mm under measurement using GSG probes.

First the VNA was calibrated using the S-O-L-T calibration structures on the ISS chip. The S-parameters for CPWs of different lengths were measured over a frequency range of 1 GHz – 67 GHz. Graphs of the obtained S_{11} and S_{21} values are included in Appendix A, from which graphs of reflection, transmission and absorption were produced and are included in Appendix B. The S-parameters were then converted into attenuation coefficients using equation (3.13). Figure 3.8 shows the attenuation for CPWs of different lengths fabricated on the uncompensated and compensated wafers with resistivities of 56 Ωcm and 70 kΩcm (dose of $4x10^{13}$ cm^{-2}) respectively, at frequencies of 1 GHz, 10 GHz and 60 GHz. For both wafers it can be seen that the attenuation is proportional to the length of the waveguide with the variation between different devices giving an error bar smaller than the size of the data points. It is evident from this graph that the attenuation values of CPWs fabricated on uncompensated Cz-Si is much higher than for those fabricated on the HRS wafer.

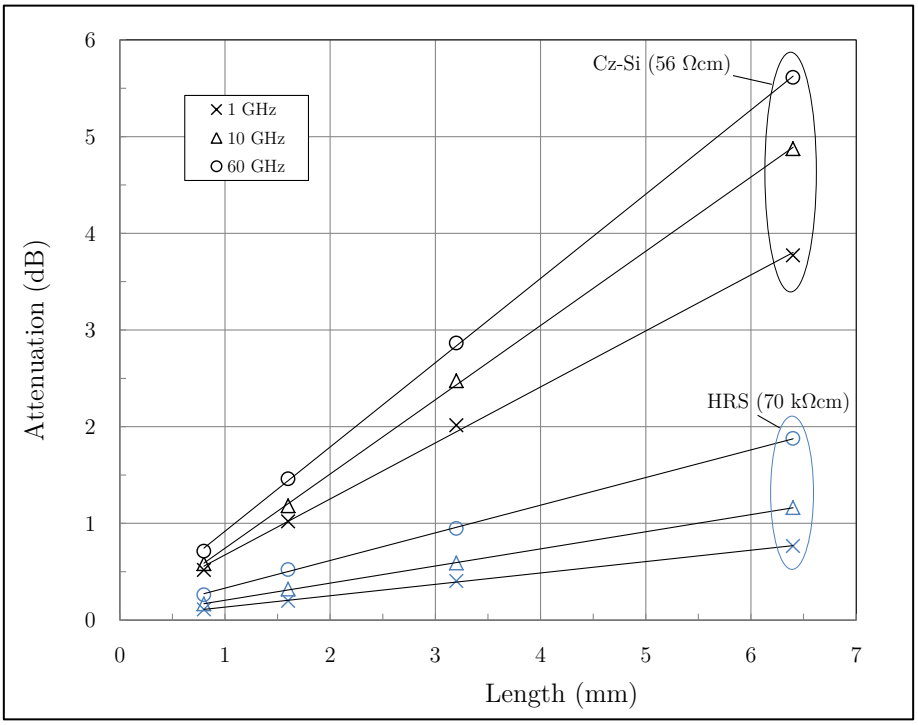

Figure 3.8 – Measured attenuation of CPWs with different lengths fabricated on an uncompensated wafer and on compensated wafers, at frequencies of 1 GHz, 10 GHz and 60 GHz.

A graph of the attenuation per unit length as a function of frequency for 6.4 mm length CPWs on uncompensated and compensated wafers and the ISS is displayed in Figure 3.9, in which it is clear that attenuation is reduced with increasing substrate resistivity. The results also show that the attenuation values of the CPWs on HRS are much closer to those on the alumina substrate than those on the virgin Cz-Si wafers. Figure 3.10 shows a comparison between the theoretical calculated attenuation values and measured values for CPWs from literature and for those fabricated. The graph is identical to that of Figure 3.4 with the addition of attenuation values at 10 GHz of the CPWs fabricated on uncompensated and compensated Si. The results show that the CPWs fabricated in this work follow the theoretical trend without deviating by much more than other CPWs reported in literature.

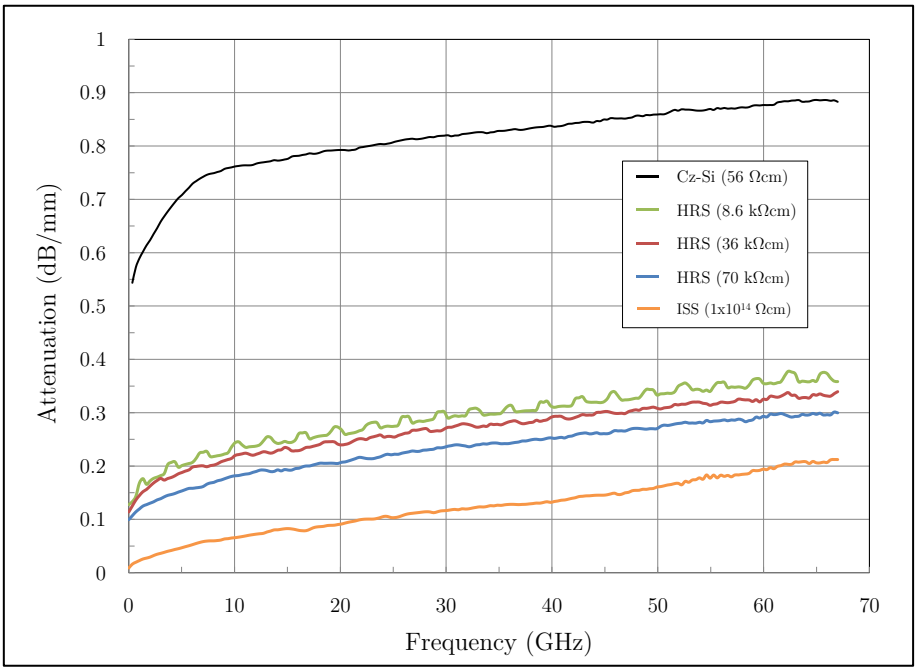

Figure 3.9 – Measured attenuation per unit area with varying frequency of CPWs (l = 6.4 mm) fabricated on wafers of different resistivities as indicated, showing reduced loss for low resistivity wafers.

From these results it can be clearly seen that at a frequency of 10 GHz, deep level doping of Cz-Si, with a Au dose of $4x10^{13}$ cm^{-2} and a 950°C activation anneal, reduces CPW attenuation per unit length from 0.76 dB/mm to 0.18 dB/mm; a decrease of over 76%. These results prove that HRS can be used to reduce the attenuation of CPWs and can hence boost the performance of passives in RFICs. Spiral inductors were also simulated and fabricated on HRS to see if any improvements in efficiency result from the deep level doped material, as detailed in the following chapter.

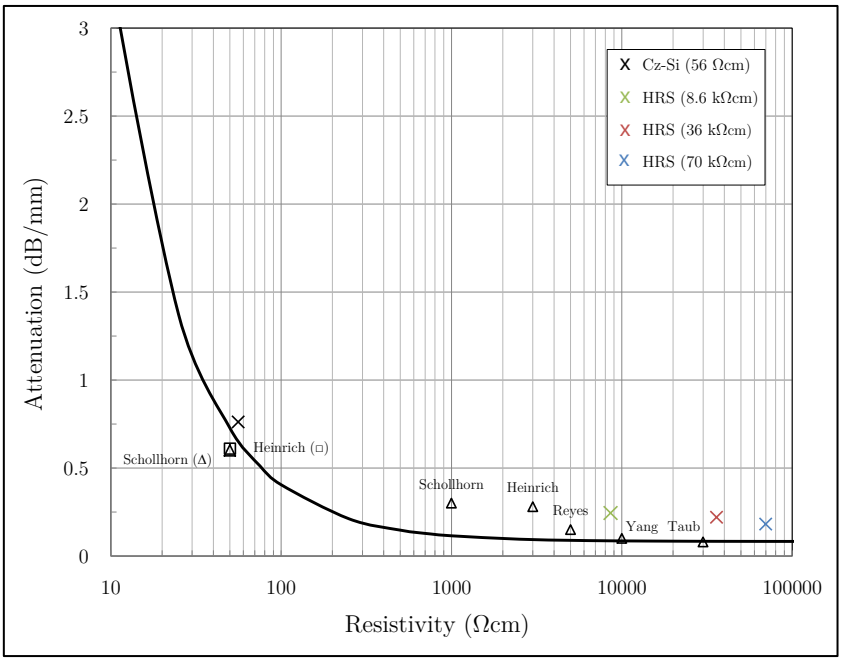

Figure 3.10 – Theoretically calculated attenuation per unit length of a coplanar waveguide ($w = 50$ μm, $s = 3.5$ μm, $t_m = 0.5$ μm) with varying substrate resistivity, along with measured values for waveguides fabricated on uncompensated and compensated Si, at 10 GHz. Values reported in literature summarised in Table 3.1 have also been included.

Chapter 4

Improved Efficiency of Spiral Inductors on Deep Level Doped Silicon

Inductors are passive elements that store energy created by the electric current passing through them in a magnetic field. Inductors are used extensively in analogue circuits and for signal processing, as well as for filters to prevent radio frequency interference from being transmitted. They are also essential in the wireless communications equipment necessary for the creation of important RF building blocks, such as LNAs, VCOs and filters. Inductors used in ICs are of a planar spiral design and hence are known as spiral inductors. High-efficiency spiral inductors are necessary to help satisfy RF design requirements, including low supply voltage, low power dissipation, low noise, and low distortion. Therefore any technology that improves inductor efficiency would also lead to enhanced RFIC performance. Inductors have been chosen not only due to the fact that they are essential passive components for RFICs, but also because the dominant RF loss mechanism is substrate related.

4.1 Geometry and Inductance of Spiral Inductors

The most basic form of a conventional inductor is a coil of wire wrapped around a ferromagnetic core that increases the efficiency of the inductor. A crucial aspect of RFIC

design, however, is the fabrication of all passive and active components on a single chip pushing for a shift towards on-chip, planar inductor designs. To realise such designs inductors are fabricated on a single metal layer in a flat, spiral fashion and the exit from the inner port of the inductor is made by transition to another metal layer though interconnecting vias. These types of inductors are known as spiral inductors and can have many different shapes, the most efficient of which are circular, spiral patterns but these are difficult to fabricate using standard techniques. For this reason square and octagonal geometries are commonly used.

An example of a square spiral inductor is shown in Figure 4.1 along with important design parameters n, w and s which are the number of turns, the metal track width and the spacing between tracks respectively. The radius, and outer and inner diameters of the inductor are represented by r, d_{out} and d_{in} respectively, while a is the average radius or the distance from the centre of the coil to the middle of the windings.

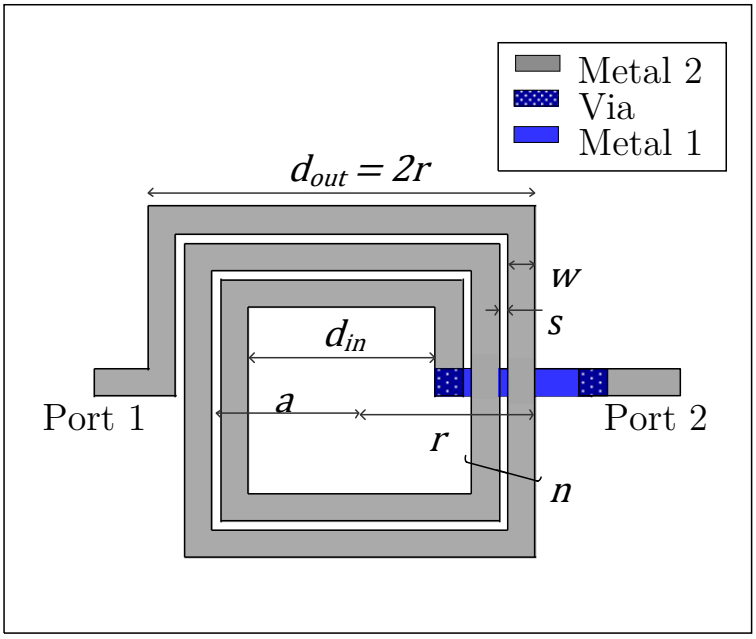

Figure 4.1 – Planar view of a spiral inductor structure showing important dimensions and design parameters.

Figure 4.2 shows a cross-sectional view of the same inductor along with metal design parameters t_{m1} and t_{m2}, which are the thicknesses of the lower metal layer (metal 1) and the upper metal layer (metal 2) respectively, as well as t_{ox1}, t_{ox2} and t_{ox3} which are the thicknesses of the oxides under metal 1 and metal 2 and in between the two metal layers respectively. A three-dimensional view of the same inductor can be seen in Figure 4.3.

Inductance is a measure of the amount of EMF generated for a unit change in current and there are many ways to calculate it for a given geometry. The most accurate method is to calculate it by solving Maxwell's equations by using 3-D, finite-element simulators for example. These processes are computationally intensive and lengthy which makes them more appropriate for design verification rather than the design itself. Alternatively there also exist a number of formulae that give good approximations for inductance.

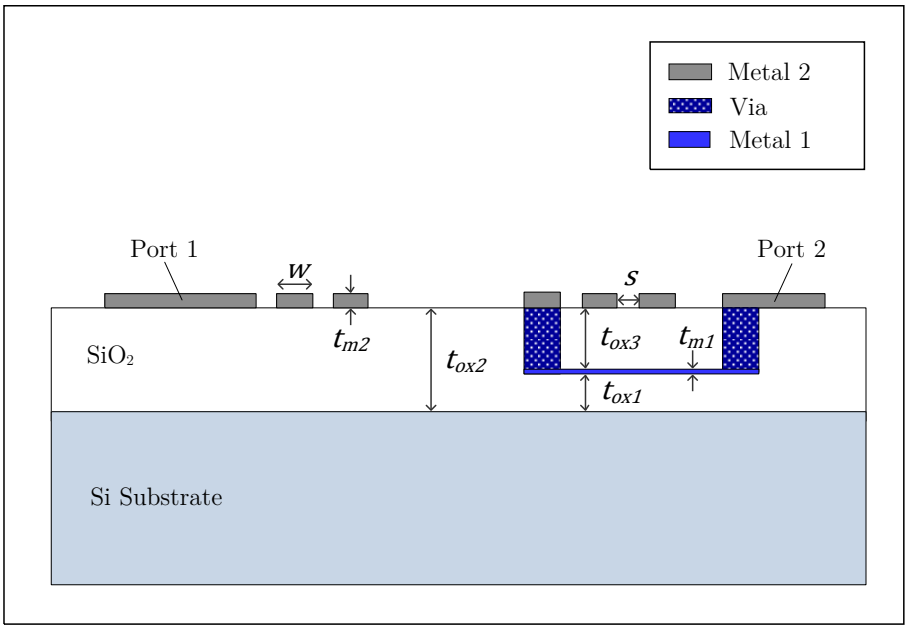

Figure 4.2 – Cross-sectional view of a spiral inductor showing important dimensions and design parameters.

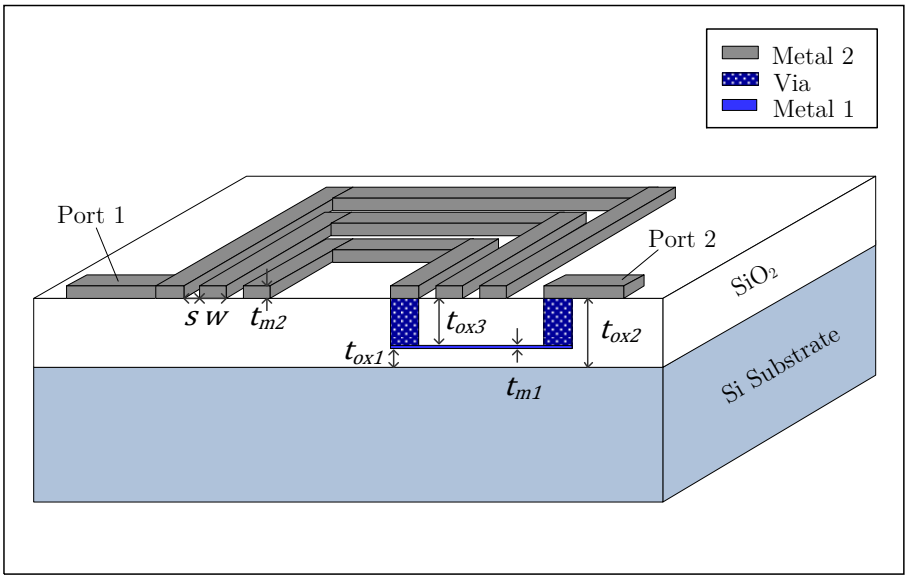

Figure 4.3 – Three-dimensional, cross-sectional layout of a spiral inductor structure showing the underpass and the vias for connecting between the two metal layers.

A recurring formula used frequently in literature [2], [65] expresses the inductance L as

$$L = \frac{37.5\mu_0 n^2 a^2}{22r - 14a} \tag{4.1}$$

in which μ_0 is the permeability of free space and a can be approximated as

$$a = r - \frac{\big(wn + s(n-1)\big)}{2} \tag{4.2}$$

Another formula known as the modified Wheeler expression [66] is given by

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \varphi} \tag{4.3}$$

where d_{avg} is the average diameter given by $d_{avg} = (d_{out} + d_{in})/2$, and K_1 and K_2 are layout specific coefficients, which for a square inductor are 2.34 and 2.75 respectively.

The fill ratio φ is defined as

$$\varphi = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{4.4}$$

Another expression is derived from electromagnetic principles by approximating the sides of the spiral by current sheets with uniform current distribution and is termed the current sheet approximation formula [65], [66] given by

$$L = \frac{\mu_0 n^2 d_{avg} c_1}{2}\left[ln\left(\frac{c_2}{\varphi}\right) + c_3\varphi + c_4\varphi^2\right] \tag{4.5}$$

in which c_1, c_2, c_3 and c_4, for a square inductor, are 1.27, 2.07, 0.18 and 0.13 respectively.

4.2 Quality Factor of Spiral Inductors

An ideal inductor has no resistance or capacitance, and does not dissipate energy. This is not the case for a real inductor which exhibits undesirable energy losses due to various geometric and technological parameters. Geometrical parameters can be changed by the inductor designer and include n, w, s, the shape and area of the inductor. The main geometric loss mechanism is metal track losses which are due to the series resistance of the coil itself. At low frequencies, current distribution inside a wire tends to be evenly distributed. However at high frequencies current distribution becomes affected by eddy currents that cause the current density near the edges of a conductor to become greater than that at its centre. This phenomenon is known as the skin effect which leads to an increase in resistance with increasing frequency. A similar geometric loss mechanism that becomes apparent at high frequency is the proximity effect, which is current crowding caused by eddy currents induced in a conductor by current travelling in a nearby conductor.

Technological parameters are specific for a given technology such as the substrate resistivity, the metal sheet resistance, and the oxide capacitance. The main technological loss mechanism, however, is the substrate losses caused by substrate currents, which are mainly composed of two parts; displacement currents from spiral traces to the substrate through the oxide capacitance, and eddy currents induced in the substrate by the inductor. Displacement currents are a product of the time varying electric field through the oxide capacitance, and increase with higher frequencies. The changing magnetic field due to the electric field induced in the spiral, induces a current to flow in the opposite direction in the substrate producing a negative effect on the performance of the inductor, as illustrated in Figure 4.4. These currents are known as eddy currents and decrease the effective inductance as they work against the spiral current and as a result the energy stored by the inductor is reduced and efficiency drops [67]. This efficiency at storing magnetic energy is called the quality factor and is a unitless ratio of the energy stored to the energy lost. The higher the quality factor, or Q-factor, of the inductor the closer it approaches ideal behaviour with a Q-factor of infinity. Therefore improvements in Q-factor can be used to investigate the benefits of using HRS.

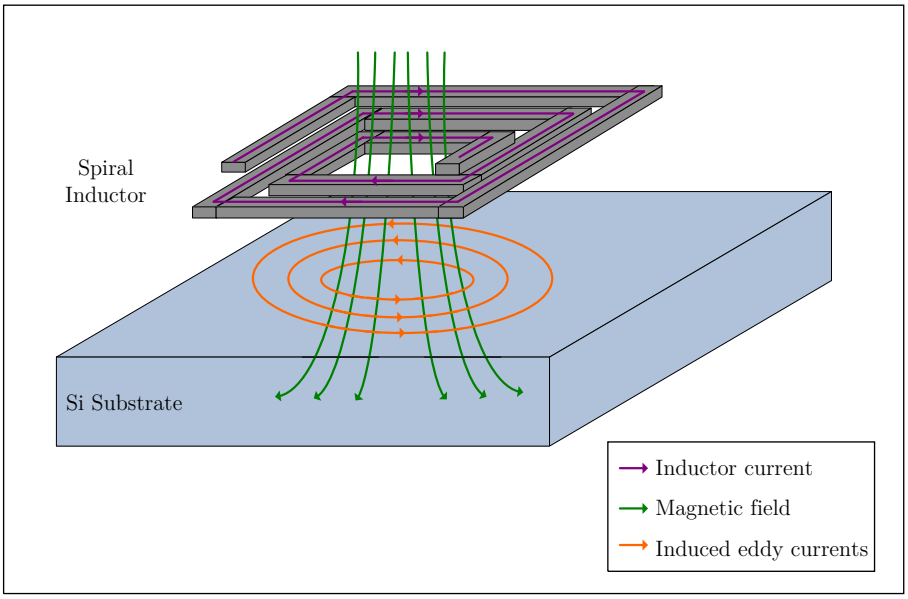

Figure 4.4 – Diagram illustrating how eddy currents are induced by magnetic fields penetrating into the substrate, which are themselves induced by the inductor current.

The frequency dependent Q-factor of an inductor can be described as the ratio of its inductive reactance to its own resistance or in other words the ratio of the real part to the imaginary part of the impedance Z at a given frequency, and is given by [65]

$$Q = \frac{|Im[Z]|}{Re[Z]} \tag{4.6}$$

In this work the S-parameters of inductors will be measured using the techniques and equipment described earlier. Q-factor can be expressed in terms of admittance parameters, or Y-parameters, which are closely related to S-parameters. The Q-factor of a spiral inductor at a given frequency can also be defined by the following commonly used formula [68]

$$Q = -\frac{Im[Y_{11}]}{Re[Y_{11}]} \tag{4.7}$$

where Y_{11} is one of the Y-parameters of the inductor, which can be obtained from measured S-parameters using the following relation [53]

$$Y_{11} = \frac{[(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}]}{[(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}]} \tag{4.8}$$

In other words to calculate the Q-factor of a spiral inductor at a given frequency, the two-port S-parameters can be measured then used to obtain Y_{11} using equation (4.8), which is then used to calculate the Q-factor using equation (4.7).

The Q-factor of a spiral inductor can also be expressed in terms of its geometric and technological parameters. These expressions can help predict the behaviour of a given inductor and are hence extremely useful when designing inductors. To derive the expressions the inductor is modelled with its parasitic losses before the impedance of the model is derived. From this the Q-factor is calculated using equation (4.6) as detailed in the following section.

4.3 Spiral Inductor Modelling

The most basic model of an inductor is simply an ideal inductor of inductance L in series with a resistor R_S as shown in Figure 4.5. The resistance of the track is represented by R_S which converts current into heat causing a loss of inductive quality. To calculate the Q-factor of this 'R_S model' an expression for the total impedance Z_{tot} is required. As the impedances of the inductor and the resistor are simply $j\omega L$ and R_S respectively, where ω is frequency and $j = \sqrt{-1}$, Z_{tot} for the model can be expressed as

$$Z_{tot} = j\omega L + R_S \tag{4.9}$$

The Q-factor of this R_S model for an inductor can therefore be derived using equation (4.6) as

$$Q = \frac{\omega L}{R_S} \tag{4.10}$$

As mentioned in section 3.1 the value of R_S is not a constant and increases with frequency due to the skin effect. R_S is more accurately expressed as

$$R_S(\omega) = \frac{l}{\sigma_m w \delta \left(1 - e^{-\frac{t_m}{\delta}}\right)} \tag{4.11}$$

where σ_m, w and t_m are the conductivity, width and thickness of the metal, respectively [65].

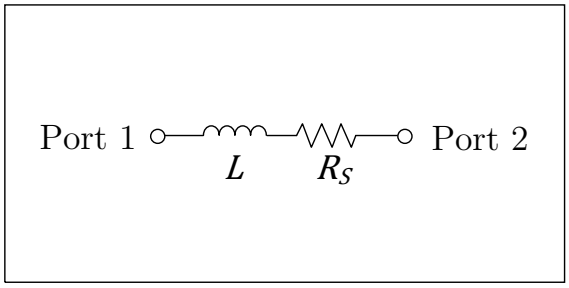

Figure 4.5 – A simple R_S model of an inductor that takes into account the series resistance R_S.

The length of the track l can be approximated as

$$l = 4[nd_{out} - n(n-1)(w+s)] - n(w+s) \tag{4.12}$$

and δ represents the skin depth [65] given by

$$\delta = \sqrt{\frac{2}{\omega\sigma_m\mu_m}} \tag{4.13}$$

in which μ_m is the permeability of the metal. To take into account high frequency losses caused by the skin effect, Q can be expressed as

$$Q = \frac{\omega L}{R_S(\omega)} \tag{4.14}$$

Equation (4.14) however still does not take into account capacitive losses associated with spiral inductors. The losses caused by the capacitance associated with the metal underpass, required to connect the inner port of the inductor to external circuitry, as well as that caused by the fringing capacitance between the metal tracks. The latter can be neglected because the tracks are almost at the same potential and the capacitance is therefore small when compared to the overlap capacitance C_S. Hence, along with R_S, C_S is a major loss source particularly at higher frequencies and can be expressed as

$$C_S = nw^2 \frac{\varepsilon_{ox}}{t_{ox3}} \tag{4.15}$$

in which ε_{ox} is the permittivity of the dielectric that separates the metal layers [65]. This capacitance can be modelled by adding a capacitor C_S between the two ports of the R_S model as shown in Figure 4.6. Once again to calculate the Q-factor of this 'C_S model' an expression for the total impedance Z_{tot} is required and it is clear from the C_S model that Z_{tot} can be represented by equation (4.9) in parallel with the impedance of C_S given by $1/j\omega C_S$.

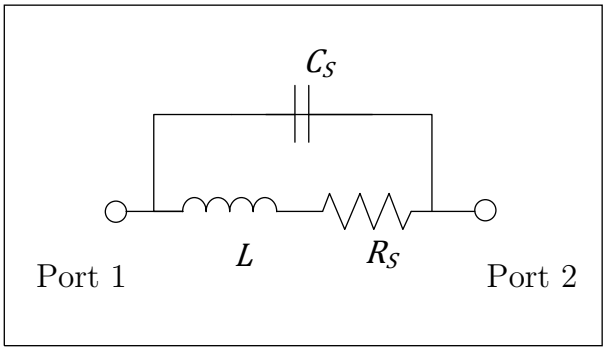

Figure 4.6 – C_S model of a spiral inductor including inductance L, series resistance R_S and capacitance C_S.

Therefore Z_{tot} for the C_S model can be derived as

$$Z_{tot} = (R_S + j\omega L)//\left(\frac{1}{j\omega C_S}\right)$$

$$Z_{tot} = \left[\left(\frac{1}{R_S + j\omega L}\right) + j\omega C_S\right]^{-1}$$

$$Z_{tot} = \frac{R_S + j\omega L}{1 - \omega^2 LC_S + j\omega R_S C_S} \tag{4.16}$$

To separate equation (4.16) into its real and imaginary components its numerator and denominator must both be multiplied by the complex conjugate of the denominator $(1 - \omega^2 LC_S + j\omega R_S C_S)$, which is $(1 - \omega^2 LC - j\omega RC)$. This changes the expression for Z_{tot} to

$$Z_{tot} = \frac{R_S + j\omega L}{1 - \omega^2 LC_S + j\omega R_S C_S} \times \frac{1 - \omega^2 LC_S - j\omega R_S C_S}{1 - \omega^2 LC_S - j\omega R_S C_S}$$

$$Z_{tot} = \frac{R_S - j\omega R_S^2 C_S + j\omega L - j\omega^3 L^2 C_S + \omega^2 LR_S C_S - \omega^2 LR_S C_S}{(1 - \omega^2 LC_S)^2 + \omega^2 R_S^2 C_S^2}$$

$$Z_{tot} = \frac{R_S + j\omega L - j\omega^3 L^2 C_S - j\omega R_S^2 C_S}{(1-\omega^2 L C_S)^2 + \omega^2 R_S^2 C_S^2} \tag{4.17}$$

The real and imaginary components of Z_{tot} can now be easily extracted and expressed as

$$Re[Z_{tot}] = \frac{R_S}{(1-\omega^2 L C_S)^2 + \omega^2 R_S^2 C_S^2} \tag{4.18}$$

and

$$Im[Z_{tot}] = \frac{\omega L - \omega^3 L^2 C_S - \omega R_S^2 C_S}{(1-\omega^2 L C_S)^2 + \omega^2 R_S^2 C_S^2} \tag{4.19}$$

respectively. Based on equation (4.10), the Q-factor of this model can be expressed as

$$Q = \frac{\omega L - \omega^3 L^2 C_S - \omega R_S^2 C_S}{(1-\omega^2 L C_S)^2 + \omega^2 R_S^2 C_S^2} \times \frac{(1-\omega^2 L C_S)^2 + \omega^2 R_S^2 C_S^2}{R_S}$$

$$Q = \frac{\omega L - \omega^3 L^2 C_S - \omega R_S^2 C_S}{R_S}$$

$$Q = \frac{\omega L(1-\omega^2 L C_S) - \omega R_S^2 C_S}{R_S} \tag{4.20}$$

The Q-factor of an Al inductor with L = 5 nH, n = 3.5, w = 10 μm, s = 3.5 μm, t_{m2} = 1.5 μm, t_{ox3} = 1 μm, and σ = 37.8 MSm^{-1} was calculated with varying frequency using equations (4.10), (4.14) and (4.20), and the results shown in Figure 4.7. As can be seen in Figure 4.7 the Q-factor frequency response of the C_S model for a spiral inductor has a bell shape and develops a maximum value Q_{max} at frequency (Q_{max}), which depends on the track loss R_S and the oxide and substrate losses.

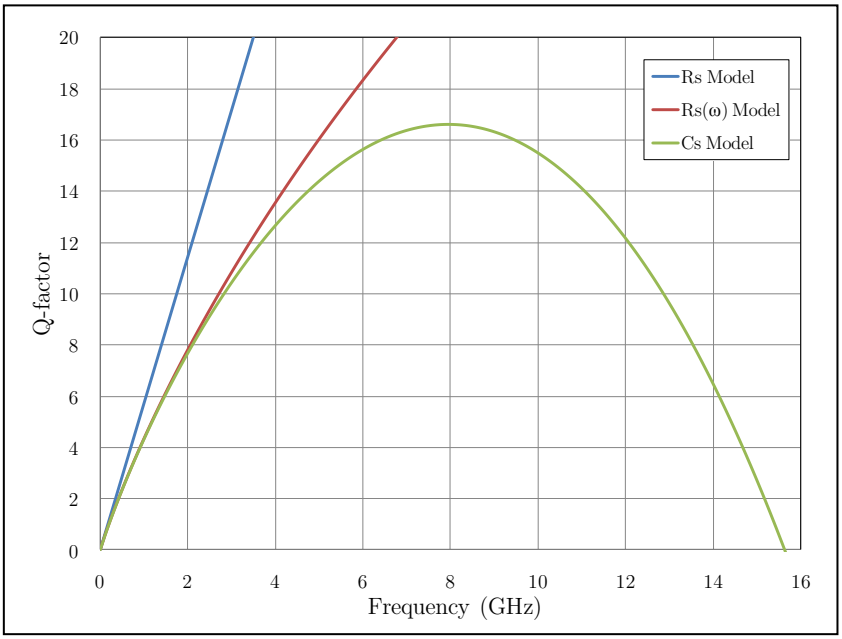

Figure 4.7 - Calculated Q-factor frequency sweep using different formulae, for a 5 nH ($n = 3.5$) inductor.

At higher frequencies capacitance C_S becomes so large that the Q-factor decreases and is eventually reduced to zero. The frequency at which this occurs is known as the self-resonant frequency and is the point where the inductor stops behaving like an inductor and starts to resemble a capacitor. The self-resonant frequency f_{SR} of the inductor can be derived by finding the non-zero frequency at which the Q-factor is zero. Using equation (4.20) for the C_S model the Q-factor becomes zero when

$$\omega^2 L^2 C_S = L - R_S^2 C_S$$

or when

$$\omega = \sqrt{\left(\frac{1}{LC_S} - \frac{R_S^2}{L^2}\right)}$$

For the same inductor modelled in Figure 4.7 with $l = 3$ mm and $d_{out} = 260$ μm, R_S at 10GHz and C_S were calculated using equations (4.11) and (4.15) to give 14.3 Ω and 0.02 pF respectively. Using these values $1/(LC_S) = 10^{22}$ s^{-2} while $R_S^2/L^2 = 8\text{x}10^{18}$ s^{-2} and therefore at

high frequencies near self-resonance $1/(LC_S) \gg R_S^2/L^2$. This along with the fact that $\omega = 2\pi f$ allows f_{SR} to be simplified as

$$f_{SR} = \frac{1}{2\pi\sqrt{LC_S}} \tag{4.21}$$

The C_S model and equations (4.20) and (4.21) help to predict the behaviour of spiral inductors but do not take into account any substrate or oxide losses beneath the inductor. For low frequencies, L and R_S can be determined accurately but at high frequencies, where the substrate losses dominate, the effects of the substrate and oxide layer must be taken into account. Commercial electro-magnetic field solvers can be used for this [69] however, due to the extensive computation times required, an equivalent circuit model that predicts the RF behaviour is more advantageous for design, simulation and optimization of inductors.

There has been extensive work performed on modelling substrate losses of spiral inductors, which requires accurate parameter extraction techniques. Figure 4.8 shows a commonly used [70–72] example of such a model while Figure 4.9 shows a cross-section of a spiral inductor, indicating the physical origin of the components.

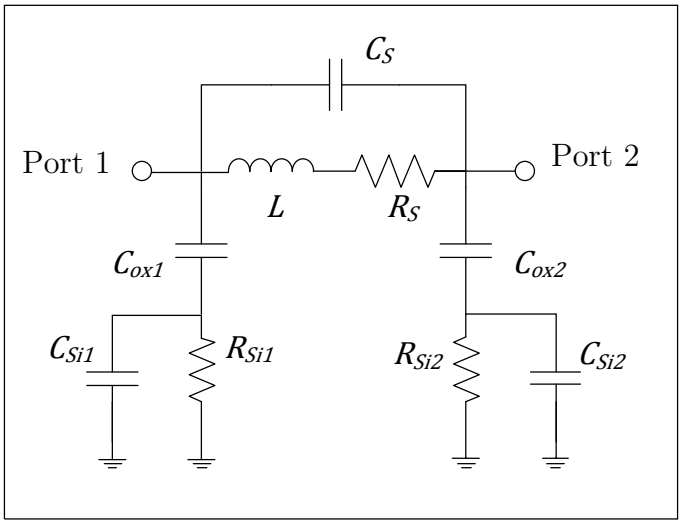

Figure 4.8 – Lumped element model of a spiral inductor that takes into account resistive, oxide and substrate losses. [70]

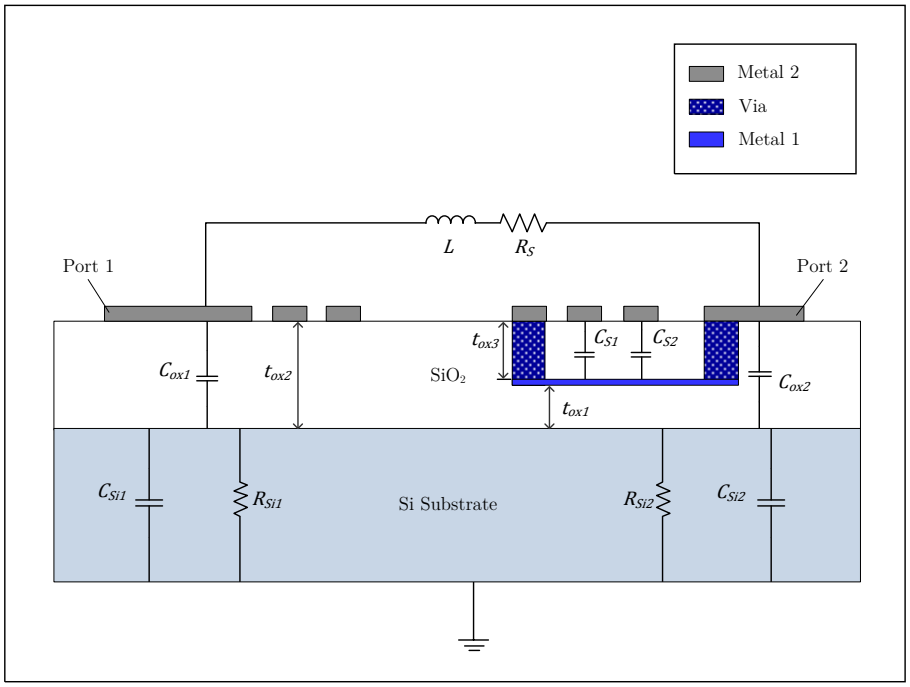

Figure 4.9 – Cross-section of a spiral inductor showing the physical origin of the components in the lumped element model of Figure 4.8.

The capacitance of the dielectric between the spiral and the substrate is represented by C_{ox}, and the substrate RF loss path to ground is represented by C_{Si} and R_{Si}, which are the capacitance and resistance of the Si substrate respectively. There are two components for each of these parameters in the model because the parasitics are assumed to be distributed equally between the two inductor ports, and the values are therefore equal and are given by

$$C_{ox} = \frac{1}{2} lw \frac{\varepsilon_{ox}}{t_{ox2}} \tag{4.22}$$

$$C_{Si} = \frac{lwC_{sub}}{2} \tag{4.23}$$

and

$$R_{Si} = \frac{2}{lwG_{sub}} \tag{4.24}$$

where C_{sub} and G_{sub} are the substrate capacitance and conductance per unit area, respectively, and are functions of substrate doping [65]. At low operating frequencies the electric field generated from the inductor magnetic flux is confined within the oxide layer. At f_{SR} however the electric field increases to a point beyond the oxide layer and capacitively couples through the substrate, causing substrate losses C_{Si} and R_{Si}. C_{Si} models the high-frequency capacitive effects occurring in the semiconductor, while the physical origin of R_{Si} is the Si conductivity, determined by the carrier concentration. Therefore increasing the substrate resistivity will increase the value R_{Si} and thereby reduce substrate losses. Examples of such methods used to maximise the Q-factor of spiral inductors as well as other techniques are discussed in the following section.

4.4 Maximising Spiral Inductor Quality Factor

Although a high Q-factor is not always desired in inductor applications, it results in low phase noise, low noise figure LNA, reduced pass-band insertion loss for narrow band filters and generally lower power consumption and improved receiver sensitivity in RF applications. These among other reasons make a high Q-factor an essential feature for RFIC inductors. Spiral inductors however have much lower Q-factors than their coil counterparts mainly due to their planar nature and the lack of a ferromagnetic core, which cannot be used at frequencies beyond 1 GHz due to high polarisation losses and low permeability [13]. There has hence been a great deal of research in improving spiral inductors efficiency in the GHz frequency range to levels closer to those experienced by their coil counterparts.

Optimising RF spiral inductors involves tweaking many different geometric and technological parameters during inductor design to maximise Q_{max}, $f(Q_{max})$ and f_{SR}. As mentioned earlier, the Q-factor of a spiral inductor is mainly limited by the resistance of the metallisation at low frequencies and losses in the conductive substrate at higher frequencies. Therefore to maximise the Q-factor R_S and C_S as well as the substrate losses determined by C_{ox}, R_{Si} and C_{Si} must be reduced. Examples of the many different techniques employed to optimise the

performance of spiral inductors in literature are included in this section. Details of the techniques mentioned and the values of Q_{max}, $f(Q_{max})$ and f_{SR} are summarised in Table 4.1.

Series resistance R_S can be reduced using a variety of different methods, all of which involve optimising the inductor physical layout and conductor material. At RF the proximity effect causes the inner tracks of a spiral to have a high resistance, due to current travelling in an opposing direction in nearby tracks [73]. By removing the centre windings of the spiral, or decreasing the fill-ratio, R_S can be reduced. Such inductors are known as hollow-coil inductors and are commonly used in RFICs. It is interesting to note that large inductance values typically combine with comparably small Q-factor values, which seems to disagree with equation (4.10). This is because as the inductance increases so does the area and in turn track length l, which results in a proportionally higher series resistance. In other words for a given inductor area a small inductance value leads to a comparably larger Q-factor [74].

R_S can also be reduced by using thick metal layers for the spiral. Another technique to reduce R_S is the use of metals with low sheet resistances such as copper (Cu) or Au. These types of metals however experience smaller skin depths at RF due to their increased conductivity, as can be seen from equation (4.13), and hence higher RF resistances. Numerous techniques have been applied in research to reduce R_S of spiral inductors. 10 nH Al inductors with a thickness of 4 μm and a dielectric thickness of 10 μm, to reduce the resistance and the capacitance of the spiral respectively, produced Q_{max} values of 5.5 at 1.2 GHz ($f(Q_{max})$) [75]. Choi *et al.* [76] also investigated the effect of metal thickness on Q-factor, and produced inductors with Q_{max} of 46 at 2 GHz using 20 μm thick copper tracks. Another technique for reducing resistance involves taking advantage of multilevel interconnect technology and using multiple metal layers shunted together to produce an effectively thicker track. One such method used 4 Al-Cu layers with the top three shunted together and the fourth used as an under pass. 1 μm thicknesses were used for the first three Al-Cu layers, and 2 μm for the top-most layer. The metal layers were separated by 1.5 μm oxide layers between each of them, and the substrate was separated from the lowest metal by a 4.5 μm oxide [77]. A peak Q-factor of 9.3 was measured at 4 GHz which is a great increase when compared to other solutions that involve Si

substrates. Inductors were also fabricated with Au tracks using the same technique but with a fifth metal layer, increasing the dielectric between the substrate and the inductor to 6 μm. This increased thickness along with the use of Au, which has a higher conductivity, lead to a Q_{max} value of 24 at 2.3 GHz [78]. The large thicknesses necessary for these solutions introduce added stress on the substrate and add immensely to the cost and complexity, making them impractical for standard RFIC fabrication. It must also be noted that Q-factor degradation at high frequencies can be attributed mainly to substrate losses [70]. Hence a solution to tackle substrate losses is more effective than reducing the resistance for RF operation.

As mentioned earlier underpass capacitance C_S decreases the Q-factor at high frequency eventually leading to self-resonance. A different approach to increasing Q-factor therefore involves reducing C_S by increasing the thickness of the dielectric between the spiral track and the underpass. A thick dielectric also helps to decrease C_{ox} and reduce substrate effects also leading to an improved Q-factor. The spiral layer of the inductor is hence fabricated on the top most metal layer and thick dielectric layers are used in between the spiral and the substrate. Inductors with a Q_{max} of 53 at 2 GHz, were produced using 20 μm thick copper tracks on a 50 μm embedded oxide island [79]. Similar methods includes the introduction of floating inductors to isolate the spiral track from the substrate but these techniques are not very practical [68].

The main problem with these techniques is that none of them tackle the RF loss factor, which is substrate loss related and caused by eddy currents. Substrate losses can be almost completely eliminated through the integration of MEMS-etched air-gaps below the inductors [72] or removal of the underlying Si by selective etching of the substrate followed by bonding onto quartz substrates [74]. An example of such was produced using chrome/Cu inductors that achieved a Q_{max} of 17 at 1 GHz, created by selectively removing the substrate material under the spiral using a wet etch process [80]. Similarly surface micromachining techniques were used by Yoon *et al.* to create an air suspended inductor with a Q_{max} of 70 at 6 GHz [81]. A self-assembly technique was used by Kiziroglou *et al.* to produce vertically oriented Au meanders [82]. The structures were fabricated in-plane atop a sacrificial photoresist before a

Ni/Sn hinge was deposited to connect it to contact pads. The photoresist was then stripped releasing the structure from the substrate and the hinge reflowed rotating the structure 90° out-of-plane. An increase of over 70% was measured with a Q_{max} of 9.5 at 5 GHz. These nonconventional VLSI processes however require additional process steps and photolithography masks that increase fabrication and package costs.

A different method of reducing substrate losses that aims to isolate the inductor from the substrate is the use of a patterned ground shield in the dielectric under the spiral, which can be a metal layer or a polycrystalline Si film. The purpose of this is to obstruct the transient electric field and electro-magnetic wave from penetrating into the substrate causing eddy currents to be induced in the shield instead of in the substrate [83]. The conductivity of the shielding layer, however, must be determined carefully since if the shielding layer is highly conductive significant losses occur and the Q-factor is actually degraded, while a highly insulating layer will be transparent to electric field and not enhance the Q-factor at all. It is also important to note that despite increasing Q_{max}, use of a patterned shield reduces the self-resonant frequency [13].

Other methods of reducing the substrate losses involve using materials with higher resistivities than Si. Q-factor measurements performed on inductors fabricated on Si and GaAs have shown that GaAs substrates provide higher peak Q-factors at higher frequencies; Q_{max} of 8 at 3 GHz compared to Q_{max} of 5 at 1.5 GHz for Si. It has also been reported in this work that passives on Si with resistivities of 3 - 7 kΩcm exhibit performances comparable to passives on GaAs [58]. Yin *et al.* have also created double-level, spiral inductors on GaAs that achieve Q_{max} values of 75 at 6 GHz [84]. Glass substrates and 3.5 μm Al tracks were also shown to improve the Q_{max} of inductors to 39 at 4.3 GHz [21]. The lack of a native oxide as well as thermal stability issues associated with these substrates however make Si substrates a more attractive option.

Several methods have been proposed to attempt to improve the resistivity of Si, including the adoption of SOI technology which can reduce parasitic capacitance and substrate absorption.

It has been extensively shown that SOI CMOS spiral inductors exhibit higher Q_{max}, $f(Q_{max})$ and f_{SR} values than identical inductor on Si. For a shunted, 2 metal layer inductor Q_{max} was found to be 7.7 at 1.3 GHz [85]. A different technique involves manipulating the Si substrate itself to increase its resistivity. It has been shown that using Si substrates with resistivities of 2 kΩcm and an Al thickness of 4.1 μm Q_{max} values of 20 can be achieved at frequencies of 3.25 GHz [86]. Another technique to increase Si resistivity involves proton implantation as mentioned earlier, which has been shown to increase substrate resistivity from 10 Ωcm to 10^6 Ωcm, thus improving the Q_{max} value from 6.3 at 3 GHz to 10.6 at 4 GHz [72]. The performance of inductors on FZ-Si, with resistivities greater than 1 kΩcm, has also been compared to standard Si and sapphire substrates by Burghartz *et al.* who have shown Q_{max} values of 18 at 3.7 GHz, 30 at 5.2 GHz, and 40 at 5.8 GHz, for inductors on standard Si, float-zone Si, and sapphire respectively [17].

The summary in Table 4.1 shows that increasing the resistivity of Si wafers can lead to higher Q-factors at RF. To validate this spiral inductors were designed and the Q-factors simulated as detailed in the following sections.

TABLE 4.1
A summary of inductor parameters as reported in literature, highlighting the different fabrication techniques used.

Description	Turns	Area (μm^2)	L (nH)	Q_{max}	$f(Q_{max})$ (GHz)	f_{SR} (GHz)
4μm Al on 10μm polyimide [75]	-	100x100 (inner)	9.3	5.5	1.2	6
20μm Cu [76]	3	380x380	5	46	2	> 5
3 shunted AlCu layers, on 4.5μm oxide [77]	4	226x226	1.95	9.3	4	20
4 shunted Au layers, on 6μm oxide [78]	3	225x226	1.45	24	2.5	> 20
20μm Cu on 50μm oxide island [79]	2	500x500	0.9	53	2	> 10
5μm circular Cr/Cu on wet etched substrate [80]	2	785x785	3.2	17	1	8.5
10μm Cu air-suspended[81]	1.5	330x330	1.4	70	6	20
5.3μm Au, out-of-plane rotated meanders [82]	-	800x300	-	9.5	5	> 6
Spiral on Si [58]	6	-	-	5	1.5	> 3.1
Spiral on GaAs [58]	6	-	-	8	3	6
3.5μm circular Al on Glass [21]	2	600 μm (diameter)	2.6	39	4.3	10.5
2 shunted layers, on SOI [85]	10.5	405x405	25	7.7	1.3	> 10
4.1μm Al on Si (ρ=2kΩcm) [86]	8	-	11.9	20	3.25	8
2μm Al, on proton implanted wafer[72]	3.5	256x256	4.6	10.6	4	10
3 shunted 2.5μm Cu layers on Si (ρ=10Ωcm) [17]	226x226		1.4	18	3.7	> 15
3 shunted 2.5μm Cu layers on FZ-Si (ρ=1kΩcm) [17]				30	5.2	
3 shunted 2.5μm Cu layers on sapphire [17]				40	5.8	

4.5 Spiral Inductor Design

Spiral inductor design and optimisation is a complicated process owing to the large number of parameters that can be tweaked to change inductor behaviour. To begin with values for w and s were chosen. Because s is the minimum feature size, a value of 3.5 μm was chosen to allow inductor fabrication using 3 μm technology. Although increasing w reduces R_S this also increases the inductor area and there is therefore a trade-off between lowering R_S and reducing layout area, hence a commonly used value of 10 μm was selected for w. These values as well as equations (4.1), (4.3) and (4.5) were used to calculate the inductance of an inductor with w = 10 μm, s = 3.5 μm, n = 2 and d_{out} = 200 μm (r = 100 μm, a = 88.25 μm, d_{avg} = 176.5 μm). The inductances calculated from these equations in Table 4.2 show there is an insignificant difference between them. Since the exact inductance in this work is not important the simpler and more commonly used expression of equation (4.1) was chosen for the design of the inductors in this work because of its simplicity.

TABLE 4.2
Comparison between inductances calculated using various formulae
(n= 2, d_{out}= 200 μm, r= 100 μm, a= 88.25 μm, d_{avg}= 176.5 μm).

	Formula	L (nH)
Common Expression [65]	$L = \frac{37.5\mu_0 n^2 a^2}{22r - 14a}$	1.522
Modified Wheeler Formula [66]	$L = K_1\mu_0 \frac{n^2 d_{avg}}{1 + K_2\rho}$	1.520
Current Sheet Approximation [65], [66]	$L = \frac{\mu_0 n^2 d_{avg} c_1}{2}\left[ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2\right]$	1.561
Average		1.534

As explained earlier high Q-factor inductors are required for RFICs which result from lower inductance values, and therefore common values of 5 nH, 10 nH and 50 nH were selected. Equation (4.1) was used to calculate the widths of 5 nH and 10 nH inductors with 3.5 turns, and a 50 nH inductor with 5.5 turns, all with $w = 10$ μm and $s = 3.5$ μm. Table 4.3 shows the results of these calculations.

After all the planar parameters of the inductors were determined, software L-Edit was used to design photolithography masks for fabrication. Owing to the difficulty of fabricating devices with multiple metal layers and the lack of planarisation facilities in the Southampton Nanofabrication Centre inductors with underpasses and wire-bonded overpasses were designed to increase the chances of fabricating functioning inductors. The 5 nH inductor was designed with an underpass, while the 50 nH inductor was designed to have a wire-bonded overpass. Designs for both an underpass and an overpass were created for the 10 nH inductor. The spiral tracks were designed on one layer for both types of inductors with the underpass and vias of the underpass inductors on two lower layers.

GSG contact pads were added to the spiral track layer with a signal track width of 50 μm and a common ground track shared on either side of the inductor to allow for measurements using GSG probes. When conducting tracks with different widths are connected together a large proportion of RF signals is reflected at the junction reducing the transmitted proportion of the signal. To avoid this, a common RFIC design technique that involves tapering or constricting the wider track down to the width of the other track with an angle of 60° was employed.

TABLE 4.3
Calculated inductor widths for the various inductors.

L (nH)	n	d_{out} (μm)
5	3.5	260
10	3.5	412
50	5.5	788

This reduces the reflected proportion of the signal when compared to an abrupt 90° junction. Thus the 50 μm GSG signal track was tapered down to the 10 μm inductor spiral track. The overpass and underpass inductors as designed in L-Edit are shown in Figure 4.10 and Figure 4.11 respectively, showing the GSG pads, wire-bonding pads and underpasses.

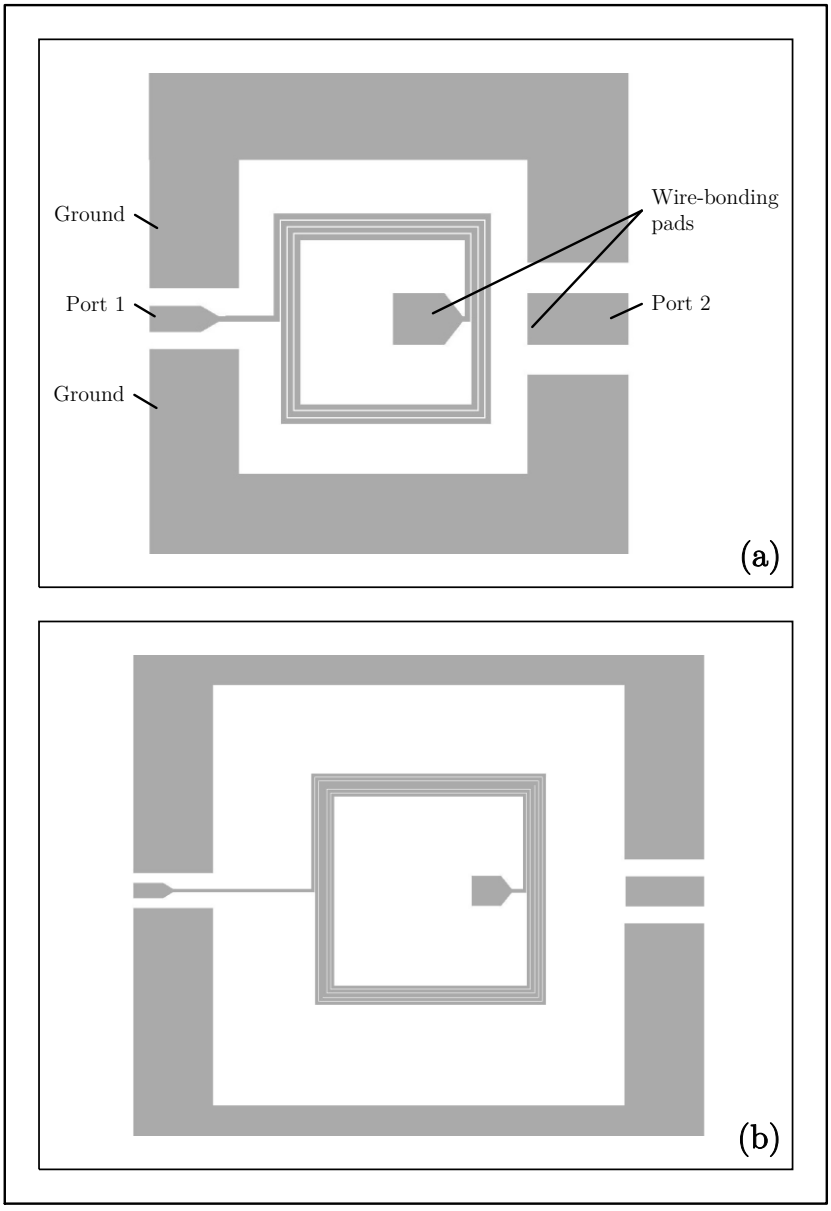

Figure 4.10 – Samples of the photolithography mask designed showing (a) the 10 nH, and (b) the 50 nH overpass inductors.

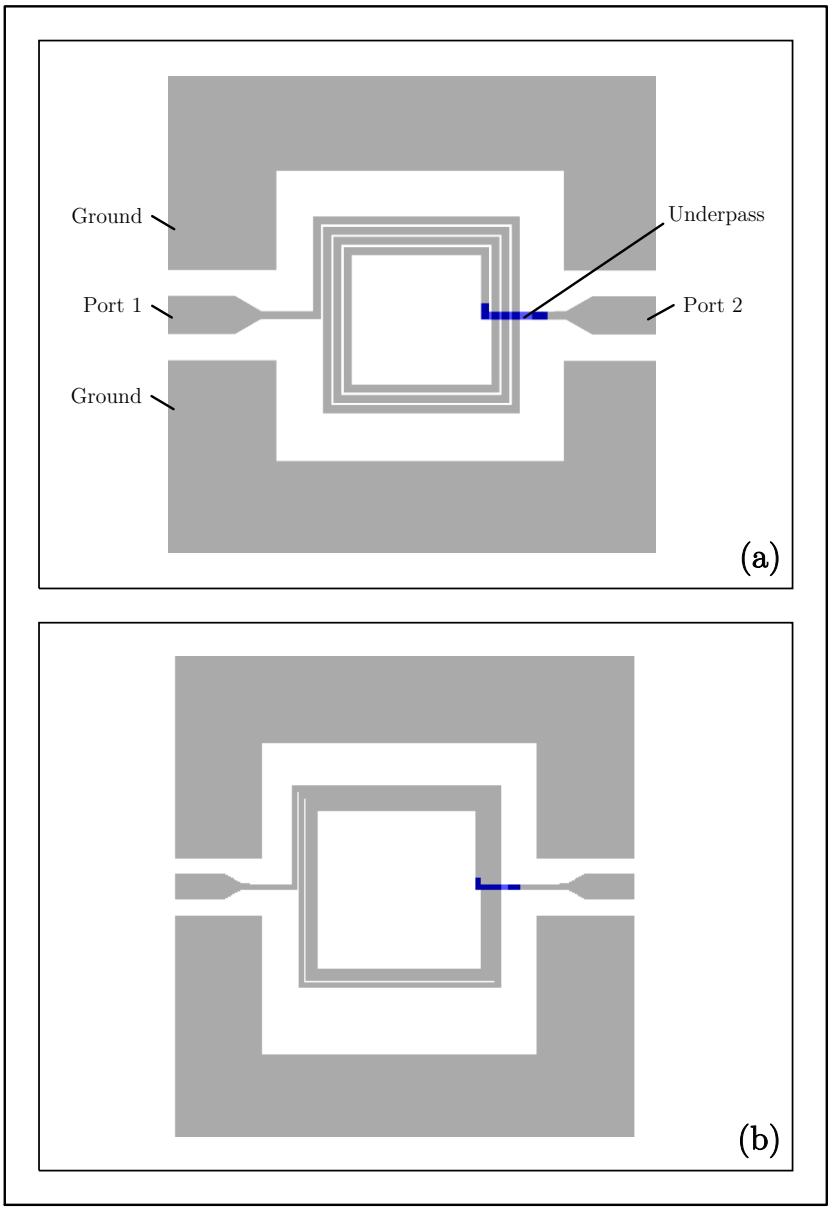

Figure 4.11 - Samples of the photolithography masks designed showing (a) the 5 nH and (b) the 10 nH underpass inductors. The blue tracks represent the underpasses on a different mask layer. The via layer has been omitted.

As mentioned earlier, the skin effect restricts current to the edges of a conductor at high frequencies. For this reason, to connect the two metal layers together multiple small vias were designed which provide a larger surface area than one large via. This technique increases current flow thereby reducing the via resistance at high frequencies. Figure 4.12 shows a sample of the mask with the 5 nH inductor along with the via layer.

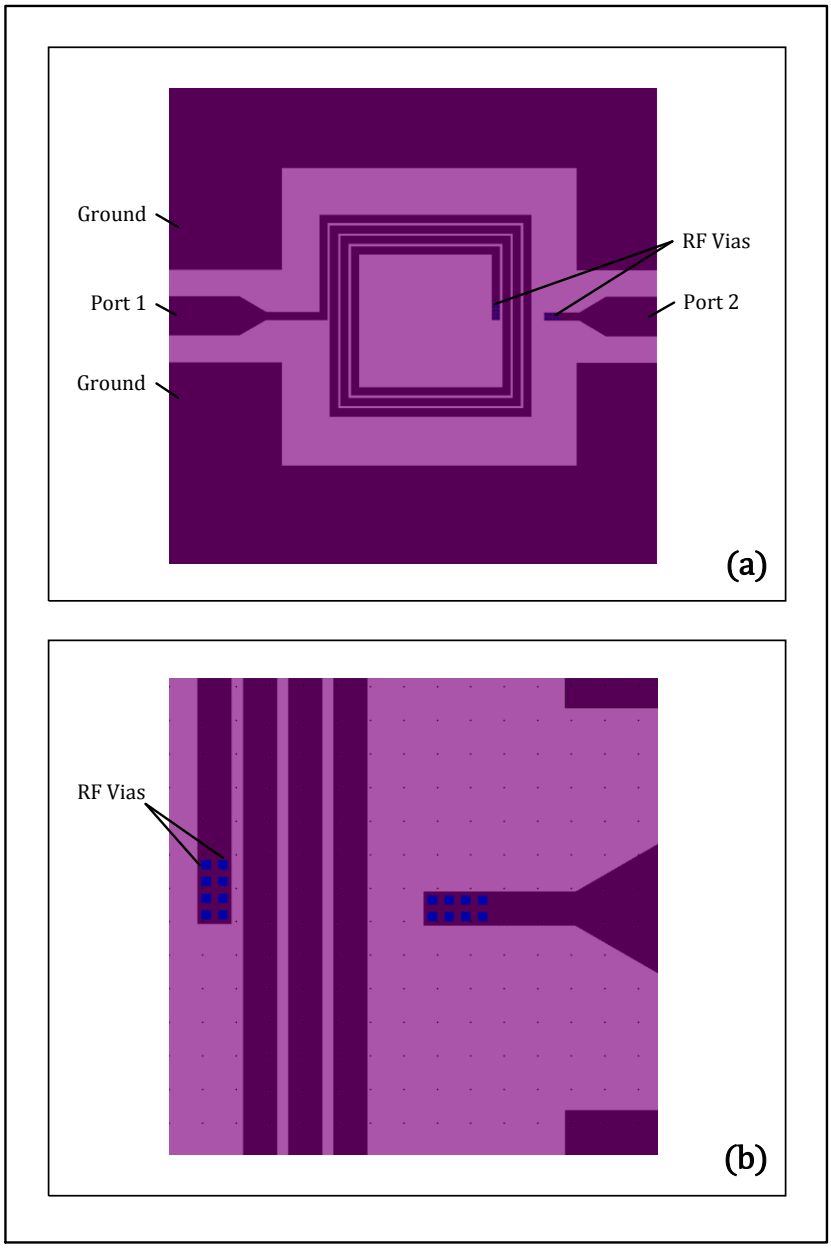

Figure 4.12 – Selected areas of the photolithography mask showing (a) the 5 nH inductor with the via mask layer (purple), and (b) a close-up of the vias. The underpass (blue) can only be seen through the via holes as it is the lowest mask layer.

The final geometric parameter set was the thickness of the spiral track t_{m2} which must be maximised to minimise R_S. However values of t_{m2} larger than the skin depth are ineffective at reducing R_S at RF as they are effectively reduced to the skin depth. A graph of the skin depth of an Al track is shown in Figure 4.13.

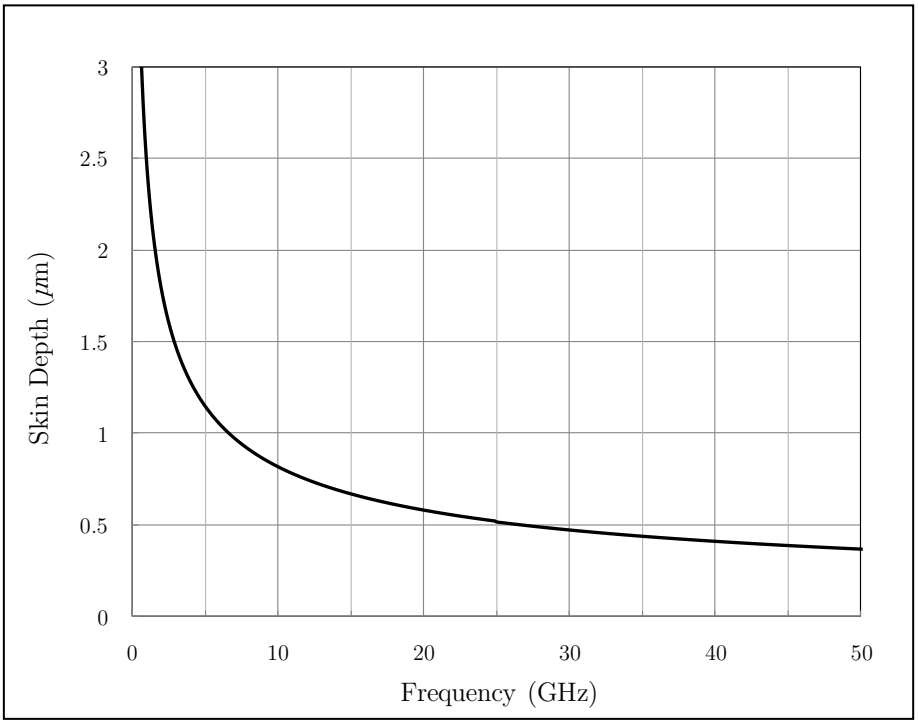

Figure 4.13 – Calculated skin depth of Al with varying frequency, showing the desired frequency range of 5 - 50 GHz.

From this it can be seen that within the desired frequency range of 5 – 50 GHz the skin depth of Al has a maximum value of 1.16 μm at 5 GHz, so any thicknesses larger than this value would effectively be reduced to this. Figure 4.14 shows a plot of $R_S(\omega)$ per length in millimetres against $1/t_{m2}$ for an Al track with a 10 μm width at different frequencies, with t_{m2} values of 0.5 μm, 1 μm, 1.5 μm and 2 μm highlighted by dashed lines as indicated. The percentage reductions in $R_S(\omega)$ with incremental increases in t_{m2} have been extracted at 5 GHz, 10 GHz and 50 GHz from the graph and are displayed in Table 4.4. These results indicate that increasing thickness above 1.5 μm provides no significant decrease in $R_S(\omega)$ even at 5 GHz and hence the spiral thickness t_{m2} was chosen as 1.5 μm. The thickness of the underpass t_{m1} which also contributes to R_S was set to 0.5 μm and not 1.5 μm since the latter would complicate the already complex fabrication process.

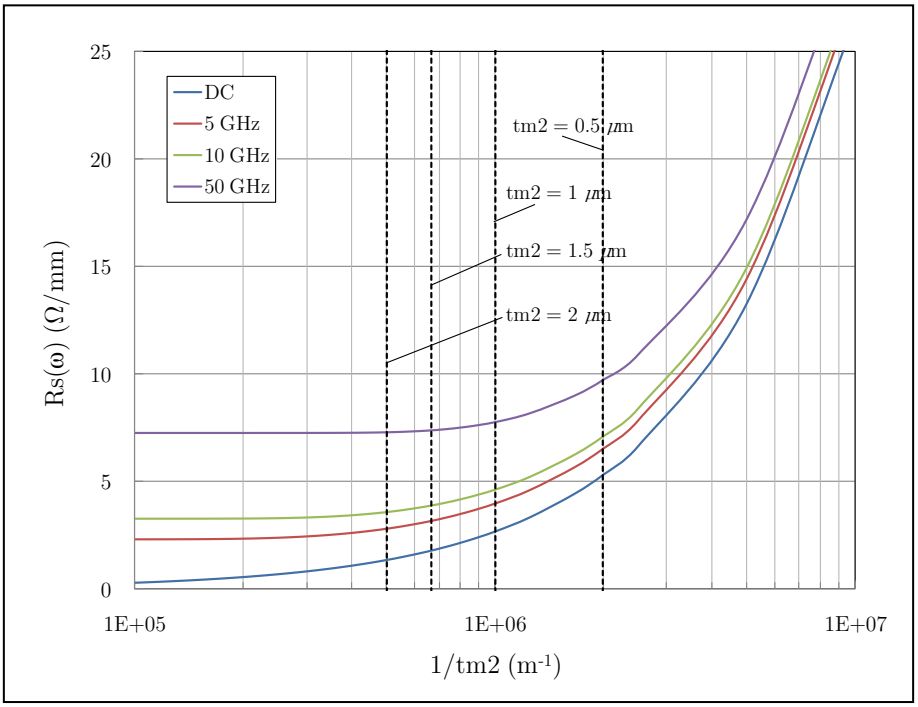

Figure 4.14 – $R_S(\omega)$ per millimetre against $(1/t_{m2})$ for an Al track with w=10 μm and at different frequencies. Dashed lines highlight t_{m2} thicknesses of 0.5 μm, 1 μm, 1.5 μm and 2 μm as indicated.

TABLE 4.4

Reductions in series resistance for increases in metal track thickness in the 5–50 GHz frequency range.

Increase in t_{m2}	Percentage decrease in $R_S(\omega)$		
	5 GHz	10 GHz	50 GHz
0.5 μm → 1 μm	39.4	35.2	20.3
1 μm → 1.5 μm	20.4	16.0	4.9
1.5 μm → 2 μm	11.7	8.0	1.2
2 μm → 2.5 μm	7.0	4.2	0.3

With the geometric parameters chosen the thickness of the oxides t_{ox1} and t_{ox3} were next selected. A 1 μm oxide was chosen for the dielectric between the underpass and the substrate to reduce microwave absorption without greatly increasing the fabrication time and complexity. As t_{ox3} increases, the values of C_{ox} and C_s decrease but it becomes increasingly difficult to etch the small RF via holes and fill them with metal. For this reason a value of 0.5 μm was chosen for t_{ox3}.

4.6 Spiral Inductor Quality Factor Simulations

ASITIC [87] is a simulation CAD software program capable of quickly simulating the behaviour of inductors based on given parameters. It was therefore used to determine whether increasing substrate resistivity would lead to an increase in Q-factor. ASITIC creates a model for the inductor, similar to the lumped element model of Figure 4.8, and assigns values to the model components, based on the inductor design and user specified substrate parameters. The program then simulates the behaviour of this circuit taking into account skin and proximity effects, as well as the effects of substrate eddy currents. Using ASITIC it is possible to quickly simulate frequency-dependent Q-factor behaviour. To simulate behaviour on a particular substrate, ASITIC uses a customisable technology file that contains technological parameters such as thicknesses and resistivities of the different layers to be fabricated. First this technology file was edited to match the metal and oxide thicknesses chosen previously as illustrated in Figure 4.15. This technology file has been included in Appendix C. It must be noted that ASITIC can only accurately simulate the behaviour of inductors if metal 2 is within the dielectric.

In order to verify the validity and accuracy of ASITIC the Q-factor of a 5 nH inductor with 3.5 turns was simulated over a frequency range, and compared to the values calculated earlier using equation (4.20) and displayed in Figure 4.7.

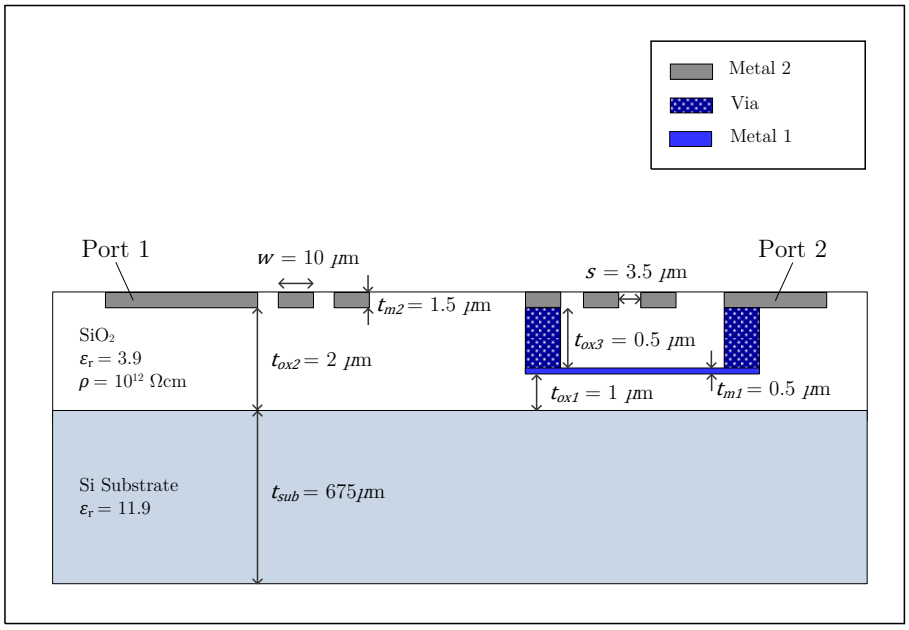

Figure 4.15 – Graphical representation of the ASITIC technology file given in Appendix C and used in this work to simulate inductor behaviour.

The technology file was first edited to place the inductor entirely within SiO_2, with no Si substrate beneath it so as to remove any Si substrate related losses, and the ASITIC simulated Q-factor frequency sweep was plotted along with the calculated results as given in Figure 4.16. It can be seen from this graph that although the values of f_{SR} differ only slightly, the simulated Q-factors are lower than the theoretical behaviour. This difference may be a result of ASITIC taking into account certain loss mechanisms, such as those due to the oxide beneath the inductor, which are not taken into account in equation (4.20). The calculated values of L and $R_s(\omega)$ were also very close to those calculated by ASITIC as can be seen in Table 4.5. These results suggest that ASITIC is reasonably accurate in predicting inductor behaviour and it was therefore used to simulate the effect that increasing substrate resistivity has on inductor Q-factor.

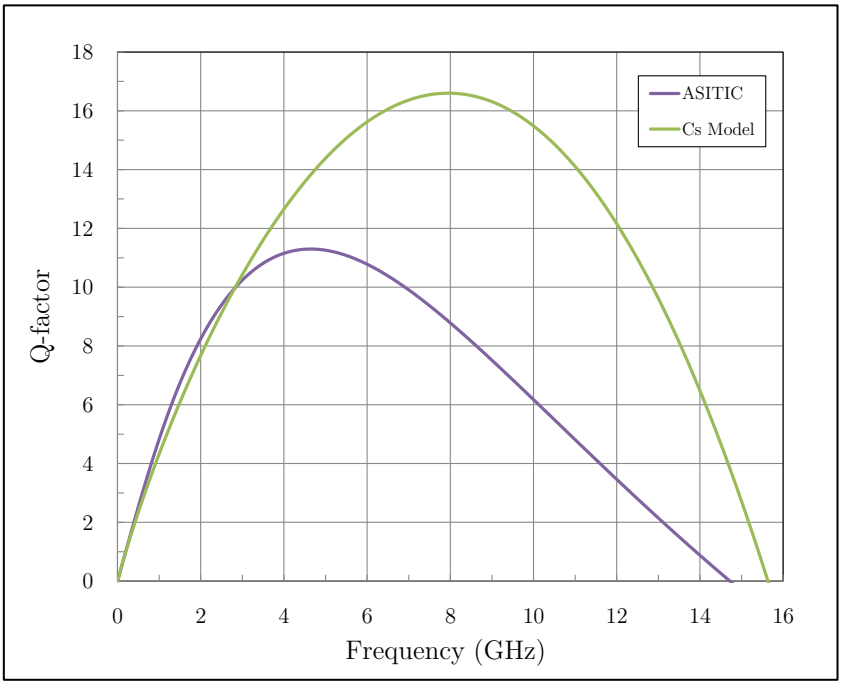

Figure 4.16 – Comparison between Q-factor frequency sweeps calculated using the equation (4.20) (C_S model) and simulated using ASITIC, for a 5 nH inductor with 3.5 turns.

TABLE 4.5
Calculated and ASITIC simulated DC inductance and series resistance values for a 5 nH inductor with 3.5 turns.

	Theoretically Calculated	ASITIC Simulated
L (nH)	5.0	5.1
R_s (Ω)	5.5	6.2

The Q-factor behaviour of a 10 nH inductor with 3.5 turns, on substrates with different resistivities was simulated and the results shown in Figure 4.17 illustrate that as the resistivity of the substrate increases not only does the value of Q_{max}, so does the value of $f(Q_{max})$ leading to an inductor that is generally more desirable for RFICs.

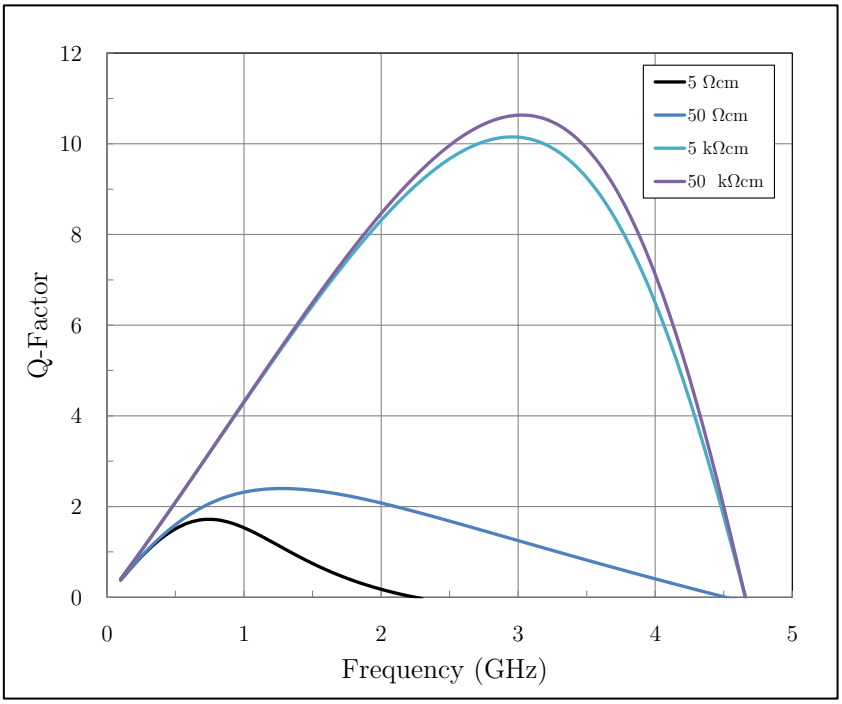

Figure 4.17 – Frequency sweep of the Q-factor of a 10 nH inductor with 3.5 turns, simulated on substrates of different resistivities in ASITIC using the technology file in Appendix C.

This simulation shows that it is possible to increase the efficiency and operating frequency range of a spiral inductor by increasing substrate resistivity. The simulation also confirms that there is not much of an increase in Q_{max} when increasing the resistivity from 5 kΩcm to 50 kΩcm and therefore resistivity values as high as 5 kΩcm should suffice in improving the microwave performance of spiral inductors.

4.7 Fabrication of Spiral Inductors

The spiral inductors were fabricated on a wafer implanted with a Au dose of $4\text{x}10^{13}$ cm^{-2} and annealed at 950°C before an oxide strip and Au etch, as well as on an unimplanted wafer with a relatively low resistivity of 56 Ωcm. Overpass inductors were also fabricated on a FZ-Si

wafer with a resistivity of 450 Ωcm. The fabrication process required for planarised inductors is much more complex than that used for the CPWs as illustrated in Figure 4.18.

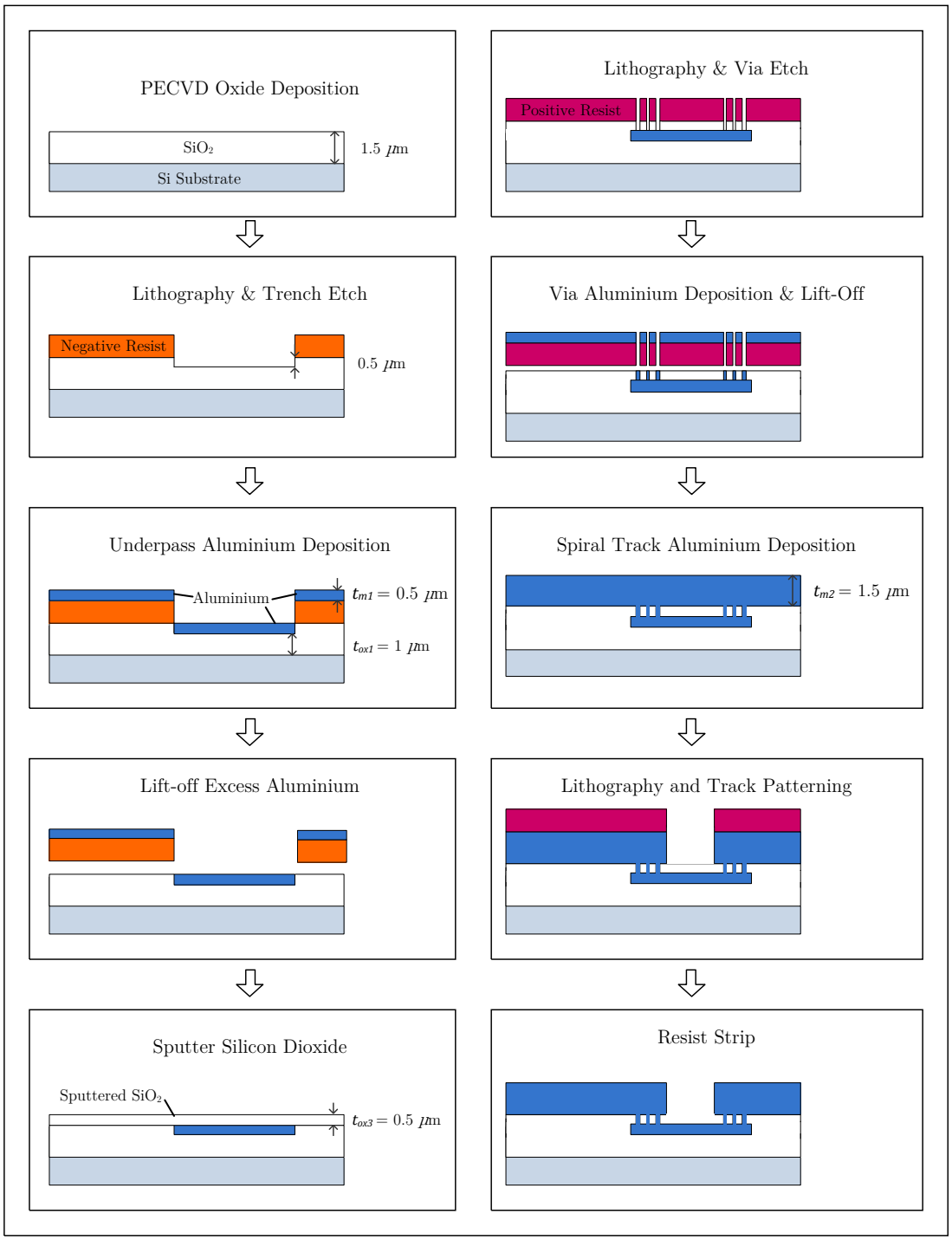

Figure 4.18 – Process steps used for the fabrication of the underpass spiral inductors to ensure more planarised final devices.

First the wafers were cleaned with a 15 minute FNA dip, after which a 1.5 μm oxide was deposited using a plasma enhanced chemical vapour deposition (PECVD) method and silane, nitrous oxide and nitrogen gasses, at 350°C in an Oxford Instruments OPT Plasmalab 100 system. This initial oxide acts as both the 1 μm underlying oxide and a 0.5 μm oxide surrounding the underpasses so as to planarise the device. MicroChemicals' negative photoresist AZ2070 was next spun atop the wafers before soft baking at 110°C for 90 seconds. The resist was then exposed to light through the photolithography mask for 5.5 seconds with the mask aligner. The resist received a post-exposure bake at 110°C for 90 seconds after which it was developed with a 70 second dip in MicroChemicals AZ 726 solution. This process created an AZ2070 mask for etching trenches with depths of 0.5 μm for the underpasses using a dry, reactive ion etching (RIE) process in an Oxford Instruments Plasmalab 80 plus system. These trenches were filled with Al by evaporating a 0.5 μm layer at a rate of 0.25 nm/s, after which the resist and the excess Al were removed by a lift-off process with N-Methyl-2-pyrrolidone (NMP) solvent followed by a quick dip in FNA.

Exposing Al to high temperatures can cause damage to the Al due to electromigration and for this reason the 0.5 μm inter-metal oxide layer was sputtered at 50°C and at a rate of 0.55 nm/s, using a Leybold Optics Helios Pro XL. Next a S1813 mask for etching the via holes was patterned and the via holes were etched using the same process used to etch the underpass trenches. The etched vias and underlying underpass are shown in Figure 4.19. The via holes were filled with 0.5 μm of Al using the same lift-off process used for the underpasses. The 1.5 μm Al spiral track was next evaporated before an S1813 resist was patterned to protect the desired Al. The unwanted excess Al was subsequently removed using a 6 minute wet etch at 40°C in Al etchant. Finally an FEK Delvotec 5430 wire-bonder was used to bond thin Al wires between the wire-bonding pads to create the overpasses for the overpass inductors.

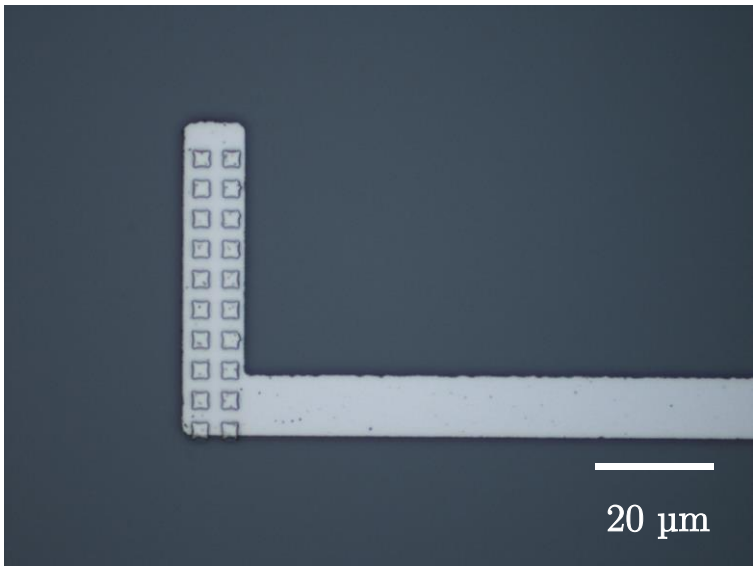

Figure 4.19 – Image of an inductor underpass and etched via holes, as observed on the wafer surface using an optical microscope.

Images of completed overpass and underpass inductors taken using an optical microscope are shown in Figure 4.20 and Figure 4.21 respectively. The underpass of the 5 nH inductor is shown in more detail in Figure 4.22. After the final step was completed a profilometer was used to check the uniformity of the process by running its needle across the oxide above the underpass along the path of the dashed yellow line in Figure 4.22. The results given in Figure 4.23 show a step of only approximately 110 nm which is much smaller than the 500 nm that would have resulted without planarisation.

The S-parameters of the completed inductors were measured with the same equipment used to analyse the CPWs and the results are included in the following section.

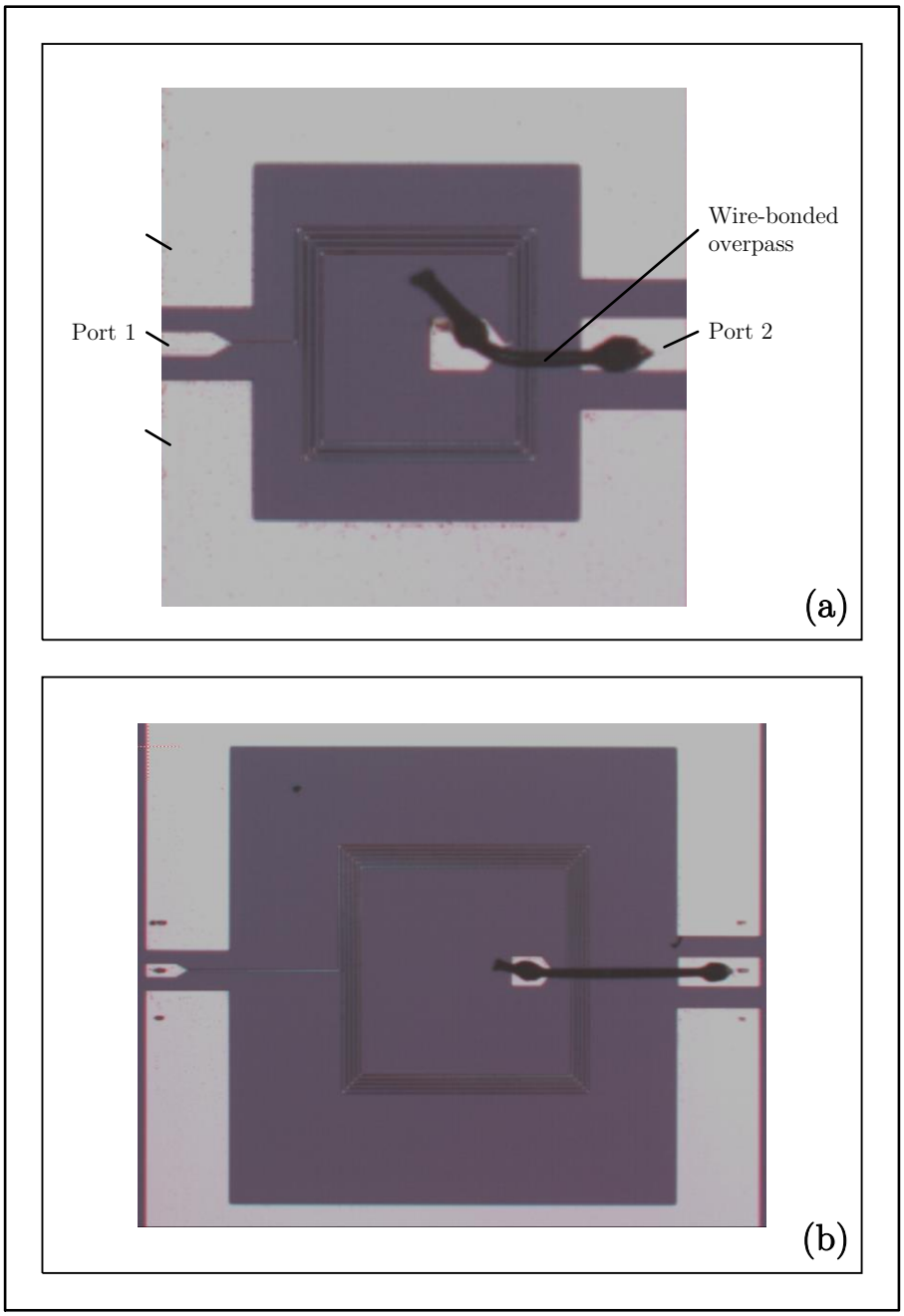

Figure 4.20 – Images of (a) a 10 nH and (b) a 50 nH overpass inductor, as observed on the wafer surface, using an optical microscope.

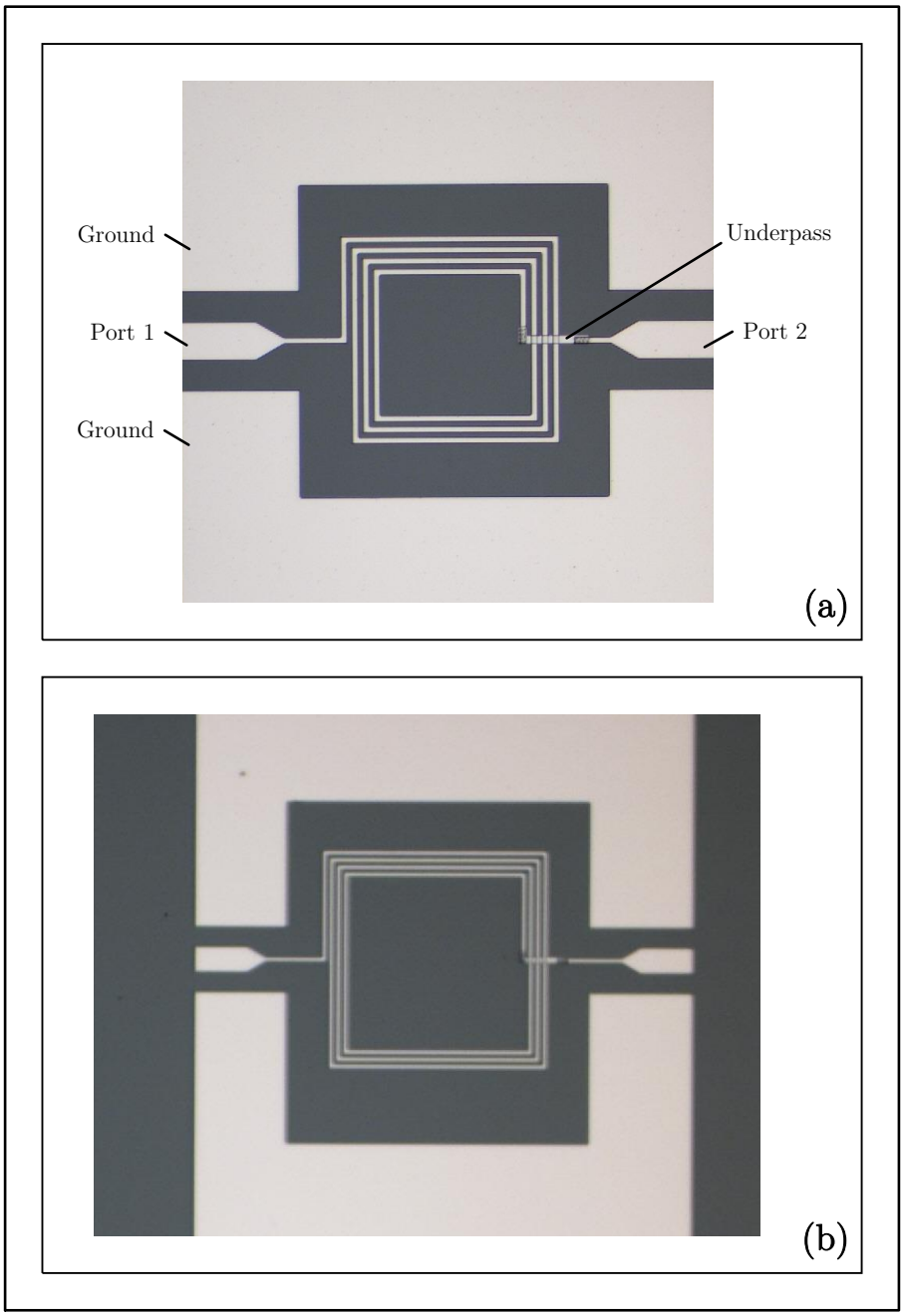

Figure 4.21 – Images of (a) a 5 nH and (b) a 10 nH underpass inductor, as observed on the wafer surface, using an optical microscope.

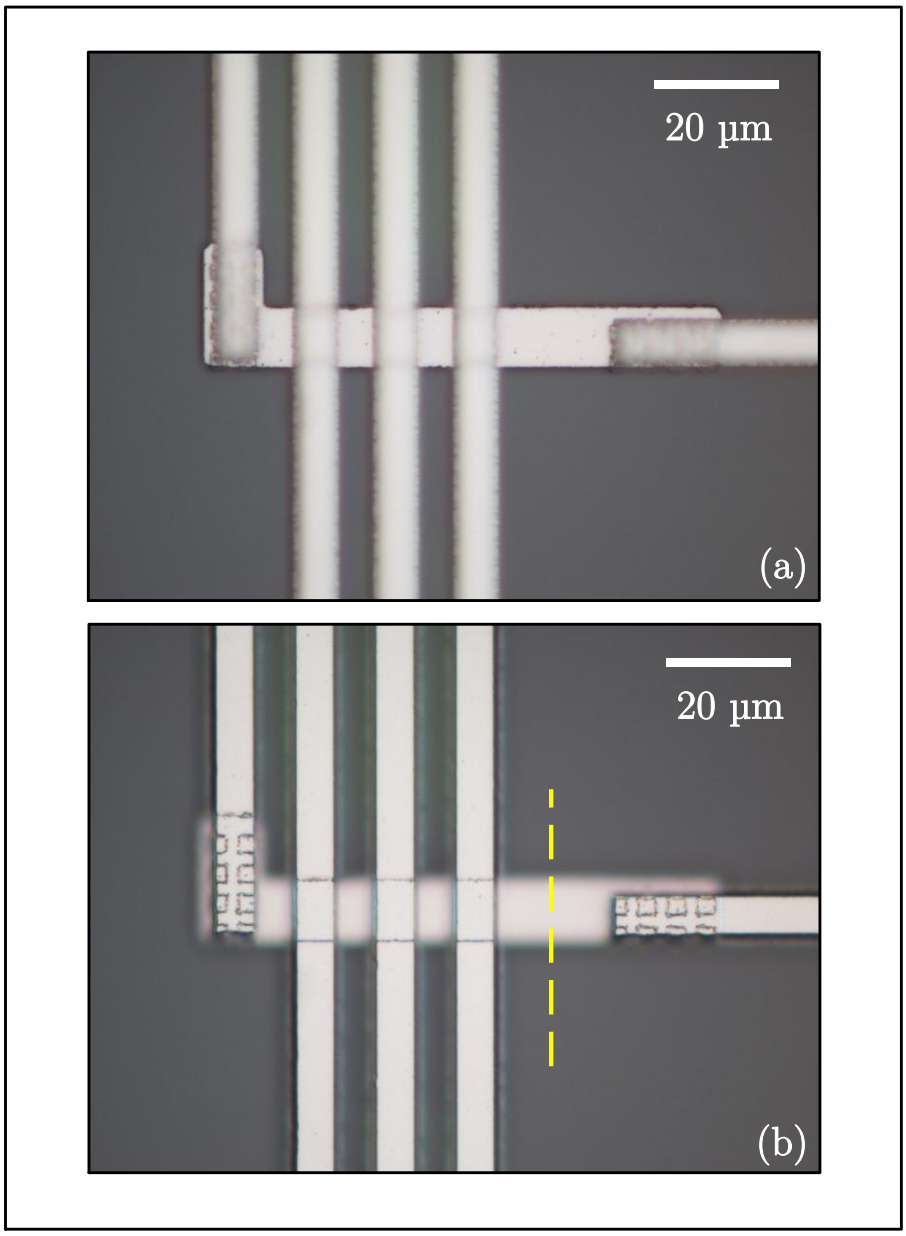

Figure 4.22 – Images of the underpass of the 5 nH inductor with focus on (a) the underpass and (b) the spiral track as observed using an optical microscope. The dashed yellow line represents the path of the profilometer needle that gave the results in Figure 4.23.

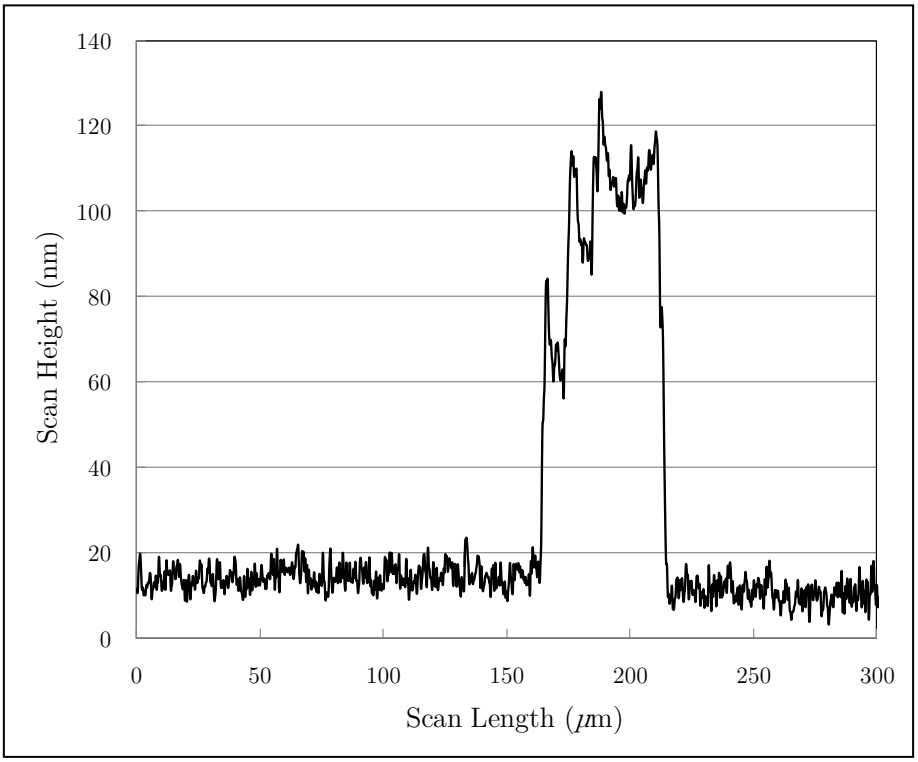

Figure 4.23 – Results from a profilometer showing a final step size over the underpass of approximately 110 nm, highlighting the effects of the planarization process.

4.8 Spiral Inductor Quality Factor Measurements

The resistivity of the compensated wafer that the inductors were fabricated on was measured as 40 kΩcm using the four-point prober. This value is lower than that of the wafer with the same implantation dose used for CPW fabrication, which was measured as 70 kΩcm. This is not fully consistent with the resistivities of many other wafers created using the same process and the reason behind this lower than expected resistivity is an area that requires further research. Nevertheless the wafer could still be used to investigate the effects of increased resistivity on Q-factor of spiral inductors, and hence the inductors were fabricated on it.

After fabrication S-parameters of the inductors were measured using the same method and equipment as those used for the CPWs in section 3.6. The obtained S_{11} and S_{21} values are included in Appendix D, from which graphs of reflection, transmission and absorption were

produced and are included in Appendix E. The measured S-parameters were then used to calculate the Q-factor of the inductors using equations (4.7) and (4.8). The resulting Q-factor frequency sweeps of the overpass inductors on the uncompensated, compensated and FZ-Si wafers are shown in Figure 4.24. These results clearly show a grand increase in Q-factor values with increasing resistivity as predicted by the simulations in section 4.6. The results also show an increase in the self-resonance frequency of the 50 nH inductor on the FZ-Si and Au-doped wafers from approximately 1 GHz to 1.5 GHz, which translates to an increased operating frequency range for the inductor. The Q_{max} values were extracted from these results and are shown in Table 4.6. The largest increase in Q_{max} of over a factor of 10 is experienced by the 50 nH inductor, from 0.3 for uncompensated wafers to 3.1 for the compensated wafer.

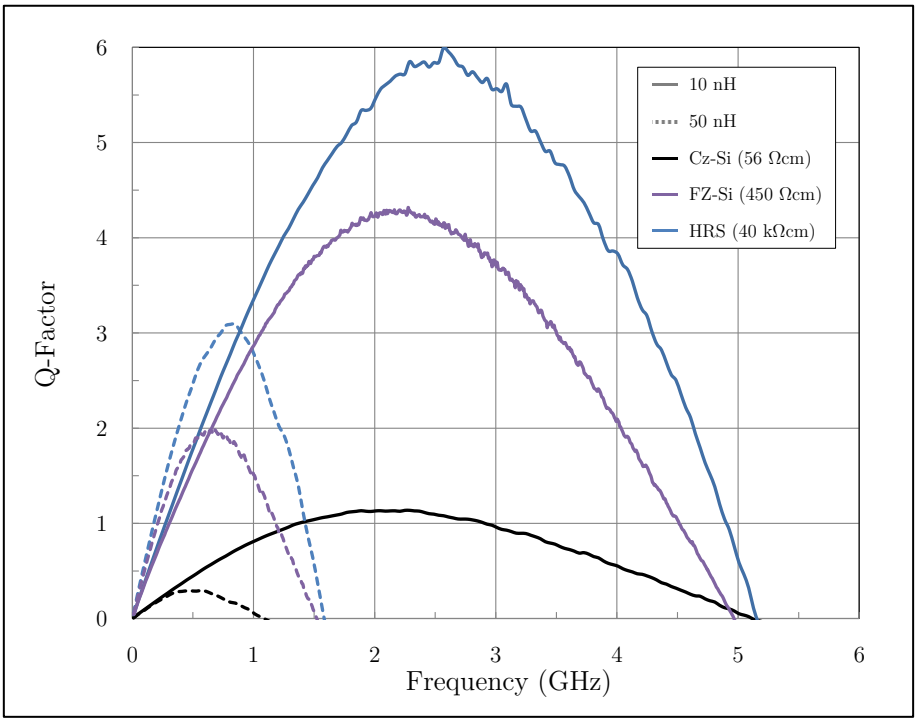

Figure 4.24 – Q-factor as a function of frequency for the wire-bonded overpass inductors, on float-zone, uncompensated and compensated Si.

TABLE 4.6
Maximum Q-factor values for overpass inductors fabricated on uncompensated, float-zone and compensated Si wafers.

L (nH)	Q_{max}		
	Uncompensated Si (56 Ωcm)	FZ-Si (450 Ωcm)	HRS (40 kΩcm)
10	1.1	4.3	6.0
50	0.3	2.0	3.1

Comparing the ASITIC simulated Q-factor frequency sweeps of the 10 nH inductor, in Figure 4.17, with the measured equivalent it is clear that there is a good agreement between the two as can be seen in Figure 4.25. From these results values of Q_{max}, $f(Q_{max})$ and f_{SR} were extracted as given in Table 4.7 from which a difference of approximately only a factor of two is evident. These differences are not of major concern and can be due to many factors of which the most likely is the overpass which was not included in the ASITIC simulation. There is likely to be signal reflection losses at the junction between the wire-bond pads and the overpass wedge and ball bonds the effects of which were not taken into account. The effects of the GSG contact pads and tapered signal tracks were also not simulated and therefore reflection losses that occur at the probes to GSG pad junctions and those due to the tapered signal line were also not taken into account. Other factors such as the junction between the PECVD deposited and sputtered oxides, the quality of the oxides and of the Al track, and the fabrication process itself could also contribute to these differences. Improvements in fabrication were therefore expected to increase the performance of the spiral inductors on uncompensated Si and would be reflected in those on compensated Si.

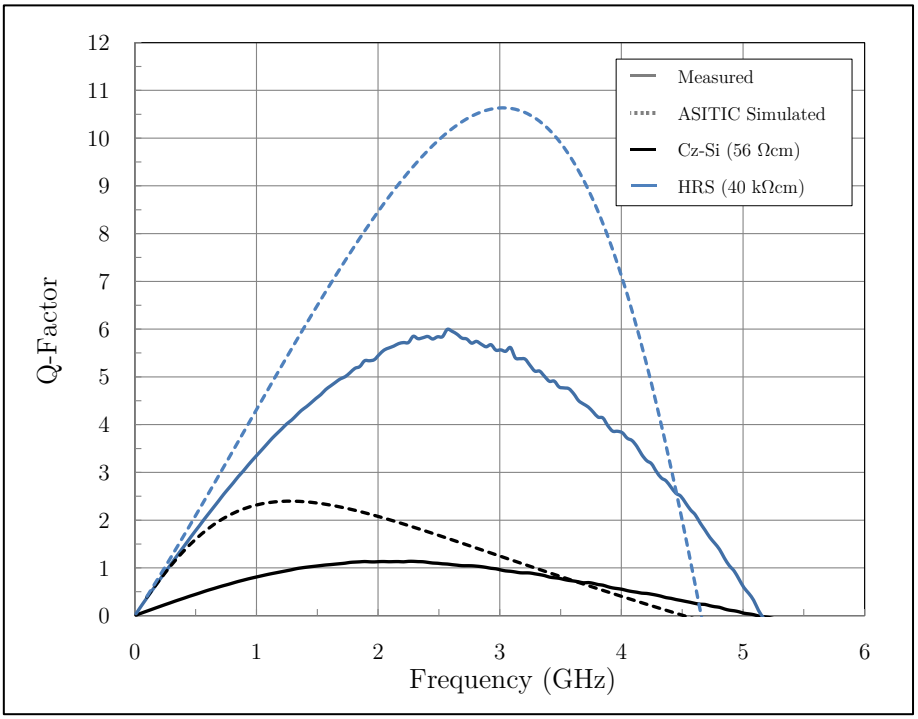

Figure 4.25 – Measured and ASITIC simulated Q-factor as a function of frequency for a 10 nH inductor on low and high resistivity substrates.

TABLE 4.7
Comparison between measured and ASITIC Q-factor parameters for a 10 nH inductor on low and high resistivity substrates.

	Uncompensated		Compensated	
	Measured (56 Ωcm)	Simulated (50 Ωcm)	Measured (40 kΩcm)	Simulated (50 kΩcm)
Q_{max}	1.1	2.4	6.0	10.6
$f(Q_{max})$ (GHz)	2.3	1.3	2.6	3.0
f_{SR} (GHz)	5.1	4.6	5.2	4.7

The underpass inductors were also measured using the same equipment and the Q-factor frequency sweeps are included in Figure 4.26. Unfortunately these results show that the underpass inductors on the compensated wafer did not behave as expected. Their negative low-frequency Q-factor values indicate a capacitive behaviour. The cause of the problem may be attributed to the underpass since all the overpass inductors exhibit inductive behaviour. Devices fabricated on the uncompensated wafer also did not show this capacitive behaviour therefore the problem most likely lies in the fabrication not the design of the underpass.

Initially the problem was believed to be caused by the via holes etching process that did not penetrate deep enough to reach the underpass leaving a thin oxide between the underpass and the vias in the case of the compensated wafer. The uncompensated and compensated wafers were processed at different times and variations in gas pressure or flow rates, humidity levels, cleanliness of the chamber and many other factors could lead to a different etch rate.

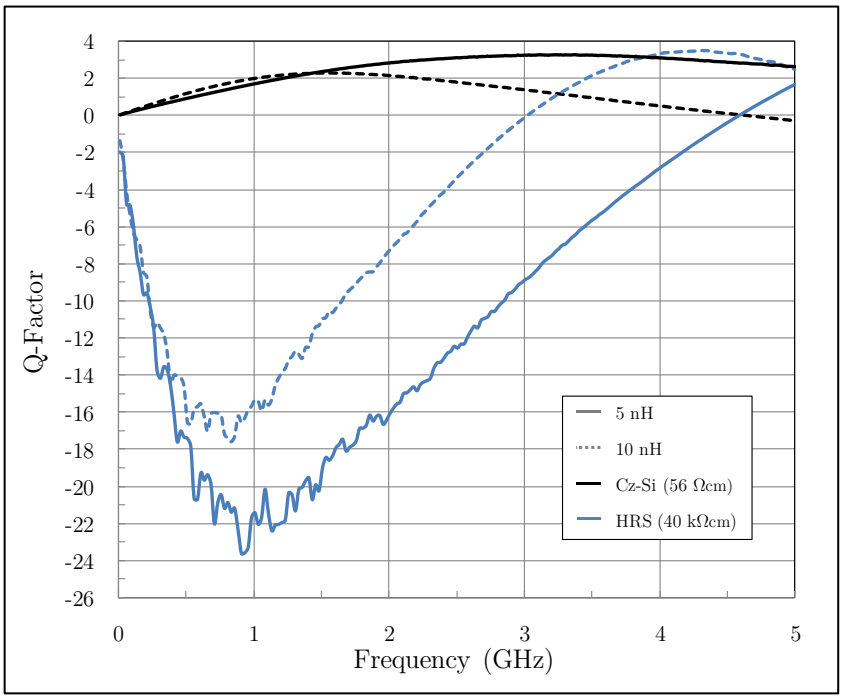

Figure 4.26 – Q-factor as a function of frequency for the underpass inductors, on uncompensated and compensated wafers.

A digital multimeter was used to measure the DC series resistance R_S between the two ports of the inductors the results of which are shown in Table 4.8 along with ASITIC simulated and theoretical values calculated using equation (2.1). From these values it is clear that there is contact between the two ports and that the inductors on both the compensated and uncompensated wafers have near identical values suggesting the problem lies not with the underpasses but elsewhere. It is however interesting to note that the measured R_S values are a factor of 3 higher for both inductors when compared to the theoretically calculated and simulated values, which could be attributed to the use of smaller RF vias.

To investigate this issue further the measured S-parameters were used to calculate the ratio of the power reflected back to the source at the input, represented by $|S_{11}|^2$, which was found to be large for the failed devices as can be seen in Figure 4.27. It can also be seen that all other inductors experience lower reflection meaning more of the signal was launched into these devices than was the case for the underpass inductor on HRS. The percentages of the power reflected for the 10 nH overpass and underpass inductors are shown in Table 4.9. From these results it is evident that almost all of the power supplied to the underpass inductor on the compensated wafer is reflected at the probes and not launched into the device which is not the case for all other inductors which show relatively low levels of reflection that are very similar in value suggesting the problem lies with that particular HRS wafer.

TABLE 4.8
Calculated, simulated and measured resistances of inductors with underpasses on compensated and uncompensated wafers.

	R_S (Ω)			
	Calculated	ASITIC Simulated	Measured	
			Uncompensated	Compensated
5 nH	5.5	6.2	20	20
10 nH	9.2	10.25	32	34

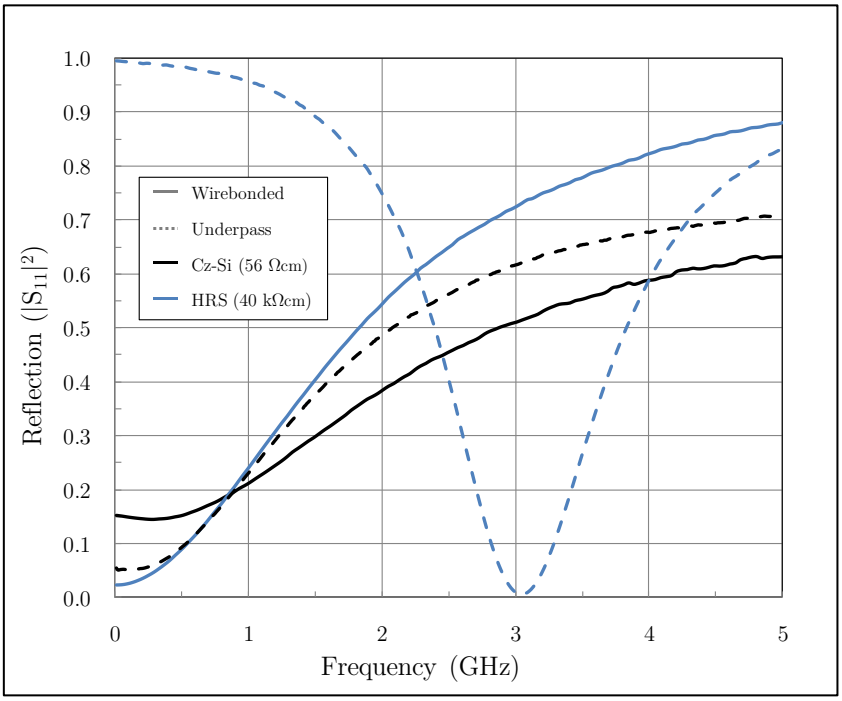

Figure 4.27 – Comparison between 10 nH wirebonded and underpass inductors on uncompensated and compensated Si.

TABLE 4.9

Reflection power percentages for 10 nH overpass and underpass inductors on float-zone, compensated and uncompensated wafers.

	Percentage of Power Reflected				
	Overpass			Underpass	
Frequency (GHz)	Cz-Si	FZ-Si	HRS	Cz-Si	HRS
0.5	15	9	9	9	98
1	21	23	24	23	96
1.5	30	39	40	37	89
2	39	52	55	48	75

Although it is not completely understood what the exact cause of the high reflection in the underpass inductors on the compensated wafer is, it is believed to be due to the fabrication process. Improvements in this process were therefore expected to increase the performance of the underpass spiral inductors on HRS. For this reason spiral inductors with underpasses were fabricated with a commercial process by Plessey Semiconductor Ltd. An in-house design was used to fabricate a 5 nH inductor with 4.5 turns and a 4 nH inductor with 3.5 turns of which details and images cannot be disclosed for confidentiality reasons. The inductors were fabricated on FZ-Si with a resistivity of 450 Ωcm, and on a Cz-Si wafer implanted with a Au dose of $4x10^{13}$ cm^{-2} and annealed at 950°C before an oxide strip and Au etch.

These Plessey fabricated inductors were also measured using the same equipment and methods used for the overpass inductors and the calculated Q-factor frequency sweeps are shown in Figure 4.28. From this it is clear that the inductors fabricated on compensated Si exhibit much higher Q-factor values at higher frequency than those on FZ-Si. The Q_{max} values were extracted from these results and are shown in Table 4.10, from which it is clear that the inductors fabricated on HRS show an increase in Q_{max} of up to 70% when compared to FZ-Si. The results in this section clearly show that the increased resistivity caused by deep level dopant compensation does increase the Q-factor of spiral inductors as predicted by simulations, thereby improving their RF performance.

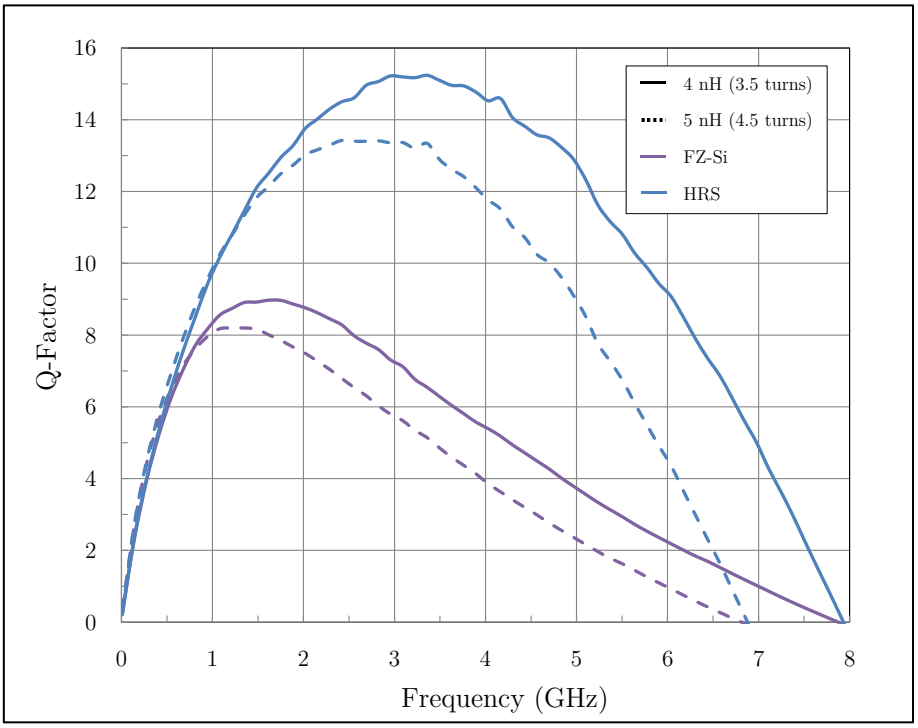

Figure 4.28 – Q-factor as a function of frequency for inductors fabricated on FZ-Si and compensated Cz-Si. These inductors were designed and fabricated by Plessey Semiconductors Ltd.

TABLE 4.10

Maximum Q-factor values for inductors fabricated on FZ-Si and compensated Cz-Si, by Plessey Semiconductor Ltd.

L (nH)	n	Q_{max}	
		FZ-Si	HRS
4	3.5	8.2	13.4
5	4.5	9.0	15.2

Chapter 5

Summary

Cz-Si is an excellent material for the fabrication of ICs that can operate at frequencies approaching those of many III-V devices. However, passive devices fabricated on Cz-Si and operated at RF suffer from substrate related losses that reduce their performances. These losses are due to absorption of microwave power by background free carriers in the Si, and are hence related to the conductivity or resistivity of the Si substrate. The main aim of this work was therefore the creation of high resistivity Si through deep level dopant compensation.

Deep level dopant compensation was successfully used to enhance the resistivity of Cz-Si wafers by up to 3 orders of magnitude from 56 Ωcm to values as high as 93 kΩcm. The wafers were implanted with different Au doses and annealed before the surface Au layer was etched. Four-point probe measurements show that anneals at 950°C produced the highest resistivities with the exception of the highest dose. The resistivities were measured as 8.6 kΩcm, 35.5 kΩcm and 70 kΩcm for doses of $1x10^{13}$ cm^{-2}, $2x10^{13}$ cm^{-2} and $4x10^{13}$ cm^{-2} respectively.

SIMS and SRP measurements confirmed that once annealed the implanted Au forms a U-shaped concentration depth profile which translates to a U-shaped resistivity depth profile with the highest values at the edges of the wafers. This property of Au in silicon makes deep level dopant compensation theoretically compatible with integrated passive devices and 3D

integration configurations. Implantation through the backside of the wafer was also found to create a U-shaped resistivity profile therefore the technique can also be used with SOI wafers, provided the buried oxide acts as a diffusion barrier preventing Au atoms from diffusing from the handle to the active wafer.

Hall measurements over a large temperature range were performed which prove that the increase in resistivity is due to a decrease in carrier concentration and not a decrease in mobility. The measured carrier concentration values were found to be only one order of magnitude larger than those of intrinsic Si over a temperature range of 200K-360K, indicating that the Fermi level is very near the intrinsic mid-bandgap level and that deep level doping greatly reduces free carrier concentration. Hall results also show that the resistivity of the compensated material remains up to two orders of magnitude larger than that of the uncompensated material at approximate operating temperature of 80°C.

To investigate the effects of deep level doped Si on passive devices Al CPWs and spiral inductors were fabricated on standard Cz-Si and compensated wafers. High frequency attenuation measurements in the 1-67 GHz range of CPWs show reductions of up to 76% at 10 GHz from 0.76 dB/mm to 0.18 dB/mm. Q-factor measurements of spiral inductors show increases in the maximum Q-factor of up to a factor of 10, from 0.3 for uncompensated wafers to 3.1 for the compensated wafer, for overpass inductors. For commercially designed and fabricated underpass inductors the maximum Q-factor was increased by up to 70%, from 9.0 to 15.2 on FZ-Si and compensated Cz-Si respectively. The CPW and spiral inductor results provide clear evidence that deep level dopant compensation is effective in improving the performance of passive devices in the GHz frequency range.

Despite the positive results summarised above, there are a few issues which should be investigated further. Firstly, the difference between the measured resistivities and the theoretical values of just under one order of magnitude. Au agglomeration is a possible reason for this difference and it is suspected that oxygen precipitates or clusters within the wafers

prevent Au atoms from taking up substitutional lattice sites leading to the agglomeration [42] and should be investigated.

With regards to the use of deep level dopant compensation with SOI wafers the effectiveness of the buried oxide in preventing Au atoms from diffusing into the active wafers should also be investigated. The compatibility of deep level dopant compensation with modern RFIC fabrication techniques should also be tested by annealing the compensated wafers at the different temperatures it would experience during a typical process run. This is particularly interesting for n-type wafers as it would determine whether the wafers can compensate for the effects of thermal donors that reduce resistivity at temperatures around 450°C, which is close to the temperature at which alloy anneals are normally performed.

Additional related work may include the investigation of deep level dopant compensation of germanium wafers. Although germanium is intrinsic at room temperature its resistivity decreases greatly with decreasing temperature. The demand for high resistivity germanium for low temperature application such as satellite equipment should be researched further. Given a significant demand germanium could be implanted with nickel or iron which introduce deep level donor and acceptor levels [88], and the properties of this material could be studied.

In conclusion deep level dopant compensation through Au implantation has proven an effective technique for increasing the resistivity of Si wafers to values much higher than the minimum required for RF performance indistinguishable from devices on GaAs. Deep level doped Si has also been shown, for the first time, to greatly improve the efficiency of passive devices when operated at RF.

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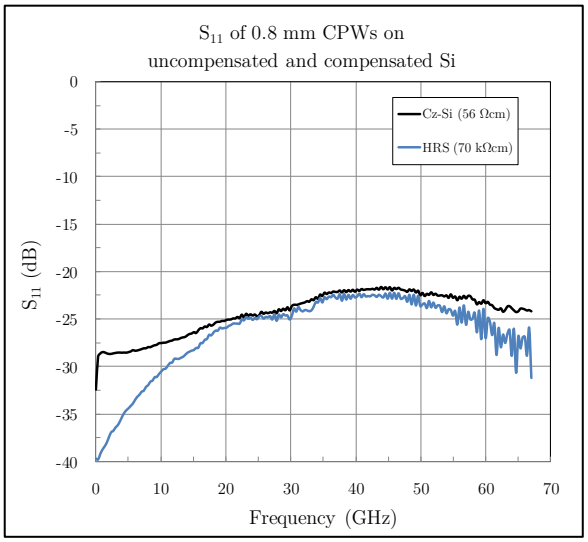
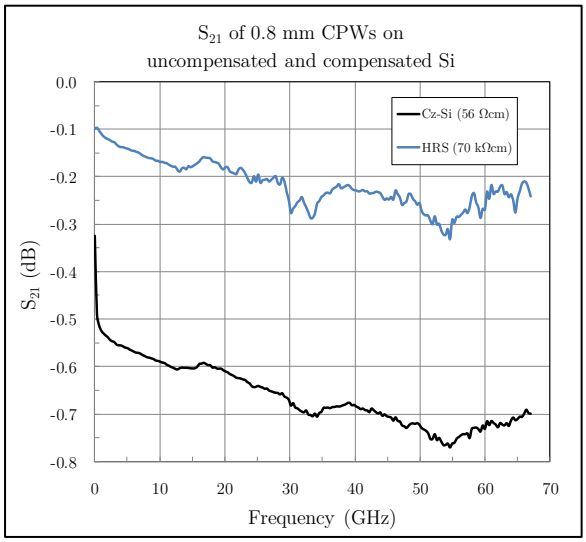
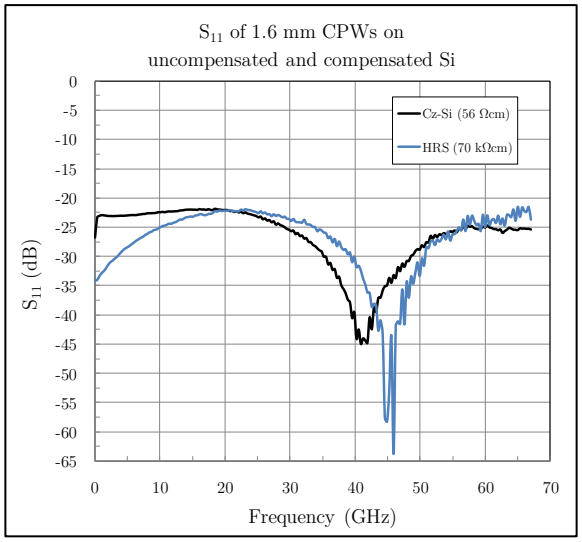
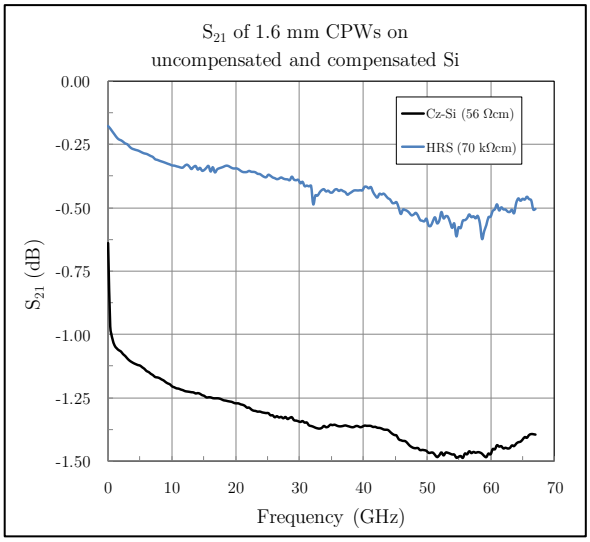
Appendix A

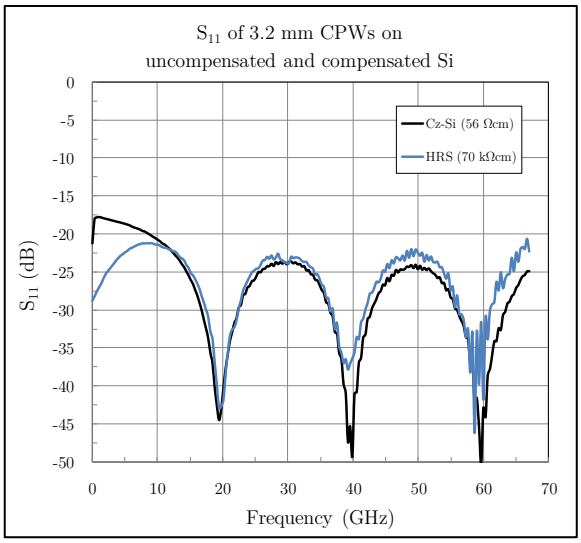
S-Parameter Graphs of Measured CPWs

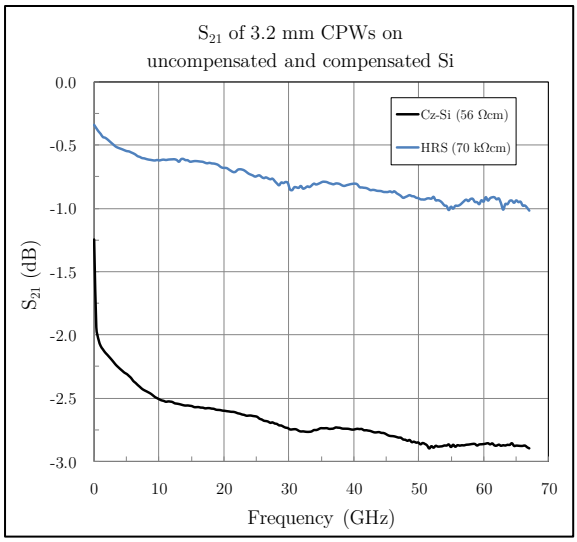


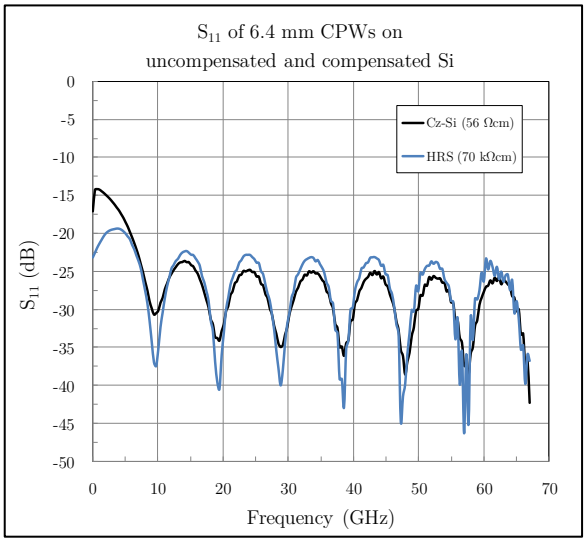


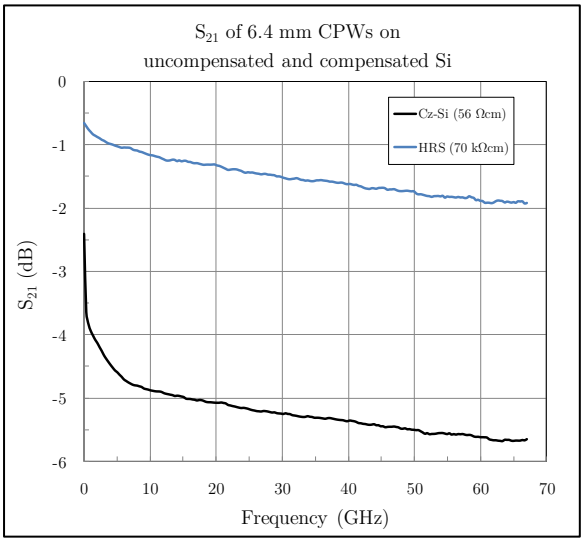





S11 of 3.2 mm CPWs on
uncompensated and compensated Si
Cz-Si (56 Ωcm)
HRS (70 kΩcm)
S11 (dB)
Frequency (GHz)
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
0
10
20
30
40
50
60
70

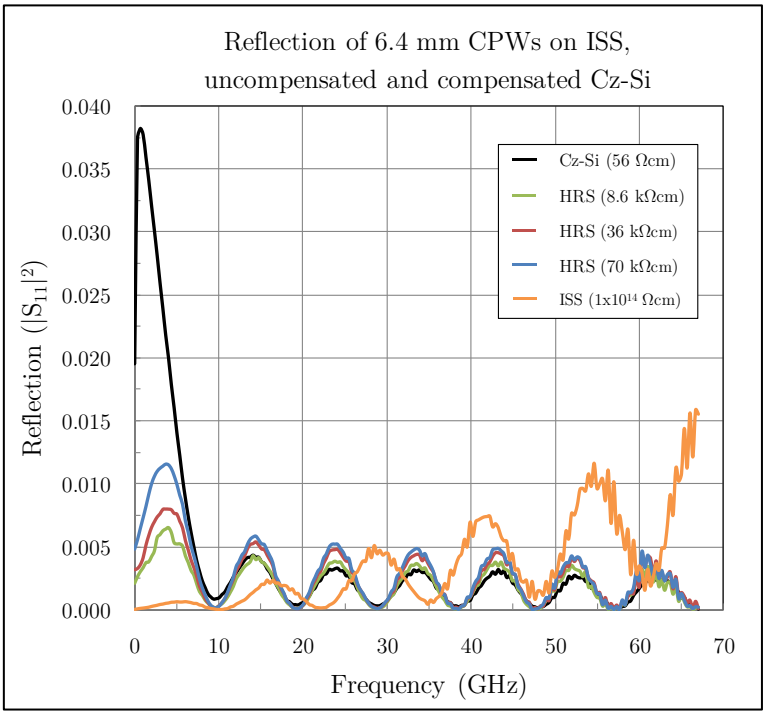

S21 of 3.2 mm CPWs on
uncompensated and compensated Si
Cz-Si (56 Ωcm)
HRS (70 kΩcm)
S21 (dB)
Frequency (GHz)
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
0
10
20
30
40
50
60
70

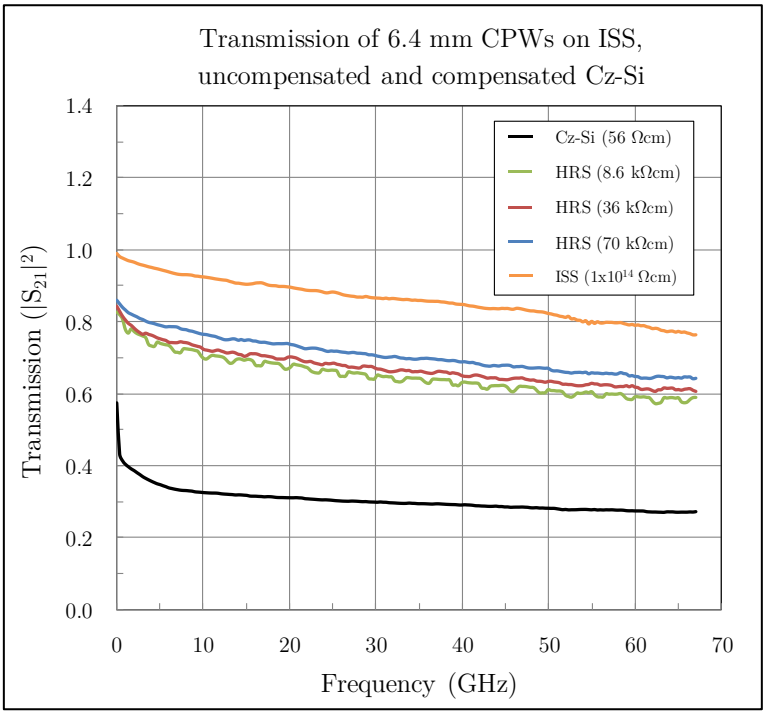

S11 of 6.4 mm CPWs on
uncompensated and compensated Si
Cz-Si (56 Ωcm)
HRS (70 kΩcm)
S11 (dB)
Frequency (GHz)
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
0
10
20
30
40
50
60
70

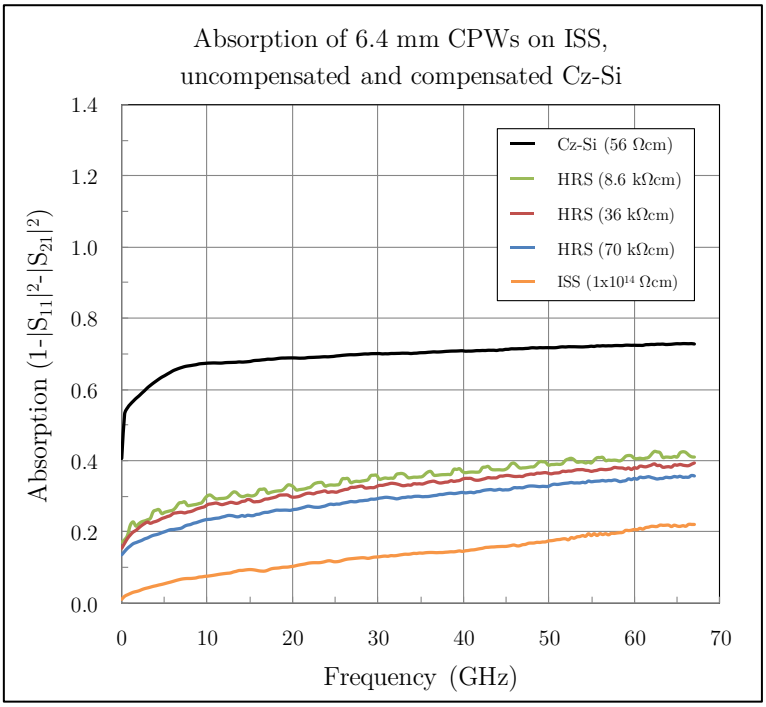

S21 of 6.4 mm CPWs on
uncompensated and compensated Si
Cz-Si (56 Ωcm)
HRS (70 kΩcm)
S21 (dB)
Frequency (GHz)
0
-1
-2
-3
-4
-5
-6
0
10
20
30
40
50
60
70

Appendix B

Reflection, Transmission and Absorption Graphs of Measured CPWs






Absorption of 6.4 mm CPWs on ISS,
uncompensated and compensated Cz-Si
Absorption (1-|S11|2-|S21|2)
Frequency (GHz)
Cz-Si (56 Ωcm)
HRS (8.6 kΩcm)
HRS (36 kΩcm)
HRS (70 kΩcm)
ISS (1x10¹⁴ Ωcm)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
0
10
20
30
40
50
60
70

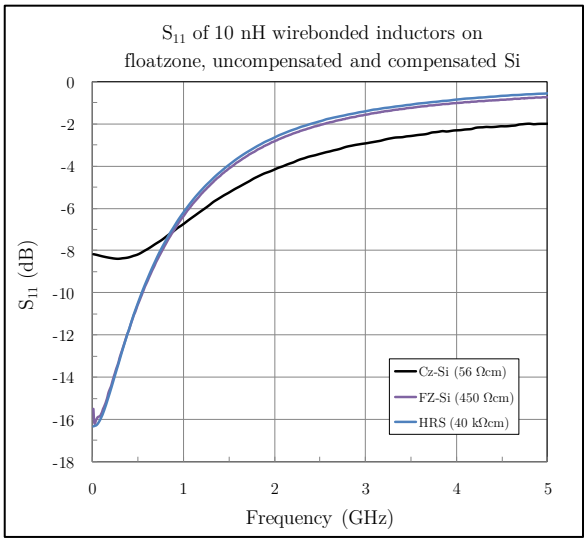
Appendix C

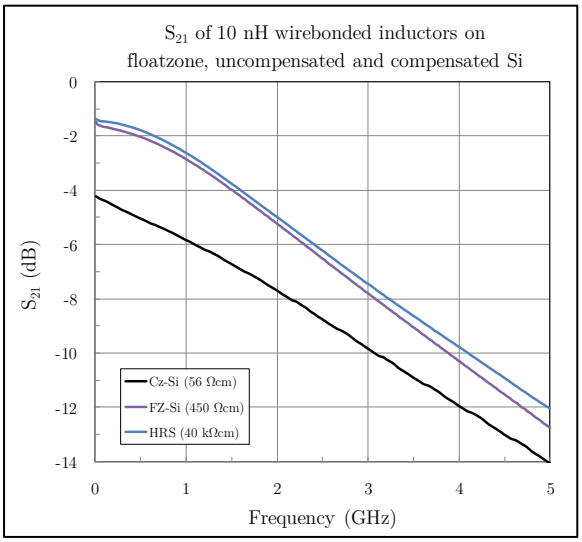
ASITIC technology file

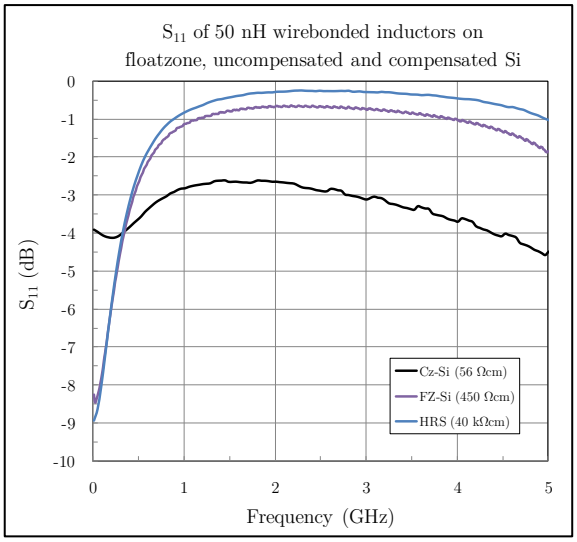
```
<chip>
        chipx = 830                 ; Chip x dimensions (microns)
        chipy = 830                 ; Chip y dimensions (microns)
        fftx = 240                  ; Resolution x-fft size
        ffty = 240                  ; Resolution y-fft size
        TechFile = ahmed.tek        ; File name
        TechPath = .
        freq = .1
        eddy = 0                    ; Layer 0 defined below is conductive

<layer> 0                           ; Bulk Substrate
        rho = 56                    ; Resistivity (Ωcm)
        t   = 675                   ; Thickness (microns)
        eps = 11.9                  ; Permitivity (relative)

<layer> 1                           ; Oxide Layer
        rho = 1e12                  ; Resistivity (Ωcm)
        t = 3.5                     ; Thickness (microns)
        eps = 3.9                   ; Permitivity (relative)

<metal> 1                           ; Metal 1
        layer = 1                   ; Layer in which the metal is present
        rsh = 56                    ; Sheet resistance (mΩ/sq typically 1-100)
        t = 0.5                     ; Thickness (microns)
        d =  1                      ; Distance from bottom of layer (microns)
        name = m1
        color = red

<via> 1                             ; Metal 1 to Metal 2 via
        top = 2
        bottom = 1
        r = 4
        width = 0.5
        space = 1.5
        overplot1 = .4
        overplot2 = .4
        name = via1
        color = white

<metal> 2                           ; Metal 2
        layer = 1
        rsh = 19
        t = 1.5
        d = 2
        name = m2
        color = blue
```

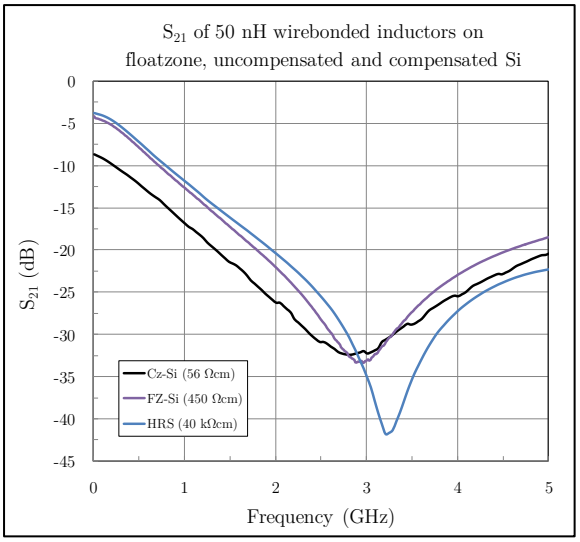
Appendix D

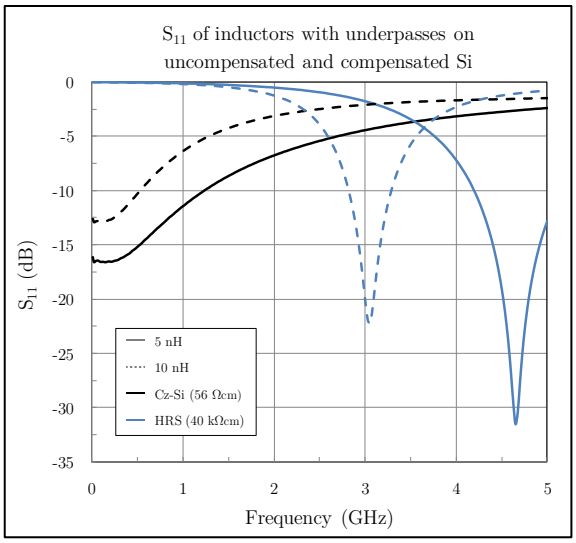
S-Parameter Graphs of Measured Spiral Inductors

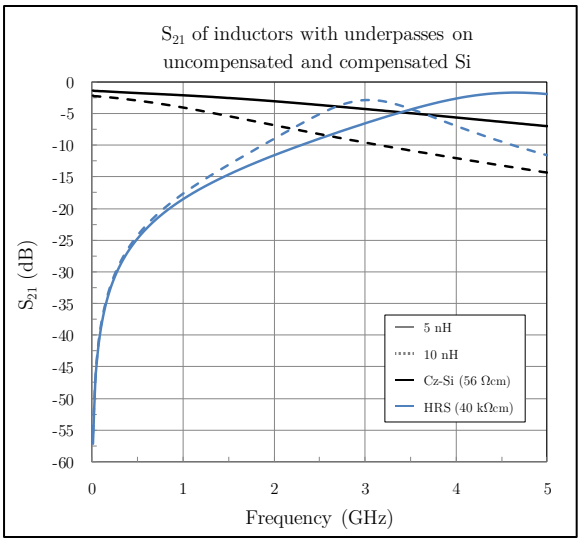


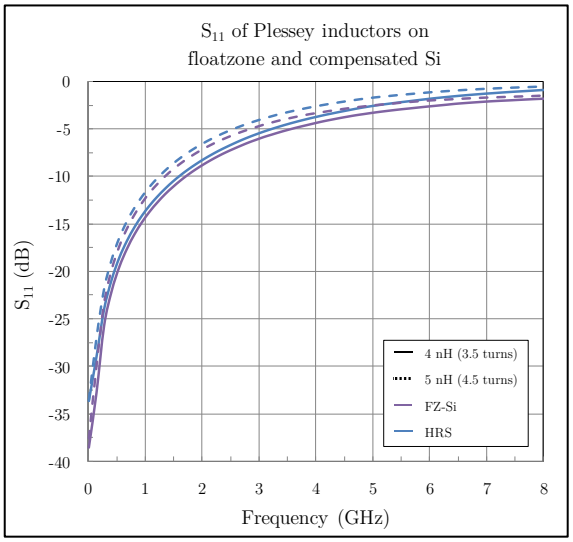


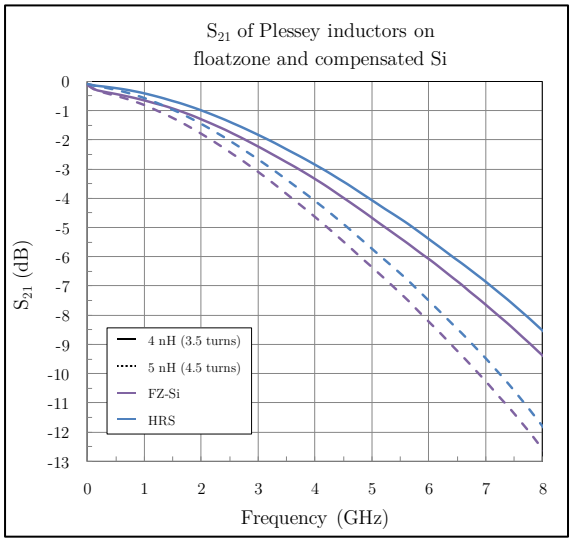





S11 of inductors with underpasses on
uncompensated and compensated Si
S11 (dB)
Frequency (GHz)
5 nH
10 nH
Cz-Si (56 Ωcm)
HRS (40 kΩcm)

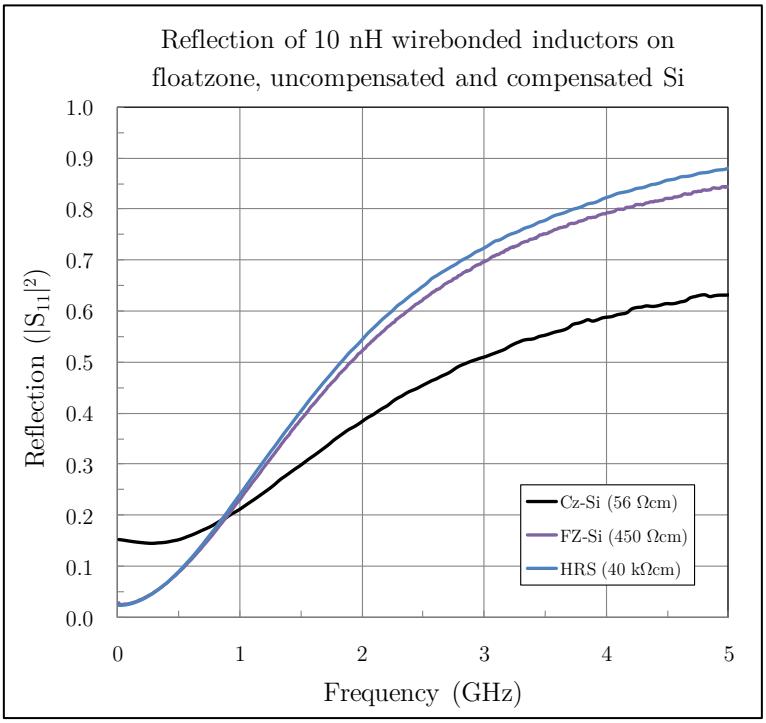

S21 of inductors with underpasses on
uncompensated and compensated Si
S21 (dB)
Frequency (GHz)
5 nH
10 nH
Cz-Si (56 Ωcm)
HRS (40 kΩcm)

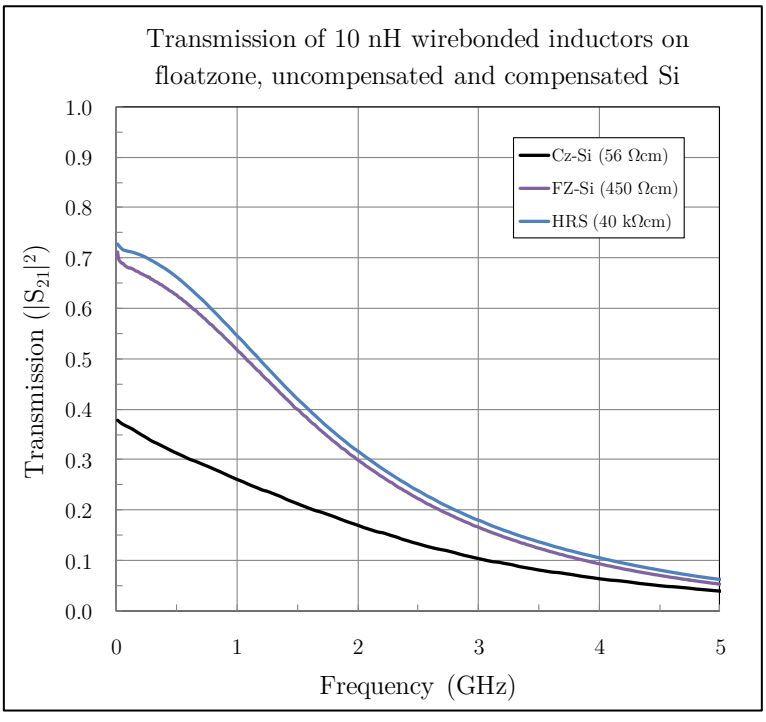

S11 of Plessey inductors on
floatzone and compensated Si
S11 (dB)
Frequency (GHz)
4 nH (3.5 turns)
5 nH (4.5 turns)
FZ-Si
HRS

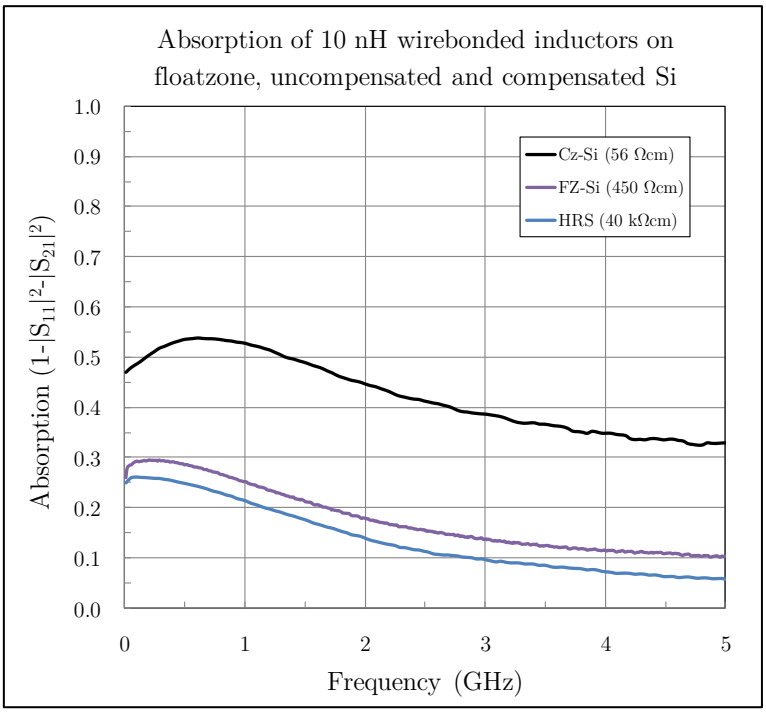

S21 of Plessey inductors on
floatzone and compensated Si
S21 (dB)
Frequency (GHz)
4 nH (3.5 turns)
5 nH (4.5 turns)
FZ-Si
HRS

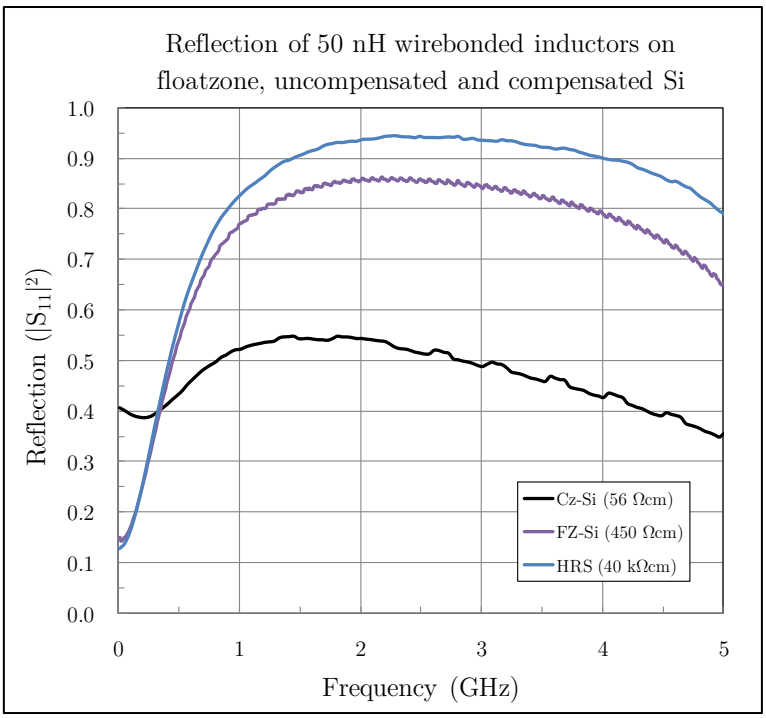
Appendix E

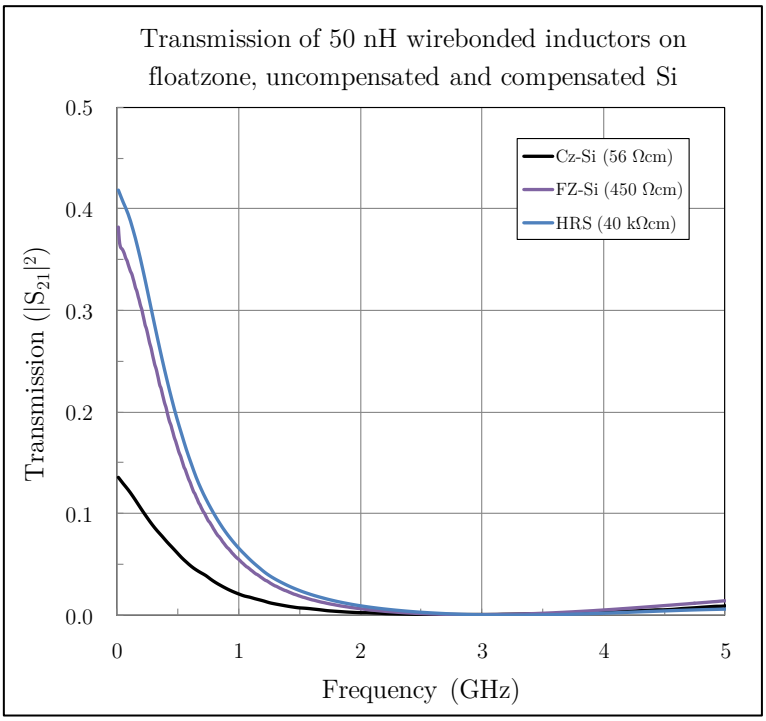
Reflection, Transmission and Absorption Graphs of Measured Spiral Inductors

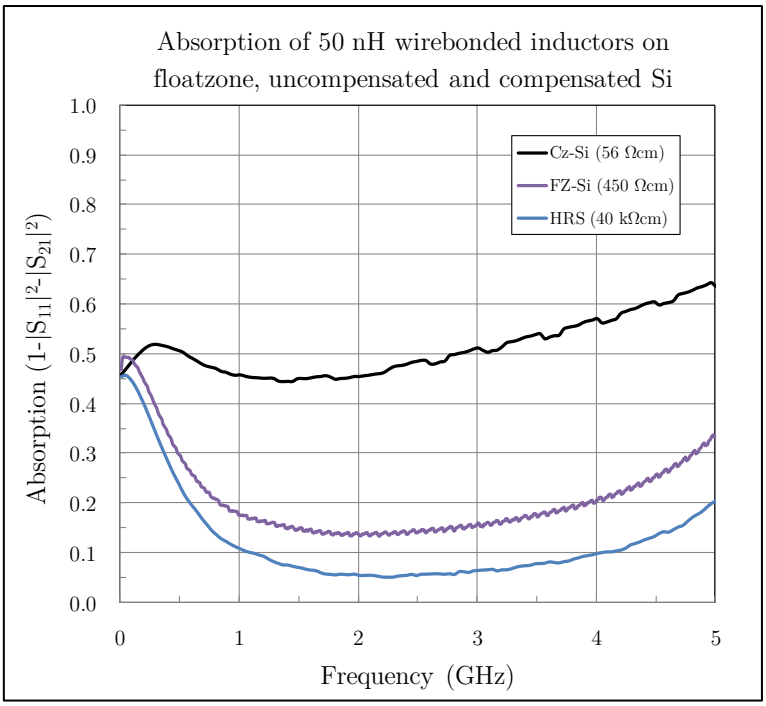


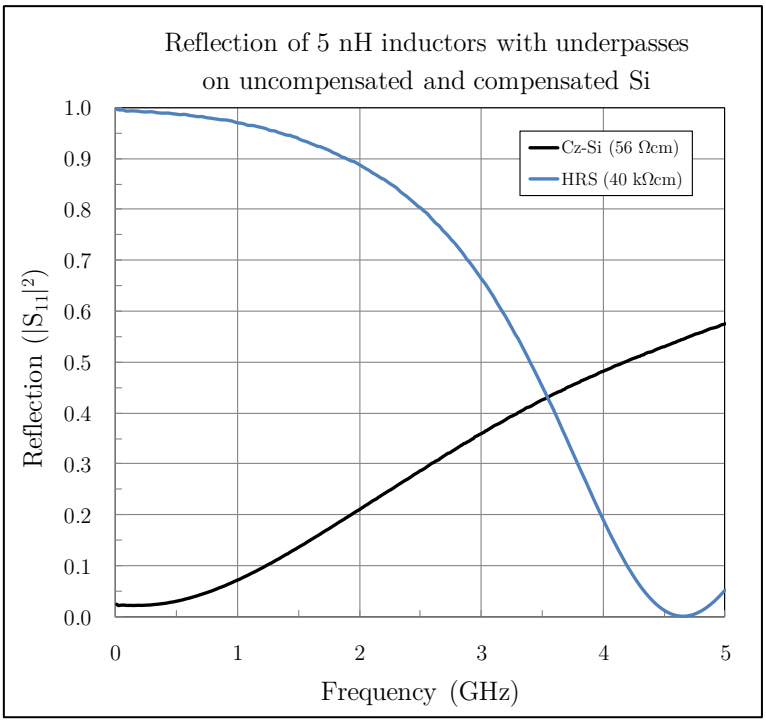


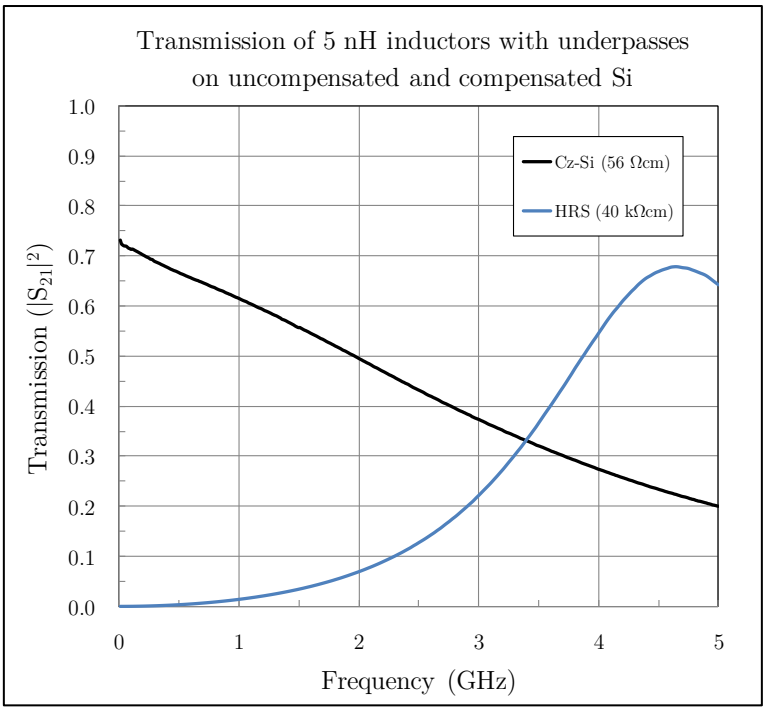

Absorption of 10 nH wirebonded inductors on floatzone, uncompensated and compensated Si
Absorption (1-|S11|2-|S21|2)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5
Frequency (GHz)
Cz-Si (56 Ωcm)
FZ-Si (450 Ωcm)
HRS (40 kΩcm)

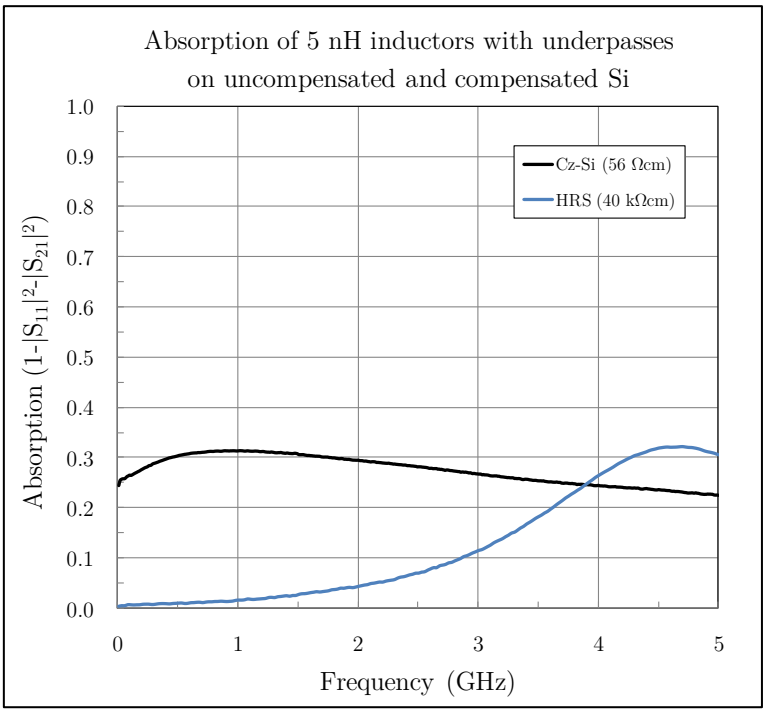

Reflection of 50 nH wirebonded inductors on floatzone, uncompensated and compensated Si
Reflection (|S11|2)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5
Frequency (GHz)
Cz-Si (56 Ωcm)
FZ-Si (450 Ωcm)
HRS (40 kΩcm)

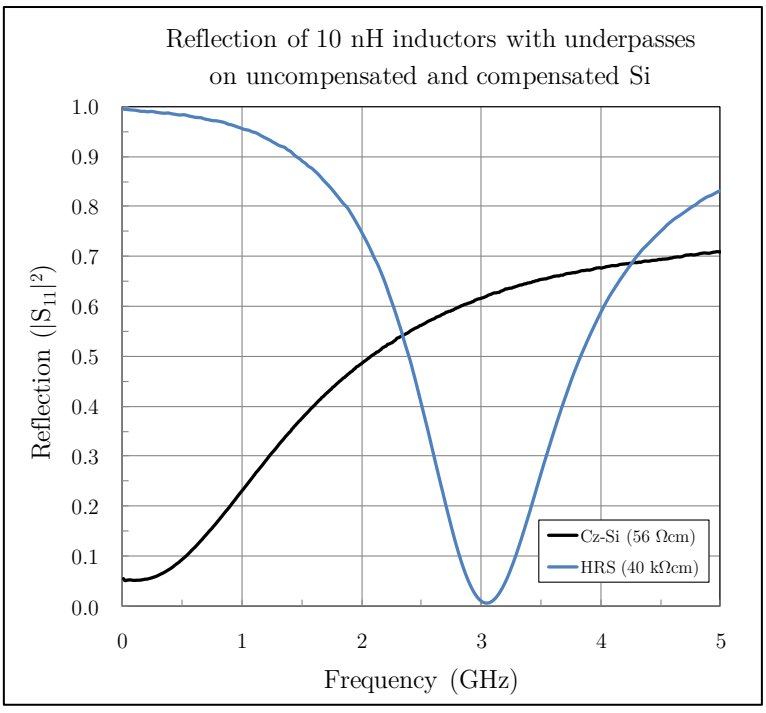

Transmission of 50 nH wirebonded inductors on floatzone, uncompensated and compensated Si
Transmission ($|S_{21}|^2$)
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5
Frequency (GHz)
Cz-Si (56 Ωcm)
FZ-Si (450 Ωcm)
HRS (40 kΩcm)

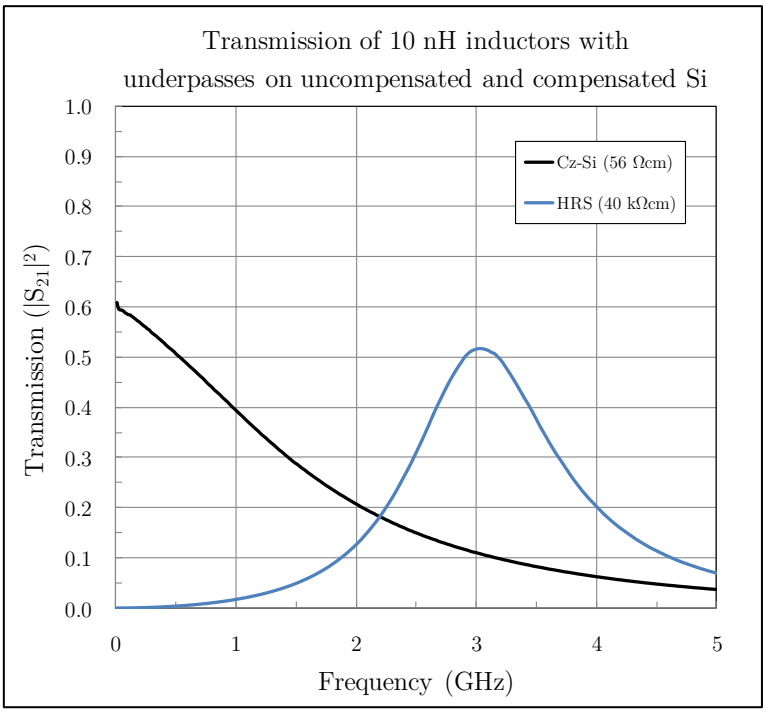

Absorption of 50 nH wirebonded inductors on floatzone, uncompensated and compensated Si
Absorption ($1-|S_{11}|^2-|S_{21}|^2$)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5
Frequency (GHz)
Cz-Si (56 Ωcm)
FZ-Si (450 Ωcm)
HRS (40 kΩcm)

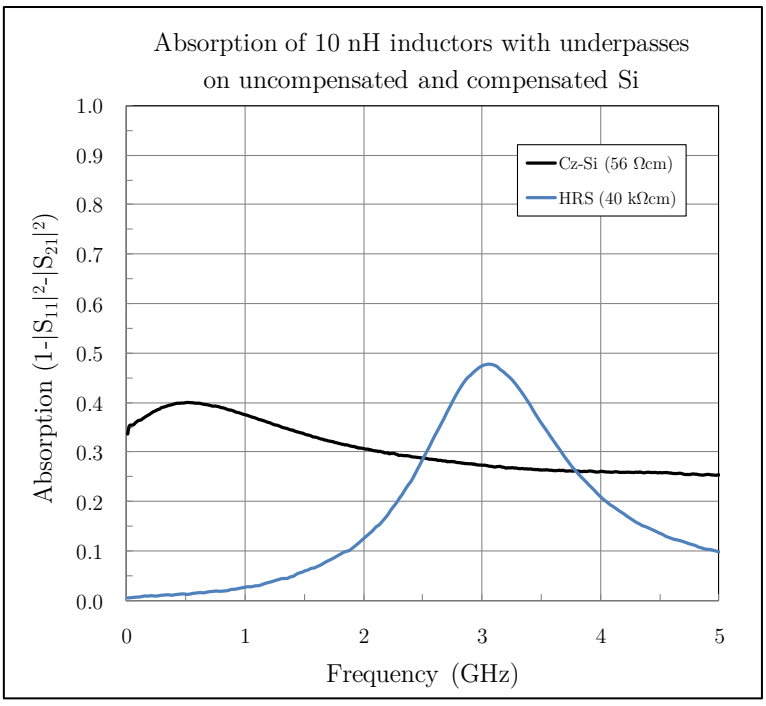

Reflection of 5 nH inductors with underpasses
on uncompensated and compensated Si
Cz-Si (56 Ωcm)
HRS (40 kΩcm)
Reflection (|S11|2)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5
Frequency (GHz)

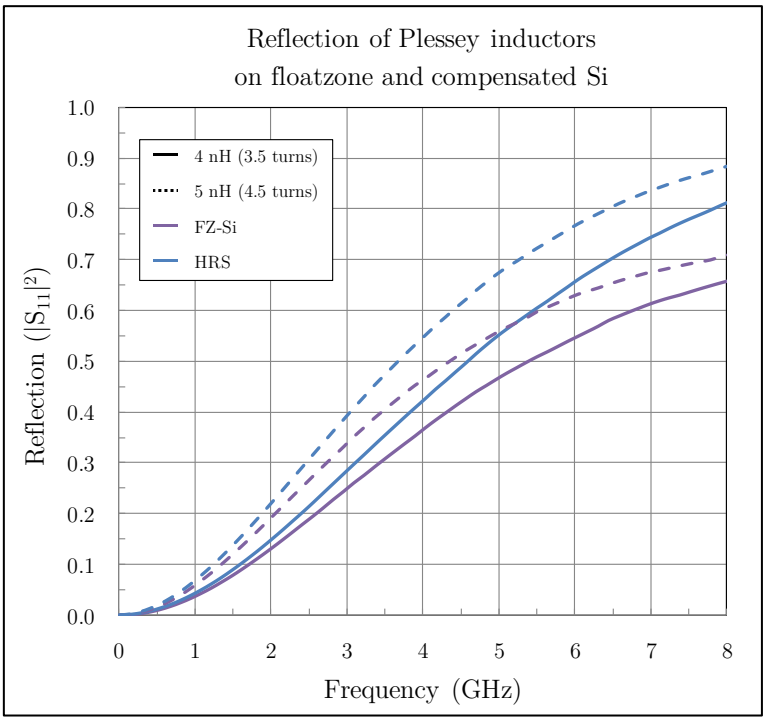

Transmission of 5 nH inductors with underpasses
on uncompensated and compensated Si
Cz-Si (56 Ωcm)
HRS (40 kΩcm)
Transmission (|S21|2)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5
Frequency (GHz)

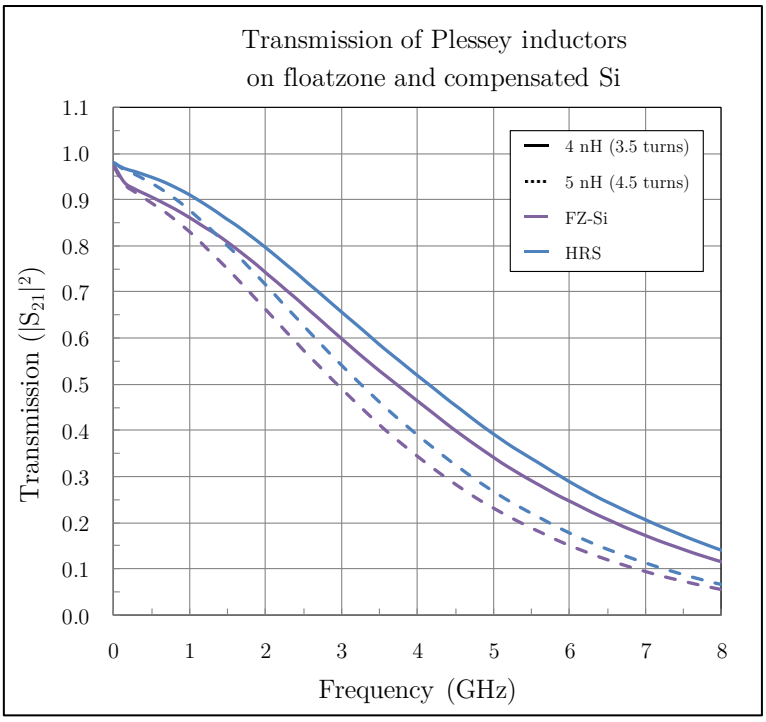

Absorption of 5 nH inductors with underpasses
on uncompensated and compensated Si
Absorption (1-|S11|2-|S21|2)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5
Frequency (GHz)
Cz-Si (56 Ωcm)
HRS (40 kΩcm)

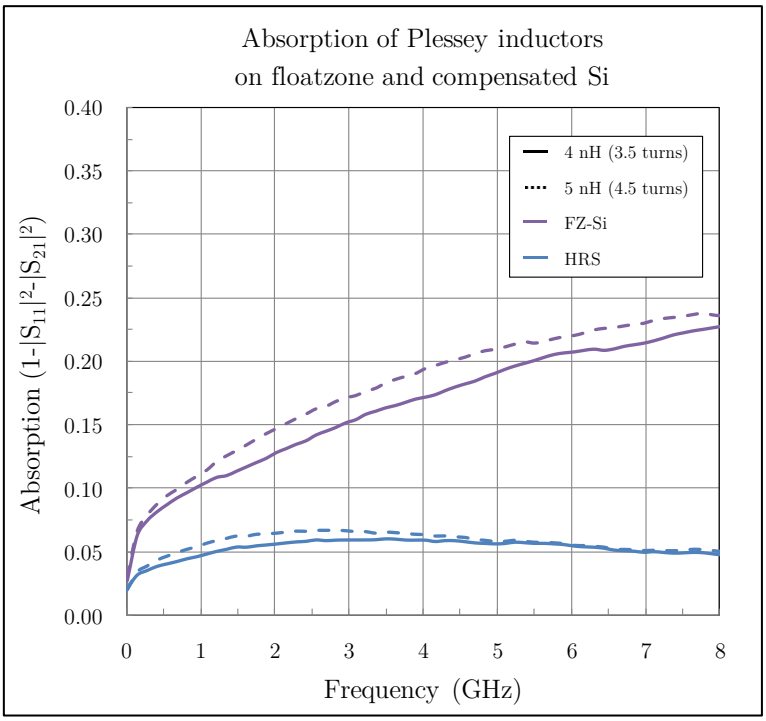

Reflection of 10 nH inductors with underpasses
on uncompensated and compensated Si
Reflection (|S11|2)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5
Frequency (GHz)
Cz-Si (56 Ωcm)
HRS (40 kΩcm)


Transmission of 10 nH inductors with underpasses on uncompensated and compensated Si
Cz-Si (56 Ωcm)
HRS (40 kΩcm)
Transmission (|S21|2)
Frequency (GHz)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5


Absorption of 10 nH inductors with underpasses on uncompensated and compensated Si
Cz-Si (56 Ωcm)
HRS (40 kΩcm)
Absorption (1-|S11|2-|S21|2)
Frequency (GHz)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
1
2
3
4
5


Reflection of Plessey inductors
on floatzone and compensated Si
Reflection ($|S_{11}|^2$)
Frequency (GHz)
4 nH (3.5 turns)
5 nH (4.5 turns)
FZ-Si
HRS
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
0
1
2
3
4
5
6
7
8


Transmission of Plessey inductors
on floatzone and compensated Si
Transmission ($|S_{21}|^2$)
Frequency (GHz)
4 nH (3.5 turns)
5 nH (4.5 turns)
FZ-Si
HRS
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
0
1
2
3
4
5
6
7
8


Absorption of Plessey inductors
on floatzone and compensated Si
Absorption (1-|S11|2-|S21|2)
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
0
1
2
3
4
5
6
7
8
Frequency (GHz)
4 nH (3.5 turns)
5 nH (4.5 turns)
FZ-Si
HRS