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A Novel Time Domain Noise Model for Voltage Controlled Oscillators

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Abstract

This paper describes a novel time domain noise model for voltage controlled oscillators that accurately and efficiently predicts both tuning behavior and phase noise performance. The proposed method is based on device level flicker and thermal noise models that have been developed in Simulink and although the case study is a multiple feedback four delay cell architecture it could easily be extended to any similar topology. The strength of the approach is verified through comparison with post layout simulation results from a commercial simulator and measured results from a 120nm fabricated prototype chip. Furthermore, the effect of control voltage flicker noise on oscillator output phase noise is also investigated as an example application of the model. Transient simulation based noise analysis has the strong advantage that noise performance of higher level systems such as phase locked loops can be easily determined over a realistic acquisition and locking process yielding more accurate and reliable results.

1. Introduction

Low jitter reference frequency generation is a key requirement for high performance analogue and mixed-signal integrated circuits and is usually achieved using a stable reference crystal and phase locked loop (PLL). An important trade-off exists between PLL phase noise and loop bandwidth and it is vital to explore this balance, particularly when targeting low output jitter [1]. At the heart of every PLL is a voltage controlled oscillator (VCO) which greatly influences the performance of the PLL itself and is typically the biggest noise contributor in the system [2]. In order facilitate PLL noise analysis, therefore, a VCO noise model is required which will accurately predict noise performance under realistic closed loop conditions whilst maintaining simulation efficiency.

It is widely agreed that time domain transistor level simulations provide the most reliable and accurate means to examine the performance of closed loop PLLs [3]. One approach for noise analysis is to include noise behavior for each transistor within the transient simulation, in a technique known as transient noise analysis. Unfortunately, however, few commercial simulators include support for noise as part of a transient simulation, focusing on less accurate linearized approaches instead. Indeed, transient noise analysis tends to be impractical for realistic circuit designs due to the huge simulation re-

sources required [3]. To address this problem, a number of alternative approaches have been proposed in the literature based on a variety of design platforms including Matlab-Simulink [3-4], C [5], and VHDL [6]. All these methods extract behavioral model parameters from transistor level simulations first, which can lead to inaccuracy since the parameters are only valid for limited operating conditions. With the decrease in technology node size this problem is exacerbated as devices are becoming increasingly difficult to characterize.

In this paper, a novel time domain VCO noise model is proposed, which incorporates transistor level noise behavior whilst maintaining simulation efficiency. In order to accurately define true dynamic behavior the VCO model accepts an instantaneous control voltage input and dynamically generates the correct output waveform, whilst incorporating the relevant noise sources to ensure an accurate representation of the phase noise performance. Further post processing of the VCO output waveform then provides both the oscillation frequency and signal purity. A careful balance is struck between accuracy and complexity to ensure meaningful results yet manageable simulation times. Section 2 introduces the VCO structure used in this work and derives the combined VCO tuning behavior and noise performance model. Section 3 presents a case study complete with transistor level simulations and measurements from a prototype chip to demonstrate the work on a realistic example. Fi-

nally, Section 4 discusses the significance of the work, with some concluding remarks.

2. VCO architecture and tuning model

A high performance VCO architecture is at the core of this approach and is detailed in this section. Both the frequency tuning behavior and noise performance characteristics are considered and combined into a complete time domain model that facilitates accurate and efficient system simulation.

2.1. VCO tuning model

Passive inductor and capacitor (LC) based VCO structures offer excellent phase noise performance yet can be difficult and expensive to integrate on deep sub-micron CMOS processes due to their large physical size and additional processing requirements. Conversely, inverter based oscillators (also referred to as RC or ring oscillators) are easily integrated onto standard CMOS processes but generally suffer from inferior phase noise perfor-

mance [7]. Despite this, their compact size and additional advantages of wider tuning range and direct quadrature output has led to great interest in RC oscillators. Recent research has focused on achieving phase noise performance in RC oscillators that is close to equivalent LC based designs [1]. Given the importance of modeling the phase noise of RC oscillator accurately, they are a suitable candidate for the development of an improved model, as described in this paper.

The oscillator architecture employed in this work is shown in Figure 1 and is based on a multiple feedback four delay cell topology in order to achieve a wide tuning range [8]. Within each delay cell, the two internal transistors, Mp1 and Mn1, operate as an inverter and the two current control transistors, Mp2 and Mn2, in each stage are responsible for frequency control. Transistors Mp3 and Mp4 form a secondary feedback loop to increase the oscillator frequency. Since the on-resistance (*Ronn* and *Ronp*) and lumped gate capacitance *C* of the two inverting transistors (Mp1 and Mn1) are independent of the frequency of oscillation, they can be modeled as fixed values defined by equations (1) to (3) [9].
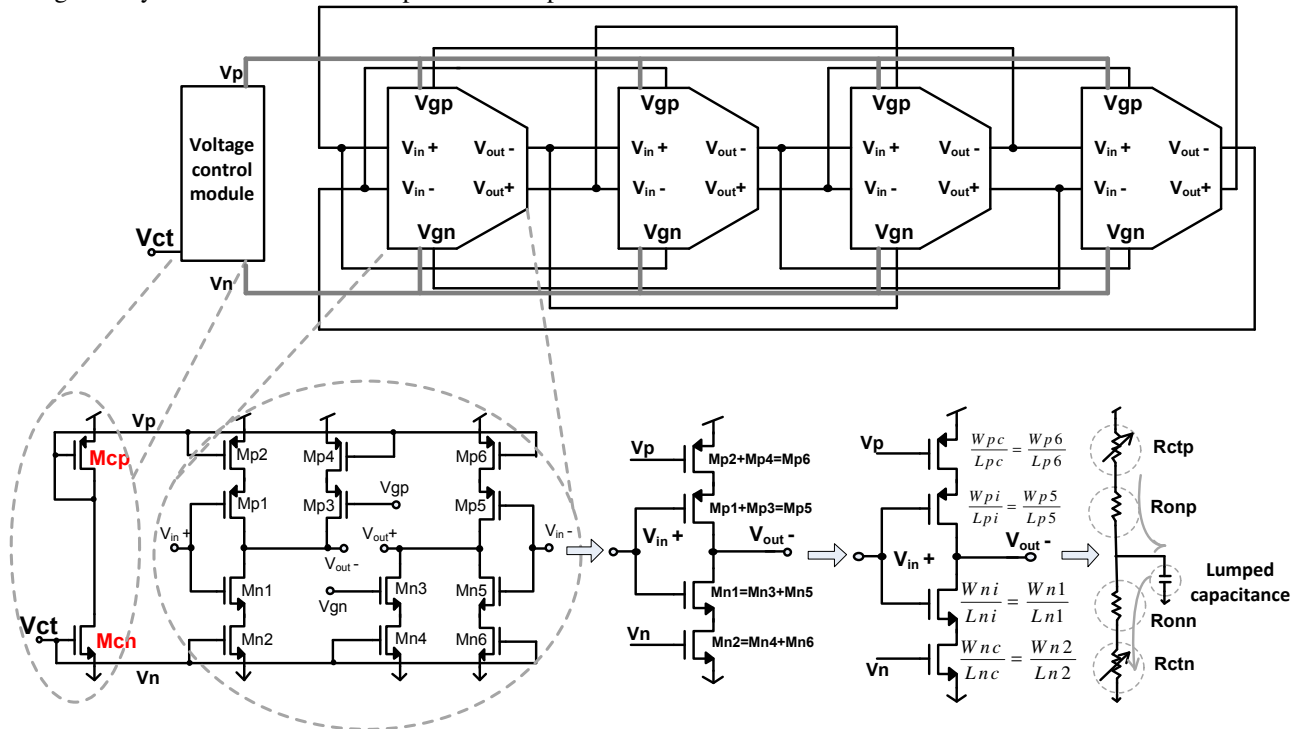

Figure 1 Modeling of effective RC delay for a VCO delay cell

$$C = \overbrace{2(C_{gdo} \cdot Wni + C_{gdo} \cdot Wpi)}^{C_{out}} + \overbrace{\frac{3}{2}(Wni \cdot Lni \cdot C_{ox} + Wpi \cdot Lpi \cdot C_{ox}) + 2(C_{gdo} \cdot Wni + C_{gdo} \cdot Wpi)}^{C_{in}} \quad (1)$$

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$$Ronn = \frac{V_{DS}}{I_{DS}} = V_{DS} / (\frac{1}{2} \mu_n C_{ox}(Wni / Lni)(V_{GS} - V_{th})^2) \quad (2)$$

$$Ronp = \frac{V_{DS}}{I_{DS}} = V_{DS} / (\frac{1}{2} \mu_n C_{ox}(Wpi / Lpi)(V_{GS} - V_{th})^2) \quad (3)$$

Where C_{ox} is the unit-area gate oxide capacitance, C_{gdo} is the gate-drain overlap capacitance per unit-length, μ_n is the mobility parameter and V_{th} is the transistor threshold voltage, *Wni/Lni* and *Wpi/Lpi* are the transistor dimensions for NMOS and PMOS inverter transistors respectively. V_{DS} and V_{GS} are the effective drain-source and gate-source voltage difference for each transistor. Defining V_{DS} and V_{GS} within equations (2) and (3) is difficult since the voltages at the gate and drain nodes of the device dynamically change within each oscillation cycle. The gate and drain voltages of Mni increase from $V_{DD}/2$ to V_{DD} and decrease from V_{DD} to $V_{DD}/2$ respectively within each propagation delay. For simplicity, therefore, it is assumed that both drain and gate nodes are fixed at $3V_{DD}/4$ within the propagation delay, ensuring that Mni stays in saturation. The two control transistors, Mpc and Mnc, are modeled as variable resistors R_{ctp} and R_{ctn} with values defined by the external control voltage, and the linearity of this relationship governs the linearity of the VCO's tuning function. The resistance relationship depends on the operating region of the transistor and for Mnc is given by equations (4) and (5) for the saturation and deep triode regions respectively. Equations (6) and (7) give the corresponding equations for Mpc.

$$Rctn\_sat = \frac{Vct}{\frac{1}{2} \mu_n C_{ox} \frac{Wnc}{Lnc}(Vct - V_{th})^2} \quad (4)$$

$$Rctn\_tri = \frac{Vct}{I_D} = \frac{1}{\mu_n C_{ox} \frac{Wnc}{Lnc}(Vct - V_{th})} \quad (5)$$

$$Rctp\_sat = \frac{Vct}{\frac{1}{2} \mu_n C_{ox} \frac{Wpc}{Lpc}(Vct - V_{th})^2} \quad (6)$$

$$Rctp\_tri = \frac{Vct}{I_D} = \frac{1}{\mu_n C_{ox} \frac{Wpc}{Lpc}(Vct - V_{th})} \quad (7)$$

As illustrated in Figure1, Wnc/Lnc and Wpc/Lpc are the dimensions of the current controlling transistors. During each period of oscillation the drain source voltage of the

control transistors Mpc and Mnc can vary by several hundred mV and so the region of operation is difficult to define. A good compromise is to assume that the effective ON resistance of the control transistor Mnc is a combination of equations (4) and (5) (or (6) and (7) for transistor Mpc). The combination is determined linearly by the instantaneous control voltage, *Vct*, and is given by equation (8) for *Rctn* and equation (9) for *Rctp*.

$$Rctn = Rctn\_sat \left(\frac{V_{DD} - Vct}{V_{DD}}\right) + Rctn\_tri \left(\frac{Vct}{V_{DD}}\right) \quad (8)$$

$$Rctp = Rctp\_sat \left(\frac{V_{DD} - Vct}{V_{DD}}\right) + Rctp\_tri \left(\frac{Vct}{V_{DD}}\right) \quad (9)$$

Now that the effective capacitive and resistive components have been modelled, the corresponding propagation delays, t_{d_push} and t_{d_pull}, can be obtained directly from equations (10) and (11). The time constant is obtained from the product of the effective resistance (R_{eff}) and capacitance (C_{eff}) in each case.

$$t_{d\_push} = R_{eff} C_{eff} = \frac{V_{DD}}{2I} C = \frac{V_{DD}/2}{I/C}$$
$$= \frac{(V_{DD}/2)}{\left(\frac{V_{DD}}{Rctn + Ronn}\right)/C} \quad (10)$$

$$t_{d\_pull} = R_{eff} C_{eff} = \frac{V_{DD}}{2I} C = \frac{V_{DD}/2}{I/C}$$
$$= \frac{(V_{DD}/2)}{\left(\frac{V_{DD}}{Rctp + Ronp}\right)/C} \quad (11)$$

As the pull-up path uses the same principle and structure as the push-down path for the dual inverter based ring oscillator, it is straightforward to combine 2N stages (as it is a dual feedback loop structure) of push delay (t_{d_push}) and 2N stages of pull delay (t_{d_pull}) to obtain the nominal oscillation cycle, T_o which is given in equation (12). Figure 2 illustrates the complete tuning model, which has been implemented in Simulink.

$$T_0 = 2N\left(t_{d\_pull} + t_{d\_push}\right) \quad (12)$$
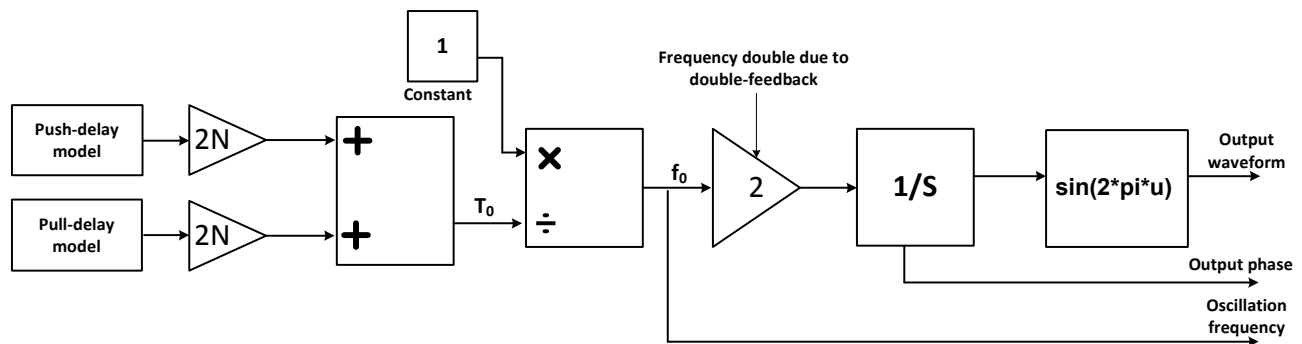
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Figure 2 Complete VCO tuning model

To verify the accuracy of the tuning model, its behaviour has been compared with schematic level transistor simulations using standard foundry models. This comparison is shown in Figure 3, where the correlation across the range of *Vct* of the oscillation frequency is good between the proposed model and the more detailed transistor level circuit.
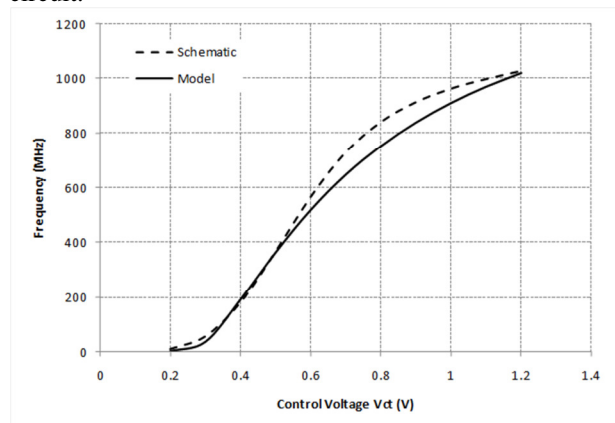

Figure 3 Comparison of transistor level schematic and model simulation results

In practice, the circuit will also suffer from layout parasitics, which will typically result in a reduced oscillation frequency. Realistic estimation of the performance with parasitic components taken into account can be achieved through post layout extraction simulations. A simple extension to the model can be included to correctly predict the performance reduction, in the form of a parasitic delay factor that can be added to the overall oscillation period as shown in equation (13). The value of parasitic delay can be quickly obtained from simple dc analyses, and the more accurate model used for later noise analysis, increasing confidence in the noise results. The effect of the parasitic delay can be seen in Figure 4, where the extracted simulation results are compared with the revised model and a clear reduction in the maximum oscil-

lation frequency from over 1GHz to 840Mhz was observed.

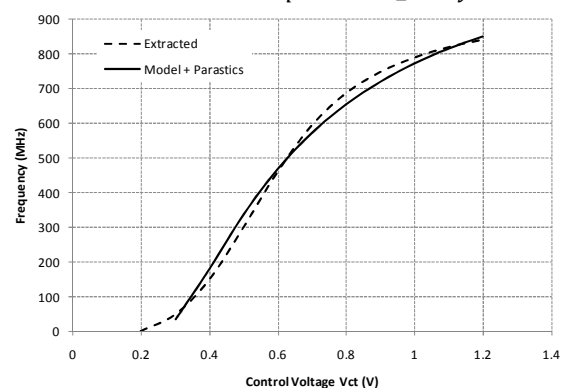$$T_0 = 2N(t_{d\_pull} + t_{d\_push}) \\ + parasitic\_delay \qquad (13)$$

Figure 4 Comparison of extracted parasitic delay simulation and model including *parasitic_delay*

2.2. Transistor level noise model

Thermal noise and flicker noise dominate a transistor's noise spectrum and can be summarised by equation (14) where $S_{in\_thermal}$ and $S_{in\_flicker}$ are the drain current noise power spectral density (PSD) for thermal and flicker noise, k is the Boltzmann constant, T is the absolute temperature in Kelvin and g_m is the device transconductance. The flicker noise coefficient K_f is a process independent parameter of the order of 10^{-24} and γ is a bias-dependent factor which may be set at 2/3 for long channel transistors and must be replaced by a larger value for submicron MOSEFTs. The point of intersection between the flicker noise and thermal noise contributions is referred to as the device's corner frequency, f_c, and is given in equation (15). Above the corner frequency, the noise level is dominated by thermal noise, whereas be-

low the corner frequency flicker noise dominates with an increasing factor of 20dB/decade [10] [9].

$$\overline{V_{n,out}^2} = (S_{i_n-thermal} + S_{i_n-flicker})R^2 = \left(4kT\gamma g_m + \frac{K_f}{C_{OX}W_{eff}L_{eff}f}g_m^2\right)R^2 \quad (14)$$

$$4kT\gamma g_m = \frac{K_f}{C_{ox}W_{eff}L_{eff}f}g_m^2 \Rightarrow$$

$$f_{corner} = f_c = \frac{K_f g_m}{C_{ox}W_{eff}L_{eff}} \cdot \frac{1}{4kT\gamma} \quad (15)$$

MATLAB code has been made available in the literature [11] to model this relationship and is used as a starting point in this work. Firstly, the thermal noise is created by a random number generator based on a variance given in equation (16), which is determined by both the absolute thermal noise level, $S_{in-thermal}$, and the system sampling time, *systs*.

$$Variance = \frac{S_{i_n-thermal}}{2systs} = \frac{4kT\gamma g_m}{2systs} \quad (16)$$

Secondly, using the mathematical functions proposed in [11], a bank of single-pole low pass filters was created to produce a noise-shaping filter, which can approximately generate the correct flicker noise response. The transfer function of this noise-shaping filter is given by equation (17).

$$H(s) = 1 + \sum_{n=0}^{K+1} \frac{10^{-0.5n}}{\sqrt{2}} \frac{2\pi f_c}{s + 2\pi 10^{-n} f_c} \quad (17)$$

Where f_c is the device's corner frequency, given in equation (15), and a K value of approximately 10 is required for correct modelling of the flicker noise. The model realization of this noise-shaping filter is illustrated in Figure 5(a). Separate output ports are used for the thermal and flicker noise contributions to allow a better understanding of how these different noise types affect the VCO noise as a whole. A power spectral density comparison of the single device noise model and a simulation in Spectre is shown together in Figure 5(b), confirming correct operation of the model at this level.
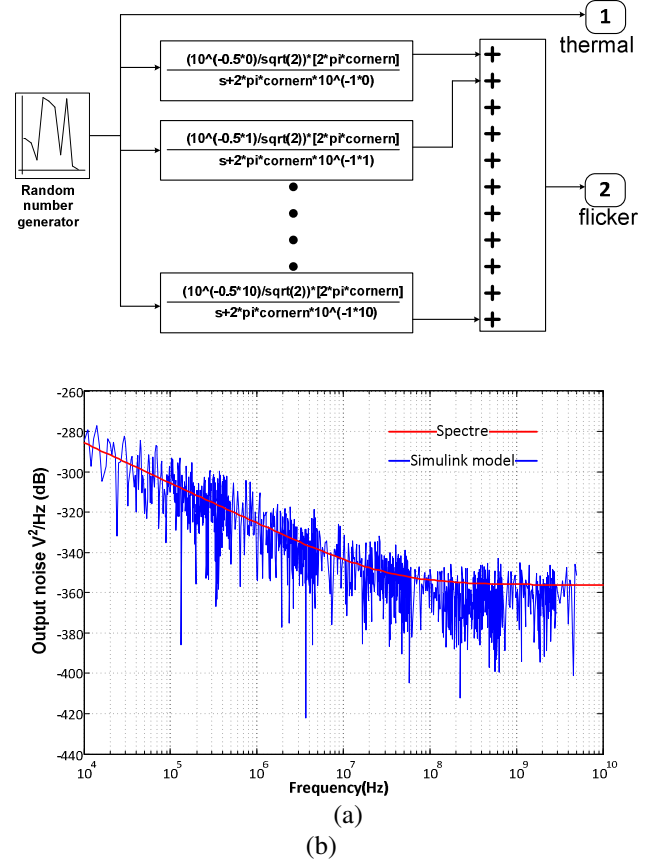

(a)

(b)

Figure 5 Simulink model of thermal and flicker noise sources (a) and PFD of single device noise (b)

1.1   *Combined VCO noise and tuning model*

Having developed both the VCO level tuning model and device level noise model the final stage is to combine both aspects in a model which will predict both the tuning and noise performance of the VCO. The first challenge in achieving this is to relate the noise quantity, currently in the form of current (A) to the VCO time domain jitter (s) and frequency domain phase noise (dBc/Hz@offset). The jitter, Δt_d occurring within a single propagation delay can be calculated by integrating the noise current, $i_n(t)$, over the time interval t_d and dividing by the pull-up/push-down current, I, as described by equations (18) and (19) [10]. The propagation delay and pull-up/push-down current can be obtained directly from the model in Figure 2.

$$v_n = \frac{1}{C}\int_0^{t_d} i_n(t)dt \quad (18)$$

$$\Delta t_d = \frac{v_n}{I} C = \frac{1}{I} \int_0^{t_d} i_n(t) dt \qquad (19)$$

It is possible at this stage to combine 4N noise generators from the previous section for an N stage VCO model where each delay cell has four transistors (Mn1, Mn2, Mp5, Mp6). However, with each noise block requiring 11 transfer functions for flicker noise generation, the total of 44 transfer functions would degrade the simulation efficiency. Furthermore, having to adjust the model structure as the number of stages changes is undesirable, so instead N should be an input variable. For this reason, three simplifications are performed on the model to improve efficiency. First, it is possible to combine pairs of noise contributors into one lumped transistor by making the reasonable assumption that the inverting and control transistors share the same dimensions. This halves the number of noise generators, which greatly enhances the efficiency of the model. Secondly, assuming a lumped transistor noise model it is important to establish the relationship between the control voltage and the trans-conductance of the lumped transistor as this will have an impact on its noise characteristics. As a result of this, the altered noise profile of this lumped transistor can be determined by equations (20) and (21) where g_{m_lump} is its trans-conductance.

$$g_{m\_lump} \approx \mu_n C_{ox} \frac{Wni}{Lni} (Vct - V_{th}) \qquad (20)$$

$$f_c = \frac{K_f g_{m\_lump}}{C_{ox} Wni \cdot Lni} \cdot \frac{1}{4kT\gamma} \qquad (21)$$

Thirdly, for short t_d time intervals it can be assumed that the noise current stays at a constant value within the in-

terval meaning that equation (19) can be reduced to equation (22). If the change in noise current within the time interval is noticeable, however, this so-called jitter amplitude spread is known to be proportional to the length of the time interval and trans-conductance, but inversely proportional to the load capacitance [10]. Furthermore, it is known that the jitter amplitude spread is proportional with the order of device's corner frequency allowing equation (22) to be extended to the more general case of equation (23).

$$\Delta t_d = \frac{1}{I} \int_0^{t_d} i_n(t) dt = \frac{i_n}{I} t_d \qquad (22)$$

$$\Delta t_d(t) = \frac{i_n(t)}{I} t_d \cdot \frac{t_d \cdot g_{m\_lump} \cdot (\log 10(fc))}{C \cdot} \qquad (23)$$

Based on the above refinement the proposed jitter generator is shown in Figure 6 which is a combination of the propagation delay generator and the noise generator. The accuracy of this model can be attributed to the noise current, the push current and the length of the propagation delay all being a function of the control voltage, rather than assuming independence from this important circuit parameter. The resulting full VCO model results in 2N PMOS and 2N NMOS based noise generators for an N stage oscillator. Summing all squares of the noise contributors gives the total noise which is then transformed into the jitter value. In order to determine the phase noise, the instantaneous oscillation frequency and output phase is also available at the model output. The phase noise, which is the parameter of ultimate interest, can be approximated by the power spectral density (PSD) function of extra phase.
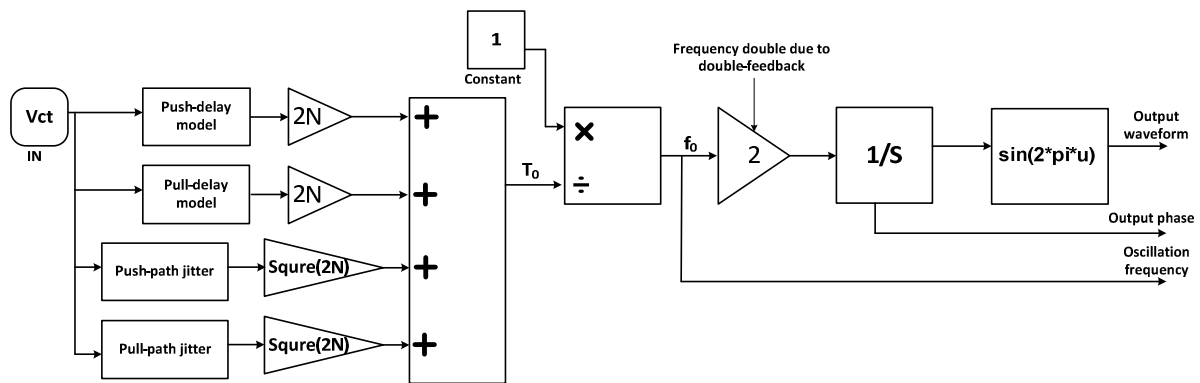

Figure 6 Combination of the noise generator with the VCO behavioral model
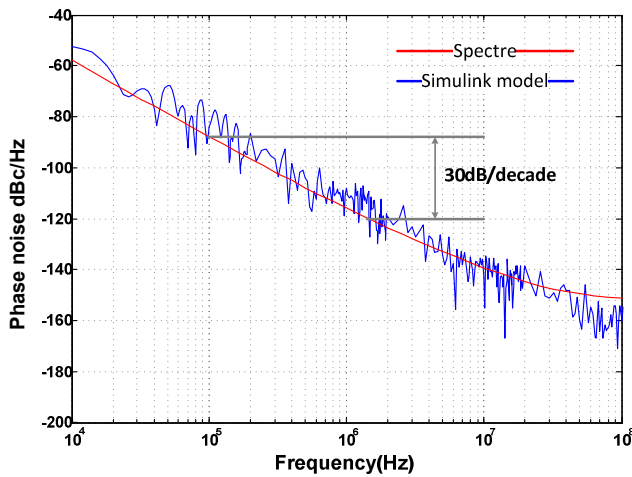
3. Results

In this section the novel VCO noise model is tested and compared to results from an industry standard simulator. A case study circuit was designed for this purpose with the dimensions given in Table 1, which refer to the schematic of Figure 1.
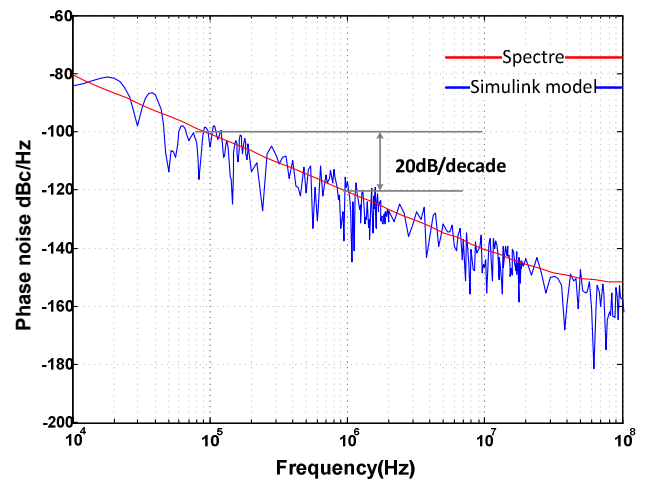
Table 1 Transistor dimensions of design example

Transistor:	W/L (μm):	Transistor:	W/L (μm):
Mp1,Mp2	100/0.4	Mn1,Mn2	64/0.4
Mp3,Mp4	100/0.4	Mn3,Mn4	32/0.4
Mp5,Mp6	199/0.4	Mn5,Mn6	32/0.4

1.2   Phase noise simulations

Figure 7(a) shows the developed model phase noise results using the case study circuit dimensions based on just flicker noise. Here the new model is shown to agree well with post layout simulations of the fully extracted circuit. Both curves have a roll-off factor of 30dB/decade, which demonstrates that the device flicker noise is being modeled correctly. For further analysis the noise source in the model was changed from flicker to thermal, which correctly resulted in a shallower roll-off factor of 20dB/decade [10] as shown in Figure 7(b). The behavioral models in both cases took 1 minutes and 45 seconds to generate, whereas the transistor level simulations took from 3-4 minutes. Although this demonstrates an efficiency saving of 50%-60%, it is important to point out, as discussed in Section 1, that the real benefit of the proposed model is its suitability for simulating the noise of complex systems such as PLLs, due to its time domain nature.

(a)

(b)

Figure 7 Comparison between the proposed Simulink model and Spectre based results for flicker noise (a) and thermal noise (b) induced phase noise.

It is well known that flicker noise in the VCO control voltage plays a more significant role than any other noise source in the oscillator circuit [10] which makes it an interesting aspect to investigate with the proposed model. Within the current mirror structure that generates the control voltage, the diode connected transistor is the major noise contributor and can be modeled by another instance of the device noise model. In order to translate the current noise of the device model to control voltage noise is it multiplied by the transistor's output resistance which is obtained through a simple DC simulation.

Table 2 shows four example designs where the current mirror transistors are varied, keeping all other design parameters the same. For the purposes of fair comparison, the differential control voltages generated from the control module were designed to be almost identical (V_{ct}=1.2V), resulting in almost identical oscillation frequencies. However, a significant difference is apparent for the phase noise performances of these four design examples, which are shown in Figure 8. As in the previous design example, both the circuit simulator based post layout simulation results and the proposed model results were obtained. The phase noise results obtained from these two methods agree strongly for these four analytical design cases, confirming the accuracy of the proposed VCO model.

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Table 2 Varying the control current mirror transistors in four design examples

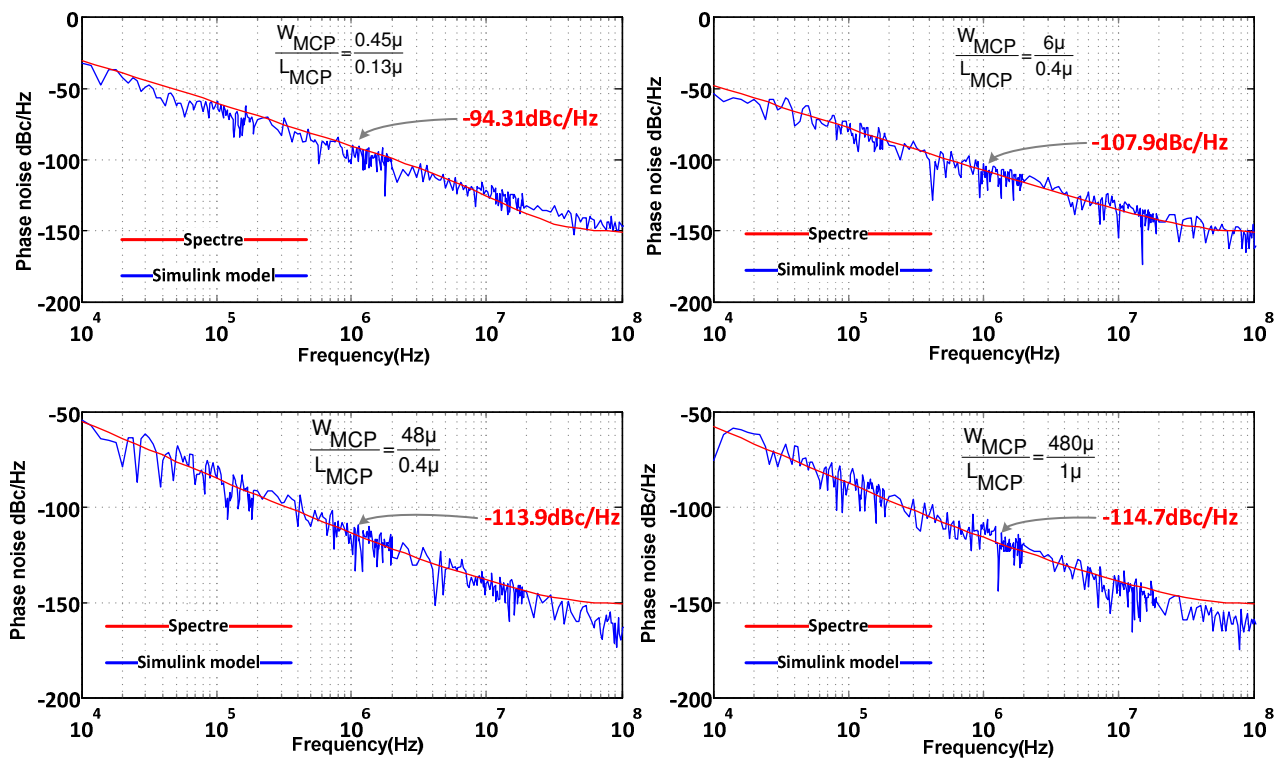| Device	Design 1	Design 2	Design 3	Design 4
M_{cn}	0.15μm/0.13μm	2μm/0.4μm	16μm/0.4μm	160μm/1μm
M_{cp}	0.45μm/0.13μm	6μm/0.4μm	48μm/0.4μm	480μm/1μm
$g_{ds}$of M_{cp}	23μ	44.77μ	374.4μ	849.2μ

Figure 8 Phase noise with different transistor dimensions

As expected, the results clearly show that lowering the transistor output resistance through a greater W/L ratio is an essential requirement for reducing the VCO output phase noise, highlighting the well-known trade-off between power and noise performance. In this example the proposed model has allowed accurate analysis of the VCO output phase noise without paying a penalty in simulation time. The recommended design going forward would be Design 3 which achieves excellent phase noise without the compromise of a large transistor area and correspondingly large gate capacitance, which could cause stability problems in a larger system.

To verify the proposed VCO model further, the VCO design example of the previous section with the recommended control module sizing of Design 3 was realized with a prototype chip fabricated on a standard 120nm 1.2V CMOS process. Figure 1(a) shows the layout view of the chip with the VCO highlighted, and Figure 1(b) shows the die being probed on a high speed wafer probing station. Bench tests used an Agilent E4443A 3Hz-6.7GHz spectrum analyser and gave the phase noise plot in Figure 10. A battery was used for the power source to ensure very low noise from the supply.
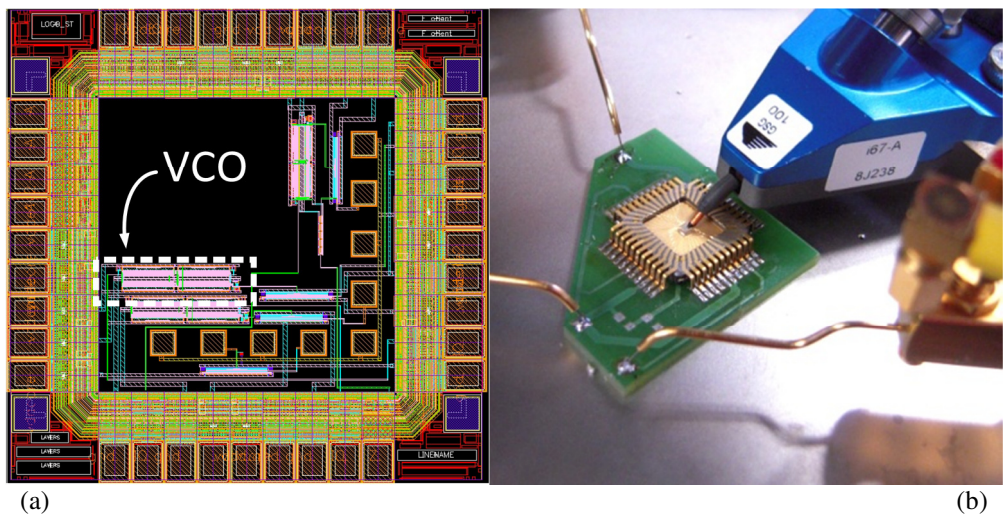
4. Prototype chip

Figure 9 Prototype chip layout view (a) and probe station setup (b)

Table 3 along with the predicted results from the developed model.
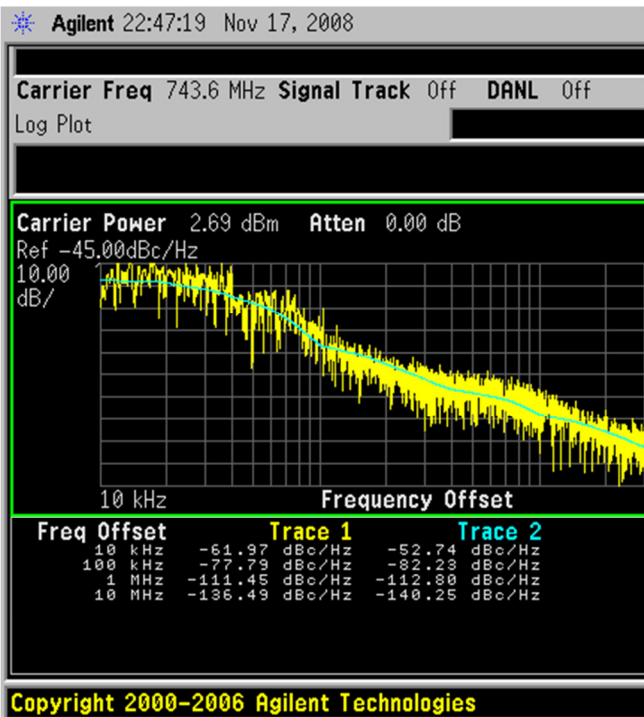

Figure 10 Measured phase noise at *744MHz*

The phase noise spectrum shows a roll off of -30dBc/Hz/decade, indicating that flicker noise is dominant in the design. The results shown in Figure 10 are consistent with the modeling results and simulation results shown in Figure 7(a). It is important to investigate the phase noise with different tuning voltages and measured results for this parameter are summarized within

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Table 3 Measured and simulated phase noise over the full tuning range

Effective control Voltage (V)	Oscillation frequency (MHz)	Measured/simulated phase noise (dBc/Hz)		
		100kHz offset	1MHz offset	10MHz offset
1.2	743.6	-82.23 / -80.09	-112.8 / -110.91	-140.25 / -140.36
1.06	721.7	-73.1 / -81.02	-112.25 / -111.34	-140.06 / -141.78
0.93	685.2	-69.38 / -82.82	-112.55 / -112.92	-139.38 / -142.48
0.8155	646.1	-87.24 / -83.31	-112.26 / -113.19	-139.66 /-142.51
0.7157	569.8	-75.56 / -84.55	-109.14 / -113.43	-137.81 / -143.01
0.619	455.7	-78.27 / -84.78	-109.45 / -114.39	-136.00 / -144.32
0.5	288.9	-79.42 / -85.37	-107.35 / -114.71	-134.75 / -145.8
0.414	164.9	-81.8 / -86.91	-109.32 / -115.85	-135.28 / -145.2
0.353	97.55	-83.17 / -87.32	-110.66 / -116.32	-136.6 / -145.19

The results are very encouraging, given the difficulty in accurately measuring noise in practice. The discrepancies at 100kHz offset and the ramp in the spectrum under 100kHz are attributed to the noise of the DC voltage source, which was not included in the model. The discrepancy towards the lower end of the frequency range with 10MHz offset is due to the noise floor of the testing platform. Elsewhere, the variations of phase noise between the simulated and measurement are generally less than *5dB*.

5. Conclusions

One of the most challenging problems when simulating PLLs is obtaining accurate jitter and phase noise performance from transient simulations. VCOs largely dominate the noise performance of PLLs and this paper presents a novel VCO noise model to address this challenge, which facilitates efficient analysis of phase noise and tuning performance from time domain simulations. The key advantage of this approach is its application in higher level PLL system simulations since commercial software seldom supports transient noise analysis, however there is also the benefit of increased simulation efficiency with reduced simulation times. The accuracy of the predicted phase noise performance using the proposed model has been extensively validated through comparison with both extracted layout simulations and measured results from a 120nm CMOS prototype chip. To demonstrate an application of the model, the effect of control voltage flicker noise on VCO output phase noise has been investigated and guidelines for the voltage control module proposed as a result. Compared with alternative approaches, the proposed model enables circuit designers to correctly and efficiently predict true time domain noise performance in VCOs allowing them to make informed decisions about transistor sizing as a result.

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