Reliability Improvement and Online Calibration of ICs
Using Configurable Analogue Transistors

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***Abstract*—Reliability of electronic circuits over an extended temperature range is a critical consideration in demanding applications such as aerospace and the military. Achieving this reliability on modern deep submicron process nodes is a significant challenge especially for analogue circuits due to the high level of device variability. A novel approach is proposed in this paper that employs online adjustment of configurable analogue transistors (CATs) to address this challenge, significantly improving the consistency of circuit performance over temperature. The proposed method involves optimally sizing configurable devices for temperature and process variation and then employing a calibration lookup table during normal operation to compensate for temperature shifts. In the presented case study of an instrumentation amplifier, the CAT approach is shown to successfully mitigate temperature induced performance loss, demonstrating significant calibration potential and reliability improvement. These advantages are enjoyed at minimal cost in terms of area and complexity overhead, and the process of implementing the circuit changes is highly automated. The promising results detailed in this work demonstrate that the CAT technique has useful applications in the area of reliability improvement for demanding environments.**

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1. Introduction

The application of modern integrated circuits in hostile environments raises several design challenges. Extreme operating temperature and elevated levels of radiation are typical characteristics of hostile environments which significantly affect circuit performance or may lead to premature ageing and potential failure [1-3]. In most cases, such extreme environment applications also place exceptional demands on the reliability of electronic circuits. Space missions and defense are typical examples, where circuit failure may cost millions or in the worst case, human lives. The majority of research in current high-reliability electronics for extreme environments focuses on two areas. The first area is concerned with devices and processes that

enable electronics to operate at extreme temperatures or under high levels of radiation. Examples for this research include silicon carbide (SiC) semiconductors [4], solid-state vacuum devices [5] and packaging and interconnect [6]. The second area is concerned with fault-tolerant circuits, which can resume normal operation despite faults by employing dynamic reconfiguration. Research in fault-tolerant circuits has been carried out for both digital [6] and analogue [7] circuits.

An area of research that has seen extensive exploration in the context of manufacturing yield improvements, but comparatively little in the context of electronics for hostile environments is calibration for device variation and temporal effects. A wide range of approaches on all levels of design exist to improve manufacturing yield or reliability by calibrating circuits after fabrication or during operation, e.g. [8, 9]. Since most of these techniques are optimized for, but not limited to, calibration for yield improvement, they can be employed for online calibration in extreme environments. However, thus far no successful attempts have been demonstrated in applying existing post-fabrication calibration techniques to enable circuits for extreme environments.

Reliability is a measure of how well a system can perform its functions to specification over a certain period and certain conditions. Traditionally, reliability is viewed in the context of hard faults, meaning that the system fails due to individual device faults or irreversible deterioration of device performances. In this case, the exact system performance is less relevant as long as it is within specification because the decision of whether or not a system has failed is a binary yes/no outcome. However, reliability can also be considered from a parametric point of view, referred to as parametric reliability, and considers parametric faults instead of hard faults. A parametric fault is a temporary condition where system performance is moved out of specifications, but returns to its normal value once the cause has been removed. A classic example for a parametric fault mechanism is temperature drift.

As discussed previously, reliability can be optimized by choosing more robust devices and fault-tolerant circuit and system architectures. On the other hand, measures to improve parametric reliability are ideally taken at the circuit level. Examples include variation-tolerant circuit design and online calibration, as will be described in this work.

The Configurable Analogue Transistor (CAT)

In this work, the Configurable Analogue Transistor (CAT) [10], is proposed as a circuit-level calibration technique that can significantly improve reliability and performance over the operating temperature range of circuits in hostile environments. The principle of CAT is to replace certain devices (critical devices) with digitally adjustable width devices, thus allowing circuit performance to be controlled. Because the background of the CAT is in calibration for device variability, it also enables the application of high-variability devices, such as SiC integrated circuits. Since the CAT technique relies on the availability of standard CMOS devices and does not extend the device operating temperature range, the absolute maximum and minimum operating temperature of a circuit are still limited by the underlying fabrication process. However, the CAT technique improves the variation of circuit performance within this range and thus extends the useable operating range of a circuit, that is, the range of temperatures over which it operates to specification. The CAT technique has previously been proposed as a means of improving reliability in hostile environments [11]. However, the discussion of this matter did not consider a specific application and environment. In this paper, temperature is suggested as a possible target environmental parameter for the application of CAT. The application of CAT to improve parametric reliability over temperature is described and the concept illustrated by means of a demonstrator circuit.

The structure of the CAT is shown in Figure 1. It consists of a main device M0 and n calibration devices M1 to Mn, which can be selected through n digital control lines, B1 to Bn. Each of these control lines either grounds the gate of a calibration device or connects it to the gate of the main device, resulting in a total of 2n discrete widths. Although similar circuit structures have previously been used in digitally adjustable analogue circuits, the CAT methodology includes a unique optimal sizing process which ensures the highest possible level of calibration [9].

The CAT technique does not only consist of the configurable CMOS device, but also of a set of design tools. These tools are an integral and unique part of the CAT technique. Figure 2 shows the typical IC design flow where CAT is employed. As can be seen, CATs are primarily applied between schematic capture and layout, with a single post-fabrication calibration step. The individual tools of the CAT design flow are briefly described below.



Figure 1. Structure of the configurable analogue transistor.



Figure 2. Design flow for CAT

The task of the first tool is to determine which devices in a circuit should be replaced by CATs, in a process called Critical Device Identification (CDI). In order to perform CDI, the circuit must be embedded in a testbench and the circuit performances such as gain, bandwidth, etc. must be described by simulator expressions. By means of sensitivity analysis, the CDI tool determines which transistors are most suited for adjusting these particular performances. A difference to conventional calibration techniques is that the addition of calibration elements (CATs) is performed after schematic capture. This means that the designer does not need to concern themselves with finding a good calibration solution during the design of the circuit. Automating this process is not only more efficient in terms of design time, but it also allows optimal selection of critical devices according to the given performance specifications.

The second tool in the CAT design process determines the optimal sizes of the calibration transistors (M1 to Mn) of the CATs. This sizing is based on stochastic information about the performances when the circuit is subject to device parameter variation. An optimal sizing algorithm [12] is then employed to size the CATs such that the overall performance variability of the circuit is minimized. Once the CATs have been sized, the design can proceed to the layout stage, where the CATs are treated like an array of regular CMOS transistors.

Once the circuit has been fabricated, the optimal configuration of CATs is determined for each individual chip. The main focus of this work, is the online reconfiguration of the CATs after fabrication. The description of the CAT design process in this section was with focus on device variability. It will be shown in the next section how this design process and the application of the CAT can also incorporate calibration for temperature variation.

The rest of this paper is structured as follows. Section 2 describes how the CAT can be used for online calibration over temperature. Section 3 applies this online calibration technique to a demonstrator circuit and discusses the obtained results. Section 4 concludes this paper and summarizes the results.

2. Application

Online Calibration Mechanism

The primary design goal of a CAT is to allow post-fabrication calibration to compensate for errors introduced by process variation. After the CAT design flow described in Section 1, each chip is individually tested and the optimal CAT settings to achieve best performance are determined. This optimal configuration is typically stored in nonvolatile on-chip memory so that it can be restored whenever necessary, e.g. after the chip is powered up.

Since both process and mismatch variation are largely time invariant, a static CAT configuration is sufficient to counteract any errors introduced by these mechanisms to achieve optimal performance. However, in this configuration the circuit is still subject to environmental influences, such as temperature, radiation and ageing. Performance degradation introduced by these means cannot be compensated with a static CAT configuration, which calls for an online calibration approach.

Online calibration of a circuit equipped with CAT is conceptually very simple, and requires the CAT configuration to be altered during run-time according to certain rules. In principle, this involves measuring the current system performance and, if necessary, switching to a different CAT configuration that will improve performance. However, there are at least two complications in this generic case. First, to determine the current performance of the circuit, it may be necessary to suspend normal operation and put the circuit in a test mode. Second, determining the optimal CAT configuration can be an iterative process, during which the circuit is likely not to operate at optimal performance. The result from these issues is that the circuit will not be able to perform its normal operation continuously and that it may operate outside specifications for a certain amount of time. In this work, it will be shown that in the case of temperature, online CAT reconfiguration can be based on a simple lookup table without the need to measure system performance or perform iterative optimization.

Online Temperature Compensation

Online calibration of CATs with respect to temperature is a special case that lends itself well to practical implementation. The dependence of circuit performance on temperature is well described through SPICE models and the temperature of the chip can be easily measured continuously, which allows the system to conduct the appropriate reconfiguration before the performance has dropped below a threshold. Additionally, the temperature behavior of the circuit can be accurately modeled before fabrication, which reduces the reconfiguration process to a simple lookup table. This type of online reconfiguration can be carried out without any interruptions in the operation of the circuit, because the current performance does not need to be measured and the optimal configuration is predetermined. However, signals processed in the system may still be subject to short glitches at the moment when the CAT configuration is changed.

Figure 3 illustrates the required system architecture for online CAT reconfiguration. The temperature of the chip is continuously monitored, and the corresponding optimal CAT configurations obtained from a lookup table. There are several points to note about this concept. First, in most practical applications, temperature does not need to be measured continuously. Instead, it may be sufficient to sample its value at given intervals or only under certain conditions. The latter is especially interesting for applications onboard spacecraft, where the system temperature may only change, for example, after certain navigational maneuvers. Similarly, the temperature of a planetary probe is likely to be known either from the current time of day or the probe’s main instruments, which completely removes the need for on-chip temperature measurement. Furthermore, discontinuous sampling of temperature also reduces power consumption, since the temperature sensor and the associated reconfiguration hardware operate only in short bursts. Secondly, the task of digitizing temperature readings and looking up the corresponding configuration words in memory bear very little computational load. It is therefore practical to handle this task in an already existing digital processing system, rather than a dedicated computer for CAT reconfiguration. Again, this is especially beneficial for applications in which energy conservation is a primary requirement.

In summary, the hardware overhead for incorporating online CAT reconfiguration is potentially very low. Apart from the CATs themselves, the only other required on-chip component is a temperature sensor, which may be as simple as an appropriately biased PN junction. All remaining components, such as the ADC, computation, lookup table and configuration memory may be incorporated into an existing signal processing system at little additional cost.

Design of CAT for online temperature calibration

The CAT design process when considering temperature variation is in principle no different to the process introduced in Section 1. However, instead of performing a Monte Carlo simulation across the process parameter space to gain stochastic information about the circuit’s performance, a simple temperature sweep across the specified range is sufficient. Figure 5 shows a typical temperature dependence of a particular circuit performance, A, exhibiting a negative temperature coefficient. To find the optimal sizes of the CAT devices, the established optimal sizing algorithm can be used with the temperature dependence as an input distribution. The resulting CATs will be sized such that the mean deviation from the nominal value over the entire temperature range is minimized. In addition to optimal CAT sizing, the design process also outputs a configuration lookup table, mapping temperature to the CAT configuration.



Figure 3. System structure for online temperature calibration using CATs

For the purposes of illustration, a possible outcome of calibrating the example performance with a 2-bit CAT device is also shown in Figure 4. The CAT configuration that is active in a certain temperature range is indicated by numbers along the temperature axis. For very low temperatures, configuration 1 is chosen, which reduces the numerical value of the performance by ∆A1. This reduction in value brings the mean of the performance between Tlow and T1 closer to the nominal performance, Anom. If the temperature rises above T1, configuration 2 is chosen. This reduces the performance only by ∆A2, thereby bringing the performance closer to the nominal value, and so on. This example should also reinforce the point that neither the temperatures at which the configurations change nor the sizing of the CAT devices, corresponding to the change in performance, are arbitrary, but must be optimized during the design stage.

While this approach to temperature compensation is valid for a single chip at nominal device parameters, it does not consider the various parameter variation processes that occur in real circuits. A real circuit design, which includes optimally sized CAT devices, is replicated several times on a wafer to yield a large number of chips. While ideally all chips from a certain design have identical behavior, in reality the performance of any two chips and indeed identical devices on the same chip is not the same. These processes are referred to as process and mismatch variation, respectively and are modeled though stochastic processes in the fundamental device parameters.



Figure 4. Principle of temperature compensation using CATs.

The consequences of these variation mechanisms on the application of CATs to compensate temperature variation are two-fold. Firstly, because the designed CAT must provide good results on all produced chips of a given circuit, optimal sizing of the CAT must now consider both temperature and parameter variation. This brings the CAT from simple temperature sweeps back to its original stochastic domain, where the temperature can be considered as an additional random variable. Secondly, because the CAT must now compensate parameter and temperature variations, the achievable level of calibration will be lower than in the case where only temperature was considered. Nevertheless, the expected improvement in performance variation is still well defined through the stochastic processes.

A crucial difference between the temperature-only and variation-aware CAT application lies in the post-fabrication stage. In the case where only temperature is considered, it is sufficient to generate a single configuration lookup table from the simulations that is valid for all chips of a particular circuit. When considering additional parameter variations, not only must the initial CAT configuration be determined on a chip-by-chip basis, but also an individual lookup table generated for each chip. This is necessary because both the initial CAT configuration and the temperature behavior are likely different between chips. However, generation of the lookup table is computationally very inexpensive and follows directly from the initial CAT configuration. Therefore, this does not require any additional post-fabrication test equipment and does not significantly prolong post-fabrication calibration time.

1. TABLE I. Opamp device sizes and component values

|  |  |  |  |
| --- | --- | --- | --- |
| Device | Dimensions | Device | Dimensions |
| **MP0** | **8.75µm / 0.35µm** | MN2 | 35µm / 0.35µm |
| MP1 | 8.75µm / 0.35µm | MN3 | 35µm / 0.35µm |
| MP2 | 105µm / 0.35µm | MN4 | 52.5µm / 0.35µm |
| MP3 | 105µm / 0.35µm | MN5 | 52.5µm / 0.35µm |
| MP4 | 105µm / 0.35µm | MN6 | 175µm / 0.35µm |
| **MP5** | **105µm / 0.35µm** | MN7 | 175µm / 0.35µm |
| MN0 | 8.75µm / 0.35µm | MN8 | 98µm / 0.35µm |
| MN1 | 8.75µm / 0.35µm | MN9 | 50µm / 0.35µm |
| Component | Value | Component | Value |
| R | 823kΩ | C | 623fF |

TABLE II. Instrumentaton amplifier component values

|  |  |  |  |
| --- | --- | --- | --- |
| Component | Value | Component | Value |
| R1 | 99k | R5 | 100k |
| R2 | 99k | R6 | 100k |
| R3 | 100k | **R7** | **2k** |
| R4 | 100k |  |  |

TABLE III. Nominal circuit performances

|  |  |  |
| --- | --- | --- |
| Performance | Symbol | Nominal value |
| Gain | G | 94.35 |
| Bandwidth | BW | 1.99×106 |
| Offset voltage | VOS | 5.55×10-5 |

Demonstrator Circuit

In order to illustrate the merits of the CAT technique in the context of this paper, it is applied to a standard instrumentation amplifier comprised of three identical operational amplifiers. The amplifier block schematic is shown in Figure 5, while the operational amplifier used in the circuit is shown in Figure 6. The resistors in the instrumentation amplifier are modeled as diffusion resistors and n-well resistors rather than ideal resistors for two reasons. Firstly, the availability of accurate foundry models means that any nonidealities of on-chip passive components are modeled correctly, resulting in a realistic description of overall circuit performance after fabrication. Secondly, being structurally equivalent to a MOS device without a gate, diffusion resistors can be replaced by CATs and therefore tuned. As will be shown later, this is of great importance in this particular circuit.



Figure 5. Circuit diagram of the instrumentation amplifier.

Table I and Table II show the transistor sizes for the operational amplifier, and resistor values for the instrumentation amplifier respectively. The nominal circuit performances are listed in Table III. The circuit is implemented in a standard 0.35µm CMOS process, where the foundry device SPICE models are valid within the temperature range from -40°C to +125°C. The critical devices in this circuit, found using the algorithm in [13], are R7, MP0B and MP5B for gain, bandwidth and offset voltage, respectively. This diffusion resistor and the MOSFETs of operational amplifier B are set in bold in Tables I and II.



Figure 6. Circuit diagram of the operational amplifier

It is worth noting that one of the resistors has been identified as a critical device. Because the operational amplifiers operate under negative feedback, gain is primarily determined by the passive components with very little effect from active components. Therefore, the only viable way to adjust gain is to equip certain passive components with a CAT structure. In the case of resistor R7, this task is very straightforward because diffusion resistors lend themselves readily to the CAT structure. Bandwidth, on the other hand, is determined by the passive components and the gain-bandwidth product of the operational amplifier and can therefore be adjusted through transistors. Finally, offset voltage is not dependent on the passive components at all and can be adjusted by varying the transistors in the differential input stages.

3. Results

Temperature and parameter variation

In this section, the results from applying online CAT calibration to a circuit that is subject to temperature and process parameter variations are presented. As described in Section 1, the CAT transistors are sized according to stochastic information about temperature and process parameter behavior. During operation, the best CAT configuration is chosen from a lookup-table, which is customized for each chip.

To illustrate this concept, a Monte Carlo simulation of the instrumentation amplifier was performed. In addition to process and mismatch variation, temperature was added as a random Monte Carlo variable. This means that each Monte Carlo iteration represents a particular circuit at a particular temperature. Since the CAT technique is based on stochastic information about circuit performance, it is possible to derive all necessary information for CAT sizing from this, without the need for a full temperature sweep for every set of Monte Carlo parameters. Indeed, such information would be meaningless for CAT sizing because the CAT is sized for a particular circuit, of which multiple copies are produced on a single wafer. CAT sizes can therefore not be optimized for a single chip, but for a particular circuit, for which only stochastic information is relevant. Figure 7 shows the results of the Monte Carlo simulation, with the circuit performances plotted against temperature and marked with the symbol ×. Gain and bandwidth clearly show a dependency on temperature, with the performances of individual circuits scattered in a band around the ideal. This scattering represents the magnitude of process parameter variation. In the case of offset voltage, the influence of mismatch variation outweighs the temperature dependence by far. This means that for a particular chip, CAT will be able to reduce the inherent offset voltage well, but online temperature calibration will not be able to improve temperature drift greatly. This can be visualized by the fact that each CAT transistor only has a finite number of possible configurations. When the effects of process parameter or mismatch variation are small compared to the effects of temperature, only a small set of the possible configurations are required for the initial post-fabrication tuning, leaving ample free configurations for online calibration. However, if the effects of process parameter variation outweigh the effects of temperature, the majority of configurations are required for the initial calibration, leaving few or no free configuration states for online temperature calibration.

Without calibration, the standard deviation of gain is 6.85, the standard deviation of bandwidth is 222kHz and the standard deviation of the offset voltage is 3.69mV. These results are listed in the upper section of Table IV.

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Figure 7. Temperature dependence of performances at with process and mismatch variation.

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For each Monte Carlo parameter set, the optimal ideal adjustment in the critical devices is determined by applying the method described in [13] until all circuit performances are within 1% of their nominal value. However, it is clear that this adjustment is unrealistic because it would require transistor widths to be adjustable with infinite granularity. In practice, the number of calibration transistors in a CAT is limited. The optimal sizing algorithm for CAT is then applied to these ideal adjustments to give optimal sizes for CATs with three adjustment transistors, resulting in eight discrete adjustment steps for each critical device. The resulting sizes of the CAT devices are listed in Table V. For each Monte Carlo parameter set, the configuration of each CAT is chosen to be closest to the ideal adjustment.

The performances after CATs have been introduced in the circuit are marked with + in Figure 7. Over the entire temperature range, the standard deviations of gain, bandwidth and offset voltage are reduced to 2.81, 65.1kHz and 1.39mV, respectively. These calibrated performances are listed in the lower section of Table IV. As can be seen, introduction of CATs again significantly reduces variation in performances over temperature.

It is worth noting that a small number of performances after CAT calibration are significantly further from the nominal values than the majority. These points correspond to parameter sets for which no improvement in performance could be achieved within the adjustment constraints. Such instances will also occur in a real set of chips, where there will be a small number that cannot be calibrated at all. Because such circuits are already identified at the post-fabrication adjustment stage, they can be discarded as necessary.

Although the results obtained thus far show a significant reduction in performance standard deviation over the entire temperature range, no statement about parametric reliability has yet been made. For each performance, a pass band can be defined around the mean within which that performance is considered to operate to specification. For both Monte Carlo and CAT calibrated performances, parametric reliability can then be defined as the probability of a certain circuit at a certain temperature being within these bands. Although this definition is equivalent to the definition of yield, there is a practical difference introduced by the inclusion of temperature.

Whilst yield is concerned with the probability of a circuit meeting specifications at static operating conditions, parametric reliability is concerned with the circuit meeting specifications over the entire range of operating conditions. For the purpose of illustration, the pass bands have been defined as ±5, ±100kHz and ±1mV, for gain, bandwidth and offset voltage, respectively. For the unadjusted Monte Carlo results, the system’s parametric reliability is 4.0%. When CAT is applied to the system, parametric reliability increases to 80.8%. This is a significant increase in the parametric reliability of the system. Although this improvement in reliability seems exceptionally large when compared to the improvement in standard deviations, it is not surprising. Firstly, standard deviation is greatly affected by even a few outliers, while they do not contribute as greatly to a decrease in reliability. Secondly, reliability requires all three performances to be within the pass band, which is very improbable in the Monte Carlo case, leading to a low uncompensated reliability.

Application for temperature compensation

The results from the statistical analysis give an overview of the expected performance improvement as a statistical result over a large number of chips over the process parameter and temperature space. To illustrate the improvements achieved by CATs in single circuits, a single Monte Carlo parameter set is chosen and a full temperature sweep performed on it. This corresponds to the performance of an individual chip form a production run.



Figure 8. Temperature dependence of gain for one chip

Similar to the previous section, the top section of Figure 8 shows the gain of the demonstrator circuit plotted against temperature. On the bottom of Figure 8, the currently chosen CAT configurations (0-7) for all three critical devices are plotted against temperature. This corresponds to the lookup table required for each individual chip and has been obtained by again finding the optimal ideal adjustment for each point and then selecting the closest configuration. Since there are only a finite number of CAT configurations, the temperature drift in gain can clearly be seen in Figure 8. However, as in the conceptual illustration of Figure 4, the absolute error in gain over temperature is improved.

4. Conclusions

In this paper, the application of the Configurable Analogue Transistor (CAT) was extended to online calibration of circuit performance for temperature variation. In an example circuit, the change in performance over the specified temperature range could be improved by between 59.0% and 70.7%, resulting in a significant improvement and potentially increasing the operational temperature range and performance of precision circuits. Furthermore, since the CAT is used to compensate for process parameter or mismatch variation at the same time, the inherent precision of circuit performance is also improved significantly. This mitigation of process variability effects enables high-temperature processes that suffer from great inherent device variability, such as SiC, to be used for precision analogue circuits. Enabling such technologies to be used in new applications will have a significant impact on the possible performance of systems in hostile environments, such as aerospace or defense.

References

Biographies

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| **Robert Rudolf** Add your bio and picture hereIEEE**Reuben Wilcock** (M’02) is a Senior Research Fellow in the in the Electrical and Electronics Engineering Group at the University of Southampton. He graduated with a B.Eng. in Electronic Engineering at the University of Southampton in 2001, and in 2004 was awarded a PhD for the development of switched-current filters and phase locked loops. He spent a year working as a Senior Design Engineer for a high tech startup company, then rejoined the University of Southampton as a Research Fellow in 2006. Since working as a research fellow he has been a named researcher on a number of high profile grants from the EPSRC and ICUK to develop novel analogue ICs and more recently interface circuits and control systems for micro-machined sensors. He has over 25 peer reviewed journal and conference publications.**Peter Wilson**peter_wilson (M’99, SM’05) is a Reader in Electronics in the Electrical and Electronics Engineering Group at the University of Southampton. He received the B.Eng. in Electrical and Electronic Engineering and Postgraduate Diploma in Digital Systems Engineering from Heriot-Watt University, Edinburgh, Scotland, in 1988 and 1992 respectively; an M.B.A from the Edinburgh Business School obtained in 1999 and obtained his PhD from the University of Southampton in 2002. He has published more than 80 papers in the areas of Electronic Design Automation, Power Electronics, Magnetics and Integrated circuit design. He has authored a number of books, and has managed numerous funded research projects in the areas of power electronics, integrated circuit design, modeling & simulation and renewable energy.He worked in the Navigation Systems Division of Ferranti plc., Edinburgh, Scotland from 1988-1990 on Fire Control Computer systems, before moving in 1990 to the Radar Systems Division of GEC-Marconi Avionics, also in Edinburgh, Scotland. During the period 1990-1994 he worked on modeling and simulation of Power Supplies, Signal Processing Systems, Servo and Mixed technology systems. From 1994-1999 he worked as European Product Specialist with Analogy Inc. During this time he developed a number of models, libraries and modeling tools for the Saber simulator, especially in the areas of Power Systems, Magnetic Components and Telecommunications. Since 1999 he has been working in the Electronic Systems and Devices group and more recently in the newly formed Electrical and Electronic Engineering research Group at the University of Southampton, UK. His current research interests include improving variability in integrated circuits, Analog and mixed Signal IC Design, modeling of magnetic components in electric circuits, power electronics, renewable energy systems, VHDL-AMS modeling and simulation, and the development of electronic design tools. He is a Member of the IEE, Senior member of the IEEE and a Chartered Engineer in the UK. He was Technical Program Chair for IEEE BMAS 2008, General Chair of IEEE BMAS for 2009, and finance chair for ETS 2006, EBTW 2006 and FDL 2010. He is the co-chair of IEEE Std 1076.1.1 and chair of IEEE Std 1573. |
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