UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND THE ENVIRONMENT

# ANALYSIS AND REDUCTION OF DC-LINK CAPACITOR VOLTAGE/CURRENT STRESS IN THREE-LEVEL PWM CONVERTERS

by

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## ABSTRACT

FACULTY OF ENGINEERING AND THE ENVIRONMENT
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# ANALYSIS AND REDUCTION OF DC-LINK CAPACITOR VOLTAGE/CURRENT STRESS IN THREE-LEVEL PWM CONVERTERS

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Power electronic converters are in the heart of modern renewable energy and motor drive systems. This Thesis focuses on the converter dc-link capacitor (bank), which is a costly component and a common source of failures. The Thesis is divided into two parts.

The first part examines the voltage and current stress induced on dc-link capacitors by the three most common converter topologies: The conventional two-level converter, the Neutral-Point-Clamped (NPC) three-level converter, and the Cascaded H-Bridge (CHB) three-level converter. The expressions derived for the rms capacitor current and its harmonics can be used as a tool for capacitor sizing.

The harmonic analysis is then extended to systems that incorporate multiple converters connected to a common dc-link capacitor. The effect of introducing a phase shift to the converter carrier waveforms is examined, showing that reductions in the order of 30 to 50% in the common capacitor rms current can be achieved using appropriate phase shifts.

The second part tackles the dc-link capacitor balancing problem, also known as Neutral Point (NP) balancing problem of the three-level NPC converter. Initially, a circuit that halves the voltage stress caused by the NP voltage oscillations (ripple) on the switching devices the NPC converter is proposed. The circuit consists of low voltage rated components which offer the advantages of lower losses, volume and cost, as compared to other balancing circuits.

Subsequently, the study focuses on modulation strategies for the NPC converter. Starting with Nearest-Vector (NV) strategies, it proves that the criterion of the direction of dc-link capacitor imbalance, which is commonly adopted by NV strategies for performing the task of capacitor balancing, poses a barrier in achieving minimum NP voltage ripple. A new criterion is proposed instead, together with an algorithm that incorporates it into existing NV strategies. For the interesting case of NPC converters operating as motor drives, the resulting reduction in the amplitude of NP voltage ripple ranges from 30 to 50%.

The study finishes with an extension of the previous concept to create hybrid (combinations of NV and non NV) strategies for the NPC converter. Hybrid strategies are proposed that can eliminate NP voltage ripple, introducing lower switching losses and output voltage distortion as compared to other methods used for the same purpose. The proposed strategies perform equally well when the converter operates with non linear or imbalanced loads. All results are verified by extensive simulations using MATLAB-Simulink.

## *Declaration of authorship*

I, Georgios I. Orfanoudakis, declare that the thesis entitled "Analysis and reduction of dc-link capacitor voltage/current stress in three-level PWM converters" and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
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- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published in peer-reviewed conferences and journals (please see list of publications in the following page).

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## *List of publications*

1. G. I. Orfanoudakis, S. M. Sharkh, M. A. Yuratich and M. A. Abu – Sara, "Loss comparison of two- and three-level inverter topologies", *5th IET International Conference on Power Electronics, Machines and Drives (PEMD 2010)*, 19 – 21 Apr. 2010.

2. G. I. Orfanoudakis, S. M. Sharkh and M. A. Yuratich, "Analysis of DC-link capacitor losses in three-level neutral-point-clamped and cascaded H-bridge voltage source inverters", *IEEE International Symposium on Industrial Electronics (ISIE 2010)*, 4 – 7 July 2010.

3. G. I. Orfanoudakis, S. M. Sharkh and M. A. Yuratich, "Circuit for reducing devices voltage stress due to DC-link capacitor voltage ripple in a Neutral-Point-Clamped inverter", *14th European Conference on Power Electronics and Applications (EPE 2011)*, 30 Aug. – 1 Sept. 2011.

4. G. I. Orfanoudakis, S. M. Sharkh and M. A. Yuratich, "Capacitor size reduction for multiple inverter systems", *IET Conference on Renewable Power Generation (RPG 2011)*, 6 – 8 Sept. 2011.

5. G. I. Orfanoudakis, M. A. Yuratich and S. M. Sharkh, "Nearest-Vector Modulation Strategies with Minimum Amplitude of Low-Frequency Neutral-Point Voltage Oscillations for the Neutral-Point-Clamped Converter", *IEEE Transactions on Power Electronics*, 2012 (to be published, available on IEEE Xplore).

6. G. I. Orfanoudakis, M. A. Yuratich and S. M. Sharkh, "Hybrid Modulation Strategies for Eliminating the Low-Frequency Neutral-Point Voltage Oscillations in the Neutral-Point-Clamped Converter", *IEEE Transactions on Power Electronics*, 2012 (to be published, available on IEEE Xplore).

7. G. I. Orfanoudakis, M. A. Yuratich and S. M. Sharkh, "Analysis of DC-link Capacitor Current in Three-Level Neutral-Point-Clamped and Cascaded H-Bridge Inverters", *IET Power Electronics*, 2012 (to be published).

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*Πᾶσα δόσις ἀγαθὴ καὶ πᾶν δώρημα τέλειον*

*ἄνωθέν ἐστι, καταβαῖνον ἐκ σοῦ*

*τοῦ Πατρὸς τῶν φώτων*

*Every pure donation and every perfect gift*

*comes from above, descending from you*

*the Father of lights*

(from the Orthodox liturgy and the Epistle of James)

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To my beloved wife Agathi,

to our families,

and to the memory of

Nikolaos Papadakis,
Eirini Orfanoudaki,
Nikolaos Liapakis,
Anastasia Liapaki,
Adamantia Voulgaraki,
Aikaterini Voulgaraki,

who left during these years

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# List of Abbreviations and Acronyms

| | |
|---|---|
| 2L | two-level |
| 3L | three-level |
| ac | alternating current |
| AFE | active front end |
| Band-NTV | Band implementation of nearest-three-vector modulation strategy |
| Band-NV | Band nearest vector |
| Band-Sym | Band implementation of Symmetric modulation strategy |
| BLDC | brushless dc |
| CHB | cascaded H-bridge |
| CI | controllable interval |
| CLC | converter loss calculator |
| dc | direct current |
| EMI | electro-magnetic interference |
| ESR | capacitor equivalent series resistance |
| FE | front end |
| GTO | gate turn-off thyristor |
| HF | high frequency |
| IGBT | insulated gate bipolar transistor |
| IGCT | integrated gate commutated thyristor |
| LF | low frequency |
| ML | multilevel |
| MOSFET | metal oxide semiconductor field effect transistor |
| NP | neutral point |
| NPC | neutral point clamped |

| | |
|---|---|
| NPS | neutral point shifter |
| NTV | nearest-three-vector modulation strategy |
| NV | nearest vector |
| PD | phase disposition |
| PV | photovoltaic |
| PWM | pulse width modulation |
| rms | root mean square |
| SHE | selective harmonic elimination |
| SPWM | sinusoidal pulse width modulation |
| SPWM+3$^{rd}$ h. | sinusoidal pulse width modulation with 1/6 third harmonic injection |
| SV | space vector |
| SVM | space vector modulation |
| Sym | Symmetric modulation strategy |
| THD | total harmonic distortion |
| UI | uncontrollable interval |
| VSC | voltage source converter |
| WTHD | weighted total harmonic distortion |

# List of Symbols

| | |
|---|---|
| C | capacitor |
| $C$ | capacitance |
| D | diode |
| $d_{\mathbf{V}}$ | duty cycle of Space Vector **V** |
| $D_{1x}$ | anti-parallel diode of module $V_{1x}$ |
| *decr* | decrement of NP voltage ripple decrement by Band-NV strategies |
| $F$ | function for the geometric wall model |
| $f$ | fundamental frequency |
| $f_s$ | switching frequency |
| $f_{s,eff}$ | effective switching frequency |
| $i_{NP}$ | locally averaged NP current |
| $I_{NP}(\mathbf{V})$ | NP current resulting from Space Vector **V** |
| **L0**, **L1** | long Space Vectors |
| **M** | medium Space Vector |
| $M$ | modulation index for carrier-based strategies |
| $m$ | modulation index for SVM strategies |
| $N$ | number of inverters in a multiple inverter system |
| $P_C$ | dc-link capacitor losses |
| $P_{C,\max}$ | maximum (affordable) dc-link capacitor losses |
| $PF$ | load power factor |
| $r$ | rotating factor for harmonics in multiple inverter systems |
| $R$ | value of Region register for NPC converter operating region |
| $R_C$ | dc-link capacitor ESR |
| $R_{C,HF}$ | value of dc-link capacitor ESR for high-frequency harmonics |

| | |
|---|---|
| $r_I$ | ratio of NP current over output rms current |
| $R_{th}$ | heat sink thermal resistance |
| **S0**, **S1** | pairs of small Space Vectors |
| $\mathbf{S0_1}$, $\mathbf{S0_2}$ | small Space Vectors of pair **S0** |
| $\mathbf{S1_1}$, $\mathbf{S1_2}$ | small Space Vectors of pair **S1** |
| $S_{1x}$ | switching element (e.g. IGBT) of module $V_{1x}$ |
| *SC* | set of switching constrains for an NPC converter modulation strategy |
| $T$ | fundamental period |
| $T_{\text{int}k}$ | duration of $k^{\text{th}}$ switching interval |
| $T_s$ | switching period |
| $V_{1x}$ | IGBT-diode module comprising IGBT $S_{1x}$ and diode $D_{1x}$ |
| $v_C$ | dc-link capacitor voltage |
| $v_{\text{C1,ref}}$ | reference voltage for dc-link capacitor $C_1$ |
| $V_{dc}$ | dc-link voltage |
| $v_{\text{NP}}$ | NP voltage |
| $v_{\text{NP,inv}}$ | NP voltage seen from the NPC converter |
| $v_{\text{NP},pk}$ | peak value of NP voltage ripple |
| $v_{\text{NP,ref}}$ | NP voltage reference |
| $v_s$ | voltage of the NPS circuit capacitor |
| $v_{x,ref}$ | reference voltage for phase *x* |
| $x_{\text{S0}}$ | duty cycle distribution factor for Space Vectors $\mathbf{S0_1}$,$\mathbf{S0_2}$ |
| $x_{\text{S1}}$ | duty cycle distribution factor for Space Vectors $\mathbf{S1_1}$,$\mathbf{S1_2}$ |
| $\mathbf{Z_1}$, $\mathbf{Z_2}$, $\mathbf{Z_3}$ | zero Space Vectors for the NPC converter |
| $\delta_{\text{int}k}$ | duty cycle of $k^{\text{th}}$ switching interval |
| $\delta_x$ | duty cycle for phase *x* |

| | |
|---|---|
| $\Delta Q_{AB}$ | charge taken from the NP during interval [$\theta_A$, $\theta_B$] |
| $\Delta Q_{AB,\min}$ | minimum value for $\Delta Q_{AB}$ |
| $\Delta V_{AB,\min}$ | minimum peak-peak NP voltage variation during interval [$\theta_A$, $\theta_B$] |
| $\Delta V_{C,\max}$ | maximum (affordable) dc-link capacitor peak-peak voltage variation |
| $\Delta V_{\mathrm{NP,Band}}$ | peak-peak NP voltage variation for a Band-NV strategy |
| $\Delta V_{\mathrm{NP,Conv}}$ | peak-peak NP voltage variation for a conventional NV strategy |
| $\Delta V_{\mathrm{NP}\|SC}$ | peak-peak NP voltage variation under switching constrains *SC* |
| $\Delta V_{\mathrm{NPn}}$ | normalised peak-peak NP voltage variation |
| $\Delta V_{\mathrm{UI1}}$ | peak-peak NP voltage variation during $\mathrm{UI}_1$ |
| $\theta$ | reference angle |
| $\theta_c$ | carrier phase angle |
| $\theta_{c,opt}$ | optimal carrier phase shift for multiple inverter systems |
| $\phi$ | load power angle |
| $\omega_c$ | carrier angular frequency |
| $\omega_o$ | fundamental angular frequency |

# Chapter 1

## Introduction

## 1.1 Multilevel power converters

Power electronic converters are in the heart of several systems that require manipulation of electrical energy. In the past, the majority of such systems could be found in the industrial and manufacturing sectors, but this situation steadily changed during the last decades. The need for securing a more sustainable and energy-efficient future brought power electronic converters closer to our society, as parts of systems like wind turbines, photovoltaic (PV) energy systems [1], and electric cars [2]. Converters were also introduced in areas such as train traction and ship propulsion [3].

The increasing power demands in modern, as well as in more traditional high-power applications (compressors, pumps, fans, mills, conveyors, etc.) created a challenge, which the power electronics community faced in two ways: A) By developing higher voltage- and current-rated semiconductors (up to 8 kV and 6 kA), to achieve increased power rating for traditional converter topologies, and B) By building multilevel converter topologies, which could be based on (higher numbers of) conventional power semiconductors [4, 5]. Although multilevel converters brought in a number of challenges with regards to their circuit implementation and control, their evolution allowed them to be the preferred solution for today's medium and high-power applications. In comparison to the conventional (two-level, 2L) converter, they offer a series of advantages, including increased efficiency, reduced harmonic distortion of output voltages and currents (thus less filtering requirements), lower common-mode voltages, and reduced voltage derivatives ($dv/dt$).

Figure 1.1 illustrates a classification of the most common ac-ac converter topologies. A first classification can be done according to whether the conversion is direct or indirect. Indirect conversion involves an intermediate dc step, and is performed in two stages: ac-dc and dc-ac. Converters operating according to it, can then be classified according to the type of their intermediate dc (voltage or current) source. This thesis covers the Voltage Source Converters (VSCs) shown shaded in Figure 1.1, namely the 2L converter and the multilevel (three-level, 3L) Neutral-Point-Clamped (NPC) and Cascaded H-Bridge (CHB) converters.

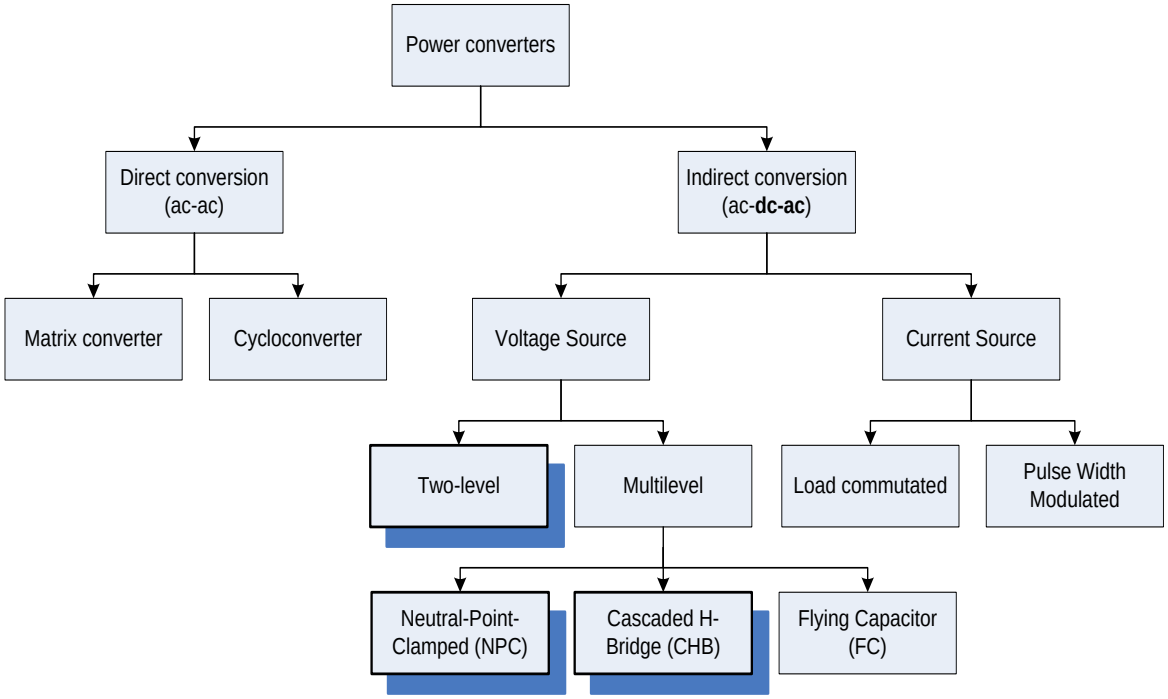


**Figure 1.1.** Multilevel converter classification **[4, 5]**.

The 2L converter is the conventional converter topology, considered today as traditional, but still dominating in low-voltage applications [6]. The 2L converter is included in parts of this study for reasons of completeness and comparison, but the main focus is on the 3L topologies.

The NPC converter, invented in 1980, is currently the preferred topology for industrial applications in the voltage range of 2.3 to 6 kV [7]. Several converter manufacturers, including ABB, Siemens and Converteam, provide commercial products based on this topology, with output voltages up to 6.6 kV and maximum power exceeding 40 MW [8]. Many of these products incorporate a back-to-back configuration of two NPC converters [9], one of which operates as an Active Front End (AFE) to reduce input current harmonics, while the other operates as inverter.

The CHB topology was first proposed in 1971 [5], but received attention from the industry later than the NPC topology. Commercial CHB converters are available with voltage and power ratings up to 13.8 kV and 120 MW, respectively. These increased ratings are achieved as a result of the series connection of more than one H-Bridge modules per phase, which also provides a higher number (7 to 19) of phase voltage levels.

The above topologies can be built using different types of power semiconductors. In cases that high blocking voltages (3.3 kV or more) are required, the commonly preferred semiconductors are high-voltage IGBTs or IGCTs. These devices have gradually replaced the formerly used GTOs [8]. For lower voltages (up to 1.7 kV), commercially available converters utilize low-voltage IGBTs, but power MOSFETs also provide an additional alternative [5]. It is worth noting that major power semiconductor manufacturers [10, 11] recently launched NPC phase leg modules (comprising four 650 V IGBTs and two clamping diodes), supporting the use of this topology in low-voltage applications.

Regarding the modulation of multilevel converters, a variety of strategies are available in the literature [12, 13, 14, 15]. Similarly to the six-step operation of 2L converters, staircase operation of multilevel converters is adopted in cases that the switching frequency should be minimized (be equal to the fundamental frequency). Likewise, Selective Harmonic Elimination (SHE) techniques are applied if switching at a small multiple (commonly less than 10 times) of the fundamental frequency can be tolerated. However, the main volume of modulation strategies for multilevel converters consists of carrier-based and Space-Vector Modulation (SVM) strategies, which operate at higher switching frequencies. These strategies perform Pulse Width Modulation (PWM), that is, adjustment of the duration and position of output voltage pulses within each switching period, to improve the converter voltage spectra. Pulse generation in carrier-based strategies relies on comparing the converter reference voltage waveforms (one for each phase) with a number of carrier waveforms. The results of the comparisons provide the switching states of the corresponding converter phase legs. Different carrier-based strategies are defined by varying the shape of the reference, or the number, shape, or phase of the carrier waveforms. SVM strategies, on the other hand, determine the durations (duty cycles) and positions of the generated voltage pulses computationally. Again, different SVM strategies can be defined by adjusting the selection, duty cycles and switching sequences of the available Space Vectors (SVs). Comparisons of most common carrier-based and SVM strategies with respect to parameters like converter losses, voltage harmonic distortion (THD or WTHD) and common-mode voltage, can be found in [13, 16]. Furthermore, conversions of strategies from one type to the other have been demonstrated in [17, 18, 19].

A significant amount of research is being carried out on modulation strategies for multilevel converters, with the aim of optimizing aspects of their performance and reducing

their cost. A decrease in converter losses, for instance, enhances the converter efficiency, but also provides the possibility of using a simpler cooling system. Similarly, lower values of output voltage THD or common-mode voltage, improve the converter power quality and Electro-Magnetic Interference (EMI), respectively, while reducing the cost of the relevant (differential/common-mode) filters [20, 21, 22, 23]. This study investigates modulation strategies and techniques that can reduce the size and cost of another converter component: the dc-link capacitors.

## 1.2 DC-link capacitors – Challenges in three-level converters

Figure 1.2 summarizes some typical configurations of power conversion systems employing one or more VSCs. In cases that power comes from an ac source, such as the grid or a generator, a Front End (FE) and possibly a transformer are required to perform the ac-dc conversion and provide the desirable dc voltage level. Most common FE's are 6- and 12-pulse diode rectifiers [24], but 2L as well as NPC converters operating as AFE's are also used to enhance the quality of the input and dc-side current.

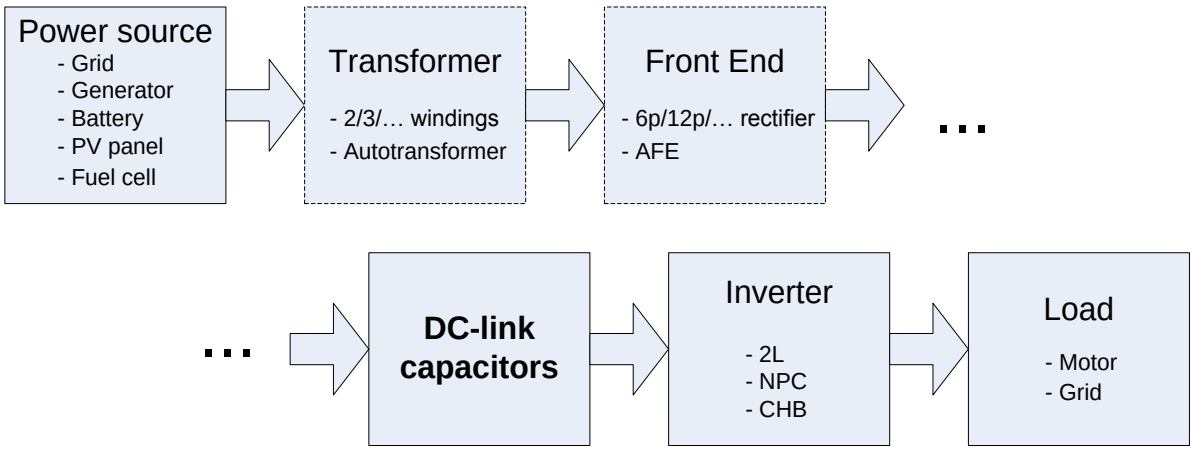


**Figure 1.2.** General block diagram of a power conversion system. Dashed-line boxes denote components that may not be present in certain systems.

DC-link capacitors have a multiple and critical role in the system. Primarily, they form a low-inductance dc source for the system's VSC(s), providing a conduction path for their fast-varying (pulsed) dc-side currents. They should therefore be in place even in cases of PV or

fuel cell dc-source systems, since these sources are not able to conduct such currents. Furthermore, they provide an intermediate energy storage stage which is essential for handling transitory or oscillating (zero-average) differences between the input and output power.

Capacitor lifetime is affected by voltage and thermal stresses occurring during the operation of a converter [25, 26]. Assessment of these stresses is essential for appropriately sizing the dc-link capacitor (bank) and avoiding premature failures. The following two sections provide an overview of characteristics and issues related to the dc-link of the NPC and CHB converter topologies.

### 1.2.1 The dc-link of the NPC converter

The dc-link of the three-phase, 3L NPC converter comprises two capacitors, connected at the Neutral Point (NP) of the dc-link. The design and operation of the converter are based on the assumption that the NP voltage w.r.t. the negative dc-link is approximately half the dc-link voltage ($V_{dc}$), thus the voltages of the two dc-link capacitors are approximately balanced. Capacitor balancing is an essential requirement for the NPC converter, since voltage imbalance beyond a certain extent causes voltage stress on the overcharged capacitor, as well as on the converter modules that switch across it. Excessive imbalance that appears recurrently during the converter operation also increases the chances for module failure due to cosmic radiation [27]. Additionally, the imbalance distorts the output (PWM) voltage waveform, unless it is compensated by the converter modulation strategy [28].

Voltage imbalance can appear in two forms during the operation of the NPC converter: A) As a voltage deviation, typically appearing during a transient, and B) As a low-frequency voltage oscillation during the converter's steady-state operation. The first type of imbalance will be referred to as transient imbalance in this study, while the low-frequency dc-link capacitor voltage oscillation is widely known as NP voltage ripple. A system FE providing two separate dc sources (of $V_{dc}$/2 each) connected at the NP, can prevent capacitor voltage imbalances. However, the NPC converter is commonly supplied by a single source, such as a 12-pulse rectifier. The following three approaches are then available in the literature to tackle the balancing problems:

A) Balancing circuits – Additional power circuitry can be introduced to the NPC converter to restore voltage balance after transients and decrease NP voltage ripple. Balancing circuits proposed in the literature [29, 30] operate as charge pumps, transferring charge from one dc-link capacitor to the other.

B) Modulation strategies – Conventionally, the NPC converter is modulated by Nearest-Vector (NV) strategies [4]. NV strategies, such as the well-known Nearest-Three-Vector (NTV) strategy, are able to handle transient imbalances but cannot avoid NP voltage ripple. The amplitude of the generated ripple increases with the inverter modulation index and decreases with the load power factor. Feed-forward techniques have been developed to remove the associated output voltage distortion, without, though, being able to reduce the voltage stress on dc-link capacitors and inverter modules [28, 31]. NP voltage ripple can only be eliminated by non Nearest Vector (non NV) modulation strategies, like the ones proposed in [32, 33, 34]. However, non NV strategies operate at a higher switching frequency, therefore increasing the converter switching losses. Additionally, they have a negative impact on the quality of the output (PWM) voltage waveform. A detailed discussion on NV and non NV strategies for the NPC converter is presented in Chapter 6.

C) Capacitor over-sizing – The amplitude of NP voltage ripple is inversely proportional to the capacitance of the dc-link capacitors. Capacitor can therefore be over-sized, to reduce the NP voltage ripple down to a level where the unwanted effects described at the beginning of this section are tolerable.

The NPC topology can be extended to output more than three (phase voltage) levels. Nevertheless, as demonstrated in [35], the dc-link capacitor voltages of such higher-order converters cannot be retained by conventional modulation strategies (the voltage of certain capacitors collapses, while others become overcharged). Strategies that can overcome this problem increase the converter switching losses and distort the PWM voltage waveform. The converter losses are also increased due to the series connection of clamping diodes, required to withstand great fractions (up to 5/6, for a seven-level converter) of the dc-link voltage. As a consequence of the above drawbacks, commercial NPC converters are exclusively based on the 3L topology [5].

### 1.2.2 The dc-link of the CHB converter

The CHB converter does not have a single dc-link; instead, it requires an isolated dc-link for each of the H-Bridges it comprises. Namely, the three-phase, 3L CHB converter requires three isolated dc-links, commonly provided by a phase-shifting transformer with three secondary windings. Each winding supplies a 6-pulse rectifier, which connects to the dc-link of an H-Bridge. The windings are phase-shifted by 20, 0, and −20 degrees, respectively, w.r.t. the primary [24], similarly to the case of an 18-pulse rectifier. As a result, input current harmonics are reduced compared to those of 6- or 12-pulse rectifiers, which can be sufficient for 2L and NPC converters. Nevertheless, the above advantage comes at the cost of a more complicated transformer, a higher number of (three-phase diode bridges for) rectifiers, and a 6- instead of an 18-pulse dc-side current for each H-Bridge.

Despite its increased dc-link requirements, the CHB is the preferred topology for multilevel converters with five or more phase voltage levels, built using a series connection of two or more H-Bridges (cells) per phase leg. Several modulation strategies have been developed to balance the real power output between the cells [36, 37], which determines the dc-side current of the respective rectifiers. Balanced dc-side currents lead to cancellation of input current harmonics and nominal operation for the multi-winding transformer.

Finally, due to the structure of its dc-link, the CHB converter has found limited application in regenerative or back-to-back configurations. Examples of such configurations for multilevel CHB converters can be found in [38, 39].

## 1.3 Aim, structure, and contribution of the Thesis

This Thesis examines the effect that 3L NPC and CHB converters have on their dc-link capacitors. It aims to contribute towards improved converter designs, by reducing capacitor size requirements and offering solutions to dc-link-related problems.

Its individual objectives are outlined below:

1. to quantify the voltage and current stress induced on dc-link capacitors by 3L NPC and CHB converters, and relate it to capacitor size requirements,
2. to investigate how this stress is affected by the converter modulation strategy,

3. to examine multiple inverter systems with a common dc-link capacitor, and derive methods to decrease the stress and size of this capacitor,
4. to reduce NP voltage ripple for the NPC converter, by means of a balancing circuit
5. to review the state-of-the-art modulation strategies for the NPC converter and analyse their operation with the aims of creating
    i. NV strategies with reduced amplitude of NP voltage ripple, and
    ii. non NV strategies which eliminate NP voltage ripple, introducing less switching losses and output voltage distortion (see Section 1.2.1).

According to these objectives, the main body of the Thesis is thematically divided into two parts:

The first part, comprising Chapters 2 to 4, covers the structure, modulation and modelling in MATLAB-Simulink of the 2L, NPC, and CHB converters (Chapter 2), and examines the voltage and current stress induced on dc-link capacitors by each of them (Chapter 3). Expressions are derived for the rms capacitor current and its harmonics, while a method is proposed for estimating parameters required for capacitor sizing. The harmonic analysis of the capacitor current is then extended to systems that incorporate multiple inverters connected to a common dc-link capacitor (Chapter 4).

The second part, consisting of Chapters 5 to 7, tackles the dc-link capacitor balancing problem of the NPC converter. Initially, a circuit that reduces the voltage stress caused by the NP voltage ripple on the switching devices of the converter is proposed (Chapter 5). The study then focuses on modulation strategies, proposing a concept to minimize the NP voltage ripple generated by NV strategies (Chapter 6). Finally, Hybrid (that is, combinations of NV with non NV) strategies are considered, which are capable of eliminating NP voltage ripple from the NPC converter (Chapter 7).

Chapter 8 presents the conclusions of this study, and outlines related future work. Finally, the Appendices include supplementary material (derivations, MATLAB-Simulink models and code, etc.), as well as two pieces of research examining converter IGBT-diode losses (Appendix B) and transformerless PV inverters (Appendix C). This research was carried out during a 6-month placement in TSL Technology Ltd, which sponsored this PhD.

The contribution of this Thesis is summarized below:

*Analysis of dc-link capacitor current in three-level NPC and CHB inverters (Chapter 3)*

Capacitor sizing for NPC and CHB inverters is investigated, based on an analysis of dc-link capacitor current. The rms value and harmonic spectrum of the capacitor current are derived using known methods from the 2L inverter. A new, numerical approach is also proposed for calculating the capacitor rms current and voltage ripple. MATLAB code is given for the proposed approach, which can be easily adapted to different modulation strategies. Capacitor sizing parameters derived according to this approach are presented for a number of common modulation strategies and are used to compare the requirements of the examined 3L topologies.

*Capacitor size reduction for multiple inverter systems (Chapter 4)*

Harmonic analysis of the dc-link capacitor current is performed on systems with multiple inverters, sharing a common dc-link capacitor. The capacitor current spectrum is derived for two-level and three-level CHB inverter systems, according to the number of inverters they comprise. The effect of introducing a phase shift between the inverter reference or carrier waveforms is then investigated, to reveal potential reductions in dc-link capacitor rms (ripple) current. It is shown that significant reductions of 40% – 50% in the capacitor rms current can be achieved, especially for three-phase inverter systems.

*Circuit for reducing devices voltage stress due to dc-link capacitor voltage ripple in an NPC inverter (Chapter 5)*

A circuit is proposed, capable of halving the NP voltage ripple seen by the NPC inverter modules. The circuit provides an alternative to over-sizing the inverter's dc-link capacitors, or using non NV modulation strategies that increase the switching frequency and associated losses. The circuit structure and operation are described, and the ratings of its components are determined. The benefits it offers are illustrated through the comparison with other solutions, on the basis of an example NPC inverter design.

*Nearest-Vector modulation strategies with minimum amplitude of low-frequency Neutral-Point voltage oscillations for the NPC converter (Chapter 6)*

Initially, a derivation of the minimum amplitude of NP voltage ripple that can be achieved by NV modulation strategies for the NPC converter is presented. It is then shown that the criterion of the direction of dc-link capacitor imbalance, which is commonly adopted by NV strategies for performing the task of capacitor balancing, poses a barrier in achieving this minimum. A new criterion is proposed instead, together with an algorithm that incorporates it into existing NV strategies. For the case of NPC inverters operating as motor drives, the resulting reduction in the amplitude of NP voltage ripple ranges from 30 to 50%. The proposed approach has the advantage of avoiding the significant increment in switching losses and output voltage harmonic distortion, caused by other methods.

*Hybrid modulation strategies for eliminating low-frequency Neutral-Point voltage oscillations in the NPC converter (Chapter 7)*

NV strategies generate NP voltage ripple under several converter operating conditions. Non NV strategies can eliminate this ripple, but at the expense of higher switching losses and PWM voltage harmonic distortion (WTHD). A simple way of creating hybrid strategies (as combinations of NV and non NV strategies) is proposed, which are also able to eliminate NP voltage ripple. The approach maximizes the participation of NV – therefore minimizing the drawbacks of non NV – strategies, and can be applied to any type of load (non linear and/or imbalanced).

*Converter IGBT-diode losses (Appendix B)*

An analytical study of semiconductor (switching and conduction) losses for the 2L, 3L NPC, and 3L CHB inverter topologies is presented. The derived loss expressions are written in terms of the inverter operating parameters and the selected semiconductor (IGBT-diode module) characteristics. The use of a converter loss calculator (CLC), built according to the loss expressions, is also demonstrated. The calculator is a tool that facilitates converter design, providing the means to appropriately select modules and adjust converter operating parameters.

*Single-phase transformerless PV inverter (Appendix C)*

Traditionally, single-phase inverters for PVs included transformers which provided galvanic isolation between the PV array and the grid. The size, weight, and cost, however, added to the inverter due to a transformer, created a trend for developing transformerless PV inverter topologies. During the last ten years, a number of such topologies have been proposed and applied to successful commercial products. This Appendix discusses the special features of transformerless PV inverters and proposes a new topology of this type (Patent pending). The structure and modulation of the proposed topology are illustrated, while its operation is validated by simulations using MATLAB-Simulink.

# Chapter 2

## Converter topologies – Structure, modulation and modelling

## 2.1 Converter Topologies

This section presents the structure of the conventional 2L, and the 3L NPC and CHB converter topologies, together with their switching states and conduction paths.

### 2.1.1 The two-level converter

The three-phase 2L converter, illustrated in Figure 2.1, consists of three legs (*a*, *b*, *c*), each comprising two switching modules ($V_{1a} - V_{2a}$, $V_{1b} - V_{2b}$, $V_{1c} - V_{2c}$). The modules are formed by an active switch (IGBT, IGCT, MOSFET, etc.) and a diode, connected anti-parallel to the switch. The three converter legs are connected across a common dc-link capacitor (C), which provides a low-inductance path for the rapidly varying currents through the modules.

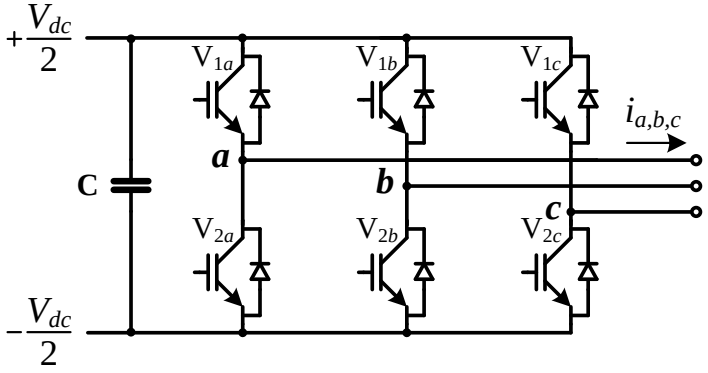


**Figure 2.1.** Two-level converter topology.

The active switching of the modules are controlled (i.e. turned on/off) by gating signals given to the module drivers. The gating signals for modules $V_{1x}$ and $V_{2x}$ will be symbolised as $g_{1x}$ and $g_{2x}$, respectively, where $x$ can be *a*, *b*, or *c*. Each gating signal can be equal either to 0 (switch is off) or to 1 (switch is on). However, $g_{1x}$ and $g_{2x}$ should never be made equal to 1 at the same time, because this would short-circuit the converter's dc-link capacitor. During the converter operation, $g_{1x}$ and $g_{2x}$ for each leg are therefore complementary (apart from short intervals of dead-time, during which both signals are set to 0).

Figure 2.2 illustrates the possible switching states ($s_x$) of each converter leg, defined by the allowed combinations of the gating signals. In the 2L converter, each leg has two possible switching states, $s_x$ = 1 or 0, outputting a phase voltage of $+V_{dc}/2$ and $-V_{dc}/2$, respectively. For a given state, the conduction path changes according to the direction of current. It can be

noticed, though, that the phase voltage is solely dependent on the gating signals; it is not affected by the phase current.

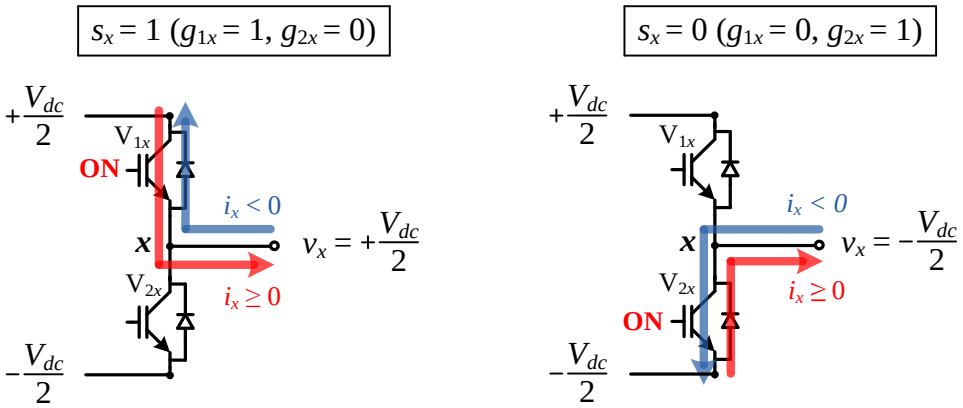


**Figure 2.2.** Switching states and conduction paths for a leg of the two-level converter.

### 2.1.2 The NPC converter

Each leg of the NPC converter comprises four switching modules ($V_{1x}$ – $V_{4x}$) and two diodes ($D_{5x}$ and $D_{6x}$). The converter's dc-link consists of two capacitors ($C_1$ and $C_2$), connected at the converter NP.

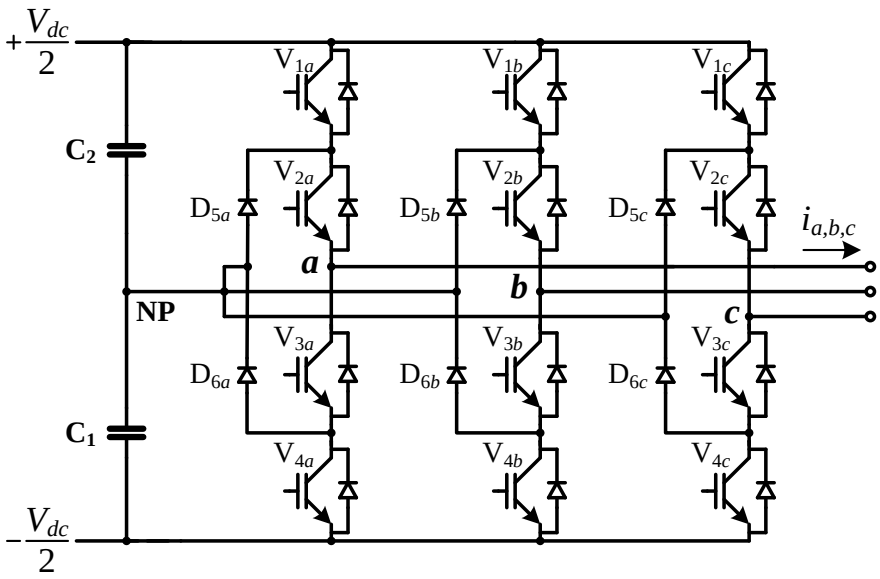


**Figure 2.3.** NPC converter topology.

The topology takes its name from the fact that the (clamping) diodes $D_{5x}$ and $D_{6x}$ clamp the voltage of the points found between the outer and inner switching modules, to the NP

voltage. This results in each converter module switching across the voltage of one of the dc-link capacitors. If the capacitors are balanced, the switching voltage for each module is therefore $V_{dc}/2$.

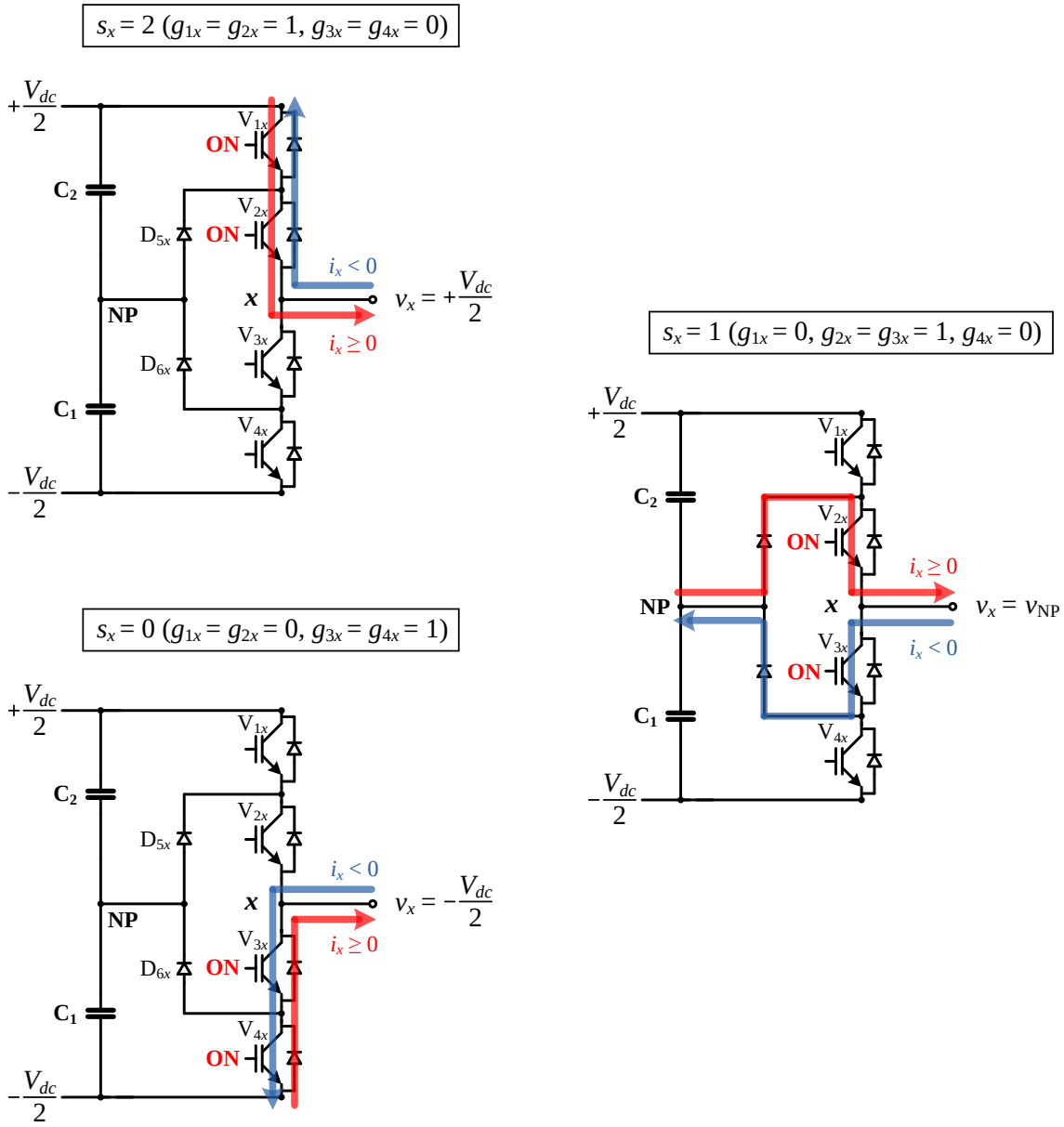


**Figure 2.4.** Switching states and conduction paths for a leg of the NPC converter.

The gating signals are provided to each leg of the NPC converter to turn on two adjacent modules at any time. Turning on the upper/lower three adjacent modules of a leg would short-circuit the upper/lower dc-link capacitor, respectively, while turning on all four modules, would short-circuit the whole dc-link. Consequently, each leg can only be found at

three different switching states, $s_x$ = 2, 1, or 0, illustrated in Figure 2.4. The phase voltage is equal to $+V_{dc}/2$, $v_{NP}$ and $-V_{dc}/2$, respectively. Again, the conduction path changes according to the direction of current, but the phase voltage remains unaffected.

### 2.1.3 The CHB converter

Unlike the 2L and 3L NPC, the CHB converter does not comprise three legs connected to a common dc-link. Instead, it is based on three H-bridge cells (single-phase, 3L converters), each having its own, isolated dc-link. As compared to the 2L and NPC, each cell of the CHB needs to have half the dc-link voltage, for the converter to be able to generate the same (fundamental) output voltage. This has been illustrated in Figure 2.5, by setting the cells' dc-link voltages to $V_{dc}/2$ in place of $V_{dc}$. As for the case of the NPC converter, the module switching voltage is therefore $V_{dc}/2$.

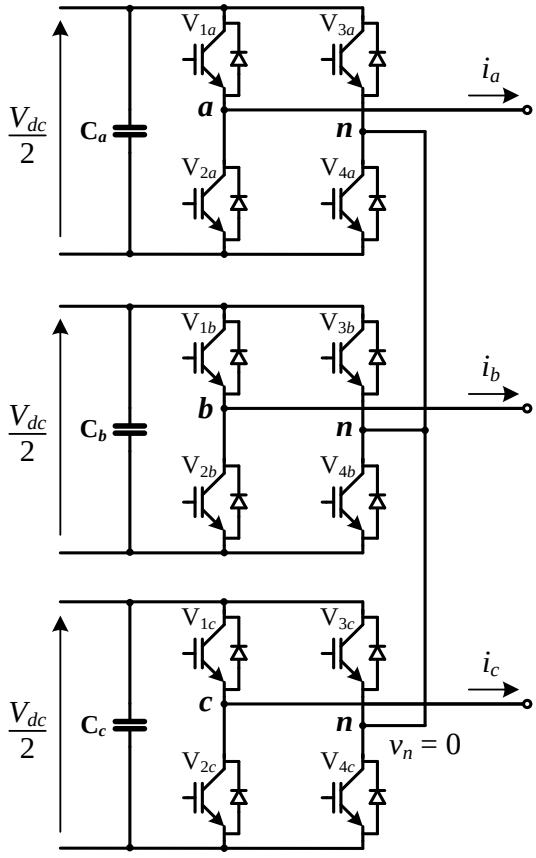


**Figure 2.5.** CHB converter topology.

The three cells are connected at a common neutral, *n*, as shown in Figure 2.5. Each cell can have four different switching states, resulting from turning on two of the cell modules that do not belong to the same leg. Figure 2.6 illustrates the allowed switching states, together with the respective conduction paths. As for the NPC converter, states 2 and 0 produce a phase voltage of $+V_{dc}/2$ and $-V_{dc}/2$, respectively. Both of the remaining states, 1a and 1b, produce a phase voltage of zero, since they connect the cell output to the neutral (*n*).

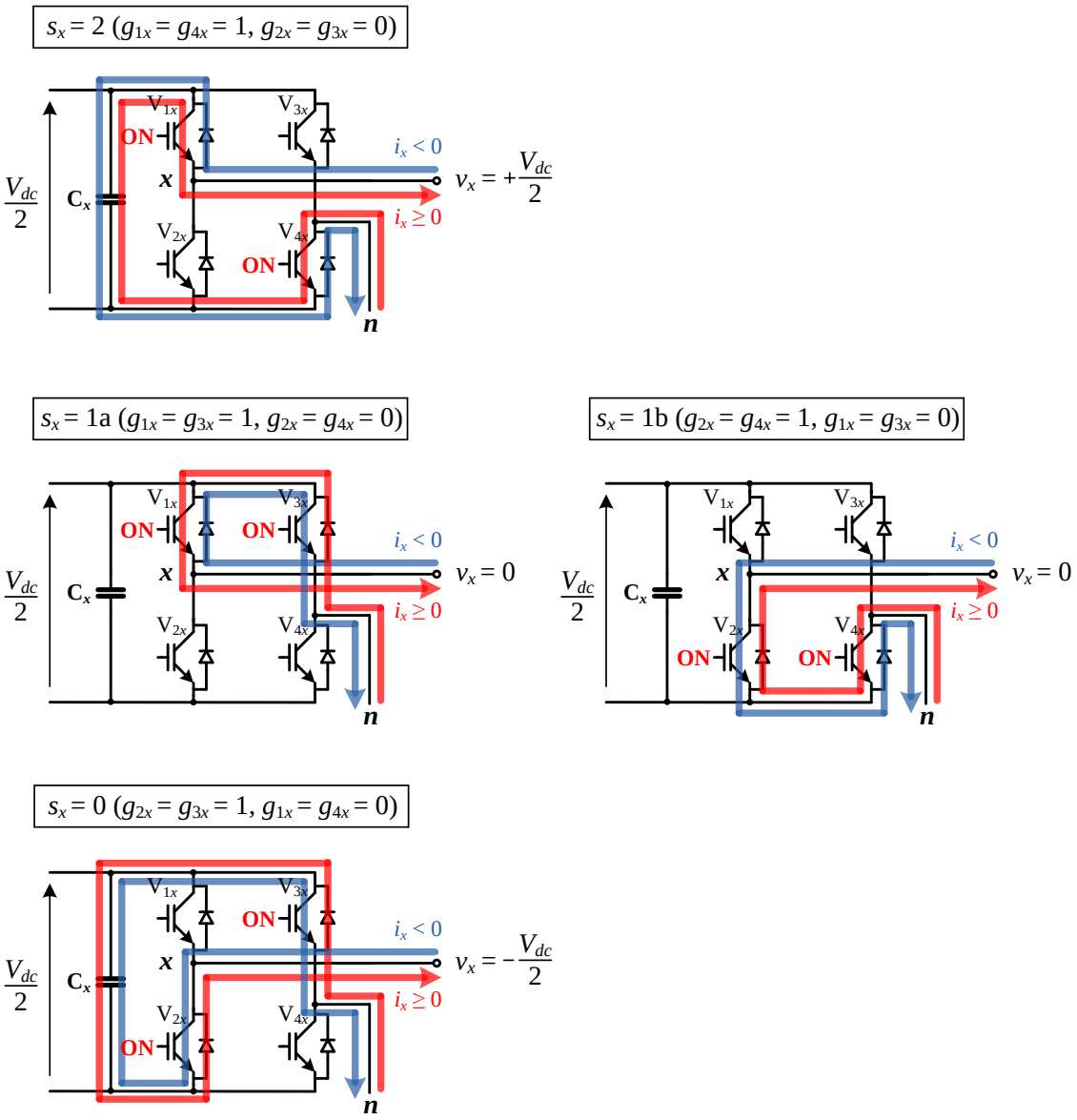


**Figure 2.6.** Switching states and conduction paths for a leg (H-Bridge) of the CHB converter.

Table 2.1 below summarizes the structural characteristics of the described topologies, relating them to their phase/line PWM voltage levels.

| | 2L | 3L NPC | 3L CHB |
|---|---|---|---|
| **No of active switches** | 4 | 4 | 4 |
| **No of diodes** | 4 | 6 | 4 |
| **No of isolated dc-links** | 1 | 1 | 3 |
| **Dc-link voltage** | $V_{dc}$ | $V_{dc}$ | $V_{dc}/2$ |
| **Switching voltage** | $V_{dc}$ | $V_{dc}/2$ | $V_{dc}/2$ |
| **Phase voltage levels** | 2 | 3 | 3 |
| **Line voltage levels** | 3 | 5 | 5 |

**Table 2.1.** Summary of converter structural and output voltage characteristics.

## 2.2 Pulse Width Modulation strategies

Unlike low-power transistors, power semiconductors do not operate in the linear amplification range. Power modules are only switched between their on and off states, in order to decrease their on-state losses. As a consequence, the process of amplification of low-voltage reference signals in Power Electronic converters is based on Pulse Width Modulation (PWM) strategies. PWM strategies generate pulsed voltage waveforms whose average (over a switching cycle) is equal to respective reference signals. Depending on the way they are implemented, PWM strategies can be categorised as carrier-based or Space-Vector Modulation (SVM) strategies.

### 2.2.1 Carrier-based strategies

Carrier-based strategies utilise a set of reference and carrier waveforms to generate the converter PWM voltages. Three reference waveforms, one for each converter leg, are used in three-phase converters. A reference waveform provides the desired value of output voltage for the respective phase, normalised with respect to $V_{dc}/2$. For the case of Sinusoidal PWM (SPWM), the reference waveforms for phases *a*, *b*, and *c*, are respectively given by the following equations:

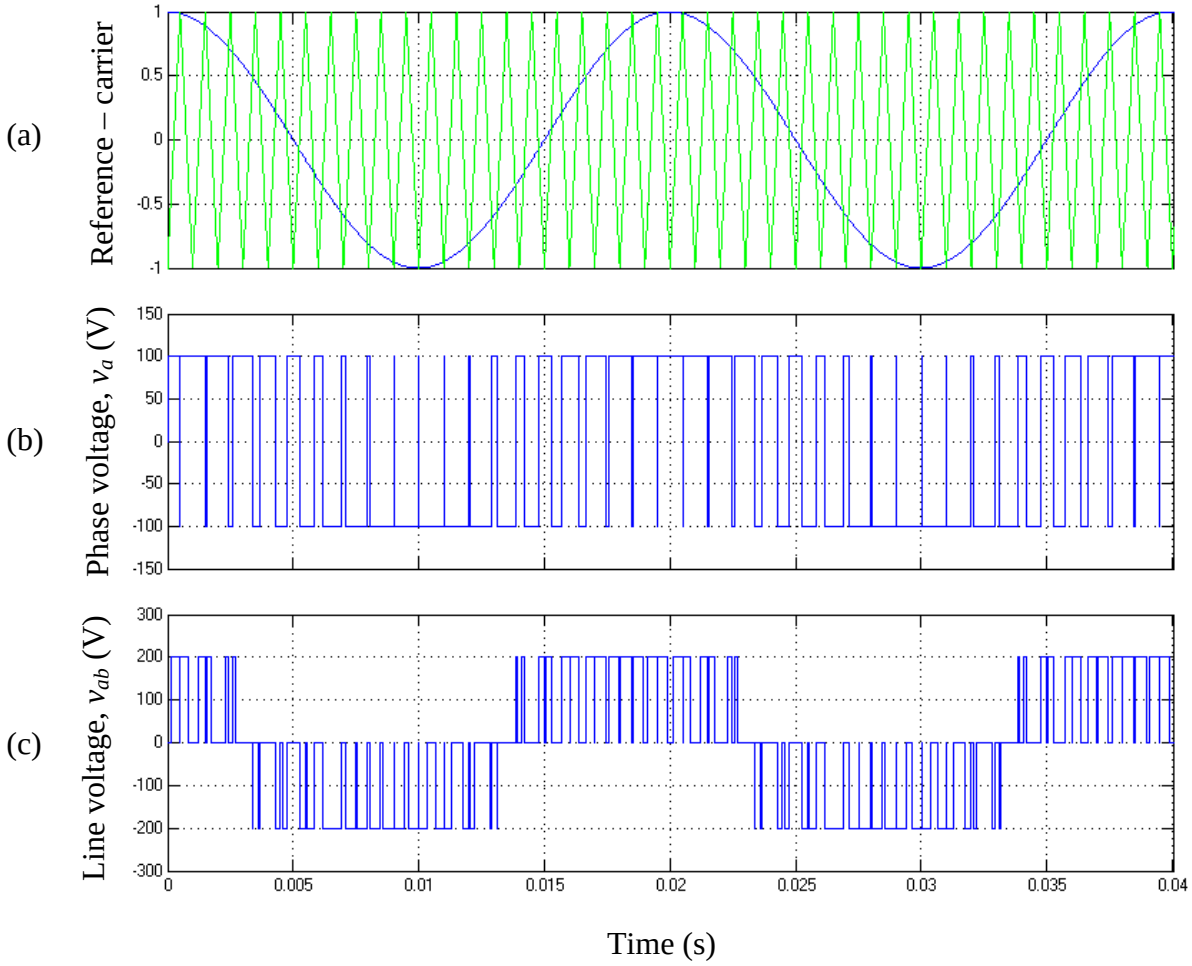


**Figure 2.7.** (a) Reference – carrier waveforms for phase *a*, (b) Phase voltage $v_a$, and (c) Line voltage $v_{ab}$ for a two-level converter, assuming $V_{dc}$ = 200 V, $f$ = 50 Hz, and $f_s$ = 1 kHz.

$$v_{a,ref} = M\cos(\theta)\ , \tag{2.1}$$

$$v_{b,ref} = M\cos\left(\theta - \frac{2\pi}{3}\right)\ , \tag{2.2}$$

$$v_{c,ref} = M\cos\left(\theta + \frac{2\pi}{3}\right)\ , \tag{2.3}$$

where $M$ is the converter modulation index and $\theta$ is the reference angle.

Figure 2.7 illustrates the carrier, reference and PWM voltage waveforms for phase *a*, for a 2L converter modulated using SPWM and unity modulation index. The reference waveforms in a 2L converter are compared with a single, common carrier waveform to determine the

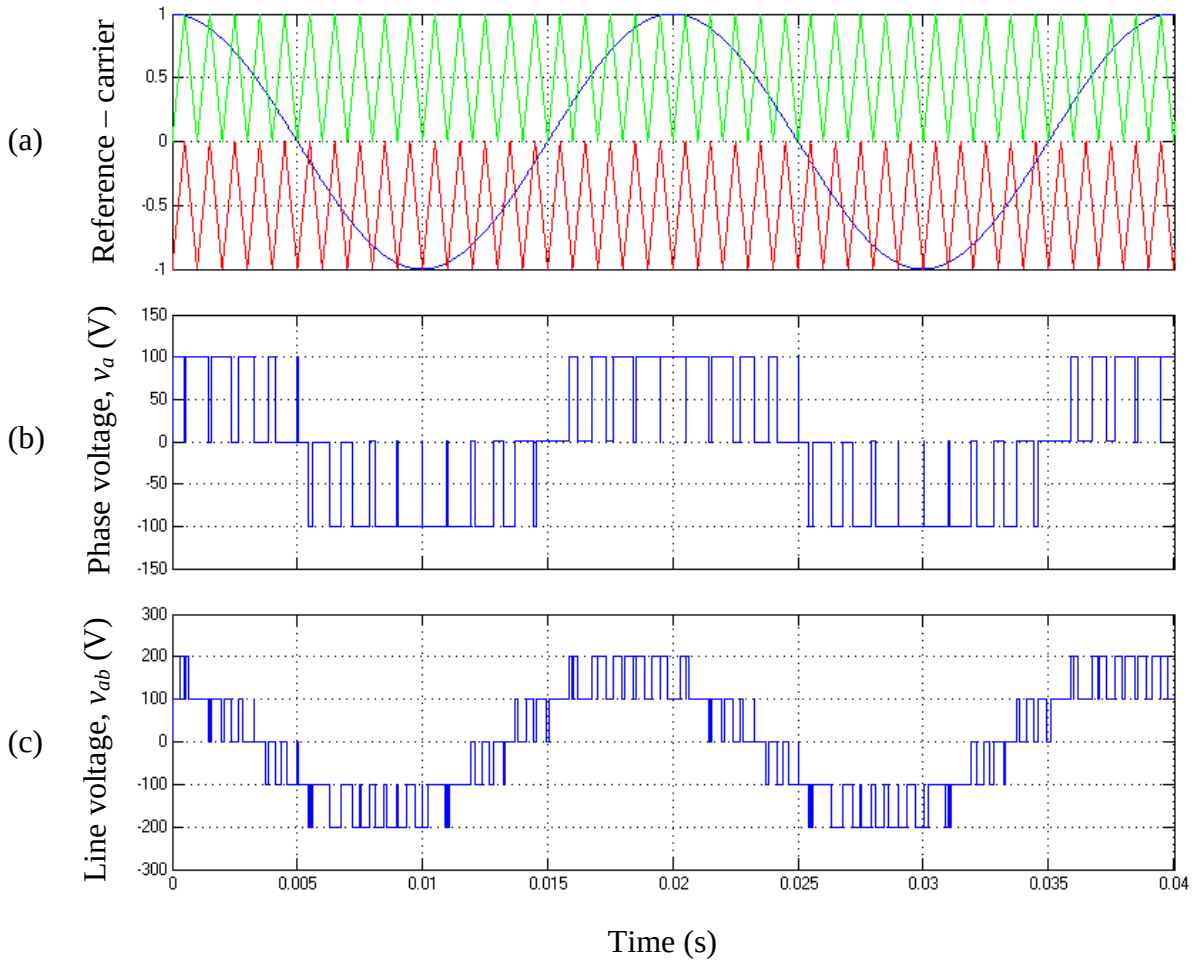


**Figure 2.8.** (a) Reference – carrier waveforms for phase *a*, (b) Phase voltage $v_a$, and (c) Line voltage $v_{ab}$ for a three-level converter, assuming $V_{dc}$ = 200 V, $f$ = 50 Hz, and $f_s$ = 1 kHz.

width of the generated pulses. The carrier waveform is commonly triangular. Its peak values are +1 and −1, and its frequency is equal to the switching frequency of the converter.

While the value of a reference is higher than that of the carrier waveform, the state, $s_x$, of the respective phase is set to 1, and the phase voltage becomes equal to $+V_{dc}/2$; otherwise, $s_x$ is set to 0 and the phase voltage becomes $-V_{dc}/2$. The resulting PWM waveform for phase $x$ has a duty cycle of

$$\delta_x = \frac{1}{2}\left(1 + v_{x,ref}\right) . \qquad \textbf{(2.4)}$$

It can be shown that over a period of the carrier, $T_s$, the area of this waveform, normalised w.r.t. $V_{dc}/2$, is the same as the area of $v_{x,ref}$. This ensures that the fundamental harmonic

component of the PWM waveform is the same as that of the reference waveform. Filtering of the higher-order harmonics turns the PWM into the desired sinusoidal voltage waveform.

The carrier-based SPWM strategy for 3L converters uses the three reference waveforms described by (2.1) – (2.3), and two carrier waveforms, arranged as shown in Figure 2.8. The carrier waveforms are in phase for the so called Phase Disposition (PD) PWM strategies, improving the PWM voltage harmonic spectra [13]. The state of each leg or cell of a 3L NPC or CHB converter, respectively, is determined as follows:

- If $v_{x,ref}$ is greater than the upper carrier, $s_x$ is set to 2.
- If $v_{x,ref}$ is between the upper and the lower carrier, $s_x$ is set to 1.
- If $v_{x,ref}$ is lower than the lower carrier, $s_x$ is set to 0.

Moreover, in the CHB converter, in order to balance the use of states 1a and 1b, the upper and lower carrier can be used to switch the first ($V_{1x}$ – $V_{2x}$) and second ($V_{3x}$ – $V_{4x}$) leg of each cell, respectively (similarly to a 2L converter).

The pulsed phase voltages in 3L converters vary between $+V_{dc}/2$ and 0 during the positive reference half cycle, and between 0 and $-V_{dc}/2$ during the negative one. The duty cycle of the voltage pulses for phase *x* is now given by

$$\delta_x = v_{x,ref} \ . \tag{2.5}$$

Again, it can be shown that the fundamental harmonic of a PWM phase voltage is the same as that of the respective reference. Furthermore, the generated three-level waveforms require less filtering as compared to those of the 2L inverter.

For both, 2L and 3L converters, the sinusoidal phase references of the SPWM strategy result in sinusoidal line voltages, which are supplied to the converter load. Sinusoidal line voltages, however, can also be generated by non-sinusoidal phase references if the latter are modified by a common-mode component, *cm*:

$$v_{a,ref} = M\cos(\theta) + cm \ , \tag{2.6}$$

$$v_{b,ref} = M\cos\left(\theta - \frac{2\pi}{3}\right) + cm \ , \tag{2.7}$$

$$v_{c,ref} = M\cos\left(\theta + \frac{2\pi}{3}\right) + cm \ . \tag{2.8}$$

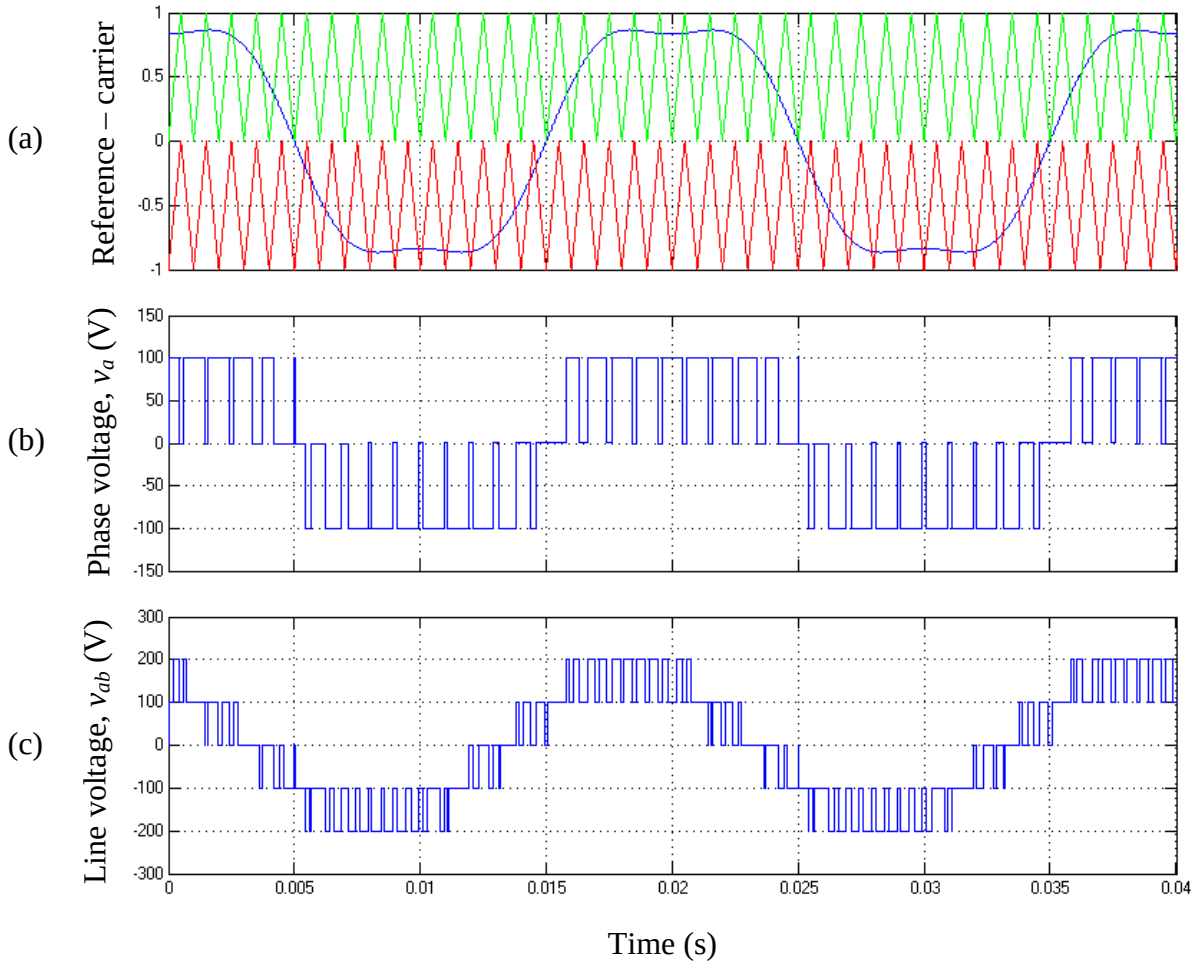


**Figure 2.9.** (a) Reference – carrier waveforms for phase *a*, (b) Phase voltage $v_a$, and (c) Line voltage $v_{ab}$ for a three-level converter modulated by SPWM+3rd harm., assuming $V_{dc}$ = 200 V, $f$ = 50 Hz, and $f_s$ = 1 kHz.

The line voltages are accordingly given by:

$$v_{ab,ref} = v_{a,ref} - v_{b,ref} = M\left[\cos(\theta) - \cos\left(\theta - \frac{2\pi}{3}\right)\right] = \sqrt{3}M\cos\left(\theta + \frac{\pi}{6}\right), \quad \textbf{(2.9)}$$

$$v_{bc,ref} = v_{b,ref} - v_{c,ref} = M\left[\cos\left(\theta - \frac{2\pi}{3}\right) - \cos\left(\theta + \frac{2\pi}{3}\right)\right] = \sqrt{3}M\cos\left(\theta - \frac{2\pi}{3} + \frac{\pi}{6}\right), \quad \textbf{(2.10)}$$

$$v_{ca,ref} = v_{c,ref} - v_{a,ref} = M\left[\cos\left(\theta + \frac{2\pi}{3}\right) - \cos(\theta)\right] = \sqrt{3}M\cos\left(\theta + \frac{2\pi}{3} + \frac{\pi}{6}\right). \quad \textbf{(2.11)}$$

It can be seen that the line voltages are not affected by the insertion of a common-mode voltage component. The amplitude of the line voltages, however, (which is equal to $\sqrt{3}M$) can be increased by using a common-mode voltage that allows an increase in the maximum value

of *M*. Namely, the maximum value of *M* for the case of SPWM is 1, since higher values lead to over-modulation and introduce low-frequency voltage distortion. An appropriate common-mode signal, on the other hand, can be added to the reference voltages to keep them in the range of ±1 while *M* increases beyond 1. It can be shown that the maximum value that *M* can take in this way is

$$M_{\max} = \frac{2}{\sqrt{3}} \approx 1.1547 \ , \qquad \textbf{(2.12)}$$

which leads to a respective maximum line voltage of $2V_{dc}$ peak-peak.

A typical common-mode waveform used for the above purpose is described by

$$cm_{3h} = -\frac{1}{6}\cos(3\theta) \ , \qquad \textbf{(2.13)}$$

corresponding to a method known as "third harmonic injection" (SPWM+3$^{rd}$ harm.). The waveform of $v_{a,ref}$ and the PWM voltages are shown in Figure 2.9 for this strategy, at unity modulation index. It can be seen from Figure 2.9(a) that the modulation index can now increase further, without leading to over-modulation of the converter.

### 2.2.2 SVM strategies

Space-Vector differ from carrier-based implementations of modulation strategies, since the former A) are based on numerical calculations instead of waveform intersections, and B) work directly with line voltages.

Starting with the 2L converter, the two states available for each leg lead to the functional diagram shown in Figure 2.10 for the entire three-phase converter.

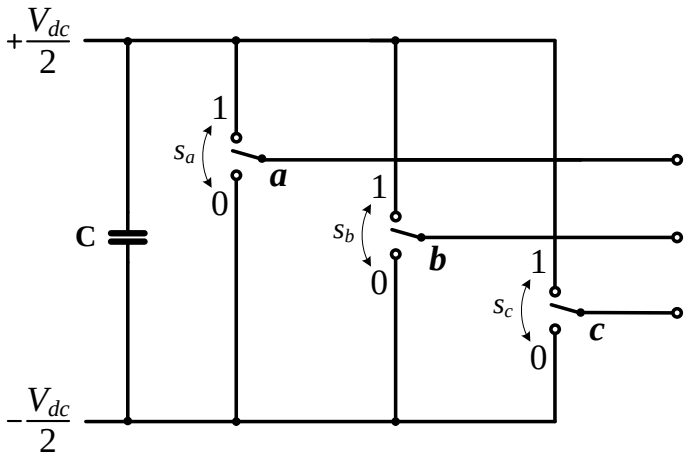


**Figure 2.10.** Functional diagram of the two-level converter.

The converter can therefore have $2^3 = 8$ switching states. Each converter state is represented by a Space Vector on the complex plane, given by the following transformation:

$$\mathbf{V} = \frac{2}{\sqrt{3}}\left( s_a + s_b e^{j\frac{2\pi}{3}} + s_c e^{-j\frac{2\pi}{3}} \right) . \qquad \textbf{(2.14)}$$

Table 2.2 lists the Space Vectors corresponding to the different states and relates them to the converter line voltages, while Figure 2.11 illustrates the Space Vectors on the complex plane.

| State ($s_a s_b s_c$) | Space Vector | Line voltages ($v_{ab}$, $v_{bc}$, $v_{ca}$) |
|---|---|---|
| 000 | 0 | 0, 0, 0 |
| 100 | $2/\sqrt{3}\cdot e^{j0}$ | $V_{dc}$, 0, $-V_{dc}$ |
| 110 | $2/\sqrt{3}\cdot e^{j\pi/3}$ | 0, $V_{dc}$, $-V_{dc}$ |
| 010 | $2/\sqrt{3}\cdot e^{j2\pi/3}$ | $-V_{dc}$, $V_{dc}$, 0 |
| 011 | $2/\sqrt{3}\cdot e^{j\pi}$ | $-V_{dc}$, 0, $V_{dc}$ |
| 001 | $2/\sqrt{3}\cdot e^{j4\pi/3}$ | 0, $-V_{dc}$, $V_{dc}$ |
| 101 | $2/\sqrt{3}\cdot e^{j5\pi/3}$ | $V_{dc}$, $-V_{dc}$, 0 |
| 111 | 0 | 0, 0, 0 |

**Table 2.2.** Space Vectors and line voltages for the two-level converter states.

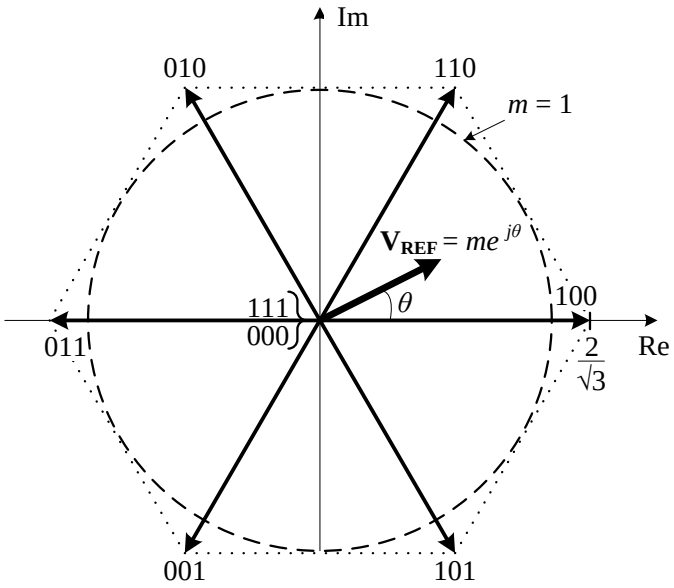


**Figure 2.11.** Space Vector diagram for the two-level converter.

Pulse Width Modulation in SVM strategies is realised by activating a number of Space Vectors, $\mathbf{V_1}$, $\mathbf{V_2}$, … , $\mathbf{V_n}$, according to respective duty cycles $d_1$, $d_2$, … , $d_n$, to create a voltage reference vector, $\mathbf{V_{REF}}$:

$$\mathbf{V_{REF}} = d_1\mathbf{V_1} + d_2\mathbf{V_2} + ... + d_n\mathbf{V_n} \ ,$$

$$\text{with} \quad d_1 + d_2 + ... + d_n = 1 \ . \qquad \textbf{(2.15)}$$

The reference vector represents the three converter line voltages on the SV plane and is defined as follows:

$$\mathbf{V_{REF}} = \frac{1}{\sqrt{3}}\left( v_{a,ref} + v_{b,ref}e^{j\frac{2\pi}{3}} + v_{c,ref}e^{-j\frac{2\pi}{3}} \right) . \qquad \textbf{(2.16)}$$

Assuming that the voltage references are given by equations (2.6) – (2.8), $\mathbf{V_{REF}}$ can be shown to be equal to

$$\mathbf{V_{REF}} = \frac{\sqrt{3}}{2} M \cdot e^{j\theta} = m \cdot e^{j\theta} , \qquad \textbf{(2.17)}$$

where $m$ will be the symbol for the modulation index for SVM strategies. As shown in Figure 2.11, $m$ is equal to 1 at the limit of the linear (not over-) modulation region, and relates to $M$ as determined by

$$m = \frac{\sqrt{3}}{2} M \ . \tag{2.18}$$

SVM strategies can operate with $m = 1$, or equivalently $M = M_{\max}$ (see 2.12), generating the maximum possible amplitude of line voltage.

Figure 2.12 illustrates the functional diagram of a 3L NPC converter. This converter can be found at $3^3 = 27$ switching states. The respective Space Vectors are now derived by

$$\mathbf{V} = \frac{1}{\sqrt{3}} \left( s_a + s_b e^{j\frac{2\pi}{3}} + s_c e^{-j\frac{2\pi}{3}} \right) , \tag{2.19}$$

and are shown in Figure 2.13. The SV diagram is the same for the 3L CHB converter. It can be noticed that there are pairs of small vectors (e.g. 100-211) and a triplet of zero vectors (000-111-222) that share the same position on the SV plane. The same is true for the two zero vectors at the middle of the SV diagram for the 2L converter (Figure 2.11). This property of the SV diagrams is essential for creating different SV modulation strategies, since vectors with the same position on the SV plane can be used alternatively to create the reference vector according to (2.15). The vector selection, on the other hand, determines the common-mode voltage of the converter, correlating SVM to carrier-based strategies, as described in [18, 19, 40, 41].

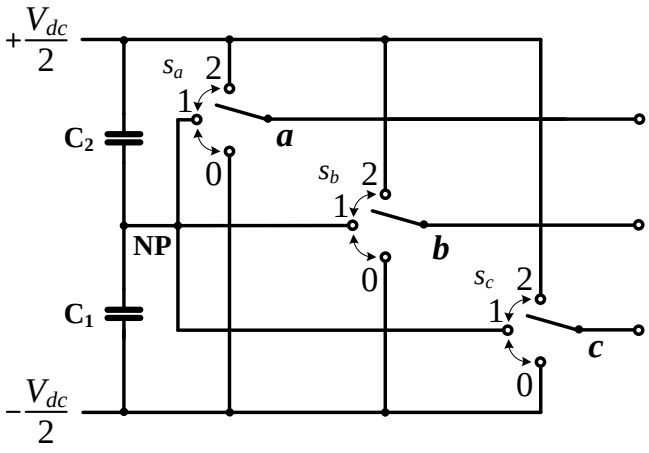


**Figure 2.12.** Functional diagram of the NPC converter.

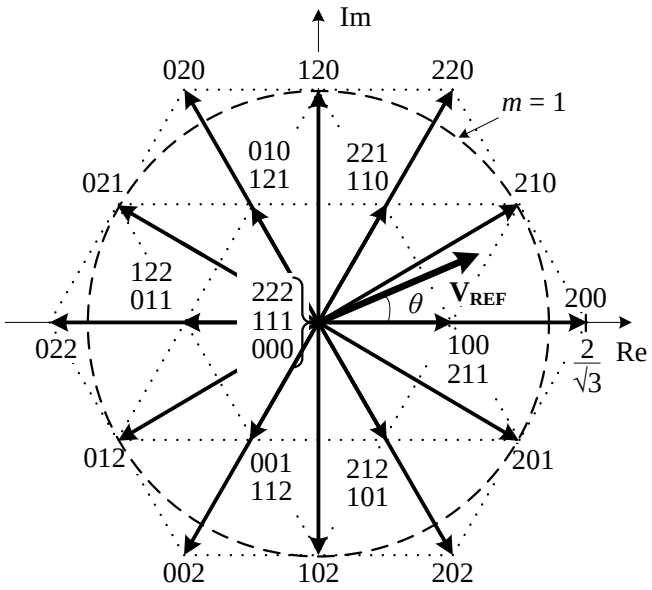


**Figure 2.13.** Space Vector diagram for three-level converters.

## 2.3 Modelling

The results of this Thesis were validated by simulations in MATLAB-Simulink. Extensive use of components from Simulink's SimPowerSystems toolbox was made to create models of converters, adjust the operating and load parameters, and acquire measurements. Modulation strategies, on the other hand, were mainly implemented (coded) as Embedded MATLAB functions.

Figures 2.14 – 2.16 illustrate simple models of the 2L, and 3L NPC and CHB converters, used for measuring dc-link capacitor voltages and currents (analysed in Chapter 3). In the models,

- the converters and their (carrier-based) modulation functions, which provide the gating signals to the converter modules are shown in light blue
- manual controls for adjusting the converter modulation index and switching between SPWM and SPWM+3$^{rd}$ harm. are shown in red, and
- the converter load and measurements associated with it are shown in orange.

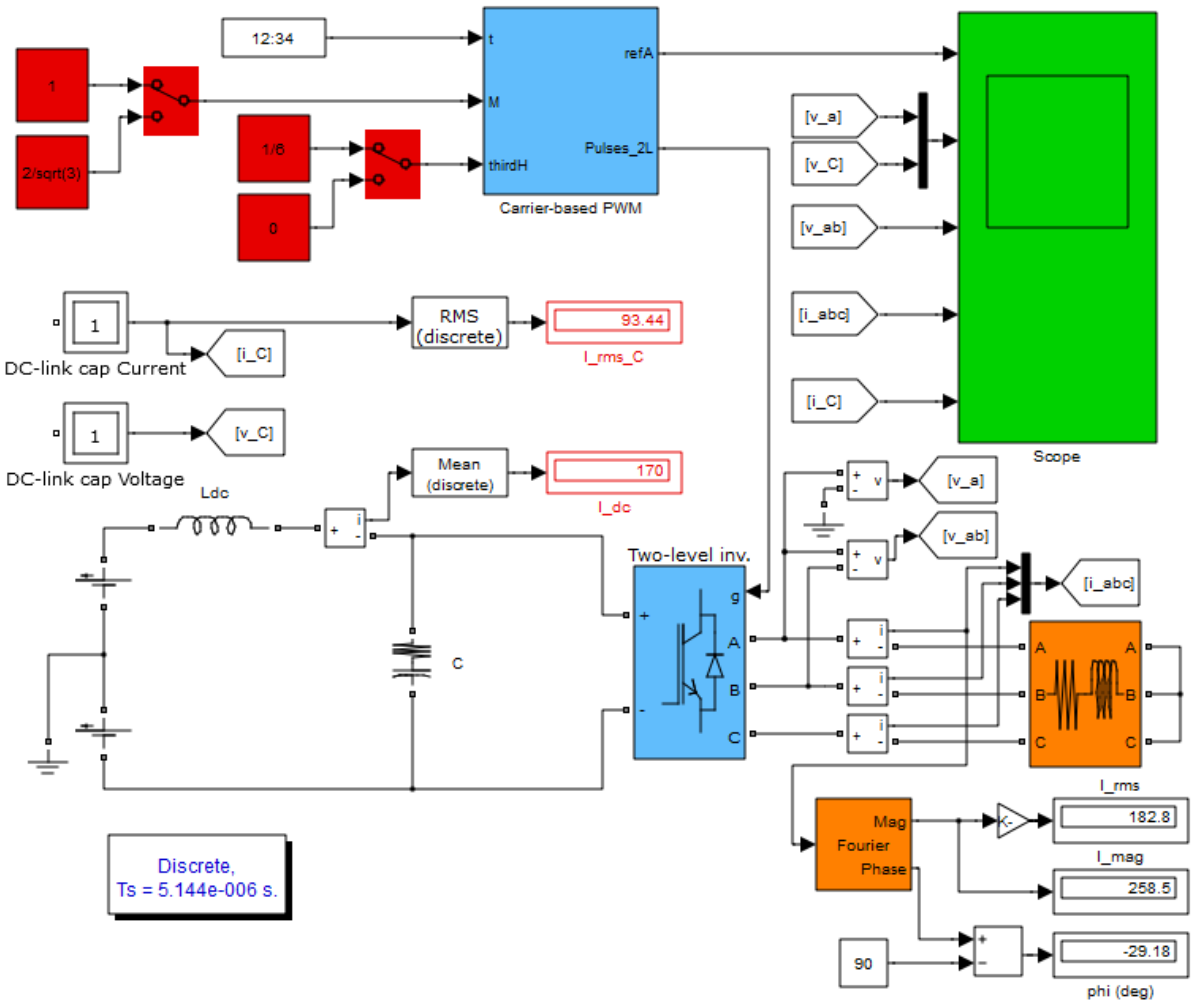


**Figure 2.14.** Simulink model for the two-level converter.

A number of different Simulink models were built to examine the subjects covered in the following chapters. The results section in each chapter provides a description of the simulated system, accompanied by the parameter values (dc-link voltage, modulation index, fundamental frequency, load power factor, etc.) used in each case. Moreover, additional Simulink models and MATLAB code are included in Appendix A.4 to cover more elaborate procedures, such as the modulation algorithm presented in Chapter 6.

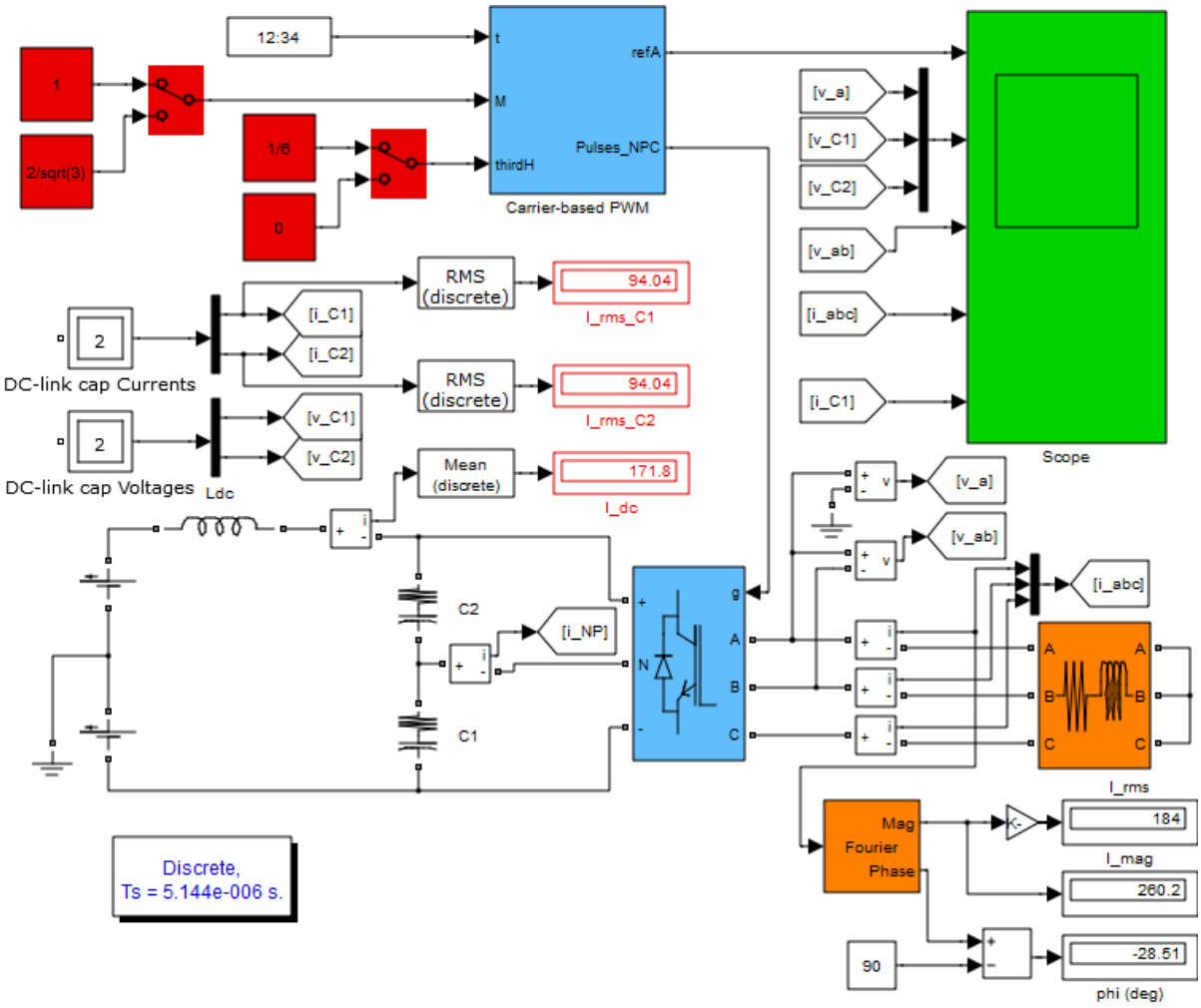


**Figure 2.15.** Simulink model for the NPC converter.

Below are given a number of general notes on the simulations:

- This study focuses on the effect of the converter (not the FE) on the dc-link capacitor current. The FE is therefore simulated as a dc voltage source, in series with a dc-link inductor (choke), sized to carry a negligible amount of ac current as compared to the dc-link capacitor. The dc source then provides the dc component of the dc-link converter current, while the capacitor carries its ac component.
- The 2L and NPC converters are built using the models available in the SimPowerSystems toolbox of Simulink. CHB converters are built using three H-bridges, also available in Simulink. The selected switching modules are IGBTs with an on-state resistance of 0.1 mΩ.

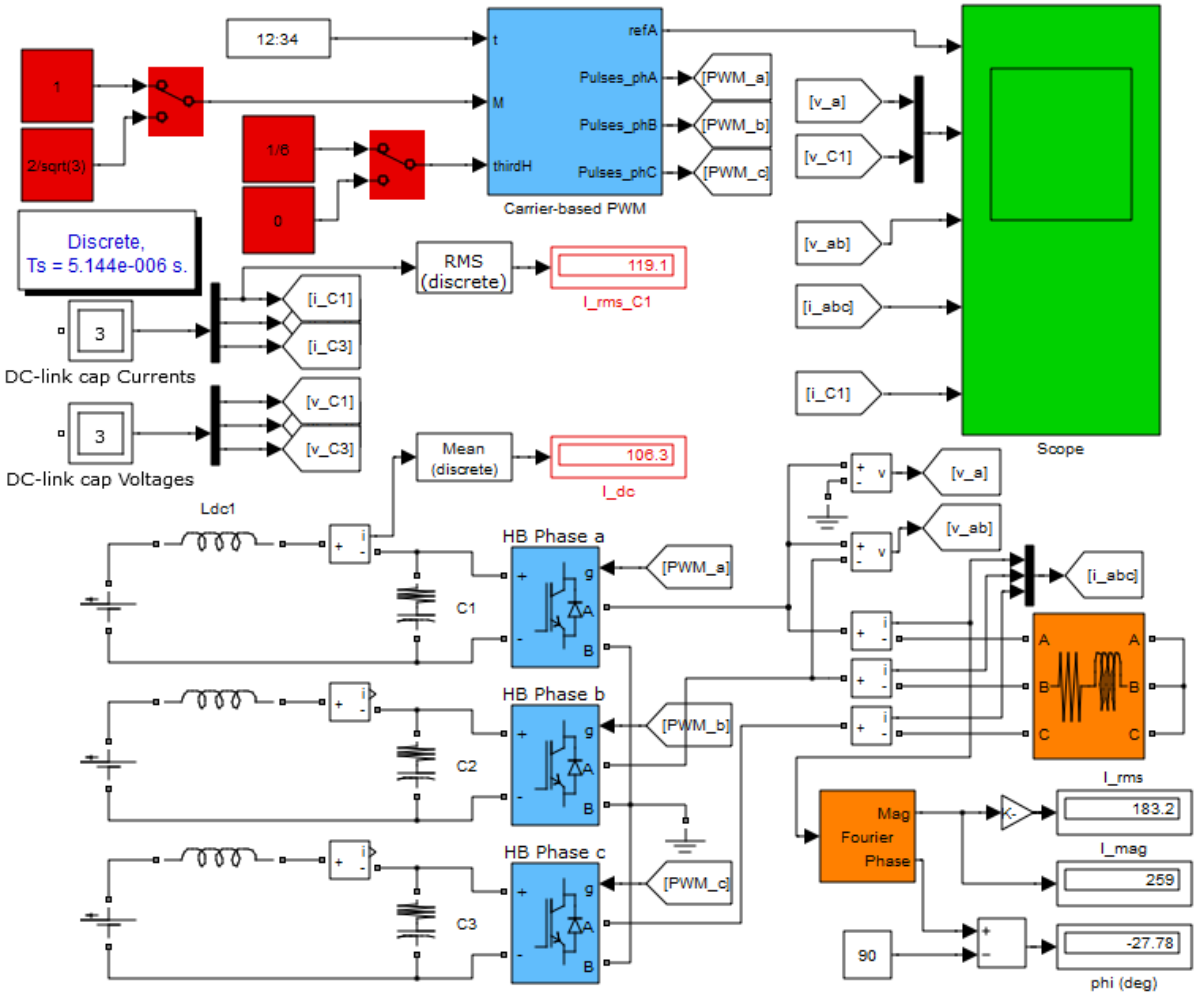


**Figure 2.16.** Simulink model for the CHB converter.

- The converters supply static RL loads. The values of R and L are selected in each case (in accordance with the converter operating parameters) to achieve the desired load power factor and current amplitude.
- Measurements are taken using Simulink's voltage, current, and multimeter blocks. Discrete mean, rms, and THD blocks are also used for calculations. Voltage/current Spectra are taken from the FFT analysis tool, found in Simulink's PowerGUI block.
- All simulations are run in discrete time, with a time step of 5.144e−7 s.

# Chapter 3

## Analysis of dc-link capacitor current in three-level Neutral-Point-Clamped and Cascaded H-Bridge inverters

## 3.1 Introduction

During the last decades, the presence of multilevel inverters has been steadily increasing in a variety of applications in the manufacturing, transport, energy, mining, and other industries [4, 5]. An essential part of multilevel inverter design is the selection of dc-link capacitors. The capacitors are a sensitive element of the inverter and a common source of failures. Capacitor lifetime is highly affected by thermal as well as overvoltage stresses, both of which can be estimated based on an analysis of the capacitor current [25, 42].

Thermal stress occurs due to losses in the dc-link capacitor's Equivalent Series Resistance (ESR). The rms value of the current flowing through a dc-link capacitor can provide a first approximation for these losses. The literature contains rms expressions for the capacitor current of the 2L [43, 44, 45] and (single-phase) 3L CHB inverters [46]. Use of these expressions for loss estimation assumes a fixed ESR value. However, the ESR is a function of the frequency of the capacitor current [25, 42]. Since the current of a dc-link capacitor comprises several harmonics located at different frequencies, it is necessary to determine the rms values of the capacitor current harmonics and use the appropriate value of ESR for each harmonic. For the 2L inverter, dc-link current harmonics have been derived in [47], while a general analytical method for calculating dc-link current harmonics in inverters has been proposed in [48].

Overvoltage stress may occur due to low-frequency capacitor voltage oscillations (ripple). In the 2L inverter, such oscillations do not appear under balanced load conditions. This is not the case, though, in 3L inverters. A plot of the amplitude of the capacitor voltage ripple in the 3L Neutral Point Clamped (NPC) inverter [49] can be found in [50], for the case of SPWM. Moreover, capacitor-balancing techniques for the NPC inverter, which achieve smaller ripple amplitudes, are described in [40, 51, 52]. Regarding the CHB inverter topology, estimates for the capacitor voltage ripple can be found in [53], again for the case of SPWM.

This chapter presents a systematic analysis of the dc-link capacitor current in 3L NPC and CHB inverters, which provides the basis for dc-link capacitor sizing in these topologies. Methods for analyzing the 2L inverter dc-link capacitor current are extended to 3L inverters, to estimate the capacitor rms current and derive its harmonic spectrum. A new, numerical approach for calculating the rms value and low-frequency harmonics of the capacitor current

is also proposed. Unlike existing methods, the proposed approach has the advantage of being easily adaptable to different modulation strategies. Results based on this approach are presented for a number of common modulation strategies.

The chapter is structured as follows: Section 3.2 gives a description of the parameters considered during dc-link capacitor sizing, explaining their relation to the capacitor current. Section 3.3 derives expressions for the rms value of the dc-link capacitor current in 3L NPC and CHB topologies [54], while Section 3.4 presents a harmonic analysis of this current [55]. Section 3.5 describes the proposed numerical method for deriving the current rms value and the amplitude of voltage ripple for the dc-link capacitors of the two topologies. Then, Section 3.6 validates the results of the previous sections using simulations in MATLAB-Simulink. Finally, Section 3.7 compares the examined 3L topologies with respect to their capacitor requirements, and discusses the accuracy and applicability of the presented methods, with a focus on the proposed approach.

## 3.2 Inverter dc-link capacitor sizing

The selection of inverter dc-link capacitors is determined by the required voltage, (ripple) current, and capacitance ratings, as explained below:

- The capacitor voltage rating is typically higher than the operating dc-link voltage, to account for voltage oscillations and other effects such as input (grid) voltage fluctuations or transitory regenerative operation of the inverter.

- The ripple (rms) current rating, $I_{C,\max}$, is a way of expressing the affordable limit for capacitor losses, $P_{C,\max}$. $I_{C,\max}$ is commonly given in capacitor datasheets [25, 42], for a certain value of ESR, $R_C$, as

$$P_{C,\max} = R_C \cdot I_{C,\max}^2 \ . \qquad \textbf{(3.1)}$$

According to the above, a calculation of the dc-link capacitor rms current in a certain inverter application can give a first estimate for the required ripple current rating. Nevertheless, for electrolytic capacitors, the value of the ESR varies with the frequency of the capacitor current. A typical ESR – frequency characteristic is illustrated in Figure 3.1 [42].

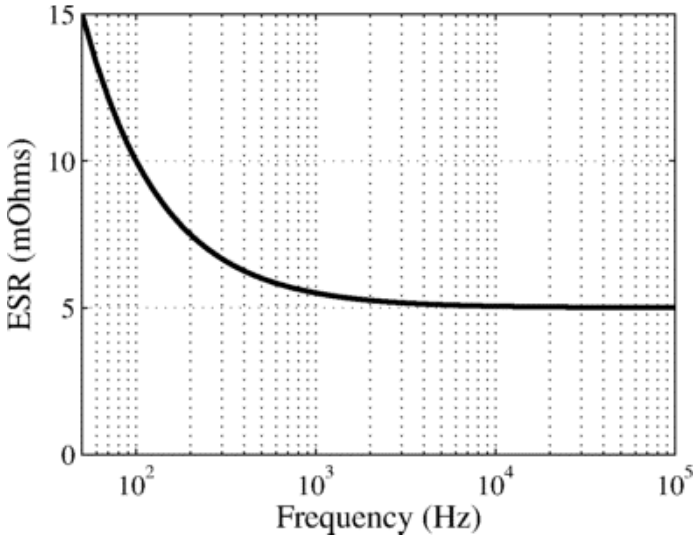


**Figure 3.1.** ESR – frequency characteristic of a 4.7 mF / 450 V capacitor (reproduced from **[42]**).

Hence, in case that more than one current harmonics, $h$, with amplitudes $I_h$ (rms values $I_{h,rms}$) and frequencies $f_h$ flow through the capacitor, the occurring losses should be calculated using

$$P_C = \sum_h R_C(f_h) \cdot I_{h,rms}^2 \,, \tag{3.2}$$

where $R_C(f_h)$ stands for the value of ESR at frequency $f_h$. Then, the capacitor's ripple current rating can be selected so that $P_C$ does not exceed $P_{C,\max}$.

- The required capacitance is determined by the affordable amplitude of dc-link voltage oscillations ($\Delta V_{C,\max}/2$), which is also dependent on the capacitor current harmonics. Assuming that, in the worst case, all these harmonics (or equivalently all peaks of voltage harmonics) are in phase, the required capacitance is given by

$$C \geq \frac{1}{\Delta V_{C,\max}/2} \cdot \sum_h \frac{I_h}{2\pi f_h} \quad . \tag{3.3}$$

According to this equation, high-frequency (HF) capacitor current harmonics, which appear due to the switching (PWM) operation of the inverter, have a small effect on the capacitor voltage ripple. Low-frequency (LF) harmonics, on the other hand, located at multiples of the inverter fundamental frequency, can increase the required capacitance, since they give rise to LF capacitor voltage oscillations. It is noted that increased capacitance can also be required for other purposes, such as for voltage support during a temporary loss of the input power source.

## 3.3 Analytical derivation of dc-link capacitor current rms expressions

In this section, the method used in [43] for the derivation of the 2L inverter (Figure 3.2) capacitor current rms expression is summarized and extended to the 3L NPC and CHB topologies. The method considers each inverter IGBT-diode module as a switch that, while on, carries the current of the respective phase. If the sum of the currents through the upper switches of an inverter is $i_d$, then the dc component of $i_d$ is (assumed to be) supplied by the inverter dc source while the ac component is filtered, that is, carried by the dc-link capacitor. The rms value of the capacitor current, $I_{C,rms}$, is calculated using the average (dc) and rms values of $i_d$, $I_{d,dc}$ and $I_{d,rms}$, respectively as

$$I_{C,rms} = \sqrt{I_{d,rms}^2 - I_{d,dc}^2} \ . \tag{3.4}$$

The calculation of the average and rms values for current $i_d$ is based on the analysis of its transitions within a single switching period. If $i_d$ is equal to $i_{d,\text{int}1}$, $i_{d,\text{int}2}$, ... , $i_{d,\text{int}k}$, during time intervals $T_{\text{int}1}$, $T_{\text{int}2}$, ... , $T_{\text{int}k}$, respectively, then its average and rms value during a switching period, $T_s$, centered at reference angle $\theta$, are given by

$$i_{d,dc}(\theta) = \frac{1}{T_s}\left(\sum_k T_{\text{int}k} \cdot i_{d,\text{int}k}\right) = \sum_k \delta_{\text{int}k} \cdot i_{d,\text{int}k} \ . \tag{3.5}$$

$$i_{d,rms}^2(\theta) = \frac{1}{T_s}\left(\sum_k T_{\text{int}k} \cdot i_{d,\text{int}k}^2\right) = \sum_k \delta_{\text{int}k} \cdot i_{d,\text{int}k}^2 \ . \tag{3.6}$$

The interval duty cycles $\delta_{\text{int}k}$ and respective currents $i_{d,\text{int}k}$ are also functions of $\theta$. The average and rms values of $i_d$ over a fundamental period are obtained using the following expressions:

$$I_{d,dc} = \frac{1}{2\pi}\int_0^{2\pi} i_{d,dc}(\theta)\, d\theta \ . \tag{3.7}$$

$$I_{d,rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{d,rms}^2(\theta)\, d\theta} \ . \tag{3.8}$$

In case that the expressions for $i_{d,dc}(\theta)$ and $i_{d,rms}(\theta)$ change during parts (sectors) of the fundamental cycle, the above expressions are written as sums of integrals for the different sectors.

### 3.3.1 Two-level inverter

Assuming SPWM, the phase reference voltages, $v_{x,ref}$, shown in Figure 3.3, and the respective duty cycles, $\delta_x$, are given by (3.9) and (3.10) below,

$$v_{x,ref} = M\cos\left(\theta + \theta_x\right), \tag{3.9}$$

$$\delta_x = \frac{1}{2}\left(1 + v_{x,ref}\right), \tag{3.10}$$

where $M$ is the inverter modulation index, while $\theta_x$ for phases $a$, $b$ and $c$ is equal to $\theta_\alpha$, $\theta_b$ and $\theta_c$, respectively:

$$\theta_a = 0, \theta_b = \frac{2\pi}{3}, \theta_c = -\frac{2\pi}{3}\ . \tag{3.11}$$

Moreover, the sinusoidal phase currents $i_x$ are assumed to be given by

$$i_x = I_{pk}\cos\left(\theta + \theta_x - \phi\right), \tag{3.12}$$

where $I_{pk}$ is the current peak value (magnitude) and $\phi$ is the power angle of the inverter load.

For the 2L inverter, current $i_d$ is shown in Figure 3.2. The dc component of $i_d$ is $I_{d,dc}$, while its ac component is the current of the dc-link capacitor. For the derivation of the dc-link capacitor current rms expression in [43], the fundamental cycle is divided into six sectors (Sector I, II, … , VI), each of which covers an angle of π/3. It is shown that the inverter operation in these sectors is symmetric w.r.t. dc-link capacitor rms current.

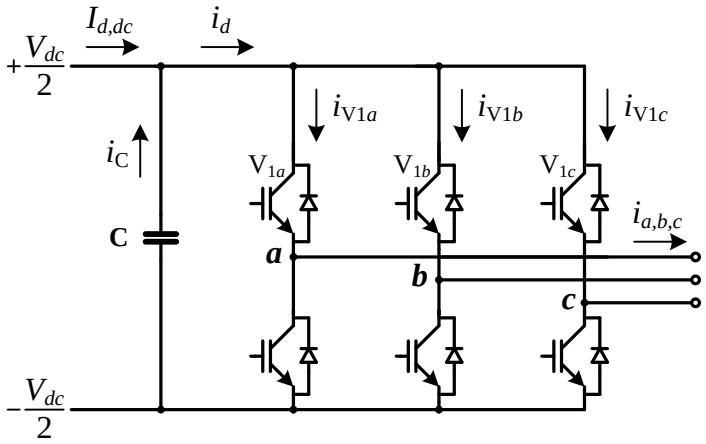


**Figure 3.2.** Two-level inverter topology, illustrating upper module currents and current $i_d$.

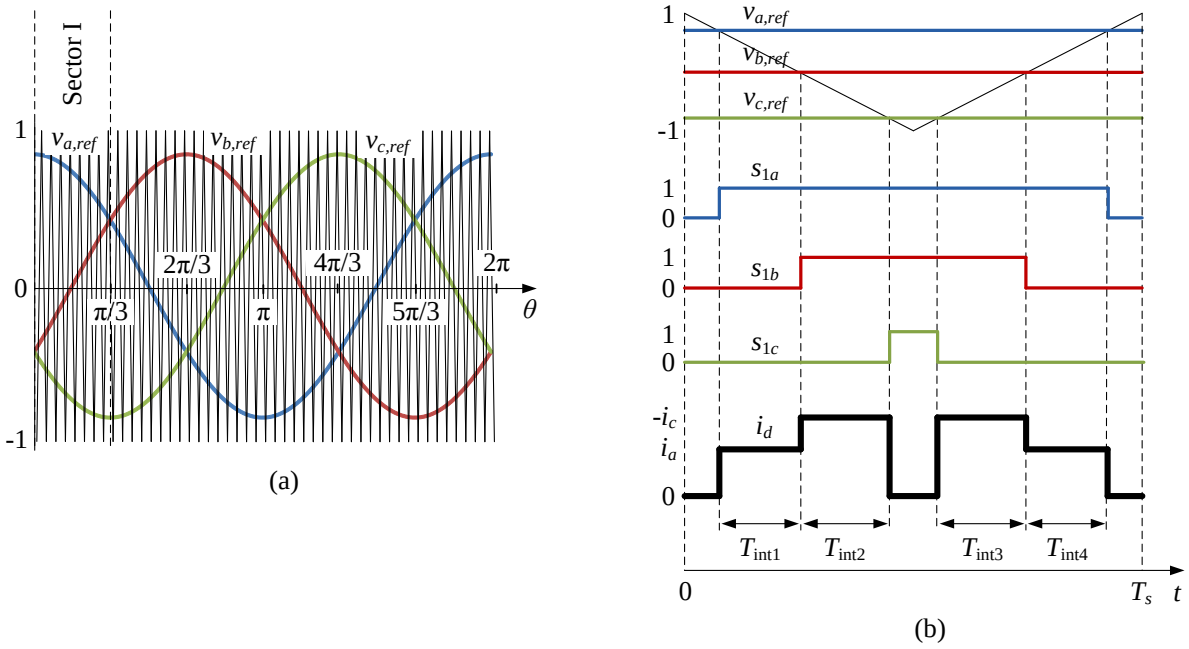


**Figure 3.3.** (a) Reference and carrier waveforms for the two-level inverter, and (b) analysis of a switching cycle for Sector I of the two-level inverter.

Table 3.1 illustrates the duty cycles of the switching intervals and the corresponding values of current $i_d$ for Sector I (0 – π/3).

| Tot. duration | Tot. duty cycle | Current $i_d$ |
|---|---|---|
| $T_{int1} + T_{int4}$ | $\delta_a - \delta_b$ | $i_a$ |
| $T_{int2} + T_{int3}$ | $\delta_b - \delta_c$ | $-i_c$ |

**Table 3.1.** Switching intervals for Sector I (0 – π/3) of the two-level inverter.

According to the table, (3.5) and (3.6) take the following form for Sector I:

$$i_{d,dc-2L}(\theta) = (\delta_a - \delta_b) i_a + (\delta_b - \delta_c)(-i_c) \quad , \tag{3.13}$$

$$i^2_{d,rms-2L}(\theta) = (\delta_a - \delta_b) i_a^2 + (\delta_b - \delta_c)(-i_c)^2 \quad . \tag{3.14}$$

It is reminded that $i_{d,dc\text{-}2L}$ in (3.13) and $i_{d,rms\text{-}2L}$ in (3.14) represent the dc and rms values, respectively, of $i_d$ (the black waveform in Figure 3.3(b)), as shown in [43]. Then, the values of $I_{d,dc}$ and $I_{d,rms}$ for the 2L inverter are given by (3.7) and (3.8) as

$$I_{d,dc-2L} = \frac{3}{\pi}\int_0^{\pi/3} i_{d,dc-2L}(\theta)d\theta = \frac{3}{4}MI_{pk}\cos\phi \ , \tag{3.15}$$

$$I_{d,rms-2L} = \sqrt{\frac{3}{\pi}\int_0^{\pi/3} i_{d,rms-2L}^2(\theta)d\theta} = I_{pk}\sqrt{\frac{\sqrt{3}M}{\pi}\left(\cos^2\phi + \frac{1}{4}\right)} \ , \tag{3.16}$$

and are used to derive the expression for the rms value of the capacitor current according to (3.4) as

$$I_{C,rms-2L} = \frac{I_{pk}}{\sqrt{2}}\sqrt{M\left[\frac{\sqrt{3}}{2\pi} + \left(\frac{2\sqrt{3}}{\pi} - \frac{9}{8}M\right)\cos^2\phi\right]} \ . \tag{3.17}$$

As explained in [43], the above expression is valid for any modulation strategy for the 2L inverter. The reason is that any common-mode signal which may be added to the three phase voltage references ($v_{x,ref}$) cancels in the calculation of ($\delta_a - \delta_b$) and ($\delta_b - \delta_c$) in Table 3.1.

### 3.3.2 NPC inverter

For the 3L NPC inverter, current $i_d$ is shown in Figure 3.4. The ac component of $i_d$ is the current of the upper capacitor of the dc-link ($C_2$). The upper modules are modulated by the upper carrier waveform, as shown in Figure 3.5. It can be shown that the waveform of $i_d$ has a period of $T/3$, where $T$ is the period of a reference waveform. Hence, for the derivation of $I_{d,dc}$ and $I_{d,rms}$, an angle interval of $2\pi/3$ needs to be analysed. The selected interval covers the values of $\theta$ between $\pi/6$ and $5\pi/6$ and can be divided into three Sectors (I, II, and III), as shown in Figure 3.5. The duty cycles of the switching intervals ($\delta_{\text{int}k}$) and the respective $i_d$ currents ($i_{d,\text{int}k}$) change between Sectors I and II, as shown in Figure 3.6, below. In the figure, $s_{1x}$ represents the state of module $V_{1x}$ (0 for OFF and 1 for ON). Tables 3.2 and 3.3 present the expressions of the above duty cycles in a concise form that can be used according to (3.7) and (3.8) to derive the dc and rms values of $i_d$ for each sector. The resulting expressions are shown in Table 3.4 (Sector III can be analysed similarly to Sector I).

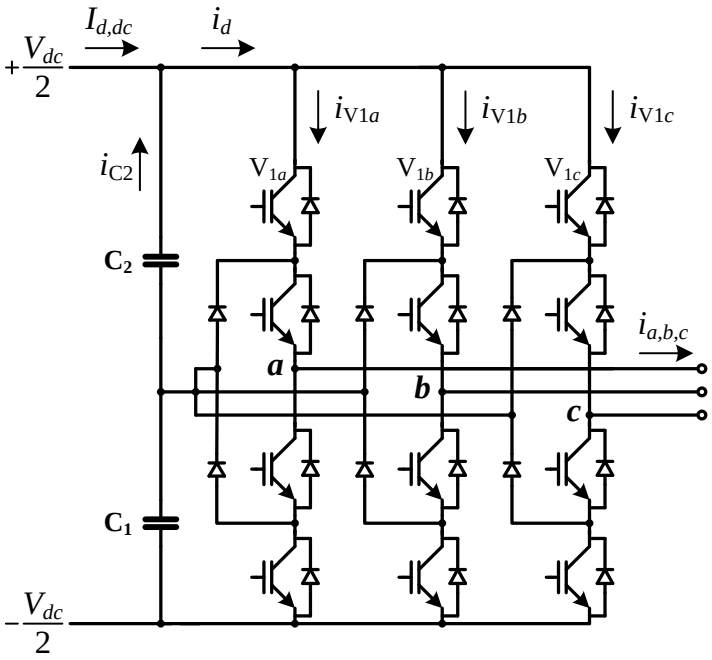


**Figure 3.4.** Three-phase NPC inverter, illustrating upper module currents and current $i_d$.

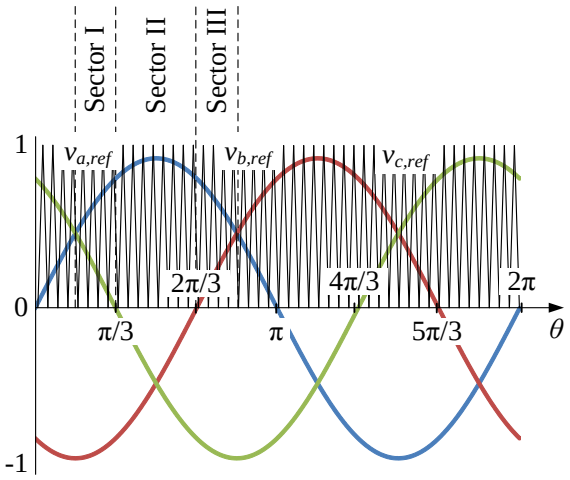


**Figure 3.5.** Reference and upper carrier waveforms for the NPC inverter.

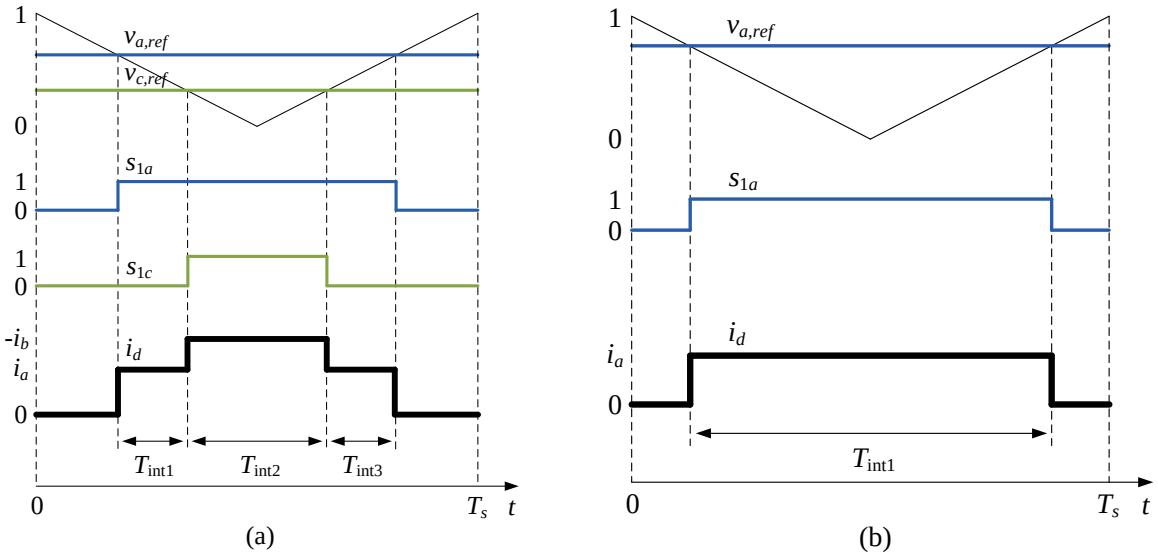


**Figure 3.6.** Analysis of a switching cycle for (a) Sector I, and (b) Sector II, of the NPC inverter.

| Tot. duration | Tot. duty cycle | Current $i_d$ |
|---|---|---|
| $T_{int1} + T_{int3}$ | $\delta_a - \delta_c$ | $i_a$ |
| $T_{int2}$ | $\delta_c$ | $-i_b$ |

**Table 3.2.** Switching intervals for Sector I of the NPC inverter.

| Tot. duration | Tot. duty cycle | Current $i_d$ |
|---|---|---|
| $T_{int1}$ | $\delta_a$ | $i_a$ |

**Table 3.3.** Switching intervals for Sector II of the NPC inverter.

| Sector I | Sector II | Sector III |
|---|---|---|
| $i_{d,dc,I-NPC}(\theta) = (\delta_a - \delta_c) i_a + \delta_c (-i_b)$ | $i_{d,dc,II-NPC}(\theta) = \delta_a i_a$ | $i_{d,dc,III-NPC}(\theta) = (\delta_a - \delta_b) i_a + \delta_b (-i_c)$ |
| $i^2_{d,rms,I-NPC}(\theta) = (\delta_a - \delta_c) i_a^2 + \delta_c (-i_b)^2$ | $i^2_{d,rms,II-NPC}(\theta) = \delta_a i_a^2$ | $i^2_{d,rms,III-NPC}(\theta) = (\delta_a - \delta_b) i_a^2 + \delta_b (-i_c)^2$ |

**Table 3.4.** Expressions for $i_{d,dc}(\theta)$ and $i_{d,rms}(\theta)$ for the three sectors of the NPC inverter.

Since the expressions for $i_{d,dc}(\theta)$ and $i_{d,rms}(\theta)$ change during sectors of the fundamental cycle, expressions (3.7) and (3.8) take the form of (3.18) and (3.19), respectively,

$$I_{d,dc-NPC} = \frac{3}{2\pi}\left( \int_{\pi/6}^{\pi/3} i_{d,dc,I-NPC}(\theta)\, d\theta + \int_{\pi/3}^{2\pi/3} i_{d,dc,II-NPC}(\theta)\, d\theta + \int_{2\pi/3}^{5\pi/6} i_{d,dc,III-NPC}(\theta)\, d\theta \right), \qquad \textbf{(3.18)}$$

$$I_{d,rms-NPC} = \sqrt{\frac{3}{2\pi}\left( \int_{\pi/6}^{\pi/3} i_{d,rms,I-NPC}^2(\theta)\,d\theta + \int_{\pi/3}^{2\pi/3} i_{d,rms,II-NPC}^2(\theta)\,d\theta + \int_{2\pi/3}^{5\pi/6} i_{d,rms,III-NPC}^2(\theta)\,d\theta \right)}. \quad \textbf{(3.19)}$$

For 3L inverters, the phase duty cycles are given by

$$\delta_x = v_{x,ref} = M\sin(\theta + \theta_x)\ , \quad \textbf{(3.20)}$$

thus (3.18) and (3.19) result in

$$I_{d,dc-NPC} = \frac{3}{4} M I_{pk} \cos\varphi\ , \quad \textbf{(3.21)}$$

$$I_{d,rms-NPC} = I_{pk}\sqrt{\frac{\sqrt{3}M}{4\pi}\left(\cos^2\varphi + \frac{1}{4}\right)}\ . \quad \textbf{(3.22)}$$

Finally, the rms current expression for the upper capacitor ($C_2$) of the 3L NPC inverter is derived according to (3.4), and is shown below:

$$I_{C,rms-NPC} = I_{pk}\sqrt{\frac{M}{2}\left[\frac{\sqrt{3}}{2\pi} + \left(\frac{2\sqrt{3}}{\pi} - \frac{9}{8}M\right)\cos^2(\varphi)\right]}\ . \quad \textbf{(3.23)}$$

Due to symmetry (between the positive and negative half cycles) of the reference and carrier waveforms, the expression for the lower dc-link capacitor ($C_1$) is identical.

### 3.3.3 CHB inverter

The derivation of the dc-link capacitor current rms for the three-phase CHB inverter is based on the analysis of a single H-Bridge, that of phase *a*. Each phase of the H-Bridge has its own capacitor whose ripple current, in contrast to the 2L and NPC topologies, is not affected by the switching operations of the other phases. Thus, the analysis of a single phase H-Bridge inverter is enough to provide the three-phase inverter expressions.

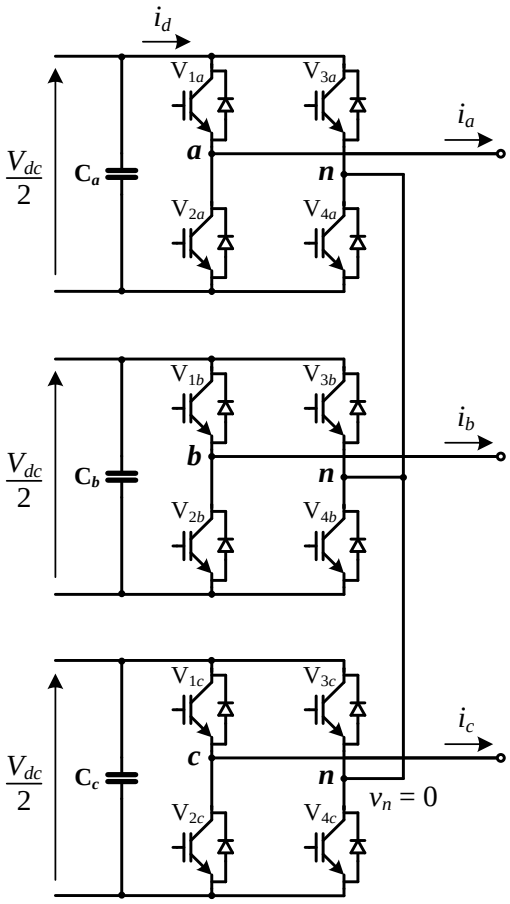


**Figure 3.7.** Three-phase CHB inverter, illustrating current $i_d$.

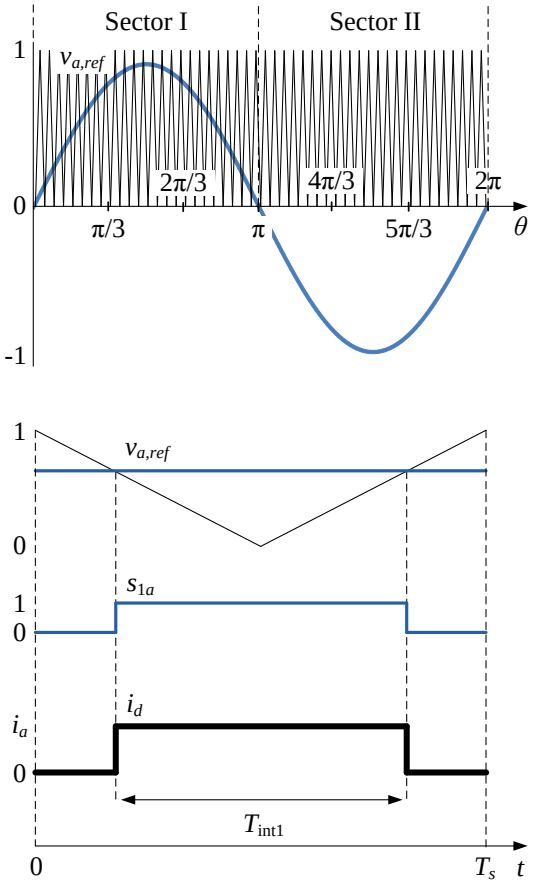


**Figure 3.8.** Analysis of a switching cycle for Sector I of the CHB inverter.

For the CHB inverter sum of the currents through the two upper IGBT-diode modules is used for the derivation. The calculation of the capacitor rms current is based on the analysis of one out of two symmetrical sectors (Sector I in Figure 3.8) covering the interval of $\theta = [0, \pi]$.

| **Tot. duration** | **Tot. duty cycle** | **Current $i_d$** |
|---|---|---|
| $T_{int1}$ | $\delta_a$ | $i_a$ |

**Table 3.5.** Switching intervals for Sector I of the CHB inverter.

According to Table 3.5,

$$i_{d,dc,I-CHB}(\theta) = \delta_a \cdot i_a \ , \tag{3.24}$$

$$i^2_{d,rms,I-CHB}(\theta) = \delta_a \cdot i^2_a \ . \tag{3.25}$$

The average (dc) and rms values of current $i_d$ for the CHB inverter are calculated using (3.7) and (3.8), respectively, for $\theta = [0, \pi]$, as

$$I_{d,dc-CHB} = \frac{MI_{pk}}{2}\cos\varphi \ , \tag{3.26}$$

$$I_{d,rms-CHB} = I_{pk}\sqrt{\frac{M\left(3+\cos(2\varphi)\right)}{3\pi}} \ . \tag{3.27}$$

The rms current expression for each capacitor in this topology is then given by (3.4), as

$$I_{C,rms-CHB} = I_{pk}\sqrt{\frac{M}{24\pi}\left[24-3M\pi+\left(8-3M\pi\right)\cos(2\varphi)\right]} \ . \tag{3.28}$$

It is noted that the dc-link capacitor current of a single-phase H-Bridge modulated by the SPWM strategy has been investigated in [46], deriving an expression for the rms value of high-frequency capacitor current harmonics. This expression is equivalent to (3.28), which also incorporates the low-frequency (baseband) harmonic of the CHB inverter dc-link capacitor current.

## 3.4 Analytical derivation of dc-link capacitor current harmonics

In this section, the geometric wall model, a method introduced by H. S. Black in [56], is used to analytically derive the dc-link current spectra of 3L inverters. The geometric wall model provides an alternative way for representing the process of pulse generation in PWM converters. As shown in [13], the carrier and reference waveforms are redrawn in a transformed plane, so that the intersections between the new waveforms define the same train of pulses as a given PWM modulation strategy. The new plane can be divided into identical unit cells, which are characteristic for each strategy. The width of the generated pulses is periodic with respect to both dimensions of this plane, thus the function ($F$) that describes the pulse train can be written as a double Fourier series.

The Fourier analysis results in a spectrum that plots the function in the frequency domain. The (complex) Fourier coefficient for a harmonic ${}^{mn}F$ of function $F$, located at frequency $nf+mf_c$ ($n$, $m$ are integers), where $f$ and $f_c$ are the fundamental and switching frequencies, respectively, are given by the following integral over the area of a unit cell:

$$ {}^{mn}F = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} F(x,y) e^{j(mx+ny)} dxdy \ . \tag{3.29} $$

The geometric wall model has been widely applied for analysing the output (PWM) voltage harmonics of different inverter topologies and PWM strategies [13]. In this case, $F$ represents a phase voltage (commonly that of phase $a$). For the analysis of the dc-link capacitor current, on the other hand, $F$ represents a module current, namely the current through the IGBT-diode module $V_{1a}$.

### 3.4.1 Two-level inverter

Assuming naturally sampled sine-triangle modulation (triangular carrier and sinusoidal reference waveforms), the Fourier coefficients of current $i_{V1a}$ for the 2L inverter were derived in [43, 48]. After some manipulation and conversion to their complex form, these coefficients take the form of (3.30) for baseband, and (3.31) for carrier-sideband harmonics.

Baseband harmonics, for $m = 0$ and $n = 1, 2$:

$$ {}^{0n}i_{V1a} = \begin{cases} \dfrac{I_{pk}}{j2} e^{j\phi}, & \text{for } n = 1 \\ \dfrac{MI_{pk}}{j4} e^{j\phi}, & \text{for } n = 2 \end{cases} \tag{3.30} $$

Carrier (for $m \neq 0$, $n = 0$) and sideband (for $m \neq 0$, $n \neq 0$) harmonics:

$$ {}^{mn}i_{V1a} = \frac{j^n e^{jm\frac{\pi}{2}} I_{pk}}{m\pi} \cdot \cos\left[(m+n)\frac{\pi}{2}\right] \cdot \left[ e^{-j\phi} J_{n+1}\left(m\frac{\pi}{2}M\right) - e^{j\phi} J_{n-1}\left(m\frac{\pi}{2}M\right) \right] \ . \tag{3.31} $$

The Fourier coefficients for the currents of the two other upper modules, $V_{1b}$ and $V_{1c}$, are given by multiplying the coefficients for $i_{V1a}$ by $e^{+2jn\pi/3}$ and $e^{-2jn\pi/3}$, respectively. Current $i_d$ is

the complex sum of these three module currents, thus its Fourier coefficients can be calculated using

$$ {}^{mn}i_d = {}^{mn}i_{V1a} \cdot \left(1 + e^{j2n\pi/3} + e^{-j2n\pi/3}\right) = \begin{cases} 3\,{}^{mn}i_{V1a}, & \text{for } n \bmod 3 = 0 \\ 0, & \text{for } n \bmod 3 \neq 0 \end{cases} . \qquad \textbf{(3.32)} $$

The coefficients for the dc-link capacitor current are also given by (3.24), excluding the dc component ($n = m = 0$). According to (3.30) and (3.32), no baseband harmonic remains in this current. Hence, the 2L inverter does not generate any low-frequency capacitor voltage ripple when it supplies a linear and balanced load.

### 3.4.2 NPC inverter

As in the 2L inverter, the instantaneous current flowing through the dc-link capacitor of the NPC inverter is the complex sum of the currents through the inverter's three upper modules ($V_{1a}$, $V_{1b}$ and $V_{1c}$), shown in Figure 3.5. Thus, harmonic analysis of $i_{V1a}$ is sufficient to calculate the dc-link capacitor current harmonics. The following solution is given for a SPWM implemented as the three-level Phase-Disposition Pulse Width Modulation (PD PWM) [13], which uses two in-phase triangular carriers (and a sinusoidal reference waveform). The application of the geometric wall model to the three-level PD PWM results in the unit cell illustrated in Figure 3.9.

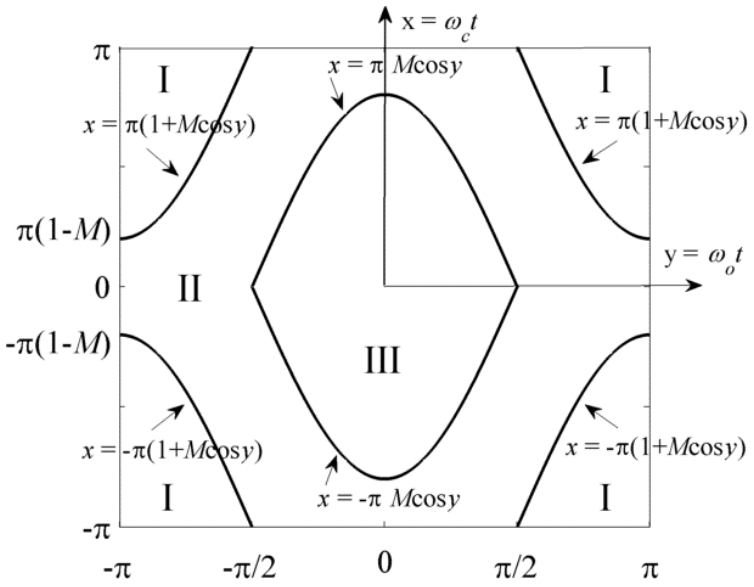


**Figure 3.9.** Unit cell for the three-level PD PWM modulation strategy **[13]**.

The complex Fourier coefficients of $i_{V1a}$ come from:

$$ {}^{mn}i_{V1a-NPC} = \frac{1}{2\pi^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi} i_{V1a-NPC}(x,y)\; e^{j(mx+ny)}dxdy \;. \tag{3.33} $$

According to [13], the output voltage for phase *a* is positive only in the closed region (III), at the center of the graph. Thus, this is the only region where module $V_{1a}$ carries the current of phase *a*. In regions I and II, the current through $V_{1a}$ is zero. The above integral therefore reduces to

$$ {}^{mn}i_{V1a-NPC} = \frac{I_{pk}}{2\pi^2}\int_{-\pi/2}^{\pi/2}\int_{-\pi M\cos y}^{\pi M\cos y} \cos(y-\varphi)\cdot e^{j(mx+ny)}dxdy \;. \tag{3.34} $$

Solution of (3.34) provides the complex Fourier coefficients for $i_{V1a}$, while (3.32) gives the respective coefficients for the upper dc-link capacitor of the 3L NPC inverter:

Baseband harmonics, for ($m$ = 0 and) $n$ = 3, 9, 15, …:

$$ {}^{0n}i_{C-NPC} = (-1)^{\frac{n-1}{2}}\frac{6MI_{pk}}{\pi(n^2-4)}\left(\frac{2\cos\varphi}{n} + j\sin\varphi\right) \;. \tag{3.35} $$

Carrier harmonics, for ($n$ = 0 and) $m$ = 1, 2, 3, …:

$$ {}^{m0}i_{C-NPC} = -\frac{3I_{pk}}{m\pi}J_1(Mm\pi)\cos\varphi \;. \tag{3.36} $$

Sideband harmonics, for $n$ even and $m$ = 1, 2, 3, …:

$$ {}^{mn}i_{C-NPC} = (-1)^{\frac{n}{2}}\frac{3I_{pk}}{2m\pi}\begin{bmatrix} e^{j\varphi}J_{n-1}(Mm\pi) \\ -e^{-j\varphi}J_{n+1}(Mm\pi)\end{bmatrix} . \tag{3.37} $$

Sideband harmonics, for $n$ odd and $m$ = 1, 2, 3, …:

$$ \begin{aligned} {}^{mn}i_{C-NPC} &= (-1)^{\frac{n-1}{2}}\frac{6I_{pk}}{m\pi^2}\sum_{k=1,3,5\ldots}J_k(Mm\pi)\cdot \\ &\left[\frac{\cos\varphi + j(n+k)\sin\varphi}{1-(n+k)^2} - \frac{\cos\varphi + j(n-k)\sin\varphi}{1-(n-k)^2}\right] . \end{aligned} \tag{3.38} $$

### 3.4.3 CHB inverter

As explained in Section 3.3.3, the current of each capacitor in this topology is only determined by the operation of the respective H-Bridge. Hence, the derivation of a capacitor current is not given by an equation in the form of (3.32). Instead, similarly to Section 3.3.3, the current that will be harmonically analysed for this topology is $i_d$, shown in Figure 3.7. The ac component of this current flows through the dc-link capacitor of phase *a*.

A modulation strategy for the CHB inverter that is equivalent to PD PWM for the NPC inverter is assumed. This strategy, that yields equal switching losses and the same output voltage spectra for the two topologies, is described in [13] (pages 504 – 506). Pulse generation is again based on the unit cell of Figure 3.9, thus

$$ {}^{mn}i_{d-CHB} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} i_{d-CHB}(x,y)\, e^{j(mx+ny)} dxdy \ . \qquad \textbf{(3.39)} $$

According to [13], the output voltage for phase *a* is positive in region III and negative in region(s) I, at the edges of the plot. The current $i_d$ of the CHB inverter is therefore equal to the phase current $i_a$, or opposite to it ($-i_a$) in these regions, respectively. The above integral then reduces to

$$ {}^{mn}i_{d-CHB} = \frac{I_{pk}}{2\pi^2} \left[ \int_{-\pi/2}^{\pi/2} \int_{-\pi M\cos y}^{\pi M\cos y} \cos(y-\varphi)\cdot e^{j(mx+ny)} dxdy - \int_{\pi/2}^{-\pi/2} \int_{\pi(1+M\cos y)}^{-\pi(1+M\cos y)} \cos(y-\varphi)\cdot e^{j(mx+ny)} dxdy \right] \qquad \textbf{(3.40)} $$

which can be shown to be equal to

$$ {}^{mn}i_{d-CHB} = \begin{cases} \dfrac{I_{pk}}{\pi^2} \displaystyle\int_{-\pi/2}^{\pi/2} \int_{-\pi M\cos y}^{\pi M\cos y} \cos(y-\varphi)\, e^{j(mx+ny)} dxdy, & for\ n+m \to even \\ 0, & for\ n+m \to odd \end{cases} . \qquad \textbf{(3.41)} $$

Solution of (3.41) yields the Fourier coefficients of $i_d$ which, apart from the dc component, are also the coefficients for the dc-link capacitor current of phase *a*:

Baseband harmonic, for ($m$ = 0 and) $n$ = 2, only:

$$ {}^{02}i_{C-CHB} = \frac{MI_{pk}}{2} e^{j\varphi} \ . \tag{3.42} $$

Carrier harmonics, for ($n$ = 0 and) $n$ even:

$$ {}^{m0}i_{C-CHB} = -\frac{2I_{pk}}{m\pi} J_1\left(Mm\pi\right)\cos\varphi \ . \tag{3.43} $$

Sideband harmonics, for $n$ even and $m$ even:

$$ {}^{mn}i_{C-CHB} = \left(-1\right)^{1+\frac{n}{2}} \frac{I_{pk}}{m\pi} \begin{bmatrix} e^{j\varphi} J_{n-1}\left(Mm\pi\right) \\ -e^{-j\varphi} J_{n+1}\left(Mm\pi\right) \end{bmatrix} \ . \tag{3.44} $$

Sideband harmonics, for $n$ odd and $m$ odd:

$$ \begin{aligned} {}^{mn}i_{C-CHB} &= \left(-1\right)^{\frac{n+1}{2}} \frac{4I_{pk}}{m\pi^2} \sum_{k=1,3,5\ldots} J_k\left(Mm\pi\right) \cdot \\ &\left[ \frac{\cos\varphi + j(n+k)\sin\varphi}{1-(n+k)^2} - \frac{\cos\varphi + j(n-k)\sin\varphi}{1-(n-k)^2} \right] \end{aligned} \ . \tag{3.45} $$

Apart from the above PD PWM equivalent, the CHB inverter can also be modulated with unipolar modulation, which is common for single-phase CHB inverters. This strategy uses a single carrier waveform and two opposite (that is, shifted by 180 degrees) reference waveforms, each of which modulates a leg of the H-Bridge. The harmonic coefficients for the capacitor current are therefore given by (3.46), below:

$$ {}^{mn}i_{C-CHB1\varphi} = {}^{mn}i_{V1a} \cdot \left(1 + e^{jn\pi}\right) = \begin{cases} 2\,{}^{mn}i_{V1a}, & \text{for } n \text{ even} \\ 0, & \text{for } n \text{ odd} \end{cases} \tag{3.46} $$

As derived from (4.42) and (4.46), the dc-link capacitor current of an H-Bridge inverter contains a single baseband harmonic ($m$ = 0, $n$ = 2) at twice the fundamental frequency:

$$ {}^{02}i_{C-CHB1\varphi} = \frac{MI_{pk}}{j2} e^{j\phi} \ . \tag{3.47} $$

## 3.5 Numerical derivation of dc-link capacitor current rms value and amplitude of voltage ripple

The analytical derivation of expressions for the rms value and the harmonics of the dc-link capacitor current in the previous sections assumed sinusoidal voltage reference waveforms (SPWM strategy). However, non sinusoidal references are commonly used in practice in order to achieve higher output (line) voltages, corresponding to a maximum modulation index of $2/\sqrt{3}$ ($\approx 1.1547$). A numerical method for calculating the capacitor rms current in case of such reference waveforms is proposed in this section.

The method is based on the analysis presented in Section 3.3 and operates according to the code included in Appendix A.4. The code divides the fundamental cycle into a number of intervals and calculates the values of (3.5) and (3.6) for each of them. The cumulative sums of these values are then used to numerically evaluate (3.7) and (3.8), and finally derive the rms capacitor current. Furthermore, in parallel to the rms current calculation, the proposed method calculates the amplitude of the capacitor voltage oscillations. The calculation can be performed for any modulation strategy, by accordingly changing the reference voltages (or, equivalently, the common-mode voltage) in the code. Results for the following strategies are presented in this study: A) SPWM, B) SPWM with 1/6 third harmonic injection (SPWM+3$^{rd}$ harm.), and C) SV Modulation (SVM) with equal distribution of duty cycles between the small vectors, implemented as a carrier-based strategy. The common-mode voltages for each of these strategies can be found in the code.

Figures 3.10(a) and 3.10(b) plot the rms value of the capacitor current for the NPC and CHB topologies, normalized with respect to the phase rms current, $I_o$ (Norm. $I_{C,rms} = I_{C,rms}/I_o$). For the NPC inverter the plot is the same for any modulation strategy (SPWM can reach up to $M = 1$), while for the CHB inverter it is shown for the SVM strategy. It is noted that for the 2L inverter (and for any modulation strategy) the rms plot is the same as the one in Figure 3.10(a), as shown in [44, 45].

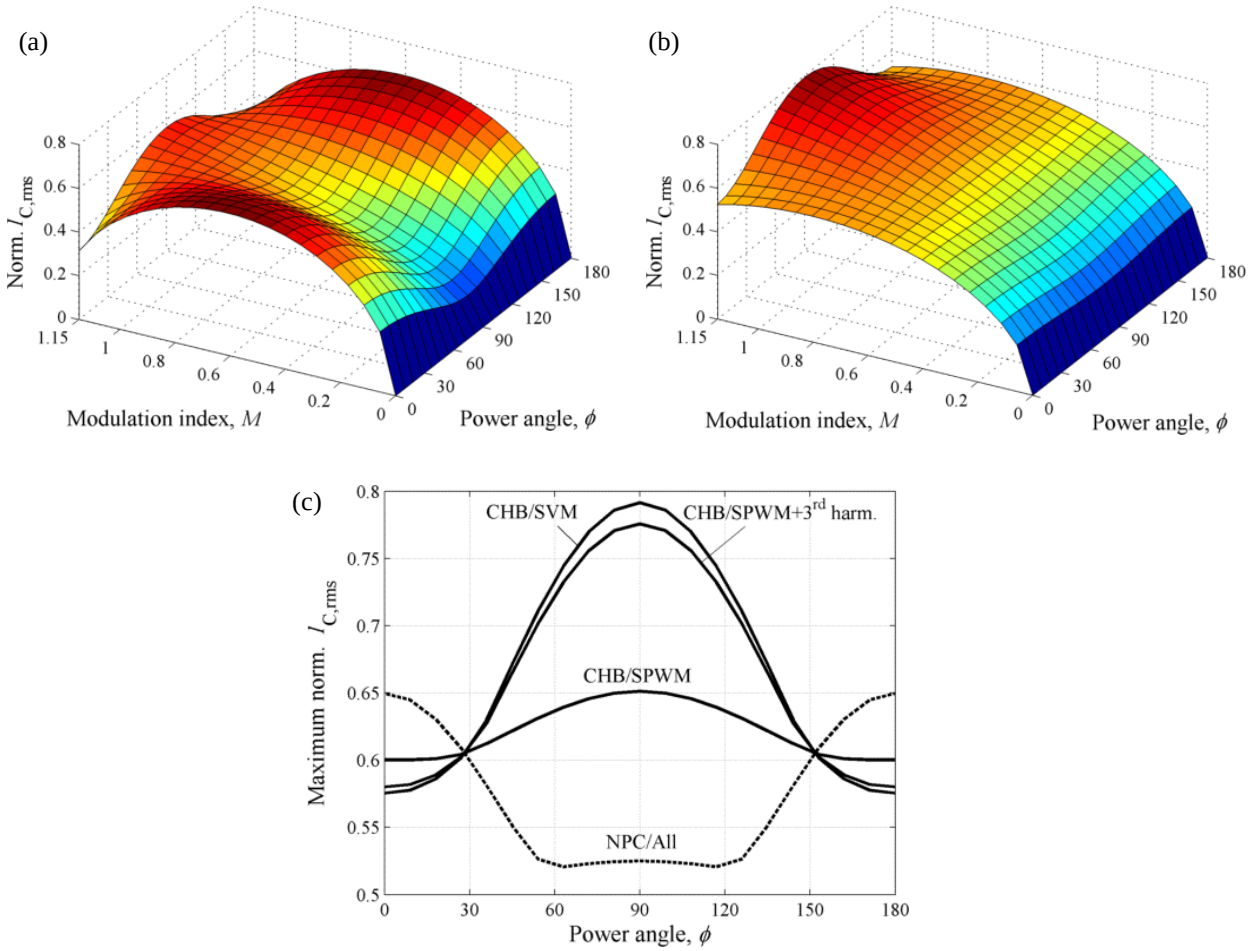


**Figure 3.10.** (a) Normalized rms capacitor current for the NPC inverter (same for all modulation strategies), (b) Normalized rms capacitor current for the CHB inverter modulated by the SVM strategy, and (c) Maximum normalized rms capacitor current for the NPC and CHB inverters, as a function of $\phi$.

The rms current rating of the dc-link capacitors is determined by the maximum value that $I_{C,rms}$ can take within the operating range of the inverter. Figure 3.8(c) illustrates this maximum (over the whole range of $M$) for each value of $\phi$, for the examined modulation strategies. Given that the range of power factor (angle) is known for most inverter applications, this figure can be used to select the required capacitor rms current rating according to the applied strategy.

Similar graphs are derived below using the proposed method, for the amplitude ($\Delta V_C/2$) of the dc-link capacitor voltage ripple. Figures 3.11(a) and 3.11(b) plot this amplitude for the NPC and CHB topologies, respectively, for the case of the SVM strategy.

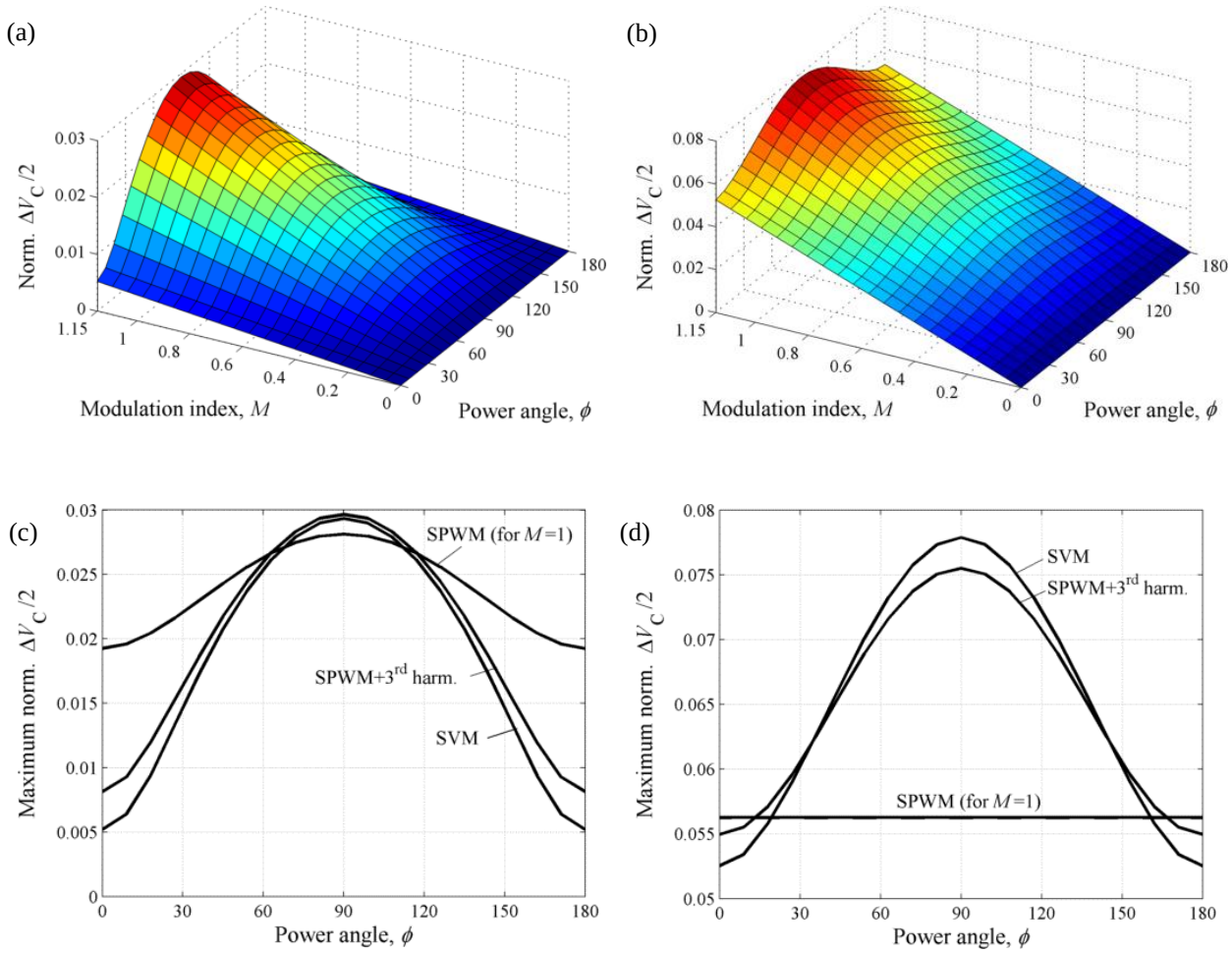


**Figure 3.11.** Normalized amplitude of capacitor voltage ripple for (a) the NPC, and (b) the CHB inverter, modulated by the SVM strategy, and maximum normalized amplitude of capacitor voltage ripple for (c) the NPC, and (d) the CHB inverter, as a function of $\phi$.

Furthermore, Figures 3.11(c) and 3.11(d) illustrate the maximum amplitude of voltage ripple (which appears for maximum *M*) for the two topologies, for each modulation strategy. The presented values are normalized according to

$$\frac{\text{Norm. } \Delta V_C}{2} = \frac{fC}{I_o}\frac{\Delta V_C}{2} \quad , \tag{3.48}$$

and can be used to determine the capacitance required to limit the voltage ripple to a desired extent, $\Delta V_{C,\max}$ (see Section 3.2). It can be observed that for any value of *M*, the maximum amplitude of capacitor voltage ripple occurs for $\phi$ = 90 degrees, that is, for purely reactive loads. This is not however always the case for the rms capacitor current, as it can be seen in

Figures 3.10(a) and (b). As an example, notice the dip in Figure 3.10(a) for $M$ between 0.1 and 0.8, and $\phi$ = 90 degrees, in contrast to the peak appearing at the respective range in Figure 3.11(a). The reason behind this difference is that the amplitude of capacitor voltage ripple is mainly determined by the LF capacitor current harmonics (as explained in Section 3.2), whereas the current rms value is equally affected by LF and HF harmonics. Thus, in cases of decreased HF harmonics, increased amplitude of capacitor voltage ripple may not be accompanied by increased capacitor rms current.

## 3.6 Simulation results

In this section, the (analytically and numerically) derived values of dc-link capacitor rms current, voltage ripple, and current harmonics are validated using detailed circuit simulations in MATLAB – Simulink (SimPowerSystems toolbox). At the same time, a capacitor sizing example is presented, followed by a discussion on the requirements of the examined 3L topologies. For the purpose of this example, the NPC and CHB inverter were simulated according to the operating parameters in Table 3.6.

| Parameter | Value |
|---|---|
| $V_{dc}$ | 400 V |
| $I_{pk}$ | 100 A |
| $f$ | 50 Hz |
| $f_c$ | 5 kHz |
| $M$ | 0.9 |
| $\phi$ | 30 degrees |
| $C_{NPC}$ | 1 mF |
| $C_{CHB}$ | 2.5 mF |

**Table 3.6.** Simulation parameters.

The capacitance value for the CHB inverter was set to 2.5 mF, as compared to 1 mF for the NPC inverter, in order to obtain a similar voltage ripple for the two topologies. The amplitude of this ripple (≈ 28 V) was selected to be equal to a small percentage (7%) of the dc-link voltage, thus avoiding a significant distortion of the line voltage.

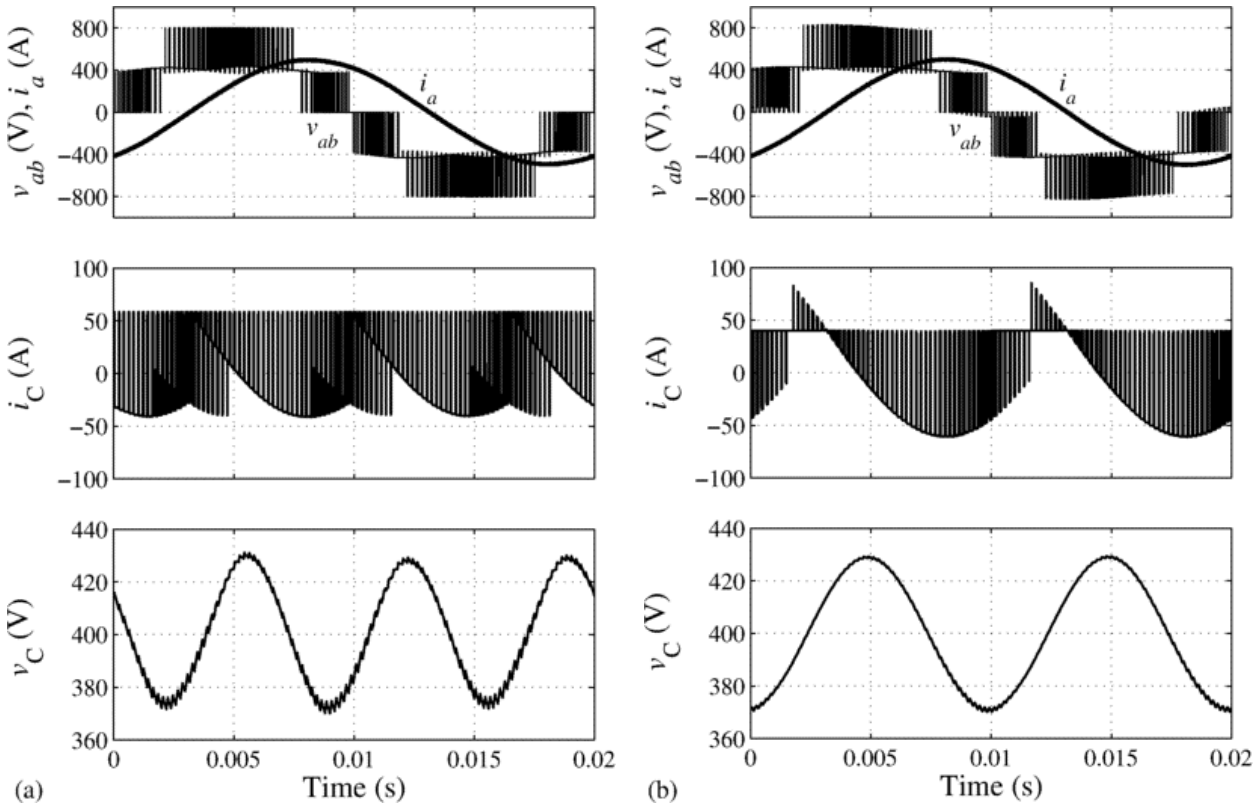


**Figure 3.12.** Simulation results for (a) the NPC ($C$ = 1 mF) inverter, and (b) the CHB inverter ($C$ = 2.5 mF).

Figure 3.12 illustrates the line voltage $v_{ab}$, phase current $i_a$, and capacitor ($C_2$ for the NPC and $C_a$ for the CHB) current $i_C$ and voltage $v_C$ for the two topologies. The simulated amplitude of capacitor voltage ripple agreed with the value of 28 V, calculated by the proposed method. Moreover, the rms values of the capacitor current measured during the simulations agreed with the values of 39.3 and 42.7 A, given by the same method as well as by (3.23) and (3.28) for the NPC and CHB inverters, respectively.

Figure 3.13, below, illustrates the capacitor current spectrum for the two topologies as derived from the above simulations, and use it to validate the expressions presented in Section 3.4. Again, it can be seen that the frequencies and magnitudes of the current harmonics can be accurately reproduced by these expressions. Furthermore, the amplitude of capacitor voltage ripple can be calculated by means of (3.3). Considering only the baseband harmonics, this calculation gives a value of 28.6 V for both topologies, which is similar to that taken from the simulations.

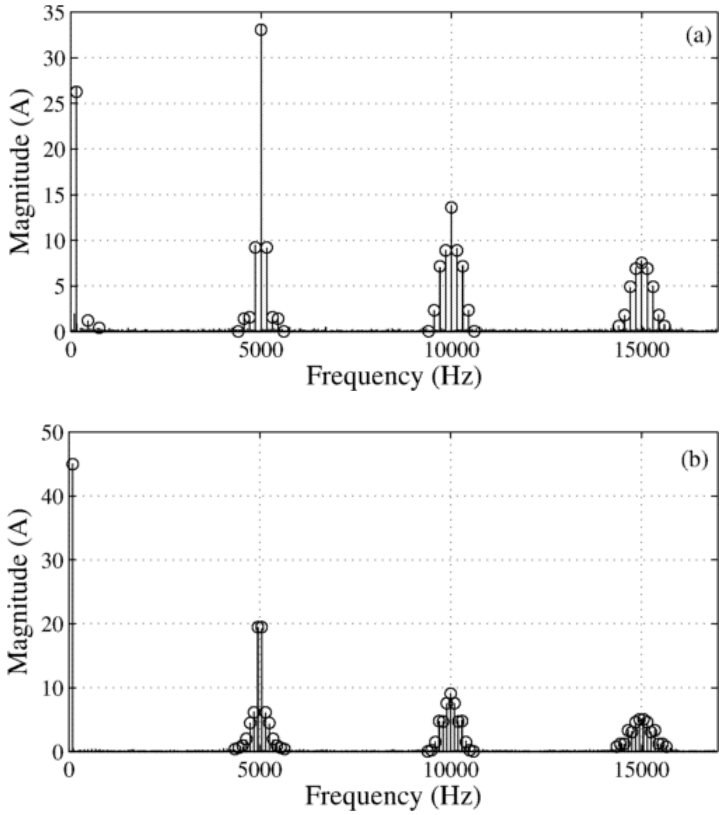


**Figure 3.13.** Spectrum of dc-link capacitor current for (a) the NPC and (b) the CHB inverter. Lines and circles represent the simulated and analytically derived magnitudes of the current harmonics, respectively.

## 3.7 Discussion

### 3.7.1 Comparison of capacitor size for the NPC and CHB inverters

The results presented in Sections 3.3 – 3.5 were validated by simulations for a wide range of inverter operating parameters (Modulation index, load power factor, fundamental and carrier frequencies). Figure 3.14 illustrates representative results from the validation process, assuming the operating parameters in Table 3.6 and covering the whole range of *M*.

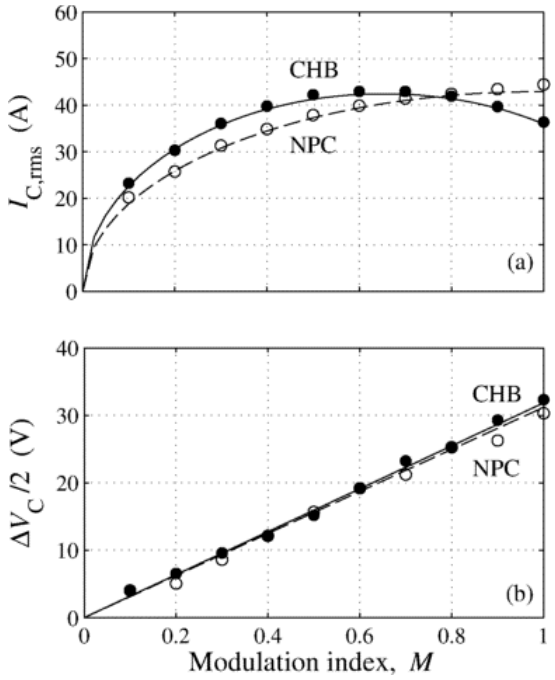


**Figure 3.14.** (a) DC-link capacitor rms current, and (b) amplitude of voltage ripple for the NPC ($C$ = 1 mF) and CHB ($C$ = 2.5 mF) topologies as a function of $M$, for the parameters shown in Table 3.6.

Figure 3.14 can also provide a comparative overview of the ripple current and capacitance requirements for the NPC and CHB topologies, at a condition (of $\phi$ = 30 degrees) which is common for inverters operating as motor drives. Namely, it can be seen that the maximum ripple current is similar for both topologies, whereas the required capacitance is 2.5 times higher for the CHB inverter. Thus, each capacitor of the CHB inverter should have 2.5 times the size (equal voltage and ripple current rating, but 2.5 times more capacitance) of a capacitor for the NPC inverter.

For a different value of $\phi$, a similar comparison between the two topologies can be obtained by means of Figures 3.10(c) and 3.11(c)-(d). As a general observation, however, we could note the following: According to Figure 3.11, for any value of $\phi$, the capacitance required to obtain the same voltage ripple is at least two times higher for the CHB inverter. For values of $\phi$ that the ripple current is comparable for the two topologies ($\phi$ < 40 degrees, according to Figure 3.10(c)), each capacitor of the CHB inverter should therefore have double the size, as compared to the NPC inverter. Additionally, since the CHB inverter requires three (instead of two) capacitors for its dc-links, the total capacitor size will be at least three times greater for this topology. Even in cases when the ripple current is higher for

the CHB inverter ($\phi$ approaching 90 degrees in Figure 3.10(c)), a similar ratio of capacitor sizes can be expected. This is due to the fact that increased capacitance (for the CHB inverter) is commonly achieved through the parallel connection of capacitors, which at the same time share the higher amounts of ripple current.

### 3.7.2 Comparison of methods for analysing dc-link capacitor current

A close examination of ESR characteristics of electrolytic capacitors indicates that their ESR decreases for harmonic frequencies between 50 Hz and 1 kHz, while it remains approximately constant (to $R_C = R_{C,HF}$) for higher frequencies. Additionally, inverter switching (carrier) frequencies are commonly higher than 1 kHz. As a result, the majority of carrier and sideband harmonic groups, which appear around multiples of the switching frequency, belong in the constant-ESR frequency range. Baseband harmonics, however, have to be associated with higher ESR values (Figure 3.1). Loss estimation based on rms current expressions (Section 3.3) fails to treat these harmonics separately, which results in an underestimation of dc-link capacitor losses for 3L inverters.

Harmonic analysis, on the other hand, can be used according to (3.2) to provide a more accurate estimate for dc-link capacitor losses. Furthermore, given that the losses arising from the carrier and sideband capacitor current harmonics can be associated with $R_{C,HF}$ in (3.2), the total capacitor losses can be taken from

$$P = \sum_{B} R_C\left(f_h\right) \cdot I_{h,rms}^2 + R_{C,HF} \cdot \sum_{C/S} I_{h,rms}^2 \quad . \tag{3.49}$$

The subscripts *B* and *C*/*S* under the sums in (3.49) denote that they refer to baseband and carrier/sideband harmonics, respectively.

Equation (3.49) can also be written as

$$P = \sum_{B} R_C\left(f_h\right) \cdot I_{h,rms}^2 + R_{C,HF} \cdot \left[ I_{C,rms}^2 - \sum_{B} I_{h,rms}^2 \right], \tag{3.50}$$

indicating that knowledge of the capacitor rms current and baseband harmonics is sufficient to obtain an accurate estimate for capacitor losses. The proposed numerical method can make use of (3.50), based on its calculation of the capacitor current rms value and an approximation for the baseband harmonics. Namely, the baseband harmonics can be

approximated by the dominant baseband harmonic, assuming that it alone generates the capacitor voltage ripple, $\Delta V_C$ (which is also calculated by the proposed strategy). Since this harmonic is located at a frequency of $3f$ and $2f$ for the NPC and CHB topologies, respectively, its amplitude can approximately be taken by

$$I_k = k\Delta V_C C\pi f \,, \tag{3.41}$$

where $k$ is equal to 3 and 2, accordingly. Thus, in addition to the calculation of $\Delta V_C$, the proposed numerical method offers a more accurate estimate of capacitor losses as compared to the analytical approach of Section 3.3. Moreover, in comparison to the harmonic analysis, it has the advantage of being easily adapted to different modulation strategies, as explained in Section 3.4.

On the other hand, the harmonic analysis can provide closer estimates of capacitor power losses for inverters that operate at low switching frequencies or use capacitors with different ESR characteristics. In these cases, certain carrier-sideband harmonic groups may belong to the low-frequency ESR region and therefore the results of a complete harmonic analysis should be used according to (3.2).

### 3.7.3 Extension to higher-level inverters

This study focused on the dc-link capacitor current analysis of 3L NPC and CHB inverters. The presented methods can also be applied to higher-level inverters, provided that they are modulated by strategies whose reference and carrier waveforms can be defined analytically. However, such conventional modulation strategies are practically not applicable to NPC multilevel (ML) inverters, since they are unable to prevent voltage collapse of the intermediate dc-link capacitors [57]. Furthermore, unconventional strategies which can retain the capacitor voltages, increase the switching frequency of the switching devices, induce higher output voltage steps ($dv/dt$), and distort the multilevel PWM waveform [5, 35].

As a consequence, multilevel converters with more than three levels are predominantly based on the series connection of H-bridge cells, creating CHB ML topologies [58]. Extension to these topologies is possible for all presented methods for analyzing the dc-link capacitor current, but the complexity of analytical derivations increases with the number of voltage levels. The proposed numerical approach, on the other hand, can be extended as

shown in the relevant part of the code (in Appendix A. to cover the CHB ML topologies. As for the 3L inverter, the code simply calculates the duty cycle of each inverter cell and numerically integrates the current (and its square) through its dc-link capacitor. Results for CHB ML inverters have also been validated with simulations.

### 3.7.4 DC-link capacitor current harmonics due to the inverter Front-End

This study focused on the dc-link capacitor current resulting from the operation of an NPC or CHB inverter. For the purposes of the analysis, the inverter FE was assumed to provide the dc component of current $i_d$ (see Section III), without injecting additional ac current to the dc-link capacitor. In cases of FEs such as batteries, PV panels and fuel cells, this assumption is accurate. Rectifiers or Active Front Ends (AFEs), on the other hand, can inject ac current to the dc-link capacitor.

- With regards to rectifiers, the harmonics of this current can be calculated as shown in [59]. The present study then offers the analytical tools to estimate the total capacitor losses and sizing requirements, by superimposing the rectifier to the inverter current harmonics. It is also noted that it is a common practice to use dc-link inductors (chokes) to suppress the ac current injected to the capacitor by a rectifier.
- The dc-link capacitor current harmonics for an AFE can be calculated as shown in this study, since an AFE is merely an inverter operating with a negative power factor load ($90 < \phi < 270$ degrees). Namely, the expressions of [47] and Section 3.4.2 can be used for the common cases of 2L and NPC-type AFEs, respectively. The resulting harmonics can then be superimposed to those due to the inverter, to derive the capacitor current spectrum.

### 3.7.5 Using the analysis to select dc-link capacitors

This section presents the results of this study in a way that they can be readily used for selecting dc-link capacitors.

*Voltage rating*

- Set to 1.2 to 1.5 times the dc-link voltage, to account for capacitor voltage ripple and supply voltage surges.

*Capacitance rating*

- Given the power angles of the loads the inverter should be able to supply, use Figure 3.11 to determine the maximum expected normalized amplitude of voltage ripple (norm. $\Delta V_C$) for the selected topology and modulation strategy.
- Consider the minimum fundamental frequency and maximum output current the inverter is expected to provide. In (3.48), use these values for $f$ and $I_o$ respectively, and the value of norm. $\Delta V_C$ from the previous step.
- Set the value of $\Delta V_C$ to the maximum acceptable amplitude of voltage ripple (typically 5 to 10% of the dc-link voltage) and solve the equation for C.

*Ripple current rating – Power losses*

- For the selected range of load power angles, use Figure 3.10 to determine the maximum normalized capacitor rms current and denormalise based on the maximum expected output current.
- Estimate the amplitude of the baseband harmonic of the capacitor current, by means of (3.41).
- Calculate the power losses in the capacitor based on its ESR characteristic and (3.50).

*Effect of the FE*

- Calculate the dc-link capacitor current due to the converter FE.
- Add that (in rms terms) to the capacitor ripple current due to the inverter.

- Calculate the additional capacitor voltage ripple based on the calculated capacitance value and the baseband harmonics of the dc-link capacitor current due to the FE.
- Increase $C$ to meet the restriction on maximum voltage ripple.
- Calculate the additional power losses in the capacitor due to the FE, based on its ESR characteristic and (3.50).

*Capacitor selection*

- Select a capacitor according to the overall requirements for voltage, capacitance and power losses.
- From the power losses, calculate the temperature rise in the capacitor. Add that to the maximum expected ambient temperature, to estimate the maximum hotspot temperature.
- If the latter exceeds the limit given by the manufacturer, consider connecting two or more capacitors in parallel.
- Repeat the calculations taking into account the equivalent value of $C$ and the current division between the paralleled capacitors.

## 3.8 Conclusion

This study presented a series of analytical and numerical tools for analysing the dc-link capacitor current in 3L NPC and CHB inverters. Its results can be practically useful for inverter designers performing the task of dc-link capacitor sizing.

Analytical expressions were derived for the rms value and harmonics of the dc-link capacitor current, whose knowledge is essential for determining the required capacitance and ripple current rating of dc-link capacitors. Moreover, the proposed numerical method provided the possibility to estimate capacitor sizing parameters for different modulation strategies, offering a simpler alternative to repeating the analytical derivations. Results based on the proposed approach were illustrated for common modulation strategies and were validated using simulations in MATLAB-Simulink. According to them, the CHB inverter has

significantly (at least three times) higher capacitor size requirements as compared to the NPC inverter.

# Chapter 4

## Capacitor size reduction for multiple inverter systems

## 4.1 Introduction

The previous chapter presented a number of methods for analyzing the dc-link capacitor current of 2L and 3L converters. Pertaining to multiple inverter systems, harmonic analysis additionally offers the basis for examining the possible capacitor current harmonic reductions or cancellations that can be achieved by connecting two or more inverters to a common dc-link. This chapter will examine systems incorporating multiple 2L, or 3L CHB inverters. Systems based on the NPC inverter are not covered due to the NP voltage ripple problem of this topology, studied separately in the following chapters.

Multiple inverter systems have been extensively incorporated in high-power applications. In addition to high-power electric motor drives, comprising multiple inverters that share the total drive current, multiple inverter systems have been used to drive multi-phase motors, or different motors in multiple motor applications. Key examples of such applications are conveyor belts and electric vehicles with direct drive wheel motors.

In a conventional multiple inverter system, each inverter is connected to its own dc-link. The present study investigates potential reduction in overall capacitor size that can be achieved in multiple inverter systems, by using a common dc-link capacitor as shown in Figure 4.1. The study covers a range of cases for multiple inverter systems, defined by the number of inverters ($N$), the phase angles of the inverter reference waveforms, and type of inverter. It is noted that for the purposes of this chapter, SPWM-modulated CHB inverters are referred to and analysed as single-phase inverters, according to Section 3.3.3.

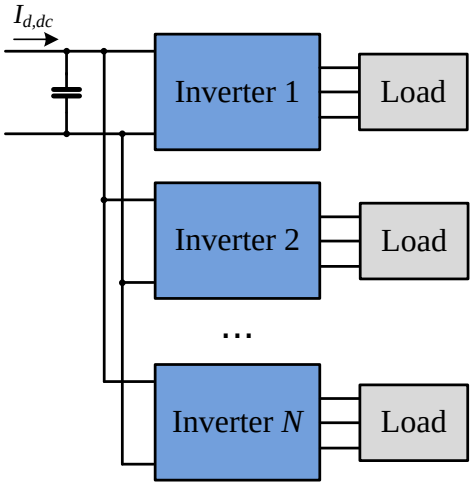


**Figure 4.1.** Block diagram of system with $N$ three-phase inverters sharing a common dc-link capacitor.

## 4.2 Common dc-link capacitor current harmonics

Assuming naturally sampled SPWM, the current harmonics for 2L and 3L CHB inverters, are given by (3.32) and (3.46), respectively. A current harmonic, ${}^{mn}h$, in its complex form, can be expressed in the time domain as

$$ {}^{mn}h(t) = \left| {}^{mn}h \right| \cdot \cos\left( n \cdot \left[ \omega_c t + \theta_c \right] + m \cdot \left[ \omega_o t + \theta_o \right] - {}^{mn}\phi \right) $$

$$ {}^{mn}\phi = \tan^{-1}\left( \frac{\mathrm{Im}\left\{ {}^{mn}h \right\}}{\mathrm{Re}\left\{ {}^{mn}h \right\}} \right) , \qquad \textbf{(4.1)} $$

where $\omega_c$ and $\omega_o$ are the carrier and fundamental angular frequencies, equal to $2\pi f_c$ and $2\pi f_o$, respectively, while $\theta_c$ and $\theta_o$ are the phase angles of the carrier and reference waveforms [13]. By convention, the phase angles $\theta_c$ and $\theta_o$ are set to zero for module $V_{1a}$ ($\theta_{c,V1a} = \theta_{o,V1a} = 0$). Use of other than zero values for $\theta_c$ and $\theta_o$ introduces a shift of $m\theta_c + n\theta_o$ to the phase of the $mn^{\text{th}}$ harmonic. Equivalently, the complex form of each current harmonic is multiplied by a rotating factor, $r$, given by

$$ r = e^{-j\left( m\theta_c + n\theta_o \right)} . \qquad \textbf{(4.2)} $$

This factor will be used below, to examine the effect of introducing a carrier phase shift between the inverters of an $N$-inverter system.

It is assumed that the $k^{\text{th}}$ inverter ($1 \le k \le N$) has its own carrier waveform, shifted by $\theta_{c,k}$ compared to the $1^{\text{st}}$ inverter ($\theta_{c,1} = 0$), and that this waveform is used to switch all its phase legs. Moreover, the reference waveform for module $V_{1a}$ of the $k^{\text{th}}$ inverter is assumed to be shifted by $\theta_{o,k}$ in relation to the respective waveform of the $1^{\text{st}}$ inverter ($\theta_{o,1} = 0$). The reference waveforms for the other modules are shifted accordingly. According to (4.2), the rotating factors, $r_k$, for the harmonics of the $k^{\text{th}}$ inverter will be

$$ r_k = e^{-j\left( m\theta_{c,k} + n\theta_{o,k} \right)} , \qquad \textbf{(4.3)} $$

hence the harmonic coefficients of the common dc-link capacitor current will be given by

$$ {}^{mn}i_C = {}^{mn}i_{C,1} \cdot \sum_k r_k , \qquad \textbf{(4.4)} $$

where $i_{C,1}$ stands for the capacitor current due to the $1^{\text{st}}$ inverter.

## 4.3 System cases - Results

Different multiple inverter systems configurations are examined in this section. The aim is to investigate whether the required dc-link capacitor size can be reduced by appropriately selecting the phases of the inverter reference and carrier waveforms. It is noted that the inverters are assumed to operate with the same fundamental frequency and modulation index, and with fixed relations between the phases of the reference-carrier waveforms.

Given that the capacitor voltage rating is primarily determined by the system specifications and therefore cannot be decreased, a reduction to the capacitor size can arise from a reduction of the capacitance or the ripple current requirements. As explained in Section 3.2, the required capacitance is mainly affected by the low-frequency capacitor current harmonics, while the ripple current rating can be approximately determined by the capacitor current rms value. With reference to the presented harmonic analysis, the low-frequency harmonics will be considered to be the baseband harmonics, while the capacitor rms current will be calculated using (4.5), below:

$$I_{C,rms} = \sqrt{\sum_m \sum_n \left\{ \frac{\left| {}^{mn}i_C \right|}{\sqrt{2}} \right\}^2} \quad . \tag{4.5}$$

Multiple inverter systems with two ($N$ = 2) and three ($N$ = 3) inverters will be examined. The inverter loads are assumed to be identical, having a power factor of 0.85, which is a typical value for motors (p. 101 in [60]). The phase shifts $\theta_{o,k}$ of the inverter reference waveforms are fixed to different values to represent different system configurations. Then, the carrier phase shift is varied, to determine the value that yields the optimum (minimum) capacitor rms current. The optimal current value is finally compared to the conventional practice of using the same carrier for all inverters.

The analytically derived current rms values are verified by simulations in MATLAB-Simulink. The simulated values are shown as points in the relative figures. Moreover, Figure 4.2 below presents an example of simulation waveforms for a system comprising two three-phase inverters (named Inv1 and Inv2) with a common reference waveform and carrier waveforms having a phase difference of 90 degrees.

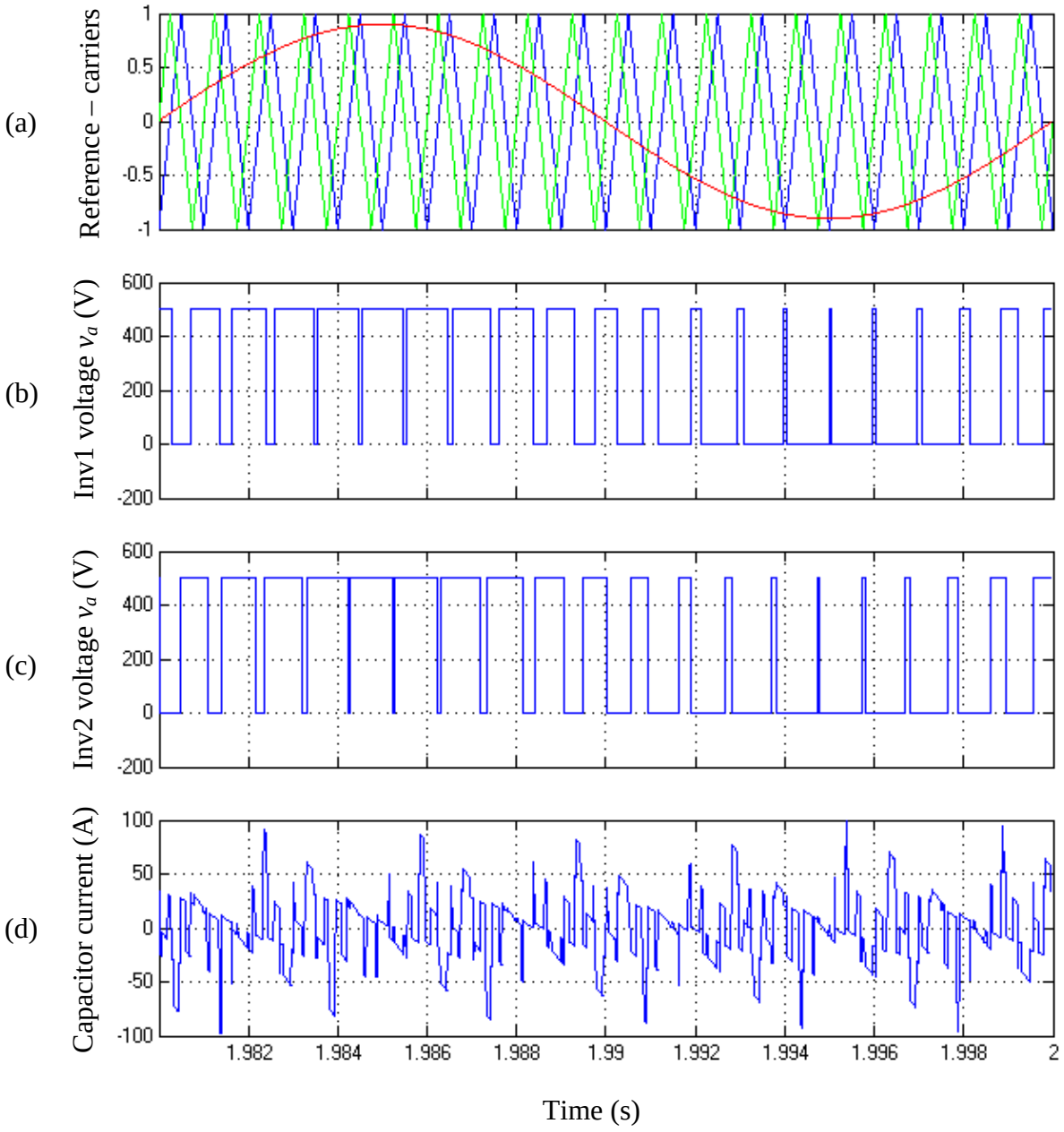


**Figure 4.2.** (a) Phase *a* reference – carrier waveforms for Inv1 and Inv2, (b) Phase voltage $v_a$ for Inv1, (c) Phase voltage $v_a$ for Inv2, and (d) Common capacitor current. The inverters are modulated with SPWM, assuming $V_{dc}$ = 500 V, $f$ = 50 Hz, and $f_s$ = 1 kHz.

### 4.3.1 Single-phase (CHB) inverter systems

The dc-link capacitor current of an SPWM-modulated H-Bridge inverter contains a baseband harmonic, described by (3.47). According to (4.4), the coefficient for this harmonic in a multiple inverter system will be given by

$$^{02}i_C = \frac{MI_{pk}}{j2} e^{j\phi} \cdot \sum_k e^{-j2\theta_{o,k}} \quad . \tag{4.6}$$

It can be noticed that the above expression is only dependent on the inverter reference phase shifts, $\theta_{o,k}$. Given that $\theta_{o,1}$ is defined to be zero, the baseband harmonic can be eliminated for $N$ = 2 if $\theta_{o,2}$ = 90 degrees, while for $N$ = 3 if $\theta_{o,2}$ = 60 degrees and $\theta_{o,3}$ = −60 (or 120 and −120) degrees.

These two cases of interest are examined with respect to their capacitor rms current, in Figures 4.3 and 4.4, respectively. The plots in Figures 4.3(a) and 4.4(a) illustrate how the capacitor rms current varies with $\theta_c$. If $I_{C,rms|\theta c}$ is the common capacitor rms current when the inverter carriers are shifted by $\theta_c$, then the variation is shown by plotting the ratio $I_{C,rms|\theta c}$ /$I_{C,rms|0}$ for different values of $\theta_c$. The optimal value for $\theta_c$, $\theta_{c,opt}$, can be seen to be equal to 90 and 60 degrees for $N$ = 2 and $N$ = 3, respectively. Adopting $\theta_{c,opt}$ as a carrier phase shift for each case, the resulting capacitor rms current, $I_{C,rms|\theta c,opt}$, is subsequently plotted against the inverters' modulation index in Figures 4.3(b) and 4.4(b), respectively, together with $I_{C,rms|0}$. The rms values are normalized w.r.t. the output rms current.

The ripple current rating of the inverter dc-link capacitors is determined by the maximum rms current that the capacitors may have to carry within the inverter operating range. For the two cases presented in Figures 4.3 and 4.4, the maximum (normalized) rms current values are given in Table 4.1.

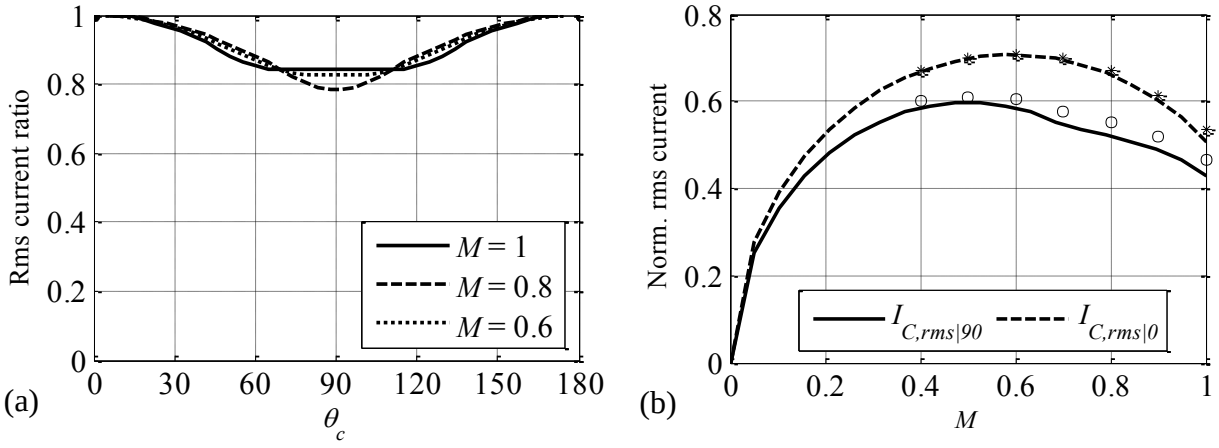


**Figure 4.3.** Capacitor rms current versus $\theta_c$ and $M$ for a single-phase inverter system with $N$ = 2, $\theta_o$ = 90 degrees.

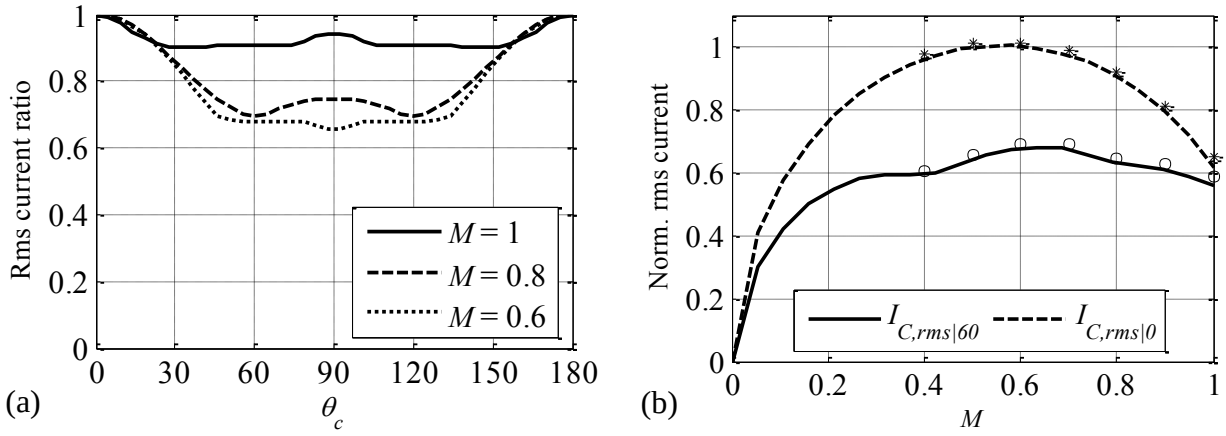


**Figure 4.4**. Capacitor rms current versus $\theta_c$ and $M$ for single-phase inverter system with $N$ = 3, $\theta_o$ = 60/120 degrees.

| $N$ | $\theta_o$ (degrees) | $\theta_{c,opt}$ (degrees) | max $I_{C,rms\|\theta c,opt}$ | max $I_{C,rms\|0}$ | Decr. (%) |
|---|---|---|---|---|---|
| 2 | 90 | 90 | 0.60 | 0.71 | 15.5 |
| 3 | 60/120 | 60/120 | 0.68 | 1.00 | 32.0 |

**Table 4.1.** Summary of results for the examined single-phase inverter systems.

The above analysis can be extended to systems incorporating inverters with other values of $\theta_o$. The carrier phase shift, $\theta_{c,opt}$, that minimizes the required ripple current rating of the dc-link capacitor can be determined for each value of $\theta_o$. It is assumed that $\theta_{o,2} = -\theta_{o,3} = \theta_o$ and $\theta_{c,2} = -\theta_{c,3} = \theta_c$. In the case of single-phase inverter systems, the study showed that $\theta_{c,opt}$ does not change with $\theta_o$: for $N$ = 2, $\theta_{c,opt}$ is 90 degrees and for $N$ = 3, 60/120 degrees. However, the maximum capacitor rms current varies significantly with $\theta_o$, as shown in Figure 4.5.

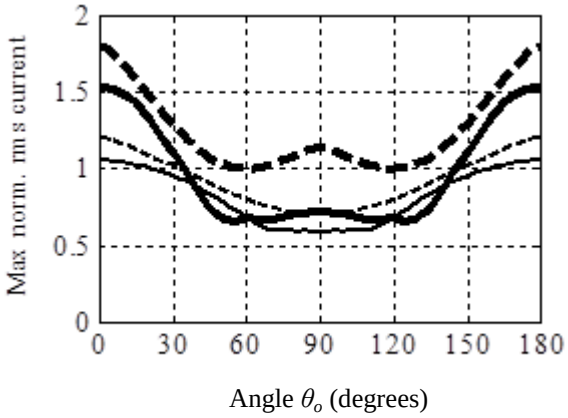


**Figure 4.5.** Maximum capacitor rms current $I_{C,rms|\theta c,opt}$ (continuous line) and $I_{C,rms|0}$ (dashed line) versus $\theta_o$, for single-phase inverter systems: Thin lines for $N$ = 2 and bold for $N$ = 3.

### 4.3.2 Three-phase (two-level) inverter systems

Assuming a linear and balanced load, the dc-link current of a three-phase, 2L inverter does not contain any baseband harmonics. Under the same assumption, no baseband harmonics appear in the dc-link of a multiple three-phase inverter system either. The case of $\theta_o$ = 30 degrees is examined as an example in Figures 4.6 and 4.7, for systems with $N$ = 2 and $N$ = 3, respectively. The value of $\theta_{c,opt}$ and the maximum capacitor rms current for each case are shown in Table 4.2. The results are the same for $\theta_o$ = 90 degrees.

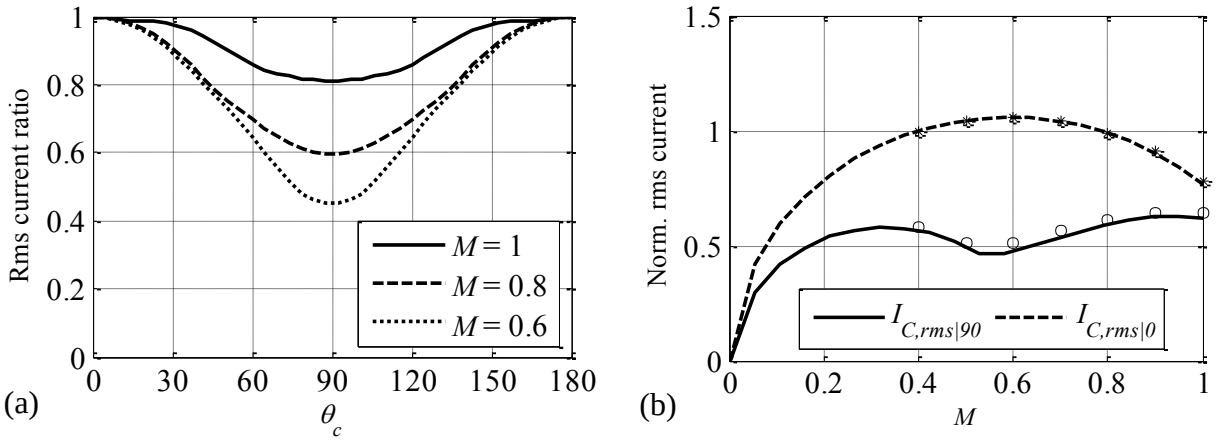


**Figure 4.6.** Capacitor rms current versus $\theta_c$ and $M$ for three-phase inverter system with $N$ = 2, $\theta_o$ = 30/90 degrees.

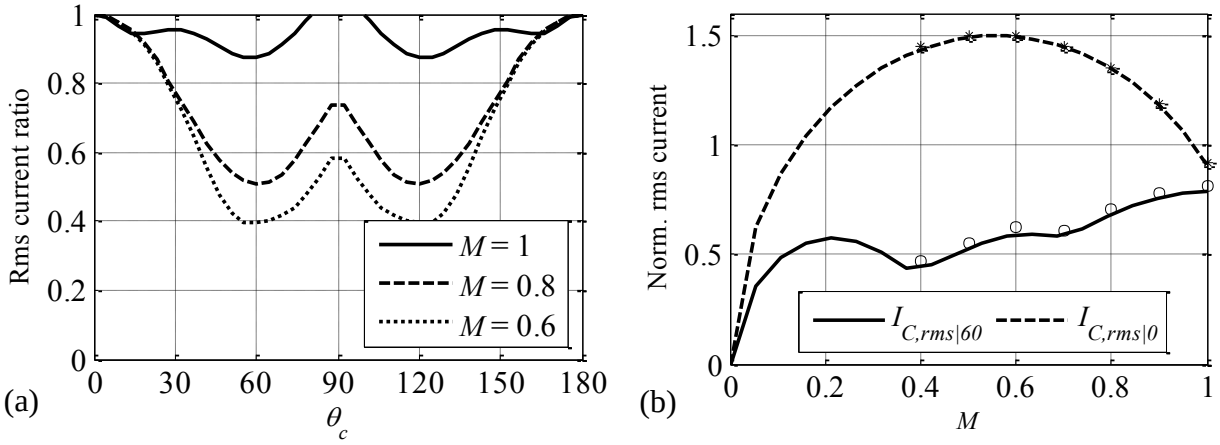


**Figure 4.7.** Capacitor rms current versus $\theta_c$ and $M$ for three-phase inverter system with $N$ = 3, $\theta_o$ = 30/90 degrees.

| $N$ | $\theta_o$ (degrees) | $\theta_{c,opt}$ (degrees) | max $I_{C,rms\|\theta c,opt}$ | max $I_{C,rms\|0}$ | Decr. (%) |
|---|---|---|---|---|---|
| 2 | 30/90 | 90 | 0.65 | 1.07 | 39.3 |
| 3 | 30/90 | 60 | 0.78 | 1.51 | 48.3 |

**Table 4.2.** Summary of results for the examined three-phase inverter systems.

Further investigation, regarding other values of $\theta_o$, yields different optimal phase shifts in the case of three-phase inverter systems. Figure 4.8 illustrates how $\theta_{c,opt}$ varies with $\theta_o$ and plots the corresponding values of the maximum capacitor rms current. According to Figures 4.5 and 4.8, a carrier phase shift of approximately 90 degrees is optimal, for both single and three-phase inverter systems with $N$ = 2. For systems with $N$ = 3, the optimal phase shift is 60 or 120 degrees. It is therefore indicated that these phase shifts affect certain carrier and sideband harmonics similarly to the single-phase inverter baseband harmonic. Other carrier and sideband harmonics may be increased when using the specific phase shifts. Nevertheless, the overall capacitor current rms value is decreased.

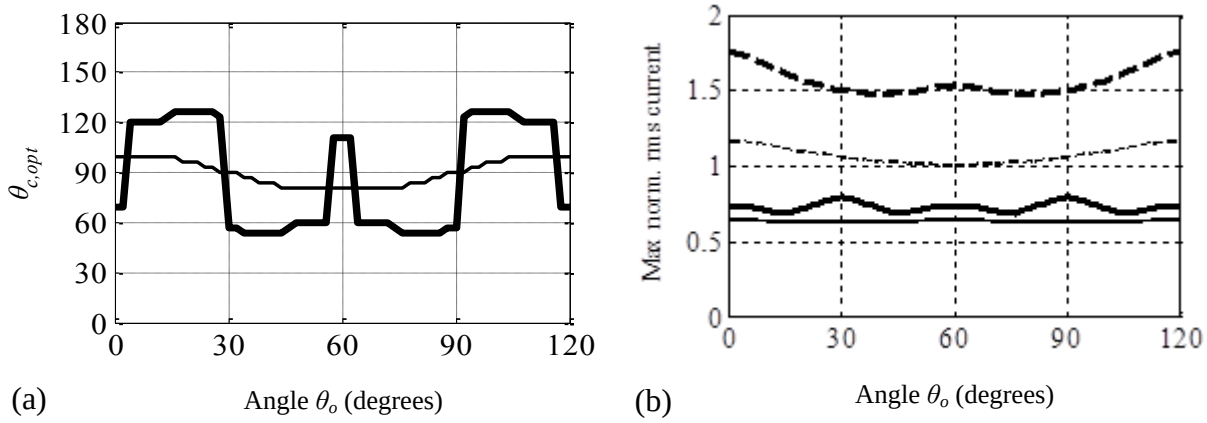


**Figure 4.8.** (a) Optimal carrier phase shift and (b) maximum capacitor rms current $I_{C,rms|\theta c,opt}$ (continuous line) and $I_{C,rms|0}$ (dashed line) versus $\theta_o$, for three-phase inverter systems: Thin lines for $N$ = 2 and bold for $N$ = 3.

## 4.4 Discussion

This section discusses a number of points regarding the applicability of the outcomes from this study. The first relates to the power factor of the inverter loads. A power factor of 0.85 was assumed in Section 4.3, and was used as a constant throughout the study. The capacitor

current of a multi-inverter system was therefore treated as a function of the inverter output current and modulation index, as well as of the angles $\theta_o$ and $\theta_c$. A preliminary investigation, however, indicated that the optimal phase shifts and current rms values are significantly different for low load power factors, below 0.5. The presented results are therefore valid when the inverter systems are used as motor drives, but have to be re-derived in case of low power factor applications.

A second comment refers to the effect of the inverter modulation strategy. SPWM was assumed for this study because analytical derivation of harmonic coefficients is intricate for other modulation strategies. For these strategies, the harmonic amplitudes can be calculated by numerical convolution of the output phase voltage and current spectra, according to [48]. The effect of using a modulation strategy other than SPWM on the presented results will depend on the degree of resemblance between their two capacitor current spectra.

Furthermore, it was assumed that $\theta_o$ is fixed, as it happens for example in a multi-phase machine, thus the carrier phase shift can be set to the corresponding $\theta_{c,opt}$. However, there are applications where $\theta_o$ varies with time. In such cases, the carrier phase shift should be controlled to the respective optimum value. On the other hand, if there is freedom to select the value of $\theta_o$, this should be done along with $\theta_{c,opt}$, to minimize the capacitor rms current according to Figures 4.5 and 4.8.

A last note refers to the physical layout of the studied multiple inverter systems. It is well known that a low-inductance connection, typically a flat bus bar, should be present between the dc-link capacitor and the switching modules of an inverter. A common dc-link capacitor was used in the examined multiple inverter systems, therefore assuming that all inverters can be laid physically close (in the same cabinet) to the capacitor and to each other.

## 4.5 Conclusions

This study investigated the effect of introducing a reference or carrier waveform phase shift to multiple inverter systems using a common dc-link capacitor. It was based on an analytical derivation of the capacitor current harmonics and the mathematical representation of introducing a reference/carrier phase shift. The study covered single- and three-phase systems, comprising two ($N$ = 2) or three ($N$ = 3) inverters. Regarding the single-phase

(CHB) inverter systems, it was shown that for $N = 2$ and $N = 3$, a decrement in the capacitor rms current of approximately 15% and 35%, respectively, can be achieved by selecting an appropriate carrier phase shift for each case. For three-phase, 2L inverter systems, the potential decrements were in the order of 40% and 50%, respectively. The results were verified by simulations using MATLAB-Simulink.

# Chapter 5

## Circuit for reducing devices voltage stress due to dc-link capacitor voltage ripple in an NPC inverter

## 5.1 Introduction

The previous chapters analysed the dc-link capacitor current in the examined converter topologies, as well as in multiple 2L and CHB converter systems. The second part of this Thesis, which focuses on the NPC topology and more specifically on its NP voltage ripple problem, begins with this chapter.

The NPC converter (Figure 5.1), invented three decades ago [49], is currently the most widely used topology in industrial medium-voltage applications [7]. Its advantages over the traditional 2L converter are expanding its range of application to low-voltage systems, such as PV (PV inverters) and low-voltage motor drives [61]. Major power module manufacturers have recently started producing 3L NPC modules to meet the increasing demand [10, 11]. Compared to the 2L topology, the NPC converter is built using modules with half the voltage rating, which decreases the total amount of switching losses [54]. The converter can therefore operate at higher switching frequencies and achieve an increased efficiency, while generating a lower-THD (3L) PWM phase voltage waveform. On the other hand, the NPC topology has the disadvantages of higher switch and driver count, as well as having to cope with dc-link capacitor imbalance.

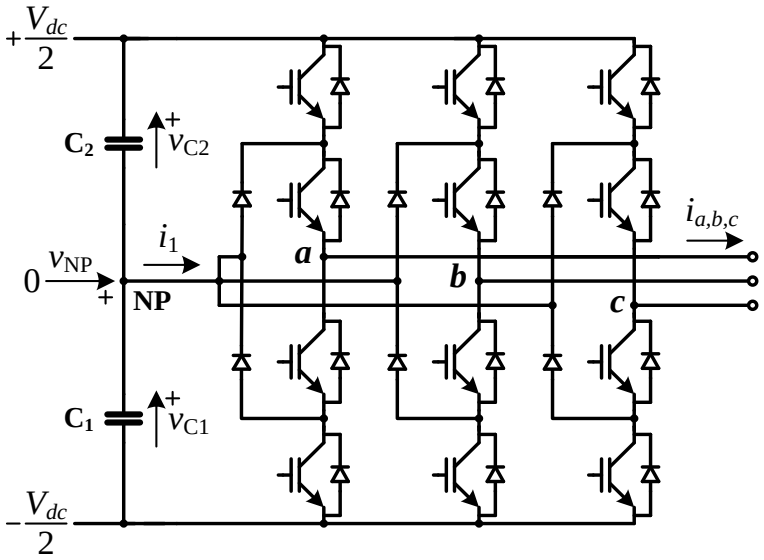


**Figure 5.1.** Three-level NPC converter, illustrating NP voltage and current.

As explained in Section 1.2.1, the voltages of the two dc-link capacitors, $v_{C1}$ and $v_{C2}$, respectively, should be kept approximately balanced, that is, equal to $V_{dc}/2$, each. Equivalently, the NP voltage, $v_{NP}$, defined as

$$v_{NP} = v_{C1} - V_{dc}/2 \quad \textbf{(5.1)}$$

in this study (Figure 5.1), is assumed to be kept approximately equal to zero. However, as explained in the same section, this may not be true in cases of transient imbalances or due to the presence of NP voltage ripple. With regards to the three approaches for dealing with NP voltage ripple, this chapter discusses a balancing circuit approach, while the following chapters focus on NPC converter modulation strategies.

## 5.2 Proposed circuit

This study proposes a circuit that is capable of reducing the amplitude of the NP voltage ripple seen by a 3L NPC inverter to half its maximum value. Its aim is to investigate the advantages that the circuit can offer, in comparison with the known methods for dealing with the NPC inverter capacitor balancing problem. The structure, operation and rating of the circuit are analysed in the following sections.

### 5.2.1 Structure

The proposed circuit, which will be referred to as Neutral Point Shifter (NPS), is illustrated in Figure 5.2. It consists of an H-Bridge ($V_{1s}$ – $V_{4s}$), connected across a capacitor, $C_s$. The main inverter circuit is modified so that the clamping diodes of the three phase legs (D5 and D6) are attached to the output of the NPS, shown as $NP_{inv}$ in the figure, instead of the NP of the dc-link.

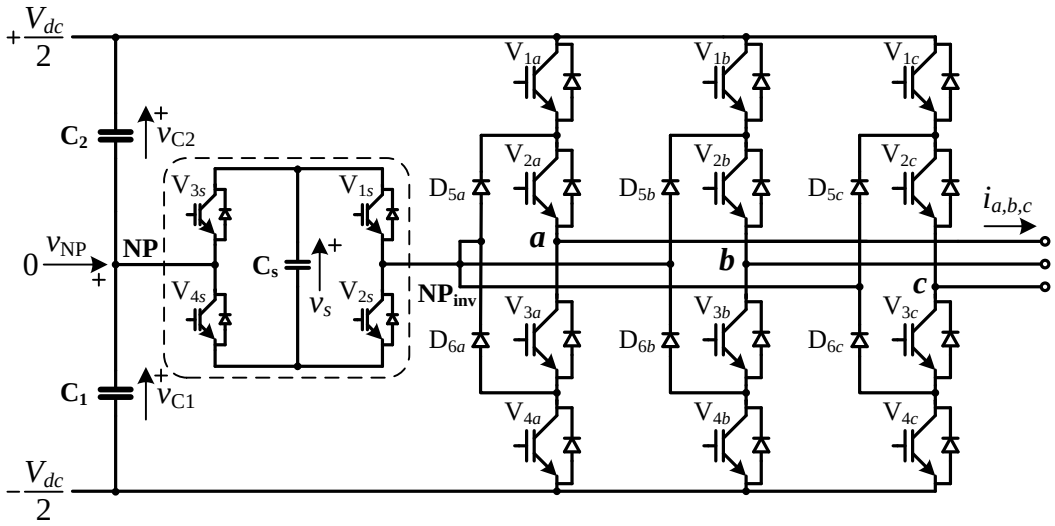


**Figure 5.2.** Three-level Neutral-Point-Clamped inverter with NPS circuit (encircled with dashed line)**.**

### 5.2.2 Operation

The NPS circuit is used to halve the amplitude of the NP voltage oscillations seen by the inverter, hence reduce the voltage stress on its IGBTs and diodes. Instead of $v_{NP}$, the NP voltage that the inverter sees when using the circuit, is $v_{NP,inv}$ (see Figure 5.2).

| $v_{NP}$ | NPS switching state | NPS modules ON | $v_{NP,inv}$ |
|---|---|---|---|
| $\lvert v_{NP}\rvert \le v_{NP,pk}/2$ | Zero | $V_{1s}$ and $V_{3s}$, or $V_{2s}$ and $V_{4s}$ | $v_{NP}$ |
| $v_{NP} < -v_{NP,pk}/2$ | Positive | $V_{1s}$ and $V_{4s}$ | $v_{NP} + v_s$ |
| $v_{NP} > v_{NP,pk}/2$ | Negative | $V_{2s}$ and $V_{3s}$ | $v_{NP} - v_s$ |

**Table 5.1.** NPS switching states.

According to Table 5.1, while the voltage $v_{NP}$ is within the limits of $\pm v_{NP,pk}/2$, the NPS stays at the zero state (output set to 0) and the inverter sees the actual NP voltage. During this state, the capacitor $C_s$ is not part of the current path and therefore its voltage, $v_s$, remains constant. The circuit is enabled as soon as $v_{NP}$ exceeds the above limits, shifting the NP voltage seen by the inverter in the appropriate direction, by $v_s$. While the NPS is at one of the two non zero states, the NP current also flows through the capacitor $C_s$, therefore affecting its

voltage. However, there is a key fact that ensures that when the circuit returns to the zero state, the capacitor voltage will regain its initial value: The NPS switches to a non zero state when the voltage $|v_{NP}|$ exceeds the critical value of $v_{NP,pk}/2$, and switches back to the zero state when $|v_{NP}|$ falls under this same value. The overall charge taken from the NP between these two instants is zero, because the initial and final values of $v_{NP}$ are equal. In addition, the NPS remains at the same non zero state during this time interval. Thus, the capacitor $C_s$ carries the instantaneous NP current, and its overall charge variation is also zero. As a result, $v_s$ returns to the same value, $v_{s0}$, at the end of each NPS switching cycle.

Two principles are followed for the NPS design, to ensure that during its operation, $v_{NP,inv}$ does not exceed the limits of $\pm v_{NP,pk}/2$: A) $v_{s0}$, the voltage of $C_s$ during the zero states, is set to $v_{NP,pk}$, and B) $C_s$ is selected to have twice the capacitance ($2C$) of the dc-link capacitors $C_1$, $C_2$. The operation of the circuit is illustrated above, using a simulation example of an NPC inverter with an NP voltage ripple of 200 V.

Figure 5.3 plots the values of $v_s$, $v_{NP}$ and $v_{NP,inv}$ for a third of the fundamental period, $T$. The peak NP voltage variation is 200 V, thus $v_{s0}$ is set to this value, as well. The NPS stays at the zero state until $v_{NP}$ reaches $v_{NP,pk}/2$ or $-v_{NP,pk}/2$. The voltage $v_{NP,inv}$ is equal to $v_{NP}$ during the zero state, while $v_s$ remains equal to $v_{s0}$. Then, the circuit switches to the negative or positive state, which shifts $v_{NP,inv}$ to the opposite extreme, $-v_{NP,pk}/2$ or $v_{NP,pk}/2$, respectively. As explained below, the limits of $\pm v_{NP,pk}/2$ for $v_{NP,inv}$ are not exceeded during these states, either. The capacitors $C_1$ and $C_2$, as seen from the NP, are connected in parallel [51]. Thus, the capacitance seen from the NP is $2C$. In addition, during the positive or negative NPS state, the capacitor $C_s$ is connected between NP and $NP_{inv}$. The capacitance of $C_s$ is also selected to be $2C$, thus the series connection of $C_1//C_2$ with $C_s$ gives the capacitance seen from $NP_{inv}$ as

$$\frac{2C \cdot 2C}{2C + 2C} = C \ . \qquad \textbf{(5.2)}$$

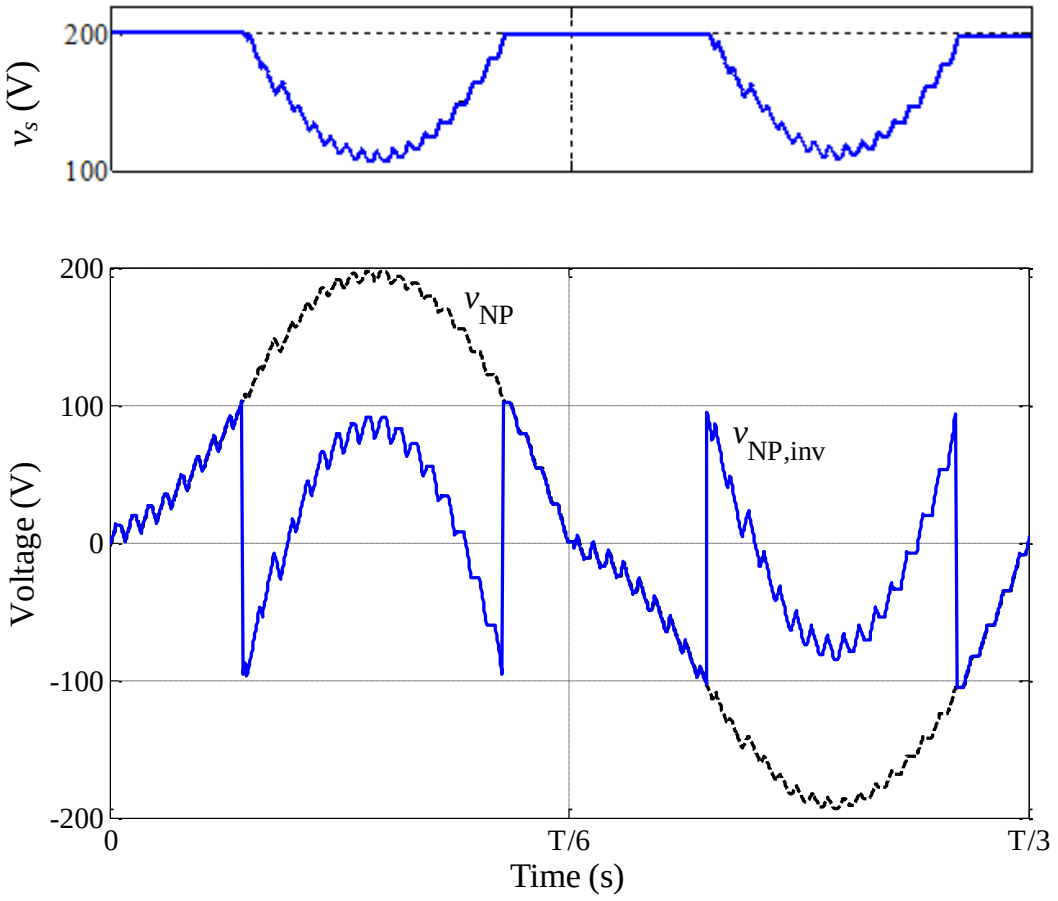


**Figure 5.3.** Simulation result illustrating voltages $v_s$, $v_{NP}$ and $v_{NP,inv}$, during a period of NP voltage oscillations, for an NPC inverter using the NPS circuit (Appendix A.4). The amplitude of NP voltage ripple seen by the inverter is decreased from 200 to 100 V.

Each variation in $v_{NP}$ during a non zero state is therefore doubled for $v_{NP,inv}$. The maximum variation of $v_{NP}$ is $v_{NP,pk}/2$ during a negative state of the NPS, since $v_{NP}$ increases from $v_{NP,pk}/2$ to $v_{NP,pk}$ (from 100 V to 200 V in Figure 5.3). At the same time, $v_{NP,inv}$ increases from $-v_{NP,pk}/2$ to $v_{NP,pk}/2$ (from –100 V to 100 V). Similarly, during a positive state of the NPS, the maximum variation of $v_{NP}$ is $-v_{NP,pk}/2$, since $v_{NP}$ decreases from $-v_{NP,pk}/2$ to $-v_{NP,pk}$ (from –100 V to –200 V), while $v_{NP,inv}$ decreases from $v_{NP,pk}/2$ to $-v_{NP,pk}/2$ (from 100 V to –100 V). Consequently, the value of $v_{NP,inv}$ does not exceed the limit of $\pm v_{NP,pk}/2$ (±100 V) at any time.

### 5.2.3 Rating

According to Section 5.2.2, the capacitance of the NPS capacitor $C_s$ should be equal to twice the capacitance of each of the inverter dc-link capacitors $C_1$ and $C_2$. However, the voltage $v_s$ across the capacitor does not exceed the value of $v_{s0}$, which is much lower compared to the dc-link capacitor voltage. The affordable amplitude of NP voltage ripple ($v_{NP,pk}$) is normally a small percentage, $p$, of $V_{dc}/2$, with $p$ ranging from 5% to 15%. Thus, given that $v_{s0}$ is set to $v_{NP,pk}$, the voltage rating of $C_s$ only needs to be a small fraction of the rating for $C_1$ and $C_2$.

The same principle applies to the voltage rating of the NPS circuit's IGBT-diode modules. Although the main NPC inverter's modules are rated to operate at a voltage equal to $V_{dc}/2$, the four modules of the NPS H-Bridge are connected across the capacitor $C_s$ and have to be rated according to its voltage. Thus, these modules can have a percentage $p$ of the main module rating.

The current rating of the NPS components depends on the current flowing to the inverter NP. The expression for the rms value of the NP current, $I_{NP,rms}$, is derived in Appendix A.2. The ratio $r_I$ of $I_{NP,rms}$ over the rms output current, $I_o$, is plotted in Figure 5.4, below. It can be observed that $r_I$ is lower than 1 for the region of modulation indices where the inverter practically operates ($M > 0.8$). The ratio $r_I$ can exceed 1 in case that the inverter supplies a high power factor load at a low modulation index. However, according to [62], the NP voltage oscillations either do not appear or have low amplitude under these conditions, causing the NPS to mainly remain at the zero state. Given that the capacitor $C_s$ does not carry the NP current while the circuit is at the zero state, it is safe to select the current rating of $C_s$ based on $I_o$ ($r_I = 1$). The same or lower rms value can be used for selecting the current rating of the NPS IGBT-diode modules. This is because the current rating is dependent on the affordable junction temperature, and therefore on the total, switching and conduction losses that occur in the module. The circuit switches at a LF $f_{NPS} = 3f$, (only 150 Hz for a 50 Hz inverter output), under a low voltage $v_s$, and therefore has very limited switching losses. Thus, its modules can be selected to have a lower current rating compared to the modules of the inverter.

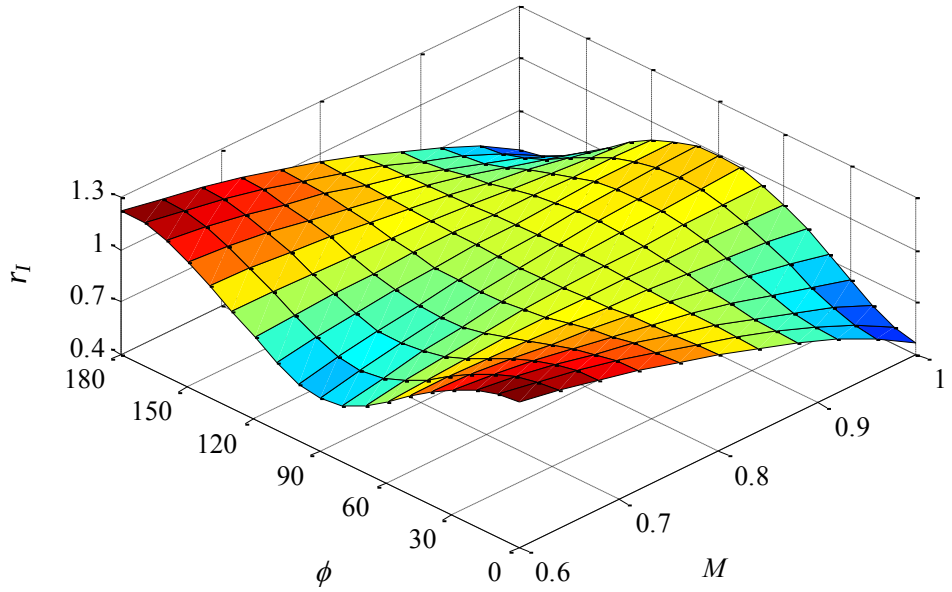


**Figure 5.4.** Ratio $r_I$ of NP ($I_{NP,rms}$) over output ($I_o$) rms current for the range of $M$ and $\phi$ where NP voltage ripple can be generated.

## 5.3 Comparison with other solutions

In this section, the NPS circuit will be compared to existing alternatives for coping with the NPC inverter capacitor balancing problem. An example of an NPC inverter operating according to the parameters presented in Table 5.2 will be used for the comparison.

| Parameter | Symbol | Value |
|---|---|---|
| DC-link voltage | $V_{dc}$ | 3.6 kV |
| Max rms output current | $I_o$ | 230 A |
| Fundamental frequency | $f$ | 50 Hz |
| Switching frequency | $f_s$ | 8 kHz |
| Load power angle / factor | $\phi$ / $PF$ | 35 degrees / 0.82 |
| Max amplitude of NP voltage oscillations | $v_{NP,pk}$ | 90 V |

**Table 5.2.** Example operating parameters for the NPC inverter.

A 3.6 kV dc-link is assumed, thus each of the dc-link capacitors $C_1$ and $C_2$ should be voltage-rated at approximately 1.8 kV. Furthermore, the NPC inverter has to be built using 3.3 kV IGBT-diode modules, which have an operating voltage of 1.8 kV. The Infineon FZ800R33KF2C (3.3 kV / 800 A) modules were selected by means of the loss calculator for the NPC inverter, found in Appendix B.

On the other hand, according to Section 5.2.3, the capacitor $C_s$ can have a voltage rating between 90 and 270 V (corresponding to $p$ = 5% – 15%), thus the NPS H-Bridge can consist of 600 V modules with an operating voltage of 400 V. Lower voltage-rated IGBT-diode or MOSFET modules can be used alternatively. The FF400R06KE3 (600 V / 400 A) dual IGBT-diode modules were selected in this case, according to respective loss expressions (see Appendix B) and the NP rms current values of Figure 5.4. It has to be noted that, owing to their negligible switching losses, the current rating of the modules for the NPS is significantly lower compared to the inverter modules.

### 5.3.1 Increment of capacitor size

In order to limit $v_{\mathrm{NP},pk}$ to the desired value, the capacitance, $C$, should be selected using

$$C = \frac{I_o}{v_{\mathrm{NP},pk} \cdot f} C_n \ , \tag{5.3}$$

where $C_n$ stands for a normalized capacitance value, plotted in Figure 5.5 for the NTV modulation strategy [51].

According to (5.3) and Figure 5.5, for unity modulation index ($M$ = 1), the capacitance required to limit $v_{\mathrm{NP},pk}$ to 90 V, is 991 μF. Two dc-link capacitors or capacitor banks, rated at 1.8 kV and 1 mF are therefore needed to fulfil this constraint. Alternatively, if the NPS circuit is in place, the capacitance can be decreased to 500 μF. In the case of capacitor banks, this would practically correspond to halving the number of capacitors in the dc-link, at the expense of introducing the NPS circuit's components.

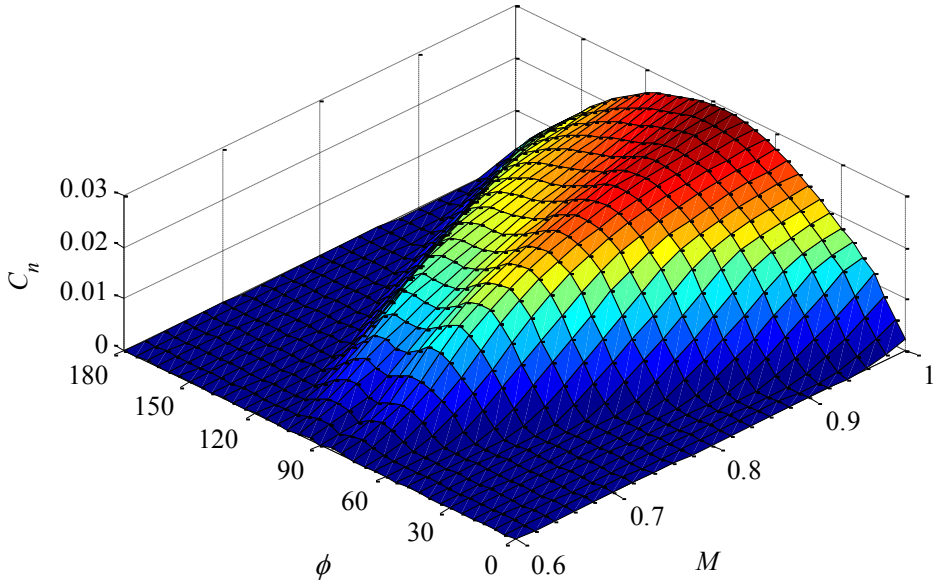


**Figure 5.5.** Normalized capacitance ($C_n$) required for the dc-link capacitors of an NPC inverter modulated with the NTV strategy **[51]**.

### 5.3.2 Increment of switching frequency

Non NV modulation strategies that can eliminate NP voltage ripple cause an increment of approximately 33% in the switching losses of the NPC inverter. According to the loss calculator (Appendix B), the 33% of the switching losses for the example NPC inverter of Table 5.2 amounts to 5.8 kW. The losses of the NPS circuit, on the other hand, are lower than 650 W. The loss overhead can be a challenge for the inverter cooling system. The system will have to be resized to handle them, while there are cases that they cannot be afforded by the inverter modules. The use of the NPS circuit removes these constraints, since its losses are significantly lower and are not internal to the inverter modules.

### 5.3.3 Balancing circuits

Capacitor balancing circuits for the NPC inverter have been proposed in [29, 30]. Unlike the NPS, these circuits are built using high-voltage IGBTs-diode modules and passive components (inductors) that are bulky and add to the cost of the system. They operate as charge pumps, transferring charge between the two dc-link capacitors. They are therefore

more effective in bringing the capacitors back to balance after transient imbalances, rather than coping with NP voltage oscillations.

On the other hand, the NPS circuit has the disadvantage of not decreasing the voltage stress on dc-link capacitors, as other balancing circuits do. This is because the circuit decreases the NP voltage ripple seen by the inverter without affecting the NP current, nor the NP voltage ripple and the value of $v_{\mathrm{NP},pk}$. Furthermore, the circuit's capacitor needs to be pre-charged to the level of $v_{\mathrm{NP},pk}$, which can call for additional circuitry.

## 5.4 Conclusion

A circuit for reducing the voltage stress caused by the dc-link capacitor voltage ripple on a 3L NPC inverter was presented, and its structure, operation and rating were analysed. The circuit is capable of reducing the NP voltage ripple seen by the inverter to half its maximum value. Unlike other circuits proposed in the literature, it is based on low-voltage components, which have smaller size and cost.

In relation to the conventional solution of over-sizing the inverter dc-link capacitors, the use of the circuit may be advantageous, depending on the cost of the capacitors in comparison to that of the circuit components. This is likely to be the case when the restriction on the NP voltage variation becomes stricter, since the voltage rating of the circuit components decreases accordingly.

The circuit does not eliminate the NP ripple as certain non NV modulation strategies do, yet avoids the increment of the inverter switching frequency that these strategies call for. It therefore provides an alternative in cases that this frequency increment is not permissible by the inverter's IGBT-diode modules. Even if the increased losses can be accepted by the modules, the cost of an over-sized inverter cooling system may be comparable to the cost of the circuit. Moreover, use of the circuit in conjunction with a capacitor-imbalance-compensating modulation strategy [28, 31] can result in operation of the inverter within the acceptable limits of NP ripple, and generation of undistorted output PWM waveforms.

# Chapter 6

## Nearest-Vector modulation strategies with minimum amplitude of low-frequency Neutral-Point voltage oscillations for the Neutral-Point-Clamped converter

## 6.1 Introduction

The previous chapter presented a circuit for decreasing the NP voltage ripple seen by the modules of an NPC converter. As explained in Section 5.3.3, however, the circuit does not decrease the actual NP voltage ripple, since it does not affect the NP current. The rest of the Thesis considers different types of modulation strategies for controlling the NP current and achieving this purpose.

This chapter proposes a new concept for the modulation of the NPC converter, according to which a family of modulation strategies can be created. These strategies are capable of generating the minimum possible NP voltage ripple, without affecting the converter's rated switching frequency or spectral performance (see Section 1.2.1). The following section places the proposed strategies in the context of the state-of-the-art modulation strategies for the NPC converter, providing further details for the contribution of this study.

## 6.2 NPC converter modulation strategies

A modulation strategy for the NPC converter should be capable of bringing the capacitors back to balance after a transient imbalance, and minimizing the NP voltage ripple during steady-state operation. Several strategies have been proposed to fulfil these requirements, using either a SV [32, 33, 51, 52, 63, 64, 65, 66] or a carrier-based [16, 21, 40, 41, 67, 68, 69,] implementation. The analysis presented in this study uses the terms of SVM. However, it encompasses carrier-based strategies, since there is a well-known equivalence between the two ways of implementation [17, 18, 41].

The SV diagram for a 3L NPC converter with balanced dc-link capacitors is illustrated in Figure 6.1. The triplets used as vector names denote the states (0 for $-V_{dc}/2$, 1 for $v_{NP}$, or 2 for $+V_{dc}/2$) of phase voltages *a*, *b*, and *c*, respectively. An SVM strategy selects a number of vectors, $\mathbf{V_1}$, $\mathbf{V_2}$, …, $\mathbf{V_n}$ and adjusts their duty cycles $d_1$, $d_2$, … $d_n$, respectively, according to the following equations to create the reference vector, $\mathbf{V_{REF}}$ (see Section 2.2.2):

$$\mathbf{V_{REF}} = d_1\mathbf{V_1} + d_2\mathbf{V_2} + ... + d_n\mathbf{V_n} \ , \tag{6.1}$$

$$d_1 + d_2 + ... + d_n = 1 \ . \tag{6.2}$$

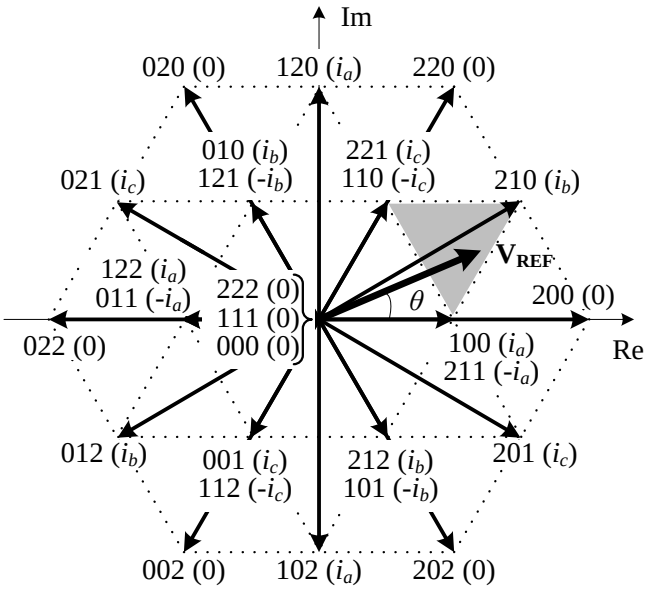


**Figure 6.1.** Space Vector diagram for a three-level NPC converter. NV strategies can only use the nearest vectors of $\mathbf{V_{REF}}$, located at the edges of the respective small triangle (here: 100, 211, 210, 221, and 110). The NP current corresponding to each vector is shown in parentheses.

Assuming that the converter does not operate in the over-modulation region, then the reference vector falls in one of the small triangles defined by the dashed lines. The vectors at the vertices of this triangle form a set that can be used according to (6.1) and (6.2), to create $\mathbf{V_{REF}}$. For a given $\mathbf{V_{REF}}$, these are also the "nearest vectors" (NVs) on the SV plane. In Figure 6.1, for example, $\mathbf{V_{REF}}$ falls in the shaded triangle, so the NVs are: 100, 211, 210, 221, and 110.

The modulation strategies for the NPC converter can then be divided into two categories. A strategy can be characterized as Nearest-Vector (NV) strategy if, in order to form the reference vector, it is only allowed to select among the respective NVs [4]. Otherwise, if it has the freedom to use additional vectors, it can be characterized as non Nearest-Vector (non NV) strategy. Examples of NV strategies are the Nearest-Three-Vector (NTV) and the Symmetric modulation strategies, described in [51], as well as the strategies described in [16, 40, 41, 67, 68], whereas examples of non NV strategies are the $NTV^2$ modulation [33] and others [21, 32, 66]. At this point, it can be noted that the well-known NTV strategy is simply a member of the family of NV strategies, which has the additional restriction of using only three of the NVs during each switching cycle [51].

As shown in [62], NV strategies can only eliminate the NP voltage ripple for a certain range of values of load power angle, $\phi$, and converter modulation index, $m$. These values define a zero-ripple region on the $\phi - m$ plane. When the converter operates outside this region, low-frequency voltage ripple appears at the NP. Non NV strategies have the advantage of achieving NP voltage ripple elimination throughout the converter operating range (i.e. for all values of $\phi$ and $m$). Nevertheless, the use of non nearest vectors introduces additional switching steps to the NPC converter, which increase its effective switching frequency. The effective switching frequency, $f_{s,eff}$, can be defined in addition to the converter's switching frequency, $f_s$ (which determines the duration, $T_s$, of the switching cycle), and be used in relation to switching losses:

$$f_{s,eff} = f_s \cdot \frac{\text{average no. of switching steps per } T_s}{6} \ . \qquad \textbf{(6.3)}$$

Conventionally, when the converter is modulated by a continuous carrier-based strategy, each of its three legs switches exactly twice (rising-falling or vice-versa) during every switching period. Hence, six switching steps take place in total during $T_s$, and therefore $f_{s,eff} = f_s$. By appropriately defining their switching sequences, NV strategies can also operate with an average of six switching steps per switching cycle, and thus achieve the above value of $f_{s,eff}$. Furthermore, fewer steps per cycle, and thus lower effective switching frequencies can be achieved by NV (SVM) strategies that correspond to discontinuous carrier-based strategies, which, however, produce lower-quality output voltage waveforms [41, 51]. In non NV strategies, on the other hand, two more switching steps are added per cycle, therefore $f_{s,eff}$ rises to $4f_s/3$ [32, 33]. This 33.3% increase has a notable effect on the converter switching losses, which is the main drawback of non NV strategies. Additionally, during each switching period, non nearest vectors cause one of the converter legs to switch between $+V_{dc}/2$, (possibly) $v_{NP}$, and $-V_{dc}/2$. This generates phase voltage pulses similar to those of a 2L converter, therefore distorting the standard three-level PWM phase voltage waveform and increasing its harmonic distortion (WTHD) [21, 32, 33, 52, 66].

Both NV and non NV strategies are used in practice for the modulation of the 3L NPC converter, at the expense of NP voltage ripple, or increased switching losses and output voltage WTHD, respectively. This trade-off has also lead to the creation of hybrid strategies, which operate as combinations of NV and non NV strategies, and will be discussed in

Chapter 7. Nevertheless, increased cooling and filtering requirements, as well as decreased converter efficiency still arise from the use of hybrid (due to the participation of non NV) strategies. NV strategies that avoid these disadvantages while abiding by the tolerable voltage limits would therefore be desirable.

This work continues in Section 6.3 with an analytical derivation of a lower boundary (approximately equivalent to a minimum) for the NP voltage ripple that can be achieved by an NV strategy. In Section 6.4, it describes the proposed concept for the operation of NV strategies, which provides the capability of achieving this minimum. Then, in Section 6.5, it examines the performance of the NV strategies created according to this concept, showing that they can decrease the NP voltage ripple of existing NV strategies by up to 50%, depending on the NPC converter's operating point on the $\phi$ - $m$ plane. Section 6.6 verifies the results by simulations in MATLAB-Simulink, focusing on the operating region of motor drives. The practical significance and applicability of the whole approach are finally discussed in Section 6.7.

## 6.3 Minimum NP ripple achievable by NV strategies

The SV diagram for a 3L converter can be divided into six 60-degree sextants, for voltage reference angle, $\theta$ = (0, 60) degrees, (60, 120) degrees, etc. In each sextant, there are two long vectors (**L0** and **L1**), one medium vector (**M**), four small vectors (**S0**$_1$, **S0**$_2$, **S1**$_1$, and **S1**$_2$) and three zero vectors (**Z**$_1$, **Z**$_2$, and **Z**$_3$), which are arranged as shown in Figure 6.2.

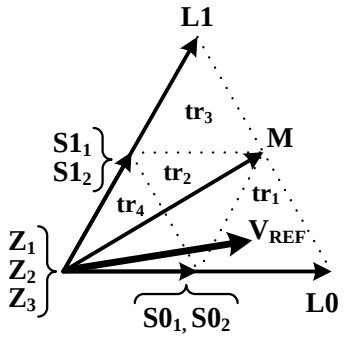


**Figure 6.2.** Space Vectors and triangles $tr_1$ – $tr_4$, in one sextant of a three-level converter. By convention, **S0**$_1$ and **S1**$_1$ will stand for positive (i.e. corresponding to $i_a$, $i_b$ or $i_c$), whereas **S0**$_2$ and **S1**$_2$ for negative small vectors.

The operation of an NV modulation strategy is summarized in the following steps, which are repeated in each switching cycle:

Step 1 – Determination of NVs: According to $\mathbf{V_{REF}}$ (see Figure 6.1).

Step 2 – Calculation of duty cycles: The duty cycles of the NVs are derived from (6.1), (6.2). However, since the two small vectors of each pair share the same position on the SV plane, solution of the above equations gives the duty cycles $d_{S0}$ and $d_{S1}$ as totals that can be distributed among $\mathbf{S0_1}$ - $\mathbf{S0_2}$, and $\mathbf{S1_1}$ - $\mathbf{S1_2}$, respectively (see Step 3 below). Similarly, the duty cycle for zero vectors, $d_Z$, is calculated as a total that can be distributed among vectors $\mathbf{Z_1}$, $\mathbf{Z_2}$ and $\mathbf{Z_3}$.

Step 3 – Distribution of duty cycles: $d_{S0}$ and $d_{S1}$ are distributed among the two vectors of the respective pairs, according to a criterion that aims to minimize the NP voltage ripple. Additionally, NV strategies commonly impose a number of constraints on this distribution (switching constraints), to reduce the converter effective switching frequency. Switching constraints also determine the distribution of $d_Z$ among the three zero vectors.

Step 4 – Selection of switching sequence: Each NV strategy has a predefined set of switching sequences, formed in accordance with the strategy's switching constraints. Depending on the results from the previous steps, one of these sequences is selected to successively activate the vectors according to the assigned duty cycles.

The following analysis is based on these four steps, to derive a lower boundary for the NP voltage ripple that can be achieved by an NV strategy.

### 6.3.1 Locally averaged NP current

Let us assume a 3L NPC converter operating at a steady-state, having a balanced set of sinusoidal output currents with rms value $I_o$, which *lead* the phase voltages by the power angle, $\phi$. The converter is modulated with an NV strategy at a modulation index, $m$. The reference frequency is $f$, while the switching frequency is $f_s$. The dc-link voltage is $V_{dc}$ and the capacitors $C_1$ and $C_2$ have a capacitance $C$, each.

The NP voltage ripple that appears at the dc-link is generated by the NP current, $i_1$, shown in Figure 5.1. Each of the Space Vectors in Figure 6.1 can be related to a specific NP current,

shown in parentheses. This current is equal to the sum of the currents of the phases that are at state "1", since these phases are connected to the NP. For example, the NP current corresponding to vector 110 is $-i_c$, because $i_a + i_b = -i_c$. The function $\mathrm{I_{NP}}(\mathbf{V})$ will be used further on to denote the value of the NP current that corresponds to vector **V**.

It can be observed from Figure 6.1 that only medium and small vectors produce a non zero NP current. If $i_\mathrm{M}$ is the locally averaged (i.e. the average during a switching period) current that is taken from the NP due to a medium vector, **M** (see Figure 6.2), then

$$i_\mathrm{M} = d_\mathrm{M}\, \mathrm{I_{NP}}(\mathbf{M}) \ , \tag{6.4}$$

where $d_\mathrm{M}$ is the duty cycle of the medium vector. The value of $i_\mathrm{M}$ is a function of angle $\theta$. Since the selection and duty cycles of medium vectors are solely determined by (6.1), (6.2), the waveform of $i_\mathrm{M}$ is the same for any NV modulation strategy.

On the other hand, if $i_\mathrm{S}$ is the locally averaged NP current that can be taken from the NP due to small vectors, then $i_\mathrm{S}$ depends on the distribution of $d_{\mathrm{S}0}$ and $d_{\mathrm{S}1}$ among the small vectors of the respective pairs. This is because the two small vectors of each pair produce opposite values of NP current (Figure 6.1). Two distribution factors, $x_{\mathrm{S}0}$ and $x_{\mathrm{S}1}$ ($x_{\mathrm{S}0}$, $x_{\mathrm{S}1} \in [-1, 1]$), can be defined for the duty cycles of small vectors. The duty cycles of small vectors $\mathbf{S0_1}$, $\mathbf{S0_2}$, $\mathbf{S1_1}$ and $\mathbf{S1_2}$ (see Figure 6.2), are then given by

$$d_{\mathrm{S}0,1} = \frac{1+x_{\mathrm{S}0}}{2}\, d_{\mathrm{S}0} \ , \quad d_{\mathrm{S}0,2} = \frac{1-x_{\mathrm{S}0}}{2}\, d_{\mathrm{S}0} \ , \tag{6.5), (6.6}$$

$$d_{\mathrm{S}1,1} = \frac{1+x_{\mathrm{S}1}}{2}\, d_{\mathrm{S}1} \ , \quad d_{\mathrm{S}1,2} = \frac{1-x_{\mathrm{S}1}}{2}\, d_{\mathrm{S}1} \ , \tag{6.7), (6.8}$$

while $i_\mathrm{S}$ is given by

$$i_\mathrm{S} = x_{\mathrm{S}0} d_{\mathrm{S}0}\, \mathrm{I_{NP}}(\mathbf{S0_1}) + x_{\mathrm{S}1} d_{\mathrm{S}1}\, \mathrm{I_{NP}}(\mathbf{S1_1}) \ . \tag{6.9}$$

For each value of $\theta$, $i_\mathrm{S}$ can reach a certain highest (maximum) value, $i_{\mathrm{S,hi}}$, as a result of setting

$$x_{\mathrm{S}0} = \mathrm{sign}\left(\mathrm{I_{NP}}(\mathbf{S0_1})\right) \text{ and } x_{\mathrm{S}1} = \mathrm{sign}\left(\mathrm{I_{NP}}(\mathbf{S1_1})\right) \ . \tag{6.10}$$

Use of

$$x_{S0} = -\text{sign}\left(I_{NP}\left(\mathbf{S0}_1\right)\right) \text{ and } x_{S1} = -\text{sign}\left(I_{NP}\left(\mathbf{S1}_1\right)\right) \quad \textbf{(6.11)}$$

results in $i_S$ taking a respective lowest (minimum) value, $i_{S,lo}$. In both of (6.10) and (6.11), ($x_{S0}$, $x_{S1}$) becomes equal to (−1, −1), (1, −1), (−1, 1) or (1, 1), assigning the whole $d_{S0}$ and $d_{S1}$ to a certain small vector from the respective pair, according to (6.5) – (6.8).

The locally averaged NP current, $i_{NP}$, is the sum of $i_M$ and $i_S$:

$$i_{NP} = i_M + i_S \ . \quad \textbf{(6.12)}$$

Given that $i_M$ cannot be controlled by an NV strategy, the highest and lowest values, $i_{NP,hi}$ and $i_{NP,lo}$, of $i_{NP}$ correspond to $i_{S,hi}$ and $i_{S,lo}$, respectively.

### 6.3.2 Effect of switching constraints

By adjusting the distribution factors of the small vectors, $i_{NP}$ can take any value between $i_{NP,lo}$ and $i_{NP,hi}$. It can be shown, however, that freedom in this adjustment can lead to increased effective switching frequency. The values of $x_{S0}$ and $x_{S1}$ are therefore normally restricted using sets of switching constraints, which differ among NV strategies.

| Triangle | $x_{S0}$ | $x_{S1}$ | Switching sequence | Steps |
|---|---|---|---|---|
| $tr_1$ | +1 | n/a | 100-200-210-200-100 | 4 |
| | −1 | n/a | 200-210-211-210-200 | 4 |
| $tr_2$ | +1 | +1 | 100-210-221-210-100 | 8 |
| | +1 | −1 | 100-110-210-110-100 | 4 |
| | −1 | +1 | 210-211-221-211-210 | 4 |
| | −1 | −1 | 110-210-211-210-110 | 4 |
| $tr_3$ | n/a | +1 | 210-220-221-220-210 | 4 |
| | n/a | −1 | 110-210-220-210-110 | 4 |
| $tr_4$ | +1 | +1 | 100-111-221-111-100 | 8 |
| | +1 | −1 | 100-110-111-110-100 | 4 |
| | −1 | +1 | 111-211-221-211-111 | 4 |
| | −1 | −1 | 110-111-211-111-110 | 4 |

**Table 6.1.** Duty cycle distribution factors and switching sequences for the NTV strategy **[51]**.

For example, in the case of the NTV strategy, $x_{S0}$ and $x_{S1}$ can only take the values of ±1. The switching sequences defined according to this restriction are shown in Table 6.1 [51]. The sequences are given for the 1st sextant, and $\mathbf{S0_1}$ and $\mathbf{S1_1}$ correspond to vectors 100 and 221, respectively (see Figures 6.1 and 6.2).

Most sequences require 4 (instead of 6) switching steps, therefore decreasing the effective switching frequency for the NTV strategy. In triangles $tr_2$ and $tr_4$, however, there are also sequences that incorporate 8 switching steps. These are available, so that $i_{NP}$ can always attain the values $i_{NP,lo}$ and $i_{NP,hi}$, by selecting $x_{S0}$ and $x_{S1}$ according to (6.10), (6.11).

Other NV strategies (for example, the Symmetric strategy in Appendix A.3) can forbid the 8-step sequences by imposing additional switching constraints in triangles $tr_2$ and $tr_4$. Then, $i_{NP,lo}$ and $i_{NP,hi}$ become unattainable for certain values of $\theta$ (which depend on $\phi$ and $m$). Given the set of switching constraints, *SC*, of such a strategy, then $i_{NP,hi|SC}$ and $i_{NP,lo|SC}$ can be defined as the highest and lowest values, respectively, of $i_{NP}$, that can be achieved while abiding by *SC*. It is noted here that the switching constraints of *SC* for triangles $tr_1$ and $tr_3$ are assumed to allow the values of ±1 for $x_{S0}$ and $x_{S1}$, as it happens in the case of the NTV strategy. This is an essential requirement if the strategy that uses *SC* wishes to have a control over the NP voltage. NV strategies that do not fulfil it, such as the SPWM or the SVM with equal duty cycle distribution among the two small vectors of each pair, have increased values of NP voltage ripple [62, 70].

Generally, the following inequality holds:

$$i_{NP,hi} \geq i_{NP,hi|SC} \geq i_{NP,lo|SC} \geq i_{NP,lo} \ . \qquad \textbf{(6.13)}$$

However, as the modulation index increases, $\mathbf{V_{REF}}$ spends a smaller fraction of the fundamental period in $tr_2$ and $tr_4$, where the additional switching constraints apply. For $m = 1$, this fraction is zero, thus $i_{NP,hi|SC}$ and $i_{NP,lo|SC}$ become equal to $i_{NP,hi}$ and $i_{NP,lo}$, respectively, during the entire cycle.

The analysis presented in the following sections assumes no switching constraints imposed on the duty cycle distribution factors, in order to derive the operational limits of the proposed concept. It can be adapted to a strategy that uses a given *SC*, if $i_{NP,hi}$ and $i_{NP,lo}$ are substituted by $i_{NP,hi|SC}$ and $i_{NP,lo|SC}$, respectively. It is important to note, however, that since

$i_{NP,hi|SC}$ and $i_{NP,lo|SC}$ approximate $i_{NP,hi}$ and $i_{NP,lo}$ when $m$ approaches 1, the presented results that refer to these values of $m$ can be used irrespective of $SC$.

### 6.3.3 Zero-ripple region

The NP voltage in the NPC inverter is determined by the integral of the NP current. Thus, $v_{NP}$ can be controlled to remain the same (at the end of each switching cycle) throughout the fundamental cycle, if $i_{NP}$ can become equal to zero for all values of $\theta$. Since $i_{NP}$ is restricted between $i_{NP,lo}$ and $i_{NP,hi}$, this is possible when

$$\left(i_{NP,lo} \le 0 \text{ and } i_{NP,hi} \ge 0\right) \quad \textbf{(6.14)}$$

holds for $\theta$ = (0, 360) degrees. Examination of this condition at different values of $\phi$ and $m$ gives the zero-ripple region for NV strategies, first presented in [62] and shown in Figure 6.6.

### 6.3.4 A lower boundary for the NP voltage ripple

Figure 6.3 plots $i_{NP,lo}$, $i_{NP,hi}$ and $i_M$, according to (6.4) and (6.9) – (6.12), during a fundamental cycle. A balanced set of sinusoidal output currents with rms value $I_o$ = 1 A is assumed which lag the phase voltages by 30 degrees ($\phi$ = −30 degrees), while $m$ is set to 0.9. The waveforms of $i_{NP,lo}$ and $i_{NP,hi}$ cross the zero axis, therefore (6.14) does not hold for certain values of $\theta$, and NP voltage ripple is expected to appear. The existence of voltage ripple cannot be avoided by any NV strategy, but its peak value depends on the use of $x_{S0}$ and $x_{S1}$.

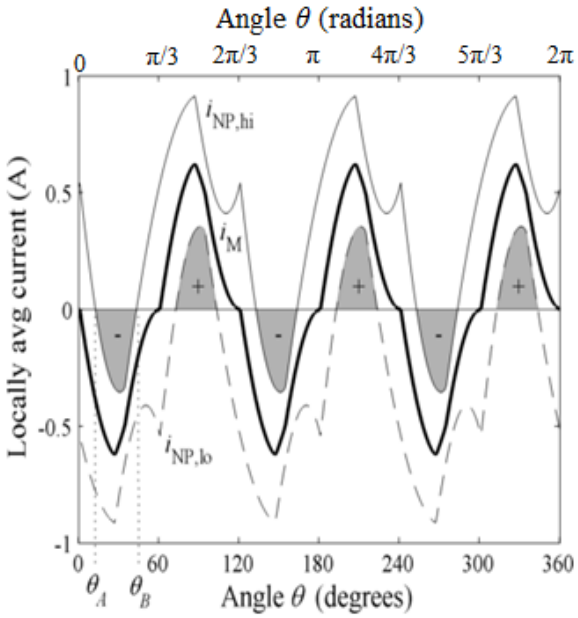


**Figure 6.3.** $i_{\mathrm{NP,lo}}$, $i_{\mathrm{NP,hi}}$ and $i_{\mathrm{M}}$ during a fundamental cycle, for $\phi = -30$ degrees and $m = 0.9$ ($I_o = 1$ A).

While (6.14) holds during the fundamental cycle, $x_{\mathrm{S0}}$ and $x_{\mathrm{S1}}$ can be adjusted to set $i_{\mathrm{NP}}$ to zero ($i_{\mathrm{S}} = -i_{\mathrm{M}}$). In this case, the small vectors fully compensate for the charge taken from the NP by the medium vectors, thus avoiding a change in the NP voltage. As soon as (6.14) ceases to hold, at an angle $\theta_A$, $i_{\mathrm{NP}}$ can no longer be set to zero, therefore charge starts to be taken from the NP. This carries on until an angle $\theta_B$, when (6.14) begins to hold again. Nevertheless, the charge $\Delta Q_{AB}$, taken from the NP during $[\theta_A, \theta_B]$ can be minimized if $i_{\mathrm{NP}}$ is adjusted to its – in absolute terms – minimum value, which is $i_{\mathrm{NP,hi}}$ for this interval:

$$\Delta Q_{AB,\min} = \frac{1}{2\pi f} \int_{\theta_A}^{\theta_B} i_{\mathrm{NP,hi}}\, d\theta \ . \qquad \textbf{(6.15)}$$

Since $i_{\mathrm{M}} < 0$ during $[\theta_A, \theta_B]$, the above adjustment ($i_{\mathrm{S}} = i_{\mathrm{S,hi}}$) corresponds to the small vectors providing the maximum possible degree of compensation against the medium vectors, while $\Delta Q_{AB,\min}$ corresponds to the minimum achievable uncompensated amount of charge. The integral term of (6.15) is equal to the area of the shaded region between points $A$ and $B$ in Figure 6.3, if $\theta$ is expressed in radians. The absolute value of $\Delta Q_{AB,\min}$ is inversely proportional to the reference frequency, while its sign is the same as the sign of $i_{\mathrm{M}}$.

Since the two dc-link capacitors, as seen from the NP, are connected in parallel [51], $\Delta Q_{AB,\min}$ causes an NP voltage variation, $\Delta V_{AB,\min}$, given by (6.16). The equation contains a negative sign, indicating that $v_{\mathrm{NP}}$ decreases (or increases) as a result of a positive (or negative) value of $\Delta Q_{AB,\min}$:

$$\Delta V_{AB,\min} = -\frac{\Delta Q_{AB,\min}}{2C} \quad . \tag{6.16}$$

The key fact is that no NV strategy can prevent $\Delta Q_{AB,\min}$ from leaving the NP. Thus, $\Delta V_{AB,\min}$ is a lower limit for the NP voltage variation that will occur during the interval [$\theta_A$, $\theta_B$]. However, if $\Delta V_{AB,\min}$ appears during an interval of the fundamental cycle, then the peak-peak NP voltage variation during the whole cycle cannot be lower than $|\Delta V_{AB,\min}|$. Consequently, $|\Delta V_{AB,\min}|$ is a lower boundary, $\Delta V_{\mathrm{NP},\min}$, for the peak-peak NP voltage ripple that can be generated by an NV modulation strategy.

The same analysis can be applied to all intervals of the fundamental cycle in which (6.14) does not hold (shaded in Figure 6.3). Those will be referred to as uncontrollable intervals (UIs), because during them the NP voltage is unavoidably driven by the uncompensated charge of the medium vectors. On the contrary, intervals in which (6.14) does hold, will be referred to as controllable intervals (CIs), since during them the small vectors can be used to keep the NP voltage constant, or control it to some extent. If $n$ uncontrollable intervals, $\mathrm{UI}_1$, $\mathrm{UI}_2$, … , $\mathrm{UI}_n$, appear during a fundamental cycle, having respective minimum NP voltage variations of $\Delta V_{\mathrm{UI1},\min}$, $\Delta V_{\mathrm{UI2},\min}$, … , $\Delta V_{\mathrm{UI}n,\min}$, then

$$\Delta V_{\mathrm{NP},\min} = \max\left\{\left|\Delta V_{\mathrm{UI}k,\min}\right|\right\}, k = 1 \ldots n \quad . \tag{6.17}$$

As dictated by (6.15) and (6.16), $\Delta V_{\mathrm{NP},\min}$ is a function of $C$ and $f$, as well as $I_o$, $\phi$ and $m$, since the waveforms of $i_{\mathrm{NP,lo}}$ and $i_{\mathrm{NP,hi}}$ change with these parameters. For given values of the above, an NV strategy that achieves $\Delta V_{\mathrm{NP},\min}$ is optimal with respect to the NP voltage ripple. This lower boundary, on the other hand, may not be attainable in cases of successive UIs with same-sign NP voltage deviations, which will be discussed in Section 6.4.3.

## 6.4 Proposed Band-NV strategies

This section investigates the effect of the criterion used in Step 3 (see Section 6.3) for minimizing the NP voltage ripple.

### 6.4.1 Criterion used by conventional NV strategies

The two main objectives of an NPC converter modulation strategy in relation to the dc-link are the ability to bring the capacitors back to balance after transient imbalances and the minimization of the NP voltage ripple. The existing NV strategies try to achieve these objectives by decreasing any voltage imbalance that appears between the two dc-link capacitors. This is obtained by measuring the capacitor voltages and adjusting $x_{S0}$ and $x_{S1}$, so that $i_{NP}$ in (6.12) will charge (or discharge) the capacitor having less (or more) voltage, respectively [41, 51, 64, 70]. Equivalently, the criterion conventionally used by the NV strategies for achieving NP balancing can be stated as follows:

"Adjust $i_{NP}$ to drive $v_{NP}$ as close as possible to zero".

This criterion, which will be referred to as the conventional criterion, is suitable for bringing the capacitors back to balance after transient imbalances. Furthermore, it intuitively seems to lead to the minimum NP voltage ripple, too. However, a simple example based on the analysis of the previous section can prove that the latter is not actually true.

Continuing the example of Figure 6.3, Figure 6.4(a) illustrates how the NP voltage, $v_{NP,Conv}$, varies during a third of a fundamental cycle when the conventional criterion is used. The NP voltage deviates from zero during the two UIs, shown in Figure 6.3 and 6.4(b). The locally averaged NP current, $i_{NP,Conv}$, provides maximum compensation during these intervals, resulting in changes in NP voltage, of $\Delta V_{NP,min}$ and $-\Delta V_{NP,min}$, respectively. Moreover, $i_{NP,Conv}$ is adjusted according to the conventional criterion, to decrease $v_{NP,Conv}$ down to zero during the controllable intervals. As a consequence, the changes of $\pm\Delta V_{NP,min}$ begin from $v_{NP,Conv} = 0$, giving a peak-peak value of $2\Delta V_{NP,min}$ to the NP voltage ripple.

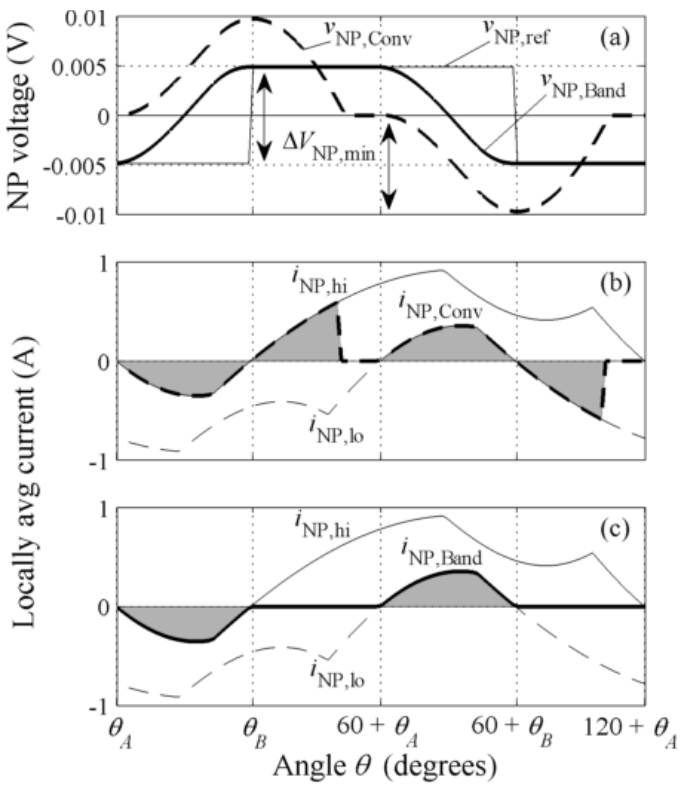


**Figure 6.4.** (a) $v_{NP,Conv}$, $v_{NP,Band}$ and $v_{NP,ref}$, (b) $i_{NP,Conv}$, $i_{NP,lo}$ and $i_{NP,hi}$, and (c) $i_{NP,Band}$, $i_{NP,lo}$ and $i_{NP,hi}$ during a third of a fundamental cycle, for $\phi = -30$ degrees and $m = 0.9$ ($I_o = 1$ A, $f = 1$ Hz, $C = 1$ F).

### 6.4.2 Proposed criterion

The above increase in the value of NP voltage ripple can be avoided by a different criterion, which relies on the following observation: The voltage deviations have the same amplitude, but their sign changes successively from positive to negative and vice versa ($\Delta V_{UI1} = -\Delta V_{UI2} = \Delta V_{NP,min}$). Therefore, the NP voltage could periodically be driven to zero, even if $i_{NP}$ was not used for this purpose. Instead, $i_{NP}$ can be used as follows:

- During UIs: Provide the maximum possible charge compensation against the medium vectors. Namely, adjust $x_{S0}$ and $x_{S1}$ to achieve $i_{NP} = i_{NP,lo}$ if $i_M > 0$, or $i_{NP} = i_{NP,hi}$ if $i_M < 0$. The resulting NP voltage change will be $-\Delta V_{NP,min}$ and $\Delta V_{NP,min}$, respectively.
- During controllable intervals: Adjust $i_{NP}$ to (drive and) keep $v_{NP}$ equal to $\Delta V_{NP,min}/2$, or $-\Delta V_{NP,min}/2$, if $i_M$ was negative, or positive, respectively, during the last uncontrollable interval.

The above can be achieved by periodically changing the NP reference voltage, $v_{NP,ref}$, as follows:

"Adjust $i_{NP}$ to drive $v_{NP}$ as close as possible to $v_{NP,ref}$, which changes to $\Delta V_{NP,min}/2$, or $-\Delta V_{NP,min}/2$, at the end of an uncontrollable interval where $i_M$ was negative, or positive, respectively".

This criterion will be referred to as the Band criterion because it restricts the NP voltage, $v_{NP,Band}$, within a band that is centered around zero and has a width of $\Delta V_{NP,min}$. The waveforms of $v_{NP,ref}$ and $v_{NP,Band}$ are illustrated in Figure 6.4(a). For this operating point, the peak-peak value of the NP voltage ripple is decreased to half. Nearest-Vector strategies that operate according to the Band criterion will be referred to as Band-NV strategies.

### 6.4.3 Regions of operation

The formulation of the Band criterion relied on the observation that the change in NP voltage is opposite for every two successive UIs. As shown below, this is true for the greatest part of the NPC converter's operating range, but not for the entire range (defined by $\phi$ and $m$). The $\phi - m$ plane can be divided in Regions, characterized by the number of UIs that appear per half cycle of $i_M$:

- Region 0: There are no UIs. $\Delta V_{NP,min}$ is equal to zero (zero-ripple region).
- Region 1: There is a single uncontrollable interval, $UI_1$, during each positive half cycle of $i_M$, with $\Delta V_{UI1} = -\Delta V_{NP,min} < 0$. The next uncontrollable interval, $UI_2$, appears in the negative half cycle of $i_M$, with $\Delta V_{UI2} = \Delta V_{NP,min} > 0$.
- Region 2: There are two UIs, $UI_1$ and $UI_2$ during each positive half cycle of $i_M$, with $\Delta V_{UI1} < 0$ and $\Delta V_{UI2} < 0$.

The example in Figure 6.3 belongs to Region 1. Figure 6.5(a) and 6.5(b) illustrate representative examples for Regions 0 and 2, respectively, while Figure 6.6 depicts the three Regions on the $\phi - m$ plane.

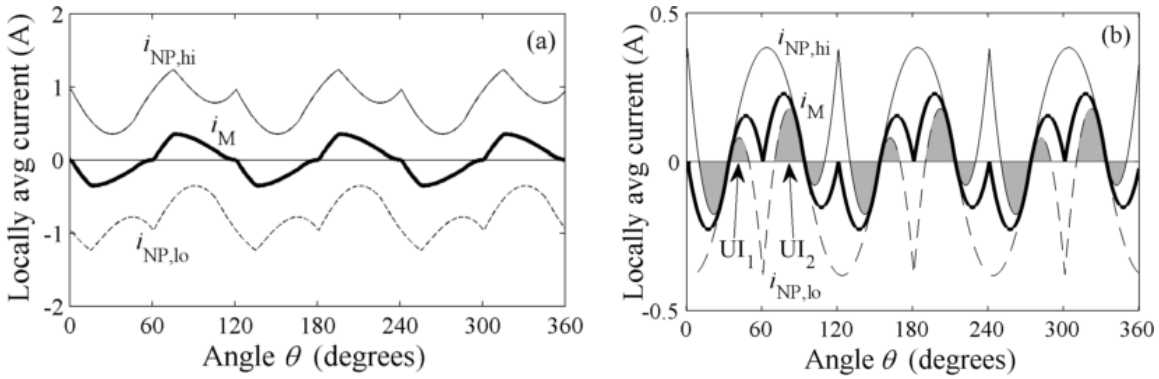


**Figure 6.5.** $i_{NP,lo}$, $i_{NP,hi}$ and $i_M$ during a fundamental cycle, for (a) $\phi = -30$ degrees, $m = 0.7$ (Region 0), and (b) $\phi = -3$ degrees, $m = 1$ (Region 2).

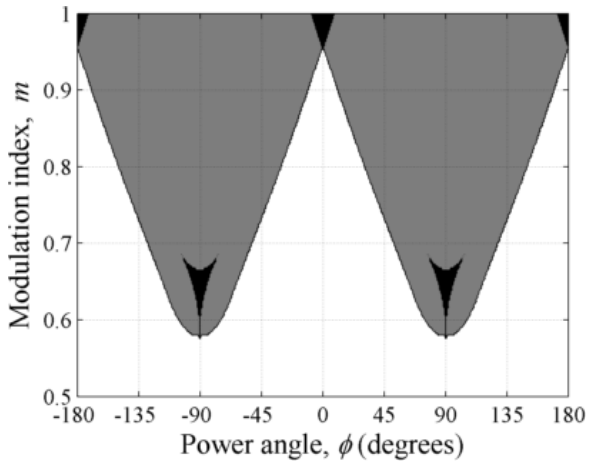


**Figure 6.6.** Regions of NPC converter operation: (White) Region 0, (Grey) Region 1, (Black) Region 2.

In Region 0, $v_{NP,ref}$ remains equal to zero (because $\Delta V_{NP,min}$ is zero) and the band criterion takes the form of the conventional criterion. Thus, in this region, a Band-NV strategy operates like a conventional one. In Region 1, $v_{NP,ref}$ keeps $v_{NP,Band}$ to its positive or negative extreme ($\pm\Delta V_{NP,min}/2$) during controllable intervals, knowing that during the following UIs the uncompensated charge will take it to the opposite extreme. This is not the case, however, in Region 2, where there are pairs of successive UIs with the same sign of uncompensated charge. The two intervals cause NP voltage deviations towards the same direction, and as a consequence a modified approach is required.

According to (6.17), a lower boundary for the peak-peak NP voltage ripple in Region 2 is given by

$$\Delta V_{\mathrm{NP,min}} = \max\left\{\left|\Delta V_{\mathrm{UI1,min}}\right|, \left|\Delta V_{\mathrm{UI2,min}}\right|\right\} \ . \qquad \textbf{(6.18)}$$

To achieve this value, the effect of $\Delta V_{\mathrm{UI1,min}}$ on the NP voltage should be partially (if $\Delta V_{\mathrm{UI1,min}} > \Delta V_{\mathrm{UI2,min}}$) or totally (if $\Delta V_{\mathrm{UI1,min}} \leq \Delta V_{\mathrm{UI2,min}}$) cancelled during the controllable interval $\mathrm{CI}_{1\text{-}2}$, found between $\mathrm{UI}_1$ and $\mathrm{UI}_2$. More precisely, during $\mathrm{CI}_{1\text{-}2}$, $v_{\mathrm{NP,Band}}$ should be driven to $\pm V_{\mathrm{CI1\text{-}2}}$, where

$$V_{\mathrm{CI1\text{-}2}} = \Delta V_{\mathrm{NP,min}} / 2 - \left|\Delta V_{\mathrm{UI2,min}}\right| \ . \qquad \textbf{(6.19)}$$

In this way, after the end of $\mathrm{UI}_2$, $v_{\mathrm{NP,Band}}$ will be equal to $\pm\Delta V_{\mathrm{NP,min}}/2$, similar to what happens in Region 1. The following, modified version of the Band criterion can be formed, to be used when the converter operates in Region 2:

"Adjust $i_{\mathrm{NP}}$ to drive $v_{\mathrm{NP}}$ as close as possible to $v_{\mathrm{NP,ref}}$, which changes to $V_{\mathrm{CI1\text{-}2}}$ or $-V_{\mathrm{CI1\text{-}2}}$ at the end of $\mathrm{UI}_1$, and to $\Delta V_{\mathrm{NP,min}}/2$ or $-\Delta V_{\mathrm{NP,min}}/2$ at the end of $\mathrm{UI}_2$, if $i_{\mathrm{M}}$ during $\mathrm{UI}_1$ and $\mathrm{UI}_2$ was negative or positive, respectively".

A simulation example illustrating the operation of the modified Band criterion is presented in Section 6.6. The modified criterion can achieve an NP voltage ripple of $\Delta V_{\mathrm{NP,min}}$ for the greatest part of Region 2, shown in Figure 6.7. In this part, $i_{\mathrm{NP}}$ can meet the implied requirement of being able to drive $v_{\mathrm{NP,Band}}$ to $\pm V_{\mathrm{CI1\text{-}2}}$ during $\mathrm{CI}_{1\text{-}2}$ (before $\mathrm{UI}_2$ begins). In the rest of Region 2, $\Delta V_{\mathrm{NP,min}}$ cannot be attained by any NV strategy (see end of Section 6.3.4).

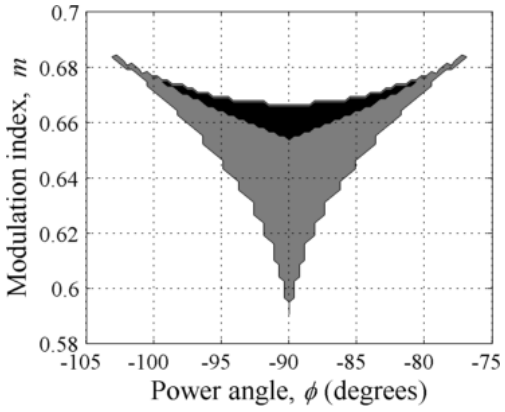


**Figure 6.7.** (White) Region 1, (Grey) Part of Region 2 where $\Delta V_{\mathrm{NP,min}}$ can be achieved, (Black) Part of Region 2 where $\Delta V_{\mathrm{NP,min}}$ cannot be achieved.

### 6.4.4 Algorithm

The proposed algorithm performs the 4-Step operation (see Section 6.3), for Band-NV strategies. A flowchart of the algorithm is illustrated in Figure 6.8. Steps 1, 2 and 4 are the same as in conventional NV strategies, while in Step 3, $v_{NP,ref}$ is adjusted according to the original/modified Band criterion, depending on the operating Region. The algorithm makes use of a set of registers, to keep certain results from the previous half cycle of $i_M$. The registers are reinitialized at the zero-crossings of $i_M$ (once every $T/6$) according to the pseudo-code in Figure 6.9, and perform the following operations, prior to the adjustment of $v_{NP,ref}$:

A) Detection of operating Region: The UIs that appear during a half cycle of $i_M$ are counted using register (counter) $R$. At the end of this half cycle, the value of $R$ is stored in register $R_{prev}$ (see Figure 6.9). $R_{prev}$ is used as an estimate for the operating Region in the new half cycle of $i_M$.

B) Calculation of $V_{CI1\text{-}2}$ (for Region 2): The algorithm makes use of the actual (minimized) NP voltage variation, $\Delta V_{NP}(1)$ and $\Delta V_{NP}(2)$ during the UIs, $UI_1$ and $UI_2$, respectively, instead of $\Delta V_{NP,min}$. $\Delta V_{NP}(1)$ and $\Delta V_{NP}(2)$ are derived from measurements of $v_{NP}$, to indirectly incorporate the values of the parameters required for the calculation of $\Delta V_{NP,min}$ and avoid the integration of (6.15). Due to this, the value of $\Delta V_{NP}(2)$ ($\Delta V_{UI2,min}$ in (6.18), (6.19)) is not yet known during $CI_{1\text{-}2}$, and thus $V_{CI1\text{-}2}$ cannot be calculated. $V_{CI1\text{-}2,prev}$ is calculated instead, based on the values of $\Delta V_{NP}(1)$ and $\Delta V_{NP}(2)$ from the previous half cycle of $i_M$. The algorithm then uses $-V_{CI1\text{-}2,prev}$ as an estimate for $V_{CI1\text{-}2}$ in the new half cycle of $i_M$.

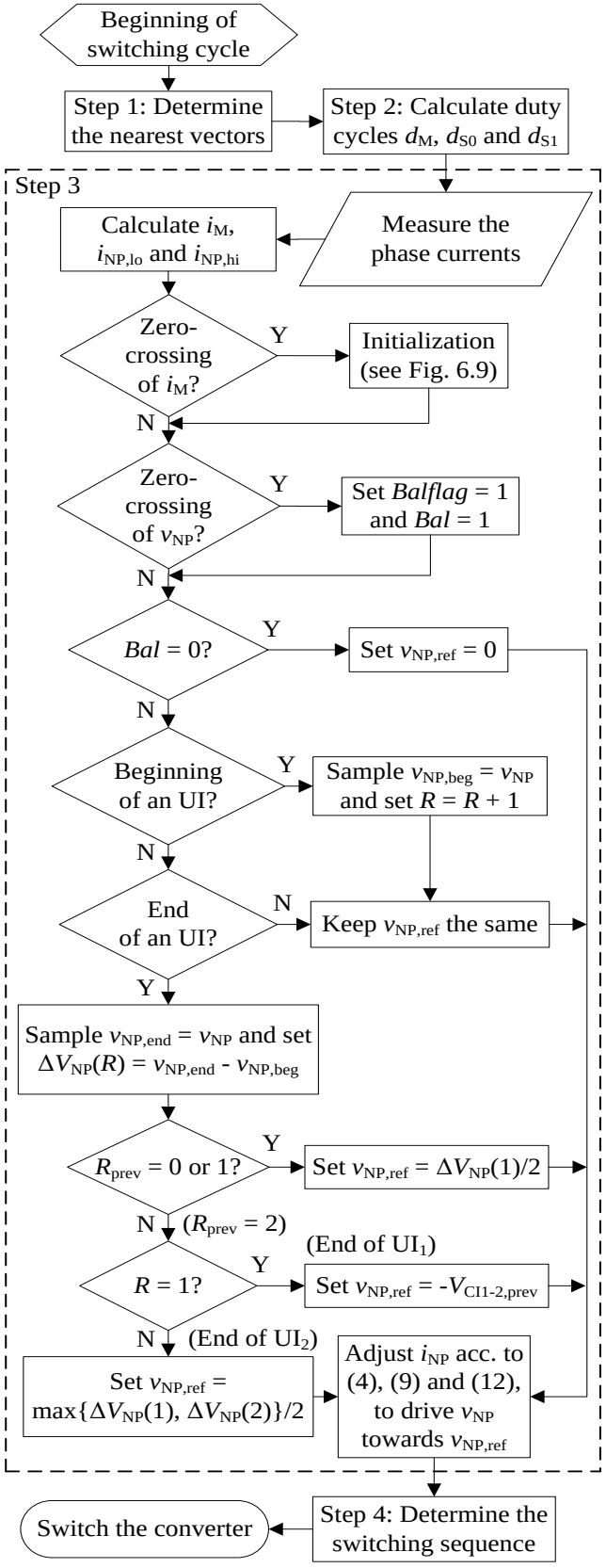


**Figure 6.8.** Flowchart of the proposed algorithm for the operation of Band-NV strategies.

| Initialization block |
|---|
| A1. If $R = 0$ then set $v_{NP,ref} = 0$<br>A2. Set $R_{prev} = R$<br>A3. Reset $R$ |
| B1. If $\|\Delta V_{NP}(2)\| > \|\Delta V_{NP}(1)\|$ then set $V_{CI1\text{-}2,prev} = -\Delta V_{NP}(2)/2$<br>else set $V_{CI1\text{-}2,prev} = \Delta V_{NP}(1)/2 - \Delta V_{NP}(2)$<br>B2. Reset $\Delta V_{NP}(1)$, $\Delta V_{NP}(2)$ |
| C1. If *Balflag* = 0 then set *Bal* = 0 else set *Bal* = 1<br>C2. Reset *Balflag* |

**Figure 6.9.** Pseudocode for the algorithm's initialization block.

C) Detection of transient imbalance: The reference NP voltage should be set to zero in case of a transient imbalance. If the converter operates in Region 0, $v_{NP,ref}$ is already zero, and therefore a Band-NV strategy performs balancing identically to a conventional one. In Regions 1 and 2, the NP voltage is expected to change sign during every half cycle of $i_M$. A register (flag), *Balflag*, which denotes that a sign change of $v_{NP}$ was encountered, is incorporated to the algorithm. If *Balflag* is not found set following a sign change of $i_M$, register *Bal* is set to 0, indicating that a transient imbalance appeared during the last half cycle of $i_M$. The algorithm then keeps $v_{NP,ref}$ to zero, until a zero-crossing of $v_{NP}$ is detected.

The values of $R_{prev}$ and $V_{CI1\text{-}2,prev}$ are available at the beginning of each half cycle of $i_M$. Unless a transient imbalance has occurred, the algorithm continues with detecting the UIs using (6.14). The NP voltage is sampled at the beginning and the end of each interval as $v_{NP,beg}$ and $v_{NP,end}$, respectively, and the NP voltage variation is stored in $\Delta V_{NP}(R) = v_{NP,end} - v_{NP,beg}$. At the end of UIs, $v_{NP,ref}$ is updated as follows:

- If $R_{prev}$ is 0, $v_{NP,ref}$ is set to zero by the initialization block. However, if an uncontrollable interval appears during the new half cycle of $i_M$, $v_{NP,ref}$ is set to $\Delta V_{NP}(1)/2$ at the end of it.
- If $R_{prev}$ is 1, at the end of $UI_1$, $v_{NP,ref}$ is set to $\Delta V_{NP}(1)/2$.
- If $R_{prev}$ is 2, at the end of $UI_1$, $v_{NP,ref}$ is set to $-V_{CI1\text{-}2,prev}$. It remains there until the end of $UI_2$, when it is set to $\max\{\Delta V_{NP}(1), \Delta V_{NP}(2)\}/2$.

It is worth pointing out that all register values are derived directly from the waveforms of $i_M$, $i_{NP,lo}$, $i_{NP,hi}$ and $v_{NP}$, and determine $v_{NP,ref}$. In addition, the use of results from the previous

half cycle of $i_M$ gives a maximum response time to a change in Region or peak-peak NP voltage ripple, of less than $T/3$ (= 6.67 ms for a 50 Hz operation). This arises from the fact that the operating conditions at the beginning of a certain half cycle of $i_M$ during which a change happens may affect the Region and NP voltage estimates for the next half cycle, starting after $T/6$, but not for the subsequent one, starting after $T/3$. A transient imbalance will also be detected, at the worst case, after $T/3$ from the time of its occurrence, depending on the direction of imbalance and its position in the cycle of $i_M$. If further reduction in this response time is needed, a threshold for $|v_{NP}|$ can be added to the algorithm to set *Bal* to 0.

The implementation of the algorithm (see Appendix A.4) requires measurement of the dc-link capacitor voltages, as well as of (two of) the three-phase converter output currents. Its computational requirements are increased compared to algorithms that implement the conventional criterion, due to a more elaborate Step 3 (in Figure 6.8). However, this increase is expected to be tolerable, since, apart from the multiplications required for the calculation of $i_{NP,lo}$ and $i_{NP,hi}$, the operations introduced in Step 3 are merely additions and comparisons.

### 6.4.5 Switching sequences – Conversion to Band-NV

The adoption of the Band criterion does not modify the switching sequences followed by a given NV strategy (Step 4); it only affects the duty cycle distribution factors of small vectors. A Band-NV strategy can therefore be fully defined using the switching sequences (together with the switching constraints) of a conventional NV strategy. Stated differently, any conventional NV strategy can be converted to operate as a Band-NV strategy, in order to achieve a lower value of NP voltage ripple.

## 6.5 Performance of Band-NV strategies

### 6.5.1 NP voltage ripple

The previous section showed how the adoption of a criterion, different from the dc-link capacitor imbalance (i.e. $v_{NP,ref} = 0$), for the duty cycle distribution of small vectors, creates the potential for decreasing the NP voltage ripple to its minimum possible value. In fact, it also proved that an NV strategy cannot obtain this minimum, unless the NP voltage at the

beginning of the UIs is equal to its appropriate, positive or negative, extreme. The conventional NV strategies do not fulfil this constraint, as they constantly drive the NP voltage towards zero. Hence, a conventional NV strategy cannot obtain the minimum value of NP voltage ripple, in contrast to a Band-NV strategy which potentially can.

Figure 6.10 plots the minimum amplitude of NP voltage ripple that can be achieved by conventional ($\Delta V_{\mathrm{NP,Conv}}/2$) and Band-NV strategies ($\Delta V_{\mathrm{NP,Band}}/2$), as a function of $\phi$ and $m$. The presented values were derived similarly to [51] and are normalized according to

$$\frac{\Delta V_{\mathrm{NPn}}}{2} = \frac{f C}{I_o} \frac{\Delta V_{\mathrm{NP}}}{2} \ . \qquad \textbf{(6.20)}$$

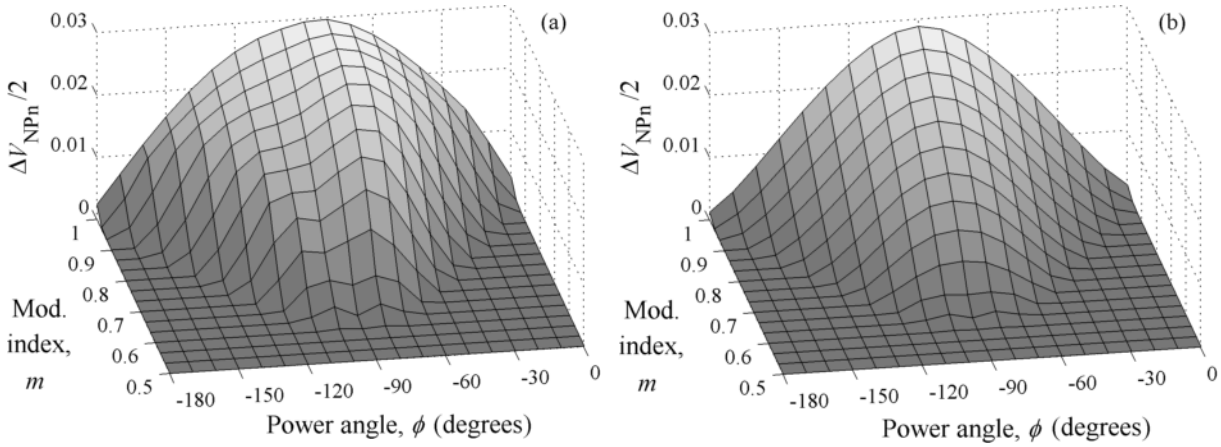


**Figure 6.10.** Minimum normalized amplitude of NP voltage ripple ($\Delta V_{\mathrm{NPn}}/2$) for (a) Conventional NV, and (b) Band-NV strategies.

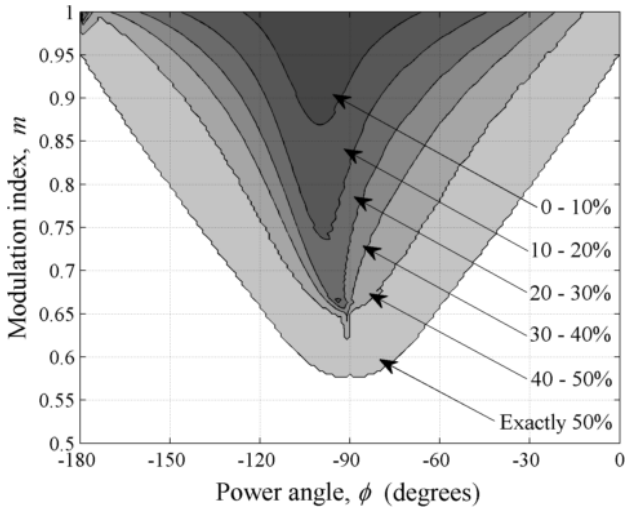


**Figure 6.11.** Value of *decr* as a function of $\phi$ and $m$.

The plots are shown only for $\phi$ = [−180, 0] degrees, because they are repeated for $\phi$ = [0, 180] degrees ($\Delta V_{\mathrm{NP}}(180 + \phi) = \Delta V_{\mathrm{NP}}(\phi)$). Their values are the minimum achievable by each strategy type because they were derived assuming no switching constraints. Applying a set of switching constraints, *SC*, may have an effect on them. However, as shown in Section 6.3.2, when $m$ approaches 1, $\Delta V_{\mathrm{NP}|SC}$ approaches $\Delta V_{\mathrm{NP}}$ for any imposed *SC*. Thus, $\Delta V_{\mathrm{NP,Conv}}$ and $\Delta V_{\mathrm{NP,Band}}$ for the critical value of $m$ = 1 can provide the information required for dc-link capacitor sizing for any conventional and Band-NV strategy, respectively. This argument is also supported by the equality of NP voltage ripple at $m$ = 1, shown in [51] for the conventional NTV and Symmetric strategies.

Moreover, the minimum NP voltage ripple achievable by Band-NV strategies is equal to $\Delta V_{\mathrm{NP,min}}$ in Regions 0 and 1, as well as in most of Region 2 (see Section 6.4.3). Thus, for these parts of the $\phi - m$ plane, Figure 6.10(b) is also a plot of $\Delta V_{\mathrm{NP,min}}$, and can be re-derived using (6.15) and (6.16). For the rest of the plane, $\Delta V_{\mathrm{NP,min}}$ is unattainable by NV strategies.

In Figure 6.11 the values of Figure 6.10(a) and 6.10(b) are used to plot the percentage decrement, *decr*, of minimum NP voltage ripple in Regions 1 and 2 as:

$$decr = \left(1 - \frac{\Delta V_{\mathrm{NP,Band}}}{\Delta V_{\mathrm{NP,Conv}}}\right) \cdot 100\% \quad . \tag{6.21}$$

Based on this figure, it is worth identifying the range of loads in terms of $\phi$, where the Band-NV strategies can offer a remarkable decrement ($decr \geq 30\%$) of NP voltage ripple. Given that the converter should be able to operate at a high modulation index ($m$ = 0.95), this range comprises the values of $\phi$ from approximately 0 to −50 (and −140 to −180) degrees. These values cover the use of the NPC converter as a motor drive ($\phi \approx -30$ degrees). On the contrary, the achievable decrement of NP voltage ripple for low power factor loads ($\phi \approx \pm 90$ degrees) is smaller than 10%. Thus, Band-NV strategies cannot offer a notable benefit in applications where the converter mainly has to provide reactive power.

Furthermore, it can be observed that *decr* is exactly equal to 50% for a large portion of Region 1. This is the region where the conventional NV strategies can hold the NP voltage to (approx.) zero for a part of the fundamental cycle. In this case, Band-NV strategies can decrease the NP voltage ripple to half, as shown in the example of Figure 6.4.

### 6.5.2 Effective switching frequency – Output voltage harmonic distortion

According to (6.3), the converter's effective switching frequency is determined by the number of switching steps followed by the selected modulation strategy. The switching steps, in turn, are defined in the strategy's switching sequences. As explained in Section 6.4.5, each conventional NV strategy can be converted to a respective Band-NV strategy having the same set of switching sequences. This conversion affects the duty cycle distribution of small vectors, but does not modify the switching sequences. Hence, the reduction in the NP voltage ripple offered by Band-NV strategies, avoids the significant increase in the effective switching frequency caused by non NV (or hybrid) strategies. Moreover, in contrast to the above strategies, Band-NV strategies do not suffer from the output voltage harmonic distortion introduced by the use of non nearest vectors.

In comparison to the respective conventional strategies, on the other hand, there is an effect which increases the effective switching frequency of Band-NV strategies when the converter operates in Region 1. The fundamental cycle can be divided into two types of interval, the duration of which is affected by the used criterion: A) Zero-$i_{NP}$ intervals, during which $i_{NP}$ should be kept to zero, so that the NP voltage remains constant, and B) Extreme-$i_{NP}$ intervals during which $i_{NP}$ should take the value $i_{NP,lo}$ or $i_{NP,hi}$, to drive the NP voltage as much as possible towards a certain direction. For the Band-NV strategies, the zero-$i_{NP}$ and extreme-$i_{NP}$ intervals correspond to the controllable and uncontrollable intervals, respectively. For conventional NV strategies, the zero-$i_{NP}$ intervals are those during which the NP voltage (neglecting the switching-frequency ripple) can be kept to zero, in contrast to the extreme-$i_{NP}$ intervals, during which the NP voltage has deviated from zero.

The average number of switching steps is higher in zero-$i_{NP}$ than in extreme-$i_{NP}$ intervals. In extreme-$i_{NP}$ intervals, each duty cycle distribution factor takes one of the extreme values of ±1, and holds it according to (6.10), (6.11). This leads to the same, single small vector (from the respective pair) and the corresponding switching sequence being selected for a number of successive switching cycles. In zero-$i_{NP}$ intervals, on the other hand, this selection changes between successive switching cycles, in order to keep the NP voltage constant. For the NTV strategy, the transition between different switching sequences typically requires additional switching steps [51]. For example, using the first two switching sequences from Table 6.1, it can be observed that, if $x_{S0}$ remains equal to +1 (same for −1) for two successive switching

cycles, 8 switching steps are induced in total. If $x_{S0}$ changes from +1 to −1, 9 steps are induced, due to the transition from vector 100 to 200. In case that a strategy's switching constraints allow the use of intermediate values (between +1 and −1) for $x_{S0}$ and $x_{S1}$, then during zero-$i_{NP}$ intervals such a value is selected, leading to the use of both small vectors from the respective pair according to (6.5) – (6.8). This again induces a higher number of switching steps compared to the extreme-$i_{NP}$ intervals, where a single small vector is used.

The increased effective switching frequency for Band-NV strategies arises from the fact that they have longer zero-$i_{NP}$ intervals than the corresponding conventional strategies. This is because the Band-NV strategies use the whole controllable intervals as zero-$i_{NP}$ intervals, whereas the conventional ones use parts of them as extreme-$i_{NP}$ intervals, to drive the NP voltage towards zero. The degree of the above increase, as well as its effect on the converter design, will be discussed in Section 6.7.

## 6.6 Simulation results

The previous sections showed that a decrement in NP voltage ripple can be achieved by the use of Band-NV strategies for the NPC converter. The results did not refer to a specific Band-NV strategy, since no set of switching sequences was assumed. As an example, this section compares the NTV modulation strategy with the respective Band-NV strategy, referred to as Band-NTV.

The two strategies were simulated using a MATLAB-Simulink model of an NPC inverter with the following parameters: $V_{dc}$ = 1.8 kV, $C$ = 0.5 mF, $f_s$ = 10 kHz, $f$ = 50 Hz. The load is varied between the presented simulations to attain the desired value of $\phi$ and an output rms current of 200 A. The current is kept to that value, so that the effect of $m$ and $\phi$ on the amplitude of NP voltage ripple can be observed more clearly and verified against Figure 6.10, by means of (6.20). The simulation figures illustrate the line-line voltage $v_{ab}$, current $i_a$, and capacitor $C_1$ reference voltage ($v_{C1,ref}$ = 900 + $v_{NP,ref}$) when the inverter is modulated by the Band-NTV strategy, as well as the voltage $v_{C1}$ and the locally averaged currents $i_{NP,hi}$, $i_{NP,lo}$ and $i_{NP}$, for both strategies.

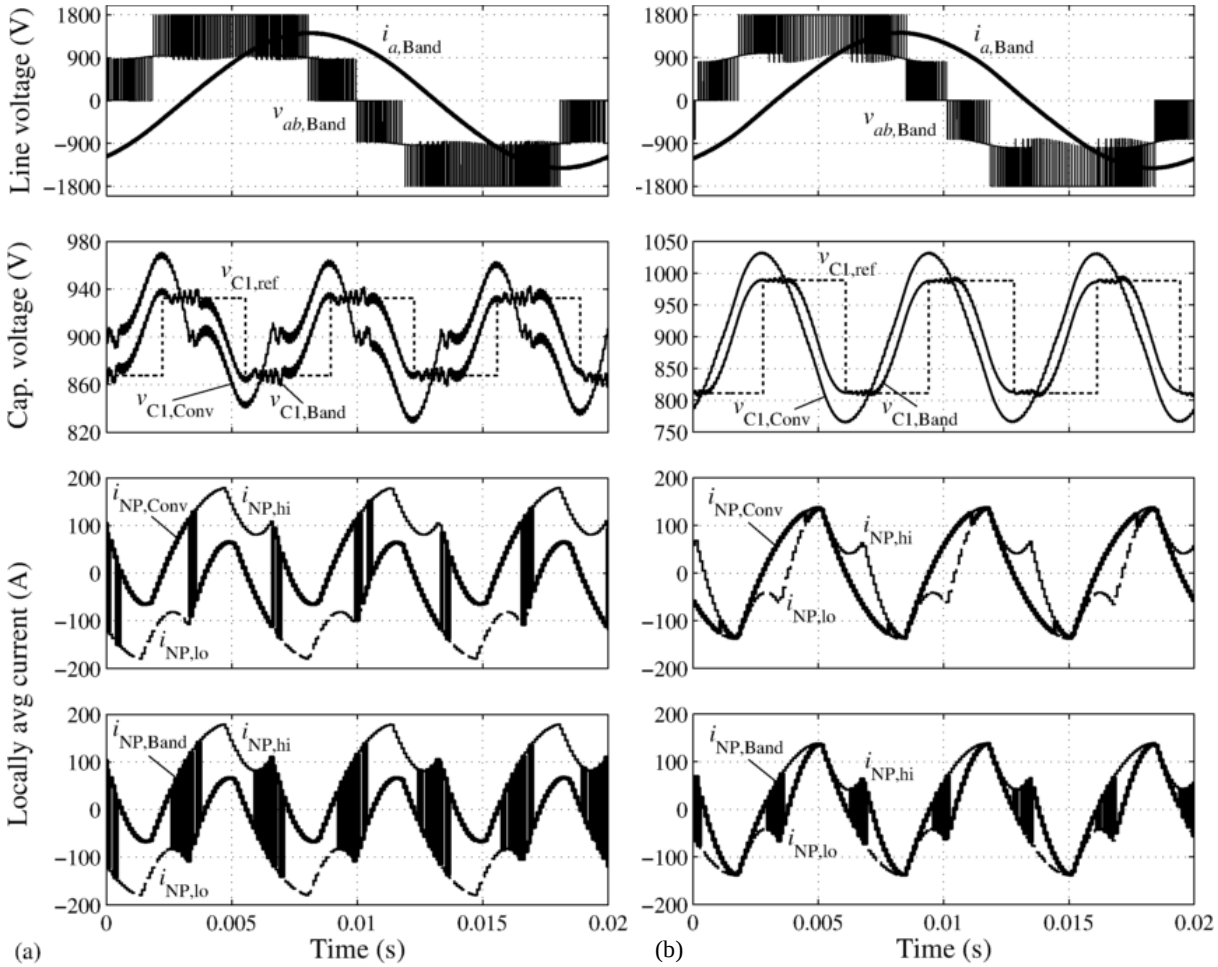


**Figure 6.12.** Simulation comparing the Band-NTV to the conventional NTV strategy during a fundamental cycle, for $\phi = -30$ degrees and (a) $m = 0.9$, (b) $m = 1$. *i*) (top) Line voltage $v_{ab}$ and current $5\times i_a$, *ii*) $v_{\mathrm{C1,Conv}}$, $v_{\mathrm{C1,Band}}$ and $v_{\mathrm{C1,ref}}$, *iii*) $i_{\mathrm{NP,Conv}}$, $i_{\mathrm{NP,lo}}$ and $i_{\mathrm{NP,hi}}$, and *iv*) (bottom) $i_{\mathrm{NP,Band}}$, $i_{\mathrm{NP,lo}}$ and $i_{\mathrm{NP,hi}}$.

The simulations in Figures 6.12 and 6.13 focus on the operating range of motor drives, assuming a representative load power angle $\phi$ of −30 degrees (power factor of 0.866). The waveforms in Figure 6.12(a) and 6.12(b) correspond to two operating points, where *decr* is exactly equal to 50% and less than 50%, respectively. It can be noticed that in the first case, the NTV strategy can drop the NP voltage down to zero during the controllable intervals. As shown in Section 6.4, the Band-NTV strategy can then halve the NP voltage ripple. In the second case, the decrement offered by the Band-NTV strategy is less than 50%, but still significant (approx. 30%). The waveforms of $i_{\mathrm{NP,Conv}}$ and $i_{\mathrm{NP,Band}}$, which are responsible for the above decrements, can be studied based on Figure 6.4. Figure 6.12(a), in particular, uses the same values of $\phi$ and $m$ as Figure 6.4, to illustrate the agreement between simulation and

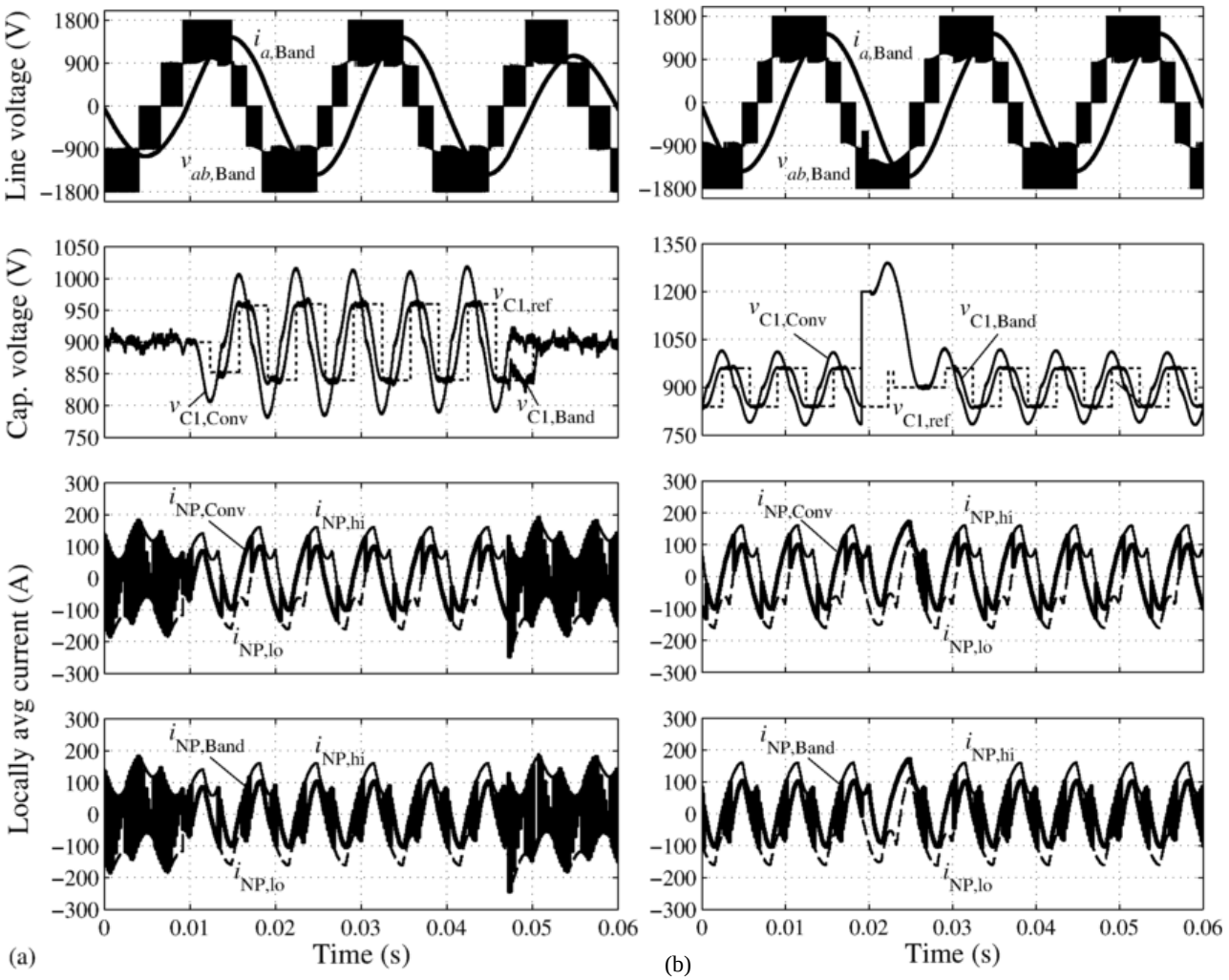


**Figure 6.13.** Simulation comparing the Band-NTV to the conventional NTV strategy, for transient responses, (a) Change of $m$ from 0.7 to 0.95 and back to 0.7, for $\phi = -30$ degrees, and (b) Balancing after a transient imbalance, while the inverter operates at $\phi = -30$ degrees and $m = 0.95$. *i*) (top) Line voltage $v_{ab}$ and current $5\times i_a$, *ii*) $v_{C1,Conv}$, $v_{C1,Band}$ and $v_{C1,ref}$, *iii*) $i_{NP,Conv}$, $i_{NP,lo}$ and $i_{NP,hi}$, and *iv*) (bottom) $i_{NP,Band}$, $i_{NP,lo}$ and $i_{NP,hi}$.

analytical results. The difference in the simulated waveforms is that, during the zero-$i_{NP}$ intervals, $i_{NP}$ gets the form of a switching-frequency ripple instead of being equal to zero. This is because the switching constraints of the NTV strategy do not allow it to adjust $x_{S0}$ and $x_{S1}$ to get a zero value for $i_{NP}$. Thus, the desired zero value is achieved as an average over more than one switching cycles, by shifting $i_{NP}$ between positive and negative values. Furthermore, as explained in Section 6.5.2, the zero-$i_{NP}$ intervals can be observed to be longer for the Band-NTV strategy.

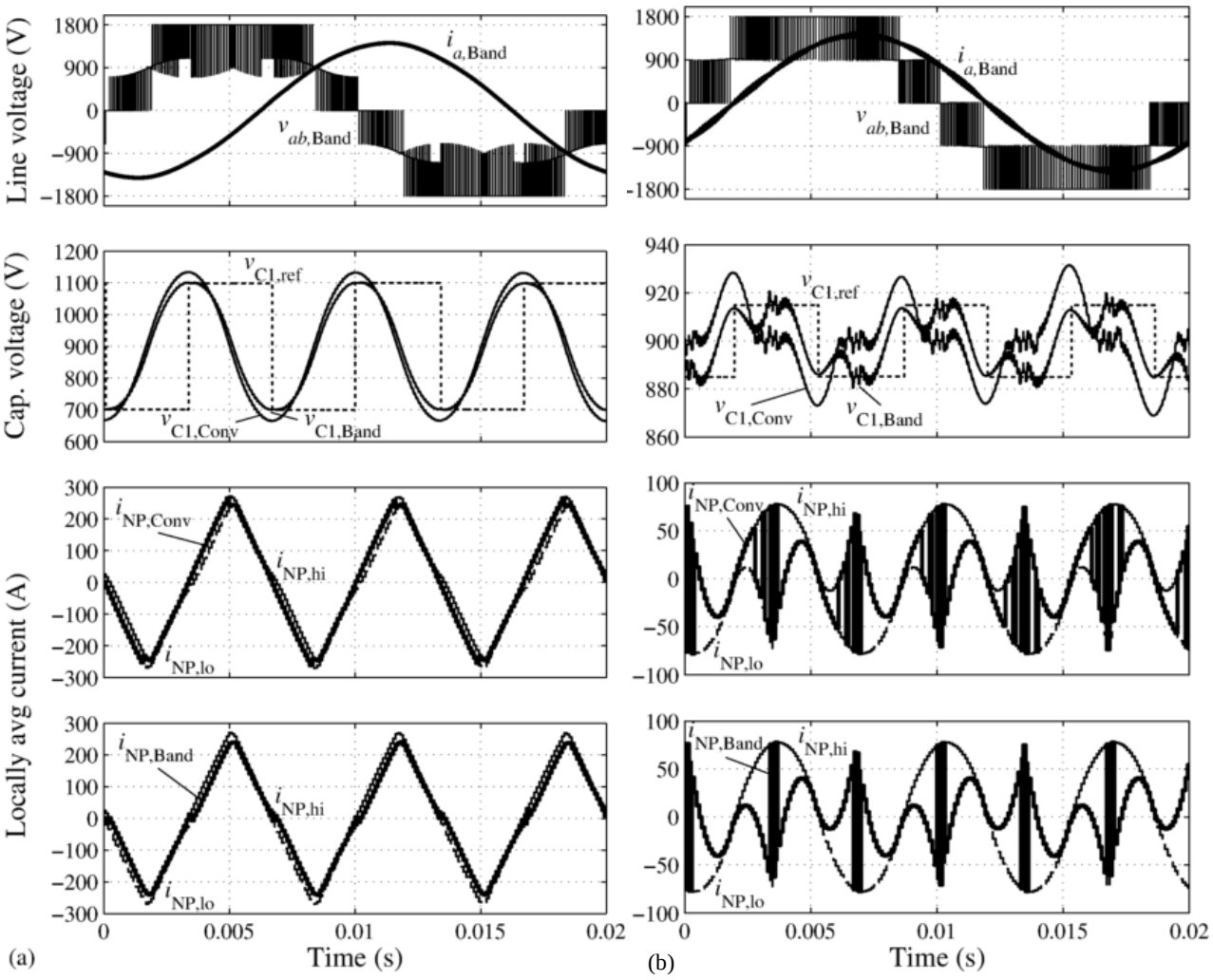


**Figure 6.14.** Simulation comparing the Band-NTV to the conventional NTV strategy during a fundamental cycle, for (a) $\phi = -83$ degrees, $m = 0.95$ (Region 1), and (b) $\phi = -6$ degrees, $m = 1$ (Region 2). i) (top) Line voltage $v_{ab}$ and current $5\times i_a$, ii) $v_{\mathrm{C1,Conv}}$, $v_{\mathrm{C1,Band}}$ and $v_{\mathrm{C1,ref}}$, *iii*) $i_{\mathrm{NP,Conv}}$, $i_{\mathrm{NP,lo}}$ and $i_{\mathrm{NP,hi}}$, and *iv*) (bottom) $i_{\mathrm{NP,Band}}$, $i_{\mathrm{NP,lo}}$ and $i_{\mathrm{NP,hi}}$.

Figure 6.13 illustrates the transient response of the proposed algorithm for the Band-NV strategies to two types of transient. In Figure 6.13(a), the modulation index is changed from 0.7 to 0.95, and back to 0.7. The operating region changes, respectively, from Region 0 to 1 and back to 0, as determined by the waveforms of $i_{\mathrm{NP,lo}}$ and $i_{\mathrm{NP,hi}}$ (see Figure 6.4 and Figure 6.5(a)). It can be noticed that it takes less than $T/3$ for the algorithm to detect each of the above changes and change $v_{\mathrm{NP,ref}}$. Figure 6.13(b) presents a voltage balancing example after a forced transient imbalance. The imbalance is detected by the algorithm and is attenuated within the same time interval as in the case of the conventional strategy.

Figure 6.14 illustrates two simulation examples, where the inverter operates with a low and a high-power-factor load, respectively. In the case presented in Figure 6.14(a) ($\phi$ = −83 degrees, $m$ = 0.95), it can be observed that the Band-NTV strategy does not decrease the NP voltage ripple significantly. This is because the inverter operates at the part of Region 1 where *decr* is lower than 10% (see Figure 6.11). In Figure 6.14(b) ($\phi$ = −6 degrees, $m$ = 1), the inverter operates in Region 2. The Band-NTV strategy therefore uses the modified version of the Band criterion, to re-adjust $v_{NP,ref}$ at the end of each of the two UIs. However, due to the fact that $\Delta V_{NP}(2) > \Delta V_{NP}(1)$ in Figure 6.14(b), $v_{NP,ref}$ does not change twice during each half cycle of $i_M$. Namely, $v_{NP,ref}$ takes the value of $\Delta V_{NP}(2)/2$ at the end of each $UI_2$, and shifts to $-V_{CI1\text{-}2,prev}$ which is again equal to $\Delta V_{NP}(2)/2$, at the end of the following $UI_1$. The achieved decrement in NP voltage ripple for this case is 50%.

## 6.7 Discussion

Figure 6.15(a) summarizes additional simulation results regarding the (normalized) amplitude of the NP voltage ripple generated by the NTV and Band-NTV strategies, for the case of $\phi$ = −30 degrees. It also includes the cross-sections of Figure 6.10(a) and 6.10(b) for the above value of $\phi$, which provide the minimum ripple achievable by conventional and Band-NV strategies, respectively. The decrement in NP voltage ripple by the Band-NTV strategy is 50% for up to $m$ = 0.925 and gradually reaches a minimum of 31%. It is important to note that, according to Sections 6.3.2 and 6.5.1, this value of 31% is expected to be the same for all other NV strategies, as it corresponds to $m$ = 1. For this case of $m$ = 1, simulated in Figure 6.12(b), the peak capacitor voltage is reduced from approx. 1040 to 995 V, which provides a significant advantage in terms of module voltage stress. The conversion to the Band-NTV strategy can alternatively be used to reduce the dc-link capacitance, and thus the cost of the converter. A reduction of $C$ by 31%, will still produce the same or lower (for $m$ < 1) NP voltage ripple as the conventional NTV strategy.

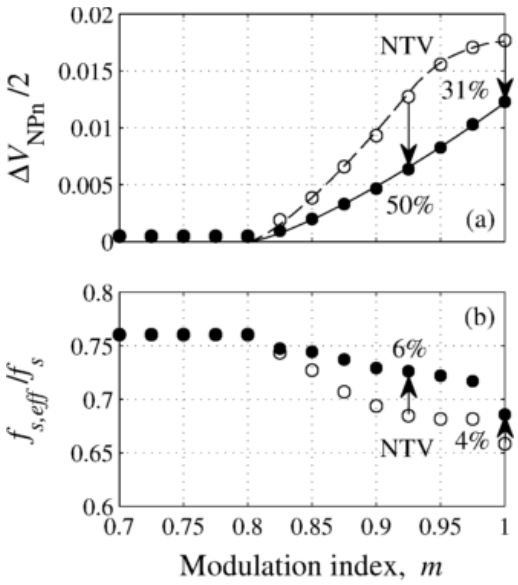


**Figure 6.15.** For $\phi = -30$ degrees and $m \geq 0.7$, (a) Normalized amplitude of NP voltage ripple: (continuous line) $\Delta V_{NPn,Band}/2$, (dashed line) $\Delta V_{NPn,Conv}/2$, (filled circles) Simulation for Band-NTV strategy, (empty circles) Simulation for NTV strategy, and (b) Ratio of $f_{s,eff}$ over $f_s$.

Figure 6.15(b) plots the simulated ratio of $f_{s,eff}$ over $f_s$ (i.e. the ratio of the counted switching steps during an extensive simulation time interval, $\Delta t$, over $6f_s\Delta t$), for the NTV and Band-NTV strategies. Although the two strategies use the same set of switching sequences, the effective switching frequency of the Band-NTV strategy is increased by 4 to 6% compared to the NTV strategy. As explained in Section 6.5.2, this difference arises from the longer zero-$i_{NP}$ intervals of the Band-NTV strategy. Nevertheless, what is important is that the (increased) effective switching frequency of the Band-NTV strategy is lower than the (common) effective switching frequency of the two strategies in Region 0 ($m \leq 0.8$). This is due to the fact that in Region 0 the zero-$i_{NP}$ intervals cover the whole fundamental cycle (for the NTV strategy this is also because $m$ is lower in Region 0, thus $\mathbf{V_{REF}}$ spends a greater part of the cycle in $tr_2$ or $tr_4$ in Figure 6.2, where the 8-step switching sequences appear). As m increases, taking the operating point from Region 0 to the upper part of Region 1, the portion of zero-$i_{NP}$ intervals, and thus the effective switching frequency, drops; it is this drop that is smaller for the Band-NTV strategy. However, a converter is commonly designed to be able to operate at a certain (rated) effective switching frequency for the whole range of $m$. Therefore, use of the Band-NTV in place of the NTV strategy may have an effect on the converter switching losses, but, unlike non NV or hybrid strategies, will not affect its rating

and design (modules, heatsink, etc). Namely, for the simulation value of $f_s$ = 10 kHz, the converter can be designed for $f_{s,eff}$ = 7.6 kHz, which is the effective switching frequency in Region 0 (see Figure 6.15(b), for $m \leq 0.8$). The use of a non NV strategy, on the other hand, would increase the effective switching frequency to a value (approx. $f_{s,eff}$ = 13.3 kHz) that cannot be reached by 1700 V modules which suit the assumed dc-link voltage level. According to Section 6.5.2, the above described effect is expected to appear in a similar way when converting other NV strategies to Band-NV. Apart from the NTV, it has also already been verified for the case of the Symmetric (NV) strategy [51], as shown in Section 8.2.1.

Finally, the following two comments refer to aspects of the proposed concept that were not included in this study (which is also the case in similar studies [16, 40, 41, 51, 52, 62, 67, 68]:

- The switching-frequency NP voltage ripple was not considered during the formulation of Band-NV strategies. However, at low switching frequencies relative to the fundamental, which are common for medium-voltage applications, this becomes important. In such cases, extra care should be taken when implementing a Band-NV strategy, since the switching-frequency NP voltage ripple will affect the NP voltage sampling, and therefore the performance of the proposed algorithm.

- The calculation of duty cycles for the NVs was based on [62], which assumes balanced capacitor voltages. However, when NP voltage ripple appears, the above duty cycles should be modified to avoid distortion (that is, injection of low-frequency harmonics) of the output voltage. Feed-forward techniques have been proposed for this purpose [28, 31, 71] which can be adapted for application on Band-NV strategies.

## 6.8 Conclusion

The mechanism of Neutral-Point voltage ripple generation by Nearest-Vector strategies for the NPC converter was analysed, and the minimum achievable ripple amplitude was derived. It was shown that conventional (that is, existing) NV strategies cannot attain this minimum, due to the criterion they use to perform NP (dc-link capacitor) balancing. A new criterion and a respective algorithm were proposed to form Band-NV strategies, which provide this possibility.

Conventional NV strategies can also be converted to operate according to the proposed approach. Analytical results showed that the conversion of a conventional to a Band-NV strategy can decrease the NP voltage ripple by approximately 30 to 50% for a motor drive application ($\phi$ = −30 degrees). Alternatively, if a certain amplitude of NP ripple can be afforded, the dc-link capacitance (required to limit the NP voltage ripple) can be reduced by 30%. For higher power factor loads this percentage can reach closer to 50%, whereas no significant benefit can be expected for very low power factor loads ($\phi$ close to ±90 degrees). The above results were verified by simulations of the well-known NTV strategy and its Band-NV equivalent. It was also shown that similar outcomes are equally attainable by the conversion to Band-NV of other conventional strategies.

As compared to non NV and hybrid strategies, which are the present alternative for decreasing the NP voltage ripple, Band-NV strategies offer the advantage of not affecting the converter's rated switching frequency. However, in comparison to the respective conventional NV strategies, a small increase in switching losses can be expected when the converter operates at a high modulation index.

# Chapter 7

## Hybrid modulation strategies for eliminating low-frequency Neutral-Point voltage oscillations in the Neutral-Point-Clamped converter

## 7.1 Introduction

The previous chapter focused on NV strategies, proposing Band-NV strategies to minimize the amplitude of NP voltage ripple in an NPC converter. As explained in Section 6.2, however, NV (and Band-NV) strategies can only eliminate NP voltage ripple for a certain range of values of load power angle and converter modulation index. Non NV strategies, on the other hand, can achieve NP voltage ripple elimination throughout the converter's operating range (i.e. for all values of $\phi$ and $m$), yet increasing the switching losses and output voltage distortion.

The trade-off between the NP voltage ripple produced by NV strategies on the one hand, and the increment of switching losses and output voltage WTHD caused by non NV strategies on the other, gave birth to hybrid strategies, which operate as combinations of the two. In [72], the well-known SPWM (which is an NV) strategy is combined with a non NV strategy, implemented as a carrier-based PWM with two carrier waveforms. A variable, $D$, determines the fraction of the fundamental cycle where SPWM modulates the converter. It is important to note that, unless $D$ is equal to zero, NP voltage ripple appears at the dc-link.

A different approach for creating a hybrid strategy can be found in [52]. There, the NTV strategy (named N3V in [52]) modulates the NPC converter in combination with a proposed non NV strategy, named S3V. S3V is characterized by using three vectors during each switching cycle, among which, one is non nearest. A threshold, $v_{NP,max}$, for the NP voltage is used to determine when S3V should be put into action ($|v_{NP}| > v_{NP,max}$), thus avoiding further NP voltage deviation (caused by the NTV). This approach also generates NP voltage ripple with amplitude $v_{NP,max}$. Moreover, in case that $v_{NP,max}$ is set close to zero with the aim of eliminating NP voltage ripple, successive transitions appear from the NV to the non NV strategy and vice-versa. As it will be shown later (in Section 7.3), this effect is undesirable since it can increase the converter's switching losses.

Finally, in [34], a strategy that mitigates the drawbacks of the NTV$^2$ [33] is described. The strategy is classified here as hybrid, because the line voltage (PWM) waveforms in [33] indicate that it can partly operate as an NV strategy. Its formulation is based on a WTHD minimization process, which should be performed offline for non linear or imbalanced loads. For the case of linear and balanced loads, the results of the above process can be

approximated by analytical equations. However, as explained in [66], an online estimator of the load power angle, as well as a detector for the linear and balanced nature of the load are still required.

This chapter proposes a straightforward way of creating hybrid strategies for the NPC converter, which have the following characteristics:

- Eliminate NP voltage ripple.
- Can operate with non linear or imbalanced loads.
- Can be built as combinations of any NV and non NV strategy.
- Use the non NV strategy to the minimum possible extent, thus minimizing the converter's switching losses and WTHD for the selected strategy combination.

## 7.2 Proposed Hybrid strategies

It is reminded that in Section 6.3.4 the fundamental cycle of the NPC converter was divided into controllable and uncontrollable intervals, according to whether the following equation holds:

$$\left(i_{\mathrm{NP,lo}} \le 0 \text{ and } i_{\mathrm{NP,hi}} \ge 0\right). \tag{7.1}$$

The above distinction can provide the basis for creating hybrid strategies which can eliminate NP voltage ripple. Given an NV strategy, *X*, and a non NV strategy, *Y*, a hybrid strategy, $H_{X\text{-}Y}$, that combines the two can be built according to the flowchart in Figure 7.1. Namely, the converter can be modulated using *X* throughout the controllable intervals, since during them, *X* is capable of holding $v_{\mathrm{NP}}$ to zero. During the uncontrollable intervals, on the other hand, *Y* should be put into action.

Controllable and uncontrollable intervals can be identified in practice using the instantaneous (sampled) values of the phase currents as values of $\mathrm{I_{NP}}(\mathbf{V})$ in (6.4) and (6.9) – (6.11). In this way, operation of hybrid strategies according to Figure 7.1 is equally achievable for converter loads that draw non sinusoidal or imbalanced currents. Moreover, it can be performed for loads that require non sinusoidal voltages, since the NVs and duty cycles $d_{\mathrm{M}}$, $d_{\mathrm{S0}}$ and $d_{\mathrm{S1}}$, can be determined for any, circular or not, movement of $\mathbf{V_{REF}}$ in the

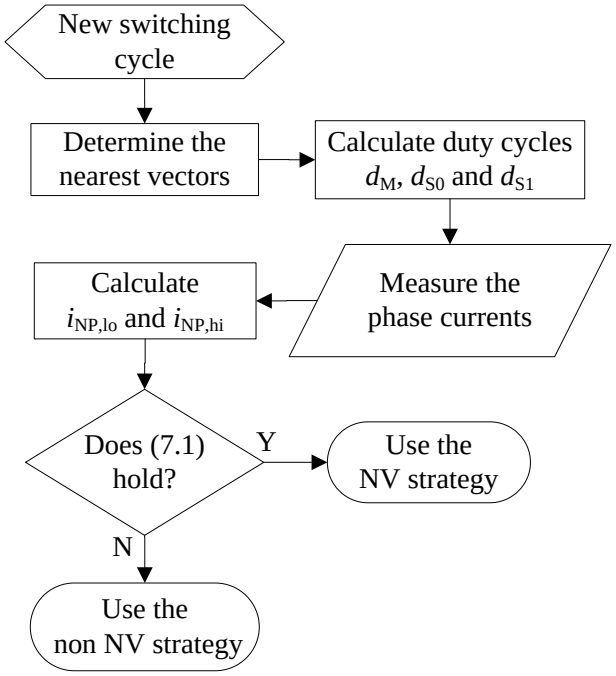


**Figure 7.1.** Flowchart for the proposed hybrid strategies.

linear modulation region (circle in Figure 2.13). An example of such a load is a motor with a non sinusoidal back-emf, which the converter has to provide with sinusoidal currents.

## 7.3 Simulation results

An NPC inverter with $V_{dc}$ = 1.8 kV, $C_1$ = $C_2$ = 0.5 mF, $f_s$ = 8 kHz, and $f$ = 50 Hz is simulated using MATLAB-Simulink (SimPowerSystems Toolbox). The simulation figures illustrate the locally averaged currents $i_{NP,lo}$ and $i_{NP,hi}$, the applied modulation strategy, the line-line voltage $v_{ab}$ and phase current(s), and the capacitor voltage $v_{C1}$. In Figure 7.2, the inverter supplies a linear and balanced load with $\phi$ = −30 degrees (power factor of 0.866), while $m$ is set to 0.9. The waveforms of $i_{NP,lo}$ and $i_{NP,hi}$ are shown for the entire simulation, but they are only used by the simulated hybrid strategy, according to Figure 7.1. This strategy, $H_{NTV-S3V}$, combines the (NV) NTV strategy [51], with the (non NV) S3V strategy, proposed in [52]. In order to demonstrate its operation as compared to the combined strategies, the inverter is modulated for one fundamental period (0.02 s) by each strategy, as follows: From 0 to 0.02 s by the S3V, from 0.02 to 0.04 s by the NTV, and from 0.04 to 0.06 s by the $H_{NTV-S3V}$ strategy. It can be observed that the low-frequency NP voltage ripple that appears when

the NTV strategy modulates the inverter is eliminated by the $H_{NTV\text{-}S3V}$. This happens even though the NTV is still applied in place of the S3V for a significant part (48.5%) of the fundamental cycle. Moreover, the line voltage waveform generated by the HNTV-S3V can be seen to be enhanced (i.e. closer to the five-level waveform generated by the NTV strategy) as compared to the S3V strategy, thus having a decreased value of WTHD.

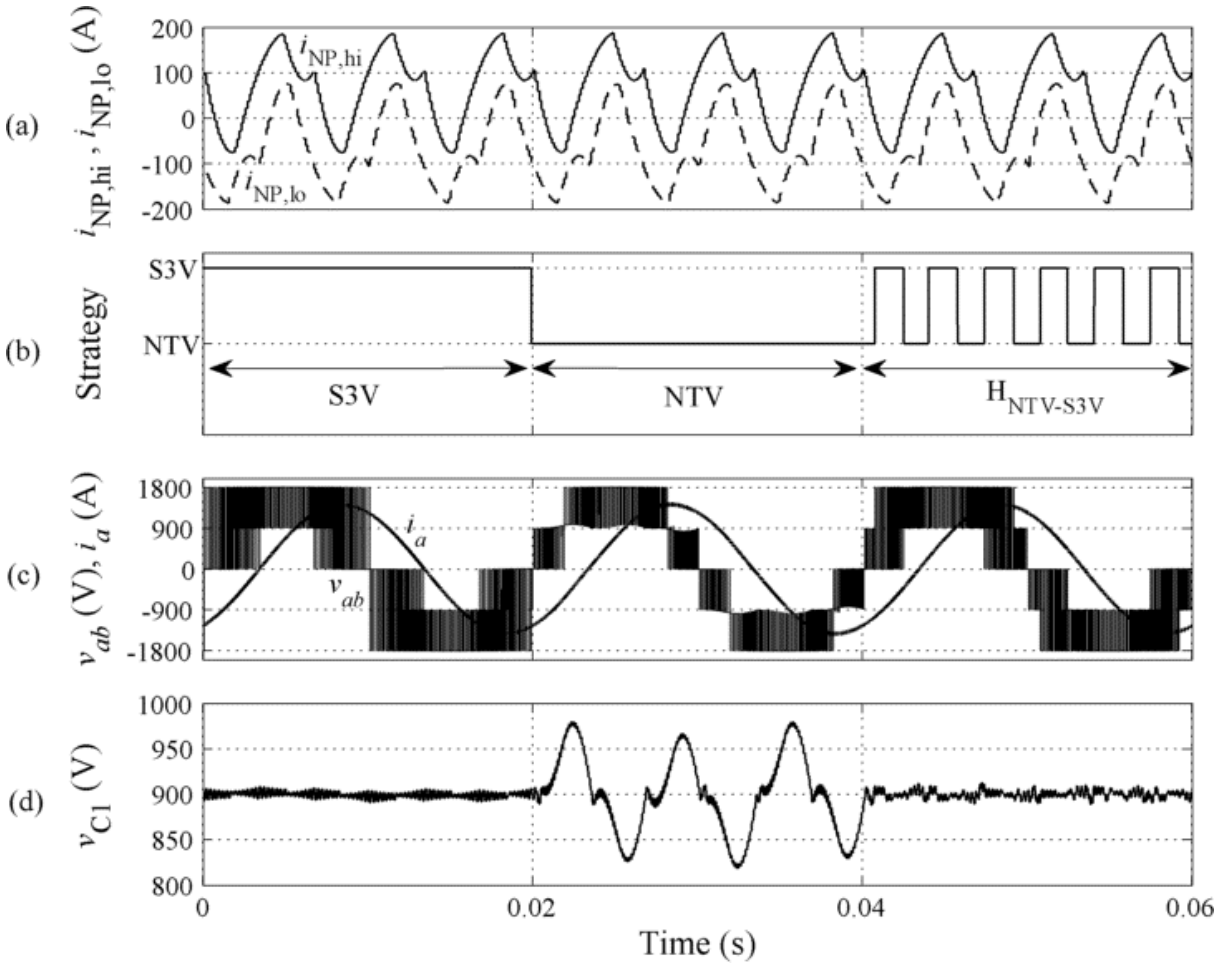


**Figure 7.2.** Simulation of NPC inverter modulated successively by the S3V, NTV and $H_{NTV\text{-}S3V}$ strategies: (a) Locally averaged currents $i_{NP,lo}$ and $i_{NP,hi,}$ (b) Applied modulation strategy, (c) Line voltage $v_{ab}$ and current $5\times i_a$, and (d) Capacitor voltage $v_{C1}$.

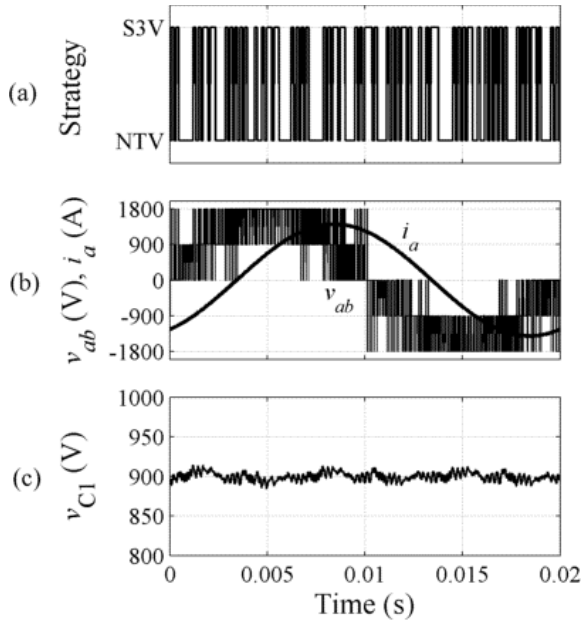


**Figure 7.3.** Simulation of NPC inverter modulated by a hybrid strategy combining the NTV and S3V according to **[52]** ($v_{NP,max}$ = 5 V): (a) Applied modulation strategy, (b) Line voltage $v_{ab}$ and current $5\times i_a$, and (c) Capacitor voltage $v_{C1}$.

Combining the NTV with the S3V according to [52] and using a voltage threshold $v_{NP,max}$ of 5 V, has the effect shown in Figure 7.3. Due to the NTV strategy, the NP voltage quickly reaches the threshold and varies around it, thus causing multiple transitions between the two strategies. Such transitions, however, can introduce additional switching steps to the converter. For example, for $\mathbf{V_{REF}}$ as in Figure 6.1, the NTV strategy may need to use the switching sequence "210-110-100-110-210" (from Table 6.1). The S3V, on the other hand, would avoid the (ripple-generating) medium vector 210 and use "100-200-220-200-100" for a similar $\mathbf{V_{REF}}$. As a consequence, for each transition between the two strategies in that area of $\mathbf{V_{REF}}$, two additional switching steps will be introduced to the converter (to switch from 100 to 210 or vice-versa). When using the above approach, the switching sequences of the combined strategies should therefore be redesigned with the aim of minimizing the added steps and their impact on the converter's switching losses.

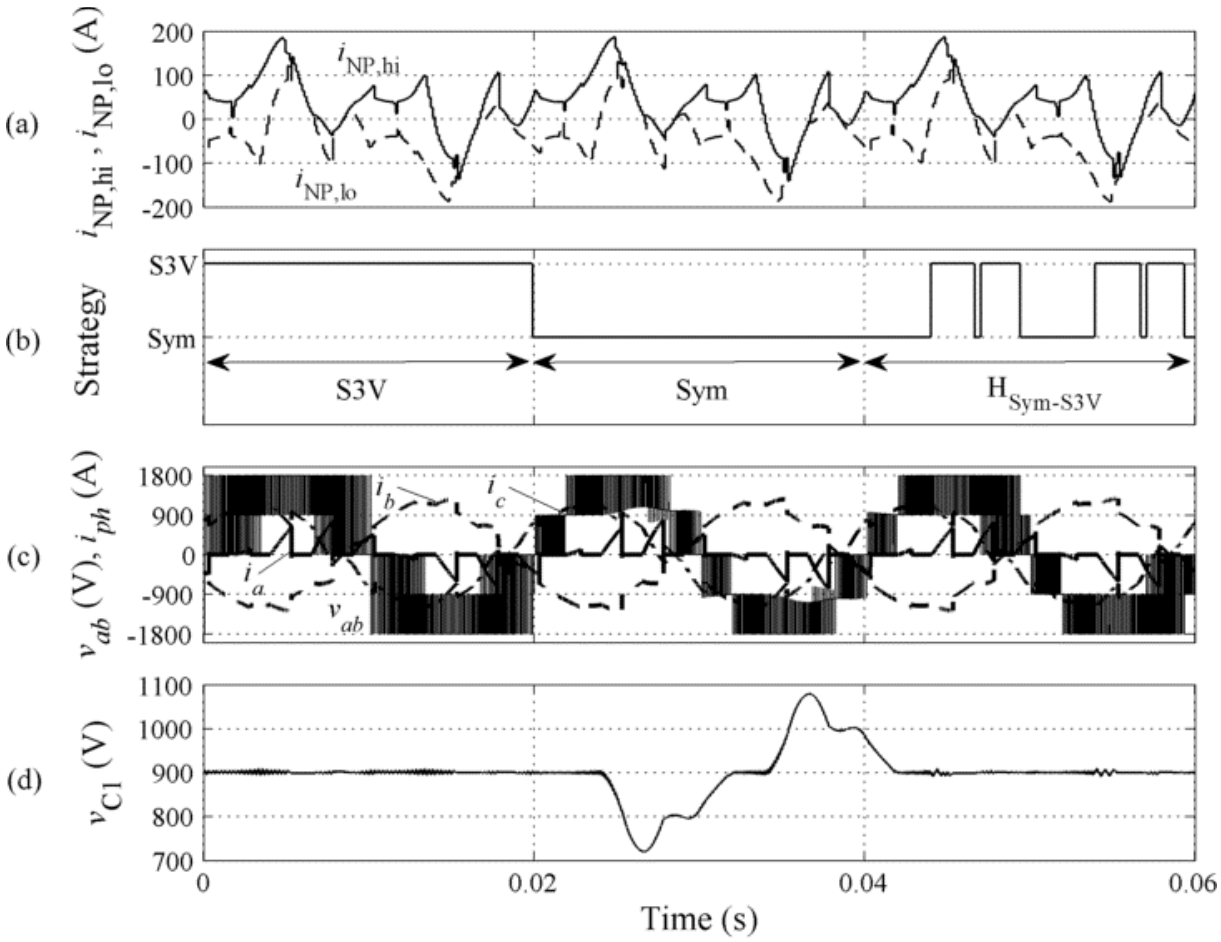


**Figure 7.4.** Simulation of NPC inverter modulated successively by the S3V, Symmetric (Sym) and $H_{Sym-S3V}$ strategies, supplying a non linear and imbalanced load: (a) Locally averaged currents $i_{NP,lo}$ and $i_{NP,hi}$, (b) Applied modulation strategy, (c) Line voltage $v_{ab}$ and three-phase currents $5\times i_a$, $5\times i_b$, and $5\times i_c$, and (d) Capacitor voltage $v_{C1}$.

In Figure 7.4, the simulated hybrid strategy, $H_{Sym-S3V}$, combines the Symmetric (Sym) NV strategy [51] with the S3V. The $H_{Sym-S3V}$ is given as a second example, demonstrating the applicability of the proposed concept on different combinations of NV and non NV strategies. Furthermore, the load in this simulation is non linear and imbalanced. It can be seen, again, that the $H_{Sym-S3V}$ eliminates the NP voltage ripple generated by the Symmetric strategy, even though the latter is still applied for approximately 50% of the fundamental cycle.

## 7.4 Discussion

Figure 7.5 plots the percentage duration of uncontrollable intervals during a fundamental cycle, as a function of $\phi$ and $m$. The presented values are derived using (6.4) and (6.9) – (6.12), for the case of sinusoidal and balanced phase currents (they are shown for $\phi = -180$ to 0 degrees; they are identical for $\phi = 0$ to 180 degrees, respectively). For hybrid strategies created according to Figure 7.1, Figure 7.5 also depicts the percentage duration of applying the (selected) non NV strategy. It can be observed that, for $\phi = -90$ degrees and $m > 0.7$, this percentage approaches 100%. Thus, for purely reactive loads, the proposed hybrid strategies offer no benefit compared to non NV strategies, since they operate as such (the same has been observed in [34]). On the other hand, for less reactive loads, the participation of non NV strategies is lower than 100% and decreases with $m$. For low values of $m$ it drops to zero, therefore the hybrid strategies operate as NV strategies.

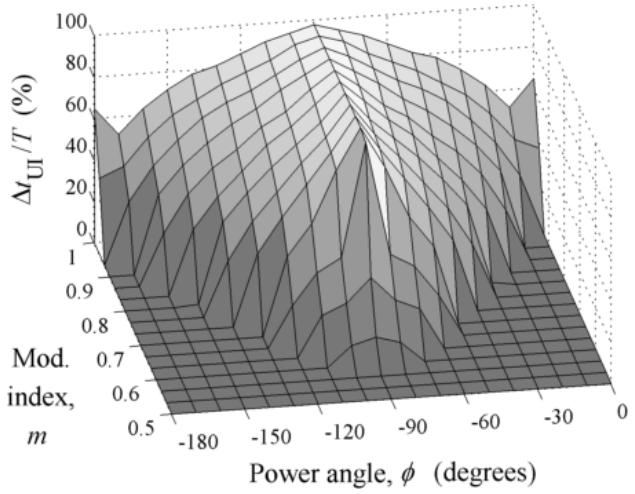


**Figure 7.5.** Percentage duration of uncontrollable intervals as a function of $\phi$ and $m$ according to (6.4) and (6.9) – (6.12), for sinusoidal and balanced phase currents.

The proposed approach inherently guarantees minimum participation of non NV strategies, since non NV strategies are only applied when an NP voltage deviation cannot be prevented by NV strategies. Hence, for a given combination of strategies, the approach yields an NP-voltage-ripple-eliminating strategy with minimum switching losses and output voltage WTHD.

An estimate for these switching losses can be obtained by an analysis similar to that included in [72]. Such an analysis can be performed owing to the fact that the intervals of the fundamental cycle where each strategy is applied can be specified analytically (as in Figure 6.3); this is not the case in the approaches of [52] and [34]. In comparison to [52], the proposed approach also has the advantage of avoiding multiple transitions between the combined strategies, and thus the need for modification of their switching sequences. In fact, operation according to Figure 7.1 can be readily added to any implemented pair of strategies. Computationally, this incurs little additional cost, since the determination of the NVs and the calculation of duty cycles (in Figure 7.1) are already in place for any NV strategy.

A last comment refers to the capacitor (or NP) balancing capabilities of the proposed strategies, after possible NP voltage deviations. Unlike non NV strategies which may need to implement additional control loops [50, 66], hybrid strategies can rely on their NV strategies to achieve this task. Namely, since the NV strategies are applied during the controllable intervals, they are given the chance to adjust $i_{NP}$ in favour of capacitor balancing (a similar comment can be found in [52]). As the percentage duration of controllable intervals increases (Figure 7.5), the balancing process can be completed within a shorter time interval. A simulation detail illustrating the balancing operation of $H_{Sym\text{-}S3V}$ can be observed in Figure 7.4 (see $v_{C1}$ being driven to 900 V at 0.04 s, when the $H_{Sym\text{-}S3V}$ is applied).

## 7.5 Conclusion

This chapter presented a simple concept for creating hybrid modulation strategies that can eliminate NP voltage ripple from the NPC converter. The proposed hybrid strategies can be based on existing NV and non NV strategies, combining the two in a way that minimizes the converter's switching losses and output voltage harmonic distortion. The benefit offered in comparison to non NV strategies (which also eliminate NP voltage ripple) increases with the load power factor and decreases with the converter modulation index. The performance of the proposed concept is also enhanced as compared to other approaches for the creation of hybrid strategies. Its operation was demonstrated for different combinations of strategies and with non linear and imbalanced loads.

# Chapter 8

## Conclusions

## 8.1 Thesis conclusions and contribution

In accordance with the objectives outlined in Section 1.3, the first part of this Thesis analysed the dc-link capacitor current of 3L NPC and CHB inverters, associating it with the induced voltage-current stress and required capacitor size. The study focused on common modulation strategies, such as the SPWM, the SPWM with 3$^{rd}$ harmonic injection, and the conventional SVM. It revealed that, for any of these strategies, the total capacitor size required for the CHB inverter is at least three times higher than that for the NPC inverter.

The capacitor size was estimated using a number of analytical and numerical methods, giving the rms value and harmonics of the dc-link capacitor current. As compared to the analytical rms current derivations, the proposed numerical approach provided a simpler alternative for deriving capacitor losses and peak-peak capacitor voltage. Moreover, in contrast to the illustrated method for harmonically analysing the capacitor current, the approach can be easily applied to different (e.g. discontinuous) modulation strategies.

The harmonic analysis, on the other hand, can be extended in a simple way to multiple inverter systems with a common dc-link capacitor. It also offers the possibility to investigate the effect of introducing a reference/carrier phase shift between the inverter waveforms on the capacitor size. The study presented in Chapter 4 covered single-phase (CHB) and three-phase 2L inverter systems comprising two or three inverters, and derived the optimal phase shifts for each case. Regarding single-phase inverter systems, it was shown that for reference phase shifts that cancel the low-frequency (baseband) harmonic, a decrement of approximately 15% for two-inverter and 35% for three-inverter systems can be achieved in the capacitor rms current, respectively. For three-phase inverter systems, this decrement reaches 40% and 50%, respectively.

The second part of this Thesis focused on the NPC converter, covering its last two objectives (as in Section 1.3). Chapter 5 presented a circuit for reducing the voltage stress caused by the NP voltage ripple on the modules of the NPC converter. The circuit is based on low-voltage components, which have smaller size and cost as compared to the components of other balancing circuits. On the other hand, the NPS circuit has the disadvantages of not reducing the voltage stress on the converter's dc-link capacitors, as well as of needing to be pre-charged before operating the converter. In relation to the conventional solution of over-sizing the inverter dc-link capacitors, the use of the circuit is expected to be advantageous

when the restriction on the NP voltage variation becomes stricter, since the voltage rating of the circuit components decreases accordingly.

The last two chapters of this Thesis provided the basis for creating modulation strategies with optimal performance with respect to NP voltage ripple generation in the NPC converter:

- Under the restriction of exclusively using the nearest vectors, the concept of Band-NV strategies set the framework for developing modulation strategies with the minimum possible NP voltage ripple.
- When the nearest vector restriction is removed, the proposed Hybrid strategies offered a simple way to eliminate NP voltage ripple, introducing minimum additional converter losses and output voltage distortion.

Regarding Band-NV strategies, particular attention was given to the operating range of NPC converters as motor drives ($PF \approx 0.85$). In that range, the conversion of a conventional to a Band-NV strategy can decrease the NP voltage ripple or the required dc-link capacitance by 30 to 50%. Although in comparison to the respective conventional NV strategies a small increase in switching losses can be expected when the converter operates at a high modulation index, this increase was shown to not affect the converter's rated switching frequency. Furthermore, the performance of Band-NV strategies was examined for highly reactive loads ($PF \approx 0$), appearing for example in STATCOM applications, where no reduction of NP voltage ripple can be offered, as well as for operation of the NPC converter as an AFE ($PF < 0$).

The distinction between controllable and uncontrollable intervals introduced in the previous study, led to the creation of hybrid modulation strategies. The proposed hybrid strategies can combine existing NV and non NV strategies to eliminate NP voltage ripple from the NPC converter. As compared to non NV strategies or to other approaches for the creation of hybrid strategies, the proposed approach was shown to minimize the converter's switching losses and output voltage harmonic distortion. It is also important that the approach can operate with non linear or imbalanced loads, always achieving elimination of NP voltage ripple.

## 8.2 Future work

### 8.2.1 Experimental results

All results presented in this Thesis were extensively validated using simulations in MATLAB-Simulink (SimPowerSystems toolbox). MATLAB code was also incorporated in Simulink models to implement elaborate procedures, such as the algorithms of Band-NV and Hybrid strategies for the NPC converter. The simulations can be expected to have provided a close representation of a real converter operation due to the level of detail embedded in them, as well as due to the nature of the problems studied in this Thesis. Namely, the waveform of the dc-link capacitor current, which determines the capacitor current rms value/harmonics and voltage ripple, is not dependent on parameter-sensitive phenomena (e.g. resonances), parasitic elements (e.g. parasitic capacitance to ground for common-mode currents), or selected converter modules. A simulation model can therefore reproduce the dc-link capacitor current in an experimental setup with greater accuracy compared to other effects which are affected by the above. Nevertheless, experimental work is also necessary to further investigate issues such as:

- Physical construction limitations in multiple inverter systems, where the length of dc-link busbars should be limited to avoid increasing their inductance.
- Pre-charging circuit for the NPS circuit.
- For the NPC converter modulation strategies,
    - algorithm implementation details and computational requirements
    - effect of dead time between converter switchings
    - operation at low switching frequencies and effect of sampling

With regards to modulation strategies for the NPC converter in particular, it should be noted that the aim of Chapters 6 and 7 was to set the basis for the creation of different Band-NV and hybrid strategies, respectively. They therefore focused on the proposed concepts, rather than on a specific strategy or experimental implementation. Simulation results were accordingly included to validate the operation of the proposed concepts at different converter operating conditions and types of load, rather than to precisely quantify parameters like converter losses and output voltage distortion, which are dependent on the implemented strategy. Experimental results will be part of studies comparing the performance of strategies

built according to the proposed concepts. Preliminary results are described in the following sections.

### 8.2.2 Extension of work on Band-NV strategies

Chapter 6 presented the concept of Band-NV strategies and explained how it can be applied to different NV strategies. There is therefore an open question as to which Band-NV strategy can perform better with regards to parameters like NP voltage ripple, effective switching frequency and output voltage harmonic distortion. Future work in this area will examine a number of Band-NV strategies, with the aim of addressing the above question. In this section, results for the Symmetric strategy (see Appendix A.3) are summarized and compared to those for the NTV strategy, included in Chapter 6.

As explained in Section 6.3.2, the switching constraints of the NTV strategy allow it to attain the values of $i_{NP,hi}$, $i_{NP,lo}$, and thus $\Delta V_{NP,min}$, for any value of $m$. The Symmetric strategy's constraints (*SC* will refer to them in this section), on the other hand, affect the highest and lowest values that $i_{NP}$ can take (observe the notches on the waveforms of $i_{NP,hi}$ and $i_{NP,lo}$ in Figure 8.1, which do not appear in Figure 6.3).

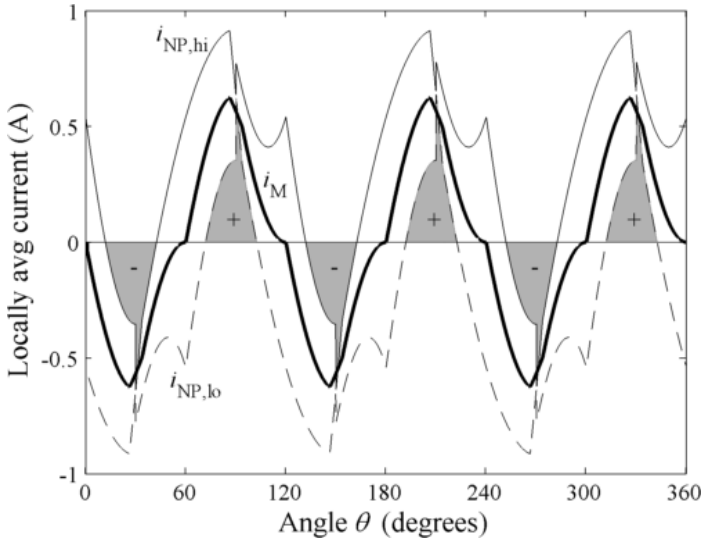


**Figure 8.1.** Waveforms of $i_{NP,hi|SC}$ and $i_{NP,lo|SC}$ for the Symmetric strategy, for $\phi = -30$ degrees and $m = 0.9$.

As a consequence, the minimum value of NP voltage ripple, $\Delta V_{NP,min|SC}$, is increased for $m < 1$ as compared to $\Delta V_{NP,min}$. Figure 8.2 plots $\Delta V_{NP,min|SC}$ for the Symmetric strategy and its Band-NV equivalent, which will be referred to as Band-Sym strategy.

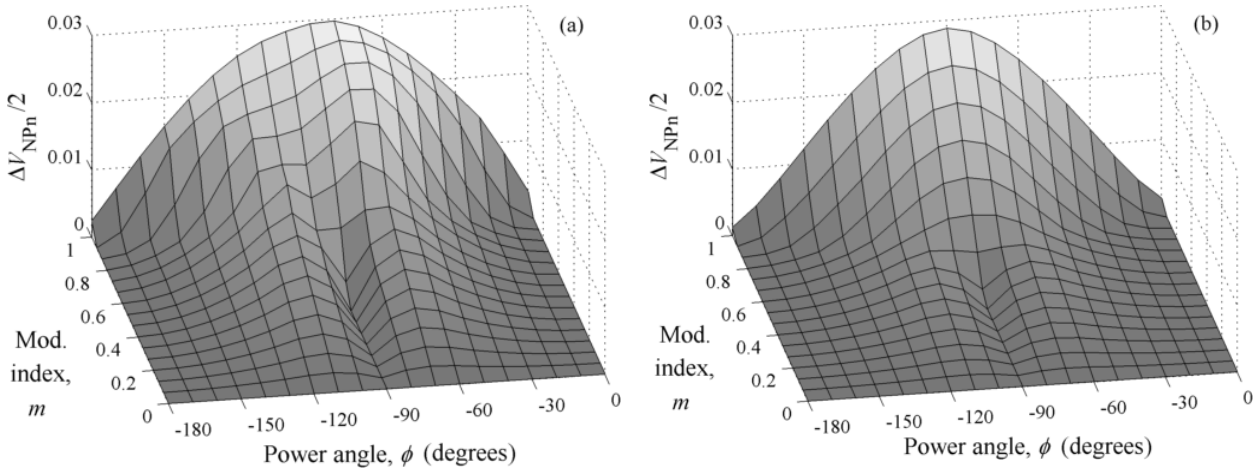


**Figure 8.2.** Normalized amplitude of NP voltage ripple ($\Delta V_{NPn|SC}/2$) for the (a) Symmetric, and (b) Band-Sym strategy.

The value of *decr* for the Symmetric and Band-Sym strategies is shown in Figure 8.3. It can be observed that the part of the plot where *decr* is exactly equal to 50% differs significantly in comparison to the NTV strategy (see Figure 6.11). This is due to the fact that, as shown in Figure 8.4, Region 1 for the Symmetric (and Band-Sym) strategy covers the part of Region 0 illustrated in Figure 6.6.

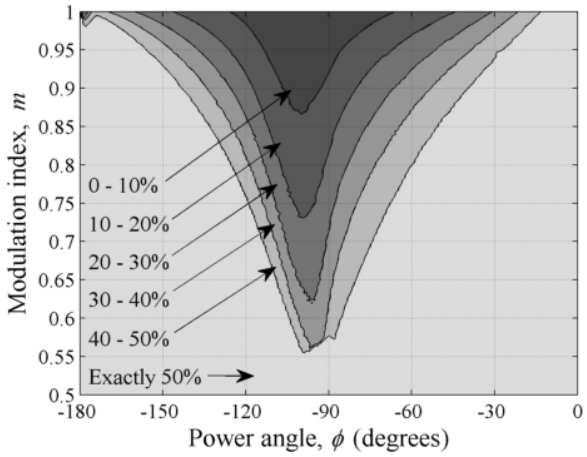


**Figure 8.3.** Value of *decr* as a function of $\phi$ and $m$, for the Symmetric and Band-Sym strategies.

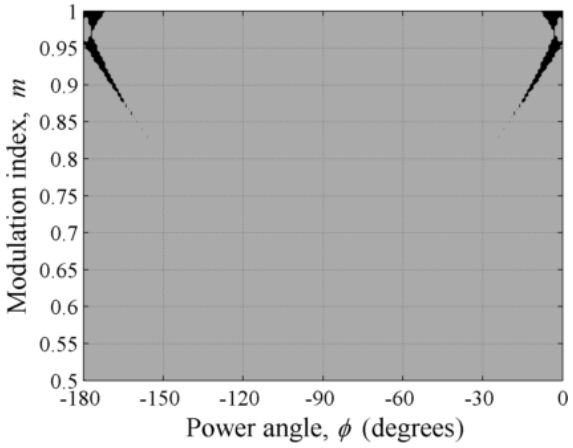


**Figure 8.4.** Regions of converter operation for the Symmetric strategy: (Grey) Region 1, (Black) Region 2**.**

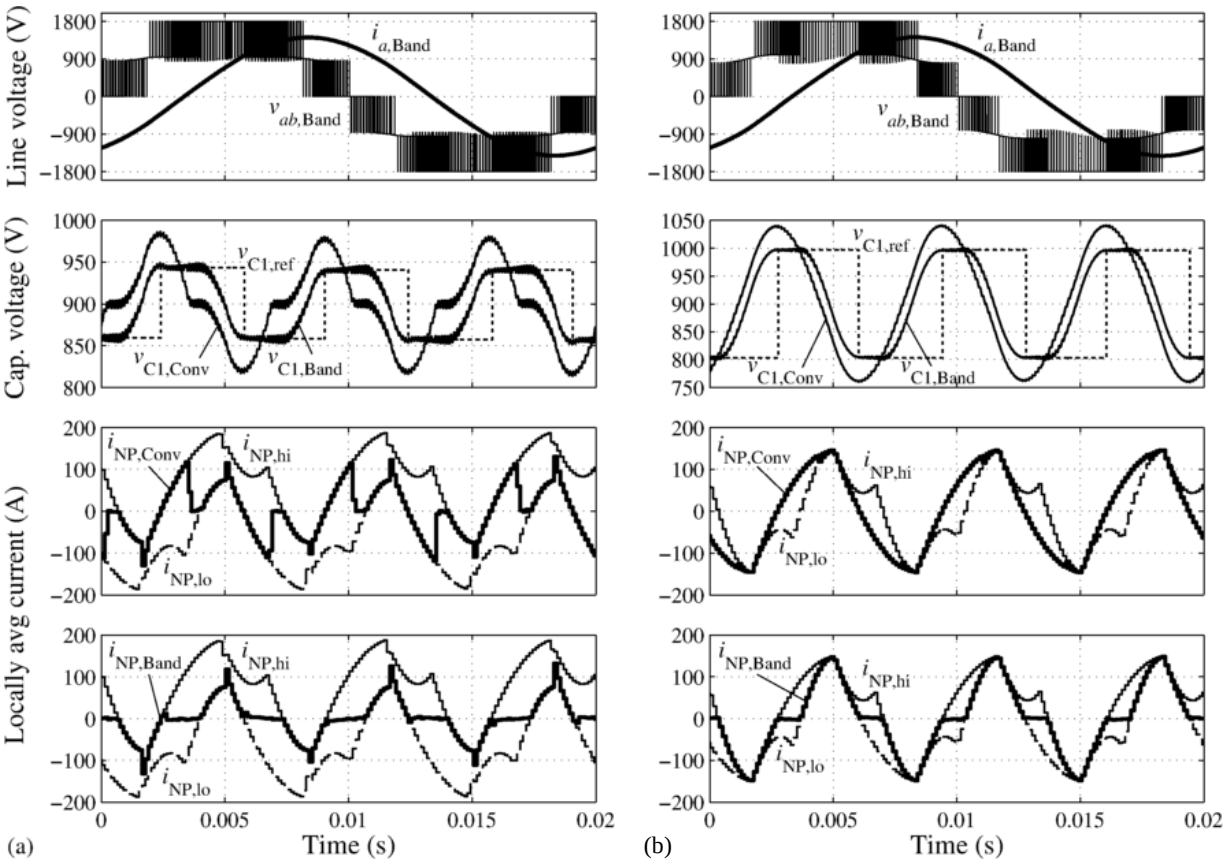


**Figure 8.5.** Simulation comparing the Band-Sym to the Symmetric strategy during a fundamental cycle, for $\phi$ = −30 degrees and (a) $m$ = 0.9, (b) $m$ = 1. *i*) (top) Line voltage $v_{ab}$ and current 5×$i_a$, *ii*) $v_{C1,Conv}$, $v_{C1,Band}$ and $v_{C1,ref}$, *iii*) $i_{NP,Conv}$, $i_{NP,lo}$ and $i_{NP,hi}$, and *iv*) (bottom) $i_{NP,Band}$, $i_{NP,lo}$ and $i_{NP,hi}$.

Figure 8.5 presents simulation results for the Symmetric and Band-Sym, which can be compared to Figure 6.12 for the NTV and Band-NTV strategies. Zero-$i_{NP}$ intervals can be observed more clearly in Figure 8.5, since $i_{NP}$ for the Symmetric and Band-Sym strategies is equal to zero during these intervals. The increased duration of zero-$i_{NP}$ intervals for the Band-Sym leads to an increased effective switching frequency in comparison to the Symmetric strategy, as shown in Figure 8.6. In comparison to the NTV and Band-NTV strategies, the figure also illustrates that for the above strategies the amplitude of NP voltage ripple is higher for $m < 1$, but not for the critical value of $m = 1$ (since, as explained in Section 6.3.2, when $m$ approaches 1, $\Delta V_{NP,min|SC}$ approaches $\Delta V_{NP,min}$).

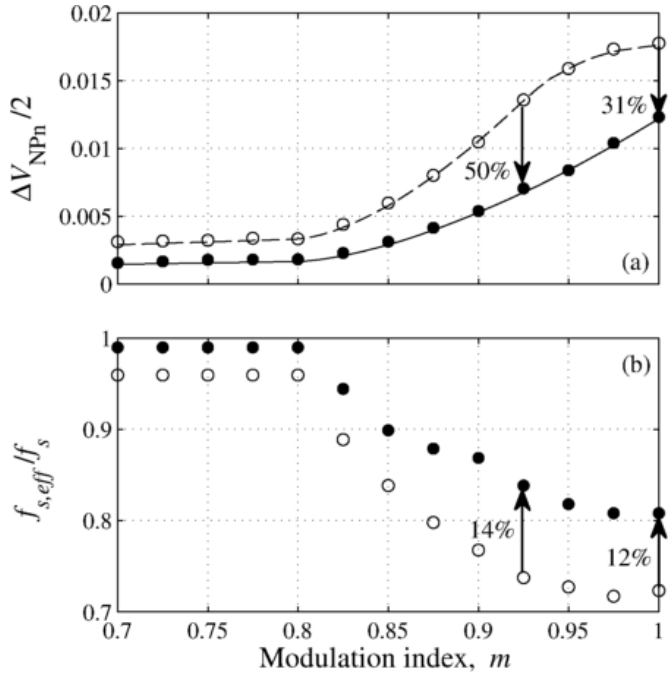


**Figure 8.6.** For $\phi = -30$ degrees and $m \geq 0.7$, (a) Normalized amplitude of NP voltage ripple: (continuous line) $\Delta V_{Band\text{-}Sym}/2$, (dashed line) $\Delta V_{Sym}/2$, (filled circles) Simulation for Band-Sym strategy, (empty circles) Simulation for Symmetric strategy, and (b) Ratio of $f_{s,eff}$ over $f_s$.

Finally, apart from the formulation and comparison of different Band-NV strategies, the work in this area can be extended with:

- Carrier-based implementations of Band-NV strategies (similarly to [41]).
- Feed-forward techniques (see [8], [29], [30]) adapted for application with Band-NV strategies.
- Studies investigating the operation of Band-NV strategies with non linear or imbalanced loads.

### 8.2.3 Extension of work on Hybrid strategies

As for the case of Band-NV strategies, there is an open question on defining a hybrid strategy that is optimized w.r.t. converter switching losses and output voltage distortion. Future studies will investigate different hybrid (i.e. combinations of NV and non NV) strategies to address this question, thus providing a practically valuable solution for NP voltage ripple elimination to NPC converter designers.

Finally, the proposed concept on hybrid strategies can be modified with the aim of creating strategies that can limit the NP voltage ripple to a desired extent (similarly to [52, 70]). Again, given the amplitude of NP voltage ripple, the created hybrid strategies can be studied further to minimize switching losses and output voltage distortion by appropriately defining the intervals when the selected NV/non NV strategy should be used.

# Appendix A

## SVM for the NPC converter – MATLAB-Simulink models

Sections A.1 – A.3 of this Appendix provide supplementary material on NV strategies for the NPC converter, while Section A.4 presents representative models/implementations of calculations, converters, and modulation algorithms in MATLAB-Simulink.

### A.1 Calculation of duty cycles for nearest Space Vectors

As explained in Section 6.3, the SV diagram of a three-level converter can be divided into six sextants. Each of them consists of four small triangles, $tr_1$ – $tr_4$, illustrated in Figure A.1. For NV strategies, the duty cycles of Space Vectors are derived from (2.15), where $\mathbf{V_1}$, $\mathbf{V_2}$, …, $\mathbf{V_n}$, are the NVs for each small triangle. Solution of the above equations does not distinguish between small (also zero) vectors that share the same position on the SV plane. Thus, the derived values of $d_{S0}$, $d_{S1}$, and $d_Z$ can be arbitrarily distributed between {$\mathbf{S0_1}$, $\mathbf{S0_2}$}, {$\mathbf{S1_1}$, $\mathbf{S1_2}$}, and {$\mathbf{Z_1}$, $\mathbf{Z_2}$, $\mathbf{Z_3}$}, respectively.

The expressions for the duty cycles of NVs are taken from [62], and include a correction in (A.3). It is noted that for the purposes of this section, angle $\theta$ stands for the angle of $\mathbf{V_{REF}}$ w.r.t. **L0**, in the sextant where $\mathbf{V_{REF}}$ belongs (see Figure A.1).

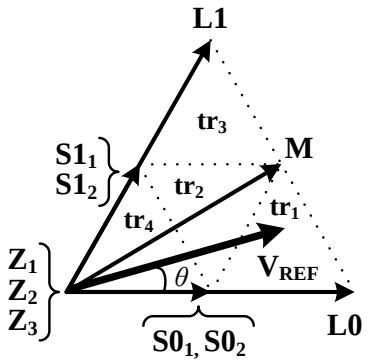


**Figure A.1.** Space Vectors and triangles $tr_1$ – $tr_4$, in one sextant of a three-level converter.

Triangle $tr_1$: {**S0₁**, **S0₂**}, **M**, **L0**

$$d_{\mathrm{S0,tr1}} = 2 - m\left(\sqrt{3}\cos\theta + \sin\theta\right), \quad \textbf{(A.1)}$$

$$d_{\mathrm{M,tr1}} = 2m\sin\theta\ , \quad \textbf{(A.2)}$$

$$d_{\mathrm{L0,tr1}} = -1 + m\left(\sqrt{3}\cos\theta - \sin\theta\right), \quad \textbf{(A.3)}$$

Triangle $tr_2$: {**S0₁**, **S0₂**}, {**S1₁**, **S1₂**}, **M**

$$d_{\mathrm{S0,tr2}} = 1 - 2m\sin\theta, \quad \textbf{(A.5)}$$

$$d_{\mathrm{S1,tr2}} = 1 + m\left(\sin\theta - \sqrt{3}\cos\theta\right), \quad \textbf{(A.6)}$$

$$d_{\mathrm{M,tr2}} = -1 + m\left(\sin\theta + \sqrt{3}\cos\theta\right), \quad \textbf{(A.7)}$$

Triangle $tr_3$: {**S1₁**, **S1₂**}, **M, L1**

$$d_{\mathrm{S1,tr3}} = 2 - m\left(\sqrt{3}\cos\theta' + \sin\theta'\right), \quad \textbf{(A.8)}$$

$$d_{\mathrm{M,tr3}} = 2m\sin\theta'\ , \quad \textbf{(A.9)}$$

$$d_{\mathrm{L1,tr3}} = -1 + m\left(\sqrt{3}\cos\theta' - \sin\theta'\right), \quad \textbf{(A.10)}$$

where $\theta' = \pi/3 - \theta$.

Triangle $tr_4$: {**Z₁**, **Z₂**, **Z₃**}, {**S0₁**, **S0₂**}, {**S1₁**, **S1₂**}

$$d_{\mathrm{Z,tr3}} = 1 - m\left(\sqrt{3}\cos\theta + \sin\theta\right), \tag{A.11}$$

$$d_{\mathrm{S0,tr3}} = m\left(\sqrt{3}\cos\theta - \sin\theta\right), \tag{A.12}$$

$$d_{\mathrm{S1,tr3}} = 2m\sin\theta\,. \tag{A.13}$$

## A.2 NP current rms value

This section presents an analytical derivation of the NP current rms value, used to plot the graph in Figure 5.4 and determine the NPS circuit current rating in Section 5.2.3.

The absolute value of the NP current is periodic with a period of π/3. Therefore, the analysis of one sextant of the SV diagram (see Figure A.1) is adequate to derive its rms value. It can be readily shown that for modulation index $m > 1/\sqrt{3} = 0.577$, $\mathbf{V_{REF}}$ passes from the outer and middle small triangles ($tr_1$, $tr_2$ and $tr_3$) without falling in the inner triangle ($tr_4$). This is the region of modulation index values where the inverter practically operates, and NP voltage ripple starts to appear [1]. For a given $m > 0.577$, the angles of transition from triangle $tr_1$ to $tr_2$, and from $tr_2$ to $tr_3$ are $\theta_{tr}$ and $(\pi/3 - \theta_{tr})$, respectively, where

$$\theta_{tr} = \arccos\left(\frac{1}{2M}\right) - \frac{\pi}{6}\quad . \tag{A.14}$$

Using the expressions for the small and medium vector duty cycles from Section A.1, as well as the NP current associated with each vector in the first sextant (see Figure 6.1), the rms NP current ($I_{\mathrm{NP},rms}$) can be calculated from

$$I_{NP,rms}^2 = \frac{1}{\pi/3}\left\{\begin{array}{l} \displaystyle\int_0^{\theta_{tr}} \left(d_{\mathrm{S0,tr1}}\cdot i_a^2 + d_{\mathrm{M,tr1}}\cdot i_b^2\right)d\theta \\ \displaystyle + \int_{\theta_{tr}}^{\pi/3-\theta_{tr}} \left(d_{\mathrm{S0},tr2}\cdot i_a^2 + d_{\mathrm{S1,tr2}}\cdot i_c^2 + d_{\mathrm{M,tr2}}\cdot i_b^2\right)d\theta \\ \displaystyle + \int_{\pi/3-\theta_{tr}}^{\pi/3} \left(d_{\mathrm{S1},tr3}\cdot i_c^2 + d_{\mathrm{M,tr3}}\cdot i_b^2\right)d\theta \end{array}\right\}\quad . \tag{A.15}$$

Numerical calculation of (A.15) gives the plot of Figure 5.4. The plotted values have also been verified with NPC inverter simulations using the SimPowerSystems toolbox of

MATLAB-Simulink. As explained in Section 6.3, different NV modulation strategies can be defined, depending on the distribution of $d_{S0}$ and $d_{S1}$ among the two small vectors of the respective pair. However, since both vectors of each pair cause the same current amplitude (only the sign changes, which cancels when squaring) to flow to/from the converter NP, the above distribution does not affect the rms value of the NP current. Consequently, (A.15) and Figure 5.4 are valid for any NV strategy.

## A.3 Symmetric modulation strategy

This section describes the Symmetric modulation strategy, presented in [51] and discussed in Chapters 6 and 7. The switching constraints and switching sequences for the 1st sextant of this strategy are presented in Table A.1.

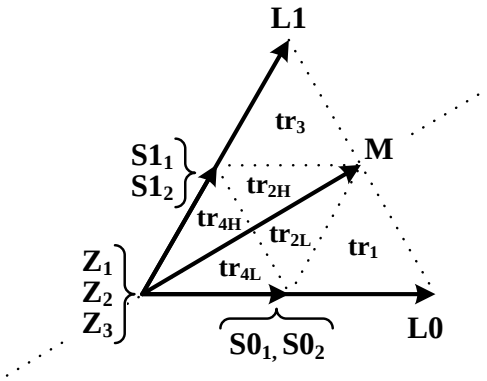


**Figure A.2.** Space Vectors and small triangles for the Symmetric strategy.

It can be observed that all switching constraints refer to triangles $tr_2$ and $tr_4$. Namely, in the higher/lower half of these triangles, the distribution factor $x_{S0}/x_{S1}$, respectively, can only take the value of −1. As explained in Section 6.3.2, this restriction affects the amplitude of NP voltage ripple for $m < 1$. However, it is imposed in order to create a set of switching sequences, each of which comprises 6 switching steps.

| Triangle | $x_{S0}$ | $x_{S1}$ | Switching sequence | Steps |
|---|---|---|---|---|
| $tr_1$ | free | n/a | 100-200-210-211-210-200-100 | 6 |
| $tr_{2L}$ | free | −1 | 100-110-210-211-210-110-100 | 6 |
| $tr_{2H}$ | −1 | free | 110-210-211-221-211-210-110 | 6 |
| $tr_3$ | n/a | free | 110-210-220-221-220-210-110 | 6 |
| $tr_{4L}$ | free | −1 | 100-110-111-211-111-110-100 | 6 |
| $tr_{4H}$ | −1 | free | 110-111-211-221-211-111-110 | 6 |

**Table A.1.** Duty cycle distribution factors and switching sequences for the Symmetric strategy **[51]**.

## A.4 MATLAB-Simulink models

This section includes the following:

*i.* MATLAB code for numerical calculation of (normalized) dc-link capacitor rms current and peak-peak voltage ripple for NPC and CHB inverters.

*ii.* Simulink model of the "Vector selection" block used by SVM for the NPC converter.

*iii.* Simulink model of NPC converter with NPS circuit.

*iv.* Simulink model of NPC converter modulated with the Band-NTV strategy.

*v.* MATLAB code embedded to the "Band-NV PWM generator" block in the Simulink model of NPC converter modulated with the Band-NTV strategy (implementing the Band-NV algorithm).

### *i) MATLAB code for numerical calculation of (normalized) dc-link capacitor rms current and peak-peak voltage ripple for NPC and CHB inverters.*

```
%INPUTS
%--------------------------------
M = 2/sqrt(3); % Modulation index
phi = 30/180*pi; % Power angle in rads
strategy = 2; % 1:SPWM, 2:SPWM+1/6 3rd harm., 3: SVM
HBperPh = 2; % Number of H-bridge cells (per phase) for the ML CHB
%--------------------------------

%NORMALISATION
%--------------------------------
f = 1; % Reference frequency in Hz
C = 1; % Capacitance of dc-link capacitors in F
Io_mag = sqrt(2); % Magnitude of phase current in A
%--------------------------------

%CALCULATION
%--------------------------------
dTheta = 2*pi/180;
count = 0;
i_d_NPC_rmssq = 0; % i.e. i_d_NPC_rms square
i_d_NPC_dc = 0;
i_d_CHB_rmssq = 0; % i.e. i_d_CHB_rms square
i_d_CHB_dc = 0;
i_d_NPC = zeros(1);
i_d_CHB = zeros(1);
i_d_CHB_rmssq_ml = zeros(10);
i_d_CHB_dc_ml = zeros(10);
i_d_CHB_ml = zeros(1,1);
duty_ml = zeros(1);

for theta = 0:dTheta:2*pi-dTheta
    count = count + 1;

    %Duty cycle calculation
    dutyA = M*cos(theta);
    dutyB = M*cos(theta - 2*pi/3);
    dutyC = M*cos(theta + 2*pi/3);

    cmSignal = 0; % Common-mode voltage reference signal
    if strategy == 2
        cmSignal = -1/6*M*cos(3*theta);
    else if strategy == 3
            dutyABC = [dutyA dutyB dutyC];
            cmSignal = -0.5*(max(dutyABC) + min(dutyABC));
        end
    end
    dutyA = dutyA + cmSignal;
    dutyB = dutyB + cmSignal;
    dutyC = dutyC + cmSignal;

    %Three-phase currents
    iA = Io_mag*cos(theta-phi);
    iB = Io_mag*cos(theta-phi-2*pi/3);
    iC = Io_mag*cos(theta-phi+2*pi/3);
    I3ph = [iA iB iC];

    %NPC inverter calculations
    [dutySorted, indices] = sort([dutyA*(dutyA > 0) dutyB*(dutyB > 0) dutyC*(dutyC > 0)],
'ascend');

    duty1 = dutySorted(1);
    duty2 = dutySorted(2);
    duty3 = dutySorted(3);
    i1 = I3ph(indices(1));
    i2 = I3ph(indices(2));
    i3 = I3ph(indices(3));
    i_d_NPC_rmssq = i_d_NPC_rmssq + (duty2-duty1)*(i2+i3)^2 + (duty3-duty2)*(i3)^2;
    i_d_NPC(count) = iA*dutyA*(dutyA > 0) + iB*dutyB*(dutyB > 0) + iC*dutyC*(dutyC > 0);
    i_d_NPC_dc = i_d_NPC_dc + i_d_NPC(count);
```

```
    %CHB inverter calculations
    i_d_CHB_rmssq = i_d_CHB_rmssq + iA^2*abs(dutyA);
    i_d_CHB(count) = iA*dutyA;
    i_d_CHB_dc = i_d_CHB_dc + i_d_CHB(count);

    %Multilevel CHB (CHB ML) inverter calculations
    HBhigh = floor(abs(dutyA)*HBperPh); %Number of cells with duty cycle = +/-1 (for phase A)
    HBduty = HBperPh * mod(abs(dutyA), 1/HBperPh);

    for n = 1:HBperPh
        if n <= HBhigh
            duty_ml(n) = sign(dutyA); % Duty cycle of the HBhigh lower cells
        else
            duty_ml(n) = 0; % Duty cycle of the (HBhigh+2) up to the highest-level cell
        end
    end
    duty_ml(HBhigh + 1) = sign(dutyA)*HBduty; % Duty cycle of the (HBhigh+1)-level cell

    for n = 1:HBperPh
        i_d_CHB_rmssq_ml(n) = i_d_CHB_rmssq_ml(n) + iA^2*abs(duty_ml(n));
        i_d_CHB_ml(count,n) = iA*duty_ml(n);
        i_d_CHB_dc_ml(n) = i_d_CHB_dc_ml(n) + i_d_CHB_ml(count,n);
    end

end

%RESULTS
%--------------------------------

%NPC inverter results
fprintf('\n\nNPC\n------------------');
i_d_NPC_rmssq = i_d_NPC_rmssq*dTheta/(2*pi);
i_d_NPC_dc = i_d_NPC_dc*dTheta/(2*pi);
i_C_NPC_rms = sqrt(i_d_NPC_rmssq - i_d_NPC_dc^2) %Capacitor rms current for NPC

i_C_NPC = i_d_NPC - i_d_NPC_dc;
dQ_C_NPC = i_C_NPC.*dTheta/(2*pi*f);
Q_C_NPC = cumsum(dQ_C_NPC);
Q_C_NPCpp = max(Q_C_NPC) - min(Q_C_NPC);
V_C_NPCpp = Q_C_NPCpp/C %Capacitor peak-peak voltage ripple for NPC

%CHB inverter results
fprintf('\n\nCHB\n------------------');
i_d_CHB_rmssq = i_d_CHB_rmssq*dTheta/(2*pi);
i_d_CHB_dc = i_d_CHB_dc*dTheta/(2*pi);
i_C_CHB_rms = sqrt(i_d_CHB_rmssq - i_d_CHB_dc^2) %Capacitor rms current for CHB

i_C_CHB = i_d_CHB - i_d_CHB_dc;
dQ_C_CHB = i_C_CHB.*dTheta/(2*pi*f);
Q_C_CHB = cumsum(dQ_C_CHB);
Q_C_CHBpp = max(Q_C_CHB) - min(Q_C_CHB);
V_C_CHBpp = Q_C_CHBpp/C %Capacitor peak-peak voltage ripple for CHB

%CHB ML inverter results
for n = 1:HBperPh
    fprintf('\n\nML CHB, Cell %d \n------------------',n);
    i_d_CHB_rmssq_ml(n) = i_d_CHB_rmssq_ml(n)*Dtheta/(2*pi);
    i_d_CHB_dc_ml(n) = i_d_CHB_dc_ml(n)*Dtheta/(2*pi);
    i_C_CHB_rms_ml = sqrt(i_d_CHB_rmssq_ml(n) - i_d_CHB_dc_ml(n)^2)

    i_C_CHB_ml = i_d_CHB_ml(:,n) - i_d_CHB_dc_ml(n);
    dQ_C_CHB_ml = i_C_CHB_ml.*Dtheta/(2*pi*f);
    Q_C_CHB_ml = cumsum(dQ_C_CHB_ml);
    Q_C_CHBpp_ml = max(Q_C_CHB_ml) - min(Q_C_CHB_ml);
    V_C_CHBpp_ml = Q_C_CHBpp_ml/C
end
```

***ii) Simulink model of the "Vector selection" block used by SVM for the NPC converter.***

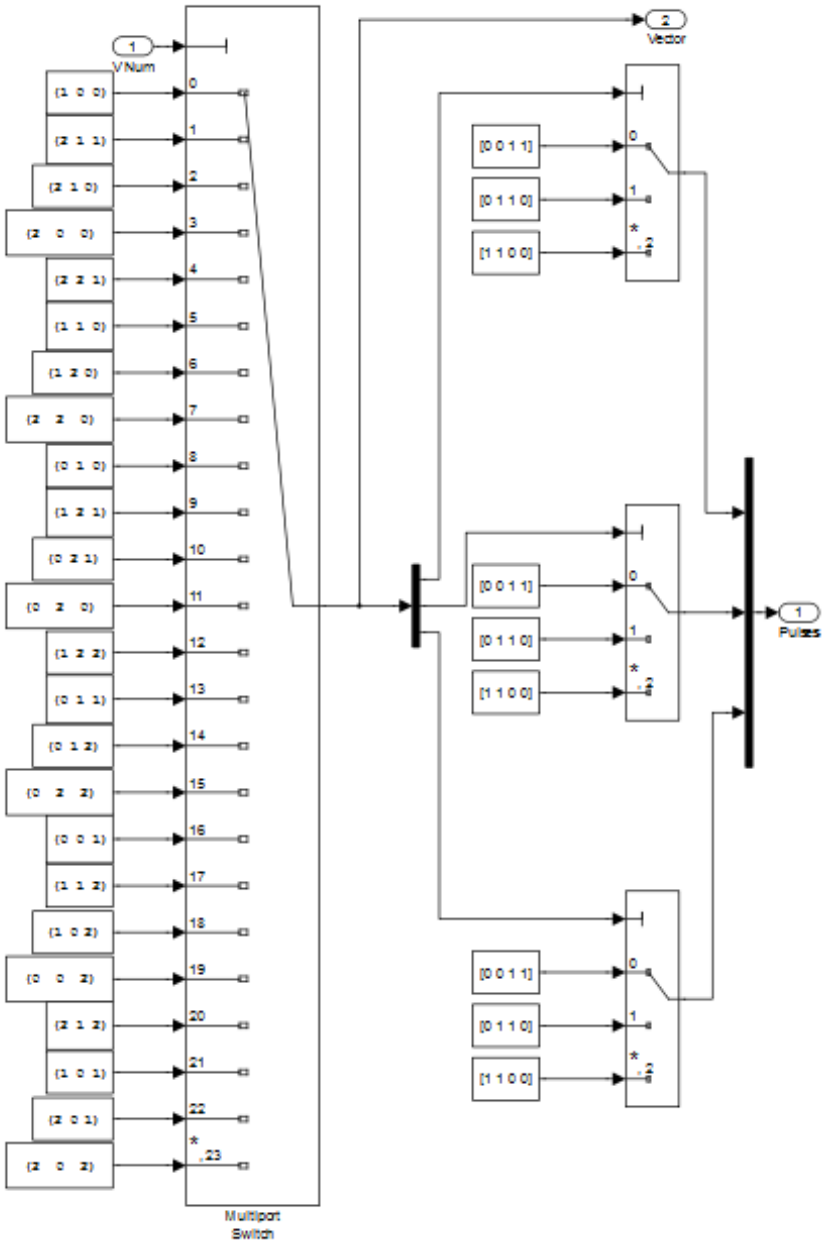


**Figure A.3.** Vector selection block.

***iii)Simulink model of NPC converter with NPS circuit.***

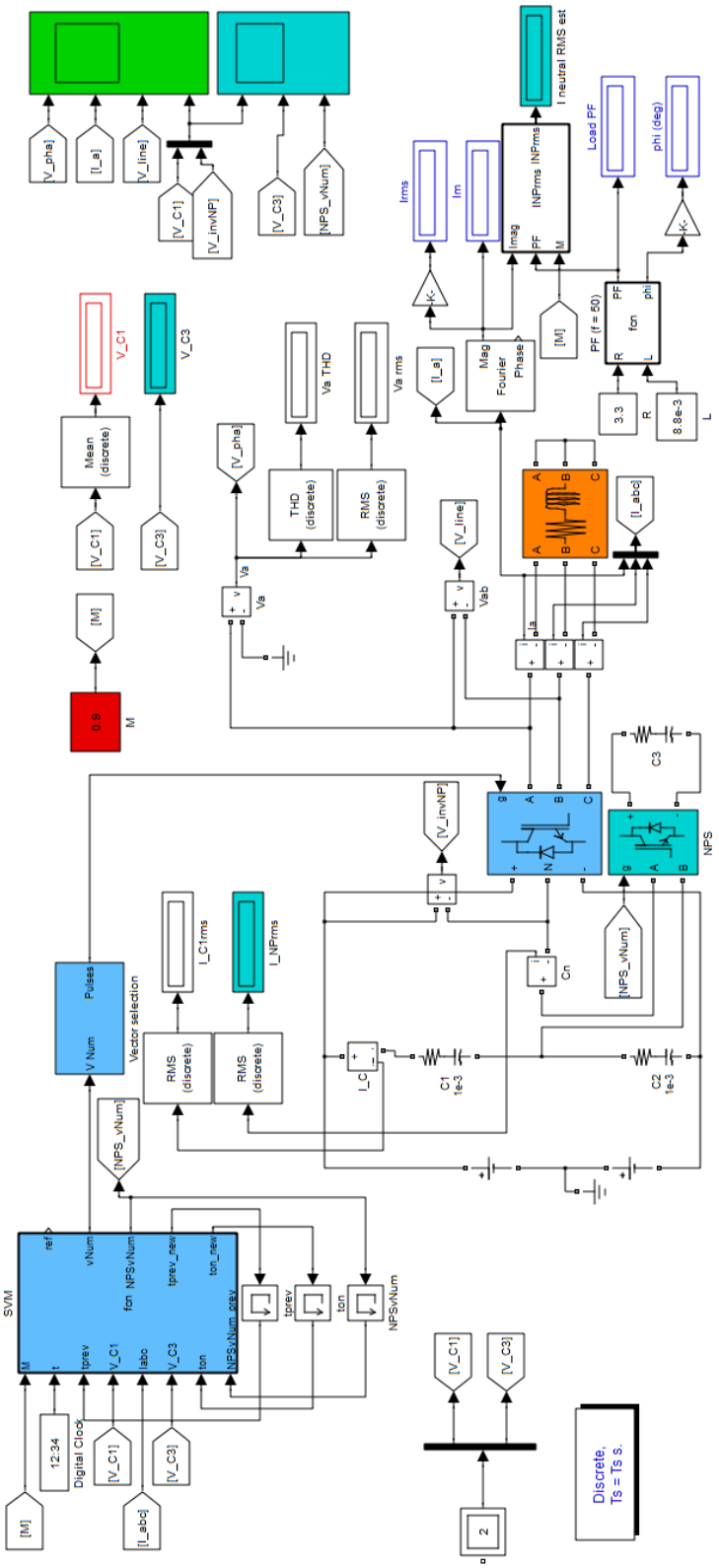


**Figure A.4.** Simulink model of NPC converter with NPS circuit.

***iv) Simulink model of NPC converter modulated with the Band-NTV strategy.***

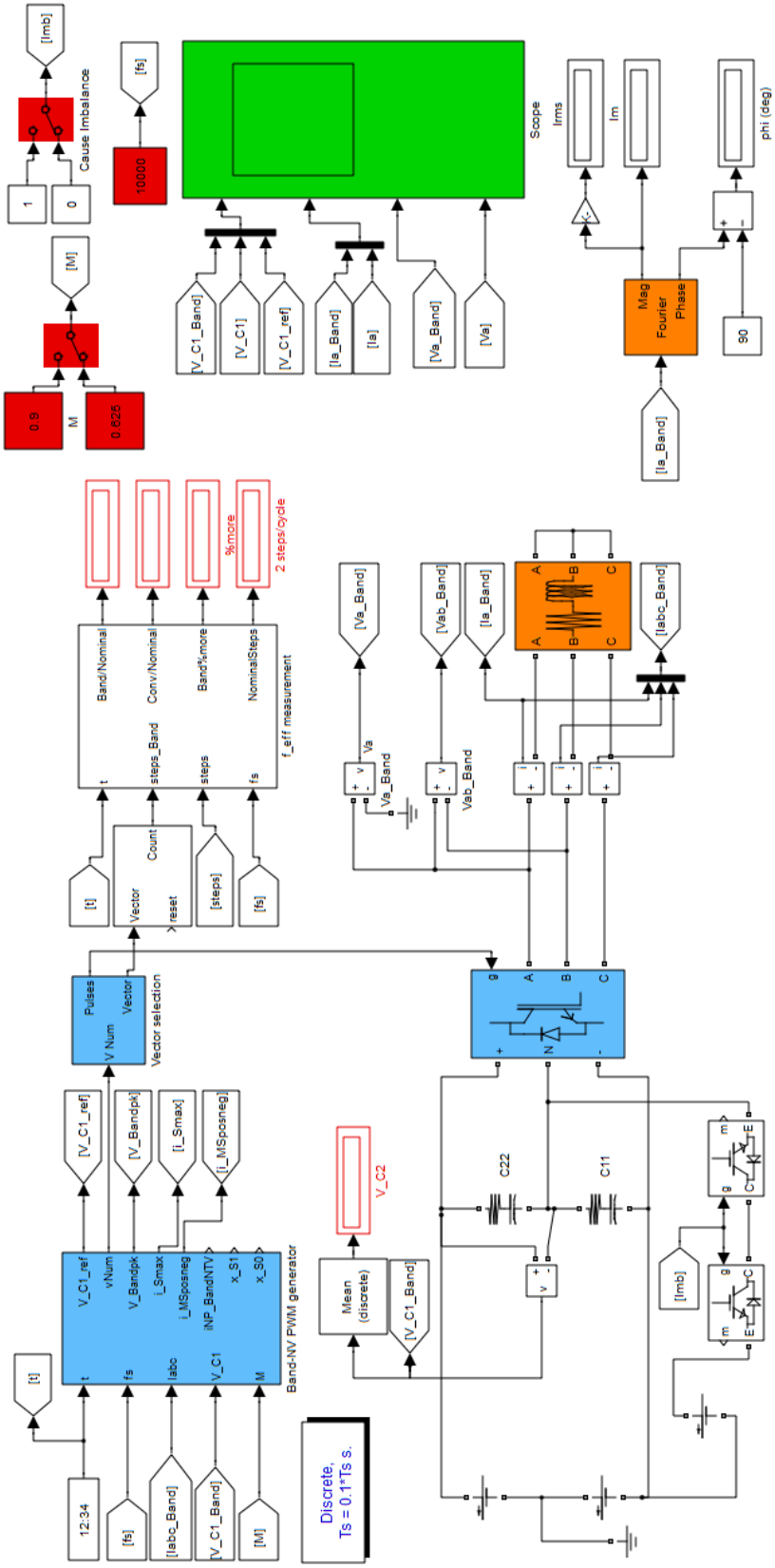


**Figure A.5.** Simulink model of NPC converter modulated with the Band-NTV strategy.

### *v) MATLAB code embedded to the "Band-NV PWM generator" block in the Simulink model of NPC converter modulated with the Band-NTV strategy.*

```
% NOTE: The code below operates through an interface to the "Band-NV PWM generator" block.

function
[vNum,i_M,i_Spos,i_Sneg,tprev_new,Vbeg,ContInt,V_C1_ref,sM,UI_Flag,UIsign,t_sM,bal_Flag,balOK
,Region,sV_C1,V_Bandpk,DQcross_flag,Vector1,Vector2,Vector3,Vector4,Time1,Time2,Time3,Time4,i
_Smax,iNP_BandNTV,x_S1,x_S0] = ...

fcn(t,fs,tprev,V_C1,Iabc,M,vNum_prev,i_M_prev,i_Spos_prev,i_Sneg_prev,Vbeg_prev,ContInt_prev,
sM_prev,UI_Flag_prev,UIsign_prev,t_sM_prev,bal_Flag_prev,balOK_prev,Region_prev,sV_C1_prev,V_
Bandpk_prev,DQcross_flag_prev,V_C1_ref_prev,Vector1_prev,Vector2_prev,Vector3_prev,Vector4_pr
ev,Time1_prev,Time2_prev,Time3_prev,Time4_prev,i_Smax_prev,iNP_BandNTV_prev,x_S1_prev,x_S0_pr
ev)

%INPUT
f = 50;
Vnom = 900;
C = 0.5e-3;
% x_max = 1;
notUsing8stepsForSmallBalancing = 1;

%Hold the values below, unless they change later
Vector1 = Vector1_prev;
Vector2 = Vector2_prev;
Vector3 = Vector3_prev;
Vector4 = Vector4_prev;

Time1 = Time1_prev;
Time2 = Time2_prev;
Time3 = Time3_prev;
Time4 = Time4_prev;

vNum = vNum_prev;
i_M = i_M_prev;
i_Spos = i_Spos_prev;
i_Sneg = i_Sneg_prev;
i_Smax = i_Smax_prev;
iNP_BandNTV = iNP_BandNTV_prev;
x_S0 = x_S0_prev;
x_S1 = x_S1_prev;

UI_Flag = UI_Flag_prev;
UIsign = UIsign_prev;
t_sM = t_sM_prev;
DQcross_flag = DQcross_flag_prev;
bal_Flag = bal_Flag_prev;
balOK = balOK_prev;
Region = Region_prev;
V_Bandpk = V_Bandpk_prev;
Vbeg = Vbeg_prev;
V_C1_ref = V_C1_ref_prev;
ContInt = ContInt_prev;
sV_C1 = sV_C1_prev;
sM = sM_prev;

Tsw = 1/fs;
w = 2*pi*f;
ref = cos(w*t);

% if M < 0.95
%     mult = 1.07;
% else
%     mult = 1.01;
% end
mult = 1;

if t > tprev+Tsw
    %New switching period!
    tprev_new = t;
```

```
% theta is calculated based on tprev,
% therefore remains the same during a switching period
theta = mod(w*tprev, 2*pi);
sextantNum = floor(theta / (pi/3));
theta = mod(theta, pi/3); % Working with the first Sextant only!
theta_tr = acos(1/(2*M))-pi/6;

%Duty cycles
dS0mod = dS0(theta, M, 1);
dS1mod = dS1(theta, M, 1);
dMmod = dM(theta, M, 1);

%Vector selection
vNumS0 = mod(4*sextantNum, 24); %S0,1->+0, S0,2->+1
vNumS1 = mod(4*sextantNum + 4, 24); %S1,1->+4, S1,2->+5
vNumM = mod(4*sextantNum + 2, 24);

%Calculating i_S0, i_S1
IofS0 = 0;
IofS1 = 0;

if vNumS0 == 0 || vNumS0 == 12
    IofS0 = Iabc(1);
else if vNumS0 == 4 || vNumS0 == 16
        IofS0 = Iabc(3);
        else if vNumS0 == 8 || vNumS0 == 20
        IofS0 = Iabc(2);
            end
    end
end

if vNumS1 == 0 || vNumS1 == 12
    IofS1 = Iabc(1);
else if vNumS1 == 4 || vNumS1 == 16
        IofS1 = Iabc(3);
        else if vNumS1 == 8 || vNumS1 == 20
        IofS1 = Iabc(2);
            end
    end
end

i_S0 = dS0mod*IofS0;
i_S1 = dS1mod*IofS1;
i_Smax = abs(i_S0) + abs(i_S1);

% Deriving i_Spos|Str and i_Sneg|Str
i_Spos = i_Smax;
i_Sneg = -i_Smax;

%Calculating i_M
IofM = 0;

if vNumM == 2 || vNumM == 14
    IofM = Iabc(2);
else if vNumM == 6 || vNumM == 18
        IofM = Iabc(1);
        else if vNumM == 10 || vNumM == 22
            IofM = Iabc(3);
            end
    end
end

i_M = dMmod*IofM;



% CALCULATION OF V_C1_ref
%--------------------------------------------------------------------------------
sM = sign(i_M);

%Checking inverter operation Region (0, 1, or 2) and Balance whenever i_M changes sign
if sM_prev ~= sM && t > t_sM_prev + 5*Tsw
```

```
        %Check that balance was not lost
        balOK = 1;
        if bal_Flag == 0
            balOK = 0;
        end

        % Check if there has been an UI between the previous change of sM and this one
        Region = 1;
        if UI_Flag_prev == 0 % If not, we are in Region 0
            Region = 0;
        end

        %Reinitialize flags for next i_M half cycle (after some delay, because between quick
sign changes
        %there are no UIs and this confuses the code, sending it to Region 0)
        bal_Flag = 0;
        UI_Flag = 0;
        DQcross_flag = 0;
        t_sM = t;
    end

    sV_C1 = sign(V_C1 - Vnom);
    % Check if V_C1 crossed Vnom between the previous change of sM and this one
    if sV_C1_prev ~= sV_C1
        bal_Flag = 1;
    end

    % Check if there has been an UI between the previous change of sM and this one
    if i_M > -i_Sneg || i_M < -i_Spos %aDQS < ai_M %Inside an uncontrollable interval
        UI_Flag = 1; % UI appeared between two sign changes of i_M, so Region = 1 or 2.
        if i_M > 0
            UIsign = 1; % Sign of i_M during last UI
        else
            UIsign = -1;
        end
    end

    if balOK_prev == 0 || Region_prev == 0
        ContInt = 1;

        Vbeg = Vnom;
        V_Bandpk = 0;
        V_C1_ref = Vnom;
    else % Region 1, Balanced operation

        % Sample V_C1 at the beginning and at the end of an uncontrollable interval.
        %Sampling voltage at the beginning and the end of uncontrollable intervals (if any)
        if ~(i_M > -i_Sneg || i_M < -i_Spos) %Inside a controllable interval
            ContInt = 1;

            %At the beginning of a controllable interval:
            %If the previous UI has driven V_C1 to its sign, sample V_C1.
            %This is the final voltage, after the uncontrollable int.
            if ContInt_prev == 0 && sV_C1 == UIsign
                %Change Vref
                V_Bandpk = mult * 0.5 * abs(V_C1 - Vbeg_prev);

                %Set the reference (target) voltage according to the sign (or 0) of i_M
                %in the previous uncontrollable interval.
                V_C1_ref = Vnom + UIsign * V_Bandpk;
            end
        else
            ContInt = 0;

            %At the beggining of an uncontrollable interval sample V_C1. This is the initial
voltage, at the beggining of the uncontrollable int.
            if ContInt_prev == 1 && DQcross_flag_prev == 0
                Vbeg = V_C1;
                DQcross_flag = 1; % To sample the very beginning of the uncontrollable
interval
            end
        end
    end
```

```
%ADJUSTMENT OF DUTY CYCLES
%-------------------------------------------------------------------------------------

%Voltage deviation due to M, S0,1 and S1,1
DVofM = i_M*Tsw/(2*C);
DVofS0 = i_S0*Tsw/(2*C);
DVofS1 = i_S1*Tsw/(2*C);

vNumS0_1 = vNumS0;
vNumS0_2 = vNumS0 + 1;

vNumS1_1 = vNumS1;
vNumS1_2 = vNumS1 + 1;

x_S0 = 0;
x_S1 = 0;

if theta < theta_tr

    Triangle = 1;

    %Low outer triangle, use S0, M, L0
    vNumL0 = mod(4*sextantNum + 3, 24);
    dL0mod = 1-dS0mod-dMmod;

    %Distribution of duty cycle between S0,1 and S0,2
    %For the NTV, it is actually selection between S0,1 or S0,2
    if DVofS0 == 0
        % Arbitrarily select x_S0 = 1, it doesn't affect vNP
        Vector1 = vNumS0_1; Time1 = dS0mod*Tsw;
        Vector2 = vNumL0; Time2 = dL0mod*Tsw;
        Vector3 = vNumM; Time3 = dMmod*Tsw;
    else
        x_S0 = (V_C1_ref - V_C1 - DVofM)/DVofS0;

        if x_S0 >= 0
            x_S0 = 1;
            Vector1 = vNumS0_1; Time1 = dS0mod*Tsw;
            Vector2 = vNumL0; Time2 = dL0mod*Tsw;
            Vector3 = vNumM; Time3 = dMmod*Tsw;
        else
            x_S0 = -1;
            Vector1 = vNumL0; Time1 = dL0mod*Tsw;
            Vector2 = vNumM; Time2 = dMmod*Tsw;
            Vector3 = vNumS0_2; Time3 = dS0mod*Tsw;
        end
    end

else if theta < pi/3 - theta_tr
        %Triangle 2
        Triangle = 2;
        balancing_flag = 0;

        if V_C1_ref > V_C1 + DVofM + abs(DVofS0) + abs(DVofS1)
            %Select the small vectors that cause positive DVs
            if DVofS0 > 0
                x_S0 = 1;
            else
                x_S0 = -1;
            end

            if DVofS1 > 0
                x_S1 = 1;
            else
                x_S1 = -1;
            end
        else if V_C1_ref < V_C1 + DVofM - abs(DVofS0) - abs(DVofS1)
                %Select the small vectors that cause negative DVs
                if DVofS0 > 0
                    x_S0 = -1;
                else
                    x_S0 = 1;
```

```
                end

                if DVofS1 > 0
                    x_S1 = -1;
                else
                    x_S1 = 1;
                end
            else
                balancing_flag = 1;
                finalV_C1_a = V_C1 + DVofM + abs(DVofS0) - abs(DVofS1);
                finalV_C1_b = V_C1 + DVofM - abs(DVofS0) + abs(DVofS1);

                if abs(V_C1_ref - finalV_C1_a) < abs(V_C1_ref - finalV_C1_b)
                    %Select S0 that causes positive DV and S1 that
                    %causes negative DV (a).
                    if DVofS0 > 0
                        x_S0 = 1;
                    else
                        x_S0 = -1;
                    end

                    if DVofS1 > 0
                        x_S1 = -1;
                    else
                        x_S1 = 1;
                    end

                else
                    %Select S0 that causes negative DV and S1 that
                    %causes positive DV (b).
                    if DVofS0 > 0
                        x_S0 = -1;
                    else
                        x_S0 = 1;
                    end

                    if DVofS1 > 0
                        x_S1 = 1;
                    else
                        x_S1 = -1;
                    end
                end
            end
        end

        if notUsing8stepsForSmallBalancing == 1 && balancing_flag == 1 && x_S0 == 1 &&
x_S1 == 1
             x_S0 = -1;
             x_S1 = -1;
        end

        if x_S0 == 1 && x_S1 == 1 % This is the 8-step sequence
            Vector1 = vNumS0_1; Time1 = dS0mod*Tsw;
            Vector2 = vNumM; Time2 = dMmod*Tsw;
            Vector3 = vNumS1_1; Time3 = dS1mod*Tsw;
        else if x_S0 == 1 && x_S1 == -1
                Vector1 = vNumS0_1; Time1 = dS0mod*Tsw;
                Vector2 = vNumS1_2; Time2 = dS1mod*Tsw;
                Vector3 = vNumM; Time3 = dMmod*Tsw;
             else if x_S0 == -1 && x_S1 == 1
                    Vector1 = vNumM; Time1 = dMmod*Tsw;
                    Vector2 = vNumS0_2; Time2 = dS0mod*Tsw;
                    Vector3 = vNumS1_1; Time3 = dS1mod*Tsw;
                 else
                     Vector1 = vNumS1_2; Time1 = dS1mod*Tsw;
                     Vector2 = vNumM; Time2 = dMmod*Tsw;
                     Vector3 = vNumS0_2; Time3 = dS0mod*Tsw;
                 end
            end
        end
    else
        Triangle = 3;

        vNumL1 = mod(4*sextantNum + 7, 24);
```

```
            dL1mod = 1-dS1mod-dMmod;

            %Distribution of duty cycle between S0,1 and S0,2
            if DVofS1 == 0
                % Arbitrarily select x_S1 = 1, it doesn't affect vNP
                Vector1 = vNumM; Time1 = dMmod*Tsw;
                Vector2 = vNumL1; Time2 = dL1mod*Tsw;
                Vector3 = vNumS1_1; Time3 = dS1mod*Tsw;
            else
                x_S1 = (V_C1_ref - V_C1 - DVofM)/DVofS1;

                if x_S1 >= 0
                    x_S1 = 1;
%                     Vector1 = vNumM; Time1 = dMmod*Tsw;
%                     Vector2 = vNumL1; Time2 = dL1mod*Tsw;
%                     Vector3 = vNumS1_1; Time3 = dS1mod*Tsw;
                    Vector1 = vNumS1_1; Time1 = dS1mod*Tsw;
                    Vector2 = vNumL1; Time2 = dL1mod*Tsw;
                    Vector3 = vNumM; Time3 = dMmod*Tsw;
                else
                    x_S1 = -1;
%                     Vector1 = vNumS1_2; Time1 = dS1mod*Tsw;
%                     Vector2 = vNumM; Time2 = dMmod*Tsw;
%                     Vector3 = vNumL1; Time3 = dL1mod*Tsw;
                    Vector1 = vNumL1; Time1 = dL1mod*Tsw;
                    Vector2 = vNumM; Time2 = dMmod*Tsw;
                    Vector3 = vNumS1_2; Time3 = dS1mod*Tsw;
                end
            end
        end
    end

    iNP_BandNTV = i_M + x_S0*i_S0 + x_S1*i_S1;
else
    %Same switching period
    tprev_new = tprev;
end


%SWITCHING THE CONVERTER
%--------------------------------------------------------------------------

if t < tprev_new + (Time1)/2
    vNum = Vector1;
else if t < tprev_new + (Time1 + Time2)/2
        vNum = Vector2;
    else if t < tprev_new + (Time1 + Time2 + 2*Time3)/2
            vNum = Vector3;
        else if t < tprev_new + (Time1 + 2*Time2 + 2*Time3)/2
                vNum = Vector2;
            else
                vNum = Vector1;
            end
        end
    end
end
```

# Appendix B

## Converter IGBT-diode losses

An analytical study of semiconductor (switching and conduction) losses for the 2L, 3L NPC, and 3L CHB inverter topologies is presented in this Appendix. Existing literature on switching and conduction losses is reviewed, and its methodologies are used to derive analytical loss expressions for each topology. Expressions are written in terms of the inverter operating parameters and module loss characteristics, assuming the SPWM modulation strategy. Screenshots from a CLC, built according to the derived expressions, are included at the end of the Appendix.

### B.1 Switching losses

Switching losses appear during the turn-on and turn-off processes of the semiconductors that create the inverter's PWM waveform. The process of estimating the switching losses for an inverter switching module (IGBTs will be assumed in this study) or diode, starts with analysing the switching energy loss for a single switching. Subsequently, the number of switchings and their position during the fundamental voltage and current cycle is determined. The sum (integration) of all switching energy losses over a fundamental period, divided by its duration, $T$, gives the switching power losses for the examined IGBT or diode.

Regarding the estimation of elementary (i.e., for a single switching) switching energy losses, two main approaches can be found in the literature. The first is based on the semiconductor current-voltage ($I$-$V$) switching transients, whereas the other uses its on/off loss-current ($E_{on/off}$ –$I$) curves. In [73, 74] the authors present an electrothermal model that approximates the switching losses in IGBTs and diodes based on the devices turn-on and turn-off $I$-$V$ characteristics. Turn-on and turn-off processes and losses are treated separately, as they are governed by different phenomena. This increases the model's complexity and

brings several curve-fitting constants in the derived expressions. On the other hand, the approach using the switching energy ($E_{on/off}$-$I$) curves is simpler, mainly because of the fact that the losses during a complete switching (turn-on and turn-off) are approximately proportional to the switching voltage and current. This argument is supported and used by many researchers [75, 76], while graphs included in IGBT-diode module data sheets indicate this approximately linear relationship [77]. Accepting this approach has the benefit of avoiding long expressions and numerous constants, while enhancing the accuracy of the results due to the use of experimental data from the relevant data sheets.

Starting with 2L inverters, switching losses have been investigated using different assumptions as a basis, giving respective approximate results [78, 79]. What is important for the case of 2L inverter is the fact that switching losses are the same and independent of the load *PF* for all continuous PWM methods. This happens because all three-phase currents are commutated during each carrier cycle [12]. Regarding the NPC inverter, expressions for switching losses have been derived in [80], using a second order approximation of the switching energy with respect to current. Finally, no study of switching losses has been found regarding the CHB inverter.

The analytical derivation of inverter switching losses in the present study was based on the assumption that the total (turn-on and turn-off) losses during one semiconductor switching are proportional to the switching voltage and current [75, 76]. The approach that uses the switching energy curves was adopted, due to the advantages explained earlier.

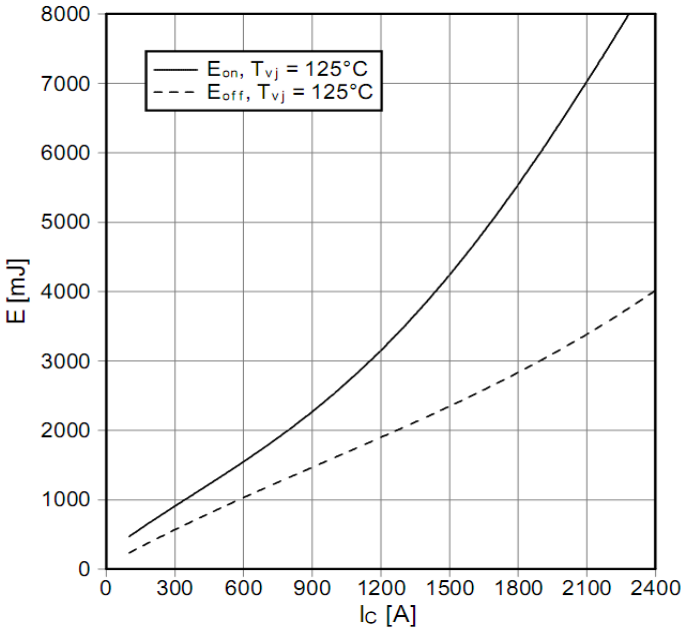


**Figure B.1.** IGBT turn-on and turn-off energy losses **[77]**.

Figure B.1 [77] illustrates the turn-on and turn-off energy losses of an IGBT with respect to its switching current. Similar graphs are also available for power diodes. The sum of the two curves for each value of the switching current represents the total switching energy loss during one complete switching. The curves are approximately linear and hence this sum can be approximated by a first order equation with respect to the instantaneous switching current, $I_{sw}$. Switching losses are also proportional to the switching voltage, $V_{sw}$, and therefore the switching energy loss characteristics (i.e. the energy losses during one on-off switching), $E_{1sw,c}$ for IGBTs and $E_{1sw,d}$ for diodes, can be mathematically described by equations of the following form:

$$\left.\begin{aligned} E_{1sw,c} &= \frac{V_{sw}}{V_{base}}\left(a_c \cdot I_{sw} + b_c\right) \\ E_{1sw,d} &= \frac{V_{sw}}{V_{base}}\left(a_d \cdot I_{sw} + b_d\right) \end{aligned}\right\} \text{ or } E_{1sw,c/d} = \frac{V_{sw}}{V_{base}}\left(a_{c/d} \cdot I_{sw} + b_{c/d}\right). \qquad \textbf{(B.1)}$$

The latter equation is written in a compact form, to cover both, IGBTs (subscript '*c*') and diodes (subscript '*d*'). The curve-fitting constants $\alpha_c$ and $b_c$ will be used for the IGBTs, while $\alpha_d$ and $b_d$ will be used for the diodes. Symbols $\alpha$ and $b$ will represent the sums $\alpha_c + \alpha_d$ and $b_c$

+ $b_d$, respectively. $V_{base}$ represents the reference switching voltage, used for the derivation of the plot in the data sheet.

In addition to the switching energy characteristics, the calculation of average switching losses for a given inverter semiconductor, requires the following parameters:

- Switching frequency, $f_s$.
- Switching voltage (i.e., the voltage across which the semiconductor has to switch), $V_{sw}$.
- The switching current (i.e., the current that flows/will flow through the semiconductor, before/after it switches off/on, respectively). For reasons of simplicity of derived expressions, angle $\theta$ in this section will represent the current angle instead of the voltage reference angle. Thus, the switching current will be $I_{pk}\sin\theta$.
- The angle interval(s) during which the semiconductor switches, expressed as portion(s) of the fundamental cycle, [$\theta_1$, $\theta_2$].

The first step for the derivation of a switching loss expression is the calculation of the average energy loss, $E_{sw}$, over a fundamental period. One complete switching happens during each switching period. Under the assumption that the switching frequency is several times higher than the fundamental frequency, the switchings can be considered to be evenly distributed over a fundamental period. Thus, for a given inverter IGBT/diode, $E_{sw}$ is given by the following integral:

$$E_{sw,c/d} = \frac{V_{sw}}{V_{base}} \frac{1}{2\pi} \int_{\theta_1}^{\theta_2} \left( a_{c/d} I_{pk} \sin\theta + b_{c/d} \right) d\theta \,. \qquad \textbf{(B.2)}$$

The switching power losses can then be found by multiplying by the inverter switching frequency:

$$P_{sw,c/d} = E_{sw,c/d} \, f_s \,. \qquad \textbf{(B.3)}$$

### B.1.1 Switching losses in the two-level inverter

The methodology introduced in the previous paragraph will be initially applied to the 2L inverter. In a 2L inverter, power semiconductors switch under:

- The full dc bus voltage: $V_{dc}$
- Instantaneous current: $I_{pk}\sin\theta$
- The switching intervals: [0, π] and [π, 2π]

The expressions for the IGBT/diode average switching energy and switching power losses in this topology are given below:

$$E_{sw,c/d-2L} = \frac{V_{dc}}{V_{base}} \frac{1}{2\pi} \int_0^{\pi} (a_{c/d} I_{pk} \sin\theta + b_{c/d})\, d\theta$$
$$P_{sw,c/d-2L} = \frac{V_{dc}}{V_{base}} \left( \frac{a_{c/d}}{\pi} I_{pk} + \frac{b_{c/d}}{2} \right) f_s \quad . \tag{B.4}$$

According to (B.4), the power loss expression is derived from the energy loss expression in a simple manner, and hence, throughout the report, the two expressions will be presented as a pair with a single equation number. The expression is the same for IGBTs and diodes. Since the three-phase 2L inverter consists of six IGBTs-diodes, its total switching losses will be given by

$$P_{sw-2L,3\phi} = 6 \frac{V_{dc}}{V_{base}} \left( \frac{a}{\pi} I_{pk} + \frac{b}{2} \right) f_s \ , \tag{B.5}$$

where

$$a = a_c + a_d$$
$$b = b_c + b_d \quad . \tag{B.6}$$

### B.1.2 Switching losses in the NPC inverter

In an NPC 3L inverter, IGBTs and diodes switch under:

- Half the dc bus voltage: $V_{dc}/2$
- Instantaneous current: $I_{pk}\sin\theta$
- Switching intervals:
  - ($S_1$) ↔ ($D_5$) switch during [0, π−$\phi$]
  - ($S_2$, $D_5$) ↔ ($D_3$, $D_4$) switch during [π−$\phi$, π]
  - ($S_4$) ↔ ($D_6$) switch during [π, 2π−$\phi$]
  - ($S_3$, $D_6$) ↔ ($D_1$, $D_2$) switch during [2π−$\phi$, 2π]

The average switching energy and the respective power loss expressions for each semiconductor of this topology will be ('/' is used as in (B.1) to provide a compact equation form for semiconductors that share the same loss expression):

$$E_{sw-NPC,S1/D5} = E_{sw-NPC,S4/D6} = \frac{V_{dc}}{V_{base}} \frac{1}{4\pi} \int_0^{\pi-\phi} (a_{c/d} I_{pk} \sin\theta + b_{c/d}) d\theta$$
$$P_{sw-NPC,S1/D5} = P_{sw-NPC,S4/D6} = \frac{V_{dc}}{V_{base}} \frac{1}{4\pi} \left[ a_{c/d} I_{pk} (\cos\phi + 1) + b_{c/d} (\pi - \phi) \right] f_s \quad \textbf{(B.7)}$$

$$E_{sw-NPC,S2/S3} = \frac{V_{dc}}{V_{base}} \frac{1}{4\pi} \int_{\pi-\phi}^{\pi} (a_c I_{pk} \sin\theta + b_c) d\theta$$
$$P_{sw-NPC,S2/S3} = \frac{V_{dc}}{V_{base}} \frac{1}{4\pi} \left[ a_c I_{pk} (1 - \cos\phi) + b_c \phi \right] f_s \quad \textbf{(B.8)}$$

$$E_{sw-NPC,D1/\ldots/D4} = \frac{V_{dc}}{V_{base}} \frac{1}{8\pi} \int_{\pi-\phi}^{\pi} (a_d I_{pk} \sin\theta + b_d) d\theta$$
$$P_{sw-NPC,D1/\ldots/D4} = \frac{V_{dc}}{V_{base}} \frac{1}{8\pi} \left[ a_d I_{pk} (1 - \cos\phi) + b_d \phi \right] f_s \quad \textbf{(B.9)}$$

According to the above expressions, the total switching losses for the three-phase 3L NPC inverter are

$$P_{sw-NPC,3\phi} = 3 \frac{V_{dc}}{V_{base}} \left( \frac{a}{\pi} I_{pk} + \frac{b}{2} \right) f_s \ . \quad \textbf{(B.10)}$$

### B.1.3 Switching losses in the CHB inverter

In a CHB 3L inverter, the semiconductors switch under conditions which are similar to the ones for the NPC inverter:

- Half the dc bus voltage: $V_{dc}/2$
- Instantaneous current: $I_{pk} \sin\theta$
- Switching intervals:
  - ($S_1$) ↔ ($D_2$) switch during [0, π−$\phi$]
  - ($S_4$) ↔ ($D_3$) switch during [π−$\phi$, π]
  - ($S_3$) ↔ ($D_4$) switch during [π, 2π−$\phi$]
  - ($S_2$) ↔ ($D_1$) switch during [2π−$\phi$, 2π]

The switching loss expressions for the IGBTs $S_1$ … $S_4$ and diodes $D_1$ … $D_4$ for each H-Bridge of the CHB topology, will be the following:

$$\begin{aligned} E_{sw-CHB,S1/D2} &= E_{sw-CHB,S3/D4} = \frac{V_{dc}}{V_{base}} \frac{1}{4\pi} \int_0^{\pi-\phi} (a_{c/d} I_{pk} \sin\theta + b_{c/d}) d\theta \\ P_{sw-CHB,S1/D2} &= P_{sw-CHB,S3/D4} = \frac{V_{dc}}{V_{base}} \frac{1}{4\pi} \left[ a_{c/d} I_{pk} (\cos\phi + 1) + b_{c/d} (\pi - \phi) \right] f_s \end{aligned} \quad \textbf{(B.11)}$$

$$\begin{aligned} E_{sw-CHB,S4/D3} &= E_{sw-CHB,S4/D3} = \frac{V_{dc}}{V_{base}} \frac{1}{4\pi} \int_{\pi-\phi}^{\pi} (a_{c/d} I_{pk} \sin\theta + b_{c/d}) d\theta \\ P_{sw-CHB,S4/D3} &= P_{sw-CHB,S4/D3} = \frac{V_{dc}}{V_{base}} \frac{1}{4\pi} \left[ a_{c/d} I_{pk} (1 - \cos\phi) + b_{c/d} \phi \right] f_s \end{aligned} \quad \textbf{(B.12)}$$

The total switching losses for the three-phase CHB comes from the following expression, which is identical to the respective one for the NPC inverter:

$$P_{sw-CHB,3\phi} = 3 \frac{V_{dc}}{V_{base}} \left( \frac{a}{\pi} I_{pk} + \frac{b}{2} \right) f_s = P_{sw-NPC,3\phi} \ . \quad \textbf{(B.13)}$$

## B.2 Conduction losses

Conduction losses occur during the semiconductor conduction intervals, due to their non-zero on-state voltage drops. Two main approaches have been used in the literature for the estimation of conduction losses, both giving the same results. The first [78] assumes a high switching frequency and divides the fundamental period into infinitesimal time intervals, equal to the switching period. Then, it multiplies the expressions for the power loss and the duty cycle of each power semiconductor for a given time instant with the elementary switching period (d$t$). Finally, it integrates this product over a fundamental period and obtains the average conduction losses. The second approach [79] performs a pulse-by-pulse analysis that examines the exact positions and durations of each semiconductor's conduction intervals. It does not assume an infinite switching frequency, hence approaching what happens in an inverter more closely, but yields complicated intermediate results. The final results of the two methods are identical, which verifies the applicability of the first approach even in lower switching frequencies.

Unlike switching losses, inverter conduction losses are affected by the selection of the PWM strategy and the load power factor. Expressions for the 2L inverter conduction losses can be found in [78, 79, 81]. Regarding the NPC inverter, expressions for IGBT and diode conduction losses are derived in [80, 81, 82], and have been verified in the context of the present work. Expressions for the NPC inverter can also be found in [75] and [83] for a number of modulation strategies. No literature has been found on the conduction losses of the CHB and the interleaved inverter topologies.

IGBT and diode conduction (instead of switching) *I-V* characteristics are used for deriving expressions for conduction losses. In order to approximate these characteristics, it is common to use two curve-fitting constants, $V_{0,c/d}$ and $R_{c/d}$ that represent the semiconductor's saturation voltage and on-state resistance, respectively. Their values are acquired from *I-V* graphs included in IGBT-diode module data sheets.

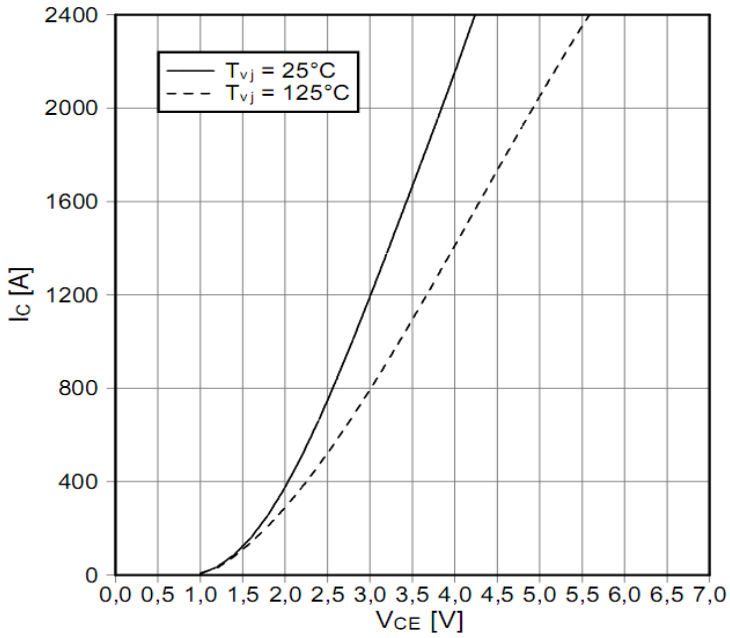


**Figure B.2.** IGBT *I-V* characteristic **[77]**.

Figure B.2 [77] presents the conduction *I-V* characteristic for an IGBT. $V_{0,c}$ is equal to the voltage at the point where the extension of the linear part of the graph intersects the horizontal axis, while $R_c$ is equal to the inverse of its gradient. $V_{0,c/d}$ and $R_{c/d}$ approximate the conduction *I-V* characteristics of IGBTs-diodes, according to

$$V = V_{0,c/d} + I\,R_{c/d} \quad . \tag{B.14}$$

The derivation of the conduction losses for an inverter semiconductor, associates its conduction characteristics with the following parameters:

- The instantaneous load current amplitude, $I_{pk}\sin\theta$ and power factor, $PF = \cos\phi$
- The conduction interval(s) during a fundamental period, $[\theta_1, \theta_2]$
- The conduction duty cycle as a function of the voltage angle, $\delta(\theta+\phi)$

The term 'conduction interval' in the present context is used macroscopically to denote the portions (in terms of current angle $\theta$) of the fundamental period, during which the examined IGBT or diode carries current while it is turned on. The device does not conduct during the whole conduction interval but during a fraction of it, which equals to the instantaneous duty cycle. Under the assumption of a high inverter switching frequency, the sum of all elementary conduction losses over a fundamental period can be approximated by a respective integral. Division by the duration of a fundamental cycle ($2\pi$) gives the expression for conduction power losses of a specific IGBT/diode of the inverter:

$$P_{con} = \frac{1}{2\pi}\int_{\theta_1}^{\theta_2} \delta(\theta+\phi) I_{c/d} V_{c/d} d\theta$$

or

$$P_{con} = \frac{1}{2\pi}\int_{\theta_1}^{\theta_2} \delta(\theta+\phi) I_{pk}\sin\theta (R_{c/d} I_{pk}\sin\theta + V_{0,c/d}) d\theta \qquad \textbf{(B.15)}$$

### B.2.1 Conduction losses in the two-level inverter

In a 2L inverter, power semiconductors conduct:

- The instantaneous load current : $I_{pk}\sin\theta$
- Conduction intervals:
  - IGBT $S_1$ and diode $D_2$ conduct during $[0, \pi]$
  - IGBT $S_2$ and diode $D_1$ conduct during $[\pi, 2\pi]$
- Duty cycles:
  - IGBTs: $\delta = \frac{1}{2}[1 + M\sin(\theta+\phi)]$
  - Diodes: $\delta = \frac{1}{2}[1 - M\sin(\theta+\phi)]$

According to the previous paragraph, the IGBT, diode and total conduction losses for the three-phase 2L inverter will be given by the following expressions:

$$P_{con-2L,S1/S2} = \frac{1}{2\pi}\int_0^{\pi}\frac{1}{2}[1+M\sin(\theta+\phi)]I_{pk}\sin\theta(R_c I_{pk}\sin\theta + V_{0,c})d\theta$$
$$P_{con-2L,S1/S2} = \left(\frac{1}{8}+\frac{M}{3\pi}\cos\phi\right)R_c I_{pk}^2 + \left(\frac{1}{2\pi}+\frac{M}{8}\cos\phi\right)V_{0,c} I_{pk} \quad \textbf{(B.16)}$$

$$P_{con-2L,D1/D2} = \frac{1}{2\pi}\int_0^{\pi}\frac{1}{2}[1-M\sin(\theta+\phi)]I_{pk}\sin\theta(R_d I_{pk}\sin\theta + V_{0,d})d\theta$$
$$P_{con-2L,D1/D2} = \left(\frac{1}{8}-\frac{M}{3\pi}\cos\phi\right)R_d I_{pk}^2 + \left(\frac{1}{2\pi}-\frac{M}{8}\cos\phi\right)V_{0,d} I_{pk} \quad \textbf{(B.17)}$$

$$P_{con-2L,3\phi} = \left[\frac{3}{4}(R_c+R_d)+\frac{2M}{\pi}(R_c-R_d)\cos\phi\right]I_{pk}^2 + \left[\frac{3}{\pi}(V_{0,c}+V_{0,d})+\frac{3M}{4}(V_{0,c}-V_{0,d})\cos\phi\right]I_{pk} \quad \textbf{(B.18)}$$

### B.2.2 Conduction losses in the NPC inverter

As for the 2L inverter, the power semiconductors that conduct in this topology conduct the instantaneous load current. The conduction intervals for each semiconductor of the NPC inverter are summarized in Table B.1. The voltage waveform produced by 3L inverters switches between $\pm V_{dc}/2$ and 0, not between $+V_{dc}/2$ and $-V_{dc}/2$ as in 2L inverters. This affects the calculation of the semiconductor duty cycles, which are different than the 2L inverter's and are shown in Table B.2 [49]. Note that in this topology certain devices conduct during two non adjacent intervals during a fundamental cycle.

| Device conducting | from | to | with duty cycle | | from | to | with duty cycle |
|---|---|---|---|---|---|---|---|
| $S_1$ | 0 | $\pi-\phi$ | $\delta_1$ | | | | |
| $S_2$ | 0 | $\pi-\phi$ | 1 | | $\pi-\phi$ | $\pi$ | $\delta_3$ |
| $D_3$ , $D_4$ | $\pi-\phi$ | $\pi$ | $\delta_4$ | | | | |
| $D_5$ | 0 | $\pi-\phi$ | $\delta_2$ | AND | $\pi-\phi$ | $\pi$ | $\delta_3$ |
| $S_4$ | $\pi$ | $2\pi-\phi$ | $\delta_4$ | | | | |
| $S_3$ | $\pi$ | $2\pi-\phi$ | 1 | | $2\pi-\phi$ | $2\pi$ | $\delta_2$ |
| $D_1$ , $D_2$ | $2\pi-\phi$ | $2\pi$ | $\delta_1$ | | | | |
| $D_6$ | $\pi$ | $2\pi-\phi$ | $\delta_3$ | | $2\pi-\phi$ | $2\pi$ | $\delta_2$ |

**Table B.1.** Conduction intervals for the NPC inverter.

| Sign of $v_{x,ref}$ | Leg $x$ in state | with duty cycle | Symbol |
|---|---|---|---|
| $v_{x,ref} \geq 0$ | (P) | $M\sin(\theta+\phi)$ | $\delta_1$ |
| | (Z) | $1-M\sin(\theta+\phi)$ | $\delta_2$ |
| $v_{x,ref} < 0$ | (Z) | $1+M\sin(\theta+\phi)$ | $\delta_3$ |
| | (N) | $-M\sin(\theta+\phi)$ | $\delta_4$ |

**Table B.2.** Conduction duty cycles for three-level inverters.

The resulting conduction power loss expressions for the inverter IGBTs are the following:

$$P_{con-NPC,S1/S4} = \frac{1}{2\pi}\int_0^{\pi-\phi} M\sin(\theta+\phi) I_{pk}\sin\theta(R_c I_{pk}\sin\theta + V_{0,c})d\theta$$
$$P_{con-NPC,S1/S4} = \frac{MR_c I_{pk}^2}{6\pi}(1+\cos\phi)^2 + \frac{MV_{0,c}I_{pk}}{4\pi}[(\pi-\phi)\cos\phi+\sin\phi] \quad \textbf{(B.19)}$$

$$P_{con-NPC,S2/S3} = \frac{1}{2\pi}[\int_0^{\pi-\phi} I_L \sin\theta(R_c I_{pk}\sin\theta + V_{0,c})d\theta + \int_{\pi-\phi}^{\pi}[1+M\sin(\theta+\phi)]I_{pk}\sin\theta(R_c I_{pk}\sin\theta + V_{0,c})d\theta]$$

$$P_{con-NPC,S2/S3} = \frac{R_c I_{pk}^2}{4} - \frac{R_c I_{pk}^2 M}{6\pi}(1-\cos\phi)^2 + \frac{V_{0,c} I_{pk}}{\pi} + \frac{MV_{0,c} I_{pk}}{4\pi}(\phi\cos\phi - \sin\phi) \quad \textbf{(B.20)}$$

The respective conduction power loss expressions for the inverter diodes are:

$$P_{con-NPC,D1/.../D4} = \frac{1}{2\pi}\int_{\pi-\phi}^{\pi}[-M\sin(\theta+\phi)]I_{pk}\sin\theta(R_d I_{pk}\sin\theta + V_{0,d})d\theta$$

$$P_{con-NPC,D1/.../D4} = \frac{MR_d I_{pk}^2}{6\pi}(1-\cos\phi)^2 + \frac{MV_{0,d} I_{pk}}{4\pi}(\sin\phi - \phi\cos\phi) \quad \textbf{(B.21)}$$

$$P_{con-NPC,D5/D6} = \frac{1}{2\pi}[\int_0^{\pi-\phi}[1-M\sin(\theta+\phi)]I_{pk}\sin\theta(R_d I_{pk}\sin\theta + V_{0,d})d\theta + \int_{\pi-\phi}^{\pi}[1+M\sin(\theta+\phi)]..d\theta]$$

$$P_{con-NPC,D5/D6} = \frac{R_d I_{pk}^2}{4} - \frac{MR_d I_{pk}^2}{3\pi}(1+\cos^2\phi) + \frac{V_{0,d} I_{pk}}{\pi} + \frac{MV_{0,d} I_{pk}}{4\pi}[(2\phi-\pi)\cos\phi - 2\sin\phi] \quad \textbf{(B.22)}$$

Using the above expressions, the total conduction losses for the three-phase NPC inverter can be proved to be the following:

$$P_{con-NPC,3\phi} = \left[\frac{3}{2}(R_c + R_d) + \frac{4M}{\pi}(R_c - R_d)\cos\phi\right]I_{pk}^2 + \left[\frac{6}{\pi}(V_{0,c} + V_{0,d}) + \frac{3M}{2}(V_{0,c} - V_{0,d})\cos\phi\right]I_{pk} \quad \textbf{(B.23)}$$

### B.2.3 Conduction losses in the CHB inverter

Instantaneous current values and duty cycle definitions are identical for the 3L NPC and CHB inverters. However, the conduction intervals, illustrated in Table B.3, are different for the CHB topology.

| Device conducting | from | to | with duty cycle | | from | to | with duty cycle |
|---|---|---|---|---|---|---|---|
| $S_1$ | 0 | $\pi-\phi$ | $\delta_1$ | | | | |
| $S_2$ | $\pi$ | $2\pi-\phi$ | 1 | | $2\pi-\phi$ | $2\pi$ | $\delta_2$ |
| $D_1$ | $2\pi-\phi$ | $2\pi$ | $\delta_1$ | | | | |
| $D_2$ | 0 | $\pi-\phi$ | $\delta_2$ | AND | $\pi-\phi$ | $\pi$ | 1 |
| $S_3$ | $\pi$ | $2\pi-\phi$ | $\delta_4$ | | | | |
| $S_4$ | 0 | $\pi-\phi$ | 1 | | $\pi-\phi$ | $\pi$ | $\delta_3$ |
| $D_3$ | $\pi-\phi$ | $\pi$ | $\delta_4$ | | | | |
| $D_4$ | $\pi$ | $2\pi-\phi$ | $\delta_3$ | | $2\pi-\phi$ | $2\pi$ | 1 |

**Table B.3.** Conduction intervals for the CHB inverter.

The resulting conduction power loss expressions for the CHB inverter's IGBTs and diodes are given below:

$$P_{con-CHB,S1/S3} = \frac{1}{2\pi}\int_0^{\pi-\phi}[M\sin(\theta+\phi)]I_{pk}\sin\theta(R_cI_{pk}\sin\theta+V_{0,c})d\theta$$
$$P_{con-CHB,S1/S3} = \frac{MR_cI_{pk}^2}{6\pi}(1+\cos\phi)^2+\frac{MV_{0,c}I_{pk}}{4\pi}[(\pi-\phi)\cos\phi+\sin\phi] \quad \textbf{(B.24)}$$

$$P_{con-CHB,S2/S4} = \frac{1}{2\pi}[\int_0^{\pi-\phi} I_{pk}\sin\theta(R_cI_{pk}\sin\theta+V_{0,c})d\theta+$$
$$\int_{\pi-\phi}^{\pi}[1+M\sin(\theta+\phi)]I_{pk}\sin\theta(R_cI_{pk}\sin\theta+V_{0,c})d\theta]$$
$$P_{con-CHB,S2/S4} = \frac{R_cI_{pk}^2}{4}-\frac{MR_cI_{pk}^2}{6\pi}(1-\cos\phi)^2+ \quad \textbf{(B.25)}$$
$$\frac{V_{0,c}I_{pk}}{\pi}+\frac{MV_{0,c}I_{pk}}{4\pi}(\phi\cos\phi-\sin\phi)$$

$$P_{con-CHB,D1/D3} = \frac{1}{2\pi}\int_{\pi-\phi}^{\pi}[-M\sin(\theta+\phi)]I_{pk}\sin\theta(R_dI_{pk}\sin\theta+V_{0,d})d\theta$$
$$P_{con-CHB,D1/D3} = \frac{MR_dI_{pk}^2}{6\pi}(1-\cos\phi)^2+\frac{MV_{0,d}I_{pk}}{4\pi}(\sin\phi-\phi\cos\phi) \quad \textbf{(B.26)}$$

$$P_{con-CHB,D2/D4} = \frac{1}{2\pi}\int_0^{\pi-\phi}[1-M\sin(\theta+\phi)]I_{pk}\sin\theta(R_c I_{pk}\sin\theta+V_{0,c})d\theta + \frac{1}{2\pi}\int_{\pi-\phi}^{\pi} I_{pk}\sin\theta(R_c I_{pk}\sin\theta+V_{0,c})d\theta$$

$$P_{con-CHB,D2/D4} = \left[-\frac{M}{6\pi}(1+\cos\phi)^2+\frac{1}{4}\right]R_d I_{pk}^2 + \left[\frac{M}{4\pi}[(\phi-\pi)\cos\phi-\sin\phi]+\frac{1}{\pi}\right]I_{pk}V_{0,d} \quad \textbf{(B.27)}$$

As for the switching losses, the expression for the total conduction losses of the three-phase CHB inverter can be shown to be the identical to the respective expression for the NPC inverter (B.23):

$$P_{con-CHB,3\phi} = P_{con-NPC,3\phi} \ . \quad \textbf{(B.28)}$$

## B.3 Converter loss calculator

The loss expressions derived in this Appendix for the 2L and the 3L NPC and CHB inverters were incorporated in an Excel spreadsheet, used as a CLC. The CLC was also extended to cover other converter types, namely the 6-pulse rectifier, the buck and boost dc-dc converters, and the 2L inverter for Brushless DC (BLDC) motor drives.

The user can select a converter type and provide input (Figure B.3), according to which the CLC estimates IGBT-diode losses and temperatures. Input includes values of parameters such as the converter switching frequency, modulation index, output current, etc., as well as the selection of IGBT-diode modules. Module data sheets are used to derive the values of loss coefficients (Figure B.4) and calculate the loss expressions and junction temperatures (Figures B.5 and B.6). Values for the ambient temperature and heat sink thermal coefficient, also provided by the user, are part of the above calculation. The calculation is recurrent, since junction temperatures affect the loss coefficients and vice-versa.

The CLC is a useful tool for converter design, since it contributes to the selection of modules, heat sinks, and operating parameters. Its copyright belongs to TSL Technology Ltd.

| | | | | | |
|---|---|---|---|---|---|
| 1 | **Loss Calculations for Three-Phase NPC Inverter** | | | | |
| 2 | Losses are for one device in the inverter. | | | | |
| 3 | | | | | |
| 4 | **Input** | | | | |
| 5 | Link voltage | Vbus | 1800 | V | |
| 6 | Fundamental freq. | f0 | 50 | Hz | |
| 7 | Switching freq. | fsw | 10000 | Hz | |
| 8 | Modulation | m | 0.99 | | |
| 9 | Power factor | cosphi | 0.85 | | |
| 10 | Max phase current | Ipk,max | 283 | A | |
| 11 | Outer devices (V1 - V4) | | FF300R17ME3 | | |
| 12 | | | | | |
| 13 | Inner devices (V2 - V3) | | FF300R17ME3 | | |
| 14 | | | | | |
| 15 | | | | | |
| 16 | Clamping diodes (D5 - D6) | | ○ Outer device | | |
| 17 | are part of / same type as: | | ◉ Inner device | | |
| 18 | | | | | |
| 19 | | | | | |
| 20 | Junction temperature | Tj | 125 | C | |
| 21 | Ambient temperature | Ta | 40 | C | |
| 22 | Heat sink thermal res. | Rthha | 0.132 | K/W | |
| 23 | | | | | |
| 24 | | | | | |
| 25 | **Derived quantities** | | SPWM | SVM | |
| 26 | Sine fundamental output | | 1091 | 1260 | Vrms |
| 27 | Max pure sine output | | 1102 | 1273 | Vrms |
| 28 | Effective link | | 900 | V | |
| 29 | Power angle | phi | 0.55 | rad | |

Rectifier | Buck | Boost | BLDC | 2L Inv. | CHB Inv. | **3L NPC Inv.**

**Figure B.3.** Converter selection and input parameters for the NPC inverter sheet of the CLC.

| **Data for selected device (V1 - V4)** | |
|---|---|
| No. | 327 |
| IGBT module | FF300R17ME3 |
| housing type | EconoDUAL3 |
| Rgon/Rgoff [W] | 4.7 |
| VDC [V] | 900 |
| Inom [A] | 300 |
| Rthjc [K/W] | 0.075 |
| Vce @ Inom [V] | 2.4 |
| Etot/Inom (25°C) [mWs/A] | 0.43 |
| Etot/Inom (125°C) [mWs/A] | 0.63 |
| V_t02 (25°C) [V] | 1.05 |
| R_ce2 (25°C) [Ohm] | 0.00317 |
| V_t01 (125°C) [V] | 0.90 |
| R_ce1 (125°C) [Ohm] | 0.00499 |
| Rthjcd [K/W] | 0.13 |
| Erec2 (25°C) [mWs] | 40.3 |
| Erec1 (125°C) [mWs] | 71.7 |
| U_02 (25°C) [V] | 1.16 |
| R_D2 (25°C) [Ohm] | 0.00213 |
| U_01 (125°C) [V] | 1.07 |
| R_D1 (125°C) [Ohm] | 0.00275 |
| R_CC´+EE´ [mOhm] | 1.1 |
| Rthch-IGBT [K/W] | 0.00 |
| Rthch-Diode [K/W] | 0.00 |
| SiC diode | 0 |

| **Derived quantities (V1 - V4)** | | | |
|---|---|---|---|
| IGBT switching | Eonoff | 188.9 | mJ |
| IGBT switching sc. | Ac | 0.63 | mJ/A |
| IGBT switching off. | Bc | 0.00 | mJ |
| IGBT threshold | Vt0 | 0.90 | V |
| IGBT resistance | Rce | 0.00499 | ohm |
| Diode recovery | Erec | 71.7 | mJ |
| Diode switching sc. | Ad | 0.11 | mJ/A |
| Diode switching off. | Bd | 39.4 | mJ |
| Diode threshold | U0 | 1.07 | V |
| Diode resistance | Rd | 0.00275 | ohm |
| Bond resistance | Rccee | 0.00152 | ohm |
| Nominal current | Inom | 300 | A |

**Figure B.4.** Datasheet values and derived loss coefficients for the selected IGBT-diode module.

| | | | | | | |
|---|---|---|---|---|---|---|
| 47 | Peak output current | Ipk [Apk] | 0 | 24 | 47 | 71 |
| 48 | Rms output current | Irms [Arms] | 0 | 17 | 33 | 50 |
| 49 | Power | Po [kW] | 0 | 27 | 54 | 80 |
| 50 | | | | | | |
| 51 | IGBT S1 conduction losses | IGBT S1 cond | 0 | 5 | 11 | 18 |
| 52 | IGBT S1 switching losses | IGBT S1 sw | 0 | 22 | 44 | 66 |
| 53 | IGBT S1 total losses | IGBT S1 tot | 0 | 27 | 55 | 84 |
| 54 | | | | | | |
| 55 | Diode D1 conduction losses | Diode D1 cond | 0 | 0 | 0 | 0 |
| 56 | Diode D1 switching losses | Diode D1 sw | 0 | 0 | 9 | 9 |
| 57 | Diode D1 total losses | Diode D1 tot | 0 | 0 | 9 | 10 |
| 58 | | | | | | |
| 59 | IGBT-diode V1 bond losses | Bond of V1 | 0 | 0 | 1 | 1 |
| 60 | | | | | | |
| 61 | IGBT-diode V1 total losses | Device V1 | 0 | 27 | 65 | 95 |
| 62 | | | | | | |
| 63 | IGBT S2 conduction losses | IGBT S2 cond | 0 | 7 | 16 | 26 |
| 64 | IGBT S2 switching losses | IGBT S2 sw | 0 | 2 | 4 | 5 |
| 65 | IGBT S2 total losses | IGBT S2 tot | 0 | 9 | 20 | 32 |
| 66 | | | | | | |
| 67 | Diode D2 conduction losses | Diode D2 cond | 0 | 0 | 0 | 0 |
| 68 | Diode D2 switching losses | Diode D2 sw | 0 | 0 | 9 | 9 |
| 69 | Diode D2 total losses | Diode D2 tot | 0 | 0 | 9 | 10 |
| 70 | | | | | | |
| 71 | IGBT-diode V2 bond losses | Bond of V2 | 0 | 0 | 1 | 2 |
| 72 | | | | | | |
| 73 | IGBT-diode V2 total losses | Device V2 | 0 | 9 | 30 | 43 |
| 74 | | | | | | |
| 75 | Diode D5 conduction losses | Diode D5 cond | 0 | 3 | 5 | 8 |
| 76 | Diode D5 switching losses | Diode D5 sw | 0 | 0 | 89 | 92 |
| 77 | Diode D5 total losses | Diode D5 tot | 0 | 3 | 94 | 101 |
| 78 | | | | | | |
| 79 | Total inverter losses | Inverter [kW] | 0.0 | 0.2 | 1.1 | 1.4 |
| 80 | % total inverter losses | Inverter [%] | | 0.88% | 2.11% | 1.78% |

| | | | | | | |
|---|---|---|---|---|---|---|
| 83 | **Temperatures** | | | | | |
| 84 | Ambient | Ta | 40 | 40 | 40 | 40 |
| 85 | Heat sink (under V1) | Th | 40 | 44 | 49 | 52 |
| 86 | Heat sink (under V2) | Th | 40 | 41 | 44 | 46 |
| 87 | Heat sink (under D5) | Th | 40 | 40 | 52 | 53 |
| 88 | Case (IGBT S1) | Tc,j | 40 | 44 | 49 | 52 |
| 89 | Case (Diode D1) | Tc,d | 40 | 44 | 49 | 52 |
| 90 | Case (IGBT S2) | Tc,j | 40 | 41 | 44 | 46 |
| 91 | Case (Diode D2) | Tc,d | 40 | 41 | 44 | 46 |
| 92 | Case (Diode D5) | Tc,d | 40 | 40 | 52 | 53 |
| 93 | IGBT S1 | Tj | 40 | 46 | 53 | 59 |
| 94 | Diode D1 | Td | 40 | 44 | 50 | 54 |
| 95 | IGBT S2 | Tj | 40 | 42 | 45 | 48 |
| 96 | Diode D2 | Td | 40 | 41 | 45 | 47 |
| 97 | Diode D5 | Td | 40 | 41 | 65 | 66 |

**Figure B.5.** Losses and temperatures for each semiconductor, as a function of the output current.

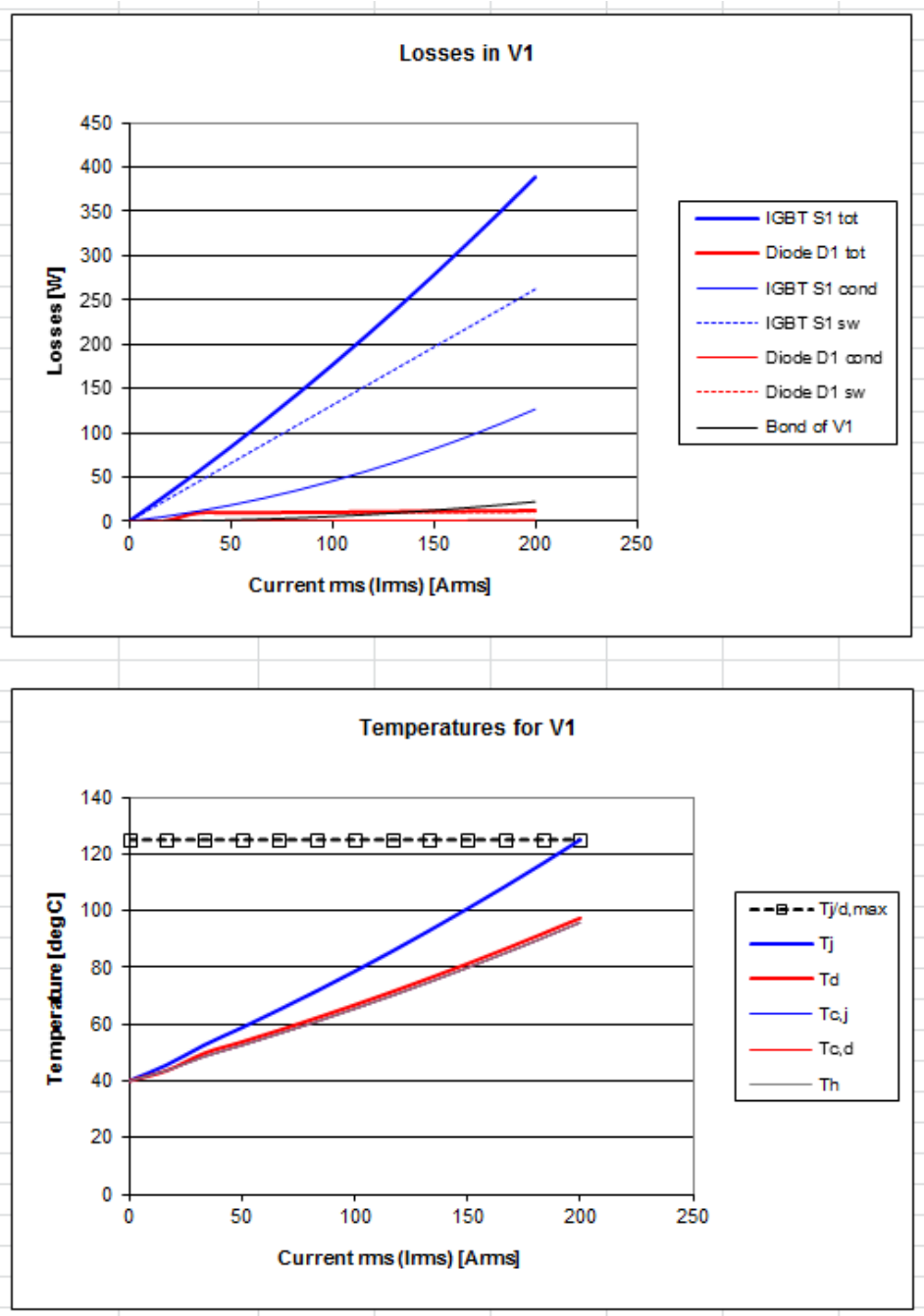


**Figure B.6.** Losses and temperatures for module $V_{1x}$, in a graphical form.

# Appendix C

# Single-phase transformerless PV inverter (Patent pending)

## C.1 Motivation

PV inverters (dc to ac power electronic converters) convert the direct current generated by the PV panels to alternating current, which is then supplied to the grid. Traditional PV inverter configurations contain transformers that provide galvanic isolation between the PV array of panels and the grid. In the absence of a transformer, however, leakage currents can circulate in a path formed by the PV array, the inverter, the (grounded) grid neutral, and the ground (Figure C.1). Even if the PV array is not grounded using an earth rod, its large surface laid against the ground forms a parasitic capacitance (in the order of nF to μF) that can conduct HF (in the order of kHz) common-mode leakage currents. Leakage currents damage the PV panels and bring up safety issues, and therefore have to be kept as low as possible (in the order of mA).

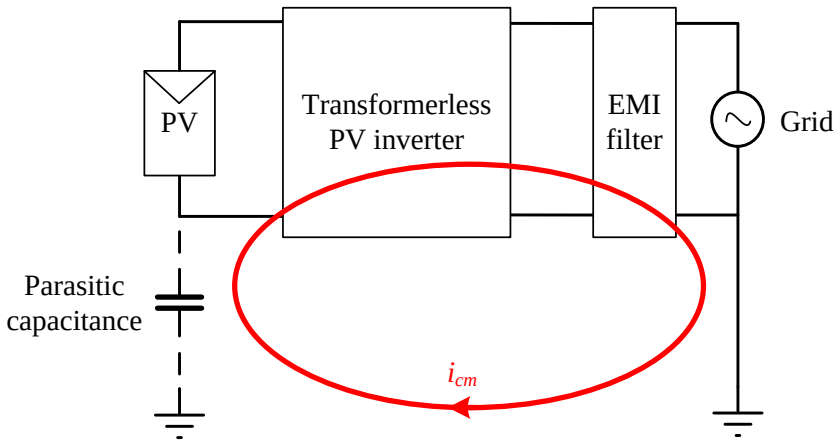


**Figure C.1.** Common-mode current ($i_{cm}$) circulation path, through the PV array's parasitic capacitance **[84]**.

## C.2 Solution – Existing topologies

Leakage currents are generated when the voltage of the PV panels with respect to ground fluctuates at HF. In this study, $v_{PV+}$ and $v_{PV-}$ will be used to denote the voltage of the positive and negative PV rail w.r.t. ground, respectively ($v_{PV+} = v_{PV-} + V_{PV}$). HF fluctuations on $v_{PV+}$ (and $v_{PV-}$) arise from the PWM operation of the inverter. The fluctuations appear across the parasitic capacitance, which has low impedance at HF, and therefore allows leakage currents to flow through it. The solution to the problem is therefore to stabilize, or only allow a LF fluctuation of $v_{PV+}$.

The value of $v_{PV+}$ is a function of the grid voltage ($v_{grid}$), the PV array output dc voltage ($V_{PV}$), and the inverter switching state. The frequency of $v_{grid}$ is typically 50 or 60 Hz, while $V_{PV}$ also varies slowly (in the order of Hz), depending on the instantaneous value of irradiance on the PV array. Thus, a value of

$$v_{PV+} = a v_{grid} + b V_{PV} \qquad \textbf{(C.1)}$$

($a$ and $b$ are constants) does not contain any high-frequency components that give rise to leakage currents.

### C.2.1 Topologies based on the NPC inverter

Figures C.2 – C.4 and C.6 – C.9 illustrate a number of existing transformerless PV inverter topologies. The first two topologies,

- the single-phase NPC inverter (Figure C.2) [49], and
- the inverter patented by Conergy (Figure C.3) [85, 86]

are related to the NPC topology. They both use a single reactor (L1) for their output filter, connected to one of their output terminals. The other terminal is connected to the grid neutral, which is grounded. As a result, $v_{PV+}$ takes the value of the upper capacitor voltage,

$$v_{PV+} = v_{C1} = 0.5 V_{PV}\,, \qquad \textbf{(C.2)}$$

avoiding high-frequency fluctuations according to (C.1) ($a = 0$ and $b = 0.5$).

The NPC inverter is built using modules with a voltage rating of $V_{PV}/2$, and is modulated as described in Chapter 2. The Conegy inverter, on the other hand, requires two modules (V1 and V2) to be rated at $V_{PV}$, while its zero state is achieved by turning on modules V3 and V4.

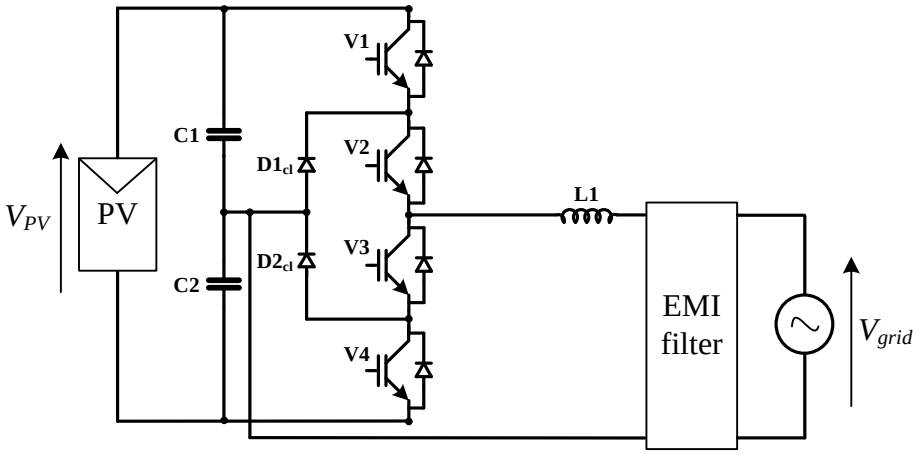


**Figure C.2.** NPC inverter topology **[49]**.

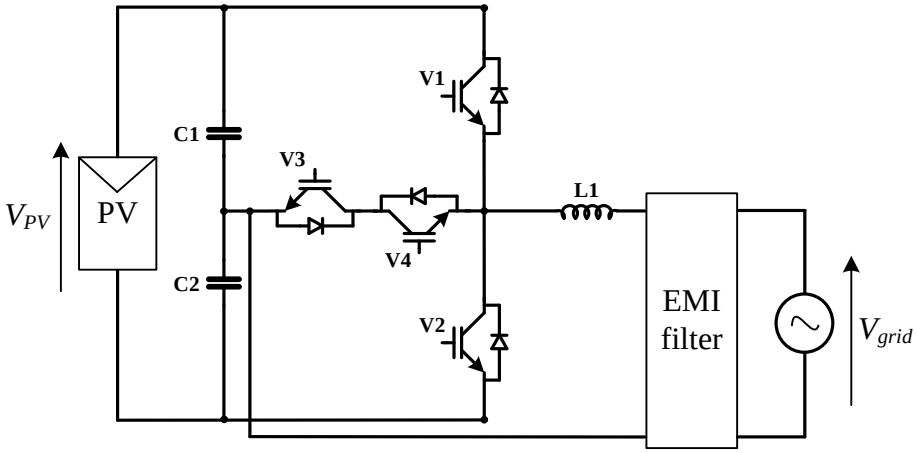


**Figure C.3.** Conergy inverter topology **[85]**.

### C.2.2 Topologies based on the H-Bridge inverter

Figures C.6 to C.9, illustrate topologies that originate from the single-phase H-Bridge inverter (Figure C.4). It has been demonstrated by several researchers [84, 87] that such topologies can avoid high-frequency fluctuations of $v_{PV+}$ only by:

- Splitting the output filter reactor in two (L1, L2), and connecting one to each output terminal, and at the same time

- ensuring that the common-mode voltage, $v_{cm}$, defined as $(v_A + v_B)/2$, is equal to $V_{PV}/2$ for all inverter switching states (points A, B and voltages $v_A$, $v_B$ are shown in Figure C.4).

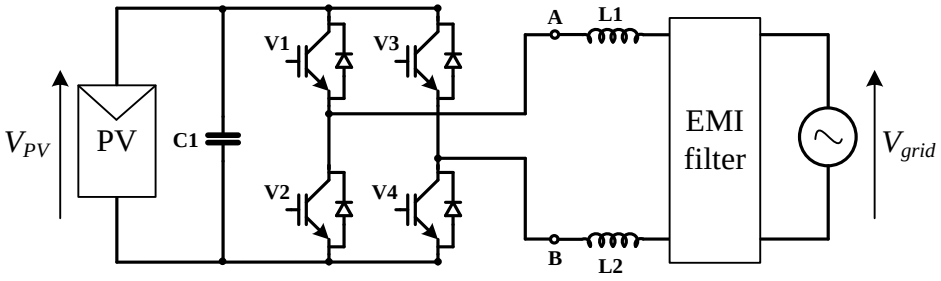


**Figure C.4.** Conventional H-Bridge inverter topology.

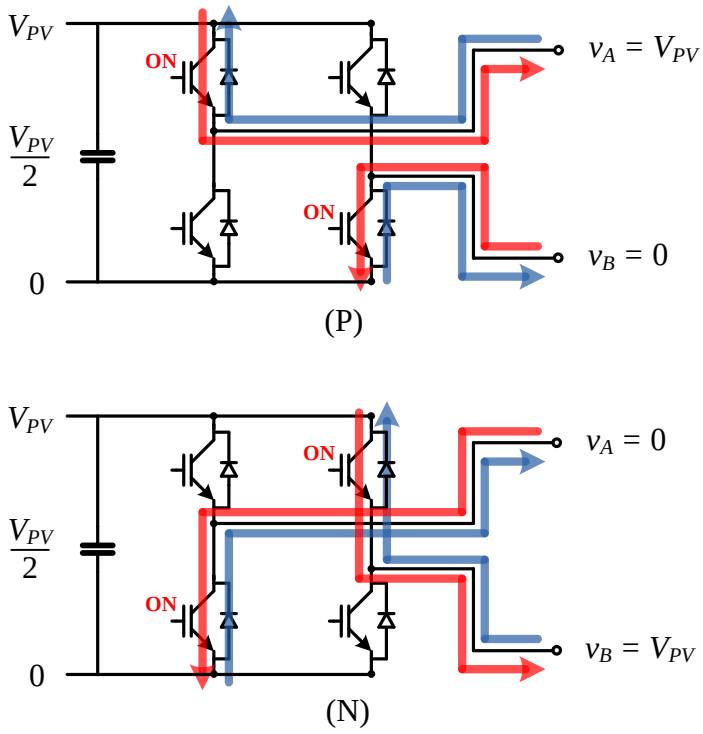


**Figure C.5.** Switching states and conduction paths for the H-Bridge inverter under bipolar modulation: (P) $v_{AB} = V_{PV}$, and (N) $v_{AB} = -V_{PV}$. Voltages $v_A$ and $v_B$ are shown w.r.t the negative PV rail. Arrows illustrate the conduction paths for both directions of current.

The H-Bridge inverter itself can be used as a transformerless PV topology, under bipolar modulation. This strategy only uses the positive (P) and negative (N) switching states of the

H-Bridge, illustrated in Figure C.5. The positive and negative states can be used, since the value of $v_{cm}$, derived in Table C.1 below, is equal to $V_{PV}/2$ for both of them.

| State | $v_A$ | $v_B$ | $v_{cm}$ |
|---|---|---|---|
| P: (V1-V4) | $V_{PV}$ | 0 | $V_{PV}/2$ |
| N: (V2-V3) | 0 | $V_{PV}$ | $V_{PV}/2$ |

**Table C.1.** Switching states for the H-Bridge inverter under bipolar modulation.

On the contrary, as shown in Table C.2, the H-Bridge zero states, $Z_P$ and $Z_N$, give a common-mode voltage which is different than $V_{PV}/2$. Hence, these states have to be avoided in an H-Bridge transformerless PV inverter.

| State | $v_A$ | $v_B$ | $v_{cm}$ |
|---|---|---|---|
| $Z_P$: (V1-V3) | $V_{PV}$ | $V_{PV}$ | $V_{PV}$ |
| $Z_N$: (V2-V4) | 0 | 0 | 0 |

**Table C.2.** Zero (forbidden) switching states $Z_P$ and $Z_N$ for the H-Bridge transformerless PV inverter.

Nevertheless, switching an H-Bridge between the positive and negative states (without zero states) deteriorates the quality of its PWM output voltage, since it results into a two-level (instead of three-level) waveform. In order to cover this drawback, transformerless PV inverter topologies based on the H-Bridge, introduce different circuit modifications to create their zero states. Their operation relies on one of the following two alternatives:

A. Keeping $v_{cm}$ equal to $V_{PV}/2$ during all inverter states, or
B. Keeping $v_{cm}$ equal to $V_{PV}/2$ during the positive and negative inverter states, and disconnecting the PV array from the grid during the zero states.

Transformerless PV inverter topologies that operate according to the first alternative are

- the iH5 inverter (Figure C.6) [88], and
- the H6 inverter (Figure C.7) [89, 90],

while topologies based on the second alternative are

- the H5 inverter (Figure C.8) [91], and
- the HERIC inverter (Figure C.9) [92].

The zero states of the above topologies are summarized in Table C.3.

| Topology | Zero state(s) |
|---|---|
| iH5 | (V1-V3-V6) |
| H6 | (V1-V3-V5-V6) or (V2-V4-V5-V6) |
| H5 | (V1-V3) |
| HERIC | (V5-V6) |

**Table C.3.** Zero states for transformerless topologies based on the H-Bridge inverter.

The iH5 and H6 inverters clamp the voltage of their zero state conduction path to the mid dc-bus voltage. This way, $v_A$, $v_B$ (see Figure C.4) and $v_{cm}$ become equal to $V_{PV}/2$ during the zero states, too. H5, on the other hand, implements a technique known as "dc bypass", decoupling the PV array from the rest of the circuit during its zero state ($Z_P$). Similarly, HERIC implements an "ac bypass", by modifying the ac side of the circuit to achieve the same effect.

According to [87, 88], the approach of iH5 and H6 (i.e., keeping $v_{cm}$ equal to $V_{PV}/2$ during all inverter states) is more reliable regarding leakage current suppression, because it has a lower dependency on the parasitic elements of the inverter circuit. Furthermore, the advantage of all topologies based on the H-Bridge as compared to those based on the NPC inverter, is that they require half the value of $V_{PV}$ to generate the same amplitude of ac voltage. In PV applications this is a significant advantage, since it affects the required number of panels per PV array, and relates to safety regulations regarding dc voltage levels.

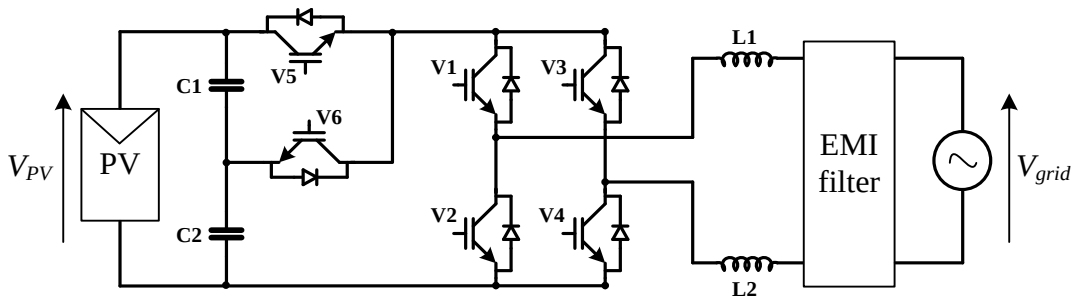


**Figure C.6.** iH5 PV inverter topology **[88]**.

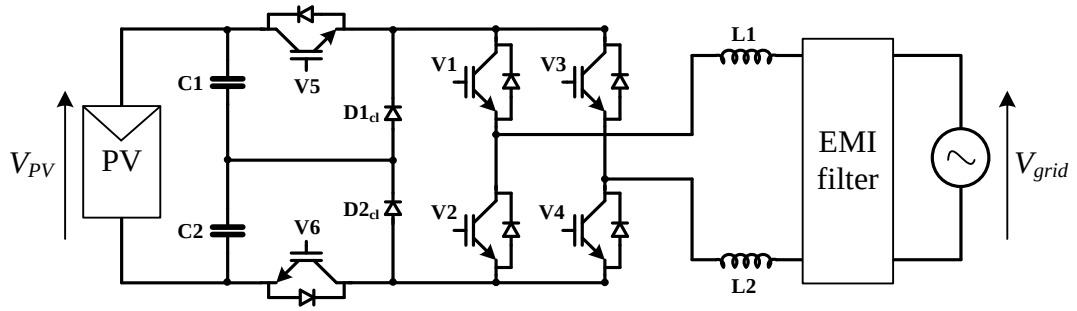


**Figure C.7.** H6 PV inverter topology **[89, 90]**.

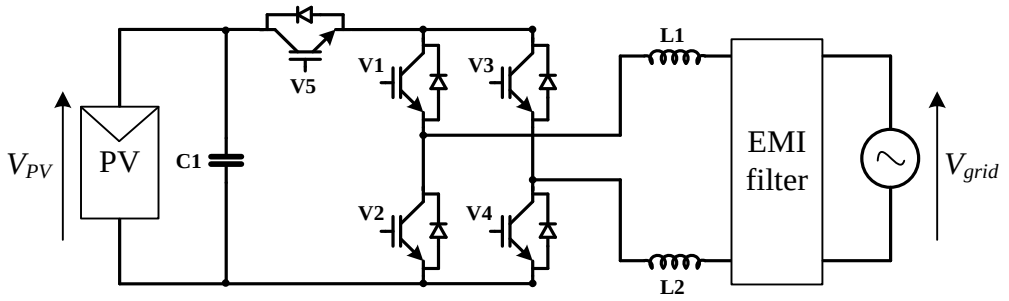


**Figure C.8.** H5 PV inverter topology **[91]**.

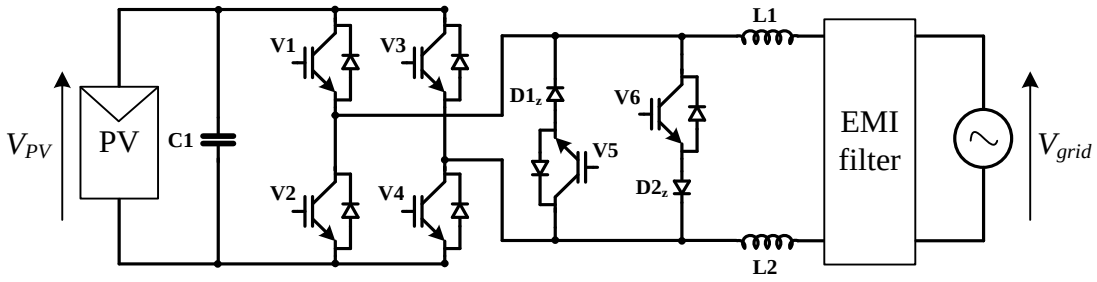


**Figure C.9.** HERIC PV inverter topology **[92]**.

## C.3 Proposed topology

The proposed transformerless PV inverter topology is illustrated in Figure C.10, below.

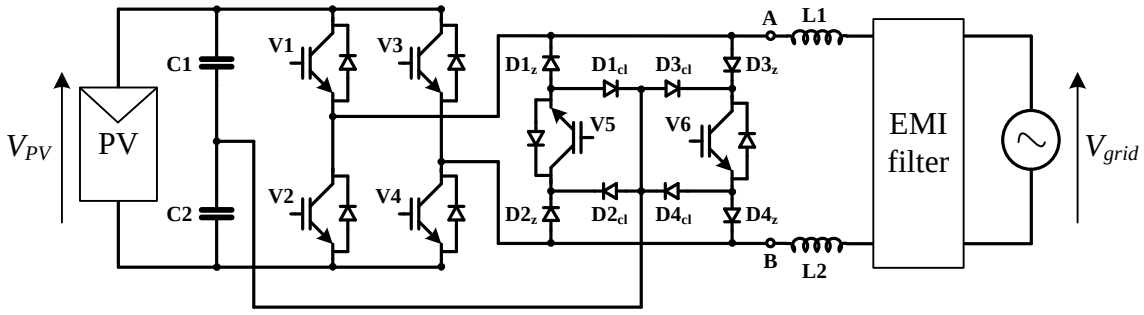


**Figure C.10.** Proposed transformerless PV inverter topology.

### C.3.1 Concept – Structure

The basic structure of the proposed topology is similar to that of the HERIC inverter. However, the topology operates according to the first alternative (in Section C.2.2), and therefore does not disconnect the PV array from the grid at any time. It actually extends the ac bypass of the HERIC inverter in the same way that iH5 extends the dc bypass of the H5 inverter. Namely, it adopts the zero state of the HERIC inverter, but also uses a capacitor bank that is split in two, to provide a connection point at half the voltage of the dc bus ($V_{PV}/2$). Additionally, it introduces a mid dc-bus clamping branch, consisting of diodes $D1_{cl}$, $D2_{cl}$, $D3_{cl}$, and $D4_{cl}$. During the inverter zero state (V5-V6), these diodes clamp the voltage of points A and B to the mid-dc bus and set $v_{cm}$ to $V_{PV}/2$, as shown in the following section.

### C.3.2 Switching states and common-mode voltage

Figure C.11 illustrates the switching states for the proposed topology, together with the respective conduction paths. The respective common-mode voltages are presented in Table C.4. The zero state, Z, is used in place of the conventional zero states $Z_P$ and $Z_N$.

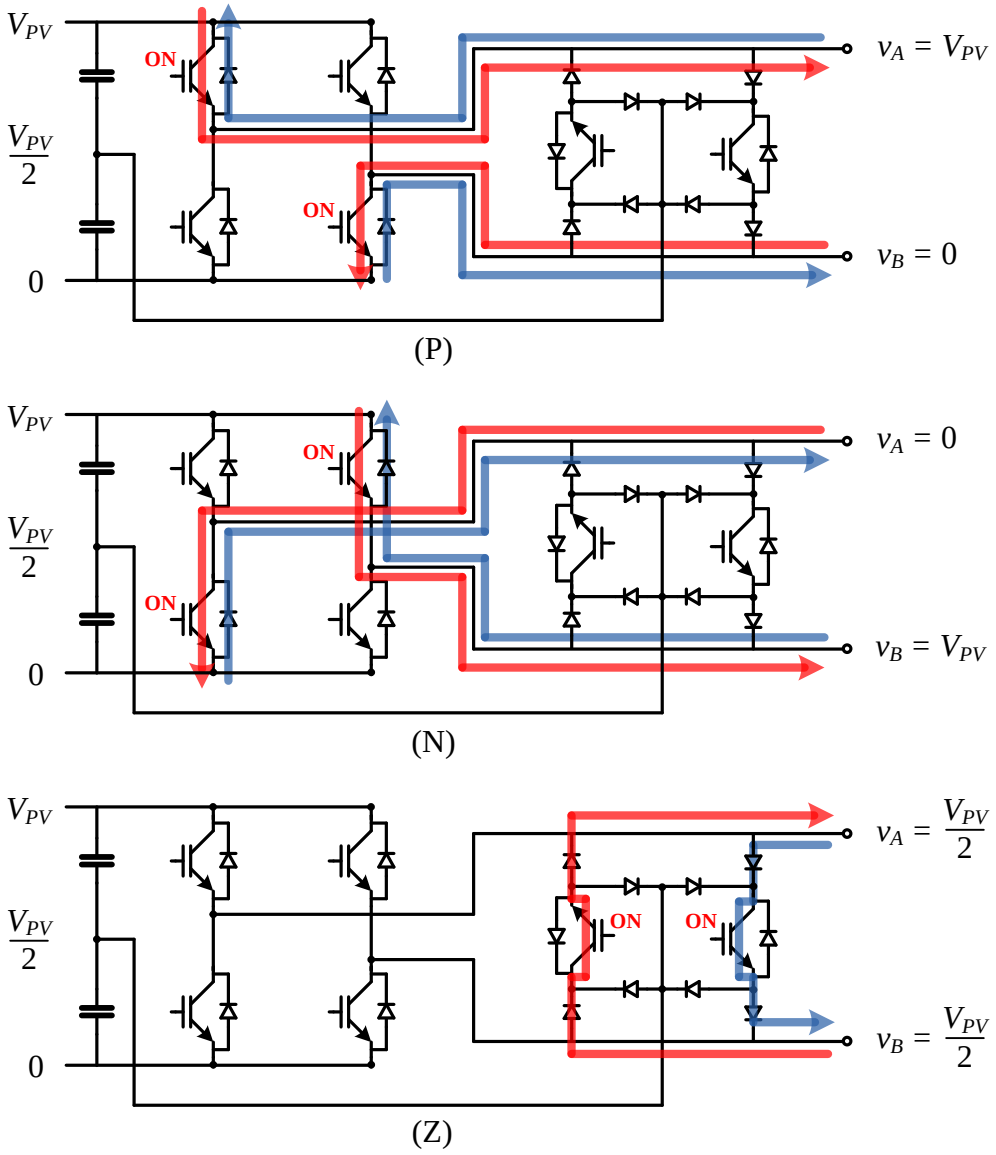


**Figure C.11.** Switching states and conduction paths for the proposed PV inverter: (P) $v_{AB} = V_{PV}$, (N) $v_{AB} = -V_{PV}$, and (Z) $v_{AB} = 0$. Voltages $v_A$ and $v_B$ are shown w.r.t the negative PV rail.

| State | $v_A$ | $v_B$ | $v_{cm}$ |
|---|---|---|---|
| P: (V1-V4) | $V_{PV}$ | 0 | $V_{PV}/2$ |
| N: (V2-V3) | 0 | $V_{PV}$ | $V_{PV}/2$ |
| Z: (V5-V6) | $V_{PV}/2$ | $V_{PV}/2$ | $V_{PV}/2$ |

**Table C.4.** Switching states for the proposed PV inverter.

### C.3.3 Simulation results

The proposed PV inverter topology was simulated according to the following parameters:

| Parameter | Value |
|---|---|
| $V_{dc}$ | 400 V |
| $I_{pk}$ | 117 A, $\phi$ = −8 degrees |
| $f$ | 50 Hz |
| $f_c$ | 5 kHz |
| $M$ | 0.8 |
| $L$ for L1, L2 | 0.6 mH |
| $V_{grid}$ | 315 V, $\phi$ = −8 degrees |

**Table C.5.** Simulation parameters.

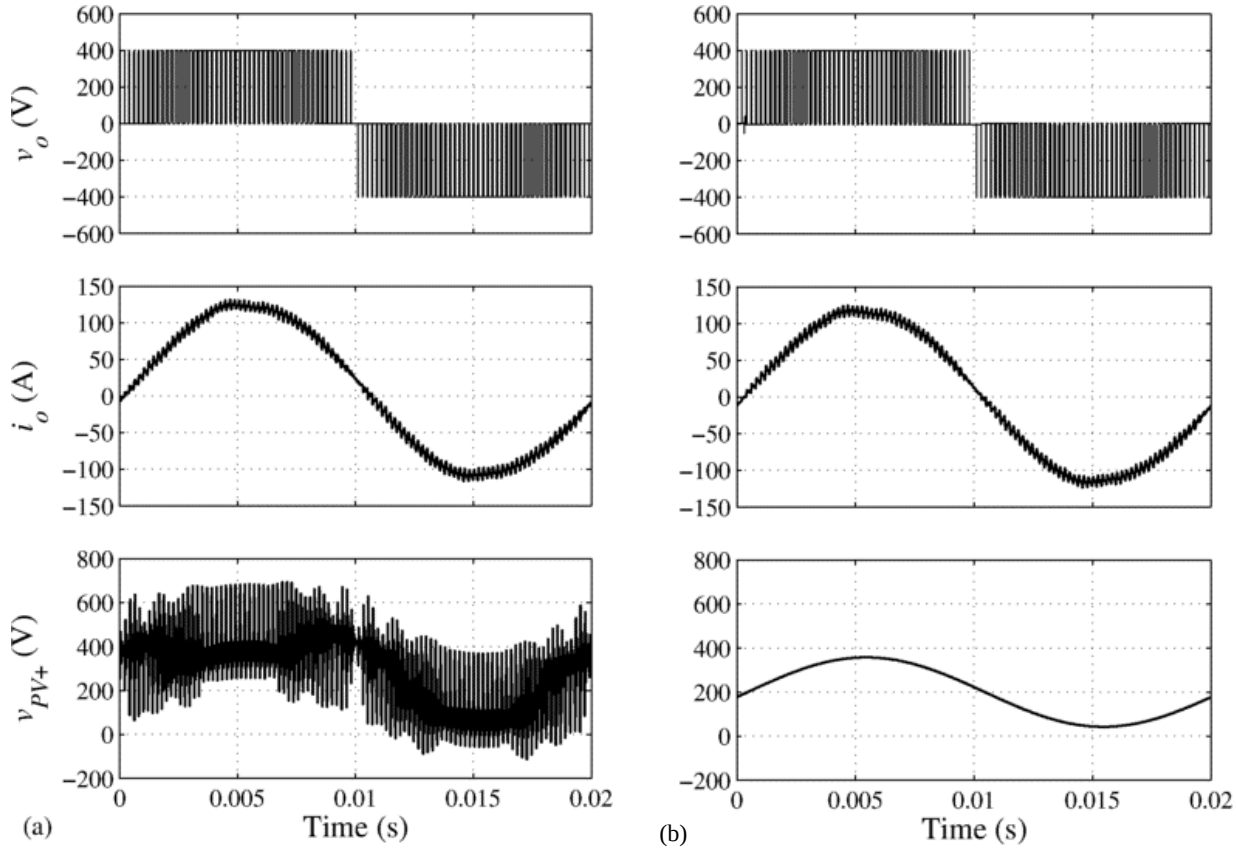


**Figure C.12.** Simulated results of the proposed PV inverter operating with the parameters of Table C.5: (a) Using the zero states $Z_P$ and $Z_N$, (b) Using the proposed zero state Z.

From Figure C.12, it can be observed that the proposed PV inverter can avoid the high-frequency fluctuations of $v_{PV+}$ generated by the conventional H-Bridge zero states. Namely,

by using state Z as a zero state, $v_{PV+}$ becomes equal to $0.5v_{grid} + 0.5V_{PV}$ for all inverter states, thus only includes a low-frequency fluctuation at the frequency of the grid (50 or 60 Hz).

The presented analysis and results indicate that the proposed topology can be used as a transformerless inverter for the suppression of leakage currents in PV applications. In comparison to the inverters in Figures C.6 – C.9, this topology can be expected to have higher cost, due to the increased number of diodes that it requires. It is noted, though, that the clamping diodes ($D1_{cl}$ – $D4_{cl}$) can have a voltage rating of $V_{PV}/2$ and a very low current rating, since they only have to carry leakage currents (less than mA).

# References

[1] F. Blaabjerg, F. Iov, T. Terekes, R. Teodorescu, and K. Ma, "Power electronics - key technology for renewable energy systems," in *Power Electronics, Drive Systems and Technologies Conference (PEDSTC)*, 2011.

[2] J. Dixon, J. Pereda, C. Castillo, and S. Bosch, "Asymmetrical Multilevel Inverter for Traction Drives Using Only One DC Supply," *IEEE Transactions on Vehicular Technology*, vol. 59, no. 8, pp. 3736-3743, 2010.

[3] J. M. Apsley, A. Gonzalez-Villasenor, M. Barnes, A. C. Smith, S. Williamson, J. D. Schuddebeurs, P. J. Norman, C. D. Booth, G. M. Burt, and J. R. McDonald, "Propulsion Drive Models for Full Electric Marine Propulsion Systems," *IEEE Transactions on Industry Applications* , vol. 45, no. 2, pp. 676-684, 2009.

[4] J. Rodriguez et al., "Multilevel Converters: An Enabling Technology for High-Power Applications," *Proceedings of the IEEE,* vol. 97, no. 11, pp. 1786-1817, 2009.

[5] S. Kouro et al., "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 8, pp. 2553-2580, 2010.

[6] H. Abu-Rub, J. Holtz, J. Rodriguez, and Ge Baoming, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 8, pp. 2581-2596, 2010.

[7] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 7, pp. 2219-2230, 2010.

[8] S. S. Fazel, "Investigation and Comparison of Multi-Level Converters for Medium

Voltage," Ph.D. Thesis, Berlin Technical University, 2007.

[9] S. R. Minshull, C. M. Bingham, D. A. Stone, and M. P. Foster, "Frequency reduction schemes for back-to-back connected, diode-clamped multilevel converters," *IET Power Electronics,* vol. 3, no. 1, pp. 65-74, 2010.

[10] Datasheet F3L300R07PE4, "Technical Information IGBT Modules," Infineon Technologies AG, Warstein, Germany, 2011.

[11] Datasheet SK100MLI0066T, "Technical Information IGBT Modules," SEMIKRON, Nuremberg, Germany, 2009.

[12] A. M. Hava, R. J Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Transactions on Power Electronics,* vol. 14, no. 1, pp. 49-61, 1999.

[13] D. G. Holmes, and T. A. Lipo, Pulse Width Modulation for Power Converters, Piscataway, NJ: IEEE Press, 2003.

[14] A. Bendre, S. Krstic, J. Vander Meer, G. Venkataramanan, "Comparative evaluation of modulation algorithms for neutral-point-clamped converters," *IEEE Transactions on Industry Applications,* vol. 41, no. 2, pp. 634- 643, 2005.

[15] K. Lee, and G. Nojima, "Quantitative Power Quality and Characteristic Analysis of Multilevel Pulsewidth-Modulation Methods for Three-Level Neutral-Point-Clamped Medium-Voltage Industrial Drives," *IEEE Transactions on Industry Applications,* vol. 48, no. 4, pp. 1364-1373, 2012.

[16] T. Bruckner and D. G. Holmes, "Optimal Pulse-Width Modulation for three-level inverters," *IEEE Transactions on Power Electronics,* vol. 20, no. 1, pp. 82-89, 2005.

[17] F. Wang, "Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters," *IEEE Transactions on Industry Applications,* vol. 38, no. 2, pp. 500-

506, 2002.

[18] Cao Da-peng, S. Wen-xiang, X. I. Hui, C. Guo-cheng, and C. Chen, "Research on zero-sequence signal of space vector modulation for three-level neutral-point-clamped inverter based on vector diagram partition," in *IEEE 6th International Power Electronics and Motion Control Conference*, 2009.

[19] N. V. Nho, and M.-J. Youn, "Comprehensive study on space-vector-PWM and carrier-based-PWM correlation in multilevel invertors," *IEE Proceedings on Electric Power Applications*, vol. 153, no. 1, pp. 149-158, 2006.

[20] H. Akagi, and T. Shimizu, "Attenuation of Conducted EMI Emissions From an Inverter-Driven Motor," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 282-290, 2008.

[21] A. Videt, P. Le Moigne, N. Idir, P. Baudesson, and X. Cimetiere, "A new Carrier-Based PWM providing Common-Mode-Current reduction and dc-bus balancing for three-level inverters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3001-3011, 2007.

[22] Z. Zhao, Y. Zhong, H. Gao, L. Yuan, and T. Lu, "Hybrid Selective Harmonic Elimination PWM for Common-Mode Voltage Reduction in Three-Level Neutral-Point-Clamped Inverters for Variable Speed Induction Drives," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1152-1158, 2012.

[23] S. Figarado, T. Bhattacharya, G. Mondal, and K. Gopakumar, "Three-level inverter scheme with reduced power device count for an induction motor drive with common-mode voltage elimination," *IET Power Electronics* , vol. 1, no. 1, pp. 84-92, 2008.

[24] B. Wu, High-Power Converters and AC Drives, Piscataway, NJ: IEEE Press, 2006.

[25] Nippon Chemi-Con., "Aluminum Elextrolytic Capacitors Catalog No. E1001M," Techical note, 2012.

[26] ELECTRONICON, "Capacitors for power electronics - Application Notes - Selection Guide," Germany, 2012.

[27] N. Kaminski and A. Kopta, Failure rates of HiPak modules due to cosmic rays, Lenzburg, Switzerland: ABB Switzerland Ltd, Appl. Note 5SYA2042-04, 2011.

[28] N. Celanovic, I. Celanovic, and D. Boroyevich, "The feedforward method of controlling three-level diode clamped converters with small DC-link capacitors," in *Proceedings of 32nd Annual IEEE PESC,* 2001.

[29] A. Von Jouanne, S. Dai, and H. Zhang, "A multilevel inverter approach providing dc-link balancing, ride-through enhancement, and common mode voltage elimination," *IEEE Transactions on Industrial Electronics,* vol. 49, no. 4, pp. 739-745, 2002.

[30] D. H. Lee, S. R. Lee, and F. C. Lee, "An analysis of midpoint balance for the neutral-point-clamped three level VSI," in *Proceedings of IEEE Power Electronics Specialists,* 1998.

[31] J. Pou, D. Boroyevich, and R. Pindado, "New feedforward space-vector PWM method to obtain balanced ac output voltages in a three-level neutral-point-clamped converter," *IEEE Transactions on Power Electronics,* vol. 49, no. 5, pp. 1026-1034, 2002.

[32] J. Pou, J. Zaragoza, P. Rodriguez, S. Ceballos, V. M. Sala, R. P. Burgos, and D. Boroyevich, "Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point," *IEEE Transactions on Industrial Electronics,* vol. 54, no. 4, pp. 2288-2294, 2007.

[33] S. Busquets-Monge, J. Bordonau, D. Boroyevich, and S. Somavilla, "The nearest three virtual space vector PWM - A modulation for the comprehensive neutral-point balancing in the three-level NPC inverter," *IEEE Power Electronic Letters,* vol. 2, no. 1, pp. 11-15, 2004.

[34] S. Busquets-Monge, S. Somavilla, J. Bordonau, and D. Boroyevich, "Capacitor voltage balance for the neutral-point-clamped converter using the virtual space vector concept with optimized spectral performance," *IEEE Transactions on Power Electronics,* vol. 22, no. 4, pp. 1128-1135, 2007.

[35] M. Saeedifard, R. Iravani, and J. Pou, "Analysis and control of DC-capacitor-voltage-drift phenomenon of a passive Front-End five-level converter," *IEEE Transactions on Industrial Electronics,* vol. 54, no. 6, pp. 3255-3266, 2007.

[36] H. Iman-Eini, J.-L. Schanen, S. Farhangi, and J. Roudet, "A Modular Strategy for Control and Voltage Balancing of Cascaded H-Bridge Rectifiers," *IEEE Transactions on Power Electronics,* vol. 23, no. 5, pp. 2428-2442, 2008.

[37] S. Vazquez, J. I. Leon, J. M. Carrasco, L. G. Franquelo, and E. Galvan, "Analysis of the Power Balance in the Cells of a Multilevel Cascaded H-Bridge Converter," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 7, pp. 2287-2296, 2010.

[38] P. Lezana, J. Rodriguez, and D. A. Oyarzun, "Cascaded Multilevel Inverter With Regeneration Capability and Reduced Number of Switches," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 3, pp. 1059-1066, 2008.

[39] J. Rodriguez, J. Pontt, M. Perez, P. Lezana, and P. W. Hammond, "High Power Synchronous Machine fed by a Cascaded Regenerative Inverter," in *Industry Applications Society Annual Meeting,* 2008.

[40] C. Wang, and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level NPC converters," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 7, pp. 2262-2271, 2010.

[41] J. Pou et al., "A Carrier-Based PWM strategy with Zero-Sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Transactions on Power Electronics,* vol. 27, no. 2, pp. 642-651, 2012.

[42] BHC Components, "Aluminum Electrolytic Capacitors," Application notes, 2002.

[43] P. A. Dahono, Y. Sato, and T. Kataoka, "Analysis and minimization of ripple components of input current and voltage of PWM inverters," *IEEE Transactions on Industry Applications,* vol. 32, no. 4, pp. 945-950, 1996.

[44] J. W. Kolar, T. M. Wolbank, and M. Schrodl, "Analytical calculation of the rms current stress on the DC link capacitor of voltage DC link PWM converter systems," in *Proceedings of the 9th International Conference on Electrical Machines and Drives*, Canterbury, UK, 1999.

[45] F. Renken, "Analytic calculation of the DC-link capacitor current for pulsed three-phase inverters," in *Proceedings of the 11th International Conference on Power Electronics and Motion Control*, Riga, Latvia, 2004.

[46] F. Renken, "The DC-link capacitor current in pulsed single-phase H-Bridge inverters," in *European Conference on Power Electronics Applications*, Dresden, Germany, 2005.

[47] M. H. Bierhoff, and F. W. Fuchs, "DC-link harmonics of three-phase voltage-source converters influenced by the pulsewidth-modulation strategy-An analysis," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 5, pp. 2085-2092, 2008.

[48] B. P. Mc Grath and D. H. Holmes, "A general analytical method for calculating inverter DC-link current harmonics," *IEEE Transactions on Industry Applications,* vol. 45, no. 5, pp. 1851-1859, 2009.

[49] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications,* Vols. IA-17, no. 5, pp. 518-523, 1981.

[50] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalán, "Voltage-balance compensator for Carrier-Based Modulation in the neutral-point-clamped converter," *IEEE Transactions on Industrial Electronics,* vol. 56, no. 2, pp. 305-314, 2009.

[51] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter," *IEEE Transactions on Industrial Electronics,* vol. 52, no. 6, pp. 1582-1588, 2005.

[52] K. Gupta and M. Khambadkone, "A simple Space Vector PWM scheme to operate a three-level NPC inverter at high modulation index including overmodulation region, with Neutral Point balancing," *IEEE Transactions on Industry Applications,* vol. 43, no. 3, pp. 751-760, 2007.

[53] D. Soto and T. C. Green, "A comparison of high-power converter topologies for the implementation of FACTS controllers," *IEEE Transactions on Industrial Electronics,* vol. 49, no. 5, pp. 1072-1080, 2002.

[54] G. I. Orfanoudakis, S. M. Sharkh, M. A. Yuratich and M. A. Abu – Sara, "Loss comparison of two and three-level inverter topologies," in *Proceedings of 5th International Conference on Power Electronics, Machines and Drives (PEMD)*, 2010.

[55] G. I. Orfanoudakis, S. M. Sharkh and M. A. Yuratich, "Analysis of DC-link capacitor losses in three-level neutral-point-clamped and cascaded H-bridge voltage source inverters," in *IEEE International Symposium on Industrial Electronics (ISIE),* Bari, Italy, 2010.

[56] H. S. Black, Modulation Theory, New York: Van Nostrand, 1953.

[57] K. Hasegawa, and H. Akagi, "Low-Modulation-Index Operation of a Five-Level Diode-Clamped PWM Inverter With a DC-Voltage-Balancing Circuit for a Motor Drive," *IEEE Transactions on Power Electronics,* vol. 27, no. 8, pp. 3495-3504, 2012.

[58] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 7, pp. 2197-2206, 2010.

[59] M. Sakui, and H. Fujita, "An Analytical Method for Calculating Harmonic Currents of a

Three-Phase Diode-Bridge Rectifier with dc Filter," *IEEE Transactions on Power Electronics,* vol. 9, no. 6, pp. 631-637, 1994.

[60] A. Emadi, Energy-Efficient Electric Motors, Third ed., New York: Marcel Dekker, 2005.

[61] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction and utility applications," *IEEE Transactions on Industry Applications,* vol. 41, no. 3, pp. 855-865, 2005.

[62] N. Celanovic, and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Transactions on Power Electronics,* vol. 15, no. 2, pp. 242-249, 2000.

[63] N. Celanovic, and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Transactions on Industry Applications,* vol. 37, no. 2, pp. 637-641, 2001.

[64] H. B. Zhang, S. J. Finney, A. Massoud, and B. W. Williams, "An SVM algorithm to balance the capacitor voltages of the three-level NPC Active Power Filter," *IEEE Transactions on Power Electronics,* vol. 23, no. 6, pp. 2694-2702, 2008.

[65] A. Lewicki, Z. Krzeminski, and H. Abu-Rub, "Space-Vector Pulse Width Modulation for three-level NPC converter with the neutral point voltage control," *IEEE Transactions on Industrial Electronics,* vol. 58, no. 11, pp. 5076-5086, 2011.

[66] S. Busquets-Monge, J. D. Ortega, J. Bordonau, J. A. Beristain, and J. Rocabert, "Closed-Loop Control of a Three-Phase neutral-point-clamped inverter using an optimized Virtual-Vector-Based Pulsewidth Modulation," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 5, pp. 2061-2071, 2008.

[67] C. Newton and M. Sumner, "Neutral point control for multi-level inverters: theory, design and operational limitations," in *IEEE Industry Applications Society Annual*

*Meeting*, New Orleans, LA, 1997.

[68] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *IEEE IAS Annual Meeting*, 1993.

[69] R. M. Tallam, R. Naik, and T. A. Nondahl, "A Carrier-Based PWM scheme for neutral-point voltage balancing in three-level inverters," *IEEE Transactions on Industry Applications*, vol. 41, no. 6, pp. 1734-1743, 2005.

[70] J. Zaragoza, J. Pou, A. Arias, S. Ceballos, E. Robles, P. Ibáñez, and I. Gabiola, "Amplitude control of the neutral-point voltage oscillations in the three-level converter," in *IEEE PESC*, 2008.

[71] J. I. Leon et al., "Three-Dimensional feedforward Space Vector Modulation applied to multilevel Diode-Clamped converters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 1, pp. 101-109, 2009.

[72] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibáñez, and J. L. Villate, "A comprehensive study of a hybrid modulation technique for the neutral-point-clamped converter," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 294-304, 2009.

[73] A. D. Rajapakse, A. M. Gole, and P. L. Wilson, "Electromagnetic Transients Simulation Models for Accurate Representation of Switching Losses and Thermal Performance in Power Electronic Systems," *IEEE Transactions on Power Delivery*, vol. 20, no. 1, 2005.

[74] A. D. Rajapakse, A. M. Gole, and P. L. Wilson, "Approximate Loss Formulae for Estimation of IGBT Switching Losses through EMTP-type Simulations," in *International Conference on Power Systems Transients (IPST)*, 2005.

[75] O. Al-Naseem, R. W. Erickson and P. Carlin, "Prediction of switching loss variations by averaged switch modeling," in *Applied Power Electronics Conference and Exposition Annual IEEE Conference - APEC*, 2000.

[76] F. Blaabjerg, “An extended model of power losses in hard-switched IGBT-inverters,” in *Industry Applications Conference. Thirty-First IAS Annual Meeting, IAS '96., Conference Record of the 1996 IEEE,* 1996.

[77] Infineon, “IGBT/Diode module data sheets,” Available: www.infineon.com.

[78] F. Casanellas, “Losses in PWM inverters using IGBTs,” in *Electric Power Applications, IEE Proceedings* , 1994.

[79] L.K. Mestha, and P.D. Evans, “Analysis of on-state losses in PWM inverters,” in *Electric Power Applications, IEE Proceedings B,* 1989.

[80] S. Dieckerhoff, S. Bernet, and D. Krug, “Power loss-oriented evaluation of high voltage IGBTs and multilevel converters in transformerless traction applications,” *IEEE Transactions on Power Electronics,* vol. 20, no. 6, pp. 1328-1336, 2005.

[81] J. W. Kolar, H. Ertl, and F. C. Zach, “Influence of the modulation method on the conduction and switching losses of a PWM converter system,” *IEEE Transactions on Industry Applications,* vol. 27, no. 6, pp. 1063-1075, 1991.

[82] T.-J. Kim, D.-W. Kang, Y.-H. Lee, and D.-S. Hyun, “The analysis of conduction and switching losses in multi-level inverter system,” in *Power Electronics Specialists Conference. IEEE 32nd Annual,* 2001.

[83] Q. Wang, Q. Chen, W. Jiang, and C. Hu, “Analysis and comparison of conduction losses in neutral-point-clamped three-level inverter with PWM control,” in *International Conference on Electrical Machines and Systems,* 2007.

[84] E. Gubıa, P. Sanchis, A. Ursua, J. Lopez, and L. Marroyo, “Ground Currents in Single-phase Transformerless Photovoltaic Systems,” *Progress in Photovoltaics: Research and Applications,* vol. 15, p. 629–650, 2007.

[85] P. Knaup.International Patent WO 2007/048420 A1, 2007.

[86] M. Lin, T. Kerekes, R. Teodorescu, J. Xinmin, D. Floricau, and M. Liserre, "The high efficiency transformer-less PV inverter topologies derived from NPC topology," in *13th European Conference on Power Electronics and Applications (EPE)* , 2009.

[87] H. F. Xiao, and S. J. Xie, "Leakage Current Analytical Model and Application in Single-Phase Transformerless Photovoltaic Grid-Connected Inverter," *IEEE Transactions on Electromagnetic Compatibility,* vol. 52, no. 4, pp. 902-913, 2010.

[88] H. F. Xiao, S. J. Xie, C. Yang, and R. H. Huang, "An Optimized Transformerless Photovoltaic Grid-Connected Inverter," *IEEE Transactions on Industrial Electronics,* vol. 58, no. 5, pp. 1887-1895, 2011.

[89] R. Gonzalez, J. Coloma, L. Marroyo, J. Lopez and P. Sanchis, "Single-phase inverter circuit for conditioning and converting DC electrical energy into AC electrical energy". Europe Patent 2 053 730 A1, 2006.

[90] R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 7, p. 2694–2702, 2008.

[91] M. Victor, F. Greizer, S. Bremicker and U. Hubler, "Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into an alternating current voltage". U.S. Patent 7 411 802 B2, 2008.

[92] S. Heribert, S. Christoph and K. Jurgen, "Inverter for transforming a DC voltage into an AC current or an AC voltage". Europe Patent 1 369 985 A2, 2003.

[93] B. A. Welchko, "Analytical Calculation of the RMS Current Stress on the DC Link Capacitor for a VSI Employing Reduced Common Mode Voltage PWM," in *European Conference on Power Electronics and Applications,* 2007.