Verilog-A based Effective Complementary Resistive Switch Model for Simulations and Analysis

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***Abstract*— Resistive memory, also known as memristor, is recently emerging as a potential successor to traditional charge-based memories. However, the nanoscale features of these devices introduce challenges in modeling and simulation. In this paper, we propose a novel Verilog-A based complementary resistive switch memory model for effective simulation and analysis. Our proposed model captures desired non-linear characteristics using voltage based state control as opposed to recently proposed current based state control. We demonstrate that such state control has advantages for our proposed CRS model based crossbar arrays in terms of symmetric ON/OFF voltages and significantly reduced sneak path currents with high noise margin compared to traditional memristor based architectures. Moreover, to validate the effectiveness of our Verilog-A based model we carry out extensive simulations and analyses for different crossbar array architectures using traditional EDA tools.**

I. Introduction

Memristor based resistive-variable memory devices have recently been proposed to overcome the limitations of traditional CMOS based memories [1]. These devices have the basic principle of storing the information bits as variable resistance values. Unlike traditional two-terminal devices, such as inductor or capacitor, memristors exhibit non-volatile state retention characteristics, making them particularly suitable for stable data storage [1], [4]. Moreover, these devices can be fabricated with finer layouts and sizes using non-lithographic methods like imprint lithography enabling nanoscale geometries with short access latencies. With these coveted properties, memristors have the potential of realizations in current and future generations of static random access memories (SRAMs), dynamic random access memories (DRAMs) and flash memories. Hence, currently there is a lot of interest both in academia and in industry in the research and development of memristor based memory devices [2].

To extract the benefits of high efficiency and packing density, various memristor array architectures have been proposed to date. For example, passive crossbar arrays of memristive elements were reported as possible non-volatile random access memories (RAMs) in [3]. However, passive crossbar arrays have the general issue with sneak-path currents due to interference from the neighbouring cells when selecting a designated cell within the arrays. To avoid sneak-path currents, recently complementary resistive switches (CRS) were proposed [10], which consist of two anti-serial memristive elements. Such interconnection introduces intermediate memristor states that can reduce the sneak-path currents significantly, facilitating the development of large passive crossbar arrays with reduced power consumption [9].

Effective simulation model is a critical requirement for the development and validation of memristor based CRS in EDA tools [10]. Although number of memristor models have been reported so far, curently there is a lack of effective simulation model for memristor based CRS. For example, memristor models proposed in [5], [6], [7] are effective for modeling basic memristor characteristics with ion drift or non-linear ion drift behavior. However, these models cannot define the non-linear memristor characteristics required in CRS systems and hence are not suitable. In [12], another memristor model suitable for CRS modeling is proposed. However, this model lacks relationship between state variable and voltage needed for simulation modeling and interoperability in EDA tools. Recently, single memristor based model, called TEAM, has been proposed in [7]. This model can characterize the non-linear behavior of memristors. However, due to current based state control in memristors, it can exhibit asymmetric ON/OFF voltages (i.e. low ON voltage and high OFF voltage). Moreover, such high OFF voltages can affect the adjacent cells by causing possible state changes during read and write operations, limiting its effectiveness in CRS systems.

In this work, we propose a novel Verilog-A based CRS model with desired non-linear memristor characteristics, achieved through combination of linear behavior described by ion drift function [6] and non-linear behavior described by Butler-Volmer equation [12]. Moreover, our proposed model uses voltage based state control, which has the advantages of symmetric ON/OFF voltages with reduced sneak path currents to adjacent cells and inter-operability with other EDA tools. The rest of the paper is organized as follows. Section II provides motivation of our research highlighting the limitations of memristor based crossbar arrays, while Section III presents the proposed Verilog-A based CRS model. Section IV outlines the sneak path current analysis to demonstrate the advantages of our proposed model. Finally, Section V concludes the paper.

II. Motivation

Crossbar array based resistive memory architecture has been recently proposed for its efficiency and high packing density [8]. Fig. 1 shows a typical single memristor based crossbar array architecture. In the following, the limitations of this architecture during write and read operations are

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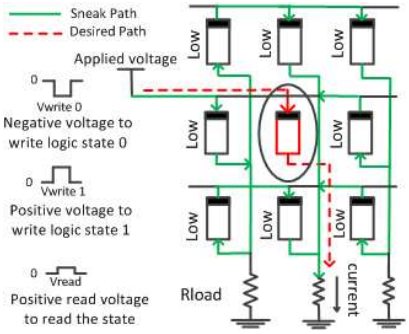

Fig. 1. Traditional memristor based crossbar architecture

highlighted, which motivates our research on an improved CRS based model (Section III).

A. Write Operation

To write logic ON state (i.e. 1) into a selected (i.e. circled) memristor based crossbar cell, a positive voltage V_{write} or V_{set} is applied in the select row for a given duration (Fig. 1) keeping other rows floating. With this voltage the memristance (i.e. resistance of the resistive-variable device) changes from R_{off} to R_{on}, where R_{on} is the ON state resistance and R_{off} is the OFF state resistance of the memristor. To write a logic OFF state (i.e. 0), a negative V_{write} or V_{clear} is applied across the device long enough for the memristance to increase from R_{on} to R_{off}. Such state control, however, exhibits higher OFF voltage (V_{clear}) compared to V_{set} when state transits from ON to OFF since the state derivative decreases sharply.

B. Read Operation

To read the logic stored in a selected memristor cell, a positive voltage (V_{read}) is applied across the cell (encircled in Fig. 1). Due to this voltage, the dopants will drift to the direction of the voltage, generating a current in the cell. This current is then compared with the I_{ref} by the sense amplifier; if it is more than I_{ref} the read logic will be ON state, otherwise it will be OFF state. However, if the neighbouring states are in ON state (i.e. low resistance), the current in the selected cell will accumulate the sneak path currents from these cells (Fig. 1). The accumulated current, known as sneak path current, reduces the noise margin significantly, causing the sense amplifier to sense ON state erroneously [10]. Clearly, high write voltage (Section II-A) and sneak path issue during read operations (Section II-B) are major limitations of single memristor based crossbar architectures [7]. To address these issues, we propose a novel Verilog-A based CRS model. To the best of the authors' knowledge, this is also the first such model, suitable and inter-operable in EDA tools.

III. Proposed Model

Fig. 2(a) shows our proposed CRS based crossbar architecture with two anti-serial (i.e. complementary) memristors, while Fig. 2(b) shows the memristor model on which it is based. The crossbar array architecture consists of vertical and horizontal conductive lines with a pinched hysteresis resistive material separating them, similar to [12]. Next, the memristor model is described, followed by details of the proposed Verilog-A based CRS model.

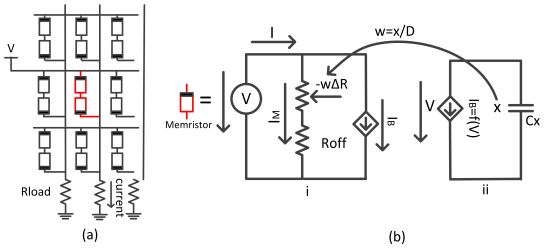

Fig. 2. (a) CRS based crossbar architecture; (b) memristor model for (a)

A. Memristor Model

To facilitate the calculation of memristance and its state variable, a memristor model can be analyzed in two behavioral parts as shown in Fig. 2(b). Part i is the main circuit for calculating the memristance of the system. It consists of a voltage source, a resistor (R_{off}) and a state variable x controlled resistor. Part ii is the state variable calculation circuit, consisting of a capacitor (C_x) and a voltage controlled current source (I_B). As can be seen, these two parts contribute two major currents: I_B from the voltage source is used for state variable calculation (part ii) and I_M which flows through the resistor of the memristor (part i). The total current of a memristor is $I = I_M + I_B \approx I_M$, since $I_M \gg I_B$ [12]. Note that the resistor of a memristor in part i can be modeled as a serial resistor R_{off} minus a state valuable x controlled resistor $\triangle R$. Hence, the supply voltage ($V(t)$) can be expressed as

$$V(t) = R(x) \times I(t) = (R_{off} - w \triangle R) \times I_M, \quad (1)$$

where $w = x/D$ is the ratio of state variable (x) derived from the state variable calculation in part ii (Fig. 2) and dope length of the memristor (D). The state variable x in (1) can be calculated from part ii as a charged voltage across C_x as

$$x = \frac{1}{C_x} \int_0^t I_B dt. \quad (2)$$

In (2), C_x can be defined in terms of dope length (D) of the memristor and the dopant mobility (μ_ν) as [5]

$$C_x = \frac{D}{R_{on}\mu_\nu}. \quad (3)$$

Replacing C_x value in (3), the state variable (x, defined in (2)) derivative can be expressed as

$$\frac{dx}{dt} = \mu_\nu \frac{R_{on}}{D} I_B. \quad (4)$$

In (4), the state transitions can be defined with different charge current (I_B). Since I_B is evaluated as a voltage dependent current, it can be expressed by Butler-Volmer equation [12] as

$$I_B = k \sinh[\alpha V(t)] \quad (5)$$

The Butler-Volmer equation in (5) gives a I-V characteristic for a certain class of memristors with symmetrical highly non-linear current-voltage characteristics with variable programming thresholds. The k and α in (5) are state-dependent constants used to characterize the state of the memristor. Fig. 3 shows I-V characteristics of the memristor model defined by (1) (in black lines). From the I-V characteristics, it can be seen that the current ($I(t)$) increases linearly between the approximately symmetric threshold voltages. However, as $V(t)$ is reduced below a threshold (V_{clear}), $I(t)$ drops sharply since the memristance decreases from R_{on} to R_{off}. At this point, any negative voltage change will retain the memristance at R_{off}. On the other hand, when $V(t)$ increases from a positive threshold (otherwise known as set voltage, V_{set}) $I(t)$

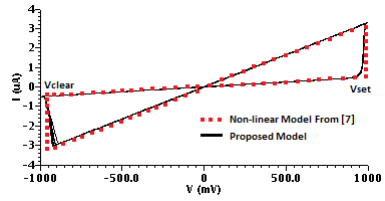

Fig. 3. I-V characteristics of a memristor

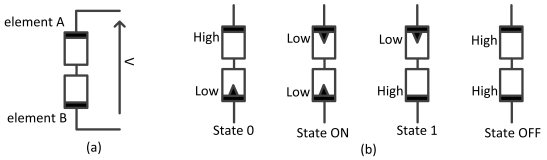

Fig. 4. (a) A CRS cell, and (b) four states of CRS

increases sharply as the memristance increases from R_{off} to R_{on}. Any positive voltage in this state will again retain its memristance at R_{on}. To further validate our proposed model, given I-V characteristics are compared with those in the non-linear model proposed in [7] (shown in red dotted line). As can be seen, both models have similar I-V characteristics with a statistical closeness of approximation defined by r^2 value of 0.989 ($r^2 \geq 0.95$ usually gives an acceptable hypothesis).

B. CRS Model

To solve the issue of sneak path currents (Section II-B), we propose a crossbar array architecture with two memristors in each cell with opposite polarities organized as complementary resistive switches, as also shown in [10], [11]. Moreover, to address the high write voltage problem (discussed in Section II-A), our CRS model uses the memristor model with voltage based state control (Section III-A). Fig. 4(a)-shows an example cell in the our proposed CRS model, while Fig. 4(b) shows the four possible CRS states. As can be seen, two memristors elements (A and B) are connected in complementary fashion. With such arrangements, state 1 for the cell is defined by element A being in low resistance state and element B being in high resistance state or vice versa. When both elements are in low resistor state or high resistor state, CRS is defined as state ON or state OFF, respectively. Usually, for CRS application, state OFF is not used for cells. However, if a CRS cell is in OFF state, a voltage larger than $2V_{th_1}$ or smaller than $2V_{th_3}$ can be applied to cause the cell to change to state 0 or 1, as shown in the I-V characteristics of a CRS cell in Fig. 5 (black lines). The I-V characteristics are obtained through simulations in Cadence Virtuoso applying a sinusoid voltage to the CRS cell. From Fig. 5, other state transitions among states 1, 0 and ON can can also be explained. For example, with given initial CRS state of 0 (i.e. element A in R_{off}), an applied voltage between V_{th1} and V_{th_2} can cause the CRS state to change to ON state. In this state CRS will have the low resistance

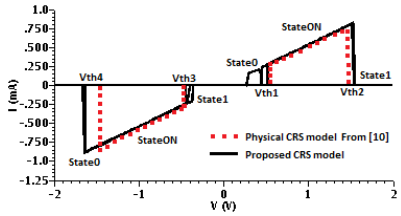

Fig. 5. I-V Characteristics of a CRS

(approx. $2R_{on}$), effectively causing a high current. However, when the applied voltage is larger than V_{th_2}, the CRS will change to state 1, causing the total resistance to be high again (approx. R_{off}), reducing the cell current. With negative applied voltages, CRS exhibits similar transitions from state 1 to ON and then to 0 (when $>V_{th_4}$). Note that, the proposed CRS model exhibits high OFF resistances (R_{off}) for states 0 and 1 and low resistances ($2R_{on}$) only when CRS reaches state ON. This can drastically reduce the sneak path current in read operations. For example, when a selected CRS is in state 1, a negative voltage (V_{th3}) can be applied to change the state 1 to ON. During this state change, other CRS will retain their states (in states 1 or 0), resulting in high resistance in them [9], [10]. Similarly, if the selected CRS is in state 0, an applied voltage V_{th3} cannot turn it into ON state, making states 1 and 0 distinguishable with drastically reduced sneak path currents. With these states, the read currents for state 0 ($I_{readout_0}$) and 1 ($I_{readout_1}$) in a crossbar array with $n \times n$ CRS cells (i.e. n rows and n columns), are given by the following

$$I_{readout_0} = \frac{V_{read}}{(R_{on} + R_{off})} + \frac{V_{read} \times (n-1)^2}{(2n-1) \times (R_{on} + R_{off})} \quad (6)$$

$$I_{readout_1} = \frac{V_{read}}{(2 \times R_{on})} + \frac{V_{read} * (n-1)^2}{(2n-1) \times (R_{on} + R_{off})} \quad (7)$$

From (6) and (7), it can be seen that during state 0 the CRS resistance is $(R_{on} + R_{off})$, while during state 1 the resistance is $(2R_{on})$, both being biased with negative voltage V_{read}. For other CRS cells, the resistances are given by $(R_{on} + R_{off})$.

To further validate our CRS model, the I-V characteristics are compared with those in the physical CRS model [10] (shown in red dotted line). As can be seen, both models have the similar V_{th1}, V_{th2}, and V_{th3} (with a combined r^2=0.95). Note that there is an offset in V_{th4} by approx. 0.2V, caused mainly by lower current given by (5). This offset, however, does not affect the overall non-linear state transition behavior.

C. Verilog-A CRS Model

With the above CRS model, a Verilog-A model is developed as shown in Fig. 6 to facilitate simulation and integrability with design automation tools. For demonstration purposes, only important descriptions are shown. As can be seen, the step and windows functions are defined initially (line 2 and lines 4-5), while the main CRS model is defined in lines 4-15. The CRS model consists of two anti-serial memristors, as expected, named as *xA_pos* and *xB_pos*. The state variable derivative, similar to (4),is defined in lines 6-7, while their actual states are evaluated in line 8 following (2). These state variables are then quantized (line 9) and the resulting currents (I_B) and resistance values (R_A and R_B for *xA_pos* and *xB_pos* elements) are estimated (lines 10-12). Finally, the element states are updated as shown in lines 14-15 (Fig. 6). Due to memristor based CRS modelling in Verilog-A (as shown in Fig. 6) there is no convergence issue for small to medium scale CRS arrays. However, for larger array sizes (i.e. of 64×64 or above) there are minor convergence issues, which can be resolved efficiently by splitting into small arrays.

```
1:  module CRS(p, n, xA_pos, xB_pos);
2:  //in: p, out: n, xA_pos, xB_pos; define step function;
3:  analog begin
4:  f_windowA = 1-pow(xA/D-stp(-IbA), 2*p_coeff);
5:  f_windowB = 1-pow(xB/D-stp(-IbB), 2*p_coeff);
6: dxdtA=uv*Ron/D*IbA*f_windowA;
7: dxdtB=uv*Ron/D*IbB*f_windowB;
8: xA=idt(dxdtA, xoA); xB=idt(dxdtB, xoB);
9: ... //quantize xA and xB to [D, 0]
10: IbA= k*sinh(alpha*VA); IbB= k*sinh(alpha*VB);
11: RA=(xA/D*Ron+(1-xA/D)*Roff);
12: RB=(xB/D*Ron+(1-xB/D)*Roff);
13: VA=I(p,n)*RA; VB=-I(p,n)*RB;
14: I(p,n) <+  V(p,n)/(RA+RB);
15: Metr(xA_pos) <+ xA; Metr(xB_pos) <+ xB;
16: end
17: endmodule
```

Fig. 6. Verilog-A description for proposed CRS model (Section III-B)

IV. Sneak Path Analysis

To evaluate the effectiveness of our proposed Verilog-A based CRS model (Section III), a number of experiments are carried out showing sneak path currents for a crossbar array architecture implemented using our proposed CRS model. To measure these currents we apply read voltage for the selected row and measure the read current in the selected column, keeping other cells floating. Cadence Virtuoso is used to simulate the CRS model assuming a load resistance (R_{load}) of 100Ω, OFF resistance (R_{off}) of $310k\Omega$ and ON resistance (R_{on}) of 460Ω, as also used in [11]. The resulting currents are measured and compared using two different read currents: read currents when the cell is in OFF state ($I_{read_{off}}$) and ON state ($I_{read_{on}}$). The sneak path current during OFF and ON states ($\Delta I_{read_{off}}$ and $\Delta I_{read_{on}}$) can be calculated as the differences between currents in the best case and the worst case [8]

$$\Delta I_{read_{off}} = I^{wc}_{read_{off}} - I^{bc}_{read_{off}}. \quad (8)$$

$$\Delta I_{read_{on}} = I^{wc}_{read_{on}} - I^{bc}_{read_{on}}. \quad (9)$$

Table I shows the comparative $\Delta I_{read_{off}}$ and $\Delta I_{read_{on}}$ values for single memristor and CRS based crossbar arrays. Column 1 shows the increasing crossbar array sizes, columns 2-3 show the comparative $\Delta I_{read_{off}}$ values, while columns 4-5 show the comparative $\Delta I_{read_{on}}$ values estimated in the crossbar architectures (Fig. 1 and Fig. 2(a)). As can be seen, as the array size increases, $\Delta I_{read_{off}}$ in single memristor based crossbar array increases significantly (approximately 3 times from size (4×4) to (16×16) in column 2, Table I). However, in the case of proposed CRS model (Section III) based crossbar array, $\Delta I_{read_{off}}$ is significantly lower, which remains approximately similar for different array sizes (column 3, Table I). Similar observations can be made for $\Delta I_{read_{on}}$ for the two different crossbar array architectures. For single memristor based crossbar array, the read current is highly depended on the content of the crossbar cell. However, for CRS based crossbar array, the read current is independent of the content.

TABLE I

Comparison of sneak path currents and noise margin

Array Size	$\Delta I_{read_{off}}$		$\Delta I_{read_{on}}$		$\Delta I/\Delta I_{read}$	
	Memristor	CRS	Memristor	CRS	Memristor	CRS
4X4	2.18E-03	1.00E-09	1.53E-03	1.00E-09	0.7986	0.9994
5X5	2.78E-03	1.00E-09	1.98E-03	1.00E-09	0.5476	1
6X6	3.30E-03	1.00E-09	2.37E-03	1.00E-09	0.4778	0.9986
7X7	3.75E-03	1.00E-09	2.71E-03	1.00E-09	0.4157	0.99833
8X8	4.14E-03	1.00E-09	3.02E-03	1.00E-09	0.3703	0.998024
9X9	4.48E-03	1.00E-09	3.30E-03	1.00E-09	0.3310	0.9977
10X10	4.79E-03	1.00E-09	3.55E-03	1.00E-09	0.2973	0.9974
11X11	5.07E-03	1.00E-09	3.76E-03	1.00E-09	0.2637	0.9971
12X12	5.32E-03	1.00E-09	3.96E-03	1.00E-09	0.2356	0.9968
13X13	5.54E-03	1.00E-09	4.15E-03	1.00E-09	0.2188	0.9965
14X14	5.74E-03	1.00E-09	4.32E-03	1.00E-09	0.2076	0.99623
15X15	5.92E-03	1.00E-09	4.48E-03	1.00E-09	0.1851	0.9959
16X16	6.09E-03	1.00E-09	4.62E-03	1.00E-09	0.1683	0.9958

The sneak path current measurements were also carried out using the CRS model proposed in [10] for comparative evaluations (not shown due to space constraints). Our proposed Verilog-A based CRS model showed up to 10% variations in the sneak path current measurements when compared with the current measurements obtained from CRS model in [10].

To further evaluate the impact of sneak path in terms of current noise margin, the ratios of sensing current margins and read currents (i.e. $\Delta I/\Delta I_{read}$) are estimated for a CRS cell. ΔI is the difference between $I^{wc}_{read_{on}}$ and $I^{wc}_{read_{off}}$, while ΔI_{read} is the difference current between $I_{read_{on}}$ and $I_{read_{off}}$ when crossbar array size is 1. Table I shows the $\Delta I/\Delta I_{read}$ of single memristor arrays compared with that of crossbar arrays implemented with proposed CRS model for different array sizes (columns 6-7). As can be seen, $\Delta I/\Delta I_{read}$ for single memristor based crossbar arrays decrease from 0.8 to 0.16. Such low values make states 0 and 1 indistinguishable as $\Delta I/\Delta I_{read}\approx0.1$ due to high sneak path currents. However, in our proposed CRS model based crossbar array, $\Delta I/\Delta I_{read}$ is approximately 1, giving significantly higher noise margin between the states and reduced sneak path currents.

V. Conclusions

A Verilog-A based complementary resistive switch (CRS) model is proposed. Extensive simulations and analyses have been carried out in EDA tools to demonstrate the effectiveness of this model. We showed that with explicit voltage based state control our model exhibited desired non-linear behavior with symmetrical ON/OFF voltages. Moreover, due to high noise margin sneak path current was drastically reduced. Ongoing research includes process variation-aware CRS model.

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