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NANO RESEARCH GROUP

Top-Down Fabrication and Characterization of Zinc Oxide Nanowire Field Effect Transistors

by

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Thesis for the degree of Doctor of Philosophy

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ABSTRACT

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TOP-DOWN FABRICATION AND CHARACTERIZATION OF ZINC OXIDE NANOWIRE FIELD EFFECT TRANSISTORS

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Top-down fabrication is used to produce ZnO nanowires by remote plasma enhanced atomic layer deposition (PEALD) over a SiO_2 pillar and anisotropic dry etching. Nanowire field effect transistors (FETs), with channel lengths in the range 18.6 to 1.3 μm, are produced in well-defined locations on a 150 mm diameter silicon wafer. The control of nanowire FET dimensions and locations is seen as the key to wafer-scale nanowire integrated circuit production. Measured electrical results show n-type enhancement behaviour and a breakdown voltage $\geq$ 75 V at all channel lengths. This is the first report of high voltage operation for ZnO nanowire FETs. Reproducible, well-behaved electrical characteristics are obtained and the drain current scales with 1/L, as expected for long-channel FETs.

This thesis reports for the first time that semiconducting quality of ZnO thin film can be achieved using remote PEALD at a minimum temperature of 100^{o}C. Remote PEALD technique offers flexible approach in controlling defects and impurities on the film even at low temperatures which remains a challenge in thermal ALD. Dry etch and remote PEALD processes have been optimised to produce high performance nanowire FET and semiconducting ZnO film. It is demonstrated that using the same CHF_3 chemistry, ICP etched nanowires have field-effect mobility six times higher than RIE etched device. The surface roughness from RIE is shown to degrade nanowire FET electrical performance. Experimental results from remote PEALD optimisation show a stoichiometric balanced ZnO film when deposited at substrate temperature of 190^{o}C, zinc precursor dose time of 1s and oxygen plasma time of 4s. Optimized ICP etched nanowire FET with 20 nm width and 10 μm long channel show a high field effect mobility of f 10 cm^2/Vs. The electrical results from the pristine state of the nanowires without any post deposition treatments such as passivation demonstrates the feasibility for high performance top-down fabricated NWFETs in line with other unpassivated bottom-up fabricated devices.

The effect of atmospheric oxygen adsorption on nanowire surface has been investigated by measuring FET characteristics particularly the threshold voltage shift and hysteresis under different environments and at different gate bias sweep rates. These top-down unpassivated NWFETs are shown to be electrically reproducible when measured in ambient air even after 3 months of fabrication. The device is shown to be electrically air stable with a shift of threshold voltage of less than 11% for unpassivated and only 2% for passivated after 30-days of fabrication. In addition, passivation improves the field effect mobility by a maximum of 4-fold. Unpassivated device measured in vacuum showed a mobility improvement by 1.8 fold. These results show the electronic transport properties of the top-down fabricated nanowires can be influenced by the surface environments. In addition, hysteresis characteristics on top-down fabricated ZnO nanowire devices have been reported for the first time. Hysteresis measurement is sensitive to gate bias sweep rate. The maximum hysteresis obtained for this top-down ZnO NWFET device is 2.2 V, 0.8 V and 1.6 V when measured in ambient air, vacuum and after passivation, respectively. The hysteresis obtained for the unpassivated top-down fabricated ZnO NWFET in this work is smaller compared to other bottom up devices due to better interface quality of remote PEALD ZnO with SiO_2 gate dielectric.

From this top-down technology, 100 parallel nanowires with channel length of 20 μm are successfully fabricated for biosensing experiments. These devices consistently show n-type enhancement mode characteristics in different solutions. The BSA molecules with negative charges in buffer solution are successfully detected by the channel conductance modulation where the drain current reduced by 12 times. Meanwhile, Lysozyme molecules with positive charges in buffer solution are also successfully detected with an increase of drain current by 21 times. This top-down fabrication approach with low temperature film deposition is promising technology for future low-cost mass manufacturable sensors for health care and biomedical research.

Contents

DECLARATION OF AUTHORSHIP

I, Suhana Mohamed Sultan, declare that the thesis entitled:

" Top-Down Fabrication and Characterization of Zinc Oxide (ZnO) Nanowire Field Effect Transistors"

and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published in research journals. A list of publications is provided with this manuscript.

Signed: ……..

Date:…….

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List of Publications

Conference Presentations

1. Fabrication of ZnO nanowire device using top-down approach.

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3. The Fabrication and Characterization of ZnO Thin Films using Remote Plasma ALD at various temperatures.

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5. Top-down fabricated ZnO nanowire Transistors for application in biosensors.

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Journals

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Chapter 1

Introduction

The semiconductor industry is now faced with the increasing importance of a new trend, “More than Moore” (MtM) where added value to devices is provided by incorporating functionalities that do not necessarily scale according to “Moore’s Law”. This trend has been recognized by the International Technology Roadmap for Semiconductors (ITRS) and has included new dimensions to be considered since their 2009 technology roadmap[1]. These new technologies involve many functional requirements such as biological functions, display electronics, sensors and actuators which do not scale with Moore’s Law but provide additional value to the end customer in different ways. This trend is represented graphically in the 2009 ITRS roadmap shown in Fig.1.1

In order to fulfil the current trend of technology, there is overwhelming research on new materials and new structures since the beginning of this decade. This is due to the various newfound physical properties obtained in new materials such as carbon nanotubes, graphene and wide band gap semiconductors which are useful in applications such as high power, transparent display technology and optoelectronics.

Zinc Oxide (ZnO) is a II-VI compound semiconductor, which crystallizes in the wurtzite phase and has a direct bandgap of 3.4 eV [2]. It has also large free-exciton binding energy of 60 meV which is significantly higher than that of ZnSe (22 meV) and GaN (25 meV). ZnO exhibits inherent properties such as larger bandgap, higher electron mobility, higher breakdown field strength, transparent to visible light and it is intrinsically n-type semiconductor. It is one of the semiconductor materials that is known for its versatile applications and thus many review articles have been written on ZnO interesting properties since the beginning of this decade [2-10].

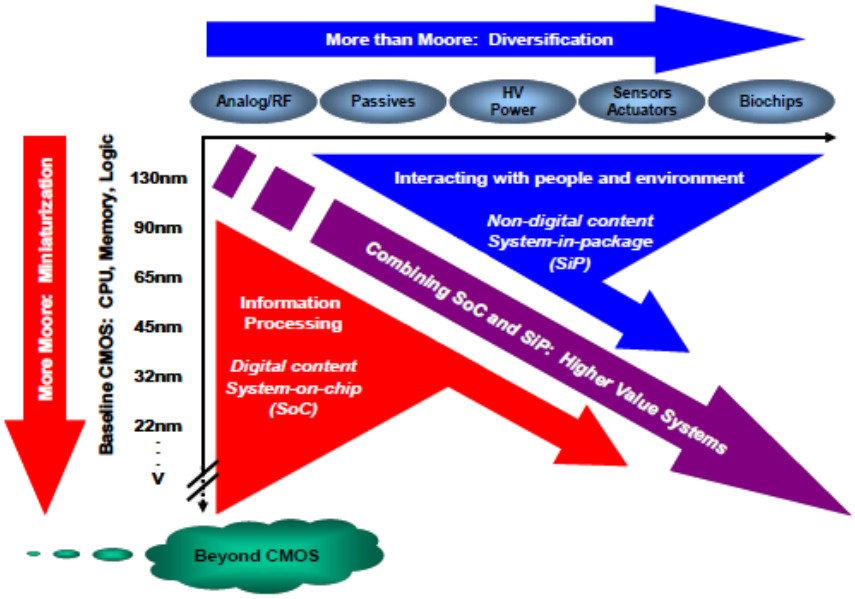

Fig.1.1 Moore's Law and More [1]

ZnO-based thin film transistors are receiving increasing attention because high values of mobility (>10 cm^2/Vs) can routinely be achieved in layers deposited at low temperature (<200ºC) [11-15]. The values of mobility achievable are significantly higher than those in more well researched materials such as α-Si:H (~1 cm^2/Vs), pentacene single crystals (~2.7 cm^2/Vs) and pentacene thin films (~1.5 cm^2/Vs) [15]. This makes ZnO-based thin film transistors very attractive for application in displays, where the higher mobility would provide higher switching speeds or lower power operation. For display applications ZnO has the additional advantage of high optical transparency, whereas α-Si: H does not. Other favourable aspects of ZnO include its broad chemistry leading to many opportunities for wet chemical etching, radiation hardness and biocompatibility. Together, these properties of ZnO make it an ideal candidate for a variety of devices ranging from sensors, UV laser diodes and nanotechnology based devices such as displays.

One distinct feature of ZnO material is the possibility to deposit the film at low temperatures compared to other thin film materials. A variety of approaches have been used for the low temperature deposition of ZnO-based materials, including sputtering [14-16], pulsed laser deposition[17], solution-based processes [18] and atomic layer deposition (ALD) [11-13],[19-21]. Among these methods, ALD is particularly attractive because it offers the prospect of good control of material structure in a manufacturing environment. ALD ZnO layers with reasonable electrical and optical properties can be obtained at deposition temperatures below 100ºC [22] and even down to room temperature [23]. This opens huge opportunities towards applications on inexpensive substrates such as glass, plastic, paper and textiles.

Recently there has been increasing interest in ZnO-based nanowire transistors. The most common method used to fabricate the ZnO nanowires are through bottom-up processing. Bottom-up method of fabrication such as chemical synthesis i.e. vapour-liquid-solid or vapour-solid, proves to be a more flexible approach to produce high quality nanowires and excellent mobility values [24-26]. The main drawback of this method is that after the growth, nanowires will be scattered on the substrate and it is necessary to employ a good pick-and-place method to place the grown nanowire on the device substrate. Moreover, too many variables such as difference in sizes of the grown nanowires and issues on the alignment prove to realize nanowire FET structure a difficult task. In addition, the output characteristics of these devices show poor saturation and operation up to voltages of only a few volts.

Meanwhile, the top-down method using e-beam and focused-ion-beam lithography has also made a great impact to investigate the basic properties of the nanowire devices but their use on a large scale is a challenge due to high cost. Recently, ZnO based nanowire transistors were fabricated by a top-down approach [27] for sensor applications but the output characteristics only showed low voltage operation up to about 2V. For successful circuit design in applications such as displays, much higher operating voltages are required [28] [29] and it is also necessary to be able to design transistors with different channel lengths.

Another critical issue for the emerging research material especially metal oxide, is the ability to characterize and control the interface properties. As features approach the nanometer scale, fundamental stability considerations may limit the ability to fabricate nanomaterials with tight dimensional distributions and controlled useful material properties. W.K.Hong *et al* [30] and P.J.Jeon *et al* [31] have shown large hysteresis in their as-grown bottom-gate ZnO nanowire FETs (> 5V) and reduced after passivation and annealing, respectively. This indicates the interface quality between gate dielectric/ZnO nanowire and ZnO nanowire/air interface is questionable. It is also known that ZnO material under oxygen exposure showed a gradual decrease of the conductivity due to oxygen adsorption on the nanowire surface and a subsequent elimination of the oxygen vacancies (as the source of intrinsic charge carriers)[32]. This suggests a post treatment procedure after NWFET fabrication is necessary to improve the material stability.

Furthermore, ZnO nanostructures have been shown to be bio-safe and biocompatible which makes them attractive for applications as biosensors. The fundamental sensing mechanism of ZnO material relies on a change in electrical conductivity due to the interaction process between the surface species such as O^-,O_2^-,H^+ and OH^- and the molecules to be detected [33]. A recent review on ZnO nanowires for biosensor applications has also shown the feasibility and higher sensitivity towards low level bioanalytes due to its high surface-to-volume

ratio [34]. This opens unexplored possibilities to novel biosensor platforms. In spite of the huge expectations, unfortunately, only a limited number of studies have described the detection of biomaterials using ZnO FET devices. Recently, Reyes *et al* [34] and A.Choi *et al* [35] demonstrated ZnO FET based biosensors for the detection of low level biomolecular interactions. ZnO NWFET biosensors based on bottom-up technique generally involve a complex fabrication process by manipulating and aligning a single strand of semiconducting nanowire as the FET channel between the source and drain patterns. Therefore, it is difficult to achieve repeatability and manufacturability in fabrication and integration of these devices for large sensor arrays. Thus, the development of a very low cost and simple fabrication route suitable for mass manufacture for nanowire sensors would accelerate their uptake as point-of-care (POC) devices.

In summary, most of the research achievements on ZnO NWFETs are still based at the random trial stage. The current challenge is to produce ZnO nanowires in defined locations and controlled dimensions with well-behaved electrical characteristics in the ambient environment. In addition, the stability of the electrical characteristics of these nanowire devices in ambient air and in liquid environment remains a challenge especially in biosensor applications. Therefore, the primary goal of this PhD project is to address these challenges using simple and low cost top-down ZnO NWFET devices.

The structure of this thesis is organized as follows. Chapter 2 gives an extensive literature review of research done on ZnO thin film deposition techniques and performance evaluations on various ZnO nanowire FETs based on bottom-up and top-down techniques. Then, Chapter 3 introduces conduction models of nanowire FET at different operating regions based on TFT operation. In addition, this chapter explains the capacitance model used for the fabricated NWFET. In chapter 4, the main aim is to demonstrate the feasibility of remote plasma enhanced Atomic Layer Deposition (PEALD) to deposit ZnO thin film with semiconducting properties which subsequently used to fabricate ZnO NWFET using top-down technique. In chapter 5, the PEALD deposition and dry etch techniques were optimized to produce high mobility ZnO NWFET. In chapter 6, results are presented on the reproducibility and hysteresis behaviour of these top-down fabricated transistors in ambient air, passivation and vacuum environment. Chapter 7 explores the possibilities of fabricated nanowires to detect different charged proteins. In addition, the stability of the electrical characteristics in liquid environment was also demonstrated. Conclusions and Future Work are given in Chapter 8.

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Chapter 2

Literature Review

This chapter highlights the background details of various ZnO film depositions, material growth and their respective electrical properties. ZnO material deposition and growth is the foundation for nanowire device fabrication regardless of the techniques used ; bottom-up or top-down. The aim is to realize the best technique to fabricate ZnO nanowire field-effect transistors (FETs) with excellent electrical characteristics at relatively low temperatures. To date, most of fabricated ZnO nanowire devices are based on bottom-up approaches and various post-fabrication techniques need to be employed to improve their electrical performance. These effects of various post fabrication treatments are discussed too. Based on these findings, this chapter provides an outline of the aims of this work and the motivation is discussed.

2.1 ZnO Film Deposition

ZnO is one of the few semiconductor materials that can be grown at low temperatures. In pursuit of this, various deposition techniques were reported to achieve high crystalline and semiconducting quality ZnO films at reasonable temperatures (< 200^{o}C). Some of these are tabulated in Table 2.1. From Table 2.1, it is observed that pulsed laser deposition (PLD), metal oxide chemical vapour deposition (MOCVD), and metal oxide vapour phase epitaxy (MOVPE) depositions normally require high temperature. Even though room temperature deposition of ZnO film was reported previously [1][2], it often requires post-deposition annealing at higher temperatures due to the lack of control of impurities.

The tabulated results also indicate that the method of ZnO film deposition can significantly affect the electrical characteristics of the film. The maximum Hall mobility reported so far is ranged from 100 to 155 cm^2/Vs [3]. The mobility values are much lower than that of single crystal of 200 cm^2/Vs [11].

TABLE 2.1 Survey of various ZnO thin film deposition techniques

Sample	Growth Temperature (^oC)	Carrier Conc. (cm^{-3})	Hall Mobility (cm^2/Vs)	Ref
PLD: ZnO thin film on sapphire substrates.	750	(2~5) $x10^{16}$	115~155	E.M.Kaidashev *et al* [3]
MBE: ZnO thin film on MgO buffered sapphire substrates	700	1.2 x 10^{17}	130	H.Kato *et al*[4]
MOCVD: ZnO thin film grown on sapphire	600	4 x 10^{17}	24	X. Wang *et al*[5]
SPUTTER: ZnO thin film on glass	Room Temperature	3 x 10^{16}	2.0	E.M.C. Fortunato *et al* [6]
ALD: ZnO thin film grown on SiO_2/Si	70~130	10^{14}~10^{19}	6.4 ~ 152	S.Kwon *et al* [7]
Thermal ALD (TH) and PEALD (PE) ZnO thin film	TH:100~250 PE:225~300	2 x 10^{17}~ 2 x 10^{19} 1 x 10^{15}~ 2 x 10^{20}	1 ~ 8 1 ~ 5	D. Kim *et al*[8]
ALD: ZnO thin film grown on SiO_2/Si substrate	70~250	10^{13} ~10^{20}	0.43 ~ 22	B.-Y.Oh *et al* [9]
ALD: ZnO thin film grown on SiO_2/Si substrate	150~400	8 x 10^{19} ~ 4 x 10^{20}	19 ~ 8	Y.S.Min *et al*[10]

The Table 2.1shows that the electron carrier concentration can vary from 10^{16} to 10^{20} cm^{-3}. Basically the electron carrier concentration increases as the growth temperature increases. Comparing the carrier concentration of the bulk crystal with an order of 10^{13} cm^{-3}[11], the cause of high carrier concentrations in ZnO material has been widely debated despite years of investigation. The n-type behaviour in this material has traditionally been attributed to native defects [12][13] such as zinc interstitials (Zn_i) and oxygen vacancies (V_o). However, most of these arguments are based on hypotheses that are not supported by experimental observations. In fact, recent first-principles calculations indicate that oxygen vacancy is actually a deep donor and zinc interstitials are shallow donors but have high formation energies [14]. In addition, it was found theoretically that hydrogen impurities which act as shallow donor observed to increase the n-type conductivity [14]. This hypotheses supported further by number of experiments which show an increase of conductivity upon exposure to H_2 during the growth environment [15][16]. Thus one approach to address the unintentional n-type conductivity due

to hydrogen impurities and native defects in ZnO film is to grow or deposit a high quality thin films in which the concentrations of impurities and defects are well controlled. The electron mobility generally decreases with increasing carrier concentration because impurity scattering increases in proportion to carrier concentration.

Based on the results tabulated, ALD is a particularly attractive technique because ZnO films can be deposited at temperatures below 100^{o}C [7][9]. In addition, the carrier concentrations and Hall mobilities obtained from ALD can be modulated with deposition temperatures to obtain semiconducting properties without the need of post- deposition treatments. Moreover, ALD offers several advantages over the other techniques such as large area uniformity and good growth control of the thickness and composition of the thin films.

2.2 ZnO Thin Film Transistor (TFT)

The ALD deposition technique is capable of producing high quality semiconducting ZnO material and subsequently good TFT devices. Since ALD facilitates low temperature film growth, ZnO thin films have found interest in transparent thin film transistors (TFT) for switching and flexible display applications. This section reviews the electrical performance of TFTs fabricated using the ALD process including thermal based and plasma enhanced ALD. Based on the TFT technology fabricated in ALD, this work provided the inspiration to move for the nanowire based devices which are discussed in Section 2.3.

Table 2.2 lists the various electrical characteristics of TFT achieved in other work. From this table, it is observed that with modest deposition temperature (≤ 250^{o}C), the threshold voltage achieved ranged from -16.5 V to 14.7 V. In addition, the maximum field-effect mobility achieved is 30 cm^{2}/Vs [12] and a minimum subthreshold swing of 0.2 V/dec is obtained [17] [18] from the ALD process.

Based on these findings, thermal based ALD which uses water vapour as the oxygen source can easily produce highly conductive ZnO film at temperature > 120^{o}C from the work of Ref [7][19] resulting in good depletion mode TFTs. In order to reduce the carrier concentration, various approaches have been used; low deposition temperatures [1] [7] [9] [19], dopant incorporation [20] and post - deposition annealing in an oxygen environment [18][21]. Nevertheless it is desirable to have a process where high resistivity films can be formed without the use of compensation doping or post - deposition annealing.

TABLE 2.2 Review of electrical performance of ALD deposited ZnO TFT.

Ref	T [^{O}C]	V_{TH} [V]	Field-Effect Mobility [cm^2/Vs]	Subthreshold Swing [V/dec]	I_{ON}/I_{OFF}
D.Kim *et al* [8]	Thermal : 125	-16.54	0.25	2.2	10^7
	PEALD : 225	11.6	0.06	1.4	10^5
S.Kwon *et al* [7]	Thermal: 70	14.7	8.82×10^{-3}	4.19	3.6×10^4
	90	13.1	0.13	1.21	2.4×10^6
	110	-12.5	0.57	24.1	11
	130	Conductive Film			
Y.Kawamura *et al* [18]	PEALD: 100		0.3		
	Post anneal in O_2 at 350	-2.1	2.1	0.22	5×10^9
N.Huby *et al* [19]	Thermal:100	1.6	1	2	10^7
	130	Conductive film			
D.M. Mourey *et al* [17]	PEALD: 200	4.5	20~30	0.2	10^8
S.H.K.Park *et al* [23]	PEALD:200	7~8	3.9~4.3	N/A	10^7

From Table 2.2, it is also shown that the subthreshold swing which indicates the interface quality between the ZnO semiconductor layer and gate dielectric interface, is poor (> 1 V/dec) for TFTs fabricated by thermal ALD especially films deposited at low temperatures. S. Jeon *et al* showed that as deposition temperature decreased in thermal based ALD, an increase in O-H bonds in the ZnO film creates defects which results in deterioration of the interface quality, which in turn decreases carrier concentration by suppressing the formation of oxygen vacancies thus reducing the carrier mobility [22].

It is also shown in Table 2.2, that plasma-enhanced ALD (PEALD) deposited ZnO films generally exhibit enhancement mode transistor action with positive threshold voltage. The highest mobility achieved is 20 to 30 cm^2/Vs [17]. PEALD provides many of the advantages of other ALD processes but with the additional ability to control defects at low temperature deposition. The use of plasma significantly reduces the incorporation of –OH groups, which are related to conduction in ZnO [17].

2.3 Fabrication of ZnO Nanowire FET (NW-FET)

Compared to TFT devices, ZnO nanostructures are more interesting because they exhibit the most diverse and abundant configurations known so far, such as nanowires, nanobelts, nanosprings, nanorings, nanobows and nanohelices [24]. Devices made from nanowires have been demonstrated to show superior performance than their thin-film counterparts or even exhibit novel properties that have never been achieved by thin film technology. Although numerous studies have demonstrated novel nanodevices and applications based on ZnO nanowires, most of these work has been done based on bottom-up fabrication approach. This section will briefly discuss the bottom-up and top-down fabrication methods. Subsequently, the electrical properties of the FETs fabricated by both methods will be compared and discussed.

2.3.1 Bottom-up Process

Among the various methods in the bottom up fabrication technique, chemical vapour deposition (CVD) and hydrothermal techniques are the most popular strategies. The growth of ZnO nanowires by the CVD technology is usually described as the vapour-liquid-solid (VLS) or vapour-solid (VS) mechanism. For ZnO nanowires grown by the VLS process, the commonly used catalyst is Au. The size of the catalyst defines the diameter of the nanowires [25][26]. The catalysts initiate and guide the nanowire growth in which the epitaxial orientation relationship between the nanowire and the substrate results in the aligned growth of nanowires normal to the substrate as shown in Fig.2.1 (a). These nanowires have a smooth and uniform cross section with a controllable space distribution depending on the initial catalysts location on the growth substrate.

In vapour-solid process (VS), no catalyst is required resulting in higher purity of the ZnO because there will be no impurities due to the catalysts. However, a higher temperature (>900^{o}C) is usually required to overcome the much higher activation energy compared with the VLS method. Unlike catalysts-directed growth, it is usually hard to effectively control the size and morphology of the nanowires during the VS growth [27].

Recently, the hydrothermal approach is gaining interest for ZnO nanowire growth in which low temperature solutions are used for the synthesis [27] [28]. Fig.2.1 (b) shows a large density of ZnO nanowires after the hydrothermal growth, many of them several tens of micrometers long, with diameters between 20 and 200 nm. The transmission electron microscopy (TEM) analysis in Fig.2.1(c) confirms the single-crystalline structure of the ZnO nanowire.

Subsequently after the nanowire growth from various methods for the fabrication of NWFET, the as-grown ZnO nanowires are usually suspended in ethanol solution and dispersed onto a device substrate. Then, the source and drain electrodes are defined with photolithography or e-beam lithography and deposited by thermal evaporation. Fig.2.1 (d) shows the atomic force microscopy image after source and drain electrode deposition to a single nanowire from the work of D.Kalblein *et al* [28].

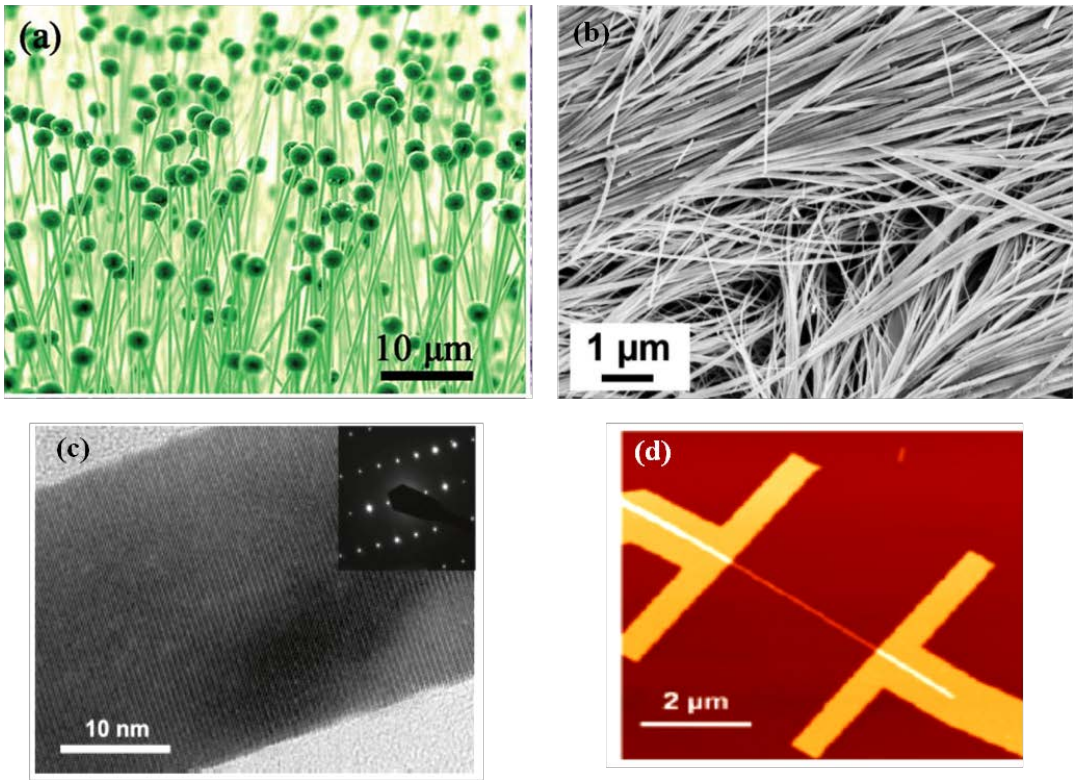


Fig. 2.1 (a) Scanning electron microscopy image of ZnO nanowires synthesized in VLS method [27] (b) Scanning electron microscopy of a dense carpet of ZnO nanowires after the hydrothermal growth [28] (c) Transmission electron microscopy image of one of the ZnO nanowire grown in hydrothermal. The inset confirms the single crystalline structure of the ZnO nanowires [28].(d) Atomic force microscopy image of an as-grown nanowire with Al source and drain contacts [28] *Reprinted with permission from Ref[28]. Copyright 2013 American Chemical Society*

Although bottom-up fabricated ZnO nanowires exhibit high crystallinity, morphology and large aspect ratio, this technique poses drawbacks which limit the production of nanowire based devices on a large scale at low cost. These drawbacks are listed below;

1. The nanowires are randomly aligned on the device substrate which limits the control over nanowire locations. Although various methods of aligning nanowires are studied such as using an electric field [29], microfluidic flow-assisted techniques [30] and

Langmuir-Blodgett method [31], these methods suffer from contamination and incompatibility with silicon processing.

2. Lack of controlled synthesis to produce controlled and uniform dimensions such as lengths of the nanowires for large-scale integration.

Therefore, bottom up technologies do not provide a viable route for addressable NWFETs due to the above disadvantages.

2.3.2 Top-Down Process

To date, there are not many top-down processes to produce ZnO NWFETs. A top-down approach is more common for Si NWFETs in which advanced lithography technologies, such as e-beam lithography or deep ultra-violet (DUV) lithography are used to pattern nanowires on SOI wafers. E-beam lithography, which uses direct pattern-writing with an electron beam, can define patterns with widths down to 10 nm. However, it has a slow writing speed, which makes it impractical for large-scale manufacturing. DUV lithography is also an expensive process because it requires advanced photoresists and light source. Hence new approaches to ZnO NWFET fabrication are required which are more cost effective and suitable for large scale manufacture.

Recently, Ra *et al* demonstrated the feasibility of top-down ZnO nanowire array fabrication using spacer lithography [32]. This technique consists of sacrificial oxide deposition, etching of the sacrificial oxide to form pillars, ZnO atomic layer deposition (ALD) on the sacrificial oxide layer, ICP etching of the ZnO film except the spacer part and finally removal of the sacrificial oxide. This approach is a good alternative to produce ZnO nanowires in defined locations with controlled nanowire dimensions. Fig. 2.2 shows the SEM image of the ZnO nanowire arrays that were successfully formed after the sacrificial oxide removal. The width and height of the ZnO nanowires are around 70 and 100 nm, respectively. One concern from this work is the removal process of the sacrificial oxide which might consequently induce surface roughness on or near the nanowire surface as shown in Fig.2.2 because ZnO can easily be etched in acids and alkalis [33]. The electrical characteristics of this device will be discussed in the next section and compared with other bottom-up techniques.

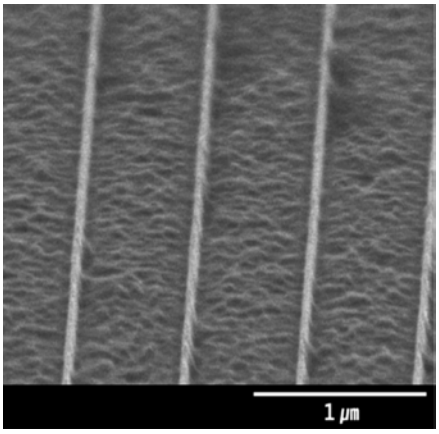


Fig.2.2 SEM image of ZnO nanowire array fabricated by top-down fabrication method [32]

2.4 Benchmarking the ZnO NWFETs

In this section, the performances of different ZnO NW-FET devices from the literature are compared based on the field effect mobility μ_{FE} and the threshold voltage, V_{TH}.
High mobility is desired for fast switching devices to enable fast signal processing while positive threshold voltage is always preferred for low power applications. In addition, low subthreshold slope, SS and high I_{ON}/I_{OFF} ratio are also favoured for high performance device applications. Table 2.3 shows the characteristics of some of the published NW-FET work.

Generally, in typical back-gate configurations in an atmosphere environment, reported values of field-effect mobility of *untreated* ZnO nanowire FETs show wide variation, with values ranging from 1 to 75 cm^2/Vs, with the threshold voltages ranging from -105 to 0.4 V and an on-off ratio about 10^4 to 10^7 as tabulated in Table 2.3. Most of these devices were fabricated using bottom-up approaches. Surprisingly, so far only one work [32] which had used the top down approach to fabricate NWFET based on ZnO semiconductor. This is an interesting fact that partly motivated the work in this thesis.

TABLE 2.3 Review of ZnO NWFET electrical performance

Ref	Method	Post-growth Treatment	μ_{FE} [cm^2/Vs]	V_{TH}[V]	SS[V/dec]	Ion/ Ioff
BOTTOM UP						
W.I.Park[34]	Bottom-up	as grown	75	-21	3.37	
2004		polyimide passivation	1000	-0.3	0.2	10^4-10^6
J.Goldberger[35]	Bottom-up	as grown	13	-12.5	N/A	10^5-10^7
2005						
(Continued)						

Ref	Method	Post-growth Treatment	μ_{FE} [cm^2/Vs]	V_{TH} [V]	SS[V/dec]	Ion/ Ioff
P.C.Chang[36]	Bottom up	as grown	30	-10	3	10^3
2006		SiO_2/Si_3N_4 passivation	3118	-18	0.15	10^4
S.N.Cha[37] 2006	Bottom-up (air as the insulator)	Top gate structure.	928	0.4	0.129	10^6
S.Ju [38]						
2007	Bottom-up organic (SAND) as gate insulator	as grown	70	-0.4	0.4	10^3
		annealed in air at 130°C		-0.25	0.23	10^5
		anneal+ozone	1175	0.2	0.13	10^7
K.Keem[39]	Bottom-up	as grown	27	conductor		
2007	SiO_2	H_2 anneal 350°C	302	-9.6	N/A	10^5
W.K.Hong[40]						
2008	Bottom-up	as grown-smooth	34	-4.16	<1	10^4
		PMMA passivation-smooth	68	-2.25	<0.5	10^6
		as grown-rough	28	-12.5	<1	10^5
		PMMA passivation-rough	48	8.9	<0.5	10^6
J.Maeng[41]	Bottom-up	as grown	16.6	11.3	0.68	10^4
2009		Excimer laser anneal	12.3	-0.7	1.17	10^4
Z.-M.Liao[42]	Bottom-up	as grown	36.7	-105	N/A	10^7
2011		Ga+ irradiation	34.5	-8.1	1	
D.Kalblein [28]	Bottom-up	as-grown	conductor			
2011		anneal 600°C in air	40	> 0	0.4	10^7
		top gate with organic gate dielectric	g_m increased x 5	> 0	0.09	10^7
T.Kwon [43]	Bottom-up	as-grown	81.3	-27	0.2	N/A
2012		H_2O_2 treatment for 5 s	34.1	-7.33	0.25	N/A
P.J.Jeon [44]	Bottom-up	as- grown	conductor			
2012	Al_2O_3 gate insulator	ambient anneal at 600°C 30 mins	6	-2	< 0.5	10^6
TOP-DOWN						
H.W.Ra[32]	Top-down	10 nw array	80	-7.5	0.7	10^5
2008						

Based on the results tabulated, most of the bottom-up fabricated nanowires must undergo various treatments such as passivation and annealing to achieve the desired electrical characteristics. In addition, it is well known that ZnO nanowires have a large amount of surface defects, mainly oxygen vacancies that will adsorb gas species and act as scattering and trapping centres thus lowering the carrier mobility [27]. Therefore, various approaches were studied in the past to enhance the electrical properties of the NWFET and the stability of the devices in air. The effects of these approaches will be discussed.

2.4.1 Effect of passivation

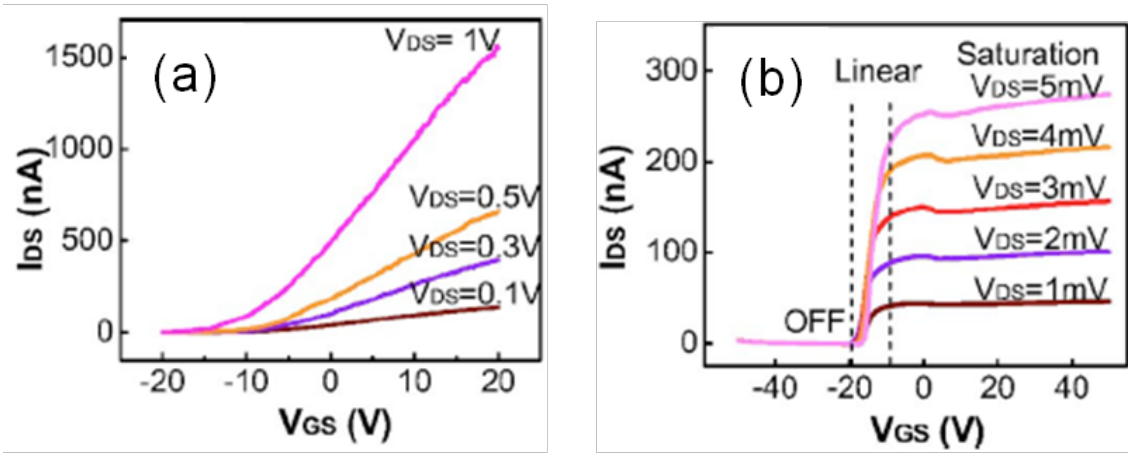


Fig.2.3 I_D-V_G curves of (a) a ZnO NWFET without surface treatments showing n-type semiconducting behaviour (b) a surface treated NWFET exhibits significantly enhanced on/off ratio and transconductance [36]

The passivation process involves coating the channel layer with dielectric or polymer materials. The purpose of this is to reduce surface influence on the electrical characteristics of the transistor. One characteristic improvement is the field-effect mobility after passivation. A very high value of mobility was obtained from passivated devices. For example, a mobility of 3118 cm^2/Vs was achieved by Chang *et al* after SiO_2/Si_3N_4 dielectric passivation [36]. In their work, the untreated NWFETs were placed in a vacuum chamber (10^{-6} torr) to remove the surface adsorbents such as O_2 and H_2O, and a layer of SiO_2 was deposited to prevent subsequent chemical readsorption. Subsequently a Si_3N_4 layer was deposited on top of the SiO_2 by plasma enhanced chemical vapour deposition (PECVD). Fig.2.3 shows the transfer curves on linear scales of as-grown and passivated devices showing enhanced gating compared to the as- grown device. However, the passivated device exhibited a high negative threshold voltage. A similar improvement in mobility from 75 to 1000 cm^2/Vs was reported by Park *et al* when their nanowires were passivated with a polymer layer [34].

Besides improving the device performance, Song *et.al* also demonstrated that passivated ZnO NWFETs with PMMA exhibited stable electrical characteristics under different environments with the highest mobility achieved at 60 cm^2/Vs[45]. The poor electrical characteristics experienced by unpassivated ZnO NWFETs can be due to physically poor contact between the nanowire and the device substrate.

Apart from improving the mobility, passivation also shifts the threshold voltages of the device towards either the positive or negative gate bias direction depending on the initial morphology and surface states of the as-grown nanowire. It was reported that passivation results in the shift of the threshold voltage toward the positive gate bias direction due to the surface-depletion-induced channel narrowing effect [40]. Hong *et al* reported that the roughly grown ZnO nanowires exhibited a dramatic threshold shift of more than 20 V towards the positive gate bias direction compared to their smooth nanowires [40]. Meanwhile Chang *et al* showed that the V_{TH} shifted negatively after their SiO_2/Si_3N_4 passivation process [36]. These results indicate that the electrical properties of the ZnO NWFETs can be tuned by controlling the surface and/or interface properties.

2.4.2 Effect of gate dielectric material

ZnO NWFET device performance can further be improved by replacing the SiO_2 gate dielectric layer with organic material[38] and high-k dielectric such as Al_2O_3 or HfO_2[44]. A maximum mobility of 1175 cm^2/Vs was achieved by Ju *et al* [38] when self-assembled nanodielectric (SAND) was used as the gate dielectric. Although the origin of this high mobility is currently unresolved, the dielectric material provides a high quality interface which is indicated by the low subthreshold swing achieved.

In another work Cha *et al* have demonstrated a mobility of 928 cm^2/Vs from their top-gated ZnO NWFET with nanosize air-gap dielectric as shown in Fig.2.4. The SEM image shows the metal-air gap-semiconductor field effect transistor (MASFET) where the ZnO nanowire is suspended between the source and drain electrodes. The air gap which acts as the gate dielectric is used to reduce the leakage current through gate and channel which is more prevalent in a solid insulator.

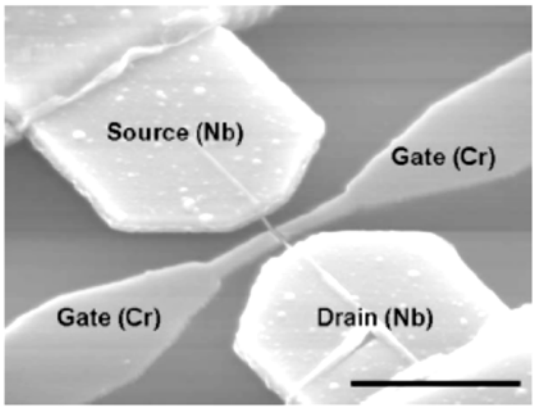


Fig.2.4 SEM image of fabricated ZnO NWFET with self - aligned gate electrodes and nanosize air gaps. Scale bar is 2.5 μm [37].

2.4.3 Effect of annealing

Bottom-up grown ZnO nanowires are well known to be conductive and unsuitable for transistor application. This large conductivity of the as-grown nanowires is believed to be due to a high density of dopants that are unintentionally incorporated into the ZnO lattice especially during VLS growth. To make the nanowires useful for FETs, the charge carrier density must be reduced. Recently, Jeon *et al* adopted ambient annealing at 600^{o}C after nanowire growth [44]. Although the annealing procedure reduced the V_{TH} from -65 V to -2 V of the NWFET, the maximum mobility achieved was only 12 cm^2/Vs. Meanwhile, Kalbein *et al* also performed annealing in ambient air and they achieved a maximum mobility of 40 cm^2/Vs [28]. Apart from ambient annealing, Keem *et al* employed H_2-annealing and the H_2-annealed device exhibited field-effect characteristics with mobility of 302 cm^2/Vs achieved after 20 mins of annealing [39]. It is known that hydrogen reduces surface states, by passivating the Si dangling bonds. However,Huang *et al* reported the occurrence of etching and redeposition of ZnO nanowires due to the H_2 annealing thus increasing the conductivity of ZnO NWFET[46]. Therefore the duration and the temperature of the H_2 anneal need to be carefully monitored.

2.4.4 Effect of other treatments

Besides annealing, other methods such as solvent [47] and acid [43] treatments were also known to shift the V_{TH} positively. The adsorption of atmospheric oxygen on the surface defect sites causes electron trapping. These treatments generate surface roughness on the nanowire surface thus inducing more trapping of electrons, causing electron depletion in the channel.

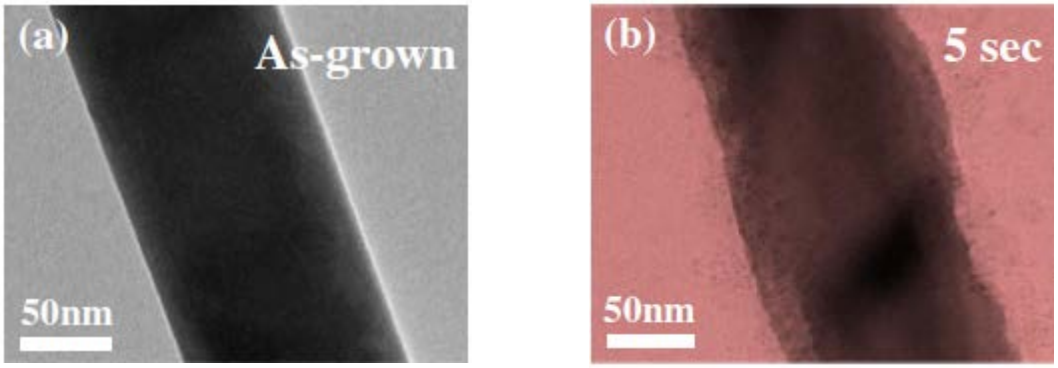


Fig. 2.5 Low resolution TEM images of (a) bottom-up as grown ZnO nanowire (b) after 5s submersion in 10% H_2O_2[43]

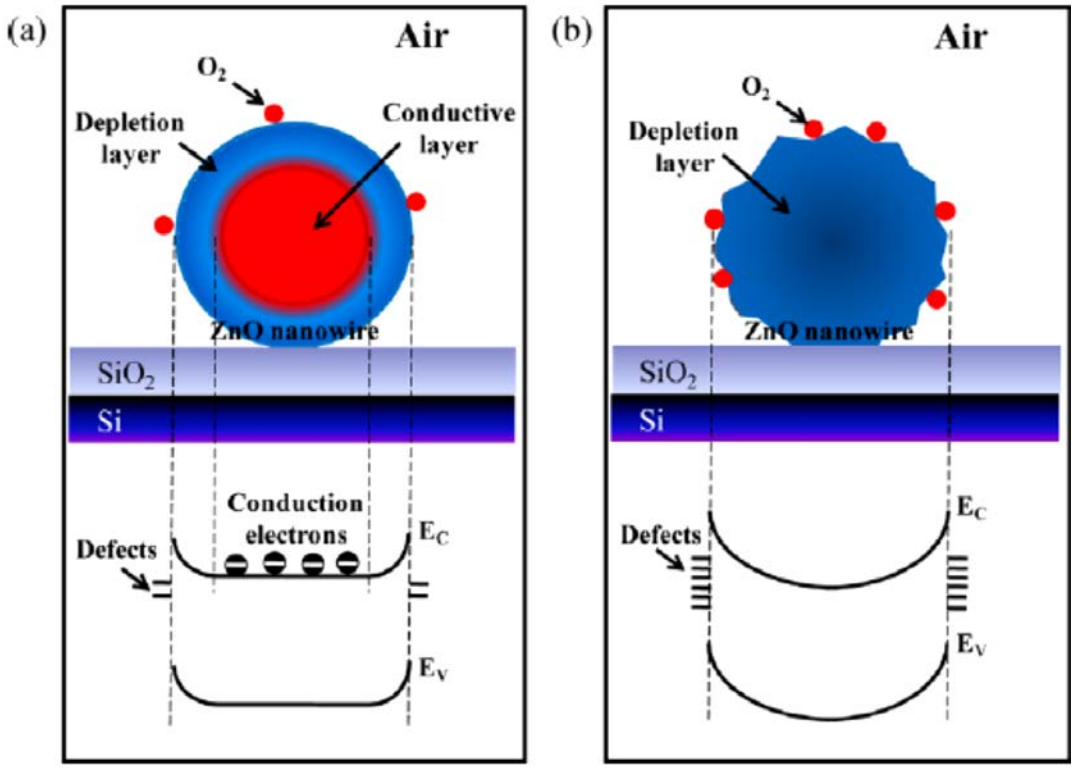


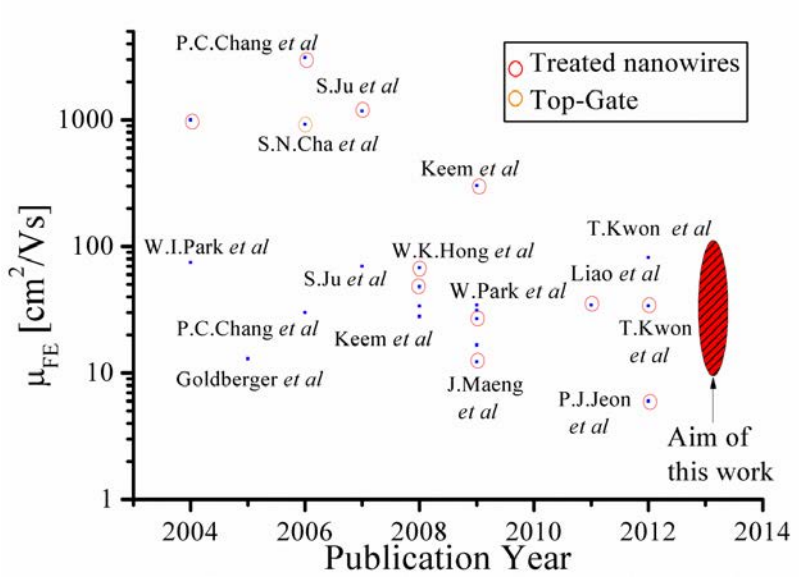
Fig 2.6 Schematic cross-sections and the corresponding energy band diagrams at V_G=0 V for (a) as-grown nanowires and (b) solvent-etched ZnO nanowires after submersion in IPA for 30 days. E_C is the conduction band and E_V is the valence band of the ZnO nanowires[47]

Fig 2.5 shows low magnification TEM images of ZnO NWs for as – grown devices and treated by H_2O_2 submersion for 5s. It is clear that the treated nanowire surface is considerably rougher than for as-grown NWs. Generally, before these treatments the ZnO NWFETs operate in depletion mode but are converted to the enhancement mode after submersion in this chemical. The observed results were explained in Fig 2.6. For the as - grown ZnO nanowires, fewer defects were generated, showing less band - bending and a smaller depletion region.

However, the chemically treated ZnO nanowire has more defects and exhibited greater surface energy band bending and large depletion region.

In another work, Liao *et al* performed Ga+ irradiation in a focused ion beam system to reduce the surface defects which resulted in a decrease in the species adsorbed on the nanowire surface [42]. As a result, the I_{ON}/I_{OFF} ratio increased and the threshold voltage shifted towards the positive direction. However, the Ga ion irradiation might lead to the implantation of Ga ions into the ZnO nanowire, which might increase the probability of impurity scatterings and reduce the carrier mobility.

(a)



(b)

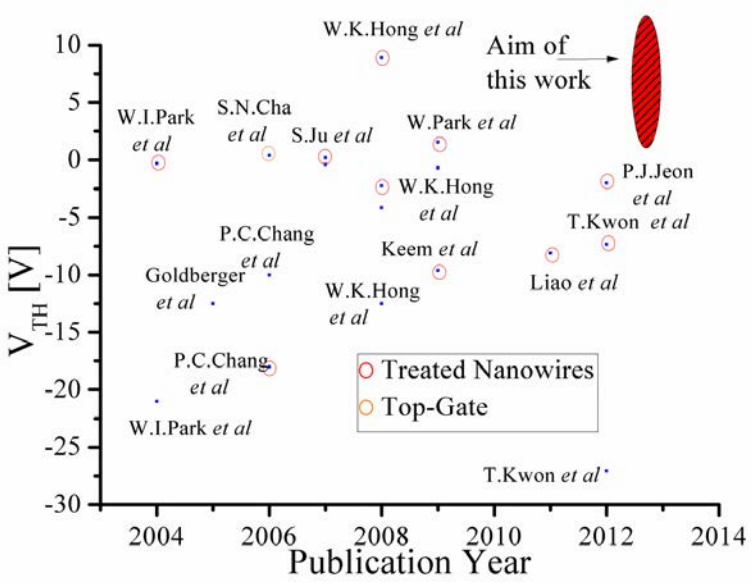


Figure 2.7 (a) Field effect mobilities, μ_{FE} (b) Threshold voltages obtained from literature on ZnO NWFETs published from 2004 to 2012 and aim of this work.

Fig.2.7 shows plots of some of the results for mobility and threshold voltage obtained from bottom-up techniques published from 2004 to 2012. From Fig.2.7(a) which shows the field-effect mobilities obtained from the literature from 2004, the values degrade from ~3000 cm^2/Vs achieved in 2006 by Chang et al [36] to a recently published device with a mobility of 80 cm^2/Vs [43]. Therefore, high mobility cannot be achieved consistently with bottom-up techniques. In addition, the mobility varies widely from 2004 to 2012. The red area highlighted in the plot shows the target that this work intends to achieve.

Fig.2.7 (b) shows the threshold voltages from the literature that were achieved. Most untreated ZnO nanowire devices exhibit depletion mode characteristics. Usually, after surface treatments such as passivation and annealing, the threshold voltages shift positively. This work aims to produce ZnO NWFET device with enhancement mode characteristics since it is preferred for low - power CMOS compatible logic applications.

2.5 Biosensor Applications

The ZnO channel has been shown to be sensitive to surface effects from changes in the environment. Due to the sensitivity of ZnO nanostructures to environment, good biocompatibility and non-toxicity, these nanostructures including nanowires have high potential in biosensing applications. Researchers have studied many ZnO nanostructures for biosensor applications that were synthesized by various bottom-up approaches [48-51]. As mentioned and discussed previously, these nanowire sensors based on bottom-up techniques generally involve a complex fabrication process for manipulating and aligning a single strand of semiconducting nanowire as the FET channel between the source and drain patterns. Therefore, it is difficult to achieve repeatability and manufacturability in fabrication and integration of these devices for large sensor arrays. Thus, the development of a very low cost and simple fabrication route suitable for mass manufacture for nanowire sensors would accelerate their uptake as point-of-care (POC) devices.

Recently, a ZnO TFT based immunosensor was demonstrated by Reyes *et al* [52]. The detection of the bioanalytes was achieved through channel carrier modulation caused by the biochemical reaction as shown in Fig.2.8. Fig.2.8 (a) shows the unfunctionalized ZnO bioTFT with positive bias at the drain and gate electrodes. Fig.2.8 (b) shows that the exposed ZnO channel is functionalized with antibodies which consequently decrease the conductivity of the ZnO surface layer. Fig.2.8 (c) shows that the conductivity increases when protein is captured by the antibodies which form positively charged tips. This experiment demonstrates that the ZnO channel layer has the ability to perform biosensing by carrier modulation.

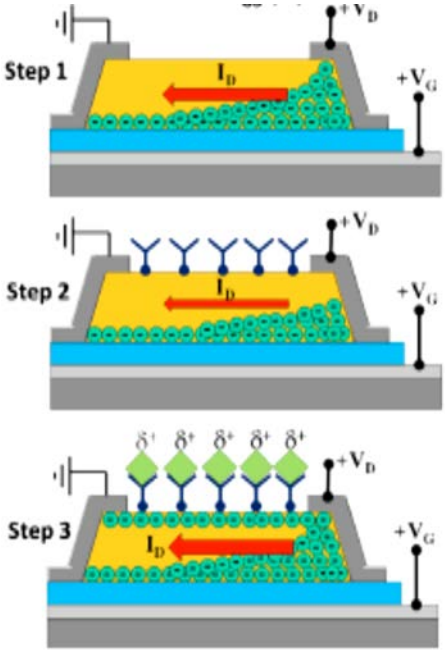


Fig.2.8 Schematic of carrier modulation mechanism (a) Bare device before functionalization (b) Antibody immobilization (c) Protein detection [52]

2.4 Motivation of this work

The electrical performance based on single nanowire FETs have been discussed and evaluated. Technology to scale transistor current by placing more than one ZnO nanowire in parallel in a controlled way is still not available at present using bottom-up techniques. In recent years, some investigations have involved the fabrication of multiple ZnO NWFETs to enhance the FET characteristics [53-56]. However, this structure suffers from variations in the contact quality of the metal/NW, the dielectric/NW and the NW/NW interfaces which affects the reproducibility of the electrical characteristics. Therefore, this work aims to tackle several issues which are not addressed in previous work.

1. This work aims to demonstrate top-down fabrication of ZnO nanowires. In this approach, the nanowires are in defined locations, controlled dimensions and alignments. This also allows nanowire transistor design with different channel lengths and number of nanowires in a single device design.
2. The top-down approach involves the use of the PEALD process to deposit high quality semiconducting ZnO layers. PEALD allows good control over carrier concentration and resistivity [57][58]. Particularly, this work will explore the feasibility of ZnO film

deposition in remote PEALD in which the O_2 reactant plasma is generated remotely from the deposition substrate.

3. This work aimed to achieve enhancement mode NWFETs with field effect mobility of ≥ 10 cm^2/Vs based on untreated individual nanowire. This can be achieved by carefully optimizing the dry etch and ALD deposition.
4. This work will study the electrical reproducibility and hysteresis behaviour for different times and environments of the top-down fabricated NWFETs. Research has shown that bottom-up nanowires exhibit high hysteresis and electrical performance deterioration over time [35] [40] [43] [44]. Will top-down fabricated NWFET show electrically reproducible characteristics because of better control of fabrication process?
5. Taking advantage of the surface sensitivity and biocompatibility, this work aimed to study the viability of biosensing mechanism of top-down fabricated NWFETs. It is anticipated that the well -controlled ZnO nanowires for bio- applications involving enzymes, proteins, DNA and CMOS compatibility makes it a promising material and technology for low - cost and mass manufacturable point-of-care devices.

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Chapter 3

Theory

3.1 Introduction

This chapter provides qualitative details of the nanowire device structure and theory based on TFT operation principles. This is because the fabricated NWFET is technically a TFT and the conduction through ZnO nanowires is surface-centred rather than bulk-centred. In addition, this chapter discusses the extraction method of the electrical characteristics such as the subthreshold slope, threshold voltage and field-effect mobility and verifies these measured values with calculations.

Fig.3.1 presents a typical bottom gate ZnO TFT structure. The structure of TFTs differs from the conventional metal-oxide-semiconductor field-effect transistor (MOSFET) due to the absence of the two n+ regions in a p-type substrate for a typical NMOS. On the contrary, for an n-channel TFT in bottom gate configuration, ohmic contacts on the undoped ZnO semiconductor surface form the source and drain electrodes. This simplified structure of the n-channel TFT distinguishes the device from the NMOS and its normal mode of operation.

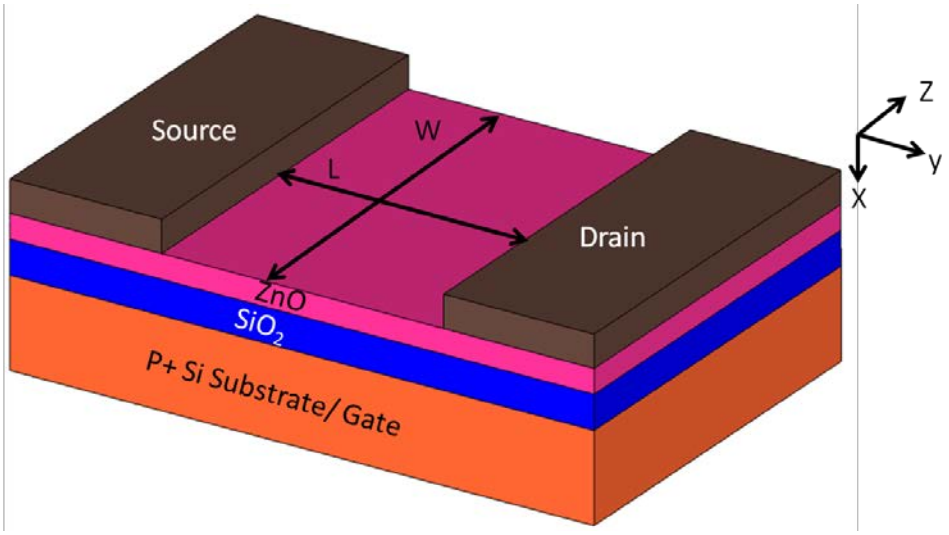


Fig.3.1 Typical ZnO bottom-gate TFT device

3.2 ZnO TFT Regions of Operation

A cross-sectional view and basic features of the ZnO TFT with an adjoining coordinate system is shown in Fig.3.1.The basic device dimensions are the channel length *L* which is the distance between source and drain in the y-direction, the channel width *W* in the z-direction, and the ZnO channel depth d_{ZnO} in the x-direction.

TFTs are field-effect transistors (FET) which operate as majority carrier devices in the accumulation regime. It has only 2 modes of operation; depletion and accumulation. The analysis of the current-voltage (I-V) characteristics for a TFT is in effect similar to that for conventional MOSFETs[1]. The following assumptions are made in order to model the I-V characteristics

1. The channel mobility μ is constant.
2. The source and drain ohmic contacts to ZnO have negligible contact resistance.
3. The flat-band voltage, V_{fb}, is taken to be much smaller than the threshold voltage, V_{TH} and thus negligible. This condition corresponds to the requirements of zero fixed oxide charge and work-function difference between gate and ZnO semiconductor.
4. The charge concentration is uniformly distributed throughout the thin film.
5. The thickness of the ZnO film, d_{ZnO} << the channel length, L.

3.2.1 Depletion Mode Operation

When a negative bias is applied to the gate electrode, the majority carriers in the p-type substrate (gate) which are holes electrostatically will be attracted towards the electrode leaving the minority electron carriers at the SiO_2 interface. Consequently, the electrons in the n-type semiconductor are withdrawn and a depletion region forms at the ZnO-insulator surface. When negative bias is increased, the depletion region in ZnO widens since more electrons are withdrawn. The TFT is said to be in its *off-state* since no conducting channel is present between the source and drain contact. Fig.3.2 shows the schematic of a ZnO TFT operates in depletion. For wide-band gap materials with inherent n-type conduction such as ZnO, the bands are bent upward.

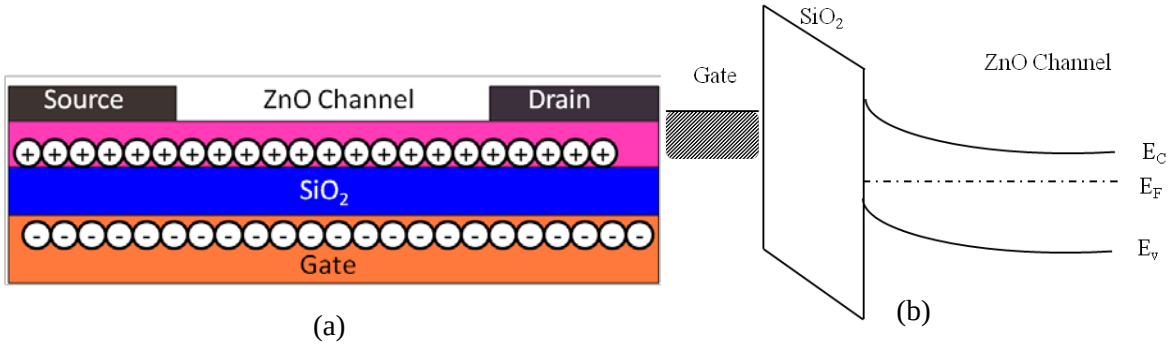


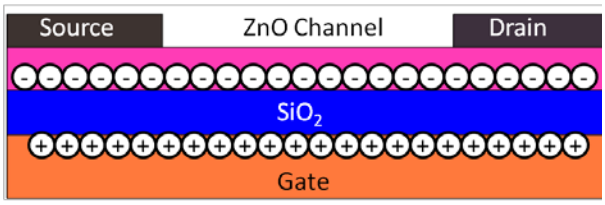
Fig.3.2 (a) Schematic of ZnO TFT (b) Energy band diagram in depletion mode of operation

3.2.2 Accumulation of Charge

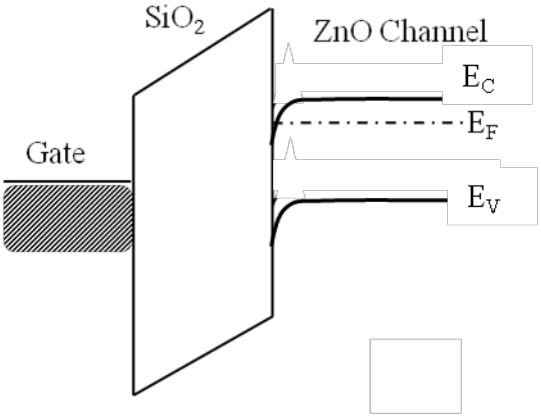
When the gate bias increases positively, charge accumulation (electrons) starts to form at the ZnO/SiO_2 interface. The voltage corresponds to this onset of charge accumulation induced and the onset of drain current on a $\log_{10}(I_D)$-V_G transfer curve is called the threshold voltage. A schematic of the ZnO TFT illustrating the accumulation of negative charge in the vicinity of the ZnO/SiO_2 interface is shown in Fig.3.3 (a) and a band diagram is shown in Fig.3.3 (b). Hence the device operates in the linear region and behaves like a voltage-controlled resistor with a small drain current ($0 < V_D < V_G$).

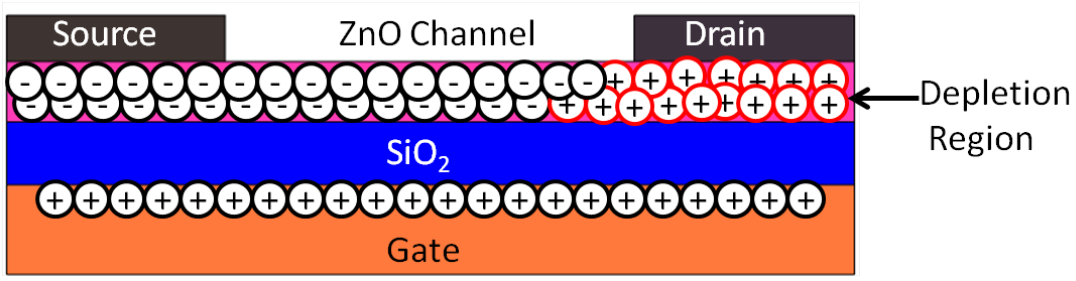
When the drain bias equals the gate bias ($V_D = V_G$), the potential near the drain end reduces. It eventually reaches a point called the pinch-off point at which the accumulation charge at the drain end, $Q_{acc}(L)$ is reduced to nearly zero and hence depletion region forms from the ZnO/SiO_2 channel interface. Beyond this drain bias, the drain current remains the same, because for $V_D > V_{Dsat}$, the pinch-off point starts to move toward the source as shown in Fig. 3.3 (c) but the voltage at this pinch-off point remains the same, V_{Dsat}.

(a)



(b)





(c)

Fig.3.3 (a) Schematic of ZnO TFT in linear operation (b) Energy band diagram in accumulation mode of operation (c) Schematic of ZnO TFT in saturation.

The drain current, I_D is a combination of drift and diffusion currents. In the linear operation region where V_D is low, the channel charge is more uniform from source to drain allowing the diffusion current to be negligible. Considering a differential drain voltage for an elemental section *dy* of the conducting channel, given by[1]

$$dV = \frac{I_D dy}{\mu_{FE} W |Q_{acc}(y)|} \qquad (3.1)$$

where μ_{FE} is the carrier mobility , W is the channel width and $Q_{acc}(y)$ is the total accumulated charge per unit area induced at a position y along the channel.

Consistent with FET operation, the drain voltage V_D drop is a function of its position along the channel from y = 0, V(y) = 0 at the source to y = L, V(y) =V_D at the drain contact. At low drain bias, Q_{acc} is uniformly distributed over the entire channel. The total charge induced in the ZnO thin film forming the accumulation layer is given by Eq.(3.2)

$$Q_{\text{acc}} = C_{\text{ins}}|V_{\text{G}} - V_{\text{TH}} - V(y)| \qquad (3.2)$$

where C_{ins} is the capacitance of the gate dielectric per unit area, V_G is the gate-to-source voltage, V_{TH} is the threshold voltage, and V(y) is the drain voltage drop along the channel. Substituting Eq. (3.2) into Eq.(3.1) yield

$$I_{\text{D}} \int_0^L dy = \mu W \int_0^{V_{\text{D}}} \left[C_{\text{ins}}\left(V_{\text{G}} - V_{\text{TH}} - V(y)\right)\right] dV \qquad (3.3)$$

The drain current as a function of drain voltage at any point along the channel can be obtained from Eq.(3.3) above. Hence in the linear region with low V_D and $V_G > V_{TH}$,

$$\therefore I_{\text{D}} = \frac{W}{L} C_{\text{ins}} \mu_{\text{FE}} \{(V_{\text{G}} - V_{\text{TH}})V_{\text{D}} - \frac{1}{2} V_{\text{D}}^2\} \qquad (3.4)$$

where μ_{FE} is the field-effect mobility.

Since $V_D << V_G - V_{TH}$, Eq.(3.4) is normally simplified into

$$I_{\text{D}} = \frac{W}{L} C_{\text{ins}} \mu_{\text{FE}} (V_{\text{G}} - V_{\text{TH}}) V_{\text{D}} \qquad (3.5)$$

In saturation mode of operation in which $V_D \geq V_G - V_{TH}$, the conducting channel is in saturation (pinch-off) and the region near the drain contact is depleted of free carriers. The drain current, I_D, now increases independently of the drain bias, V_D

$$I_{\text{D}} = W \frac{C_{\text{ins}}}{2} \mu_{\text{sat}} \frac{(V_{\text{G}} - V_{\text{TH}})^2}{L} \qquad (3.6)$$

where μ_{sat} is called the saturation mobility.

3.2.3 Threshold Voltage Formulation for NWFET

Previously, we have assumed that the flat band voltage is negligible. In addition, the surface potential between ZnO/air is ignored. However, this is not the case particularly for nanowire FET. With its large surface-to-volume ratios, the electronic properties of NWs are strongly affected by the surface effects via chemisorptions/desorption and native surface defects. Fig.3.4 shows the energy band diagram of n-type ZnO nanowire under zero gate bias. It can be seen from the energy band diagram that the surface region between NW/dielectric and NW/air are depleted under zero gate bias. The positive charge at these interfaces is responsible for the

possible threshold voltage. These surface charges are attributed to traps which must be filled with electrons injected from the source electrode into the channel under the application of a positive gate voltage.

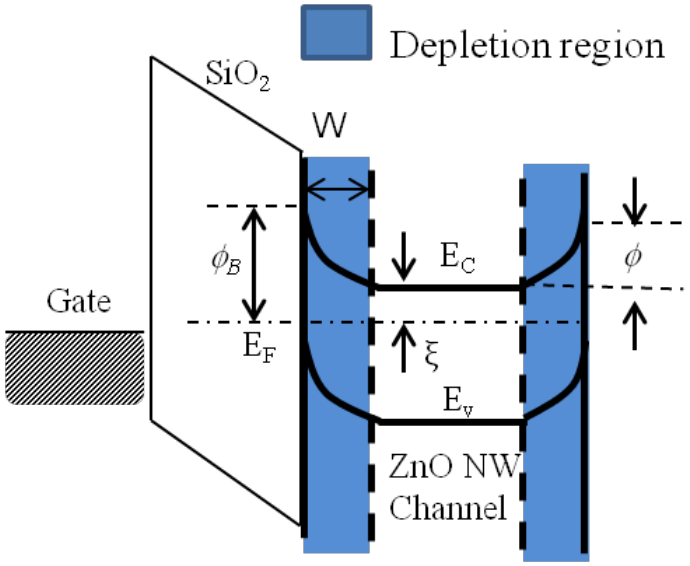


Fig.3.4 Energy band diagram for an n-type ZnO NW at zero gate bias. ϕ, ,surface band bending; ϕ_B,surface barrier height; and W, width of surface band bending region.

The surface band bending (SBB) of the NWs is related to NW diameter, doping level, surface roughness and molecule adsorption on NW surfaces. As considering the diameter and the doping only, a qualitative description of the energy difference, ϕ produced by SBB obeys the following equations [2]. The derivation is shown in Appendix A.1.

$$\phi = \frac{qN_D d^2}{2\varepsilon_{ZnO}\varepsilon_0} \qquad (3.7)$$

where N_D is the donor concentration, d is the depletion width of the NW , ε_{ZnO} is the dielectric constant of the NW and ε_o is the permittivity of free space.

From Fig.3.4, the term ξ is the bulk potential which can be determined by [2]

$$\xi = E_C - E_F = (kT/q)\ln(\frac{N_C}{N_D}) \qquad (3.8)$$

where E_C is the conduction band minimum, k is Boltzmann constant, T is Kelvin temperature, q is the elementary charge, N_C is the conduction band density of states ~ 2.94 x 10^{18} cm^{-3}[3]. As the temperature is 300 K and considering the N_D ~ 10^{17} cm^{-3}, the E_F lies 0.034 eV below the E_C (i.e $\xi = E_C - E_F = 0.034$ eV).

From Fig.3.4, the gate bias applied to achieve this condition is called the flat band voltage V_{fb}, which is the work function difference between the metal gate and the ZnO channel as:

$$V_{fb} = \psi_{ms} = \psi_{m} - \psi_{ZnO} \quad (3.9)$$

In Eq.(3.9), the gate oxide was assumed to be an ideal insulator. However, this is not true and hence gate oxide charges and their influence are shown in Deal's work in which four types of oxide charges are modelled [4]; (1) fixed oxide charges, Q_f, (2) mobile ionic charge, Q_m (3) oxide trapped charge, Q_{tot}, and (4) interface trapped charge, Q_{it}.

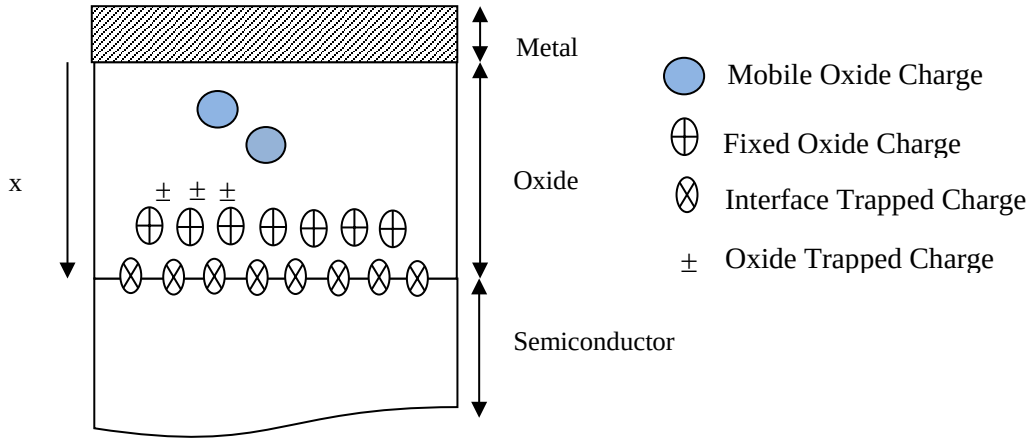


Fig.3.5 The modelled charges in gate oxide [3]

Although, this model is used in Si/SiO_2 interface, it is also considered in the analysis of ZnO/SiO_2 interface. The most relevant charges which will be discussed in this section are the interface charges. These charges have also been called surface states, fast states and interface states, respectively. The effects of the interface charge can be simplified using an effective net interface charge, Q_{IT} (C/cm^2). Thus, the influence of this charge on flat band voltage can be modelled together with flat band voltage as:

$$\therefore V_{fb} \approx \psi_{ms} - Q_{IT}/C_{ins} \quad (3.10)$$

where Q_{IT} is the effective net interface charge and C_{ins} is the gate oxide capacitance per unit area.

Therefore, V_{TH} is the gate voltage which accounts for the flatband correction and all charges in the insulator, at the insulator/ZnO interface and also at the accumulation charge, Q_{acc}. Then the V_{TH} may be expressed as

$$V_{TH} = V_{fb} + Q_{acc}/C_{ins} \quad (3.11)$$

By solving Poisson's equation shown in Ref[1], Q_{acc} is expressed as

$$Q_{acc} = \sqrt{2\varepsilon_{ZnO}\varepsilon_0 q N_D \phi} \quad (3.12)$$

where N_D is the channel dopant concentration, ε_{ZnO} is the permittivity of ZnO, ε_0 is the permittivity of space and ϕ is the surface potential defined in Fig.3.4.

The expression for V_{TH} can be obtained by substituting Eq. (3.10) and Eq.(3.12) into Eq.(3.11),

$$V_{TH} = -\frac{Q_{IT}}{C_{ins}} + \frac{1}{C_{ins}}\sqrt{2q^2 d^2 N_D^2} \quad (3.13)$$

assuming ψ_{ms} is negligibly small.

3.2.4 Subthreshold Region

Besides the discussed linear and saturation regions, another operation region is discussed in this section. When the gate bias is slightly lower than V_{TH}, the drain current in this region, named the subthreshold current, is nonnegligible and is a critical characteristic for transistors operated at low voltage for low power applications.

In the linear and saturation regions, the drift current, controlled by the drain source electric field, is the dominant part of the drain current. When the gate voltage is less than the threshold voltage, a small amount of drain current may flow. This occurs because of electron injection into the channel. This type of injection current is modelled as the subthreshold current. In the subthreshold region, the current is mainly due to diffusion current. The drain current operating in this region is given by [5] which is derived from inversion-mode device,

$$I_D = I_{D1} \exp\left(\frac{q(V_G - V_{TH})}{nkT}\right)\left(1 - \exp\left(-\frac{qV_D}{kT}\right)\right) \quad (3.14)$$

where I_{D1} depends on temperature, device dimensions and channel doping. The term n given by

$$n = 1 + \frac{C_{acc}}{C_{ins}} \quad (3.15)$$

where C_{acc} is the capacitance per unit area during accumulation and defined as

$$C_{acc} = \frac{\varepsilon_{ZnO}}{W_{acc}} \quad (3.16)$$

where W_{acc} is the accumulation width and can be solved as

$$W_{\text{acc}} = \frac{Q_{\text{acc}}}{qN_{\text{D}}} \tag{3.17}$$

Substituting Eq.(3.12) into Eq.(3.17), W_{acc} is defined as

$$W_{\text{acc}} = \frac{\sqrt{2\varepsilon_{\text{ZnO}}\varepsilon_0 qN_{\text{D}}\phi}}{qN_{\text{D}}} = \sqrt{\frac{2\varepsilon_{\text{ZnO}}\varepsilon_0\phi}{qN_{\text{D}}}} \tag{3.18}$$

Thus Eq.(3.16) becomes

$$C_{\text{acc}} = \sqrt{\frac{qN_{\text{D}}\varepsilon_{\text{ZnO}}}{2\phi}} \tag{3.19}$$

Eq. (3.14) is derived from the electron density gradient in the channel in which the the electron density depends exponentially with the channel potential. Thus, Eq. (3.14) is applicable for accumulation mode device. When V_D is larger than kT/q, the last term in Eq.(3.14) can be ignored. Therefore, the subthreshold current varies exponentially with gate bias. Thus, a graph of log (I_D) against V_G is linear in the subthreshold region, as shown in Fig.3.6. Such a plot has a slope of [5],

$$slope = q/[\ln(10)nkT] \tag{3.20}$$

The slope is usually expressed as the subthreshold swing, SS, which is the gate voltage necessary to change the drain current by one decade, and is given by

$$SS = \frac{1}{slope} = \left(\frac{\ln(10)nkT}{q}\right) = 2.3\frac{kT}{q}\left(1 + \frac{C_{\text{acc}}}{C_{\text{ins}}}\right)\ V/decade \tag{3.21}$$

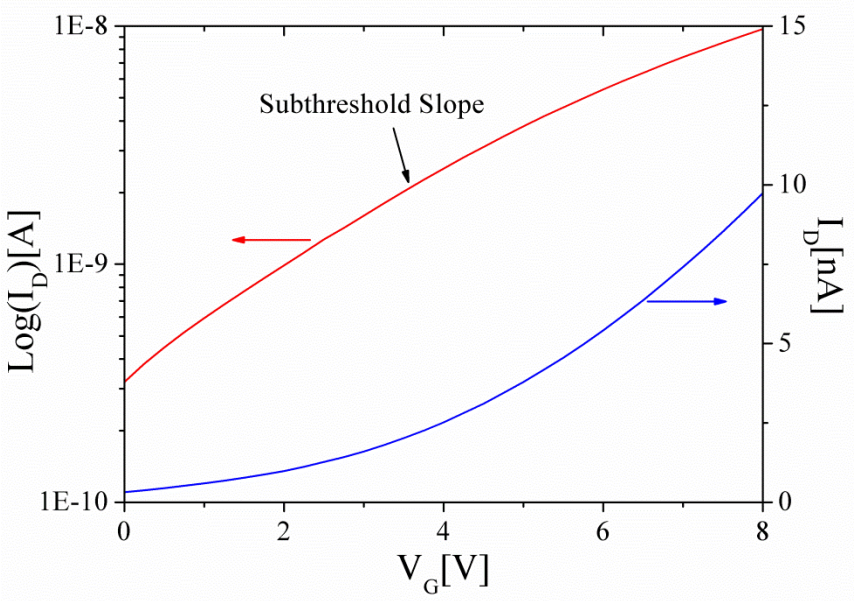


Fig.3.6 The I_D-V_G curve plotted in linear (blue) and logarithmic scales of I_D

It is noted that a steeper subthreshold slope (SS) should be achieved in devices in order for the transistor to be turned on using a lower voltage. In the extreme of zero oxide thickness, $C_{acc} << C_{ins}$, the SS reaches a theoretical limit, which is 60 mV/decade. For non – zero oxide thickness, the swing is degraded by a factor which is a voltage divider of two capacitors in series, whose ratio is C_{acc}/C_{ins}. Since C_{acc} depends on the channel doping, N_D, the SS is degraded when the channel doping increases. An additional contribution to C_{acc} may arise due to the unavoidable presence of surface states in the semiconductor. To take surface and interface states into account, an interface capacitance, C_{int} is introduced in parallel with the accumulation capacitance for the ZnO FET device. Therefore, SS can be written as

$$SS = 2.3\frac{kT}{q}\left(1 + \frac{C_{\text{acc}}}{C_{\text{ins}}} + \frac{C_{\text{int}}}{C_{\text{ins}}}\right) V/decade \qquad (3.22)$$

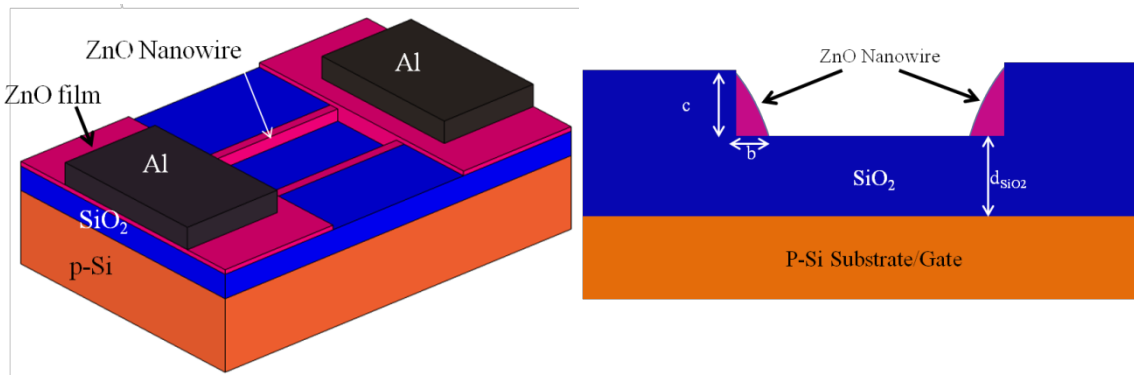
Thus, the SS is degraded by the charges at the ZnO/SiO_2 interface. From the SS, the interface trap density, $N_T = C_{int}/q$ $cm^{-2}eV^{-1}$ can be determined by Eq.(3.23)

$$SS = 2.3\frac{kT}{q}\left(1 + \frac{qN_{\text{T}}}{C_{\text{ins}}}\right) V/decade \qquad (3.23)$$

assuming $C_{acc} << C_{ins.}$

3.3 Electrical Parameters Extraction

Based on the operation principle discussed previously, electrical parameters such as gate oxide capacitance, V_{TH} and field-effect mobility extraction will be discussed in this section



(a) (b)

Fig.3.7 (a) ZnO NWFET structure from this work (b) Cross-sectional view of the ZnO nanowire

based on the fabricated nanowire FET. Fig.3.7 (a) shows the structure of a nanowire FET and Fig.3.7 (b) shows the cross - section view of the nanowire FET fabricated in this work. The nanowire is considered to have triangular cross section. The width at the base, *b* is typically 35 nm, the height, *c* is 100 nm which is the height of the SiO_2 pillar and the SiO_2 thickness,d_{SiO2} is100 nm

3.3.1 Oxide Capacitance

To determine the oxide capacitance or the gate capacitance of the nanowire FET, usually the metallic cylinder on an infinite metal plate model is used [6-8]. The cross-section geometry and the equipotential lines of this model are shown in Fig. 3.8. In order to use this model, it is assumed that the nanowire is completely embedded in the dielectric and has a circular cross section. This assumption was reexamined by Wunnicke [9] and will be presented in this chapter based on the NWFET.

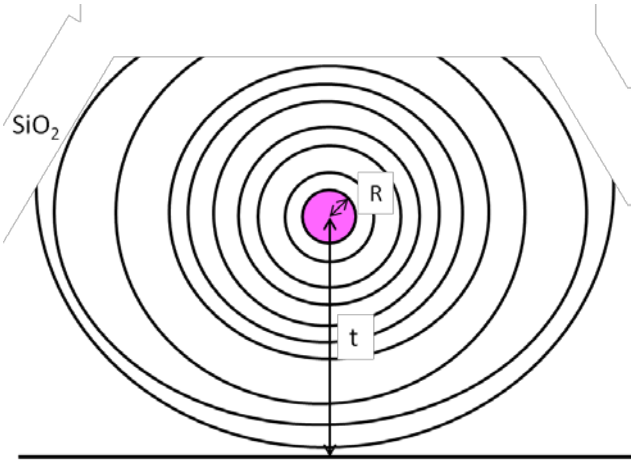


Fig.3.8 Cross - section geometry of back-gated NWFETs of embedded NW with t/R =6. The lines are equally separated constant potentials obtained by FEM calculations in Ref [9]

The model yields an analytical equation for the gate capacitance per unit length shown in Eq.(3.24)

$$\frac{C_{\mathrm{NW}}}{L} = \frac{2\pi\varepsilon_0\varepsilon_{\mathrm{r}}}{cosh^{-1}(\frac{t}{R})} \tag{3.24}$$

where ε_r is the dielectric constant of the embedding dielectric, t is the distance between the metal plate and the centre of the cylinder, and R is the radius of the cylinder as shown in Fig.3.5. For $x = t/R \gg 1$, the approximation $cosh^{-1}(x) = \ln(x + \sqrt{x^2 - 1} \approx \ln(2x)$ can be used. Eq. (3.24) then becomes

$$\frac{C_{\mathrm{NW}}}{L} = \frac{2\pi\varepsilon_0\varepsilon_{\mathrm{r}}}{\ln(2\frac{t}{R})} \tag{3.25}$$

Relating this with the NWFET structure shown in Fig. 3.7(b), $t = (100 + c/2)nm$ where c = 100 nm, so $t = 150\ nm$. If the base is taken as the diameter of the nanowire, the radius, $R = \frac{b}{2} = 17.5\ nm$. So $t/R \gg 1$ thus Eq.(3.25) can be used to calculate the gate capacitance in this work.

However, in this work, the NW is lying on top of the gate dielectric in which there is missing dielectric material around the NW (Fig.3.7). Therefore, Eq.(3.25) can only give an upper limit for the gate capacitance.

In the literature, the capacitance of non-embedded NWFETs is taken into account by an experimental effective dielectric constant for SiO_2 of $\varepsilon_{r,eff} = 2.5$ [10][11] or $\varepsilon_{r,eff} = 1.95$ [12] in combination of Eq.(3.25). In addition, Wunnicke also considered different shapes of the nanowires for his Finite Element Method (FEM) gate capacitance calculations [9]. An effective dielectric constant of $\varepsilon_{r,eff} = 2.25$ for the hexagonal, $\varepsilon_{r,eff} = 2.45$ for the squarelike, and $\varepsilon_{r,eff} = 2.65$ was found for the triangular cross sections of nanowires. The triangular cross section has a higher effective dielectric constant due to the larger contact area between these NWs and the gate dielectric compared to circular cross section [9]. Therefore in this work, an effective dielectric constant of $\varepsilon_{r,eff} = 2.65$ will be used. From Eq.(3.24), the capacitance is then calculated to be 0.52 fF.

3.3.2 Threshold Voltage, V_{TH}

Fig.3.9 shows the I_D-V_G plot of the NWFET structure shown in Fig.3.7 in linear scale (red) and logarithmic scale (blue) at V_D=1V. The channel length, L= 10 μm. The threshold

voltage, V_{TH} is extracted from the linear plot of I_D-V_G characteristics shown in Fig.3.9. This method utilises Eq. (3.5) when I_D=0,

$$I_D \approx (V_G - V_{TH})V_D = 0$$

$$\therefore V_{TH} = V_G$$

assuming drain current depends linearly with gate voltage at low drain bias, V_D = 1 Hence, V_{TH} is determined from the extrapolated or intercept of gate voltage, V_G at I_D = 0 shown in Fig.3.9. This is the method which is used to extract V_{TH}.

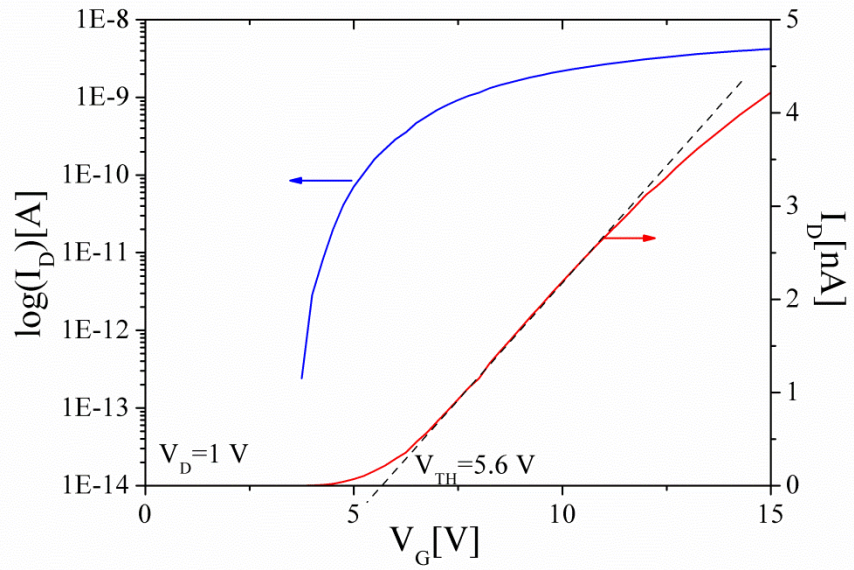


Fig.3.9 Linear I_D-V_G plot (red) at V_D = 1 V and subthreshold characteristics (blue) of ZnO NWFET structure with channel length, L = 10 μm.

Eq.(3.13) is used to calculate V_{TH} and verify if it agrees with the extracted value.

$$V_{TH} = -\frac{Q_{IT}}{C_{ins}} + \frac{1}{C_{ins}}\sqrt{2q^2d^2N_D{}^2} \qquad (3.13)$$

From Fig.3.9, SS determined from the steepest slope of the subthreshold characteristics and found to be 0.35 V/dec. Therefore from Eq. (3.22),

$$SS = 2.3\frac{kT}{q}\left(1 + \frac{qN_T}{C_{ins}}\right) V/decade$$

$$\frac{qN_T}{C_{ins}} = 5\ eV$$

The carrier concentration of the NW can be obtained by

$$N_D = \frac{C_{NW}|V_G - V_{TH}|}{q\pi R^2 L} \quad (3.26)$$

where the capacitance is defined in Eq.(3.25), R is the NW radius and L is the channel length. Using the experimental parameters, the carrier concentration is estimated to be ~ 4.5 x 10^{17} cm^{-3} at $|V_G - V_{TH}|$=1 V.

Substituting qN_T/C_{ins} into Eq.(3.13) to calculate V_{TH} and N_D= 4.5 x10^{17}/cm^3, ε_{ZnO}=8.66 [13],

$$V_{TH} = \frac{qN_T}{C_{ins}} + \frac{1}{C_{ins}}\sqrt{\frac{2q^2 d^2 N_D^2}{\varepsilon_0}}$$

$$V_{TH} = 5 + 1.1 = 6.1\ V$$

The calculated V_{TH} value differs from the measured value by 26 % which indicates (Eq. 3.13) is valid to determine the V_{TH} for these NWFET devices.

3.3.3 Field-effect mobility, μ_{FE}

The field-effect mobility, μ_{FE} is related to the transistor switching time from the ON-state to the OFF-state which is crucial for electronic applications. In the linear region, for $V_D < V_G$, the charge accumulation across the channel is essentially uniform (the depletion layer near the drain contact is insignificant). With small V_D and sufficient V_G to ensure above-threshold current conduction, the drain current is drift-dominated as shown in Eq. (3.4) previously.

$$I_D \approx \frac{W}{L} C_{ins} \mu_{FE} \{(V_G - V_{TH})V_D\} \quad (3.4)$$

The field effect mobility can then be determined from the transconductance, g_m which is given by

$$g_m = \frac{\partial I_D}{\partial V_G}|_{VD=constant} \cong \frac{W}{L} \mu_{FE} C_{ins} V_D \quad (3.25)$$

For example, the transconductance plot of Fig.3.9 is shown in Fig.3.10. The maximum g_m from the plot is 0.58 nS. If W is taken as the base width of the nanowire = 35 nm, L is the channel

length = 10 μm, μ_{FE} is calculated to be 1.16 cm^2/Vs. However, this is the total mobility achieved for a 2 nanowire device as shown in Fig. 3.7. Therefore, μ_{FE} for a single nanowire device is 0.58 cm^2/Vs.

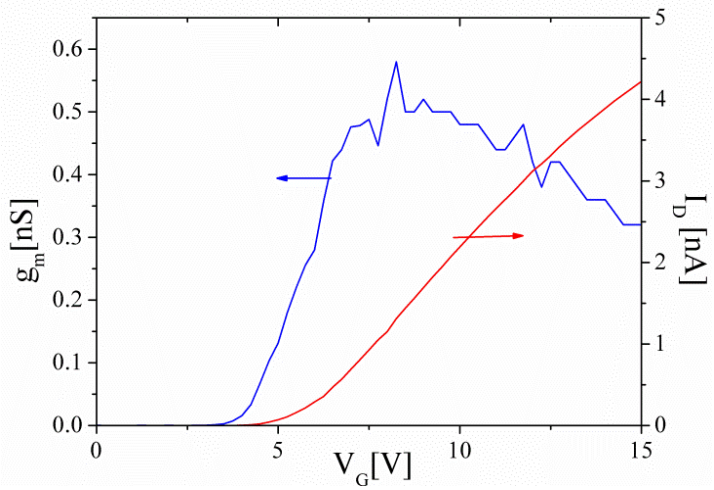


Fig.3.10 Transconductance plot (blue) and linear I_D-V_G plot (red) at V_D= 1 V of the ZnO NWFET structure with channel length, L = 10 μm.

Due to scattering at the surface of the channel, the field-effect mobility is lower than the bulk mobility. For this reason, ZnO/SiO_2 interface quality and surface roughness are critical for transistor performance. In addition, the effective dielectric constant,$\varepsilon_{r,eff}$ of 2.65 is used to model the non - embedded nanowire FET structure and subsequently to calculate the field-effect mobility. If a dielectric constant for SiO_2, ε_r of 3.9 is used to determine the gate capacitance, the field - effect mobility is underestimated by 50%. In order to verify the measured mobility with theory, Fig. 3.11 shows the I_D-V_G of the measured device compared with calculated drain current based on the obtained μ_{FE} of 1.16 cm^2/Vs and Eq. (3.5) for the dual nanowire FET. The maximum percentage difference between these two drain currents is only 16% which is small. This implies that the field effect mobility obtained based on the modelled capacitance is valid for these NWFETs.

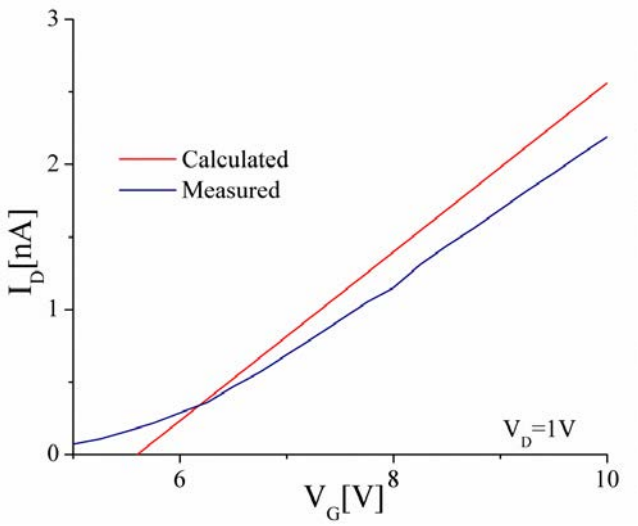


Fig.3.11 Linear I_D-V_G plot measured (blue) and calculated (red) at V_D= 1 V of the ZnO NWFET structure with channel length, L = 10 μm.

3.4 Conclusions

In summary, a perspective view and qualitative discussion of a NWFET device based on TFT operation were discussed. This chapter introduces the operation regions of a TFT device; depletion and accumulation. Threshold voltage formulation was derived based on the accumulation charge TFT and agreed reasonably well with a measured NWFET structure. A capacitance model which uses the effective dielectric constant, $\varepsilon_{r,eff}$ of 2.65 is used to model a triangular non-embedded NWFET. The field effect mobility, μ_{FE} obtained from this capacitance model is almost 50% more than mobility achieved by using capacitance for an embedded circular nanowire model. A comparison between the calculated drain current based on the triangular non-embedded NWFET and measured value yielded a maximum of 16% difference which implied that the capacitance model used is valid for this NWFET structure.

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Chapter 4

Remote PEALD of ZnO Thin Film and Top-Down Fabrication of ZnO NWFETs

4.1 Introduction

In the literature review chapter, it was revealed that most ZnO nanowires were fabricated using bottom-up approach techniques. However, these techniques suffer from inherent drawbacks, such as random placement, contamination during growth and general incompatibility with conventional silicon processing. Top-down methods using electron-beam and focused ion-beam lithography [1][2] have also made great impact to investigate the basic properties of nanowire devices but their use on a large scale is a challenge due to high cost. Recently, H.-W.Ra *et.al* demonstrated top-down fabrication of ZnO nanowires for sensor applications[3], but again the output characteristics only showed a limited low voltage operation up to about 2 V. For successful circuit design in applications such as displays, much higher operating voltages are required [4][5] and it is also necessary to be able to design transistors with different channel lengths.

Therefore, this work demonstrates the fabrication of ZnO nanowire field-effect transistors (NW-FET) using top-down approach starting with thin film deposition in Remote Plasma Enhanced ALD (PEALD) and anisotropic reactive ion etch (RIE) to produce nanowires with controlled channel lengths and dimensions. This chapter will start with the Remote PEALD deposition technique followed by NW-FET device fabrication process and finally the electrical characteristics of these devices.

4.2 Remote PEALD of ZnO thin film

ALD of ZnO is a process that has shown great potential to deposit conformal and high quality film. The technique is cyclic, based on two self limiting reactions: 1) metallization and 2) oxidation. These reactions are separately executed on a substrate surface. Diethyl Zinc, DEZ is used as the Zn metal precursor. During metallization, DEZ adsorbs to the substrate surface. Subsequently, the absorbed DEZ are reacted with an oxidant in the oxidation step. Usually the oxidant is water which is widely known as thermal ALD. To assure both reactions are executed separately, pump and purge steps are implemented between the metallization and oxidation step. In each ALD cycle, the surface is ideally left with one monolayer of ZnO. The ALD process of ZnO using water as an oxidant has already been extensively studied and can be considered as a model system for ALD [6 - 9].

Recently, plasma assisted ALD method has been explored [10 – 19] and it is found that the use of plasma species as reactants allow more freedom in processing conditions and wider range of material properties compared with the conventional thermal ALD. The use of plasma also significantly reduced the OH impurity which affect the conductivity of the semiconductor film and induce defects in dielectric materials [20]. In the advent of this, remote plasma enhanced ALD (PEALD) has been widely reported to form high quality dielectric films, particularly for high-k dielectric materials [18], [19], [21]. Very few have reported using remote PEALD for semiconductor layer especially ZnO film [10], [11]. In this work, we study the remote PEALD process to deposit semiconducting and high quality ZnO layer for electronic device applications. Series of experiments were conducted to investigate the effect of plasma parameters on the film quality, investigate the growth rate and study the deposition temperature effect on the film quality.

Fig. 4.1.FlexAl Atomic Layer Deposition Tool from Oxford Instruments.

The deposition of ZnO film was carried out in Oxford instrument's "FlexAL" deposition tool shown in Fig. 4.1. DEZ (Zn $(C_2H_5)_2$) was used as the Zn metal precursor. During metallization cycle, DEZ was injected into the reactor at 30 ms and Zn $(C_2H_5)_2$ was chemisorbed to the substrate surface. After reaching saturation, residual Zn $(C_2H_5)_2$ and reaction products were removed by Ar purge. Subsequently, the - C_2H_5 ligands of the chemisorbed Zn $(C_2H_5)_2$ species were removed by a reaction with oxidant in the oxidation step. In this work, oxygen radicals were created by an inductively coupled plasma source. The O_2 flow was kept constant at 60 sccm during this cycle. To ensure only one reactant was present in the ALD chamber at a given time, oxygen was purged using Ar for 4s before the next DEZ injection into the chamber. This constitutes one cycle and the substrate surface was ideally left with one monolayer of ZnO. Remote plasma ALD combines a high reactivity with low ion energy, typically below the threshold energy for plasma damage. Fig. 4.2 shows 1 cycle of remote PEALD process.

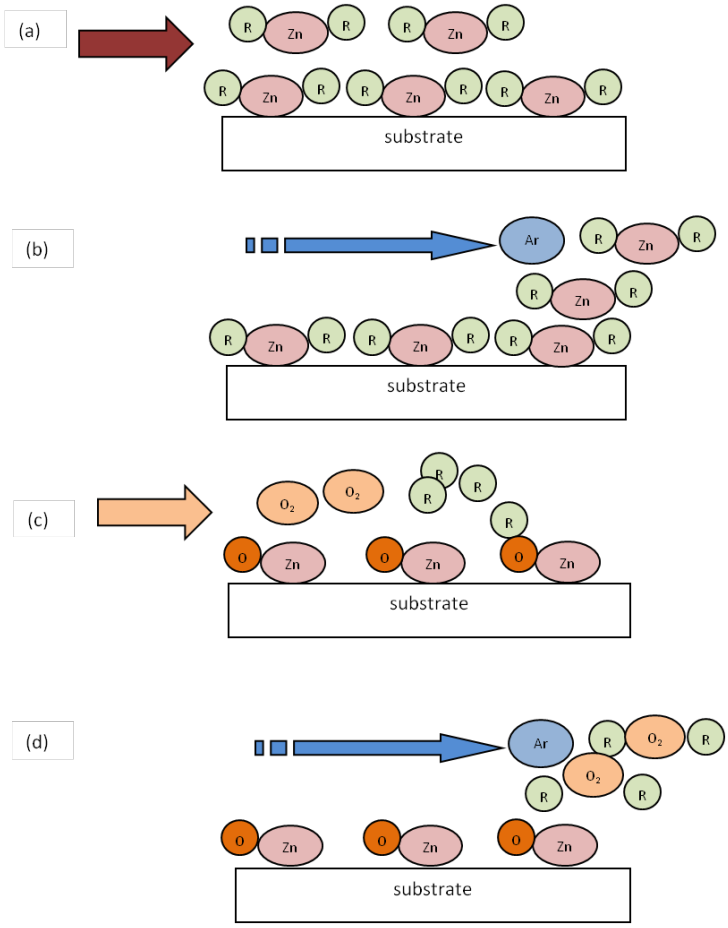


Fig. 4.2.Illustration of one ALD ZnO film reaction cycle.

4.2.1 Experiment

Design of Experiment (DOE) was used to study the impact of the oxygen plasma parameters such as the RF power, pressure and plasma time to realize semiconductor quality of ZnO thin film. DOE is a structured and organized method for statistically analyzing the relationships among factors affecting the process outputs. Reference [22] provides details on the DOE methodology. The Box-Behnken design [22] was used in the DOE that includes 3 design points for all the plasma parameters that represent the experimental run to be conducted in the ALD. The 3 design points were RF power at 100, 250 and 400W, plasma pressure at 15, 57.5 and 100 mTorr and plasma time at 2, 6 and 10s. These parameters were varied simultaneously rather than one at a time which allows for the study of interactions between the factors.

ZnO films were prepared on 200 nm SiO_2/p-Si substrate. The Si wafers with 200 nm thick thermally grown SiO_2 were cleaned in acetone and IPA ultrasonically for 1 min, respectively. The samples were immediately loaded into the reactor and ALD process was performed based on DOE technique. The deposited films were then characterized in X-ray photoemission

spectroscopy (XPS) for surface material composition. The Hall mobility and resistivity of the ZnO films were measured by Hall-effect measurements using the four-probe approach at a magnetic field of 0.5 T. For this test, a quartz substrate was used to avoid any conductivity effect from the substrate.

4.2.2 Results and Discussion

XPS was used to evaluate the content of ZnO film processed with different plasma parameters in the remote PEALD. This is an important technique to study the effect of plasma parameters alone on the film quality since the DEZ dose cycle was kept constant. Fig. 4.3 shows the XPS spectrum obtained from a ZnO film processed at a plasma power of 100 W, plasma pressure of 57.5 mTorr and plasma exposure time of 2s. The O1s and the $Zn2p_{3/2}$ peaks were observed at about 531 eV and 1022 eV, respectively.

The stoichiometry was determined from the ratio of the atomic percentages of the $Zn2p_{3/2}$ and O1s photoelectron peaks [23]. The C1s peak which is the carbon impurity appeared at 285 eV for all samples deposited. From this peak, the carbon impurity content present in the ZnO films has been analyzed. The presence of carbon impurity in the ZnO film is due to the unreacted or by-product of the metal-organic precursor source. The carbon impurity can induce defect states in ZnO. Meanwhile, the four probes Hall measurements give indication of the semiconducting properties of the deposited ZnO films from the Hall mobility and resistivity, which are vital properties for typical thin film transistor (TFT) applications.

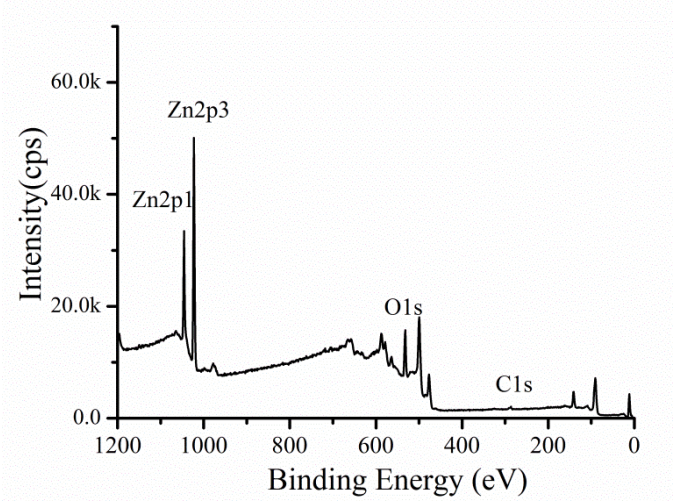


Fig. 4.3. XPS spectrum of ZnO film deposited with 2s oxygen plasma time in the PEALD

TABLE 4.1: DOE generated with results obtained in the XPS and Hall measurements

RF Power [W]	Plasma Time [s]	Pressure [mTorr]	Zn/O	C1s	Hall Mobility [cm2/Vs]	Resistivity [Ω.cm]
100	10	57.5	0.76	37.35	1.06	3.9
250	6	57.5	0.89	21.25	1.01	1.84
250	10	100	0.82	32.79	3.31	2.78
250	6	57.5	0.89	21.25	3.84	0.22
250	2	15	0.79	32.08	9.8	0.33
400	6	15	0.94	16.77	0.55	32.77
400	6	100	0.91	17.92	2.76	6.14
100	6	100	0.97	13.91	1.00	5.36
100	6	15	0.89	23.44	0.9	24.67
100	2	57.5	0.95	12.33	3.69	0.29
250	2	100	0.96	12.5	3.57	0.17
250	6	57.5	0.89	20.62	3.84	0.22
400	2	57.5	0.93	19.01	2.21	0.82
400	10	57.5	0.88	16.55	2.02	11.36
250	10	15	0.93	25.8	0.79	47.53

Table 4.1 shows the first design of experiment generated in Minitab. The RF power, plasma time and the pressure were varied randomly from 100 to 400W, 2 to 10s and 15 to 100 mTorr, respectively. All other factors such as temperature (150^{o}C), DEZ dose time (30 ms), oxygen flow (60 sccm), Ar purge (100 sccm) and number of cycles (500) were set to be constant.Fig. 4.4 shows the contour plots of all four responses from the DOE model. These responses include the Zn/O ratio, the carbon impurity, Hall mobility and resistivity of the ZnO film. These contour plots were used to extract the ZnO film surface and electrical information and finally the desired operating conditions.

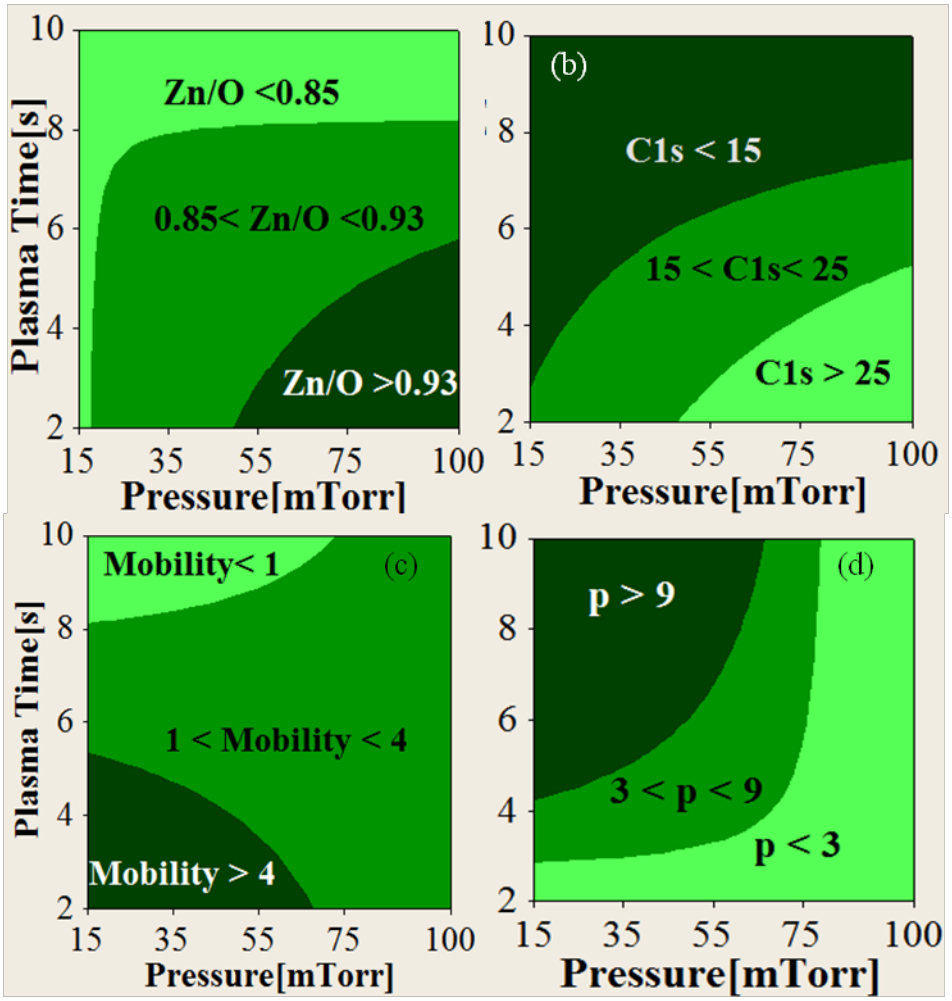


Fig. 4.4. Generated contour plot of (a) Zn/O ratio, (b) carbon impurity in %, (c) Hall mobility in cm^2/Vs and (d) resistivity in Ω.cm when plasma time and plasma pressure were varied at constant plasma power of 100 W [24]

The contour plot was used to give two plasma factors and the plasma power was fixed at 100 W. In Fig. 4.4(a), it was observed the Zn and O compositions changed as the plasma time and pressure being varied. The ZnO films became oxygen rich at plasma times greater than 8 s regardless of the plasma pressure. This is due to an insufficient Ar purge after the long exposure of the oxygen plasma. There could be some oxygen ion residue left which bound loosely onto the surface of the ZnO film resulting in a highly oxygen rich film.

Interestingly, Fig. 4.4(b) indicates that there was a low presence of carbon impurity at < 15 at. % when plasma pressure was lower. However, it is still considered high compared with other ALD ZnO films [7] [8]. The carbon content can be further reduced by optimizing the DEZ dose time. This carbon content originated from the incomplete decomposition of DEZ . Higher oxygen plasma and low pressure generally increases the carbon impurity. This increase was due to the insufficient Ar purge, which leads to the simultaneous presence of both precursors in the gas phase near the substrate which can result in chemical vapour deposition (CVD) type growth. CVD growth reactions can lead to particle formation such as carbon impurity which degrades

device performance [19]. This result agrees well with the observed electrical properties from the Hall measurements. Figure 4.4(c) and (d) show mobilities and resistivities of RPALD ZnO films as a function of plasma time and pressure at constant plasma power at 100 W. For longer plasma exposure time, the Hall mobility of the ZnO film is reduced to < 1 cm^2/Vs. During this time, the ZnO films consistently demonstrate an elevated film resistivity which was due to carbon impurity. As a result, the carrier scattering increases and reduces the mobility of the film.

Based on these findings, a good quality stoichiometric ZnO thin film with low carbon impurity, resistivity and high mobility can be achieved with a plasma power of 100 W, plasma pressure of less than 57.5 mTorr and plasma exposure of less than 4s. With this optimized condition, a ZnO thin film was deposited at 1s plasma exposure time. The measured carbon impurity was about 11 %.at and Zn/O ratio was 1.02. This indicates that a low plasma exposure time during remote PEALD, can produce a stoichiometric film with low carbon impurity.

4.2.3 Summary

A ZnO thin film with controlled semiconductor properties was successfully deposited by remote PEALD from this DOE method. Film stoichiometry was reduced and carbon impurity content was increased by long oxygen plasma exposure time and very low plasma pressure. The results show film resistivity and carrier mobility were affected by the presence of the carbon impurity. Finally, remote PEALD process has a great potential in producing semiconductor quality metal-oxide film.

4.3 Fabrication of Top-Down ZnO Nanowire Transistors using Remote PEALD

With the optimized remote PEALD conditions discussed previously, top-down ZnO nanowires were fabricated using mature >1 μm photolithography and anisotropic reactive ion etching (RIE) to produce nanowires. Nanowire FETs with different channel lengths were fabricated and well-behaved electrical characteristics were obtained, with excellent values of breakdown voltage.

4.3.1 Device Fabrication

Fig.4.5 shows the fabrication process steps. The process starts with a p-type Si wafer. The wafer was cleaned in fuming nitric acid for 15 mins and dipped in a hydrofluoric acid before a layer of SiO_2 was thermally grown by wet oxidation. The SiO_2 was then etched anisotropically by photolithography pattern transfer and reactive ion etching (RIE). The etched depth was 100

nm. The SiO_2 etch was executed in CHF_3 and Ar mixture at a pressure of 30 mTorr. Figure 4.5(b) shows the SiO_2 trench formed after the RIE etch. A 35 nm layer of ZnO film was deposited on top of the trenches (Fig.4.5(c)). The ZnO film was deposited using the remote PEALD using DEZ precursor with oxygen plasma time of 4s, an RF power of 100 W, a pressure of 57.5 mTorr and an O_2 flow 60 sccm. After deposition, the films were etched in anisotropic reactive ion CHF_3 etch to form nanowires at the sides of the SiO_2 pillars as illustrated in Fig 4.5 (d).

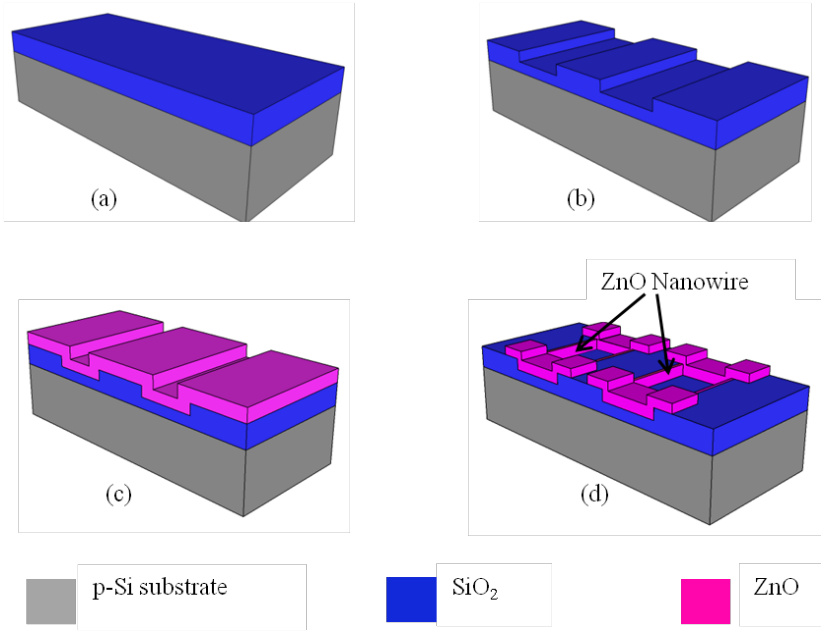
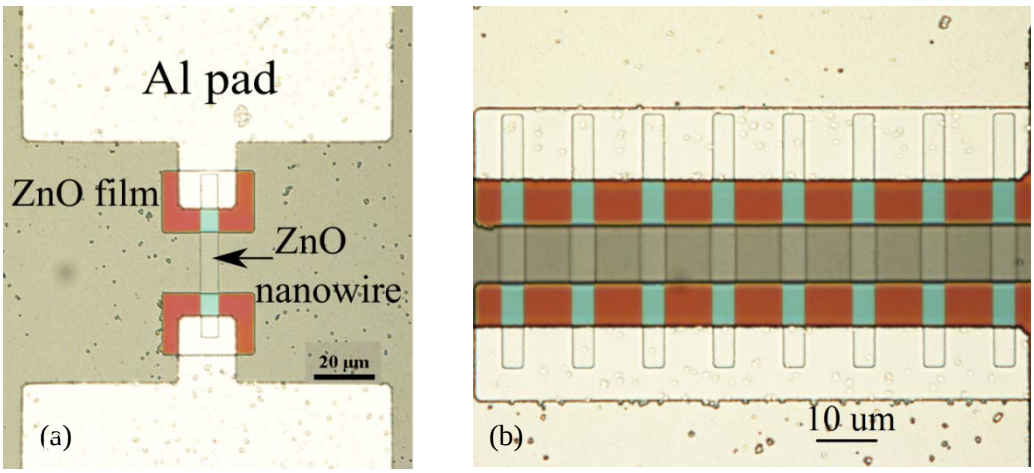


Fig.4.5 Top-down fabrication process of ZnO NW-FET (a) SiO_2 thermally grown through wet oxidation ~200nm (b) SiO_2 dry etched in the RIE to form 100 nm trench (c) ZnO thin film deposited in the PEALD (d) Anisotropic RIE etch to obtain nanowires at the side of the oxide trenches.

Aluminum source and drain contacts were evaporated and lifted off in NMP solution. The contacts were annealed in Rapid Thermal Annealer (RTA) for 2 mins at 350^{o}C to improve the ohmic contact [25]. Al is used because it was known to form good Ohmic contacts with ZnO because it has a work function, Φ_{AL} of 4.28 eV which is close the electron affinity of ZnO, χ_{ZnO} of 4.29 eV. It is also found that Al has better surface quality with ZnO than Ti which can reduce surface states [26]. Optical microscope and cross-sectional SEM images were used to observe the fabricated nanowires. In addition, Raman spectroscopy with laser source of 532 nm was used to detect the presence of ZnO nanowires at the sides of the SiO_2 spacers. Finally the electrical characteristics of the NW-FETs were measured in dark, room ambient in HP 4155C Parameter Analyzer.



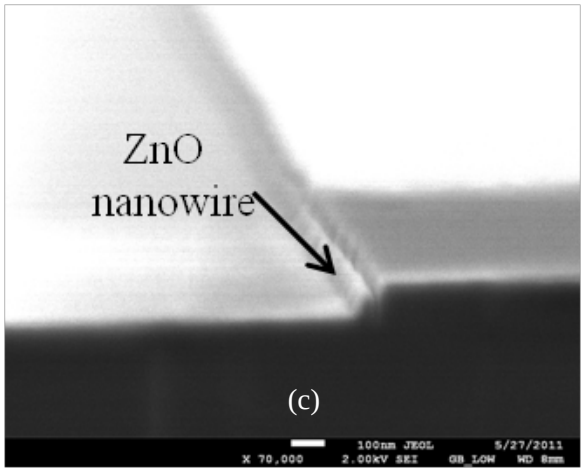


Fig.4.6 (a) Optical microscope view of a pair of ZnO nanowire in contact with Al pad (b) Optical image of 16 nanowire array contacted with Al pad (c) Cross-section of a single ZnO nanowire after RIE etch [27]

4.3.2 Results

The fabricated nanowire device structure with Al pad is shown in the optical microscopy image in Fig. 4.6(a). The nanowires fabricated have length range from 2 μm to 20 μm. The width and height of the ZnO nanowires were 40 nm and 80 nm, respectively. These dimensions can be controlled by adjusting the thickness of the ZnO layer and the height of the SiO_2 trench. Fig. 4.6(b) shows 16 identical wires across the two Al electrodes demonstrating ZnO nanowire arrays were successfully formed at the side of the oxide spacers. Figure 4.6(c) shows single nanowire using Field-Emission SEM (FESEM) after the RIE etch. The nanowire height was approximately 80 nm and was determined by the height of the SiO_2 pillar and the amount of over-etch of the ZnO layer (by 20% in this case). The nanowire width was

approximately 40 nm at the base, which was 14% thicker compared to the 35 nm ZnO film deposited. This discrepancy will be discussed later.

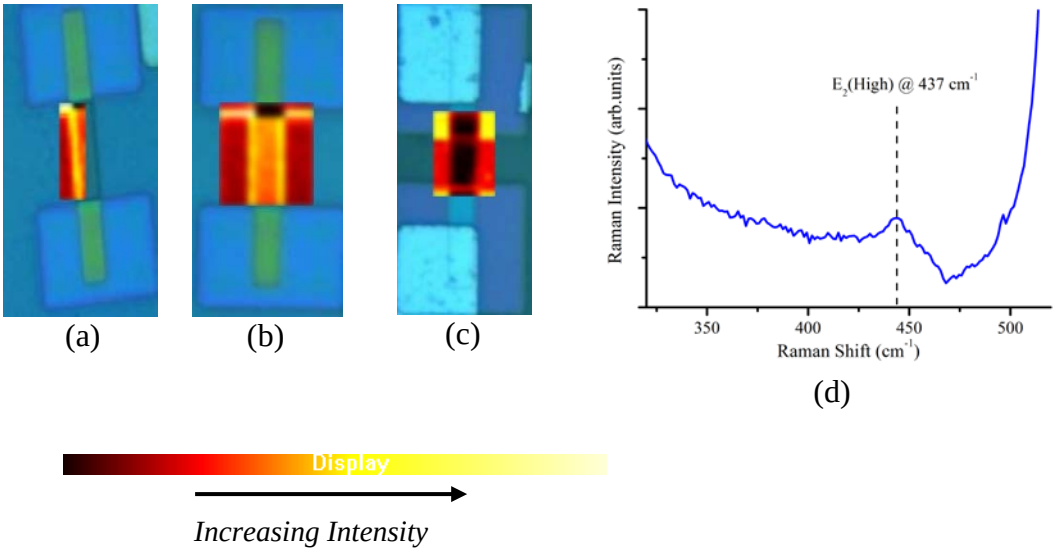


Fig.4.7 Raman image mapping at E_2 phonon mode (a) Sample 1 (b) Sample 2 (c) Sample 3 (d) Raman spectra obtained from one of the mapped point along ZnO nanowire device [25]

Fig.4.7 shows the results from Raman mapping of the ZnO nanowires at the side of the oxide trenches. Fig. 4.7(a) shows a bright yellow region, indicating the presence of ZnO and this was verified by the Raman spectrum shown in Fig.4.7 (d). If the incident light was exactly normal to the surface, only the E_2 phonon modes and the A_1(LO) phonon mode can be observed in ZnO [5]. The peaks at 437 cm^{-1} should be assigned to the vibration modes of E_2. The E_2 mode was related to band characteristics of the wurtzite phase, and it can be shifted due to residual stress in the nanowire. Figure 4.7(a) of Sample 1 and Figure 4.7 (b) of Sample 2 show high intensity (yellow) at the side of the oxide trench, which indicate the existence of ZnO nanowires. Meanwhile Figure 4.8(c) of Sample 3 does not show peaks at the E_2 mode near the oxide trench which suggests that the ZnO film has been etched completely.

Fig. 4.8 shows the output I_D-V_D characteristic of a ZnO nanowire FET with two parallel nanowires and a channel length L = 8.6 μm measured in the dark at room temperature. The transistor operates in the n-type enhancement mode and the output characteristics show a well-defined linear region at low bias and excellent saturation at higher bias, indicating clear pinch-off behaviour. A breakdown voltage of 75 V was obtained at V_G = 0 V and I_D = 5 nA.

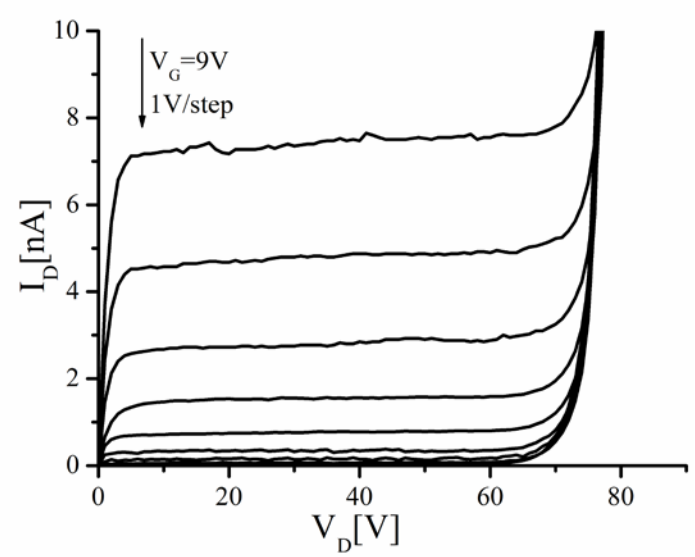


Fig.4.8 The output characteristics of a ZnO nanowire FET comprising two parallel nanowires with length of , L=8.6 μm [27]

To test the scalability of the top-down ZnO nanowire process, Fig. 4.9 shows results for nanowire FETs with channel lengths of 1.3, 8.6 and 18.6 μm. Well - behaved output characteristics were obtained at all channel lengths, with clearly defined linear and saturation regions. The poor saturation seen in Fig. 4.10 (a) for the 1.3 μm transistor suggests the presence of short-channel effects. Similar behaviour has been observed in short-channel ZnO thin film transistors[28]. In addition, the source and drain contacts with 1.3 μm channel length device behaves like Schottky contacts as observed from the output characteristics.

At V_G = 10 V and V_D = 5 V, drain currents of 110 and 8.8 nA were obtained for L=1.3 and 18.6 μm, respectively. This factor of 12.4 difference in drain current was consistent with the expected value of 14.3 obtained from the 1/L scaling behavior of long-channel FETs [29]. Breakdown voltages of 79 and 78 V were measured for channel lengths of 1.3 and 18.6 μm respectively.

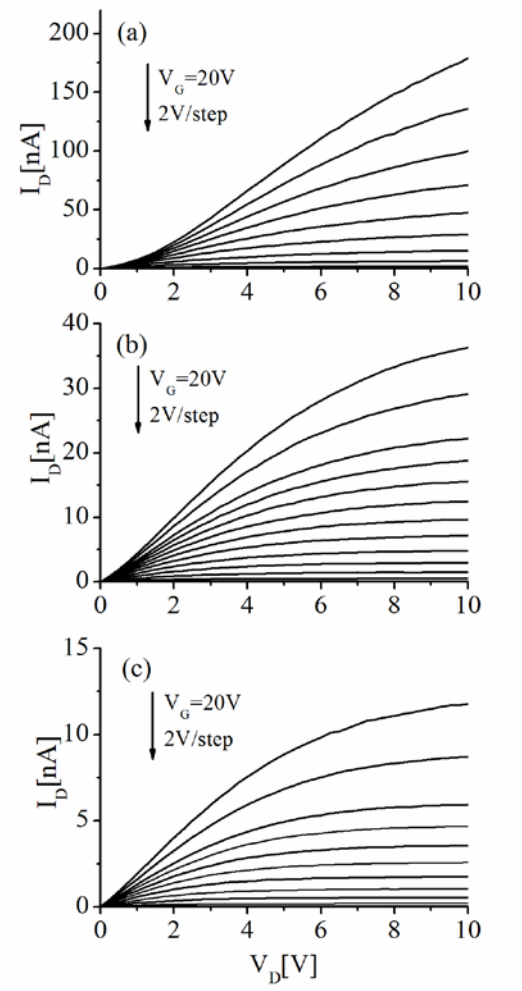


Fig.4.9 Output characteristics of ZnO nanowire FET comprising two parallel nanowires with channel lengths L of (a) 1.3 μm (b) 8.6 μm (c) 18.6 μm [27]

To test the reproducibility of the fabrication process, Fig.4.10 shows the transfer characteristic of a device with 16 parallel nanowires. This device has a drain current of 35.7 nA at V_D=5 V and V_G=10 V, which compares with a drain current of 4.3 nA for the transistor with two parallel nanowires. The × 8.3 difference in current demonstrates that the drain current scales in a reproducible way.

Fig.4.10 also shows sub-threshold characteristics for nanowire FETs with different channel lengths at V_D=5 V. Sub-threshold slopes of 1.02, 0.69, and 0.9 V/dec are obtained for transistors with channel lengths of 1.3, 8.6, and 18.6 μm, respectively. The poor value of sub-threshold slope for the 1.3 μm device can be explained by short-channel effects due to poor control of the channel by the gate as a result of the thick gate oxide. The 8.6 μm transistor shows a respectable I_{ON}/I_{OFF} ratio of 2×10^6, measured between V_G = 20 V and 3 V.

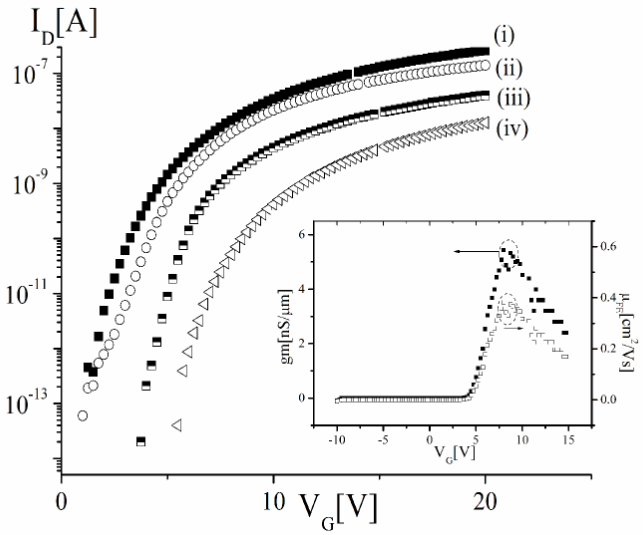


Fig.4.10 Transfer characteristics for devices with different channel lengths and different numbers of parallel nanowires; (i) 16 nanowire FET with L=8.6 μm (ii) 2 nanowire FET with L=1.3μm (iii) 2 nanowire FET with L=8.6 μm and (iv) 2 nanowire FET with L=18.6 μm. The inset shows the transconductance (g_m) and field-effect mobility (μ_{FE}) as a function of gate bias at V_D = 5V for L=8.6 μm plot [27].

4.3.3 Discussion

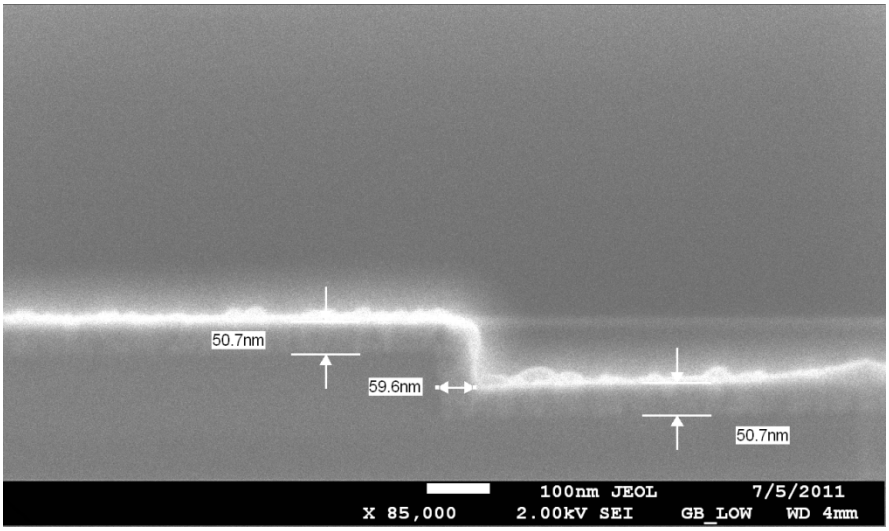


Fig.4.11 A ZnO layer after PEALD deposition

From the ellipsometer measurements, the thickness of the ZnO layer grown in remote PEALD was 35 nm. The nanowire width at the base was measured to be around 40 nm, which was closer to the thickness after the deposition. The small discrepancy in the thickness could be due to the non-conformal deposition of the ZnO ALD. Fig.4.11 shows an SEM image after ZnO deposition in remote PEALD for a different sample. As can be seen, the thickness on the pillar sidewall was about 17.5% thicker than on the planar surfaces thus contributing to the small

discrepancy in the nanowire width measurement. It should be noted that the ZnO thickness after deposition was measured using ellipsometry, so there may be a systematic error between these two measurement techniques.

The transistor operation up to a voltage of 75 V shown in Fig.4.8 was significantly better than the 3 V operation reported by Park *et al* [30] and the 1.5 V operation reported by Cha *et al* [31]for ZnO nanowire transistors fabricated by bottom-up self-assembly. This high operating voltage in small dimension nanowire devices indicates the suitability of this device for applications such as high resolution flat panel displays [4][5], which require a supply voltage of 15-20 V. This was the first demonstration of high voltage operation for ZnO nanowire transistors. The output characteristics obtained with our process were also significantly better behaved than those reported for ZnO nanowire transistors fabricated by bottom-up self-assembly. These devices tend to show either a lack of saturation or very poor saturation [30][31]. Furthermore, the use of a top-down fabrication technique has enabled the fabrication of nanowire transistors with different channel lengths, thereby demonstrating the suitability of this approach for circuit design in applications such as display electronics. The realization of transistors with different channel lengths in bottom-up processes would be much more difficult to achieve.

The field-effect mobility, μ_{FE} can be calculated from the peak transconductance g_m given in the inset of Fig.4.10, following the method in Ref [30] . An electron mobility of 0.5 cm^2/Vs was obtained for L = 8.6 μm device, which is consistent with the range of values from 0.3 to 17 cm^2/Vs reported for thin film ZnO transistors fabricated using ALD[7][9][12][16][32 - 34]. A mobility towards the bottom end of this range might be expected for these nanowire FETs due to roughness from the nanowire reactive ion etch, which has not been optimized. To test this possibility, the mobility was measured on thin film transistors (TFT) on the same wafer as the nanowire transistors with the same deposition process. A mobility of 1.0 cm^2/Vs was obtained, which was higher than the value obtained on nanowire transistors. This result suggests that there is considerable scope to improve the mobility of the nanowire FETs by optimizing the ZnO ALD process and dry etch process.

Reported values of mobility for bottom-up ZnO nanowire FETs show a wide variation, with values ranging from 0.53 [35] to 3118 [36] cm^2/Vs. This very high value of mobility was obtained on passivated nanowires and much lower values of 10 to 80 cm^2/Vs were obtained on unpassivated nanowires. A similar improvement in mobility from 75 to 1000 $cm^{2/}Vs$ was reported by Park *et al* when their nanowires were passivated with polymer [30]. It is likely, therefore, that much higher values of mobility could be achieved in these ZnO nanowire FETs by using a passivation layer.

A simple comparison with theory was done based on Eq.(4.1) which shows a typical MOSFET device operating in saturation region.

$$I_{\mathrm{D}} = W\frac{C_{\mathrm{ins}}}{2}\mu_{\mathrm{FE}}\frac{(V_{\mathrm{G}} - V_{\mathrm{TH}})^2}{L} \qquad (4.1)$$

where W is the nanowire width, C_{ins} is the gate capacitance per unit area and L is the channel length.

The measured I_D values were compared with calculated values to obtain a better understanding of the nanowire FET transistor operation. From the plots in Fig. 4.12, it was shown for channel length of 8.6 μm and 18. 6μm, the transistor current matches very well with the calculated values. This shows the reliability of this device operation without the influence of other issues such as series resistances, short channel effects *etc*.

However, for L = 1.3 μm, the measured current is higher from the theoretical prediction. As can be observed in Fig. 4.10, the subthreshold slope is poor for this channel length due to thick gate oxide. Due to poor control of the gate on the channel, the drain current increases rapidly thus the discrepancy with calculated values.

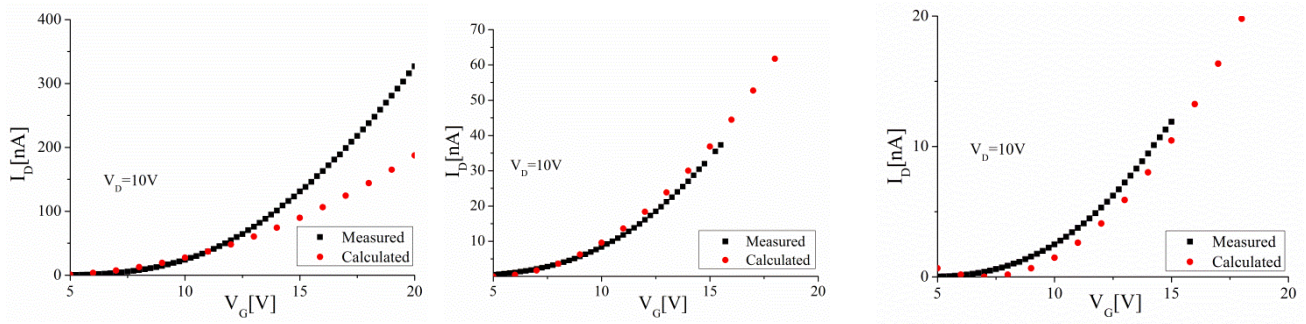


Fig.4.12 I_D comparison between measured and calculated values for (a) L = 1.3 μm (b) 8.6 μm (c) 18.6 μm.

4.3.4 Summary

In conclusion, the top-down fabrication of ZnO nanowire FETs using remote plasma ALD and anisotropic reactive ion etching was successfully demonstrated. Transistors with channel lengths in the range 18.6 to 1.3 μm have been fabricated and a breakdown voltage of $\geq$ 75 V has been achieved at all channel lengths which is ample for applications such as active-matrix display electronics. Well-behaved electrical characteristics were obtained and the drain current scales as 1/L, as expected for long-channel FETs. The current conduction also agrees well with typical MOSFET theory for long channel devices.

4.4 Conclusions

In this work, it was successfully demonstrated that a semiconductor quality ZnO thin film was deposited by remote PEALD. A systematic DOE method was used to study the effects of oxygen plasma parameters interactions on the film composition and electrical properties. Based on these findings, a good quality stoichiometric ZnO thin film with low carbon impurity, resistivity and high mobility can be achieved at plasma power of 100 W, plasma pressure of less than 57.5 mTorr and plasma exposure of less than 4s. With this optimized condition, ZnO nanowires from top-down were then fabricated using remote plasma ALD at plasma exposure of 4s and anisotropic reactive ion etch. Transistors with channel lengths in the range 18.6 to 1.3 μm have been fabricated and a breakdown voltage of ≥ 75 V was achieved at all channel lengths which is ample for applications such as active-matrix display electronics. Well-behaved electrical characteristics were obtained and the drain current scales as 1/L in agreement with theory calculations, as expected for long-channel FETs.

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Chapter 5

Technology Optimization

5.1 Introduction

The exceptional thickness control and conformality of ALD has made it the process of choice for numerous applications from microelectronics to nanotechnology. Its benefits derive from the self-limiting character of surface chemical processes (adsorption and chemical reaction) that occur upon saturation of the active sites present on the surface. Apart from ALD depositions, dry etch technology is preferred in this top-down process due to the anisotropic etching which produced well controlled nanowires.

However, identifying a suitable process window in which deposition and etching benefits can be a challenge. The preliminary results of plasma enhanced ALD deposition (PEALD) and RIE etch process exhibit ZnO NWFETs with the highest mobility of 0.5 cm^2/Vs. From this early ALD deposition technology, the growth per cycle (GPC) was less than 1 angstrom per cycle. The low GPC and low field-effect mobility garnered the need to optimize the deposition and etching techniques in order to improve the film properties and transistor characteristics. This section is started with process optimization on dry etch before discussing various experiments conducted in order to optimize the PE-ALD deposition process.

5.2 Effect of ZnO Dry Etch Techniques

5.2.1 Introduction

Etching of ZnO films plays an important role in producing high conductivity ZnO nanowire FETs. Since these nanowires are not covered by the photoresist, they are prone to be bombarded by plasma ions and radicals from the etching gas. Thus it is important to monitor the

various etching methods on ZnO film. Table 5.1 shows a review of how ZnO can be etched using various dry etch equipment. All results shown are based at room temperature etching. Since nanowires are formed from anisotropic etching, only dry etch techniques have been considered.

Basically, the mechanism of all these techniques is the same, which is utilizing the plasma to etch the material. RIE etch is typically performed at 10-100 mTorr pressure in a parallel plate reactor and is highly anisotropic. The ion density is in the range of 10^{10} to 10^{11} cm^{-3}[1].In comparison, Electron Cyclotron Resonance Plasma (ECR) also produces high anisotropic etch with lower gas pressures of 0.2-10 mTorr and the etch rate is faster than in RIE. This is due to higher ion density (up to 10^{12} cm^{-3}). However, ECR technology is expensive and the etch uniformity is not good due to the presence of a magnetic field. The ICP tool provides the same advantage as ECR *i.e.* low pressure (1 mTorr), and higher etch rate because of a high ion density. In ICP, the ion flux is controlled by the ICP power and the gas pressure while the ion energy is controlled by the RF power of the substrate holder.

TABLE 5.1 ZnO etch overview from previous work.

Machine	Power (W)	Gas	Pressure (mTorr)	Etch Rate (nm/min)	Mask	Ref
Reactive Ion Etcher (RIE)	200	CHF_3	20	5	Cr	Schuler *et al* [2]
Electron-cyclotron-resonance plasma (ECR)	80	CF_4+CH_4	0.075	55	Resist	K.Ogata *et al*[3]
Inductive Coupled Plasma (ICP)	RF = 150 ICP =300	Ar/Cl_2 Ar/CH_4	5	15	SiNx	W..Lim *et al* [4]
Inductive Coupled Plasma (ICP)	RF = 400 ICP =800	CF_4/Ar	15	45.2	-	J.C.Woo *et al*[5]

5.2.2 RIE Etch of ZnO

Based on this review, the initial experiment of this work was executed by reactive ion etch in CHF_3 gas flow. ZnO films were deposited in Filtered Cathodic Vacuum Arc (FCVA) at The McDiarmid Institute for Advanced Materials and Nanotechnology in New Zealand for this etching experiment. The mask used was a positive resist. The CHF_3 gas flow used was 25 sccm with a pressure of 20 mTorr following Schuler *et al*[2]. The RF power was varied at 100 W, 150 W and 200 W. The etch rates were measured by ellipsometry. Note that the mask is used for the thin film area and not for the nanowire.

Fig. 5.1shows the etch rate of ZnO films with increasing RF power. Higher power led to higher etch rate as well as higher selectivity towards the underlying SiO_2 film. However, the selectivity towards the photoresist mask was not good (< 1). The etch rate was highest at 1.64 nm/min for RF power of 200 W, followed by 0.72 nm/min and 0.3 nm/min for RF power of 150 W and 100 W, respectively.

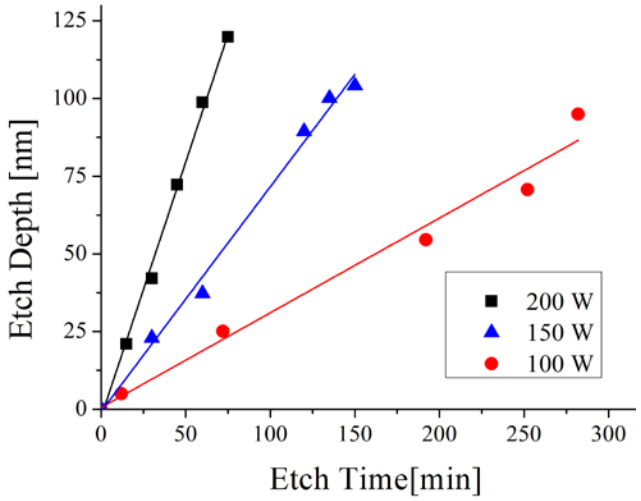


Fig 5.1 The etch rate of ZnO film with pressure =20 mTorr and CHF_3=25 sccm.[6]

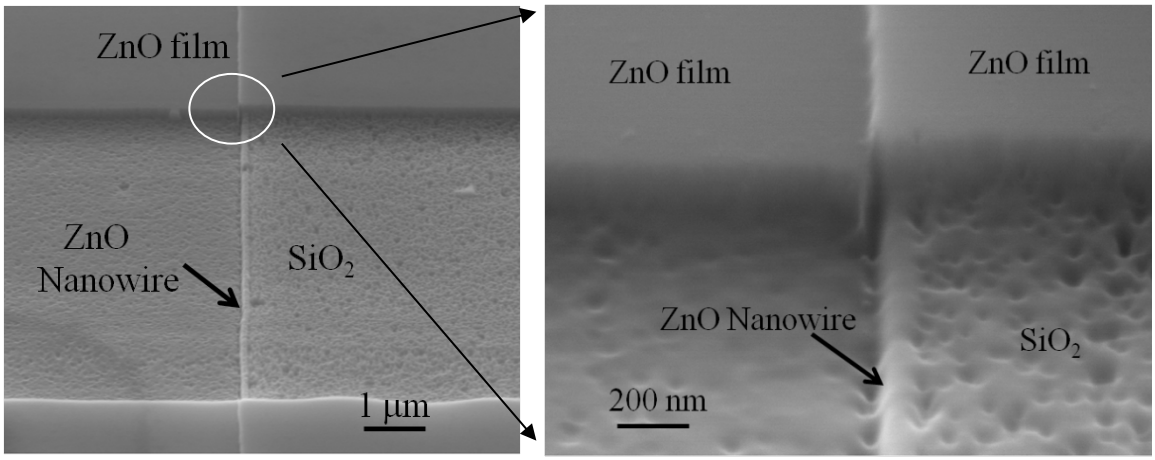


Fig 5.2: (a) Planar SEM image of top-down fabricated ZnO nanowire after RIE etch (b) Enlarged view of the circled area.

Fig. 5.2 shows the SEM images of top-down fabricated ZnO nanowires in planar view after the RIE etch. The nanowires were formed at the side of the SiO_2 pillar. However from the enlarged view of part of the etched nanowire shown in Fig.5.2 (b), it is clear that the nanowire had a rough surface after the etch. In addition, the SiO_2 surface left after the RIE etch was also rough due to prolonged ion bombardment.

In general, the etch rate was very slow in RIE etch. Due to prolonged exposure to ion bombardment, the nanowires obtained from RIE etch developed high surface roughness. Therefore, there is a need to develop a better dry etch technique which exhibits higher etch rate and less surface roughness.

5.2.3 ICP Etch of ZnO

a) Experiment

In this experiment, ZnO films were deposited in Plasma Enhanced ALD (PEALD) with DEZ dose of 30 ms, O_2 plasma time of 4s and temperature of 150^{o}C. The films were patterned with photoresist and etched in ICP with various CHF_3/Ar gas flow rates. However, the total gas flow rates, RF power and ICP power were fixed at 25 sccm, 300 W and 1000 W, respectively with a pressure of 10 mTorr. The etch rates and the selectivity were measured using surface profiler and ellipsometer. The selectivity is measured by measuring the ratio of the etch rate of ZnO film against the etch rate of the photoresist on the same sample as shown below.

$$Selectivity = \frac{ZnO\ Etch\ Rate}{Photoresist\ Etch\ Rate}$$

Nanowire profiles were also measured by Atomic Force Microscopy, AFM.

b) Results and Discussion

Fig. 5.3 shows the etch rate of ZnO in ICP and selectivity over the photoresist mask as CHF_3 gas concentration was increased from 0 to 100%. The etch rate of ZnO at 100% Ar was 19.51nm/min. With further increase of CHF_3 content, the etch rate of ZnO increases and is maintained at about 50 nm/min. The selectivity of ZnO to the photoresist shows an increase from 0.05 at 100% Ar to 0.353 at 40% of CHF_3 and reduced to 0.26 at 100% of CHF_3. At 100% Ar, the etching is considered as purely physical and is also known as Ar sputtering. It lacks selectivity among different materials because the ion energy required to eject the surface atoms is very large compared to the surface bond energies. Thus the etch rate is low. At 100% CHF_3, it is considered as purely chemical and etching in this manner need to be carefully monitored as it could be etching isotropically.

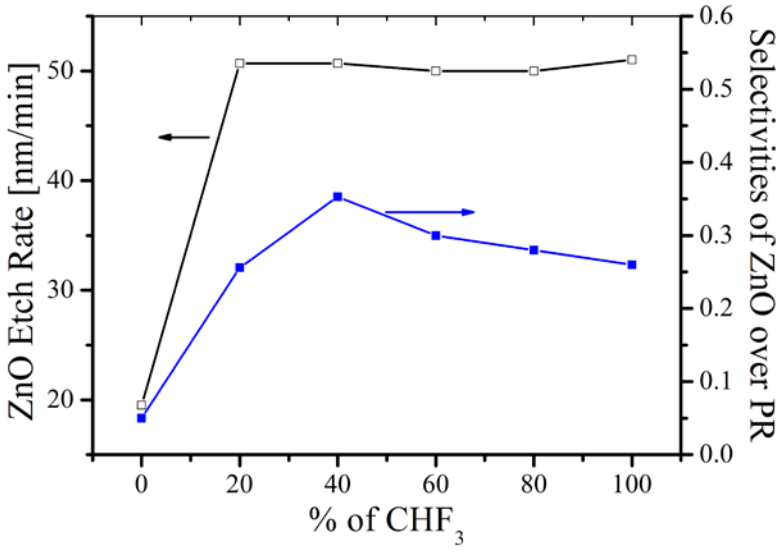
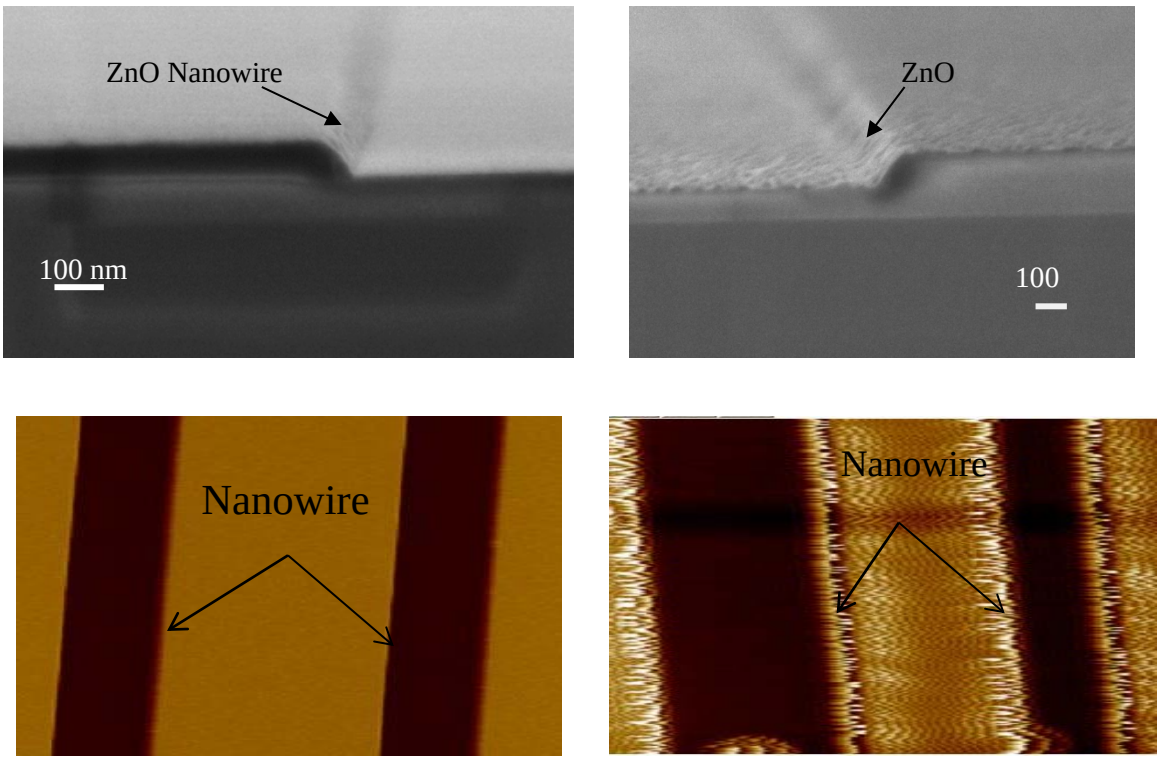


Fig. 5.3 ICP Etch rate and selectivities of ZnO film as a function of CHF_3/Ar ratios. All the films were deposited in PEALD with DEZ dose of 30 ms, O_2 plasma time of 4s and temperature of 150°C.



(a) (b)

Fig. 5.4 Cross-sectional SEM and top-view of AFM image of ZnO nanowire etched in ICP with (a) 100% CHF_3 (b) 20% of CHF_3 and 80% Ar gas flow.

Fig. 5.4 shows the SEM and AFM image of the ZnO nanowire after the ICP etch. The AFM image was measured across a 35 μm x 35 μm surface area on the sample. Fig. 5.4 (a) shows the ZnO nanowire formed after 1min ICP etch with only CHF_3 while Fig. 5.4 (b) shows the ZnO nanowire forming at the SiO_2 pillar with 20% of CHF_3 gas and 80% of Argon gas flow. Etching in pure CHF_3 produces a smoother surface compared with Ar assisted etch as shown. Smoother nanowires are desirable for fabricating top - down ZnO NWFETs.

In summary the etch rate increased by 30 x from 1.64 nm/min in RIE to 50 nm/min in ICP. It was also found that etching in pure CHF_3 chemistry without Ar ions produced smoother nanowires at the edge of the SiO_2 pillars which are desirable for fabricating top down ZnO NWFETs.

5.3 Effect of RIE and ICP Etch on ZnO NWFETs

5.3.1 Experiment

In order to investigate the effect of RIE and ICP etch on the performance of ZnO NW FETs, two samples from the same batch PEALD deposited ZnO films were prepared on SiO_2/p-Si substrates. The highly doped p-Si substrate acted both as the substrate and gate. This atomic layer deposition process used 333 cycles comprising an initial 2 s Ar purge, a 4 s exposure to oxygen plasma, a 30 ms does time exposure to diethyl zinc (DEZ) and a final 4 s Ar purge. The RF power was 100 W and the pressure was 15 mTorr. The layer thickness was measured using ellipsometry and found to be 36 nm. A comparison was then made of two different anisotropic ZnO etches based on fluorine chemistry. On some chips, a reactive ion etch (RIE) was performed in an Oxford Instruments Plasma Technology 80+ system using 25 sccm CHF_3 at a pressure of 20 mTorr and an RF power of 300 W. On other chips, a remote plasma inductively coupled plasma etch (ICP) etch was performed in an Oxford Instruments Plasma Technology System 100 ICP 380 using 25 sccm CHF_3, 300 W RF power, 1000 W ICP power and a pressure of 10 mTorr. The ZnO RIE etch rate was 1.6 nm/min and the ICP etch rate 50 nm/min.

After etching, aluminum source and drain electrodes were evaporated and patterned by a lift-off method. The FETs were dual nanowires with channel length of 10 μm. The electrical measurements on the nanowires were conducted with an HP 4155 semiconductor parameter analyzer with a grounded source voltage.

5.3.2 Results

Fig.5.5 shows Scanning Electron Microscope (SEM) cross-section images of ZnO nanowires fabricated with RIE and ICP etching. The images were obtained from nanowires produced in the same ZnO layer, which was deposited at 150ºC using the process described above. The RIE nanowire has a width at the base of 40 nm and a height of 83 nm, while the ICP nanowire has a width at the base of 40 nm and a height of 87 nm measured along the pillar. Note that these results were tilt - corrected as the sample was tilted during the measurement. The nanowire width of 40 nm at the base for both nanowires compares with a thickness of 36 nm measured by ellipsometry after deposition. This is reasonable agreement (11%) given the uncertainties in measuring thickness from an SEM image. Surface roughness can be seen on the sidewall of the RIE nanowire in Fig. 5.5(a). To quantify the surface roughness for RIE and ICP etched nanowires, the surface roughness along the nanowire sidewall was measured using atomic force microscopy. These measurements showed that the RIE nanowires had a surface roughness of 6.4 nm and the ICP nanowires 1.5 nm.

To assess the effect of the dry etch on the nanowire transistor behaviour, Fig.5.6 compares the transfer characteristics of RIE and ICP nanowire transistors measured at a drain voltage of 1 V. It can be seen that the characteristic of the ICP nanowire transistor is shifted to higher values of gate voltage with respect to the RIE transistor. Values of threshold voltage of 10 and 22 V were extracted for RIE and ICP nanowire transistors respectively by extrapolation of the linear transfer characteristic.

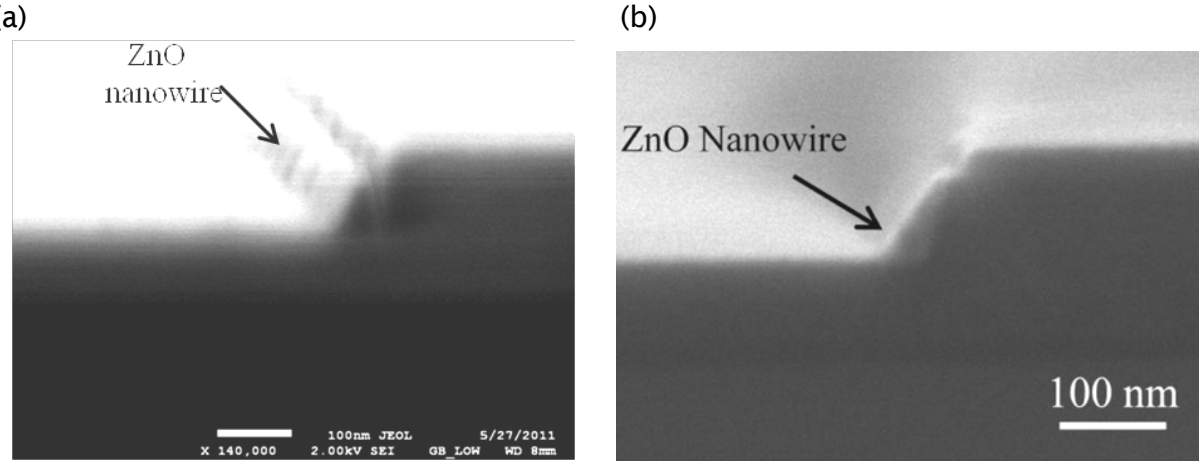
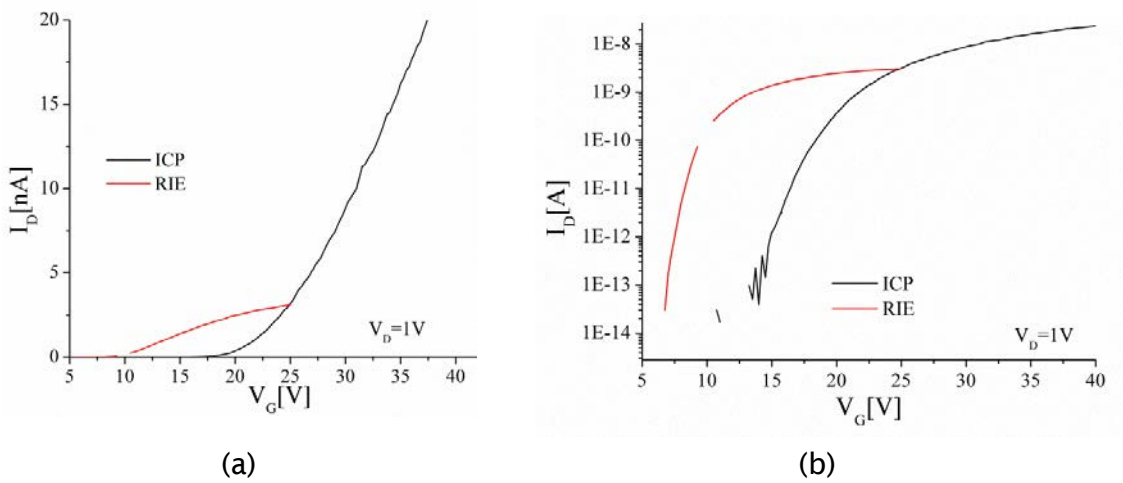


Fig.5.5 Cross-sectional SEM images of ZnO nanowires fabricated using a) reactive ion etch and b) inductively coupled plasma etching. The ZnO layer was deposited at 150ºC using 200 cycles comprising an initial Ar purge of 2s, a 4s exposure to oxygen plasma, a 30 ms exposure to DEZ and a final Ar purge of 4s. The ALD RF power was 10 0W and the pressure was 15 mtorr.

Furthermore, the drain current at high gate bias is significantly higher for the ICP transistor than the RIE transistor. For a gate overdrive, $V_G - V_{TH}$, of 6 V, the ICP nanowire transistor has a drain current of 6.4 nA, compared with value of 1.6 nA for the RIE transistor.



(a) (b)

Fig.5.6 (a) Transfer characteristics in linear scale and (b) Sub-threshold characteristics of dual NWFET etched in RIE and ICP.

Fig.5.7 compares output characteristics for ZnO nanowire transistors produced using reactive ion etching and inductively coupled plasma etching. Both transistors show well behaved transistor characteristics with clear saturation at higher values of drain bias. However, the ICP nanowire transistor shows higher values of drain current than the RIE transistor. Defining a drain current, I_{ON}, at V_D = 15 V and 6 V gate overdrive, the ICP nanowire transistor has an I_{ON} of 27.6 nA, compared with a value of 6.5 nA for the RIE transistor. Therefore an ICP etch gives nanowire transistors with a 4.2 times higher drain current than an RIE etch.

Table 5.2 summarises the parameters obtained from electrical measurements on these transistors. The threshold voltage of the ICP nanowire transistor is 22 V, compared with 10 V for the RIE transistor and the field effect mobility is 3.0 cm^2/Vs compared with 0.5 cm^2/Vs respectively. Thus an ICP etch gives a 6 times higher field effect mobility than an RIE etch.

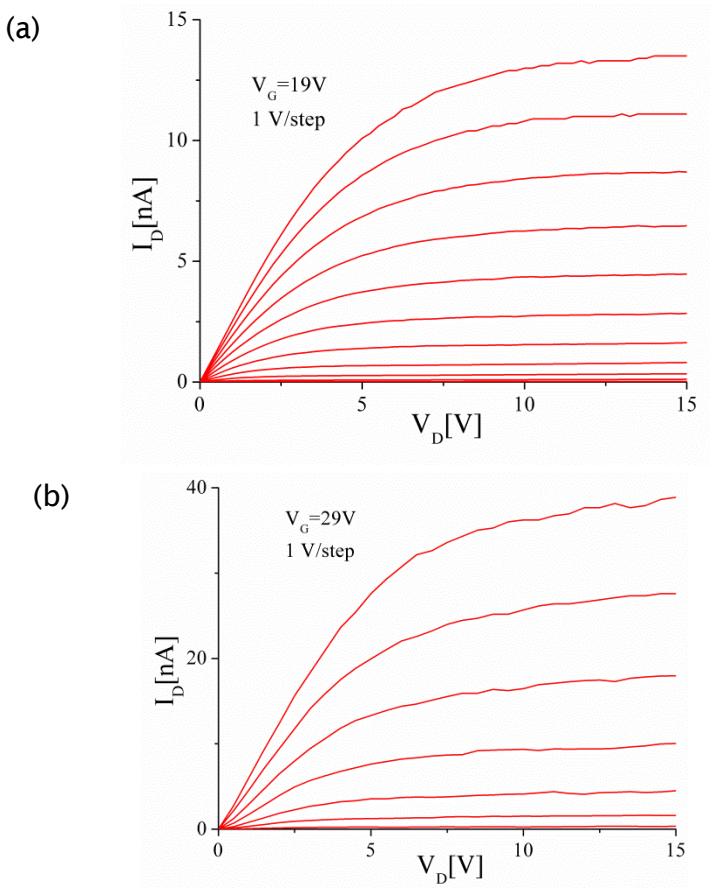


Fig. 5.7 Output characteristics of ZnO nanowire transistors with fabricated using (a) reactive ion etch and (b) inductively coupled plasma etching. The transistors comprised two parallel nanowires with a channel length of 10 µm. The ZnO layer was deposited at 150ºC using 200 cycles comprising an initial Ar purge of 2s, a 4s exposure to oxygen plasma, a 30ms exposure to DEZ and a final Ar purge of 4s. The RF power was 100 W and the pressure was 15mtorr.

TABLE 5.2 Summary of parameters obtained for ZnO nanowire transistors fabricated by reactive ion etch and inductively coupled plasma etch. The threshold voltage was determined by extrapolation of the linear transfer characteristics and the field effect mobility was determined from the transconductance. The on-current was determined from the output characteristics at V_D = 15 V using a gate overdrive, $V_G - V_{TH}$, of 6V.

Dry etch method	Threshold voltage [V]	Field Effect Mobility, μ_{FE} [cm^2/Vs]	I_D at $\lvert V_G-V_{TH}\rvert$ = 6 V [nA]	On-current, I_{ON} [nA]
RIE	10	0.5	1.6	6.5
ICP	22	3.0	6.4	27.6

5.3.3 Discussion

The results in Table 5.2 show significantly higher values of field effect mobility (3.0 cm^2/V.s compared with 0.5 cm^2/V.s) for nanowire transistors fabricated by ICP rather than RIE etch, which correlates with lower surface roughness (1.5 nm compared with 6.4 nm). This correlation suggests that the field effect mobility in nanowire transistors is limited by roughness on the nanowire sidewall induced by the plasma etching, particularly in RIE transistors. The RIE etch process utilises a high energy plasma with direct ion impingement on the ZnO surface. The high RIE etch pressure of 30 mT means a short ion mean free path and hence there are many ion collisions with the ZnO surface [7] that can lead to surface roughness. In contrast the ICP pressure is set at 10 mTorr and the high density plasma is remotely generated. The lower etch pressure gives a longer ion mean free path length and this combined with the remote plasma gives fewer ion collisions with the ZnO surface and hence a smoother surface.

The electrical results in Table 5.2 show that ICP nanowire transistors have 6 times higher values of field effect mobility than RIE transistors. The value of I_D in the linear region of the two nanowires can be estimated from the following equation [8] :

$$I_D \approx \frac{C_{dual}\mu_{FE}(V_G - V_{TH})V_D}{L^2} \qquad (5.1)$$

where C_{dual} is the total gate dielectric capacitance of two nanowires, μ_{FE} is the field-effect mobility of a single nanowire device and L is the nanowire channel length. The capacitance of a single nanowire can be determined by Eq. (5.2) which was discussed in Chapter 3 previously.

$$C_{nw} = \frac{2\pi\varepsilon_0\varepsilon_{r,eff}L}{ln\left(\frac{2t}{r}\right)} \qquad (5.2)$$

$$\therefore C_{dual} = 2C_{nw}$$

where $\varepsilon_{r,eff} = 2.65$ for the triangular cross sections of non-embedded nanowire structure, t is the gate oxide thickness and r is the nanowire radius which is considered as the half of the base width of the nanowire.

The key variables influencing the value of I_D in the linear region are the field effect mobility, μ_{FE}, the capacitance, C, and the threshold voltage V_{TH}. The SEM images in Fig. 5.5 indicate that the RIE and ICP nanowire widths are approximately the same, so with the assumption that the values of capacitance are the same, the ratio of the drain currents at $|V_G\text{-}V_{TH}| = 6$ V can be calculated using the extracted values of field effect mobility and threshold voltage. This gives an I_D of 1.8 nA for RIE etched device which is in good agreement with measured value of 1.6 nA. Meanwhile, a calculated I_D of 9.7 nA is obtained from ICP etched device which is 51%

more than measured value. This discrepancy could be due to the uncertainties in the extraction of the values of threshold voltage and/or field-effect mobility.

Meanwhile, the RIE etched NW-FET exhibits lower threshold voltage compared to ICP etched device. The ICP etched nanowire is more influenced with positive charges in the oxide because there are two sides of the nanowire in contact with SiO_2. However, for RIE etched nanowire only has one side of its surface (bottom) which is in contact with the SiO_2 dielectric. Thus the threshold voltage needed to compensate for the oxide charges is less compared to ICP etched nanowire devices.

5.3.4 Summary

It was shown that RIE etched devices suffered from surface roughness which caused deterioration in the channel conductance and field-effect mobility. The ICP etched device exhibits mobility improvement by 6-fold to 3 cm^2/Vs and increase of I_{ON} by 4.2 due to its smoother surface. This shows surface roughness caused significant impact on the electrical performance of the NWFET device.

5.4 Effect of ALD O_2 Pressure on Film Properties

This experiment is to study the effect of O_2 plasma pressure during ALD deposition on the Growth Per Cycle and surface roughness of the ZnO film. From Chapter 4, it was found an optimized plasma pressure should be <57.5 mTorr. However, it was found the oxygen plasma pressure can affect the growth rate as well as the film roughness.

5.4.1 Experiment

Prior to deposition, samples were cleaned in fuming nitric acid (FNA) for 10 mins to remove any contamination. ZnO films were deposited on 2 x 2 cm^2 SiO_2/Si substrates with two O_2 pressures; 15 mTorr and 57.5 mTorr. All remaining parameters including temperature at 150^oC and DEZ dose time of 30 ms were kept constant. The film thicknesses were measured ex-situ using a J.A.Woollam ellipsometer. Atomic force microscopy (AFM) measurements were performed with a multimode AFM using the tapping mode cantilever to obtain the film roughness.

5.4.2 Results and Discussion

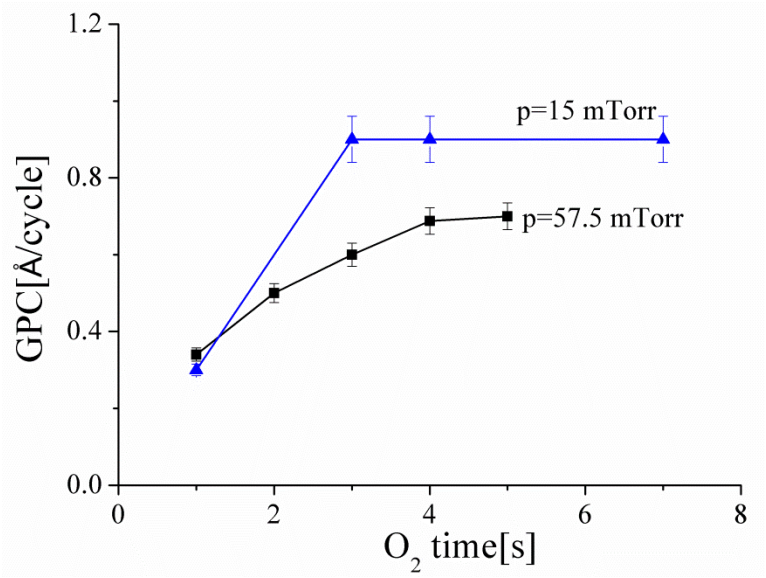
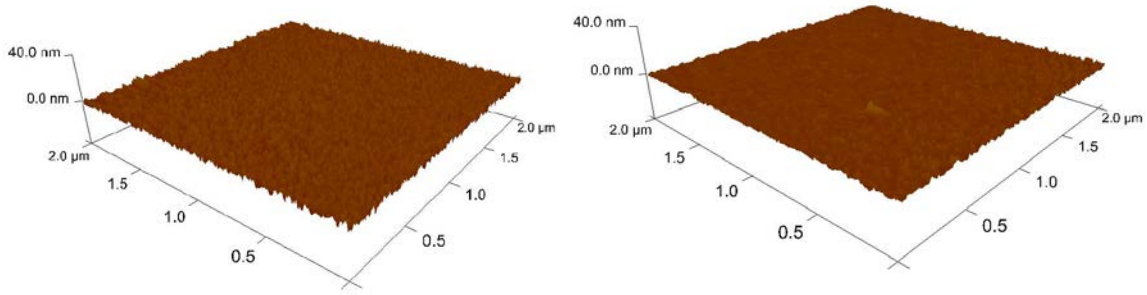


Fig 5.8 Growth per cycle (GPC) with increasing oxygen plasma reactant time at different oxygen pressure during deposition**.**

Fig. 5.8 shows the Growth Per Cycle (GPC) of ZnO film deposited with increasing plasma time at two O_2 pressure; 15 mTorr and 57.5 mTorr. Both experiments show a self-saturated PEALD process in which at a pressure of 15 mTorr (black plot), the GPC saturated at about 0.85 to 0.9 Angstrom per cycle which is 32% higher than films deposited at 57.5 mTorr.

The film surface roughness was measured in terms of Root Mean Square (RMS) values obtained using atomic force microscopy for films deposited at two different pressures at O_2 plasma time of 4s. Fig.5.9 (a) and (b) show the 3-D AFM images of a 2 μm x 2 μm surface area for ZnO films deposited at O_2 plasma time of 4s at pressures of 57.5 mTorr and 15 mTorr, respectively. Both films are about 35 nm in thickness. Films deposited at 57.5 mTorr have an RMS value of 1.7 nm while the film deposited at 15 mTorr has 0.7 nm which is 58 % less surface roughness than films deposited at 57.5 mTorr.



(a) (b)

Fig 5.9 AFM image of ZnO films deposited at (a) 57.5 mTorr and (b) 15 mTorr

Though in Chapter 4, ZnO films deposited at O_2 pressure of 57.5 mTorr showed low contamination and better electrical characteristics, it is also important to obtain films with high GPC and low surface roughness. The partial pressure is a way of expressing the concentration for gases. The number of collisions increases with increase in the partial pressures of gases. Hence the rate of surface reactions decreases and film roughness increases which causes the decrease of deposition rate. A rough surface is expected for this pressure since the saturated GPC was only on average, 0.68 angstrom per cycle which is less than one atomic layer thickness. Incomplete atomic layer formation induces higher surface roughness. Meanwhile at low O_2 pressure (15 mTorr), the mean free path of the O_2 reactant increases due to less collisions causing higher deposition rate hence higher GPC. The surface area is much smoother due to complete surface reaction. The RMS roughness obtained for this pressure (15 mTorr) was 0.7 nm which is lower than that obtained with a pressure of 57.5 mTorr. Similar oxygen pressure effects on film roughness have been reported for ZnO films with other deposition techniques [9].

In conclusion, the O_2 reactant pressure during ALD deposition was important to control the deposition rate as well as the film surface roughness. It was found that at a low O_2 pressure of 15 mTorr, a higher film deposition rate and smoother ZnO film was achieved.

5.5 Effect of DEZ Dose

The lower film growth rate (0.9 Å/cycle) and low field effect mobility achieved from previous experiment could be due to a non-optimal condition on DEZ dose times. Therefore, this experiment was conducted to study the optimal DEZ dose times for ZnO film condition based on the film growth rate, electrical characteristics and the surface compositions obtained.

5.5.1 Experiment

A P-type <100> oriented Si wafers were cleaned and a 200 nm thermal SiO_2 was grown by a wet oxidation at 1000^oC. Subsequently, the SiO_2 layer was etched by 100 nm in RIE to form trenches. The wafer was diced into 2 cm x 2 cm chips for different deposition experiments. The diced chips were further cleaned in fuming nitric acid before ZnO film deposition. ZnO films were deposited on these trenches using remote PEALD. The atomic layer deposition used 200 cycles of a process comprising an initial Ar purge of 2s, a 4s exposure to oxygen plasma, an exposure to DEZ for a given time and a final Ar purge of 4s at deposition temperature of 150^oC. The RF power was 100 W and the pressure was 15 mtorr. All ALD ZnO films were terminated with an oxygen monolayer at the end of each deposition.

The thicknesses of the ZnO films were measured by an ellipsometer. Hall measurements were carried out to obtain resistivity, carrier concentration and Hall mobility. For Hall measurement, quartz substrates were used. Additionally, XPS measurements were conducted to determine the stoichiometry of the deposited film. The stoichiometry was determined from the ratio of the atomic percentages of the $Zn2p_{3/2}$ peak and the O1s peak observed at ~1022 eV and ~531 eV, respectively from the XPS. XPS measurements were performed on a Thermo Scientific Theta Prober spectrometer using monochromatized Al Kα emission. Binding energies were measured using the C 1*s* peak (284.8 eV) of the carbon as an internal standard.

5.5.2 Results

Fig. 5.10 shows the growth rate, given by growth per cycle [GPC] of the remote plasma ALD on the SiO_2/p-Si substrate with increasing DEZ dose time. The growth rate increases from 0.85 Å/cycle and reached saturation at ~1.08 Å/cycle at about 1.5 s of DEZ dose time. This result confirms the self-limiting growth behaviour of the ZnO film.

All deposited ZnO thin films showed n-type conductivity. Figure 5.11 show the resistivity and Hall mobility of the remote plasma ALD ZnO as a function of DEZ dose time in secs, respectively.

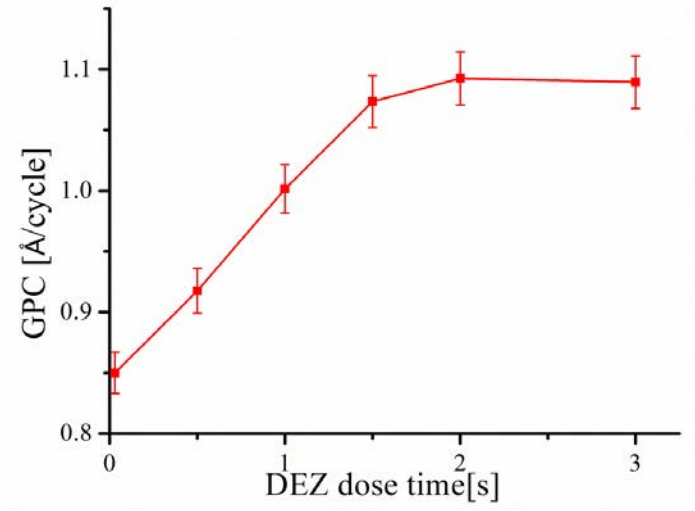


Fig 5. 10 The growth per cycle [GPC] as a function of DEZ dose time in Remote PEALD. ZnO layers deposited at 150ºC, using an initial Ar purge of 2s, a 4s plasma exposure in oxygen, an exposure to DEZ for a given time and a final Ar purge of 4s. The ALD RF power was 100 W and the pressure was 15 mTorr.

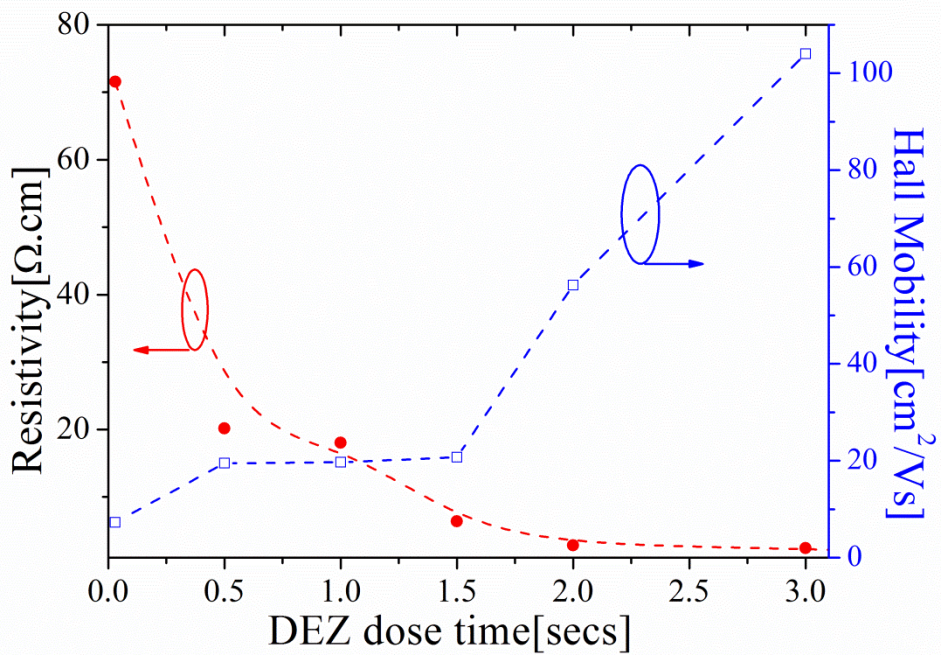


Fig.5.11 Resistivity and Hall mobility as a function of DEZ dose time for ZnO layers deposited at 150ºC, using 200 cycles of a process comprising an initial Ar purge of 2s, a 4s plasma exposure in oxygen, an exposure to DEZ for a given time and a final Ar purge of 4s. The ALD RF power was 100 W and the pressure was 15 mtorr.

The Hall mobility remains at or below 20 cm^2/Vs for DEZ dose times up to and including 1.5 s, but then increases sharply to a value of 104 cm^2/Vs for a dose time of 3 s. Fig. 5.10 shown

previously indicates that a DEZ dose time of 1.5 s corresponds with the start of saturation of the growth per cycle. Thus the low values of mobility seen for short DEZ dose times are due to a DEZ dose step that is too short for a ZnO monolayer to completely form. The resistivity variation with DEZ dose time mirrors the mobility variation, with high values of resistivity obtained at low DEZ dose times and low values at high DEZ dose times.

To investigate the stoichiometry of the ALD ZnO films, XPS measurements were made after film deposition. Fig. 5.12 shows a graph of Zn/O ratio and Hall carrier concentration as a function of DEZ dose time at a deposition temperature of 150ºC. A stoichiometric ZnO film is obtained for a DEZ dose time of 30 ms, but slightly Zn rich films are obtained for longer dose times. The Hall carrier concentration does not vary strongly with DEZ dose time, but stays in the range 1.5 to 4 × 10^{16} cm^{-3}. The inset in Fig. 5.12 shows a graph of carbon impurities in .at% measured in XPS as a function of DEZ dose time. The carbon impurity is highest at the lowest DEZ dose time at 30 ms and decreases with increasing DEZ dose but increases again at 3 ms of DEZ dose time.

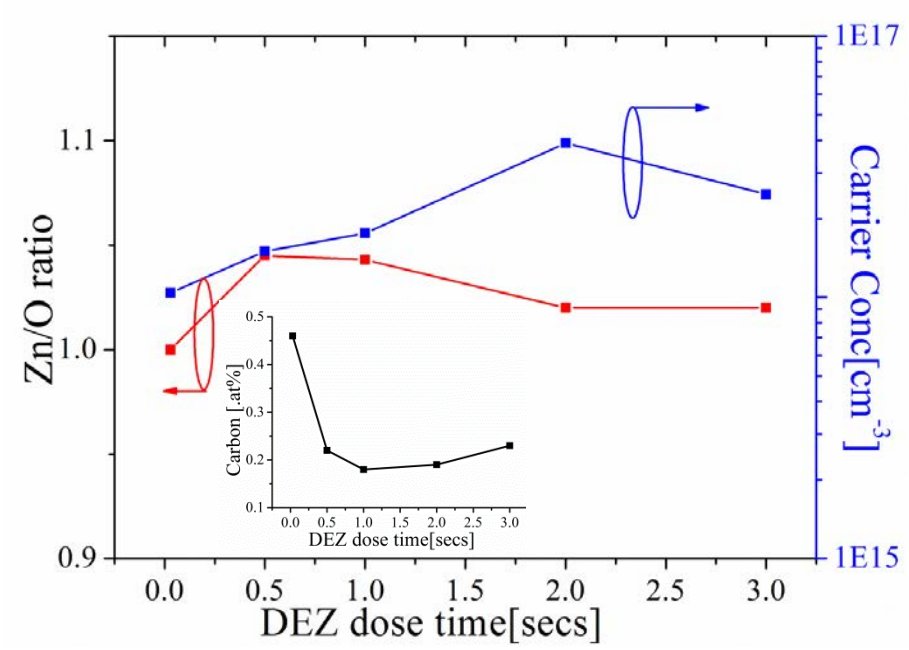


Fig.5.12 Zn/O ratio measured using XPS and Hall carrier concentration as a function of DEZ dose time for ZnO layers deposited at 150ºC, using an initial Ar purge of 2s, a 4s plasma exposure in oxygen, an exposure to DEZ for a given time and a final Ar purge of 4s. The ALD RF power was 100 W and the pressure was 15 mTorr. The inset shows a graph of Carbon concentration in .at% measured in XPS as a function of DEZ dose time.

5.5.3 Discussion

The saturated growth rate per cycle [GPC] achieved in this experiment was 1.08 Å/cycle at about 1.5 s of DEZ dose time. Generally, this growth rate is lower compared to ZnO films deposited in other PEALD techniques [10][11]. Although plasma assisted ALD was shown to exhibit higher growth rate than thermal ALD due to the high reactivity of oxygen plasma than water reactant, remote plasma ALD used in this experiment had lower ion energy (< ~20 eV) . Current experiment also had used lower plasma power of 100 W compared to higher plasma power used in other PEALD work [12]. Ion energy and plasma power influence the growth rate of materials in PEALD process. Variations in growth rates are, however, common in the ALD processing of metal oxides and tend to depend also on the oxidant source, the Zn source and the reactor configuration used in the experiments [13].

From the Hall and XPS measurements, ZnO films with low DEZ time exhibit higher resistivity and higher carbon impurity. According to the previously reported characteristics of the ALD ZnO film, carbon content in the ZnO film increased with decreasing process temperature due to incomplete decomposition of DEZ. However, this experiment was conducted at a fixed temperature of 150^{o}C which is believed to be sufficient for decomposition of DEZ precursor. Therefore the high carbon impurity observed at low DEZ dose time could be due to the insufficient time for the DEZ reactant to move to the equilibrium atomic sites. It has also been speculated that during the oxygen plasma step, combustion products such as CO, CO_2 and H_2O and hydrocarbon species such as C_2H_x were formed and even detected in other PEALD processes [13]. Therefore, in oxygen rich conditions (t <0.5s) , these products are high relative to number of surface species created by the DEZ precursor chemisorptions thus it appears there is a preference for CO production [13]. Subsequently, these carbon impurities act as electron traps which increase the film resistivity and decrease the Hall mobility at low DEZ dose time as shown from the electrical measurements.

Interestingly, the stoichiometry and the carrier concentration did not change significantly with DEZ dose times. At low DEZ dose times, the ZnO film exhibited slightly higher oxygen rich as indicated from the Zn/O ratio and accordingly the measured carrier concentration was low in this region (1 to 1.5 x10^{16} cm^{-3}). At high DEZ dose times , the ZnO films exhibited higher carrier concentration (1.5 to 4 x10^{16} cm^{-3}) in which the films were found to be Zn rich from the XPS measurements . These results emphasized that the carriers in ZnO film for this process temperatures are dominated by oxygen vacancies, V_o as shown in previous work [14] and demonstrated the relationship between the stoichiometry and the carrier concentration of the ZnO film.

5.5.4 Summary

ZnO film growth by remote PEALD with increasing DEZ precursor times has been investigated. The process was proven to exhibit true ALD-like properties with saturated film growth at a rate of 1.08 Å/cycle at 150^{o}C. The film resistivity increased to maximum of 71.58 Ω.cm and Hall mobility decreased to minimum of 7.3 cm^2/Vs with decreasing DEZ dose times. This was shown to be due to high levels of carbon impurities incorporated during the ZnO film growth at low DEZ dose times. The highest Hall mobility of 104 cm^2/Vs was achieved at a DEZ dose time of 3 s. Low DEZ dose time (t = 30 ms) produced films with low carrier concentration at 1 x 10^{16} cm^{-3} and with high carbon impurities. Based on this investigation, the optimized range of DEZ precursor was found to be >1 s for low resistivity and carbon impurity as well as high mobility ZnO film.

5.6 Effect of Substrate Temperature on Film Properties

There have been various results reported on the effect of substrate temperatures on ZnO film properties using thermal ALD [15-19]. However, thermal ALD suffers from narrow temperature window and produced films with high carrier concentration in the order of 10^{20} cm^{-3} even at low deposition temperatures. PEALD is known to facilitate deposition at low temperatures with wider temperature window which produces improved material properties compared to thermal ALD. There are not many reports investigating ZnO film properties using PEALD process [10] [20]. Therefore, the goal of the experiment conducted in this work was to develop and investigate the effect of substrate temperatures on the surface roughness, electrical conductivity, film stoichiometry and chemical bonding and also on the optical transparency of the deposited ZnO films in remote PEALD.

5.6.1 Experiment

The substrates were prepared using the same method described in Section 5.5. A SiO_2/p-Si substrate was diced into 2 cm x 2 cm chips. Quartz chips were also prepared with the same dimensions for Hall and transmittance measurements. The diced chips were further cleaned in fuming nitric acid before ZnO film depositions. ZnO films were deposited under the conditions of optimal reactant feeding and pressure determined by previous experiments. The cycle sequence of DEZ/Ar/O_2/Ar was 1/2/4/4 s. Substrate temperatures were varied from 100 ^{o}C to210 ^{o}C. The number of cycles was fixed at 200 cycles. The RF power was 100 W and the pressure was 15 mtorr. All ALD ZnO films were terminated with an oxygen monolayer at the end of each deposition.

The deposited ZnO layers were characterised using Hall effect measurements of bulk mobility and carrier concentration, sheet resistance measurements for resistivity, XPS measurements of film stoichiometry and atomic force microscope measurements of surface roughness. Additionally, transmission measurements were conducted in a commercial system from Bentham, consisting of a TMc300 monochromator and a DTR6 integrating sphere fitted with a silicon photodiode as the detection unit.

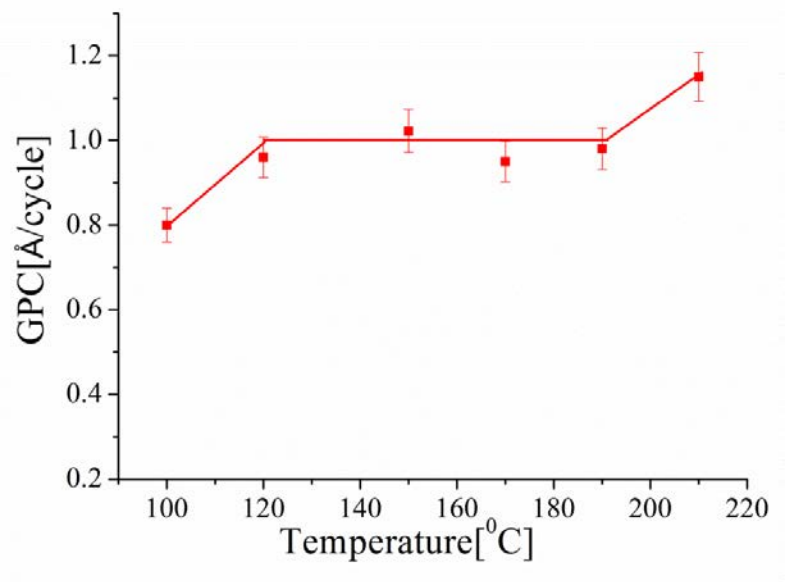
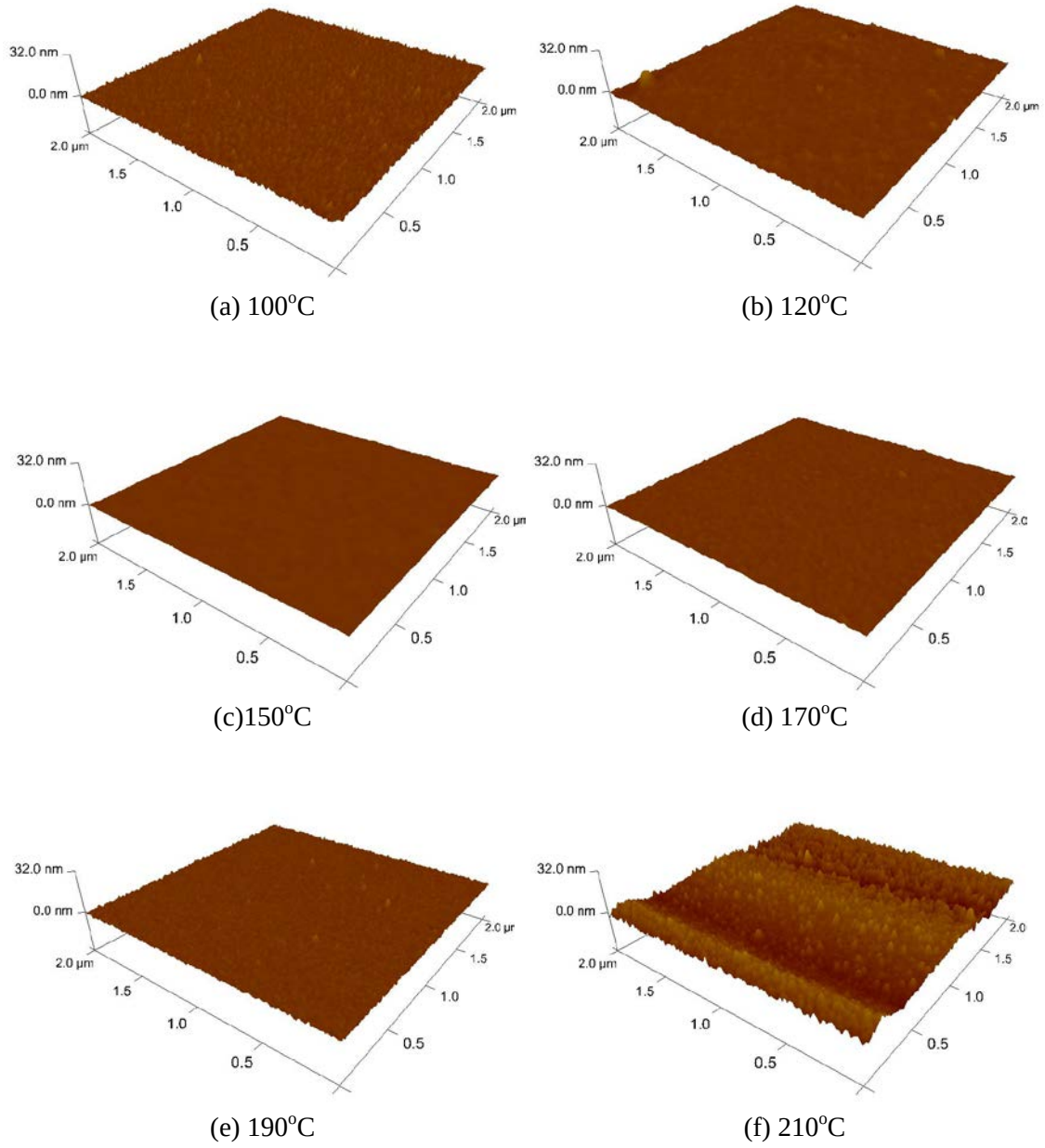


Fig 5.13 Growth per cycle (GPC) of ZnO film as a function of atomic layer deposition temperature for ZnO layers deposited using an initial Ar purge of 2s, 4s of oxygen plasma exposure, 1s of DEZ dose time, an RF power of 100W, a pressure of 15 mtorr and a final Ar purge of 4s.

5.6.2 Results

Fig .5.13 shows the ZnO film growth rates plotted as a function of the substrate temperature. The substrate temperatures did have a significant effect on the film growth. At a low temperature at 100^{o}C, the GPC was the lowest at 0.8 Å/cycle. This is because the reactants do not have sufficient energy to react chemically at this low temperature. In the temperature range from 120 to 190 ^{o}C the film growth rate did not change significantly with temperature. However, at a substrate temperature of 210^{o}C, the GPC increased to 1.15 Å/cycle.



(a) 100°C (b) 120°C

(c)150°C (d) 170°C

(e) 190°C (f) 210°C

Fig 5.14 3D-AFM images of ZnO films deposited at various atomic layer deposition temperature for ZnO layers using an initial Ar purge of 2s, 4s of oxygen plasma exposure, 1s of DEZ dose time, an RF power of 100 W, a pressure of 15 mTorr and a final Ar purge of 4s.

The film surface roughness was measured in terms of Root Mean Square (RMS) values obtained using atomic force microscopy. Fig.5.14 (a) to (f) show the 3-D AFM images of 2 µm x 2 µm surface area for ZnO films deposited at various temperatures. Figure 5.15 shows the RMS values of the surface roughness of these films. From these results, the film deposited at 100 °C (Fig 5.14(a)) shows a rough surface and exhibits surface roughness with an RMS

value of 1.02 nm. Films deposited from 120 to 190 ^{o}C (Fig 5.14(b)-(e)) show very flat surfaces without any sharp peaks appearing in the domain. The RMS values are in the range of 0.3 to 0.6 nm. Films deposited at 210oC (Fig 5.14(f)) show a very rough surface with the highest RMS value of 2.7 nm.

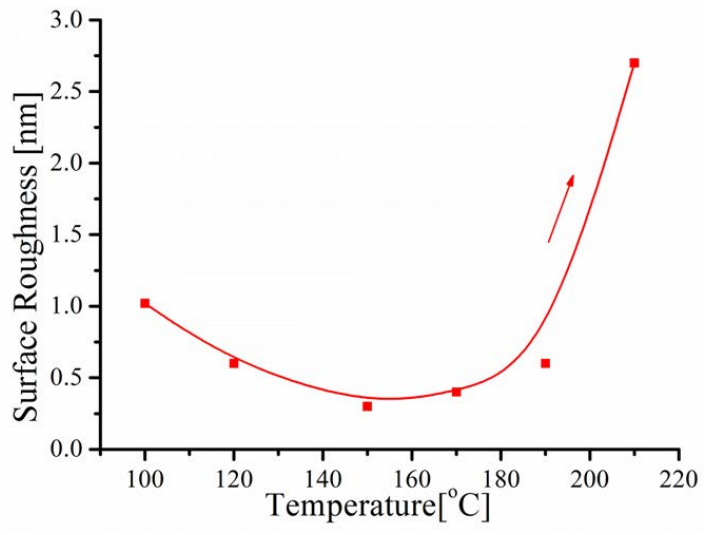


Fig 5.15 Surface roughness measured using atomic force microscopy as a function of atomic layer deposition temperature for ZnO layers deposited using an initial Ar purge of 2s, 4s of oxygen plasma exposure, 1s of DEZ dose time, an RF power of 100 W, a pressure of 15 mTorr and a final Ar purge of 4s.

All the PEALD ZnO thin films showed n-type conductivity which agrees well with previous experiments. Fig 5.16 shows a graph of resistivity and Hall mobility as a function of deposition temperature. The Hall mobility increases slowly from a value of 6 cm2/V.s at a deposition temperature of 100ºC to a value of 30 cm2/V.s at 170ºC and then sharply increases to a value of 118 cm2/V.s at 190ºC. The mobility then falls sharply to a value of 16 cm2/Vs at a deposition temperature of 210ºC. High values of resistivity above 10 Ω.cm are obtained for deposition temperatures up to 170ºC, but the resistivity then decreases sharply to 3.4 Ω.cm at 190ºC and 0.4 Ω.cm at 210ºC.

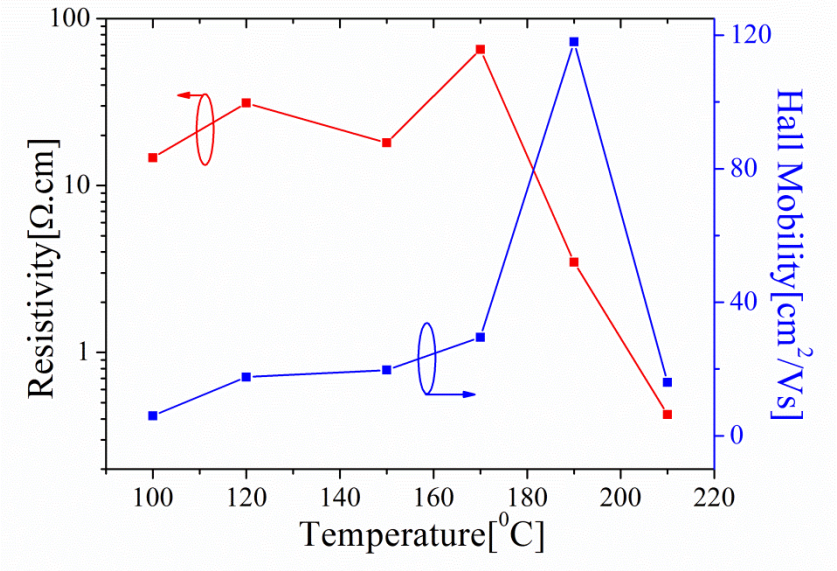


Fig.5.16 Resistivity and Hall mobility as a function of atomic layer deposition temperature for ZnO layers deposited using an initial Ar purge of 2s, 4s of oxygen plasma exposure, 1s of DEZ dose time, an RF power of 100 W, a pressure of 15 mTorr and a final Ar purge of 4s.

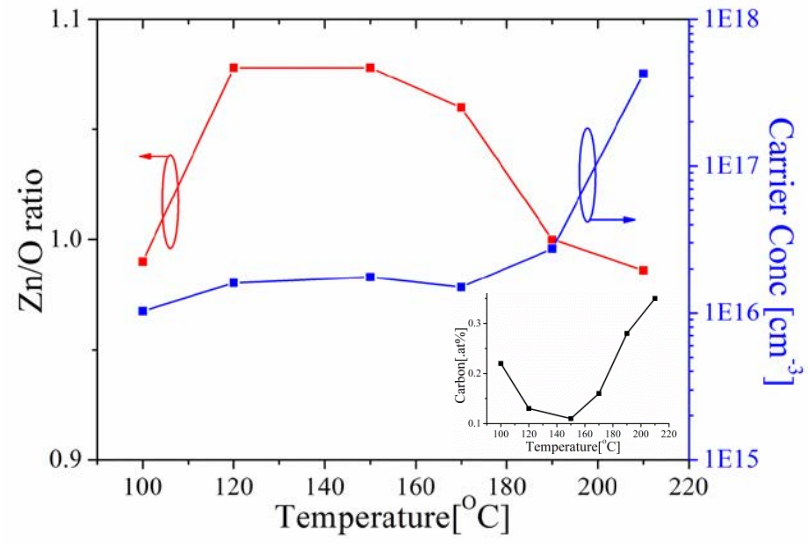


Fig.5.17 Carrier concentration measured using Hall Effect as a function of atomic layer deposition temperature for ZnO layers deposited using an initial Ar purge of 2s, 4s of oxygen plasma exposure, 1s of DEZ dose time, an RF power of 100 W, a pressure of 15 mTorr and a final Ar purge of 4s. The inset shows a graph of Carbon concentration in .at% measured in XPS as a function of substrate temperatures.

Fig. 5.17 shows a graph of Zn/O ratio and Hall carrier concentration as a function of ALD deposition temperature. At a deposition temperature of 100ºC, a slightly oxygen-rich film is produced. At temperatures in the range of 120 to 170ºC zinc-rich films are produced, at a temperature of 190ºC a stoichiometric film is produced and at a temperature of 210ºC a slightly oxygen-rich film is produced. At deposition temperatures between 100 and 190ºC the carrier concentration remains approximately constant at a value in the range 1×10^{16} to 2.7×10^{16} cm^{-3} and then increases sharply to 4.3×10^{17} cm^{-3} at 210ºC. The inset in Fig. 5.17 shows a graph of carbon impurities in .at% measured with XPS as a function of substrate temperature. Initially at 100^{o}C of substrate temperature, the film exhibits 0.22% of carbon impurities. However at temperatures from 120^{o}C to 170^{o}C, the film carbon impurities range from 0.13 % to 0.16 %. At substrate temperature of 210^{o}C, the film exhibited the highest carbon impurity at 0.34%.

Optical transmittance measurements were conducted on all the ZnO/quartz films to compare the substrate temperature effect on optical properties of ZnO films. The substrates were irradiated at a perpendicular angle of incidence with blank quartz being the reference. Figure 5.18 shows the plot of optical transmittance spectra (%) versus wavelengths from 300 to 1100 nm for all ZnO films. All the ZnO films demonstrate transmittance of above 90% in the range of the visible spectrum. The oscillations observed in all the curves could be due to the irregular surface of the ZnO films.

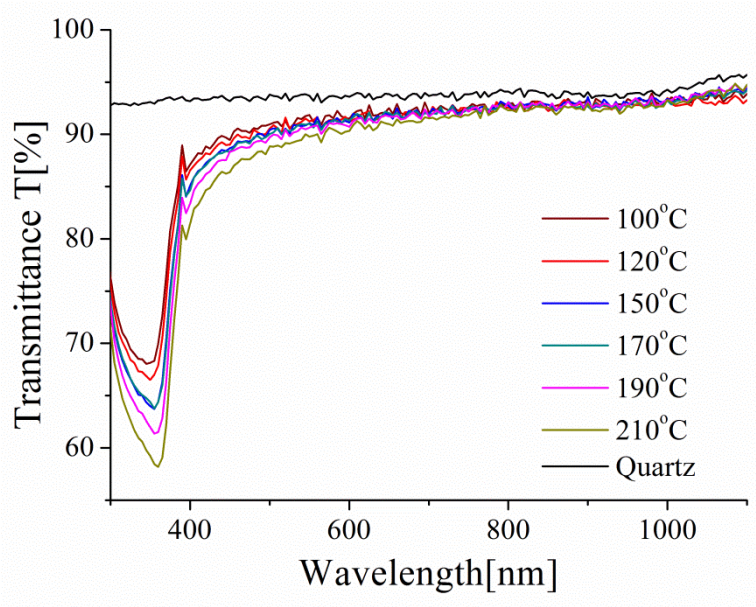


Fig 5.18 Optical transmittance of ZnO films at different substrate temperatures. ZnO layers deposited using an initial Ar purge of 2s, 4s of oxygen plasma exposure, 1s of DEZ dose time, an RF power of 100 W, a pressure of 15 mtorr and a final Ar purge of 4s

5.6.3 Discussion

One of the characteristics of an ALD process is the process window. In the ALD window, the growth rate and hence the film thickness, only depends on the number of growth cycles. The ALD process window for ZnO film deposition was experimentally determined to lie in the temperature range from 120 to 190^{o}C. The observed deposition rate in the ALD process window was around 1.02 Å/cycle. It was also known that the ALD process is ideal within the process window. An ideal ALD process is established by sufficient feed of reactants and sufficient purging of remaining reactants and desorbed by-products. Therefore, the increase of the film growth rate at a temperature range above 190^{o}C was not attributed to the formation of an atomic layer of ZnO by surface reaction between DEZ and oxygen plasma but due to a chemical vapour deposition (CVD) mode growth due to decomposition of the DEZ precursors.

From the electrical, AFM and surface measurements, it can be concluded that the deposition at a substrate temperature of 210^{o}C was not an ideal ALD process. For this reason, the surface roughness and the carbon impurities were seen to be increased. An increase of carbon impurities decreased the mobility due to defects and traps. However the resistivity of the ZnO films decreased at higher temperature due to higher carrier concentration. At a low substrate temperature of 100^{o}C, the Hall mobility and carrier concentration were the lowest at 6 cm^{2}/Vs and 1 x 10^{16} cm^{-3}, respectively. The carbon content was also slightly higher compared to other films deposited at higher temperatures (except 210^{o}C). This was thought to be due to the unreacted DEZ adsorbed to the surface by low thermal activation energy [15]. Consequently, defects formed from the carbon reduced the carrier density and mobility.

At a substrate temperature of 190^{o}C, the Hall mobility obtained was the highest at 118 cm^{2}/Vs and the ZnO film was stoichiometric from the XPS study. The Hall mobility obtained was the highest so far achieved using PE-ALD. In D.Kim *et al* work, the highest Hall mobility achieved was 22.5 cm^{2}/Vs at a substrate temperature of 300^{o}C [10]. In addition, the carrier concentrations and resistivities varied significantly with more than 4 orders of magnitude with substrate temperatures in this work [10]. In this current experiment, the carrier concentrations did not change significantly with temperatures in which the carriers are within 1.6 to 2.7 x 10^{16} cm^{-3} within the ALD window which indicates a more controlled and stable deposition process. Low carrier concentration is preferred in order to utilize the ZnO film as a channel layer in FET device. This enables the device to be easily switched off and avoids undesirable drain-to-source current at zero gate voltage. In contrast, thermal ALD always produced ZnO films with high carrier concentrations in the range of more than 10^{17} cm^{-3} even at low substrate temperatures which is not suitable for transistor applications[10][15][20].

From the optical transmittance measurement results, it was found that the optical transmittance in the visible range was above 90% for all deposition temperatures. This means that the deposition temperature does not have a significant effect on the transparency of the films. The transparency of ZnO films is important in particular for display panel applications.

5.6.4 Summary

Self-limiting growth of zinc oxide was accomplished over a temperature window from 120^{o}C to 190^{o}C using remote PEALD deposition process. Hall mobility showed the highest with 118 cm^{2}/Vs at 190^{o}C due to its enhanced stoichiometry from the XPS measurements. Other films exhibited either Zn rich or an oxygen rich film which indicates that film stoichiometry affects the bulk mobility. At the lowest substrate temperature (100^{o}C), surface roughness was higher by 40%-50% compared to roughness for films deposited within the ALD window. In addition, the film was oxygen rich with higher carbon impurities and had the lowest carrier concentration at 1x10^{16} cm^{-3} due to the unreacted DEZ adsorbed on the surface by low thermal activation energy. Meanwhile a substrate temperature of 210^{o}C showed the highest surface roughness at 2.7 nm and highest carbon impurities due to non-ideal ALD process In addition, all ZnO films showed transparency >90% in the optical region indicating substrate temperature does not affect the transparency characteristics.

5.7 Effect of Substrate Temperatures on Device Properties

Based on the understanding of effects of substrate temperatures on film properties, top - down ZnO nanowire field-effect transistor (NW-FET) devices were fabricated. The strong background in the study of optimization of dry etches techniques and thin film growth in PEALD provided an exceptional environment for the studies of transistor device characteristics which will be described in this section.

5.7.1 Experiment

Top-down ZnO nanowire FETs were fabricated as explained in Chapter 4 and illustrated in Fig 5.19. ZnO films were deposited using PEALD at different substrate temperatures from 100^{o}C to 210^{o}C with all other deposition conditions kept constant. The atomic layer deposition used 200 cycles of a process comprising an initial Ar purge of 2s, a 4s exposure to oxygen plasma, an exposure to DEZ for a given time and a final Ar purge of 4s. The RF power was 100 W and the pressure was 15 mTorr. The ZnO layers were anisotropically etched using the ICP process described above. The thicknesses of the ALD films varied somewhat with

deposition temperature, from 16 nm at 100°C to 23 nm at 210°C. Aluminum source and drain electrodes were deposited by e-beam evaporation and patterned by lift-off. The Al contacts were then annealed at 350°C for 2 mins to improve the ohmic contact. The electrical properties of the NW-FETs were analyzed using an Agilent 15000 Parameter Analyzer at room temperature and in dark normal ambient. The field effect mobility was determined from the transconductance using the standard method described in Section 3.3.3 and the threshold voltage was determined by extrapolation of the linear transfer characteristic. Note that the device is a dual nanowire FET with channel length of 10 μm.

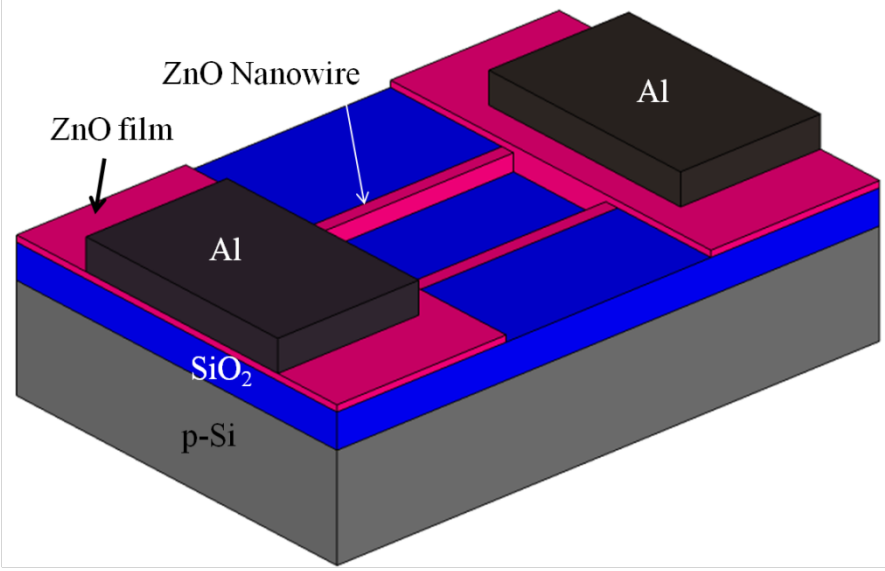


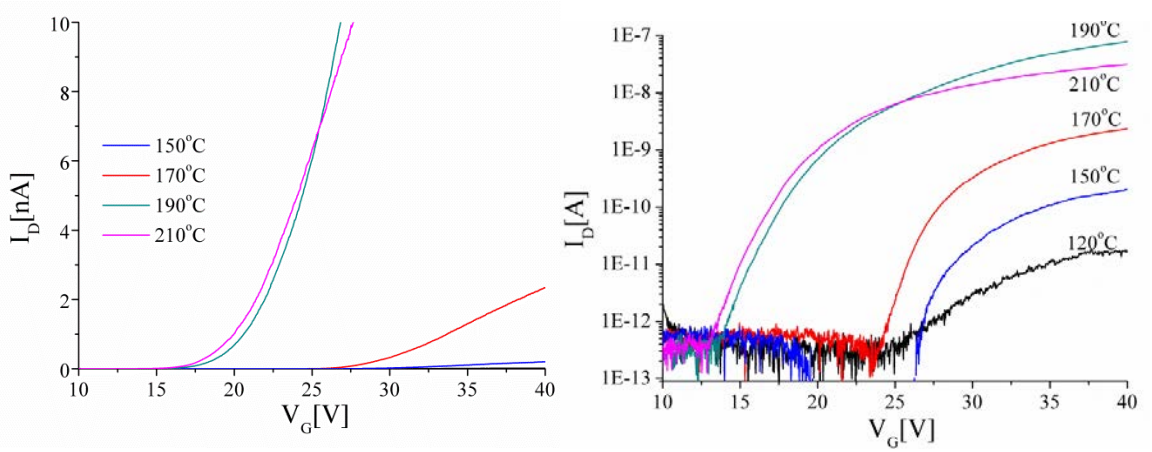
Fig.5.19 Schematic illustration of the top-down fabricated ZnO NW-FET structure.

5.7.2 Results

Figure 5.20 (a) and (b) show the source-to-drain current (I_D) as a function of gate voltage, V_G in linear and logarithmic scale, respectively. All the devices except for 100°C processed film exhibited typical n-type enhancement mode field-effect transistor characteristics. Device processed at 100°C did not show any transistor characteristics probably due to its small nanowire width of only 16 nm and a film with the lowest carrier concentration obtained previously from the Hall measurement.

From Fig.5.20, the drain current at high gate voltage increases with increasing ALD temperature up to a temperature of 190°C and then decreases at the highest ALD temperature of 210°C. The maximum drain current is obtained at an ALD temperature of 190°C, which corresponds to the maximum in the Hall mobility obtained in Fig 5.16. In addition the sub-threshold parts of the characteristics show a systematic shift towards negative gate voltages with increasing ALD temperature. Values of threshold voltage were extracted by extrapolation of the linear transfer characteristic and values of field effect mobility were extracted from the

transconductance and are summarised in Table 5.3. A maximum field effect mobility of 10 cm^2/Vs is obtained for an ALD deposition temperature of 190ºC. This temperature again corresponds with the maximum in the Hall mobility in Fig. 5.16. The on/off current ratio (I_{ON}/I_{OFF}) is measured by the ratio of maximum to minimum I_D on the gate voltage axis. The I_{ON}/I_{OFF} ratio is 80, 1.5 x 10^3, 2 x 10^4, 2 x 10^5 and 8.2 x 10^4 for channels processed at 120, 150, 170, 190 and 210°C, respectively.



(a) (b)

Fig 5.20 Transfer characteristics in (a) linear plot and (b) subthreshold plot of nanowire transistor with channel length of 10 µm and dual nanowire for ZnO layers deposited at various temperatures. The ALD process used an initial Ar purge of 2s, 4s of oxygen plasma exposure, 1s of DEZ dose time, an RF power of 100 W, a pressure of 15 mTorr and a final Ar purge of 4s.

TABLE 5.3 Summary of parameters obtained for ZnO nanowire transistors fabricated using ALD layers deposited at different temperatures. The threshold voltage was determined by extrapolation of the linear transfer characteristics and the field effect mobility was determined from the transistor transconductance. The on-current was determined from the output characteristics at V_D = 15 V using a gate overdrive, $V_G - V_{TH}$, of 6V.

ALD growth temperature [ºC]	Threshold voltage, V_{TH} [V]	Field effect mobility [cm^2/Vs]	I_{ON}/I_{OFF}	On-current I_{ON} [nA]
120	31	0.1	80	0.08
150	29.7	0.6	2 x 10^4	0.32
170	29	2.5	2 x 10^4	2.8
190	24	10	2 x 10^5	150
210	22	4.9	8 x 10^4	17

Fig. 5.21 shows output characteristics for ZnO nanowire transistors fabricated using ALD ZnO deposited at 150, 170, 190 and 210ºC. The output characteristics for device processed at 120ºC showed very low output current and affected by contact problem thus not shown here. It can be seen that the largest drain current is obtained for the 190ºC transistor, which again corresponds with the maximum in the Hall mobility in Fig. 5.16. At a drain bias of 15 V and a gate bias of 40 V, drain currents of 0.45, 5.3, 900 and 187 nA are obtained for ALD temperatures of 150, 170, 190 and 210ºC respectively. Correcting for the differences in threshold voltage (Table 5.3) gives values of drain current (I_{ON}) of 0.32, 2.8, 150 and 17 nA respectively for a gate overdrive $V_G - V_{TH}$ of 6 V.

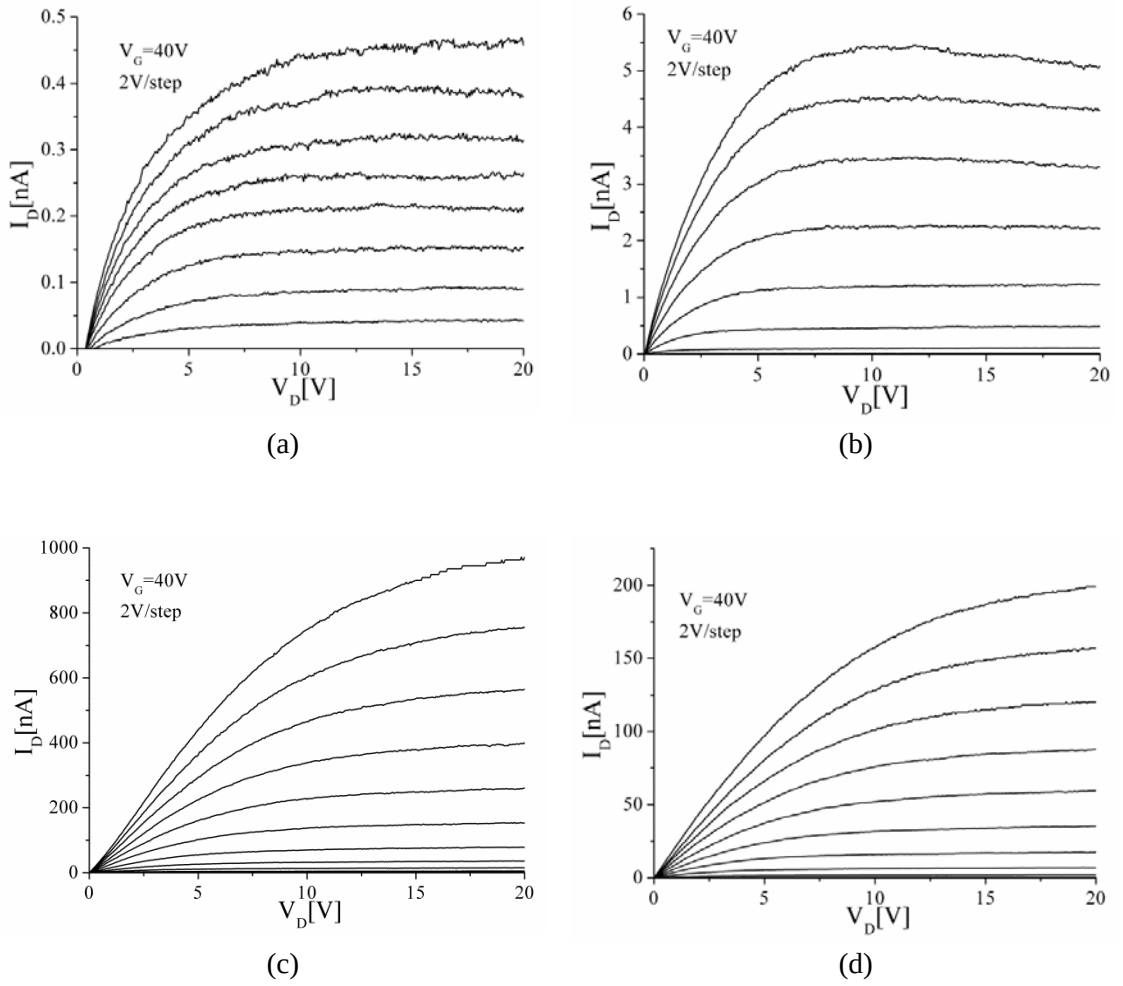


Fig. 5.21 Output characteristics of nanowire transistor with channel length of 10 μm and dual nanowire for ZnO layers deposited at temperatures of a) 150˚C, b) 170ºC, c) 190ºC and d) 210ºC. The ALD process used an initial Ar purge of 2s, 4s of oxygen plasma exposure, 1s of DEZ dose time, an RF power of 100 W, a pressure of 15 mTorr and a final Ar purge of 4s.

5.7.3 Discussion

The results in Table 5.3 indicate that the best value of field effect mobility is obtained for an ALD temperature of 190ºC and that significantly lower values of mobility are obtained at other temperatures. A comparison with the stoichiometry results in Fig. 5.7 indicates that this deposition temperature gives a stoichiometric ZnO film. To further investigate the relationship between film stoichiometry and mobility, Fig. 5.22 shows a graph of field effect mobility and Hall mobility as a function of film stoichiometry for ALD ZnO layers deposited at different temperatures. A similar trend can be seen for both field effect mobility and Hall mobility in which the values of mobility fall off sharply as the film composition departs from stoichiometry. While other factors such as surface roughness undoubtedly influence the mobility, this figure clearly demonstrates the importance of ZnO film stoichiometry in determining both field effect and Hall mobility. The fall-off of mobility is particularly sharp for the oxygen-rich sample that was deposited at 210ºC. This sharp fall-off of mobility is probably caused by the large surface roughness seen for this sample, as shown in Fig. 5.15. The results in Figs. 5.16 and Fig.5.17 also suggest that there is considerable scope for achieving higher values of field effect and Hall mobility at lower ALD temperatures by adjusting the deposition process to give more stoichiometric films. For example, at temperatures between 120 and 170ºC this could be achieved by decreasing the zinc content in the films.

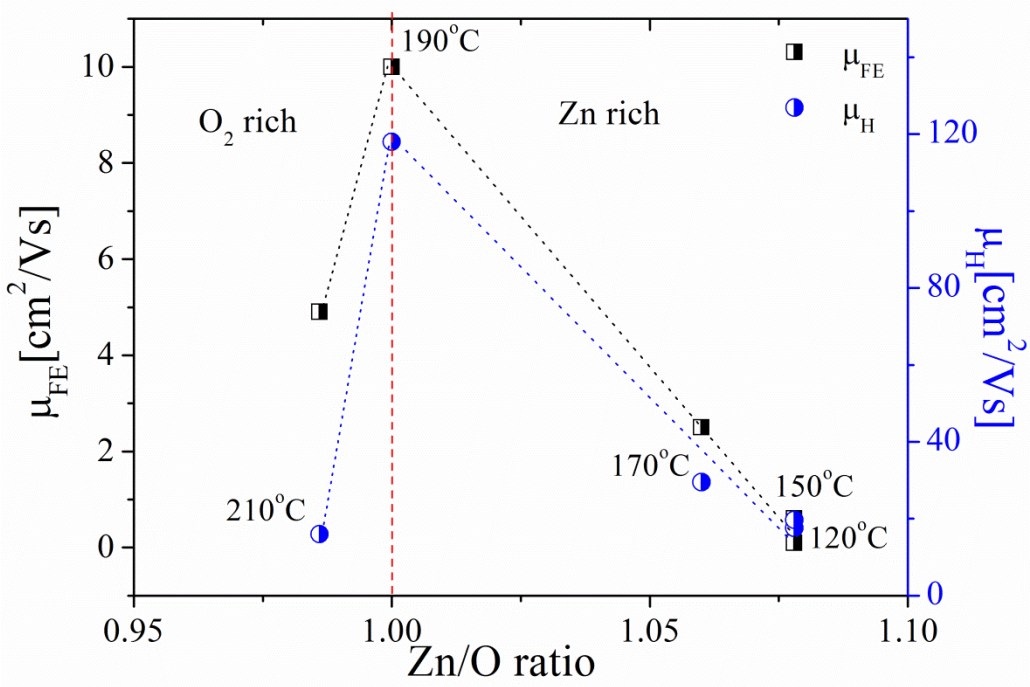


Fig.5.22 Field effect mobility and Hall mobility as a function Zn/O ratio obtained from XPS measurements. The ZnO layers were deposited using an initial Ar purge of 2s, 4s of oxygen plasma exposure, 1s of DEZ dose time, an RF power of 100W, a pressure of 15mtorr and a final Ar purge of 4s. The deposition temperature is shown at each measurement point.

Nevertheless, the ZnO NW-FET with channel processed at 190^{o}C exhibited outstanding results for top-down fabricated nanowires with a mobility of 10 cm^2/Vs. This value of field effect mobility compares with values of 1, 6.7 and 12.5, cm^2/V.s reported by Huby *et al* [20], Lim *et al* [21] and Levy *et al* [22], respectively in ZnO thin film transistors fabricated using atomic layer deposition. Despite smaller widths of the nanowire and thicker SiO_2 gate dielectric, the electrical characteristics achieved are better compared to other bottom-up NW-FETs [23-28] in terms of mobility, I_{ON}/I_{OFF} ratio and the output characteristics. These bottom-up devices always exhibit depletion mode characteristics with high carrier concentration which is difficult to control. Higher mobility values were achieved by various techniques such as passivation [23], high temperature annealing [29], ozone treatment [27] and many other techniques. However, the electrical characteristics displayed in this work represent pristine ZnO semiconductor nanowires without going through any treatments and fabricated at a maximum substrate temperature of 210^{o}C. This implies the high potential fabrication on low-cost substrates such as plastic towards various applications such as roll-on display technology and biosensing. In addition, the top-down approach is convenient in defining the nanowire positions, the lengths and geometry compared to randomly oriented nanowires produced using bottom-up approach.

5.7.4 Summary

A high field-effect mobility of 10 cm^2/Vs and I_{ON}/I_{OFF} of 2 x 10^5 were achieved for top-down fabricated ZnO NWFET at a substrate temperature of 190^{o}C. This is due to the excellent film stoichiometry. The threshold voltage decreases systematically with increasing deposition temperature from 31 to 22V due to decreasing film resistivities. At low processing temperatures, the device exhibits low carrier concentrations, high resistivity and low field-effect mobility. At high processing temperatures, devices tend to exhibit improved field-effect mobility and I_{ON}/I_{OFF} ratio. Based on these results, it can be concluded that the electrical characteristics of ZnO NW-FETs are determined by the processing temperature as this temperature has an influence on the film stoichiometry, resistivity and surface roughness. This study demonstrates that the electrical characteristics of top-down fabricated ZnO NW-FET can be controlled by the film deposition temperatures in PEALD which is not possible in bottom-up fabricated nanowires. Thus, an optimum processing temperature is very important to achieve excellent ZnO NW-FET characteristics; a processing temperature of 190^{o}C shows excellent mobility.

5.8 Conclusions

In summary, this chapter describes the various efforts to optimize the dry etch techniques as well as the PEALD deposition. ICP etch produced smoother nanowire surface with an improvement in the etch rate by 30 x from 1.64 nm/min in RIE etch to 50 nm/min in ICP etch in only CHF_3 chemistry. From the device point of view, mobility of the ICP etched NW-FET exhibited 6-fold improvement and enhanced I_{ON}/I_{OFF} ratio by one order compared to RIE etched device. In the PEALD ZnO film deposition, the O_2 plasma pressure was also optimized to 15 mTorr to produce higher film deposition rate and smoother ZnO film. With this plasma pressure, efforts to increase the deposition rate or growth per cycle [GPC] were continued by increasing DEZ precursor times. With increasing DEZ dose times, film resistivity decreased to a minimum of 2.4 Ω.cm and maximum Hall mobility achieved at 104 cm^2/Vs at DEZ dose time of 3s. This was due to fewer carbon impurities incorporated at higher DEZ dose times. It was found that the optimized range of DEZ precursor should be >1s for low resistivity and low carbon impurity as well as high mobility ZnO film.

Further investigations were executed at a fixed DEZ dose of 1s with different substrate temperatures from 100^{o}C to 210^{o}C. The GPC was constant over a temperature window from 120^{o}C to 190^{o}C. The film surface roughness, carrier concentration, carbon impurities and Zn/O ratio did not change significantly within this temperature window. At the lowest substrate temperature, the film was rough and exhibited the lowest carrier concentration which caused resistivity to increase. This was due to insufficient energy to decompose ZnO precursors at this low temperature to form monolayer ZnO film. Therefore, NW-FETs fabricated at this temperature did not display any field-effect characteristics. Meanwhile at the highest substrate temperature of 210 ^{o}C, the film indicated highest surface roughness due to the non-ideal ALD process. In addition, XPS measurements showed the highest carbon impurities at this temperature which in turn caused a deterioration of the Hall mobility due to impurity scattering. ZnO film deposited at 190^{o}C showed the highest film mobility at 118 cm^2/Vs due to enhanced stoichiometry. Other films showed either Zn-rich or oxygen- rich films indicating that film stoichiometry affects the bulk mobility. All the ZnO films deposited at different temperatures also showed high transparency >90% in the optical region.

From these films, NW-FET devices exhibit a decrease of V_{TH} systematically with increasing substrate temperature due to increasing carrier concentrations. A highest mobility of 10 cm^2/Vs and I_{ON}/I_{OFF} of 2 x 10^5 were achieved from films deposited at 190^{o}C. These excellent results are comparable and even better than other bottom-up nanowire FETs. Therefore, this study demonstrates the bright prospect of using the remote plasma ALD technique to deposit

semiconducting ZnO film using anisotropic ICP etch to form nanowire FETs which exhibit excellent electrical characteristics after various efforts in process technology optimization.

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Chapter 6

Reproducibility and Hysteresis

6.1 Introduction

The main issues that affect suffered by metal-oxide especially ZnO nanowire FETs are the electrical instabilities in air due to the presence of charged species at or near the surface of the nanowire [1-6]. Furthermore, the influence of charged or neutral adsorbed molecules has been observed to play a dramatic role on the transport properties of semiconductor nanowires [7]. These charged species cause electron trapping and detrapping on the nanowire surface hence affecting the electrical stability of the device in terms of characteristics such as hysteresis, V_{TH} shift and mobility degradation.

For example, Dayeh *et al* have shown large hysteresis and V_{TH} shift in InAs nanowire FETs [1]. Although the field-effect mobility was high, the devices suffer from the effect of moisture and oxygen in the environment. Maeng *et al* have also observed hysteresis and a maximum V_{TH} shift of 11.6 V on unpassivated ZnO nanowire FETs but reduced to 3.3 V after PMMA passivation [2]. Similarly, Hong *et al* showed a maximum hysteresis width of 35 V for unpassivated devices [8].

These nanowires were fabricated using the bottom-up approach. The large hysteresis suffered and electrically unstable characteristics in air of these bottom-up fabricated devices can be due to a poor interface between the NW and gate dielectric. Although there have been a few reports on top-down fabricated ZnO nanowire devices [9], studies on their electrical stability against environment and time are still lacking. For this purpose, ZnO nanowire FETs were fabricated using the top-down approach in which the nanowires were in defined locations and with controlled geometries. Two different studies were conducted on the same nanowire device

1. Study on stability and reproducibility of these NWFETs under different environments and against time.
2. Study on the hysteresis properties in different environments and against time

It is found that these top-down ZnO NWFETs exhibit reproducible electrical characteristics with small hysteresis compared to other bottom-up fabricated devices reported in the literature.

6.2 Experiment

Fig. 6.1 shows a schematic diagram of the top-down fabrication process. The process is similar to the fabrication process explained in Chapter 4. A 34 nm (measured by ellipsometer) layer of ZnO was conformally deposited at 100^{o}C using remote plasma atomic layer deposition (PEALD) in an Oxford Instruments Plasma Technology (OIPT) FlexAl system. The precursor used was diethyl zinc (DEZ) with an RF power of 100 W, a pressure of 15 mTorr and an O_2 flow of 60 sccm. ZnO nanowires were then fabricated using an optimized anisotropic Inductively Coupled Plasma (ICP) CHF_3 etch to form nanowires at the sides of the SiO_2 pillars as shown in Fig. 6.1(d). Aluminum source and drain electrodes were deposited by e-beam evaporation and patterned by lift-off. The Al Ohmic contacts were then annealed in a Rapid Thermal Annealer (RTA) at 350^{o}C for 2 mins.

The current-voltage characteristics of the devices were measured with an Agilent Technologies B1500 Semiconductor Parameter analyzer. All electrical measurements were done in the dark at room temperature unless otherwise specified. The first electrical measurements were done with two devices; Device 1 and Device 2 which consist of two nanowires with the same channel length, L=10 μm immediately after fabrication. Note that this is not a statistical study but rather to compare the trends of the electrical characteristics exhibited on both devices in different environments.

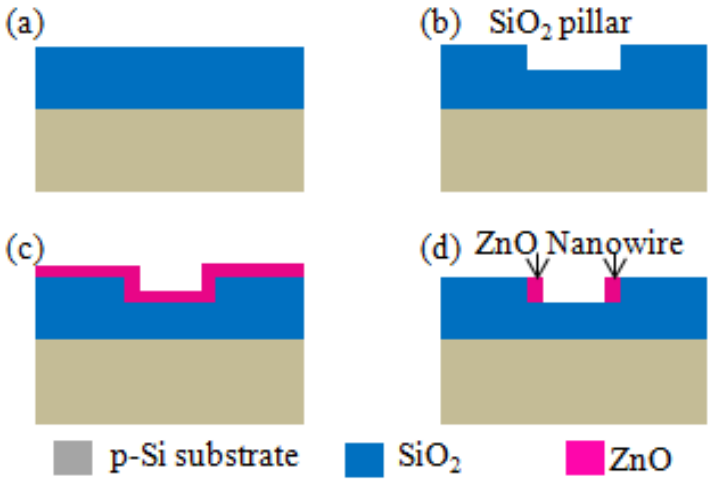


Fig.6.1 Top-down fabrication process of ZnO nanowire FET (a) a 200 nm SiO_2 thermally grown through wet oxidation (b) SiO_2 dry etched to form ~100 nm pillars (c) ZnO thin film deposited by ALD (d) anisotropic ICP etch to obtain nanowires at the side of the oxide pillars.

In order to study the effect of time, these devices were kept in ambient air for 30 days and the electrical characteristics were remeasured. Next these same devices were passivated with 4.5 μm of AZ series negative resist. In the passivation process, the devices were dried in an oven at a temperature of 120^{o}C for 10 mins to ensure the nanowire surface was dry. Then, the chip was spin coated with AZ2070 resist before soft baking at 110^{o}C and subsequently exposed under UV light. After exposure, the chip went through post exposure bake at 110^{o}C before developing to open the source and drain contacts. Now the devices were completely covered by the negative resist which is to serve as the passivation layer. The electrical characteristics were measured after the passivation process. In order to test the stability of the passivation layer, the passivated devices were kept in ambient air for another 30 days and the electrical characteristics were measured again. The resist which acts as a passivation layer was removed by rinsing with acetone and IPA and finally dried using N_2 gun. The electrical characteristics were remeasured again.

To understand the effects of oxygen adsorption on the nanowire surfaces, the same devices were then measured in vacuum at a fixed pressure of $5x10^{-3}$ mbar. After allowing sufficient settling time of 15 mins, the transfer characteristics were measured. The chronology of the electrical measurements is given in Table 6.1.

For each measurement, the gate bias was swept from +10 V to +40 V and from + 40 V to +10 V at V_D=1 V at various sweep rates. The sweep rates were 2500, 250, 100, 6, 3 and 1.2 V/s. Different sweep rates were used to introduce variable gate field strengths to observe the behaviour of defects and traps on the nanowire surface from the measured hysteresis values. In the first part of the results, transfer characteristic plots are shown with a single sweep of gate bias at a speed of 1.2 V/s in order to study the general trend of the electrical characteristics when these devices were subjected with different time and environment. In the second part of the results, transfer characteristics are shown with double sweep of gate bias at various sweep rates starting from 2500 V/s to 1.2 V/s in order to study the hysteresis characteristics of these devices.

TABLE 6.1 Electrical measurements procedure in this experiment

	Device 1 and Device 2*	**Device 2**
As fabricated electrical measurements	I_D-V_G @ V_G=1.2 V/s	I_D-V_G @ V_G=2500→1.2 V/s
After 30-days electrical measurements	I_D-V_G@ V_G=1.2 V/s	I_D-V_G @ V_G=2500→1.2 V/s
After passivation electrical measurements	I_D-V_G@ V_G=1.2 V/s	I_D-V_G @ V_G=2500→1.2 V/s
30-days after passivation electrical measurements	I_D-V_G@ V_G=1.2 V/s	I_D-V_G @ V_G=2500→1.2 V/s
After depassivation electrical measurements	I_D-V_G@ V_G=1.2 V/s	I_D-V_G @ V_G=2500→1.2 V/s
Vacuum measurements	I_D-V_G@ V_G=1.2 V/s	I_D-V_G @ V_G=2500→1.2 V/s

* Device 1 and Device 2 are dual nanowires with the same channel length, L=10 μm

6.3 Results

Fig. 6.2 shows an SEM cross-section of the ZnO nanowire after the ICP etch. The dimensions were measured as shown in Fig. 6.2. Note that all measured results were tilt corrected as the sample was tilted during the measurement. The nanowire height and width were measured at 93 nm and 38 nm, respectively. The nanowire height is determined by the height of the SiO_2 pillar and the amount of over-etch of the ZnO layer (9% in this case). The nanowire width is 38 nm at the base, which is the same as the thickness of ZnO film after deposition.

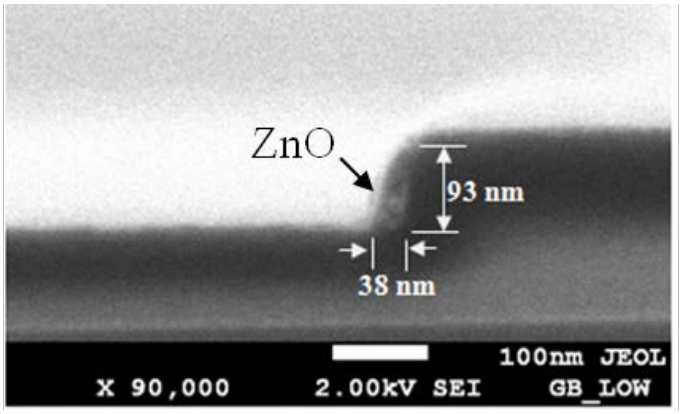
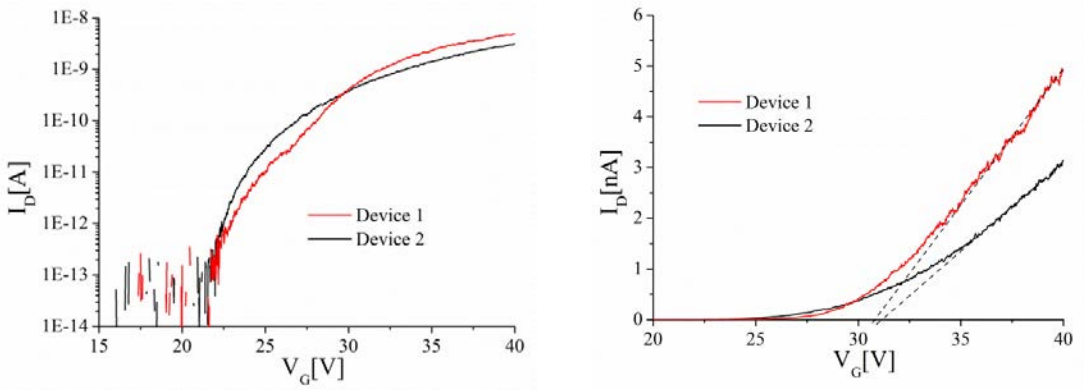


Fig.6.2 SEM cross-section of ZnO nanowire formed at the side of a SiO_2 pillar [10]

6.4 Results I-Reproducibility

6.4.1 As Fabricated Device

Fig.6.3 (a) and (b) show the transfer characteristics in semi - logarithmic and linear plots respectively for two devices; Device 1 (red) and Device 2 (black) measured on the same chip. Both devices show similar n-type enhancement mode characteristics. From the measurements, V_{TH} was measured from the linear extrapolation on the linear I_D-V_G characteristics. The field-effect mobility, μ_{FE} was extracted based on Eq. 3.4 which was derived in Chapter 3. The V_{ON} was measured at a fixed drain current, I_D of 1pA from the subthreshold characteristics.

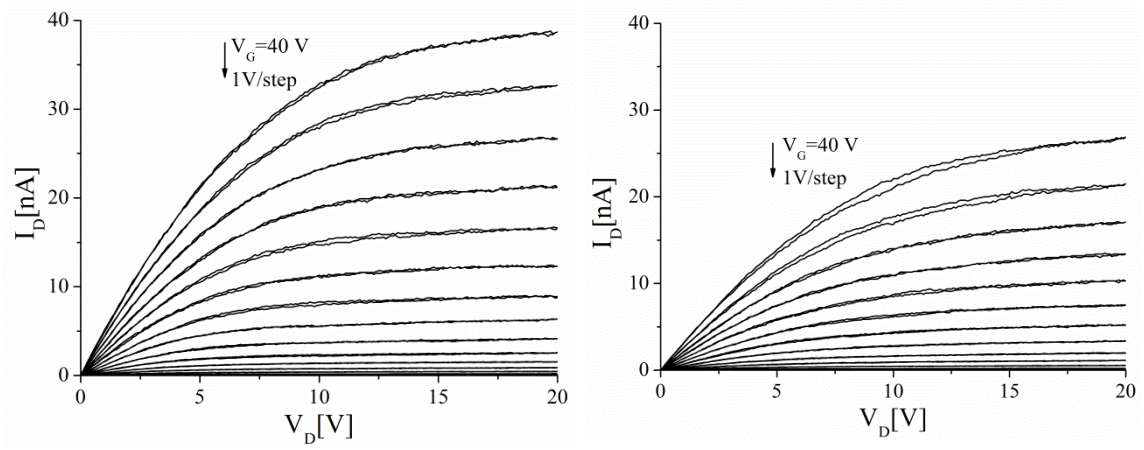


(a) (b)

Fig.6.3 (a) Subthreshold slope plot and (b) Linear plot of Device 1 and Device 2 measured after fabrication at V_D=1 V

Device 1 and Device 2 exhibit V_{TH} of 30.8 and 31.1 V, respectively while the V_{ON} are about 31 V and 23 V, respectively. The I_D measured at V_G = 40 V, V_D=1 V for Device 1 is 4.9 nA which is 58% higher compared to Device 2. The calculated mobility for Device 1 is 1.3 cm^2/Vs while Device 2 has 30% lower with 0.9 cm^2/Vs. Device 1 and Device 2 exhibit a subthreshold swing of ~1.5 V/dec and 1.02 V/dec, respectively.

Fig 6.4 shows the output characteristics of Device 1 and Device 2. Both devices show clear pinch-off and saturation. The I_{ON} is measured at V_D=20 V and V_G=40 V for both devices. The I_{ON} for Device 1 is 38.7 nA while for Device 2 was measured to be at 26.8 nA which is 30% less than Device 1.

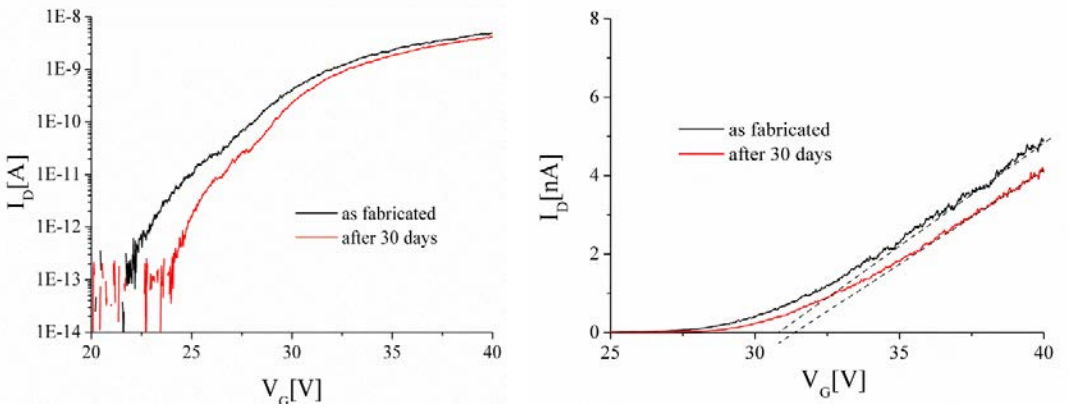


(a) (b)

Fig.6.4 Output characteristics of as fabricated for (a) Device 1 (b) Device 2

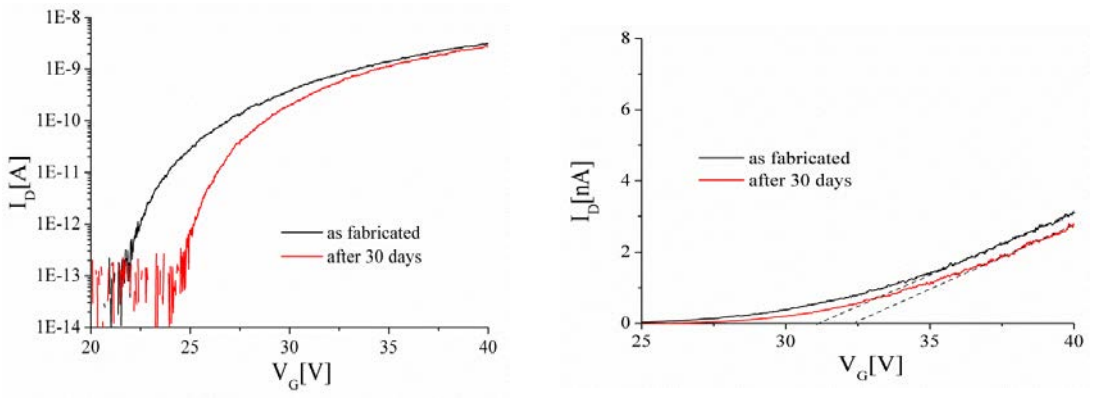
6.4.2 Time Dependence Results

These devices were kept in ambient air for 30 days and the electrical characteristics were remeasured. Fig.6.5 (a) and (b) show the plots in semi logarithmic scale and linear scale, respectively for as-fabricated Device 1 (black) and 30 days after fabrication (red). Fig.6.6 shows the same plots for Device 2. The V_{TH}, $V_{ON,}$ field-effect mobility and the measured I_D at V_G=40 V, V_D=1 V were extracted and tabulated in Table 6.2.



(a) (b)

Fig.6.5 (a) Subthreshold slope plot and (b) Linear plot of as fabricated (black) and after 30 days (red) measured at V_D=1V for Device 1.



(a) (b)

Fig.6.6 (a) Subthreshold slope plot and (b) Linear plot of as fabricated (black) and after 30 days (red) measured at V_D=1V for Device 2.

TABLE 6.2 Summary of electrical characteristics extracted from as fabricated and 30 days fabricated devices.

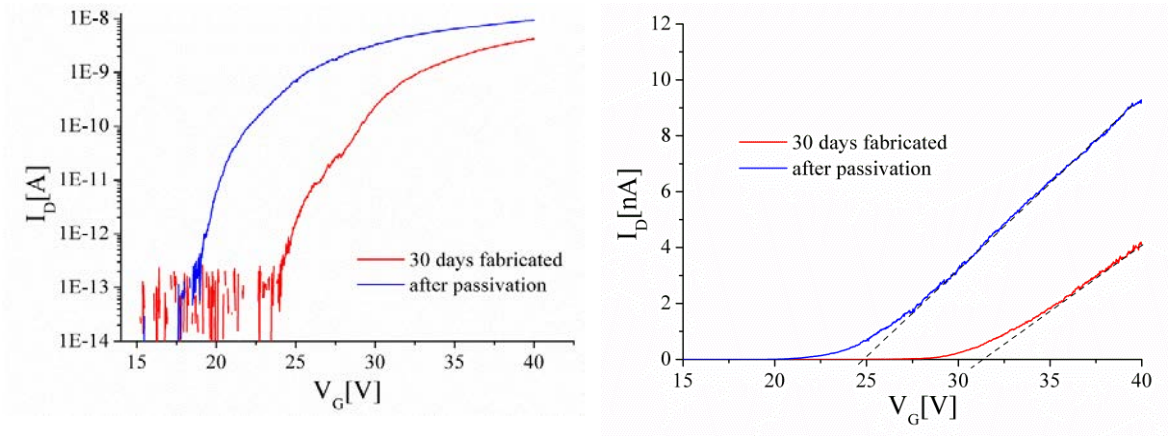
	As fabricated					30 days After				
Dev	V_{TH} [V]	V_{ON} @ 1pA [V]	I_D @ V_G=40V [nA]	μ [cm^2/Vs]	SS [V/dec]	V_{TH} [V]	V_{ON} @ 1pA [V]	I_D @ V_G=40V [nA]	μ [cm^2/Vs]	SS [V/dec]
1	30.8	22.9	4.9	1.3	1.5	31.4	24.7	4.2	1.1	1.1
2	31.1	22.5	3.1	0.9	1.02	32.3	25	2.8	0.8	0.9

Generally, V_{TH} and V_{ON} increase slightly in the positive direction after 30 days for both devices. The V_{TH} shift after 30-days was less than 5% for both devices while the shift in V_{ON} was less than 11% for both devices. There is no significant change in the measured I_D at V_G = 40 V, V_D = 1 V and the mobility. Interestingly, the subthreshold swing for Device 1 and 2 decreased from 1.5 to 1.1 V/dec and from 1.02 to 0.9 V/dec, respectively after 30-days.

6.4.3 Effect of Passivation

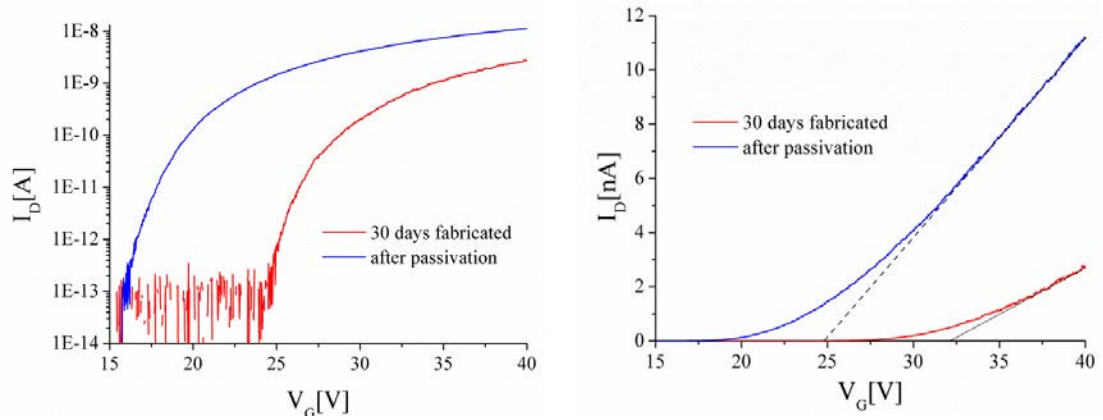
The same devices were passivated with photoresist which was described in the experiment section earlier. Fig.6.7 and Fig.6.8 show the effect of passivation on the transfer characteristics for Device 1 and Device 2, respectively. All the measured and calculated electrical parameters are tabulated in Table 6.3. The passivated devices exhibit a decrease of V_{TH} by 21 to 23% and a decrease of V_{ON} by 21 to 34 % compared to the one measured before passivation. The measured I_D at V_G = 40 V in the linear plot shows an increase by a maximum of 4-fold for Device 2 after passivation which also accounted for the mobility enhancement by

the same factor. There is no significant improvement in the subthreshold swing after passivation for both devices.



(a) (b)

Fig.6.7 (a) Subthreshold slope plot and (b) Linear plot of 30-days fabricated device (red) and after passivation (blue) measured at V_D=1 V for Device 1.



(a) (b)

Fig.6.8 (a) Subthreshold slope plot and (b) Linear plot of 30-days fabricated device (red) and after passivation (blue) measured at V_D = 1 V for Device 2.

TABLE 6.3 Summary of electrical characteristics extracted from 30 days fabricated and passivated devices

	30 days after					Passivated				
Dev	V_{TH} [V]	V_{ON}@ 1pA [V]	I_D @ V_G=40V [nA]	μ [cm^2/Vs]	SS [V/dec]	V_{TH} [V]	V_{ON}@ 1pA [V]	I_D @ V_G=40V [nA]	μ [cm^2/Vs]	SS [V/dec]
1	31.4	24.7	4.2	1.1	1.1	24.8	19.3	9.3	2.5	0.95
2	32.3	25	2.8	0.8	0.9	24.8	16.5	11.2	3.3	0.91

Fig 6.9 shows the output characteristics of both devices after passivation. The I_{ON} measured at V_D = 20 V, V_G = 40 V is at 89.5 and 96 nA for Device 1 and Device 2, respectively. These values are about 2 to 3.5 fold of increase compared to as-fabricated measured $I_{ON.}$

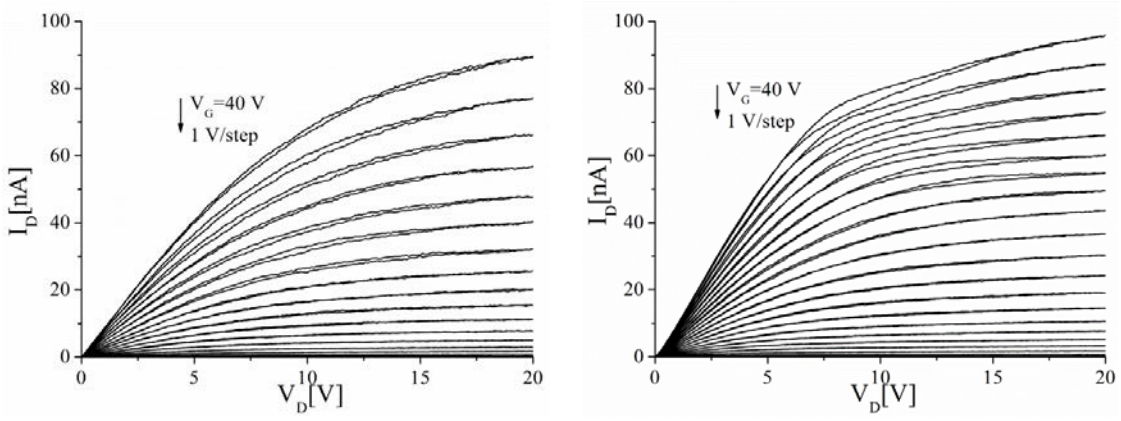
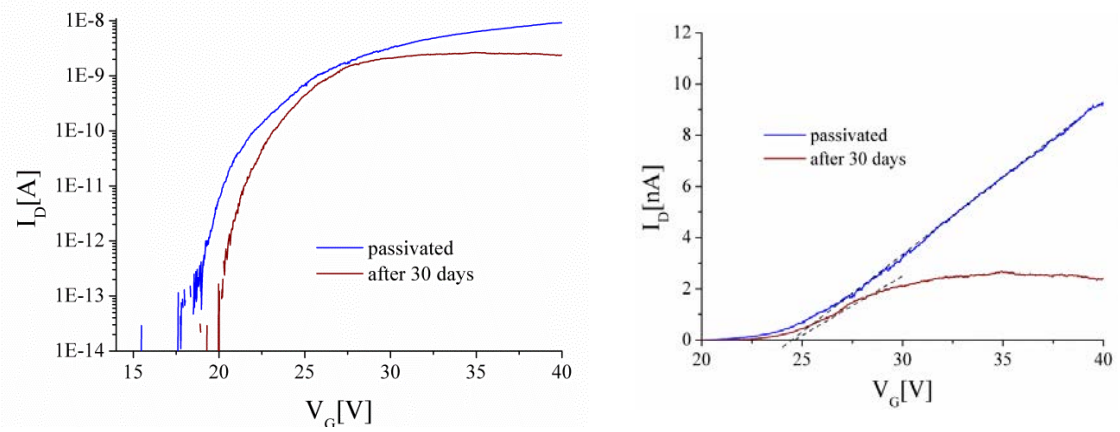


Fig.6.9 Output characteristics after resist passivation for (a) Device 1 (b) Device 2

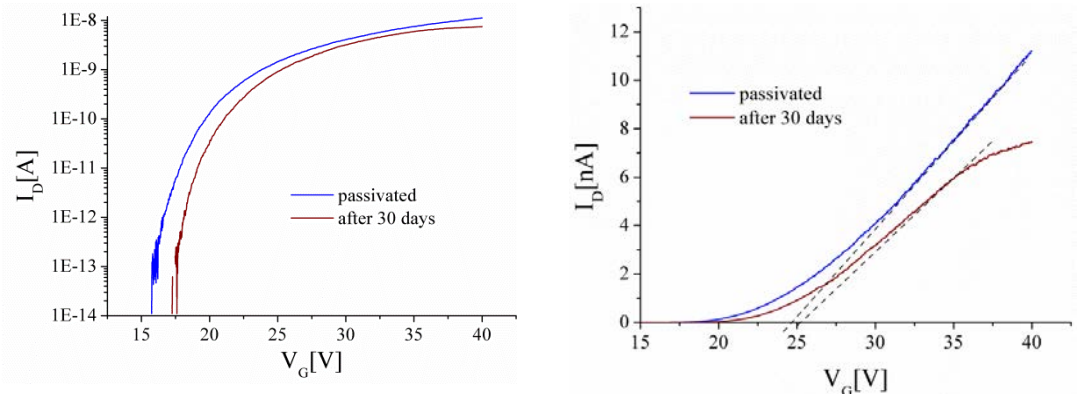
6.4.4 Effect of Passivation after 30 days

The passivated devices were kept in ambient air for another 30 days and the electrical characteristics were measured. Fig.6.10 and Fig.6.11 show the transfer characteristics of both passivated devices measured after 30 days. Table 6.4 is a summary of the electrical characteristics for devices measured after passivation and 30-days after passivation.



(a) (b)

Fig.6.10 (a) Subthreshold slope plot and (b) Linear plot of passivated device (blue) and after 30-days passivation (brown) measured at V_D = 1V for Device 1.



(a) (b)

Fig. 6.11 (a) Subthreshold slope plot and (b) Linear plot of passivated device (blue) and after 30-days passivation (brown) measured at V_D = 1 V for Device 2.

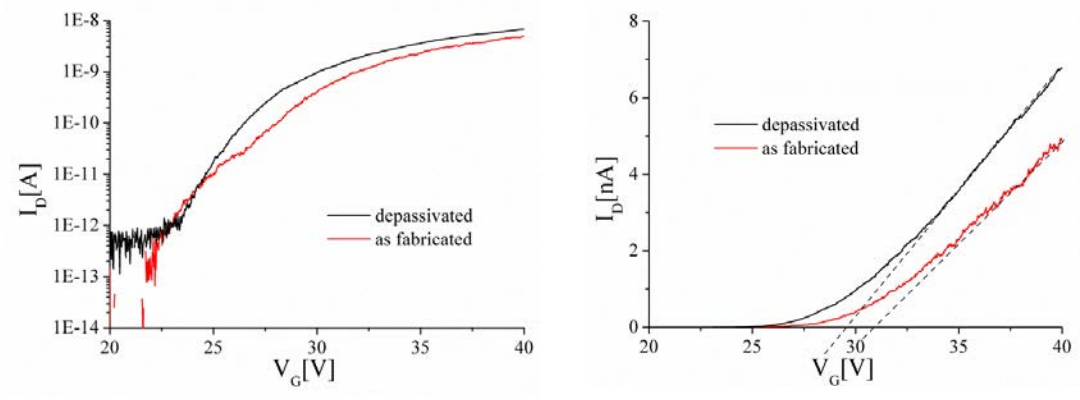
TABLE 6.4 Summary of electrical characteristics extracted from passivated and after 30 days passivated devices.

	Passivated					After 30 days				
Dev	V_{TH} [V]	V_{ON} @ 1pA [V]	I_D @ V_G=40V [nA]	μ [cm^2/Vs]	SS [V/dec]	V_{TH} [V]	V_{ON} @ 1pA [V]	I_D @ V_G=40V [nA]	μ [cm^2/Vs]	SS [V/dec]
1	24.8	19.3	9.3	2.5	0.95	24.7	20.6	2.4	1.7	0.46
2	24.6	16.5	11.2	3.3	0.91	24.3	18.2	7.4	3	0.75

After 30-days of passivation, the V_{TH} and V_{ON} are observed to shift slightly towards the positive direction for both devices. However, the measured I_D at V_G=40 V deteriorated and reduced by 34 to 74 % compared to the values on the as-passivated devices. Consequently, the mobilities for Device 1 and Device 2 are reduced by 30 % and 9%, respectively. This indicates the deterioration of the passivation layer. This could be due to the passivation layer which is resist, having light sensitive components which can react with ambient light thus creating charges and defect states in the layer. The subthreshold swing for both devices reduced after 30-days of passivation to a maximum of 50% for Device 1 and 17.5% reduction on Device 2.

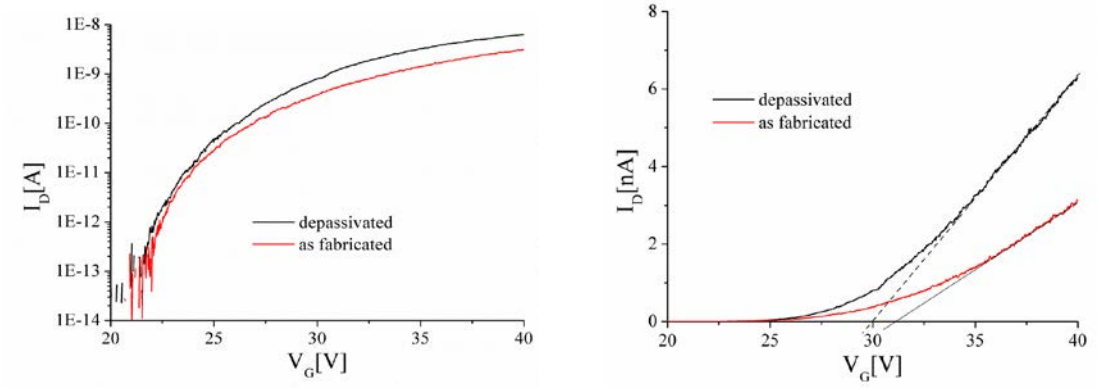
6.4.5 Effect of depassivation

The passivation layer on the nanowire devices was removed by rinsing in acetone and IPA. The reason for depassivation was to enable electrical measurements to be executed in vacuum chamber for the next step. Therefore, it is important to ensure the electrical characteristics of the devices did not change significantly after the removal of the passivation layer. Fig.6.12 and Fig.6.13 show the transfer characteristics in semilogarithmic and linear scale of device 1 and device 2, respectively after the removal of the resist.



(a) (b)

Fig. 6.12 (a) Subthreshold slope plot and (b) Linear plot of depassivated (black) and as fabricated device measured at V_D = 1 V for Device 1.



(a) (b)

Fig. 6.13 (a) Subthreshold slope plot and (b) Linear plot of depassivated (black) and as fabricated device measured at V_D = 1 V for Device 2.

The transfer characteristics measured on as-fabricated devices are included as means of comparison to verify whether the device behaviour has returned to the initial fabricated characteristics. Table 6.5 shows the various electrical parameters measured after depassivation for Device 1 and Device 2. Data measured from as - fabricated devices are also included for comparison. From these results, the V_{TH} and V_{ON} almost returned to initial values with a maximum of 3.5% of error margin. The I_D measured at V_G = 40 V and the field-effect mobility are still higher than as-fabricated devices. This could be due to incomplete removal of the passivation layer causing less surface scattering on the nanowires compared to as-fabricated devices. However, the subthreshold swing seemed to return to the measured as-fabricated values for both devices.

TABLE 6.5 Summary of electrical characteristics extracted for as-fabricated devices and after depassivation.

	As fabricated					Depassivated				
Dev	V_{TH} [V]	V_{ON}@ 1pA [V]	I_D@ V_G=40V [nA]	μ [cm^2/Vs]	SS [V/dec]	V_{TH} [V]	V_{ON}@ 1pA [V]	I_D @ V_G=40V [nA]	μ [cm^2/Vs]	SS [V/dec]
1	30.8	22.9	4.9	1.3	1.5	29.5	22.9	6.7	1.6	1.2
2	31.1	22.5	3.1	0.9	1.02	30	22.2	6.2	1.5	1.1

6.4.6 Effect of vacuum measurements

To understand the effects of oxygen adsorption on the nanowire surfaces, the same devices were then measured in vacuum. These measurements were executed in the cleanroom environment hence the vacuum measurements were compared with that measured in the cleanroom. However, there were no significant changes on the device characteristics measured in the cleanroom and in normal air environment.

After pumping down the chamber with a fixed pressure of $5x10^{-3}$ mbar, electrical characteristics were measured after allowing sufficient settling time of 15 mins. Fig.6.14 and Fig.6.15 show the electrical characteristics for both devices in air and in vacuum. The general trend which is observed for both devices is the negative shift of V_{TH} and V_{ON}. Both devices exhibit an increase of 18% in I_D at V_G = 40 V in the linear plot and 25% increase in μ_{FE} for Device 1 and 76% increase in μ_{FE} for Device 2. Table 6.6 shows a summary of electrical characteristics extracted for devices measured in cleanroom air and in vacuum for comparison.

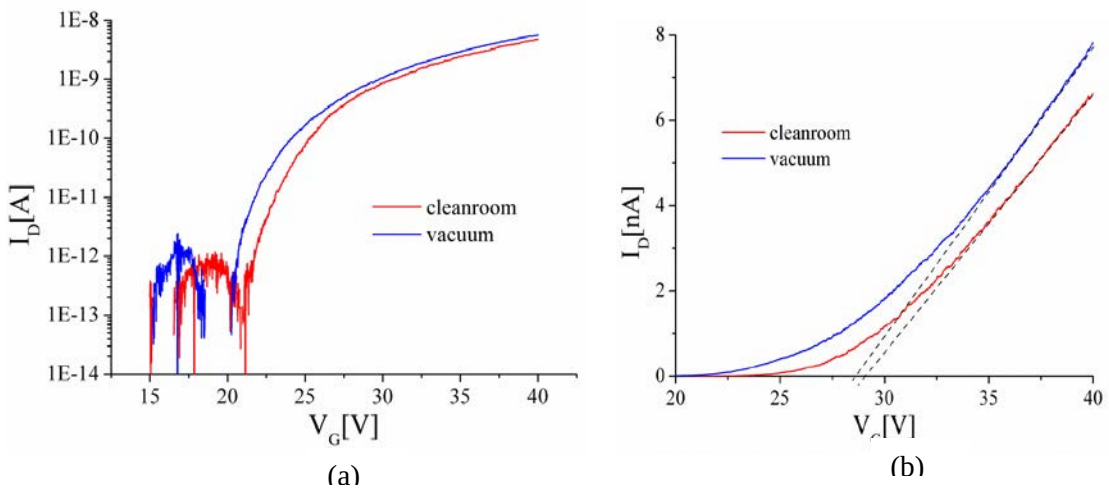
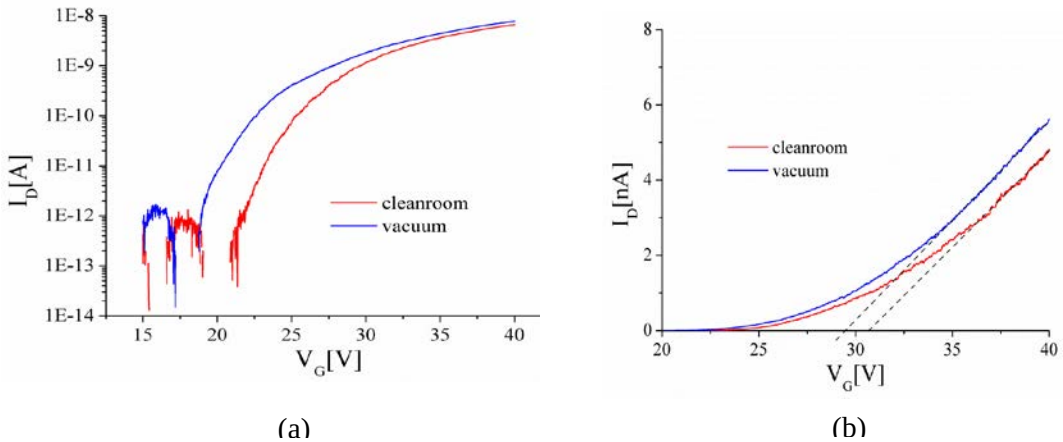


Fig. 6.14 (a) Subthreshold slope plot and (b) Linear plot measured in Cleanroom air (red) and in vacuum (blue) at V_D = 1 V for Device 1.



(a) (b)

Fig. 6.15 (a) Subthreshold slope plot and (b) Linear plot measured in Cleanroom air (red) and in vacuum (blue) at V_D = 1V for Device 2.

TABLE 6.6 Summary of electrical characteristics extracted from devices measured in air and in vacuum.

	Cleanroom Air					Vacuum				
Dev	V_{TH} [V]	V_{ON}@ 1pA [V]	I_D@ V_G=40V [nA]	μ [cm^2/Vs]	SS [V/dec]	V_{TH} [V]	V_{ON}@ 1pA [V]	I_D@ V_G=40 V [nA]	μ [cm^2/Vs]	SS [V/dec]
1	30.7	21.7	4.8	1.2	1.1	29.5	20.6	5.6	1.5	0.74
2	28.9	21.6	6.6	1.53	1.02	28.5	18.9	7.8	2.7	0.74

6.5 Reproducibility Discussion

The purpose of these measurements was to analyze the behaviour of these top-down fabricated ZnO NWFET when measured at different times and environment. This work focused on the general trend of the V_{TH} and V_{ON} shifts, the changes in I_D, SS and the mobility. It was found that both devices exhibit a similar trend hence Table 6.7 summarizes the general trend of Device 2 in chronological order. In the table, $I_{D,cal}$ is defined as the calculated drain current based on the extracted V_{TH} and μ_{FE} at V_G =40 V from the experiment.

The calculated drain current for the dual nanowire device with channel length, L of 10 μm is determined from Eq. (6.1) below which follows the typical MOSFET equation in the linear region of operation [11].

$$I_{\mathrm{D,calc}} \approx \frac{C_{dual}\mu_{FE}(V_G - V_{TH})V_D}{L^2} \qquad (6.1)$$

where C_{dual} is the gate dielectric capacitance for two nanowires.

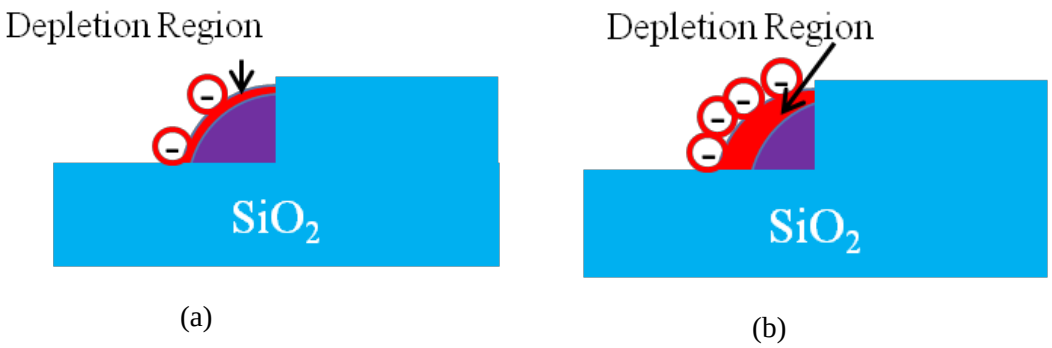
TABLE 6.7 Summary of electrical characteristics extracted for Device 2 in different environments.

Environment	V_{TH} [V]	I_D@ V_G=40V [nA]	$I_{D,cal}$ @ V_G=40V [nA]	μ_{FE} [cm^2/Vs]	SS [V/dec]
As-fabricated in ambient air	31.1	3.1	4.3	0.9	1.02
30 days after in ambient air	32.3 ↑	2.8 ↓	3.3 ↓	0.8 ↓	0.9 ↓
Passivated and measured in ambient air	24.8 ↓	11.2 ↑	26 ↑	3.3 ↑	0.91
30-days passivated and measured in ambient air	24.3	7.4 ↓	25 ↓	3 ↓	0.75 ↓
Passivation removed and measured in ambient air	30 ↑	6.2 ↓	8 ↓	1.5 ↓	1.1 ↑
Measured in Cleanroom air	28.9	6.6	9	1.53	1.02
Measured in Vacuum	28.5 ↓	7.8 ↑	16 ↑	2.7 ↑	0.74 ↓

The calculated and measured drain current agree well with less than 50% discrepancy except for measurements on the passivated device and in the vacuum environment. For passivated device, the calculated current is more than 2 fold compared to measured current. This could be due to the uncertainties in the capacitance measurement for passivated device. As mentioned in Chapter 3, the capacitance model used for the fabricated nanowire device uses the non-embedded NWFETs model with triangular cross-section. This can differ for passivated device as well as for vacuum measurements.

The general trend of the device behaviour is discussed below. As - fabricated devices exhibited n-type enhancement mode operation with V_{TH} of 31.1 V and field-effect mobility of 0.9 cm^2/Vs. After 30 days, the drain current decreased and the V_{TH} shifted to the positive gate bias direction. This phenomenon can be explained by Fig. 6.16 which illustrates the cross-section of the ZnO nanowire for as-fabricated sample and after 30-days. As mentioned in

previous studies [3][4][12-14], metal oxides strongly interact with environmental species such as O_2 and H_2O. Considering that the nanowire channel has a large density of defects such as oxygen vacancies, such defects can work as adsorption sites [12]. The oxygen adsorption at these sites is reported to happen as a two-step process: initially oxygen is physiosorbed, leading to weakly bounded molecules; then, the physiosorbed molecules capture electrons from the nanowire surface and are converted into chemisorbed and strongly bonded species in the forms of O^-,O^{2-}, or O_2^- [4][15].



(a) (b)

Fig.6.16 Schematic illustrates the ZnO nanowire surface from (a) as-fabricated sample (b) after 30-days of fabrication

When the nanowire surface was exposed in ambient air for prolonged time, more oxygen adsorbed on the nanowire surface resulting wider depletion width. As a result, the carrier concentration decreased causing the conductivity to decrease too. Subsequently, the I_D and mobility decreased as well. Interestingly, the subthreshold swing of the devices reduced after 30 days. This might be because the nanowire surface was already saturated with oxygen ions. Since the nanowire surface was full of oxygen adsorbants which might be tightly bound to the surface, surface scattering between air/nanowire surface was reduced hence the improved subthreshold swing.

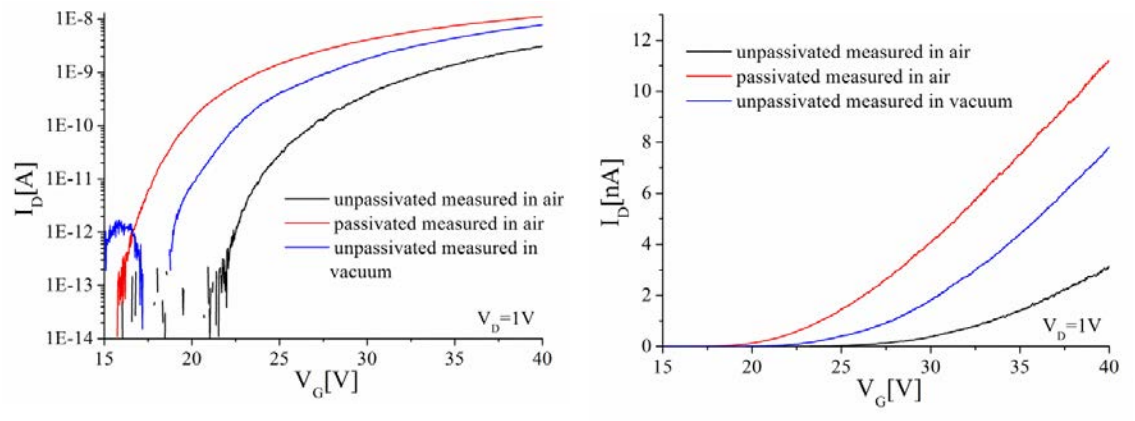
However, the V_{TH} shift of the devices over time was only a maximum of 1.2 V after 30-days. Po-Tsun Liu *et al* showed their indium gallium zinc oxide (IGZO) TFT experienced a V_{TH} shift of ~1.3 V after only 7 days exposed to the atmosphere [16]. In other work, Barquinha *et al* showed the continuous evolution of electrical characteristics on air-exposed GIZO (Ga_2O_3: In_2O_3: ZnO) TFTs and the V_{TH} shifted by ~5 V within 4-days of air-exposure [17]. The top-down fabricated ZnO NWFETs reported here did not show significant shift in the V_{TH} characteristics indicating lower density of interface defects on the nanowire surface. This might be attributed to the ZnO film quality obtained from the remote PEALD deposition.

The passivation process in this work involves a non - vacuum technique (spin-coating), soft baking to evaporate solvents, UV exposure, post exposure baking to promote cross-linking

reaction and development. Given that a non - vacuum deposition technique was used, oxygen could remain at the ZnO nanowire surface. However, the V_{TH} was shifted in a negative direction indicating the large depletion layer on the nanowire surface before passivation was removed. In fact, the I_D and the mobility were increased by 4-fold and the electron carriers were increased by 13-fold for Device 2. To infer about the effectiveness of the resist passivation layer, the passivated layer was again left in normal ambient air for 30-days. Since the nanowire surface is covered by a thick passivation layer, the surface will experience less trapping effects from the oxygen. However, after 30 days, oxygens might penetrate through the passivation layer and be adsorbed on the passivated devices thus the I_D was decreased by 34%, the mobility and V_{TH} did not change significantly.

After removing the passivation layer, the device characteristics almost return to the original behaviour of as - fabricated device with V_{TH} increased to 30 V. This value is almost the same with as-fabricated measured device. This shows that once the passivation layer was removed, oxygen continues to adsorb on the nanowire surface causing the depletion layer to widen and carrier concentration to reduce.

When these devices were brought into the cleanroom for vacuum measurements, the electrical characteristics did not change significantly in that environment. However, in the vacuum measurement, the devices exhibit a small negative shift in V_{TH} after 15 mins of pump down (5×10^{-3} mbar). This is directly related to the increase of carrier concentration by almost 3-fold. This is due to the reduction of the trapping effects of oxygen in vacuum causing the reduction in the depletion width and increase of the electrons in the nanowire channel. Thus, the mobility increased to 2.7 cm^2/Vs in the vacuum. Similar trends have been reported in other ZnO nanoscale devices when measured in vacuum [4] [13]. Although the $V_{TH,}$ mobility and the carrier concentration obtained of the passivated ZnO NWFET look similar to that of the unpassivated nanowire measured in vacuum, the subthreshold swing values are different. The transfer characteristics of Device 2 for passivated measured in air and unpassivated measured in vacuum are plotted in Fig.6.17. The subthreshold swing (SS) is determined to be 1.02 V/dec and 0.91 V/dec for the unpassivated and passivated ZnO NWFET measured in ambient air, respectively. In the vacuum, the SS improved as it decreased to 0.74 V/dec which is due to the enhancement of gate coupling effect due to less electron trapping from the oxygen molecules. These results indicate that although the passivation layer improves the mobility, there could be mobile ions in the passivation layer that promote electron trapping on the nanowire surface.



(a) (b)

Fig.6.17 I_D-V_G plot in (a) logarithmic (b) linear for as fabricated device measured in air, passivated device measured in air and unpassivated device measured in vacuum.

6.6 Summary

The top-down ZnO NWFET is found to be electrically air stable with less than 11% shift in the threshold voltage after 30-days of fabrication. Passivation improves the mobility by a maximum of 4-fold presumably due to the reduction of oxygen trapping on the nanowire surface. The change in V_{TH}, I_D and mobility were not significant when measured after 30-days of passivation. After depassivation, the device electrical characteristics return to the initial as-fabricated values which demonstrate the reproducibility of these devices. In vacuum measurements, the mobility improves by 1.8-fold due to reduction of oxygen trapping effects on the nanowire surface. These various measured results are useful to analyze early-stage aging of devices and also to infer about the instability mechanisms that present on the nanowire surface.

6.7 Results II-Hysteresis

6.7.1 As - Fabricated

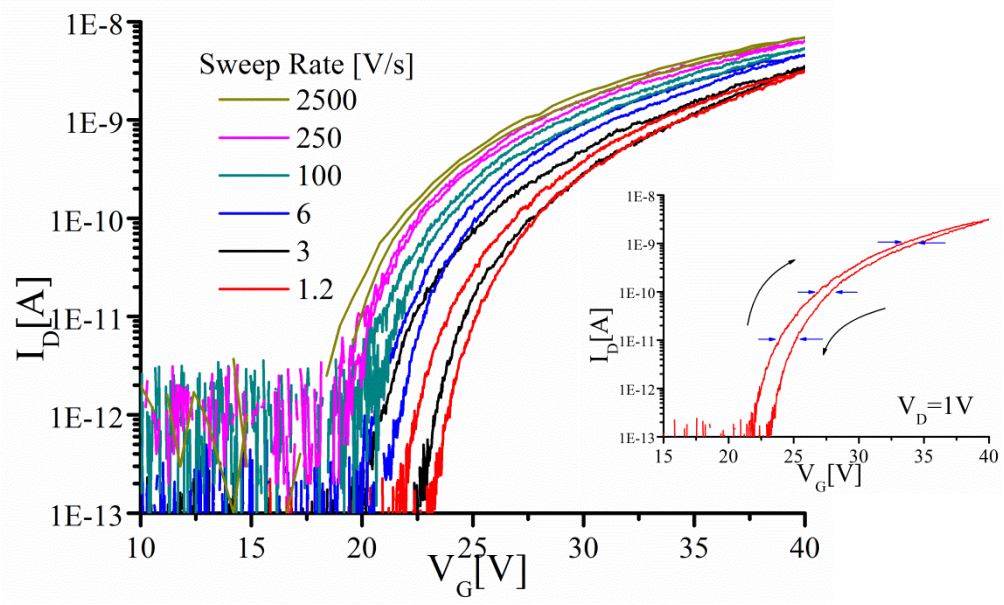
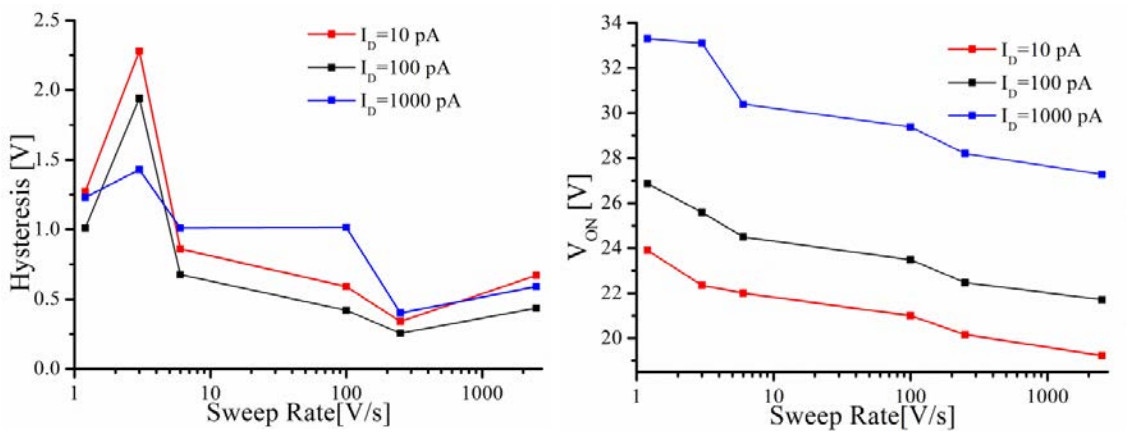


Fig.6.18 I_D-V_G curves measured on Device 2 as V_G is swept from 10 to 40 V and back to 10 V at various sweep rates from 2500 V/s to 1.2 V/s in air. Bias voltage, V_D = 1V. (inset) I_D-V_G plot at a sweep rate of 1.2 V/s. The blue arrows indicate the hysteresis width measured at different I_D level and the black arrow shows the drain current direction during forward and reverse gate bias sweep.

Fig.6.18 shows the transfer characteristics in semi - logarithmic scale when V_G was swept from 10 to 40 V then back to 10 V at various rates from $V_G/\Delta t$ = 2500, 250, 100, 6, 3 to 1.2 V/s. Hysteresis is measured to be the difference of V_G at a fixed drain current from the two sweep directions. In this case I_D is fixed at 10 pA, 100 pA and 1000 pA in order to study the general trend of hysteresis change with different V_G sweep rates. Note that the hysteresis shows clockwise direction. It is found that the hysteresis width generally wider at slow sweep rate compared to fast sweep rate. It can also be seen that as the gate bias sweep rate was decreased from 2500 to 1.2 V/s, the transfer characteristics were shifted in the positive gate bias direction. In addition, I_D at V_G = 40 V decreased with decreasing gate bias sweep rate.

Based on these plots, hysteresis values are extracted from three different I_D; 10 pA, 100 pA and 1000 pA and plotted in Fig 6.19 (a). The V_{ON} is also extracted from the subthreshold characteristics and defined to be the voltage during forward bias direction at three different I_D; 10 pA, 100 pA and 1000 pA and plotted in Fig 6.19 (b).



(a) (b)

Fig.6.19 (a) Hysteresis, (b) V_{ON} measured at three different I_D;10, 100 and 1000 pA as a function of gate bias sweep rate from 2500 to 1.2 V/s.

From Fig.6.19 (a), the hysteresis values initially increased with decreasing gate bias sweep rate for all three different I_D levels and then finally dipped at the slowest sweep rate. However, the hysteresis at the slowest sweep rate (1.2 V/s) is always larger than at the fastest sweep rate (2500 V/s). For example, at I_D=10 pA, hysteresis increased from 0.67 to 1.27 V at V_G sweep rates of 2500 and 1.2 V/s, respectively. From Fig.6.19 (b), the V_{ON} increased steadily with decreasing V_G sweep rate for all three I_D. At I_D=10 pA, the V_{ON} increased from 19.3 V to 24 V when V_G sweep rates decreased from 2500 and 1.2 V/s. The V_{ON} shift which is defined as the difference of V_{ON} between the lowest (1.2 V/s) and the highest (2500 V/s) V_G sweep rates. It indicates the dispersion of the transfer characteristics in subthreshold. From measured as-fabricated device, the V_{ON} shifts observed are 4.7 V, 5.15 V and 6.03 V at I_D = 10 pA, 100 pA and 1000 pA, respectively.

6.7.2 Effect of Passivation

Fig.6.20 shows the subthreshold plots of the same device measured after passivation. For the passivated device, a slight positive shift is observed on the transfer characteristics when the gate bias sweep rates decreased from 2500 V/s to 1.2 V/s. Fig.6.21 (a) and (b) present the hysteresis and V_{ON} measured at a constant I_D of 10 pA on the passivated device. Plots from as - fabricated device are also included for comparison. Interestingly, the hysteresis decreases slightly with decreasing V_G sweep rates for passivated device. In addition, the hysteresis does not vary significantly as observed for as- fabricated device. A maximum value of 1.6 V (at V_G=2500 V/s) and a minimum of 0.7 V (at V_G=1.2 V/s) are obtained for the passivated device. Meanwhile, the

V_{ON} increases steadily from 14.4 V to 17.7 V when the V_G sweep rate decreases. The V_{ON} shift observed is 3.4 V which is 27 % less than the as - fabricated device.

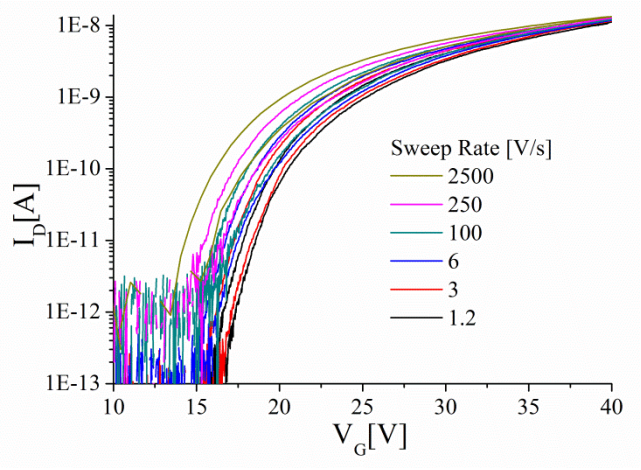
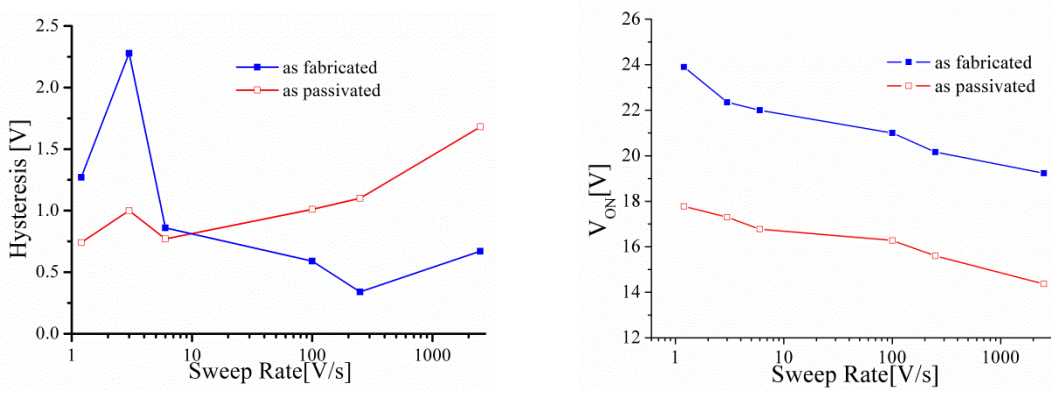


Fig.6.20 Subthreshold plots of Device 2 after passivation as V_G swept from 10 to 40 V and back to 10 V at various sweep rates from 2500 V/s to 1.2 V/s measured in air. Bias voltage, V_D = 1 V.



(a) (b)

Fig.6.21 (a) Hysteresis, and (b) V_{ON} measured at I_D = 10 pA as a function of gate bias sweep rate from 2500 to 1.2 V/s for passivated device.

6.7.3 Effect of depassivation

Fig.6.22 show the subthreshold hysteresis plots with different V_G sweep rates, measured after removing the passivation layer. The obvious observation is the whole subthreshold plots being shifted in positive gate bias direction after passivation removal. As discussed previously, the device characteristics such as the threshold voltage almost return to the original behaviour of as - fabricated devices. In this study, the hysteresis and V_{ON} values are extracted and studied

with different V_G sweep rates and compared with the as - fabricated device and plotted in Fig.6.23 (a) and (b), respectively.

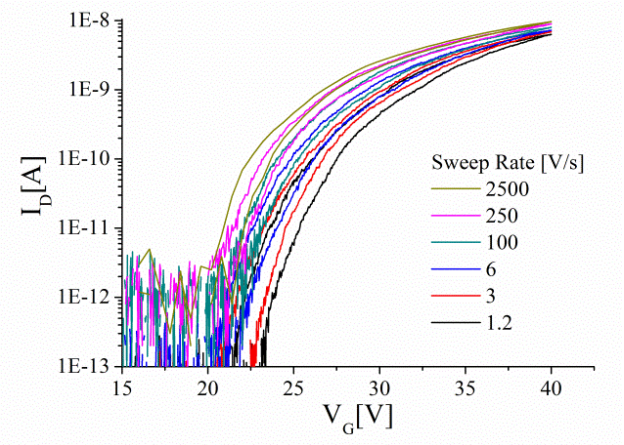


Fig.6.22 Subthreshold plots of Device 2 after removing the passivation layer as V_G is swept from 10 to 40 V and back to 10 V at various sweep rates from 2500 V/s to 1.2 V/s measured in air. Bias voltage, V_D = 1 V.

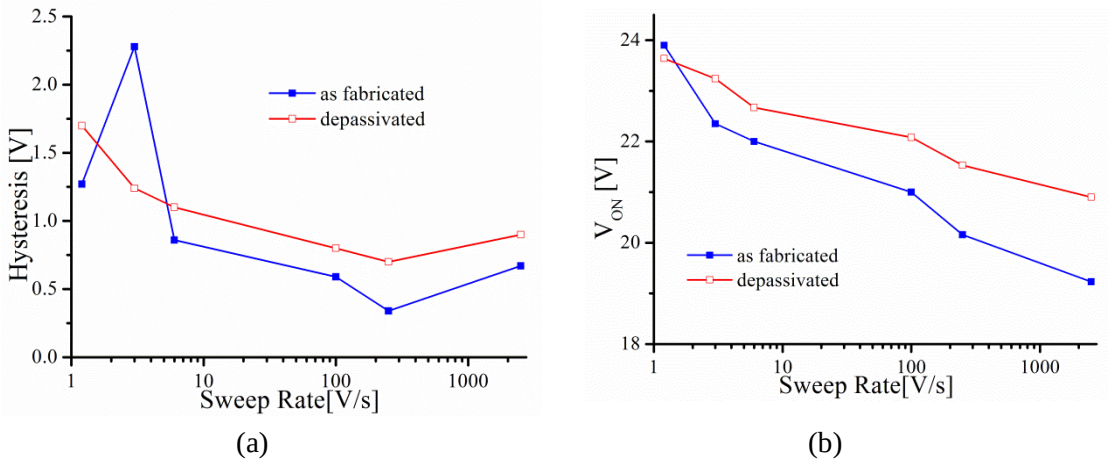


Fig.6.23 (a) Hysteresis, and (b) V_{ON} measured at I_D = 10 pA as a function of gate bias sweep rate from 2500 to 1.2 V/s measured after removing the passivation layer.

After removing the passivation layer, the hysteresis is higher at a slow V_G sweep rate compared to a fast V_G sweep rate. This trend is in agreement with the as - fabricated device mentioned previously. The hysteresis values are also generally closer to the as - fabricated device with average of 6.8% margin of deviation. Initially, the hysteresis is 0.9 V at V_G sweep rate of 2500 V/s and increases to a maximum of 1.7 V at 1.2 V/s. Meanwhile, the V_{ON} increases on average 24% after passivation removal and moves closer to the as-fabricated

device with a maximum deviation of 8%. The depassivated device also exhibits a V_{ON} shift of 2.74 V which is 42.5 % less than the as fabricated device.

6.7.3 Effect of vacuum measurements

The device was then measured in vacuum chamber and the result is shown in Fig.6.24 which shows the hysteresis plots with decreasing V_G sweep rates from 2500 V/s to 1.2 V/s. Visually observed from the transfer characteristic plots, hysteresis is not as large as seen in ambient air measurement. In addition, there is only a small positive shift in the V_{ON} . There is almost no change in the drain current with different V_G sweep rates. Fig.6.25 (a) and (b) show the analytical change of values in hysteresis and V_{ON} in which the values are compared with a depassivated device measured in ambient air. It is noticed that these parameters did not change significantly with V_G sweep rates in vacuum environment.

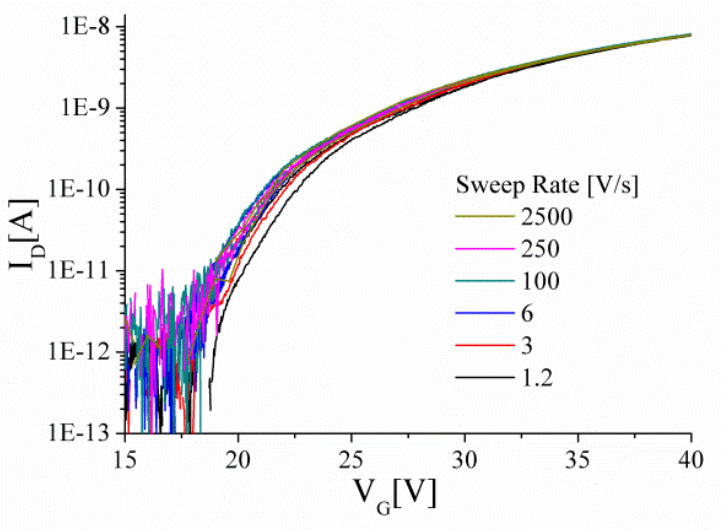
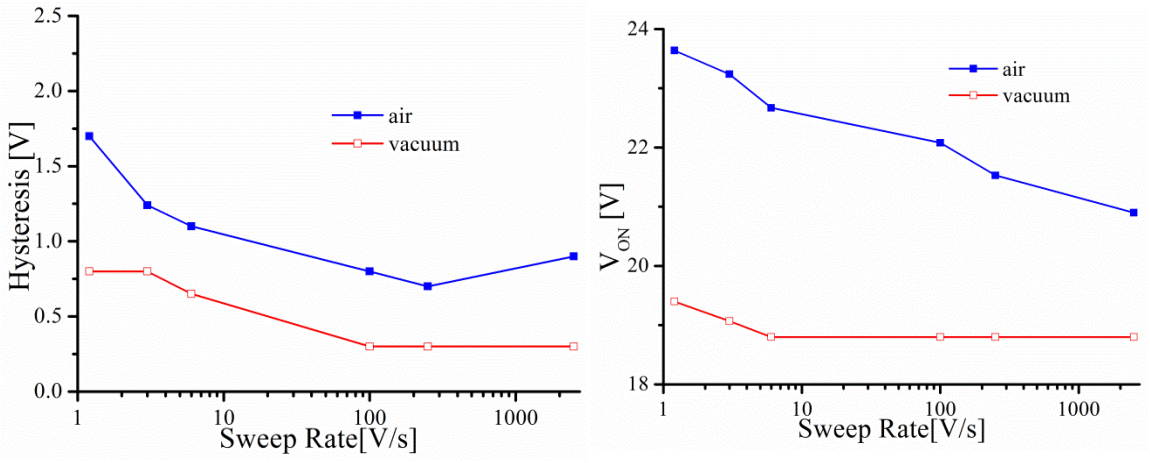


Fig.6.24 Subthreshold plot of Device 2 measured in vacuum as V_G swept from 10 to 40 V and back to 10 V at various sweep rates from 2500 V/s to 1.2 V/s measured in air. Bias voltage, $V_D = 1$ V.



(a) (b)

Fig.6.25 (a) Hysteresis, and (b) V_{ON} measured at I_D = 10 pA as a function of gate bias sweep rate from 2500 to 1.2 V/s measured in air and vacuum environment.

The hysteresis remains unchanged at about 0.3 V at V_G sweep rate of 2500 V/s, 250 V/s and 100 V/s. It then increases to 0.8 V at V_G sweep rate of 3 V/s and remains constant at 1.2 V/s. The hysteresis values are on average 50% lower compared to the air-measured device. Meanwhile the V_{ON} does not change from gate bias rate of 2500 V/s to 6 V/s. However, it increases from 18.8 V to a maximum of 19.4 V at the slowest gate bias sweep rate. However, V_{ON} is always lower compared to the value measured in ambient air at all V_G sweep rates. The V_{ON} shift is calculated to be 0.6 V which is 4.5 times lower than measured in ambient air. Therefore, unlike the case of the nanowire device measured in ambient air, the unpassivated nanowire device in the vacuum environment was not influenced by the gate bias sweep rate.

6.8 Discussion-Hysteresis

In this experiment, two phenomena were observed for the top-down fabricated ZnO NWFET. The first important effect is the hysteresis and its change with different gate bias sweep rates. The second effect is the hysteresis change in different environments. The first phenomena will be discussed first.

The hysteresis phenomena itself is explained by charge trapping and detrapping which occurs at the interface between ZnO NW and SiO_2 dielectric layer [18]. Without any bias, the nanowire surface is depleted from free carriers due to oxygen molecules adsorption. When the back gate bias sweeps from low voltage (10 V), the initially trapped electrons at the interface between ZnO NW and SiO_2 dielectric layer would be compensated by the increasing voltage thus inducing high current. Meanwhile, when the back gate bias sweeps from higher voltage

(40 V), some free electrons would be trapped at the interface between ZnO NW and SiO_2 dielectric layer, causing a positive V_{TH} shift and reduced current value. Therefore, high current can be obtained for bias sweeping from 10 to 40 V, while low current can be obtained for bias sweeping from 40 to 10 V, showing clockwise sweeping direction.

The effect of hysteresis with gate bias sweep rate is attributed to the presence of adsorbed species on the NW surface. Surface defects on ZnO NWs serve as adsorption sites of O_2 molecules [18] and these adsorbed O_2 molecules form O_2^- at defect sites and act as electron acceptors. When the nanowire FET is applied with a slower gate bias rate, more electrons on the ZnO nanowire surface are trapped by the negative species, which results in a reduction in nanowire conduction channel region by the more depleted region. Thus, the current decreases and the hysteresis increases. The V_{ON} which was defined as the gate voltage at a fixed I_D in the subthreshold plot shifts to the positive gate bias direction as observed in ambient air measurement.

From all the measurement results, the hysteresis changes significantly with the gate bias sweep rates for device measured in ambient air. Minimum hysteresis value achieved in ambient air was 0.34 V at V_G sweep rate of 250 V/s and a maximum of 2.2 V at a sweep rate of 3 V/s. This phenomena was also observed by other work and it was explained by the presence of O_2 molecules in ambient air which causes the trapping and detrapping of the conducting electrons on the nanowire channel more severe. [3][6][8][17][18]

The hysteresis and V_{ON} shift were less affected by the gate bias sweep rate on passivated ZnO NWFET device. Since during the passivation process, devices were heated at 110^oC which is a suitable temperature to remove water molecules, it can be concluded that the hysteresis and the continuous positive shift in V_{ON} with decreasing V_G sweep rate were mainly caused by the depletion of carriers by the adsorption of oxygen. The reduction of V_{ON} shift by almost 28% compared to as fabricated device indicates the degree of changes in the electrical properties is smaller after passivation. This is due to less effective oxygen adsorption on the nanowire surface.

When the passivation layer was removed, oxygen molecules start to adsorb on the nanowire surface causing electron trapping and detrapping activities to be increased as compared to during passivation. Consequently, hysteresis increased and the change in the hysteresis and V_{ON} against gate voltage bias rates was almost similar to as-fabricated device with an average of 6.8% margin of deviation. This indicates the electrical properties of the device were reproduced after more than 3 months since fabricated and kept in ambient air.

In addition, the effect of the gate bias sweep rate on the same ZnO nanowire FET device in vacuum chamber was explored. In vacuum environment, the nanowire FET has fewer oxygen ions on the surface, thus less surface depletion of electrons resulting in an increase in the current. Unlike the case of the nanowire measured in ambient air, the unpassivated nanowire device in the vacuum environment was not influenced by the gate bias sweep rate. The hysteresis and V_{ON} did not change significantly. This is because of the relative less oxygen in vacuum [6] and weakly adsorbed water molecule on NW surface can be easily removed by vacuum pumping [19]. Therefore, there is a very small effect of molecule adsorption even at different gate bias sweep rates causing hysteresis to be reduced by more than 50% at all V_G sweep rates compared to ambient air measured device. However, hysteresis was not completely eliminated. This could be caused by other strongly bounded water molecule on the SiO_2 surface at close proximity to the NWs which are difficult to remove in vacuum due to hydrogen bonding to the Si-OH groups [19].

The top-down unpassivated ZnO NWFET exhibits a maximum hysteresis of 2.2 V in ambient air. This is significantly better than bottom-up unpassivated devices [8][18]. Hong *et al* showed a value of hysteresis width of 35 V on unpassivated rough ZnO nanowire device. This value reduced to 5 V for unpassivated smooth nanowire device [8]. Zhang *et al* demonstrated a maximum hysteresis of 40 V for an unpassivated In_2O_3 device [20]. Recently, Jeon showed hysteresis of more than 5 V on bottom gate, bottom-up fabricated ZnO NWFET which reduced after air-ambient annealing at high temperatures [21]. This indicates the top-down ZnO NWFET produced from this work exhibits less hysteresis which is an important result for stable electronic and sensing device applications.

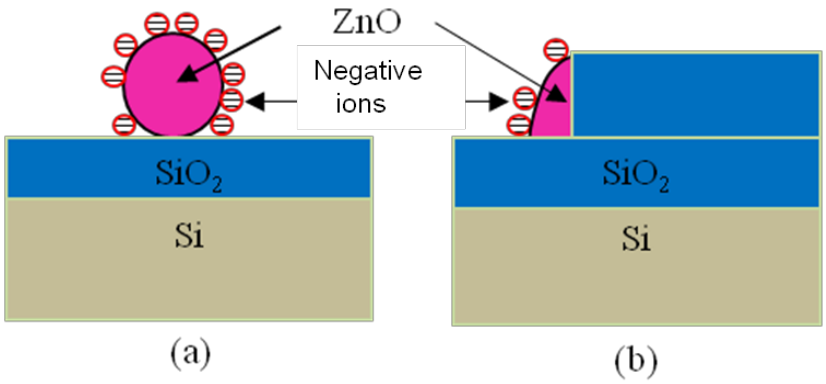


Fig. 6.26. Cross-sectional schematics of ZnO nanowires (a) bottom-up ZnO nanowire (b) top-down fabricated ZnO nanowire.

Fig. 6.26 shows the schematic cross-section diagram of a typical bottom-up ZnO nanowire and this top-down ZnO nanowire. One of the surfaces of the latter nanowire is positioned against the SiO_2 wall, which means that less surface area is exposed to the air, resulting in less influence from the adsorption of negative ions from oxygen molecules due to the applied positive gate bias. This may be the reason for the lower hysteresis observed in the device. In addition, the ZnO film is grown by ALD, which may give better control over the film quality and a better interface between ZnO/SiO_2 than that typically obtained with bottom - up grown nanowires.

6.9 Summary

The hysteresis properties of ZnO NWFETs as a function of gate bias sweep rate under different environments, including ambient air, passivation and vacuum were studied. The hysteresis is sensitively dependent on the gate bias sweep rate. Slower gate bias sweep rates result in larger depletion regions in the nanowire channel with more negatively charged ions adsorption for longer gate biasing time. This results in increase of the hysteresis and shift in V_{ON} in the positive gate bias direction. Maximum hysteresis obtained for this top-down ZnO NWFET device when measured in air was 2.2 V. However, hysteresis was less significant after passivation (maximum = 1.6 V) and when measured in vacuum environment (max=0.8 V). Nevertheless, the hysteresis obtained for the unpassivated top-down fabricated ZnO NWFET in this work is smaller compared to other bottom - up devices. This indicates better interface quality between ZnO nanowire/SiO_2 interfaces. Subsequently, this is an important feature in order to produce a reliable platform for electronic applications particularly sensing.

6.10 Conclusions

This chapter has given insights into the electrically reproducible characteristics of the top-down fabricated ZnO NWFET and its hysteresis behaviour. The top-down ZnO NWFET is found to be electrically air stable device with less than 11% shift in the threshold voltage after 30-days of fabrication. The maximum hysteresis value was 2.2 V measured in ambient air. Passivation improves the mobility by a maximum of 4-fold due to the reduction of oxygen trapping on the nanowire surface and hysteresis behaviours were less significant for passivated device. After depassivation, the device electrical characteristics return to the initial as-fabricated values including the threshold voltage and hysteresis which demonstrates the reproducibility of these devices. In vacuum measurements, the mobility improves by 1.8-fold due to reduction of oxygen trapping effects on the nanowire surface. Hysteresis reduced by 50% for all gate bias sweep rates in vacuum measurement. These results imply that these top-down nanowire

transistors are more reliable and stable which provides a promising platform for low-cost mass manufacturing of ZnO nanowire FETs for biosensor applications.

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Chapter 7

Towards Biosensing Applications

7.1 Introduction

The aim of this chapter is to demonstrate the feasibility of using the ZnO NWFET as a biosensing device given the demonstration of low temperature deposition in PEALD and promising electrical performance described in the previous chapters. This is done by using basic charged bioanalytes such as lysozyme and BSA solution. The work in this chapter has been done in collaboration with Dr. Maurits de Planque who has prepared the buffer solutions and bioanalytes for device measurements.

Nanomaterials such as quantum dots, nanoparticles, nanowires, nanotubes, nanogaps and nanoscale films [1-6], have received enormous attention due to their suitable properties for designing novel, nanoscale biosensors. For example, the dimension of nanomaterials of ~ 1-100 nm provides a perfect feature to study most biological entities, such as nucleic acids, proteins, viruses and cells as illustrated in Fig. 7.1. In addition, the high surface-to-volume ratios for nanomaterials allow a large amount of the atoms related to the biomaterials to be located at or close to the surface, for detection.

To date, a variety of nanoscale sensing techniques have been used for biological research and applications. It is vital to produce rapid and precise detection especially when monitoring living systems. Consequently, the demands of sensor architectures become challenging [3]. Several factors need to be considered such as sensitivity, specificity and low-cost when designing and fabricating nanoscale biosensors. Among diverse electrical biosensing architectures, devices based on field-effect transistors (FETs) have attracted great attention

because they are an ideal biosensor that can directly translate the interactions between target biomolecules and the FET surface into a readable electrical signal [2][3][7-9].

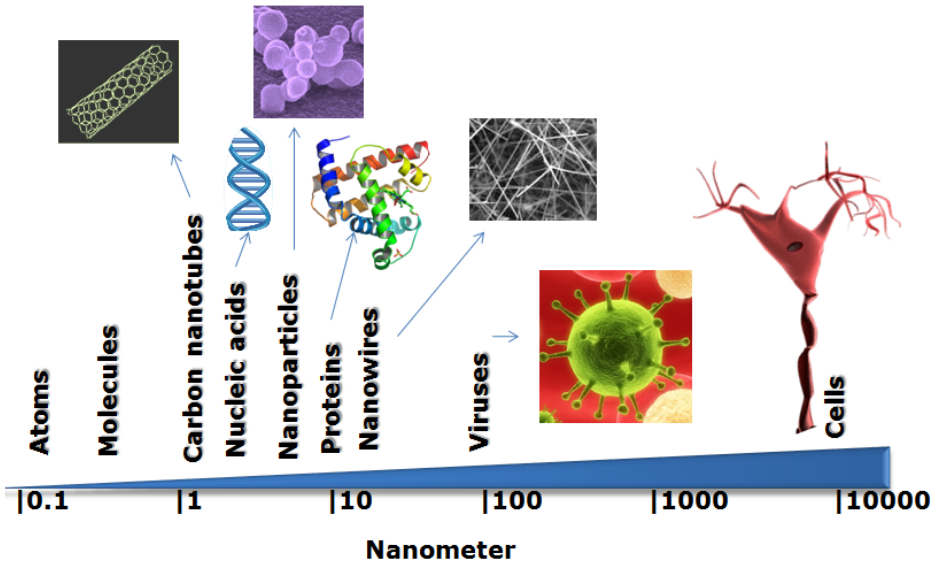


Fig. 7. 1 The sizes of nanomaterials (nanowires and nanotubes) in comparison to some biological entities, such as bacteria, viruses, proteins, and DNA [2].

The conventional complementary metal oxide semiconductor transistor has a conducting channel which is buried inside the substrate. In FET-based biosensors, the channel is in direct contact with the environment which gives better control over the surface charge due to its high sensitivity. This implies that the nanowire-based FET biosensors are more sensitive: biological events occurring at the channel surface could result in a surface potential variation of the semiconductor channel thus modulating the channel conductance. Several review papers have discussed the recent progress in ultra-sensitive biosensors formed from nanomaterials-based FETs including single-walled carbon nanotubes (SWNT) [10], graphene [11], and metal oxide NWFETs [12-15].

Among these nanomaterials, ZnO has attracted increasing attention due to its potential range of applications. Nanostructured ZnO possesses high surface area, good biocompatibility and chemical stability and is non-toxic. It also shows biomimetic and high electron communication features, making it suitable for potential applications in biosensors [16]. Researchers have studied a myriad of ZnO nanostructures for biosensor applications that have been synthesized by various bottom-up approaches [15-18]. These nanowire based sensors generally involve a complex fabrication process by manipulating and aligning a single strand of semiconducting nanowire as the FET channel between the source and drain patterns. It is difficult to achieve repeatability and manufacturability in fabrication and integration of these

devices for large sensor arrays. Therefore, the development of a very low-cost and simple fabrication route suitable for mass manufacture of nanowire sensors would accelerate their uptake as point-of-care (PoC) devices [19].

In conjunction with the cost-effective and controlled nanowire top-down fabrication process as discussed in previous chapters, these nanowire FET devices were characterized under different aqueous conditions towards the application in biosensing. A biosensor generally consists of a biosensitive layer that can either contain biological recognition elements or can be made up of biological elements covalently attached to the transducer [20]. In a typical biosensing experiment, the surface of the sensing element (nanowires) needs to be modified so that the device acquires specific recognition toward a desired analyte. This selectivity is typically achieved by anchoring a specific recognition group called receptors to the surface of the nanowires. However the main aim of this experiment is to study the modulation of the electrical conductance of the top-down fabricated nanowire FET in the absence of the bioreceptors.

7.2 Fabrication

Fig. 7.2 shows the schematic illustration of the fabricated ZnO nanowire biosensor. The fabrication process is the same as explained in Chapter 4. In this experiment, the ZnO film was deposited at 100^{o}C, DEZ dose time of 30 ms and O_2 plasma time of 4s. After the deposition, the samples were patterned by photolithography using a positive resist S1813 to cover the source/drain regions. The ZnO film was then etched anisotropically in ICP to form nanowires. The ZnO etch process development is described in more detail in Chapter 5. After the formation of the ZnO nanowires, the samples were patterned by photolithography using photoresist AZ2070. After the development, 200 nm Al was evaporated in a BAK 600 e-gun evaporator at a rate of 2.3 Å /seconds. Al lift-off was executed in 1-Methyl-2-pyrrolidon (NMP) solution. The samples were then annealed in Ar at 350^{o}C for 2 minutes to improve the Al Ohmic contact with the ZnO. Finally, the samples were coated with 4.8 μm of SU8-3005 photoresist and then patterned using photolithography to open the sensing and probing windows over the bond pads as illustrated in Fig. 7.2.

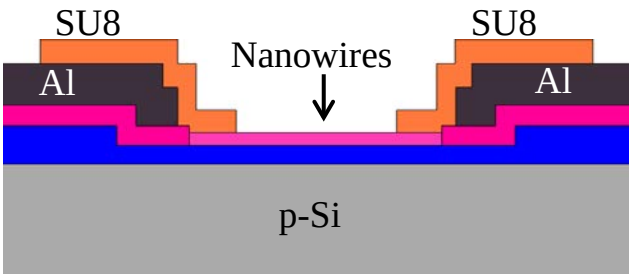


Fig. 7. 2 Schematic illustration of fabricated ZnO NWFET biosensor

For this biosensing experiment, the device consists of an array of 100 nanowires bio-FET device with channel length of 20 μm. All electrical measurements were taken using Agilent 15000 Semiconductor Parameter Analyzer in room temperature and in dark normal ambient.

7.3 Biosensing Measurements

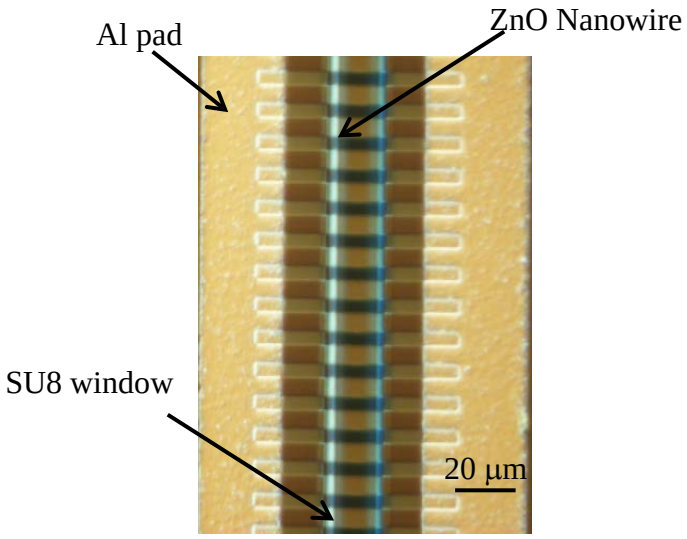


Fig.7.3 Optical image of a completed ZnO nanowire biosensor

Fig. 7.3 shows the optical image of the fabricated biosensor. A window has been opened to expose the nanowires to the solution. The nanowire length is about 20 μm and the measured offsets between the SU8 window edges and the nearest source/drain are 3.4 μm and 2.3 μm, respectively. These offsets ensure that there is no connection between the source and drain through the liquid when the sensor is exposed to the bioanalytes.

The biosensing measurements were executed on a FET device comprising 100 parallel nanowires. The nanowire width is measured to be 35 nm at the bottom of the pillar and the height to be about 100 nm. The nanowire length is 20 μm.

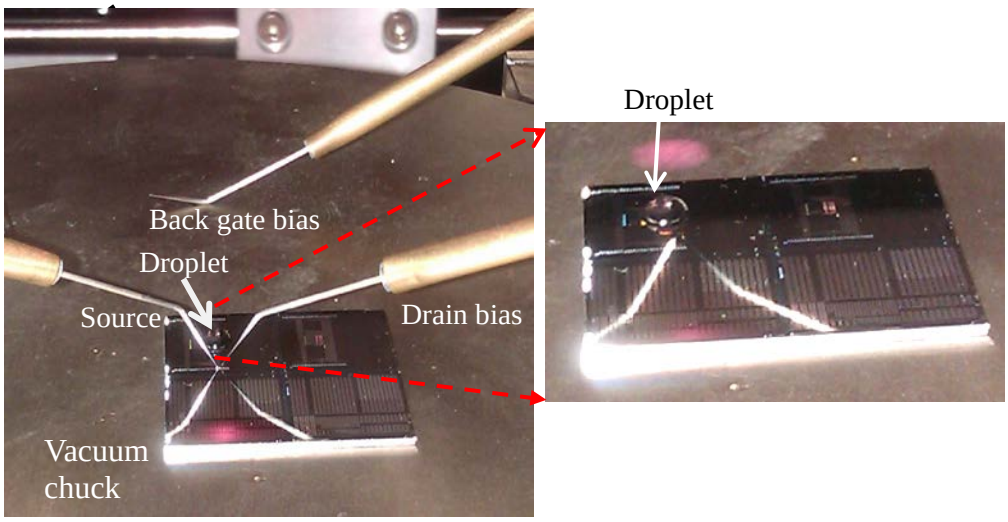


Fig 7. 4 Biosensing measurement set-ups with droplet on the nanowire surface. The measurement area is enlarged to have a better view of the droplet on the sensing device.

The biosensing measurements started by introducing a 5 μL aqueous droplet such that it covers the nanowire window as shown in Fig 7.4. Then the transfer characteristics and the output characteristics were measured. After the measurements, the nanowire surface was cleaned by depositing a drop of de - ionized water and removing it with adsorbent paper. This step was performed repeatedly for ten times to ensure the nanowire surface is completely dried before depositing a droplet of the new solution.

First, electrical measurements were done in phosphate buffered saline (PBS) solutions. The solutions were diluted in deionized water with x1000, x100 and x10 dilutions. A PBS solution with 100 ml deionized water contains 137 mM of NaCl, 2.7 mM of KCl, 8.1 mM of Na_2HPO_4, 1.5 mM of KH_2PO_4, 140 mM of salt and 10 mM buffer with pH 7.4. A PBS solution with x1000, x100 and x10 dilutions contain 0.14 mM, 1.4 mM and 14 mM of salt at pH 7.4, respectively. Electrical characteristics were measured for each PBS dilutions.

After removing these solutions with DI water and drying with adsorbent paper repeatedly, solutions of protein in diluted PBS were dropped onto the nanowire surface. The protein solutions were categorized into two types; B1 and L1. B1 solution consists of 31.5 mg of bovine serum albumin (BSA) from Sigma A3059 in 960 μL of PBS which makes 0.5 mmol/liter BSA. This protein has an overall negative charge at a pH of 7.4. Meanwhile L1 protein solution consists of 10 mg of lysozyme of chicken egg white from Fluka 62970 in

1430 μL PBS which makes 0.5 mmol/liter lysozyme. This protein has an overall positive charge at a pH of 7.4. It is important that there are more buffer molecules than protein molecules in all the solutions. Otherwise the buffer could not sustain the pH at 7.4 and the proteins may not have an effective overall charge. The chronology of the biosensing measurement steps are listed below:

i) Measurement in air
ii) Measurement in PBS x1000 solution
iii) Cleaned and measurement in air
iv) Measurement in PBS x100 solution
v) Cleaned and measurement in air
vi) Measurement in PBS x10 solution
vii) Cleaned and measurement in air
viii) Measurement in PBS x1000 solution
ix) Cleaned and measurement in B1 x1000 solution
x) Cleaned and measurement in PBS x1000 solution
xi) Cleaned and measurement in L1 x1000 solution

Note that the nanowire surfaces were rinsed in deionized water and dried with adsorbent paper several times before introducing a new solution on the surface.

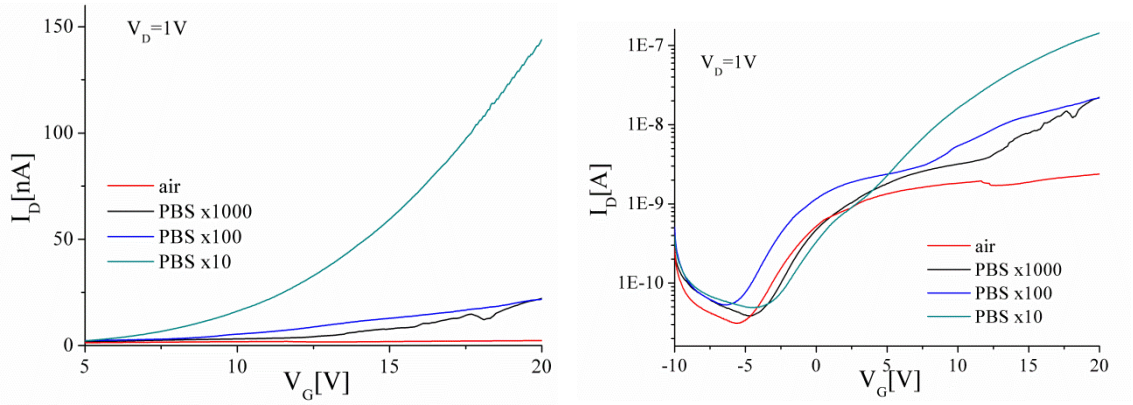
7.4 Results with PBS solutions

Fig 7.5 (a) and (b) show the transfer characteristics in linear and logarithmic scale respectively at a drain voltage of V_D = 1 V with different PBS solutions. In air, the transfer characteristics show clear n-type conduction. A good pinch-off characteristic with a threshold voltage, V_{TH} of 7.7 V is achieved. When each PBS solution was introduced into the biosensing area, the device transfer characteristics were measured within 10 secs. From the measured transfer characteristics, the device remained as n-type NWFET in all PBS solutions. The V_{TH} changed from 11.2 V in PBS x1000, 13.3 V in PBS x100 and 12.5 V in PBS x10 solutions, respectively.

The subthreshold characteristics in Fig.7.5 (b) show a kink in all measured solutions at high gate voltage (V_G > 2.5 V). The kink which is observed when measured in air could be due to the strain induced by the SU8 resist. The kink effects are more prominent in PBS solutions especially in PBS x 10 solutions. This may be due to higher mobile charges in the solution which acquire higher kinetic energy at high gate bias. This causes higher impact ionization rate of electrons in the nanowire channel. An increase in drain current, I_D is measured at V_G=20 V

as the PBS concentration is increased. This measured I_D is plotted in Fig.7.6 and it shows the plot increases exponentially with decreasing PBS dilutions. In PBS x1000 solution, the I_D increases by 9 fold compared to the I_D measured in air. Meanwhile, the I_D increases by 6.6 times when PBS x100 introduced on the nanowire surface. However, I_D was measured the highest in PBS x10 solution which exhibited an increase of 39 times the I_D measured in air.

It is important to remeasure the electrical characteristics in air after the removal of each PBS solution and before introducing new solution on the nanowire surface, to verify any drift in the I_D. The drift in the I_D is plotted in Fig 7.6. The I_D after PBS x1000 and x100 solutions exhibits a 32% increase compared to the I_D measured before dropping the solutions. Meanwhile a maximum drift of 155 % in the I_D is shown after the PBS x10 solution. This large drift in I_D could be due to incomplete removal of the PBS x10 solution in DI water.



(a) (b)

Fig. 7.5 (a) Linear I_D-V_G plots (b) Subthreshold characteristics at V_D=1V for different PBS dilutions

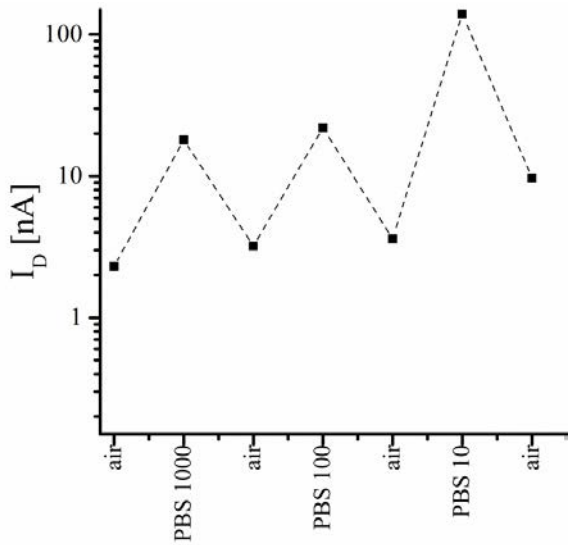


Fig 7.6 The I_D measured at V_D=1 V and V_G= 20 V during liquid and air measurements.

The output characteristics were also measured for each PBS solutions. These are plotted in Fig 7.7(a)-(d). Interestingly, the characteristics show clear pinch-off and saturation regions when measured in air as well as in liquid environment. There is a general trend of increasing I_{ON} at a fixed V_G with decreasing PBS dilutions. At V_G = 20 V and V_D = 20 V, the measured I_{ON} are 9.5 nA, 35 nA, 48 nA and 196 nA when measured in air, PBS x1000, PBS x100 and PBS x10 solutions respectively. The I_{ON} increases as the PBS concentration increases. The I_{ON} when measured in PBS x10 solution is almost 20 times the value measured in air.

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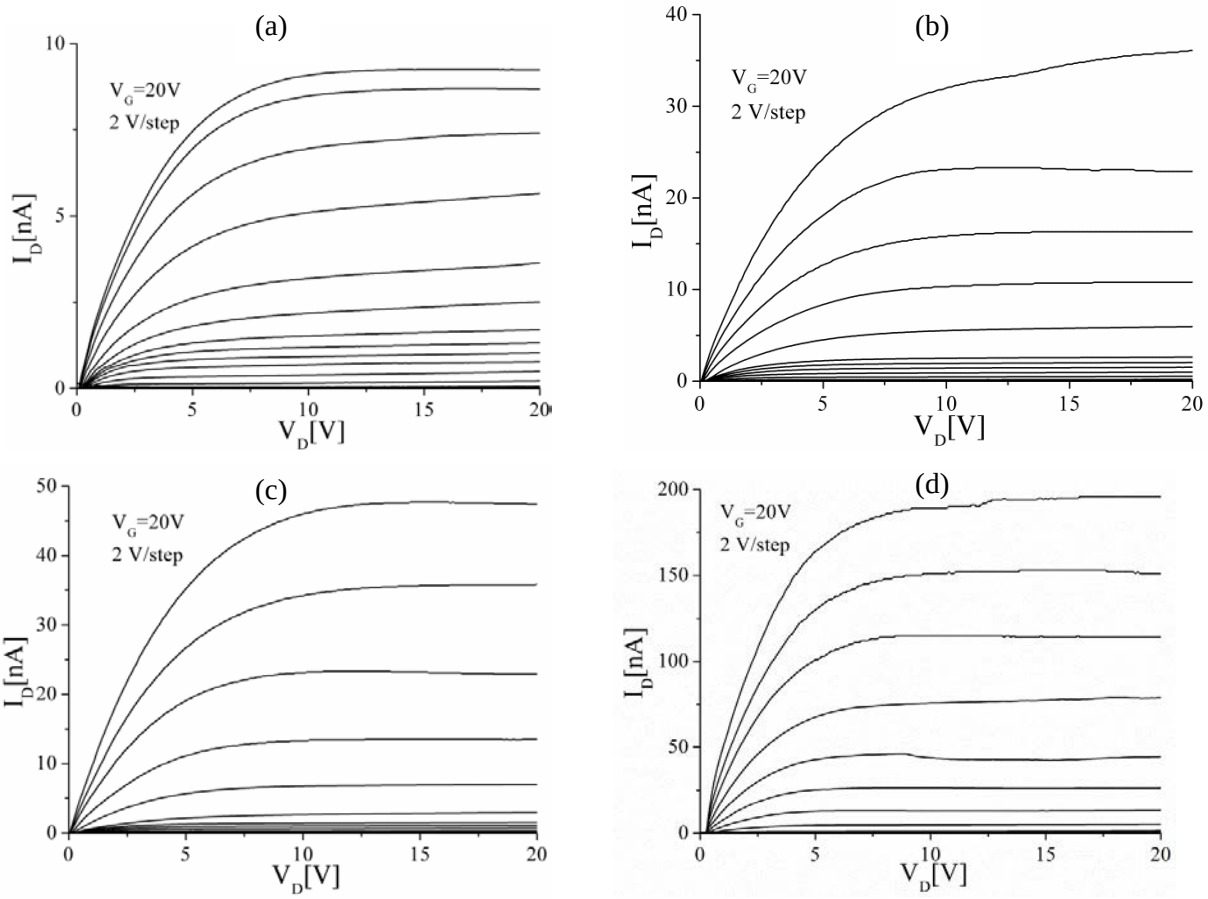


Fig 7.7 The I_D-V_D output characteristics measured in (a) air (b) PBS x1000 (c) PBS x100 (d) PBS x10 solutions

7.5 Discussion on PBS results

So far, most ZnO NWFETs have operated either under vacuum, gaseous and/or atmospheric conditions but there are very few reports on the stability of the transistors in solutions[12][24]. For all the PBS dilutions, clear n-type conduction was observed even though the ZnO nanowires were exposed to ions and H_2O molecules. The output characteristics measured in all PBS dilutions indicate that the n-type conduction was successfully maintained and can be effectively used for the sensing of biomolecules. This is important since in biosensing, the biological analytes are usually dissolved in aqueous buffers, preferably at a pH and electrolyte concentration similar to that of physiological solution. PBS is a good model for human serum which has a pH value of 7.4[2]. Therefore, the electrolyte concentration is critical experimental variables to be considered.

From computational models of the response time of a nanobiosensor in a diffusion-capture regime, calculations predict that the sensor response varies linearly with pH and logarithmically with electrolyte concentration [21]. The PBS solutions introduced in this experiment were all at pH of 7.4 but the ionic strength decreases with increasing dilutions. In this experiment, the response was determined by the change of the I_{ON} at V_G=20 V which increases exponentially with decreasing PBS dilutions. This is in agreement with the theoretical simulations [21] [22] and other experimental results [2].

The increase of I_{ON} and channel conductance with increasing electrolyte concentrations is related to the Debye length, λ_D. The Debye length is defined as the maximum distance at which an external charge can influence the NW carrier concentration [2]. The value can be calculated using the formula $\lambda_D = 0.32(I)^{-1/2}$ where I is the ionic strength of the buffer solution. In this experiment, three different PBS solutions were used which result in three different Debye lengths in each solution; 2.7 nm for x10 PBS (14 mM), 8.5 nm for x100 PBS(1.4 mM) and 27 nm for x1000 (0.14 mM) PBS solutions. The calculated Debye length is then plotted in Fig 7.8. The measured I_{ON} from the output characteristics is also included in the plot for comparison. From the plot, the Debye length decreases when the concentration of the ions increased. Meanwhile the measured I_{ON} increases with increasing concentration of ions. Thus small λ_D results in higher I_{ON} response compared to longer λ_D in the electrolyte solution.

In air, the I_{ON} is smaller compared to in PBS solutions because oxygen molecules, O_2^- and moist, OH^- from the air deplete the nanowire surface as discussed in Chapter 6. However, in

PBS solution there are phosphate ions which form the actual buffer. These ions neutralize OH^- released by other molecules in the solution thus keeping the pH of the solution constant, in this case pH 7.4. Consequently, less OH^- molecules are available to trap electrons in the nanowire surface resulting in the increase of the I_{ON}. In PBS x 10 solutions, the Debye length is smaller which means more effective screening of the charged ions. These screening causes the OH^- charged molecule to have little effect on the surface depletion phenomenon on the nanowire surface thus providing an increase of the device conductance resulting in 39 times the I_{ON} measured in air.

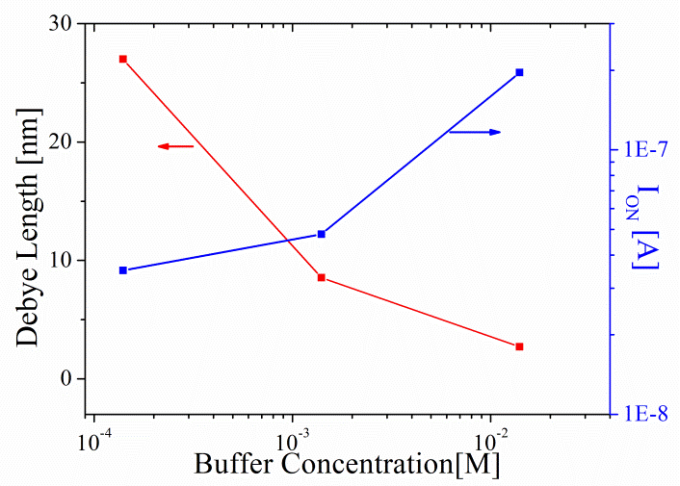


Fig 7.8 Calculated Debye lengths and measured I_{ON} for various ion concentrations in the phosphate buffer solution at pH=7.4.

When operating at a lower electrolyte concentration (PBS x1000), the OH^- ions in the solution are poorly screened, and thus, a larger depletion layer occurs as more electrons in the nanowire channel are trapped. This demonstrates that the PBS solution acts as a self-passivation layer due to its ability to screen molecules which depletes the carriers on the nanowire surface as illustrated in Fig 7.9. From these results, the top-down fabricated nanowires were continuously studied to investigate the sensing capabilities by detecting the biomolecules.

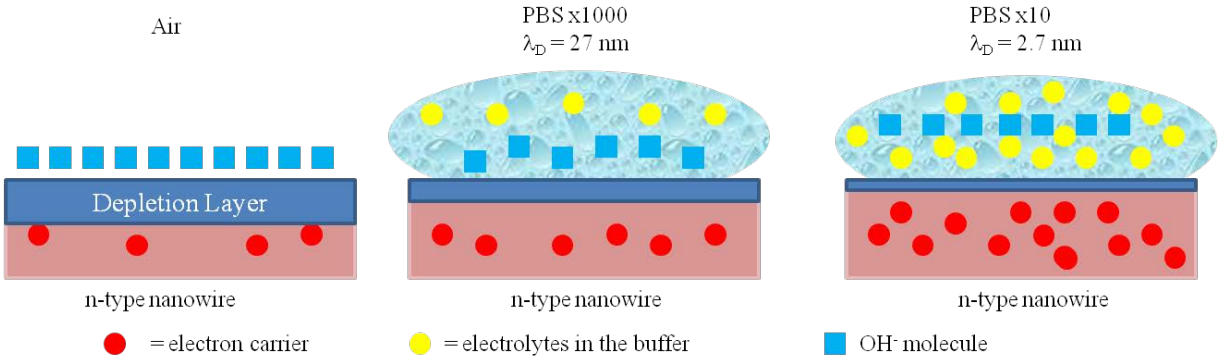


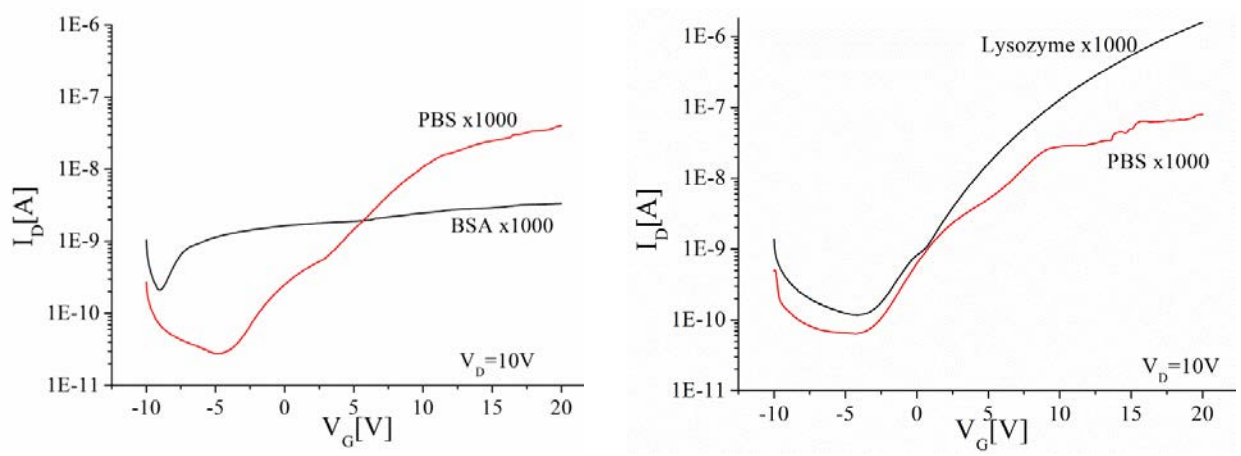
Fig 7.9 Effect of PBS solutions on the electrical conductance of the ZnO NWFET.

7.6 Results with Protein solutions

A PBS x1000 solution which has 0.14 mM salt at pH 7.4 was used as the electrolyte solution. The negatively charged bovine serum albumin (BSA; Sigma A3059) with 0.5 μM concentration dissolved in PBS x1000 solution was used as the next target for sensing, and was introduced onto the n-type ZnO NWFET. The BSA molecules are negatively charged. Figure 7.10(a) shows the transfer characteristics measured at a fixed drain voltage of 10 V, in PBS and immediately after the PBS x1000 and BSA protein introduced on the nanowire surface. The red plot is the characteristic in PBS x1000 solution and the black plot is the measurement in BSA solution. A clear reduction in I_D is observed after the introduction of negatively charged BSA of 0.5 μM. The measured I_D at V_G=20 V was 44 nA in PBS x1000 solution and the I_D was reduced by 93% when the negatively charged protein was dropped onto the nanowire surface. The subthreshold characteristics measured in BSA protein solution show a very small modulation of I_D with increasing V_G indicating a high channel resistance.

The protein solutions were rinsed in PBS x1000 solutions and de-ionized water several times before the next measurements were taken. Again, a PBS x1000 solution was introduced onto the sensing area and the electrical measurements were taken at a fixed V_D of 10 V. Next, lysozyme which is a positively charged protein from chicken egg white (Fluka 62970), was prepared in x1000 dilution which results in 0.5 μM of lysozyme of concentrations. This solution was pipetted onto the PBS x1000 droplet and again electrical measurements were taken. Figure 7.10(b) shows the transfer characteristics measured in PBS x1000 solutions (red plot) and in 0.5 μM of Lysozyme at a fixed V_D of 10 V (black). The I_D at V_G=20 V was 73 nA in PBS x1000 solution and the I_D increased to 1.56 μA after the Lysozyme protein pipetted onto the nanowire surface.

V_{ON} is defined in this experiment as the minimum voltage, V_G from the subthreshold characteristics shown in Fig 7.10. In PBS x1000 solution, the V_{ON} was measured to be at -4.7 V. When BSA protein was introduced onto the nanowire surface, the V_{ON} reduced to -9 V. Meanwhile the V_{ON} did not change significantly in positively charged lysozyme protein solution. These measurement results indicate the negative charges of BSA molecules and positive charges of lysozyme molecules induce band modulation in the channel region, which acts as a barrier and enhancement of electron conduction, respectively.



(a) (b)

Fig 7.10 I_D-V_G characteristic of ZnO NWFET at V_D=10 V measured in (a)PBS x1000 and in BSA x1000 (b) PBS x1000 and in Lysozyme x1000 solutions.

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7.7 Discussion of Protein Results

This biosensing experiment demonstrates the exposed ZnO nanowire channel in direct interaction with the biochemical species without any biofunctionalization. The mechanism of detection of the charged bio-analytes is illustrated in Fig 7.11 (a)-(c). In the first step [Fig 7.11(a)], PBS x1000 solution was dropped on the nanowire surface and the FET was positively biased at the drain and the gate electrode. The positive voltage at the gate causes the majority carriers of n-type ZnO channel to accumulate near the base of the ZnO/SiO_2 layer to facilitate a conduction path for the current to flow from drain to source.

When negatively charged 0.5 μM of BSA protein solution was introduced on the nanowire surface, the FET was positively biased at the drain and the gate electrode as shown in Fig 7.11 (b). The negatively charged BSA molecules cause a significant decrease in conductivity of the ZnO surface layer, thus, reducing the drain current. The conduction layer is

reduced to a thin region with a large depletion layer above. These BSA molecules act like a negative back-bias which in turn reducing the V_{TH}. The reduction of I_D in 0.5 μM of negatively charged BSA by 93% is higher compared to results shown from n-type CNTFET [23] in which the I_D was only reduced by about 30% in 5.7 μM of BSA.

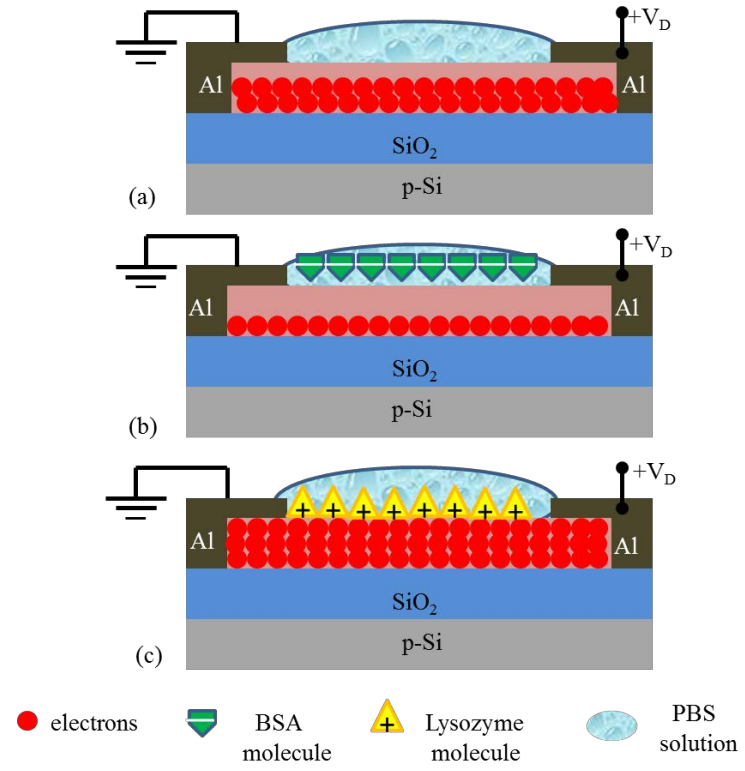

Fig 7.11 Schematic of carrier modulation mechanism in (a) PBS (b) BSA (c) Lysozyme solutions. V_D is biased in the linear region and V_G is biased > V_{TH}.

In positively charged protein solution, the positive lysozyme molecules adsorbed on the n-type ZnO surface led to the further accumulation of negative carriers within the ZnO channel as shown in Fig 7.11(c). These molecules act like a positive back-bias causing an increase in the current flow by almost 21 times than the initial current which is from I_D of 73 nA to 1.56 μA.

7.8 Conclusions

An n-type ZnO NWFET consisting of 100 nanowires in a device was fabricated. The device exhibits n-type characteristics not only in air but also in solutions. Electrical measurements in buffered solutions show higher drain current compared to air with increasing electrolyte concentrations. This is due to the effective charge screening from the OH^- molecules (shorter Debye length) which means that the solution itself acts as self-passivation layer on the nanowire

surface. The negative charged protein molecules in buffer solution were successfully detected by the channel conductance modulation where the I_D reduced by x12. Lysozyme molecules contains positive charge in buffer solution were also successfully detected with an increase of I_D by x21. This experiment shows the possibility to use the same biosensor chip several times in different solutions to produce electrical read-outs according to the charged molecules present on the nanowire surface. This demonstrates ZnO as a feasible material for biosensing. This top-down fabrication approach with low temperature film deposition is a promising technology for future low-cost mass manufacturable sensors for health care and biomedical research.

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Chapter 8

Conclusions and Future Outlook

8.1 Conclusions

ZnO is an interesting material due to its transparency, non-toxicity, surface sensitivity to various environments and the possibilities to deposit at low temperatures (< 200^{o}C). This thesis has demonstrated the fabrication of ZnO nanowire field-effect transistors from a top-down method which consists of ZnO film deposition, conventional optical lithography and anisotropic dry etch. This approach is based on thin film transistor (TFT) technology; which is commonly used in flat panel displays. The freedom to control the nanowire locations, lengths and sizes without the problems of employing the transfer techniques necessary for bottom-up technique makes the fabrication more cost-effective and mass manufacturable.

This thesis reports the feasibility of remote plasma enhanced ALD (PEALD) technology to deposit semiconducting quality of ZnO film. The remote PEALD technique offers flexibility in controlling the flow of remote oxygen plasma, pressure and the RF plasma to obtain the desired film characteristics. Consequently, defects which are associated with impurities can be controlled in the ZnO film even at low temperatures. This important feature remains a challenge in low temperature thermal ALD which uses water as oxidant.

Measurement results of transfer and the output characteristics always yielded n-type enhancement mode FET. Transistors with channel lengths in the range 18.6 to 1.3 μm and array of 16 nanowires have been fabricated using the preliminary non-optimized PEALD deposition at 150^{o}C and anisotropic RIE etch. The device with channel length of 8.6 μm exhibited a field effect mobility 0.5 cm^{2}/Vs and a respectable I_{ON}/I_{OFF} ratio of 2×10^{6}. A breakdown voltage of ≥ 75 V has been achieved at all channel lengths which is ample for applications such as active-matrix display electronics. Well-behaved electrical characteristics were obtained and the drain current scales as 1/L, as expected for long-channel FETs.

The significant progress highlighted in the early work encouraged further research efforts to address the technical challenges and to explore the technology challenges. One key issue is the field effect mobility. The low field effect mobility from early work shows the need for the remote PEALD approach and dry etch process optimisation. Realizing the low field effect mobility achieved in the early work, optimizing the dry etch and film deposition is important to realize devices for high performance applications. It was demonstrated that using the same CHF_3 chemistry, ICP etched nanowires have field-effect mobility higher by x6 compared to RIE etched device. ICP etch produced smoother nanowire surface with an improvement in the etch rate by 30 x from 1.64 nm/min in RIE etch to 50 nm/min in ICP etch. This implies roughness on the surface of the nanowires that can cause a detrimental effect on the field-effect mobility of the device.

For the remote PEALD technique, it was shown that higher growth per cycle (> 1 Å/cycle) and smoother ZnO films can be achieved by reducing the oxygen pressure during the remote plasma oxidation cycle. Using this optimized pressure at 15 mTorr, self - limiting ALD growth was observed with increasing DEZ dose times. Based on this investigation, an optimized range of DEZ precursor was found to be > 1 s for low resistivity and carbon impurity as well as high mobility. When investigating the effect of substrate temperatures at a DEZ dose time of 1s, the ALD deposition window was achieved at a temperature range from 120 to 190 ^{o}C. At 190^{o}C, the film exhibited stoichiometric (Zn/O = 1) with the highest Hall mobility of 118 cm^2/Vs and highest field effect mobility of 10 cm^2/Vs. Other films which were either Zn rich or oxygen rich, showed low Hall and field effect mobilities. This indicates that the film stoichiometry affects the bulk and device mobility. The electrical results from this pristine state of the nanowires demonstrated the potential for high performance top-down fabricated NWFETs. In addition, the ZnO films consistently showed high optical transparency of > 90% regardless of the substrate temperatures during the remote PEALD deposition.

This work has also demonstrated the electrical reproducibility of NWFET characteristics measured in ambient air. To date, the reproducibility of electrical measurements of nanowire devices is largely absent particularly for top-down fabricated nanowire transistors. This device is shown to be electrically air stable with less than 11% shift in the threshold voltage after 30-days of fabrication. However, the passivated device exhibited a threshold voltage shift of only 2% after 30 days. In addition, passivation improves the field effect mobility by a maximum of 4-fold. The threshold voltage shifted in the negative direction from 32.3 V before passivation to 24.8 V after passivation. Upon removing the passivation layer, the threshold voltage returned to the as - fabricated value which demonstrates the reproducibility of the electrical properties. Unpassivated device measured in vacuum showed a mobility improvement by 1.8 fold.

Results for the hysteresis behaviour on top-down fabricated ZnO nanowire devices have been reported for the first time. Hysteresis is sensitively dependent on the gate bias sweep rate. The maximum hysteresis obtained for this top-down ZnO NWFET device was 2.2 V, 0.8 V and 1.6 V when measured in ambient air, vacuum and after passivation, respectively. The hysteresis obtained for the unpassivated top-down fabricated ZnO NWFET in this work is smaller compared to other bottom up devices. Both voltage shift and hysteresis are associated with fluctuations of film quality due to deposition method and surface chemical stability of the nanowire transistors in ambient air. These characteristics are also indication of measurement accuracy thus consequently imply that these nanowire transistors are more reliable and stable which provides a promising platform for the low-cost mass manufacturing of ZnO nanowire FETs for various electronic applications.

ZnO nanowire biosensors were successfully fabricated using the same top-down technology with 100 parallel nanowires and a channel length of 20 μm. These devices consistently showed n-type behaviour not only in air but also in different solutions. The BSA molecules with negative charges in buffer solution and Lysozyme molecules with positive charges in buffer solution were successfully detected via channel conductance modulation on the NWFET. All results of this work are summarized in Fig.8.1.

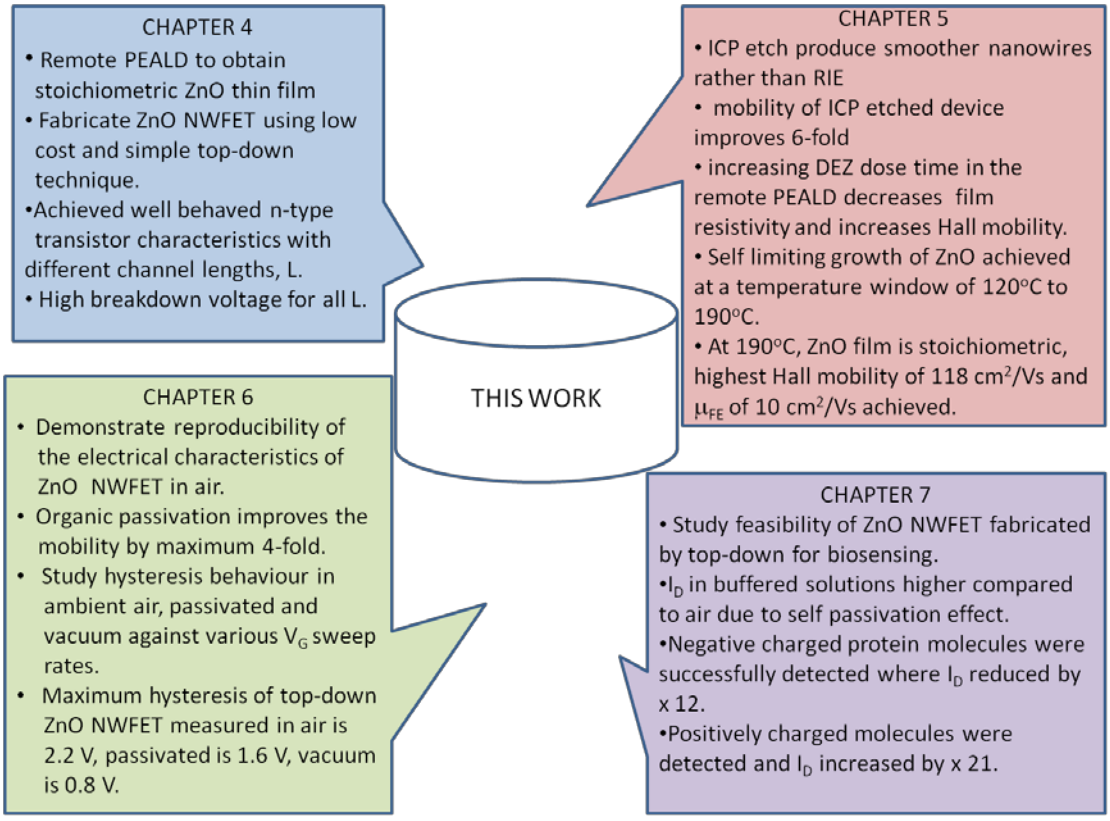
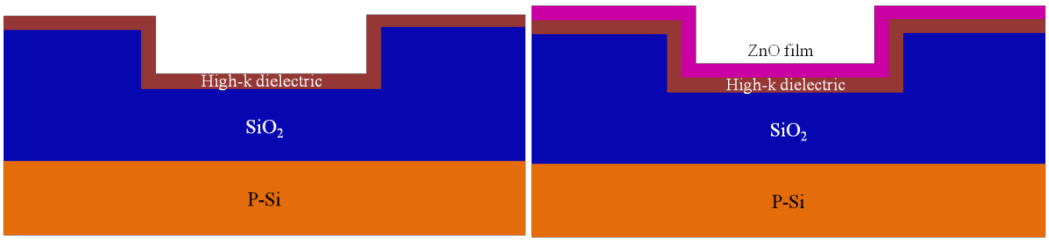


Fig 8.1 Illustration of work done in this thesis

8.2 Future Outlook

While the enhancement in the device characteristics was shown, it is believed that there is room for further improvement. Future recommendations are listed below.

- **Exploring different gate dielectric materials such as Al_2O_3 and HfO_2.**
  The gate dielectric was etched to form oxide pillars before ZnO PEALD deposition. There could be defects or traps which were caused by the RIE etch during the oxide pillar formation, which could induce hysteresis. Further work is needed to investigate hysteresis behaviour if other dielectrics such as Al_2O_3 or HfO_2 are deposited onto the SiO_2 layer after the RIE etch, as shown in Fig. 8.2 below. In this case, these dielectrics could possibly act as passivation layers from the previous etch damage. It has been reported that an etch of the native silicon oxide followed by passivation, eliminated hysteresis in Si NWFETs [1]. Thus, the deposition of ZnO film could be continuously executed in the same chamber after ALD deposition of the high-k gate dielectric. Consequently, this will avoid any exposure of the surface of the high-k dielectrics to air before ZnO deposition.



(a) (b)

Fig.8.2 Schematic Illustration of (a) high-k dielectric deposition on the RIE etched SiO_2 pillars (b) ZnO film deposition after high-k dielectric deposition in the same remote PEALD chamber.

- **Effect of ZnO nanowire polarity on the device characteristics**
  It was shown by Kim *et al* in their bottom-up grown device that the oxygen - poor nanowire device exhibited an I_{ON}/I_{OFF} ratio of 10^7 which is 3 orders of magnitude more than the oxygen rich nanowire device [2]. In addition, the stability of the oxygen rich device degrades in which the device experienced a large threshold voltage shift and hysteresis after more than 50 days. There was no experimental evidence of the polarity of the ZnO nanowires in this experiment. Due to the random nature of the bottom-up grown nanowires, the channel length and the diameter of both oxygen rich and oxygen poor devices were different during the measurement. In this work, the nanowire polarity

is still ambiguous after the dry etch since the nanowire is not covered by photoresist during the dry etch. Therefore, it would be interesting to investigate the effect of polarity on the top-down fabricated ZnO nanowire device. This can be achieved easily by depositing a monolayer of Zn (for Zn rich) and oxygen (for oxygen rich) in the PEALD after the nanowire dry etch as shown in Fig.8.3. Subsequently, the stability of these two nanowire devices with different polarities can be studied by addressing the hysteresis and threshold voltage shift as shown in this work.

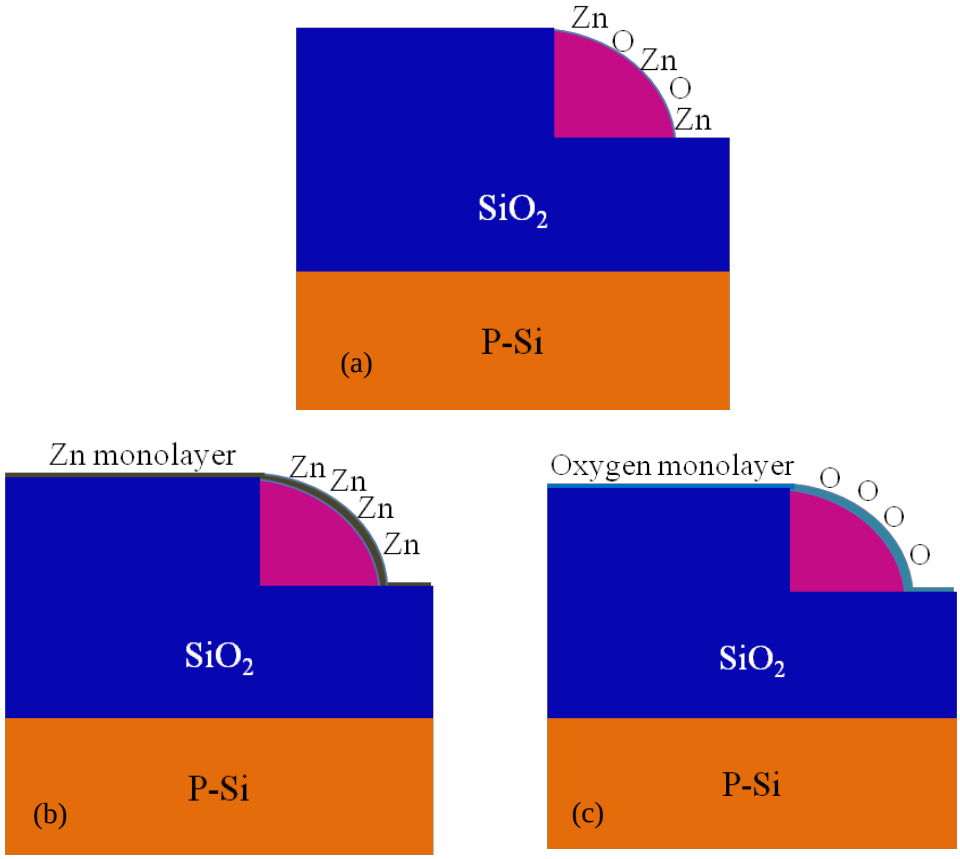


Fig.8.3 Schematic Illustration of dry etched ZnO nanowire (a) after dry etched as demonstrated in this work (b) after deposition of Zn monolayer for Zn-polar device (c) after deposition of oxygen monolayer for O-polar device.

- **Effect of different passivation layer**

  Further work is needed to address the challenges associated with improved control of the electronic properties especially the field-effect mobility. There is certainly room for investigating surface passivation on these top-down fabricated NWFETs with different passivation layer. Recently, Ye and Wong achieved a mobility enhancement by almost x 60 on their ZnO TFT after fluorine incorporation [3]. This improvement is attributed to the passivation of the carrier traps by fluorine. Other passivation layers such as SiO_2,

Si_3N_4 and Al_2O_3 could be explored in order to improve the device performance and stability. In addition, for simple logic circuits, a top - gated device is necessary for addressability since the global back gate does not allow the nanowires to be addressed individually. Therefore, top gate dielectric layers such as SiO_2, Si_3N_4 and Al_2O_3 need to be developed partly as passivation layers and also as gate dielectrics.

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Appendix A1

Derivation of Poisson's Equation

$$\frac{\partial^2 \emptyset}{\partial x^2} = -\frac{\rho_s(x)}{\varepsilon_{ZnO}\varepsilon_0}$$

where ρ is the surface charge density and $\varepsilon_{ZnO}\varepsilon_0$ is the dielectric permittivity of ZnO and free space, respectively.

$$\rho_s = -qN_D$$

$$\frac{d^2 \emptyset}{dx^2} = -\frac{qN_D}{\varepsilon_{ZnO}\varepsilon_0}$$

where N_D is the channel doping concentration. Integration of the above equation

$$\frac{d\emptyset}{dx} = \frac{qN_D}{\varepsilon_{ZnO}\varepsilon_0} x;$$

where x is the depletion width.

Second integral of the above equation,

Potential, $\emptyset = \frac{qN_D x^2}{2\varepsilon_{ZnO}\varepsilon_0}$

Appendix A2

TABLE A.2 Summary of the experimental parameters used in this work and the outcomes.

Work	Variable	Key Comments (regarding material and device performance
Remote PEALD deposition	O_2 Plasma < 4s O_2 pressure < 57.5 mTorr	Low carbon, resistivity, higher mobility and stoichiometry
Remote PEALD deposition	O_2 plasma pressure = 15mTorr	Growth per cycle= 0.9 Å/cycle
Dry Etch	RIE: CHF_3 =25 sccm, RF = 300 W, pressure = 20 mTorr ICP: CHF_3 =25 sccm, RF = 300 W, ICP power = 1000 W, pressure = 10 mTorr.	RIE etch rate ~ 1.6 nm/min ICP etch rate ~ 50 nm/min
NWFET Fabrication	Oxygen Plasma = 4s , 57.5 mTorr, DEZ dose = 30 ms, T=150^{o}C Etched in RIE	L = 8.6 µm, V_{TH} = 6.5V, μ_{FE} = 0.5 cm^2/Vs
	Oxygen Plasma = 4s, 15 mTorr, DEZ dose = 30 ms, T=150^{o}C Etched in RIE	L = 10 µm, V_{TH}=10 V, μ_{FE} = 0.5 cm^2/Vs
	Oxygen Plasma = 4s, 15 mTorr, DEZ dose = 30 ms, T=150^{o}C Etched in ICP	L = 10 µm, V_{TH}=22 V, μ_{FE} = 3.0 cm^2/Vs
	Oxygen Plasma = 4s, 15 mTorr DEZ varied from 30 ms to 3 s, T=150^{o}C	Optimized DEZ dose >1s Growth per cycle =1.08 Å/cycle
	Oxygen Plasma = 4s, 15 mTorr DEZ dose =1s, T varied from 100 to 210^{o}C	Optimized T = 190^{o}C Hall mobility = 118 cm^2/Vs L = 10 µm, V_{TH} = 24 V, μ_{FE} = 10.0 cm^2/Vs
Reproducibility and Hysteresis	Oxygen Plasma = 4s, 15 mTorr DEZ dose =30 ms, T = 100 ^{o}C	
Biosensing	Oxygen Plasma = 4s, 15 mTorr DEZ dose =30 ms, T 100 ^{o}C	Use 100 parallel nanowires with L =20 µm

PEALD = Plasma Enhanced Atomic Layer Deposition, L = device channel length, μ_{FE} = field effect mobility