Pulse-induced resistive and capacitive switching in TiO2 thin film devices

Iulia Salaoru, Ali Khiat, Qingjiang Li, Radu Berdan, and Themistoklis Prodromakis
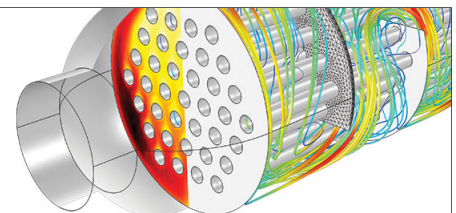
Pulse-induced resistive and capacitive switching in TiO$_2$ thin film devices

Iulia Salaoru,[1,a)] Ali Khiat,[1] Qingjiang Li,[1,2] Radu Berdan,[3] and Themistoklis Prodromakis[1,3]

[1]*School of Electronics and Computer Science, Nano Research Group, Southampton Nanofabrication Centre, University of Southampton, Southampton SO17 1BJ, United Kingdom*
[2]*College of Electronic Science and Engineering, National University of Defence Technology, Changsha 410073, China*
[3]*Department of Electrical and Electronic Engineering, Circuits and Systems Group, Imperial College London, London SW7 2AZ, United Kingdom*

In this study, we exploit the non-zero crossing current–voltage characteristics exhibited by nanoscale TiO$_2$ based solid-state memristors. We demonstrate that the effective resistance and capacitance of such two terminal devices can be modulated simultaneously by appropriate voltage pulsing. Our results prove that both resistive and capacitive switching arise naturally in nanoscale Pt/TiO$_2$/Pt devices under an external bias, this behaviour being governed by the formation/disruption of conductive filaments through the TiO$_2$ thin film. © 2013 AIP Publishing LLC.
[http://dx.doi.org/10.1063/1.4840316]

Memristors have recently been gaining a wide interest mainly due to their capability of being scaled down to less than 10 nm (Ref. 1), their simple (two terminal) structure, zero power drawn for sustaining a resistive state (Ref. 2), high-speed operation (Refs. 3 and 4) and also their multistate capacity (Refs. 5–7). These features find a wide range of applications in reconfigurable architectures (Ref. 8), neuromorphic computing (Refs. 9–12), artificial synapses (Refs. 13 and 14), non-volatile memory (Ref. 15), and analogue signal processing (Ref. 16).

The concept of memristors has been theoretically conceived in 1971 by Chua (Ref. 17) through his famous symmetry argument. The memristor's distinct behaviour is characterized by its capability of exhibiting memory, while operating as a variable two-terminal resistor. The memristor concept was further generalized to memristive systems (Refs. 18 and 19), defining all two terminal non-volatile memory devices based on resistive switching, independently of the employed material and the physical operating mechanisms. The typical signature of a memristive device is a pinched hysteresis loop in the first and the third quadrants of the current-voltage (I-V) characteristic. Similar behaviours have been observed (Ref. 20) in many unrelated fields, such as biology, chemistry, physics but it has attracted enormous interest of research community, only after Strukov *et al.* (Ref. 21) identified similar attributes with what Chua predicted almost 40 years ago on nanoscale TiO$_2$-based resistive switches. Furthermore, in 2009, Di Ventra *et al.* (Refs. 22 and 23), advanced the field by theoretically defining two other types of devices: memcapacitors and meminductors that can be considered as mem-devices (Refs. 24–26). The memristor, memcapacitor, and meminductor have similar characteristics in terms of dependence on the state and history of the system. The concurrent resistive and capacitive switching effect have been reported in perovskite oxide (Ref. 27), LaAlO$_3$ (Ref. 28), and VO$_2$ (Ref. 29).

Here, we demonstrate the coexistence of both resistive and capacitive features in nanoscale TiO$_2$ based solid state memristive devices. The I-V characteristics of our employed Pt/TiO$_2$/Pt devices display a combination of hysteresis and non-zero crossing, which supports a further investigation on the capacitive behaviour of resistive random access memory (ReRAM) cells. We demonstrate that the effective resistance and capacitance of the utilised cells can be modulated simultaneously by appropriate voltage pulsing. We ascribe the physical origin of resistive and capacitive memory effects to the dynamical properties of TiO$_2$ constituents (oxygen vacancies and titanium interstitials) that form and rupture conductive filaments at low resistive state (LRS) and high resistive states (HRS), respectively, through a fuse-antifuse mechanism (Refs. 30 and 31).

All ReRAM devices investigated, in this work, were fabricated on typical 4-in. silicon wafers. A SiO$_2$ thin film was thermally grown on Si to serve as an insulating medium. Bottom electrodes (BE) were defined by lift-off process after using conventional optical photolithography and electron beam evaporation to deposit 5 nm Ti and 30 nm Pt films. TiO$_2$ active core was deposited and patterned on top of the BEs via RF - sputtering. Finally, a 30 nm thick Pt layer was deposited and patterned on top to form the ReRAM cells' top electrodes (TE), by adhering to the same process used for the fabrication of the BEs. Fig. 1(a) illustrates the optical microscope view of a dense cross-bar array of 2×2 μm^2 core areas. The schematic configuration of the fabricated devices is depicted in Fig. 1(b).

All devices were electrically evaluated on wafer via a Semiconductor characterisation suite Keithley SCS-4200. During the measurements, the voltage bias was applied to the TE, while maintaining the BE grounded. The probe/point contacts to the TE and BE of the devices under test were realized through a pair of Wentworth probe-needles, using a Wentworth Laboratories AVT 702 semi-automatic prober. The current-voltage characteristics were studied by quasi-static voltage sweeping measurements. To program the devices in different capacitive and resistive states, several voltage pulses were applied to the device using the two pulsed measure units (PMUs) of the same characterization system. Voltage pulses of 6 V of magnitude and duration of
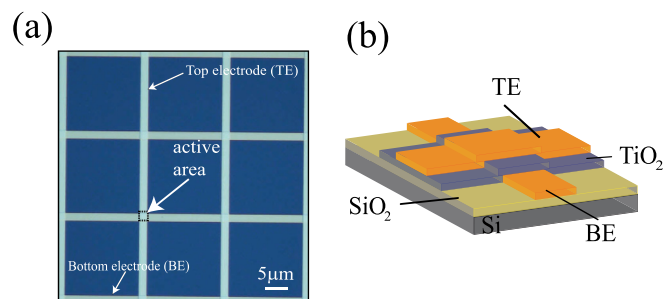
a)Electronic mail: I.Salaoru@soton.ac.uk

(a)

(b)

FIG. 1. (a) Optical microscope image of a crossbar-type array comprising devices with active areas of 2×2 μm^2; (b) Schematic configuration of the Pt/TiO$_2$/Pt fabricated devices.

1 ms were used to program simultaneously the capacitive and resistive states. The resistive states have been read out by a small voltage pulse with 0.5 V amplitude and 1 ms pulse width. Additionally, the capacitive states of the devices' were measured by employing a small AC 30 mV stimulus at 1 MHz.

The current- voltage (I-V) characteristics of the Pt/TiO$_2$ (22 nm)/Pt cells were studied by DC sweep measurements with the results shown in Fig. 2, where the arrows indicate the switching direction.

During the measurements, the compliance current was maintained at 1 mA to avoid any hard-breakdown of the devices. Fig. 2(a) illustrates the I-V characteristics of a Pt/TiO$_2$/Pt cell, when the voltage was swept in steps of 0.25 V, within a ± 4 V range. The device is originally in a HRS and a LRS is attained as the voltage bias approaches V$_{set}$ = 3.6 V. Reversing the voltage polarity causes the device to switch back to HRS at V$_{reset}$ = -4 V. The investigated device exhibits bipolar switching, with LRS and HRS achieved after the device was biased with positive SET and negative RESET, respectively. This biasing trend resulted in a pinched-hysteresis loop with zero crossing of I-V characteristics, which is a typical signature of a memristive device (Refs. 17–19). It is noteworthy that our devices are also capable of the non-zero crossing in their I-V characteristics as shown in Fig. 2(b). This was evoked by a ± 3 V voltage sweep in 0.25 V steps. As shown in Fig. 2(b), the device exhibits a bipolar switching mode with a positive sweep causing a HRS to a LRS transition and a negative potential resetting the device to a HRS. We experimentally observed a non-zero crossing behaviour only when the applied voltage induced hysteresis in I-V characteristics but not an abrupt switching between high and low resistive states. The pinched

hysteresis loop is attained when a sharp switching takes place.

To further investigate resistive and capacitive features of solid state ReRAM cells, we employed a voltage pulsing scheme shown in Fig. 3(c). A single device was subjected to a train of 100 consecutive voltage pulses, with a SET voltage of 6 V and 1 ms width to allow programming the TiO$_2$ cells in low and high resistive and capacitive states, respectively. After each SET pulse, the resistive states was evaluated at 0.5 V (a low potential which does not disrupt the current state) and the capacitive state at 1 MHz using a sensing signal of 30 mV. The exhibited concurrent capacitive and resistive modulation responses of the device are shown in Figs. 3(a) and 3(b) when excited with the voltage pulsing shown in Fig. 3(c). The pristine state of TiO$_2$ based devices is in a HRS and LCS. A unipolar switching trend was observed after the application of consecutive voltage pulses that induce multiple reversible changes to the devices' resistance and capacitance, as shown in Figs. 3(a) and 3(b).

In this work, all devices were electrically characterized without any post-fabrication electroforming step (Refs. 32 and 33). As such, the active core of our prototypes only undergoes a reduction, i.e., from TiO$_2$ to TiO$_{2-x}$, after the application of a number of pulses that induce a cumulative thermally driven mechanism (Joule heating Refs. 34–38). In consequence, the first resistance and capacitance switching event took place after 37 continuous applied pulses with the resistance switching from a HRS to a LRS and the capacitance from a LCS to HCS. Subsequent pulses cause the device to toggle, respectively, between LRS, HCS, and HRS, LCS and finally remains in LRS and HCS. It is interesting to note that by increasing the switching events the number of the applied pulses required for toggling between low and high resistive and capacitive states decreases. This demonstrates that in the case of pristine active layer the energy required to induce local modification of the active material in the form of a conductive filament is substantially high. On the other hand, for later switching events, when the chemistry of the active core is altered enough, the accumulated energy is dissipated by Joule heating, which causes the rupture/re-formation of conductive filaments (Refs. 34–38).

Contrary to the bipolar switching mode, where resistive switching is attained via the displacement of ionic species (a well-controlled process), unipolar switching is mainly ascribed to a thermally driven reduction of TiO$_2$, which may cause inconsistent switching. In our case, the first switching event (observed at cycle 37) also serves as electroforming
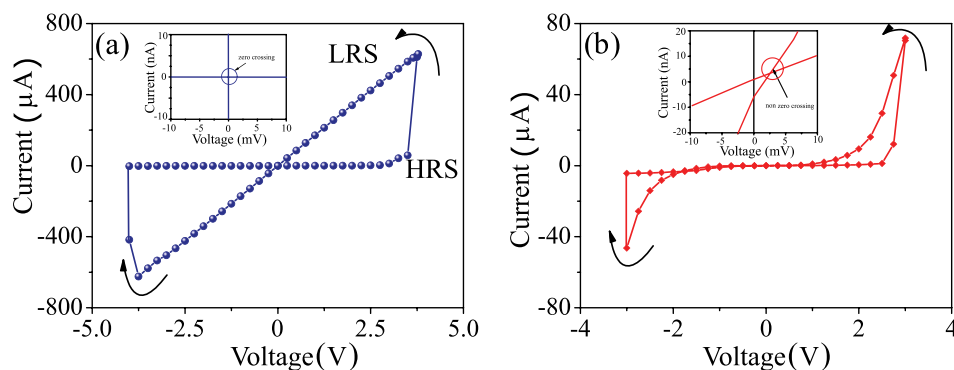
FIG. 2. I-V characteristics of TiO$_2$ based ReRAM cells: (a) zero-crossing I-V characteristic of device, which is a memristor signature, (b) non-zero crossing I-V characteristic indicating capacitive capabilities of TiO$_2$ cells. Inset figures illustrate zoom-in captions of the zero and non-zero crossing in I-V characteristics of Pt/TiO$_2$/Pt devices.
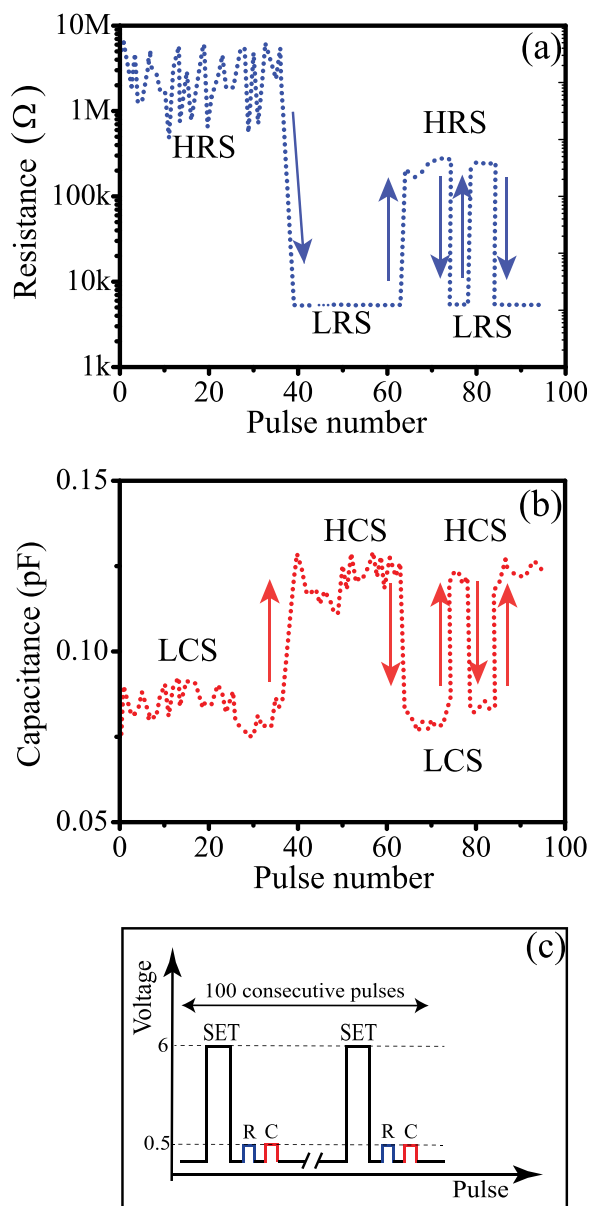
FIG. 3. Concurrent resistive and capacitive state programming of the fabricated prototype based on TiO_2 active core (a) electrical pulse induced resistance change; (b) electrical pulse induced capacitance change, (c) pulsing sequences utilized for concurrent resistive and capacitive state programming.

conductive filament(s) that expand across the TiO_2 layer to bridge the top and bottom electrodes. This results in the reduction of the resistance. On the other hand, the same mechanism is leading to the enhancements of the capacitance and the MIM structure now behaves as a leaky capacitor. Ruptured or partially formed filaments at HRS create localized highly insulating areas, which subsequently enhance the resistivity and diminish the capacitance of the system.

It is worth pointing that crystalline defects in metal oxides, such as oxygen vacancies and/or Ti interstitials have a strong impact on the film's resistance and its dielectric properties. Various groups have studied the effect of oxygen vacancies on electrical conductivity and was demonstrated that the electrical resistance of TiO_2 is proportional to the concentration of oxygen vacancies (Refs. 39–41). On the other hand, it was further proved that the same defects also affect the dielectric constant of TiO_2 (Refs. 42–45) and hence in our case the devices' capacitance.

As the above presented results are qualitatively supported through single device measurements, we have tested 15 devices from different locations within the same wafer. Fig. 4 further supports our results demonstrating that the observed concurrent capacitive/resistive modulation is not an isolated event. It is important to remark that the HRS ($\sim 10\,M\Omega$) and LCS ($\sim 0.05\,pF$) are the original states of the tested devices, measured with a low potential of 0.5 V prior any programming.

Fig. 4 illustrates the measured switching ration (OFF/ON) for both resistance and capacitance. In the case of resistive switching, we were able to show an OFF/ON ratio as high as 4 orders of magnitude, while in the capacitive case; the attainable switching ratios were limited in the range of 1 to 2 orders of magnitude. For the particular results presented in Fig. 3, the minimum attained resistive state is $5.3\,k\Omega$, while the attained HRS is $5\,M\Omega$. This results in a 3 orders of magnitude OFF/ON resistive ratio. On the other hand as we consider that the capacitance modulation is due to a thermal alteration of the TiO_2 dielectric constant, we extrapolated the film's $\varepsilon_{r,eff}$ to be equal to 42 in the LCS, while in HCS it becomes $\varepsilon_{r,eff} = 68$; justifying the observed 1–2 orders of magnitude OFF/ON capacitance ratio. These values are in qualitative agreement with the data obtained by different authors for TiO_2 (Refs. 42–45).

and thus any following switching events are accomplished with fewer pulses.

Moreover, as shown in Fig. 3(a) the original HRS ($>1\,M\Omega$) could not be recovered and a high sub-resistive state ($\sim 250\,K\Omega$) is achieved as the electrical pulses were applied to the cell. This demonstrates that the original resources (i.e., oxygen ions) cannot be re-attained once the device undergoes resistive switching. Our experimental results indicate that the switching dynamics depend on the origin/history of the system in terms of "state" of active core.

As can be seen in Figs. 3(a) and 3(b), the switching trend of resistance is anti-correlated with that of capacitance, i.e., decrease in resistance with an increase in capacitance. We argue here that the applied potential causes a displacement of ionic species such as V_O^{-2} and/or Ti^{n+} within the active core that foster the formation of current percolation paths, i.e.,
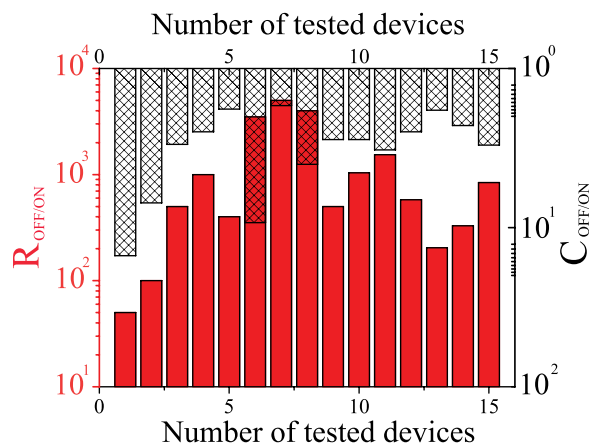

FIG. 4. OFF/ON ratios of resistance and capacitance vs number of the tested devices.

In summary, we have studied the dual resistive and capacitive capabilities of $Pt/TiO_2/Pt$ nanoscale ReRAM cells. The I-V characteristics of TiO_2 based solid state devices display a hysteresis loop with non-zero crossing indicating that our devices also exhibit capacitive effects. Furthermore, the effective resistance and capacitance of TiO_2 two terminal devices were modulated simultaneously by appropriate voltage pulsing; rendering resistive and capacitive memory effects in a single device. We suggest that both the resistive and capacitive switching modes appear to be involved in the creation and annihilation process of filaments, comprising of reduced TiO_{2-x}, caused via thermal effects as Joule heating. Unfortunately, the thermally driven mechanism limits the performance characteristics of our ReRAM prototypes in terms of endurance, as we anticipate that the long-term programming of the devices will result into an irreversible condition, where most of the oxygen species will not be able to be recovered. However, we still believe that this approach can be employed in write-once read many scenarios for avoiding any destructive evaluation of memory states.

[1]B. Govoreanu, G. S. Kar, Y.-Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I. P. Radu, L. Goux, S. Clima, R. Degraeve, J. Jossart, O. Richard, T. Vandeweyer, K. Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D. J. Wouters, J. A. Kittl, and M. Jurczak, Technical Digest International Electron Devices Meeting, 2011.

[2]J. P. Strachan, A. C. Torrezan, G. Medeiros-Ribeiro, and R. S. Williams, Nanotechnology **22**, 505402 (2011).

[3]X. A. Tran, H. Y. Yu, H. C. Yeo, L. Wu, W. J. Liu, Z. R. Wanf, Z. Fang, H. L. Pey, X. W. Sun, A. Y. Du, Y. Nguyen, and M. F. Li, IEEE Electron Device Lett. **32**, 396 (2011).

[4]H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien, and M. J. Tsai, Technical Digest International Electron Devices Meeting (2008), pp. 297–300.

[5]S.-J. Choi, G.-S. Park, K.-H. Kim, S. Cho, W.-Y. Yang, X.-S. Li, J.-H. Moon, K.-J. Lee, and K. Kim, Adv. Mater. **23**, 3272 (2011).

[6]M. Liu, Z. Abid, W. Wang, X. He, Q. Liu, and W. Guan, Appl. Phys. Lett. **94**, 233106 (2009).

[7]C. He, Z. Shi, L. Zhang, W. Yang, R. Yang, D. Shi, and G. Zhang, ACS Nano **6**, 4214 (2012).

[8]A. Gelencser, T. Prodromakis, C. Toumazou, and T. Roska, Phys. Rev. E **85**, 041918 (2012).

[9]T. Hasegawa, T. Ohno, K. Terabe, T. Tsurvoka, T. Nakayama, J. K. Gimzewski, and M. Aono, Adv. Mater. **22**, 1831 (2010).

[10]S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, Nano Lett. **10**, 1297 (2010).

[11]K.-H. Kim, S. Gaba, D. Wheeler, J. M. Cruz-Alberecht, T. Hussain, N. Srinivasa, and W. Lu, Nano Lett. **12**(1), 389 (2012).

[12]T. Serrano-Gotarredona, T. Masquelier, T. Prodromakis, G. Indiveri, and B. Linares-Barranco, Front. Neurosci. **7**(2), 1 (2013).

[13]L. Camunas-Mesa, C. Zamarreno-Ramos, J. A. Perez-Carrasco, T. Masquelier, T. S. Gotarredona, and B. Linares-Barranco, Front. Neurosci. **5**, 26 (2011).

[14]A. Afifi, A. Ayatollahi, and F. Raissi, IEICE Electronics Express **6**(3), 148 (2009).

[15]M. J. Rosenberg, I. H. Inoue, and M. J. Model, Phys. Rev. Lett. **92**, 178302 (2004).

[16]S. Shin, K. Kim, and S. M. Kang, IEEE Trans. Nanotechnol. **10**, 266 (2011).

[17]L. Chua, IEEE Trans. Circuit Theory **18**, 507 (1971).

[18]L. Chua, Appl. Phys. A: Mater. Sci. Process. **102**, 765 (2011).

[19]L. Chua and S. M. Kang, Proc. IEEE **64**, 209 (1976).

[20]T. Prodromakis, C. Toumazou, and L. O. Chua, Nature Mater. **11**, 478 (2012).

[21]D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, Nature **453**, 80 (2008).

[22]M. D. Ventra, Y. V. Pershin, and L. O. Chua, Proc. IEEE **97**(10), 1717 (2009).

[23]M. D. Ventra, Y. V. Pershin, and L. Chua, Proc. IEEE **97**, 1371 (2009).

[24]Y. V. Pershin and M. D. Ventra, Electron. Lett. **46**(7), 517 (2010).

[25]Y. V. Pershin, Adv. Phys. **60**, 145 (2011).

[26]M. D. Ventra, Mater. Today **14**, 584 (2011).

[27]S. Liu, N. Wu, A. Ignatiev, and J. Li, J. Appl. Phys. **100**, 056101 (2006).

[28]S. X. Wu, H. Y. Peng, and T. Wu, Appl. Phys. Lett. **98**, 093503 (2011).

[29]T. Driscoll, H. T. Kim, B. G. Chae, B. J. Kim, Y. W. Lee, N. M. Jokerst, S. Palit, D. R. Smith, M. D. Ventra, and D. N. Basov, Science **325**, 1518 (2009).

[30]I. G. Baek, M. S. Lee, S. Seo, M. J. Lee, D. H. Seo, D.-S. Suh, J. C. Park, S. O. Park, H. S. Kim, I. K. Yoo, U.-I. Chung, and I. T. Moon, Technical Digest International Electron Devices Meeting (2004), p. 587.

[31]B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg, and S. Tiedke, J. Appl. Phys. **98**, 033715 (2005).

[32]J. J. Yang, F. Miao, M. D. Pickett, D. A. A. Ohlberg, D. R. Stewart, C. N. Lau, and R. S. Williams, Nanotechnology **20**, 215201 (2009).

[33]D. S. Jeong, H. Schroeder, U. Breuer, and R. Waser, J. Appl. Phys. **104**, 123716, (2008).

[34]K. M. Kim, D. S. Jeong, and C. S. Hwang, Nanotechnology **22**, 254002 (2011).

[35]K. L. Yoon, M. H. Lee, G. H. Kim, S. J. Song, J. Y. Seok, S. Han, J. H. Yoon, K. M. Kim, and C. S. Hwang, Nanotechnology **23**, 185202 (2012).

[36]Y.-C. Chen, Y.-L. Chung, B.-T. Chen, W.-C. Chen, and J.-S. Chen, J. Phys. Chem. C **117**, 5758 (2013).

[37]C. Schindler, K. Szot, S. Karthauser, and R. Waser, Phys. Status Solidi (RRL) **2**(3), 129 (2008).

[38]D. Ielmini, F. Nardi, and C. Cagli, Nanotechnology **22**, 254022 (2011).

[39]B. Huber, H. Gnaser, and C. Ziegler, Surf. Sci. **566**, 419 (2004).

[40]J. Nowotny, M. Radecka, M. Rekas, S. Sugihara, E. R. Vance, and W. Weppner, Ceram. Int. **24**, 571 (1998).

[41]M. Redecka and M. Rekas, J. Eur. Ceram. Soc. **22**, 2001 (2002).

[42]K. K. Bamzai, S. M. Koohpayeh, B. Kaur, D. Fort, and J. S. Abell, Ferroelectrics **377**(1), 1 (2008).

[43]H. Fukuda, S. Namioka, M. Miura, Y. Ishikawa, M. Yoshino, and S. Nomura, Jpn. J. Appl. Phys., Part 1 **38**, 6034 (1999).

[44]V. Bessergenev, ECS Trans. **25**, 35 (2010).

[45]V. Bessergenev, Mater. Res. Bull. **44**, 1722 (2009).