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Development of Novel Fabrication Technology for SOI Single Electron Transfer Devices

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ABSTRACT

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Doctor of Philosophy

DEVELOPMENT OF NOVEL FABRICATION TECHNOLOGY FOR SOI SINGLE ELECTRON TRANSFER DEVICES

By: Feras M. Alkhalil

This report presents the design, simulation and fabrication of a spin qubit platform on ultrathin SOI (Silicon-on-Insulator) using Al FinSET (Single electron transistor) gates and Si side gates. A new design layout is proposed for the double spin qubits co-integrated with a single electron electrometer, a waveguide and a nanomagnet. This platform aims to demonstrate the full operation of double spin qubits by integrating the following three key techniques in one compact footprint: a precisely controlled single electron transfer technology, a high speed charge detection technique and a single spin detection technology based on spin to charge conversion. A single electron transfer device (SETD) integrated with an electrometer is introduced here as the main building block of the spin qubit platform. The single electron transfer device consists of three nanowire MOSETs connected in series, and is capacitively coupled to an SET electrometer. A unique layout design for the SETD and a novel single electron transfer voltage pulse sequence are introduced. Simulation and dynamic analysis of this device operation are preformed using a finite element capacitance based simulation method and a Monte Carlo based single electron circuit simulation. The simulations demonstrated the ability of this platform to transfer single electrons and these characteristics are analyzed to optimize the layout. A novel fabrication process to realize high density silicon quantum dots (QDs) with Al FinSET gates and close proximity Si gates on ultrathin SOI, for single electron transfer and detection, is successfully established with a number of different device layouts realized. In these devices, Al FinSET gates surround an SOI nanowire channel forming electrically tunable potential barriers and defining QDs among them; Si plunger side gates are included to enable precise control of the QDs potential. Five SETD and electrometer device generations have been realized, tested and analyzed to improve the device yield; this extensive process development work is concluded with a novel fabrication approach to demonstrate successful FinSET Al gate technology for SOI nanowires. This QDs platform is fabricated using a multi-layer electron beam lithography process that is fully compatible with metal oxide semiconductor technology. The fabrication process is fully developed with a yield of 92% and a great flexibility to enable the realization of more complex structures and even for devices beyond the scope of this project as shown in the appendices of this report.

Contents

Declaration of Authorship

I, Feras Alkhalil, declare that the thesis entitled ‘Development of Novel Fabrication Technology for SOI Single Electron Transfer Devices’, and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research.

I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University;
- Where any part of this thesis has been previously submitted for a degree or any other qualification at this University of any other institution, this has been clearly stated;
- Where I have consulted published work of others, this is always clearly attributed;
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledges all main sources of help;
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
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List of Publications

Journal publications

- Alkhalil, F.M., Perez-Barraza, J.I., Husain, M.K., Lin, Y.P., Lambert, N., Chong, H.M.H , Tsuchiya, Y., Williams, D.A., Ferguson, A.J., Saito, S. and Mizuta, H. Realization of Al tri-gate single electron turnstile co-integrated with a close proximity electrometer SET (2013). Microelectronics Engineering, 111, 64-67. doi: 10.1016/j.mee.2013.02.007.

- Lin, Y. P., Husain, M. K. and Alkhalil, F. M. et al. (2013) VLSI compatible parallel fabrication of scalable few electron Silicon Quantum Dots. IEEE TNANO, doi:10.1109/TNANO.2013.2263964.
- Boden S A, Moktadir Z, Alkhalil F M, Mizuta H, Rutt H N and Bagnall D M (2012) Nanofabrication with the helium ion microscope Proc. MRS Journal Proceedings, 1412, mrsf11-1412-ff08-08 doi:10.1557/opl.2012.978.
- Lin, Y. P., Husain, M. K. and Alkhalil, F. M. et al. (2012) Design and fabrication of densely integrated silicon quantum dots using a VLSI compatible hydrogen silsesquioxane electron beam lithography process (2012). Microelectronics Engineering, 98, 386-390. doi:10.1016/j.mee.2012.07.011.

Conference publications

- Alkhalil, F.M., Perez-Barraza, J.I., Husain, M.K., Lin, Y.P., Lambert, N., Chong, H.M.H , Tsuchiya, Y., Williams, D.A., Ferguson, A.J. and Mizuta, H. (2012) Realization of fully tunable FinFET double quantum dots with close proximity plunger gates. In, 12th International Conference on Nanotechnology (IEEE NANO 2012), Birmingham, GB, 20 - 23 Aug 2012. 2pp.(doi:10.1109/NANO.2012.6321993).
- Alkhalil, F., Perez-Barraza, J., Husain, M., Lin, Y., Lambert, N., Chong, H. , Tsuchiya, Y, Williams, D., Ferguson, A. and Mizuta, H. (2012) Al FinFET single electron devices with close proximity Si plunger gates. At Silicon Quantum Information Processing Meeting, Warwick, GB, 14 Sep 2012. 1pp.
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- Lin, Y.P., Perez-Barraza, J.I., Husain, M.K., Alkhalil, F.M., Lambert, N., Chong, H.M.H., Ferguson, A.J., Williams, D.A. and Mizuta, H. (2013) Fabrication and characterisation of down-scaled multi-configuration Silicon quantum dot devices. At the 2013 Silicon Nanoelctronics Workshop (SNW), Kyoto, Japan.
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- Lin, Y.P., Perez-Barraza, J.I., Husain, M.K., Alkhalil, F.M., Lambert, N., Chong, H.M.H., Ferguson, A.J., Williams, D.A. and Mizuta, H. (2012) VLSI Compatible parallel fabrication of scalable few electron silicon quantum dots. In, 12th International Conference on Nanotechnology (IEEE NANO 2012), Birmingham, GB, 20 - 23 Aug 2012. 2pp.
- Alkhalil, F. M., Husain, M. K., Lin, Y. P., Chong, H. M. H., Ferguson, A. J., Tsuchiya, Y. and Mizuta, H. (2011) Realization of an integrated double spin qubit device on ultra-thin Silicon-on-insulator. At Quantum information processing and communication international conference at ETH Zurich, Zurich, 05 - 09 Sep 2011. (Submitted).
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Chapter 1

Introduction

1.1 Quantum information processing

The remarkable growth of the electronics industry is reflected by the increasing number of transistors on a single chip and the spectacular size reduction of these transistors. However, as the electronics industry approaches the nanometre scale, the laws of quantum mechanics starts to control the behaviour of electrons in semiconductors. This has led to serious research and investigation into alternative directions for the electronics industry: one of these new directions is the use of the electron spin degree of freedom, in what is known as spintronics.

The purpose of spin based devices (Spintronics) is to control the quantum mechanical properties of the electron spin. Therefore, it is possible to employ spin based devices to perform quantum information processing tasks, like single electron spin initialization, manipulation and readout [1]. The term quantum information processing describes devices and systems in which information is handled and processed under the laws of quantum mechanics [2].

Quantum computing and quantum information processing have been proposed as a possible solution to maintain the growth of the transistor density on a chip, as predicated by Moore's law. The field of quantum computing started in the early 1980s, and it describes systems in which all the components are in the nanometer scale, since quantum mechanics control the behavior of devices in the nanoscale, these nanoscale systems will exhibit quantum behavior, hence the term quantum computers [1].

The spin state of localized electrons is naturally a two level system; this makes it an ideal candidate to realize a quantum bit (qubit is the elementary unit of quantum information processing) [1]. Electron spins can be localized by confining them to lithographically defined quantum dots, where the quantum dot (QD) is a fabricated structure that provides confinement in all three spatial dimensions [3]. The ability to realize a system where a single bit of information can be represented by a single electron would possibly be one of the most revolutionary achievements in the field of information processing and computing, because devices like this would be ultra fast and would consume very little power [4]. Such systems would have components that are able to transfer, manipulate and detect single electrons.

Quantum systems are extremely complex systems, and simulation of their dynamics is a very demanding task for classical computers, because the resources required for simulating a quantum system increase exponentially with the system size. The state of a quantum system is represented by a Hilbert space element, and the computational space dimensions required to simulate the state of n qubits is 2^n, i.e. to simulate an n qubit quantum system, an exponential number of 2^n classical bits are required [1]. Therefore, Richard Feynman concluded in the 1980s that some quantum mechanical effects cannot be properly simulated using classical computers, and he proposed that quantum systems should be simulated by a device of the same nature; a quantum device [1], [5].

The field of quantum computing didn't really take off until 1994, when Peter Shor introduced a Polynomial time quantum algorithm for large-scale prime factorization of integers. Factoring an N digit number using a classical algorithm would require an exponentially growing time (logN), while Shor's algorithm requires a time growth that is bound by a polynomial [1]. This discovery showed a clear advantage of this quantum factoring algorithm over classical factoring algorithms, especially in the field of cryptography, where the RSA public key algorithm currently used for cryptography is based around the fact the large scale prime factorization of over than 100 digits using classical computers is unfeasible. In 2001, a remarkable breakthrough was made when researchers at IBM demonstrated Shor's algorithm to factor the number 15 using a liquid state NMR quantum computer [5]. Another milestone in quantum computing was the introduction of error correcting codes. Error correcting codes compensate the effect of noise and the interactions with the environment [1]. The appearance of various quantum algorithms and the development of error correction codes have simulated a great deal of interest in different quantum computing proposals; some of these proposals will be discussed in detail in chapter 3 of this report.

This work presents a novel silicon based double spin qubits system integrated with an electrometer, and the aim of this platform is to demonstrate spin initialization, manipulation and readout operations. However, this report mainly focuses on the design, simulation, nanofabrication techniques and process developments necessary to realize this platform.

1.2 Report Structure

This report is divided into five main chapters.

Chapter two gives an overview of single electron devices operating principles, carrier transport theory, Coulomb blockade, Coulomb blockade oscillation, Coulomb diamond analysis and single electron tunnelling. It covers: the single electron box, the single electron transistor, double dot single

electron transistor and the single electron turnstile device. This chapter also gives an overview of spintronics and spin based quantum computation.

Chapter three examines various theoretical concepts and experimental efforts made towards the realization of solid quantum information processing. This chapter discusses the DiVincenzo criteria for quantum computing, and describes in detail many quantum computing proposals especially those based on electron charge, electron spin and impurity spins in semiconductor quantum dots.

Chapter four is dedicated to the Silicon-based Integrated Single-Spin Quantum Information Technology (SISSQIT) project. This chapter describes in great detail the components of the SISSQIT platform, the SISSQIT operation, techniques that will be employed for this system and the project methodology.

Chapter Five introduces the main building block of the SISSQIT platform, the single electron/spin transfer device (SETD) with an electrometer. This chapter discusses the significance behind this device for the experimental characterization of single electron transfer and single electron detection. Also in this chapter, layout of the SETD device with the electrometer, 3D FEM capacitance simulation, a unique single electron transfer scheme, and a full comprehensive description of the fabrication process is included.

Chapter six discusses the electrical characteristics, at room temperature and 4 K, of the first device batch in detail. It describes the process challenges and the proposed solutions and modifications required. A total of five device generations are discussed in this chapter, highlighting the process evolution of the metal FinSET quantum dot devices from a low yield first device batch to the first successful fabrication technology, to the best of my knowledge, for realizing FinSET-like metal gates for SOI nanowire structures.

Appendix A, B, C, D and E of this report include, respectively, a detailed step by step guide to the fabrication process, an overview of the different device layouts realized, the realization of a phosphorus doped charge qubits platform consisting of two quantum dots electrostatically coupled to a double quantum dot electrometer using lithographically defined constrictions, the development of extremely thin SOI (ETSOI) samples (approximately 7 nm thick) and He Ion lithography experiments on ETSOI, and finally the realization of an Extraordinary Magnetoresistance (EMR) platform for low temperature magnetic field experiments.

Chapter 2

Single electron devices

2.1 Single electron devices

Single electron devices (SEDs), as the name implies, have the ability to control, manipulate and transfer electrons on an elementary charge level. This property is based on the Coulomb blockade (CB) principle, which is a product of electrostatic forces generated by the confinement of electrons in small conductive structures [6].

Both metals and group III-V compound semiconductors SEDs have been implemented. However, Silicon SEDs are of special interest because of their ability to be integrated with other conventional complementary metal-oxide semiconductor (CMOS) circuits. Using Silicon based SEDs also means that the advanced CMOS large scale integrated circuits fabrication technologies can be utilized for the fabrication of the single electron devices extremely small structures [6].

Since SEDs have the potential of manipulating a single electron; they offer substantial savings in power consumption, their operating principle is relatively simple, and the performance of SEDs improves as they are scaled down. These factors make SEDs an attractive alternative for CMOS in future large scale integrated circuits [6].

2.1.1 Single electron devices operating principle

Single electron devices operation is based on two phenomena: Coulomb blockade and single electron tunnelling. The simplest example of a single electron device is the single electron box (SEB), the SEB will be used to give an overview of the operating principle of single electron devices.

The SEB consists of a small conducting island (also referred to as a quantum dot) and a specially fabricated junction, referred to as a tunnel junction, which permits quantum mechanical tunnelling of electrons. The SEB also has two electrodes, one connected to the island via the tunnel junction and the second electrode is capacitively coupled (through a gate capacitance C_g) to the island, the gate capacitance C_g does not permit quantum electron tunnelling which leaves the tunnel junction as the only way for an electron to transfer to or from the island [6],[7].

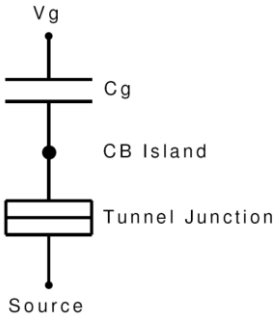


Fig. 2.1: Single electron box (SEB) equivalent circuit.

From a physical point of view, the tunnel junction is a thin insulating region that may be formed by a pattern dependant oxidation process (PADOX); this insulating region creates an energy barrier (tunnel junction) where electrons can tunnel through to reach the island [6]. PADOX oxidation for SOI (Silicon-on-Insulator) nanostructures is governed by two phenomena; the suppression of oxidation by mechanical stress (induced by mechanical expansion of the newly grown oxide) and oxidation from below the nanostructure (oxygen atoms diffusing through the buried oxide layer), this local oxidation process is strongly dependant on the size and shape of the nanostructure [8].

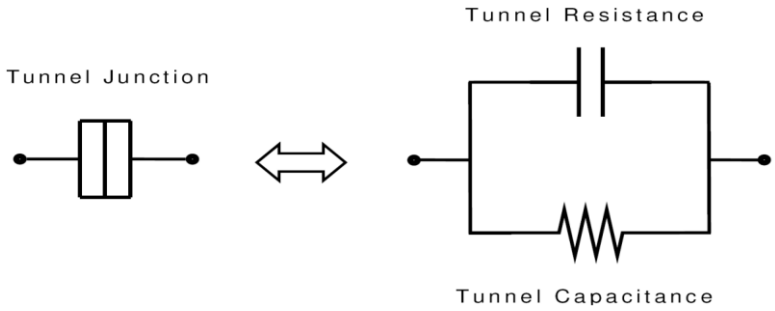


Fig 2.2: Equivalent circuit of a tunnel junction.

For a single electron device in thermal equilibrium at a temperature T, its steady state operation should satisfy the following relationship [9]:

$$\frac{\Gamma_{+}}{\Gamma_{-}} = \frac{1}{\exp(-eV / k_B T)} \tag{2.1}$$

Where Γ_{+} is the electron tunnelling rate in the forward direction, Γ_{-} is the electron tunnelling rate in a reverse direction, e is the elementary electron charge, k_B is Boltzmann constant, V is the voltage applied across the terminals of the tunnel barrier and eV is the amount of energy dissipated by forward electron tunnelling and is equivalent to the work done by the voltage source [9].

The net transfer of electrons in the forward direction (Γ_{net}) can be expressed by [9]:

$$\Gamma_{net} = \Gamma_{+} - \Gamma_{-} = \Gamma_{+}[1 - \exp(-eV / k_B T)] \tag{2.2}$$

And the current in the forward direction can be given by [9]:

$$I(V) = e\Gamma_{net} \tag{2.3}$$

From equations (2.2) and (2.3) , the electron tunnelling rate in the forward direction can be expressed by [10]:

$$\Gamma_{+} = \frac{I(V)}{e} \times \frac{1}{1 - \exp(-eV / k_B T)} \tag{2.4}$$

Therefore, the tunnelling of electrons through a tunnel barrier is dependent on the voltage applied across the terminals of the tunnel barrier. Looking back at the single electron box of fig. 2.1, to add a single electron to the CB (Coulomb blockade) island a voltage must be applied across the tunnel barrier, and the energy required to add a single electron to the island is known as the charging energy (E_c), E_c can be expressed by [11]:

$$E_c = e^2 / 2C_{\Sigma} \tag{2.5}$$

Where e is the electron charge and C_{Σ} is the total capacitance of the island.

When an electron transfers to the island, an electric field is created that resists the addition of further electrons to the island. Provided that the island size is small enough (nanoscale), the electric field created is inversely proportional to the square of the island size. This phenomenon is known as Coulomb blockade [11], [7].

The charging energy represents the Coulomb blockade energy (the electrochemical potential required to overcome the blockade), it increases as the CB island becomes smaller in size. For large values of E_c, no additional electron can transfer across the tunnel junction to the CB island unless the island potential is reduced [6].

2.1.2 The single electron transistor

A three terminal example of a single electron device is the single electron transistor (SET), the SET has a single island (quantum dot), two tunnel junctions and a voltage source to control the number of electrons in the island [6].

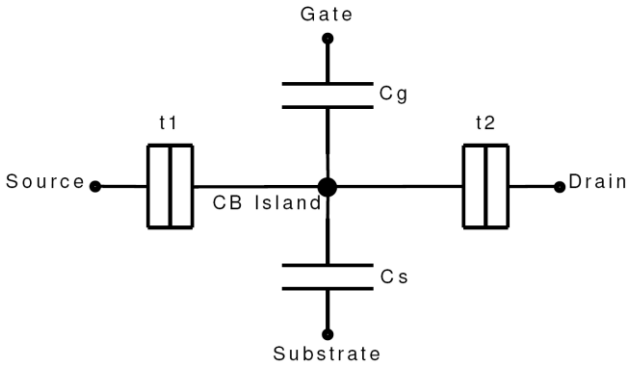


Fig. 2.3: Single electron transistor (SET) equivalent circuit.

The total capacitance C_{Σ} of the SET (Fig. 2.3) CB island is given by:

$$C_{\Sigma} = C_{t1} + C_{t2} + C_{g} + C_{s} \tag{2.6}$$

Where C_g is the SET gate capacitance, C_s is the substrate capacitance; C_{t1} and C_{t2} are the capacitances of the two tunnel junctions.

There are two criteria that must be met to ensure successful operation of a single electron transistor, or any single electron device in general:

- To ensure that each electron in the system is localized to a particular conducting island at any time, the resistance of the tunnel junction (t_1 and t_2) must be larger than the quantum resistance R_q [11], [6]: $R_t >> R_q$ (2.7)

  Where the quantum resistance is given by [6]:

  $$R_q = h / e^2 \cong 25.8k\Omega \tag{2.8}$$

  Relation (2.7) means that a tunnel junction with low electron transparency limits the quantum mechanical uncertainty of an electron location, which makes controllable manipulation of a single electron possible [11].

- To ensure that thermally heated electrons are not able to transfer across the tunnel barriers and consequently prevent the formation of a CB region, the charging energy must be sufficiently larger than the thermal energy. From (2.5) this condition can be expressed by [6]:

  $$E_c = \frac{e^2}{2C_{\Sigma}} >> k_B T \tag{2.9}$$

Assuming that the CB island has a spherical shape with a diameter d, and is immersed in a dielectric medium with a dielectric constant of ε, the island capacitance C_{Σ} can then be expressed by [6]:

$$C_{\Sigma} = 2\pi d\varepsilon_o\varepsilon \tag{2.10}$$

Equations (2.9) and (2.10) suggest that a smaller island size increases the charging energy, and consequently allows operation at a higher temperature. However, this introduces a greater challenge of fabricating such extremely small structure to achieve SEDs room temperature operation.

If the total capacitance of the single electron transistor (SET) island is close to 10^{-15} F, then the charging energy of adding a single electron to the SET island is larger than the thermal energy k_BT only at cryogenic temperatures, and conduction across this single electron transistor is accomplished by applying a source-drain potential higher than the island charging energy. On the other hand, room temperature SET operation requires the island total capacitance to be in aF range, this translates to an SET island of 10nm or less in size [12].

The single electron transistor has a very important property, where at constant source drain voltage; the source-drain current of an SET in Coulomb blockade is a periodic function of the gate voltage (V_g) with the period ΔV_g given by [11]:

$$\Delta V_g = \frac{e}{C_g} \tag{2.11}$$

The amplitude of these periodic oscillations is given by [11]: e/C_Σ (2.12)

If V_g changes by ΔV_g, the charge in the CB island changes by e. The change in the island charge is then compensated for by an electron tunnelling into or from the island.

This phenomenon is known as Coulomb blockade oscillation (shown in Fig. 2.4 (b)) , where the gate voltage effect is similar to injecting the island with a charge equal to V_gC_g, by allowing the island potential to periodically overcome the island charging potential producing an Ids oscillation with a period equal to (2.11). This change in the island charge effects the charge balance at the tunnel junction capacitances C_{t1} and C_{t2} [11].

The electron transport mechanism through a single electron transistor relies on the electrochemical potential of its charging island (CB island), the charging island is a small conductive island holding a charge Q, the island is separated from the external bias electrodes by two tunnel junctions and the gate and substrate capacitances. The electrostatic energy of the SET before any electron transfer events can be given by [13]:

$$E_1 = \frac{Q^2}{2C_\Sigma} \tag{2.13}$$

Q here is the background charge of the island and can be expressed as: $Q = N \times e$ (2.14)

Where N is the number of electrons in the CB island.

Assuming a single electron tunnels from the source across the tunnel barrier t1, the electrostatic energy of the system can then be expressed by [13]:

$$E_2 = \frac{(Q - e)^2}{2C_\Sigma} \tag{2.15}$$

An electron can transfer to the charging island only if it decreases the total energy of the system, this can be verified with the following [13]:

$$E_1 - E_2 = \frac{e(Q - e/2)}{C_\Sigma} > 0 \tag{2.16}$$

Q can also be described with the following [13]: $Q = C_\Sigma |V|$ (2.17)

Where $|V|$ is the potential drop across a tunnel junction, from (2.16) and (2.17); electron transfer across a tunnel junction is only possible if the potential across that tunnel junction satisfies the following [13]:

$$|V| \geq \frac{e}{2C_\Sigma} \tag{2.18}$$

$|V|$ in equation 2.18 represents the Coulomb blockade threshold voltage, and if the potential difference across a tunnel junction is less than $|V|$; then there is no electron transfer as the device is in Coulomb blockade.

With this conclusion in mind, the potential conditions required for SET operation can be easily described. For the SET shown in fig. 2.3, the gate and drain electrodes are connected to external bias sources V_g and V_d respectively, while the source and substrate electrode are chosen to be grounded. The potential of the charging CB (V_{island}) before any electron transfer can be given by [13]:

$$V_{island} = \frac{C_g}{C_\Sigma} V_g + \frac{C_{t2}}{C_\Sigma} V_d \tag{2.19}$$

C_{t2} is the capacitance of the tunnel junction t2.

From (2.18), electron transfer across the tunnel junction t1 is only possible if [13]:

$$|V_{island}| > \frac{e}{2C_\Sigma} \tag{2.20}$$

And electron transfer across the tunnel junction t2 is only possible when [13]:

$$|V_d - V_{island}| > \frac{e}{2C_\Sigma} \tag{2.21}$$

Considering all the information mentioned above and to ensure electron transfer across both tunnel junctions of the SET, the following scheme can be adopted [13]:

The source and substrate are kept grounded; the drain voltage is kept at $e/2C_{\Sigma}$ and only the gate voltage is varied (from zero to any higher positive value). This setup ensures that the island potential will have a voltage range from $eC_{t2}/2C_{\Sigma}^{2}$ to higher positive values linearly with any increase of the gate voltage [13]. These conditions satisfy both (2.20) and (2.21) allowing electron transport across the SET.

2.1.3 Theory of carrier transport in single electron devices

Analysis of single electron transport characteristics through quantum dots is very important; it provides means of verifying quantum dots formation and assists in evaluating their capacitance characteristics. A typical single electron transistor, like the one shown in Fig. 2.3, will be used in this section to explore the single electron transport via a single quantum dot. Fig. 2.4 (a) shows the SET Coulomb blockade characteristics, the CB region reflects the suppression in the number of electrons due to the quantum dot electrostatic energy. Addition of an electron to the charging island requires that the charging island electrochemical potential be lower than that of the source and the drain, otherwise no electron can tunnel to the charging island. To overcome the Coulomb blockade; a large potential bias (larger than the charging energy) must be applied. In addition, the electron thermal energy can also overcome Coulomb blockade. Therefore, low bias voltages and low temperature measurements are necessary to observe the Coulomb blockade characteristics [14].

The Ids-Vds characteristics as shown in Fig. 2.4(a) are linear outside the Coulomb blockade gap for similar SET tunnel resistances, if the two SET tunnel resistance are very different then the Ids-Vds characterises are stepped and these characteristics are referred to as Coulomb staircases [12].

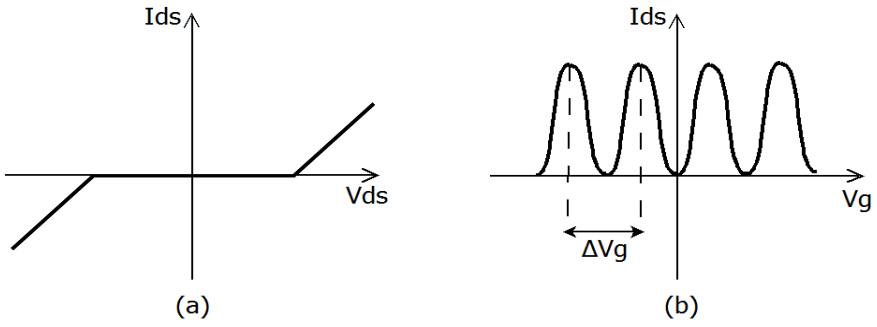


Fig. 2.4: Schematics showing (a) Coulomb blockade characteristics and (b) Coulomb blockade oscillation characteristics [14].

For a single electron transistor, the current can be plotted as a function of the gate voltage and the source drain voltage to give the schematic shown in Fig. 2.5. This schematic is known as the Coulomb diamond, the shadowed region represents the region where single electron transfer is suppressed (Coulomb blockade region).

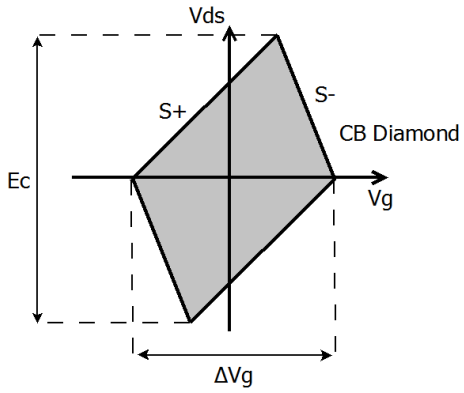


Fig. 2.5: Coulomb Blockade diamond, the shadowed region represents zero conduction current [14].

The SET shown in Fig. 2.3 has two control gates, the first one is the gate electrode that is coupled to the charging island through the gate capacitance C_g, and the second electrode is the substrate electrode which is capacitively coupled to the island through the substrate capacitance C_s. In this case two Coulomb blockade diamonds have to be considered: one for the current as a function of gate voltage and source drain voltage, and the other for the current as a function of the substrate voltage and the source drain voltage. From these two Coulomb diamonds, all the capacitance characteristics between the quantum dot and the other electrodes of the single electron transistor can be concluded [14].

The first diamond (current as a function of gate voltage and source drain voltage) gives the following capacitance information [14]:

$$\Delta V_g = \frac{e}{C_g} \tag{2.22}$$

$$S_+ = \frac{C_g}{C_g + C_{t2} + C_s} \tag{2.23}$$

$$S_- = -\frac{C_g}{C_{t1}} \tag{2.24}$$

The second diamond (current as a function of the substrate voltage and the source drain voltage) gives the following capacitance information [14]:

$$\Delta V_g = \frac{e}{C_s} \tag{2.25}$$

$$S_{+} = \frac{C_s}{C_s + C_{t2} + C_g} \tag{2.26}$$

$$S_{-} = -\frac{C_s}{C_{t1}} \tag{2.27}$$

S_+ and S_- are the positive and negative slopes of the Coulomb diamond.

To further extend on the Coulomb blockade diamond analysis, a double quantum dot (DQD) single electron transistor will be discussed here. A double dot SET is a series connected double quantum dots with two control gates (same as the normal SET) are coupled to each quantum dot, a schematic diagram of this device is shown in Fig. 2.6. Single electron transport through the DQD structure requires Coulomb blockade tuning of both the quantum dots, and the Coulomb oscillation characteristics of the DQD are no longer single periodic oscillations as it is the case for a single dot SET [14].

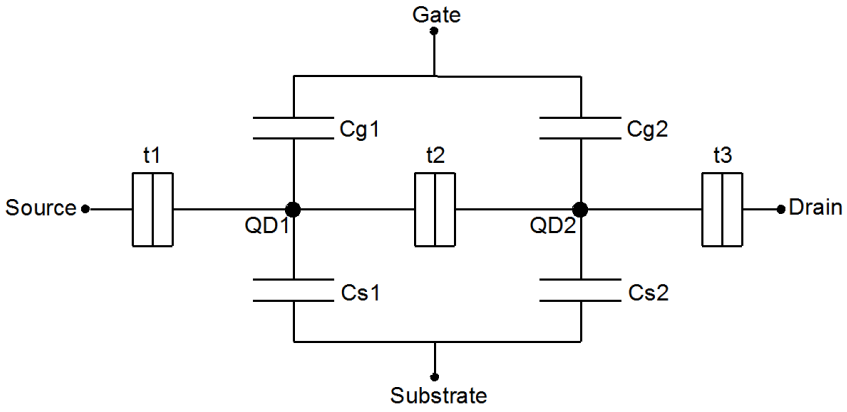


Fig. 2.6: Equivalent circuit of a double quantum dot (DQD) SET.

Sweeping both control gates of the DQD SET in Fig. 2.6 (the gate and the substrate) alters the electrochemical potential of each QD, plotting the current resulting from this sweep produces a contour plot known as the stability diagram. On the stability diagram the point of maximum current conduction is known as a triple point; this point represents the point at which the electrochemical potential (energy bands) of the two quantum dots are aligned together. The region enclosed by the triple points constitutes a region of stable electron numbers; it also has a honeycomb shape and is usually referred to as the honeycomb region [14]. A schematic of the stability diagram for a DQD SET is shown in Fig. 2.7 below. The electron transport via the DQD at zero temperature occurs only at the triple points. While at higher temperatures (for example 4.2 K) the electrons are transferred around the triple points, this effectively defines the boundaries of the honeycomb stable region [14].

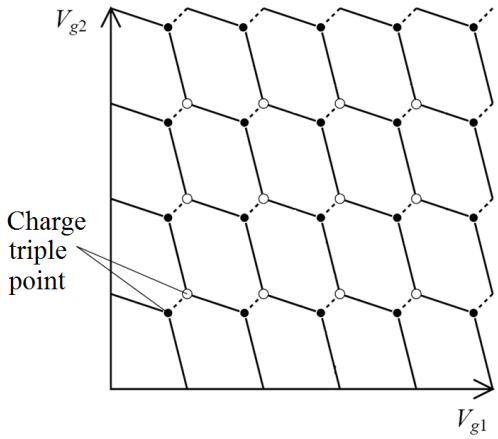


Fig. 2.7: Stability diagram of an intermediately coupled DQD SET [14].

The shape of the honeycomb pattern is specific to the electrical characteristics of the structure and is mainly defined by the coupling between the two QDs. The honeycomb pattern shown in Fig. 2.7 shows an anti-crossed charging lines pattern; this is a signature pattern of intermediately coupled quantum dots [14].

For strongly coupled QDs (Fig. 2.8 (a)), single parallel charging lines are observed in the stability diagram. The strongly coupled QDs in this case effectively behave as a single dot, and therefore this pattern is usually observed in single dot SETs [14]. On the other hand, weak coupling between the two QDs (Fig. 2.8 (b)) produces a stability diagram where each charging line crosses one triple point. The characteristics observed for very weakly coupled QDs are the same as the characteristics observed for series connected SETs [14].

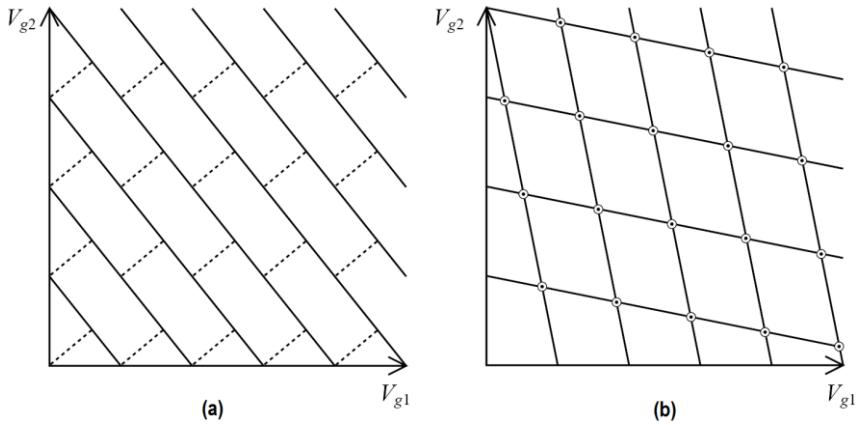


Fig. 2.8: Stability diagrams of (a) strongly coupled DQDs (equivalent to a single QD) and (b) weakly coupled DQDs [14].

Another important observation is that the stability diagram of a multiple QD structure, like the one in Fig. 2.7, shows charging lines with more than three different slopes. While, only a single uniform slope can be observed in the stability diagram of a single QD structure (Fig. 2.8 (a)) [14]. Stability diagrams analysis of multiple QD systems can be used to extract all the capacitance characteristics of

the systems, it also indicates the number of QDs formed their sizes and positions. Such analysis of electron transport characteristics is discussed in great detail by Wiel et. al. in [15].

2.1.4 Single electron turnstile devices

A single electron transistor is capable of transferring electrons one by one. However, the stochastic nature of tunnelling makes the time period of each tunnelling event uncontrollable in a SET. Therefore, it is harder for a single electron transistor to transfer one electron while stopping a second electron from transferring [4].

This lead to the development of a group of devices capable of transferring single electrons with high accuracy, known as the single charge transfer devices, this group includes single electron turnstiles, single electron pumps and single electron charged coupled devices [4].

Fig. 2.9 shows the equivalent circuit of a turnstile device. Formed by two series connected MOSFETs, control gates of the two MOSFETs (LTG1a and LTG2a) act as single electron barriers and are used to transfer single electrons from the electron reservoir (turnstile source) to the memory node (MN) (turnstile drain). By applying periodic pulse voltages (V_{g1} and V_{g2}) to the two gates, the potential barriers under theses gates change and the channel under each gate can be turned ON and OFF [4], [16].

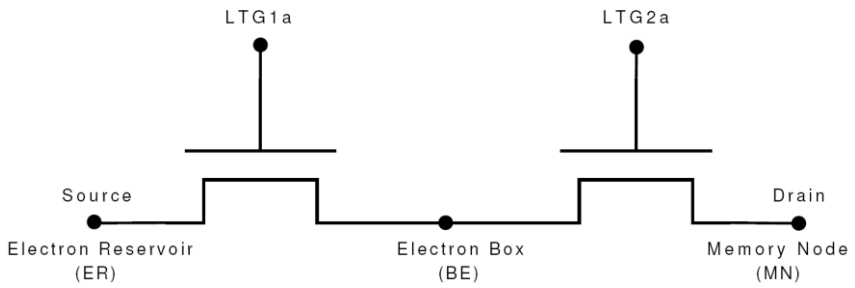


Fig. 2.9: Turnstile device equivalent circuit, the FET gates here are acting as single electron barriers.

With the gate voltages (V_{g1} and V_{g2}) cycled periodically, a single electron can be transferred from the source to the drain of the turnstile each cycle.

One cycle of the turnstile operation has the following steps [4], [16]:

- In the initial step (fig. 2.10 (a)), the island is isolated with both gates turned OFF.
- In the second step (fig. 2.10 (b)), LTG1a turns ON and the island between the two gates is connected to the source.

- In the third step (fig. 2.10 (c)), the potential barrier under gate LTG1a is raised and the gate turns OFF. A CB island is formed between the two gates, the island is electrically isolated from the source and a single electron remains in the island.
- In the next step (fig. 2.10 (d)), the gate LTG2a turns ON and the electron in the island is transferred to the drain because the island energy potential is higher than the energy potential of the drain.
- In the final step (fig. 2.10 (e)), LTG2a turns OFF and the electron is stored in the drain.

The operation sequence of the proposed turnstile device is shown below [4], [16]:

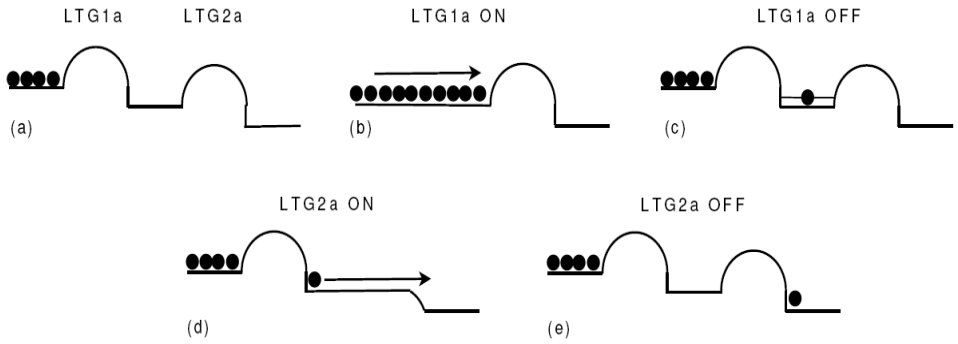


Fig. 2.10: Single electron transfer sequence of a turnstile device.

2.1.5 The single electron transistor as an electrometer

By biasing a single electron transistor slightly higher than the Coulomb blockade threshold voltage, the SET can be used as an electrometer. Where any change in the SET island potential causes a variation in the I_{ds}-V_g (Coulomb oscillation) characteristics of the single electron transistor [4]. By capacitively coupling the memory node of the turnstile device to the island of a single electron transistor, it is possible to detect the number of electrons at MN by observing the changes in the SET current oscillation. The figure below shows an equivalent circuit of the proposed configuration [4], [16], [17]:

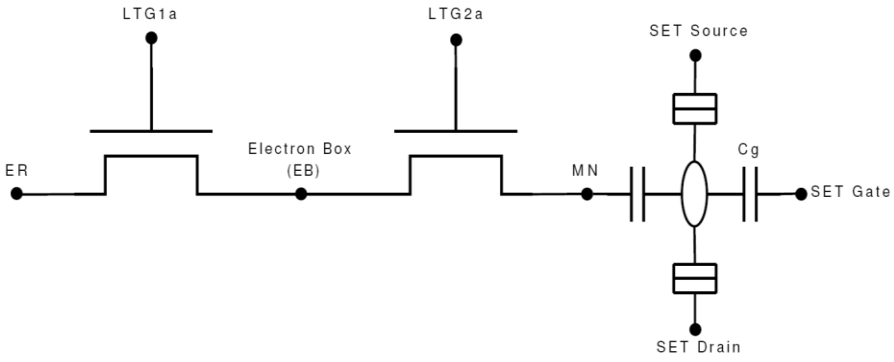


Fig. 2.11: Equivalent circuit of a turnstile device and a SET electrometer.

2.2 Spintronics and spin based quantum computing

Spin is one of the natural fundamental properties of all elementary particles. In classical physics, spin is defined as a small magnetic moment. However, measurement of a spin state in the presence of an external magnetic field, results in one of two discrete spin states: parallel or anti-parallel to the magnetic field. This behaviour, of having only two possible outcomes for the spin state, is the basis of the quantum mechanical nature of the spin [18].

Applications like magnetic resonance imaging and magneto electric devices have employed ensembles of many spins. On the other hand, the quantum mechanical nature of individual spins (the electron spin is a two state system, spin up and spin down), have made them suitable candidates for non-volatile memory applications, and to carry quantum information by using an individual spin to represent a quantum bit (qubit), where the single spin can potentially provide the ultimate bound for information storage [1], [3], [18]. The purpose of spin based devices (Spintronics) is to control the quantum mechanical properties of the electron spin. Therefore, it is possible to employ spin based devices to perform quantum information processing tasks, like single electron spin initialization, manipulation and readout [1].

Semiconductor structures, like quantum dots can be used to confine electrons, this provides a good degree of control and isolation of the electron spin state from its environment [1]. In addition, a technique like single electron turnstile (together with the application of a magnetic field) is capable of preparing the initial state of a single spin, and the spin state of a single electron can be detected using a spin to charge conversion method which utilizes spin dependant single electron tunnelling [19].

2.3 Summary

In this chapter, an overview of single electron devices and their operating principle was given. Single electron devices have proven to provide various advantages, including savings in power consumption, simple operation and high performance when scaled down. Single electron devices like the single electron transistor and the single electron turnstile will be utilized in this project for single electron detection and single electron transfer.

Spintronics and spin based quantum computing have also been covered in this chapter. This chapter provides a background overview for the project presented in this report. The SISSQIT project, presented in this report, proposes an integrated single electron double spin qubits system on a silicon on insulator platform, silicon has a low nuclear spin density, therefore increasing the spin decoherence time of our qubit.

Chapter 3

Physical realizations of quantum computing

3.1 Introduction

In version 2 (2004) of the quantum information science and technology roadmap, the relevant technology experts panel concluded that solid state quantum computing proposals (especially those related to localized spin or charge qubits) offer the best chances of progress towards the realization of a quantum computer [20]. In this chapter, we will describe various theoretical and experimental approaches for the realization of a semiconductor-based solid state quantum computing system, and we start by describing the DiVincenzo criteria, this criteria discusses the requirements for implementing a functional quantum computer.

3.2 Quantum computing and the DiVincenzo criteria

A quantum computer by definition is a machine that employs the full complexity of a many-particle quantum wavefunction to solve a computational challenge [21]. In quantum computing, the computational space available increases exponentially with the number of bits used. Therefore, quantum computing provides exponential parallelism; this in principle can lead to exponentially faster quantum algorithms than any other classical alternatives [22].

To understand the principle of quantum computing we can look at the basic principle of classical computing: we have a principle information unit known as the bit; this bit can have only one of two states 0 or 1. These classical 0 and 1 states can be represented by the ON/OFF state of a transistor, the presence/absence of charge in a memory cell or the magnetization direction of a magnetic body in a hard disk. Similar to a classical computer, a quantum computer uses a quantum bit (qubit) as its principle information unit expressed with two states of 0 and 1 to represent quantum information. The main difference here, is that quantum computing has a special state knows as superposition, in this state a qubit can take on the characteristics of both 0 and 1 states simultaneously at any moment in time. Therefore, a two qubit system in a superposition state can have any of the following states: 00,

01, 10 and 11 all at any one time. By employing superposition states expressed with N qubits, a quantum computer can perform simultaneous parallel processing of 2^N values; this property allows quantum computers to perform high speed processing faster than any processing speed available with classical computers [23].

There are a number of requirements that defines the implementation of a true quantum computer, these requirements are known as the DiVincenzo criteria and include [2]:

1. A scalable physical system with well characterized qubits.
   A well characterized qubit can be implemented by using a two level quantum system. For example, an electron, a spin ½ nucleus, or two orthogonal polarization states of a single photon.

2. The ability to initialize the state of the qubits to a simple fiducial state.
   Assuming a two level qubit, initialization would be achieved by polarizing the qubit to one of the two quantum levels.

3. Long decoherence times, much longer than the gate operation time.
   Decoherence is caused by the interaction of quantum states with the environment and leads to the degradation of most quantum states. Decoherence time doesn't necessarily have to be large, as long as the ratio of decoherence time to gate operation time satisfies this criteria at all times.

4. A universal set of quantum gates.
   Sufficient quantum computation operations can be carried out by having a gate for single qubit rotations and a two qubit gate to control the interactions between two qubits.

5. A qubit-specific measurement capability.
   A measurement capability provides readout of the qubit computation (interaction) outcome.

3.3 Quantum computing physical realizations

Various quantum computing proposals have been introduced in the past few years, based on a wide range of quantum phenomena, below is a list of some of these candidates [1]:

- Solid and liquid state NMR [24] and [25].
- Trapped ions [26].
- Cavity quantum electrodynamics [27] and [28].

- Neutral atoms in optical lattice.
- Linear optics [29].
- Solid state spin based and charge based systems.
- Charge, flux and phase Josephson junctions [30] and [31]
- Electrons on liquid helium surface [32].

Some of the early quantum computing proposals were cavity quantum electrodynamics (QED) [28], trapped ions and nuclear magnetic resonance. These proposals offer relatively high decoherence times, but they mostly fail to meet the scalability condition of the DiVincenzo criteria.

In this chapter, we will mostly discuss solid state quantum computing proposals with emphasis on electron spin and electron charge proposals.

3.3.1 Nuclear spin of phosphorous donor atoms in silicon

The first Si based qubit proposal was by B. E. Kane in 1998 [33], he proposed to use the nuclear spins of an array of ^{31}P donor atoms in a spin free ^{28}Si substrate, therefore this proposal offered very long decoherence times of nuclear spins in Si. Kane described this system at low ^{31}P concentrations and at a temperature of 1.5K, with an electron relaxation time of up to thousand of seconds and a ^{31}P nuclear relaxation time of about 10 hours, indicating that if this system is implemented it would provide the longest relaxation times for quantum computation [33].

The Phosphorous nuclear spins and the electron spins are coupled by a hyperfine interaction, where spin polarization can be conveyed between the electrons and the nuclear spins systems. This means that nuclear spins can be manipulated and detected electronically by integrating them with electronic devices. Larger hyperfine interaction between the two spin systems results in a system with better sensitivity. Electrons are sensitive to external electric fields, therefore, the hyperfine interaction and consequently the nuclear spin dynamics can be controlled by applying external voltages to metallic electrodes in silicon based devices [34].

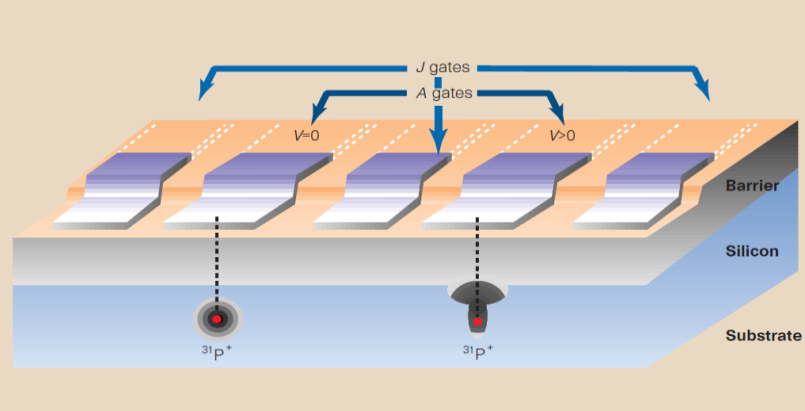


Figure 3.1: Quantum computing with nuclear spin of P donors in Silicon [35].

The nuclear spin states are detected by converting their polarization to electrons, these interactions are mediated through the use of a 2DEG layer, and then the electrons spin state is determined from the electron orbital wavefunctions by special capacitance measurements. Finally, operations must be carried out at low temperature (around 1.5K), to ensure that electrons only occupy non-degenerate low energy states in order to prevent reverse interactions between electrons and nuclear spins [34].

Kane's proposal satisfies all the theoretical requirements for quantum computing (the DiVincenzo criteria). However, this proposal requires very challenging bottom-up nanotechnologies, to control the number and position of the phosphorous atoms in the silicon substrate and there is little control over the exact position of the ^{31}P donor atoms in silicon. The donor atoms used in this proposal must be organised in a one or two dimensional array placed at only hundreds of angstroms beneath the surface of Si and under the barrier layer, conventional techniques like ion implantation and lithography are not useful. Another difficult element is the growth of subsequent Si layer on top of the donor array. The control gates needed must have dimensions and spacing in the range of 100 angstroms (10 nm). Even with the advanced nanofabrication techniques currently available, pattering such dimensions is considered very challenging [34].

There have been attempts to realize the Kane proposal by using Scanning tunnelling microscopy (STM) lithography and Hydrogen resist technology in what is known as STM induced hydrogen desorption technology. However, the use of STM lithography for atomic level arrangement in semiconductors is a challenging process because of the strong covalent bonds present in semiconductors [36], a schematic process flow is shown in fig. 3.2 below. That being said, the STM and hydrogen-resist lithography approach has progressed significantly from its early start and has demonstrated not only individual manipulation of atoms and molecules but also recently achieved deterministic placement of a single phosphors donor atom within an epitaxial silicon structure forming the first ever single atom transistor [37]

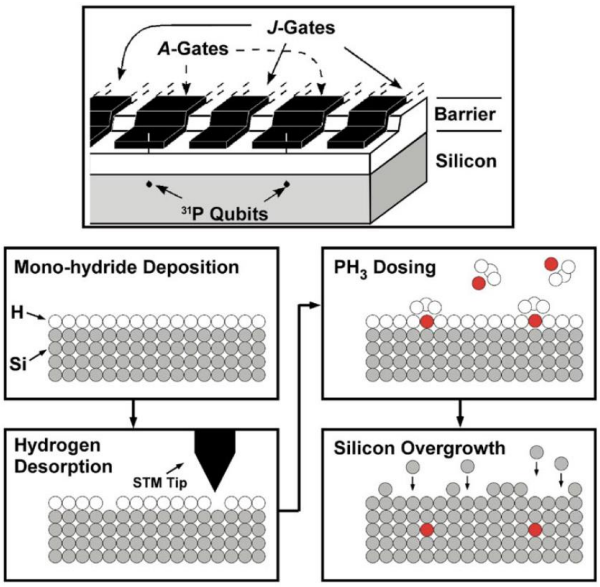


Figure 3.2: Process flow to realize the Kane architecture [36].

More developments in this field have been demonstrated by Morello et. al. also from the University of New South Wales. By using phosphorus implanted donors in Si coupled to a 2DEG single electron transistor, they successfully demonstrated a single shot readout of a single electron spin bound to a phosphorus implanted donor in Si. Their experiment showed an electron spin life time of about 6 seconds at a magnetic field of 1.5 Tesla and a spin readout fidelity of 90% [38]. Previous electron spin readout experiments in GaAs/AlGaAs employed charge sensors that are electrostatically coupled to the electron location, and the spin detection technique used was based on spin dependant tunnelling (this method will be described in detail in the next chapter) to a nearby electron reservoir. In the structure used by Morello et. al., the charge sensor used was electrostatically and tunnel coupled to the electron site where the electrometer island is used as the electron reservoir for the donor electron to directly tunnel to the electrometer island during the read out stage, this strong coupling between the electron site and the electrometer provides a charge transfer signal an order magnitude higher than signals obtained with electrostatically coupled charge sensors and it is the reason they managed to show such high fidelity rates in their single shot spin dependant tunnelling measurements.

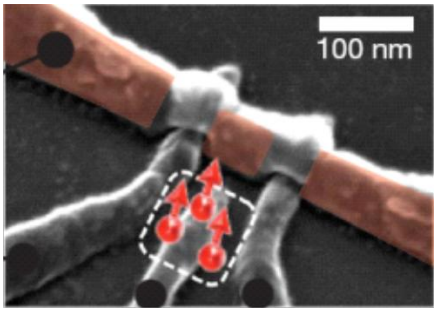


Figure 3.3: SEM image of the device used by Morello et. al., the dashed region shows the P donors location, the red region shows the 2DEG channel induced by the Al gates [38].

An SEM image of the device used in this experiment is shown in fig. 3.3 above, the electrometer is defined electrostatically in the underlying SiO2 layer using metal gates, the phosphorus donors are implanted in a small 90 nm x 90 nm region close to the electrometer QD, a top electrometer gate and a plunger gate over the donors location are also used to provide complete electrostatic control. The tunnelling between the charge site and the electrometer quantum dot is spin dependant when a large external magnetic field is applied (Zeeman splitting effect) , under the influence of the magnetic field (B) the spin up state has a higher energy level than the spin down state by a quantity equal to the Zeeman splitting energy (E_z) [38], [39]:

$$E_z = g u_B B \qquad (3.1)$$

Where g is the spin gyromagnetic ratio, and u_B is the Bohr magnetron. Spin to charge conversion is then accomplished by tuning the electrometer island potential so that only the spin up state energy is higher than the electrochemical potential of the electrometer island [38], [39].

More recently, with the addition of a microwave strip line to the structure shown in Fig. 3.3, the same researche demonstrated coherent manipulation of an individual electron spin bound to a phosphorus donor atom. Electron spin resonance and Han echo pulse sequence were used to trigger a Rabi oscillation with and measure a spin coherence time of approximately 200 us [40].

3.3.2 Quantum dot quantum computing (The Loss-DiVincenzo quantum computer)

A different approach to the donor atoms array for quantum computing is the confinement of single electron spins in nanofabricated structures known as quantum dots (QDs). In 1998, Daniel Loss and David DiVincenzo described a detailed set-up of a coupled quantum dot computing system, the qubit was realised using the spin states of a confined electron in the QD. Loss and DiVincenzo proposed initializing the qubits by applying an external magnetic field at low temperature. Single qubits

operations (like spin rotation) can be accomplished by applying a large gradient magnetic field to alter the effective Zeeman splitting of individual qubits, and two qubits gated operation is achieved by modifying the electrostatic potential barrier between the two coupled QDs [41].

Loss and DiVincenzo predicted that decoherence times of electron spin in QDs to be longer than decoherence times of charge degrees of freedom in QDs, because the common decoherence caused by electric potential fluctuations has only a small effect on the spin degree of freedom [41].

3.3.3 Electron spin in GaAs gate defined double quantum dots

This proposal was originally introduced by researchers at Harvard University, and is based on confining single electron spins in quantum dots. To define the quantum dots, they used electrostatic gates on top of AlGaAs/GaAs heterostructure grown by molecular beam epitaxy with a two dimensional electron gas below the surface [42].

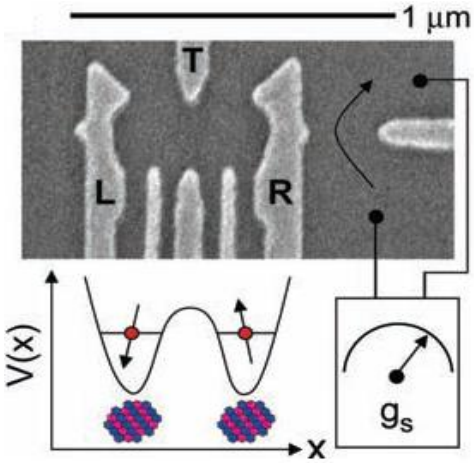


Figure 3.4: SEM image of the device proposed by Petta et al. [42].

Gate voltages V_L and V_R (Fig. 3.4) control the transfer of electrons from the reservoirs to the right and left dots, and gate voltage V_T is used to control the tunnel coupling between the two quantum dots. The readout technique is based on using a quantum point contact (QPC), sensitive to the number of electrons in the right QD, and employs spin to charge conversion technique to detect the electron spin state [42]. This quantum computing proposal showed coherent control over the electron spin state using fast electrical control of the exchange interaction of two neighbouring electron spins, and demonstrated most of the initialization and measurement operations with integrated electrostatic gates. This work also provided measurement of spin dephasing (decoherence) time in the range of 10 nanoseconds [42]. However, gallium arsenide itself is a nuclear spin rich environment, and the hyperfine interaction of the electron spin with the gallium arsenide host nuclei leads to rapid loss of the electron spin coherence. Petta et al. have since used a spin echo pulse sequence to overcome the

hyperfine dephasing problem, and they were able to demonstrate a two electron spin state coherence time of more than 1 microsecond [42]. Nevertheless, without using quantum control techniques like spin echo pulse sequence, the electron spin coherence times in gallium arsenide remain very short for quantum information processing purposes.

3.3.4 Electron charge in double quantum dots

Electron charge has also been utilized for quantum computing applications. Relatively long decoherence times has been achieved by confining electrons in isolated quantum dot structures with control gates capacitively coupled to the qubit. One clear advantage of using charge qubits is the inherently simple measurement of the charge qubit, charge readout can be achieved by using a capacitively coupled quantum point contact (QPC) or a single electron transistor (SET). A major source of decoherence for charge qubits would be fluctuations of the gates voltages that are used to control the qubits electrically. Therefore, most charge qubit proposals tend to have isolated qubits, where the control gates effect the charge qubits electrostatically.

Gorman et al. demonstrated complete operation of isolated charge qubits by using dedicated capacitively coupled gates for initialization and manipulation of the charge qubit, a single electron transistor was also used to readout the charge qubit [43].

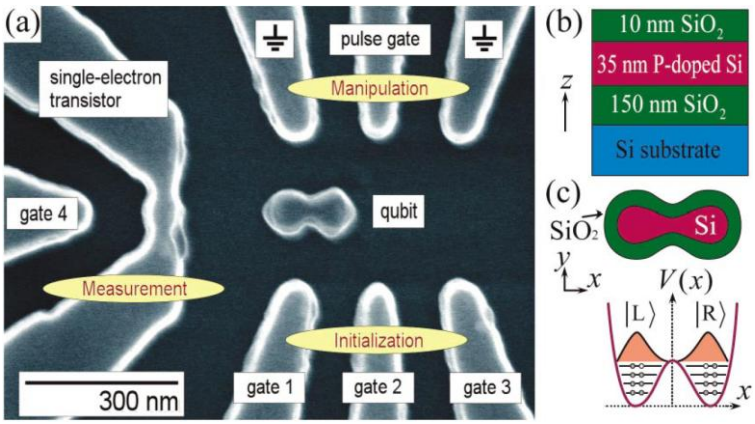


Fig. 3.5: (a) SEM image of the device introduced by Gorman et al. (b) material profile of the QD and c) Oxidized double quantum dot and localized electron charge configurations $|L\rangle$ and $|R\rangle$ [43].

The structure was fabricated using high resolution electron beam lithography and reactive ion etching. The platform of this device uses an SOI wafer with an active region doped with phosphorous, this layered insulator structure provides confinement in the vertical direction. Electrons are strongly isolated and confined to the double well potential formed by the QDs, the two QDs are connected together by a 20 nm wide constriction (tunnel barrier like structure) to form the qubit, and the potential of the QDs can be controlled by externally applied electric fields [43]. Gorman et al.

observed qubit coherence time of 200 ns, they attribute this to the presence of decoherence sources like: the back-action of the stochastic tunnelling events through the SET electrometer on the isolated double quantum dots, and the coupling of electromagnetic noise from the coplanar waveguide. They also suggested the use of an RF-SET to improve the charge qubit coherence times [43].

A similar isolated silicon double quantum dots device was also introduced by researchers from Hitachi Cambridge Laboratory. They used phosphorous doped (doping level of $3x10^{19}$ cm^{-3}) SOI isolated QDs coupled electrostatically to an SET electrometer and in-plane side gates, to demonstrate single charge transitions in the isolated quantum dots and they successfully controlled the charge occupancy of the QDs using in-plane side gates. They also observed clear variations in the electrometer current and shifts in the gate voltage Coulomb peaks of the electrometer as a result of inter dot single electron transfers in the isolated double QDs [44], [45].

Another charge qubit proposal was introduced by Kawata et al., their project featured two charge qubits integrated with a double dot single electron transistor (DSET) readout, where the DSET is used to measure the charge polarization of two charge qubits [46].

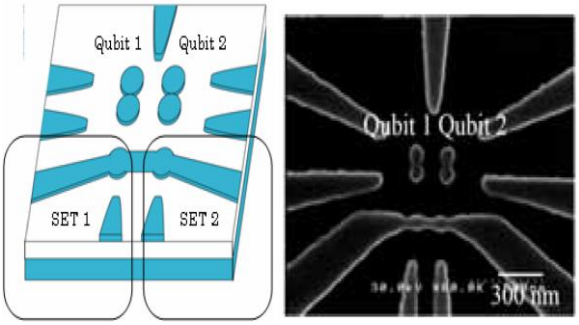


Fig. 3.6: Schematic and SEM image of the system proposed by Kawata et al [46].

The system was also fabricated on phosphorous doped silicon on insulator substrate, the double quantum dots were fabricated using electron beam lithography and reactive ion etching, and finally thermal oxidation was used to reduce the overall dimensions and to passivate the surface states. Kawata et al. demonstrated the possibility of having multiple SETs connected in series, instead of having dedicated SETs for individual qubits (which can take up a considerably large substrate area) and therefore demonstrating a scalable readout method [46].

3.3.5 Quantum computing with electron spin in silicon

Silicon is a fundamental element in the electronics industry, silicon processing and fabrication technology is well established and mature compared to other semiconductors. Natural silicon has the advantage of having only 4.7% (^{29}Si) nuclear spin carrying isotopes, where the other 95.3% (^{28}Si and

^{30}Si) are spin free; this effectively reduces the effect of the hyperfine interaction. In addition, spin orbit interactions in silicon are weak [47]. Therefore, Silicon is a very strong candidate for quantum computing applications.

Friesen et al proposed one of the early Si-based systems for quantum dot qubits in silicon-germanium heterostructures, where electron spins are used as qubits in this scalable system [48].

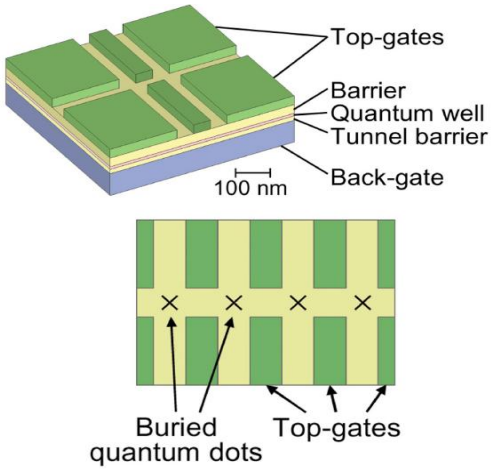


Fig. 3.7: SiGe two (top) and four dot (bottom) quantum computer proposed by Friesen et al [48].

The proposed structure (fig. 3.7) has a quantum well that provides confinement in the vertical direction, while the surface top gates provide electron confinement in the lateral direction. The presence of the top gates and the tunnel coupled back gate, allows lateral and vertical electron tunnelling to the quantum dots [48]. Similar to the Loss DiVincenzo proposal, an electrostatic control gate is employed here to control the wavefunctions overlap between two neighbouring electron, and consequently control the two qubit operations. They have also developed a spin to charge transduction technique to provide spin readout and initialization for this system [15].

Liu et. al. proposed a Si double quantum dot MOS structure with a 15 nm SOI thick layer as a platform for spin based quantum computing. They managed to tune the tunnel coupling between two dots to demonstrate an excitation spectrum for weakly coupled dots and energy level anticrossing for strongly coupled ones at 30 mK. For weakly coupled dots they describe a resonant tunneling through the quantized energy levels reflecting the electrostatic interdot coupling between the two dots. As for the strongly coupled dots, they observe a clear energy level anticrossing caused by quantum interdot tunneling [50]. The structure used by Liu et. al. can be seen in fig. 3.8 below. A positive potential is applied to the top gate to form an electron inversion layer in SOI, and negative potentials are applied to the lower poly-si gates to deplete electrons in the underlying SOI layer and create tunnel barriers the at define the Si quantum dots. This structure presented a fully tunable Si QDs with both charge and energy quantization. However, this structure may suffer from parasitic dots formation due to the oxidation process, the roughness at the Si/SiO2 interface or in the Poly-Si gates themselves [50].

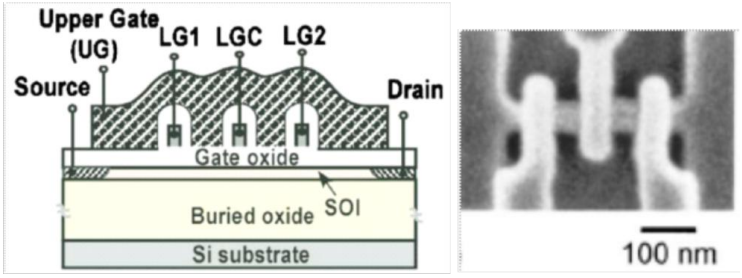


Figure 3.8: Schematic of the SOI MOS-like double QDs structure introduced by Liu et. al. [50].

A Si 2DEG proposal was introduced by Lim et. al. from the University of New South Wales. They developed a tunable gated double quantum dots in intrinsic Si, Al gates were used to define two series connected QDs in the intrinsic underlying Si layer. The middle Al barrier gate offered a wide electrical tuning range of the interdot coupling between the QDs from the weakly coupled to the strongly coupled regime, demonstrating resonant single electron tunneling through the double QDs ground and excited states [51]. The device was fabricated by defining metal barrier gates and a metal top gate on top of an 8 nm oxide layer that covers the intrinsic Si device layer, the two Al gates layers are separated by 5 nm Al2O3 produced by oxidizing the first Al barrier gates layer in oxygen plasma. The device is show in fig. 3.9 below, the top gate and the three barrier gates form a 2DEG layer in the intrinsic Si and the barrier gates locally deplete the 2DEG to form three tunnel barrier forming two adjacent QDs in the intrinsic Si, the quantum dots size is defined by the Al gates dimension and spacing to be 30 nm x 50 nm [51].

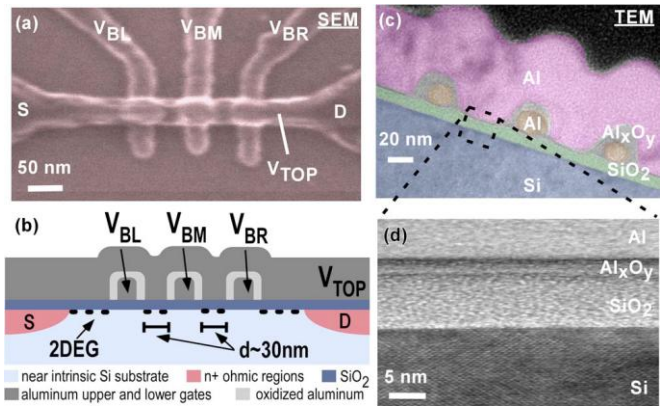


Fig. 3.9: (a) SEM image of the Si 2DEG MOS device introduced by Lim. et. al., (b) and (c) schematic and TEM cross sections of the same device, (d) TEM cross section image of the Si substrate, 8 nm SiO2, 5 nm Al2O3 and the Al top gate [51].

They reported a charging energy of 5 and 2.5 meV for the two QDs at 50 mK, and they estimated 20 electrons dot occupancy. To enable device operation in the few electron regime, the authors propose integrating a charge detector into their structure and to introduce more plunger gates to control each QD independently [51].

As a follow up to the Si 2DEG efforts at the University of New South Wales, Podd et. al. introduced a similar structure that includes a charge sensor which can be used to confirm QD single electron occupancy and to provide single shot measurement of the electron spin state. This structure consisted of two single electron transistors (SET) electrostatically formed in bulk Si using Al surface gates, the two SETs are facing each other, one used as a quantum dot and the second as an electrometer. They demonstrated that the addition of one electron to the quantum dot induced a charge equal to 0.2e on the SET electrometer at 100mK [52]. An SEM image of the device is shown below. The shared Al barrier gates approach was adopted for ease of fabrication, however because they are used to define both the QD and the electrometer operating regime, this approach has limited the device operation. Due to this the minimum QD electron occupancy number was 25 at the lowest possible barrier gate potential (lowest possible for the electrometer to also be operational) and the authors concluded with the need to replace the shared barrier gates with independent control gates to allow access to the few electron regime and provide a more tunable device [52].

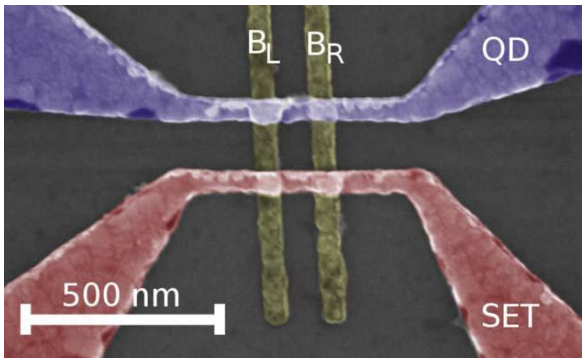


Fig. 3.10: SEM image of the Si 2DEG device introduced by Podd et. al. [52].

The Si MOS double QDs device shown in fig. 3.9 included barrier control gates to define the tunnel barriers and a top gate to control the quantum dot and the accumulation layer electron density at the source-drain simultaneously. As a result the source-drain become depleted and switched off as the number of electrons in the QD is reduced, this makes it difficult to reach single electron dot occupancy with such structures. Therefore, a more advanced silicon metal oxide semiconductor quantum dot was once more reported by Lim et. al. in 2009, the device they developed this time included electrostatic gates that control the quantum dot and the source-drain electron densities independently, enabling this device to operated in the single electron regime where the QD occupancy can be reduced to a single electron while maintaining a large electron density in the source and the drain. This optimized structure is shown in fig. 3.11 below [53].

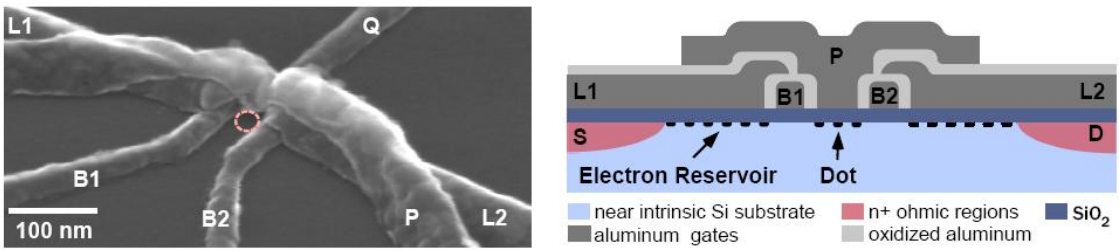


Fig. 3.11: SEM image and schematic cross section of the Si MOS three control gates layers structure developed by Lim et. al. [53].

The QD formed by this structure has a size of 30 nm X 50 nm and 50 mK measurements showed that the QD has a charging energy of 6meV. With this high tunability QD structure the authors observed single electron occupancy in the Si QD [53]. In 2011, the same research group from the University of New South Wales integrated the device shown in fig. 3.11 with another identical structure to be used as a charge detector. The spacing between the QD and the island of the SET charge sensor was 120 nm, and they successfully identified single electron QD occupancy using the electrometer [54].

All of the Si electron spin proposals discussed so far are based on defining quantum dots and structure electrostatically in Si. At the same time, many other proposals have introduced electron spin qubits by lithographically defining quantum dots in silicon on insulator layer (SOI). One of the early proposals based on this approach was the work done by Kodera et. al., they fabricated a single quantum dot single electron transistor (SET) in a heavily doped n-type (phosphorus doping level of 2.9×10^{19} cm^{-3}) with lithographically defined constrictions using electron beam lithography and reactive ion etching,. They observed two series of Coulomb diamonds with different periodicity, evidence of the formation of two different size quantum dots inside the single island of the patterned SET (the final size of the SET QD is 50 nm x 50 nm after oxidation). They conclude that a smaller quantum dot and a top gate electrode is necessary to provide better electrostatic tuning of the single electron transistor [55].

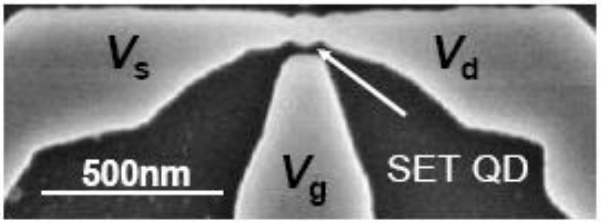


Fig. 3.12: SEM image of the single electron transistor studied by Kodera et. al. [55].

Rossi et. al. investigated a device that is very similar to the SET structure in fig. 3.12 above, their structure included two identical SETs facing each other, where the quantum dot of the SETs are capacitively coupled together. The structure is lithographically defined in heavily doped n-type SOI and the fabrication process of this device is also very similar to the one used by Kodera et. al. to

fabricate their SET structure. The authors investigated using their structure for charge sensing, where one SET is used as a quantum dot and the second as a single electron electrometer, below is an SEM image of the structure investigated by Rossi et. al. [56].

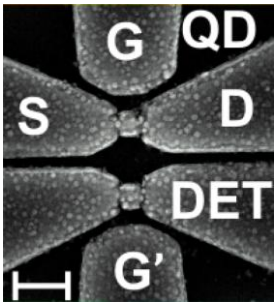


Fig. 3.13: SEM image of the structure investigate by Rossi et. al., scale bar is 200 nm [56].

Yamahata et. al. also proposed the use of a Si quantum dot (QD), with two lithographically defined constrictions and side gates to offer tunable coupling of neighboring QDs as a candidate to implement a spin based quantum computing system. The device they introduced consisted of two quantum dots (a main QD and an unintentional formed second QD) coupled in series with a top gate and side gates; the top gate is used to control the concentration of electrons in the QDs by creating an inversion carriers layer. They demonstrated electron transport through the Si double quantum dots and modulation of inter-dot electrostatic coupling between the two QDs using the side gate at 4.5K [57]. The QD confinement principle for this device is based on the surface potential associated with the constrictions region, it has been previously demonstrated that potential tunnel barriers effectively form a QD between the lithographically defined constrictions [12]. This device was fabricated with e-beam lithography in a 60nm SOI, reactive ion etching was used to transfer the pattern, thermal oxidation to from the gate oxide and shrink the device dimensions, and finally the poly-silicon top gate was deposited using LPCVD and was utilized as ion implantation mask during the formation of the n-type source and drain regions. Figure 3.14 (a) below shows an SEM image of the fabricated device, the right side constriction has a bumpy side wall, this led to the formation of a smaller unintentional quantum dot in the right constriction as shown in fig. 3.14 (b), dimensions of these coupled quantum dots and their potential diagram is also shown. Yamahata et. al. also studied the honeycomb charge stability diagram of this device at 4.5K, from which they obtained the charging energies of these two quantum dots to be 10.1 and 17.2 meV, these values indicate the formation of unintentional smaller quantum dot, they estimated that the two quantum dots sizes to be 55 x 35nm and 20 x 10nm [57].

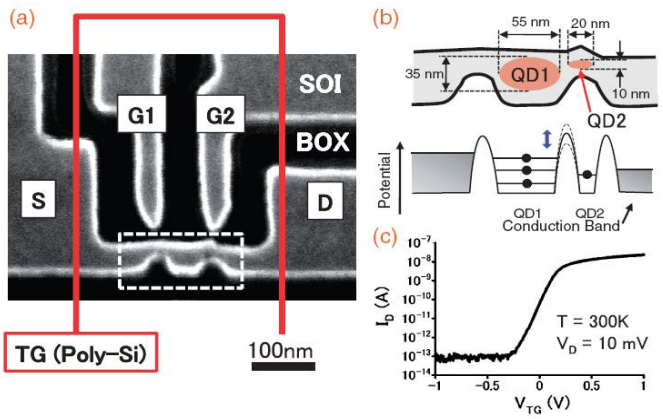


Figure 3.14: (a) SEM image of the device developed by Yamahata et. al., (b) schematic presentation of the double QDs, (c) drain current of the double QDs as a function of the top gate potential [57].

In 2011 Yamahata et. al. introduced another lithographically defined quantum dot device, this time the device consisted of three constrictions between the source and drain, five side gates to control the potential of the quantum dots and the constrictions, and also a top gate (similar to the previous device) to tune the carrier density in the device. From the electron transport measurements, the authors concluded that the size of both their QDs is close to 70 nm x 40 nm, an SEM image of this device is shown below [58] , [59]. The fabrication process for this device was the same as the one described above for the first device (fig. 3.14). However, the dry etch process to transfer the device pattern to SOI for this device used Cl_2 gas chemistry instead of CF_4 gas chemistry. Etching with Cl_2 provided a smoother surface and more vertical sidewalls than before; this eliminated surface deformation and the unwanted localized potentials that lead to the formation of the unintentional quantum dot in the right constriction of their previous device [60].

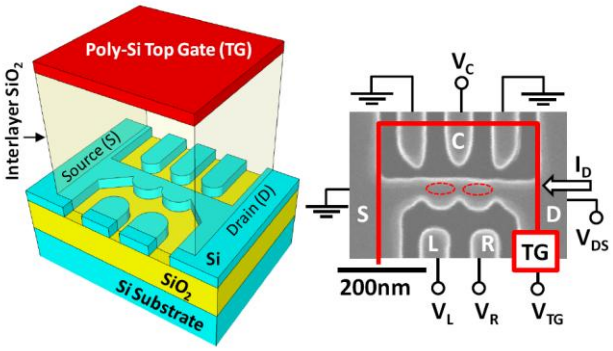


Figure 3.15: Schematic view and SEM image (showing potential set up) of the double QDs device used by Yamahata et. al. for their spin relaxation experiments [59].

Using the device shown in fig. 3.15, Yamahata et. al. observed spin dependant tunneling and investigated spin relaxation in Si double QDs by studying the leakage current produced by varying the QDs interdot coupling and the external magnetic field while the device is in Pauli spin blockade

regime. Their experiments concluded that at low external magnetic field level of 40 mT, they can observe a dip in the leakage current which they attribute to spin-orbit mediated spin relaxation. While at a higher magnetic field level of 400 mT, they observe a peak in the leakage current and they expect this effect to be caused by spin-flip cotunnelling [59], [61].

Other lithographically defined single electron devices include structures that have no etched constrictions but are based on doping modulation in silicon nanowires. These structures commonly use two deposited silicon oxide or nitride spacers on both sides of a Poly-Si gate wrapped around an etched SOI nanowire as a self-aligned mask for a subsequent ion impanation process for n+ source and drain regions. Therefore, the area underneath the SiO2 spacers is undoped creating doping modulation along the nanowire and these two undoped areas of the NW act as two tunnel barriers. These structures are relatively simple to fabricate, however the main drawback is the fact that the tunnel barriers that are created by the variation in the nanowire doping profile are fixed by the lithography process and cannot be adjusted [62], [63]. Fig. 3.16 and 3.17 below shows images of these structures.

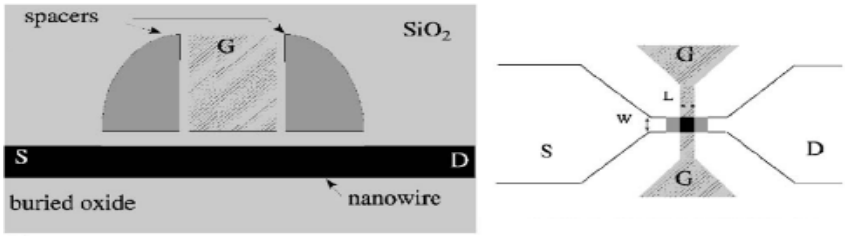


Fig. 3.16: Left: cross section of a single dot SET along the channel, right: top view schematic of the SET where the nanowire is heavily doped except for the grey area under the spacers [62].

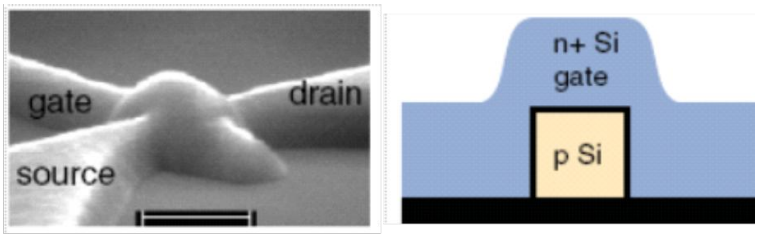


Fig. 3.17: Left: SEM of a single QD structure based on doping modulation developed by Lansbergen et. al., right: cross section schematic taken perpendicular to the SOI NW [63], [64].

3.4 Summary

It is clear that all the different platforms introduced in this chapter have advantages and drawbacks; it is also a difficult task to directly compare these platforms as they offer different number of quantum gates and different initialization and measurement methods. However, it is safe to use a property directly related to the quantum information unit (qubit) itself to subjectively compare these various types of quantum computing platforms. The corruption of any qubit information has two scales, taking the example of an electron spin qubit then the first time scale is the relaxation time (T_1) of the quantum information from the qubit excited state (spin-up) to the qubit ground state (spin-down), and it represents the loss of the classical information stored in the spin state. The second time scale is the coherence time (T_2) which represents decoherence of the qubit (spin) state and more specifically it represents the loss of the phase information stored in the spin state. For most systems the relaxation time is a number of magnitudes larger than the coherence time which makes T_2 a more suitable parameter to compare different platforms [21], [65].

Table 3.1: Measured coherence time (T_2) for various quantum computing platforms [21], [65].

Qubit platform	Coherence time (T_2)	Reference
Infrared photon	0.1 ms	[66]
Trapped ion	15 s	[67]
Trapped neutral atom	3 s	[68]
Liquid molecules nuclear spins	2 s	[69]
Electron spin in GaAs 2DEG QD	3 us	[70]
Electron spin bound to phosphorus in ^{28}Si	0.6 s	[71]
Ensemble of MOS-based QDs	30us	[72]
^{29}Si nuclear spins in ^{28}Si	25 s	[73]
Electron spin in Si/SiGe 2DEG QD	3 us	[74]
Electron spin in Si/SiO2 2DEG QD	0.3 us	[72]
Superconducting circuit	4 us	[75]

The most actively perused solid state quantum computing proposals at the moment are those involving impurity spins, electron spins and electron charge. Below is a comparison table that shows how each of these methods fulfils the DiVincenzo criteria [2] and [20].

Semiconductors electron spin-based solid state quantum computing proposals offer inherent scalability, use of the advanced and well established semiconductor technologies, compatibility and integrability with current CMOS technologies. The electron spin state in semiconductors is also a natural two level system, making it a perfect candidate for qubit representation, and semiconductor spin qubits can be decoupled from charge fluctuations which leads to long spin qubit decoherence times [5]. Silicon in particular, is a very attractive candidate for quantum computing due to its low spin-orbit coupling, the recent development of isotopically pure Si materials (^{28}Si 99.9%) also works in favour of Si-based systems by reducing nuclear-spin interactions and further increasing spin decoherence time.

Finally, the most significant advantage of using Si is the advanced state of Si fabrication techniques currently available, offering a shared platform for both quantum electronics and advanced complex integrated circuits [47], [65]. All of this has provided motivation for this research work; to develop an integrated single-electron spin qubits for the first time using a silicon-on-insulator (SOI) technology, the silicon based integrated single spin quantum information technology platform [SISSQIT], and to demonstrate its operation based on single-spin operation [19]**.**

Table 3.2: Comparison of currently perused quantum computing proposals [2], [20].

The DiVincenzo Criteria	Electron Charge in QDs	Electron Spins in QDs	Impurity Spins
A scalable physical system with well characterized qubits.	Electrons confined in lithographically defined quantum dots.	Lithographically defined QDs, Spin confinement in 2-D systems, or high spin magnetic nanoparticles.	Shallow donors in Si, SiGe and GaAs, Paramagnetic ions in C_{60}.
The ability to initialize the state of the qubits to a simple fiducial state.	External voltages are used to control the electron position.	Electron spins requires cryogenic temperatures, individual spin preparation using magnetic field gradients.	Dynamic nuclear polarization, optical pumping, electric field or magnetic field gradients.
Long decoherence times, much longer than the gate operation time.	Electron spatial coherence times in the range of 1ns in GaAs QDs.	GaAs electron ensemble decoherence time measurements in the range of 1us, with gate operation time in the order of 1ns.	Phosphorous in Si ensemble decoherence time measurements of 1ms, with gate operation time in the order of 1ns.
A universal set of quantum gates (techniques used to perform single qubit rotation and two qubit coupling).	Techniques used for single qubit operation: electrostatic gates.	Techniques used for single qubit operation: local magnetic fields, spin rotation using electron spin resonance (ESR) and magnetic field gradients.	Techniques used for single qubit operation: nuclear resonances using surface gates, optical resonance techniques, and local magnetic and rf fields.
A qubit-specific measurement capability.	Simple electrostatic readout using SETs, or optical techniques like luminescence readout and ensemble optical readout.	Spin to charge conversion, spin filters such as magnetic semiconductor, detection of spin polarized transport current thorough the QD, and magnetic resonance force microscope (MRFM)	Information stored on nuclear spins can be transferred to the impurity electron spin through the hyperfine interaction; the same techniques outlined for measurement of electron spin can be used.

Chapter 4

Silicon-based Integrated Single-Spin Quantum Information Technology (SISSQIT)

4.1 Introduction

As discussed earlier, the first Si-based qubit was proposed by Kane [34] using nuclear spins of phosphorous donor atoms in silicon benefitting from the very long decoherence time of nuclear spins in Si. However, the proposal requires extreme bottom-up nanotechnologies, e.g. STM lithography, to control the number and position of the P donor atoms within the silicon wafer.

An exquisite degree of control over single electron spins has been demonstrated for quantum dots defined on the two-dimensional electron gas formed at the GaAs/AlGaAs heterojunction by using top-down lithography technology [42]. Unfortunately the coherence of electron spins deteriorates rapidly in GaAs due to its rich nuclear spin density; electron spins can be confined in silicon based QDs, benefiting from the low nuclear spin density of silicon based materials [76]. Recently, QDs capable of confining few electrons have become feasible in silicon [46], providing a motivation for this research. Here, we propose a new Si-based double spin qubit system on ultrathin silicon-on-insulator (SOI) and present the design, layout and operation scheme of the integrated system.

The SISSQIT platform is proposed here as a novel Si-based double spin qubit system on ultrathin Silicon-on-insulator (SOI), co-integrated with a single electron electrometer, a μ-ESR and a nanomagnet. Table 4.1 below shows the DiVincenzo criteria for quantum computation and the proposed SISSQIT methods for satisfying these requirements.

Table 4.1: Summary of the DiVincenzo criteria and the SISSQIT system approach.

DiVincenzo Criteria Requirements	SISSQIT Implementation
1. A scalable physical system with well characterized qubits.	Electron spins qubits in silicon.
2. The ability to initialize the state of the qubits to a simple fiducial state.	A magnetic field is used to prepare the initial state of single electron spins.
3. Long decoherence times, much longer than the gate operation time.	Long spin decoherence times in silicon have been demonstrated, and fast gate operations can be achieved using electrostatic gates.
4. A universal set of quantum gates.	An electrostatic control gate will be used to control the entanglement of two qubits.
5. A qubit-specific measurement capability.	A single electron transistor will be used to readout the spin state utilizing a spin to charge conversion method.

4.2 Overview of the SISSQIT Platform

The proposed system of silicon-based integrated single-spin qubits (SISSQIT) is schematically shown in Fig. 4.1. The system is to be formed on an ultrathin intrinsic silicon-on-insulator (SOI) substrate and features double single electron transfer devices (SETDs) built as parallel SOI nanowires (NWs) where their edges are interconnected by another short NW. There is an upper metal gate used to induce a weak inversion channel in the NWs. The individual SETDs are equipped with a pair of lower poly-Si control gates (LTG1a,b and LTG2a,b), and one other poly-Si gate (JG) is placed in the middle of the interconnect. This SETD pair is integrated with three other key components [19]: An in-plane single-electron electrometer formed adjacent to the edge of the upper SETS, a μ-ESR device formed by using a metallic waveguide and placed near the interconnect NW, and finally a nanomagnet which generates a magnetic field gradient along with the interconnect NW.

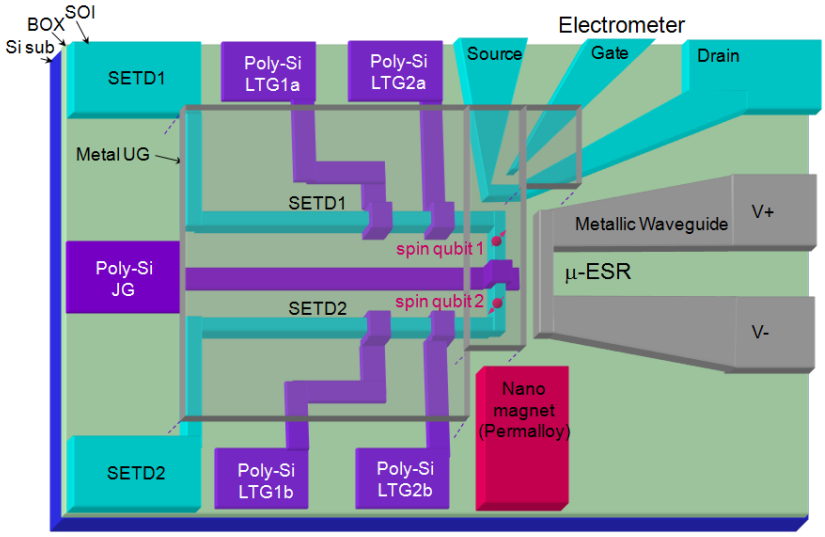


Figure 4.1: Schematic diagram of SISSQIT platform [19].

The proposed fabrication process for the double spin qubit platform is to pattern the NW MOSFET channel and the electrometer on an ultrathin intrinsic SOI substrate using electron beam lithography. Thermal oxidation will be used to reduce the effective channel dimensions and subsequent pattern transfer will be done with dry etching and deposition. The poly-Si gate width and spacing are intended to be about 100 nm. After all the patterning is completed, an interlayer oxide and an upper metallic gate will be deposited. At the L-shaped corners on the edge of the NW interconnect, oxidation is accelerated due to stress (known as the PADOX process [77]). The PADOX process leads to the formation of electrostatic potential barriers at the L-shaped corners, which creates another QD in the middle of the interconnect [19]. The nanomagnet and the metallic waveguide are included to selectively address and control the rotation operation of the two spin qubits by utilizing qubit specific electron spin resonance conditions created by a Zeeman energy gradient induced by the nanomagnet, both components are to be patterned with e-beam lithography, evaporation and lift off.

4.3 SISSQIT Operating Principles

The SISSQIT platform aims to demonstrate the full operation of double spin qubits by integrating the following three key techniques in one compact footprint [19]:

4.3.1 Single electron turnstile technology

The first technique is a single-electron turnstile device platform developed by L. J. Geerligs [78]. Researchers at NTT Basic Research Laboratories (NTTBRL) have built on this technology [77], they developed a precisely controlled single electron transfer platform on an SOI substrate to realize a room-temperature single-electron multilevel memory (where each level is given by a single electron) and a time division weighted sum circuit. The turnstile operation is achieved by alternately opening

and closing two metal oxide field effect transistors. The device introduced by NNTBRL also featured a high charge sensitivity electrometer placed next to the electron memory node (MN), to detect the presence of electrons in the memory node. This device is shown in Fig. 4.2 below [77].

In this device, the MOSFET gates control the thickness and height of the formed turnstile energy barriers. This arrangement of dynamically controllable barriers allows room temperature operation by reducing the size of the single electron box (SEB) to a small enough size, so that Coulomb blockade can overcome the thermal energy. The MOSFET controlled energy barriers also demonstrated fast electron transfer times of less than 10 ns, and extremely long retention of 10^4 s [77].

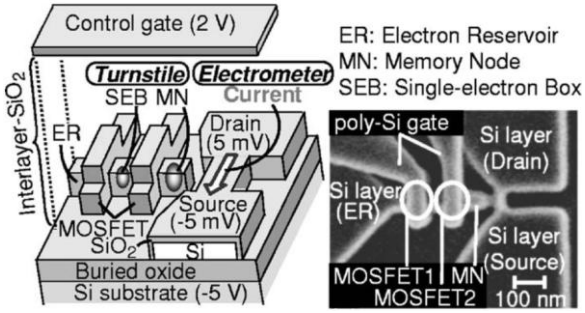


Fig. 4.2: Single electron turnstile and electrometer [77].

The transfer of electrons across the turnstile device is accomplished using the following sequence: When the first MOSFET gate (FET1) of the turnstile device is turned ON, electrons enter the single electron box (SEB) from the electron reservoir (ER). By switching FET1 from ON to OFF, the potential barrier under the poly-Si gate is raised and the transferred electron is confined to the SEB. Turning the second MOSFET gate (FET2) ON and due to the higher energy potential of the SEB, the electrons transfer from the SEB to the memory node (MN). Fig. 4.3 below shows the electron transfer sequence [16]:

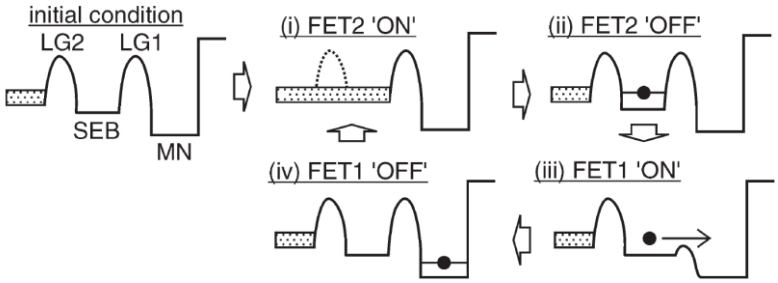


Figure 4.3: Single electron turnstile transfer sequence [16].

Another electron turnstile device was introduced by Ono et. al. from NNTBRL, they used a silicon based dual gate single electron transistor, and applied ac potentials to each of the two gates to achieve single electron transfer at 25 K, the dual gates effectively served as controllable electron channels of a MOSFET. This work was the first demonstration of single electron transfer operation in silicon [79]. An SEM image and a schematic view of this device are shown in Fig. 4.4 below:

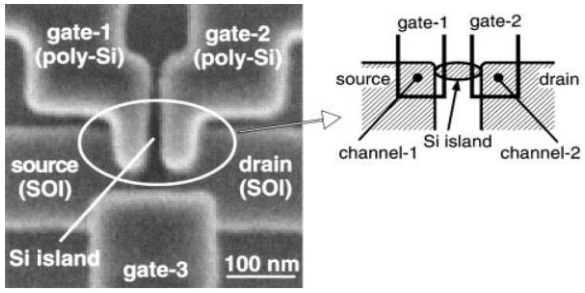


Fig. 4.4: SEM image and a schematic view of the device developed by Ono et. al. [79].

High speed single electron transfer has also been demonstrated using charge coupled devices, shown in Fig. 4.5, where electrically tuneable potential barriers are used to control the electron transfer operation [80]. This device was also developed by NTTBRL, and is very similar in structure and operation to the turnstile device of Fig. 4.2. The single electron turnstile technology is adopted here for the SISSQIT system, to store an electron in the single electron boxes at the top of the individual SETDs, followed by the application of a magnetic field, to prepare the initial state of truly single electron spins.

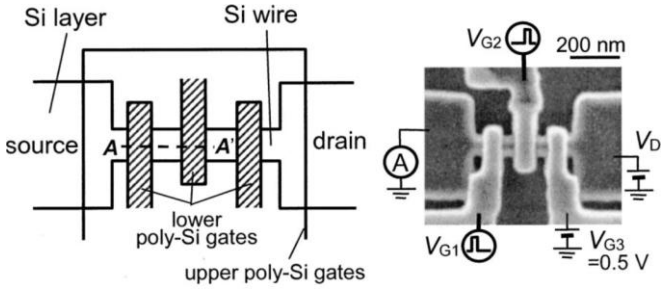


Figure 4.5: Nanometre-scale charge coupled device for single electron transfer, with single electron transfer operation demonstrated at 20 K [80].

4.3.2 High speed charge detection

In electron spin quantum computation, it is necessary to measure the state of an isolated electron spin system without dramatically affecting its coherence. Therefore, it is essential for such systems to employ suitable readout and measurement techniques that satisfy this requirement. The readout requirement for quantum information processing applications has been mainly met by the use of quantum point contacts (QPCs) or single electron transistors (SETs) as charge sensors. Due to their intrinsic sensitivity, very low detector noise, and the possibility to optimize for high-bandwidth operation; QPC and SETs have proven to be very effective as electrometers [81].

The use of a GaAs QPC integrated with an RF impedance matching circuit, for high bandwidth charge sensing measurement has been successfully demonstrated in the work of Reilly et. al. They used the RF QPC to detect single electron fluctuations in the charge configuration of a double quantum dot

structure with 8 MHz bandwidth [81]. The device they developed was based on a GaAs/$Al_{0.3}Ga_{0.7}As$ heterostructure with 2DEG below the surface. A top gate of Ti/Au was used to define the structure of the double quantum dot and the QPC [81].

The use of charge sensors for single shot readout of an electron spin has been demonstrated in the work done by Elzerman et. al. This work demonstrated spin measurement of an electron confined in a quantum dot using a spin to charge conversion method with a single shot charge detection using a quantum point contact [18]. The spin to charge conversion here is based on correlating the spin state of the electron with its charge state; this is done by applying a magnetic field to separate the two different spin states (spin up and spin down) by the Zeeman energy. The QD potential is then tuned, so that an electron can only remain in the dot if it has a spin up state, and it would leave the dot if it has a spin down state. This way, charge measurement of the QD will determine if there is an electron in the dot or not, reflecting the spin state of the electron [18]. The quantum dot featured in this work was formed in the two dimensional electron gas (2DEG) of a GaAs/AlGaAs heterostructure by applying negative potential to metal surface gates. The QD and the QPC are shown in the figure below:

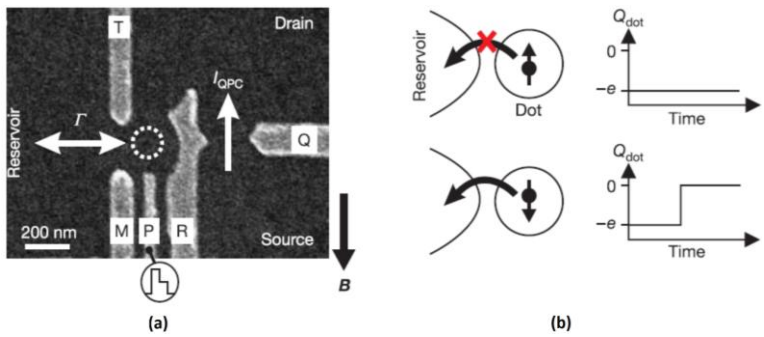


Fig. 4.6: Spin measurement using a spin to charge conversion method, (a) quantum dot coupled to a quantum point contact, (b) spin to charge conversion principle, where the charge on the QD only remains constant if the electron spin is up [18].

Single electron transistors have also been used as charge sensors, and dynamic charge sensing has been reported with the use of radio frequency reflectometry. Angus et. al. reported the use of a silicon radio frequency single electron transistor for charge measurements displaying charge sensitivity of greater than 10 μe/$\sqrt{Hz}$ at megahertz bandwidth . The Si RF-SET island was defined by electrostatically controllable tunnel barriers in a narrow channel silicon MOSFET. Compared to previous attempts of utilizing aluminium RF SETs; silicon RF-SET demonstrated higher charge sensitivity, higher operating temperatures and simpler fabrication flow [82]. This Si RF-SET has been recently used to measure the charge state on a silicon quantum dot as shown in Fig. 4.7 below:

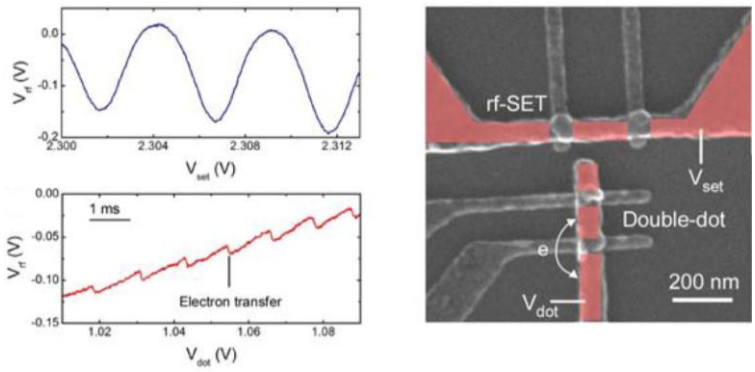


Figure 4.7: Si double QDs with the RF-SET (right), charge detection characteristics (left) [82], [83].

SOI based SETs have also been demonstrated, and as mentioned earlier they offer higher operating temperature compared to similar 2-DEG systems. Manoharan et. al demonstrated operation of an SOI based radio frequency single electron transistor at a temperature of about 12.5 K with charge sensitivity estimated to 36 μe/$\sqrt{Hz}$. The RF SET reported in this work operated with charge offset stability, long term drift stability, and good charge sensitivity at high operating temperatures (compared to cryogenic temperature) [84].

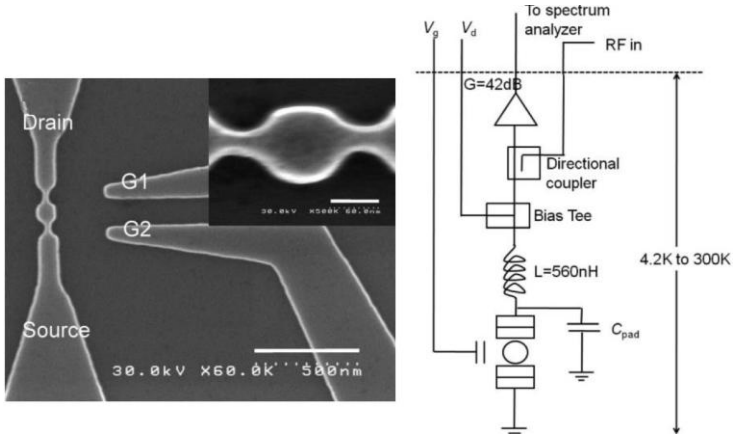


Fig. 4.8: SEM image of the silicon SET developed by Manoharan et. al, and a schematic showing the RF and DC measurement setup [84].

Si RF-SET can provide high speed charge detection, and realize a single-shot measurement of the Si qubits, i.e. to perform an unaveraged measurement of electron spin within the spin relaxation (T1) time. This type of measurement also has the advantage of suppressing unwanted backactions from the electrometer and improving decoherence time of the qubits. Therefore the SISSQIT platform will utilize and a reflection type Si RF-SET, in which RF waves reflected from the electrometer are measured using an integrated LC resonant circuit for impedance matching [19].

4.3.3 Spin to charge conversion

The third key technique to be employed is the detection of single-spin states based on a spin-to-charge conversion method by utilizing spin-dependent single electron tunnelling rates. This measurement method employs energy selective readout based on the Zeeman energy splitting in a single QD [85].
The magnetic moment of an electron spin is very small and difficult to directly measure. Therefore, an electrical measurement, rather than a magnetic measurement, specifically a spin to charge conversion measurement is usually employed for spin readout. This method is based on converting the electron spin state to a correlated charge state and subsequently measuring the charge state using a quantum point contact or a single electron transistor to determine the spin state [85]. There are mainly two schemes used for spin to charge conversion:

- The first technique employs an energy selective readout (Fig. 4.9a). This method places the spin levels close to the electrochemical potential of the electron reservoir of the semiconductor QD, this arrangement allows the electron to tunnel off the quantum dot if it has a spin excited state (ES) and energetically forbid the tunnelling of electrons from the spin ground state (GS), detecting the quantum dot charge then determines the electron spin orientation [85].
- The second technique is a tunnel rate selective readout (Fig. 4.9b). In this method, an electron is allowed to tunnel off the quantum dot to the reservoir regardless of its spin state, but the tunnel rate strongly relies on the spin state of the electron. The tunnel rate of an electron in a spin excited state (ES) is higher than the tunnel rate of an electron in a spin ground state (GS). Therefore, the spin state of the electron can be determined by measuring the number of electrons in the quantum dot; if the electron has left the QD that means it has an ES spin state, while the spin state is declared as GS if it the electron is still in the QD [85].

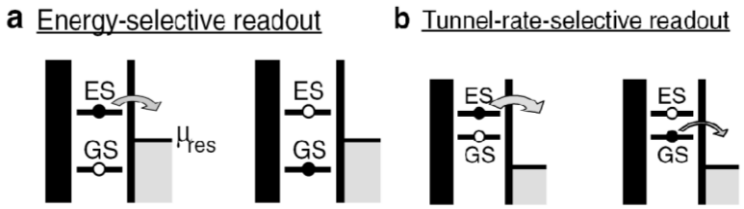


Fig. 4.9: Energy diagrams showing the two methods for spin to charge conversion. Thick arrows represent higher tunnelling probability than thin arrow, and μ_{res} is the potential of the reservoir [85].

Hanson et. al. have demonstrated readout of two spin states using the tunnel rate selective readout method and achieved a single shot visibility of about 80%. They used in their setup a quantum dot and a quantum point contact defined in a 2DEG below the surface of a GaAs/AlGaAs heterostructure [85]. A single shot readout was successfully demonstrated but the term single shot here reflects the fact that the spin measurement in this work was destructive. A destructive measurement is a measurement, in which the state after the measurement is identical to the measurement outcome, any

second measurement produces a different outcome compared to the original measurement, and the single shot tunnel rate selective readout, in particular, changes the number of electrons in the dot after readout.

A successful implementation of a non-destructive spin to charge conversion readout was demonstrated by Meunier et. al.[86]. They adopted a tunnel rate dependant readout scheme, and demonstrated operation of this scheme to distinguish two electron singlet from triplet states in a quantum dot with the spin state remaining the same before and after the measurement (non-destructive measurement as the spin state remains the same after the measurement) [86]. The 2DEG QD with a QPC experimental setup of this work is very similar to the work introduced by Hanson et. al.[85]. An energy diagram of the quantum dot demonstrating the singlet/triplet non-destructive measurement scheme is shown below. For a singlet initial state, the state remains single through the whole measurement and doesn't change. For a triplet initial state, the state is reinitiated to triplet state after the measurement process. The excited orbital has a stronger overlap with the reservoir compared to the lowest orbital, this leads to the high tunnel rate to and from the triplet state compared to the low tunnel rate to and from singlet state. During the measurement, the dot potential is pulsed for a short time period τ at zero magnetic field to keep the electrochemical potential of both the singlet and triplet states above the Fermi level of the reservoir, however this time period is designed to be less than the tunnel time of the singlet state and therefore only allowing tunnelling to and from the triplet state and no tunnelling to or from the singlet state even though it is energetically allowed [86].

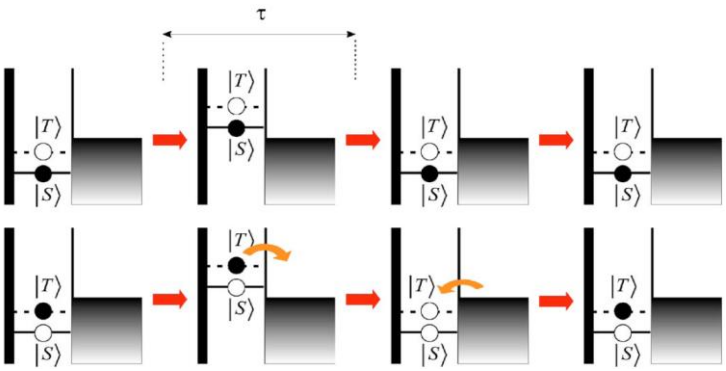


Fig. 4.10: Energy diagrams of a quantum dot showing non-destructive measurement for a singlet spin state (top) and a triplet spin state (bottom), arrows represent the tunnelling events [86].

Other attempts that investigated the use of spin to charge conversion based on spin dependant tunnelling readout includes the work done by Liu et. al. [87]. They investigated the spin dependence of single electron tunnelling for an SOI based double quantum dot structure, and successfully accessed the singlet and triplet states of two electrons in the double quantum dot [87].

The spin to charge conversion technique will be employed in this project to make use of the energy difference between spin states that is caused by the Zeeman energy due to a static magnetic field. This

technique is very similar to the approach employed in [88] to measure the spin relaxation time in a GaAs single quantum dot. The SISSQIT spin to charge conversion will employ an energy selective readout method and proceeds as follows: the QD at the end of SETD1 will initially be fully depleted of electrons in a static magnetic field, the Zeeman energy levels will then be pulsed lower than the Fermi level of the electron source electrode, this causes a single electron with a random spin state to enter the QD. After that, a second pulse will be applied such that the lower Zeeman level is placed lower than the Fermi level of the electron source, and the upper Zeeman level is above. This setup will energetically prohibit any tunnelling from the lower Zeeman energy level (if it is occupied). However, tunnelling from the upper Zeeman level is allowed, where the QD is emptied and then refilled into the lower sublevel [19]. Finally, for the integrated SET to act as an efficient electrometer and accurately monitor the electron occupancy of the QD and consequently demine the spin state; the tunnel rates should be adjusted to the following [19]:

$$\frac{1}{T_1} < \Gamma_{tunnel} < \Gamma_{detection} \tag{4.1}$$

Where T_1 is the spin relaxation time, Γ_{tunnel} is the electron tunnelling rate and $\Gamma_{detection}$ is the measurement bandwidth.

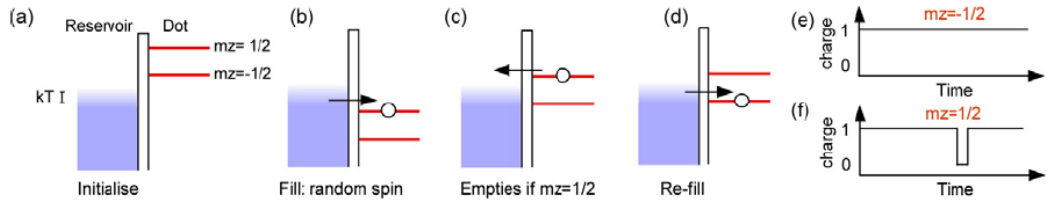


Fig. 4.11: SISSQIT spin to charge conversion scheme. (a) - (d) Voltage pulse sequence for single electron spin detection, events (c) and (d) only occur for the case of a spin up. (e) and (f) are the SET characteristics in the case of a spin down and a spin up electrons [19].

4.3.4 Controlled interaction of two electron spins

In the SISSQIT platform, two electrons spins will occupy two adjacent quantum dots (spin qubit1 and spin qubit2). This project aims to demonstrate independent control of each electron spin in the adjacent QDs, and to establish a controllable interaction between the electron spins. Control of the individual electron spins will be established using the nanomagnet and the nanoscale electron spin resonance (ESR) waveguide. The nanomagnet produces a magnetic field gradient across the quantum dots; this gradient will consequently create a Zeeman energy gradient and form a different ESR condition for each of the dots, making it possible to use only one ESR to control the rotation operation of two separate electron spins.

A similar approach has been previously demonstrated by Laird et. al. [89], they used a micro-magnet in proximity to GaAs QDs to demonstrate the magnetic field gradient between these dots, they also presented a scheme (very similar to the one described above) to selectively address individual electron spins in any of the dots [89]. The interaction between two electron spins will be carried out using a gate controlled exchange interaction. Where the electrostatic control gate JG, between the two adjacent QDs, will be pulsed to establish a strong exchange coupling between the two electrons [19].

4.4 SISSQIT Operation

Basic operation of the proposed spin qubit system is shown in Figs. 4.12(a) – (d). Firstly, two individual electrons are transferred from the electrodes, source1 and source2, towards the edge of the NWs (Fig. 4.12a). The two single-spins are called the spin qubit 1 and 2 hereafter. The L-shaped corners at the bottom of the NWs act as an electrostatic potential barrier caused by pattern-induced oxidation (PADOX) process, and the spin qubits 1 and 2 are therefore confined in the QDs formed between the 2nd lower gates (LTG2a and LTG2b) and the L-shaped corners. A sufficiently high external magnetic field is then applied to initialize the two spin qubits [19].

The nanomagnet placed near the edge of SETD2 generates a significant magnetic field gradient and causes different magnitudes of Zeeman splitting for the 1st and 2nd spin qubits. Manipulation and entanglement of the two spin qubits are achieved by applying a positive voltage to JG, sufficiently large enough so that the spin qubits 1 and 2 surmount the potential barriers at the corners and interact with each other in the QD formed on the interconnect (Fig. 4.12c). After entanglement, the bias voltage to the JG is switched to negative, and the two spin qubits are pushed back to the individual QDs on the SETDs. Finally the spin state of the spin qubit 1 is detected with the single-electron electrometer by using the spin-to-charge conversion method. This method utilizes a difference in the tunnelling probability of spin qubit 1 from the QD back to the adjacent QD between the LTG1a and LTG2a due to a finite Zeeman splitting under an external magnetic field (Fig. 4.12d) [19]. The system presented here is purely based on single-electron-spin operation, and is significantly different to previous Si charge qubits where a few tens of electrons were involved on a fabricated qubit [43].

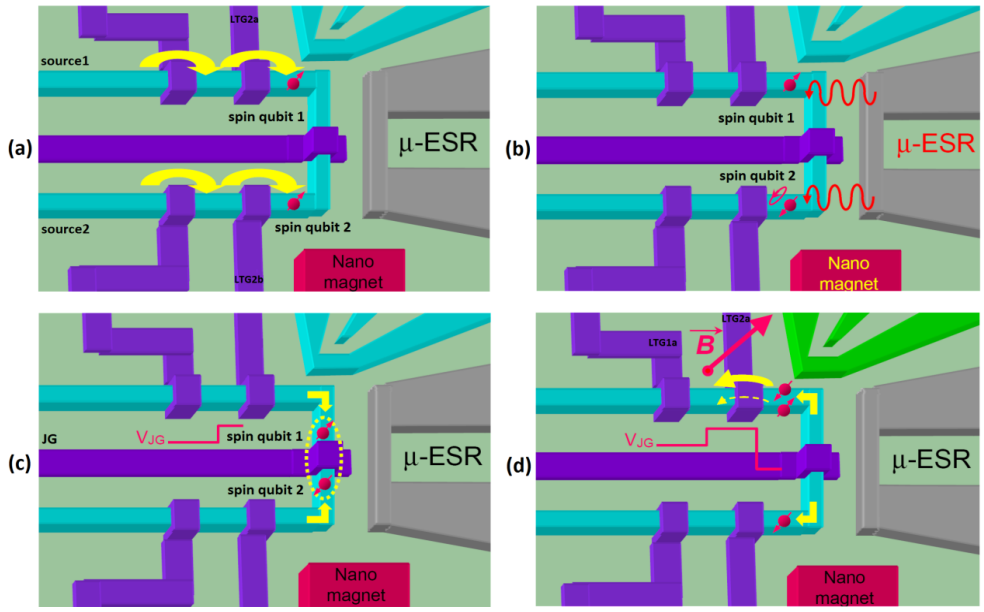


Fig. 4.12: Operation of single spin qubits (upper gate is not shown for clarity). (a) single electron transfer into quantum boxes, (b) selective rotation by using µ-ESR, (c) entanglement and (d) readout using spin to charge conversion [19].

4.5 Project Methodology

The goal of this project is to build an integrated Si double spin qubit system using VLSI compatible techniques and to investigate initialization, manipulation and readout of single spin qubits. The most significant milestone for this project is the fabrication of a single spin turnstile device (SETD) and an electrometer, the SETD is a series connected MOSFETs with a quantum dot at its end that is capacitively coupled to a single electron transistor; this SETD will be similar to the device introduced by NTBRL in [77]. The SETD MOSFET channel and the electrometer will be patterned on a 30-50 nm intrinsic SOI substrate using electron beam lithography; the electrometer is to be fabricated simultaneously next to the edge of the SETD. The pattering process will then be followed by a thermal oxidation to reduce the effective channel dimensions. Two MOSFET control gates will then be patterned. The NW channel width will initially be set to 100 nm, the control gates are intended to have a width and spacing of about 100 nm, and the spacing between the SETD quantum dot and the electrometer is chosen initially as 100 nm. However, after optimizing the oxidation process parameters, the NW width will be reduced to 50 nm or less, to reduce the dimensions of the QD and ensure single electron transfer operation. The separation between the electrometer and the SETD quantum dot will also be reduced to about 50 nm or less, to increase the electrometer sensitivity. The final step in the fabrication of the SETD with the electrometer is the deposition of an interlayer oxide and an upper metal gate [19].

3D structural design, simulation and dynamical analysis of the SETD with an electrometer operation and the operation of an interconnected double SETDs (series connection between two SETD devices)

with an electrometer operation will be carried out by combing 3D FEM capacitance simulation and Monte Carlo single electron circuit simulation. After sufficient experimental verification and optimization of the transfer and detection operations, the interconnected double SETDs will be integrated with a μ-ESR, multiple control gates and a nanomagnet, forming a fully integrated double spin qubit system [19].

4.6 Summary

Chapter four presented the SISSQIT platform in great detail; we presented a practical system of two spin qubits by integrating all the key components in one compact silicon platform, which features excellent versatility, scalability and compatibility with conventional VLSI technology**.** This is the minimum necessary system to demonstrate the full operation of double spin qubits but can be scaled-up in a straightforward way to large scale systems in the future.

The work presented in this report proposes an SOI-based integrated platform for electron spin initialization, manipulation and readout. The design and fabrication of the main building blocks of this platform the single electron transfer device (turnstile) and the electrometer are presented in this report.

The focus of this report is the two main building blocks of the SISSQIT platform: the single electron transfer device and the integrated charge sensor. Even at this level, the single electron transfer and detection platform can be used to demonstrate novel experiments in intrinsic silicon quantum dots like spin to charge conversion and the measurement of decoherence time in a single quantum dot in silicon.

Chapter 5

The Single Electron Transfer Device (SETD)

5.1 Introduction

Our approach to the SISSQIT system is to break down the platform into its building blocks: Single spin transfer device, electrometer, u-ESR and a nanomagnet. We aim to build up a design library and standardise the design and fabrication process for each of these components. The first of these building block devices to be designed, simulated, fabricated and tested is the single spin transfer device (SETD) integrated with an in-plane single electron transistor electrometer. This device represents the upper turnstile device and the in-plane SET part of the SISSQIT platform, shown in Fig. 5.1 below:

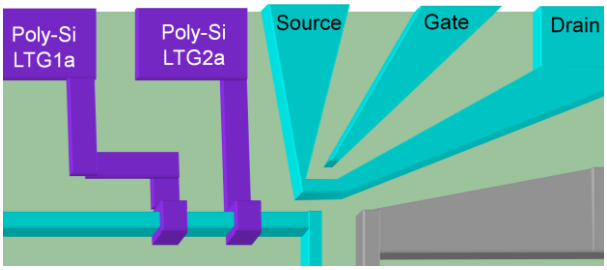


Fig. 5.1: The upper turnstile device and the SET electrometer of the SISSQIT platform [19].

5.2 Layout of the SETD with an electrometer

Initial Layout of the proposed SETD with the electrometer is shown schematically in fig. 5.2 below. The SETD is a series connected two NW MOSFETs with a capacitively coupled single electron transistor electrometer (the SET Island is coupled to the SETD QD) as show in fig. 5.2 [19].

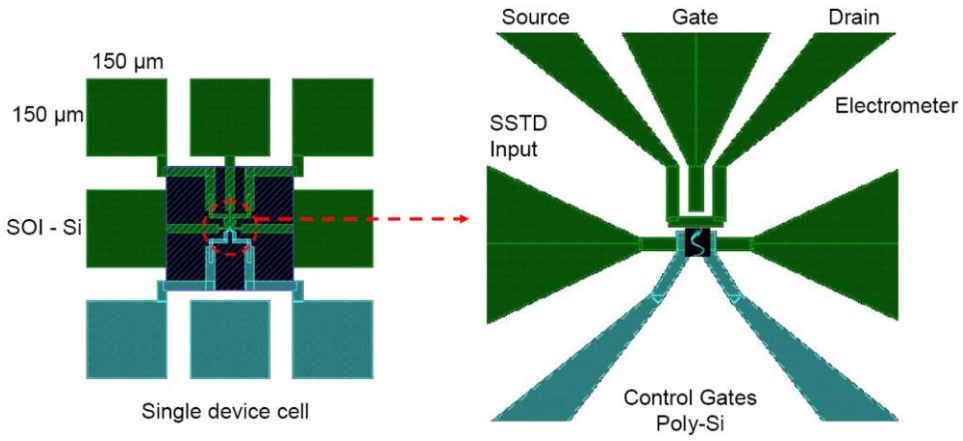


Fig. 5.2: Initial layout for the SETD with the integrated electrometer [19].

Proposed fabrication of the SETD device, shown in fig. 5.2, follows the same fabrication flow outlined for the SISSQIT platform (described in chapter 4). As previously mentioned, oxidation at the L-shaped corners of the electrometer in fig. 5.2 is accelerated due to compressive stress (PADOX). However, the PADOX process conditions can be difficult to optimize and the oxide thickness at the corners of the Si-NWs of Fig. 5.2 can be challenging to control at extremely small dimensions. Therefore, an alternative layout is proposed for the SETD device as shown below:

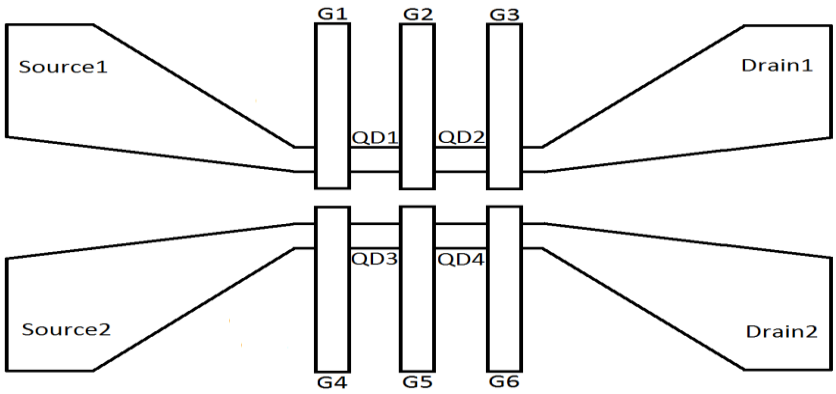


Fig. 5.3: Modified layout of the SETD with an electrometer.

In this new layout, the SETD is a series connected three NW MOSFETs, and the electrometer is a double dot single electron transistor (DSET) instead of a single dot single electron transistor. The DSET electrometer is an axial reflection of the SETD structure (as show in fig. 5.3), and is used to detect changes in the charge state of the two QDs of the SETD (the DSET is capacitively coupled to both of the SETD QDs). The advantage of the modified SETD layout (fig. 5.3) is that it doesn't include any PADOX process as the layout employs straight lines and duplicate designs for the SETD and the integrated electrometer.

5.3 3D FEM capacitance simulations

A 3D model of the SETD device with the electrometer was constructed using COMSOL; COMSOL is a finite element method (FEM) based simulator with a graphical user interface that offers: geometry modelling, computer aided design (CAD) tools, material properties definitions, meshing and various post-processing functions [90]. A 3D view of the structure is shown in fig. 5.4 below:

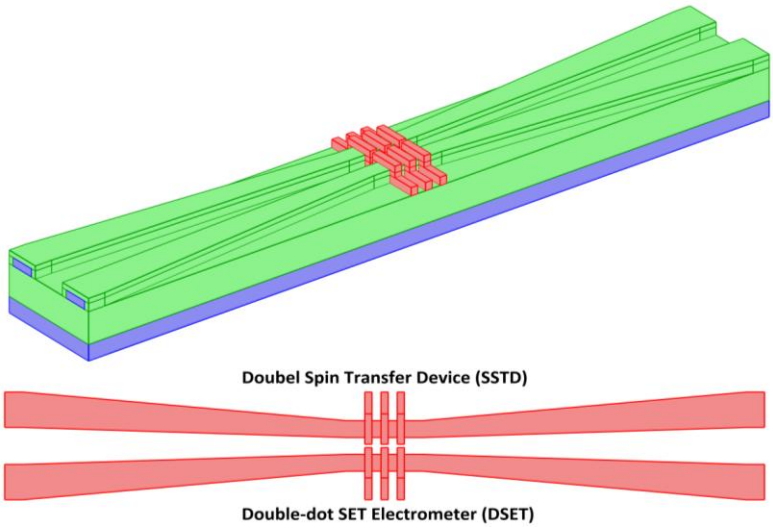


Fig. 5.4: 3D and 2D view of the SETD device with the DSET electrometer (upper gate and upper oxide are not shown for clarity).

The 3D model was based on an SOI thickness of 50 nm, box oxide thickness of 200 nm and a substrate thickness of 100 nm. The poly-silicon control gates are 40 nm wide and the spacing between them is 50 nm. The coupling distance between the SETD device and the DSET is 160 nm. The natural oxide layer surrounding the Si-NWs is 30 nm thick, and the whole structure is covered with an upper oxide interlayer of 130 nm thickness and a 50 nm thick metal top gate. The simulator calculates the distribution of potentials and electrostatic fields through the structure [10]. To obtain a certain capacitance value, for example the substrate capacitance of the electrometer's island, all the external boundaries of the structure are grounded and a potential of 1 V is applied to the substrate top surface (the interface between the substrate and the buried oxide), as shown below:

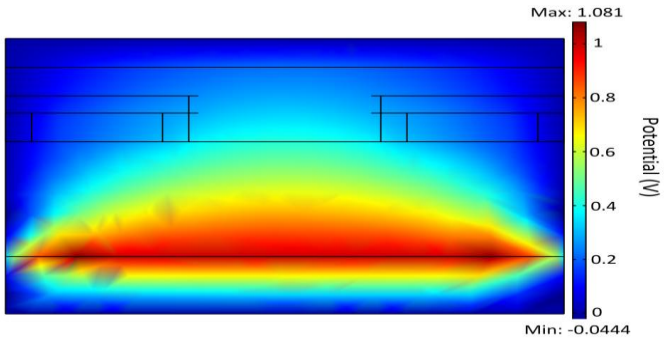


Fig. 5.5: Potential distributions across the SETD with a potential of 1 V applied to the substrate.

To extract the electrometer island substrate capacitance, the electrometer island boundaries must be specified so that COMSOL can integrates the electric field displacement over the electrometer's island; this gives the total surface induced charge of the island. Since the potential applied to the substrate was 1 V, the required capacitance value is obtained from [10]:

$$C = \frac{Q}{V} \tag{5.1}$$

Where C is the capacitance, V is the voltage applied to the substrate and Q is the charge.

All the relevant capacitance values of the SETD and the DSET structure of Fig. 5.3 are extracted. The capacitance values of the structure are listed in table 5.1 and 5.2 below:

Table 5.1: Extracted substrate, upper gate and gate capacitance values of the SETD with the DSET electrometer.

Component	Substrate Capacitance	Upper gate Capacitance	Gate Capacitance
QD1	2 aF	2.1 aF	-
QD2	7.3 aF	1.21 aF	-
QD3	1.6 aF	1.23 aF	-
QD4	1.15 aF	6.42 aF	-
G1	6.34 aF	1.33 aF	3.52 aF
G2	1.04 aF	8.74 aF	4 aF
G3	1.7 aF	1.45 aF	2.25 aF
G4	4.18 aF	3.8 aF	2.06 aF
G5	3.97 aF	3.54 aF	3.54 aF
G6	5.23 aF	4.64 aF	2.92 aF

Table 5.2: Extracted coupling capacitance values between the four quantum dots of the SETD and the DSET structure.

Quantum dots coupling	Coupling Capacitance
QD1 – QD3	1.22 aF
QD1 – QD4	5.66 aF
QD2 – QD3	8.47 aF
QD2 – QD4	6.57 aF

5.4 Monte Carlo single electron circuit simulation

Monte Carlo simulation techniques are one of the most important methods used for the simulation of single electron devices. The Monte Carlo method lists all the possible tunnelling events, determines their probabilities, and by employing these probabilities for weighting; the Monte Carlo technique selects one of these tunnelling events randomly, and this process is repeated for a number of times. The phenomenon of electron tunnelling through tunnel junctions is a stochastic process in nature, and these tunnelling events are independent of each other and exponentially distributed [13].

CAMSET is a Monte Carlo based single electron circuit simulator developed by Hitachi Cambridge Laboratory [91]. It is used for the single electron circuit analysis in this project, where the capacitance matrices of the substrate, gate and coupling of the quantum dots extracted from the 3D FEM simulations are fed into this simulator. CAMSET is used here to simulate the equivalent circuit of the SETD device (shown below) to demonstrate single electron transfer operations. For simplicity purposes, in the single electron simulations, the MOSFETs (fig. 5.6) are represented by single electron transistors.

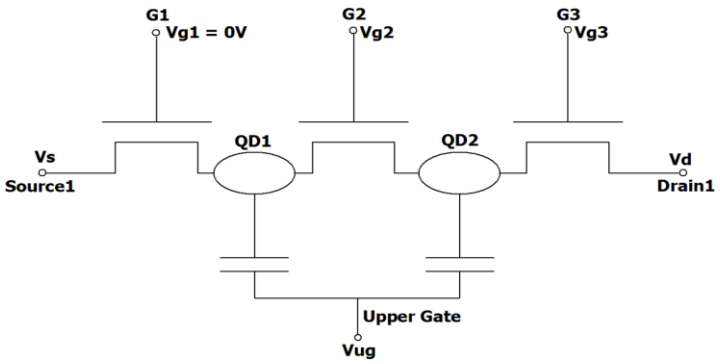


Fig. 5.6: Equivalent circuit of the SETD device, the FET gates here act as single electron barriers.

The single electron simulation approach is based on characterizing each circuit component (each SET) on its own and determining the transfer characteristics of each SET separately. After successful simulation of each SET, these SETs (equivalent to the control gates G1-G3) are combined together to form the single spin transfer device shown in Fig. 5.6. Therefore, we start the simulation process with one SET (equivalent to MOSFET control gate G1) with a floating memory node as shown in Fig. 5.7 below. All the single electron simulations were performed at T = 4.2 K to ensure that the charging energy is much larger than the electrons thermal excitation energy according to (2.9).

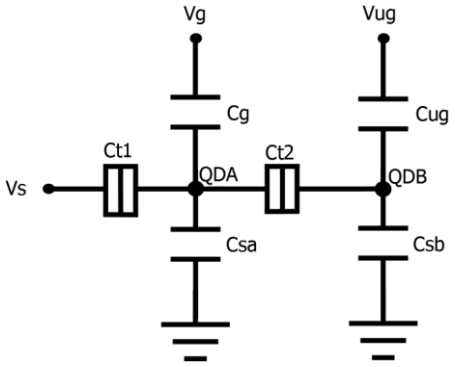


Fig. 5.7: Equivalent circuit of gate G1 with a memory node.

The simulation approach adopted here is based on an operating scheme demonstrated by Mizuta et. al.[92], to inject electrons into a quantum dot for memory applications. The structure featured in that work is a lateral single electron memory cell (L-SEM) and it is in many ways similar to the SET with the memory node structure of fig. 5.7, the L-SEM structure is comprised of an in-plane multiple tunnel junction (MTJ) integrated to the gate of a MOSFET, with the MOSFET channel serving as the target memory node. There are also trimming side gate electrodes on the two sides of the MTJ, a schematic of the structure is shown in fig. 5.9 below. The memory write operation of this structure is achieved by electrons tunnelling through the MTJ from the word electrode to the memory node (MOSFET channel) [92].

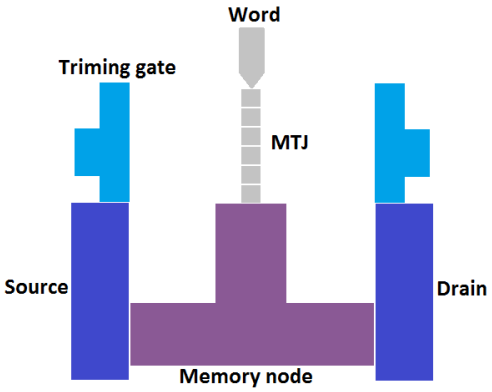


Fig. 5.8: Schematic of a lateral single electron memory (L-SEM) developed by Mizuta et al [92].

The similarities between our SET with a memory node and the L-SEM structure are very clear now: the source electrode for the SET acts as the L-SEM word electrode, there is only two tunnel junctions in the SET compared to the MTJs of the L-SEM , the SET gate and substrate electrodes act as the L-SEM side trimming gates, the memory node of the SET represents the L-SEM MOSFET channel memory node, and finally the top gate and the substrate gate of the SET memory node act as the L-SEM source and drain electrodes. Detailed operation of the memory write operation and the voltage scheme used can be found in [92], the same operating voltage scheme used for injecting tens of electrons will be adopted here and optimized for single electron transfer. The first SET of the SETD device of fig. 5.6 will be operated with the same scheme used for the memory cell write operation (applying a fixed upper gate voltage and pulsing the source potential). On the other hand, the last two SETs of the SETD will be operated as switches in a pure turnstile manner, where by turning the second SET ON, an electron transfers from QD1 to QD2, and turning the last SET ON transfers the electron from QD2 to drain1.

This scheme combines an electron injecting sequence for the first SET [92], with pure turnstile operation sequence for the last two SETs [16], [17]. To optimize the memory write operating voltage scheme for single electron transfer; the simulations were initially carried using the tunnel capacitance and resistance values of 0.371 aF and 5 MΩ respectively provided in [92]. Using the capacitance values obtained from the 3D FEM simulations, Another SET is added in series to the SET of fig. 5.6, and the single electron transfer operations were successfully simulated for the two series connected SETs. Finally, after successful testing of the transfer operation across two SETs; the final SET was added to form the three SET series connected SETD device of fig. 5.6.

The simulation procedure for the three FET SETD is as follows: Initially, the *I-V* characteristics of each transistor shown in Fig. 5.6 were simulated to determine the Coulomb Blockade (CB) gap. After that, a voltage sequence for single electron transfer was developed as shown in Fig. 5.10. A positive voltage of 0.2 V is applied to the top gate (Fig. 5.10a), followed by a negative potential of -54 mV applied to the source (Fig. 5.10b). This negative voltage shifts the operating point of the first SET to outside the CB region, and causes the transfer of one electron across the SET from the source (source1) to quantum dot 1 (QD1). Since the operating point of the SET cannot remain outside the CB region, it shifts back and remains inside the CB region [92].

Turning the upper gate and the source voltages to zero, the transferred electron is confined to QD1. A potential of 275 mV is then applied to V_{g2} (Fig. 5.10c) to turn the second SET ON and transfer the electron form QD1 to quantum dot 2 (QD2). V_{g2} is then switched back to zero confining the electron to QD2. With both SETs turned off, the electron is stored in QD2. The electron remains in QDB until we raise the potential of V_{g3} (Fig. 5.10d) to 275 mV, this allows the electron to transfer across the last SET from QD2 to the drain (drain1). Finally V_{g3} is switched to zero, and with all the SETs turned off,

the electron is stored at the drain (drain1). The results (Fig. 5.9 (e-f)) clearly show that single electron transfer operations have been achieved using the pulse sequence shown in Fig. 5.9 (a-d).

The time required for a single electron to be transferred from source1 to QD2 was estimated to be 1.85 μs from the simulation result of Fig. 5.9. The turnstile device of Fig. 5.6 used tunnel resistance and capacitance values of 5 MΩ and 0.371 aF, respectively. These values determine the time scale (1.85 μs) of the single electron circuit simulation. This time scale can be improved by optimizing the tunnel resistance and capacitance values of the structure.

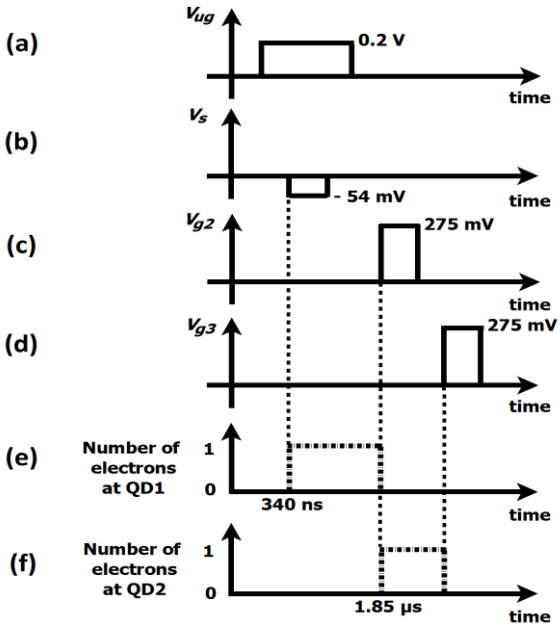


Fig. 5.9: Single electron transfer operation through the SETD, showing the voltage pulse sequence used and the number of electrons at QD1 and QD2.

Here, we discuss the controllability of the number of electrons to be transferred in the device. To transfer the desired number of electrons across the SETD, the voltage scheme of Fig. 5.9 relies on choosing appropriate values for the upper gate and the source voltages. The upper gate voltage defines the operating point of the SET within the CB region, while the source voltage pulse determines the shift of the SET operating point outside the CB region. We fixed the pulse height of the upper gate voltage at 0.2 V and changed the pulse height of the source voltage. Fig. 5.10 below proves that changing the pulse height of the source voltage directly affects the number of electrons transferred to QD1.

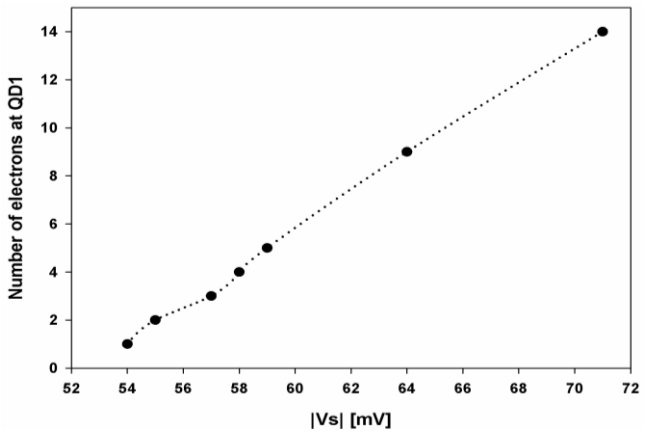


Fig. 5.10: Effect of varying *Vs* on the number of electrons transferred from source1 to QD1.

5.5 Fabrication of the single electron transfer device and electrometer

So far in our discussion, the single electron turnstile and the electrometer FinSET control gates are intended to be realized using Polysilicon gates. However, Poly-Si as a gate material had to be abandoned due to delays in commissioning the Poly-Si PECVD facilities (in particular the temperature table for any PECVD deposition above 400 C) at the Southampton nanofabrication center for almost 2 years since the start of this project, even doped amorphous Si capabilities were not available for a long period of time (delayed commissioning of phosphine gas) excluding the option of depositing amorphous silicon and then crystallizing it at a higher temperature.

On the other hand, Poly-Si control gates depending on their grain structure, grain boundaries and grain size, can potentially introduce random telegraph signal (RTS) noise when operating in the single electron regime. In addition, the formation of accidental quantum dots in the control gates themselves is also a possibility; this can be very disadvantageous for our device application. It has been reported that QDs and the tunnel barriers can be inherently formed by the crystalline grains and the grain boundaries of Polycrystalline silicon, and the formation of these QDs is directly dependent on the grains size and the gains density of the deposited Poly-Si layers [12], [93]. Nevertheless, Poly-Si is in fact the most common gate material in single electron devices for memory application and quantum coherence experiments as demonstrated by various research groups..

Aluminum is a good candidate to replace Poly-Si as the control gates material, it would be electrically suitable for the device performance, has proven beneficial in the CMOS technology due to the absence of any gate depletion, and it can be patterned using e-beam lithography and lift off. In addition, Al gates can possibly provide a more uniform gate operation across fabricated devices on the chip where Poly-Si gates may suffer from local variations in the potential profile of each fabricated

gate. Al as a gate material for SOI nanowires is a novel process, which might require special techniques to insure gate coverage and continuity, and is chosen here to realize FinSET gates for the SISSQIT devices. Below are the proposed fabrication process steps for Al FinSET QD devices.

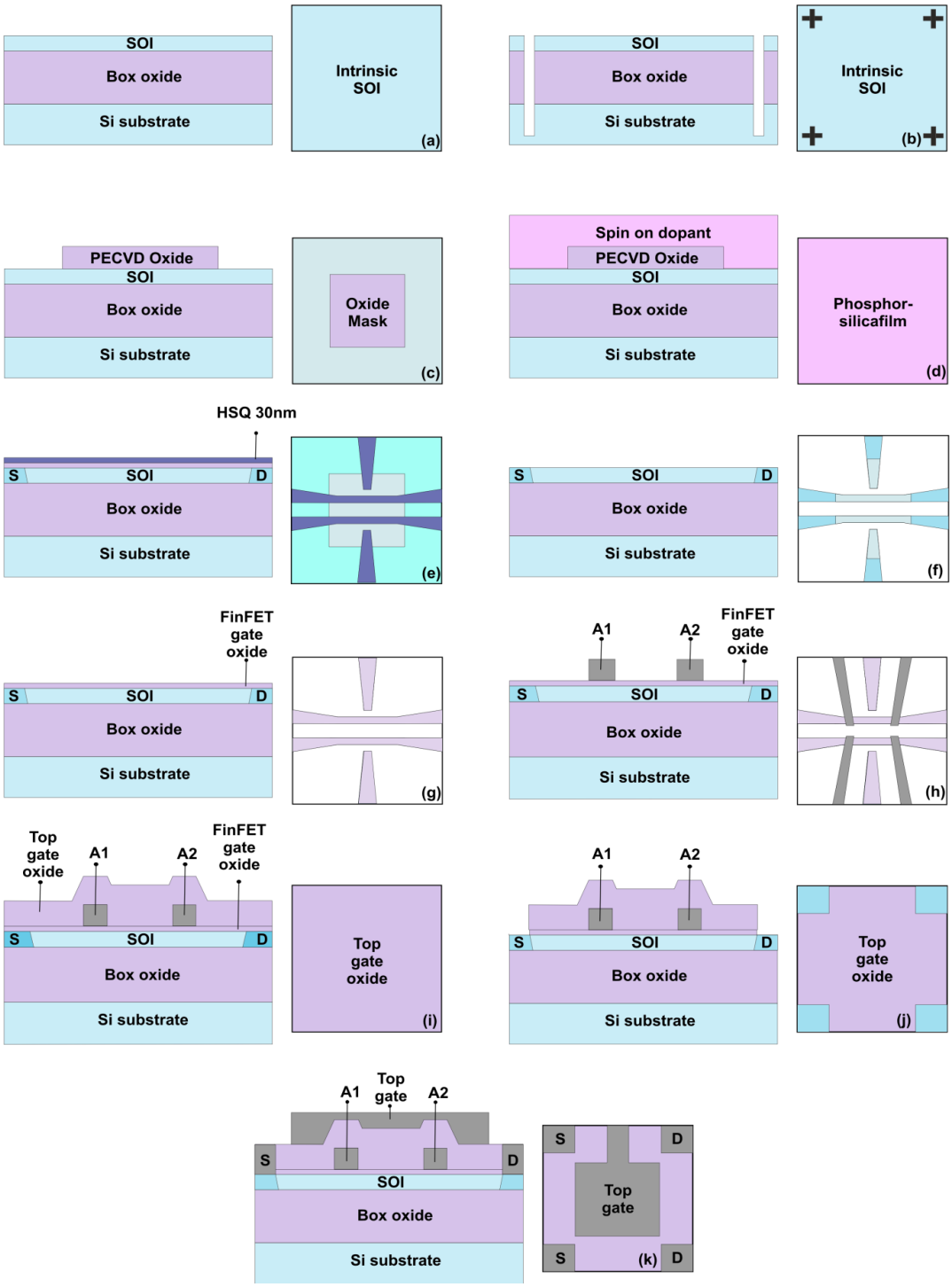


Fig. 5.11: Fabrication flow for the Al FinSET single QD platform. (a) SOI thinning, (b) alignment marks definition, (c) and (d) selective doping using Phosphorosilica film, (e) and (f) Si layer definition with e-beam and RIE, (g) gate oxide growth, (h) Al device layer definition with e-beam and lift off, (i) top gate oxide deposition, (j) contact via layer formation with e-beam and HF etching, (k) top gate and contacts layer definition with e-beam and lift off.

5.5.1 Thermal oxidation and SOI thinning

Thermal oxidation

Thermal oxidation is a process where a Si surface is exposed to an oxidizing environment at an elevated temperature, when the oxidizing ambient includes steam water vapour the oxidation process is known as wet oxidation and if the process uses only pure O2 then the process is known as dry oxidation, these two processes can be expressed with the following [94], [95], [96]:

$Si\ (solid) + O2\ (vapour) \rightarrow SiO2\ (solid)$ Dry oxidation

$Si\ (solid) + H2O\ (vapour) \rightarrow SiO2\ (solid) + 2H2\ (gas)$ Wet oxidation

A tenacious silicon oxide (SiO2) layer is formed as a result of the thermal oxidation process; thermal oxide layers are very stable to temperature above the melting temperature of Si (around 1420C). Therefore, SiO2 has played an essential role in the electronics industry, it has been used extensively as a masking layer for ion implantation and diffusion, tunnelling dielectric, passivation layer, field oxide and gate oxide for MOS devices [94].

Oxidation work for this project has been carried out using Tempress horizontal ambient oxidation furnaces at the Southampton nanofabrication centre (SNC). Experimental work started by running multiple oxidation runs on test Si 6 inch wafers (wafer were then recycled after HF removal of the thermal oxide), for the purpose of creating experimental oxide thickness vs. time plots for both wet and dry oxide. Such oxidation plots are essential for SOI thinning and to precisely control the gate oxide formation, two of the essential processes for the success of this work.

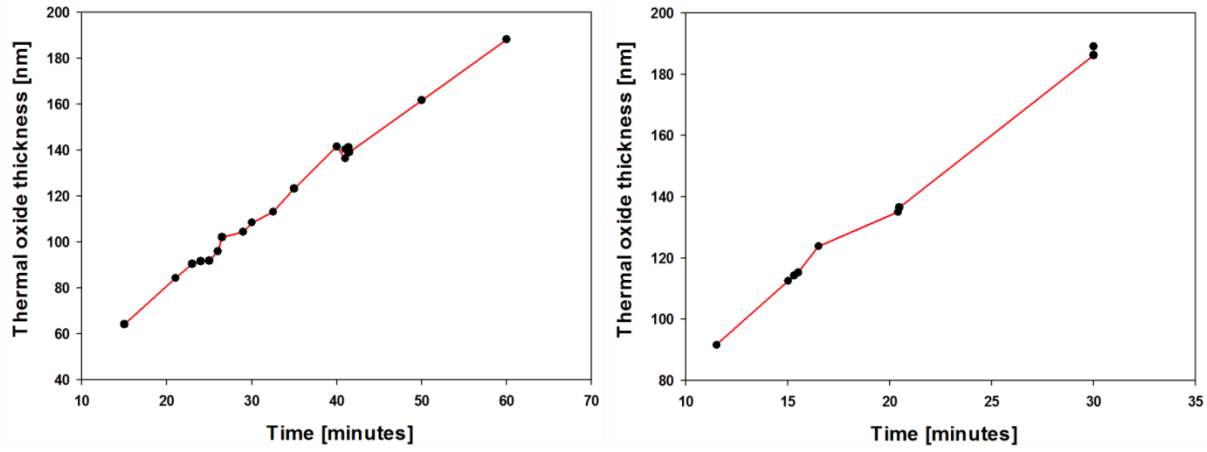


Fig. 5.12: Wet thermal oxide vs. Time at 950C (left) and 1000C (right) for Si using the Tempress wet oxidation furnace at the Southampton nanofabrication centre with 3slm (standard litter per minute) H2O steam.

950C is chosen (over 1000C) for SOI thinning because it is at a high enough temperature to give good quality oxide and at the same time it has a slower more controllable growth rate compared to 1000C. For comparison purposes, oxidation tests were also performed at 1000C as shown in the right side graph of fig. 5.12. By fitting theses experimental results to a polynomial model, wet oxidation equations for the SNC's Tempress furnace at 950C and 1000C can be produced below.

For wet oxidation at 950C (t is the oxidation time in seconds):

$$\text{Oxide thickness} = 0.06878t - 5.0024\times10^{-6}t^2 \tag{5.5}$$

For wet oxidation at 1000C (t is the oxidation time in seconds):

$$\text{Oxide thickness} = 0.14118t - 2.09742\times10^{-5}t^2 \tag{5.6}$$

Due to the fast growth provided by wet oxidation, the use of this process in our project was specific to SOI thinning. On the other hand, the device gate oxide requires very thin oxide layers with high quality; therefore dry oxidation is used exclusively for this process. As described earlier, dry oxidation provides higher quality oxides compared to wet oxidation and it also has a much slower growth rate, allowing the realization of very thin oxide layers (below 10nm). Dry oxidation experiments using the SNC's dry oxidation furnace are shown in the figure below:

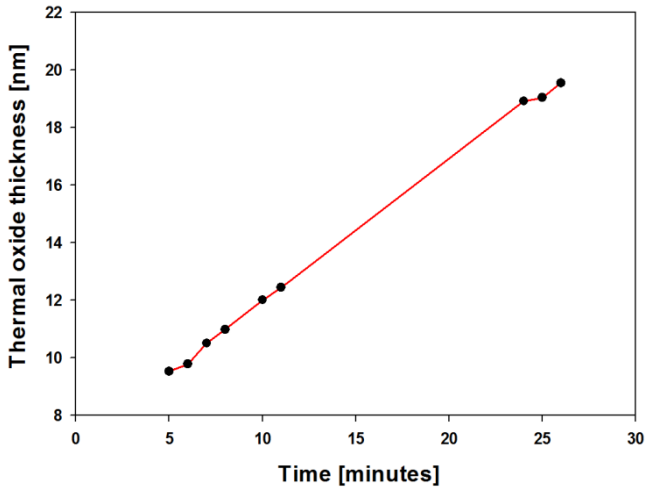


Fig. 5.13: Dry thermal oxide vs. Time at 950C for Si using the Tempress dry oxidation furnace at the Southampton nanofabrication centre with 5 slm O2 gas flow.

SOI thinning process

The Si device layer thickness for devices introduced in this project is between 30 nm to 50 nm, these dimensions are designed to provide sufficient QD confinement during device operation, and also to meet some fabrication process requirements (for example, the FinSET device structure requires the thickness of the SOI device layer to be less than the thickness of evaporated Al for the second layer). Therefore, commercially available 100 nm intrinsic silicon-on-insulator wafers (from Soitech) with a 200 nm thick buried oxide layer are thinned down to below 50nm. To accomplish this, wet oxidation is used to consume the Si layer by growing wet thermal oxide, after that buffered HF is used to remove the thermal oxide layer leaving an SOI wafer with the required Si device layer thickness, the thermal oxide thickness and the Si device layer thickness before and after the oxidation process are characterized using the SNC's Woollam M-2000 ellipsometer.

The wet oxidation process used for SOI thinning is fully optimized to provide: the best possible uniformity profile across the wafer, precious control of the thermally grown oxide thickness (and consequently the SOI device layer thickness), reproducible results across runs, and the smallest possible surface roughness. The oxidation process optimization was achieved after an extensive amount of testing and characterization, it included optimizing the heating profile (using a two heating stages, the initial heating stage has a fast temperature ramp followed by a final heating stage with a slow temperature ramp to the target oxidation temperature), process gas flows, process partial pressure, boat insertion speed and N2 gas flow during boat insertion.

As an example, one of the SOI thinning processes is as follows:

- To reduce the thickness of an SOI wafer from 100nm to 50nm.
- Thermal oxide needed = 50nm/0.44 = 114nm.
- From the 950C wet oxidation experimental results shown in fig. 5.13, an oxidation time of 33 minutes is required to from 114nm oxide.
- The oxidation process resulted in an average of 114nm oxide across the wafer as shown by the ellipsometry profile of fig. 5.16 (a) below; fig. 5.16 (b) shows the resulting 50nm SOI profile after BHF removal of the 114 nm thermal oxide.
- The ellipsometry results for the 950C wet oxidation shown in fig. 5.16 (a) had a measurement mean squared error (MSE) value 4.23, measured 133 points on the wafer, maximum oxide thickness on the wafer is 116.4nm, and the minimum value is 112.11nm , oxide thickness range across the wafer is 4.3nm, and the standard deviation of this measurement is 1.62

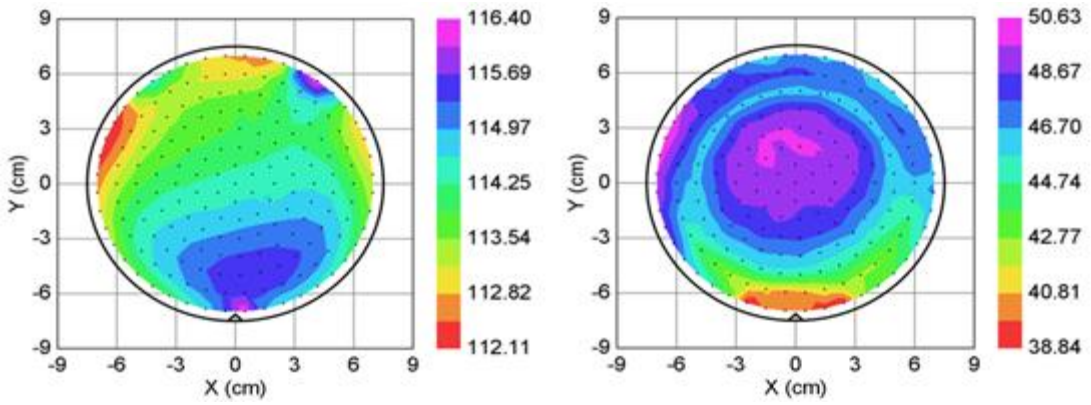


Fig. 5.14: Left: Oxide thickness vs. position on wafer ellipsometer profile of a thermally oxidized SOI wafer, right: SOI thickness vs. position on wafer profile of a thinned SOI wafer.

5.5.2 Sample Layout

Before discussing the deep etched alignment marks process development, we will start by describing the alignment marks used and the sample layout. The sample size used in this project is 3.5cmx3.5cm, the sample contains 144 devices divided into two 1cmx1cm size chips, each chip has 9 device columns by 8 device rows. The 3.5cmx3.5cm sample has three types of alignment marks:

- 24 optical alignment marks that are 800umx800um, with a mark width of 40um.
- 6 E-beam global alignment marks that are 1mmx1mm, with a mark width of 1um (P1/Q1), 500nm (P2/Q2), and 2um (P3/Q3).
- 180 E-beam local alignment marks (four local alignment marks for each device) that are 100umx100um, with a mark width of 300nm.

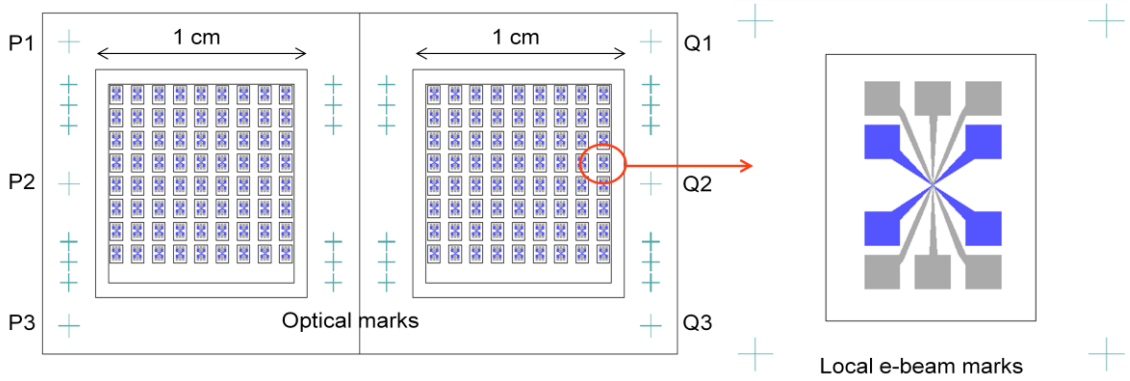


Fig. 5.15: Sample layout for the devices presented in this report, showing devices and alignment marks arrangement.

The 3.5 cm x 3.5 cm sample layout also includes a number of accessory devices that are fabricated at the same time as the devices; these accessories are located at the base of each 1 cm x 1 cm chip. The accessory cells include vernier scales, AFM lines, isolation pads, van der pauw structures, gated van der Pauw structures, TLM structures, dummy Si nanowire device, intrinsic and doped nanowire arrays. After device fabrication, these structures are used to check lithography alignment, dry etch conditions, electrical isolation, oxide capacitance determination, Si channel resistance measurements, resistivity measurements, mobility and carrier concentration measurements. A schematic image of some of the layout accessory structures is shown below.

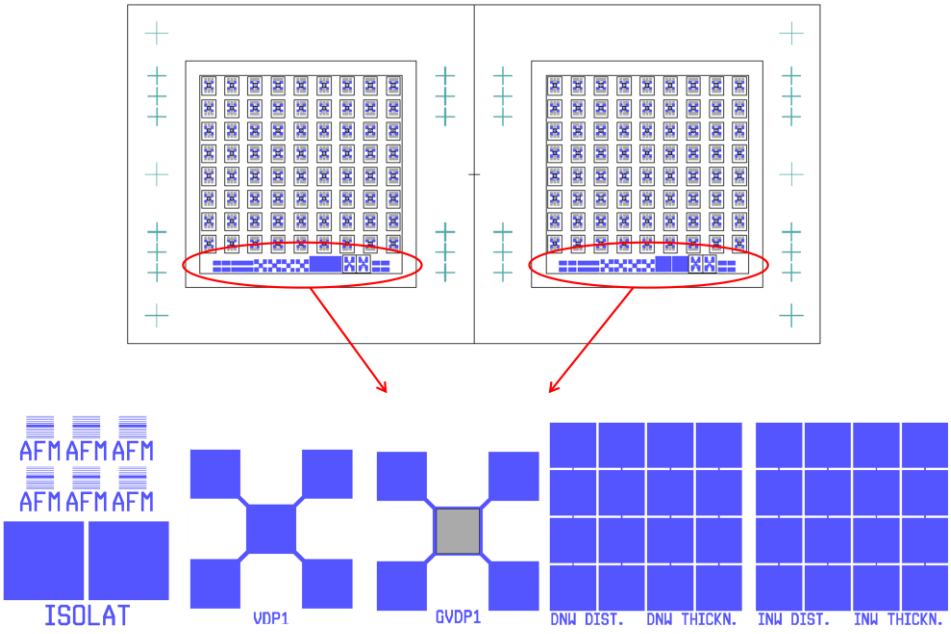


Fig. 5.16: A schematic showing some of the accessory cells, other structure that are not shown here include vernier scales, TLM structures and dummy Si nanowire devices.

5.5.3 Electron beam lithography

Photolithography techniques are limited by wavelength of the light source used for exposure; this limits typical photolithography process resolution to about 1 µm. On the other hand, electron beam lithography (EBL) provides nanofeature resolution due to the small wavelength and small spot size (down to few nanometres) used in this lithography technique, electron beam lithography is currently the main tool for nanostructures fabrication. Most e-beam exposure systems use high energy electrons to provide very high resolution (SNC's JEOL system uses a 100 keV source for most exposures). However, using high energy electrons for e-beam exposures mean that the electrons have a high penetration depth, and this leads to electrons backscattering at the sample substrate causing exposures at areas in proximity of the required pattern, this is known as proximity effect in EBL. This

effect can be corrected for by using proximity effect correction software that fractures the intended exposure pattern to a set of exposure doses and assigns different dose levels to specific areas of the exposure pattern, effectively reducing the proximity effect. Since electron scattering occurs in the resist layer and the substrate, another method of reducing the volume of electron scattering while maintaining high resolution is by using very thin resist layers [97].

Electron beam lithography works by irradiating the sample with electrons causing chemical changes in the exposed resist area, these chemical changes effect the solubility of the exposed area compared to the un-exposed resist area in the developing solution. The amount of electron irradiation is referred to as exposure electron dose [uC cm^{-2}], the exposure dose can be defined as the number of electrons per unit area required to achieve the desired chemical response in the resist material [97]. To realize the spin qubit devices in this project, multiple layers of e-beam lithography are required. The e-beam resists used to make this process possible are: ZEP520A, UVN30, HSQ, PMMA single layer and PMMA bi-layer process.

5.5.4 Alignment marks definition using ZEP520 e-beam lithography

The e-beam alignment marks are patterned using a 100keV e-beam system with beam current of 25 nA and a 200 µm aperture. The alignment marks were realized on a 400 nm thick ZEP520A layer, as a result of spinning the resist at 3370rpm for 2 minutes, resist spinning was followed by a hot plate bake at 180C for 3 minutes. E-beam exposure was carried out using a dose of 450 uC/cm^2. After e-beam exposure, the sample is developed in ZED-N50 (special ZEP520A developer supplied from Zeon Corporation) for 2 minutes, rinsed in IPA and dried.

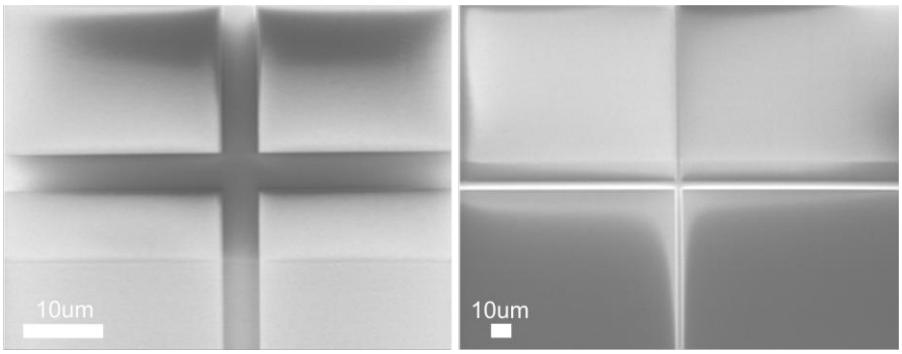


Fig. 5.17: Global e-beam alignment marks patterned on ZEP520A with dose of 450 uC/cm^2.

5.5.5 Alignment marks pattern transfer with reactive ion etching

After patterning the alignment marks using e-beam lithography on 400 nm ZEP520A, we are left with 400 nm trenches in the resist pattern as shown in fig 5.21 below.

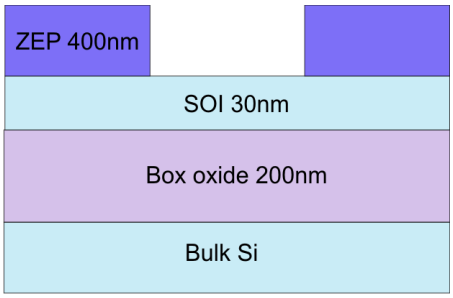


Fig. 5.18: Schematic showing the alignment marks profile before dry etching.

To transfer the alignment pattern to the underlying SOI, dry etching must be employed. These etched marks will be used for global and local e-beam alignment; this means that the marks must be as deep as possible with good vertical side walls, improperly etched alignment marks can lead to significant e-beam misalignment or even failure in writing the patterns. Therefore, the alignment marks dry etch process requires the highest possible Si and SiO2 etch selectivity against ZEP520A resist, in addition the Si etch profile must be anisotropic. The target alignment marks etch depth is 700nm and dry etching process is divided into three stages:

- The first stage is to etch the 30 nm top Si layer, the sample is then characterised using ellipsometry and profiler.
- Stage two involves etching the 200 nm thick buried oxide layer, after that the sample is characterized again using ellipsometry and profiler.
- Finally in the last stage as much Si as possible is etched from the bulk Si while keeping a sufficient thickness of ZEP520A resist on the sample surface to protect the Si device layer. Further characterization is also preformed after that.

The SiO2 dry etch process is based on CHF3/Ar gas chemistry using Oxford instrument RIE 80+ system, this process is used to etch the 200 nm buried oxide of our SOI stack. Since the target etch depth for the alignment marks is 700 nm, anisotropy of the 200 nm buried oxide can be scarified to achieve the highest possible selectivity with ZEP520A. However anisotropy of the Si etch has be sufficiently anisotropic to make the e-beam alignment process possible. The SiO2 etch process started using a CHF3:Ar ratio of 1:3, 100 W RF power, pressure level of 30 mTorr and at a platen temperature of 20 C. Etching using this recipe produced a SiO2:ZEP520A etch selectivity of 2:1, and needed improvement on the etch selectivity. To maximize the SiO2:ZEP520A selectivity, this process is carried with CHF3 without any Ar flow at a reduced RF power of 50 W while the platen

temperature and pressure left at the standard RIE machine levels. This dramatically improved the selectivity, with a high SiO2:ZEP520A selectivity level of 6:1 achieved. However, this is also accompanied by slow SiO2 etch rate of 9 nm/min.

Therefore, to etch all of the 200 nm buried oxide, an etch step of 20 minutes or more is needed. Due to the low RF power used (50 W), the DC bias levels across the top and bottom electrodes of the machine was dropping dramatically from 130 V at the start of the etch process to almost 20 V after 5 minutes, this means that SiO2 etching would effectively stop in about quarter of the time required to etch the whole 200 nm buried oxide layer, using four etch steps by stopping and restarting the etch process every 5 minutes can overcome this problem but this solution is time consuming. The main reason for the DC bias drop is the quartz bottom electrode that becomes more and more insulating at low RF power levels, and this causes the DC bias to continuously decrease with time. Therefore, we need to maintain the DC bias levels between the top and bottom electrodes without increasing the RF power, without introducing Ar into the etch process, and while keeping the etch process time as low as possible. In addition to the quartz base plate, the Oxford instruments RIE 80+ system also has a graphite plate that can be fitted to the machine when needed, offering a much higher conductivity than the quartz base plate. Using the graphite plate base plate instead of the quartz plate as the RIE bottom electrode maintained the DC bias levels through the 20 minutes etch process (time required to etch the 200nm buried oxide) and successfully etched all of the buried oxide layer in one etch process. Below is a plot showing the graphite and quartz plate DC bias response with time during the etch process.

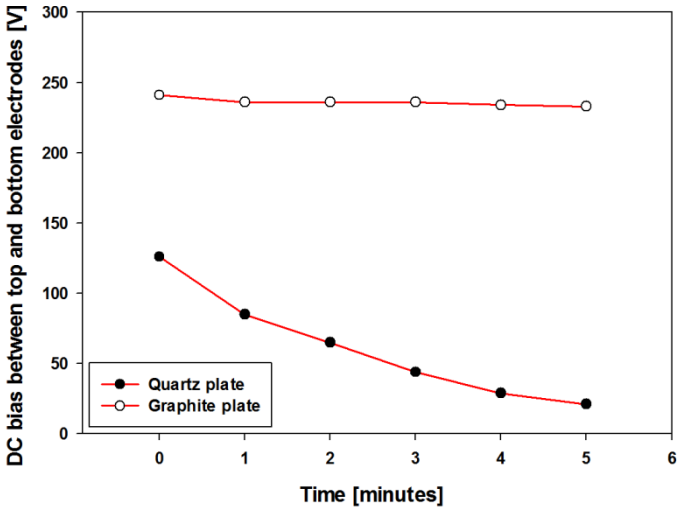


Fig. 5.19: DC bias between top and bottom electrodes of the RIE 80+ vs. time during the SiO2 etch recipe (minute zero refers to the start of the etching process).

In summary, a novel low power (50 W) SiO2 etch process using a graphite base plate with pure CHF3 chemistry has been developed. This process offers extremely high SiO2:ZEP520A etch selectivity

(6:1), and it successfully removes the entire 200 nm buried oxide layer in a single step reasonable 20 minutes dry etch process time.

The Si dry etch process is based on SF6/O2 gas chemistry using Oxford instruments RIE 80+ system, this process is for etching the top Si device layer and the bulk Si. The Si dry etch experiments started using an SF6:O2 ratio of 5:1 with pressure of 30 mTorr, RF power of 50 W at a platen temperature of 20 C. The platen temperature and pressure are standard level for the RIE machine; however the low RF power and low oxygen gas level was chosen to provide the highest possible selectivity between Si and ZEP520A. This process produced a Si etch rate of 170 nm/min with a Si:ZEP520A selectivity of 1:7. Due to the low RF and O2 gas flow levels used, the side walls were expected to be slightly isotropic, therefore an AFM scan of the alignment marks was preformed as shown below:

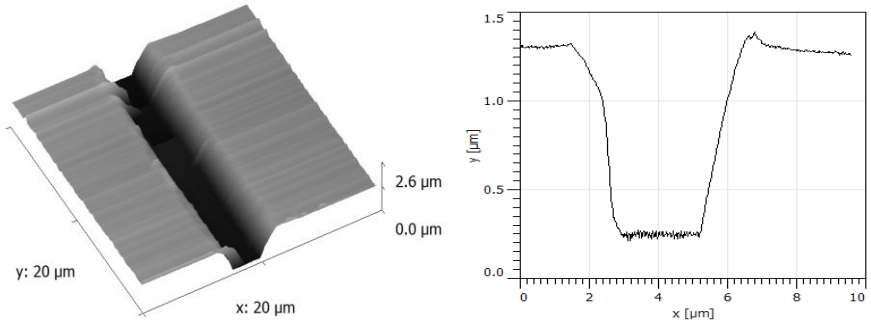


Fig. 5.20: AFM scan of one of the alignment marks bulk Si etch with SF6:O2 5:1 and RF of 50 W.

The AFM results showed an etch depth close to the expected etch depth, however the side walls profile seemed much better than expected (with the low O2 and RF levels) especially that there is a chance that the AFM tip could be too large to properly scan the side walls especially if these side walls are isotropic. The only conclusive methods to determine the Si etch anisotropy, an SEM cross section is preformed and the cross section image is shown below:

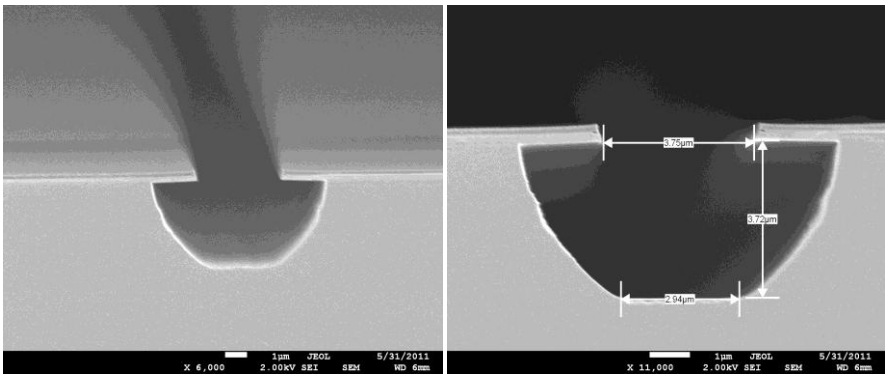
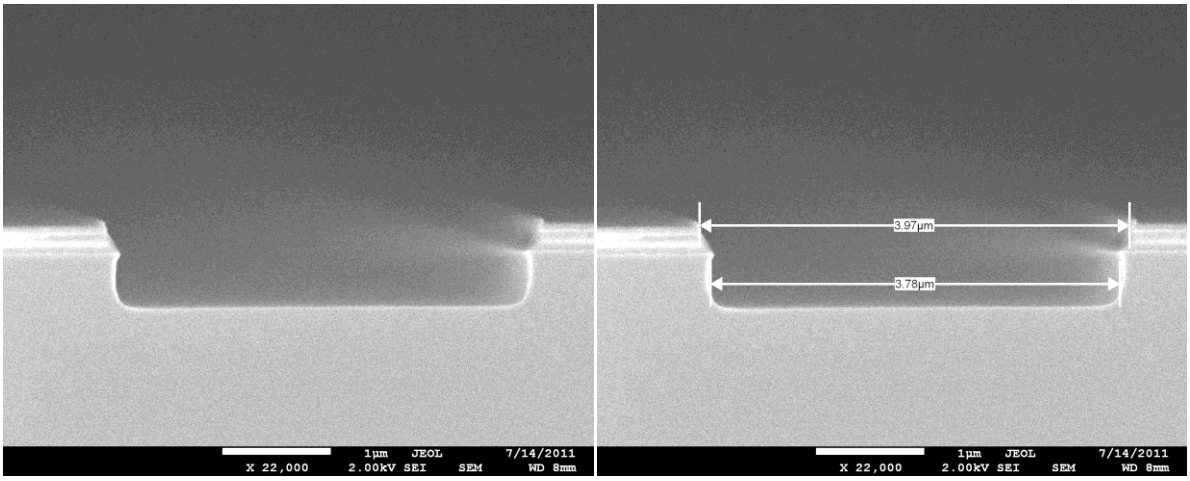


Fig. 5.21: SEM image of one of the alignment marks bulk Si etch with SF6:O2 5:1 and RF of 50W.

This proved conclusively that the AFM scan produced false results and that O2 flow and RF power in the Si etch recipe must be increased to improve the side walls profile, even if this mean we lose the high selectivity and etch rate levels we achieved. Following the anisotropic etch profiles demonstrated in [98], the SF6/O2 ratio is increased to 4:3 and the RF power level is increased to 160 W. These modifications to the Si etch recipe produced vertical side walls, increased the etch rate to 400 nm/minute, but they also reduced the Si:ZEP520A selectively to 1.5:1.

In conclusion, the Si etch stage: an optimized SF6/O2 ratio of 4:3 with a relatively high RF power level (160W) produces very anisotropic side wall profile (an essential requirement for e-beam alignment marks), high etch rate of 400nm/minute and a modest Si:ZEP520A etch selectivity of 1.5:1.

The low selectivity of the Si etch recipe could not be improved without sacrificing the anisotropy level achieved using that recipe, but since the SiO2 etch recipe of this process provides a SiO2:ZEP520A selectivity of 6:1, the 700 nm alignment mark target etch depth can still be achieved even with the low Si:ZEP520A selectivity of the Si etch recipe. The complete etch process (two Si etch steps and one SiO2 etch step) consumed 320 nm ZEP520A and produced alignment marks with an etch depth of 740 nm. SEM images of the deep etched alignment marks (after removing the remaining 80 nm ZEP520A) are shown below.



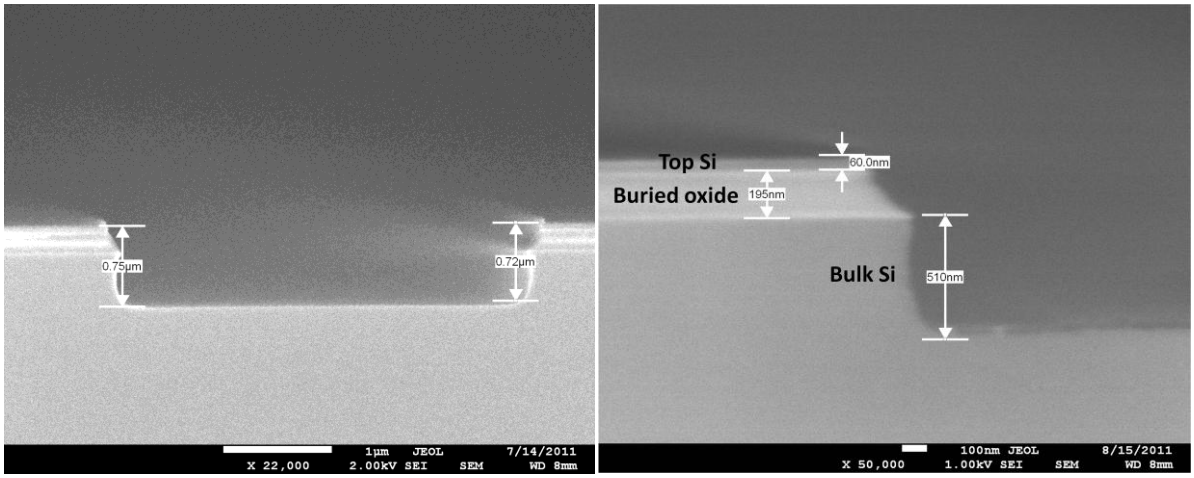


Fig. 5.22: SEM images of a deep etch global e-beam alignment mark.

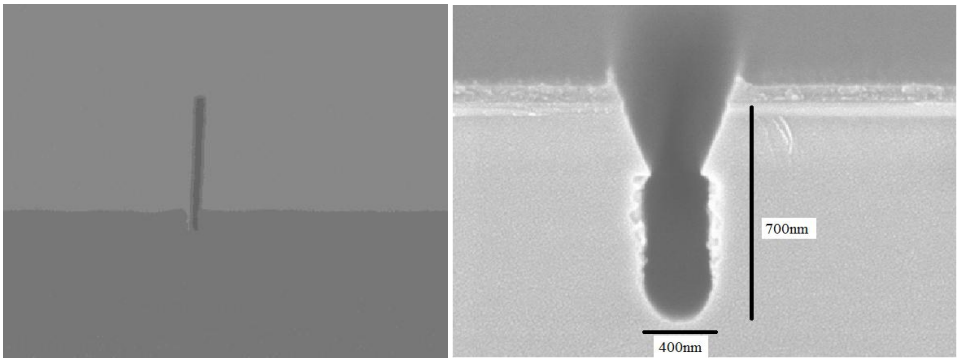


Fig. 5.23: SEM images of a deep etch local e-beam alignment mark.

To this date, this alignment marks dry etch process has produced many samples (more than 60) with excellent reproducibility for the alignment marks definition. Both global and local e-beam marks have been successfully scanned using the e-beam, they show very good contrast, easily detectable by the electron sensor even at low signal to gain ratio. This novel dry etch process realizes very well-defined deep etched e-beam alignment marks (close to 800 nm deep for some samples); enabling excellent e-beam alignment with a misalignment error of less than 10 nm (will be shown shortly).

After this three stage dry etch process, the remaining ZEP520A resist is removed using a plasma asher.

5.5.6 Spin on dopant and Oxide doping mask definition using UVN30 e-beam lithography

The spin on dopant process starts by defining the dopant mask material, the most widely used dopant masking material in the VLSI industry is silicon nitride and silicon dioxide [99]. Due to the relative

ease of deposition, patterning and etching, Silicon dioxide is chosen here as the dopant mask material as it has been commonly used as impurity diffusion barrier material [99].

100 nm thick silicon dioxide is chosen as the dopant layer thickness; this layer is deposited with PECVD at 350 C. The oxide is deposited via a chemical reaction between SiH4 and N2O, at a pressure level of 1000 mTorr with the 20 W RF power, SiO2 deposition rate of 1 nm/second is achieved using this process. To prevent pin holes formation in the deposited PECVD oxide, the 100 nm oxide is deposited in three steps of 35 nm instead of a single 100 nm step. Between each of the 35 nm SiO2 deposition steps the reaction gasses are purged away from the sample surface so that even if pin holes are formed in one 35 nm layer, deposition of the subsequent 35 nm SiO2 layer effectively cover these pin holes.

SiO2 doping mask definition

A 2 µm x 2 µm SiO2 doping mask window is defined by e-beam lithography on 100 nm PECVD silicon dioxide using negative tone UVN30 resist. With the aid of the local alignment marks, the doping oxide mask is placed exactly in the centre of each device area; the 2 µm x 2 µm SiO2 pattern covers the QDs and electrometer region masking them from Phosphorus dopants diffusion.

Initial exposure tests using UVN30 on the SiO2 covered samples were not successful in realizing the 2 µm doping mask patterns. After careful inspection, it was obvious that some of the resist patters are being washed off during the development process, indicating a UVN30 adhesion problem to the SiO2 sample surface. This is due to the Silicon dioxide layer itself as it is a hydrophilic surface (water attracting) by nature, while most resists (including UVN30) are hydrophobic materials (water repelling). This leads to poor adhesion of any resist material spun on silicon dioxide, silicon dioxide layer on a sample can effectively absorb moisture from the atmosphere, and therefore resist adhesion is reduced because no wetting can occur in the hydrophobic resist on top of the hydrophilic SiO2 surface [99].

Dehydration oven bake prior to spinning at 210 C helps to improve resist adhesion by liberating surface water molecules, with spin coating carried out immediately after the dehydration bake. Dehydration bake of 10 minutes is usually sufficient for most substrate types. However dehydration bake alone has not proven to be sufficient to insure good resist adhesion on oxide substrates, therefore a silylating priming agent is used here to modify the oxide surface to improve resist adhesion. HMDS (hexamethyldisilazane) is one of the most widely used alkylsilane resist adhesion promoter. HMDS first reacts with the water on the oxide surface, producing in the process gaseous NH3, oxygen and inert hexamethyldisiloxane compound. This reaction effectively removes OH groups from the sample surface creating a dehydrated surface, after that additional HMDS reacts with the gaseous oxygen produced by the initial reaction to form trimethylsily ($Si[CH3]_3$) oxide species that are chemically

bound to the sample surface, this reaction continues until all of the sample surface is covered with these species. The result of these two HMDS reactions is a hydrophobic sample surface with a surface energy comparable to the resist surface energy, leading to excellent resist adhesion to the oxide sample surface [99]. HMDS is usually applied by vapour priming, this is done by exposing a sample in HMDS vapour at elevated temperatures (100C) for a few minutes; usually in a special HMDS vapour priming oven. Unfortunately, we don't have such a system at the Southampton nanofabrication centre; therefore an alternative arrangement is introduced.

A simple set up for HMDS vapour priming at room temperature was used here instead, this arrangement involved using a medium size beaker with a small amount of HMDS covering its base, and then a second smaller beaker was placed upside down inside the HMDS beaker, with the sample placed on top of the small beaker. After placing the sample, the HMDS beaker is covered with Al foil to prevent HMDS vapour from escaping and the sample was left in this setup for 3 minutes. This simple HMDS priming set up has been successfully tested and demonstrated excellent results in improving UVN30 adhesion to the silicon dioxide sample surface. This arrangement is shown schematically in the figure below.

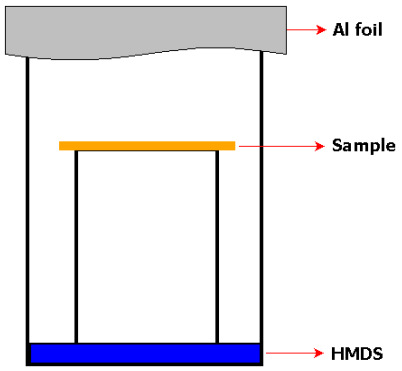


Fig. 5.24: HMDS room temperature vapour priming arrangement.

The process starts by placing the sample in a dehydration oven for 15 minutes, followed by HMDS priming layer coating, UVN30 resist was then spun at 4000 rpm for 60 seconds to give a layer thickness of 390 nm, after spinning the resist was baked at 110 C for 1 minute. The oxide doping mask pattern is exposed with a dose of 100 uC/cm^2 using a 100 keV electron source, current of 25 nA with an aperture size of 100 µm. A post exposure bake at 110 C for 1 minute is preformed, followed by development in MF CD26 for 30 seconds after which the development is stopped with a DI water rinse. The bake conditions and the developer used are based on conditions reported by references that realized similar scale references in UVN30 [100], [101]. The exposure dose and development time was obtained after exposing four test samples containing 2 µm x 2 µm box patterns, each with 10 exposure doses from 100 uC/cm^2 to 300 uC/cm^2, the four samples were then developed at four different development times 30s, 40s, 50s and 60s to determine suitable lithography conditions.

5.5.7 Doping mask pattern transfer with reactive ion etching

A process for silicon dioxide dry etching is required here to define the 100 nm PECVD SiO2 doping mask pattern against 400 nm negative tone UVN30 e-beam resist.

The 100 nm doping mask layer is used as a dopant masking layer. Therefore, the dry etch processes for this layers is quite simple and requires only a good SiO2:UVN30 etch selectivity to realize the SiO2 patterns. The standard SiO2 Oxford Instruments recipe installed on the 80+ RIE machine uses a CHF3:Ar 1:3 gas chemistry with pressure of 30 mTorr, RF power of 100 W at a platen temperature of 20 C [102]. This standard etch process provides an SiO2: UVN30 etch selectivity of 3:1 and an SiO2 etch rate of 25 nm/minute. After the SiO2 doping mask dry etch process, the remaining UVN30 resist is removed using plasma asher.

5.5.8 Phosphorus spin on dopant process

The purpose of the doping process is to create n-type source and drain regions while keeping the device region intrinsic. A commercially available $3x10^{20}$ Phosphorosilica film from Emulsitone (New Jersey, USA) is used here as the n-type phosphorus dopant source.

A suitable spinning recipe for the spin on dopant is developed to insure uniformity across the 3.5 cm x 3.5 cm sample. The Phosphorosilica film is spun at 2500 rpm for 60 seconds, followed by a hot plate bake at 110 C for 2 minutes. The hot plate bake effectively hardens the resist by removing some of its solvent content (the Phosphorosilica film is diluted in ethyl alcohol) providing doping characteristics stability and reproducibility across runs, especially when considering the delay between the spinning process and the activation anneal. The resulting spin on dopant film is a 300 nm thick transparent layer as determined by ellipsometry.

The Phosphorosilica film technical data sheet lists a set of anneal conditions corresponding to the dopant target depth, the smallest dopant depth described is 130 nm junction depth achieved by a 15 minutes N2 ambient anneal at 950 C [103]. Since 50 nm is the maximum SOI thickens used in this project, these conditions are adopted for the anneal process. Before experimentally using these condition, a series of Athena process simulations were preformed to verify the anneal process outcome. Dopant activation anneal simulations were performed using Athena, on the device structure (SOI profile with 50nm Si device layer) with an SiO2 dopant mask of 2 µm width, at an anneal temperature of 950 C and anneal times of 5, 10, 15 and 20 minutes. The spin on dopant Phosphorosilica film was modelled as a 250 nm Silicon layer with $3x10^{20}$ cm^{-3} Phosphorus net

doping, the bulk Silicon and the top Si device layer background doping was also included in the simulation based on the original specifications of SOI wafers used for the device fabrication.

The simulations showed that for all the different anneal times; the undoped Si area underneath the oxide mask was equal to 1.3 µm. This means that regardless of the anneal time; the lateral diffusion of the phosphorus dopants underneath the 2 µm oxide mask is limited to about 0.35 µm from each side of the oxide mask. The simulation also showed that the phosphorus diffusion profile into the box oxide is minimum and the effect of the anneal times used on the vertical diffusion profile is negligible.

As for the net doping concentration in the Si device layer outside the oxide mask, the simulation showed that the net doping increases as the anneal time is increased, for example we have a net Si doping concentration of $6x10^{19}$ cm^{-3} for a 5 minutes anneal and $9x10^{19}$ cm^{-3} for a 15 minutes anneal. From a process simulation point of view, an anneal time of 15 minutes at a temperature of 950C has proven satisfactory. Below are the process simulation results for 15 minutes activation anneal at 950C.

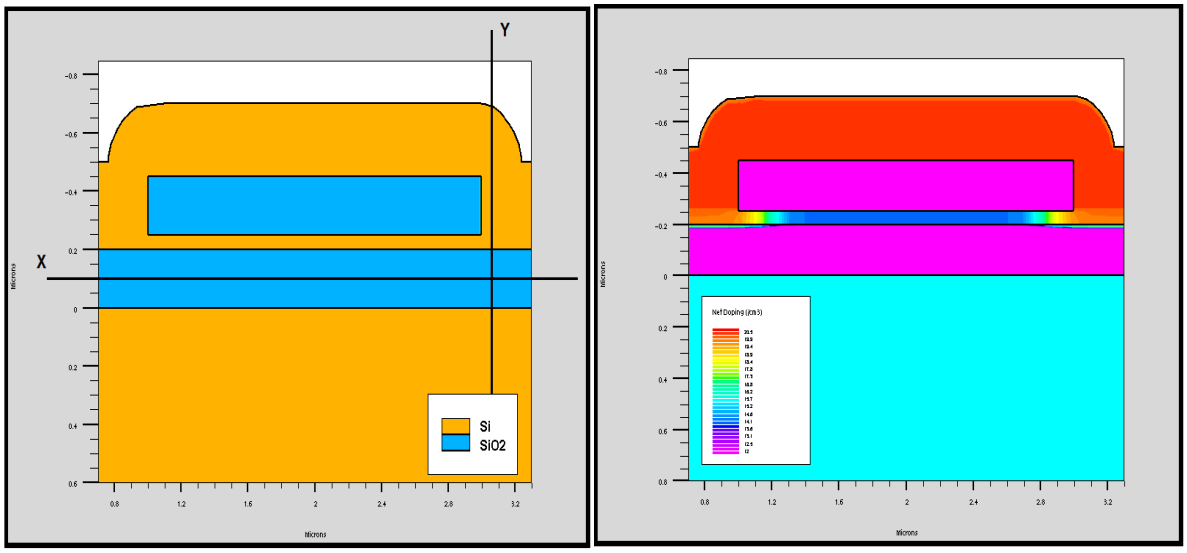


Fig. 5.25: Athena process simulation: Left image shows bulk Si, burried oxide, si deivce layer, oxide doping mask and 250 nm spin on dopant. Right image shows the net doping profile after the anneal process (net doping label not visible, doping levels can be observed in the cross sections below).

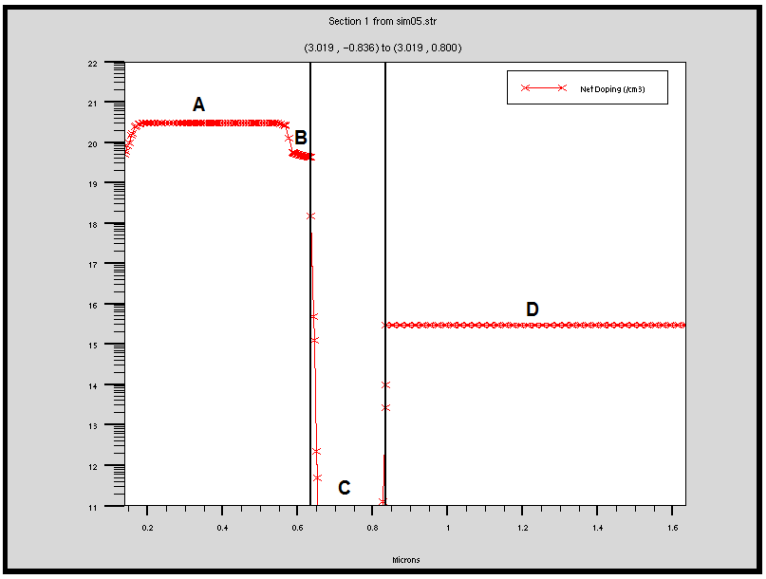


Fig. 5.26: Vertical cutline (Y) of the net doping profile: A is the net doping level of the spin on dopant region, B is the net doping level of the si device layer (region outside the oxide mask), C is the net doping level of the burried oxide region, and D is the net doping level of the bulk Si region.

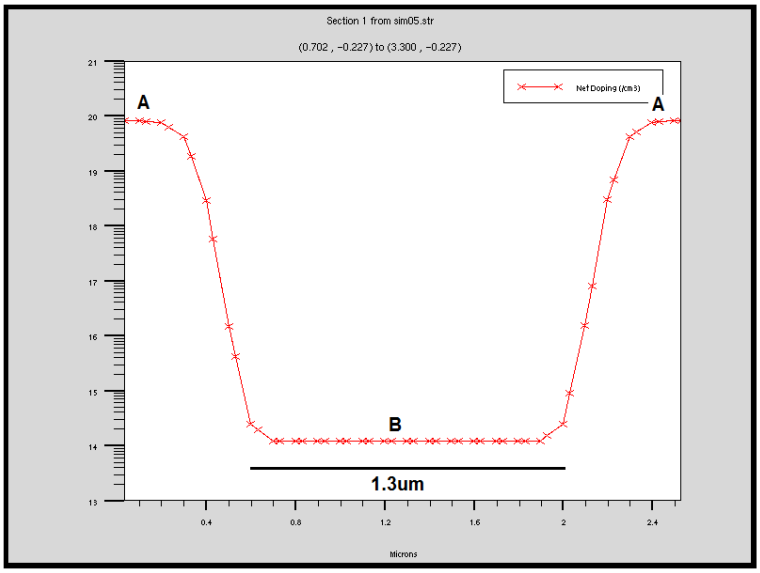


Fig. 5.27: Horizantal cutline (X) of the net doping profile: A is the net doping level of the Si device layer (region outside the oxide doping mask), and B is the net doping level of the Si device layer (1.3 µm region underneath the oxide doping mask).

Therefore, the anneal activation process is carried out at 950C for 15 minutes in a nitrogen ambient. Finally, the Phosphorosilica film data sheet recommends using HF to remove the spin on dopant material [103]. Experimentally, a number of test sample covered with Phosphorosilica film were immersed in buffered HF to determine the Phosphorosilica film removal rate in 20:1 BHF, theses

experiments showed that the Phosphorosilica film is completely removed after a 2minutes, 30 seconds dip in 20:1 buffered HF.

Room temperature hall measurement was performed to verify the doping level produced by this spin on dopant process. The average net doping for a number of samples measured is $2x10^{19}$ cm^{-3}.

5.5.9 Si device layer definition using HSQ e-beam lithography

HSQ is one of the few negative e-beam resist that offers very high resolution and a relatively good etch resistance, therefore it is used here to define the SOI device layer, Initial HSQ test exposures of the first device layer demonstrated that exposing the complete device layout, coarse and fine features, with one exposure conditions can cause merging of the fine device features due to influence of the coarse features high exposure dose, and this effect is known as the exposure proximity error.

The Si device layer patterns are fed into a proximity error correction (PEC) software to optimize the HSQ exposure dose across the pattern area, this software effectively fractures the pattern layout into various exposure areas, so that the fine features receives the high exposure dose they require while the coarse pattern features receive a much lower, but still sufficient, exposure dose. This PEC technique effectively prevents merging of the device's fine features. A PEC software image of the device layout after dose fracturing is shown below.

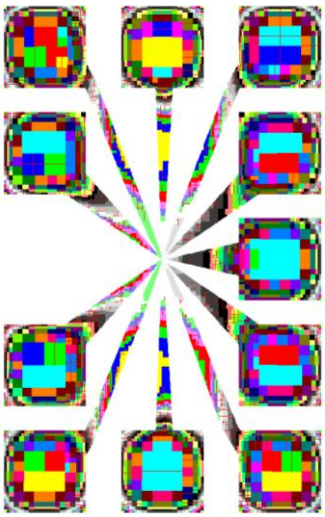


Fig. 5.28: An example of the device layout after PEC simulation. Each colour corresponds to a specific exposure dose; hence the exposure dose is fractured across the layout.

In reference to the figure shown above, the PEC software assigns a low dose level to the centre of the 100 µm x 100 µm contact pads to minimize the effect of exposure proximity. On the other hand, the

fine feature area and most of the pattern line edges receive a much higher exposure dose to provide good feature definition and low edge roughness

Another e-beam writing technique utilized to pattern the Si device layer, is the use of two separate beam conditions, one for the fine device features and the other for the coarse features.

The sub 50 nm fine device features requires a 4 nm e-beam spot size to be properly realized. However, the coarse features that includes the contact pads and the channels running to the fine features device area, have a minimum feature size between 150 nm to 200 nm, therefore these features can be realized with a larger e-beam spot size than the one required for the fine features. Before the development of the deep etched alignment marks, the whole device layout was defined using the 1 nA e-beam required to realize the sub 50 nm fine features. This resulted in long exposure times, and also showed e-beam drift effects at the fine features. The e-beam drift issues arise due to the e-beam writing strategy, the e-beam starts writing at the device corner (at the contact pads) and moves from there towards the centre leaving the fine features region to be last exposed and causes small exposure shifts at the fine features area.

With the deep etched alignment process successfully established, the devices are now exposed using two e-beam conditions. The exposure starts with 1 nA e-beam current to expose the fine device area; after all the fine areas on the sample are exposed, a 25 nA current condition is used to expose the coarse device features. This technique of exposing the fine features first followed by the large device area prevents any e-beam drift at the fine features. And the use of a large 25 nA e-beam current spot size, instead of the fine 1 nA, to expose the coarse device features reduces the device exposure time significantly (144 devices using only fine beam (1 nA) exposure requires 13 hours exposure time, while suing the split beam technique (1 nA and 25 nA) requires only 5 hours exposure time to realize the same 144 devices).

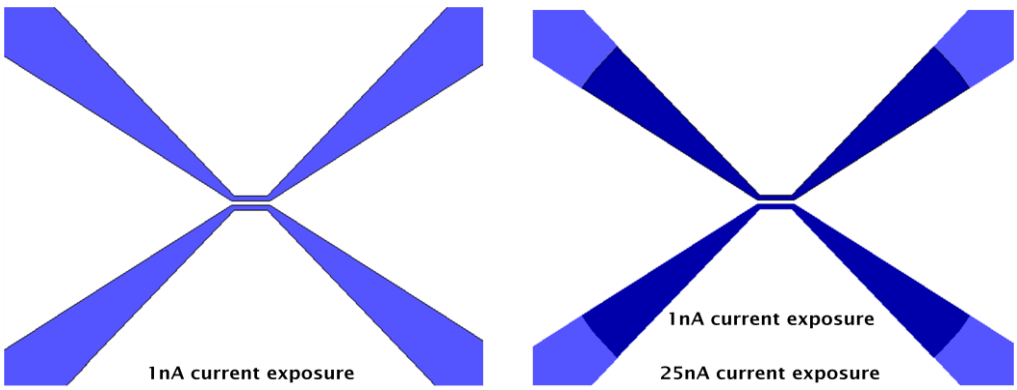


Fig. 5.29: Left: a schematic showing the e-beam exposure used for a device with no alignment marks, right: a schematic showing the device layout split for two e-beam exposures made possible by the deep etched alignment marks.

With the writing strategy of the Si device HSQ layer established using PEC with fine and coarse e-beam exposures, a number of comprehensive HSQ dose tests for the first layer design were preformed with a dose range from 500 uC/cm^2 to 800 uC/cm^2, the results of these dose tests are shown in the SEM images below, exposure is preformed on 60 nm thick HSQ resist layer spun at 5000 rpm for 45 seconds from 4% solid content HSQ (HSQ is commercially available from Dow Corning Corporation).

Development of HSQ is carried out at room temperature using MICROPOSIT MF-319 developer (Tetramethylammonium hydroxide (TMAH) at 2.45% diluted in water) for 1 minute, 40 seconds. As discussed earlier, TMAH is the recommended developer for HSQ; however we observed a much better features definition and edge line roughness for samples developed using MF-319 due to the low concentration of TMAH in this developer.

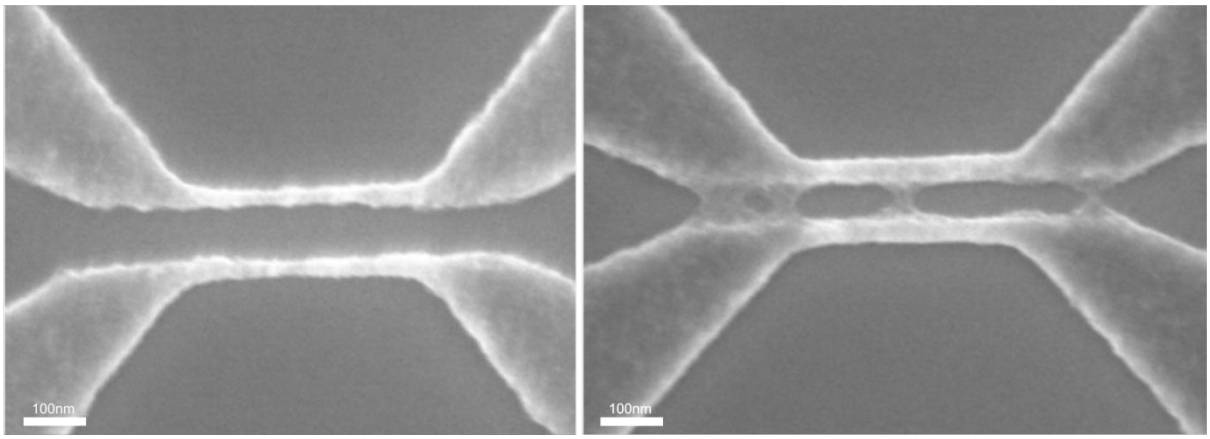


Fig. 5.30: SEM images of HSQ first layer resist pattern on Si: underexposed pattern with a dose of 525 uC/cm^2 (left image), overexposed pattern with a dose of 700 uC/cm^2 (right image).

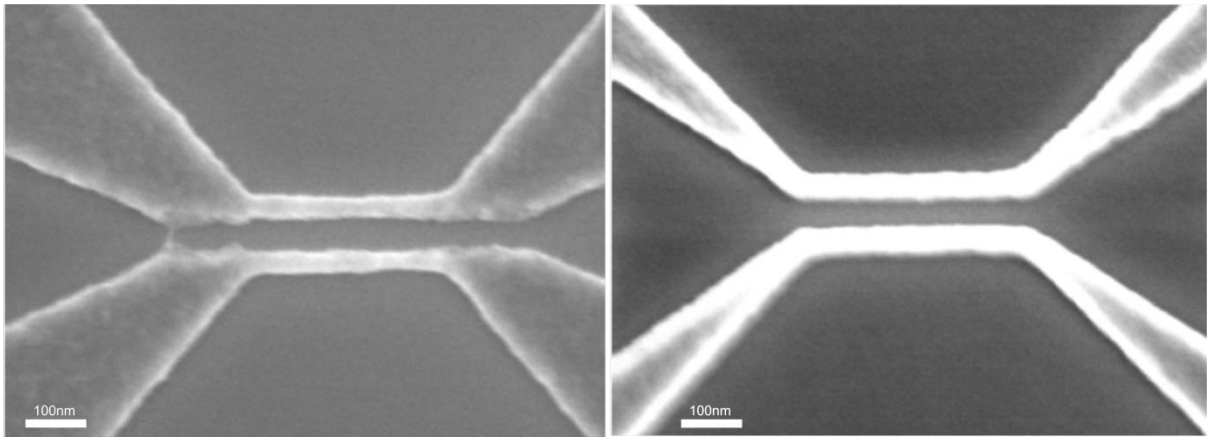


Fig. 5.31: SEM images of properly exposed HSQ resist pattern on Si using a dose of 525 uC/cm^2. Right image shows a narrower source drain tapering compared to the left image, this is adopted to reduce the capacitance between the top gate and the source leads for RF measurement purposes.

After exposure and development, a small number of HSQ first device layer patterns are inspected with the SEM to verify the e-beam exposure results. After that, in preparation for the first layer pattern transfer with dry etching, the sample is baked at 250 C for 4minutes and 30 seconds using the hot plate to harden the HSQ etch mask. Below is an SEM image of HSQ resist first device layer pattern on SOI (just before the Si dry etching process) showing a very good contrast between the doped and intrinsic Si device region.

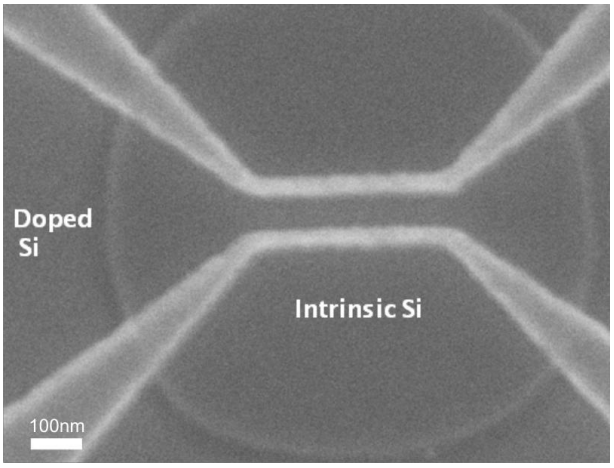


Fig. 5.32: SEM image of the HSQ first device layer pattern on SOI, showing a good contrast between the intrinsic and doped device region.

5.5.10 HSQ device layer pattern transfer with reactive ion etching

The first Si device layer is patterned with e-beam lithography using negative tone 60 nm thick HSQ resist. The e-beam pattern is then transferred to the SOI sample by dry etching the Si device layer against the HSQ resist. As discussed earlier, HQS physically and chemically behaves like silicon dioxide. Therefore, this etch process requires a good Si: SiO2 etch selectivity in addition to anisotropic Si etch profile to preserve the sidewalls of the Si channel.

The standard Oxford Instruments recipe installed on the 80+ RIE machine offers a very good Si:SiO2 etch selectivity of 4:1, it is based on SF6/O2 gas chemistry and uses an SF6:O2 4:3 gas ratio, pressure of 30 mTorr, RF power of 100 W at a platen temperature of 20 C [104]. This standard recipe is used to etch the Si device layer due to the good etch selectivity it offers. However, to fine tune the side walls anisotropy [98], the SF6:O2 gas flow ratio is modified to be 1:1, this improved the Si channel side wall profile, it also slightly reduced the process selectivity to be 3:1 Si:SiO2. However, this is still very sufficient to etch the 50 nm Si device layer against 60 nm of HSQ resist, the Si etch rate for this process is 60 nm/min. After etching the entire 50 nm Si device layer with this process, the remaining HSQ resist is removed with a short dip (less than a minute) in 20:1 BHF.

5.5.11 Phosphorus dopant redistribution during thermal oxidation

After defining the first device layer in Si using e-beam lithography and dry etching, the sample is oxidized to form the Al control gates oxide and to shrink the dimensions of the Si nanowire. This dry oxidation process will affect the doping profile of the Si layer, by causing lateral or vertical diffusion of the dopants. As discussed earlier, unlike boron impurities, phosphorus dopant redistribution is quite limited and it does not cause significant dopant migration. This was verified by Athena process simulation to show the effect of dry oxidation on the phosphorus dopant profile as follow:

A dry oxidation process, at 950 C for 20 minutes, to form 30 nm thermal oxide on the intrinsic and doped Si nanowire area was simulated. The results showed that the oxidation affects the lateral diffusion of the dopants, reducing our original 1.3 µm undoped Si region to about 1 µm after the oxidation. As for the dopants vertical diffusion, the simulations showed that the dopant diffuse down towards the box oxide layer as well as upwards into the 30 nm thermal oxide layer, the effect of this seems to be reasonable and the amount of diffusion into the box layer is limited.

In addition, the oxide growth rate follows the expected trend, where the oxidation rate is higher in the doped si region compared to the intrinsic region. Below are the process simulation results with vertical cutline through the SOI and thermal oxide showing the net doping levels after oxidation (the oxidation step had only a very small effect on the doping levels). Horizontal cutline of the net doping through the Si device layer and the thermal oxide is also shown below.

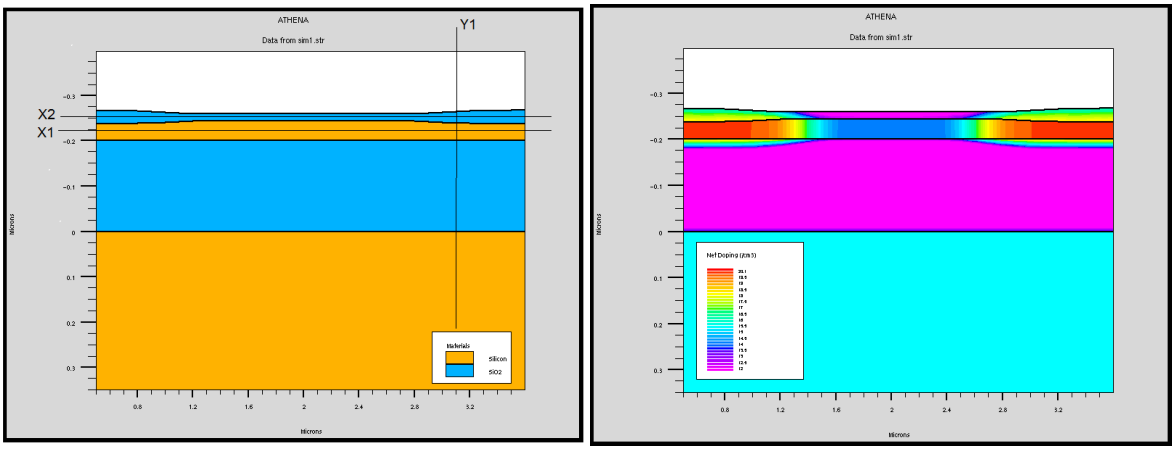


Fig.5.33: Athena process simulation, left image shows the Si channel after dry oxidation, right image shows the doping profile after dry oxidation at 950 C for 20 minutes (net doping label not visible, however the doping levels can be observed in the cross sections below). Doping profile before the oxidaiton process is shown in fig. 5.25.

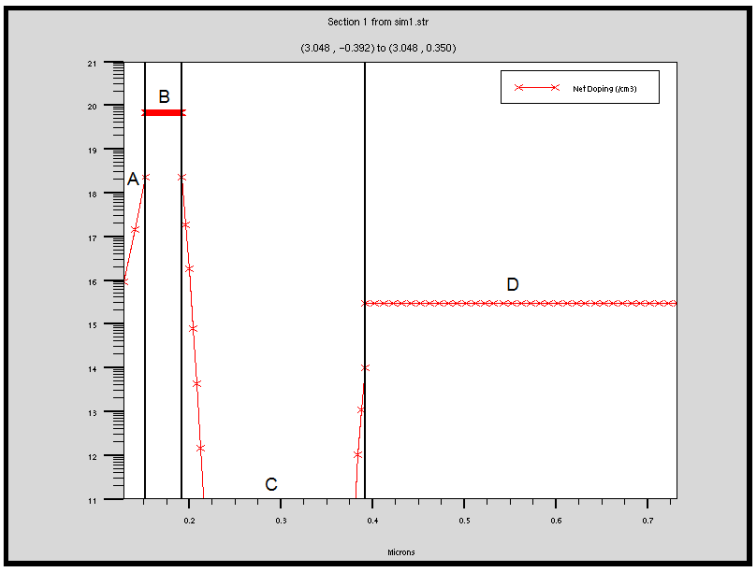


Fig. 5.34: Vertical cutline (Y1) of the net doping profile, where A is the net doping level of the dry thermal oxide region, B is the net doping level of the Si device layer (doped area), C is the net doping level of the box oxide region, and D is the net doping level of the bulk Si region.

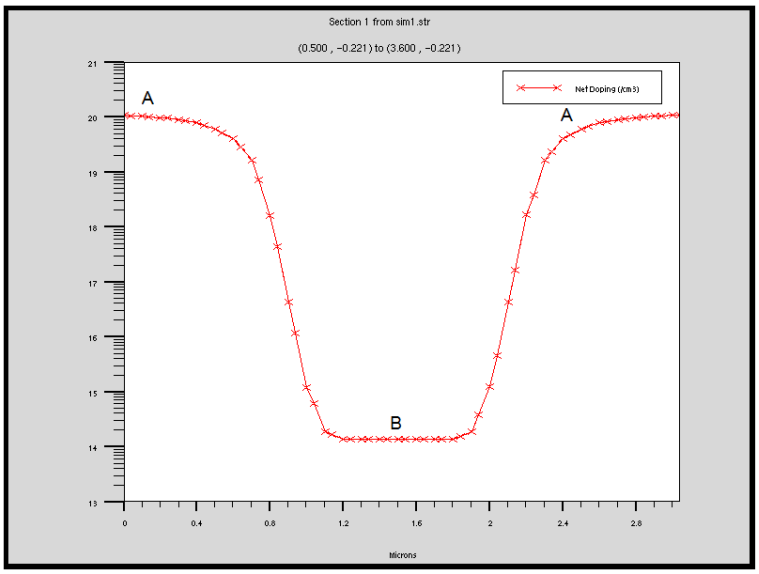


Fig. 5.35: Horizontal cutline (X1) of the net doping profile (through the Si device layer), where A is the net doping level of the Si device layer (doped area), and B is the net doping level of the Si device layer (2 µm undoped region).

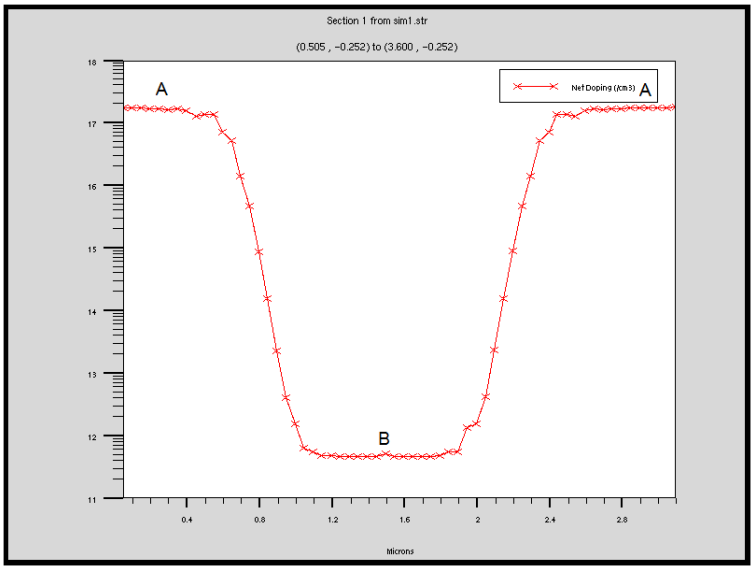


Fig. 5.36: Horizontal cutline (X2) of the net doping profile (through the thermal oxide layer), where A is the net doping level of the thermal oxide layer (oxide on top of the doped Si region), and B is the net doping level of the thermal oxide layer (oxide on top of the undoped Si region).

5.5.12 Al control gates layer definition using PMMA e-beam lithography

The Al control gates layer utilizes the same e-beam writing techniques as the Si HSQ device layer, proximity error correction (PEC) software is used to fracture the exposure dose across the layout with fine (1 nA) and coarse (25 nA) e-beam exposures employed, by virtue of the well-defined deep etched alignment marks, to reduce the e-beam write time and reduce the effect of e-beam drift.

This process is a lift off process aiming to realize 50 nm wide FinSET Al gates surrounding the device Si nanowire channel, this means that not only 50 nm fine Al features are required but also the continuity of the Al over the Si channel must be insured. Therefore, this process is very challenging due to the number of process parameters that must be optimized, these include: establishing an e-beam lithography process to define 50 nm features in PMMA, optimizing the Al evaporation to insure good uniformity and continuous coverage over the Si channel, and finally the lift off process needs to be tailored to provide successful metal lift off while protecting the 50 nm features from damage.

E-beam lithography experiments started with 400 nm PMMA 495 stack (MMA/PMMA layer) by performing dose tests/development time test to realize 40-50 nm features, these experiments showed that achieving such dimensions is not possible as the resist is too thick (PMMA 495 on its own is about 200 nm, spun at 6000 rpm), this thick resist causes too much electron backscattering and limits the minimum achievable feature size to above 70 nm.

Instead of diluting PMMA 495 and repeating the dose test and development time test; PMMA 950 is investigated instead. Although it has a higher molecular weight, this single layer resist offers a thinner resist layer that would effectively allow smaller feature to be defined. PMMA 950 (4% solid content diluted in anisole) layer thickness versus spin speed was developed as shown below, as shown in the figure spinning the resist at 6000 rpm provides a layer thickness of 140 nm. This potentially allows the definition of sub 50 nm features and at the same time would be suitable to lift off Al layers of up to 70 nm in thickness making this process suitable to realize the Al FinSET control gates.

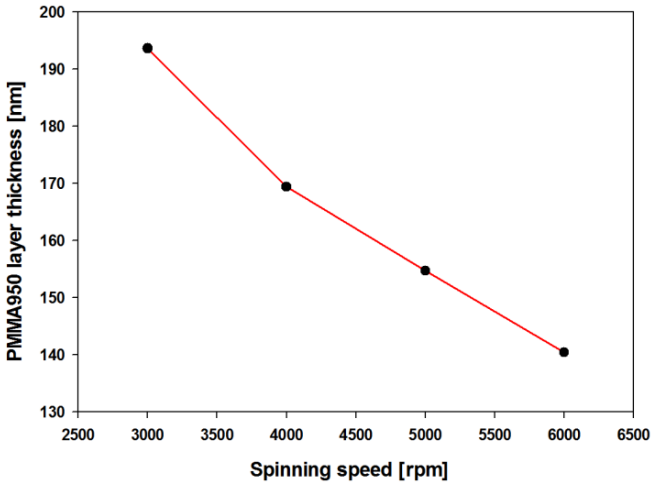


Fig. 5.37: PMMA 950 A4 (4% solid content diluted in anisole) layer thickens versus spin speed curve.

To establish this process, line test patterns are employed to determine the exposure dose and development time required for PMMA950, Al evaporation conditions and lift off parameters. The line patterns consisted of six groups of three 50 nm wide lines (500 µm long) with separation between the three lines of 50 nm, 60 nm, 70 nm, 80 nm, 90 nm, and 100 nm. The six line groups were arrayed 10 times to use 10 different exposure doses from 400 to 1200 uC/cm^2 with steps of 50 uC/cm^2. The array of six line groups exposed at 10 different doses were then repeated 8 times a across a 6 inch wafer and then manually diced to provide sufficient number of samples to test for PMMA 950 development time. This exposure was done on a 140 nm thick PMMA 950 spun at 6000 rpm and baked at 180 C for 3 minutes. This arrangement provides a true cross examination of both the exposure doses and the development times of PMMA950 at the same time while maintain a good e-beam writing efficiency. The 50 nm line patterns were used because they have similar dimensions as the target Al control gates layer however the exposure time for these patterns is much shorter making it possible to test more exposure doses and development times.

MIBK:IPA 1:3 is used for the development of PMMA950 test samples, this higher MIBK dilution rate has proven to provide a more gentle development of the fine 50 nm features compared to the standard MIBK:IPA 1:1 dilution ratio. Development time tests were performed by developing the line patters samples in MIBK:IPA 1:3 for 50 s, 55 s, 60 s, 65 s, 70 s and 75 s.

During the initial lift off experiments with bi-layer PMMA (PMMA 495), it was observed that SEM inspection of the resist pattern causes further exposure to the resist, causing pattern deformation. For this reason, the dose tests/development time tests samples were not imaged with SEM after e-beam exposure, instead 50 nm Al was deposited by electron beam evaporation and lifted off using acetone and pipette agitation. SEM inspection of the Al line patterns showed that the sample developed for 50 seconds has the largest number of properly defined line patterns from 650 uC/cm^2 up to 850 uC/cm^2, SEM images of this sample is shown below.

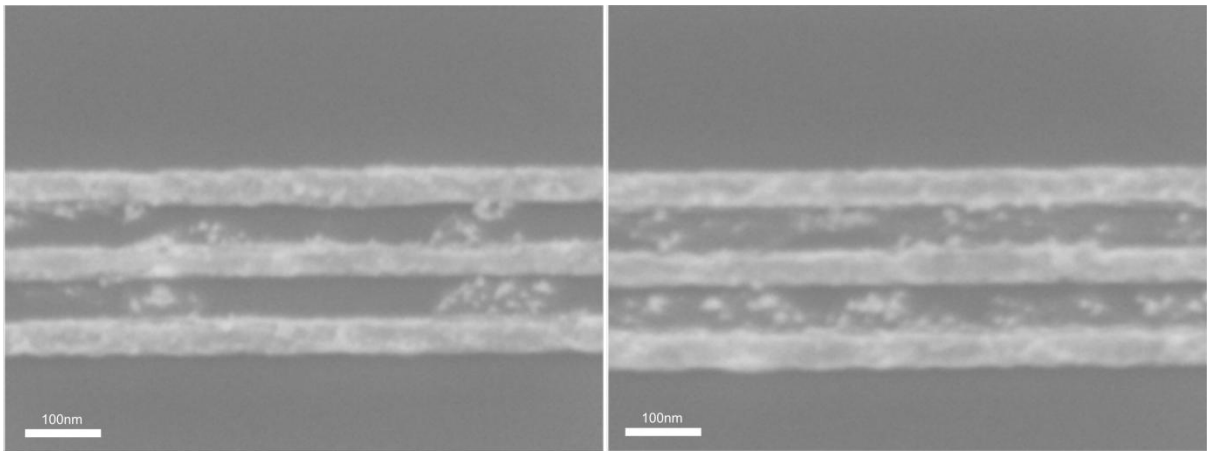


Fig. 5.38: SEM images showing the acetone lift off results of the 50 nm wide, 50 nm separated lines.

At this stage, an appropriate exposure dose and development time to realize the Al FinSET control gates is obtained from the line pattern experiments. On the other hand, these experiments demonstrated that the manual acetone lift off process is time consuming, and Al was lifting off with difficulty. In addition the SEM images showed a very porous Al layer with a large amount of Al debris present between the 50 nm lines (clear in fig. 5.38).

The challenges in lifting off Al indicate that the resist layer is relatively hard making resist removal and Al lift off more difficult. Therefore, to reduce the resist hardness, a shorter 90 seconds pre-exposure PMMA bake is used instead of the 3 minutes bake previously used.

As for the Al debris observed, this is mostly likely to have resulted from manual acetone pipette agitation, where neither acetone (as a resist remove) nor pipette agitation are sufficient to efficiently lift off Al especially around the 50 nm wide line patterns. To overcome this challenge, an automated 60 C heated NMP (N-Methyl-2-pyrrolidone) process is used instead of the manual acetone process to lift Al; the automated lift off process is performed in OPTI ST30 wet processing station, the sample is soaked in heated NMP for a controlled period of time (60 minutes), this is followed by an NMP Jet spray and DI water spray. Finally To improve the Al layer quality: the Al evaporation process is optimized to use an evaporation rate of 0.5 A^o/s (instead of 2.5 A^o/s), an evaporation pressure level of 2e-7 mbar with overnight pumping (lower evaporation pressure provides better quality films and

improves metal stiction to the sample), and finally the sample rotation during evaporation is set to 20 rpm to improve Al layer uniformity. These modifications improved the Al layer quality considerably (observed by SEM), SEM images of the porous Al observed earlier and the improved Al evaporation recipe result are shown below.

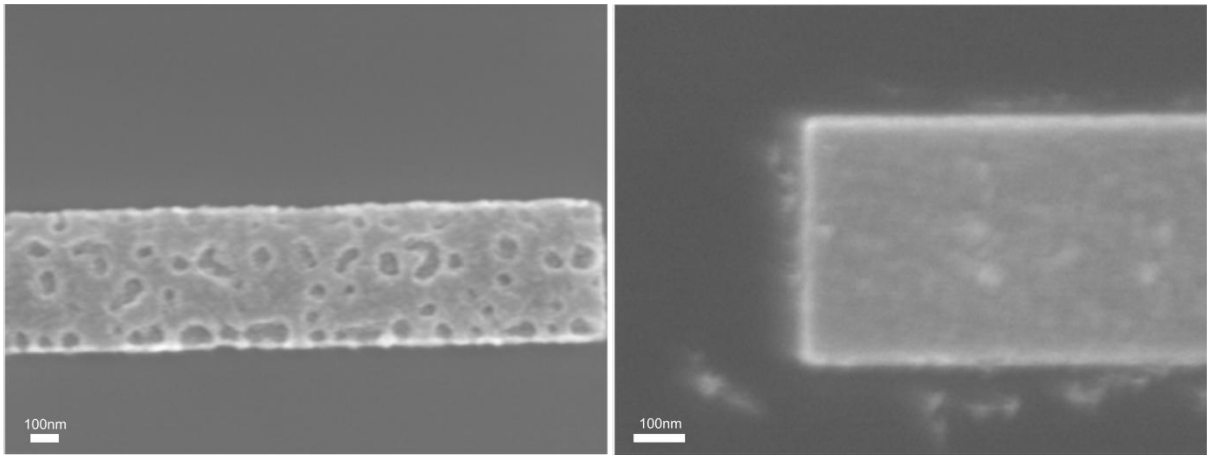


Fig 5.39: SEM images of the evaporated Al surface: Left image shows Al evaporated at 2.5 A^o/s at standard pressure level, right image shows improved Al film quality by using 0.5 A^o/s evaporation rate and overnight pumping for evaporation pressure.

Reducing the pre-exposure bake time for PMMA, using heated NMP with automated soak and spry functions, and improving the quality of evaporated Al result in a successful process that properly defines 50 nm wide Al lines with 50 nm separation, SEM images of the improved Al lift evaporation and lift off process is shown below:

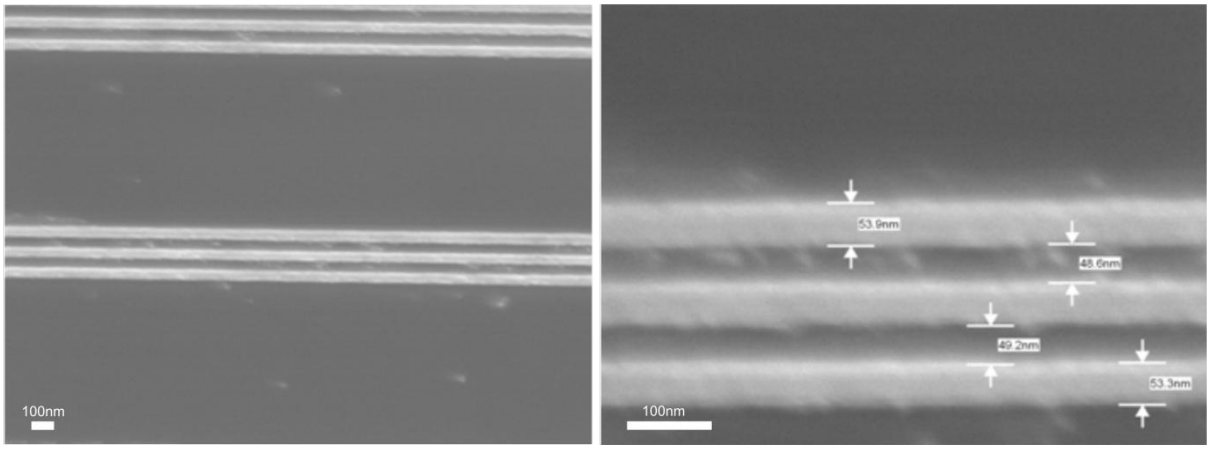


Fig. 5.40: SEM images showing the improved NMP lift off results of the 50 nm wide 50nm separated line patterns, lift off results are improved in comparison to fig. 5.38.

Using the line patterns process parameters, a simple dose test with a range of 700 - 1000 uC/cm^2 is preformed on the Al FinSET layout of the second device layer. This dose test showed that dose of 890

uC/cm^2 is the most suitable to realize the Al FinSET control gates. Using this dose and the same process parameters described above, the second device layer of FinSET style Al control gates is fabricated, SEM and optical images of the single electron turnstile and electrometer at this stage of the fabrication process are shown below.

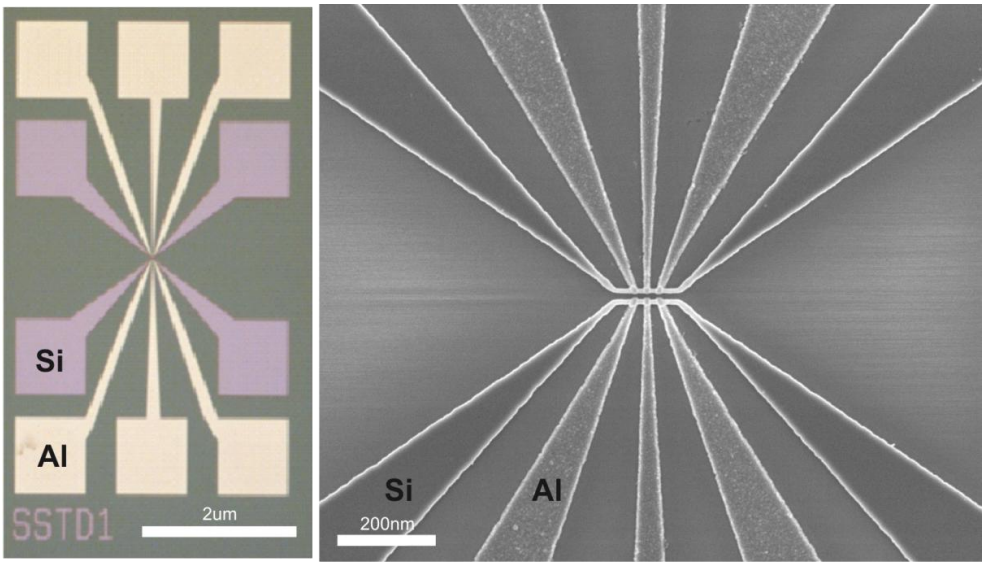


Fig. 5.41: FinSET Al control gate process, left image shows an optical image of the device, and the right image shows an SEM image of the first and second device layers.

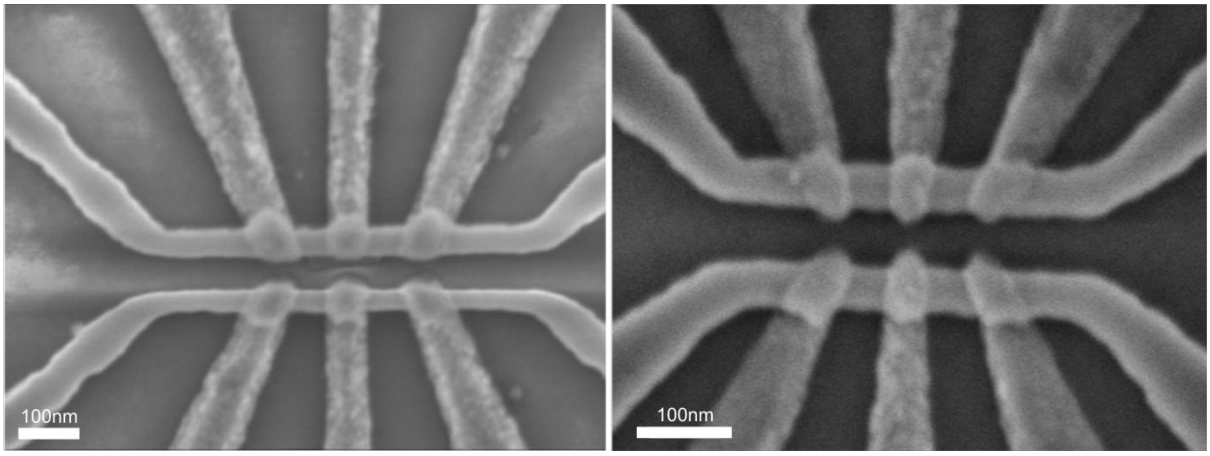


Fig. 5.42: SEM images showing the FinSET Al control gates on top of the Si nanowire channels.

From the SEM images of fig. 5.42, it is clear that the e-beam alignment between the first and second device layers is excellent, with misalignment estimated to be less than 10nm; these results were only possible due to the well-defined deep etched alignment marks process developed earlier.

5.5.13 Al control gates continuity over the SOI NW channels

The main challenge for the Al control gates process is to ensure that the Al control gates layer is uniform and continuous over the Si device channel (to ensure continuous FinSET gate coverage over the Si device channel).

For this reason, simple techniques like rotating the sample during evaporation to improve the deposited Al layer uniformity are employed. However, the main concern to insure control gates continuity is by using an Al layer thickness at least twice the thickness of the Si device layer underneath the Al control gates. Since the PMMA resist layer thickness is 140 nm, thickness of the Al layer evaporated is restricted to 70 nm to insure successful Al lift off. At the same time, thickness of the PMMA resist layer cannot be increased because that would compromise the 50 nm minimum feature size achievable with this resist (a thicker resist layer produces lower features resolution).

In other words, the maximum Al thickness possible for the second layer is 70 nm. Therefore, to insure Al control gates continuity; thickness of the Si device layer must be controlled precisely to be less than 35 nm. This is possible by starting with a 30 nm SOI substrate thickness instead of the previous suggested value of 50 nm. However, using HSQ resist to pattern the first device layer causes a problem. After pattern transfer of the first device layer to Si with dry etching, the remaining HSQ resist has to be removed with BHF; this process removes the reaming HSQ and at the same time etches down in the exposed buried oxide layer increasing the Si device layer step profile. There are two solutions to this problem, the first is to use a thinner HSQ layer to pattern the device layer, and this should leave a thinner HSQ layer after dry etching that requires a minimum removal time in BHF and consequently reduce BHF etching of the buried oxide to a minimum. The second solution is to use a different resist, that doesn't require HF processing to pattern the first device layer, however this less favourable due to the good resolution and etch resistance offered by HSQ.

Spin speed vs. HSQ layer thickness characterization has been preformed, results from that revealed that the minimum resist thickness possible (by spinning at maximum speed), without diluting the resist, is 55 nm. Therefore, this 55 nm resist was used to realize the first device layer with extra attention to the Si device layer dry etch step and the HSQ removal step with BHF, a shorter dry etch steps was used to minimize the possibility of buried oxide layer etching during the Si device layer etch process, the HSQ BHF removal time was also reduced from 30 seconds to 15 seconds to minimize buried oxide removal due to HF wet etching.

A special design with connected FinSET control gates, the electrometer Al control gates are connected to the turnstile Al control gats as shown below, is added to the fabricated designs on the sample. This will be used at the start of the measurement process to test if the Al layer is continuous over the Si nanowire or not.

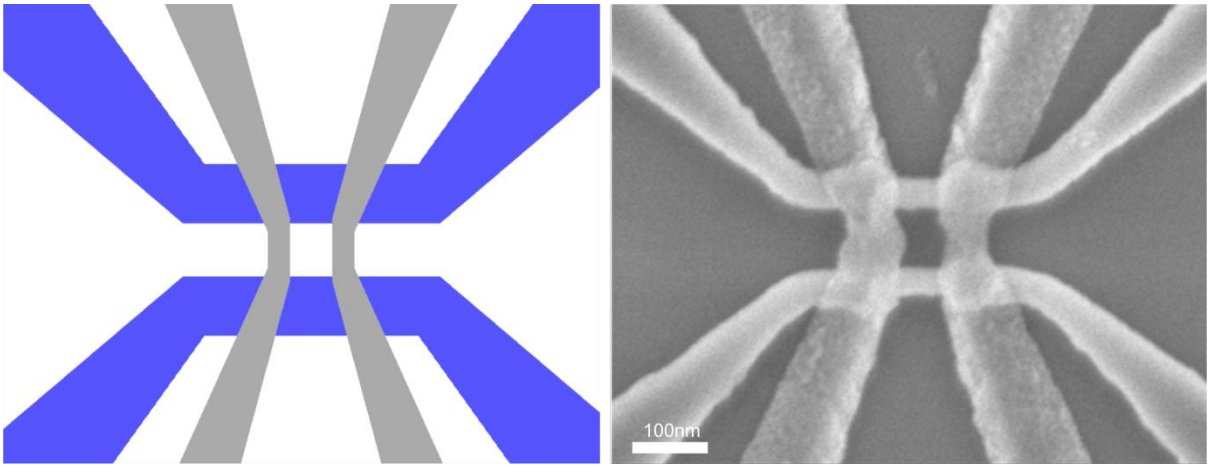


Fig. 5.43: Connected Al FinSET structure used to test Al layer continuity over the Si device channel.

5.5.14 Top gate oxide and contact via layer formation using bi-layer PMMA e-beam lithography

The top gate oxide is a 180 nm thick PECVD silicon dioxide layer deposited using four steps of 50 nm (PECVD process parameters are the same as the 100 nm doping mask PECVD process parameters described earlier).

For a more uniform inversion from the source to the fine device area, the contact layer includes metal tapering running from the source/drain region all the way close to the fine device area. To remove the 200 nm thick top gate oxide layer from the area under the metal contact pads and the metal tapering a positive resist mask profile is designed to form via holes through the top gate oxide layer all the way to the SOI device layer. A bi-layer MMA/PMMA layer with thickness of 400 nm is used here to define the positive profile on top of the 200 nm oxide layer, a special diluted BHF solution (BHF 5%) is then prepared to remove the 200 nm oxide layer at a moderate etch speed (10 nm / 15 s) with the MMA/PMMA used as an etch mask for the BHF solution. MMA 8.5 is spun at 5000 rpm to form a 150 nm thick MMA layer; sample is then baked at 150C for 65 seconds. After that PMMA 495 is spun at 5000 rpm forming a 250 nm thick layer, this is followed by a hot plate bake at 180 C for 65 s. Development of this bi-layer rest is done using MIBK:IPA 1:1 for 90 seconds.

The design of this contact via layer is basically the same as the coarse HSQ device layer design with one alteration: the original coarse design of the Si device layer is negatively biased (similar to a shrink function) by 100 nm in the fine tapering region and by 10 µm in the large pads area. To estimate the exposure dose required to realize these patterns, a dose test from 450 to 700 uC/cm^2 was preformed. Based on the dose test results, a dose of 525 uC/cm^2 is suitable to realize the contact via layer for both

the fine tapering region and the large pads region. Optical images of the top gate oxide via layer are shown below after the BHF etch process.

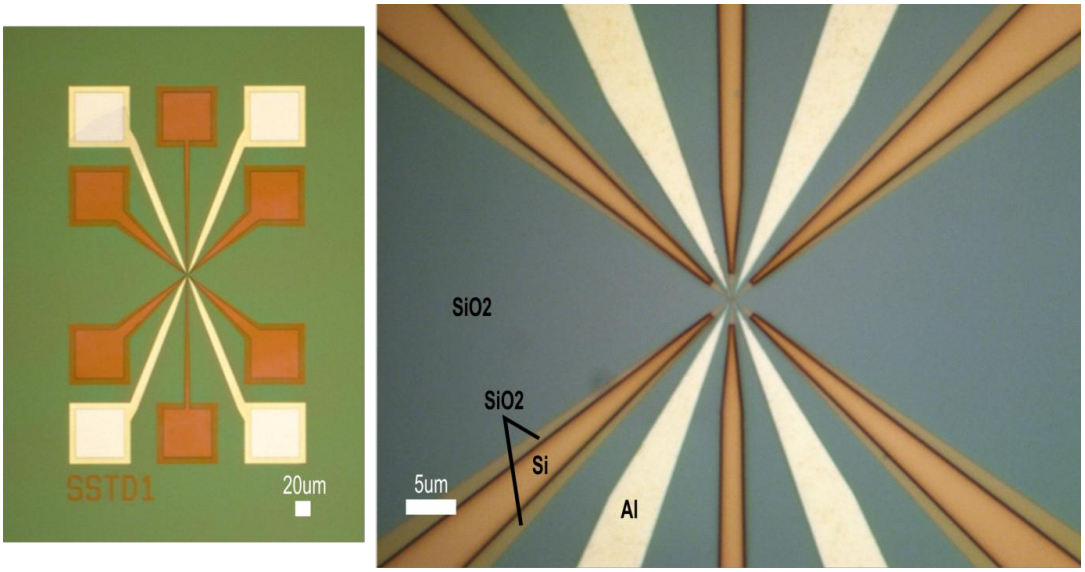


Fig. 5.44: Optical images showing the etched contacts via layer prior to contacts and top gate metallization

5.5.15 Al top gate and contacts layer definition using bi-layer PMMA e-beam lithography

After defining the silicon dioxide top gate oxide layer, 3 um x 3 um Al top gate and 100 µm x 100 µm Al contact pads are defined using bi-layer PMMA (PMMA 495) e-beam lithography and lift off. This resist process is used because it provides sufficient resolution for the relatively large features of the top gate and contacts layer, at the same time the bi-layer resist profile of 450 nm makes the lift off for 250 nm thick Al contact layer easy.

The process parameters including resist coating, exposure dose, post-exposure bake, development, and are the same as the conditions used to realize the contacts via layer described in the previous section. SEM image of this exposure after 250 nm Al evaporation and lift off is shown below. Al evaporation and lift off parameters are similar to the conditions used to realize the FinSET control gates layer.

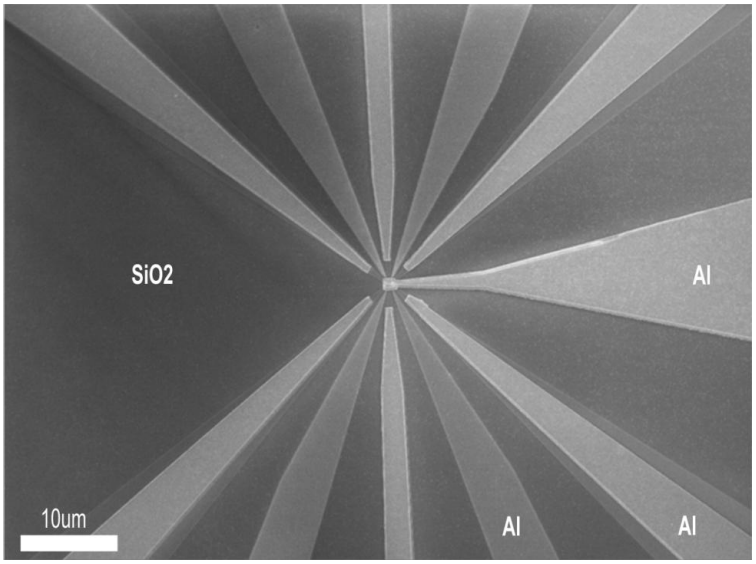


Fig. 5.45: SEM image, at the end of the fabrication process, showing the Al top gate and the Al contacts layer.

After the top gate and contacts layer lithography and pattern transfer via lift off, the sample is annealed with forming gas (5% H2) at 400 C for 10 minutes, this anneal process is used to improve the ohmic characterises of the Al contact pads. This recipe has proven to improve the ohmic characteristics of Al contact pads on Si during hall measurement, used to determine carrier concentration. This anneal process concludes the fabrication process of the Al FinSET single electron turnstile and electrometer device.

5.6 FinSET device layouts

With the FinSET device fabrication process established, other exciting device layouts are investigated, these include devices with a single quantum dot turnstile and electrometer, devices with side gates to provide extra control of the quantum dot potential, devices where the electrometer QD is larger than the single electron turnstile QD to increase the detection current and devices with double quantum of different sizes (asymmetric double QDs) for the purpose of simplifying the QDs characterization during measurements. Some of the successfully fabricated Al FinSET structures are shown below. Appendix B includes schematics and SEM images of all the fabricated Al FinSET devices.

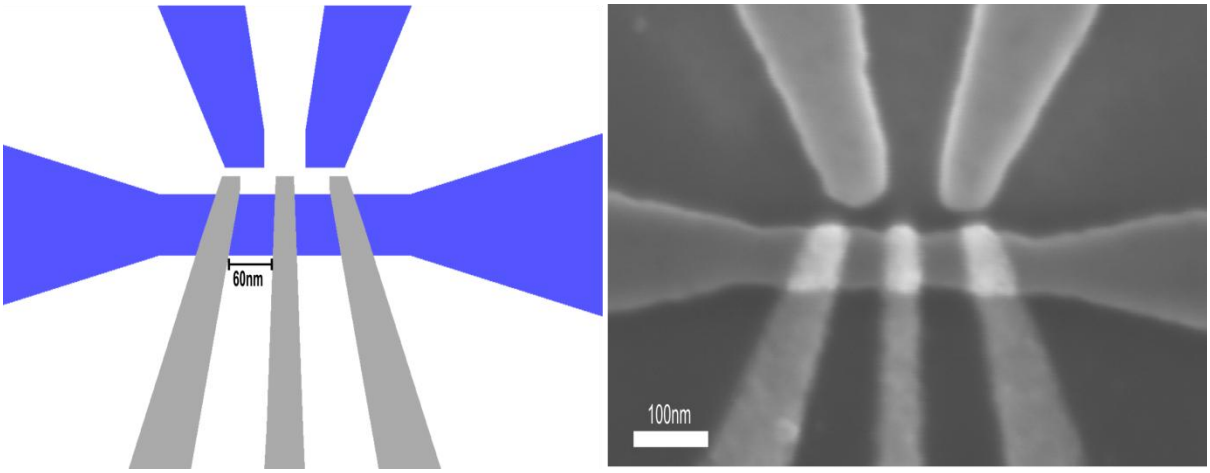


Fig. 5.46: Double quantum dots turnstile device with side gates, both QDs are 60nm in size.

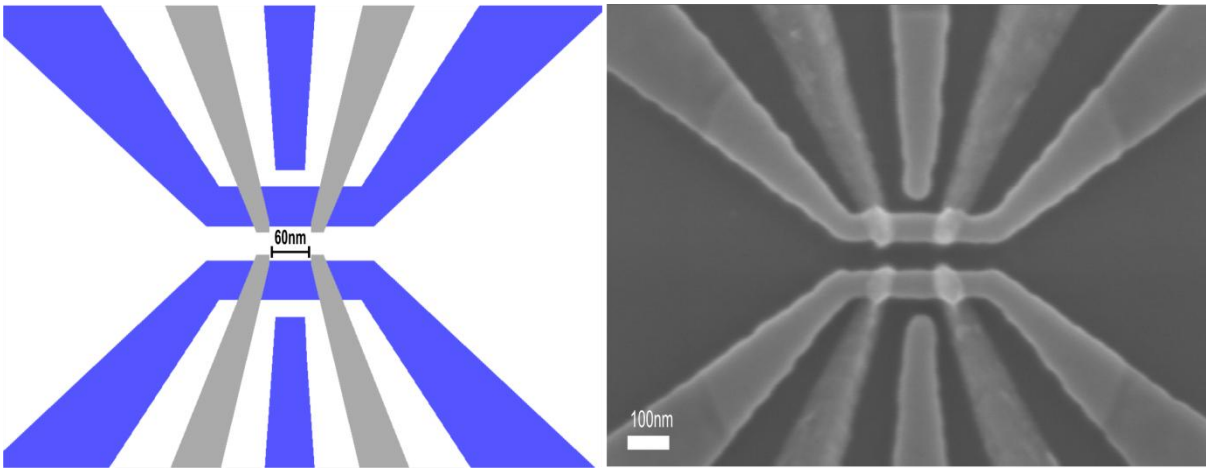


Fig. 5.47: Single quantum dot turnstile and electrometer with Si side gates, both QDs are 60nm in size.

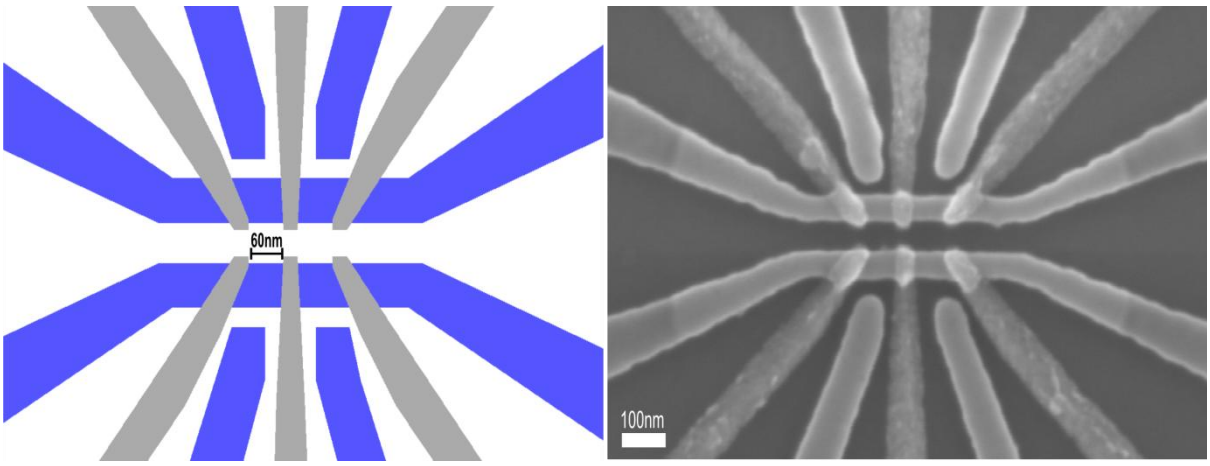


Fig 5.48: Double quantum dot turnstile and electrometer with Si side gates, all QDs are designed to be 60nm in width.

5.7 Summary

In this chapter, an important building block of the SISSQIT platform, the single spin transfer device (SETD) was introduced. A novel design for the SETD integrated with an electrometer was described; where the proposed SETD design used straight lines to avoid pattern dependant oxidation. 3D FEM capacitance simulations of the SETD were preformed, to extract the electrical characteristics of the structure, followed by single electron circuit simulations. A novel simulation approach is used to apply a fixed potential to the upper gate and a specially designed pulse sequence to source and the gates. This simulation scheme demonstrated successful single electron transfer operations.

This chapter also described the full fabrication process of the metal FinSET single electron turnstile and electrometer platform, Appendix A has a full list of the fabrication process parameters used to realize these devices. For the first device batch, this fabrication method of using both Al and Si gates to form quantum dots demonstrates a fabrication process yield close to 90%, where the fabrication yield here represents the yield of the lithography, dry etching and lift off processes and is determined from SEM inspection of 144 devices fabricated on the same substrate.

This fabrication approach utilizing Al and Si gates to form quantum dots and to control their potential is compatible with conventional MOS technologies, shows good reproducibility and offers great flexibility to integrate more complex structures.

Chapter 6

Characterization and Evolution of the Single Electron Transfer Device

6.1 First device generation with Al FinSET barrier gates

Initial measurements and characterization of the single electron transfer devices with Al control gates is carried out, at the University of Southampton, by simply measuring the source drain channel resistance at room temperature with all the metal barrier gates and the top gate grounded. As the device channel is intrinsic in the centre, typical values for the channel resistance are between 2-5 MΩ at room temperature. This simple check also helps to verify good ohmic contacts between the metal pads and the doped silicon pads underneath. Figure 6.1 below shows the channel resistance of one of the fabricated SETs at room temperature. As expected, when no top gate is applied the channel is not conducting; however at a top gate voltage of around 4 V (all other gates grounded) an inversion layer starts to form and the channel is populated with carriers reducing the channel resistance to only 124 KΩ.

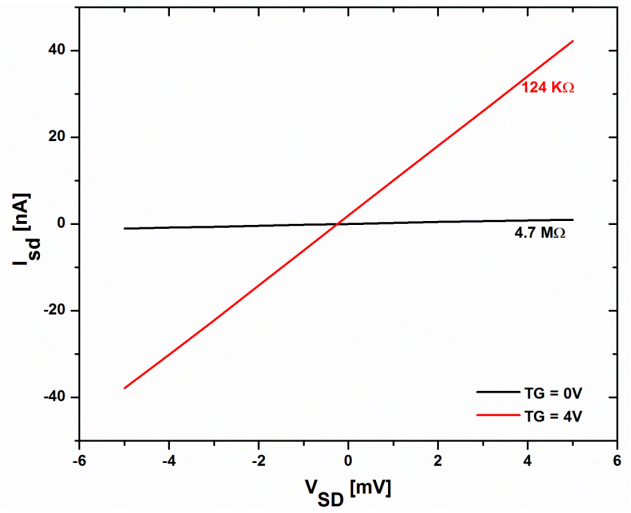


Fig. 6.1: Effect of the top gate potential on the source drain conductance of a fabricated SET structure (similar to the one shown in fig. 6.2) with all other gates grounded at room temperature.

After the room temperature channel resistance tests, the devices are then tested at liquid Helium temperatures (4.2 K), at the University of Cambridge in collaboration with Julia Perez-Barraza, to examine the transport properties of the SETs and the performance of the Si side gates and Al control gates in details. The sample is submerged in a liquid helium dewar using a dipping probe stick. In the following sub sections, a number of different designs from the first device batch are tested:

6.1.1 Double quantum dots SET

The first device to be characterised is shown in fig. 6.2 below, it has a single SET channel with two Si side gates (S1 and S2) and three Al barrier gates (A1, A2 and A3) designed to form two quantum dotes connected in series.

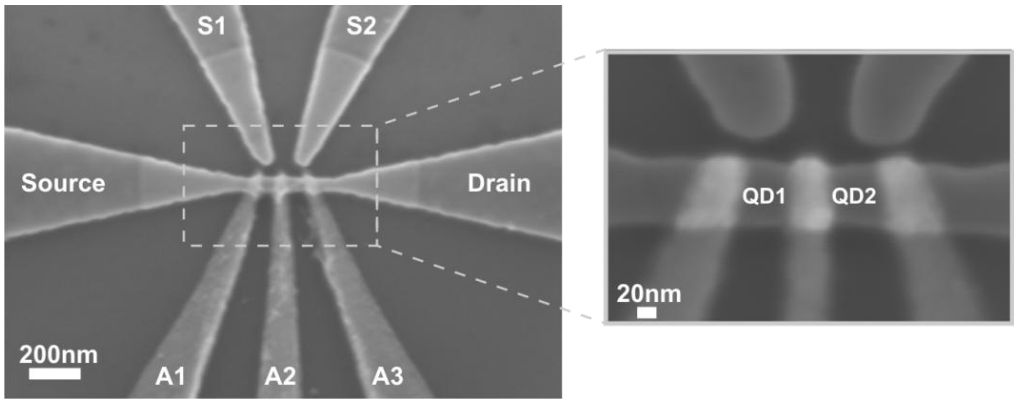


Fig 6.2: SEM image of a FinSET double quantum dot SOI transistor. Right side image a close-up SEM view of the structure, in this device gates A1 and A3 are 40 nm wide, gate A2 is 30 nm wide and the separation between the Al FinSET gates is 50 nm.

The dc measurements were performed at a constant source drain potential of 1 mV. The effect of the top gate potential (V_{TG}) on the source-drain dc current (I_{SD}) at 4.2 K and 300 K is investigated in Fig. 6.3 below, these characteristics are similar to the characteristics of a MOS field effect transistor, Fig 6.3 also shows an approximate top gate threshold voltage of 1.2 V and demonstrates the effectiveness of the top gate in forming the carrier inversion layer in the intrinsic SOI.

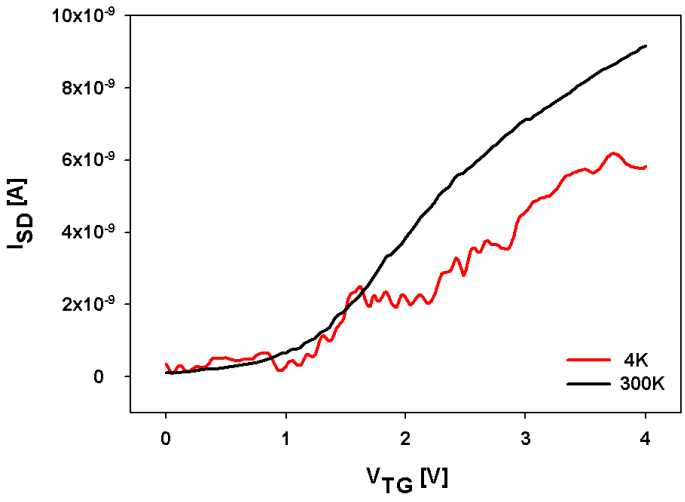


Fig 6.3: Electrical characteristics of the FinSET DQD transistor showing the source drain current as function of the top gate voltage with all gates grounded at 300 K and 4 K.

At a constant V_{TG} of 5 V, I_{SD} as a function of each of the Al FinSET gates with all other gates grounded at 4.2 K is shown in Fig. 6.4; this figure demonstrates the effectiveness of the Al FinSET gates in controlling the channel conductance as reflected by the rapid current change from 0 nA to 6 nA. These results show that the Al gates can be used to turn the device channel on and off, proving that these gates are able to form the designed double quantum dots. However, the conductivity curves of Fig 6.4 show that gate A2 has a slightly weaker effect on the channel conductance compared to gates A1 and A3 and this can possibly make it difficult to control the designed interdot QD coupling.

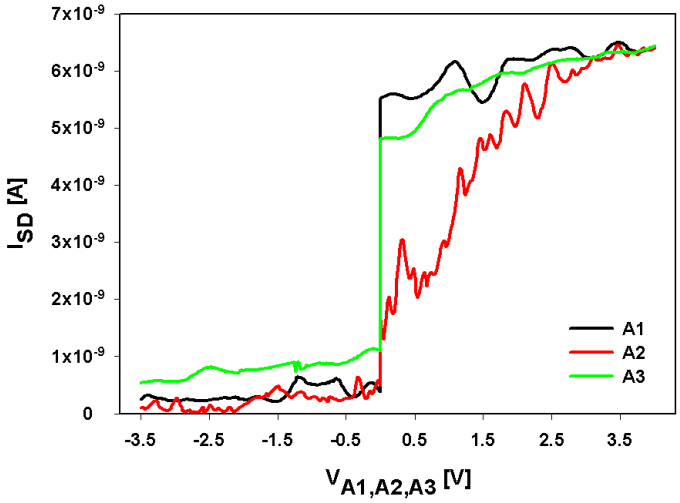


Fig 6.4: Electrical characteristics of the FinSET DQD transistor showing the source drain current as function of V_{A1}, V_{A2} and V_{A3} with top gate voltage at 5 V and all gates grounded at 4 K.

On the other hand, the relatively high OFF current observed in this device (shown in fig. 6.4) is unclear, it mostly indicates possible leakage through the Al gates or even defect switching characteristics. At 4 K with a top gate voltage of 5 V and with V_{A1} = V_{A3} = 0.2 V and V_{A2} = 0 V, we have recorded I_{SD} as a function of the Si plunger gates potential in Fig. 6.5. These results show complex Coulomb oscillations characteristics that reflect the characteristics of a multiple quantum dots system.

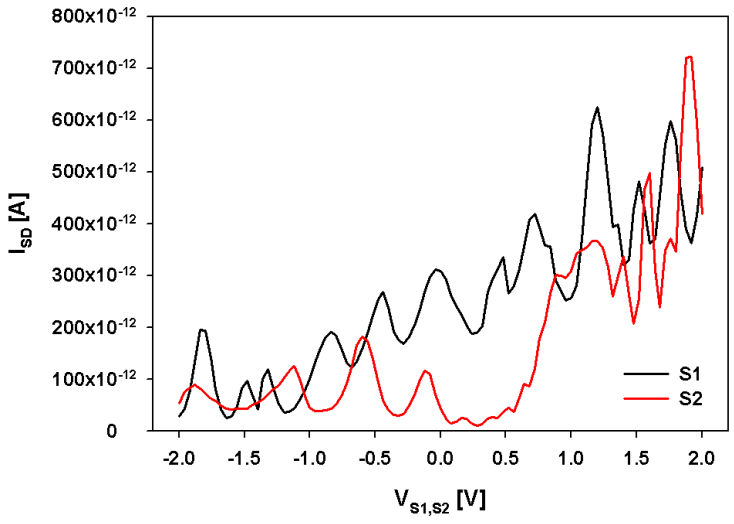


Fig 6.5: Coulomb oscillations characteristics of the double quantum dot structure observed at 4 K with top gate at 5 V, V_{A2} at 0 V, V_{A1} and V_{A3} at 0.2 V.

6.1.2 Single quantum dot SET with a charge sensor

Some of the other devices tested include a single quantum dot SET coupled to a charge sensor; these structures are symmetrical and therefore interchangeable, for characterization purposes the two single quantum dot SET parts of the device are referred to as a top SET and a bottom SET, an SEM image of the device tested is shown below.

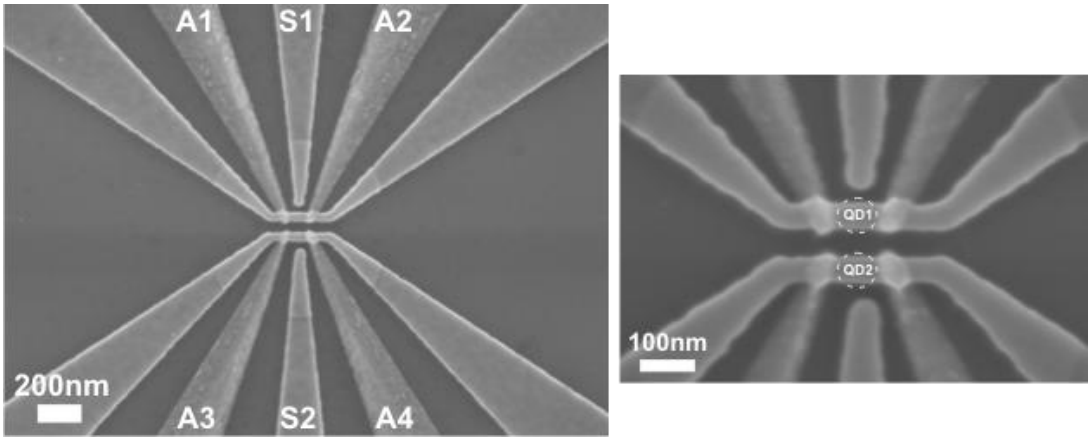


Fig 6.6: SEM image of a single QD Al FinSET turnstile and electrometer platform, (right side) a close-up SEM view of the structure, the Al gates here are 35 nm wide with a spacing of 60 nm, the Si plunger gates are 60 nm wide and 25 nm away from the SOI channel.. The separation between the turnstile and the electrometer is approximately 45 nm

Prior to the low temperature measurements, Initial room temperature measurements are carried out by sweeping the top gate to find the threshold voltage required for conduction in the intrinsic device channel. After that suitable operation voltage range must be identified for each of the Al barrier gates and the Si side gates in order to observe Coulomb oscillations and allow this device to be operated in the few electrons regime.

The effect of the top gate potential V_{TG} on the source-drain dc current I_{SD}, at the source-drain voltage of 1 mV at room temperature, for the top and bottom SETs of this device are shown in Fig. 6.7 below. Typical threshold behaviour similar to n-type MOSFET can be observed suggesting the inversion layer formation in the intrinsic SOI channel.

Ideally the top gate potential required to turn the channel is a positive potential, however as fig. 6.7 below shows the top gate inversion of this device starts slightly below 0V. This indicates the presence of some fixed charges in the top gate oxide of this device causing a slight shift in the top gate threshold voltage.

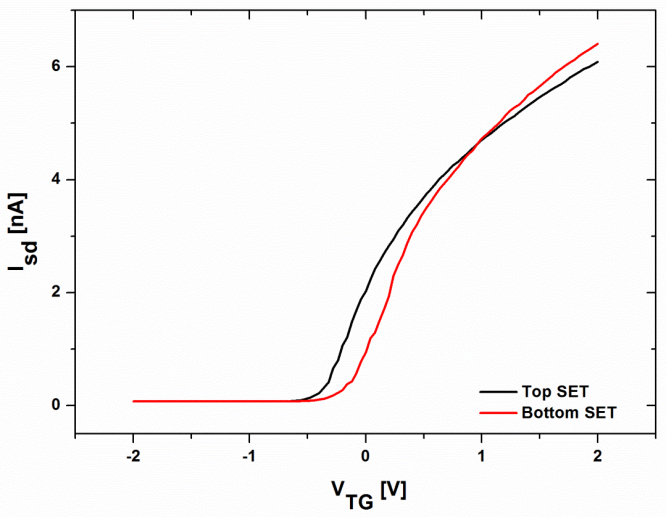


Fig. 6.7: Source drain current of both the top and bottom SETs of the single electron transfer device and electrometer as a function of the top gate voltage at room temperature 300 K with a source drain voltage of 1 mV and all other gates grounded.

As mentioned earlier, the second step is to focus on characterizing each single electron transistor individually at low temperature to see how the patterned Al FinSET gates and Si plunger gate work. First, in order to find out the region where single electron transfer characteristics are observed, we have measured I_{SD} against the Si plunger gate voltage at the various Al FinSET gate voltages. Figure 6.8 shows I_{SD} of the top SET as a function of the voltages applied to the Al barrier gates, V_{A1} and V_{A2}, and the Si plunger gate, V_{S1} at V_{SD} of 1 mV and V_{TG} of 2 V at 4 K. The observed Coulomb oscillation characteristics show that the single electron island is successfully defined by the Al FinSET gates, and the potential of the island is tunable by the Si plunger gate. According to this contour current plot, the characteristics of this device can be divided into three operation regimes: (1) less than threshold regime, (2) Coulomb oscillation regime, and (3) highly conductive regime. These operation regimes correspond to the numbers shown on the current contour plot of Fig. 6.8.

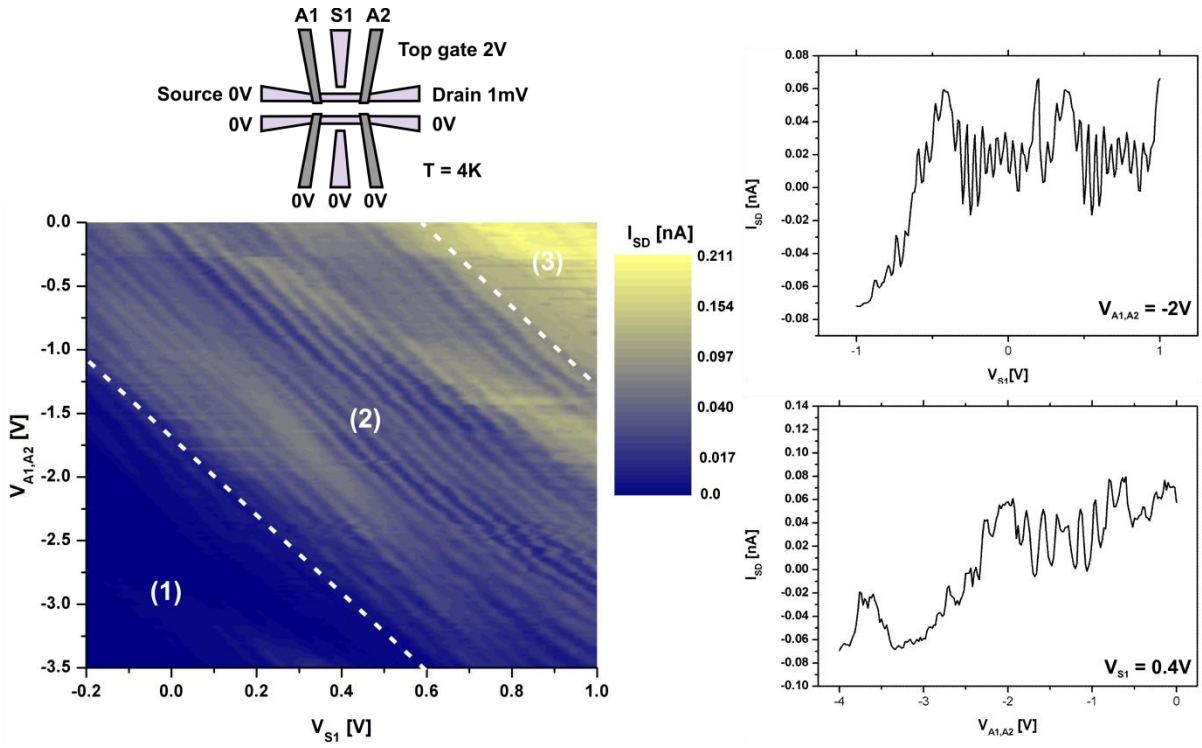


Fig. 6.8 Left: source drain current of the top SET as a function of the Al barrier gates potential (V_{A1}, V_{A2}) and Si plunger gate potential (V_{S1}) with source drain of 1 mV and top gate voltage of 2 V at 4 K with all other gates grounded. Top right: source drain current of the top SET as a function of V_{S1} at a fixed V_{A1}, V_{A2} value of -2V. Bottom right: source drain current of the top SET as a function of V_{A1}, V_{A2} at a fixed V_{S1} value of 0.4V.

In region 1, where the larger negative voltage is applied to A1 and A2 and V_{S1} is also low, the current level of I_{SD} is very low. In this regime, holes would be accumulated on the top surface of the channel under the Al FinSET gates due to the negative V_{A1} and V_{A2}. This hole accumulation causes relatively high potential barrier against the electrons on the source and drain regions. At a fixed V_{A1} and V_{A2} in this region, with increasing V_{S1}, threshold behaviour at which the current starts to flow is identified. The threshold voltage V_{th} is at around 0.6 V for V_{A1} = V_{A2} = -3.5 V and then decreased down to -0.2 V with increasing V_{A1} and V_{A2} up to -1.2 V. Obviously the boundary between regions (1) and (2) drawn in Fig. 4 is roughly tracing V_{th}. This result suggests that the threshold voltage of our SET is tunable by altering the tunnelling barriers and has a simple correlation with the tuning voltage V_{A1} and V_{A2}. Ono et al. [12] has realized the turnstile operation just below the threshold voltage of the tunable double-gate SET, indicating the optimum operation condition of our double FinSET gate turnstile device would be around the boundary.

In region number 2, where the oscillation of the I_{SD} is clearly observed, we can assume that the potential barriers created by two Al FinSET gates are low enough to allow electron tunnelling. It is

worth noting that even at V_{A1} = V_{A2} = 0, we can identify the Coulomb oscillation with respect to the sweep of V_{S1}. This suggests that the constant 2 V applied to the top gate is enough to demonstrate the Coulomb blockade effect thanks to partial screening by the Al FinSET gates. The Coulomb oscillation structure is identified through region 2 but the period is not uniform and in some part the current level of the valley of the oscillation is not low enough. Ideally the parallel diagonal lines are expected if only the single dot contributes to the Coulomb blockade. The observed deviation indicates that more than one QD should be considered to analyse this data in detail.

In region 3, where V_{S1} is high, the oscillation characteristics have mostly disappeared and relatively high level of current flows regardless of V_{S1}. The positive potential applied to the Si plunger gate places the QD in a mostly transparent barriers regime. This clearly suggests that V_{S1} is coupled not only to the QD but also to the tunnelling barrier.

From the current contour plot of fig. 6.8, the source drain current as a function of V_{S1} at a fixed V_{A1}, V_{A2} value of -2V (top right plot in fig. 6.8) and the source drain current as a function of V_{A1}, V_{A2} at a fixed V_{S1} value of 0.4V (bottom right plot in fig. 6.8) have been extracted. These two plots show signature Coulomb oscillation characteristics due to the Al and Si gates effect on the QD potential. From these two plots, the coupling capacitance between the SET QD and the Si side gate S1 is approximately 0.8aF, and the coupling capacitance between the QD and the Al gates A1 and A2 is approximately 0.5aF.

For the bottom QD SET, we have investigated the effect of the top gate and source-drain voltages at a certain biasing condition of the Al FinSET gates and Si plunger gate. Figure 6.9 shows the source drain current of the bottom QD transistor as a function of voltage applied to V_{SD} and V_{TG} at constant Al FinSET gates voltage, V_{A3} and V_{A4} of -1 V and a Si plunger gate voltage V_{S2} of 0.9 V. The Coulomb diamond characteristics are clearly observed in Fig. 5. Assuming a single QD formation in this structure, we have extracted that the total capacitance of the QD is approximately 23 aF. From that the charging energy is estimated to be 7 meV, corresponding to a quantum dot diameter of approximately 60 nm which is roughly in agreement with the length of QD shown in the SEM image of Fig. 2. However, as mentioned before, actual maximum size of the QD are estimated to be 28 x 24 x 60 nm due to the thermal oxidation step. Furthermore, in our SET operation, electron confinement effects in the 2D inversion layer could play an important role to define the effective size of the QD. To establish a more precise comparison, further measurements and analysis to estimate the various possible coupling capacitances, such as between the QD and other individual Al and Si gates are needed.

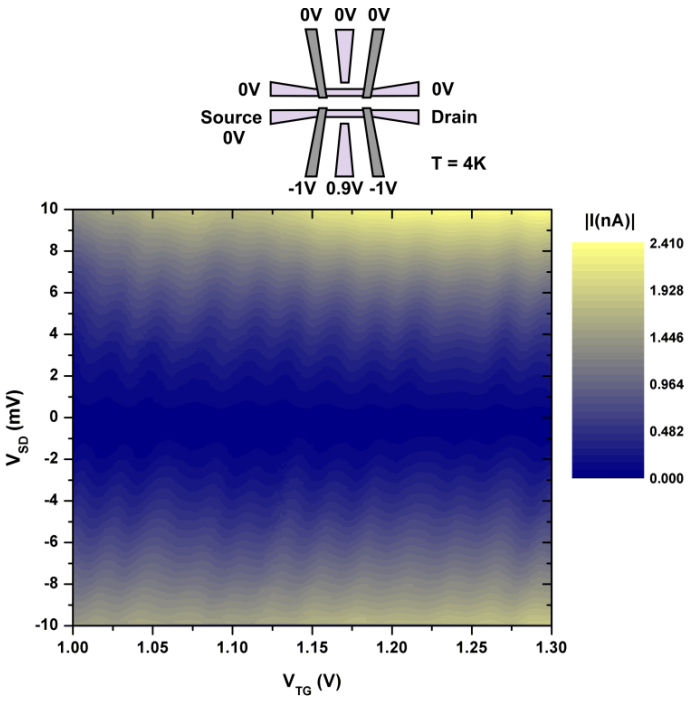


Fig. 6.9: Source drain current of the bottom SET as a function of the source drain potential (V_{SD}) and the top gate potential (V_{TG}) at 4 K with 0.9 V applied to S2 and -1 V applied to A3 and A4.

So far the Al barrier gates have been used together (same voltage applied to both) to define the potential barriers in the channel in order to form a quantum dot. Further investigation into the performance of each barrier gate is carried out by sweeping the barriers individually while recording the source drain current at 4.2 K. Fig. 6.10 below shows the Source drain current as a function of the voltage applied to barrier gate A1, barrier gate A2, top gate and the Si side gate for the top (left image) and bottom (right image) SET of the structure shown in fig. 6.6.

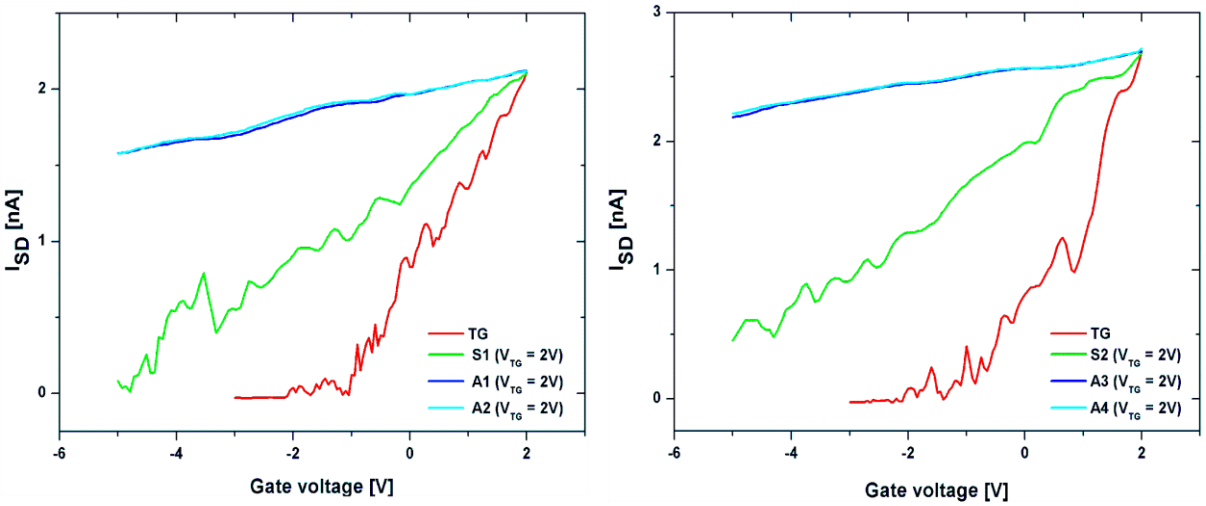


Fig. 6.10: Source drain current of the top (left) and bottom (right) SET as a function of the top gate voltage (with all gates grounded), the Si side gates and the Al barrier gates with a top gate voltage of 2 V at 4.2 K with a source drain voltage of 1 mV.

From fig. 6.10, it is very clear that for this device the effect of the top gate and the Si side gates on the channel conduction is much greater than the effect of the Al barrier gates for both the top and bottom SET. It is expected that the top gates has a stronger effect than all the other gates, however the influence of the Al barrier gates in any case should still be stronger than the influence of the Si side gates as the Al gates are designed and fabricated to be covering the channel (as shown in the SEM images) while the Si side gates are approximately 20 nm away from the NW channel.

In order to better understand this issue, five other devices of this same design (shown in SEM image of 6.6) have been tested in the same way: recording the source drain current as a function of the individual Al barrier gates and the Si side gates at 4.2 K. in all these device the weak Al barrier effect is consistent where only two Al metal barriers, in the five devices tested, managed to pinch off the conduction in the channel completely. In these tests the Al barriers effect on the channel conduction is significant only when the top gate potential is less than 1.5 V (similar to fig. 6.10 of the top SET). However at a top gate voltage of 1.5 V, the 2DEG is not homogenously formed in the SOI nanowire channels and the channel conduction is irregular with a lot of extra defects (as can be clearly seen in the switch on curve of the top gate in fig. 6.3).

The ideal operation regime for this device is at higher top gates voltages (above 2-3 V) due to the relatively thick 180-200 nm top gate oxide, at this regime the 2DEG would be properly formed and the transport through the channel would be regular. At the low 2DEG density regime (top gate below 1.5 V) the Coulomb diamonds do not close (the conduction lines forming the Coulomb diamonds are not crossing similar to fig. 6.9) and no periodic Coulomb oscillations can be observed. On the other hand, at higher top gate voltages, the effect of the Al barriers is weak and it is difficult to form an opaque potential barrier using the Al control gates. On the other hand, in all of these single dot devices with a charge sensor, the effect of the Si side gates was stronger than the effect of the Al barrier gate suggesting that most of the Al control gates are somehow physically broken prior to electrical testing.

This poor yield of effective Al control gates is more evident in structures with a larger number of Al control gates. For a double quantum dots turnstile device coupled to a double quantum dot charge sensor, the number of Al control gates required is 6 (to define the required 4 quantum dots). An SEM image of this structure is shown in fig. 6.12 below:

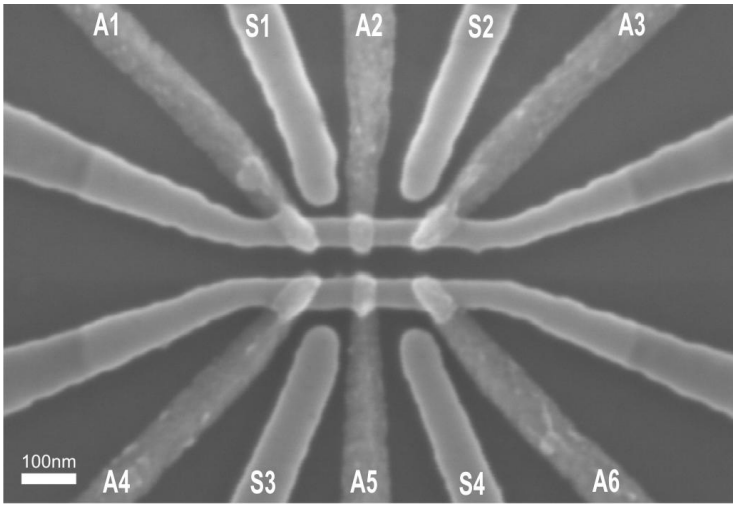


Fig. 6.11: SEM image of a double QD single electron transfer device coupled to a double QD charge sensor utilizing 6 Al control gates and 4 Si side gates.

The effect of the top gate, the Al control gates and the Si side gates on the source and drain current of both the top and bottom SETs at 4.2 K is recorded and shown in figure 6.13 below.

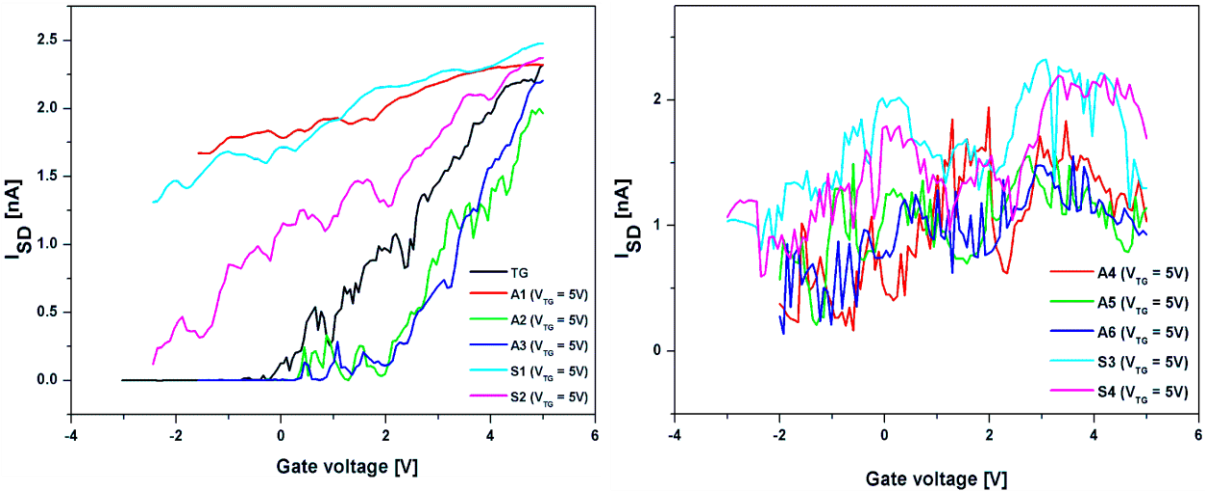


Fig. 6.12: Source drain current of the top (left image) and bottom (right image) SET as a function of the top gate voltage (with all gates grounded), the Si side gates and the Al barrier gates with a top gate voltage of 5V at 4.2K with a source drain voltage of 1mV.

As shown in fig. 6.13, the effect of the control gates A2 and A3 on the conduction of the top SET is much more significant than the effect of Al. On the other hand, the effect of control gates A4, A5 and A6 on the conduction of the bottom SET is very weak (as shown in fig. 6.14).

In conclusion, while some of the Al control gates have a strong effect on the source-drain current of the SET and can be used successfully to pinch of the channel's conduction the yield of having

effective Al control gates is very low, this is especially troublesome for structures with many Al control gates as it means that we cannot successfully form and define the designed quantum dots.

To further investigate the discontinuity problem in the Al control gates, a test structure that includes two Al metal gates each with two contact pads on both sides of the nanowire has been fabricated; the purpose of this structure is to directly check if there is any metal breakage between the two contact pads of each Al gate, an SEM image of this structure is shown below:

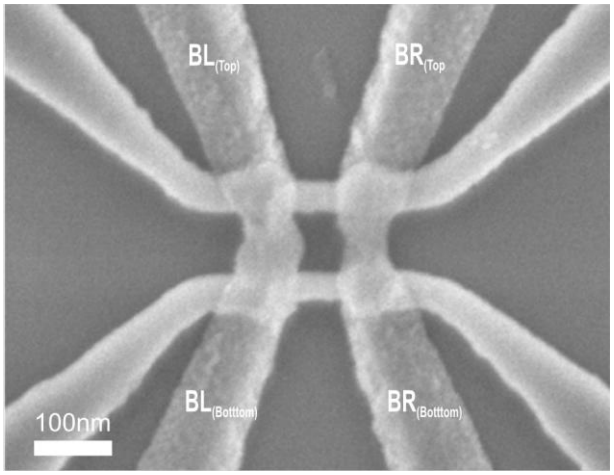


Fig. 6.13: SEM image of a shared metal barrier structure. Each metal line has a contact pad on both sides on the SOI NWs.

This structure has been tested at 4.2 K with the source drain current of both SOI nanowire channels recorded as a function of the voltage applied to the Al metal shared barriers and the top gate. Fig. 6.16 show the source drain current as a function of the voltage applied to Al barrier gates for the top (left image) and bottom (right image) SOI NWs.

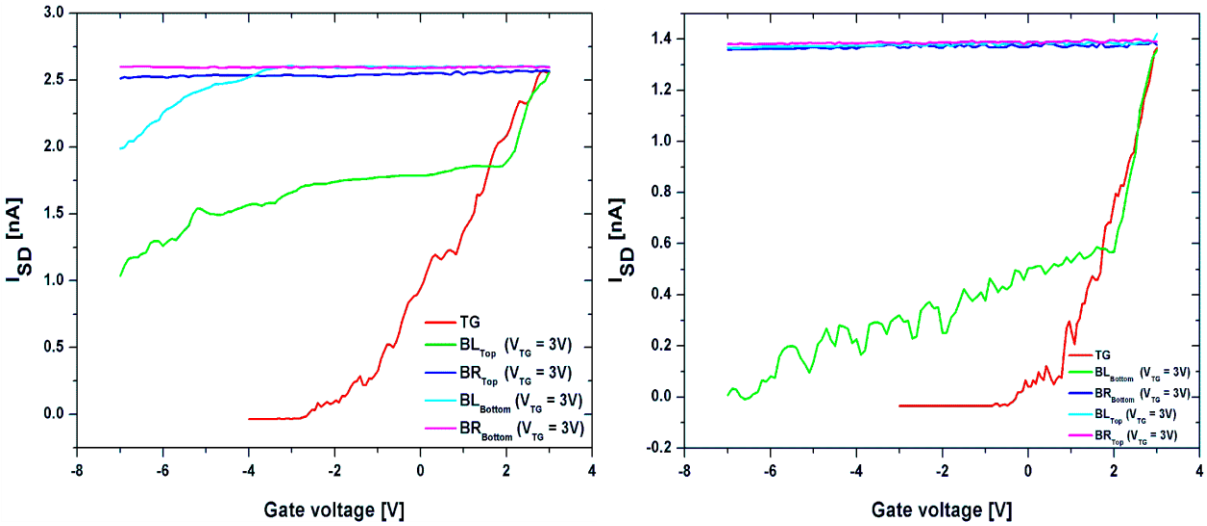


Fig. 6.14: Source drain current of the top (left) and bottom (right) SET as a function of the top gate voltage (with all gates grounded), and the Al barrier gates with a top gate voltage of 3 V at 4.2 K with a source drain voltage of 1 mV. BL and BR are further defined as top and bottom due to the electrical discontinuity of the metal lines.

From fig. 6.14, both Al barrier gates seem to be disconnected and therefore can be considered as BL_{Top}, BL_{Bottom}, BR_{Top} and BR_{Bottom}. The right barrier (BR) appears to be completely disconnected on both sides of the NW channels as it has no effect on the conduction of either channel and no measureable current can be measured between both sides of the barrier. The left barrier is also somewhat disconnected as the resistance between the top and bottom contact pads is measured as 70 MΩ, the discontinuity in the left barrier is close to the top channel due to the fact that the BL_{Bottom} does manage to pinch off the bottom NW channel and it also has an effect on the conduction of the top NW channel. BL_{Top} on the other hand has some effect on the conduction of the top channel but no effect of the bottom channel indicating a break closer to the top channel.

In conclusion, the first batch of fabricated devices was characterized to determine the best operation regime for the top gate, Si side gates and Al barrier grates. The metal top gates demonstrated good effect on forming the carrier inversion layer and controlling the 2DEG uniformity in the SOI NW channel. The Si side gates have also demonstrated good control on the channel's conduction, proving that they can be used to fine tune the potential of the defined quantum dots. The Al control gates are in principle capable of forming potential barrier and forming quantum dots in the Si NW layer as demonstrated for the double quantum dot SET (structure with 3 Al barrier gates) and for some of the single quantum dot SETs with a single quantum dot charge sensor (structure with 4 Al control gates). However, the yield in finding effective Al control gates is quite poor (between 10% to15%), this problem is more significant with more complicated structures like double quantum dot SET with double quantum dot charge sensor (structure with 6 Al barrier gates).

Few researchers have investigated the behaviour of wrap around metal gates at this scale. Most recently, Gonzalez-Zalba et. al. discussed the operation of an Al gated SOI etch nanowire in heavily doped Silicon. Out of 15 Al barriers they tested, only 5 barriers demonstrated low resistance as proof of electrical continuity, the other 10 gates were electrically disconnected. By biasing both sides of the metal barrier gates with contact pads included on both sides of the NW, originally included to test the continuity of the Al gates, they managed to pinch of the current in the NW channel and effectively use theses broken gates as potential barriers. They concluded by proposing that the Al metal used for theses gates to be deposited with sputtering rather than evaporation, and also to consider using other metals with lower thermal expansion coefficients like Titanium or Tungsten as the difference in thermal expansion coefficients between Si and Al through the thermal budget of the fabrication and measurements can have a severe impact on the continuity of the metal gates [105].
To address this Al continuity challenge, a number of possible solutions are considered and investigated. Some of these are based on modifications to the metal gates layer and some are modifications to the SOI NW layer as shown below.

Possible modifications to the metal layer:

- To use Al side gates instead of the current tri-gate structure by slightly moving the current Al gates layout away from the NW channel.
- To sputter Al instead of electron beam evaporation. This can help by improving the side wall coverage but would make lift off very challenging.
- To use different metals for the gate material, possible metals that can be evaporated in our cleanroom are Au, Ag, Ti, Cr, Ni and Al. Ni and Cr are both magnetic materials and Ag is very brittle material, therefore possible metals that can be investigated are Ti and Au.

Possible modifications to the SOI NW layer:

- To use a thinner SOI substrate. To use a 25 nm or 20 nm thick SOI substrate to reduce the SOI NW step height.
- To change the side wall profile of the SOI NW by introducing PECVD SiO2 spaces to reduce the slope of the SOI NW.
- To change the side wall profile of the SOI NW with anisotropic wet silicon etching (crystal orientation dependant) or by modifying the RIE process to produce a similar effect (less farmable due to the plasma damage).

6.2 Second device generation with Al side gates

As discussed in the previous section, the yield of Al control gates wrapped around the SOI NWs is poor. One of the easiest possible ways to address this problem is to modify the design of the structure without changing any of the process parameters. This can be done by pulling the Al control gates away from the SOI NW by few tens of nanometres. This way the Al control gates are turned into very-close proximity side gates rather than Al tri-gates. SEM images of one of the Al and Si side gate devices is shown below, the structure on the right is designed as a single QD SET coupled to a single QD charge sensor, the structure on the left is designed as a double QD SET coupled to a double QD charge sensor.

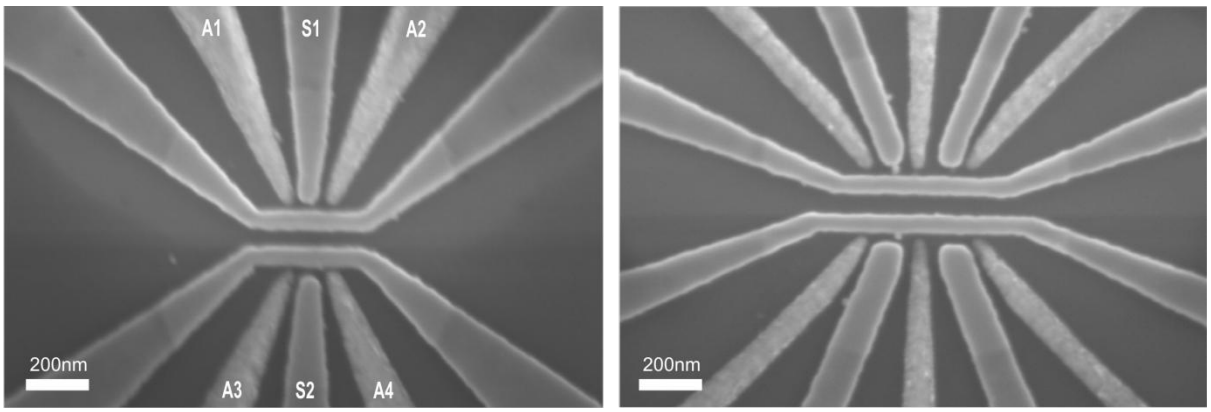


Fig. 6.15: SEM images of the single QD (left image) and double QD (right image) platforms using Al and Si side gates.

The single dot SET with single dot charge sensor showing in the SEM image above was characterized at 4.2 K. The source drain current of the bottom SET channels have been recorded as a function of the top gate, the Al side gates and the Si side gate (fig 6.16 below).

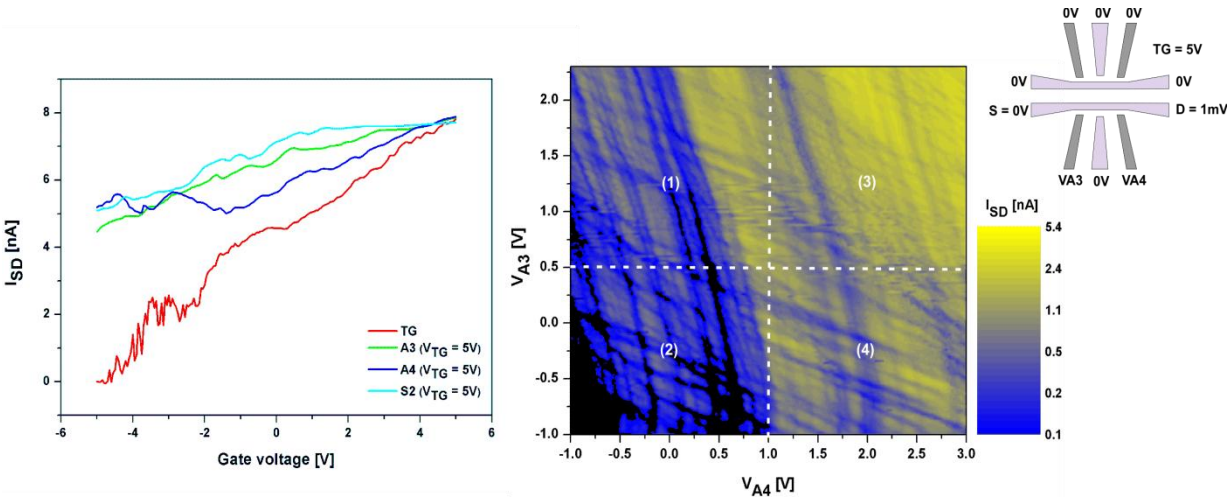


Fig. 6.16: Electrical characteristics of the bottom SET (left side of fig. 6.15) with source drain of 1 mV and top gate voltage of 5 V at 4 K. Left image: Source drain current of the bottom single QD SET as a function of the top gate (all other gates grounded), Si side gate and the Al side gates. Right image: source drain current of the bottom SET as a function of the voltage applied to Al side gates.

As can be seen from the channel conductivity plot for the bottom SET channel, the Al side gates have a stronger effect than the "broken" Al barrier shown in the previous section. In fact, these Al gates have a similar but slightly stronger effect than the Si side gates.

The success of the new Al metal gates can only be verified by their effectiveness in forming tunable potential barriers in the NW channel. Unfortunately, these metal side gates are most effective below top gate voltages of 2 V, below this value they can be used to pinch off the channel effectively switching from transparent to opaque barriers. However, at these top gates values the 2DEG in the SOI is not homogenous with a large amount of irregularities. At higher top gate values (above 2 V), the 2DEG is properly formed but the effect of the Al side gate is reduced to a degree where it is not possible to form Coulomb diamonds or precisely control any Coulomb oscillations. This can be seen in the contour conductivity plot (fig. 6.19) of the source drain current of the bottom SET channel as a function of the voltage applied to the Al side gates.

Nevertheless, the source drain contour plot of the bottom SET shows interesting double quantum dot characteristics. Unfortunately this measurement was made with a rough voltage sweep of 20mV; this makes it difficult to extract any coupling capacitance values directly from the plot as triple points cannot be observed with 20mV resolution. One alternative to explore these characteristics further is with single electron simulations; therefore an equivalent circuit model (fig. 6.17) is created based on known structural parameters of the device. The resistance and capacitance values of the tunnel junctions (T1, and T3) are set to 500KΩ and 0.8aF ,respectively, based on previous simulation models of the SISSQIT platform and similar simulation models from literature [106], [107].

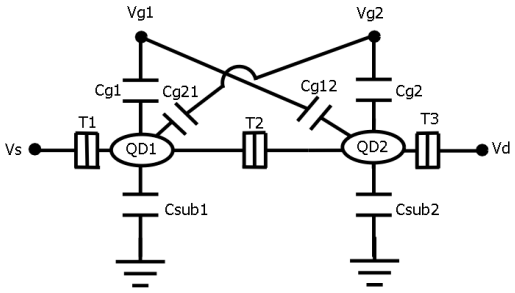


Fig. 6.17: Equivalent circuit model of the bottom SET of fig. 6.15 (left image).

The coupling capacitance (Cg1 and Cg2) between gates A3, A4 and the SET QD1, QD2 (the QDs positions in the simulations are the same as the one shown in the equivalent circuit of fig. 6.17) are set to 3.7aF based on COMSOL FEM capacitance simulations of the structure. Cross coupling capacitances (Cg12 and Cg21) between gates A3, A4 and QD2, QD1 were also extracted from the FEM simulations to be 2.1aF. Other capacitance values including top gate coupling capacitance, substrate coupling capacitance and Si side gate (S2) coupling capacitances were all extracted and included in the single electron circuit model but not shown in the equivalent circuit model of fig. 6.17 for clarity. The single electron simulations were conducted with a source drain voltage of 1mV with a 5V top gate voltage at 4.2K. The main component of the single electron simulation is the coupling capacitance between the two QDs, a number of values have been simulated and the value that most accurately replicates the measurement results (in regards to current magnitude and conduction line patterns) of fig. 6.16 is 2.5aF with a tunnel resistance of 500KΩ. Restrictions to this simulation approach include the fact that the tunnel junction values are based on previous modelling work and similar models from the literature. The second factor is the actual effect of the Si side gate S2 in the measurement; although it is grounded during low temperature measurements it is likely that this gate has a direct effect on the channel conductance through edge or defect states, unfortunately these effects cannot be accounted for in the simulation model.

Region 1 (in fig. 6.16 and 6.18) shows a dominant effect of QD1 on the SET conduction due to the relatively large positive voltage applied to gate A3 (0.5V to 2.5V) while gate A4 has a small effect (voltage applied to A4 is -1V to 1V). The simulation result for this region is similar to the measurements outcome with similar current magnitude and increment in the current magnitude. Region 2 (in fig. 6.16 and 6.18) shows a high barrier effect from both metal gates (A3 and A4), this region is a high resistance and low current regime due to the relatively small voltage values (-1V to 1V) applied to gates A3 and A4. The single electron simulations present a close match of the measurement's conduction characteristics in this region.

Region 3 (in fig. 6.16 and 6.18) has relatively large positive voltage values applied to both gates A3 and A4 (1V to 2.5V) allowing the definition of both QDs in the channel. The conduction lines shown in both the measurement and simulation reflect the presence of a strongly coupled quantum dots

regime due to large interdot coupling capacitance (T2 coupling capacitance) between the two quantum dots (QD1 and QD2), in this strong coupling regime the two QDs behave like a single dot [108]. Region 4 of fig. 6.16 demonstrates a dominant effect from QD2 on the channel conduction due to the relatively large voltage values applied to gate A4 (1V to 3V) and the weak effect of gate A3 (-1V to 1V). However, in addition to this dominant single dot behaviour (QD2) in this region, between V_{A4} of 2.5V and 3V in fig. 6.16 a clear double quantum dot anticrossing signature can be observed. The fact that these anticrossing characteristics are only observed around a high positive A4 gate voltage and not observed anywhere else in region 4 indicates that the second quantum dot is an accidental small (smaller than QD2) quantum dot coupled to QD2 to the right hand side of QD2 (as these characteristics are not present in region 3), this is further verified by region 4 simulation (fig. 6.18) that have been modified to include a small QD coupled to the right hand side of QD2, these simulation characteristics match the measurement anticrossing pattern and magnitude. The mechanism behind the formation of this third accidental QD is unclear, since the device layout is symmetrical, it is most likely due to line edge roughens associated with the dry etch definition of the SOI NW channel.

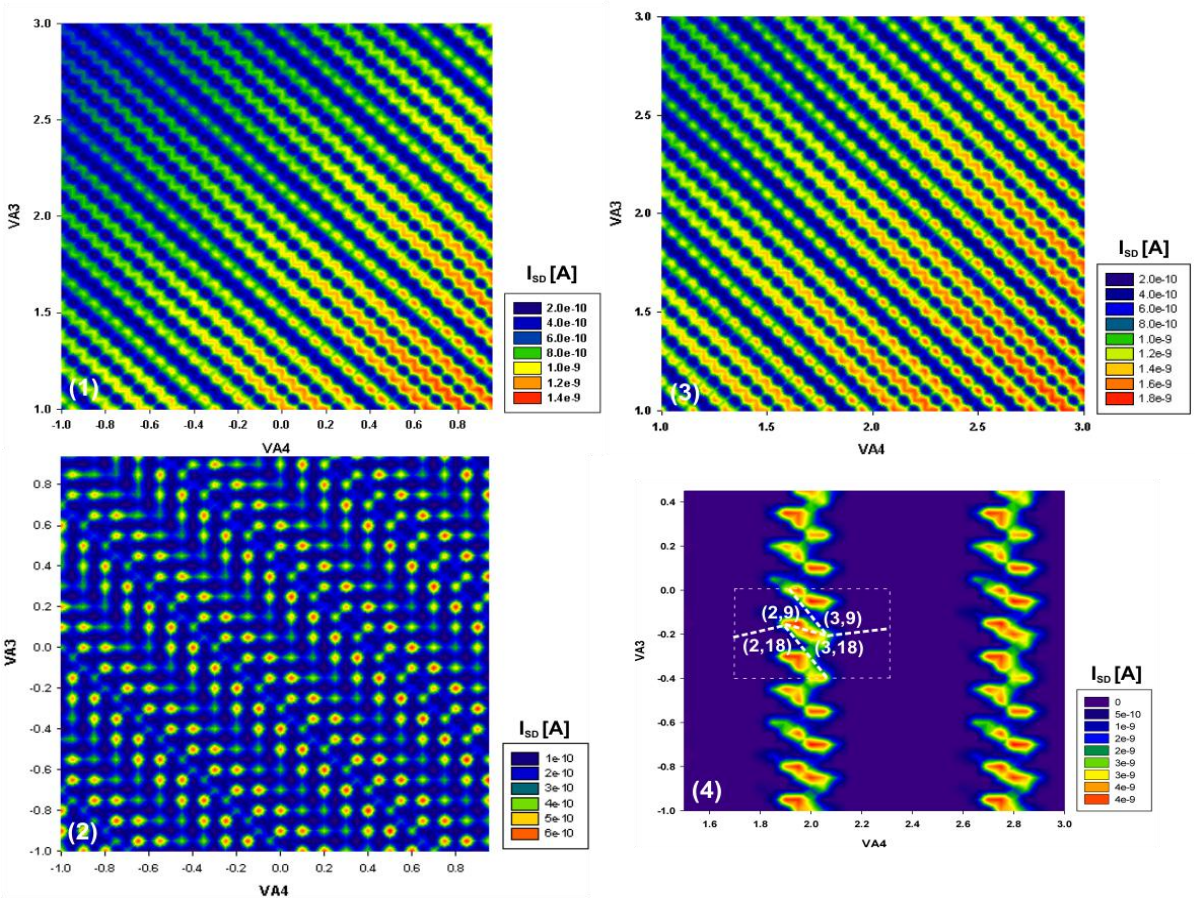


Fig. 6.18: Single electron simulations of the bottom left SET of fig. 6.15, the numbered regions correspond to the regions of fig. 6.16, numbers in the brackets of the bottom right figure (region 4) correspond to the number of electrons in the accidental QD and QD1 respectively.

6.3 Third device generation with Au FinSET barrier gates

One of the other possible ways to solve the metal gates continuity problem is to deposit the Al for the control gates by sputtering rather than electron beam evaporation. Sputtering improves the metal side wall coverage of the SOI NW, however this same property leads to coverage of the resist side wall making the lift off process very challenging at this scale. This process has been attempted but unfortunately most of the fine feature structures were not defined properly. This method has demonstrated successful lift off definition only for patterns with 1 µm dimensions or larger.

Therefore, sputtering has proven unsuitable for lift off purposes of fine structures. One other possible modification to the metal gate layer is to replace Al with other evaporated metals. The possible metals that can be evaporated in our cleanroom include Au, Ag, Ti, Cr, Ni and Al. Ni and Cr are both magnetic materials making them disadvantageous for the proposed application of this device, Ag is a very brittle material and therefore the two possible replacements for the Al control gates are Ti and Au control gates.

Au on its own is a soft material that doesn't adhere well to silicon or silicon oxide; therefore it is common practise to use Ti as an adhesion layer for Au. Using Ti on its own as a gate material is also not practical as wire bonding to a Ti bond pad would be very challenging.

Both Ti and Au have small grains, as observed by cross section and top layer SEM inspection, this fact is also reflected by the minimum stable evaporation rate that can be achieved for Ti and Au of 0.1 A/s in comparison to a minimum achievable stable evaporation rate of 0.5 A/s for Al. A number of test samples have been processed to determine what suitable Ti and Au thickness required to from the Ti/Au gate layer. Lift off for a number of samples with Ti thickness of 20 nm or more has proven challenging. Therefore, Ti thickness is set to 10 nm to provide sufficient adhesion for the gold layer and the Au thickness is set to 90 nm to make lift off process as reliable and repeatable as possible. Below are SEM images of some of the device structures realized using Ti/Au control gates.

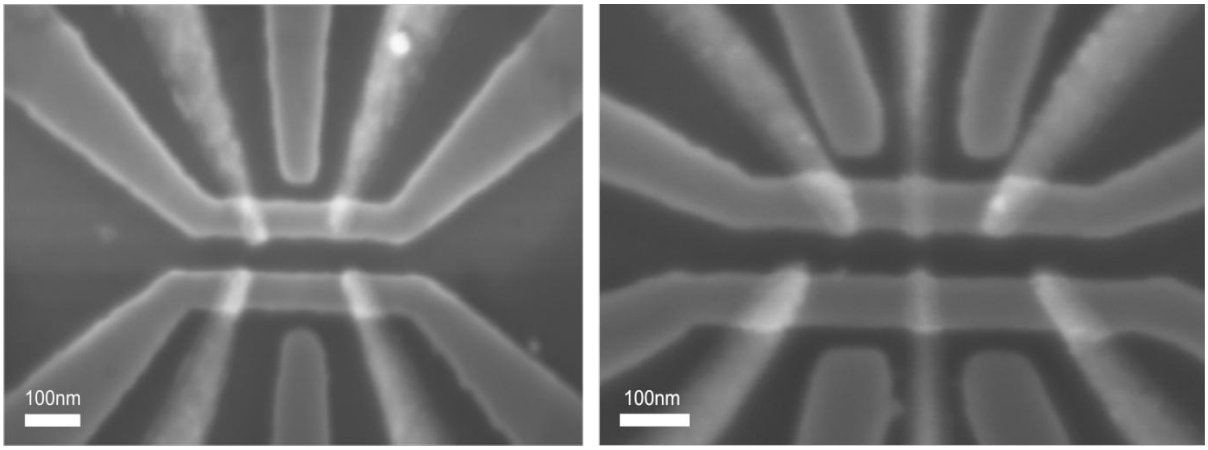


Fig. 6.19: SEM images of the single QD (left image) and double QD (right image) platforms using Au FinSET gates and Si side gates.

In addition to all the standard device structures, 24 shared Ti/Au barrier structures (50 nm wide and similar to the one shown in fig. 6.13 each with 2 shared barrier gates) were included to examine the yield of connected Ti/Au gates that wrap around the SOI NW.

After room temperature electrical characterization, only 20 gates out of the 48 shared barrier gates demonstrated electrical continuity on both sides of the SOI NWs, these 20 Au gates measured a resistance of 4.5 KΩ between the contact pads, the rest of the gates showed resistance levels of 5 GΩ indicating a breakage in these gate. This translates to an effective control gates yield of 40%, and this is an improvement to the Al gates yield of 12.5%. However, this yield is still too low when it comes to testing any structure with four metal gates or more, bearing in mind that a four metal gate structure is the minimum number of gates required to form a single electron transfer device coupled to a charge sensor.

With this last experiment to modify the metal gates layer, it is clear that the metal breakage at the edges of the nanowires is due to properties related to the metal as demonstrated by the higher yield of connected Au gates compared to Al connected gates. This is mostly likely be due to the smaller grain and therefore better Au layer side wall coverage of the SOI NW compared to the Al side wall coverage. Although there has been some improvement to the control gates yield by using Au, this is still not sufficient to meet the desired operation of the designed quantum dots and charge sensors.

6.4 Fourth device generation with Al FinSET barrier gates and SiO2 spacers

Modifications to the metal gate layer has proven to improve the yield of effective control gates, however the yield is still relatively poor to accomplish the desired operation of the single electron

transfer structures. In this section, process modifications to the SOI NW layer are introduced. These include reducing the SOI thickness to 25 nm (instead of 30 nm previous used) and to include SiO2 spacers to both sides of the SOI NW to improve the side wall coverage of the metal FinSET gates. Oxide and nitride spacers have been commonly used to fabricate a number of MOSFET structures and devices by utilizing the anisotropic etching properties of uniformly deposited films over a step like structure [109], [110]. A schematic of the metal gate on top of the SiO2 spacers is shown below.

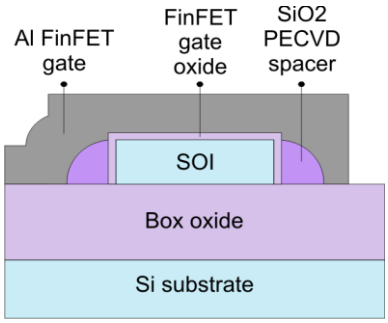


Fig. 6.20: Schematic cross section, perpendicular to the SOI NW, showing the proposed SiO2 spacers on both sides of the SOI NW.

The single electron transfer devices with spacers are fabricated following the same process outline as the main devices, however there are a number of additional steps to deposit and pattern the oxide spacers: after the RIE definition of the SOI device layer, the resist is removed and the device is oxidized in a 950 C dry environment to form an oxide layer of 10 nm to serve as the FinSET gates oxide. After the thermal oxidation step, SiO2 to from the spacers is deposited using PECVD. The SOI step underneath the metal gates is approximately 45 nm after the RIE and dry oxidation steps, therefore the thickness of the PECVD SiO2 layer required to form the spacers is investigated with two different samples: one as 50 nm and the second as 200 nm.

After the PECVD deposition, RIE is used to etch back the 50 nm /200 nm PECVD oxide. Once all of the deposited PECVD has been etched, a diluted BHF solution is set up and characterized to remove 1 – 2 nm of the PECVD spacers precisely to clear as much as possible of the RIE plasma damage to the spacers oxide layer. Finally after the diluted BHF clean, the structure is oxidized for a second time at 950 C for 1 minute to improve the density of the PECVD SiO2 layer and to help further passivate the spacers layer.

Shared Al barrier test structure were fabricated using this SiO2 spacers process on two samples as shown below, one with 50 nm starting PECVD spacers thickness and the second with 200 nm starting PECVD spacers thickness.

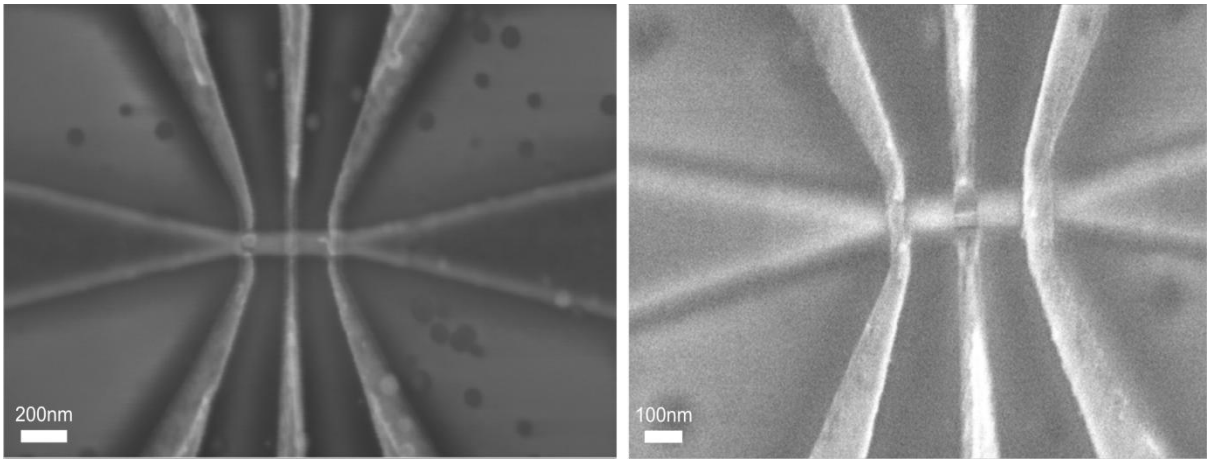


Fig. 6.21: SEM images of shared barrier test structures employing PECVD oxide spacers, the image on the left is for a starting spacer oxide thickness of 50 nm and the image on the right is for a starting spacer oxide thickness of 200 nm. The Al gates are 40 nm, 50 nm and 60 nm wide from left to right.

Room temperature resistance measurements were then preformed on these shared barrier structures to determine if they are continuous and connected on both sides of the SOI NW. For the 200 nm thick deposited SiO2 spacer layer: 72 gates (50 nm wide) in total were tested, 50 of these gates showed electrical continuity with a an average resistance value of 4.5 KΩ, the other gates in this sample showed resistance values in the GΩ range indicating a breakage in the metal line. The 50 nm thick deposited SiO2 spacer sample was also tested: Out of 72 gates tested, only 8 shared barrier gates demonstrated a resistance of 4.5 KΩ with all the other gates indicating a breakage in the metal line with a resistance in the GΩ range.

To understand this large variation between the 50 nm thick deposited SiO2 spacer layer and the 200 nm thick deposited layer, two cross section samples were prepared using the same process conditions as the devices that were electrically tested. Cross section images of SOI NWs covered with a 100 nm Al FinSET gate on top of a 50 nm thick deposited spacer layer are shown on the left, the SEM images on the right are for cross section of a structure with 200 nm thick deposited spacer layer.

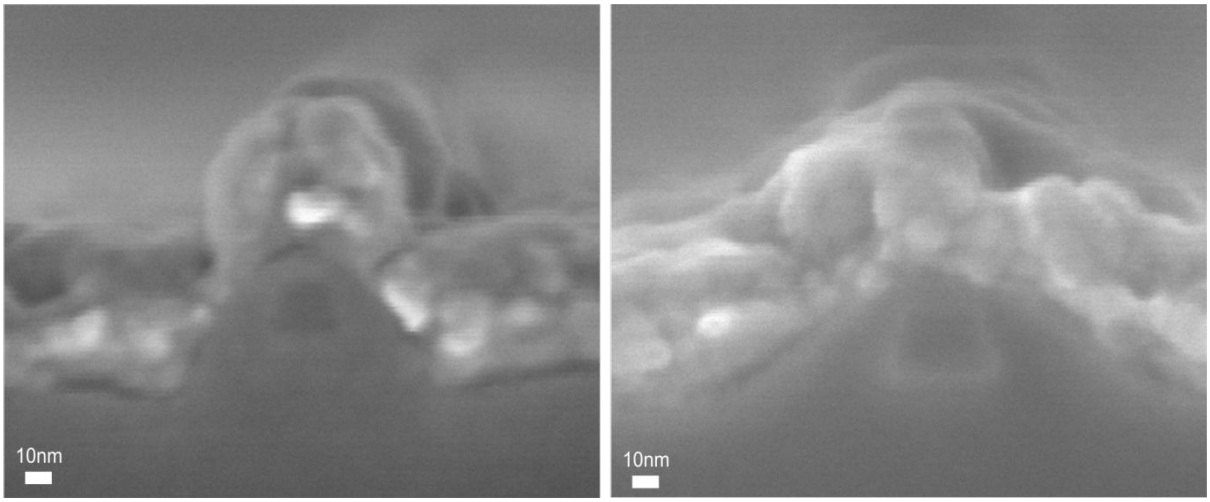


Fig. 6.22: Cross section SEM of a 50 nm SOI NW (perpendicular to the NW) with PECVD oxide spacers and Al FinSET gates. Left image is for a spacer starting oxide thickness of 50 nm and the image on the right is for a spacer starting oxide thickness of 200 nm. Al is the top layer in bright grey, oxide layer is directly underneath the Al and the Si part is the dark grey polygon area in the centre.

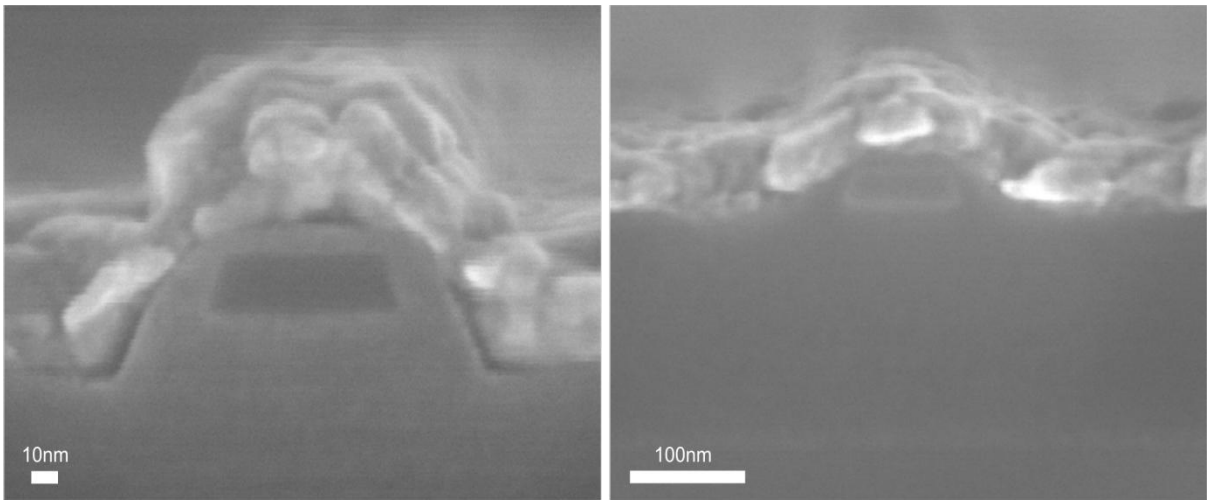


Fig. 6.23: Cross section SEM of a 100 nm SOI NW (perpendicular to the NW) with PECVD oxide spacers and Al FinSET gates. Left image is for a spacer starting oxide thickness of 50 nm and the image on the right is for a spacer starting oxide thickness of 200 nm. Al is the top layer in bright grey, oxide layer is directly underneath the Al and the Si part is the dark grey polygon area in the centre.

The two samples (50 nm deposited spacer and 200 nm deposited spacers) were both processed in parallel using the same process conditions; one with a 50 nm thick PECVD SiO2 deposited starting layer and the other with a 200 nm thick PECVD SiO2 deposited starting layer. The only other process variation between the two samples is a slight over etch (about 10 nm) into the box layer of the 50 nm

spacer sample compared to the 200 nm spacer sample as shown in the cross sectional SEM images above.

From the SEM images above, it is clear that the 200 nm SiO2 deposited layer provides a lower side wall slope; this dramatically improves the profile of the metal gates around the SOI NW and therefore must increase the probability of having a continuous metal connection over the NW compared to the 50 nm thick depicted oxide spacer layer. This can be further examined by measuring the slope angle of the SOI NW side walls, as shown in fig. 6.24 below. All of shared barrier gates that were conductive with resistance values close to 4 KΩ rest on an SOI NW with a side wall slope of 35 degrees or less. On the other hand, the shared barrier gates that proved to be discontinuous with GΩ resistance values rest on a side wall slope of 60 degrees or higher.

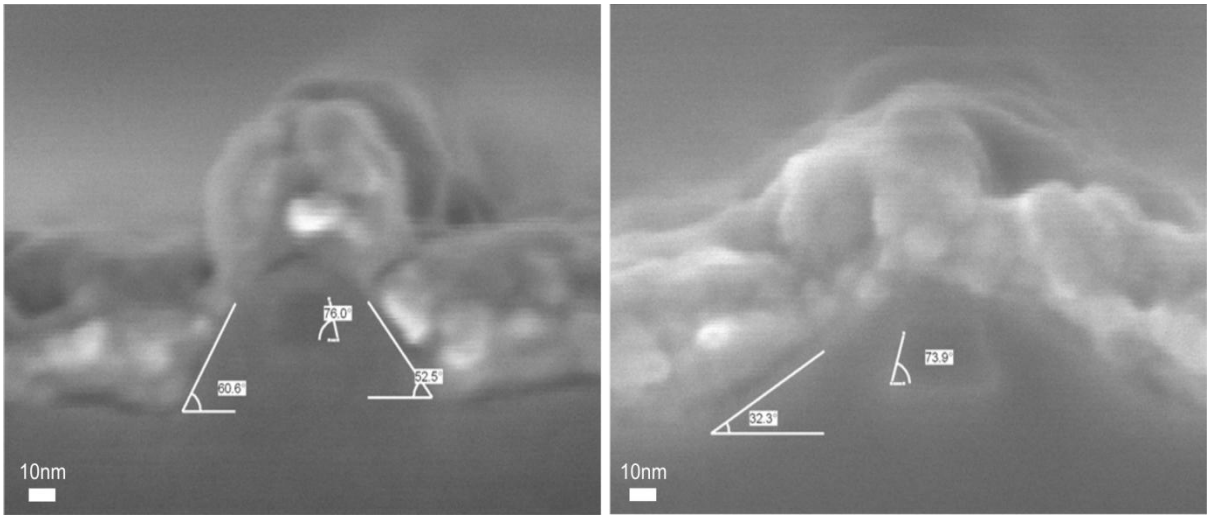


Fig. 6.24: Cross section SEM of a 50 nm SOI NW (perpendicular to the NW) with PECVD oxide spacers and Al FinSET gates showing the side wall slope of the SOI NW. Left image is for a spacer starting oxide thickness of 50 nm and the image on the right is for a spacer starting oxide thickness of 200 nm. Al is the top layer in bright grey, oxide layer is directly underneath the Al and the Si part is the dark grey polygon area in the centre.

In summary, using oxide spacers to fill the side walls of the SOI NW helps the metal coverage over the NW and produces continuous metal gates with no breakage. However, the thickness of the starting deposited PECVD layer thickness is very critical. Thicker PECVD layers provide more coverage at the side walls and produce a low sloped side wall after the anisotropic etch process. The minimum required PECVD deposition thickness to make this process successful is at least four times the thickness of the SOI NW step, the test structures investigated used a 200 nm PECVD layer thickness for an SOI NW step of 45 nm and produced a shared barrier gates yield of 70% while the test structure with 50 nm PECVD layer thickness for a similar SOI NW step of 45 nm demonstrated a continuous shared barrier yield of only 11%. It is expected that even thicker PECVD deposited layers

(250 nm or thicker) will provide an even better continuous shared barriers yield (higher than 70%); however this compromises the reliability and repeatability of the lift off pattern process required to define the metal control gates layer.

200 nm SiO2 spacers provide a good yield Al control gates yield and it is a successful process to reduce the slope of the NW side walls, however this thick layer has proven to severely affect the metal gates pattern definition, especially for structure with two channels facing each other, more PECVD oxide deposited fills more of the void between the two channels and causes the tips of the metal FinSET gates to break off at the edge. Without sacrificing the desired charge sensor sensitivity by pushing the two channels apart, a number of experiments have proven that it is difficult to have reliable lift off pattern definition with any PECVD spacer layer thickness above 50 nm. This point is very clear in the SEM images shown below, fig. 6.25 (right side) shows the standard single quantum dot transfer device and charge sensor and the left side image shows a double quantum dot transfer device and charge sensor, in both structures a 50 nm thick PECVD layer was deposited to from the side wall oxide spacers. On the other hand, fig. 6.26 shows the same structures with a 200 nm thick PECVD spacer's layer, this has a demonstrated a severe setback to the success of the lift off process making the 200 nm PECVD deposited spacer layer unsuitable for most of the desired structures in this project.

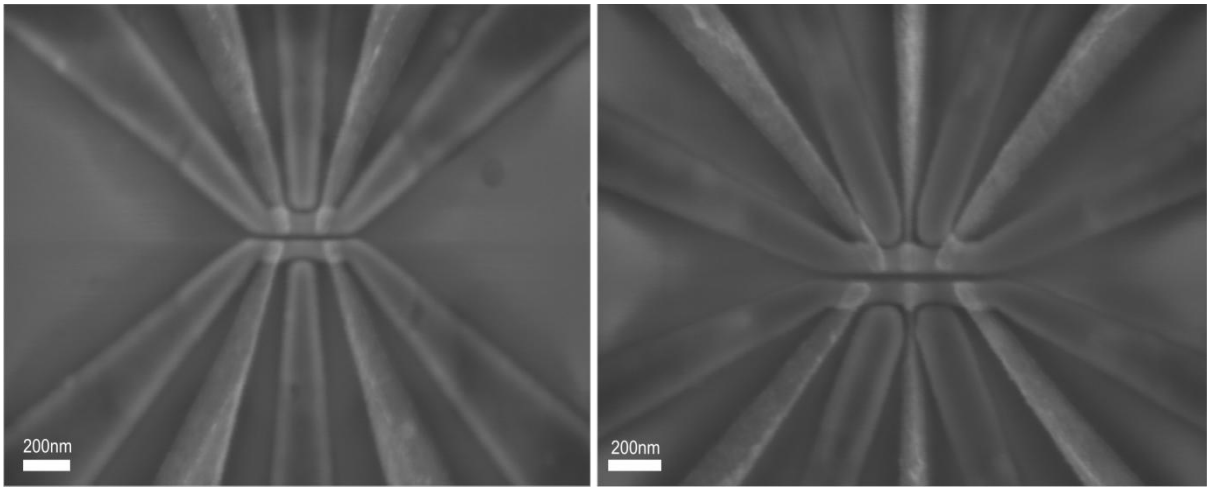


Fig. 6.25: SEM images of a single QD and a double QD single electron transfer and electrometer platforms utilizing Al FinSET gates and PECVD oxide spacers with a starting oxide thickness of 50 nm.

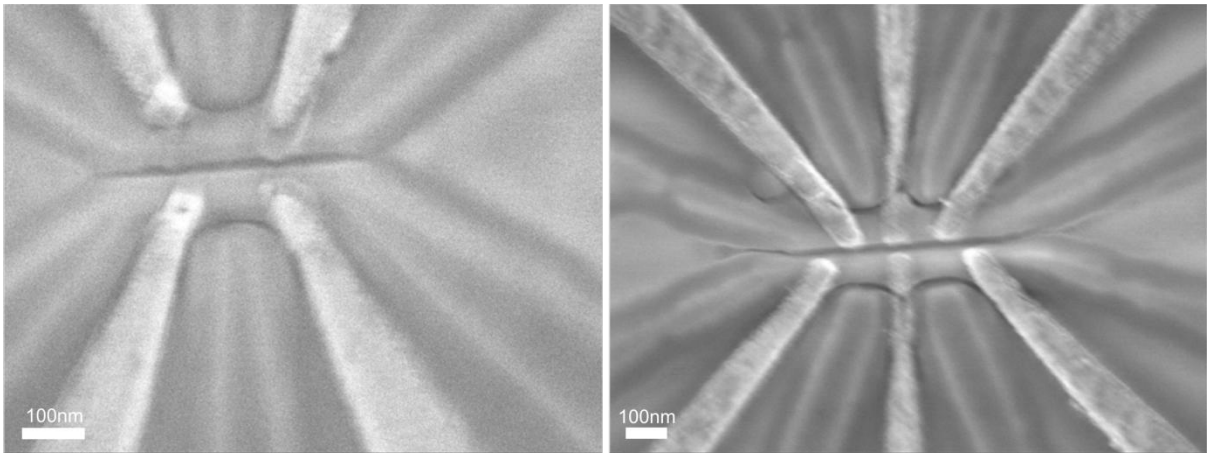


Fig. 6.26: SEM images of a single QD and a double QD single electron transfer and electrometer platforms utilizing Al FinSET gates and PECVD oxide spacers with a starting oxide thickness of 200 nm.

6.5 Fifth device generation with Al FinSET gates on atomically defined NW side walls

So far changing the profile of the SOI NW layer has proven to be more successful to produce continuous wrap around FinSET metal gates than any modifications to the metal gate layer itself.

Therefore, following on the same track of modifying the side wall profile of the SOI NW discussed in the previous section, in this section we discuss the use of a crystal-orientation dependant wet etch process to define the SOI NWs and expose the Si (111) plane on both sides of the NW. This process utilizes the atomically defined 54.74 degrees (the angle between the {100} and {111} family of planes) of an anisotropically etched Si NW to support the metal control gates continuity over the NWs [111].

The {111} family of planes represents the highest atom packing density of planes and is etched at a much slower rate than other planes, therefore sidewall profiles of (100) Si NW will always be defined by the (111) plane with the specific 54.74 degrees after a sufficient etch time [111]. In addition to the improved side wall profile, this process will improve the NW performance by eliminating line edge roughness and plasma damage to the surface of the NW that is commonly associated with reactive ion etching [112].

Tetramethyl Ammonium Hydroxide (TMAH) is commonly used as an anisotropic etch solution and is proposed here to define the SOI NW. TMAH offers excellent selectivity to silicon oxide of the BOX layer underneath the Si NW, the oxide etch selectivity is so significant (four order of magnitudes lower) that it is necessary to remove the thin native oxide (1-2 nm) of the SOI layer

before carrying out the TMAH etch process [111]. To define small Si structures in TMAH; it is necessary to use a solution concentration above 22 wt%, as lower concentration can result in considerable roughness on the etched surfaces. Temperature of the TMAH bath is directly related to the Si etch speed, where increasing the solution temperature increases the etch rate rapidly [111], [113].

A number of research groups have demonstrated Si nanoscale nanowires using TMAH anisotropic etching for applications including AFM nano-needles, biosensors and ultra-narrow channel MOSFETs. The fabrication of these structures mostly follow one of two methods: the first uses a positive resist profile to define the nanowire on top of a thermal oxide layer, the NW pattern is initially transferred to the thermal oxide layer with a wet HF etch and then finally transferred to the underlying Si with TMAH using the thermal oxide as the etch mask [114], [115]. This process can suffer from e-beam proximity effects and lead to distortion and reduction of the NW pattern dimensions due to the relatively large exposure areas on both side of the relatively small (50 nm or less) targeted NW width. In addition, the wet HF etch of the thermal oxide nanowire pattern is an isotropic process and can lead to further significant undercut of the nanowire mask reducing the size of the oxide nanowire mask and putting constraints on the smallest dimensions that can be defined for a single nanowire or on the minimum separation that can be achieved between two coupled nanowires.

The second most common fabrication method uses a negative resist profile to define the nanowire pattern on top of the Si layer directly or on top of a thermal oxide or a non-doped silicate glass (NSG) layer with RIE pattern transfer, and then utilizes the relatively-thick negative resist layer itself or the oxide/NSG layers respectively as the TMAH etch mask [116], [117]. This process offers more control over the final dimensions of the Si NW as the TMAH etch mask is either patterned via RIE for the case of oxide or with the original e-beam exposure in the case of the negative resist. However, with this process option, an HF wet etch step is needed right before the TMAH etch to remove any native oxide from the Si device layer.

6.5.1 TMAH mask definition

The width of the rectangular top plane (aligned to the <110> direction) of the Si NW B is defined by the etch depth t, the etch mask width A and the side wall slope of 54.74 degrees as shown below [111].

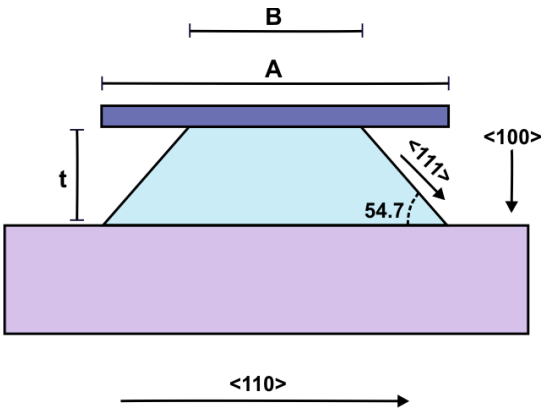


Fig. 6.27: A schematic showing the mask dimensions and orientation for TMAH Si etching

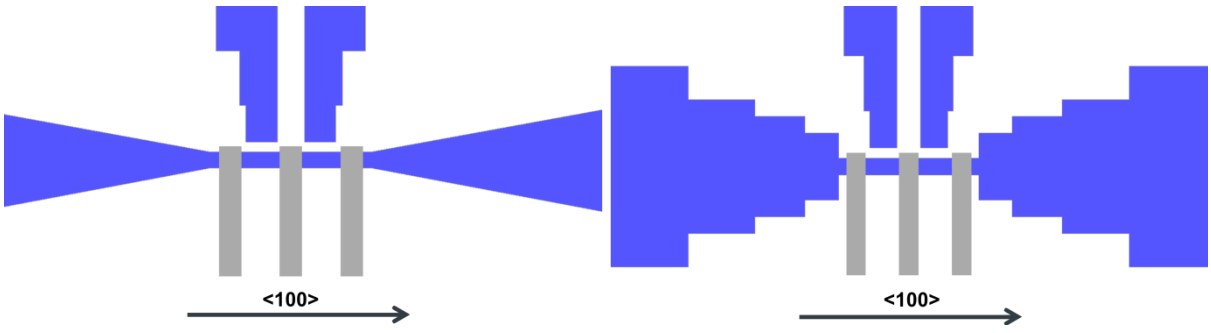
The width of the top nanowire mesa can be expressed as:

$$B = A - t \times \tan(54.7) \tag{6.1}$$

The etch depth of the SOI NW is the thickness of the top Si layer of the SOI stack. Therefore for an SOI substrate with top layer Si thickness of 25 nm: TMAH etch mask width A of 40, 50 and 60 nm will result in a top nanowire mesa width of 4.6, 14.6 and 24.6 nm respectively. This small NW top surface area in addition to the atomically defined side wall slope of 54.74 degrees can establish continuity for the metal gates over the SOI nanowires step.

6.5.2 Nanowires mask design

Due to the anisotropic nature of the TMAH etch process, the {100} planes will etch at a much faster rate than the {111}, therefore the NW etch mask must be precisely aligned to the <110> direction and it is essential that all the NW mask geometry follow a 0, 45 or 90 degrees with respect to the <110> direction so that the NW exposes the <111> direction along all its sides and edges and maintain the final Si NW shape and dimensions as defined by the etch mask. New nanowire layouts are designed to follow these new design rules; the new NW designs are show below:



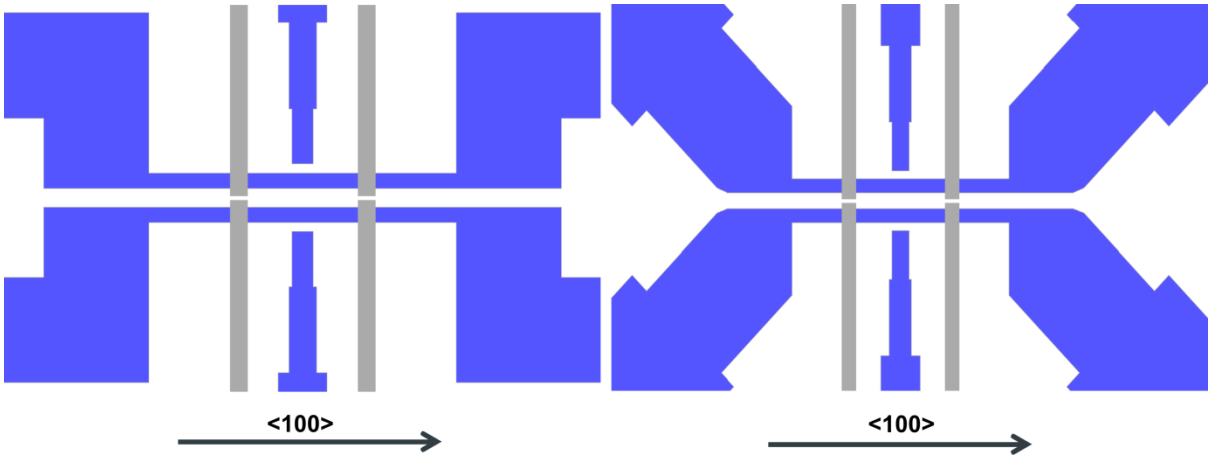


Fig. 6.28: Schematics showing the proposed NW designs for the Si TMAH process. All of these layouts have been designed to be parallel, 45 degrees or 90 degrees in relation to the <100> wafer flat.

6.5.3 Nanowires fabrication

The two possible fabrications methods include using a positive or a negative profile to define the NW TMAH etch mask. As previously discussed, the negative profile offers more control over the NWs mask definition, offers more flexibility in regards to integrating more complex Si layer designs and it is more compatible with the second metal layer (the metal gates would face a higher NW step with a positive NW profile definition).

Following the same initial process steps as previously described (fig. 5.11), the NWs in this process are fabricated on a 25 nm thick SOI substrate. The process starts with a 6 inch SOI wafers from Soitech with a 100 nm thick lightly boron-doped Si top layer ($\rho \sim 18\ \Omega$-cm at 300 K) and a 200 nm buried oxide layer. The 6 inch (100) SOI wafer is thinned down to 25 nm, after the thinning process deep etched alignment marks are defined using e-beam lithography followed by RIE pattern transfer to the top Si layer, the buried oxide layer and the Si substrate. The alignment marks pattern were aligned to the flat of the wafer as carefully as possible to ensure that the NW mask pattern in the next step are aligned as precisely as possible to the crystallographic <110> axes of the SOI wafer. E-beam lithography is used to define the NW patterns with HSQ, 2% HSQ is applied by spin coating and yields a layer thickness of approximately 30 nm that is used after e-beam patterning as the NWs etch mask for TMAH.

However, as mentioned earlier even native oxide layers o 1 – 2 nm can prevent TMAH from etching the Si. Therefore, any thin native oxide has to be removed directly before the TMAH etch process. For this purpose a special diluted buffered HF solution (1%) is prepared and carefully characterized to have an exact oxide etch rate of approximately 1.5 nm per minute (this etch rate was characterized

with dry thermal oxide samples). This 1% BHF is used immediately before the TMAH etch step to remove any native oxide present on the SOI surface. However, this raises another challenge: as previously mentioned HF is specifically used to strip HSQ with a very high removal rate. Regardless of the short etch time and small concentration of the 1% BHF; the native oxide removal step would also results in the complete removal of the HSQ patterns on the substrate.

A number of tests were performed using hot plate bakes, RTA and furnace anneals to harden the HSQ layer and increase it's etch resistance to 1% BHF. The HSQ layer has to be annealed to a sufficient temperature to drive any remaining hydrogen out of the Hydrogen Silsesquioxane (HSQ) layer to produce an SiO2 like layer with improved etch resistance [118]. However, this has to be carefully balanced so that minimal or no oxidation happens on the Si surface during the anneal process as this would increase the amount of oxide that needs to be removed prior to the TMAH etch and therefore increase the time that the HSQ patterns will spend in the 1% BHF solution. Out of the three different anneal methods, furnace anneal at 900 C in a nitrogen ambient has proven to be the most suitable method, it offers the highest 1% BHF etch resistance (6.5 nm per minute) and causes the smallest amount of additional Si oxidation (only an additional 0.9 nm to the native oxide thickness of 1 – 2 nm) due to the enhanced inert Nitrogen environment achieved inside the furnace tube.

After the e-beam lithography on HSQ, the sample is then annealed at 900 C for 1 minute in a nitrogen ambient furnace tube. The sample is then dipped in the customized 1 % BHF solution for 2 minutes to remove any oxide covering the SOI device layer, straight after the oxide removal the sample is immersed in a 50 C heated TMAH (25% wt) bath for 1 minute. After the TMAH etch step, the remaining HSQ resist is removed with a short dip (3 minutes) in the 1% BHF solution.

Figures 6.29, 6.30 and 6.31 below show SEM images of some of the SOI NW structures defined using the anisotropic TMAH etch process, it is clear from the images that the TMAH etch produces smooth side walls with minimal line edge roughness as defined by the (111) planes on all edges of the structures. In addition to the role of defining a (111) NW side wall profile to improve metal gate continuity over the NWs, the TMAH process provides a significantly lower density of surface and bulk trap states in the NWs when compared to the traditional RIE method of NWs definition, where RIE plasma damage commonly causes surface damage and shallow ion implants effectively forming trap states [119].

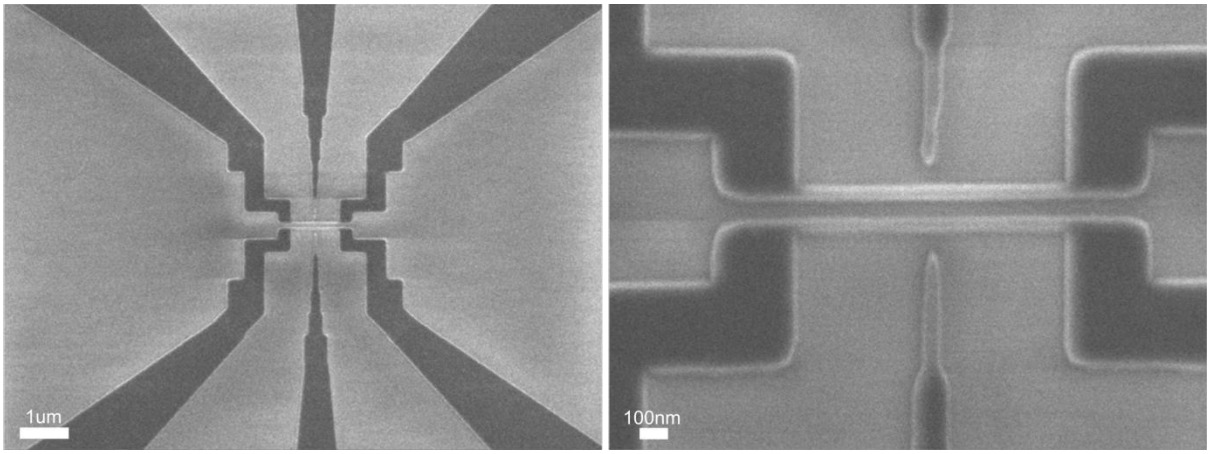


Fig. 6.29: SEM images of SOI NWs with Si side gates for a single QD single electron transfer and electrometer platform, defined with the TMAH wet etch process.

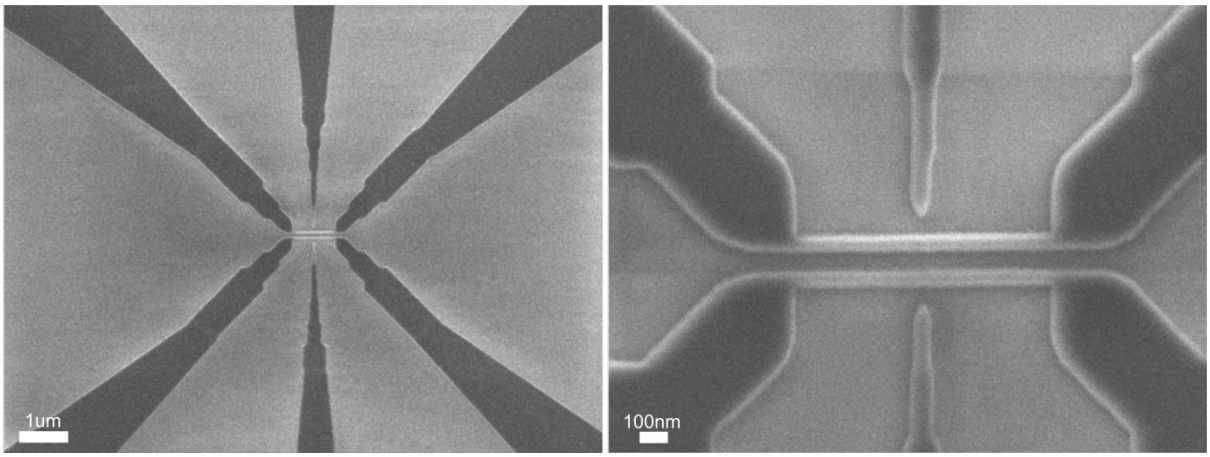


Fig. 6.30: SEM images of SOI NWs with Si side gates for a single QD single electron transfer and electrometer platform, defined with the TMAH wet etch process.

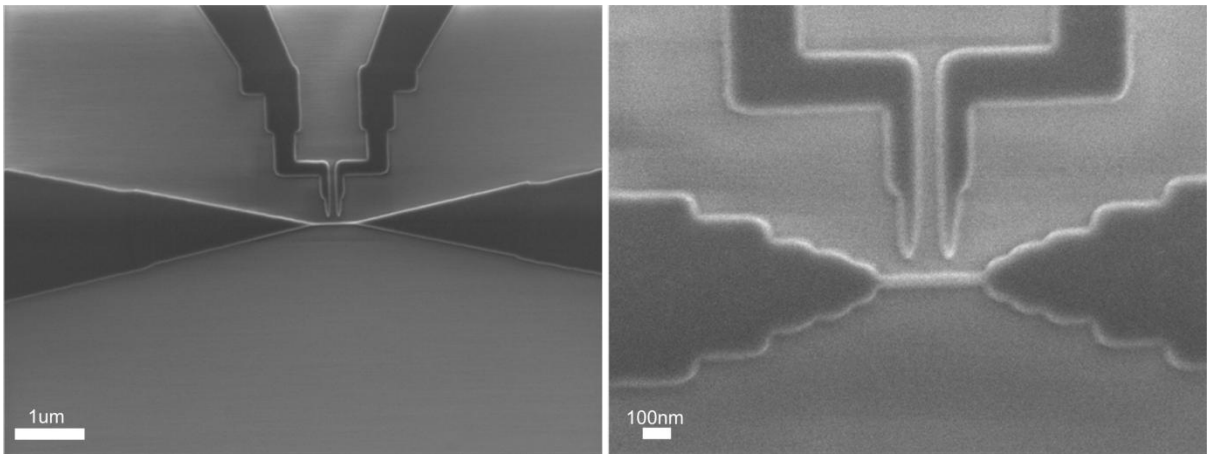


Fig. 6.31: SEM images of SOI NWs with Si side gates for a double QDs SET, defined with the TMAH wet etch process.

6.5.4 Shared Al barriers and metal coverage tests

A number of tests structures were fabricated to test the effect of the atomically defined (111) sidewall profile of the SOI NWs on the continuity of the metal gates around the wire. After HSQ resist removal, dry oxidation at 950 C for 3 minutes is carried out on the sample to form an approximately 10 nm gate oxide layer to simulate the same exact fabrication conditions that the real device structure undergoes before defining the metal control gates. E-beam lithography, 100 nm Al electron beam evaporation and lift off was then preformed to realize a shared Al gates structure, each Al gate is connected to two pads on both sides of the SOI NW to make it possible to measure the Al gate resistance over the SOI NW. Half of the test structures were for connected metal gates over one SOI NW and the other half was for gates going over two SOI NWs facing each other as shown in the SEM images below.

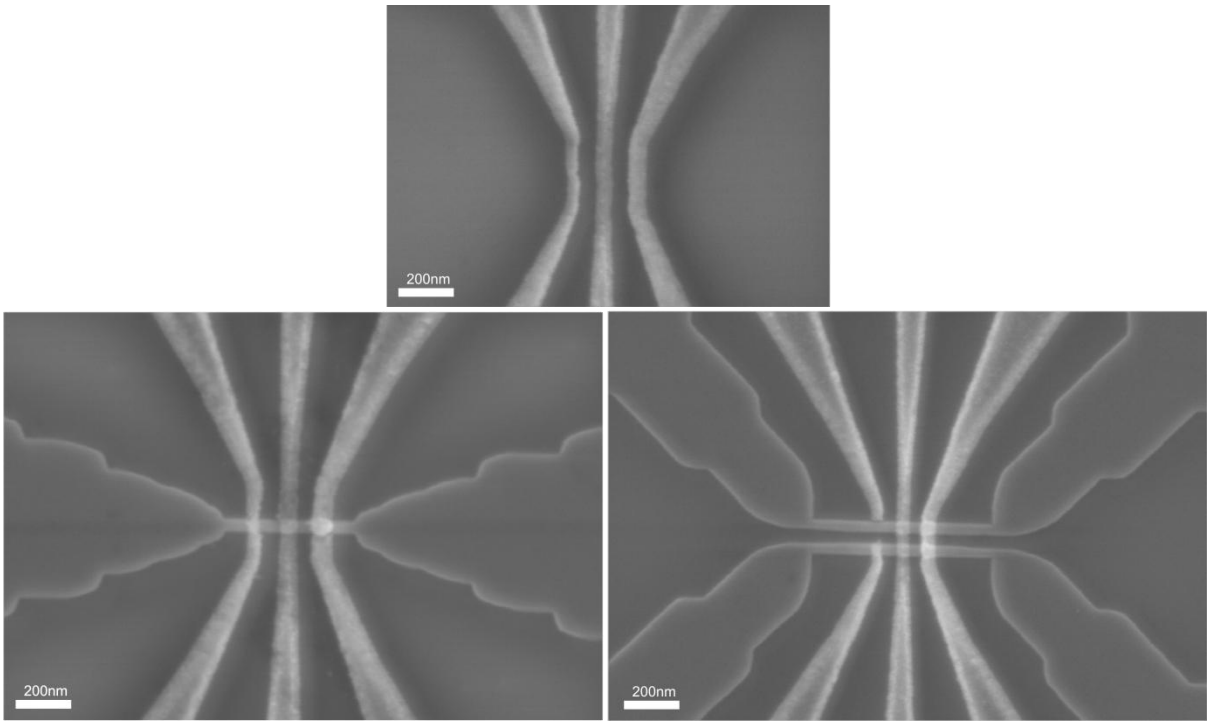


Fig. 6.32: SEM images of shared Al FinSET barrier test structures with the TMAH atomically defined NW side walls. The top image shows simple reference Al NWs, the left image is for Al gates over one SOI NW and the image on the right is for Al gates over two SOI NWs.

To determine the resistance of an Al continuous NW with the specific deposition process conditions at room temperature a number of simple reference Al NWs were defined on the buried oxide layer (top image in fig. 6.32) and measured at room temperature, the resistance of these reference wires is measured to be approximately 4.3 KΩ.

41 Al shared barrier gates, which are 50 nm wide, were measured at room temperature. The resistance of 38 of these gates is measured as 4.3 KΩ while the other 3 devices showed a resistance in the GΩ range. Half of the gates measured (21 gate) pass one SOI NW (as shown in the left image of Fig. 6.32) and the other half (20 gates) passes two SOI NWs (as shown in the right image of fig. 6.32). Therefore, the yield of continuous Al gates over TMAH defined SOI NWs is 92%:

This 92 % yield of continuous Al metal gates has not been previously possible, this wet orientation-dependent definition of the SOI NWs sidewall provides a successful solution to the metal continuity problem, it also indicate that it we can at last reliably realize effective Al FinSET gate structures over SOI NWs.

6.6 Summary

The first generation of these structures used Al FinSET style control gates to act as potential barriers and electrostatically define the desired quantum dot structures. The yield of effective Al FinSET control gates in this first generation of devices was poor (10% - 15%) especially in structures with four or more Al control gates. Further investigation into the weak effect of these Al FinSET gates has led to the conclusion that most of these Al gates are broken close to the SOI NW region and the main reason of this breakage is due to the sharp vertical sidewall profile of the SOI NW.

A number of design and process modifications to the metal control gates layer and the SOI NW layer are then proposed and investigated to solve this challenge. The second device generation utilized Al side gates to act as electrostatic potential barriers, this batch did not require any process alteration but simple changes to the design by putting the metal gates in close proximity to the NW (much close to the NW than the Si side gates) without having the gates cross over the SOI NW. The effect of these Al side gates was more effective than any of the broken FinSET Al gates but unfortunately, these metal side gates were not sufficient to pinch off the NW current completely off (the opaque tunnel barrier regime) and therefore were not successful in reaching the single electron regime.

One of the other suspected causes of the weak FinSET effect of the first device generation was the grain structure of the evaporated Al layer, the Al layer for the control gates was evaporated with the best possible process conditions: lowest evaporation rate possible 0.5 A/s, highest vacuum levels possible, sufficient sample cleaning prior to evaporation and very short time delay between e-beam lithography and evaporation. Nevertheless, under SEM inspection the deposited Al layer shows a grainy cross section and poor layer coverage at the edge of the NW. The last process modification to the metal control gates layer is to examine a different metal, a metal that has a relatively smaller grain size and hence provide better layer coverage at the edge of the SOI layer. Au was investigated as the

replacement metal, this process modification has improved the effective control gates yield to 40% which is an improvement on the Al FinSET gates yield but is still considered as a low device yield.

The fourth device generation tested medications to the SOI NW layer rather than the metal layer itself, here an SiO2 spacers process was developed to include spacers at both corners of the SOI NWs effectively reducing the side wall slope of the NW so that the metal layer rests on a relatively flat surface without any sharp vertical edges. This process improved the Al metal control gates yield significantly, however this came at the cost of the reliability and repeatability of the control gates lift off definition due to the relatively thick (200 nm) starting SiO2 spacers layer required to achieve Al FinSET gates continuity of yield of 70% and higher.

The SiO2 spacers process demonstrated direct relation between the angel of the SOI NW side wall and the continuity of metal gates over the NW steps. In other words, it provided information about the exact NW side wall slope angle that prevents the FinSET metal gates from breaking. These finding are therefore are employed to develop an orientation dependant Si wet etch process to atomically define an angel of 54.74 degrees at the NW side walls. By demonstrating a metal gates yield of 92%, this fifth generation process successfully solves, for the first time, the technology challenge relating to the metal FinSET gates over the SOI NW. Due to the anisotropic nature of this wet etch process, the SOI NW fabricated with this process has almost no line edge roughness and is completely free from all types of plasma damage that is typical to RIE defined NWs. Fig. 6.33 below shows an approximate time scale of the fabrication and characterization stages for each of the five device generations; it reflects the amount of time and effort dedicated to realize the Al FinSET single electron devices.

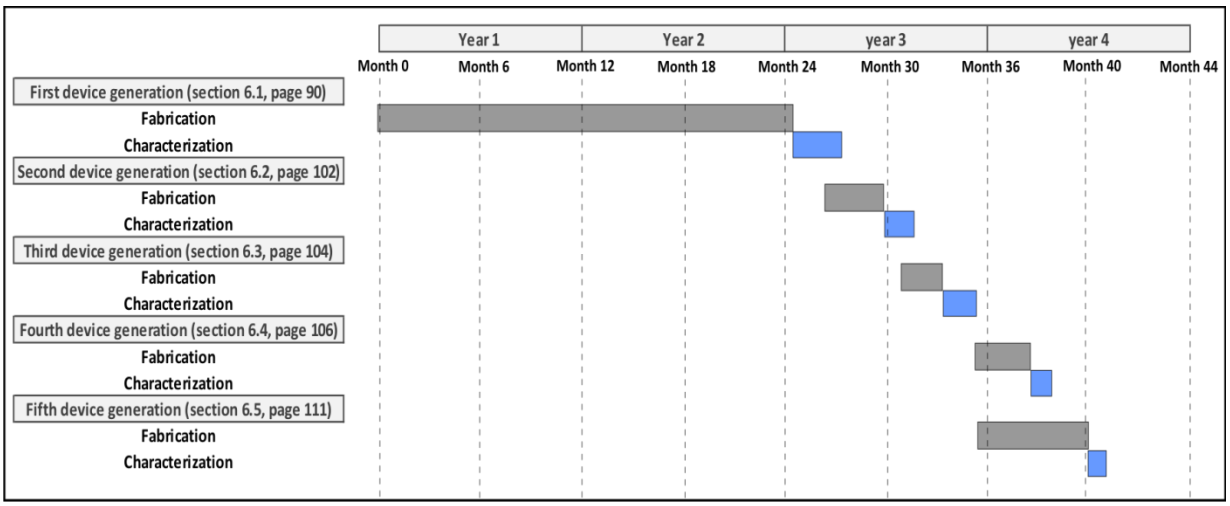


Fig. 6.33: Gantt chart of the fabrication and characterization stages of the FinSET single electron devices.

Chapter 7

Conclusions

7.1 Project Summary

The work presented here is part of an integrated system (SISSQIT) with aims to provide a practical platform for spin qubit applications by integrating key components in one compact silicon platform, featuring excellent versatility, scalability and compatibility with conventional VLSI technology**.** This is the minimum necessary system to demonstrate the full operation of double spin qubits but can be scaled-up in a straightforward way to large scale systems in the future.

The scope of this report covers the design, simulation and fabrication of the main building blocks of the SISSQIT platform: A single electron transfer (turnstile) device integrated with a charge sensor. Structural design and analysis of the structure was carried out using 3D finite element method capacitance simulation, and dynamical analysis of single electron transfer operation through the single electron transfer device (SETD) was demonstrated using Monte Carlo based single electron circuit simulation. The single electron transfer approach constitutes a novel approach for single electron operation, as it combines a modified electron injection technique previously demonstrated for memory write operations together with a pure single electron turnstile operation.

A novel fabrication process for the single electron transfer device with the electrometer with Al FinSET gates and close proximity Si side gates is successfully established and reported here with a number of device layouts realized with different number of quantum dots and different quantum dot sizes. Five device generations have been realized and electrically tested. Appendix B, C, D and E of this report are evidence of the versatility and flexibility of this advanced fabrication process.

This PhD project has been, without a doubt, an extensive fabrication and process development effort to realize a novel structure for electron spin qubit applications in Si. The lengthy two fabrication chapters are a reflection of the time, effort, and the amount of process development invested to establish a successful fabrication process for the single electron SISSQIT device, this has concluded with the realization, for the first time, of successful Al FinSET gate technology for SOI nanowires. This achievement is made possible by using a special anisotropic TMAH etching process to define the SOI device layer, this process exposes atomically defined <111> side walls of the SOI NW providing a precise 57.74 side wall slope to support metal coverage of the NWs.

To this date, gate structure at this nanoscale have relied mainly on Poly-Si or titanium nitride as the gate material, even then silicon nitride or oxide spacers are usually included to insure the gate continuity over any step topography, this only introduces extra defects into the NW structure. The atomically wet defined NW approach, presented here, not only provides an excellent metal gates continuity yield (92%) but also creates atomically defined SOI NWs, with almost no line edge roughness, that are completely free from all types of plasma damage typical to RIE defined NWs or spacers based gate structures.

7.2 Future work

The next goal for the SISSQIT project, after this PhD work, is to complete the fabrication process of the current Al FinSET devices batch; a device batch that uses TMAH wet etching to define the SOI device layer for single QD and double QD structure with charge sensors, Al FinSET gates will then be patterned, evaporated and defined with lift off. Top gate oxide and Al top gate and contacts layer will finally be defined. Once the sample is complete, it will be send to the University of Cambridge (project partners) for initial 4 K characterization followed by a more thorough measurement of the devices characteristics at 80 mK in a dilution refrigerator.

The single electron transfer device and electrometer will hopefully provide a great insight into single electron transfer and detection operations, the spin to charge conversion principle can also be demonstrated in the future using this structure with the application of a magnetic field. We believe that this architecture of Al FinSET and Si side gates, expected to provide better tunability to form the QD, would be a good candidate for future electron spin qubit applications.

After sufficient experimental verification and optimization of the transfer and detection operations, the SETD will evolve into an integrated SETD pair that will be further characterised and tested, to achieve the goal of the SISSQIT project of integrating the SETD pair with an electrometer. An Al u-waveguide (defined with e-beam, evaporation and lift off) and a Ni-Co nanomagnet permalloy (defined with e-beam, evaporation or electroplating and lift off) will be the final components to be investigated and integrated into the platform to demonstrate the operations of a double spin qubits system.

In addition to the main SISSQIT single electron transfer and detection devices, the fabrication process developed here will be further utilized to realize various devices and platforms including: charge qubit devices in doped silicon, extreme magneto resistance (EMR) structures, Kelvin probe force microscopy (KPFM) structures for few and single dopants studies and extremely thin SOI (ETSOI) and He Ion lithography experiments.

Appendix A

Process	Process conditions
SOI substrate	100nm Si device layer and 200nm buried oxide
SOI thinning	
SOI thinning	Wet oxidation at 950C, process time is variable.
Thermal oxide removal	Dip in 20:1 BHF, process time is variable.
Wafer clean	RCA1/RCA2 clean, 10 minutes in each bath at 45C
Alignment marks definition	
ZEP520A coating	400nm resist layer spun, followed by 180C hot plate bake for 3 minutes.
E-beam exposure	A dose of 450uC/cm^2 is applied using a 25nA beam current.
Development	Development in ZED-N5 for two minutes followed by an IPA rinse.
RIE dry etch	Three steps etch process: Si device layer etch using SF6:O2 (4:3) gas chemistry (160W RF power) , followed by a buried oxide CHF3 gas chemistry etch (50W RF power) and finally the same Si device layer etch recipe is used for to etch the bulk Si.
Resist removal	The remaining ZEP520A is removed with an Oxygen plasma using a plasma asher.
Wafer clean	RCA1/RCA2 clean, 10 minutes in each bath at 45C
SiO2 doping mask definition	

PECVD deposition	100nm SiO2 is deposited from SiH4 and N2O at 350C, three individual deposition steps are employed.
UVN30 coating	HMDS priming followed by spin coating and a hot plate bake at 110C for 1 minute to form a 360nm thick layer.
E-beam exposure	A dose of 100uC/cm^2 is applied using a 25nA beam current.
Post exposure bake	Hot plate bake at 110C for 1 minute.
Development	Development in MF CD26 for 30 seconds, followed by a DI water rinse.
RIE dry etch	CHF3:Ar (1:3) gas chemistry is used (200W RF power).
Resist removal	The remaining UVN30 is removed with a 5 minutes Oxygen plasma using a plasma asher.
Wafer clean	RCA1/RCA2 clean, 10 minutes in each bath at 45C
Spin on dopant (Phosphorsilicafilm) process	
Phosphorsilicafilm coating	Phosphorsilicafilm is spun at 2500rpm for 6os followed by a hot plate bake at 110C for 2 minutes to form 300nm thick film.
Activation anneal	N2 ambient anneal at 925C for 15 minutes.
Phosphorsilicafilm removal	Phosphorsilicafilm is removed with a 20:1 BHF dip.
Wafer clean	RCA1/RCA2 clean, 10 minutes in each bath at 45C
Si device layer definition	

HSQ 4% coating	Resist spun at 5000rpm to yield a 60 nm thick layer, followed by 80C hot plate bake for 4 minutes.
E-beam exposure	A PEC base dose of 880uC/cm^2 is applied to the fine features using a 1nA beam current, and a PEC base dose of 700uC/cm^2 is applied to the coarse features using a 25nA beam current.
Development	Development in MF 319 for 1 minutes, 40 seconds followed by a rinse in DI water.
HSQ hard mask bake	Hot plate bake at 250C for 4 minutes, 30seconds.
RIE dry etch	SF6:O2 (1:1) gas chemistry is used (100W RF power).
Resist removal	The remaining HSQ is removed with a dip in 20:1 BHF.
Wafer clean	RCA1/RCA2 clean, 10 minutes in each bath at 45C
Al FinSET gate oxide formation	
Thermal oxidation	Dry oxidation at 950C to form 10nm gate oxide.
Al device layer definition	
PMMA950 A4 coating	140nm resist layer spun at, followed by 180C hot plate bake for 90 seconds.
E-beam exposure	A PEC base dose of 920uC/cm^2 is applied to the fine features using a 1nA beam current, and a PEC base dose of 890uC/cm^2 is applied to the coarse features using a 25nA beam current.
Development	Development in MIBK:IPA 1:3 for 50 seconds followed by a rinse in IPA.
Al Evaporation	80nm Al evaporated at a base pressure of 2e-7 mbar with an evaporation rate of 0.5 A/s.
Lift off	60C heated NMP (N-Methylpyrrolidone) with 1 hour NMP soak time.
Top gate oxide and contact via layer formation	

PECVD deposition	200nm SiO2 is deposited from SiH4 and N2O at 350C, four individual deposition steps are employed.
MMA/PMMA495 coating	MMA 8.5 is spun to form a 150nm thick MMA layer; this is followed by a hot plate bake at 150C for 65 seconds. After that PMMA 495 is spun, forming a 250nm thick layer, followed by a final hot plate bake at 180C for 65s, forming a total of 400nm resist profile.
E-beam exposure	A dose of 550uC/cm^2 is applied using a 25nA beam current.
Development	Development in MIBK:IPA 1:1 for 90 seconds followed by a rinse in IPA.
Oxide wet etch	200nm SiO2 etched in 5% diluted BHF
Resist removal	The MMA/PMMA resist is removed with an NMP soak.
Al top gate and contacts layer definition	
MMA/PMMA495 coating	MMA 8.5 is spun to form a 150nm thick MMA layer; this is followed by a hot plate bake at 150C for 65 seconds. After that PMMA 495 is spun, forming a 250nm thick layer, followed by a final hot plate bake at 180C for 65s, forming a total of 400nm resist profile.
E-beam exposure	A dose of 550uC/cm^2 is applied using a 25nA beam current.
Development	Development in MIBK:IPA 1:1 for 90 seconds followed by a rinse in IPA.
Al Evaporation	200nm Al evaporated at a base pressure of 5e-6 mbar with an evaporation rate of 2 A/s.
Lift off	60C heated NMP with 20 minutes NMP soak time..
Ohmic Al contacts anneal	
Contact anneal	Forming gas anneal at 400C for 10 minutes.

Appendix B

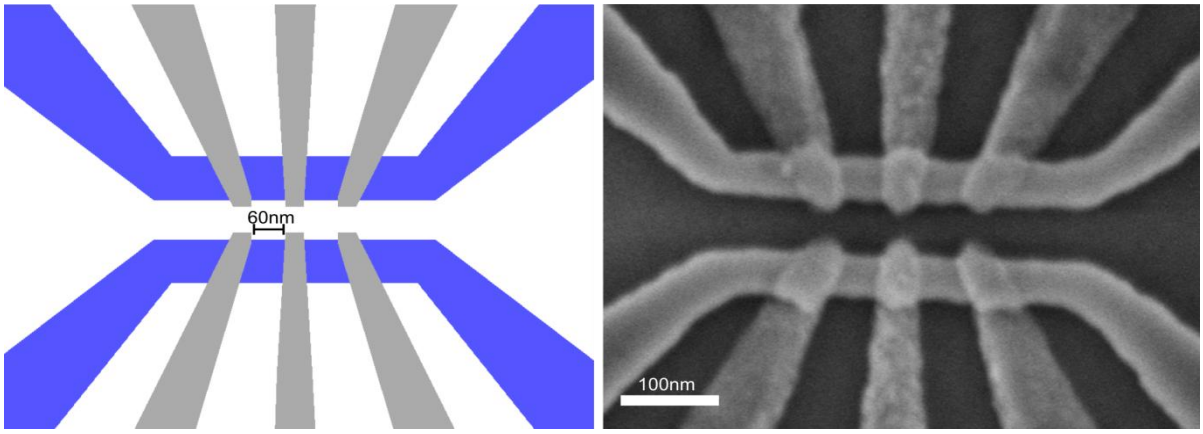


Fig. B.1: Double quantum dot turnstile and electrometer, all QDs are designed to be 60 nm in width.

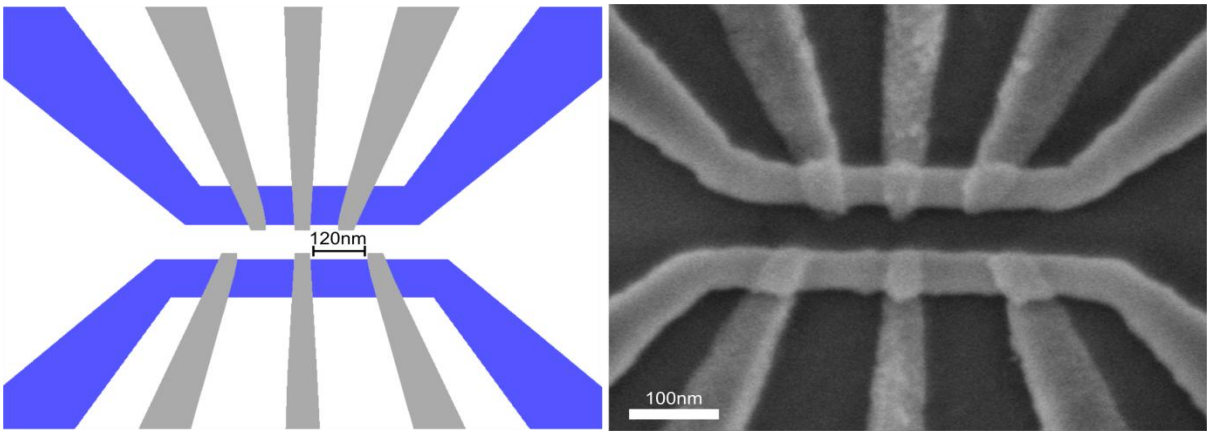


Fig. B.2: Double quantum dot turnstile and electrometer, the bottom QDs are designed to be 120 nm in width while the top QDs are 60 nm in width.

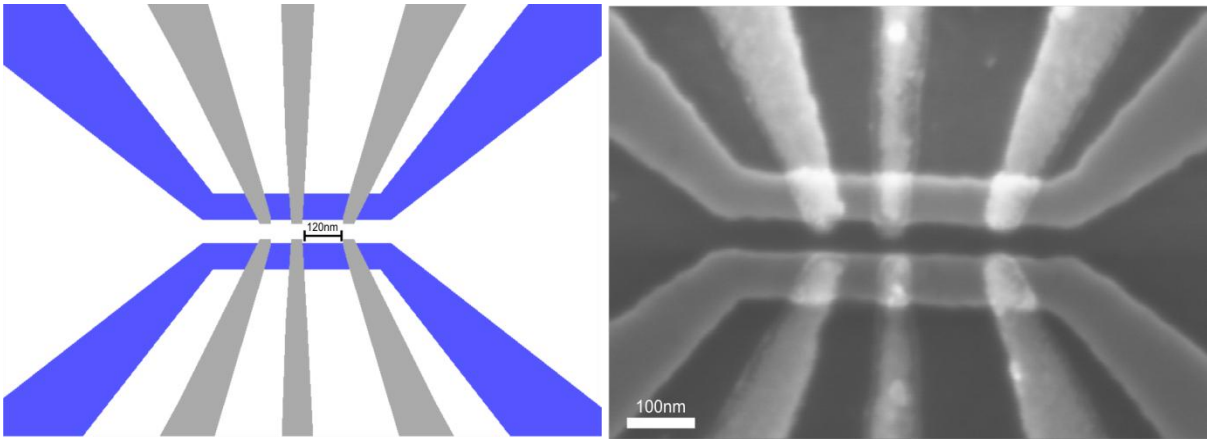


Fig. B.3: Double quantum dot turnstile and electrometer, the QDs on the right are designed to be 120 nm in width while the left QDs are 60 nm in width.

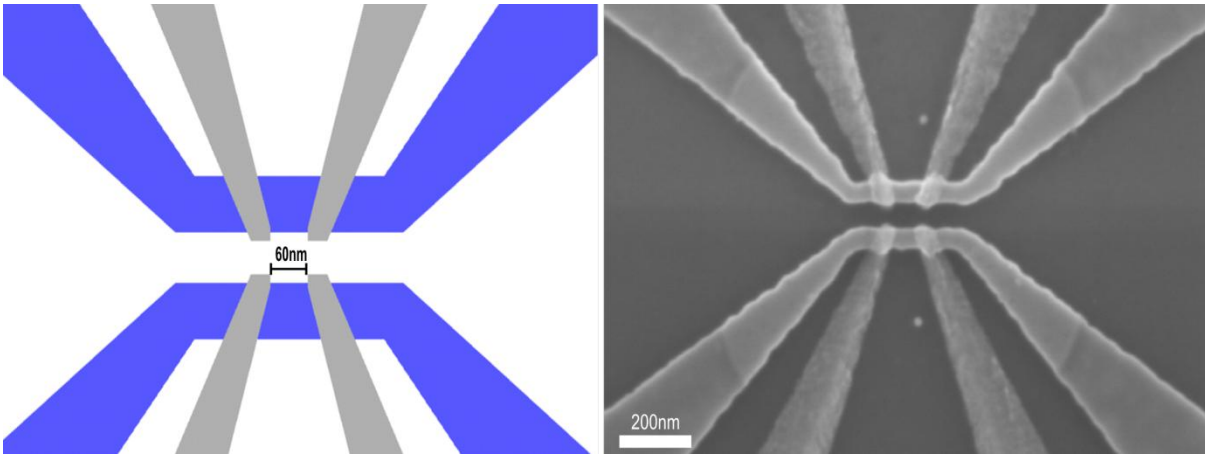


Fig. B.4: Signal quantum dot turnstile and electrometer, all QDs are designed to be 60 nm in width.

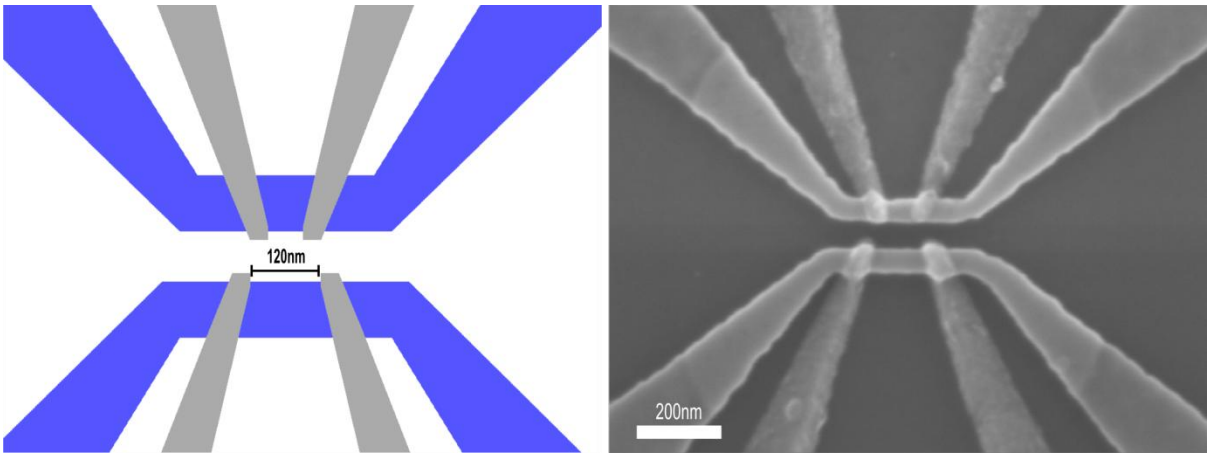


Fig. B.5: Single quantum dot turnstile and electrometer, the bottom QD are designed to be 120 nm in width while the top QD are 60 nm in width.

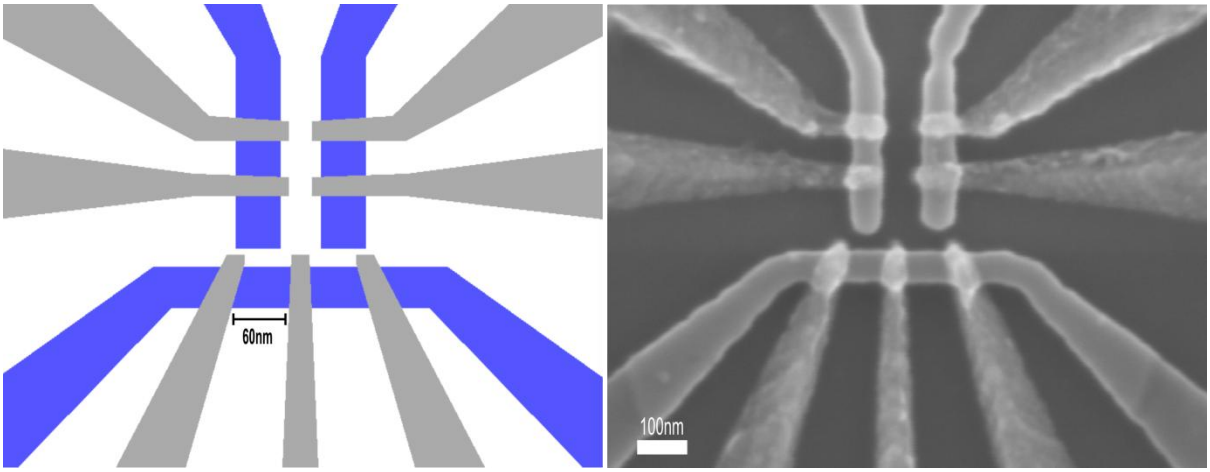


Fig. B.6: Charge qubits platform consisting of two reservoir-connected charge qubits coupled to a double QDs electrometer.

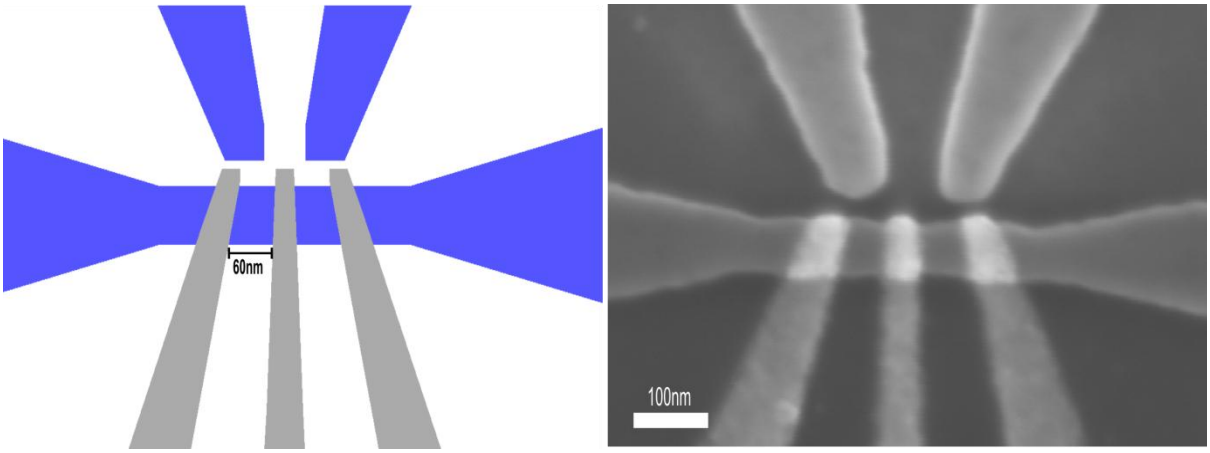


Fig. B.7: Double quantum dots turnstile device with Si side gates, both QDs are 60nm in size.

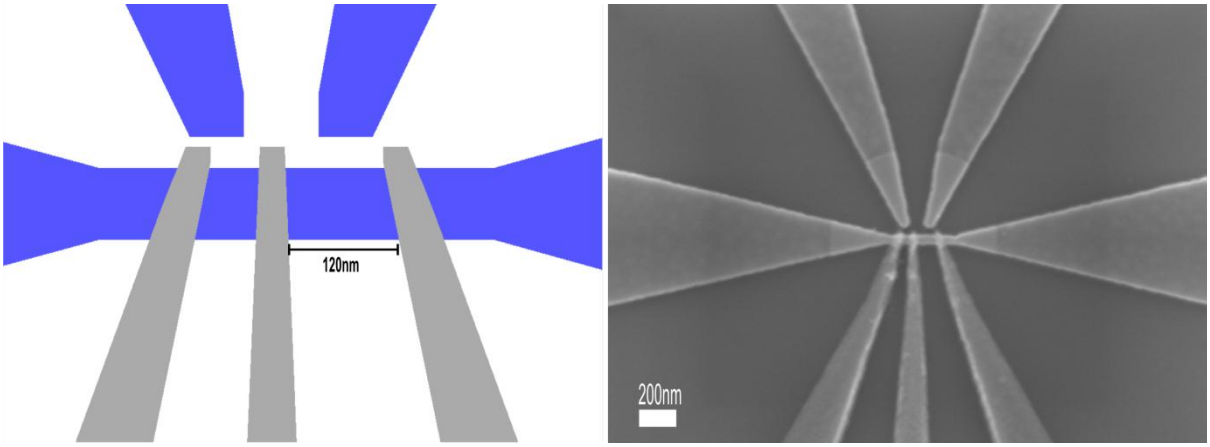


Fig. B.8: Double quantum dots turnstile device with Si side gates, right QD is 120 nm wide while the left QD is 60 nm wide.

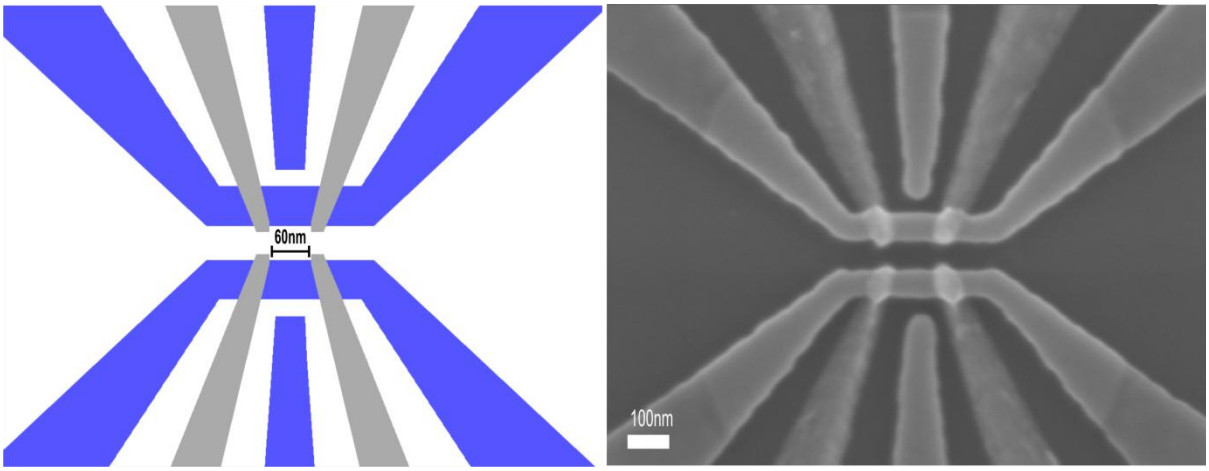


Fig. B.9: Signal quantum dot turnstile and electrometer with Si side gates, all QDs are designed to be 60 nm in width.

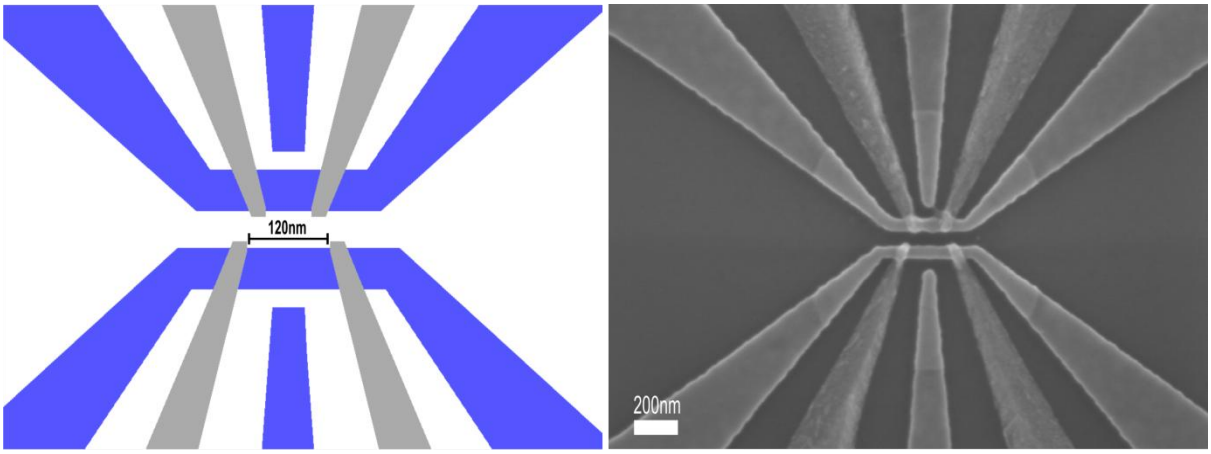


Fig. B.10: Single quantum dot turnstile and electrometer with Si side gates, the bottom QD are designed to be 120 nm in width while the top QD are 60 nm in width.

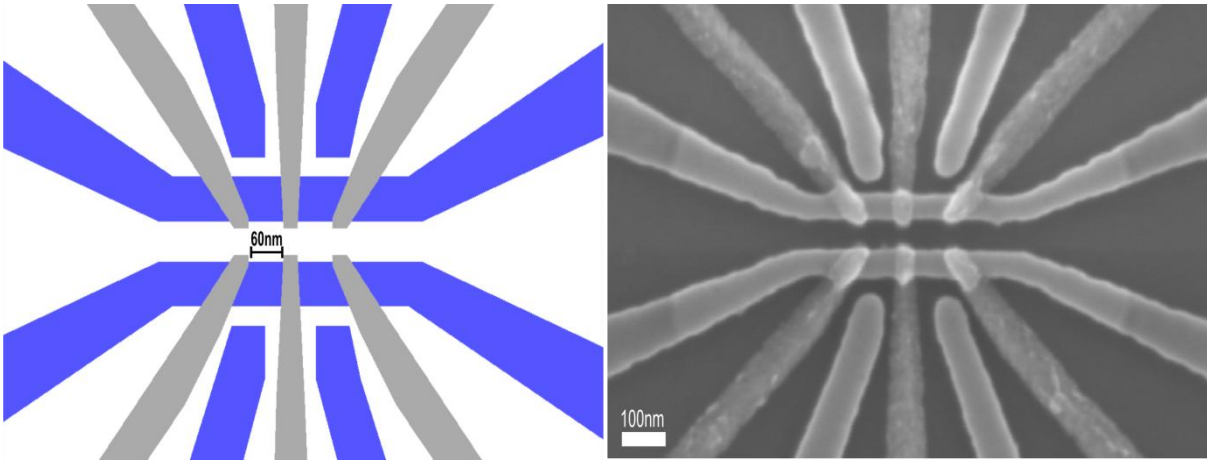


Fig. B.11: Double quantum dot turnstile and electrometer with Si side gates, all QDs are designed to be 60 nm in width.

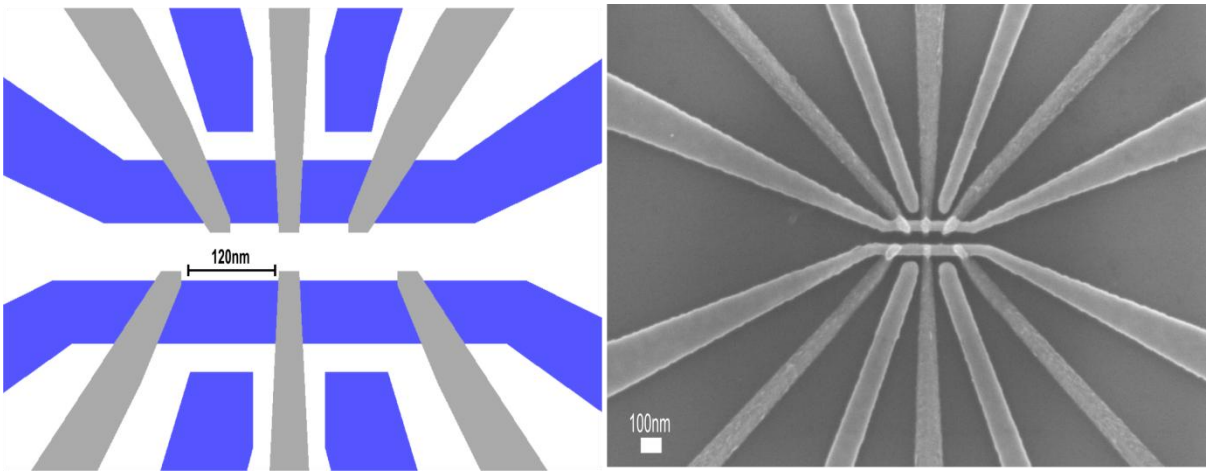


Fig. B.12: Double quantum dot turnstile and electrometer with Si side gates, the bottom QDs are designed to be 120 nm wide while the top QDs are 60 nm in width.

Appendix C

Charge qubits platform

C.1 Introduction

This section introduces the development of a charge qubits platform in Phosphorus doped SOI, the goal of these device is to study charge transfer and charge detection in Si:P quantum dots.

Charge qubits have attracted a great deal of interest due to the relatively simple qubit read out methods that can be used (the charge state can be detected directly using a QPC or an SET). Coherent manipulation and successful single charge detection has been demonstrated with a number of isolated charge qubits systems, as described in chapter 3, these charge qubits systems included electrostatically coupled side gates to provide sufficient control of the isolated QDs. However, correct operation of doped isolated quantum dots strongly depends on the density of excess charge that is permanently stored in the isolated structure as a result of the fabrication process of these isolated QDs, this can lead to a limited system performance and low process yield [120]. Therefore, we introduce here Si:P double QDs that are electrically connected to an electron reservoir via lithographically defined tunnel barrier constrictions, the device we developed includes two double QDs coupled to a double QDs single electron electrometer realized in Phosphorus doped 40 nm thick SOI (doping level of $2x10^{19}$ cm^{-3}).

The charge qubits platform consists of two parallel single electron turnstile devices that form the two charge qubits at the end of the turnstile; 50 nm x 50 nm charge qubits are realized by lithographically defined constrictions with four Si side gates electrostatically coupled to the constrictions to control their potentials. The two charge qubits are electrostatically coupled to a double QD electrometer, the electrometer is used to detect the charge qubits occupancy and study their characteristics. Below is a schematic showing the charge qubits platform.

C.2 Capacitance and single electron simulations

To study the single electron transfer and detection characteristics of the charge qubits platform, 3D FEM modelling of this platform is carried out using COMSOL Multiphysics. The extracted capacitance values are then fed into a Monte Carlo based single electron simulator (CAMSET), the single electron simulation is used to demonstrate single electron transfer and single electron detection

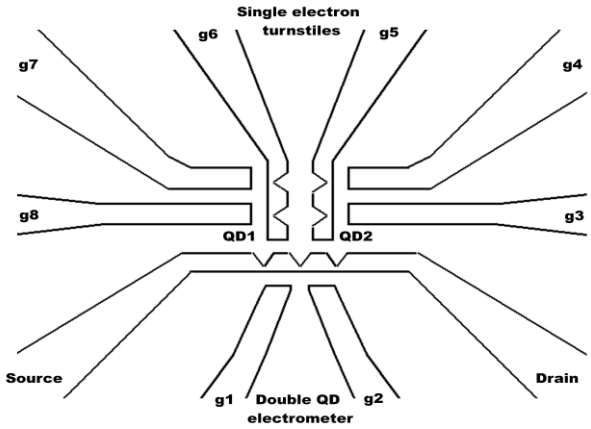


Fig. C.1: Schematic showing the two charge qubits platform (QD1 and QD2).

of the charge qubits platform. COMOSL simulation is carried out in the same manner described in chapter 5. The extracted capacitance characteristics are used to build an equivalent capacitance circuit of the platform using the Monte Carlo single electron simulator. The two parallel single electron turnstile devices capacitance characteristics are very similar to the characteristics of the spin qubits device structure described in chapter 5. Therefore, the operation of these turnstile devices employs the same operation scheme that successfully demonstrated single electron transfer operation show in fig. 5.9. However, since the electrometer operation scheme was not discussed in chapter 5, the charge qubits electrometer operation scheme is described here. The equivalent circuit of the double QDs electrometer coupled to the two charge qubits (QD1 and QD2) is shown below in fig. C.2.

The double QDs electrometer is initially simulated at a source drain of 1mV at 4 K with both QD1 and QD2 empty, the resulting honey comb pattern is shown in fig C.2. The electrometer is then simulated by recoring the source drain current as a function of gate g2 with a source drain voltage of 1 mV at 4 K and no electrons in QD1 and QD2, g1 here was fixed to 12 mV (this value is selected because it produces two current peaks shown by the white trace in fig. C.2). The result of this simulation is shown as state A shown in fig. C.3 below. This simulation set up is repeated three more times to check the electrometer current response to the three other possibilities of single electron occupancy in QD1 and QD2 as shown in fig. C.3. These four states of single electron occupancy in QD1 and QD2 show clear and measurable shifts in the electrometer current. For example state A is distinguished from state B by a current shift of 0.1 nA, while state C and D can be identified by a current shift 0f 0.2 nA. By selecting Vg2 voltage of 1.5 mV (sense voltage 1), states A or B can be identified from states C and D. on the other hand, If Vg2 voltage of 3.3 mV (sense voltage 2) is selected then states C and D can be identified. This simulation method is similar to a simulation approach reported by Kawata et al. [121]. The electrometer here is capable of identifying four individual single electron occupancy states of the charge qubits, where these states represent the transfer of a single electron to one of the charge qubits (QD1 and QD2).

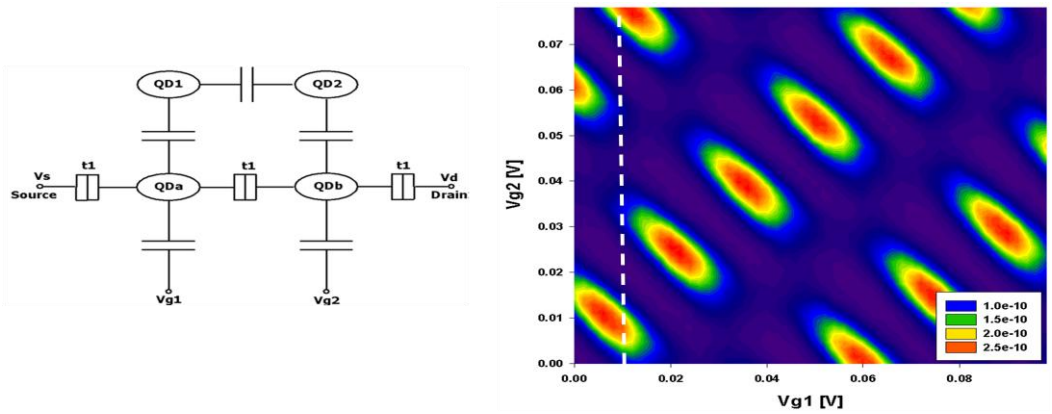


Fig. C.2 Left: a simplified equivalent circuit of the double QDs electrometer coupled to the charge QDs. Right: Contour plot of the electrometer current as a function of side gates potential at 4 K.

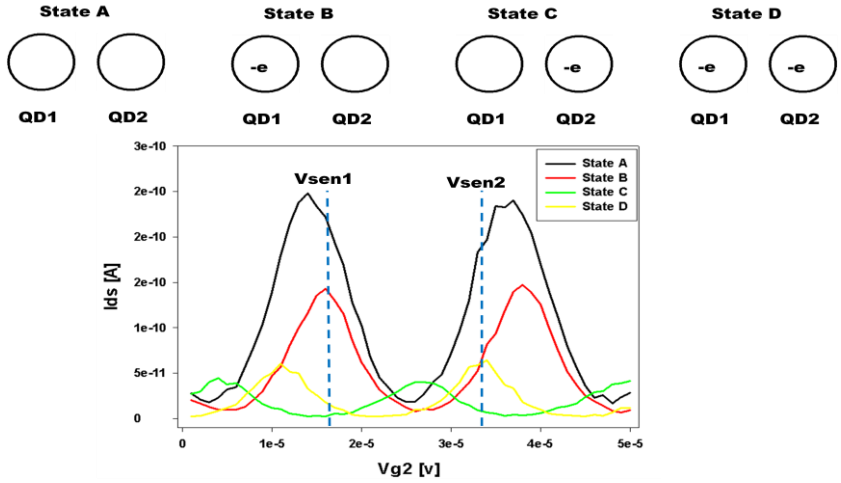


Fig. C.3 Top: Four possible single electron occupancy configurations for QD1 and QD2. Bottom: electrometer current as a function of Vg2 for the four charge states above at 4 K.

C.3 Fabrication of the charge qubits platform

As described earlier, the charge qubit devices have lithographically defined constrictions, and side gates to control the potential at the quantum dots and the constrictions. These charge qubit devices were proposed as devices that can be easily and quickly fabricated at a time when the alignment marks etch process and the Al FinSET lift off process were being developed and tested. The fabrication process for these devices is similar to Al FinSET devices fabrication. It starts by thinning the SOI device layer from 100 nm to 50 nm. The thinned SOI is then doped using the Phosphorosilica film spin-on process. Hall measurements demonstrated that the spin-on dopant process produces phosphorus doping level of $2x10^{19}$ cm^{-3}. The device layer is patterned using HSQ e-beam lithography. HSQ was then used as an etch mask during RIE patter transfer. The patterned device is then oxidized to shrink the size of the QDs and the constrictions; 25 nm thick oxide layer was formed and the NWs

shrunk by 11 nm in all directions. Al contacts layer is then patterned followed by evaporation and lift off. The sample is then finally annealed in forming gas.

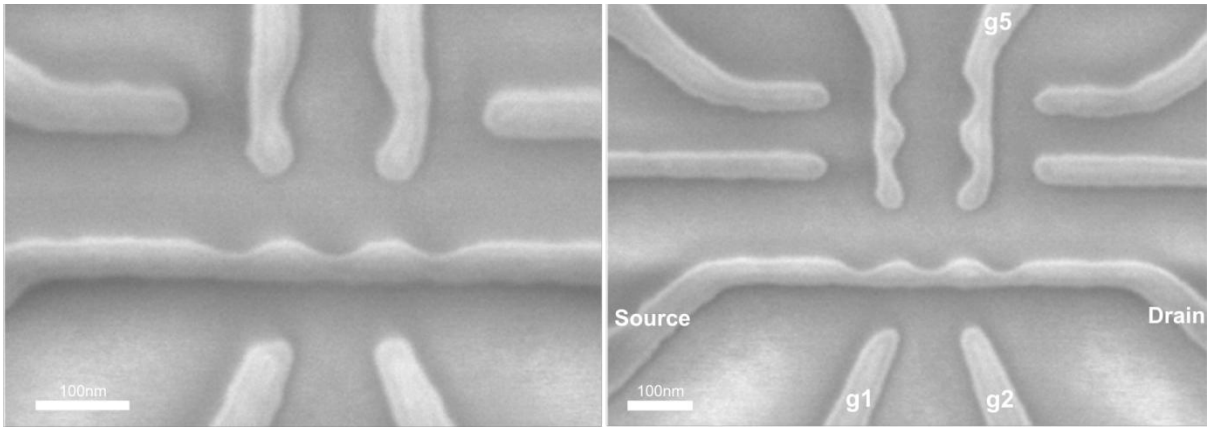


Fig. C.4 Left: charge qubits with two side gates. Right: charge qubits device with four side gates.

C.4 Measurements and characterization

Measurements started by characterising the channel resistance at room temperature and 78K (liquid Nitrogen) as shown in fig. C.5, this is measured as 10 KΩ at 78 K, and 200 KΩ at room temperature. Also at room temperature, the source drain current was then recorded as a function of both side gates at various source drain potentials (left side image fig. C.5). This demonstrated the effectiveness of the Si side gates in controlling the channel conductance. After the basic DC characterization of the device at the University of Southampton, the devices were then sent to Hitachi Cambridge laboratory (project partner) to perform low temperature measurements (4 K). At 4 K, the two side gates of the double QD electrometer were swept together and the electrometer current was recorded. The resulting stability diagram is show in fig C.6, this shows two sets of lines, indicating the presence of two series connected QDs representing the patterned QDs without any unintentional extra dots. However, the triple points are not well defined which may indicate weak coupling between the two quantum dots. The device was quite stable with small drift in time and only 2 RTS events observed per hour.

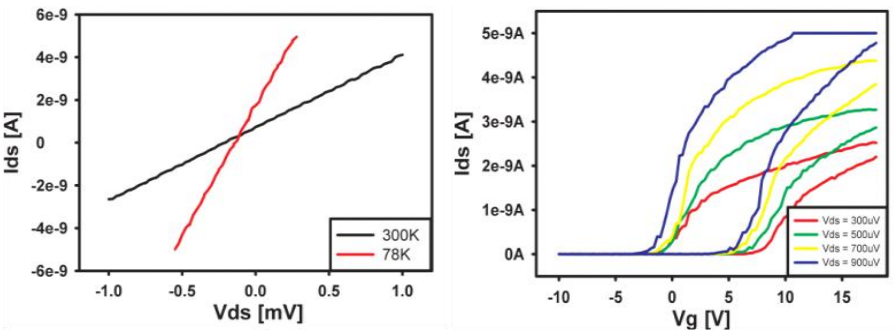


Fig. C.5 Left: Channel resistance at 300 K and 78 K. Right: effect of the side gates at 300 K.

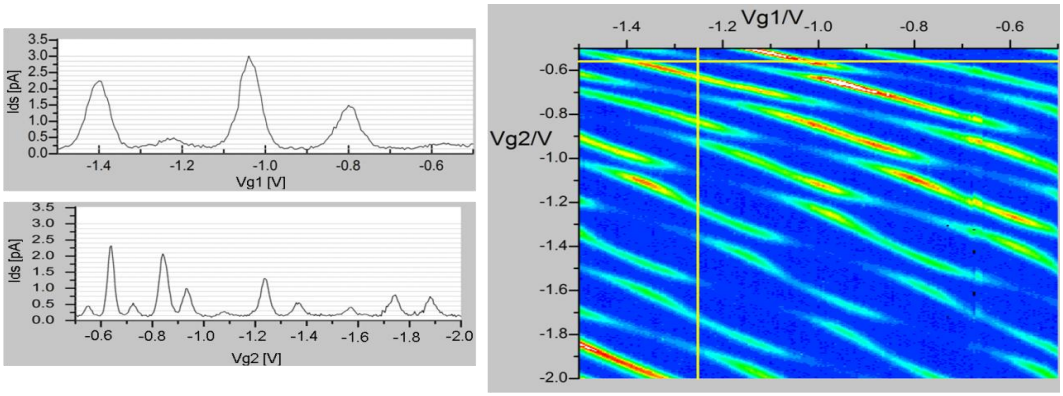


Fig. C.6 Left: electrometer Coulomb oscillations characteristics. Right: stability diagram.

To test the operation of the double QD electrometer as a charge detector, the electron reservoir of QD2 (gate g5) is swept from 0V to -2V to inject electrons into QD2. The change in the number of electrons in QD2 was successfully detected in the electrometer current by sweeping Vg1 or Vg2. The stability diagrams for the electrometer current as a function of Vg1, Vg5 and of Vg2, Vg5 are shown below. We can clearly observe shifts in the position of the Coulomb current peaks, these shifts are not present in the Vg1, Vg2 stability diagram, and they also appear around very similar Vg5 values (-1.5 V) for both plots of Vg1, Vg5 and Vg2, Vg5. These two factors indicate that these shifts in the electrometer current are due to tunnelling events through the constrictions of charge qubit QD2.

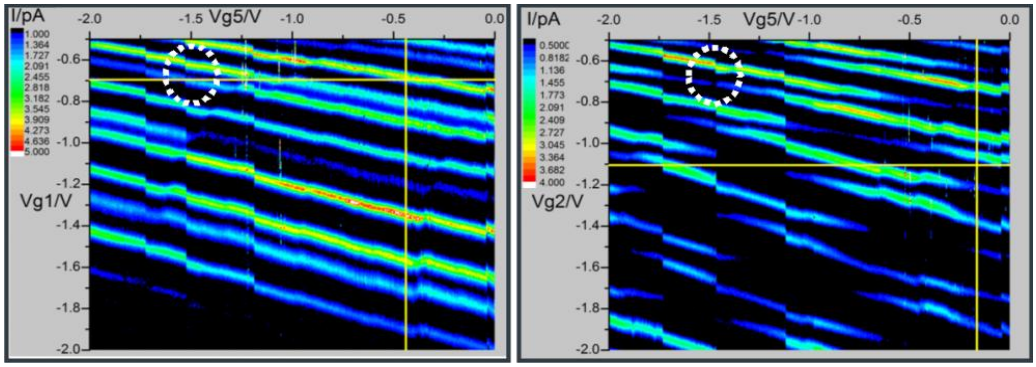


Fig. C.7: Electrometer Stability diagrams as a function of the turnstile reservoir potential (Vg5).

C.5 Summary

A phosphorus doped SOI process is developed here to realize a charge qubits platform, consisting of two charge qubits coupled to a double QDs electrometer. This process produced charge qubit-electrometer separation of about 30 nm and fast prototyping time. Measurements have demonstrated the electrometer success in detecting changes in the charge qubits, it also showed the success of the fabrication process with devices showing stable characterises with minimal noise and drift effects. 3D FEM capacitance simulation and single electron simulations have also been used to verify the electrostatically coupled electrometer ability to detect the electron occupancy of the charge qubits.

Appendix D

Extremely Thin SOI (ETSOI) and He Ion Lithography

Using a similar SOI thinning approach, as the one described in chapter 5, with extra optimization to control the thermal oxide thickness and surface roughness; extremely thin SOI (ETSOI) samples with device layer thickness of 7 nm were successfully developed. Atomic force microscopy (AFM) was used to measure the surface roughness of the 7 nm ESTOI samples; AFM revealed an average surface roughness of 0.11 nm and an RMS surface roughness of 0.13 nm in a randomly selected 1.5 µm x 1.5 µm surface area.

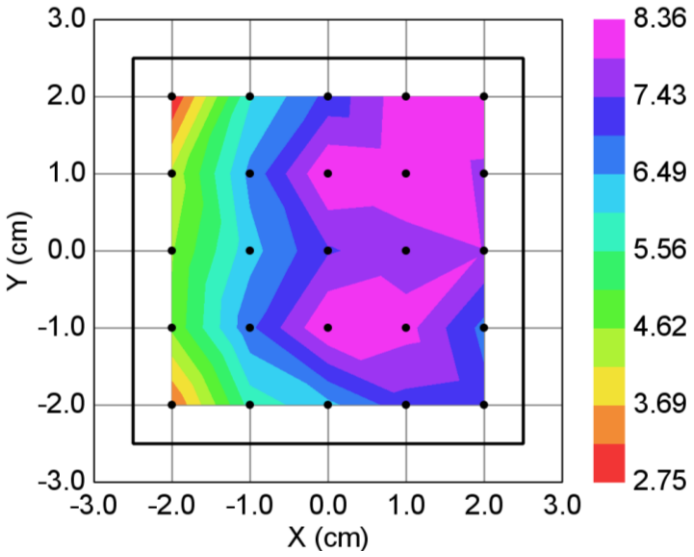


Fig. D.1: ellipsometry scan showing the SOI device layer thickness vs. position on sample for an extremely thin SOI square sample (2 cm x 2 cm).

ETSOI is currently investigated for use in fully depleted MOS architectures as a solution to overcome the scaling challenges of CMOS technology [122]. In this work, ETSOI has been developed for use as a platform for charge qubit devices (same layout as the devices presented in Appendix C) using He Ion lithography. The Orion He Ion microscope at the Southampton nanofabrication centre provides a great potential for rapid prototyping of sub 10 nm device features by selective material removal using the He Ions. Collaborative work in this area has been ongoing with Dr. Stuart Boden and Dr. Zakaria

Moktadir, recently we completed a study investigation the correlation between helium ion milling dose , size of milled area and their effect on the pattern milling depth in ETSOI, and we also demonstrated successful milling of depths larger than 7 nm in ETSOI demonstrating that He Ion milling has strong potential for nanoelctronic devices fabrication [123].

Future work in this area includes realizing the platform on phosphorus doped extremely thin 7 nm SOI (a number of 7nm thick SOI samples have been already created), the use of extremely thin SOI for charge qubits application is a novel subject that could unveil very interesting device characteristics and can potentially allow the realization of single dopant devices.

By using the 7 nm thick SOI, the charge qubits platform will also be scaled to have charge qubits - electrometer separation of less than 10 nm by employing He Ion lithography with two approaches: direct beam milling and He Ion resist lithography. A great deal of progress has already been achieved on direct beam milling experiments to determine the suitable exposure dose required to mill through the 7 nm thick SOI layer [123]. An image of the charge qubits platform patterned using direct beam writing in 7 nm thick SOI, with a minimum feature size of 14 nm (separation between the electrometer and the charge qubits) is shown below.

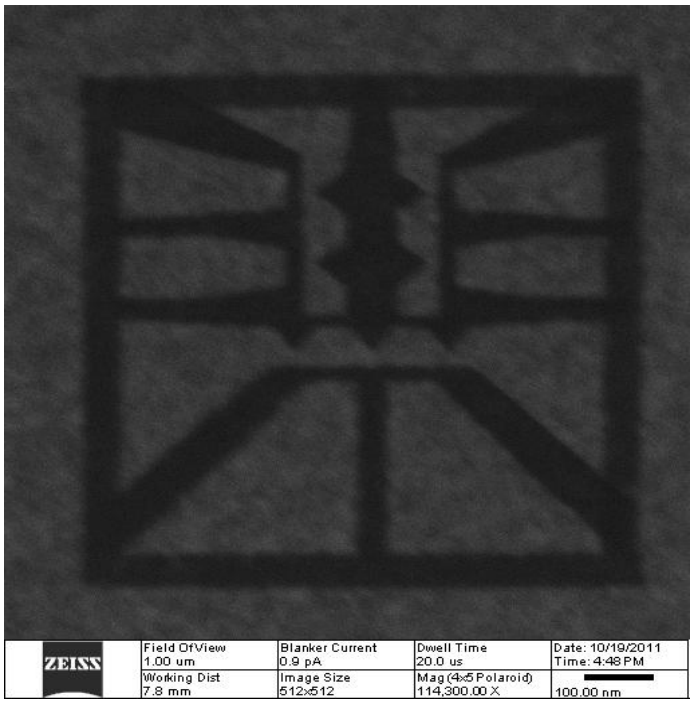


Fig. D.2: A He Ion microscope image of the charge qubits platform patterned in 7 nm thick SOI, exposure dose of the device in the image is currently being optimized to insure complete milling of the ETSOI layer.

Appendix E

Extraordinary Magnetoresistance (EMR) Devices

Building on the fabrication process developed for the Al FinSET single electron devices; novel EMR devices in thin SOI are investigated. This ongoing work is in collaboration with Dr. Zakaria Moktadir, this section gives a brief overview of the fabrication and measurement of the structures currently investigated.

The term extraordinary Magnetoresistance was coined in 2000 by S. Solin relating to structures exclusively formed of a semiconductor and conducting component. His experiments used a van der Pauw disc structures made of non magnetic semiconducting material (indium antimonide) with an embedded smaller inclusion of a conducting material (gold), these experiments demonstrated very high percentage of Magnetoresistance with the application of a magnetic field (MR of million percent in a 5 T magnetic field). These experiments attracted attention for their potential to realize high sensitivity magnetic field sensor and to improve read head mechanisms for magnetic disk drives [124], [125], [126]. The structure investigated here consists of a phosphorus doped ($7x10^{19}$ cm^{-3}) SOI component and an Al fishbone inclusion embedded in the SOI layer as the conducting component in a Van der Pauw configuration as shown in fig. E.1 below.

The fabrication process for these devices is derived directly from the Al FinSET devices fabrication. It starts by thinning the SOI device layer from 100 nm to 50 nm. The thinned SOI is then doped using ion implantation to achieve a doping level of $7x10^{19}$ cm^{-3}. The device layer is patterned using HSQ e-beam lithography. HSQ was then used as an etch mask during RIE patter transfer. The Al embedded inclusion and the Al contacts layer are patterned with e-beam, this is followed by e-beam evaporation and lift off. The sample is then finally annealed in forming gas at 400 C.

The fabricated structures are characterized in a cryogen free high magnetic field measurements system from Cryogenic ltd, providing room temperature and low temperature (down to 4 K) measurements with the application of a perpendicular magnetic field (up to 12 T). Fig. E.2 (right) shows Magnetoresistance of one of the fabricated structures as a function of a perpendicular magnetic filed at 5 K, for three different input current values.

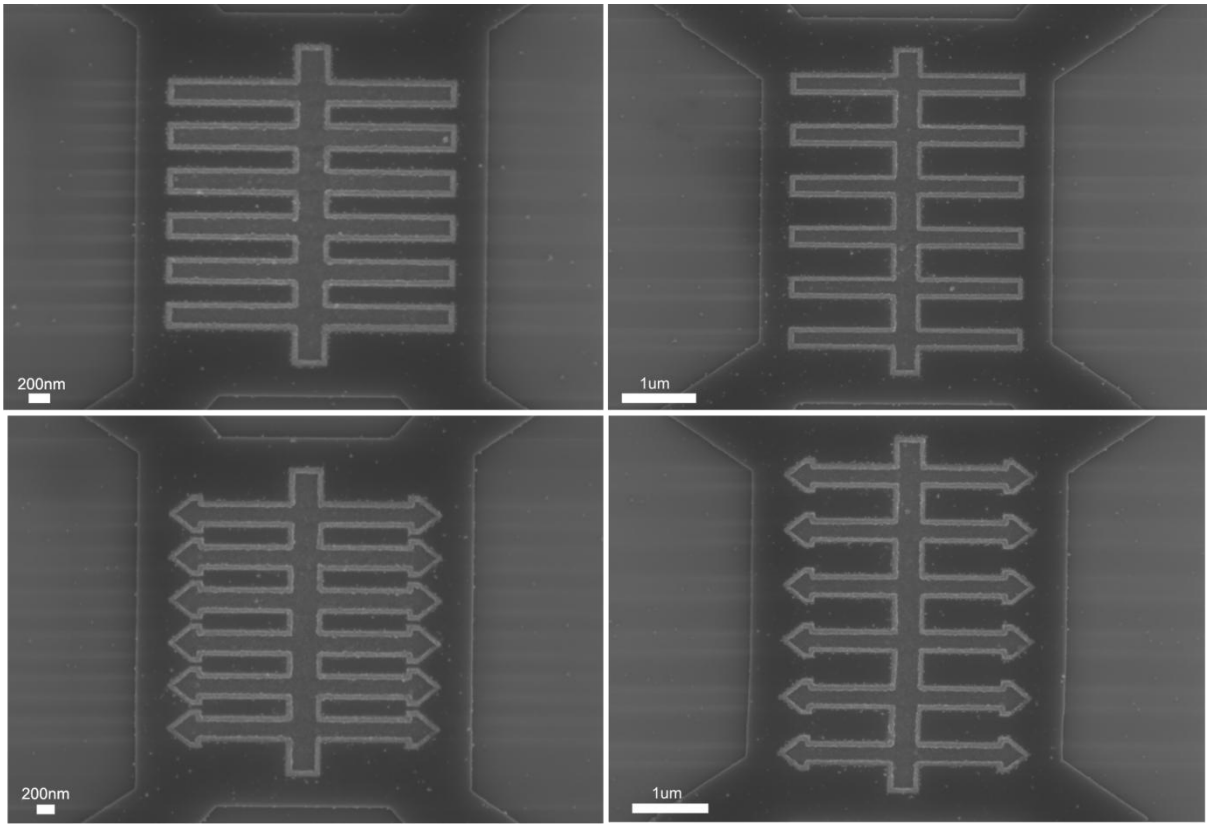


Fig. E.1: SEM images of some of the fabricated EMR device. Devices on the right has a smaller metal filling factor (ratio of the metal area to the Si area) compared to the devices shown on the left side.

Magnetoresistance is determined by applying a perpendicular magnetic field; with four contact pads placed in equal distance to the center of the structure. Current is injected into two adjacent contacts and the potential difference created is measured across the other two contacts. The Magnetoresistance values are calculated using the resistance value at no magnetic field R(0) and the resistance value measured under the influence of a perpendicular magnetic field R(H) [126]:

$$MR = \frac{R(H) - R(0)}{R(0)} \times 100\% \qquad \text{(E.1)}$$

At low or no applied magnetic field, the injected current passes through the embedded metal structure, as it provides the least resistive path. The application of a magnetic field forces the current away from the metal inclusion and causes it to flow through the edges of the semiconductor structure and therefore increases the resistance of the current path. Larger areas of metal inclusion in the semiconductor structure (larger metal filling factor) translates to higher Magnetoresistance (EMR), this forces the current path further towards the edge of the semiconductor area and therefore further increases the current path resistance. In this project, a number of different layouts employing different metal filling factor and different metal fishbone layouts have been realized as shown in the SEM images of fig. E.1.

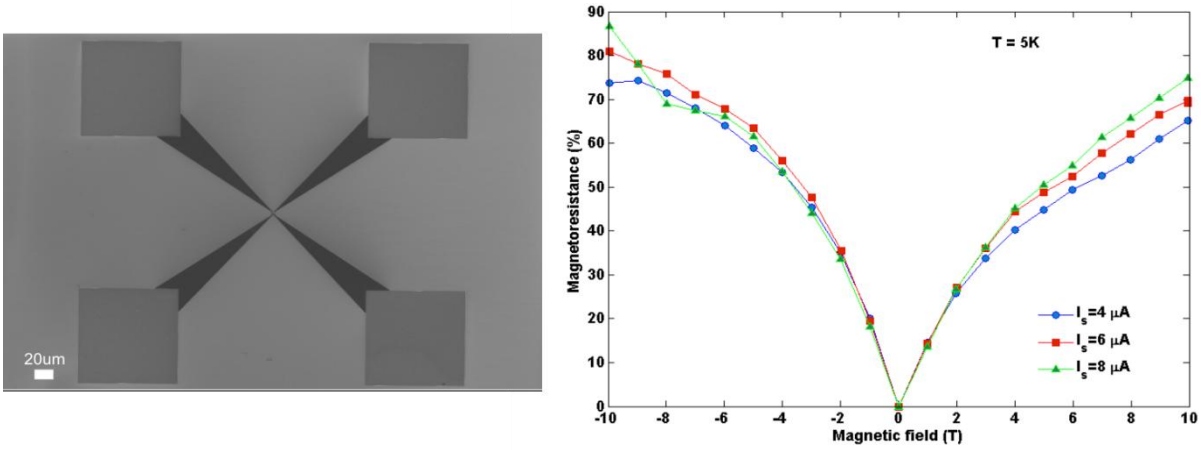


Fig. E.2 Left: Van der Pauw layout for measuring Magnetoresistance. Right: Magnetoresistance as a function of the perpendicular magnetic field at 5 K, for a similar structure to the one shown in the top left SEM of fig. E.1, the slight asymmetry in the MR plot is due to lithographic variations between the left and right sides of the Al fishbone inclusion in this device.

So far, the low temperature experiments have demonstrated relatively good EMR values (90% in fig. E.2) and we are currently investigating the different geometries and layouts of Al fishbone structures (fig. E.1), and studying their effect on the EMR performance of these structures. The room temperature EMR is very weak as the SOI has a very low mobility (which is 62.5 $cm^2/V.s$ as determined by Hall measurements).

The EMR effect is strongly dependant on the geometry of the structure, geometry of the semiconductor and conductor components and the electrical properties (especially mobility) of the materials used. Therefore, future work in this area will investigate optimized geometries of novel semiconductor platforms including low mobility intrinsic SOI, extremely thin SOI (ETSOI) and graphene [127].

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