UNIVERSITY OF SOUTHAMPTON

CMOS COMPATIBLE VERTICAL SURROUND GATE MOSFETS WITH REDUCED PARASITICS

by

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This thesis is dedicated to my father,

Veit Martin Kunz

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ABSTRACT

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The international technology roadmap for semiconductors predicts that downscaling of the dimensions of electronic devices will continue according to Moore's law for the next 10 to 15 years. However, device scaling is getting more and more complicated due to physical limitations. Novel device architectures are needed to overcome these problems. Vertical transistors could be one potential solution since the channel length is independent from the device layout.

In this thesis, novel concepts to reduce parasitic behaviour in vertical single and surround gate MOSFETs are presented. This includes a novel fillet local oxidation (FILOX) process, optimisations of the pillar, a pillar top insulator and the incorporation of polySiGe into the source of a vertical MOS transistor.

Calculations based on industry layout rules at the 100nm technology node for vertical and lateral devices are presented. For the optimised minimum geometry single gate vertical MOSFET incorporating FILOX with optimised pillar structure, the gate/drain capacitance is 40% and the gate/source overlap capacitance 60% of that of a minimum dimension lateral MOS device. For optimised surround gate transistors the overlap capacitance is 20% and 5% of that of a lateral transistor. These calculations demonstrate the potential of optimised vertical MOS transistors.

Pillar capacitors incorporating the FILOX process have been fabricated and a reduction in the measured capacitance is obtained by a factor of 1.4 and 5.6 for structures with nitride top and nitride top and FILOX, respectively. Device simulations confirm the measured reduction in capacitance. The extracted oxide thickness on the pillar sidewall is 9.3nm for the fabricated structures, which agrees within a factor of 1.18 with the simulated oxide thickness on the sidewall. Kinks in CV measurements have been investigated and explained by the formation of an inversion layer underneath the field oxide.

A low overlap capacitance, surround gate, vertical MOSFET technology is presented, which uses FILOX to reduce the overlap capacitance between the gate and the drain on the bottom of the pillar. Fabricated n-channel devices show subthreshold slopes of 111 and 123mV/decade for 3nm gate oxide thickness and a channel length of about 105nm for single and surround gate devices, respectively. The devices show good symmetry between the source on top and source on bottom configuration.

To reduce parasitic transistor action in vertical MOS transistors a theory for the base current of a polySiGe emitter (source) is developed, which combines the effects of the polySiGe grains, the grain boundaries and the interfacial layer at the

polySiGe/Si interface into an expression for the effective surface recombination velocity of a polySiGe emitter (source). Silicon bipolar transistors have been fabricated with 0, 10 and 19% Ge in the polySiGe emitter and the variation of base current with Ge content is characterised. The measured base current for a polySiGe emitter increases by a factor of 3.2 for 10% Ge and 4.0 for 19% Ge compared with a control transistor containing no germanium. These values are in good agreement with the theoretical predictions. The competing mechanisms of base current increase by Ge incorporation into the polysilicon and base current decrease due to an interfacial oxide layer are investigated.

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List of Symbols

a	-	pillar length [m]
a_{AA}	-	width of active area [m]
A_c	-	cross-section area of the channel [m^2]
A_{ox}	-	oxide area [m^2]
A_{sub}	-	cross-section area of current flow [m^2]
b	-	pillar width [m]
b_{AA}	-	length of active area [m]
BV_{CBO}	-	common base breakdown voltage [V]
BV_{CEO}	-	common emitter breakdown voltage [V]
β	-	common emitter gain / process transconductance parameter
C_d	-	depletion capacitance [F]
C_{GD}	-	gate/drain overlap capacitance [F]
C_{GDall}	-	overall gate/drain overlap capacitance [F]
C_{GDfill}	-	gate/drain overlap capacitance caused by fillets [F]
C_{GS}	-	gate/source overlap capacitance [F]
C_{GSall}	-	overall gate/source overlap capacitance [F]
C_{GSfill}	-	gate/source overlap capacitance caused by fillets [F]
C_{GSub}	-	gate/substrate overlap capacitance [F]
C_{jD}	-	drain junction capacitance [F]
C_{jDall}	-	overall drain junction capacitance [F]
C_{jS}	-	source junction capacitance [F]
C_{jSall}	-	overall source junction capacitance [F]
C_{ox}	-	oxide capacitance [F m^{-2}]
c_p	-	trap capture cross section [m^{-2}]
d_g	-	polySiGe grain width [m]
d_{gb}	-	grain boundary thickness [m]
D_{gb}	-	hole diffusion coefficient in grain boundary [$m^2 s^{-1}$]
D_n	-	electron diffusion coefficient [$m^2 s^{-1}$]
D_{nb}	-	electron diffusion coefficient in base [$m^2 s^{-1}$]
D_{pe}	-	hole diffusion coefficient in emitter [$m^2 s^{-1}$]
D_{pSiGe}	-	hole diffusion coefficient in polySiGe grain [$m^2 s^{-1}$]
E	-	electric field [V m^{-1}]
E_c	-	energy level of the conduction band [eV]
E_f	-	Fermi energy level [eV]

E_{Fp}	-	quasi Fermi level [eV]
E_g	-	semiconductor band gap [eV]
E_i	-	intrinsic energy level [eV]
E_s	-	electric field at the silicon surface [V/m]
E_v	-	energy level of the valence band [eV]
ϵ_0	-	vacuum permittivity [F/m]
ϵ_{Si}	-	relative dielectric constant of silicon
ϵ_{SiO_2}	-	relative dielectric constant of silicon dioxide
η	-	viscosity [kg $m^{-1}s^{-1}$]
f_{max}	-	maximum oscillation frequency [Hz]
f_T	-	cutoff frequency / transit frequency [Hz]
ϕ_f	-	Fermi potential [V]
ϕ_m	-	metal work function [V]
ϕ_{poly}	-	Fermi potential of polySi [V]
ϕ_s	-	silicon work function [V]
ϕ_{ms}	-	metal/silicon work function difference [V]
ϕ_{ss}	-	surface potential at the source [V]
ψ_{bi}	-	built-in voltage of the pn-junction [V]
ψ_s	-	surface potential [V]
I_B	-	base current [A]
I_C	-	collector current [A]
I_D	-	drain current [A]
I_{Dsub}	-	subthreshold drain current [A]
I_{on}	-	on-current [A]
J	-	hole current density [A m^{-2}]
k	-	Boltzmann constant [J K^{-1}]
K	-	form factor for narrow-width effect
L	-	channel length [m]
L_{do}	-	pillar to active area spacing [m]
L_{do1}	-	FILOX length at the bottom of the pillar [m]
L_{do2}	-	bird's beak length at the bottom of the pillar [m]
L_{eff}	-	effective channel length [m]
L_j	-	implanted length [m]
L_P	-	pinch-off length [m]
L_{pSi}	-	hole diffusion length in Si [m]
L_{pSiGe}	-	hole diffusion length in SiGe [m]
L_{so}	-	bird's beak length at the top of the pillar [m]
μ_n	-	channel mobility [m^2 V^{-1} s^{-1}]
n	-	electron concentration [m^{-3}]
N_A	-	acceptor doping concentration [m^{-3}]
N_{Abeff}	-	effective acceptor concentration in the base [m^{-3}]

N_{CSi}	-	effective densities of states in the Si conduction band [m^{-3}]
N_{CSiGe}	-	effective densities of states in the SiGe conduction band [m^{-3}]
N_D	-	donor doping concentration [m^{-3}]
N_{Deeff}	-	effective donor concentration in the emitter [m^{-3}]
n_i	-	intrinsic carrier concentration in silicon [m^{-3}]
n_{iSiGe}	-	intrinsic carrier concentration in SiGe [m^{-3}]
n_p	-	electron concentration in substrate [m^{-3}]
N_{st}	-	trap density [m^{-3}]
N_{VSi}	-	effective densities of states in the Si valence band [m^{-3}]
N_{VSiGe}	-	effective densities of states in the SiGe valence band [m^{-3}]
ν_{th}	-	thermal velocity [m s^{-1}]
p_{Si}	-	hole concentration in silicon [m^{-3}]
p_{SiGe}	-	hole concentration in SiGe[m^{-3}]
q	-	elementary charge [A s]
Q_B	-	depletion charge density [C cm^{-2}]
Q_f	-	fixed-oxide charge [cm^{-2}]
Q_{it}	-	interface-trapped charge [cm^{-2}]
Q_m	-	mobile ionic charge [cm^{-2}]
Q_{ot}	-	oxide-trapped charge [cm^{-2}]
ρ	-	charge density [Cm^{-3}]
S	-	subthreshold swing [V/decade]
S_{EFF}	-	effective surface recombination velocity [m s^{-1}]
S_G	-	surface recombination velocity at the grain boundary [m s^{-1}]
S_{GB}	-	recombination velocity at grain boundary contact [m s^{-1}]
S_I	-	recombination at the polySi/silicon interface [m s^{-1}]
S_M	-	recombination velocity at metal contact [m s^{-1}]
σ_{xx}	-	normal stress in x-direction [dyne m^{-2}]
σ_{yy}	-	normal stress in y-direction [dyne m^{-2}]
T	-	temperature [K]
T_I	-	tunnelling coefficient [m s^{-1}]
t_{hLox}	-	bird's beak thickness at the top of the pillar [m]
t_{ox}	-	oxide thickness [m]
t_{pInox}	-	insulator thickness on top of the pillar [m]
t_s	-	shallow trench isolation oxide thickness [m]
V_B	-	substrate bias voltage [V]
V_{be}	-	base emitter voltage [V]
V_c	-	channel voltage [V]
V_{DS}	-	drain/source voltage [V]
$V_{DS,sat}$	-	source/drain voltage at saturation [V]
V_{FB}	-	flat band voltage [V]
V_G	-	gate voltage [V]
V_j	-	reverse bias voltage across the junction [V]

V_T	-	threshold voltage [V]
V_{Tbias}	-	threshold voltage with substrate bias [V]
V_{TSCE}	-	short-channel threshold voltage [V]
V_{TNWE}	-	narrow-width threshold voltage [V]
V_{ox}	-	voltage at the oxide [V]
V_0	-	voltage drop across the interfacial oxide [V]
W	-	channel width [m]
W_{all}	-	overall channel width [m]
W_B	-	base width [m]
W_E	-	emitter depth [m]
W_s	-	gate over STI overlap [m]
x_a	-	length of capacitor [m]
x_b	-	width of capacitor [m]
x_c	-	channel thickness [m]
x_{ceff}	-	effective channel thickness [m]
x_d	-	depletion region width [m]
x_{poly}	-	polysilicon layer thickness [m]
χ_e	-	electron affinity [V]
χ_h	-	hole affinity [V]

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Chapter 1

Introduction

According to the semiconductor roadmap the gate length of MOS transistors will be decreased to 40nm in production by 2011 [1]. To achieve device scaling down to 40nm and below double gate devices are currently considered the most promising option because the double gate gives better control of the channel and hence better short-channel effects [2]. In general, three possible architectures can be classified by the orientation of the channel:

- planar SOI
- SOI fin (horizontal current flow)
- vertical (vertical current flow)

Planar SOI double gate transistors are an extension of the conventional SOI-MOSFET. A back gate for better control of the channel is added by etching a cavity into the buried oxide layer underneath the active silicon region [3]. The fabrication process of planar double gate devices is complicated and can involve several critical steps like epitaxy and chemical mechanical polishing (CMP) [4]. The authors in [5] suggest a bonding techniques to achieve the oxide/gate/oxide structure.

An early approach to SOI fins, called the DELTA transistor, was presented in [6, 7]. These devices were fabricated by oxidising the silicon underneath the active channel area to obtain a SOI structure. However, very good control of the oxidation is needed to accurately control the thickness of the silicon fin which is protected by nitride fillets at the sidewalls. A similar device called the FinFET [8–23] has recently gained attention by the industry and channel lengths of less than 20nm have been reported in [10, 17]. To increase the current drive, the width of the device is increased by the parallel connection of several fins. However, Chang et al. [17] reported increased source and drain resistances for very thin fins.

All of the above concepts require stepper lithography to define the channel region. Lithography tools for sub 100nm channel lengths are extremely expensive and CMOS mask sets cost over $1 million per set. Recently there has therefore been considerable interest in vertical MOS transistors to overcome these lithography limitations. By arranging the channel vertically the channel length becomes independent of the lithography capability. Several approaches have been investigated for the design and fabrication of vertical MOSFETs. These approaches can be partitioned into four broad categories, namely epitaxy, replacement gate, ion implantation and vertical devices incorporating SiGe.

The epitaxy approach is illustrated in figure 1.1 [24–34]. A MOS transistor is created by growing epitaxial layers for the n^+ drain, p-channel and n^+ source. The channel length can be very small because of the good control of layer thickness that can be achieved using molecular beam epitaxy (MBE) or low pressure chemical vapor deposition (LPCVD). Following epitaxy, a pillar is etched, a gate oxide is grown and a polysilicon gate deposited to create the vertical MOS transistor. Transistors with channel lengths in the range 100-30nm have been produced in this way [32]. There are three main disadvantages of this approach. The first is overlap capacitance where the polysilicon gate passes over the drain at the bottom of the pillar and over the source at the top of the pillar. The second is the very high parasitic bipolar transistor gain that is obtained because both the source and drain extend across the full width of the pillar. The third is the integration of epitaxial layers into a standard CMOS process.

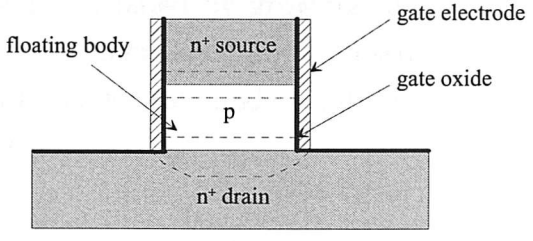


Figure 1.1: Vertical MOSFET based on epitaxy

A variant of the epitaxy approach has been developed, which uses selective epitaxy [35–39], as illustrated in figure 1.2. In this approach, an oxide/polysilicon/oxide stack is created before the epitaxy. A gate oxide layer is then formed on the side of the polysilicon gate and the n^+ drain, p-channel and n^+ source are grown using selective epitaxy. This approach has the advantage that the overlap capacitance is eliminated, but the high parasitic bipolar gain remains as a problem. Furthermore, additional problems are introduced, in particular the growth of a high quality gate oxide on polysilicon and the problem of controlling facets during selective epitaxy.

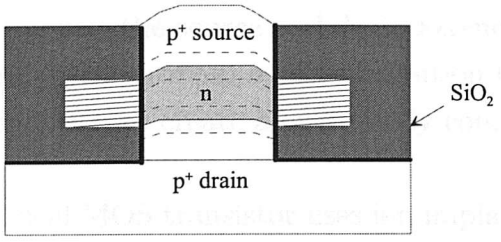


Figure 1.2: Vertical MOSFET based on selective epitaxy with reduced overlap capacitance

In a final variant of the epitaxy approach [32–34], a surround gate or double gate structure is created by extending the polysilicon gate over the entire width of the pillar. If the pillar width is dramatically reduced, a fully depleted device can be produced analogous to those produced using SOI technology. A double gate, fully depleted vertical MOS transistor would be very attractive for deep sub 0.1μm CMOS because of improved short channel effects. However, such a device would potentially have the same disadvantages as the transistor in figure 1.1, namely high overlap capacitance and high parasitic bipolar gain.

The second category of vertical MOS transistor [40–42] uses layer deposition to create a channel length that is defined by the layer thicknesses, as illustrated in figure 1.3. The source and drain regions are created by diffusion from PSG. This means that the channel length is defined by the thickness of the gate layer and by the amount of out-diffusion from the PSG layers. The p-channel region is grown by selective epitaxy, and the faceting problem is avoided by growing the layer thicker than needed and polishing back. A gate replacement technique is used to create the gate which means that the gate oxide can be grown on single crystal silicon rather than on polysilicon as in the device in figure 1.2.

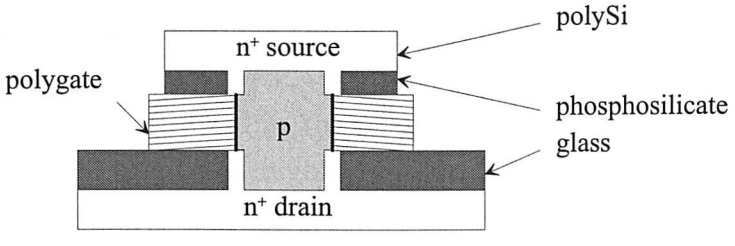


Figure 1.3: Vertical replacement-gate MOSFET

Contact to the drain is made through a buried n^+ layer and to the source through a n^+ polysilicon source pad. In this device, overlap capacitances are lower than in the device in figure 1.1 because it is determined by the thickness of the insulators between the PSG layers and the gate layer. However, parasitic bipolar transistor

action is still a problem because the source and drain extend across the entire width of the pillar. The authors in [42] propose a partial solution to this problem by using a shallow polysilicon source pad to create a leaky body contact.

The third category of vertical MOS transistor uses ion implantation [43–53] to create the source and drain regions, as illustrated in figure 1.4. In this device, the channel length is defined by the pillar height and the implant energy. The drain region behaves like an elevated source/drain. Ion implanted devices with threshold voltage adjustment using phosphorous silicate glass (PSG) as a dopant source have been proposed by Mori et al. [52, 53]. The parasitic bipolar gain is lower than that in the device shown in figure 1.1, because the drain does not penetrate across the width of the pillar. However, overlap capacitances are still a problem.

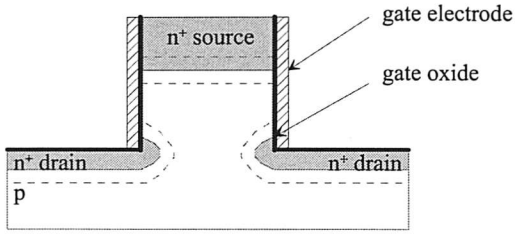


Figure 1.4: Vertical MOSFET based on ion implantation

The fourth category of vertical MOS transistor is appropriate for p-channel transistors and uses SiGe in the source. The insertion of SiGe into the source has the advantage of introducing a potential energy barrier that decreases drain induced barrier lowering and hence improves short channel effects [54–59]. Devices down to a channel length of 25nm have been fabricated [59]. Unfortunately, this technique can only be used in p-channel transistors because a potential energy barrier is not obtained in n-type SiGe. This device again has the disadvantage of a high overlap capacitance, though the SiGe layer has the benefit of reducing the parasitic bipolar gain.

Strained SiGe has also been used in the channels of vertical MOSFETs as reported in [55, 60–63]. The SiGe gives a higher surface mobility and as a result increased current drives of up to 100% and 50% over silicon control devices for PMOS and NMOS devices, respectively. To overcome the problem of oxidising SiGe the authors in [58, 64] deposited a silicon epitaxial layer (Si-cap) which is oxidised during gate oxidation.

The above literature review demonstrates that overlap capacitance and parasitic bipolar gain are two fundamental problems with vertical MOS transistors. This work addresses the reduction of overlap capacitance by using a fillet local oxidation

(FILOX) scheme to reduce the overlap capacitance between the polysilicon gate track and the source and drain. It is shown that the FILOX process is capable of reducing the overlap capacitance by a factor of 3.9 in vertical capacitors. Electrical characterisation of 105nm channel length NMOS transistors incorporating the FILOX process are presented and show a subthreshold slope of 111mV/decade. Parasitic bipolar gain is investigated through the use of a polycrystalline SiGe layer in the source. It is shown that the polySiGe source reduces the parasitic bipolar gain by up to a factor of 4.0. A dielectric pocket in combination with a retrograde channel is proposed to confine the source regions to the corners of the pillar and reduce short-channel effects.

Chapter 2

Theory of MOSFETs

In this chapter the fundamental theory of MOS devices will be discussed. The following considerations are made for a uniformly doped p-type semiconductor substrate.

2.1 Two-terminal MOS structure

A two-terminal metal oxide semiconductor (MOS) structure, also known as a MOS capacitor, consists of three layers namely a semiconductor layer, an embedded insulator layer and a conducting layer. Figure 2.1 illustrates the energy band diagram of an ideal two-terminal MOS structure.

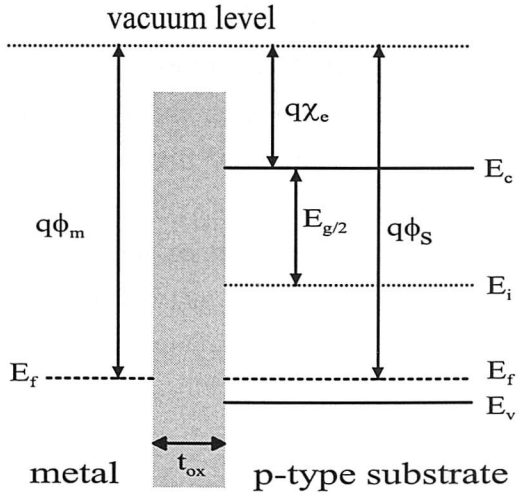


Figure 2.1: Band diagram of an idealised two-terminal MOS structure in flat band condition

In an idealised MOS structure the flat band voltage V_{FB} defined as the energy band difference between the metal work function ϕ_m and the silicon work function ϕ_s is

zero so that

$$qV_{FB} = q\phi_{ms} = q\,\phi_m - q\,\phi_s = q\,\phi_m - \left(q\,\chi_e + \frac{E_g}{2} + q\,\phi_f\right) = 0 \tag{2.1}$$

where ϕ_{ms} is the work function difference, q is the elementary charge, χ_e is the electron affinity, E_g the band gap between the conduction and valence band, E_v the energy level of the valence band, E_c the energy level of the conduction band, ϕ_f is named the Fermi potential and is the difference between the Fermi level E_f and the intrinsic energy level E_i divided by the electron charge q .

The Fermi potential of a p-type substrate can be calculated using the substrate doping concentration N_A and the intrinsic carrier concentration n_i as

$$\phi_f = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{2.2}$$

where k is the Boltzmann constant and T the temperature in Kelvin.

Applying a voltage to the semiconductor changes the charge in the substrate. Three modes of operation can be differentiated between namely accumulation, depletion and inversion, as shown in figure 2.2. In the case of a p-type substrate and a voltage $V_G < 0V$ applied to the gate contact, whilst the substrate is connected to ground, free charge carriers (holes) are accumulated under the insulation layer (oxide). Since free holes are moving towards the silicon surface layer, the surface charge is of the same type as in the substrate, but of higher concentration. This layer is called accumulation layer (figure 2.2a). The applied voltage causes a voltage drop over the oxide as well as bending the energy bands in the substrate. At the oxide/semiconductor interface the surface potential ψ_s can be found.

If $V_G > 0V$, free positive charge carriers are pushed away from the surface layer and thereby a depletion region of the width x_d is formed. This process is termed depletion (figure 2.2b).

In figure 2.2c a large voltage is applied to the gate. The surface layer inverts from p-type to n-type as nearly all free holes are pushed away from the surface layer and at the same time free electrons accumulate underneath the oxide. As soon as the intrinsic level E_i increases beyond the Fermi level E_f to obtain a negative charged surface layer, the surface is in weak inversion mode ($\psi_s \geq \phi_f$). At the onset of strong inversion the surface potential barrier ψ_s is defined by $\psi_s = 2\,|\phi_f|$ as shown in figure 2.3.

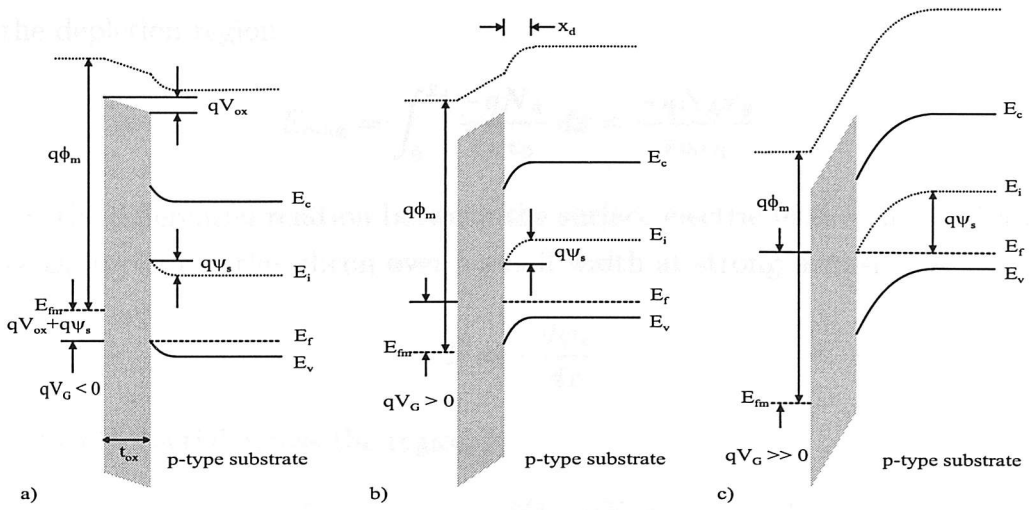


Figure 2.2: One-dimensional MOS structure a) accumulation ($\psi_s < 0$) b) depletion ($0 < \psi_s < \phi_f$) c) onset of weak inversion ($\psi_s = \phi_f$)

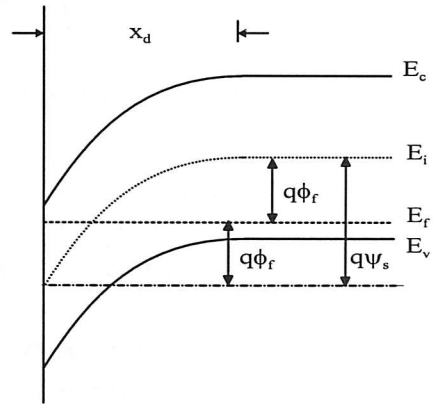


Figure 2.3: Energy band diagram showing the onset of strong inversion ($\psi_s = 2\phi_f$)

The gate voltage to bring the surface layer into strong inversion is termed the threshold voltage V_T. In order to calculate the threshold voltage, first the depletion width x_d of a doped semiconductor needs to be calculated. This can be achieved by solving the one-dimensional Poisson's equation which relates the electric field E(x) to the charge density $\rho(x)$ as follows

$$\frac{dE(x)}{dx} = \frac{\rho(x)}{\epsilon_{Si}\epsilon_0} \quad for\ 0 < x < x_d \tag{2.3}$$

where ϵ_0 is the dielectric constant in vacuum and ϵ_{Si} is the dielectric constant of silicon [65].

The charge density equals the number of acceptors in the substrate $\rho(x) = -qN_A$ for an abrupt junction. The maximum field can now be calculated by integrating

over the depletion region

$$E_{max} = \int_0^{x_d} \frac{-qN_A}{\epsilon_{Si}\epsilon_0}\, dx = \frac{-qN_A x_d}{\epsilon_{Si}\epsilon_0} \tag{2.4}$$

Further, the differential relation between the surface electric field E at $x = 0$ and the voltage ψ_s applied to the silicon over a small width at strong inversion is

$$E = -\frac{d\psi_s}{dx} \tag{2.5}$$

The surface potential across the region is

$$\psi_s = -\int_0^{x_d} E\, dx = -\int_0^{x_d} \frac{-qN_A x_d}{\epsilon_{Si}\epsilon_0}\, dx = \frac{qN_A x_d^2}{2\epsilon_{Si}\epsilon_0} \tag{2.6}$$

The depletion layer width for a p-type semiconductor can hence be calculated as

$$x_d = \sqrt{\frac{2\epsilon_{Si}\epsilon_0|\psi_s|}{qN_A}} \tag{2.7}$$

The substrate depletion charge Q_B density at the onset of strong inversion ($\psi_s = 2|\phi_f|$) can be written as

$$Q_B = -qN_A x_d = -qN_A\sqrt{\frac{2\epsilon_{Si}\epsilon_0\ 2|\phi_f|\ qN_A}{q^2N_A^2}} = -\sqrt{4qN_A\epsilon_{Si}\epsilon_0|\phi_f|} \tag{2.8}$$

The applied gate-substrate voltage drops over the oxide as well as over the depletion region. The threshold voltage V_T is therefore

$$\begin{aligned} V_T &= V_{ox} + |\psi_s| = -\frac{Q_B}{C_{ox}} + 2|\phi_f| \\ &= \frac{\sqrt{4qN_A\epsilon_{Si}\epsilon_0|\phi_f|}}{C_{ox}} + 2|\phi_f| \end{aligned} \tag{2.9}$$

where V_{ox} is the oxide voltage.

Equation 2.9 shows that varying the substrate doping concentration changes the threshold voltage. This knowledge can be used to explicitly influence the threshold voltage in order to change the on/off voltage of the transistor. The desired threshold voltage is typically ± 0.3V for n- and p-channel MOSFETs, respectively.

2.1.1 Work Function Difference

In practice, the work function in the silicon is different than the work function in the gate. This is certainly true for polysilicon, which is commonly used as a gate material in CMOS, as shown in figure 2.4. In this case the Fermi potential ϕ_{poly}, assuming non-degeneration, of the n-type poly silicon can be written as

$$\phi_{poly} = \frac{kT}{q} \ln\left(\frac{n_i}{N_D}\right) \tag{2.10}$$

where N_D is the doping concentration of the poly silicon gate.

However, if the doping concentration of the polysilicon gate is higher than 10^{18}-10^{19}cm^{-3} the Fermi level is equal to the energy level of the conduction band, so that $E_f \simeq E_c$ [66].

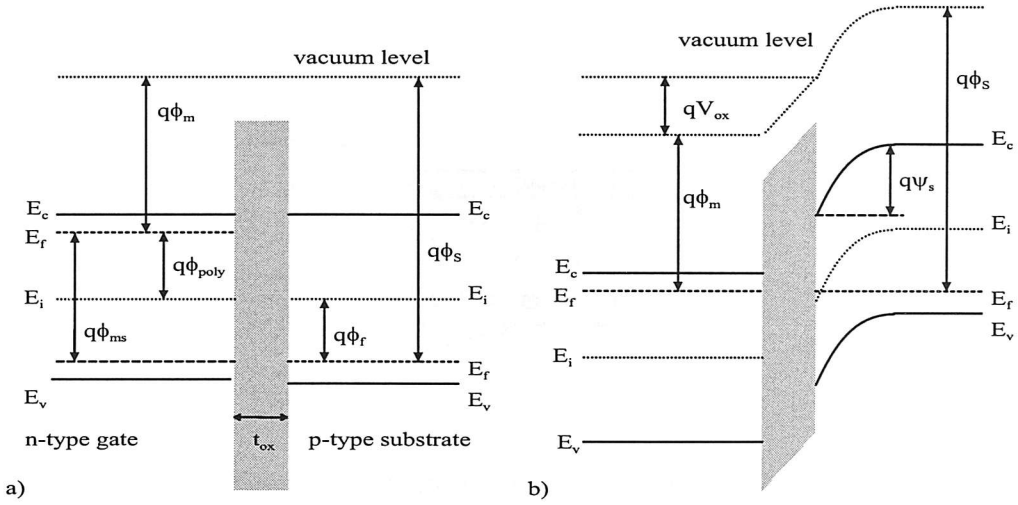


Figure 2.4: Energy band diagram of a MOS structure with degenerated polysilicon a) flat band condition b) zero bias

Figure 2.4a illustrates the semiconductor/oxide semiconductor stack in flat band. The work function difference in this case is

$$q\phi_{ms} = -\left(q\phi_{poly} + q\phi_f\right) \tag{2.11}$$

If the gate and the substrate are under zero bias condition the semiconductor is depleted as shown in figure 2.4b. Here, the Fermi energy levels E_f of the gate and the substrate are aligned and the MOS structure is in weak inversion.

The threshold voltage can now be written as

$$V_T = \frac{\sqrt{4qN_A\epsilon_{Si}\epsilon_0|\phi_f|}}{C_{ox}} + 2|\phi_f| + V_{FB} \tag{2.12}$$

2.1.2 Oxide Interface Traps

The oxide charge Q_{ox} is the inherent charge embedded between the gate and semiconductor and is strongly affected by the gate oxidation conditions as well as the crystal orientation. In the previous section the voltage to achieve flat band V_{FB} was only dependent on the work function difference ϕ_{ms} so that $V_{FB} = \phi_{ms}$.

The flat band voltage needs to be modified to take care of charges in the silicon/gate oxide interface. These charges are namely interface-trapped charges, fixed-oxide charges, oxide-trapped charges and mobile ionic charge carriers as shown in figure 2.5.

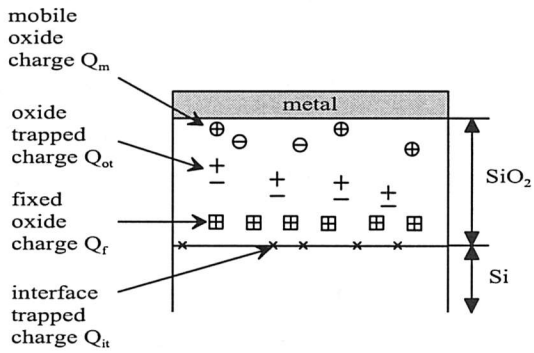


Figure 2.5: Oxide traps in the gate oxide

Interface-trapped charges Q_{it}, with energy states in the silicon forbidden band gap are located at the Si-SiO_2 interface. The interface trap density is orientation dependent. A variation in the order of one magnitude can be found in <100> orientation compared with silicon in <111> orientation. Sze [67] reports values of Q_{it} in the region of $10^{10}cm^{-2}$.

Fixed-oxide charges Q_f are also depending on the oxidation and annealing conditions. Typical densities for a <100> surface are $10^{10}cm^{-2}$ and for a <111> surface $5 \times 10^{10}cm^{-2}$.

Oxide-trapped charges Q_{ot} are caused by defects in the SiO_2 layer due to X-ray radiation or high energy electrons.

Contamination during the oxidation process can leave alkali ions as mobile carriers in the silicon oxide causing mobile ionic charges Q_m. Assuming that all charges are very close to the oxide/silicon interface, the flat band voltage including the above discussed oxide charges can be written as

$$V_{FB} = \phi_{ms} - \frac{Q_{it} + Q_f + Q_m + Q_{ot}}{C_{ox}} \tag{2.13}$$

2.1.3 Small-signal capacitance

So far the two terminal MOS structure has been evaluated under static conditions. In this section the ac signal behaviour will be investigated. The capacitance C_{ox} between two plates of a parallel plate capacitor is given by

$$C_{ox} = \frac{\epsilon_{ox}\ \epsilon_0\ A_{ox}}{t_{ox}} \tag{2.14}$$

where t_{ox} is the thickness of the oxide and A_{ox} the area.

Equation 2.14 is valid to calculate the capacitance in accumulation as shown in figure 2.6. If the two-terminal MOS structure is in depletion condition, the oxide capacitance and the capacitance of the depletion region are in series. The overall capacitance under this condition is

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d} = \frac{C_{ox} + C_d}{C_{ox}C_d} \tag{2.15}$$

where C_d is the depletion capacitance.

At high measurement frequencies, as the gate voltage is increased the capacitance drops to its minimum value so that the capacitance is given by equation 2.15. This is because the inversion layer charge (minority charge carriers) cannot keep up with the fast changing voltage applied to the device and only the depletion charge can respond to the applied ac-signal. The inversion layer charge can only be changed by the mechanism of thermal generation and recombination which is a relatively slow processes.

At low measurement frequencies a different behaviour is observed because the inversion layer charge can follow the variation of the applied signal. In this case the depletion charge is constant. All of the applied voltage drops across the oxide so that $C=C_{ox}$ as in accumulation. Thus, if the capacitance is plotted as a function of V_G, a graph similar to figure 2.6 is obtained.

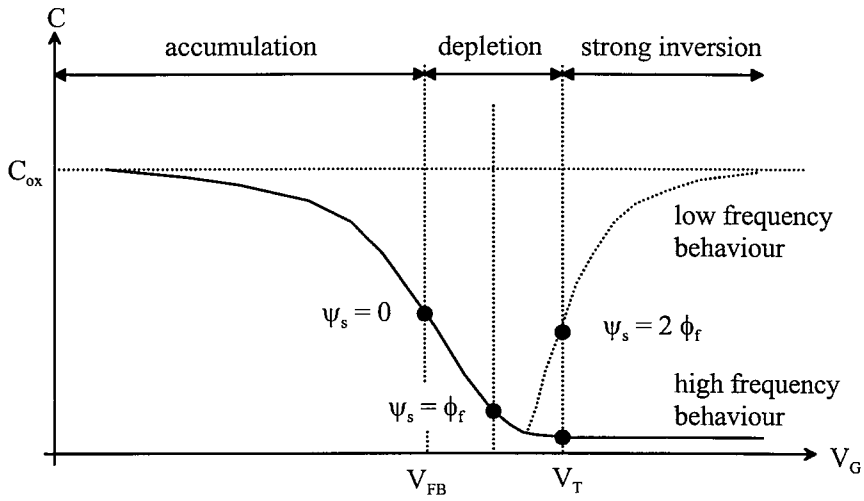


Figure 2.6: Capacitance of a two-terminal MOS structure as function of gate voltage. dotted line: deviation found at low frequencies

2.2 Four-terminal MOS structure

The four-terminal MOS structure or MOSFET is similar to a two-terminal MOS structure with the addition of source and drain regions. Two types of MOS transistors can be distinguished, namely enhancement mode and depletion mode devices. In this section the enhancement mode MOSFET will be discussed. For the following description of the device, it is assumed that the source is tied to ground.

Figure 2.7a shows a zero biased gate, source, drain and substrate. Around the $n^+ - p$ junctions, there is a small depletion region. The resistance between source and drain is very high, as the two pn-junctions are of opposite polarity.

Applying a gate voltage V_G of $V_{FB} < V_G < V_T$ depletes the p-type semiconductor underneath the gate oxide. The space charge region around source and drain now extends under the gate. Increasing the gate voltage so that $V_G > V_T$ adds to the already existing depletion region an inversion layer connecting the source and drain regions. However, since there is no voltage difference between the source and drain, no current can flow and $I_D = 0$.

2.2.1 Linear operation

A positive gate voltage V_G of $V_{FB} < V_G < V_T$ as well as a positive voltage connected to the drain ($V_{DS} > 0$) forms a depletion layer underneath the gate oxide. Since the

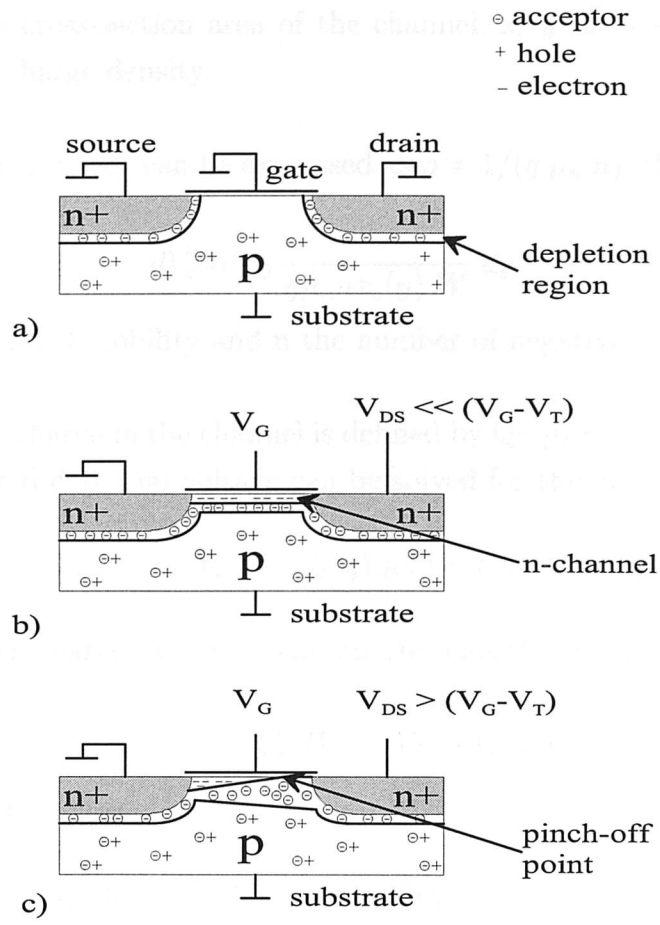


Figure 2.7: Four terminal MOSFET structure a) with zero biased gate b) in cutoff mode c) in saturation

gate voltage is not sufficient to create an inversion layer, no channel exists to connect the source and drain regions. Without taking leakage currents into account it can be said that I_D=0. This mode of operation is called the cutoff mode. For the condition of $V_G > V_T$ and $V_{DS} < (V_G - V_T)$, a channel is formed, connecting source and drain as shown in figure 2.7b. The MOSFET is said to be nonsaturated. Due to the inversion layer, free electrons lower the drain/source resistance, which is now much less than in depletion mode and, furthermore, can be controlled by the positive gate voltage. This mode of operation is called linear mode. The maximum channel voltage ($V_{c,max}(y = L) = V_{DS}$) can be found at the drain and drops to $V_{c,min}$(y=0)=0V at the source.

It is assumed that the channel is of constant length L, and of constant width W and its thickness changes between source and drain. In the following, the drain current for the linear region will be derived. The differential voltage drop in the inversion channel, parallel to the surface is defined as

$$dV_c = I_D\, dR = I_D \frac{\rho}{A_c(y)}\, dy = I_D \frac{\rho}{x_c(y)\, W}\, dy \tag{2.16}$$

where $A_c(y)$ is the cross-section area of the channel, $x_c(y)$ is the channel thickness and ρ the channel charge density.

Since the channel resistivity can be expressed as $\rho = 1/(q\ \mu_n\ n)$, the differential voltage is

$$dV_c = I_D \frac{1}{q\mu_n n x_c(y)\ W}\ dy \tag{2.17}$$

where μ_n is the channel mobility and n the number of negative charge carriers.

The inversion layer charge in the channel is defined by $Q_I(y) = -q\ n\ x_c(y)$. Therefore the equation of the differential voltage can be solved for the drain current, to

$$I_D\ dy = -Q_I(y)\ \mu_n\ W\ dV_c \tag{2.18}$$

The inversion layer charge is dependent on the effective voltage across the MOS capacitor so that

$$Q_I(y) = -C_{ox}(V_G - V_T - V_c(y)) \tag{2.19}$$

The drain current becomes

$$I_D\ dy = C_{ox}(V_G - V_T - V_c(y))\ \mu_n\ W\ dV_c \tag{2.20}$$

Integrating the left term of the equation over the given channel length L, whilst integrating the right term of equation 2.20 over the voltage drop across the channel gives

$$\begin{aligned} I_D \int_0^L dy &= C_{ox}\ \mu_n\ W \int_0^{V_{DS}} (V_G - V_T - V_c(y))\ dV_c \\ I_D\ L &= C_{ox}\ \mu_n\ W \left((V_G - V_T)\ V_{DS} - \frac{1}{2}\ V_{DS}^2 \right) \end{aligned} \tag{2.21}$$

With

$$\beta = C_{ox}\ \mu_n \frac{W}{L} \tag{2.22}$$

the process transconductance parameter, equation 2.21 becomes the equation for the drain current in linear mode.

$$I_D = \beta \left((V_G - V_T)V_{DS} - \frac{1}{2}\ V_{DS}^2 \right) \tag{2.23}$$

2.2.2 Saturation operation

The drain current cannot be continuously increased. At some point ($V_{DS} = V_G - V_T$) the channel pinches off as illustrated in figure 2.7c. The MOSFET is now in saturation

mode. The onset of saturation can be approximated by finding the maximum current using

$$\frac{dI_D}{dV_{DS}} = 0 = \beta(V_G - V_T - V_{DS}) \tag{2.24}$$

At this point the drain voltage is

$$V_{DS,sat} = V_G - V_T \tag{2.25}$$

The current previously calculated for the linear region in equation (2.23) now changes, after substituting the drain voltage by its saturation value to

$$I_D = \frac{1}{2}\beta(V_G - V_T)^2 \tag{2.26}$$

Equation 2.26 is valid for long channel devices and does not take velocity saturation found in short channel devices into account.

Figure 2.8 illustrates the output characteristic of a MOSFET based on equation 2.23 and 2.26. Furthermore, figure 2.8 shows the locus of $V_{DS,sat}$ where the current reaches its maximum value.

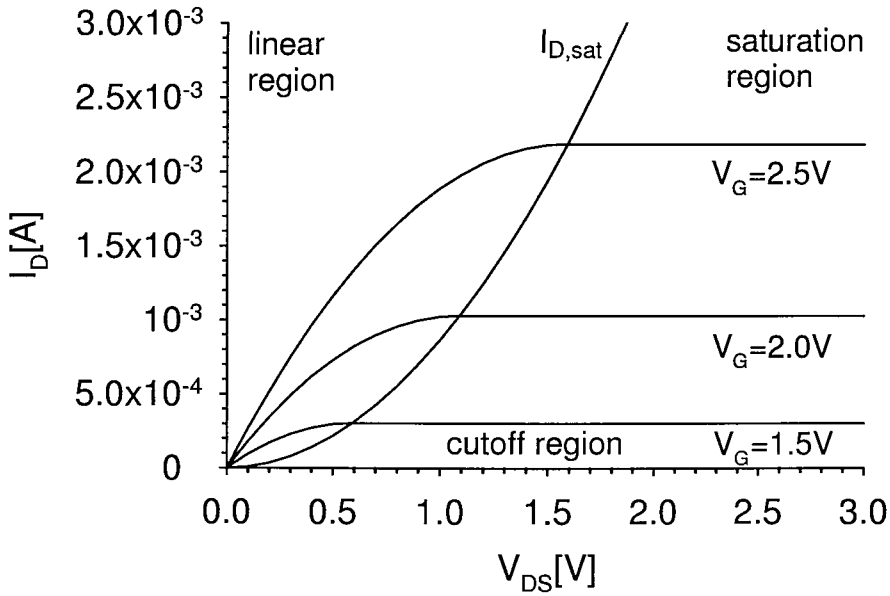


Figure 2.8: Idealised output characteristic of a 100nm channel length (W=1μm) MOSFET

2.2.3 Body bias effect

Biasing the substrate, changes the voltage across the depletion layer and therefore its thickness and hence the threshold voltage. The depletion layer charge (see equa-

tion 2.8) changes to

$$Q_B = -\sqrt{4\, qN_A\epsilon_{Si}\epsilon_0\,(|\phi_f| + V_B)} \tag{2.27}$$

where V_B is the substrate bias voltage.

The change in threshold voltage can now be determined as

$$\Delta V_{Tbias} = \frac{\sqrt{4\, qN_A\epsilon_{Si}\epsilon_0\ (|\phi_f| + V_B)}}{C_{ox}} - \frac{\sqrt{4\, qN_A\epsilon_{Si}\epsilon_0\ |\phi_f|}}{C_{ox}} \tag{2.28}$$

2.2.4 Detailed MOSFET analysis

For the previous analysis it was assumed that the threshold voltage V_T was constant along the channel. However, in reality the channel voltage $V_c(y)$ changes the substrate depletion charge density Q_B. Assuming ($V_S = V_B = 0$) the threshold voltage can be written as

$$V_T(V_c) = \frac{1}{C_{ox}}\sqrt{2\, q\epsilon_{Si}\epsilon_0 N_A(2|\phi_f| + V_c)} + 2|\phi_f| + V_{FB} \tag{2.29}$$

The nonsaturated drain current can be written as

$$\begin{aligned} I_D &= \beta \int_0^{V_{DS}} \{(V_G - V_{FB} - 2|\phi_f|) - V_c \\ &\quad - \frac{1}{C_{ox}}\sqrt{2q\epsilon_{Si}\epsilon_0 N_A\,(2|\phi_f| + V_c)}\ \}\, dV_c \end{aligned} \tag{2.30}$$

Integrating the above equation leads to the following equation

$$\begin{aligned} I_D &= \beta\Bigg((V_G - V_{FB} - 2|\phi_f|)\, V_{DS} - \frac{1}{2}V_{DS}^2 \\ &\quad - \frac{2}{3C_{ox}}\sqrt{2q\epsilon_{Si}\epsilon_0 N_A}\{(2|\phi_f| + V_{DS})^{3/2} - (2|\phi_f|)^{3/2}\}\Bigg) \end{aligned} \tag{2.31}$$

At the peak value of the nonsaturation current ($dI_D/dV_{DS} = 0$) the saturation voltage is

$$\begin{aligned} V_{DS,sat} &= V_G - V_{FB} - 2|\phi_f| \\ &\quad - \frac{q\epsilon_{Si}\epsilon_0 N_A}{C_{ox}^2}\left(\sqrt{1 + \frac{2C_{ox}^2}{q\epsilon_{Si}\epsilon_0 N_A}(V_G - V_{FB})} - 1\right) \end{aligned} \tag{2.32}$$

Substituting equation 2.32 into equation 2.31 allows a more accurate calculation of the drain current in the nonsaturated region. In comparison with equation 2.23, the values of I_D in the detailed analysis tend to be lower than in the simple equations.

2.2.5 Subthreshold region

When $\phi_f < \psi_s < 2\psi_f$ the semiconductor surface is in weak inversion. At this point the minority carrier concentration is still lower than the substrate doping concentration N_A. The corresponding drain current I_D is termed subthreshold current. The subthreshold current is of particular importance for low-power applications as it determines the off-current [67].

In weak inversion the subthreshold current is dominated by diffusion instead of drift. Due to the arrangement of the MOSFET, I_{Dsub} can be approximated in the same way as the collector current of an npn-bipolar transistor with homogeneous base doping to

$$I_{Dsub} = -qA_{sub}D_n\frac{dn}{dy} = qA_{sub}D_n\frac{n(0) - n(L)}{L} \tag{2.33}$$

where A_{sub} is the cross-section of current flow, $D_n = \mu_n kT/q$ the electron diffusion coefficient and n(0) and n(L) the electron densities in the channel at the source and the drain.

The area A_{sub} of current flow is given by the width W of the device and the effective channel thickness x_{ceff}. The effective channel thickness can be calculated as

$$x_{ceff} = \frac{kT}{q}E_s \tag{2.34}$$

where E_s is the electric field at the silicon surface in weak-inversion.

E_s is given by

$$E_s = \frac{-Q_B}{\epsilon_{Si}\epsilon_0} = \sqrt{\frac{2qN_A\phi_{ss}}{\epsilon_{Si}\epsilon_0}} \tag{2.35}$$

where ϕ_{ss} is the surface potential at the source.

The electron densities are given by

$$\begin{aligned} n(0) &= n_i \exp\left(\frac{q(\phi_{ss} - \phi_f)}{kT}\right) \\ n(L) &= n_i \exp\left(\frac{q(\phi_{ss} - \phi_f - V_{DS})}{kT}\right) \end{aligned} \tag{2.36}$$

Substituting equation 2.36 into equation 2.33 gives

$$I_{Dsub} = \frac{qA_{sub}D_n n_i \exp\left(\frac{-q\phi_f}{kT}\right)}{L}\left(1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right)\exp\left(\frac{q\phi_{ss}}{kT}\right) \tag{2.37}$$

The subthreshold swing is defined as

$$S = \left(\frac{d(\log_{10} I_D)}{dV_G} \right)^{-1} \tag{2.38}$$

Figure 2.9 shows the idealised subthreshold characteristic based on equation 2.37. For the simulation it was assumed that the surface potential at the source is equal to the surface potential given by $V_G - V_{FB}$. The extracted subthreshold slope S was 60mV/dec.

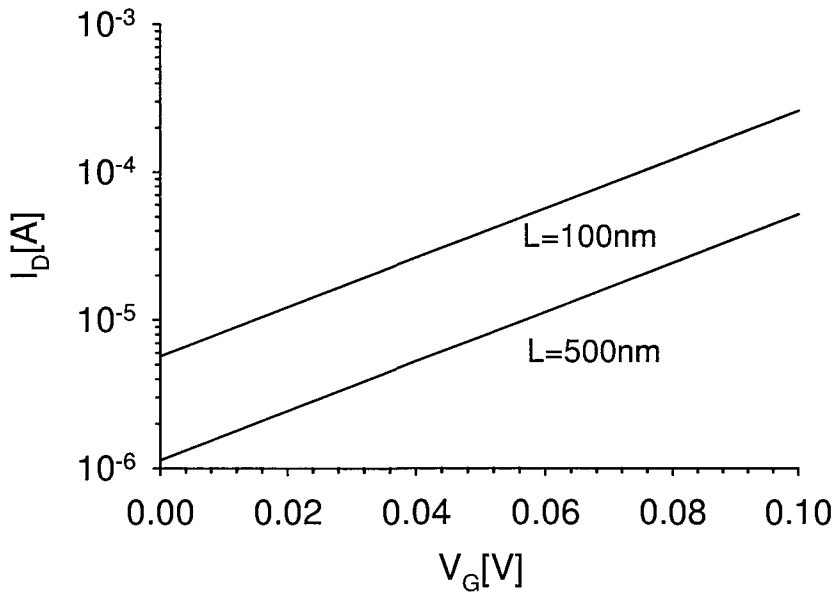


Figure 2.9: Idealised subthreshold characteristic of a 100 and 500nm channel length MOSFET

Equation 2.37 shows the linear relation between the channel length L and the drain current I_{Dsub} which is illustrated in figure 2.9. In the subthreshold region a higher drain current can be observed in short channel devices compared to long channel MOSFETs.

2.2.6 Short channel and narrow-width effects

The equations discussed in the previous section are fairly accurate for describing large devices, they cannot be applied to small-geometry MOSFET devices.

Charge sharing effects

A significant fraction of total substrate depletion charge underneath the gate originates from the pn-junctions. This charge must be subtracted from the threshold

voltage expression since it is independent from the applied gate voltage. For low V_{DS} the depletion region thickness can be considered constant throughout the channel. The depletion charge controlled by the gate can be modelled as a trapezoidal volume. For this case the ratio $-Q_B/C_{ox}$ changes due to the geometry dependence to

$$-\frac{Q_B L_{eff}}{C_{ox} L} \tag{2.39}$$

where L_{eff} is the effective channel length.

The bottom of the trapezoid has the same length L as the channel, whilst the top of the trapezoid has a length of L_1, such that

$$L = L_1 + 2\,\Delta L \tag{2.40}$$

where ΔL is the lateral extent of the depletion width at the source and drain as shown in figure 2.10a.

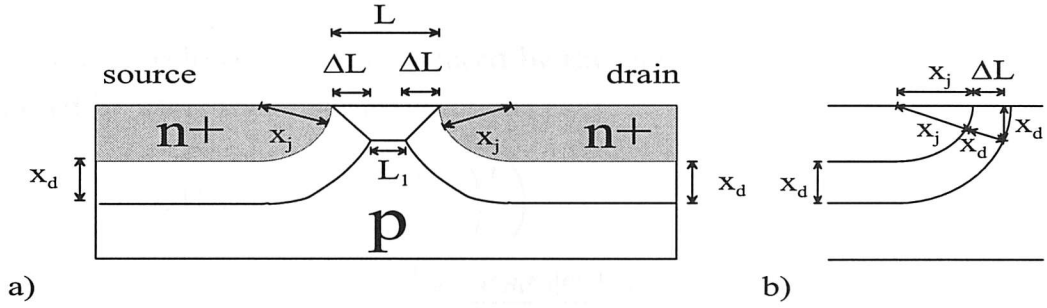


Figure 2.10: Schematic diagram of a charge sharing model showing the depletion regions of a short channel device.

The effective channel length can be written as

$$L_{eff} = \frac{L + L_1}{2} = L - \Delta L \tag{2.41}$$

Substituting equation 2.41 into equation 2.39 gives

$$-\frac{Q_B}{C_{ox}}\left(\frac{L - \Delta L}{L}\right) = -\frac{Q_B}{C_{ox}}\left(1 - \frac{\Delta L}{L}\right) \tag{2.42}$$

Assuming that the pn-junctions are shaped like quarter-circular arcs and extend a distance x_d into the p-substrate the depletion depth for the source and drain, respectively, can be expressed as

$$x_d = \sqrt{\frac{4\epsilon_{Si}\epsilon_0}{qN_A}\,|\phi_f|} \tag{2.43}$$

In order to calculate ΔL of the triangle shown in figure 2.10b, we can say

$$(x_j + \Delta L)^2 + x_d^2 = (x_j + x_d)^2 \tag{2.44}$$

where x_j is the junction depth of the n^+ implant.

The solution of this quadratic is

$$\Delta L = -x_j + \sqrt{x_j^2 + 2\, x_j x_d} \tag{2.45}$$

The short-channel threshold voltage V_{TSCE} can now be calculated as

$$\begin{aligned} V_{TSCE} &= V_{FB} + \frac{\sqrt{4qN_A\epsilon_{Si}\epsilon_0|\phi_f|}}{C_{ox}}\left(1 - \frac{\Delta L}{L}\right) + 2|\phi_f| \\ &= V_{FB} + \frac{\sqrt{4qN_A\epsilon_{Si}\epsilon_0|\phi_f|}}{C_{ox}}\left(1 - \frac{x_j}{L}\left(\sqrt{1 + \frac{2x_d}{x_j}} - 1\right)\right) \\ &\quad +2|\phi_f| \end{aligned} \tag{2.46}$$

The threshold voltage reduction induced by the short-channel effect ΔV_{TSCE} can be computed by using the above assumptions as

$$\begin{aligned} \Delta V_{TSCE} &= \frac{Q_B}{C_{ox}}\left(-\frac{\Delta L}{L}\right) \\ &= -\frac{\sqrt{4\, qN_A\epsilon_{Si}\epsilon_0|\phi_f|}}{C_{ox}}\,\frac{x_j}{L}\left(\sqrt{1 + \frac{2x_d}{x_j}} - 1\right) \end{aligned} \tag{2.47}$$

Channel Length Modulation

Increasing the drain voltage beyond the onset of saturation ($V_{DS} > V_{DS,sat}$) moves the pinch-off point away from the drain towards the source. This movement of the pinch-off point is called channel length modulation. It should be noted, that the termination of the channel at the pinch-off point does not shut off the current. It rather injects carriers travelling from the source towards the drain into the drain depletion region. Since the voltage drop from the pinch-off point to the source is still $V_{DS,sat}$, the portion of the applied drain voltage beyond $V_{DS} - V_{DS,sat}$ is dropped across the depletion layer at the drain. Compared to the onset of pinch-off, the same voltage is now dropped across a smaller channel length L' so that L'<L as illustrated in figure 2.11.

The resulting drain current will increase slightly. This effect can be analytically modelled by approximating the inversion layer charge $Q_I(L') = 0$, which implies that

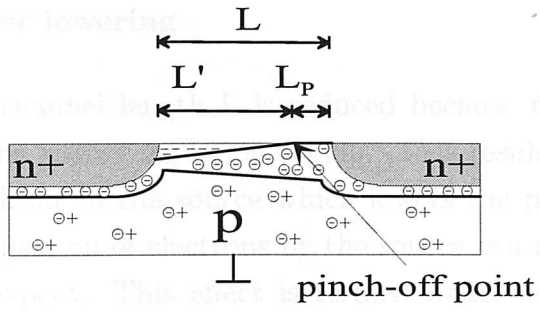


Figure 2.11: Channel under pinch-off condition

the channel voltage at L' is $V_{DS,sat}$. The pinch-off length L_P can be calculated using the approximation of a depletion region, whereby the voltage drop across this region is $V_{DS} - V_{DS,sat}$, to

$$L_P \simeq \sqrt{\frac{2\epsilon_{Si}\epsilon_0}{qN_A}\ (V_{DS} - V_{DS,sat})} \tag{2.48}$$

The relation of the saturation current and the channel length modulation can now be approximated as

$$I_D \simeq \frac{I_{D,sat}\ L}{L - L_P} = \frac{I_{D,sat}}{\left(1 - \frac{L_P}{L}\right)} \tag{2.49}$$

Figure 2.12 illustrates the effect of channel length modulation. Simulating the effect of channel length modulation using equation 2.49 shows that the drain current does not saturate. Increasing the drain/source voltage V_{DS} above $V_{DS,sat}$ increases the drain current I_D in the saturation region.

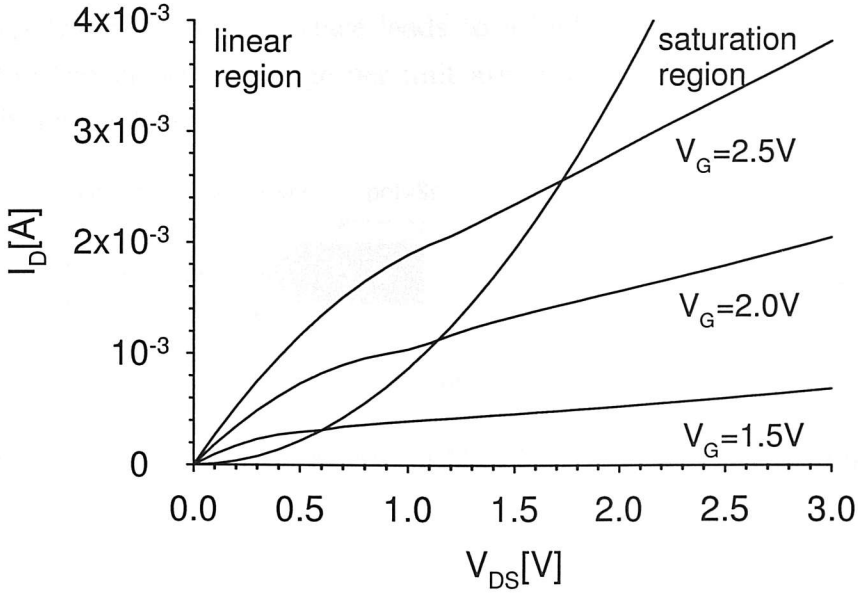


Figure 2.12: Output characteristic of a 100nm channel length (W=1μm) MOSFET with channel length modulation

Drain induced barrier lowering

As V_{DS} increases the channel length L is reduced because the drain depletion region moves closer to the source depletion region. This results in a significant field penetration from the drain to the source which lowers the potential barrier at the source. An increased injection of electrons by the source can now conduct more current than one would expect. This effect is termed drain-induced barrier lowering (DIBL) [68]. Furthermore, the depletion charge density Q_B of short channel devices, where the geometry of the depletion region is approximated as a trapezoid as shown in figure 2.10, is lower than for long channel devices, where a rectangular depletion region was assumed. This lowers the threshold voltage V_{TSCE} for increasing drain voltages V_{DS}.

Punch-through effect

Punch through occurs when, due to the drain applied voltage V_{DS}, both depletion regions merge and $V_G < V_T$. In this case, where L=2ΔL, the gate loses control over the drain current I_D [69]. To overcome the effect of punch-through, higher doping of the substrate is required to minimise the depletion region.

Narrow-width effects

The definition of the active area and the resulting depletion region beneath the silicon/oxide/polysilicon layer interface leads to a higher threshold voltage caused by an increase of the substrate charge per unit area Q_B. Two different approximations are shown in figure 2.13.

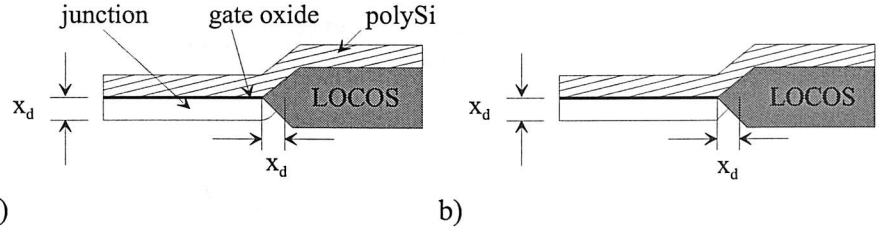


Figure 2.13: Narrow width effect of lateral MOSFETs a) circle approximation b) triangular approximation

The narrow-width threshold voltage V_{TNWE} can be calculated as

$$V_{TNWE} = V_{FB} + \frac{\sqrt{4qN_A\epsilon_{Si}\epsilon_0|\phi_f|}}{C_{ox}}\left(1 + \frac{K\ x_d}{W}\right) + 2|\phi_f| \qquad (2.50)$$

where K is the form factor depending on the chosen model shown in figure 2.13 for both sides of the nonuniformly shaped depletion regions.

Table 2.1 shows different values for the form factor K.

	circle	**triangular**
shape		
formfactor K	$\pi/4$	$x_d/2$

Table 2.1: Form factors for modelling the narrow width effect

The term of the threshold voltage V_T can be modified by adding the narrow-width effect voltage ΔV_{TNWE}

$$\Delta V_{TNWE} = \frac{1}{C_{ox}} \sqrt{2q\epsilon_{si}\epsilon_0 N_A(2|\phi_f|)} \left(\frac{K\, x_d}{W}\right) \tag{2.51}$$

2.2.7 Parasitic bipolar effects

Reducing the channel length L whilst keeping the drain/source voltage V_{DS} constant increases the maximum electric field experienced by the charge carriers (electrons) near the drain region. Energetic charge carriers can create new electron-hole pairs by impact ionisation as illustrated in figure 2.14.

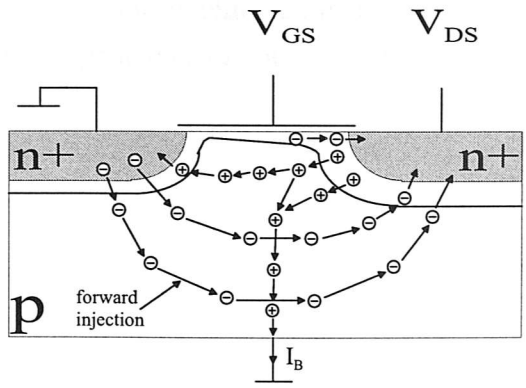


Figure 2.14: Parasitic bipolar transistor action

Holes injected into the substrate will flow to the substrate contact where they will give rise to a substrate current. This substrate current flow will give rise to voltage drops in the substrate that can cause the forward biasing of the substrate/source junction. In this case, electrons are injected into the substrate which will be collected

by the drain. This effect is known as parasitic bipolar transistor action.

Parasitic bipolar transistor action can have significant effects when the substrate contact is remote from the drain or when the substrate is floating. In the latter case, floating body effects occur that seriously influence the behaviour of the device.

The severity of the parasitic transistor action is determined by the gain of the bipolar transistor. The gain of a bipolar transistor is given by the ratio of the collector current I_C and the base current I_B as follows

$$\beta = \frac{I_C}{I_B} \tag{2.52}$$

The base current I_B of the bipolar npn-transistor shown in figure 2.14 is given by [70]

$$I_B = \frac{q\ A\ D_{pe}\ n_i^2}{W_E\ N_{Deff}} \exp\left(\frac{q\ V_{be}}{kT}\right) \tag{2.53}$$

where D_{pe} is the hole diffusion coefficient in the emitter (source), W_E is the emitter depth, N_{Deff} is the effective donor concentration in the emitter and V_{be} the base emitter voltage which is caused by the potential shift in the substrate.

The collector current I_C is given by

$$I_C = \frac{q\ A\ D_{nb}\ n_i^2}{W_B\ N_{Abeff}} \exp\left(\frac{q\ V_{be}}{kT}\right) \tag{2.54}$$

where D_{nb} is the electron diffusion coefficient in the base, W_B the width of the base and N_{Abeff} the effective acceptor concentration in the base.

Substituting equation 2.53 and 2.54 into equation 2.52 gives the gain of the parasitic npn-bipolar transistor as follows

$$\beta = \frac{D_{nb} W_E N_{Deff}}{D_{pE} W_B N_{Abeff}} \tag{2.55}$$

Chapter 3

Parasitic capacitances in vertical MOSFETs

3.1 Introduction

This chapter considers parasitic capacitances in vertical MOS transistors. In general two types of parasitic capacitances can be found in MOSFET devices, namely overlap and junction capacitance [66]. A critical theoretical comparison between the parasitic capacitances of idealised lateral devices, single gate and surround gate vertical devices is presented. A novel process called FILOX is introduced in section 3.3.4, which reduces overlap capacitance in vertical devices. The discussed vertical device concepts are based on a device in which the gate is defined after the source/drain implant (gate after implant (GAI) approach). A comparison with vertical devices in which the gate is defined before the source/drain implant (gate before implant (GBI) approach) is presented in section 3.4.2. Finally, a new device concept, namely the dielectric pocket vertical MOSFET, is discussed in section 3.6.

3.2 Assumptions

In this section assumptions are made for the comparisons of parasitic capacitances presented. These are partitioned in technological and in layout considerations.

3.2.1 Technological considerations

A number of different types of devices are considered namely lateral MOSFETs, vertical single gate and vertical surround gate devices. The following technological considerations were taken into account when calculating the parasitic capacitances.

T1 All devices are isolated with an oxide thickness t_s of 300nm by shallow trench isolation (STI).

T2 All polysilicon gates are degenerately doped and have a thickness of 40nm.

T3 The SiO_2 gate oxide thickness t_{ox} is 2nm.

T4 The source/drain junction depth x_j and the lateral diffusion of the source/drain junctions are 20nm. This value is typical of a lightly-doped drain (LDD) implant for a 100nm transistor.

T5 The polysilicon interconnect track up to the edge of the active area is not considered in the calculations as it is assumed that the resulting overlap capacitances are the same for both, lateral and vertical devices.

T6 The doping concentrations are uniform in the source, drain and substrate.

T7 The source, drain and substrate doping concentrations are $5.0\times10^{20}cm^{-3}$, $5.0\times10^{20}cm^{-3}$ and $1.0\times10^{18}cm^{-3}$, respectively.

T8 The as-drawn channel length L is 100nm. When the 20nm source/drain lateral diffusion is considered, this gives an electrical channel length L_{eff} of 60nm.

As will be discussed later, for the vertical transistor some additional technology steps are performed, in particular a LOCOS process referred to as FILOX process. The assumptions associated with this process and other technology issues associated with the pillar formation are as follows

T9 The FILOX oxide thickness is 40nm (t_{vLox}).

T10 The insulator on top of the pillar is assumed to be 40nm thick (t_{pInox}).

T11 The FILOX lateral bird's beaks at the bottom of the pillar is assumed to be 40nm long (L_{do2}).

T12 The FILOX vertical bird's beak at the top of the pillar is assumed to be 20nm long (L_{so}).

T13 The FILOX vertical bird's beak at the top of the pillar is assumed to be 40nm thick (t_{hLox}).

3.2.2 Layout considerations

Industry-based layout rules [71] at the 100nm technology node were used for the parasitic capacitance calculation. These layout rules where consistently applied to both lateral and vertical devices. The layout rules are as follows

L1 Minimum contact size 160×160nm.

L2 Minimum contact to active area spacing 20nm.

L3 Minimum contact to contact spacing 200nm.

L4 Minimum metal over contact overlap 10nm.

L5 Minimum metal to metal spacing 180nm

L6 Minimum polySi gate to contact spacing 80nm.

L7 Minimum gate track width W 220nm.

L8 Minimum gate over STI overlap W_s 200nm.

L9 Minimum gate over pillar overlap W_s 200nm.

L10 Minimum polySi gate to pillar edge spacing on pillar top 40nm.

L11 Pillar to active area spacing L_{do} (single gate) 100nm.

L12 Pillar to active area spacing L_{do} (surround gate) 140nm.

L13 Minimum polySi track width for polySi fillet contact W 100nm.

The above list shows the applied layout rules for the lateral MOS transistor. For the vertical transistor there are currently no production layout rules available. Several design rules (L9-L13) were therefore assumed, and were chosen to be consistent with the layout rules for the lateral transistor. For example the overlap of the polysilicon gate over the pillar (L9) was chosen to be the same as the overlap of the gate over the STI (L8).

Figure 3.1 and 3.2 illustrate the schematic layout of two lateral device with 220nm and 1.32μm gate width using the design rules given. It can be seen that the device size is determined by the polysilicon gate width. Metal contacts are assumed on each side of the polysilicon gate to connect the source and drain. Furthermore, metal contacts contact the p^+ substrate, isolated by the STI. The width of the device is scalable down to a minimum gate width of W=220nm (L7) as shown in figure 3.1.

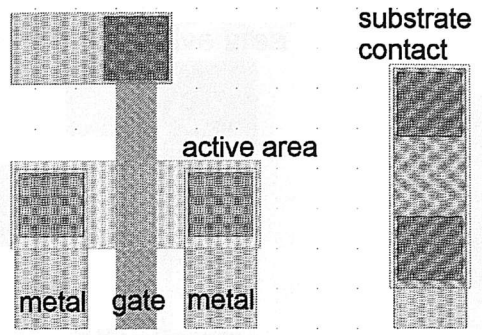


Figure 3.1: Schematic lateral MOSFET layout (W=220nm) - grid size: 100nm

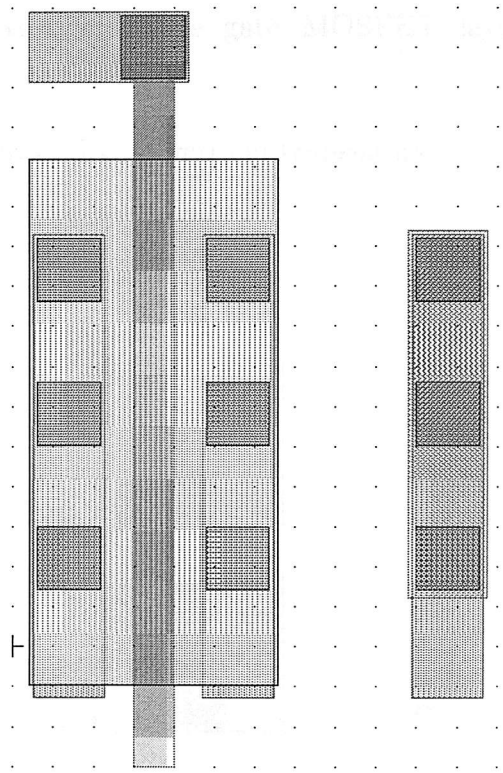


Figure 3.2: Schematic lateral MOSFET layout (W=1.32μm) - grid size: 100nm

Figure 3.3 illustrates a schematic layout of a minimum geometry single gate vertical device. A minimum gate width of 220nm has been used. The source contact is on top of the pillar, whilst the drain contact is adjacent to the pillar at the bottom of the layout.

A layout for the vertical surround gate device is presented in figure 3.4. The gate width is determined by the perimeter of the pillar which is 1.32μm. This layout can therefore be directly compared with that of the lateral transistor in figure 3.2. It can be seen that the vertical transistor occupies less area than the lateral transistor. For example, the active area of the surround gate vertical transistor is $0.46\mu m^2$ compared with $0.82\mu m^2$ for the lateral transistor with the same gate width. This is an

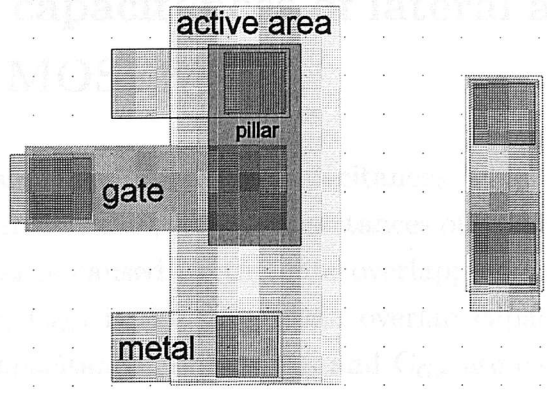


Figure 3.3: Schematic vertical single gate MOSFET layout (W=220nm) - grid size: 100nm

important benefit of surround gate vertical transistors.

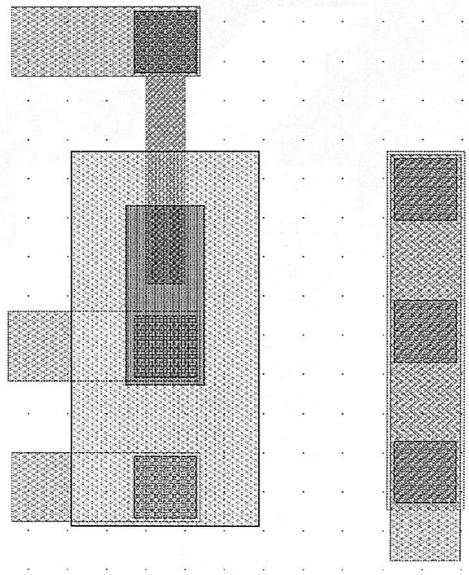


Figure 3.4: Schematic vertical surround gate MOSFET layout (W=1.32μm) - grid size: 100nm

3.3 Overlap capacitances of lateral and single gate vertical MOSFETs

The gate causes several unwanted overlap capacitances, which limit the device performance. Figure 3.5 illustrates the overlap capacitances of a lateral device, where C_{GSub} is the overlap capacitance caused by the gate overlapping the shallow trench isolation (STI) field oxide, C_{GD} is the gate/drain overlap capacitance and C_{GS} is the gate/source overlap capacitance. Both, C_{GD} and C_{GS} are caused by the lateral diffusion of the source/drain implant underneath the gate by the amount of x_j. The lateral diffusion underneath the gate decreases the gate length L to the effective gate length L_{eff}.

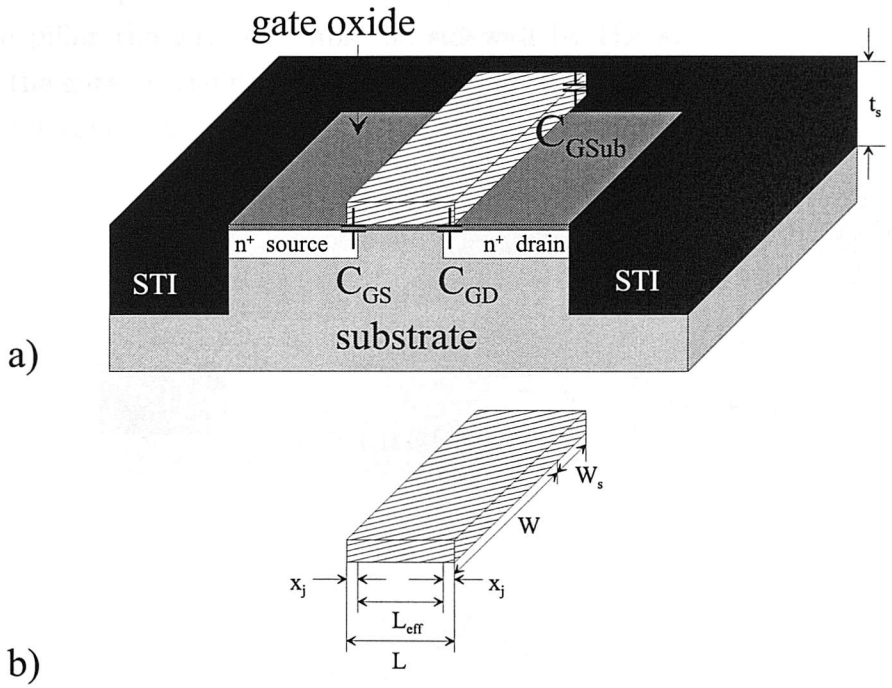


Figure 3.5: Parasitic capacitances of a lateral MOSFET a) cross-section showing overlap capacitances b) gate dimensions

To a first order approximation the parasitic capacitances of the lateral MOS transistor can be calculated as shown in table 3.1. In order to simplify the calculations, all introduced capacitances are modelled as parallel plate capacitors with no stray capacitance.

The gate/substrate capacitance C_{GSub} is caused by the gate overlapping the STI by the amount of W_s, where t_s is the STI thickness. The overlapping area of C_{GD} and C_{GS} is caused by lateral diffusion. The diffusion length under the gate is equal to the junction depth x_j. W is the active gate width.

capacitance	type	equation
C_{GSub}	gate/substrate	$\frac{\epsilon_0 \epsilon_{SiO_2} W_s\, L}{t_s}$
C_{GD}	gate/drain	$\frac{\epsilon_0 \epsilon_{SiO_2} W\, x_j}{t_{ox}}$
C_{GS}	gate/source	$\frac{\epsilon_0 \epsilon_{SiO_2} W\, x_j}{t_{ox}}$

Table 3.1: Parasitic overlap capacitances of a lateral device

Figure 3.6 illustrates the cross-section of an idealised single gate vertical MOS transistor based on a pillar structure. The channel width W is defined by the width of the polysilicon gate. The gate overlaps the bottom of the trench and causes the parasitic gate/drain overlap capacitance C_{GD}. The drain has diffused to the edge of the pillar, so there is no component of gate/drain capacitance on the side of the pillar. On the side of the pillar the gate overlaps the sidewall by the amount of $L_{eff} + x_j$. Furthermore, the gate overlaps the top of the pillar and causes the parasitic gate/source overlap capacitance C_{GS}.

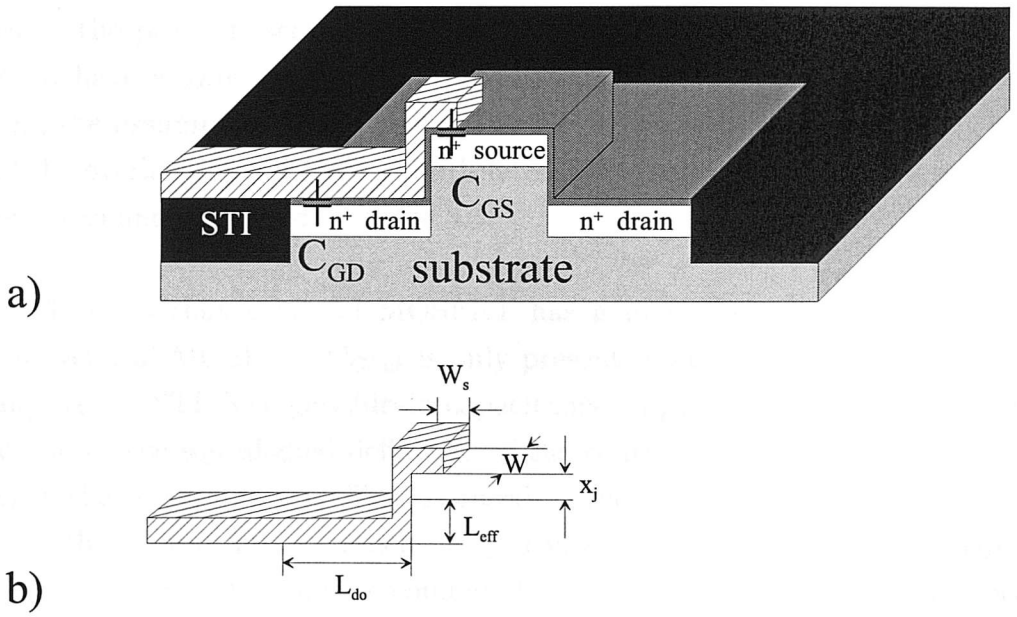


Figure 3.6: Parasitic capacitances of a basic single gate vertical MOSFET a) cross-section showing overlap capacitances b) gate dimensions

The approximate equations for the parasitic capacitances of the vertical MOSFET illustrated in figure 3.6 are listed in table 3.2, where, L_{do} is the amount by which the gate overlaps the drain at the bottom of the pillar and W_s is the amount by which the gate overlaps the source on top of the pillar (L9).

At the bottom of the trench the gate overlaps the drain over its full length L_{do}, and the capacitance is inversely proportional to the gate oxide thickness t_{ox}. The

capacitance	type	equation
C_{GD}	gate/drain	$\frac{\epsilon_0 \epsilon_{SiO_2} W L_{do}}{t_{ox}}$
C_{GS}	gate/source	$\frac{\epsilon_0 \epsilon_{SiO_2} W (x_j + W_s)}{t_{ox}}$

Table 3.2: Parasitic overlap capacitances of a basic vertical device

gate/source overlap capacitance C_{GS} consists of two capacitances. The gate overlaps the side of the pillar by the amount of the junction depth x_j, and the top of the pillar by the amount of W_s. Both overlap capacitances depend on the gate oxide thickness t_{ox}.

3.3.1 Calculation of overlap capacitances for lateral- and basic single gate vertical devices

In this section typical capacitances for lateral and single gate vertical devices described in the previous section are calculated and compared. The transistor is assumed to have a gate oxide layer covering the drain, source and pillar side. By applying the assumptions made in section 3.2 to the equations of table 3.1 and table 3.2 the overlap capacitances of both lateral and basic single gate vertical devices can be determined as shown in table 3.3.

Table 3.3 shows that a lateral MOSFET has a much lower parasitic capacitance than the vertical MOSFET. C_{GSub} is only present in lateral devices due to the gate overlapping the STI. The gate/drain capacitance C_{GD}, which is small on the lateral device due to the self aligned definition of the source- and drain regions, is 5 times greater in the vertical device. This is caused by the overlap of the gate over the drain region at the bottom of the trench. C_{GS}, caused by the gate/source overlap, is 11 times larger in the vertical device compared to its lateral counterpart mainly because of the overlap of the gate over the top of the pillar. Novel methods have therefore to be found to reduce these parasitic overlap capacitances.

capacitance	lateral	basic vertical	$C_{Vertical}/C_{Lateral}$
C_{GSub}[F]	2.3×10^{-18}	-	-
C_{GD}[F]	7.6×10^{-17}	3.8×10^{-16}	5
C_{GS}[F]	7.6×10^{-17}	8.4×10^{-16}	11

Table 3.3: Calculated overlap capacitances for a lateral and a basic single gate vertical device (W=220nm)

3.3.2 Optimisation of pillar fabrication

Two alternative methods can be considered for fabricating the pillar. The first uses a trench etch after LOCOS or shallow trench isolation, as illustrated in figure 3.7a-c. After the standard LOCOS process (figure 3.7b), the pillar is defined using photo lithography and an anisotropic silicon etch. The final structure illustrated in figure 3.7c shows the pillar isolated in the trench. The disadvantage of this approach is that the exposed vertical surface adjacent to the LOCOS of depth $L_{eff} + x_j$, gives additional gate/substrate overlap capacitance.

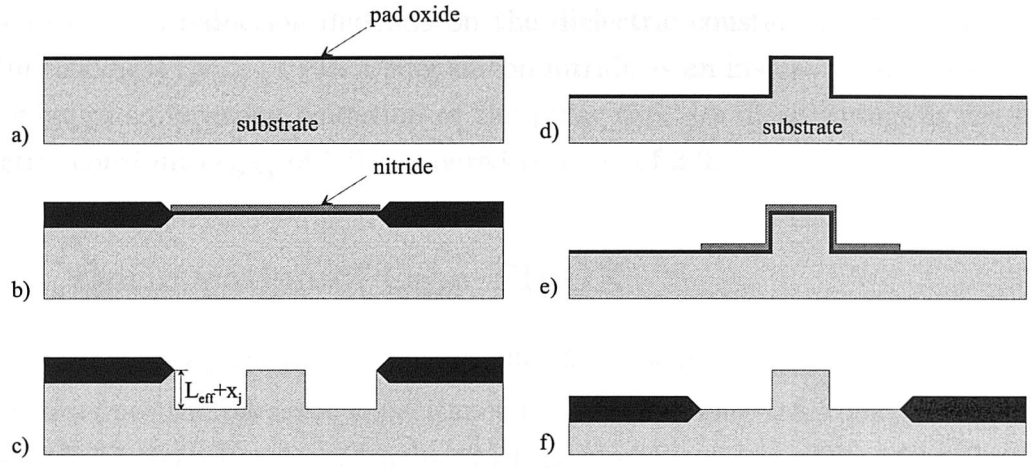


Figure 3.7: Process sequences of two ways to define the pillar structure of a vertical MOSFET

The second approach uses a pillar etch prior to isolation fabrication. Figures 3.7d-f shows this approach for LOCOS isolation. The first process step is etching the pillar structure into the silicon wafer and growing a pad oxide as shown in figure 3.7d. Now a silicon nitride layer is deposited and the active area is defined (figure 3.7e). The next process step is to perform the LOCOS. After removal of the nitride and pad oxide the pillar structure shown in figure 3.7f is obtained. The gate overlap length is shorter by the amount of the trench height $L_{eff} + x_j$ as illustrated in figure 3.7c. Applying this process sequence therefore eliminates the gate/sidewall substrate capacitance C_{GSub} that is present for the process sequence shown in figure 3.7a-c.

3.3.3 Optimisation of C_{GS}: pillar top insulator

In figure 3.6 the gate oxide on top of the pillar separates the gate from the source, which gives a large value of gate/source overlap capacitance. The gate/source overlap capacitance C_{GS} can be greatly reduced by covering the pillar top with an insulator prior to the pillar etch as shown in figure 3.8.

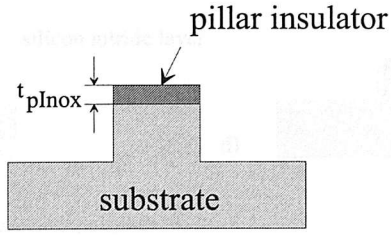


Figure 3.8: Inclusion of an insulator on top of the pillar to reduce gate/source overlap capacitance

The capacitance reduction depends on the dielectric constant of the insulator and its film thickness t_{pInox} (T10). Using silicon nitride as an insulator has the additional advantage of suppressing oxidation of the pillar top. Its disadvantage is the higher dielectric constant $\epsilon_{Si_3N_4}$ of 7.0 compared to ϵ_{SiO_2} of 3.9.

3.3.4 Optimisation of C_{GD}: FILOX

In this section, a novel process namely fillet local oxidation (FILOX), will be introduced to reduce the parasitic capacitance between the gate track and the drain [72]. Figure 3.9 illustrates two approaches with and without deposition of an insulation layer prior the pillar etch.

For the first approach, after the anisotropic pillar etch, a pad oxide is grown and a silicon nitride layer is deposited (figure 3.9a). Etching the silicon nitride layer with an anisotropic etch leaves nitride fillets on all sidewalls as shown in figure 3.9b. The FILOX process is then completed by growing a layer of SiO_2. The thickness of the grown oxide determines the parasitic gate/drain capacitance. Figure 3.9c illustrates the pillar structure after the FILOX process, with the nitride spacers on the sidewalls of the pillar still in place. An oxide layer of thickness t_{vLox} (T9) is grown on all lateral (unprotected) exposed areas. Since the FILOX oxide is also on top of the pillar, this process has the additional advantage of reducing the gate/source overlap C_{GS} at the same time.

Figures 3.9d-f show a different approach. The insulator illustrated in figure 3.9d is deposited prior to the pillar etch as discussed in section 3.3.3. After the pillar etch a thin pad oxide is grown and nitride is deposited over the pillar structure. Again, after the anisotropic nitride etch, nitride fillets are left on all sidewalls (figure 3.9e). An oxidation is then performed to grow an oxide on the bottom of the pillar whilst the top of the pillar is protected. After the oxide growth, the nitride fillets are etched off. The insulator layer on top of the pillar still covers the pillar top and the FILOX

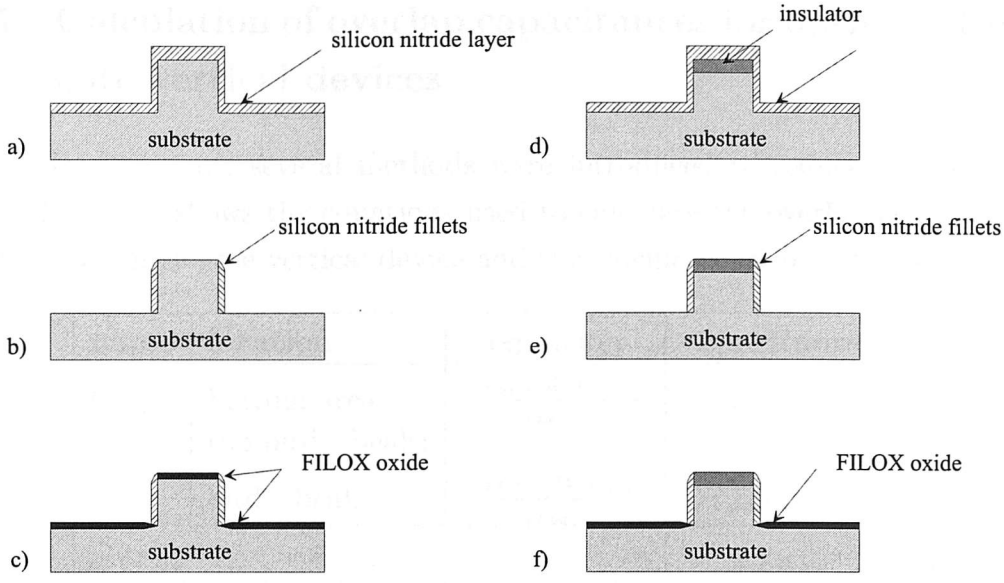


Figure 3.9: FILOX process flow

oxide is present at the bottom of the pillar.

The FILOX process causes bird's beaks at the top and bottom of the pillar as illustrated in figure 3.10. At the bottom of the pillar a bird's beak will be caused by the lifting of the nitride spacer during oxidation. In the calculations below, the length of the bird's beak is defined as L_{do2} (T11). Furthermore, a bird's beak in the vertical direction will be formed on the top of the pillar bending the nitride fillet during the FILOX oxidation. The thickness of the bird's beak is defined as t_{hLox} (T13) whilst its length is defined as L_{so} (T12). From the point of view of overlap capacitance these bird's beak's are advantageous. The bird's beak at the top of the pillar will reduce the gate/source overlap capacitance compared with the basic vertical device and that at the bottom will reduce gate/drain overlap capacitance.

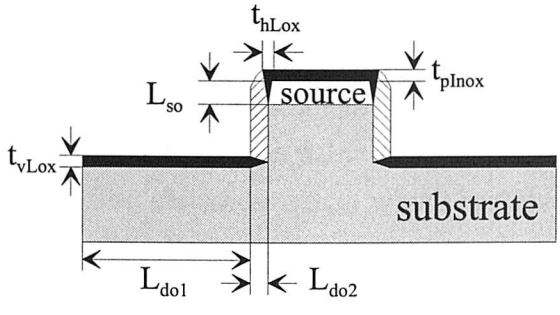


Figure 3.10: Bird's beak dimensions caused by FILOX process without pillar top insulator

3.3.5 Calculation of overlap capacitances for optimised single gate vertical devices

In the above sections, several methods were introduced to reduce overlap capacitances. Table 3.4 shows the equations used to calculate the overlap capacitances of an optimised single gate vertical device and the calculated values of capacitance.

name	location	equation	capacitance [F]
C_{GD}	bottom area (no bird's beak)	$\frac{\epsilon_0 \epsilon_{SiO_2} W\ L_{do1}}{t_{vLox}} +$	1.1×10^{-17}
	bird's beak	$\frac{\epsilon_0 \epsilon_{SiO_2} W\ L_{do2}}{t_{vLox}/2}$	1.5×10^{-17}
	=		2.7×10^{-17}
C_{GS}	side of pillar	$\frac{\epsilon_0 \epsilon_{SiO_2} W x_j}{t_{hLox}/2} +$	7.6×10^{-18}
	top of pillar	$\frac{\epsilon_0 \epsilon_{SiO_2} W\ W_s}{t_{pInox}}$	3.8×10^{-17}
	=		4.6×10^{-17}

Table 3.4: Parasitic overlap capacitances of an optimised single gate vertical device

The gate/drain overlap capacitance C_{GD} of vertical devices is partitioned into two terms. The first term describes the area covered by the gate track without the bird's beak, the second the area covered by the bird's beak. This latter term assumes that the bird's beak extends all the way to the edge of the pillar, as shown in figure 3.10. This assumption is the 'best case' for gate/drain overlap capacitance reduction.

The gate/source capacitance C_{GS} also consists of two terms. The first term expresses the capacitance caused by the gate track overlapping the source on the pillar sidewall and depends on the bird's beak on top of the pillar. This bird's beak extends to the full depth of the source junction, so $L_{so} = x_j$. This assumption is the 'best case' for gate/source overlap capacitance reduction. The second term describes the overlap capacitance on the pillar top which heavily depends on the thickness t_{pInox} of the insulation layer. C_{GS} can be reduced by decreasing the junction depth x_j or by increasing the insulating film thickness t_{pInox} which certainly decreases the source overlap capacitance at the sidewall.

Table 3.5 summarises the total overlap capacitances of a lateral and an optimised single gate vertical transistor.

For vertical devices the gate/substrate capacitance C_{GSub} is non-existent, which is

capacitance	lateral	single gate vertical	$C_{Vertical}/C_{Lateral}$
C_{GSub}[F]	2.3×10^{-18}	-	-
C_{GD}[F]	7.6×10^{-17}	2.7×10^{-17}	0.4
C_{GS}[F]	7.6×10^{-17}	4.6×10^{-17}	0.6

Table 3.5: Calculated overlap capacitances for a lateral and an optimised single gate vertical device (W=220nm)

considerably better than that of the lateral device. The gate/drain overlap capacitance of the vertical transistor is significantly lower than that of the lateral device. This result can be explained because the FILOX oxide t_{vLox} can in theory be made as thick as needed to eliminate the bottom area capacitance. If this is done, the bird's beak then determines the value of the gate/drain overlap capacitance as shown in table 3.4. This component of overlap capacitance should always be smaller than that in the lateral transistor, where no bird's beak is present.

The gate/source capacitance in the vertical device is also much smaller than that found in the lateral device. Care should be taken to ensure that the vertical bird's beak caused by the FILOX process does not extend into the active vertical channel as it would thicken the gate oxide, and degrade the the transistor performance. This practical point is addressed in chapter 4.

3.4 Overlap capacitances of optimised surround gate vertical MOSFETs

In this section a surround gate structure is described and it will be shown that this device has even lower gate/source and gate/drain overlap capacitances per unit gate width than the single gate vertical MOSFET. This is done by introducing a polysilicon fillet that surrounds the pillar on four sides. This is achieved with only a slight increase in device area of a factor of 1.07. The gate width per unit silicon area is therefore dramatically increased. Figure 3.11 depicts a cross-section of a surround gate device with polySi fillets.

It is assumed that the pillar is of rectangular shape as illustrated in figure 3.12 and the polysilicon fillet thickness is the same as the bird's beak length of the FILOX oxide L_{do2} as discussed in section 3.2. The width W of the gate interconnect can be reduced to the minimum gate length of a lateral device (L=100nm) as given by

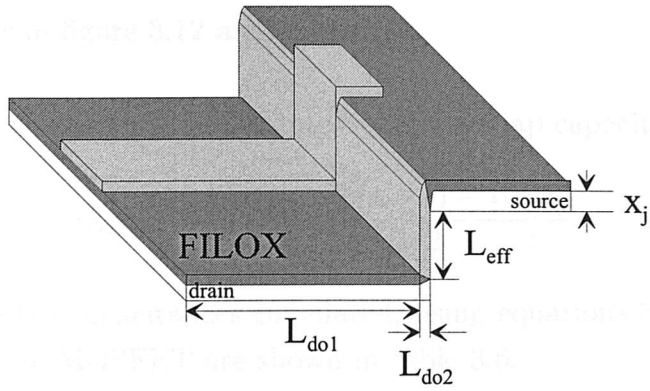


Figure 3.11: Cross-section showing polysilicon fillets covering channel- and source region

layout rule L13.

At the sidewalls of the pillar, adjacent to the source, a vertical bird's beak separates the gate fillet from the source junction, as seen previously in the single gate transistor in figure 3.10. A similar bird's beak is present at the bottom of the pillar adjacent to the drain. The surround gate width is according to figure 3.12 $W_{all} = 2(a + b) = 1.32\mu$m, where a is the length of the pillar and b its width.

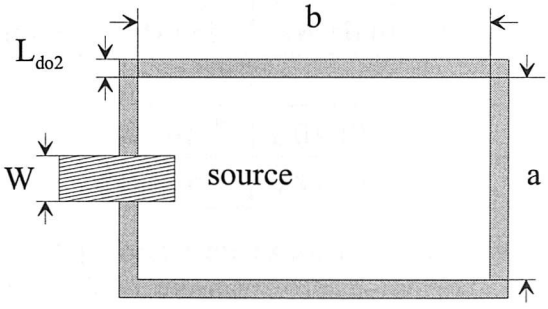


Figure 3.12: Top-view of a vertical MOSFET; in light grey: the area covered by the polysilicon fillets

For vertical surround gate devices the overall gate/drain capacitance becomes $C_{GDall} = C_{GD} + C_{GDfill}$, where C_{GDfill} is the additional drain overlap capacitance caused by the fillets overlapping the drain region at the bottom of the pillar. Similarly for the overall gate/source overlap capacitance one can say that $C_{GSall} = C_{GS} + C_{GSfill}$. To calculate the overall gate/drain capacitance, the following term has therefore to be added to C_{GD}

$$C_{GDfill} = \frac{\epsilon_0 \epsilon_{SiO_2} \left(2\left(a+b\right) - W\right) L_{do2}}{t_{vLox}/2} \tag{3.1}$$

This equation assumes that the perimeter of the pillar is much greater than the thickness of the fillet ($2(a+b) \gg L_{do}$). In other words, the overlap capacitances in the

corners of the pillar in figure 3.12 are ignored.

Making the same assumptions for the gate/source overlap capacitance, we have

$$C_{GSfill} = \frac{\epsilon_0 \epsilon_{SiO_2} \left(2\left(a+b\right) - W\right) x_j}{t_{hLox}/2} \tag{3.2}$$

The additional overlap capacitances calculated, using equations 3.1 and 3.2, for the vertical surround gate MOSFET are shown in table 3.6.

capacitance	**value**
C_{GDfill}[F]	8.4×10^{-17}
C_{GSfill}[F]	4.2×10^{-17}

Table 3.6: Calculated overlap capacitances caused by fillets (W=1.32μm)

Table 3.7 compares the parasitic capacitances of a lateral device with a gate width of 1.32μm and an optimised vertical surround gate device with the same gate width.

capacitance	**lateral**	**vertical**	$C_{Vertical}/C_{Lateral}$
C_{GSub}[F]	2.3×10^{-18}	-	-
C_{GDall}[F]	4.6×10^{-16}	1.0×10^{-16}	0.2
C_{GSall}[F]	4.6×10^{-16}	6.3×10^{-17}	0.1

Table 3.7: Calculated overlap capacitances for a lateral device and an optimised surround gate vertical device (W=1.32μm)

For the lateral device the increase in channel width by a factor of 6 compared with the results in table 3.3 causes the gate/source and gate/drain overlap capacitance to rise by the same amount.

The gate/source and gate/drain capacitances of the vertical device are much lower compared to the lateral control. This results from the vertical bird's beaks caused by the FILOX oxidation at the side and bottom of the pillar. For surround gate devices with high channel width $W_{all} \gg W$ the capacitance of the fillets dominates the gate/source and gate/drain overlap capacitance (see table 3.6). The key result in table 3.7 is that the overlap capacitances of the surround gate vertical MOSFET are dramatically lower than those of the lateral MOSFET. Furthermore, a thicker

FILOX film would certainly reduce the parasitic capacitance even further.

Comparing tables 3.5 and 3.7, the following conclusion can be drawn. The overlap capacitance per unit gate width of the surround gate transistor is lower than that of the single gate transistor because the gate fillet adds proportionally little extra gate/drain overlap capacitance. This occurs partly because of the self-aligned structure of the surround gate and partly because the overlap capacitance is determined by the FILOX oxide.

3.4.1 Overetching the surround gate

Although the gate/source overlap capacitance is nearly half of that found in a lateral device, a further reduction of the gate/source overlap capacitance could be achieved by overetching the polysilicon fillets as illustrated in figure 3.13. Here, the fillets do not cover the source area on the pillar sidewalls and therefore no further overlap capacitances caused by the fillets need be added to the overall gate capacitance C_{GSall}, since $C_{GSfill} = 0$.

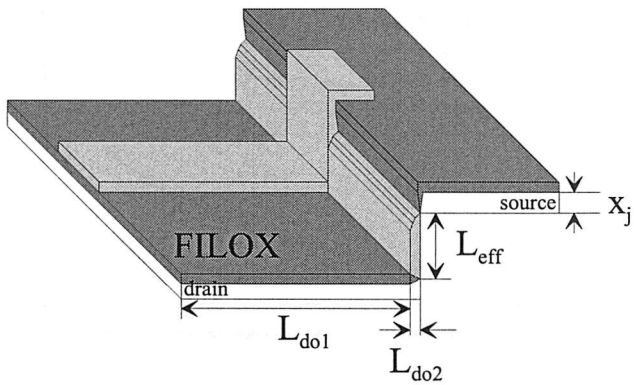


Figure 3.13: Cross-section showing overetched polysilicon fillets (W=1.32μm)

Table 3.8 displays the results for vertical devices with overetched polysilicon fillets. Whilst the gate/drain overlap capacitance has not changed (see table 3.7), the gate/source overlap capacitance is even lower.

Process control would be a major problem in the structure shown in figure 3.13. However, with partial over etch of the fillets it should be possible to obtain a reduction of the gate/source overlap capacitance with good process control. In this case, the value of the gate/source overlap capacitance would be part way in between those in table 3.7 and those in table 3.8.

Figure 3.14 shows the overlap capacitances as a function of gate oxide thickness

capacitance	lateral	vertical	$C_{Vertical}/C_{Lateral}$
C_{GSub}[F]	2.3×10^{-18}	-	-
C_{GDall}[F]	4.6×10^{-16}	1.0×10^{-16}	0.2
C_{GSall}[F]	4.6×10^{-16}	2.0×10^{-17}	0.05

Table 3.8: Calculated overlap capacitances for a lateral device and an optimised surround gate vertical device with overetched fillets (W=1.32μm)

for lateral devices and optimised vertical surround gate devices. Both, gate/drain and gate/source overlap capacitances of the vertical devices are independent of the gate oxide thickness since they are determined by the oxide thickness and the FILOX bird's beak. This is not the case for the lateral device where the overlap capacitances increase with decreasing gate oxide thickness. For gate oxide thicknesses less than ~9nm both types of vertical surround gate devices have lower overlap capacitances than lateral devices.

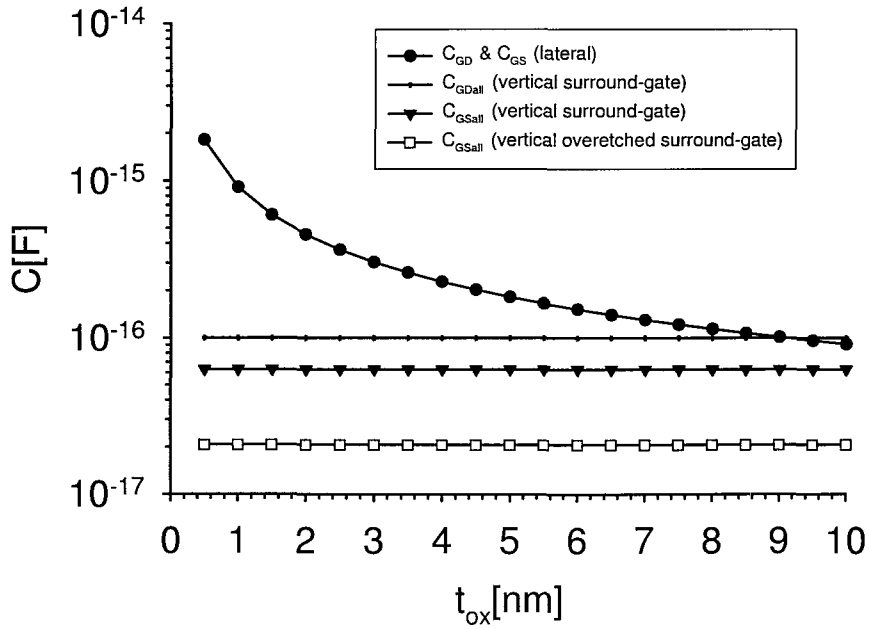


Figure 3.14: Gate/source and gate/drain overlap capacitances for a lateral and an optimised vertical surround gate devices as a function of gate oxide thickness t_{ox} (W=1.32μm)

3.4.2 Alternative gate process sequence

A further reduction in both, gate/source and gate/drain overlap capacitance can be obtained by fabricating the gate before the source/drain implant (GBI) rather than

after the source/drain implant (GAI). In the GBI process the source/drain implant only penetrates underneath the polysilicon gate track at the edge of the gate as illustrated in figure 3.15. This gives rise to a decrease in gate/drain overlap capacitance compared with the GAI process. Since the gate overlaps the substrate on the bottom of the pillar, a new component C_{GSub} is introduced. In the GAI process, the gate overlaps the drain area over the full width W of the gate.

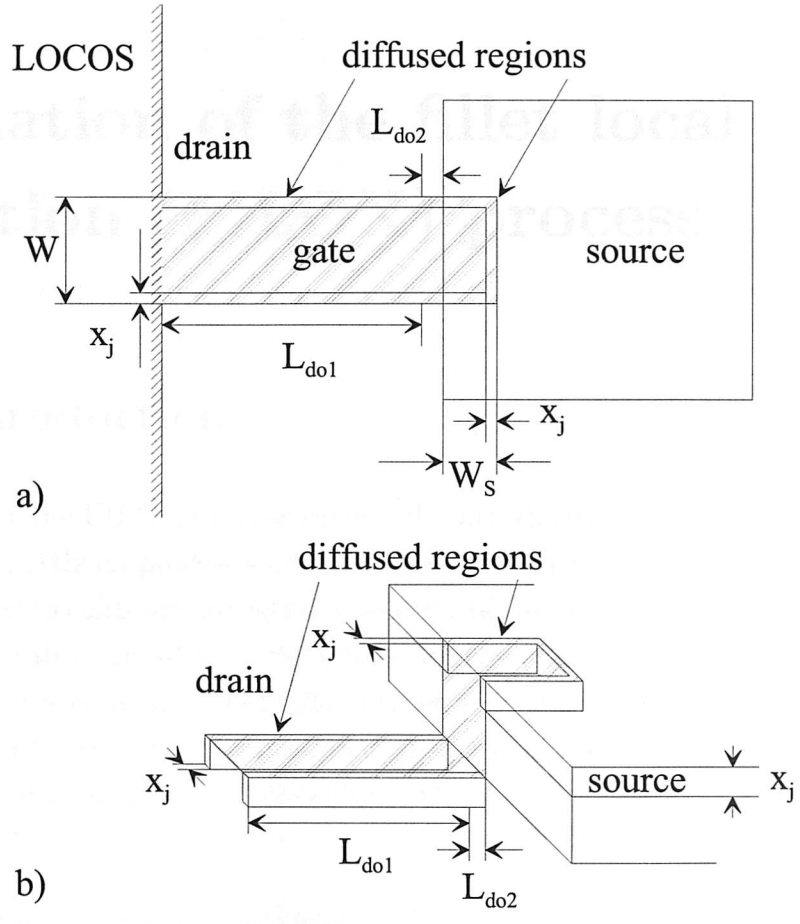


Figure 3.15: GBI MOSFET a) top-view showing the underneath the gate diffused source- and drain regions b) cross-section

It should be noted that the GBI process can only be used for transistors containing fillets because in this approach only the fillet act as the gate of the transistor. The polysilicon track merely provides a contact to the fillet. However, GBI devices are, in comparison with GAI devices highly CMOS compatible since the gate track and the fillets are implanted at the same time as the source/drain junctions.

The channel width W_{all} for a GBI device with surround gate can be calculated as

$$W_{all} = 2(a+b) - W + 2x_j \tag{3.3}$$

where a is the length of the pillar, b the width of the pillar and W is the width of the polysilicon track which contacts the gate. For GBI devices the parasitic capacitances can be calculated as shown in table 3.9.

name	location	equation
C_{GSub}	bottom area (no bird's beak) bird's beak side of pillar (channel area) side of pillar (source area) top of pillar	$\frac{\epsilon_0\epsilon_{SiO_2}(W-2x_j)\,L_{do1}}{t_{vLox}}+$ $\frac{\epsilon_0\epsilon_{SiO_2}(W-2x_j)\,L_{do2}}{t_{vLox}/2}+$ $\frac{\epsilon_0\epsilon_{SiO_2}W\,L_{eff}}{t_{ox}}+$ $\frac{\epsilon_0\epsilon_{SiO_2}(W-2x_j)\,x_j}{t_{hLox}/2}+$ $\frac{\epsilon_0\epsilon_{SiO_2}(W-2x_j)(W_s-x_j)}{t_{pInox}}$
C_{GD}	bottom area (no bird's beak) bird's beak	$\frac{\epsilon_0\epsilon_{SiO_2}2x_jL_{do1}}{t_{vLox}}+$ $\frac{\epsilon_0\epsilon_{SiO_2}2x_jL_{do2}}{t_{vLox}/2}$
C_{GS}	side of pillar top of pillar	$\frac{\epsilon_0\epsilon_{SiO_2}2x_j^2}{t_{hLox}/2}+$ $\frac{\epsilon_0\epsilon_{SiO_2}x_j(2(W_s-x_j)+W)}{t_{pInox}}$

Table 3.9: Parasitic overlap capacitances of an optimised single gate vertical device based on the GBI process sequence

In general the gate/substrate capacitance consists of five terms. The gate track covers the bottom of the pillar where the gate track is separated from the substrate due to the FILOX oxide. At the side of the pillar, the gate track overlaps the sidewall by the amount of L_{eff}. Here, the gate track is isolated by the gate oxide. Because of the vertical bird's beak caused by the FILOX process at the top of the pillar, the overlap capacitance is reduced. On top of the pillar the insulating layer, again caused by the FILOX separates the gate from the substrate.

For the gate/drain capacitance only the, by the amount of $2x_j$, under the gate track diffused area needs to be considered. Again, the FILOX process reduces the overlap capacitance.

The gate/source overlap capacitance consist of two terms. Likewise for the gate/drain capacitance, for the gate/source overlap capacitance only the underneath the gate in lateral direction diffused area needs to be taken into consideration (see figure 3.15).

Table 3.10 compares values of overlap capacitance for surround gate GBI and GAI transistors. The GBI process gives slightly lower values of gate/source and gate/drain overlap capacitance, but at the cost of increased gate/substrate capacitance.

capacitance	lateral	GBI	GAI
C_{GSub}[F]	2.3×10^{-18}	1.6×10^{-16}	-
C_{GDall}[F]	4.6×10^{-16}	9.0×10^{-17}	1.0×10^{-16}
C_{GSall}[F]	4.6×10^{-16}	5.1×10^{-17}	6.3×10^{-17}

Table 3.10: Calculated overlap capacitances for a lateral device and optimised vertical surround gate GBI and GAI devices (W=1.32μm)

3.5 Junction capacitance in lateral and vertical MOSFETs

Junction capacitances occur between the source and drain diffusion regions and the substrate. Figure 3.16 illustrates the junction capacitances of a lateral device. The depletion regions of each junction consists of two components, the planar depletion region across the implanted length L_j and the peripheral depletion region under the gate. For this calculation the junctions are assumed to be rectangular in shape and abrupt. Figure 3.16 also shows that the source C_{jS} and drain C_{jD} capacitances are equal due to the symmetry of the device.

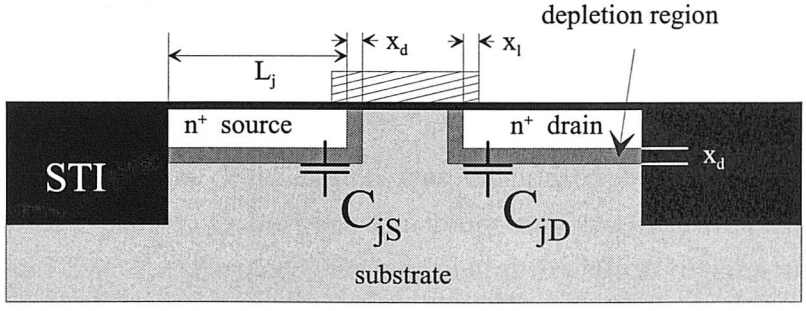


Figure 3.16: Lateral MOSFET with junction and depletion regions

From equation 2.7 for the depletion layer width, the junction capacitance per unit area is given by

$$\frac{C_j}{A} = \frac{\epsilon_{Si}\epsilon_0}{x_d} = \sqrt{\frac{\epsilon_{Si}\epsilon_0 q N_A}{2\left(\psi_{bi} + V_j\right)}} \tag{3.4}$$

where A is the area, V_j the reverse bias voltage across the junction and ψ_{bi} is the built-in voltage of the pn-junction given by

$$\psi_{bi} = V_{th}\, ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{3.5}$$

A high value of V_j causes a wide depletion region and therefore decreased junction capacitance. Equation 3.4 also shows that a low doped substrate can minimise the junction capacitance since x_d is high.
For a lateral MOSFET the junction capacitances at the source C_{jS} and drain C_{jD} are equal and can be calculated in the same way

$$C_j = \sqrt{\frac{\epsilon_{Si}\epsilon_0 q N_A}{2\left(\psi_{bi} + V_j\right)}}\left(L_j + x_j\right) W \tag{3.6}$$

Table 3.11 shows the equations used to calculate the junction capacitance for the vertical GAI device shown in figure 3.17.

capacitance	**type**	**equation**
C_{jD}	drain junction capacitance	$\sqrt{\frac{\epsilon_{Si}\epsilon_0 q N_A}{2(\psi_{bi}+V_D)}}\left(a_{AA}b_{AA} - ab + 2x_j\left(a+b\right)\right)$
C_{jS}	source junction capacitance	$\sqrt{\frac{\epsilon_{Si}\epsilon_0 q N_A}{2(\psi_{bi}+V_S)}}ab$

Table 3.11: Parasitic junction capacitances for a single gate device and a surround gate vertical device (GAI).

The depletion area of the drain region was calculated by considering the overall n^+ implanted area (a_{AA} b_{AA}) between the pillar and the active area as illustrated in figure 3.3 and 3.4. Furthermore, the peripheral depletion regions underneath the pillar need to be added. The depletion region at the source of the vertical MOSFET is determined by the area of the pillar (a b).

Table 3.12 illustrates the zero bias junction capacitance values for a lateral and a single gate vertical device width of W=220nm.

Vertical single gate devices show 5.1 times more drain junction capacitance compared to their lateral counterpart. This is mainly caused by the extended drain area surrounding the pillar as shown in figure 3.3. The source junction capacitance is similar for both device types.

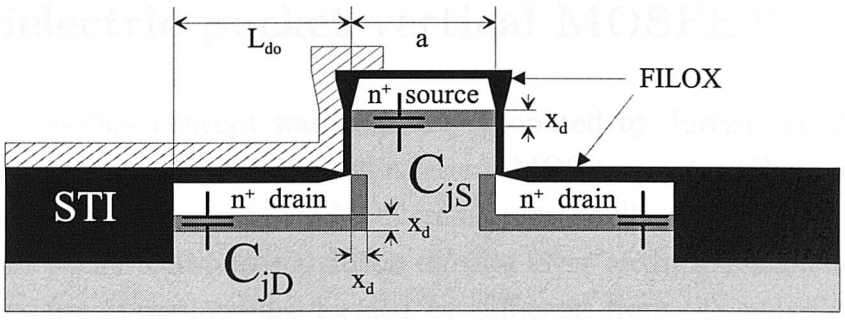


Figure 3.17: Optimised vertical single gate MOSFET with junction and depletion regions

capacitance	lateral	vertical	$C_{Vertical}/C_{Lateral}$
C_{jD}[F]	1.8×10^{-16}	9.3×10^{-16}	5.1
C_{jS}[F]	1.8×10^{-16}	3.4×10^{-16}	1.9

Table 3.12: Calculated zero bias junction capacitances for a lateral device and a vertical single gate device (GAI) with W=220nm

The junction capacitances C_{jSall} and C_{jDall} for a lateral and a vertical surround gate device with a 1.32μm gate width are shown in table 3.13.

capacitance	lateral	vertical	$C_{Vertical}/C_{Lateral}$
C_{jD}[F]	1.1×10^{-15}	1.1×10^{-15}	1.0
C_{jS}[F]	1.1×10^{-15}	2.5×10^{-16}	0.2

Table 3.13: Calculated zero bias junction capacitances for a lateral device and a vertical surround gate device (GAI) with W=1.32μm

At this large gate width the benefits of the vertical surround gate transistor are clearly apparent. The source junction capacitance of the surround gate vertical transistor is a factor of 5 lower than that of the lateral device. This is because the pillar defines the source area and this is much smaller than that of the lateral device, as can be seen by comparing figures 3.4 and 3.2. The drain junction capacitance of the surround gate vertical transistor and the lateral transistor are comparable as can be seen by comparing figures 3.4 and 3.2.

3.6 Dielectric pocket vertical MOSFET

The dielectric pocket concept was originally proposed by Jurczak et al. [73, 74] to suppress punch-through in the bulk of a lateral MOS transistor. However, this concept can also be applied to vertical MOS transistors, as illustrated in figure 3.18 [75]. The dielectric pocket comprises a silicon dioxide layer of thickness x_{tp} on top of the pillar. The source junctions are formed by diffusion from the polysilicon layer of thickness x_{poly} on top of the oxide. Very shallow junctions can be obtained in this way. A thin epitaxial layer is deposited over the pillar to ensure a good connection between the polysilicon layer and the substrate. This epitaxial layer can also act as a retrograde channel. Figure 3.18 shows that the dielectric pocket has dramatically reduced the active source area of the device.

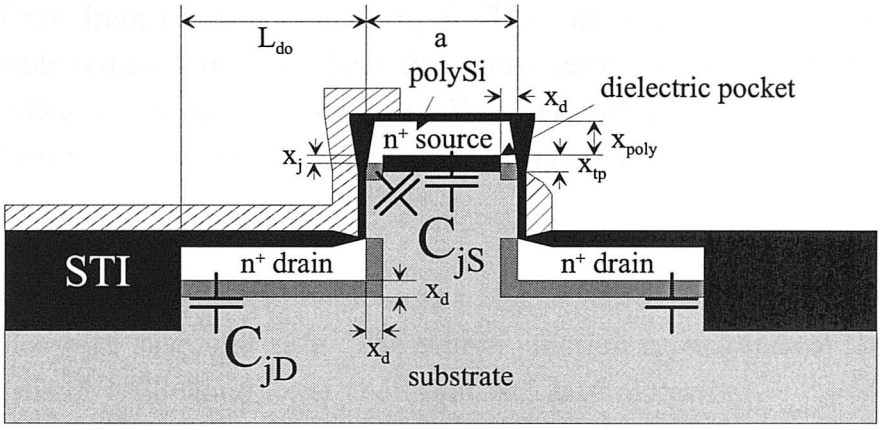


Figure 3.18: The dielectric pocket vertical MOSFET and the associated junction capacitances

3.6.1 Overlap capacitance of dielectric pocket vertical MOSFET

For a dielectric pocket thickness of $x_{tp} = 40nm$ and a polySi thickness of x_{poly}=40nm the gate/drain overlap capacitance C_{GDall} of the dielectric pocket device listed in table 3.14 is the same as that in table 3.8. Assuming that the FILOX bird's beak on top of the pillar covers the polySi and junction so that $L_{so} = x_{poly} + x_j$, the gate/source overlap capacitance is only slightly higher because of the longer source region on top of the pillar compared with that shown in table 3.8. It can therefore be concluded that the overlap capacitances of a dielectric pocket device are very similar to those of the optimised vertical transistor.

capacitance	lateral	vertical	$C_{Vertical}/C_{Lateral}$
C_{GSub}[F]	2.3×10^{-18}	-	-
C_{GDall}[F]	4.6×10^{-16}	1.0×10^{-16}	0.2
C_{GSall}[F]	4.6×10^{-16}	2.8×10^{-17}	0.06

Table 3.14: Calculated overlap capacitances for a lateral device and a dielectric pocket surround gate devices with overetched surround gate fillets (W=1.32μm)

3.6.2 Junction capacitance of dielectric pocket vertical MOSFET

The drain junction capacitance is not altered by the dielectric pocket, since the shape and size of the drain junction is unchanged. The junction capacitance at the source is considerably reduced, because the active source area is only located at the perimeter of the pillar as shown in figure 3.18. However, the dielectric pocket causes the source/substrate capacitance C_{SSub} which is in parallel with the source junction capacitance C_{jS}.

Table 3.15 lists the calculated junction capacitance values for an optimised dielectric pocket device with surround gate. The source junction capacitance of the dielectric pocket transistor is 33 times lower than that of a lateral device.

capacitance	lateral	vertical	$C_{Vertical}/C_{Lateral}$
C_{jD}[F]	1.1×10^{-15}	1.1×10^{-15}	1.0
C_{jS}[F]	1.1×10^{-15}	3.5×10^{-17}	0.03
C_{SSub}[F]	-	6.8×10^{-17}	-

Table 3.15: Calculated junction capacitances for a lateral device and an optimised vertical dielectric pocket surround gate device based on the GAI process sequence (W=1.32μm)

3.7 Summary

In this chapter calculations of parasitic overlap and junction capacitances have been made based on advanced 100nm industry design rules. Table 3.16 illustrates the gate/drain and gate/source overlap capacitances for different types of vertical MOS transistors and for comparison a standard lateral devices.

type	device	C_{GD}[F]	C_{GDVert}/C_{GDLat}	C_{GS}[F]	C_{GSVert}/C_{GSLat}
single gate	standard lateral	7.6×10^{-17}	-	7.6×10^{-17}	-
	basic vertical	3.8×10^{-16}	5.0	8.4×10^{-16}	11.0
	optimised vertical	2.7×10^{-17}	0.4	4.6×10^{-17}	0.6
surround gate	standard lateral	4.6×10^{-16}	-	4.6×10^{-16}	-
	optimised vertical	1.0×10^{-16}	0.2	6.3×10^{-17}	0.1
	optimised vertical overetched surround	1.0×10^{-16}	0.2	2.0×10^{-17}	0.05

Table 3.16: Summery of parasitic overlap capacitances for GAI based vertical devices

The basic single gate vertical MOS device shows high parasitic overlap capacitances compared with the standard lateral device. This device is therefore not suitable for high performance applications.

A fillet local oxidation (FILOX) process has been developed to reduce both, gate/drain and gate/source overlap capacitances. For the minimum geometry single gate vertical MOSFET in table 3.16, the gate/drain capacitance is lower by a factor of 2.9 and the gate/source overlap capacitance is lower by a factor of 1.7. From the point of view of overlap capacitances, this device would give higher switching performance than the standard lateral transistor. This conclusion is even more valid for surround gate transistors, where the reduction in overlap capacitance is even larger.

Table 3.17 lists the junction capacitances of lateral and different types of vertical devices. Here, minimal geometry single gate vertical devices show higher drain and source junction capacitance than the standard lateral transistor. However, the vertical surround gate device shows much lower source junction capacitance than the standard lateral devices with the same gate width, but a comparable drain junction capacitance.

A dielectric pocket concept has been introduced for vertical MOSFETs which gives a dramatic reduction of the source junction capacitance due to the confinement of the source junction to the pillar perimeter.

In conclusion surround gate vertical transistors incorporating FILOX and a dielectric pocket are ideally suited for high performance applications.

type	**device**	C_{jD}[F]	C_{jDVert}/C_{jDLat}	C_{jS}[F]	C_{jSVert}/C_{jSLat}
single gate	standard lateral	1.8×10^{-16}	-	1.8×10^{-16}	-
	vertical	1.0×10^{-15}	5.5	2.5×10^{-16}	1.4
surround gate	standard lateral	1.1×10^{-15}	-	1.1×10^{-15}	-
	vertical	1.1×10^{-15}	1.0	2.5×10^{-16}	0.2
	dielectric pocket	1.1×10^{-15}	1.0	3.5×10^{-17}	0.03

Table 3.17: Summery of parasitic junction capacitances for GAI based vertical devices

Chapter 4

Simulation of the fillet local oxidation (FILOX) process

4.1 Introduction

In this chapter the FILOX process previously introduced in section 3.3.4 is simulated using Silvaco's Athena process simulation tool. A test-batch has been fabricated and cross-sectioned to calibrate the nitride viscosity of the simulator. After calibration the new viscosity values are applied to investigate the encroachment on top and bottom of the pillar for various pad oxide thicknesses as well as different nitride thicknesses. Furthermore, FILOX with a nitride top insulator is introduced and simulated in order to reduce the encroachment on top of the pillar and its sidewalls.

4.2 Fabrication of the calibration structure

A test batch was fabricated to calibrate the simulator. Figure 4.1 illustrates the fabricated structure. Two areas shown in figure 4.1 are of particular interest namely the pillar top and the pillar bottom. The FILOX oxidation causes the nitride fillet to bend at the top of the pillar. Furthermore, the FILOX bends the nitride fillet at the bottom of the pillar as will be shown in the next section. Both encroachments are of particular importance for the successful implementation into the fabrication process of vertical MOSFETs as will be shown in chapter 6. The calibration structure was used to calibrate the viscosity of the silicon dioxide to ensure good agreement between measured and simulated encroachments at both the top and bottom of the pillar.

Table 4.1 lists the process steps to fabricate the structure shown in figure 4.1. The

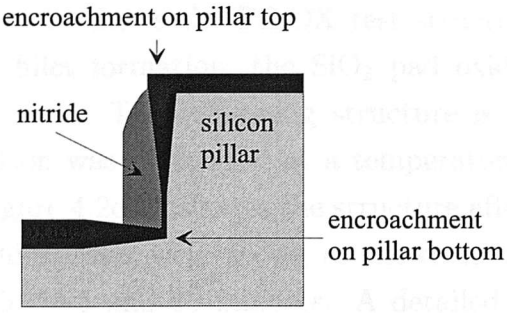


Figure 4.1: Nitride encroachment due to FILOX oxidation on pillar top and pillar bottom

initial wafer was p-type <100> with a resistivity in the range of 10 to 33Ωcm. The fabrication process started with an implant and anneal to give a substrate doping of $2\times10^{16}cm^{-3}$. The implant was at an energy of 50keV and a dose of $5.0\times10^{14}cm^{-2}$ and was followed by a drive-in at 1100°C to activate and anneal the dopants. In the following process step the thin oxide built during the previous anneal stage was removed. A 1.1μm lightfield photoresist layer (SPRT 510) was spun onto the wafer to protect future pillar areas. After hardbaking the wafer for two hours at 140°C the pillar was anisotropically etched using a HBr etch. The photoresist was removed using a plasma asher.

stage	description
1	boron substrate implant ($5.0\times10^{14}cm^{-2}$ at 50keV)
2	boron drive-in (1100°C 10' O_2, 30' N_2)
3	dip etch in HF to remove oxide
4	pillar lithography
5	anisotropic pillar etch (250nm)
6	resist strip
7	dry oxidation (5nm at 800°C)
8	deposit 40/70/130nm Si_3N_4 at 740°C
9	dry etch Si_3N_4 to leave fillets on sidewalls
10	dry etch SiO_2 to remove pad oxide layer
11	FILOX 40/80/120/160nm at 1000°C (O_2, HCL)

Table 4.1: Process list for FILOX test structures

After an RCA cleaning stage a 5nm pad oxide was grown using a dry oxidation O_2 ambient at 800°C. This oxide acts as a stress relief oxide for the following nitride deposition process. Three different nitride thicknesses were deposited as shown in table 4.1. The formation of the nitride fillets was performed using an anisotropic

CHF_3+Ar etch. Figure 4.2a shows the FILOX test structure after the anisotropic nitride etch. After the fillet formation, the SiO_2 pad oxide layer was anisotropic etch using a CHF_3+Ar etch. The remaining structure is depicted in figure 4.2b. The FILOX local oxidation was performed at a temperature of 1000°C in a hydrogen/oxygen ambient. Figure 4.2c illustrates the structure after the FILOX oxidation. Four different FILOX thicknesses were grown as shown in table 4.1 which required oxidation times of 1, 5.5, 11.5 and 16 minutes. A detailed process listing is in appendix C.1.

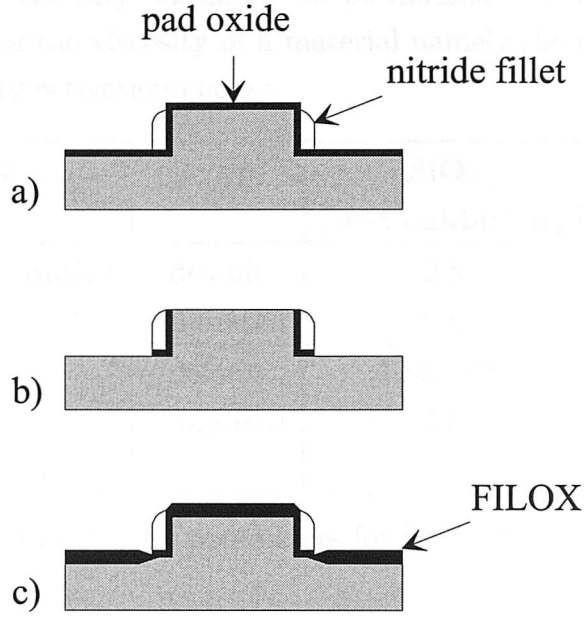


Figure 4.2: Process flow of the FILOX test structures a) after anisotropic nitride etch b) after anisotropic oxide etch c) after FILOX oxidation.

4.3 Simulation models

In this section the different models used for simulating the FILOX process are explained. For the silicon pillar etch as well as for the nitride fillet etch, the reactive ion etch model (rie) was used. The isotropy parameter of the etchant is defined as the contribution of thermal atoms, radicals and molecules coming out of the plasma and may lead to an underetching of the mask. For the silicon pillar etch the *isotropy* parameter of the etch as well as the *direction* of the ions was modified to achieve a steep pillar sidewall of 7°. The parameters *chemical* and *divergence* define the etch rate normal to the ion beam and the divergence of the beam respectively. The parameter values used are shown in the input file in appendix A.1.

Athena's dry oxidation model (dryo2) was used for pad oxidation at standard pres-

sure (1 atmosphere) and a temperature of 900°C. The parameter *hcl.pc* was modified to adjust the HCL content in the oxygen gas.

Athena's viscous flow model based on the work of Chin et al. [76] was used to grow the FILOX oxide. This model simulates elastic, stress-dependent and viscous oxide flow for temperatures above 960°C [77]. Above this temperature two mechanisms are involved in the oxidation process, namely flow of oxidant through the SiO_2 and oxide flow due to the volume expansion and associated stress [78, 79]. Athena allows the stress-dependent viscosity parameter to be modified. Table 4.2 shows the two parameters controlling the viscosity of a material namely the pre-exponential coefficient and the viscosity activation energy.

parameter	**type**	**SiO_2 (wet oxidation)**	**Si_3N_4**
viscosity activation energy (visc.E[eV])	default	2.8	0.99411
	calibrated	2.8	2.5625 [80]
pre-exponential coefficient (visc.0[$gcm^{-1}s^{-1}$])	default	1.55×10^{4}	3.75×10^{11}
	calibrated	2.8	2.3×10^{3}

Table 4.2: Default and calibrated parameters for stress dependent viscous oxidation simulations.

The viscosity η of a material can be calculated using the following equation [80]:

$$\eta = visc.0 \exp\left(\frac{visc.E}{kT}\right) \tag{4.1}$$

Table 4.2 summarises the default viscosity parameters, from which a default nitride viscosity of $3.8\times10^{16} gcm^{-1}s^{-1}$ can be calculated.

4.4 Calibration of the simulator

Figure 4.3 shows a TEM cross-section of the fabricated structure described in the previous section. The initial nitride thickness was 70nm. On top and bottom of the pillar a 40nm thick oxide layer was grown during the FILOX process. The nitride fillet was overetched during the anisotropic fillet etch which decreased the initial thickness of 70nm to 36nm in the middle of the fillet. The encroachment on top and bottom of the pillar were measured as shown in figure 4.3 and were found to be 27.2 and 7.0nm,

respectively.

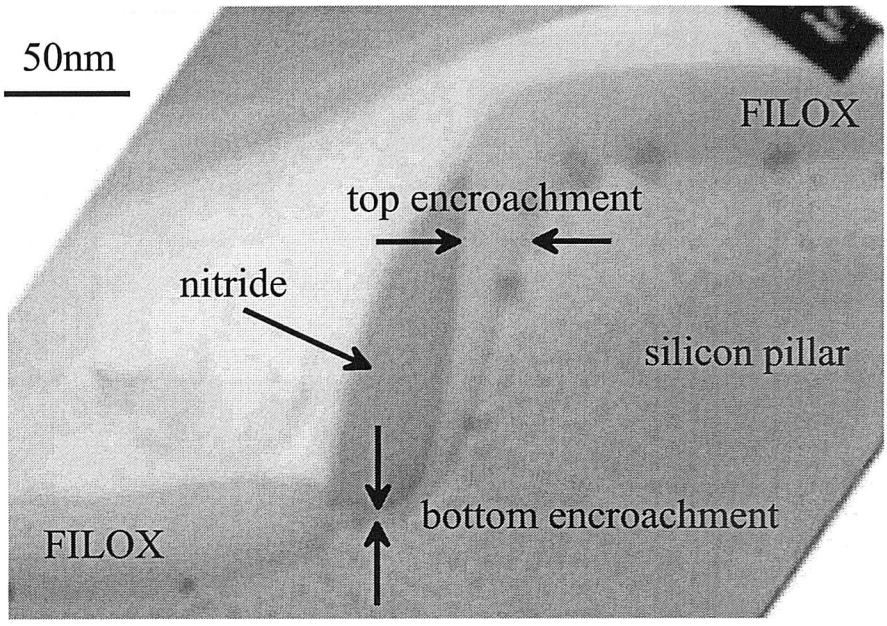


Figure 4.3: TEM cross-section of a FILOX test-structure directly after the oxidation at 1000°C for 1min. The initial pad oxide thickness was 5nm and the nitride thickness 70nm. The thickness of the FILOX oxide is 40nm.

Figure 4.4 shows a FILOX simulation using Athena's default parameter values for both, oxide and nitride viscosity. The FILOX oxide thickness at x=1.15μm is 38.8nm. The encroachment on top of the pillar at y=0.05μm is 12.2nm which is much less than the encroachment in the experimental test structure. The encroachment at the bottom of the default test structure at x=0.96μm is 7.8nm which is slightly higher than the encroachment of the experimental test structure.

Figure 4.5 plots the encroachment on the pillar top (at y=0.05μm) and bottom (at x=0.96μm) as a function of nitride viscosity. Simulating the given structure with a low nitride viscosity of $2\times10^{14} gcm^{-1}s^{-1}$ causes large encroachments at the pillar top and bottom. Increasing the nitride viscosity up to $1.6\times10^{16} gcm^{-1}s^{-1}$ leads to a high encroachment at the pillar top, but a lower encroachment at the pillar bottom. At this value good agreement between simulation and experimental data is achieved as can be seen from figure 4.3 and 4.6. A further increase of the nitride viscosity decreases the encroachment at the pillar top dramatically and gives poor agreement. Table 4.2 lists the calibrated viscosity parameter values which give a nitride viscosity of $1.64\times10^{16} gcm^{-1}s^{-1}$.

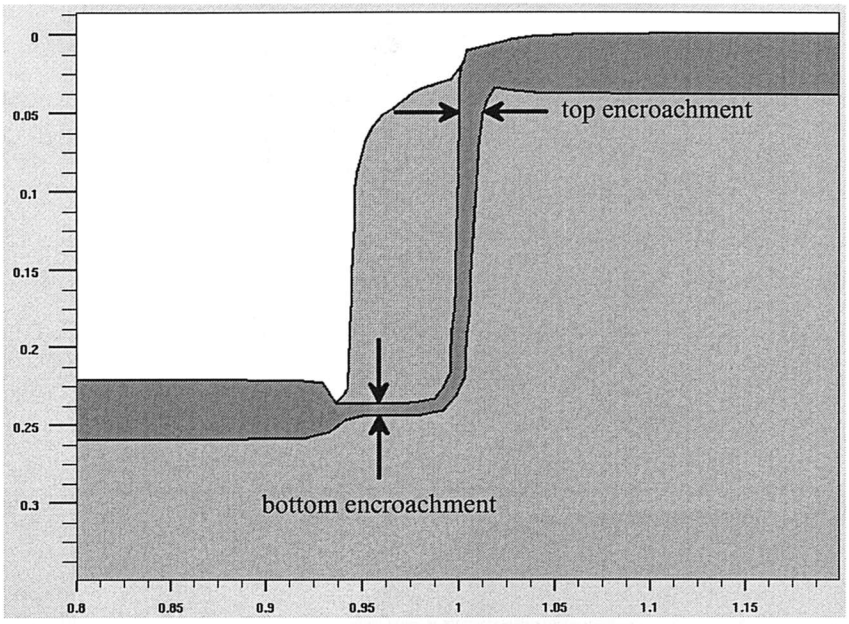


Figure 4.4: FILOX simulation using the default parameter set for oxide grown at 1000°C. The initial pad oxide thickness was 5.3nm and the nitride thickness 70nm. The thickness of the FILOX oxide is 38.8nm at x=1.15μm. Arrows showing the encroachment on top and bottom of the pillar which were considered for calibration.

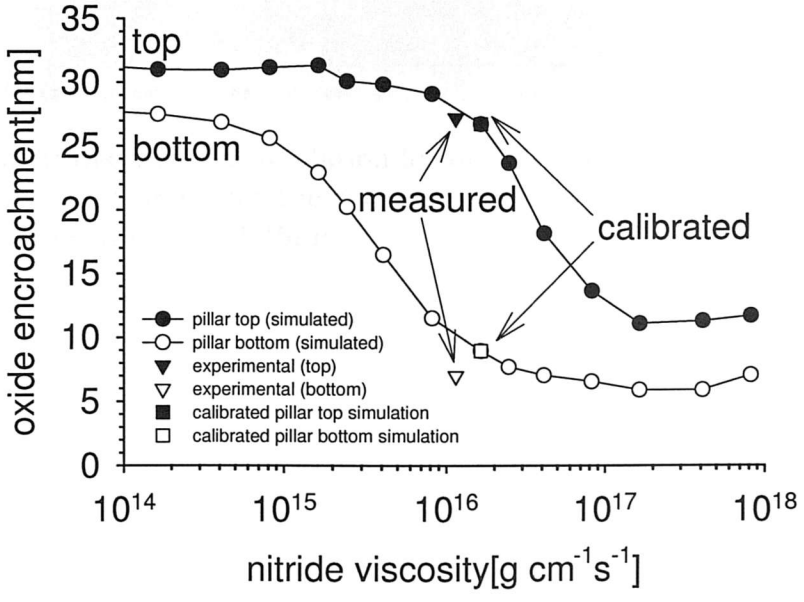


Figure 4.5: Encroachment on the pillar top and pillar bottom as a function of nitride viscosity for 38.8nm oxide thickness grown at 1000°C. The initial pad oxide thickness was 5.3nm and the nitride thickness 70nm.

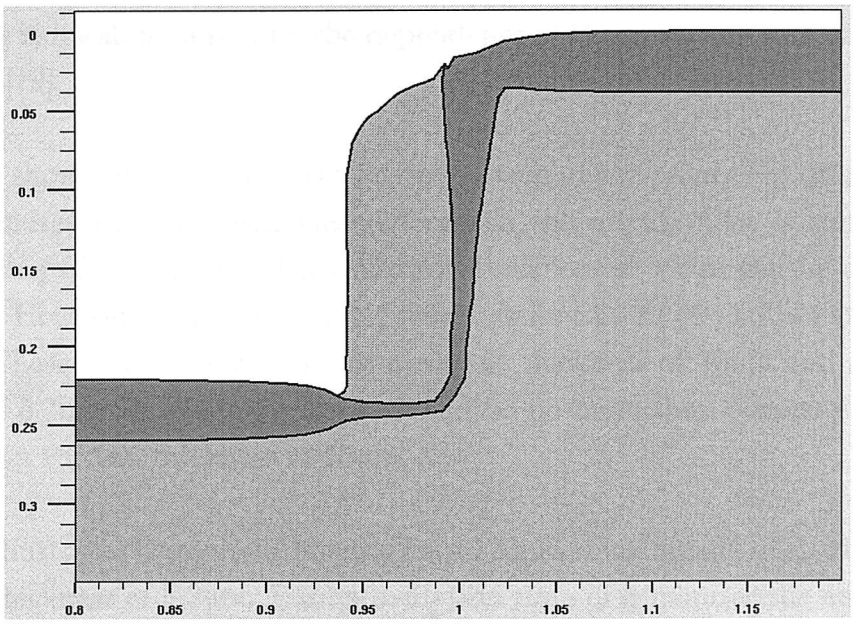


Figure 4.6: Calibrated FILOX simulation for oxide grown at 1000°C. The initial pad oxide thickness was 5.3nm and the nitride thickness 70nm. The thickness of the FILOX oxide is 39.1nm at x=1.15μm.

4.5 FILOX simulation results

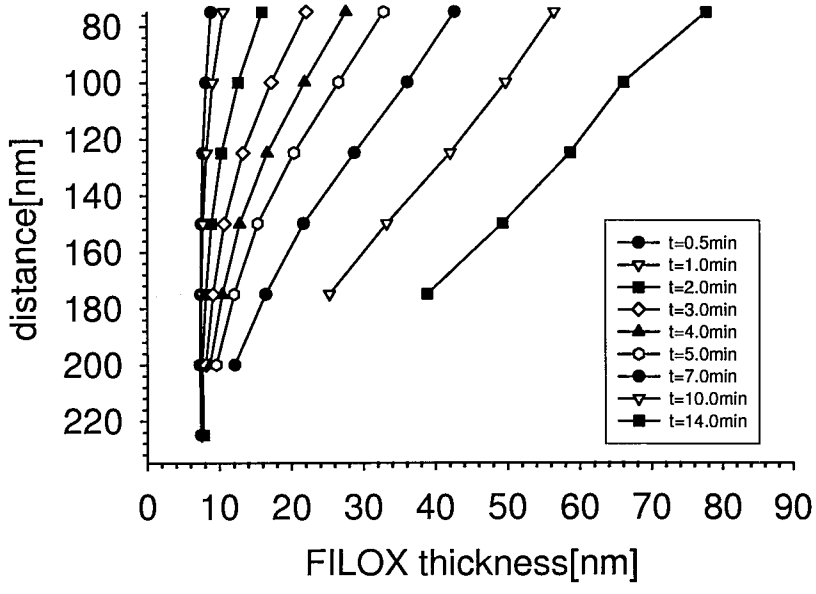
In this section the influence of the nitride thickness and the initial pad oxide thickness on the encroachments on top and bottom of the pillar are investigated for different FILOX oxidation times. Figure 4.7a illustrates the encroachment down the side of the pillar for a structure with initially 5.3nm pad oxide and a nitride fillet thickness of 70nm. For oxidation times up to 5 minutes the encroachment at y=80nm at the pillar top is below 33nm. For this case the fillet is bending at the top, but has not moved significantly from its original position at the bottom. Increasing the oxidation time causes the fillet to both, bend at the top and move from its original position at the bottom of the pillar. The initial pad oxide thickness was 5.3nm on the horizontal surfaces but figure 4.7a shows that it is 7.3nm at the pillar sidewall. The thicker oxide on the sidewall is caused by the dependence of the oxidation rate on the crystal orientation [79].

Figure 4.7b shows the encroachment at the bottom of the pillar. For oxidation times up to 5 minutes the encroachment underneath the nitride fillet is small. For an oxidation time of 5 minutes a FILOX oxide thickness of 12nm can be extracted at x=960nm. However, longer oxidation times cause the fillet to dramatically bend upwards. These results show that for a nitride thickness of 70nm and a pad oxide thickness of 5.3nm the oxidation time should be no more than 5 minutes. This corresponds to a FILOX thickness of 58nm.

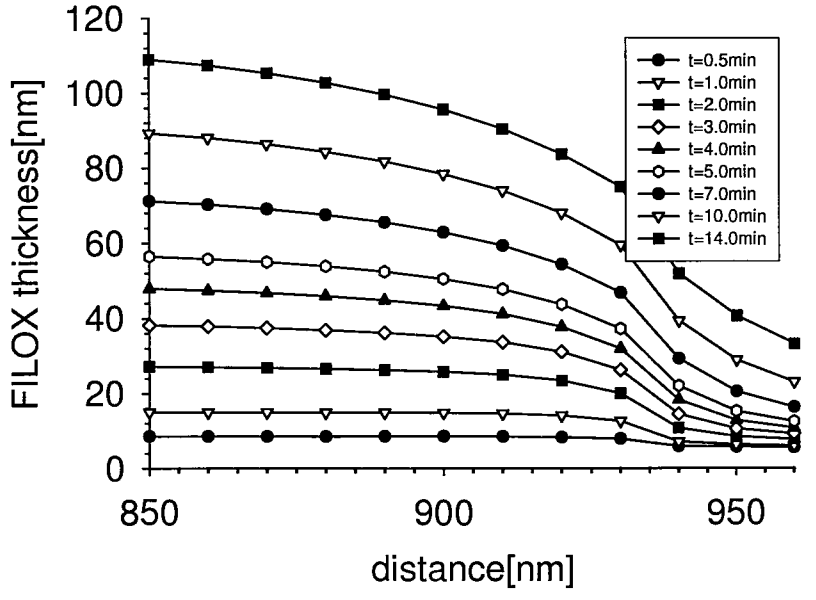
Figure 4.8 illustrates the encroachments for a 130nm thick nitride fillet with an initial pad oxide thickness of 5.3nm. For an oxidation time of 5 minutes the encroachment at the top of the pillar can be extracted to be 35nm which is very similar to the encroachment shown in figure 4.7a. However, the encroachment at the pillar bottom is slightly reduced. An oxide thickness of 7nm can be found at x=960nm compared with 12nm for the structure with a 70nm nitride spacer.

Figure 4.9a depicts the encroachment on top of the pillar for a 130nm thick nitride fillet with an initial pad oxide thickness of 20.4nm. Comparing figures 4.8a and 4.9a shows that a thicker oxide layer gives slightly higher encroachment on top of the pillar. The encroachment towards the bottom of the pillar sidewall at y=200nm is increased for the structures with a 20.4nm oxide layer. Figure 4.9b shows a slight increase in encroachment at x=960nm compared with figure 4.8b. It can be concluded that a thinner pad oxide for a given nitride thickness decreases the encroachment on the pillar sidewall as well as at the bottom of the pillar.

Figure 4.10 shows the distribution of stress for a structure with 5.3nm initial pad



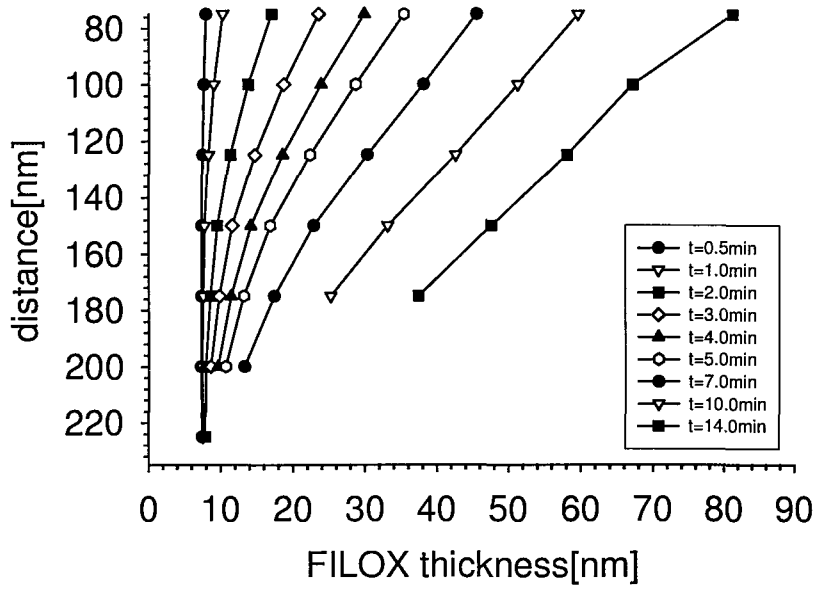
a)



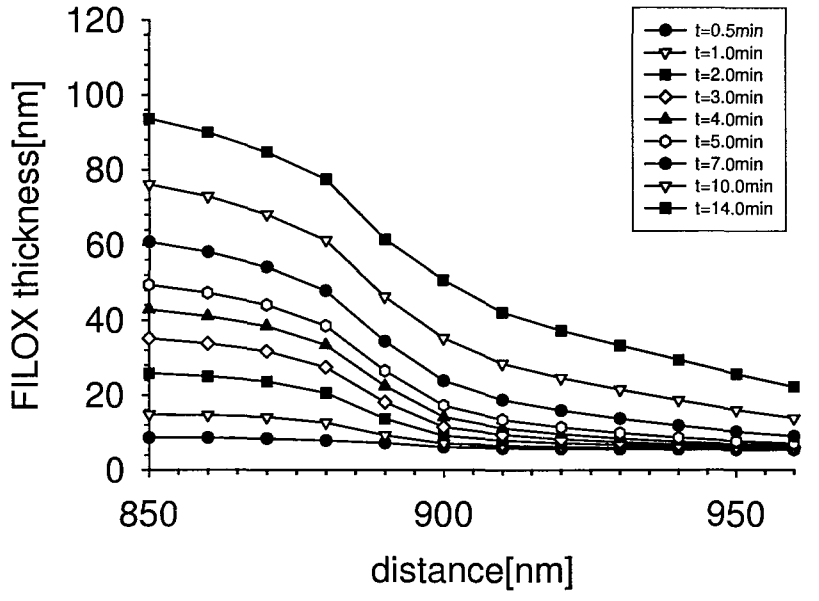
b)

Figure 4.7: FILOX thickness as a function of distance for a 5.3nm pad oxide grown at 1000°C and 70nm nitride thickness a) pillar top b) pillar bottom. The distance scale is obtained from the distance scale in figure 4.6.

oxide, a nitride fillet thickness of 70nm and an oxidation time of 3 minutes. The FILOX oxide thickness was 38.8nm at x=1.15μm. The highest amount of normal stress in the y-direction can be found in the nitride at the bottom of the pillar, as shown by the arrow in figure 4.10. Furthermore, figure 4.10 indicates a large amount of stress in the nitride fillet at the top of the pillar. It can be seen that a high amount of stress is also found in the oxide. Table 4.3 summarises the values of maximal normal stress found in the structure.



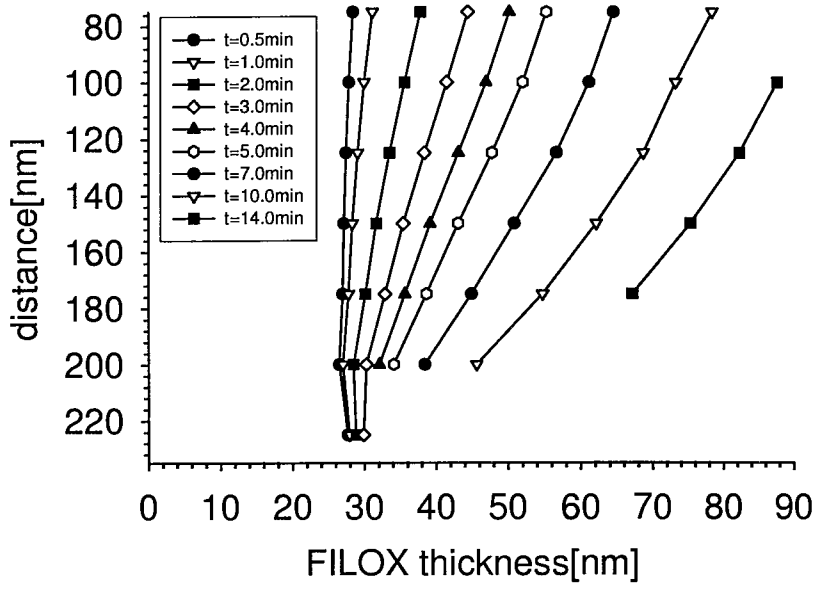
a)



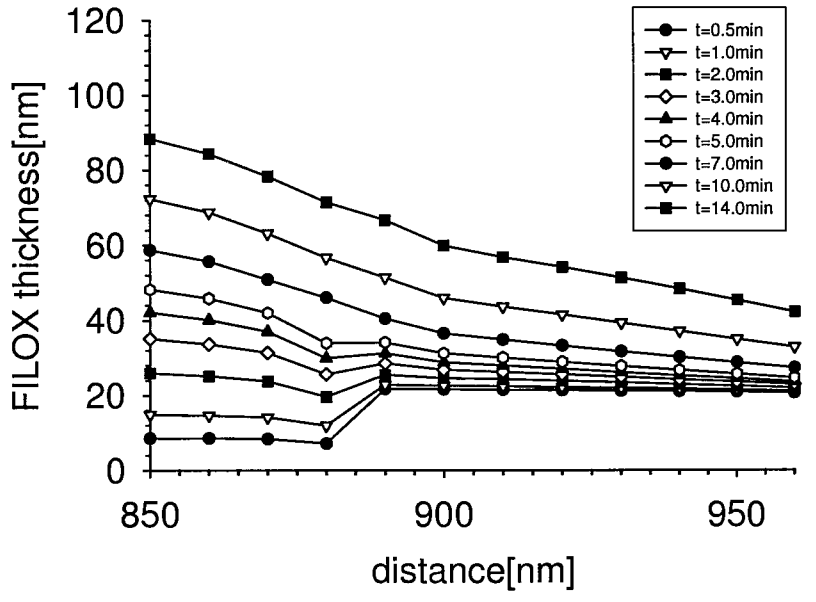
b)

Figure 4.8: FILOX thickness as a function of distance for a 5.3nm pad oxide grown at 1000°C and 130nm nitride thickness a) pillar top b) pillar bottom. The distance scale is obtained from the distance scale in figure 4.6.

Figure 4.11 shows a TEM cross-section of a fabricated test structure with a pad oxide thickness of 5nm, a nitride fillet of 40nm, a pillar height of 320nm and a FILOX oxide thickness of 160nm. It can be seen that at the bottom of the pillar a dislocation is propagating into the silicon substrate from the bottom corner of the pillar. The presence of this dislocation provides experimental evidence of the high stress at the corner of the pillar in the FILOX process when a thick oxide is grown (160nm). A comparison with the results in figure 4.7 shows that the 160nm FILOX oxide thickness in this sample would be expected to give considerable encroachment



a)



b)

Figure 4.9: FILOX thickness as a function of distance for a 20.4nm pad oxide grown at 1000°C and 130nm nitride thickness a) pillar top b) pillar bottom. The distance scale is obtained from the distance scale in figure 4.6.

at both, the bottom and top of the pillar. It can therefore be concluded that the FILOX oxide thickness should be much less than 160nm if problems with stress are to be avoided.

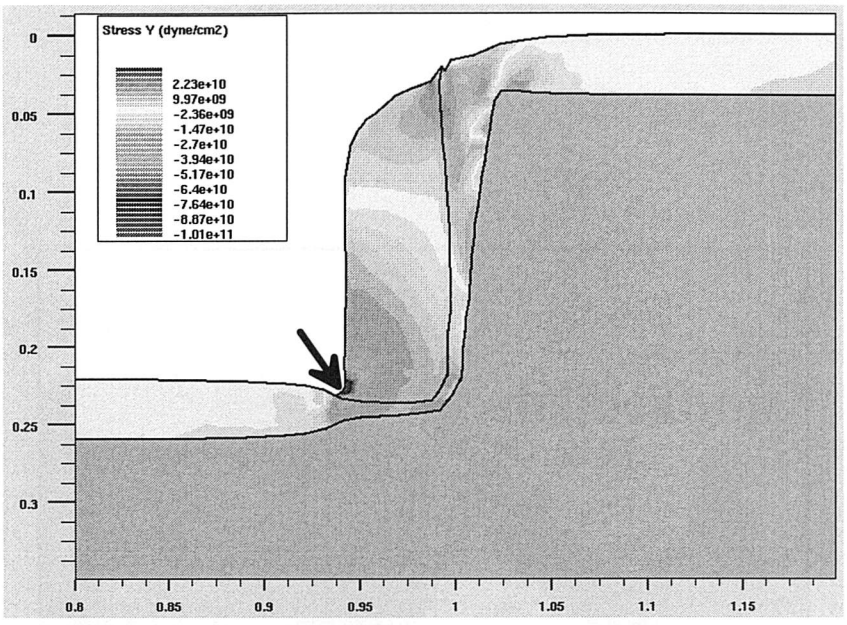


Figure 4.10: Regions of normal stress σ_{yy} in nitride for a 5.3nm initial pad oxide grown for 3 minutes at 1000°C and 70nm nitride thickness. The thickness of the FILOX oxide is 38.8nm at x=1.15μm. Arrow indicating the highest amount of normal stress σ_{yy} in the nitride fillet.

material / location	σ_{xxmax}[dyne/cm]	σ_{yymax}[dyne/cm]
oxide	6.50×10^{10}	4.73×10^{10}
x	0.931	0.940
y	0.248	0.237
nitride	1.05×10^{11}	1.01×10^{11}
x	0.940	0.942
y	0.229	0.224

Table 4.3: Extracted amounts of stress and their location in the nitride fillet and oxide for the structure shown in figure 4.10.

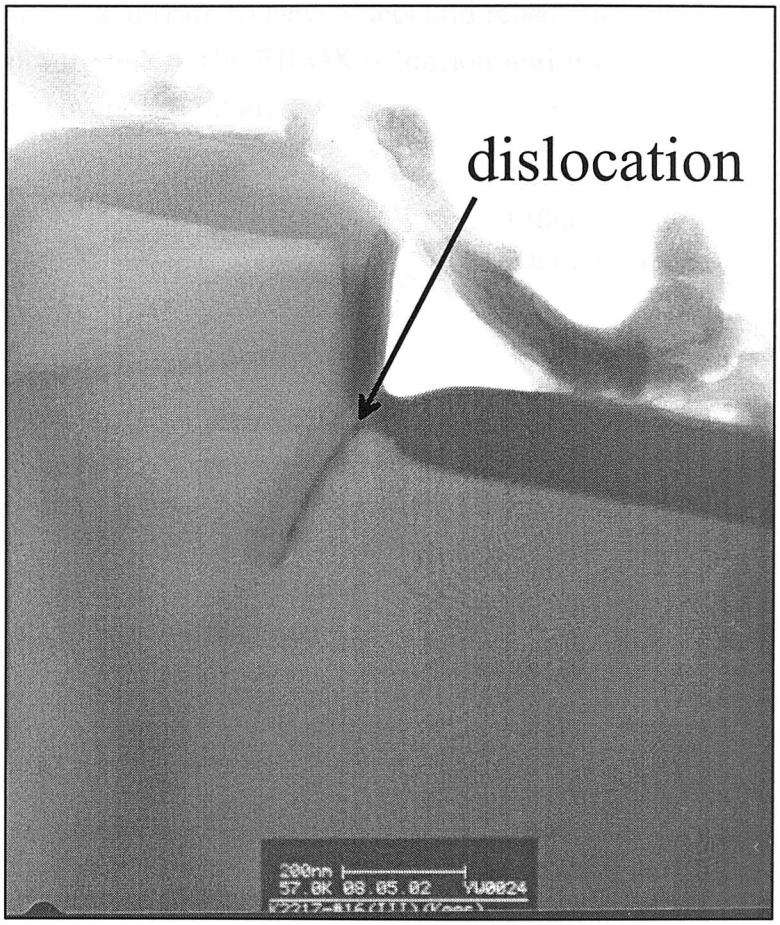


Figure 4.11: TEM cross-section of the FILOX process directly after the oxidation for 11.5 minutes at 1000°C showing dislocations at the bottom corner of the pillar. The initial pad oxide thickness was 5nm and the nitride thickness 40nm. The thickness of the FILOX oxide is 160nm.

4.6 FILOX with nitride top insulator

The encroachment at the top of the pillar can be dramatically reduced by introducing a nitride layer on top of the pillar. Figure 4.12 illustrates the process flow. A oxide/nitride/oxide stack is first deposited on a plane wafer as shown in figure 4.12a. In the following process step the nitride stack and the silicon is anisotropically etched in order to form the pillar structure. After growing the pad oxide a structure similar to that shown in figure 4.12b is obtained. The following steps include deposition and anisotropic etch of the nitride to leave fillets and anisotropic oxide etch. Figure 4.12c depicts the structure before the FILOX oxidation and it can be seen that the nitride layer completely covers the pillar.

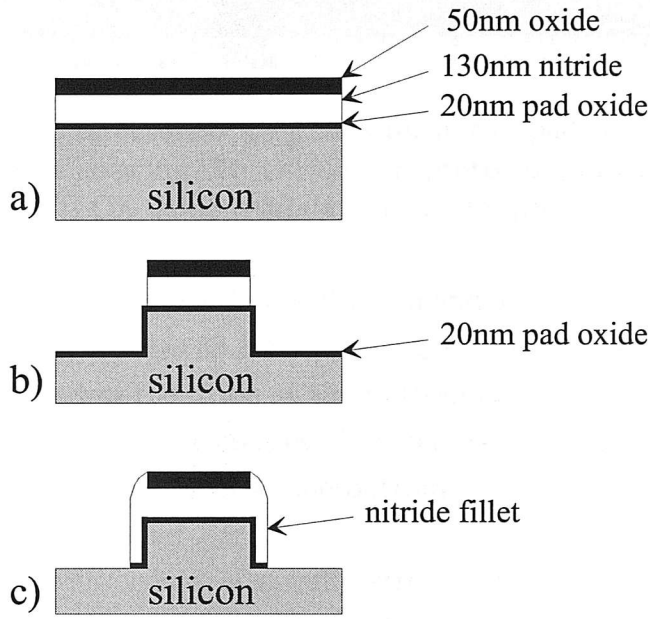


Figure 4.12: Process flow of a structure with nitride as a top insulator a) oxide/nitride/oxide stack b) after pillar etch and pad oxide growth c) after fillet and pad oxide etch

Figure 4.13 shows a simulated cross-section of the structure under consideration. The nitride layer forms a cap protecting the whole pillar structure and hence there is negligible encroachment at the top of the pillar during the FILOX oxidation. This result is confirmed in figure 4.14 which shows a graph of FILOX thickness for different oxidation times.

It can be seen that the nitride cap has completely eliminated the encroachment down the side of the pillar for oxidation times as long as 7 minutes.

Figure 4.15 shows the distribution of stress for a nitride cap structure with 5.3nm

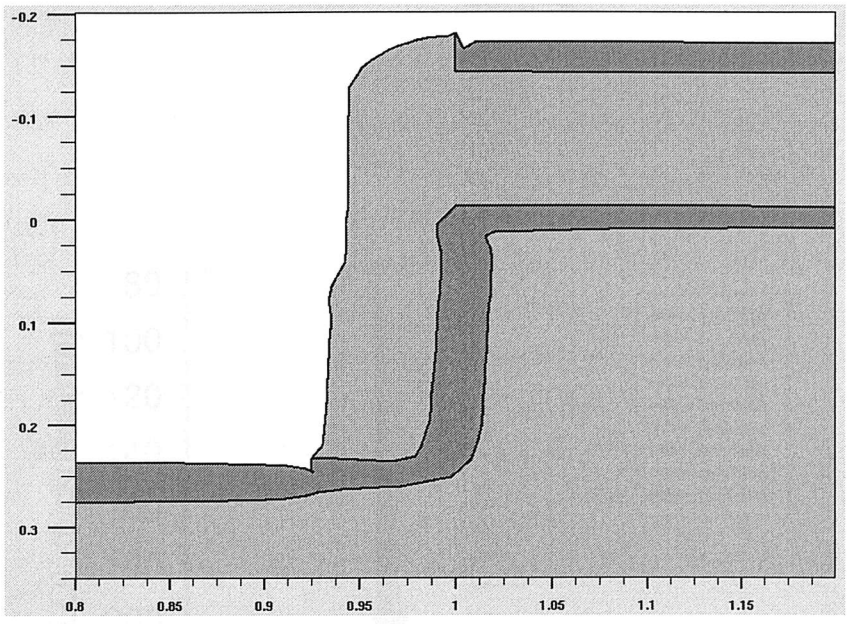
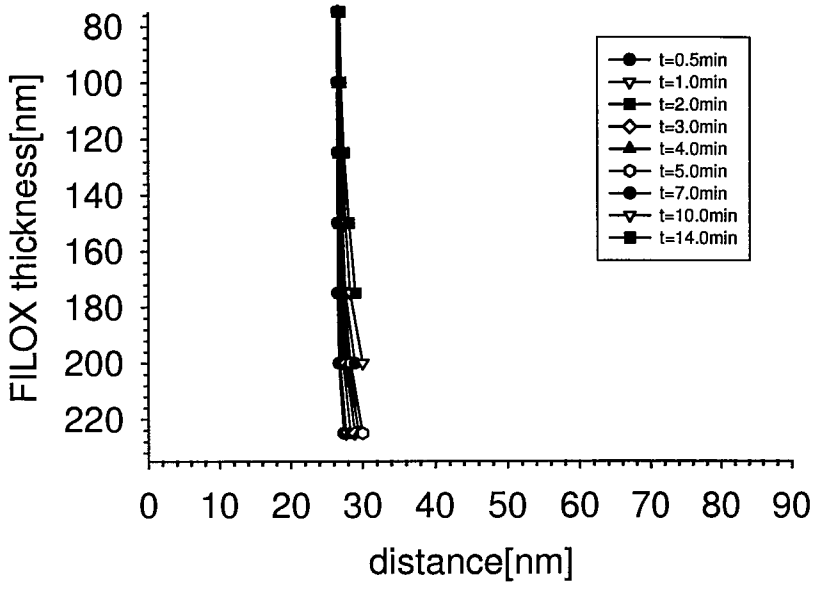


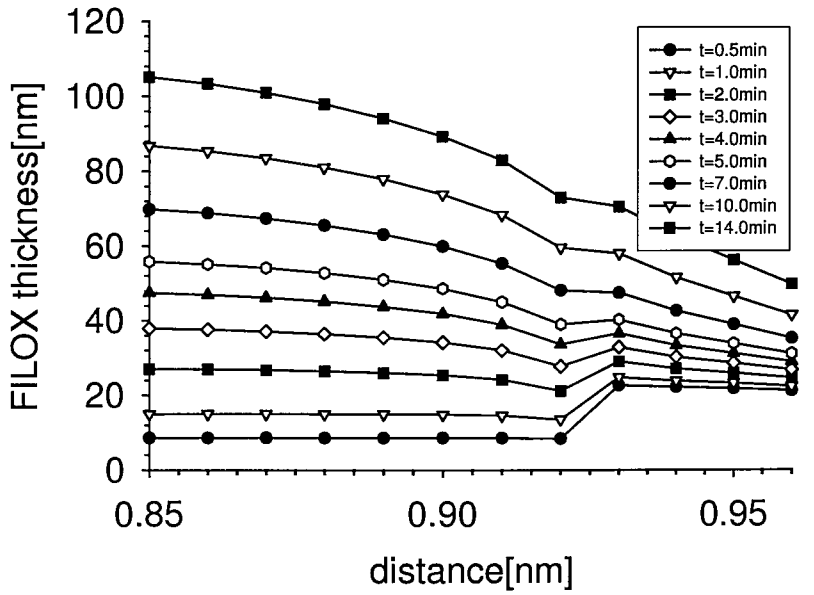
Figure 4.13: Simulated structure with a 20.4nm initial pad oxide grown at 1000^{o}C and 70nm nitride fillet showing the nitride cap protecting pillar top and sidewalls. The thickness of the FILOX oxide is 39.0nm at x=0.85μm.

initial pad oxide, a nitride fillet thickness of 70nm and an oxidation time of 3 minutes. The FILOX oxide thickness was 38.8nm. The highest amount of normal stress in the y-direction can be found in the oxide at the bottom of the nitride fillet at the bird's beak where the oxide thickness increases. Furthermore, figure 4.15 indicates a large amount of stress in the nitride fillet at the bottom of the fillet.

Table 4.4 summarises the values of normal stress found in the structure shown in figure 4.15 in both x- and y-directions. It can be seen that a high amount of stress is found, particularly in the oxide. However, comparing table 4.4 with table 4.3 shows that the stress in both the nitride and oxide in both, x- and y-direction are lower for the structures with a nitride cap than for the structure with oxide on top of the pillar. The lower stress in the structures with nitride cap could be due to the distribution of stress over a greater area of the nitride cap.



a)



b)

Figure 4.14: FILOX thickness as a function of distance for a 20.4nm pad oxide grown at 1000°C and 70nm nitride thickness a) pillar top b) pillar bottom. The distance scale is obtained from the distance scale in figure 4.6.

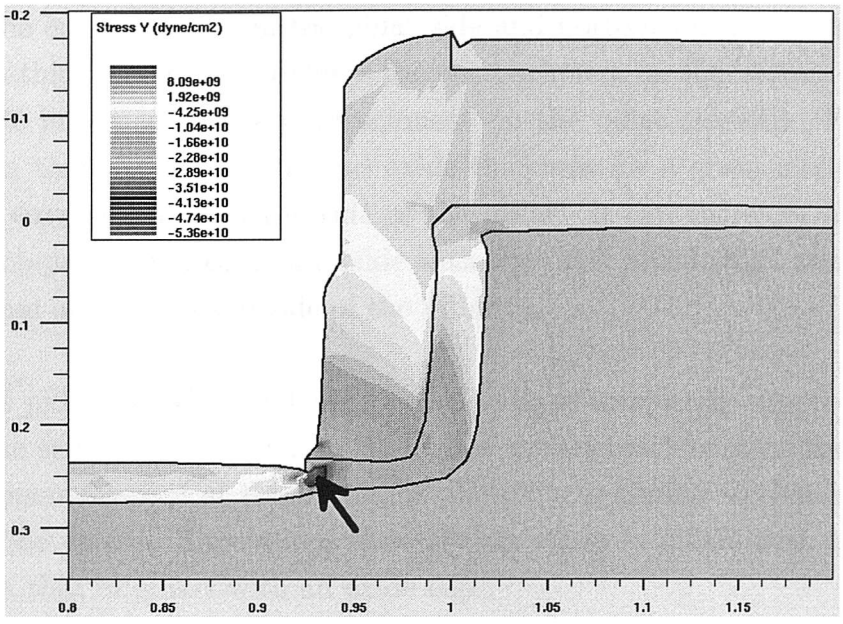


Figure 4.15: Regions of normal stress σ_{yy} in nitride for a 20.4nm initial pad oxide grown for 3 minutes at 1000°C and 70nm nitride thickness. The thickness of the FILOX oxide is 38.8nm. Arrow indicating the highest amount of normal stress σ_{yy} in the oxide.

material / location	σ_{xxmax}[dyne/cm]	σ_{yymax}[dyne/cm]
oxide	5.91×10^{10}	5.36×10^{10}
x	0.922	0.930
y	0.269	0.244
nitride	2.58×10^{10}	3.77×10^{10}
x	0.977	0.930
y	0.232	0.218

Table 4.4: Extracted amounts of stress and their location in the nitride fillet and oxide for the structure shown in figure 4.15.

4.7 Summary

In this chapter the FILOX process was simulated using calibrated values of nitride viscosity. The encroachment on the pillar side and bottom was investigated. It was found that a thick nitride fillet reduces the encroachment on the bottom of the pillar but has little influence on the encroachment on the pillar sidewall. Furthermore, it was shown that decreasing the pad oxide thickness for a given nitride thickness reduces the encroachment on the side of the pillar. It can therefore be concluded that the combination of a thin pad oxide with the thick nitride fillet results in small encroachments on the top and side of the pillar.

Covering the pillar top with a nitride insulation layer completely suppresses the oxidation on the sidewall and therefore eliminates the encroachment on the side of the pillar. The encroachment at the bottom of the pillar is similar to that in the pillars without nitride on top. Simulations showed that stress in pillars with a nitride cap is lower than that in pillars with an oxide cap.

Chapter 5

CV-characteristics of FILOX vertical capacitors

5.1 Introduction

To experimentally investigate the capacitive reduction obtained with the FILOX process a batch of capacitors was fabricated. Three different types of capacitor were fabricated namely capacitors incorporating a nitride top insulator, capacitors incorporating the FILOX process and control capacitors with neither a nitride insulator level nor the FILOX oxide. The measured results of these capacitors are compared with simulated results using Silvaco's Athena/Atlas software tool.

5.2 Experimental procedure

Figure 5.1 illustrates schematic cross-sections of the three fabricated structures. The control structure shown in figure 5.1a consists of the substrate, a thermally grown gate oxide, a polysilicon gate layer and a metal layer. Figure 5.1b shows a structure with a nitride top insulator. This insulator stack is of the same type as shown in figure 4.12a. Capacitors incorporating the FILOX process are depicted in figure 5.1c. The structure is similar to that shown in figure 5.1b with the difference that a FILOX oxide was grown at the bottom of the pillar to further reduce the capacitance.

Table 5.1 lists the process flow for the structures under consideration. The initial wafer was p-type <100> with a resistivity in the range of 0.5 to 1.0Ωcm. The fabrication process starts with a standard LOCOS process with a 20nm pad oxide and a 130nm thick nitride layer to define the active area. To build the nitride top insulator stack for the structure with nitride top insulator, a 50nm low temperature

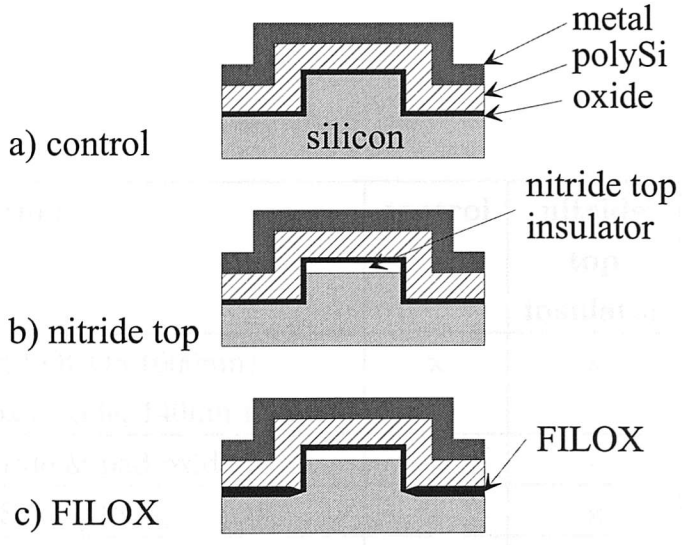


Figure 5.1: Cross-sections of fabricated capacitors a) control b) with nitride top insulator c) with FILOX and nitride top insulator.

oxide (LTO) layer was deposited on top of the nitride layer used in the LOCOS processing. All structures underwent a 300nm pillar etch. After the pillar etch a pad oxide was grown using a dry oxidation process. Nitride fillets were produced by depositing a nitride layer and anisotropic etching as shown in stages 8 and 9. Using an anisotropic oxide etch, the pad oxide was etched so that it left exposed silicon as shown in figure 4.12c. After a 100nm FILOX oxidation the nitride spacers were stripped and the 20nm pad oxide that protected the sidewalls was wet etched using a diluted 20:1 HF solution. Due to the isotropy of the oxide etch, the FILOX oxide thickness reduces to about 80nm during this step. Three different oxide thicknesses were grown in stage 14 for the three capacitor types at 800°C. A 200nm in-situ doped phosphorous polysilicon layer with a concentration of $1\times10^{19}cm^{-3}$ was used for the gate before the metal layer was deposited. The metal was masked to define the metal area and etched using a wet etch process. The polysilicon underneath the oxide was etched afterwards so that the polySi layer was self aligned to the photoresist covering the metal layer. The process finished with the deposition of the aluminium back contact. A detailed process listing can be found in the appendix C.2.

stage	description	control	nitride top insulator	FILOX	mask
1	standard LOCOS (600nm) (20nm pad oxide, 140nm nitride)	x	x	x	AA
2	strip nitride & pad oxide	x	-	-	
3	deposit SiO_2 (50nm)	-	x	x	
4	pillar lithography	x	x	x	PL
5	anisotropic SiO_2 & Si_3N_4 & SiO_2 etch	-	x	x	
6	anisotropic pillar etch (400nm into Si)	x	x	x	
7	dry oxidation (20nm at 800°C)	x	x	x	
8	deposit 70nm Si_3N_4 at 740°C	-	-	x	
9	dry etch Si_3N_4 to leave fillets	-	-	x	
10	dry etch 20nm pad oxide	-	-	x	
11	100nm FILOX at 1000°C	-	-	x	
12	strip nitride spacers	-	-	x	
13	wet etch 20nm pad oxide	x	x	x	
14	4/8/12nm gate oxidation at 800°C	x	x	x	
15	200nm in-situ P doped polySi ($1\times10^{19}cm^{-3}$)	x	x	x	
16	metal deposition	x	x	x	
17	metal/polySi lithography	x	x	x	M1
18	metal etch	x	x	x	
19	polySi etch	x	x	x	
20	back contact	x	x	x	

Table 5.1: Process list and batch splits for vertical capacitors

Table 5.2 shows the measured material thicknesses of all three fabricated structures. It can be seen that there is some variability in the pillar height because of difficulty in controlling the etch as it has no end point and is very short (~1.5min). Electrical measurements showed that the substrate resistivity was 0.75Ωcm which corresponds to a doping concentration of $2\times10^{16}cm^{-3}$. For the deposited polysilicon a thickness of 220nm was measured. The measured polysilicon resistivity was 0.011Ωcm which implies a doping concentration of $1\times10^{19}cm^{-3}$.

material	**control[nm]**	**nitride top insulator[nm]**	**FILOX[nm]**
nitride	138	150	146
LTO	-	63	64
pillar height	400	320	460
FILOX thickness	-	-	97
LOCOS thickness after HF dip etch	511	500	510

Table 5.2: Measured material thicknesses for control, nitride top and FILOX capacitors

5.2.1 Mask layout

For each of the three types of capacitors, three different devices were fabricated to investigate the capacitive behaviour of all horizontal and vertical surfaces. Figure 5.2a shows a trench capacitor. The dimensions of the capacitor are given by x_a and x_b (see appendix B.1). The gate is contacted via a metal layer on top of the polySi layer and by the backside contact of the silicon wafer. This capacitor can be used to characterise the FILOX process. Figure 5.2b shows a top capacitor similar to the one in figure 5.2a but with the capacitance on top of the pillar. This capacitor can be used to characterise the insulator on top of the pillar. Figure 5.2c depicts a pillar capacitor in which the polySi/metal stack is deposited over the entire pillar and trench structure. Again, this capacitor consists of a polySi gate which is self aligned to the photoresist layer on top of the metal layer. The structure has no corners since the metal/polySi area is smaller than the length of the pillars. Various pillar/trench ratios have been realised. The capacitor shown in figure 5.2c has a trench width of 3μm and a pillar width of 1.5μm.

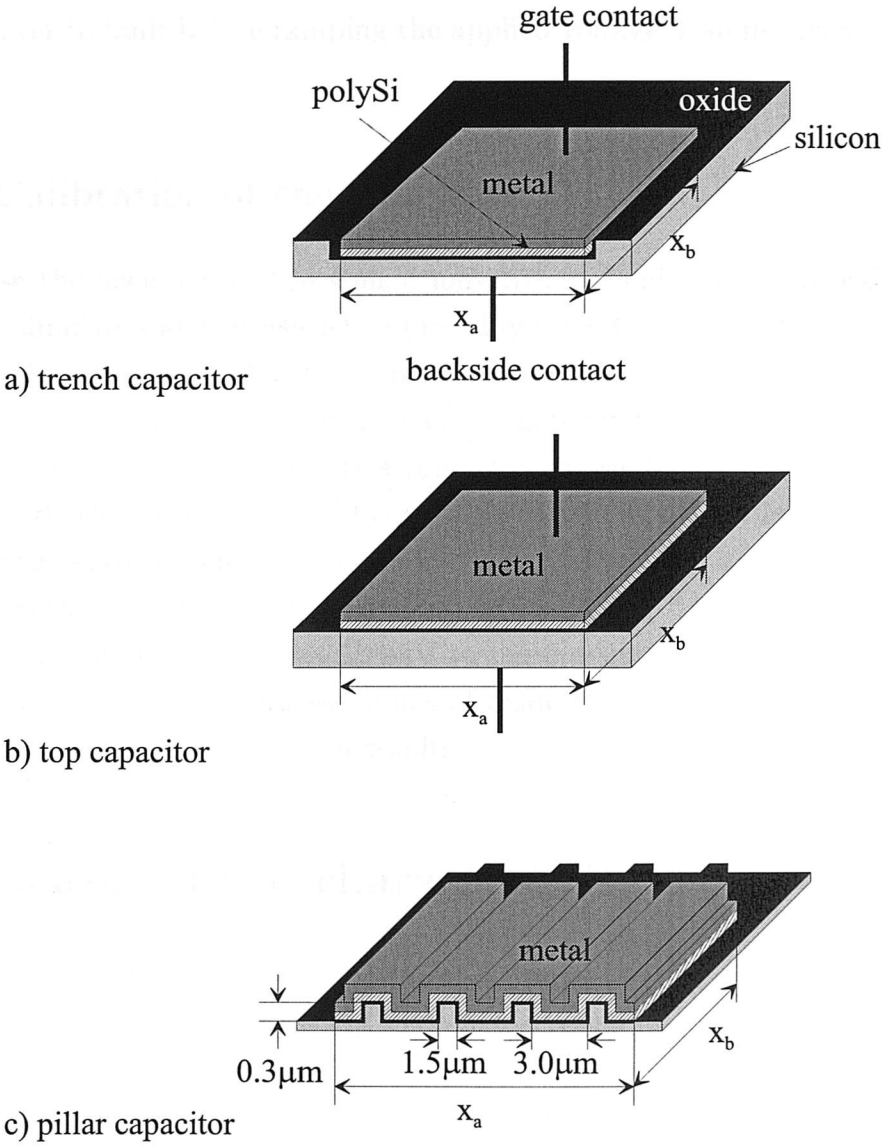


Figure 5.2: Fabricated capacitors a) cross-section of a trench capacitor b) cross-section of a top capacitor c) cross-section of a pillar capacitor.

5.2.2 Electrical characterisation

To characterise the fabricated capacitors, high frequency (HF) capacitance/voltage (CV) characteristics were measured using an HP4280A capacitance meter. The frequency for all measurements was 1MHz and the ac signal amplitude 30mV. For all measurements *ground* was connected to the back of the wafer whilst the *signal* was connected to the probe pad. The wafer was illuminated for 10 seconds to allow an inversion layer to built before ramping the applied voltage from inversion to accumulation.

5.2.3 Calibration of the simulator

To optimise the accuracy of the simulations Athena and Atlas were calibrated by comparing simulated and measured results. Figure 5.3 illustrates the measured and simulated CV curves of a pillar top capacitor. In accumulation the measured capacitance is $7.0\times10^{-3}\mathrm{Fm}^{-2}$ at -4V for a measured gate oxide thickness of 3.9nm. Using the default parameters, Athena/Atlas predicts a capacitance of $8.6\times10^{-3}\mathrm{Fm}^{-2}$ for the same oxide thickness at -4V. This value is clearly to high. Simulating the same structure with an oxide thickness of 4.8nm decreases the capacitance to the measured value. Furthermore, a fixed oxide charge Q_f of $7\times10^{10}cm^{-2}$ was included in the simulation to shift the plot by about 100mV to more negative voltages compared with no oxide charge. These calibrated values of oxide thickness and fixed oxide charge are used in the following simulation results.

5.3 Measured CV characteristics

Figure 5.4 depicts typical CV plots of the three types of pillar capacitor namely control, nitride top insulator and FILOX. The metal probe pad capacitance of the three structures (1.19, 1.30 and 1.24pF) was subtracted prior to plotting. The nitride top capacitor shows a lower capacitance at V_G=-4V by a factor of 1.43 compared with the control. The FILOX capacitor shows a lower capacitance by a factor of 5.64 compared with the control.

In inversion a small increase in capacitance can be seen for the control structure at about -0.1V. This effect will be discussed in detail in section 5.5.2. Beyond 0.7V the capacitance decreases gradually with increasing gate voltage, probably due to oxide leakage. Similar behaviour can also be seen for the capacitors with nitride top and FILOX.

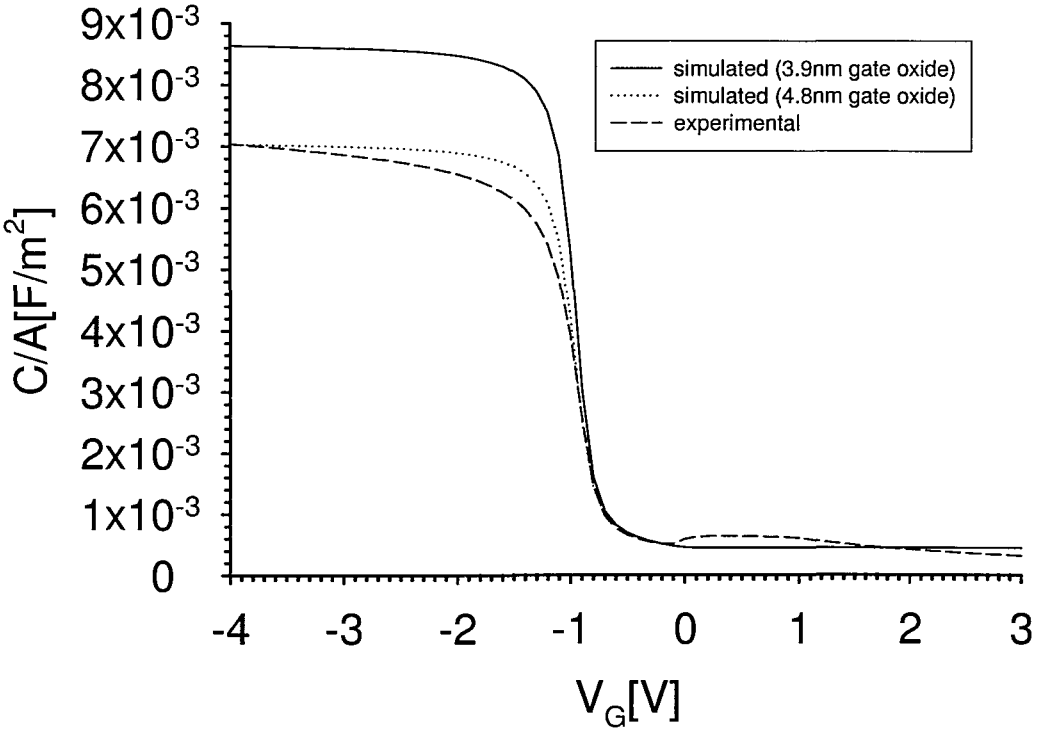


Figure 5.3: Comparison of simulated default, calibrated and measured capacitances per unit area for a top capacitor. For the simulation and measurements the frequency was 1MHz. The ac amplitude was 30mV for the measured structure and 100mV for the simulation.

5.4 Simulated CV characteristics

Figure 5.5 shows a comparison of simulated and measured CV results of all three capacitors. For the simulations calibrated values of oxide thickness and fixed oxide charge were assumed. For the control structure the agreement between measured and simulated data is reasonably good. The simulated capacitance in accumulation at -4V is slightly higher than the measured value by a factor of 1.05 compared with the measured result. For the structures with a nitride top insulator the simulated value at -4V is higher by a factor of 1.10. In contrast for the FILOX capacitor the simulated capacitance at -4V is slightly lower than the measured value by a factor of 1.04. The simulation gives a FILOX thickness of 92nm compared with the measured value of 97nm for the fabricated structure.

Figure 5.6 compares simulated and measured values of capacitance on a total of 4 capacitors from one part of the wafer. Means and standard deviation are presented at V_G=-4V. The standard deviations σ for the control, nitride top and FILOX capacitors are 0.21, 0.14, $0.08\times10^{-3}F/m^2$, respectively. The mean values of capacitance follow the same trend as seen in figure 5.5.

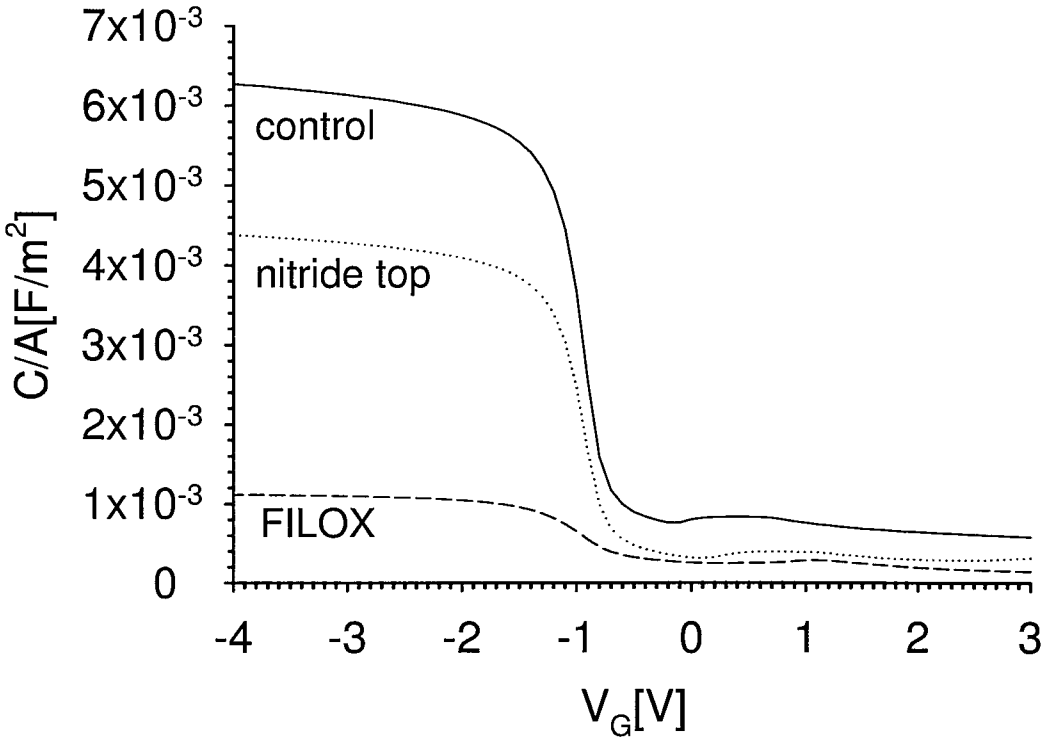


Figure 5.4: Comparison of measured CV graphs of a control, nitride top insulator and FILOX capacitor. The frequency was 1MHz and the ac amplitude 30mV.

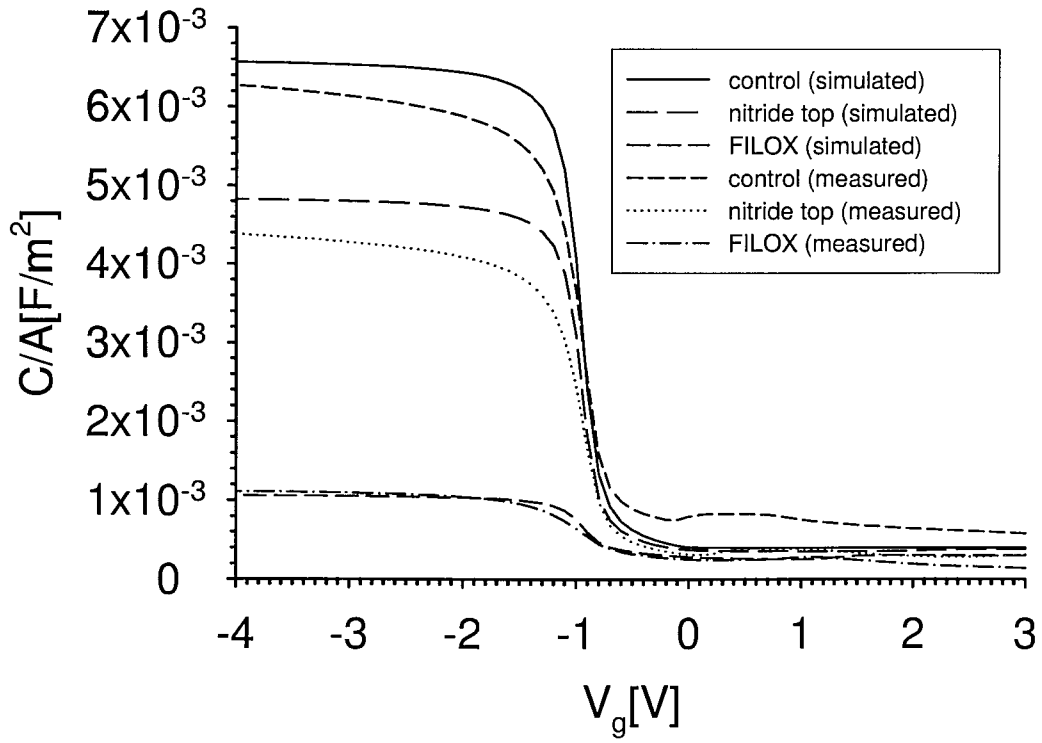


Figure 5.5: Comparison of calibrated simulated and measured CV graphs of control, nitride top and FILOX capacitors. For the simulation and measurements the frequency was 1MHz. The ac amplitude was 30mV for the measured structures and 100mV for the simulations.

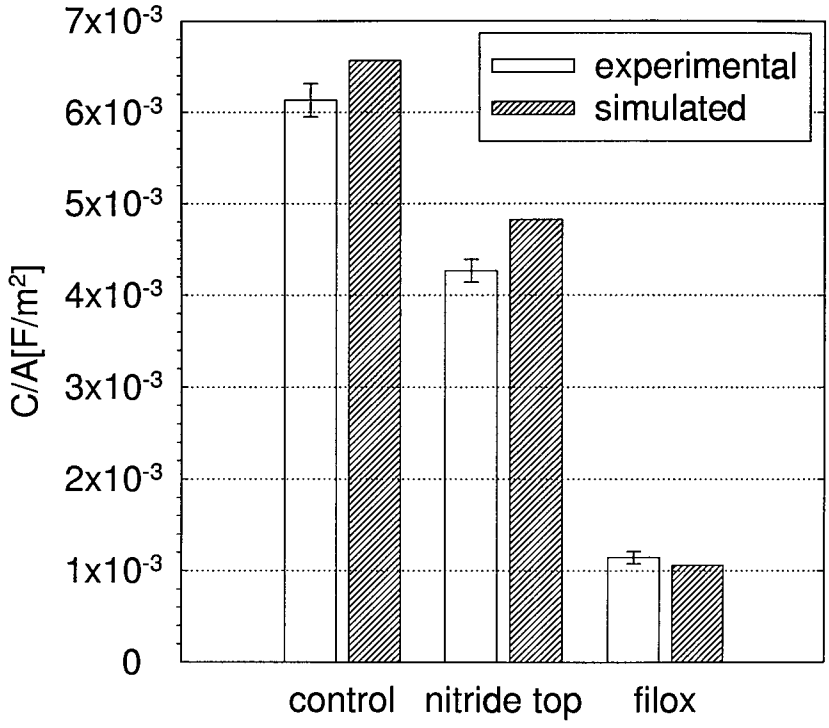


Figure 5.6: Comparison of calibrated simulated and measured capacitances at V_G=-4.0V of control, nitride top and FILOX capacitors. Also shown is the standard deviation of 4 measured structures for each capacitor type.

5.5 Discussion

In this section the oxide thickness on the sidewall of the pillar will be extracted. Furthermore, an explanation for the increased capacitance in inversion is presented.

5.5.1 Extraction of oxide thickness on the pillar sidewall

To perform the extraction of oxide thickness on the pillar sidewall, measured capacitance values at -4V have been used. Top and trench capacitors were measured to get accurate capacitance values of the top and trench areas covered by the polySi for the extraction of the sidewall capacitance. Figure 5.7 depicts the dimensions of a control capacitor cell used in the following for the extraction of the oxide thickness on the pillar sidewall.

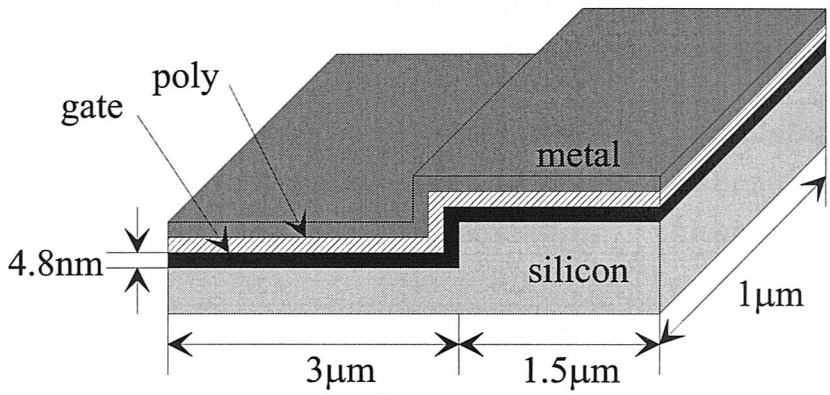


Figure 5.7: Cross-section of a control capacitor cell showing the dimensions.

Table 5.3 shows the extracted capacitance values for all three capacitor types as well as capacitance values for top and trench capacitors (see figure 5.2) per cell. To extract the oxide thickness on the sidewall, the pillar height shown in table 5.2 was used. For both, control and nitride top capacitors the extracted sidewall capacitance is up to 15 times smaller than the top or trench capacitance which can result in significant errors in the extracted sidewall capacitance. This is not the case for the FILOX capacitor, where the extracted sidewall capacitance is about three times higher than the top capacitance and about two times higher than the trench capacitance.

Table 5.4 shows the extracted and simulated oxide thicknesses on the pillar sidewalls for three types of pillar capacitors based on the extracted capacitance values of table 5.3. For the control capacitor the extracted oxide thickness is higher by a factor of 2.5 compared with the simulated oxide thickness on the sidewall. The extracted sidewall oxide thickness of the nitride top capacitor is a factor of 1.9 higher than the

type	total C	top C	trench C	extracted sidewall C
control [$\times 10^{-15} F/\mu$m per cell]	32.5	10.4	20.7	1.37
nitride top [$\times 10^{-15} F/\mu$m per cell]	21.9	1.33	19.2	1.44
FILOX [$\times 10^{-15} F/\mu$m per cell]	6.20	1.08	1.70	3.41

Table 5.3: Extracted capacitance values for control, nitride top and FILOX capacitors per cell (see figure 5.7). Also shown are the associated top and trench capacitances. All capacitances were measured at -4V.

simulated value. These discrepancies can be explained by the errors in subtracting the top and trench capacitances from the total capacitance, as seen in table 5.3.

type	extracted sidewall oxide thickness[nm]	simulated sidewall oxide thickness[nm]	simulated planar oxide thickness[nm]
control	20.1	8.1	4.8
nitride top	15.3	8.2	4.8
FILOX	9.3	7.9	4.8

Table 5.4: Extracted and simulated oxide thickness on the pillar sidewalls for control, nitride top insulator and FILOX capacitors

5.5.2 Behaviour in inversion

In this section the increase in capacitance for the control capacitors and the FILOX capacitors will be investigated in more detail. A model will be introduced to show the increase of capacitance in inversion for control capacitors. This model will be used to interpret the results on the FILOX capacitors.

The measured result in figure 5.4 showed that there was an increase in capacitance in inversion. For the control capacitor an increase in capacitance in inversion can be seen from the expanded plot in figure 5.8 at about -0.1V whilst the onset of increased inversion capacitance for nitride top capacitors is at about 0.2V. FILOX capacitors show an increase in capacitance at about 0.7V.

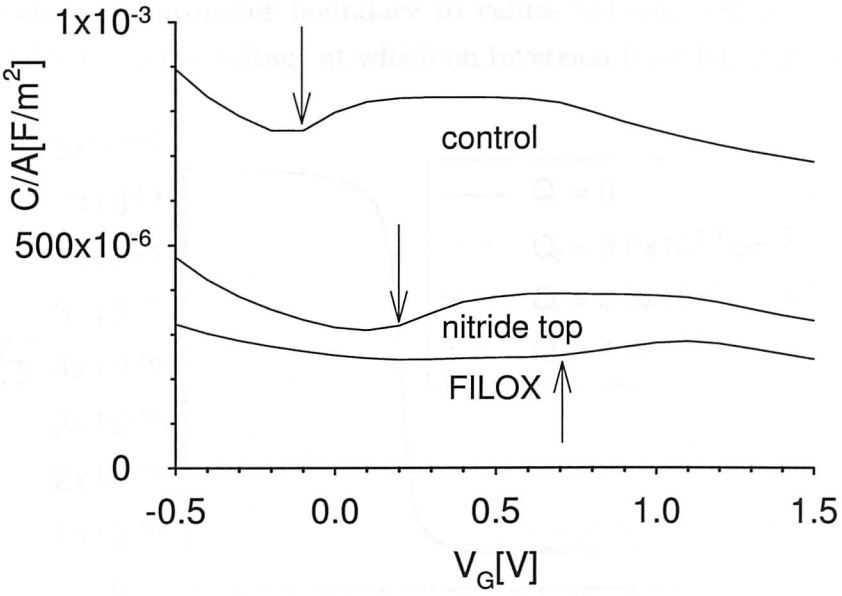


Figure 5.8: Measured CV graphs of a control, nitride top insulator and FILOX capacitor in inversion. The frequency was 1MHz and the ac amplitude 30mV.

Control capacitors

To explain this behaviour the structure depicted in figure 5.9 is considered which comprises two adjacent capacitors C_1 and C_2. Both capacitors share the same substrate but have different oxide thicknesses. This mimics the situation in practice for a control capacitor, where the two oxides are a gate oxide of 4.8nm thickness and a LOCOS field oxide of 510nm thickness.

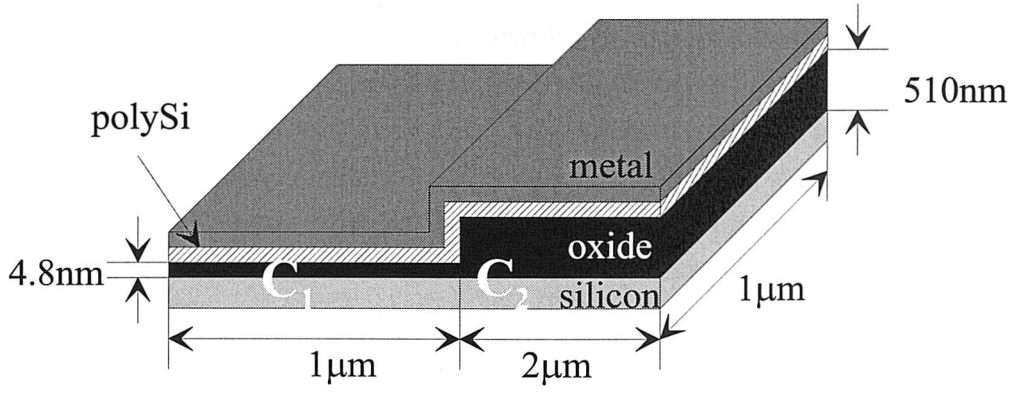


Figure 5.9: Simulated structure with two different oxide thicknesses

To investigate the voltage at which the increase in capacitance in inversion occurs, capacitors were simulated with different values of fixed charge in capacitor C_2 as shown in figure 5.10. The oxide thickness of C_1 was 4.8 and 510nm for C_2. For the case of no interface charge no increase in capacitance in inversion is observed since the threshold voltage of C_2 is very high. However, increasing the interface charge

at the semiconductor/insulator boundary to values between 3.0 and $4.0\times10^{11}cm^{-2}$ dramatically decreases the voltage at which an inversion layer forms in capacitor C_2.

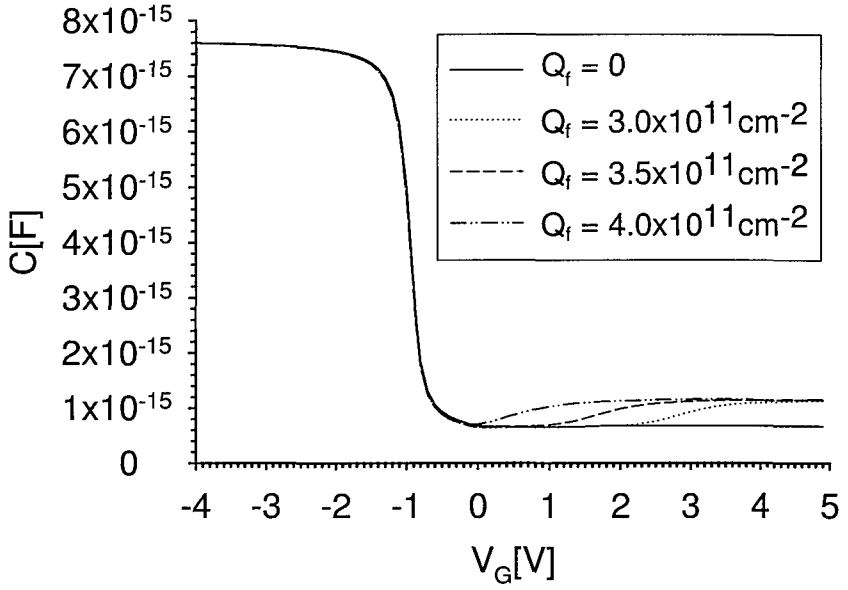


Figure 5.10: Simulated CV graphs for the structure shown in figure 5.9 for various interface charges Q_f at the interface of C_2. The oxide thickness was 4.8 and 510nm for C_1 and C_2, respectively.

Figure 5.11 shows the simulated electron concentration n_p in the substrate of C_2 for two different gate voltages. At a distance of 300nm from the surface the electron concentration is in equilibrium ($n_{p0} \simeq n_i^2/N_A$) for all applied voltages. A value for n_{p0} of $1\times10^4cm^{-2}$ can be extracted from the graph. At a gate voltage of 0V, C_2 is in weak inversion since the electron concentration at the surface ($8.5\times10^{12}cm^{-2}$) is between the intrinsic carrier concentration n_i and the substrate doping concentration N_A of $2\times10^{16}cm^{-2}$. This case is depicted in figure 5.12a where the depth of the two depletion regions of both capacitors are different. However, further increase in the gate voltage to 5V causes strong inversion for both capacitors C_1 and C_2. The electron concentration of C_2 is at the surface in this case greater than the substrate doping concentration, with a value of $2\times10^{17}cm^{-2}$. A continuous inversion layer connects both capacitors as shown in figure 5.12b.

Figure 5.13 depicts the equivalent circuits for three regions of operation. In accumulation, at V_G=-4V the structure behaves as two oxide capacitances C_{ox1} and C_{ox2} in parallel. The model for this region of the characteristic is presented in figure 5.13a. For more positive voltages both capacitors deplete until C_1 the capacitor with the thinner oxide reaches inversion (at a gate voltage of about 0V). At this voltage C_2 is still in depletion/weak inversion and hence there is no continuous inversion layer

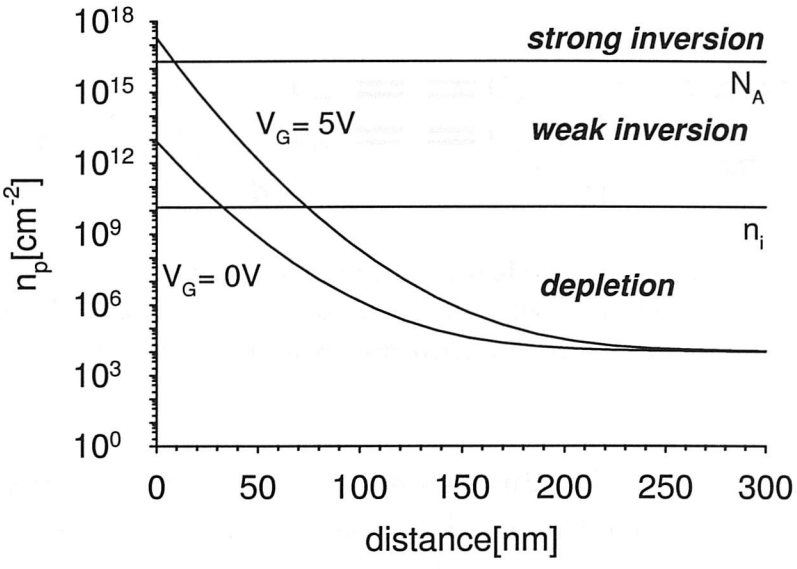


Figure 5.11: Simulated electron concentration in the substrate for 2 different gate voltages for C_2 of the structure shown in figure 5.9. The oxide thickness was 510nm and the interface charge Q_f was $3.5\times10^{11}cm^{-2}$.

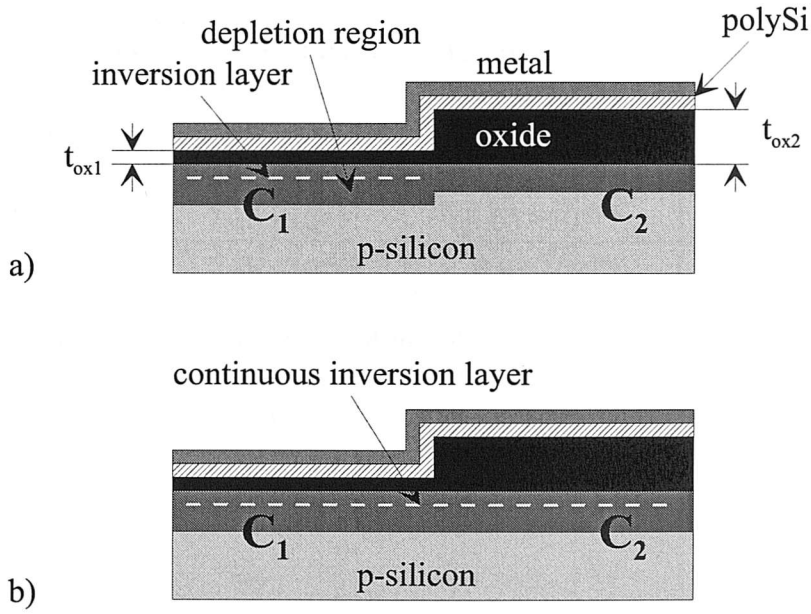


Figure 5.12: Cross-section of a capacitor with two different oxide thicknesses a) C_1 in inversion whilst C_2 is in depletion/weak inversion b) C_1 and C_2 in strong inversion.

for C_2. The simulations show that the depletion region widths differ as illustrated in figure 5.12a. Here, the depletion region of C_1 has reached its maximum value whilst the depletion region of C_2 is smaller. The model for this case is shown in figure 5.13b where the structure behave as two independent capacitors connected in parallel. A further increase in gate voltage causes a continuous inversion layer to build for both capacitors. Electrons can now move between the two adjacent capacitors. The model

for this situation is shown in figure 5.13c.

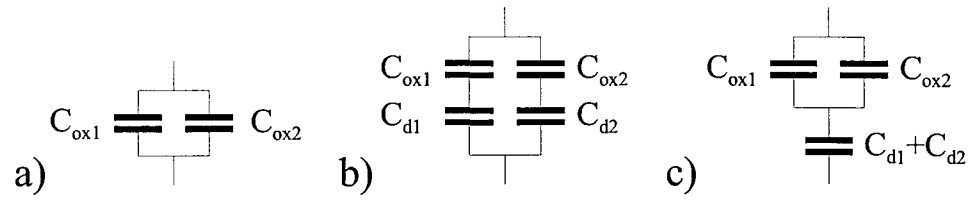


Figure 5.13: Equivalent circuits of the structure shown in figure 5.9 for three modes of operation a) C_1 and C_2 in accumulation b) C_1 in inversion, C_2 in depletion/weak inversion c) C_1 and C_2 in strong inversion with a continues inversion layer.

To test the model shown in figure 5.13 a comparison between capacitances calculated using the model in figure 5.13 and the simulated CV characteristics was made. Table 5.5 compares calculated and simulated capacitance values for three regions of operation. For the calculations an abrupt junction was assumed. The maximum depletion region width x_d was calculated to be 217nm. Very good agreement for all three regions is achieved.

capacitance	**accumulation at V_g=-4V**	**C_1 in strong inversion, C_2 in depletion at V_g=0.0V**	**C_1 and C_2 in strong inversion at V_g=5V**
calculated[F]	7.33×10^{-15}	5.65×10^{-16}	1.20×10^{-15}
simulated[F]	7.59×10^{-15}	6.9×10^{-16}	1.15×10^{-15}

Table 5.5: Calculated and simulated capacitances of the plot shown in figure 5.10 for three modes of operation as depict in figure 5.13. The oxide thickness of C_1 was 4.8nm and 510nm for C_2. The width of C_1 was 1μm and 2μm for C_2 and the interface charge $4.0\times10^{11}cm^{-2}$.

Figure 5.14 compares the CV characteristics of a measured and simulated control capacitor. For the simulation the interface charge was $4.5\times10^{11}cm^{-2}$. The ratio of field oxide to gate oxide area was for both cases 1.0. The simulated and measured results show very similar behaviour in inversion. The onset of the capacitance increase in inversion of the simulated plot is at -0.2V, which is in very good agreement of the increase in inversion compared with the measured results. The high value of field oxide charge of $4.5\times10^{11}cm^{-2}$ used in the simulations implies that the quality of the LOCOS field oxide is poor in these capacitors. The 600nm LOCOS field oxide was grown at a temperature of 1000°C in a hydrogen/oxygen ambient for 128 minutes. Performing a high-pressure dry oxidation would probably reduce the interfacial oxide

charge. Another way would be to perform a hydrogen anneal to reduce the amount of dangling bonds at the oxide silicon interface.

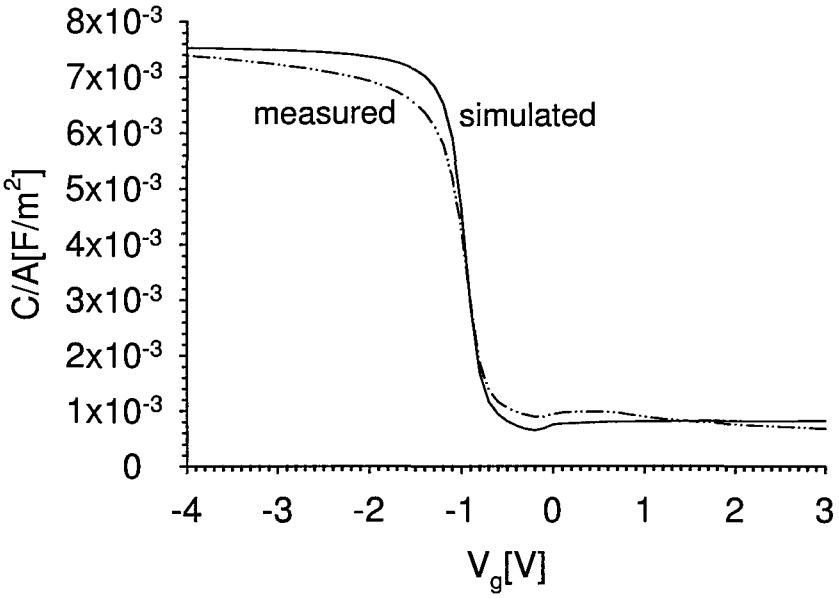


Figure 5.14: Simulated and measured results of a control device including the probe pad. The simulated structure was similar to that shown in figure 5.9 with the exception that the width of C_2 was 1μm and the interface charge $4.5\times10^{11}cm^{-2}$.

FILOX capacitors

To investigate the influence of the increase in capacitance in inversion for FILOX capacitors, a structure was simulated as shown in figure 5.15. The structure consists of three oxide thicknesses of 510, 92 and 4.8 nm to mime the LOCOS field oxide, the FILOX oxide and the gate oxide. The width of the LOCOS region was 6.3μm, the width of the FILOX region 3.0μm and of the gate region 0.6μm.

Figure 5.16 shows the simulated CV characteristics of the structure shown in figure 5.15. The interface charge Q_f at the LOCOS field oxide/silicon and FILOX oxide/silicon interface were 3.0 and $3.5\times10^{11}cm^{-2}$ and for the gate oxide/silicon interface $7.0\times10^{10}cm^{-2}$. For an interface charge of $3.0\times10^{11}cm^{-2}$ a kink is visible at a gate voltage of 0.6V caused by the formation of an inversion layer underneath the FILOX oxide. A second kink at a gate voltage of 3.2V is caused by an inversion layer building up underneath the LOCOS field oxide. Increasing the interface charge at the LOCOS field oxide/silicon and FILOX oxide/silicon interface to $3.5\times10^{11}cm^{-2}$ shifts both, the kink caused by the FILOX oxide and the kink caused by the LOCOS field oxide. A shift of 1.7V can be found for the LOCOS field oxide whilst for the FILOX oxide a shift of 0.2V can be found. A comparison of the simulation results in

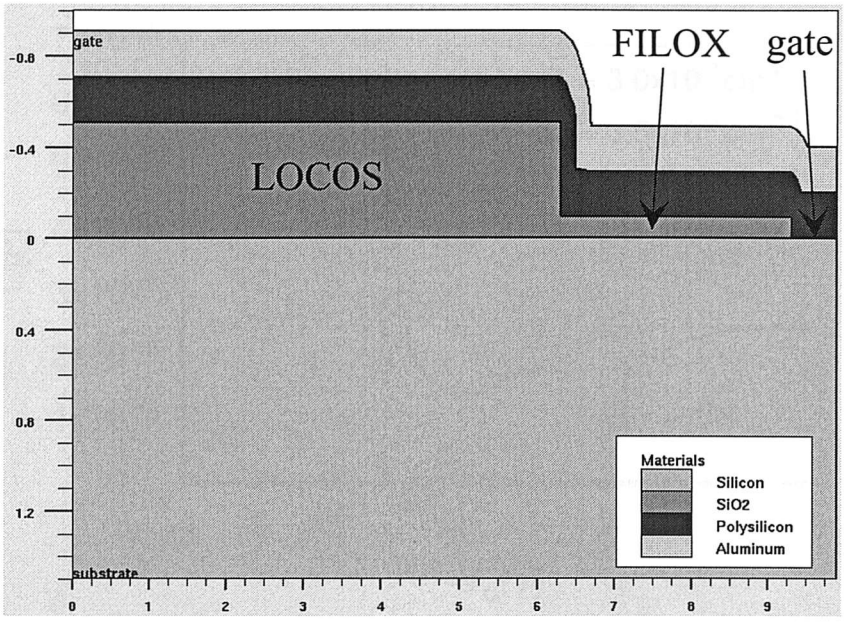


Figure 5.15: Simulated structure with three different oxide thicknesses (510, 92, 4.8nm).

figure 5.16 with the measured results in figure 5.8 shows that there is no evidence of a double kink in the FILOX capacitors. This suggests that the fixed oxide charge in the FILOX oxide is much lower than the values used in the simulations. The 100nm FILOX oxide was grown at a temperature of 1000°C in a hydrogen/oxygen ambient for 8 minutes. This method is the same as that used for the LOCOS field oxide and hence we could expect similar values of fixed oxide charge for the two oxides. However, the LOCOS field oxidation might cause segregation of boron into the oxide. This could causes a drop in surface concentration and therefore an inversion layer underneath the oxide. The kink caused by the FILOX oxidation can not be seen.

5.6 Summary

In this chapter the FILOX process was applied to fabricate pillar capacitors. A comparison between pillar control structures, pillar structures with nitride top and pillar structures with FILOX showed great reduction of capacitance for structures with nitride top ($\times 1.4$) and FILOX ($\times 5.6$). The fabricated structures were compared with simulated capacitors, and agreement within a range of 10% was obtained in accumulation.

The sidewall oxide thickness was extracted and compared with the simulated sidewall oxide thickness. The extracted sidewall oxide thickness for FILOX capacitors was 9.3nm, compared with the simulated value of 7.9nm. Kinks in the CV character-

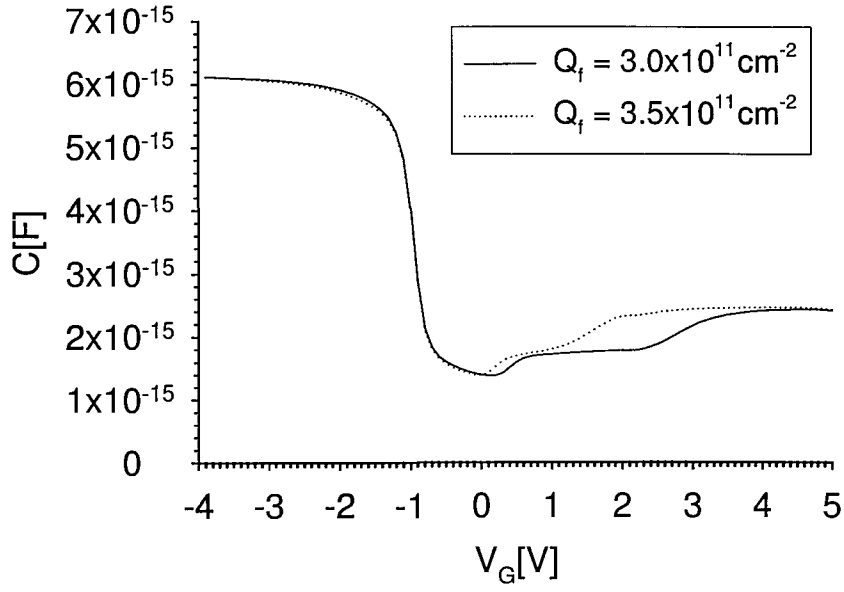


Figure 5.16: Simulated CV graphs for the structure shown in figure 5.15 for two interface charges Q_f at the interface of the two thick oxides and an gate oxide charge of Q_f=$7.0\times10^{10}cm^{-2}$.

istics in inversion have been explained by the formation of an inversion layer beneath the LOCOS field oxide.

Chapter 6

DC-characteristics of FILOX vertical MOSFETs

6.1 Introduction

In this chapter results of fabricated vertical single and surround gate n-channel MOS devices based on the gate after implant (GAI) and gate before implant (GBI) process sequences incorporating the FILOX process are presented. Process and device simulations are shown for comparison with the measured results. Furthermore, vertical logic gates are presented.

6.2 Concept

Figure 6.1 illustrates a cross-section of a vertical surround gate MOSFET incorporating the FILOX process. The drain area at the pillar bottom surrounds the pillar and the p^+ region functions as a substrate contact. The FILOX oxide covers the bottom of the trench as well as the top of the pillar and reduces the gate/drain and gate/source overlap capacitances. A further reduction of these overlap capacitances is obtained from the FILOX bird's beaks at the top and bottom of the pillar.

Figure 6.2a shows a top-view of a surround gate transistor. A polySi removal mask is introduced, which allows the fabrication of single, multi or surround gate transistors on the same wafer. Figure 6.2 illustrates the process sequence for using the polySi removal mask (PR). The mask only covers the top area where the polySi should remain (figure 6.2b). After an isotropic polySi etch which etches off parts of the polySi sidewall spacer, a single gate structure as shown in figure 6.2c is obtained.

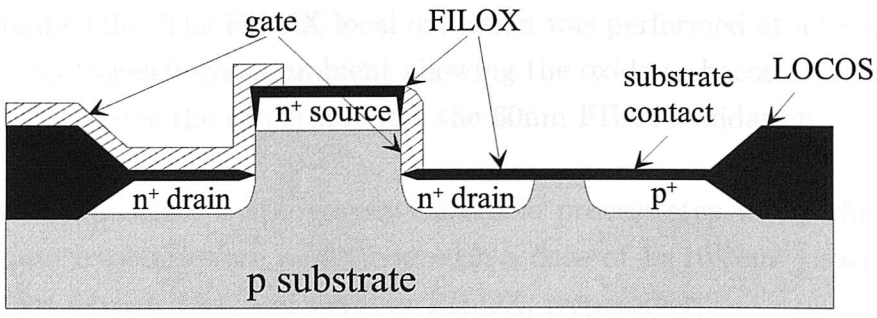


Figure 6.1: Cross-section of a surround gate vertical MOSFET with FILOX.

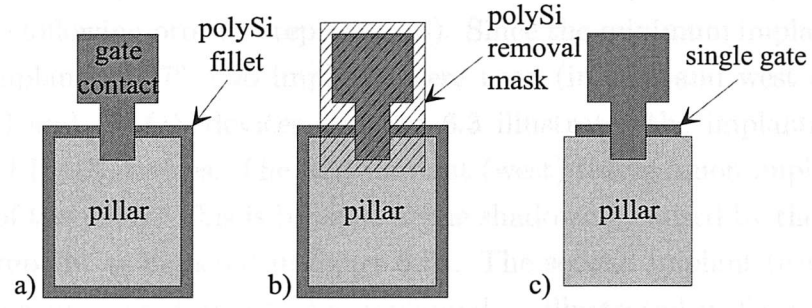


Figure 6.2: Top-view of a vertical MOSFET structure a) after polySi deposition and etch b) with polySi removal mask c) after second polySi etch. The polySi removal mask reduced the surround gate to a single gate.

6.3 Experimental procedure

A batch was fabricated to demonstrate the feasibility of the FILOX process in CMOS compatible vertical MOS devices. Table 6.1 lists the process steps used to fabricate the vertical n-channel MOSFETs.

The initial wafers were p-type <100> with a resistivity of 10-33Ωcm. The fabrication process started with a $5\times10^{14}cm^{-2}$ boron substrate implant at 50keV which was annealed at 1000°C in a dry and wet ambient for 10 and 30 minutes, respectively. A 1.1μm lightfield photoresist layer (SPRT 510) was spun onto the wafer to protect future pillar areas. After the lithography stage (PL) the wafers were hardbaked for two hours at 140°C. The pillars were anisotropically etched using a HBr etch. The photoresist was removed using a plasma asher. Table 6.1 illustrates the batch splits used to achieve different pillar heights (stage 2). In the following process steps a 20nm pad oxide layer was grown at 900°C and a 130nm thick nitride layer deposited. The active area (AA) was defined using a lithography process. The 600nm thick LOCOS oxide was grown at a temperature of 1000°C in a hydrogen/oxygen ambient.

In order to leave nitride fillets on all pillar sidewalls as shown in figure 4.2a, the nitride and the pad oxide was anisotropically etched to leave a structure as illus-

trated in figure 4.2b. The FILOX local oxidation was performed at a temperature of 1000°C in a hydrogen/oxygen ambient allowing the oxide to become viscous [79, 81]. Figure 4.2c illustrates the structure after the 60nm FILOX oxidation.

To contact the substrate a lithography dark field process step was performed (PP). Two p^+ boron implants were performed with a dose of $1\times10^{15}cm^{-2}$ each, at 47keV and 25keV for devices with and without FILOX, respectively.

The source/drain implants for devices based on the GAI process sequence were performed in the following process step (stage 8). Since the minimum implantation angle of the ion implanter is 7°, two implants were used (in east and west direction) for both, control and FILOX devices. Figure 6.3 illustrates the implantation process sequence for FILOX devices. The first implant (west) leaves a non implanted area at the bottom of the pillar. This is because of the shadowing caused by the pillar due to the angled implant as depicted in figure 6.3a. The second implant (east) allows the previously non implanted area to be implanted as illustrated in figure 6.3b so that both sides of the pillar are symmetrical.

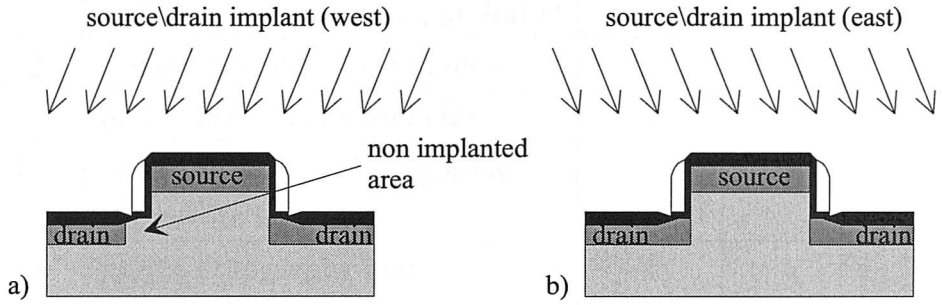


Figure 6.3: Source/drain implant steps. a) First implant (direction west) leaves a non implanted area at the bottom left hand side of the pillar. b) The second implant (direction east) implants the previously not implanted area.

In the following stage (9) the nitride fillets are removed in orthophosphoric acid at 160°C. The 20nm thick pad oxide was removed to expose the silicon sidewalls of the pillar using a 20:1 HF dip etch solution for 40 seconds. After a RCA clean the pillar sidewalls were dry oxidised at 800°C to create a gate oxide. Three different gate oxide thicknesses as shown in table 6.1 were used.

A 200nm thick in-situ phosphorous doped polySi layer with a concentration of $5\times10^{19}cm^{-3}$ was chosen to form a uniformly doped gate. After an anisotropic polySi etch, polySi fillets surrounding all vertical surfaces are left as illustrated in figure 6.2a. A further source/drain lithography step for devices based on the GBI process was performed. The arsenic implant concentration, again in both directions (east and west), was

stage	description	control	FILOX	mask
1	boron substrate implant and drive in at 1000°C	x	x	-
2	pillar lithography and etch (250/300/350nm into Si)	x	x	PL
3	standard LOCOS (600nm) (20nm pad oxide, 130nm nitride)	x	x	AA
4	dry etch Si_3N_4 to leave fillets	x	x	-
5	dry etch 20nm pad oxide	x	x	-
6	60nm FILOX at 1000°C	-	x	-
7	p^+ substrate contact lithography and boron implant	x	x	PP
8	source/drain GAI lithography and n^+ As implant	x	x	GAI
9	strip nitride spacers	x	x	-
10	wet etch 20nm pad oxide	x	x	-
11	3/6/9nm gate oxidation at 800°C	x	x	-
12	200nm in-situ P doped polySi	x	x	-
13	polySi lithography and etch	x	x	P1
14	source/drain GBI lithography and n^+ As implant	x	x	GBI
15	polySi lithography and fillet removal etch	x	x	PR
16	SILOX and BPSG deposition	x	x	-
17	RTA for 10sec at 1100°C	x	x	-
18	contact window lithography and etch	x	x	CW
19	metal deposition	x	x	-
20	metal lithography and etch	x	x	M1

Table 6.1: Process list and batch splits for vertical MOSFETs with and without incorporated FILOX. Also shown are the mask indices.

$2\times$ $3\times10^{15}cm^{-2}$. The implant energy for the control devices was 50keV and for the FILOX devices 90keV. Figure 6.2a illustrates the device after stage 14 and shows the pillar surrounded by a polySi fillet. In order to fabricate single and double gate devices on the same wafer, a polysilicon removal mask (PR) was used to mask parts

of the polySi as shown in figure 6.2b. Following the polySi removal mask lithography and isotropic silicon etch using SF_6, the polySi fillets are partially removed as depicted in figure 6.2c.

The backend process include the deposition of 100nm undoped silicon dioxide (SILOX) followed by a boron phosphorous silicate glass (BPSG) deposition. After the deposition, a rapid thermal anneal (RTA) for 10 seconds at 1100°C was performed to activate the dopants. To contact the devices, contact windows were etched into the BPSG/SILOX layer (CW). A 2.2μm thick photoresist layer was used to protect the glass layer. In the following process step a 1μm thick Ti-Al/Si layer was deposited. A metal mask lithography step (M1) was used to define the probe pads and the metal tracks. A detailed process listing can be found in appendix C.3.

6.4 Mask layout

The vertical MOS transistor batch was designed using 9 masks as shown in table 6.1. The minimum feature size of the stepper used is 1.5μm and the alignment tolerance $\pm$1.0μm. Three different sizes were designed with minimum line widths of 1.5, 2 and 4μm. Figure 6.4 illustrates a layout of a vertical surround gate MOSFET based on 2μm design rules. The minimum gate track width is 2μm and the alignment tolerance is also 2μm.

Figure 6.5 depicts the alignment sequence of the vertical MOSFET batch. Apart from the backend process, all masks are aligned to the pillar mask PL to assure minimum misalignment. The metal mask M1 is aligned to the contact window mask CW.

In addition to the layout shown in figure 6.4, devices with single and double gates as well as devices with different channel widths were designed. Furthermore, the mask contains several NAND and NOR gates as well as inverter and ring oscillators and devices for RF measurements. Several test structures, for example van der Pauw structures to extract the sheet resistance were included as well as diodes, capacitors and polySi fillet based resistors. Since cross-sectioning of a MOS device is difficult, transmission electron microscope (TEM) bars were designed which are also very useful for scanning electron microscopy cross-sections (SEM). To extract the doping profiles secondary ion mass spectrometry (SIMS) structures were added. A detailed description of the mask layout can be found in appendix B.2.

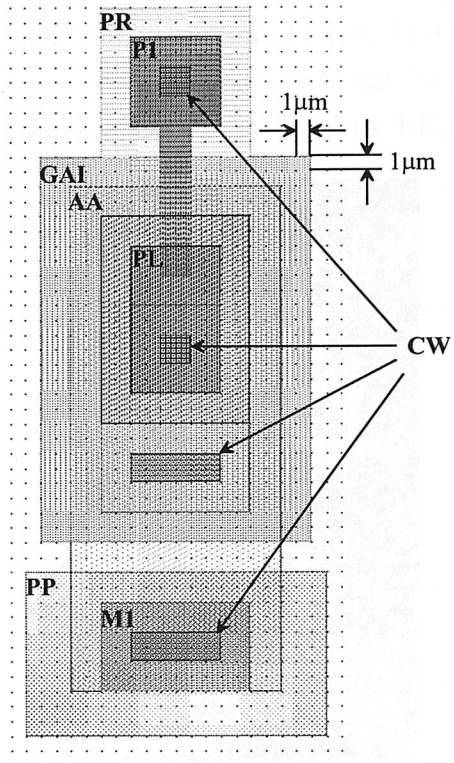


Figure 6.4: Vertical surround gate MOSFET layout based on 2μm design rules.

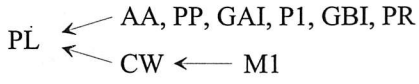


Figure 6.5: Mask alignment sequence

6.5 Results on GAI devices

In this section measurements of fabricated n-MOSFETs and logic gates fabricated using the GAI process are presented. Figure 6.6 shows a photograph of a fabricated MOSFET based on 2μm design rules. The gate overlaps the top of the pillar to ensure a connection to the polysilicon surround gate. The source contact is on top of the pillar, whilst the drain and substrate contacts are located at the bottom of the pillar. The pillar top and trench areas are covered by FILOX oxide.

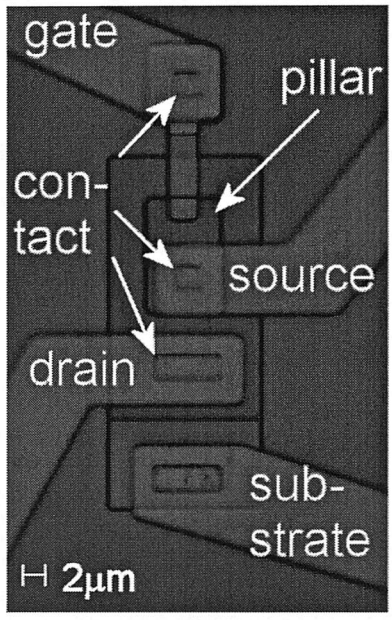


Figure 6.6: Top-view of a fabricated MOSFET with surround gate based on 2μm design rules.

Table 6.2 presents extracted sheet resistance values obtained from van der Pauw measurements [82] and the calculated average doping concentrations [66]. The measured values of resistance and the extracted acceptor doping concentration of the substrate on top off the pillar and at the bottom indicate that the channel doping is graded. This was expected as the wafer was boron implanted as the first process step to increase the initial doping concentration of the wafer (see table 6.1 stage 1). The source/drain sheet resistances on top and bottom of the pillar are identical. The dopant concentration in the polySi gate layer for the GAI device is due to the in-situ doping since the polySi layer was deposited after the source/drain implant.

6.5.1 SEM cross-sections

Figure 6.7 depicts a FESEM cross-section of a fabricated single gate GAI structure with a measured gate oxide thickness of 3.0nm on a planar surface. In order to in-

area	R[Ω/□]	D[cm^{-2}]	N[cm^{-3}]
p substrate on pillar top	128.91	5.39×10^{14}	5.39×10^{18}
p substrate on pillar bottom	168.30	3.55×10^{14}	3.55×10^{18}
n^+ source/drain on pillar top	48.96	2.84×10^{15}	1.42×10^{20}
n^+ source/drain on pillar bottom	48.57	2.86×10^{15}	1.43×10^{20}
n^+ gate polySi	58.29	-	5.23×10^{19}

Table 6.2: Sheet resistances R, implant dose D and doping concentrations N of the fabricated vertical GAI MOSFETs. The doping concentration was extracted assuming a junction depth of 1μm for the substrate and 115nm for the source/drain junctions.

crease visibility of the junction, the junctions were etched back using a 20:1 HF etch for 40 seconds followed by an 1:400 HF/HNO_3 etch for 15 seconds [69]. The junction depth was extracted to be 115nm for both, source and drain and the polySi fillet thickness to be 230nm. The polySi fillet was overetched by about 45nm at the top of the pillar. Figure 6.7 also shows that the drain junction reaches underneath the polySi fillet so that the channel is formed on the vertical surface of the pillar. The extracted channel length was 105nm.

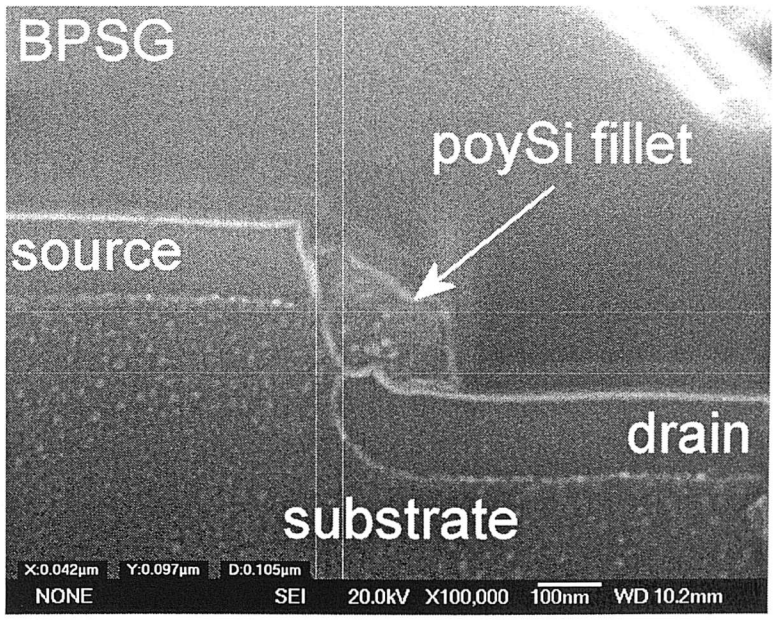


Figure 6.7: FESEM cross-section of a GAI vertical n-MOSFET single gate structure with 3nm oxide thickness showing the source and drain junctions.

Figure 6.8 depicts the encroachment caused by the FILOX oxidation at the top and bottom of the pillar. Bird's beaks can be seen at the top and bottom of the pillar that have the advantage of reducing the gate/drain and gate/source overlap capacitance. The encroachment of the bird's beak on the top of the pillar is 26nm at a distance of

about 45nm from the pillar top. At the pillar bottom the encroachment is 30nm at a distance of 200nm from the pillar edge.

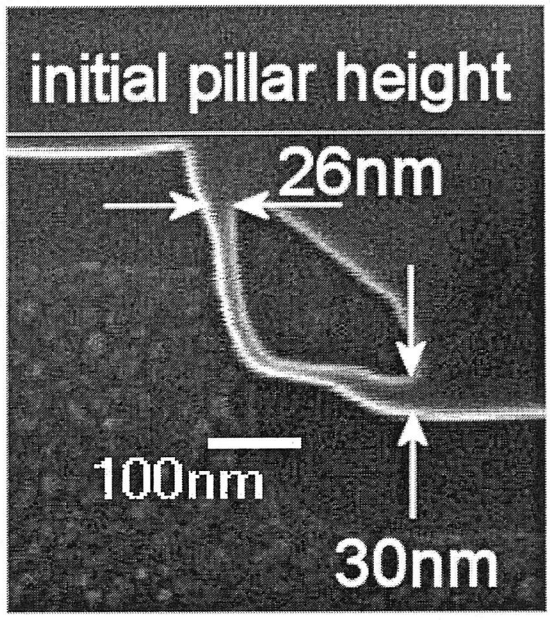
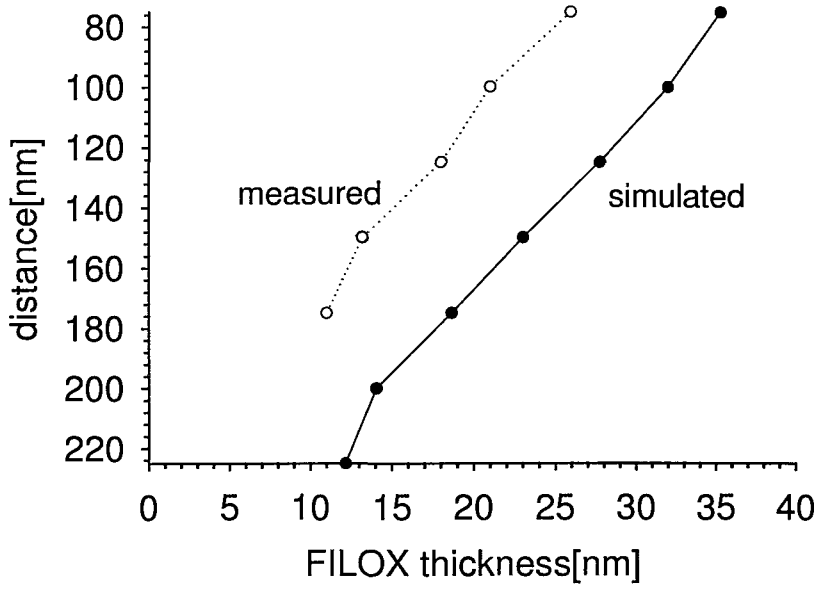


Figure 6.8: FESEM cross-section of a GAI vertical n-MOSFET single gate structure with 6nm oxide thickness showing the source and drain junctions.

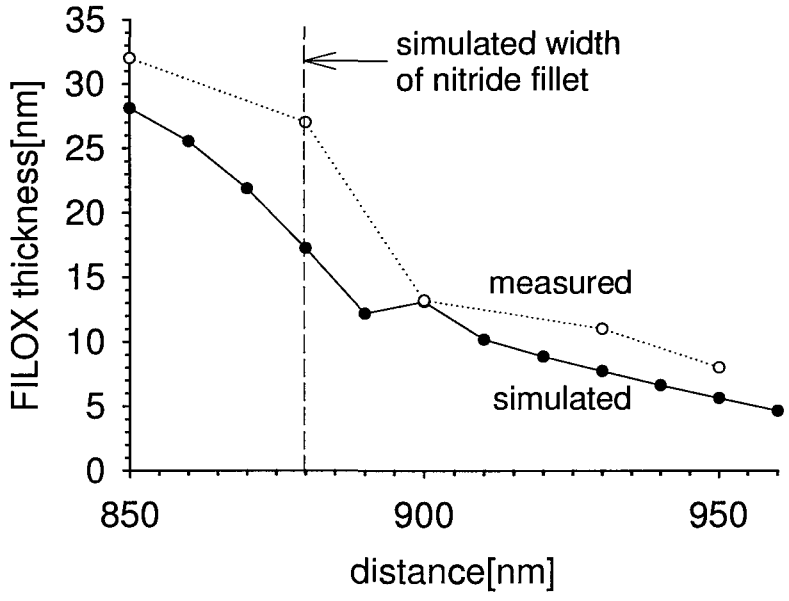
Figure 6.9 illustrates measured and simulated data of the encroachments on top and bottom of the pillar and the measured values extracted from figure 6.8. To obtain the simulated encroachment the simulation results in figure 4.9 were used together with a nitride strip and a 20nm wet etch to remove 20nm pad oxide (see appendix A.7).

Figure 6.9a shows that the simulated encroachment on top of the pillar is a little larger than the measured value. However, figure 6.9b shows that the simulated encroachment at the bottom of the pillar is very similar to the measured value. There are three contributions to the encroachment seen in figure 6.9. The first arises from the fact that the nitride spacer used in the FILOX process is thinner than the polysilicon gate. This causes the FILOX layer to extend underneath the polysilicon gate at the bottom of the pillar. The second arises from the overetch of the nitride spacer used in the FILOX process. This causes the FILOX oxide to extend down the side of the pillar at the top of the pillar. The third arises from the bird's beak that is generated during local oxidation. It should be noted that these effects are beneficial to the transistor performance because they reduce gate/source and gate/drain overlap capacitance.

Figure 6.10 shows a FESEM cross-section of two GAI vertical MOS structures with a 6nm gate oxide. Bird's beaks due to the FILOX oxidation can be seen at the top



a)



b)

Figure 6.9: Measured and simulated FILOX thickness as a function of distance for a simulated 20.4nm pad oxide grown at 1000°C and 130nm nitride thickness a) at the pillar top and b) at the pillar bottom. The distance scale is obtained from the distance scale in figure 4.6.

and bottom of the pillar. The bird's beaks do not reach into the vertical channel area of the MOSFET so the transistor operation is not degraded.

Table 6.3 presents the extracted encroachments at the top and bottom of the pillar for the structures shown in figure 6.10. The values of encroachment at the top and bottom of the pillar indicate that the measured bird's beak is shorter.

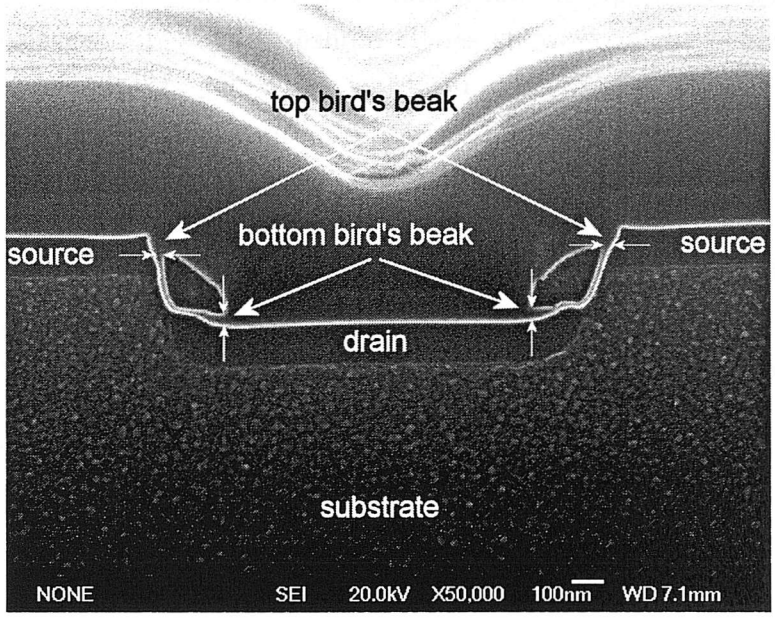


Figure 6.10: FESEM cross-section of two GAI vertical n-MOSFET structures with 6nm oxide thickness.

location	left structure	right structure	simulated
top[nm]	26	22	35
bottom[nm]	30	37	40

Table 6.3: Top and bottom encroachment of the two MOS structures shown in figure 6.10 versus the simulated results based on figure 6.8b and 6.8c.

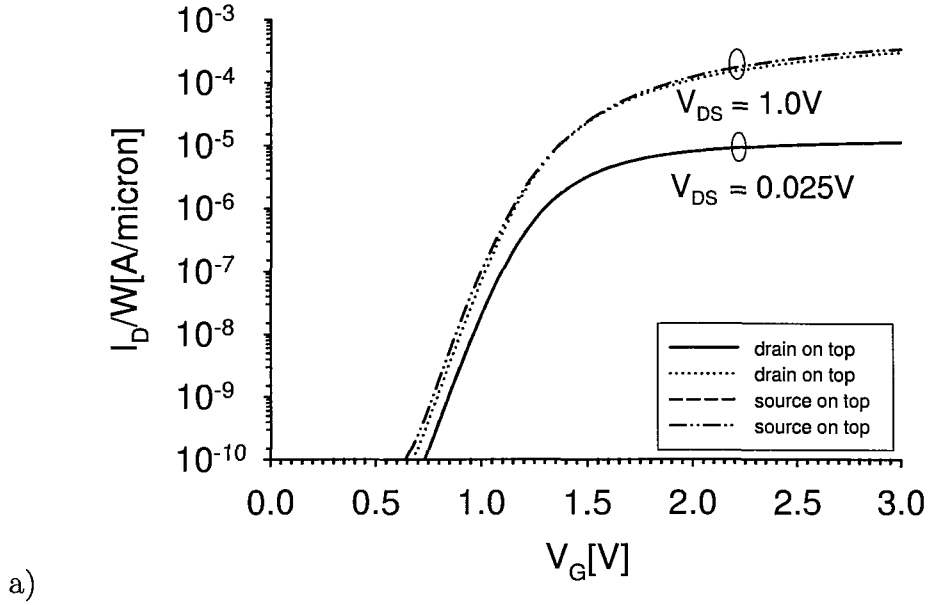
6.5.2 Single gate transistors

In this section electrical parameters of a typical single gate transistor will be presented. Figure 6.11a illustrates the subthreshold characteristics for single gate vertical MOSFETs with source on top (SOT) and drain on top (DOT) for two different source/drain voltages. The subthreshold slopes show excellent behaviour down to a drain current of 10^{-10}A. For a source/drain voltage of 0.025V both, SOT and DOT plots are identical. The threshold voltage was extracted by extrapolating linearly plotted $I_D(V_G)$ to zero as described in [83] and is in both directions of operation (SOT, DOT) 1.25V. The subthreshold slope was extracted at a drain current of 10^{-10}A to be 111mV/dec. This is similar to the results reported by Schulz et al. [46] of 102mV/dec for an ion implanted vertical surround gate device with a channel length of 100nm and a gate oxide thickness of 3nm in SOT configuration as shown in table 6.4. The results presented in figure 6.11a show values of DIBL of 55mV and 75mV in DOT and SOT, respectively. These values compare with a value of 70mV for the device reported in [46]. The on-current (V_{DS}=1.0V) is a factor of 1.13 higher for the SOT transistor than the DOT transistor. The extracted transconductance in the SOT configuration is also higher compared with the DOT configuration. Table 6.4 presents the extracted parameters for a single gate device.

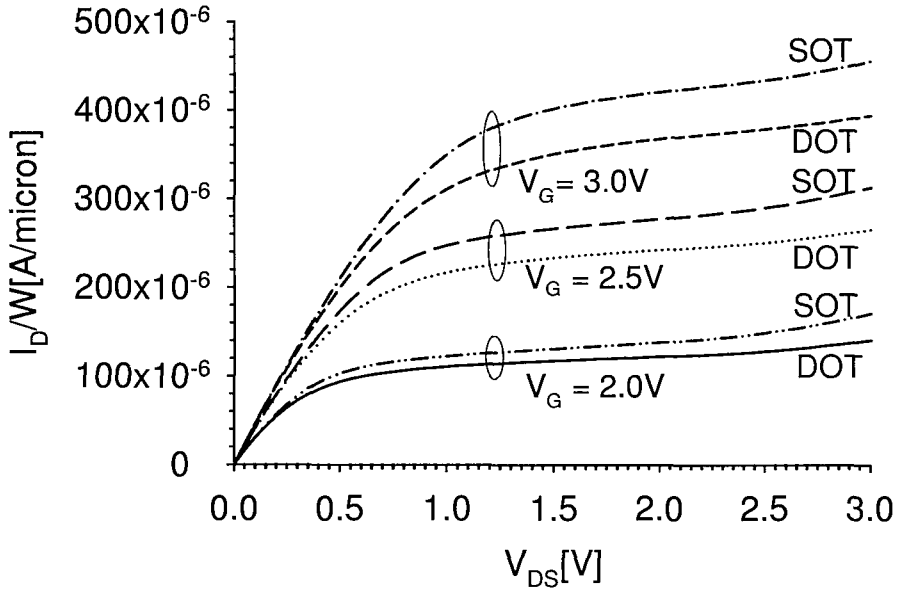
parameter	**SOT**	**DOT**	**Schulz et al. [46]**
$\mathbf{V_T(V_{DS}=0.025V)[V]}$	1.25	1.25	0.6
$\mathbf{S(I_D = 10^{-10}A)[mV/dec]}$	111	111	102
$\mathbf{DIBL(I_D = 10^{-9}A)[mV]}$	75	55	70
$\mathbf{g_m(V_{DS}=1V)[S/m]}$	261	219	-

Table 6.4: Measured and extracted electrical parameter for a GAI single gate vertical MOSFET. Source on top (SOT) and drain on top (DOT) configurations are presented.

Figure 6.11b illustrates output characteristics of a typical single gate device for three different gate voltages. Higher drain currents can be seen for measurements with the SOT configuration compared with the DOT configuration. At a source/drain and gate voltage of 3.0V a factor of 1.16 can be extracted. This result may be due to a difference in channel length in the DOT and SOT configurations because of the graded substrate doping. This would give a wider depletion region in the SOT configuration and hence a shorter channel length. Both, the increased I_{on} and the increased output conductance for the SOT configuration tend to point to this explanation. The higher DIBL for the SOT configuration could also be explained in this way. Detailed device simulations are needed to confirm this hypotheses.



a)



b)

Figure 6.11: Typical electrical characteristics of a single gate GAI vertical n-MOSFET based on 1.5μm design rules with source on top (SOT) and drain on top (DOT). a) Subthreshold characteristics for V_{DS}=0.025 and 1.0V. b) Output characteristics. The channel length was 105nm and the channel width 4.5μm.

6.5.3 Surround gate transistors

Figure 6.12 illustrates the measured subthreshold and output characteristics of a surround gate transistor. For a source/drain voltage of 0.025V both, SOT and DOT subthreshold plots are identical. However, for a source/drain voltage of 1.0V the SOT configuration gives a higher DIBL of 95mV compared with 55mV for DOT. Compared with the single gate device the surround gate device shows a slightly higher threshold voltage of 1.35V for both, SOT and DOT configurations. The subthreshold slope of

the surround gate MOSFET is slightly higher than that of the single gate MOSFET. The extracted on-current at V_{DS}=1.0V is a factor of 1.12 higher for the SOT transistor than the DOT transistor. The transconductance in the SOT configuration is also higher compared with the DOT configuration but less compared with the single gate device. Table 6.5 presents the extracted parameters for a surround gate transistor.

parameter	**SOT**	**DOT**	**Schulz et al. [46]**
$\mathbf{V_T(V_{DS}=0.025V)[V]}$	1.35	1.35	0.6
$\mathbf{S(I_D = 10^{-10}A)[mV/dec]}$	123	123	102
$\mathbf{DIBL(I_D = 10^{-9}A)[mV]}$	95	55	70
$\mathbf{g_m(V_{DS}=1V)[S/m]}$	127	109	-

Table 6.5: Measured and extracted electrical parameter for a GAI surround gate vertical MOSFET. Source on top (SOT) and drain on top (DOT) configurations are presented.

Figure 6.12b shows output characteristics of the surround gate device. Comparing the output characteristic of a surround gate device shown in figure 6.12b with that of a single gate transistor shown in figure 6.11b shows that a higher current drive per unit gate width is obtained for the single gate transistor. This could be caused by the lower threshold voltage of the single gate device. A possible explanation for the higher V_T in the surround gate transistor could be a thickening of the gate oxide. This would also explain the higher subthreshold slope and DIBL in the surround gate transistor.

6.5.4 Reproducibility of single and surround gate MOS transistors

Figure 6.13 shows subthreshold characteristics of six single and surround gate devices taken at V_{DS}=0.1V. The measurements were taken from three adjacent chips and show the spread of the subthreshold characteristics. The threshold voltage for single gate transistors varies from 1.25 to 1.4V and for surround gate transistors from 1.075 to 1.3V. Whilst the threshold voltage for single gate devices varies by about 0.15V, for surround gate devices the variation is 0.225V and therefore significantly bigger.

6.5.5 Process/device simulations of a single gate transistors

In this section a comparison between a simulated and a measured single gate MOSFET is presented. All data presented is for the drain on top (DOT) configuration.

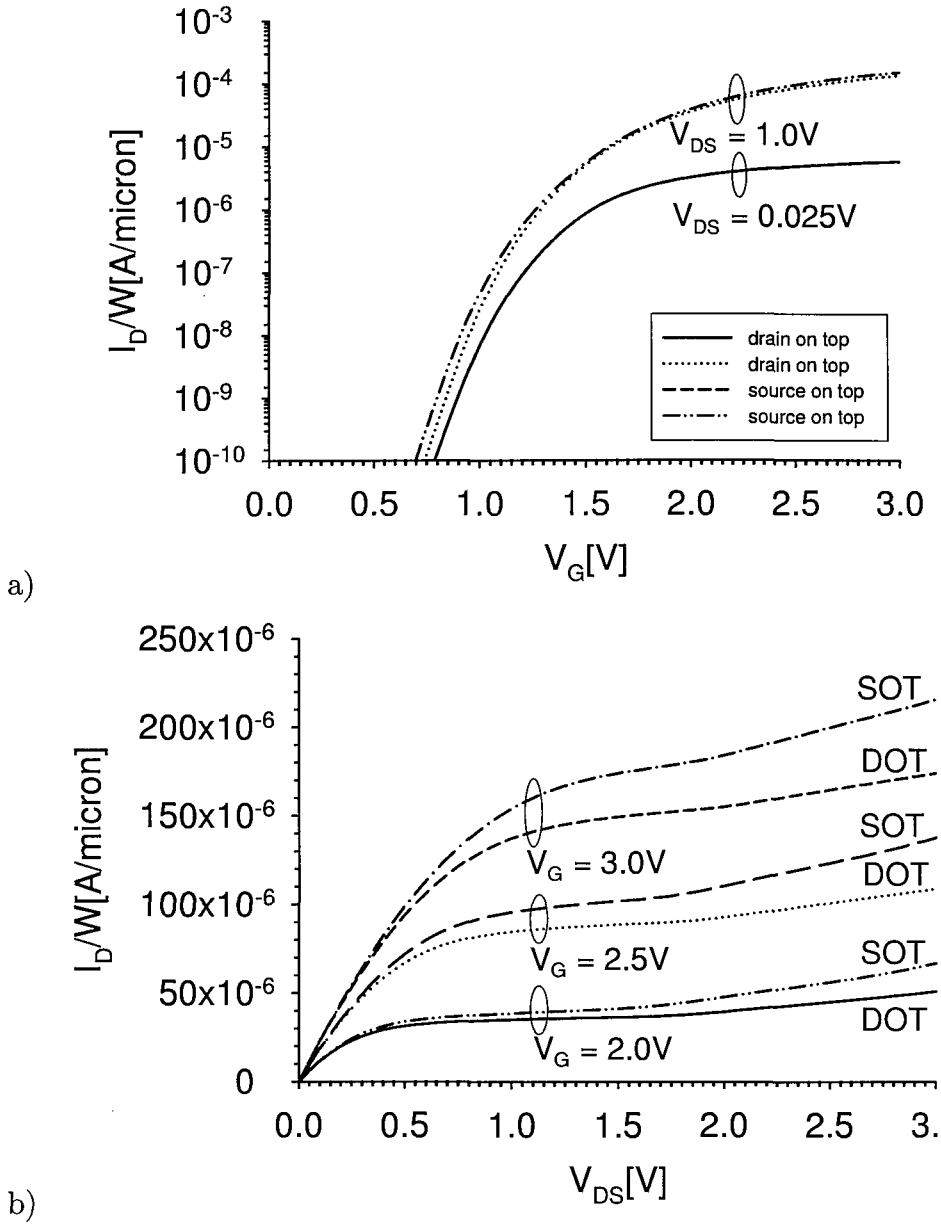


Figure 6.12: Typical electrical characteristics of a surround gate GAI vertical n-MOSFET based on 1.5μm design rules with source on top (SOT) and drain on top (DOT). a) Subthreshold characteristics for V_{DS}=0.025 and 1.0V. b) Output characteristics. The channel length was 105nm and the channel width 24μm.

Calibration of the simulator

To optimise the accuracy of the simulations two process parameters were modified. Initial simulations showed that the diffusion of the source junction in the x-direction was less than that shown in figure 6.7 so that the junction did not reach the edge of the pillar. However, a reduction of the nitride spacer thickness from 130 to 70nm allowed the source at the bottom of the pillar to reach the edge of the pillar as illustrated in figure 6.14. Furthermore, the gate oxide thickness was reduced from 3.3 to 2.9nm

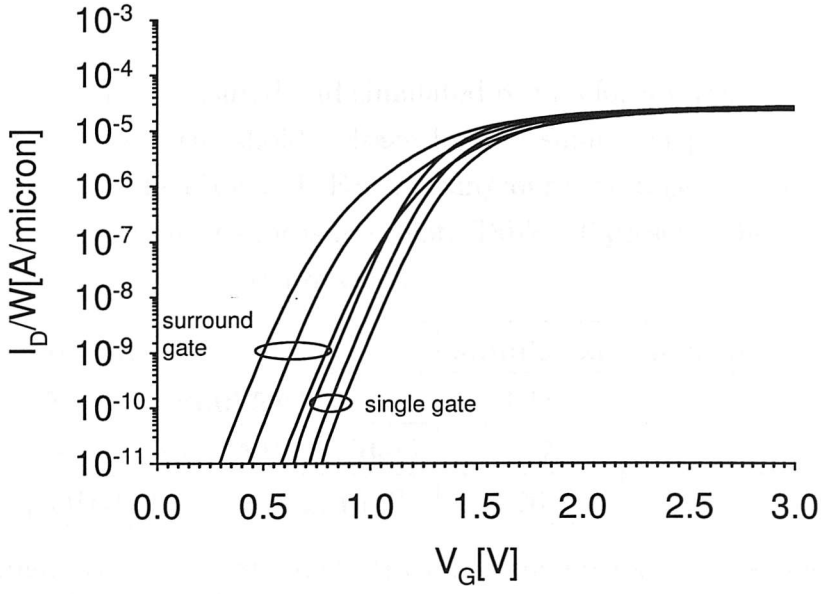


Figure 6.13: Variation of subthreshold characteristics of single and surround gate GAI vertical n-MOSFETs based on 1.5μm design rules for V_{DS}=0.1V and a channel length of 105nm. The channel width of the single gate transistor was 4.5μm and that of the surround gate transistor 24μm. All devices were measured with drain on top (DOT).

at the side of the pillar to give the correct threshold voltage. The simulation file is listed in appendix A.8.

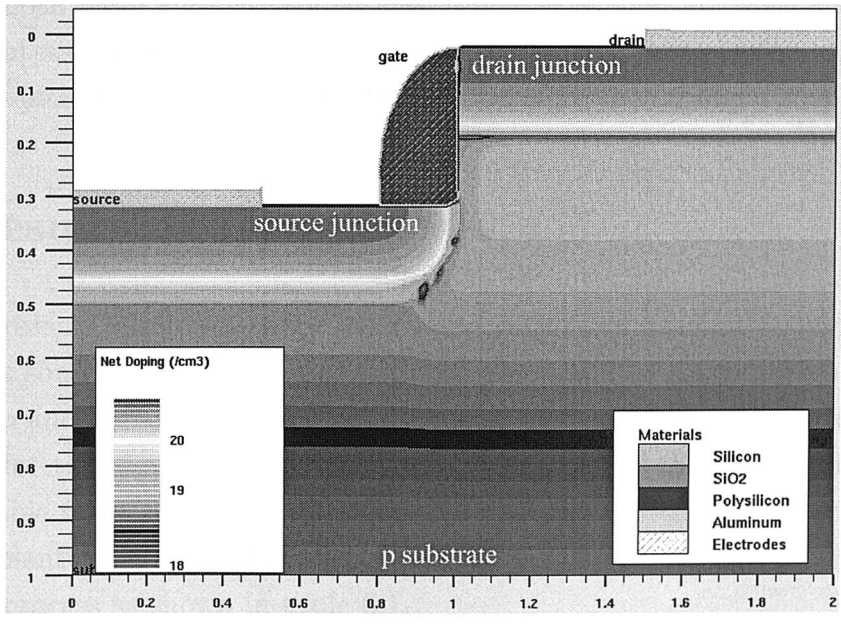


Figure 6.14: Simulated structure of a single gate GAI vertical n-MOSFET with drain on top (DOT). The channel length was 105nm and the extracted junction depth 169nm and 164nm at the pillar top and bottom, respectively.

Results

Figure 6.15a compares measured and simulated results for a vertical single gate transistor. A slightly lower threshold voltage for the simulated plot at a drain/source voltage of 0.025V can be observed. For a drain/source voltage of 0.1V the simulated plot shows less DIBL than the measured plot. Table 6.6 presents the extracted values for both simulated and measured devices.

parameter	simulated	measured
$\mathbf{V_T(V_{DS}=0.025V)[V]}$	1.18	1.25
$\mathbf{S(I_D = 10^{-10}A)[mV/dec]}$	117	111
$\mathbf{DIBL(I_D = 10^{-9}A)[mV]}$	26	55

Table 6.6: Simulated and measured electrical parameters for a GAI single gate vertical MOSFET in drain on top (DOT) configuration.

Figure 6.15b compares simulated and measured output characteristics. For a gate voltage of 2.0V the measured plot shows increased current drive at V_{DS}=3.0V of a factor of 1.5 compared with the measured. Similar behaviour can be observed for a gate voltage of 2.5V where the measured current is higher by a factor of 1.4. However, at V_G=3V both plots are nearly identical. The discrepancy between simulated and measured output characteristics could be caused by a higher channel doping in the simulation which decreases the mobility and therefore the current drive.

6.6 Results on GBI devices

Table 6.7 presents sheet resistance values and estimated average doping concentrations for the source and drain regions of GBI devices. The source/drain sheet resistance on top and bottom of the pillar are nearly identical. All other extracted sheet resistances for this device type are the same as those for the GAI devices and are shown in table 6.2. The sheet resistances of the two devices are different because the two implant steps for GBI and GAI where performed at different stages of the fabrication process as shown in table 6.1.

Figure 6.16 depicts a FESEM cross-section of the fabricated GBI structure with a gate oxide thickness of 3nm. The junction depth was extracted to be 140nm for both, source and drain. The channel length was extracted to be 240nm. Figure 6.16 shows that the drain junction reaches underneath the polySi fillet but does not reach to the edge of the pillar. This can be explained as follows. For GAI devices the implant is

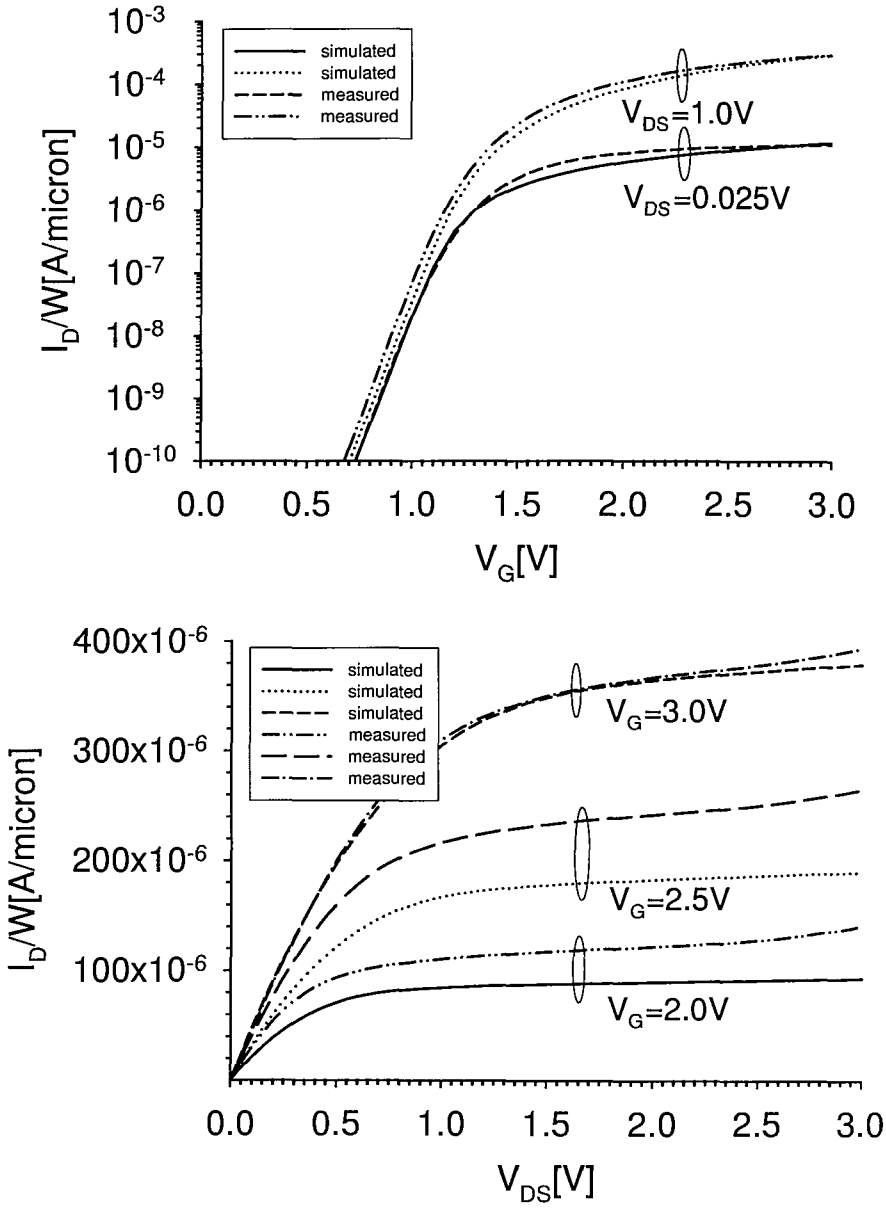


Figure 6.15: Simulated and measured electrical characteristics of a single gate GAI vertical n-MOSFET based on 1.5μm design rules with drain on top (DOT). a) Subthreshold characteristics for V_{DS}=0.025 and 1.0V. b) Output characteristics. The channel length was 105nm.

area	R[Ω/□]	D[cm^{-2}]	N[cm^{-3}]
n$^+$ source/drain on pillar top	41.73	2.72×10^{15}	1.36×10^{20}
n$^+$ source/drain on pillar bottom	41.59	2.72×10^{15}	1.36×10^{20}

Table 6.7: Sheet resistances R, implant dose D and doping concentrations N of the fabricated vertical GBI MOSFETs. The doping concentration was extracted assuming a junction depth of 140nm for the source/drain junctions.

performed after the pillar sidewall is protected by the nitride fillets with a thickness of 130nm (see table 6.1 stage 8). For GBI devices the implant is performed after the polySi deposition with the polySi fillets in place with a thickness of 200nm (stage 14). The lateral penetration of the source/drain implant would therefore be expected to be 70nm less in the GBI devices. The channel length is formed partly on the pillar sidewall and partly at the bottom of the pillar. This is clearly undesirable as the gate oxides on vertical and horizontal surfaces will be different. Figure 6.16 shows that the gate oxide at the edge of the drain is ~17nm thick, due to the encroachment of the bird's beak into the channel.

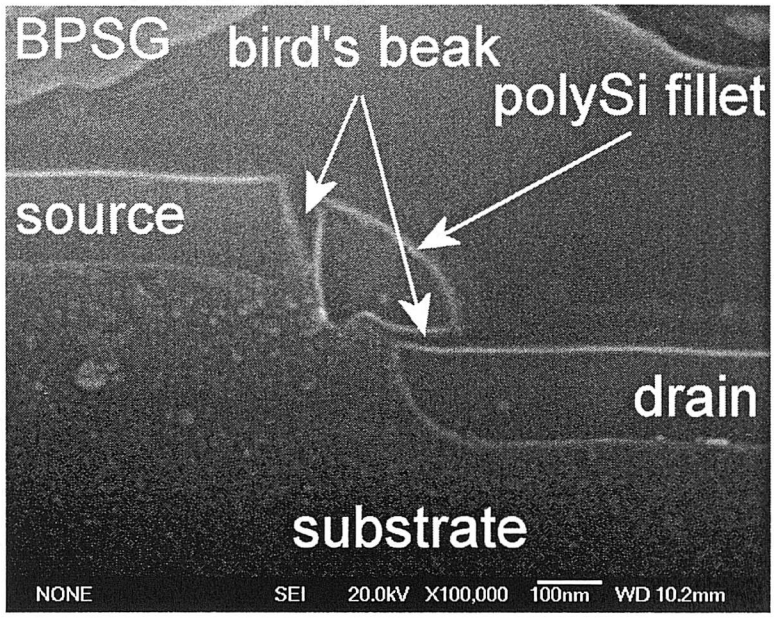


Figure 6.16: FESEM cross-section of a GBI vertical n-MOSFET structure with 3nm oxide thickness showing the source and drain junctions and the bird's beak on top and bottom of the pillar caused by the FILOX oxidation.

Figure 6.17 depicts the subthreshold characteristic of a surround gate GBI device. For a drain/source voltage of 0.025V identical plots are observed for both SOT and DOT configurations. The subthreshold characteristics show a dramatic shift in threshold voltage from 1.35 to 2.7V compared with the GAI devices. A possible explanation for this result could be a thicker oxide on the horizontal surface adjacent to the drain. A first order calculation, assuming a substrate doping concentration of $4.5\times10^{18}cm^{-3}$ gives a threshold voltage of 2.7V for a gate oxide thickness of 7.8nm compared with a threshold voltage of 1.3V for an oxide thickness of 3.9nm. While the calculated value of V_T does not exactly agree with the measured value, the trend is in the right direction. It can therefore be concluded that for the GBI device the V_T shift is due to the bird's beak encroachment into the channel. Table 6.8 summarises the measured parameter values.

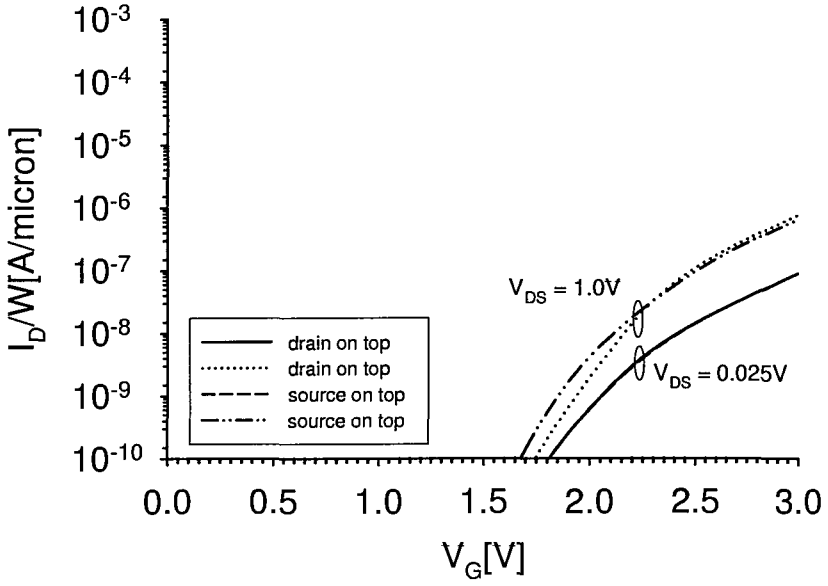


Figure 6.17: Subthreshold characteristics of a surround gate GBI vertical n-MOSFET based on 1.5μm design rules for V_{DS}=0.025 and 1.0V with a channel length of 175nm and a width of 24μm. Source on top (SOT) and drain on top (DOT) configurations are presented.

parameter	SOT	DOT	Schulz et al. [46]
$\mathbf{V_T(V_{DS}=0.025V)[V]}$	2.7	2.7	0.6
$\mathbf{S(I_D = 10^{-10}A)[mV/dec]}$	171	170	102
$\mathbf{DIBL(I_D = 10^{-9}A)[mV]}$	210	120	70

Table 6.8: Measured electrical parameters for a GBI surround gate vertical MOSFET. Source on top (SOT) and drain on top (DOT) configurations are presented.

6.7 Logic gates

In this section novel logic gates based on GAI vertical MOSFETs are introduced. A vertical NOR gate as well as a two pillar vertical NAND gate are presented.

6.7.1 Concept of a vertical NOR gate

Figure 6.18 illustrates a cross-section of a proposed vertical NOR gate. The basic concept behind the device shown is that it consists of two independent single gate transistors on two sides of the pillar. In order to divide the initial surround gate, parts of the left and right side of pillar need to be masked using the polysilicon removal mask (PR) as discussed in section 6.2.

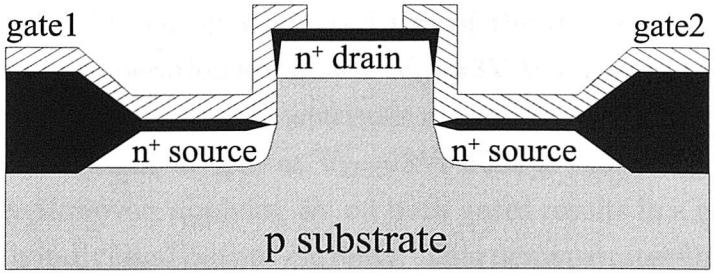


Figure 6.18: Cross-section of a vertical NOR gate.

6.7.2 Results

Figure 6.19 shows a photograph of the device under consideration. The device is fully symmetrical with a gate on each side of the pillar. The source is located on the bottom and the drain on the top of the pillar. It is also possible to swap source and drain. The following measurements were taken in the DOT configuration.

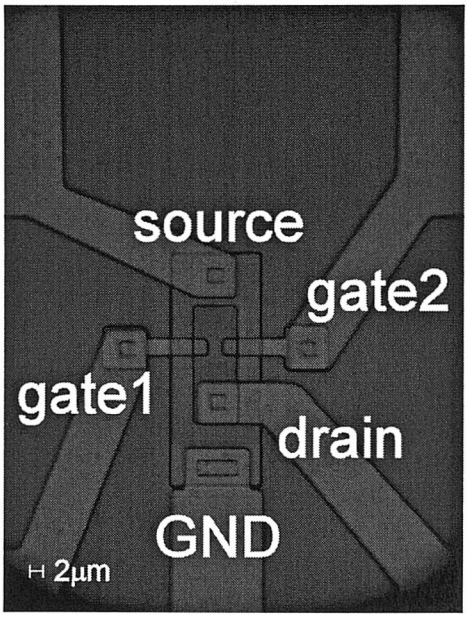
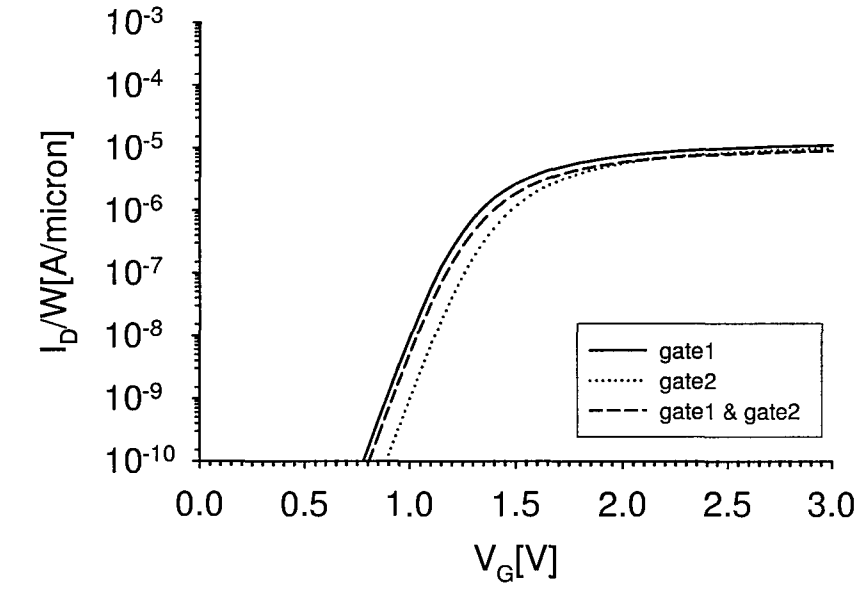


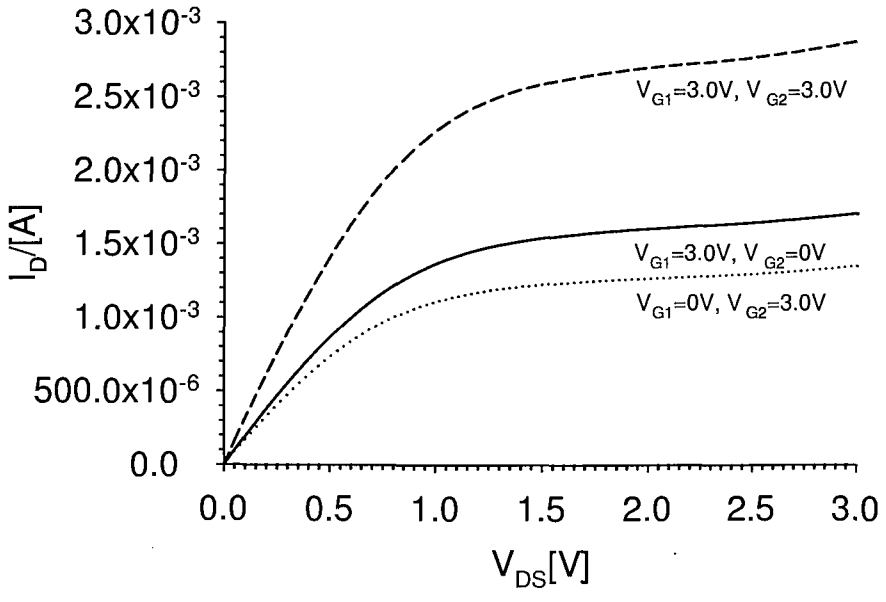
Figure 6.19: Top-view of a fabricated vertical NOR gate based on 2.0μm design rules and a channel width of 4.5μm per gate.

Figure 6.20a depicts the subthreshold characteristics for three configurations of the device: V_{gate1}=input & V_{gate2}=0V, V_{gate1}=0V & V_{gate2}=input and V_{gate1}=V_{gate2}=input. The threshold voltage of the transistor at the left side (gate1) of the pillar was extracted to be 1.24V, while the threshold voltage of the transistor on the right side was extracted to 1.38V. Connecting both gates together resulted in a threshold voltage of 1.3V. This difference suggests different gate oxide thicknesses on the two sides of the pillar. First order calculation suggest a variation in oxide thickness of 0.4nm.

Figure 6.20b depicts the output characteristics of the device shown in figure 6.19. Three configurations of operation are shown: V_{G1}=3V & V_{G2}=0V, V_{G1}=0V & V_{G2}=3V and V_{G1}=V_{G2}=3V. The output characteristics of the two transistors show differences in current drive by a factor of 1.26 at V_{DS}=3V. This is caused by the difference in threshold voltage. However, applying 3V on both gates results in a current consisting of the sum of both individual output currents. This demonstrates that the NOR gate is working correctly.



a)



b)

Figure 6.20: Typical electrical characteristics of a vertical NOR gate based on 1.5μm design rules with drain on top (DOT). The channel length was 105nm and the channel width was 4.5μm for each gate. a) Subthreshold characteristics for V_{DS}=0.025V b) Output characteristics.

Figure 6.21 depicts the transfer characteristics of the NOR gate. To obtain the transfer characteristics of the device, a 55kl resistor was connected in series with the drain. Up to a gate voltage of 1.0V the measured output voltage of the NOR gate is about 2.85V. The voltage drop of 0.15V is partially caused by the transistor and by the input resistance of the measurement setup and was extracted to 1MΩ. For voltages greater about 1.7V the output voltage is pulled down to ground. The input voltage at which this occurs varies for the three different configurations due to the difference in threshold voltage. The logic low voltages are 0.027, 0.003 and 0.017 for V_{G1}=3V & V_{G2}=0V, V_{G1}=0V & V_{G2}=3V and V_{G1}=V_{G2}=3V, respectively.

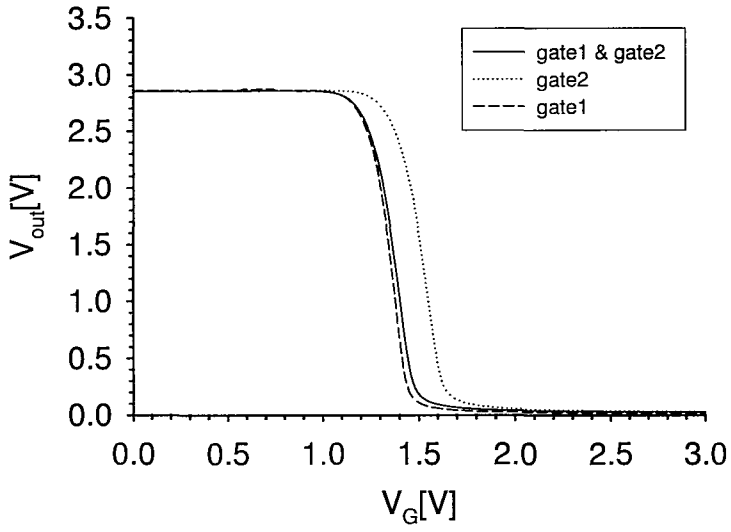


Figure 6.21: Transfer characteristics of a typical vertical NOR gate based on 1.5μm design rules (see figure 6.19). The channel width was 4.5μm for each gate. A 55kl resistor was connected to V^+ in series with the drain.

6.7.3 Concept of a NAND gate based on two pillars

Figure 6.22a illustrates a cross-section of a two pillar vertical NAND gate. The device shown consists of two vertical surround gate transistors (T1, T2), one on each pillar. The transistors are joined together by the implanted area at the bottom of the pillar. This area functions as the drain for transistor 1 and the source of transistor 2. The two surround gates are contacted by gate tracks to the left and right of the pillar. Figure 6.22b illustrates a circuit diagram of the NAND gate.

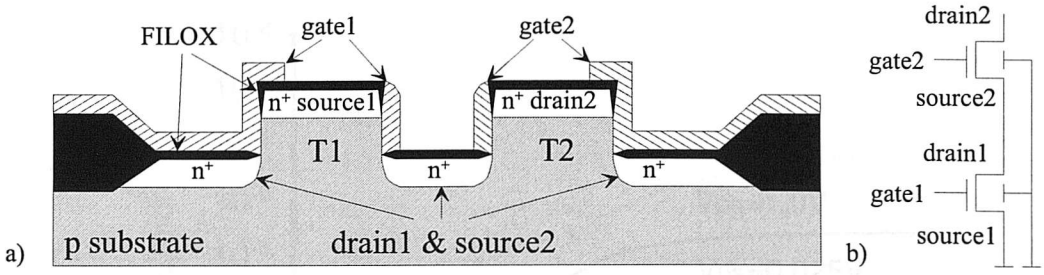


Figure 6.22: a) Cross-section of a vertical NAND gate based on two pillars b) circuit diagram.

6.7.4 Results

Figure 6.23 shows a photograph of the above described device. The source and drain of the device are located on top of the pillar. The two inputs are contacted to the left and right of the pillars. The contact labelled GND represents the substrate contact.

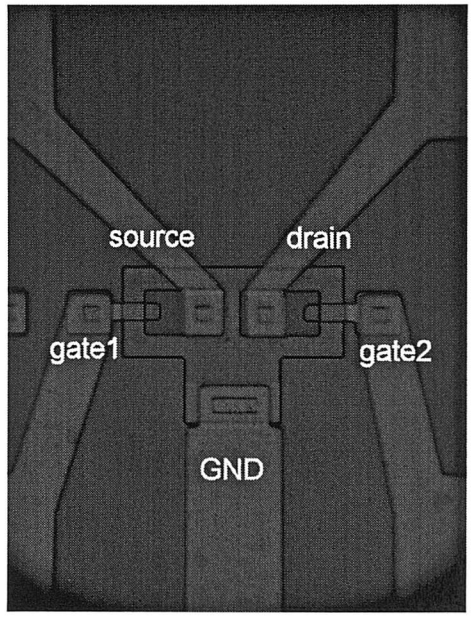
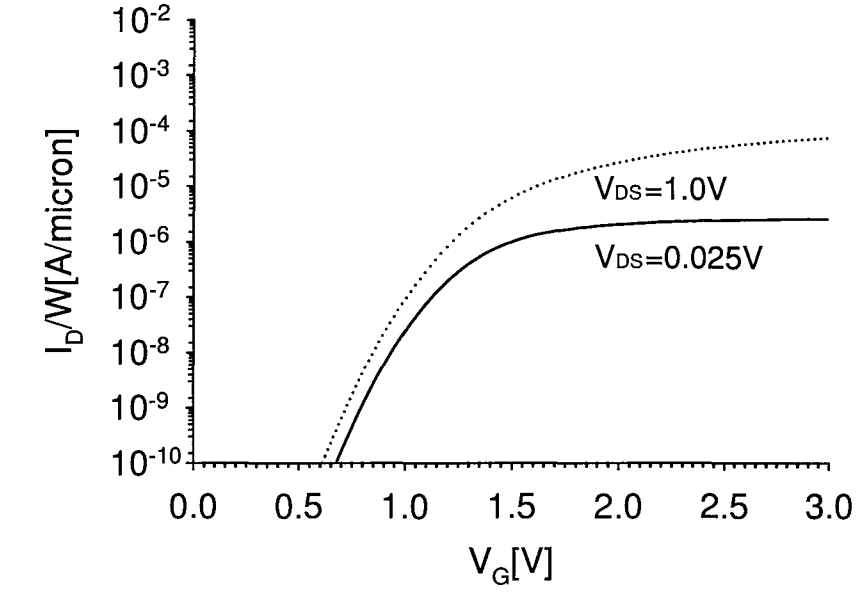
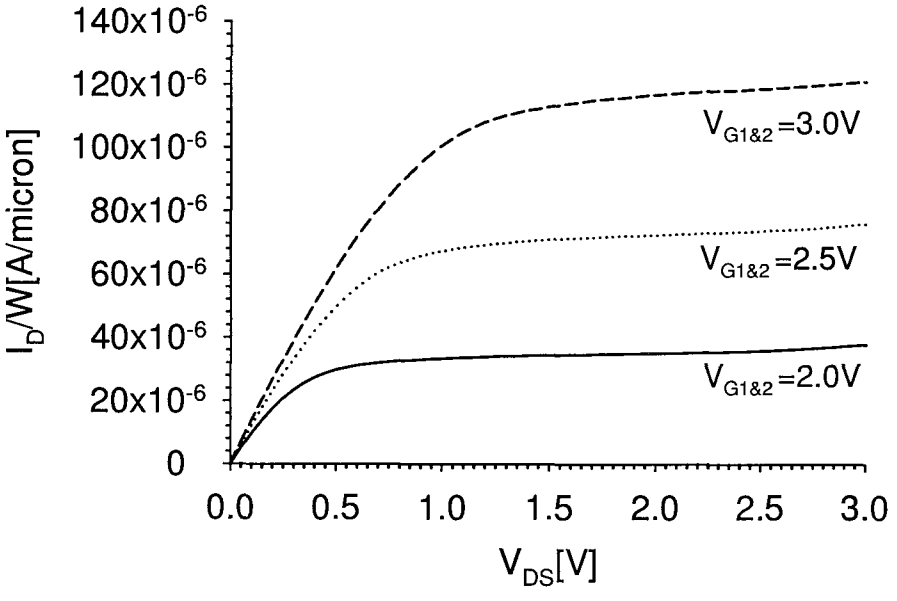


Figure 6.23: Top-view of a fabricated vertical NAND gate based on 2.0μm design rules and a channel width of 32μm. This logic gate consists of two pillars.

Figure 6.24a shows the subthreshold characteristics for V_{G1}=V_{G2}. The extracted threshold voltage was 1.17V and the subthreshold slope 108mV at $I_D = 1 \times 10^{-10}$A. Figure 6.24b depicts the output characteristic of a vertical NAND gate based on two pillars with a channel length of 2×105nm. Compared with the single gate transistor the current drive at $V_G = V_{DS}$=3V is smaller by a factor of 0.3.



a)



b)

Figure 6.24: Typical electrical characteristics of a vertical NAND-gate for V_{DS}=0.025 and 1.0V. b) Output characteristics. The channel length was 105nm and the channel width 24μm.

6.8 Summary

In this chapter experimental results on single and surround gate transistors incorporating the FILOX process have been presented. Devices based on the GAI process flow showed excellent electrical behaviour and compared favorably with reported vertical devices in the literature. However, a slight discrepancy in threshold voltage between single and surround gate devices was observed which is most likely due to the variation in oxide thickness. A comparison of measured and simulated results for

the single gate GAI transistor showed good agreement. The fabricated GBI device shows increased threshold voltage which is caused by the FILOX oxide reaching into the channel area. Vertical NOR and NAND gates have been proposed and shown to work correctly.

Chapter 7

Reducing parasitic bipolar transistor action in vertical MOSFETs

7.1 Introduction

As previously discussed in section 2.2.7 parasitic bipolar transistor action can be a problem in short channel MOS transistors because carriers are injected into the channel if the source junction becomes forward biased. This mechanism also gives rise to floating body effects in SOI transistors [84] and latchup in bulk CMOS [79, 85, 86]. In a lateral MOSFET the gain of the parasitic bipolar transistor is very small (<10), because carriers are only collected from the sidewall of the source, as shown in figure 7.1.

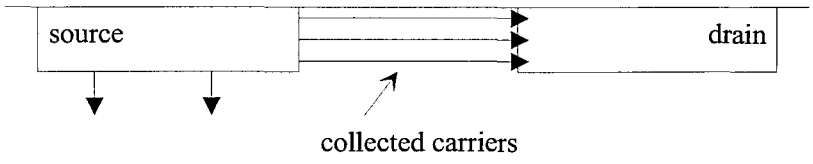


Figure 7.1: Schematic illustration of carrier collection in a lateral MOSFET

In an epitaxial vertical MOSFET the drain is located directly below the source as illustrated in figure 7.2. Almost all carriers injected from the source are collected by the drain. Therefore, the gain of the parasitic bipolar transistor created by the source (emitter), substrate (base) and drain (collector) is likely to be very high (>100).

In this chapter a method is described for reducing the gain by using polySiGe in the source. A theory is developed based on a surface recombination velocity model

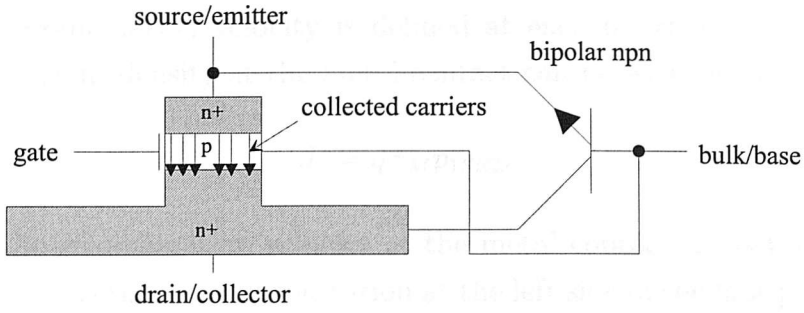


Figure 7.2: Parasitic transistor action in vertical n-MOSFET

and model predictions are compared with measured results on bipolar transistors incorporating polySiGe emitters. An increase in base current and therefore a reduction in bipolar gain will be shown.

7.2 Theory

Figure 7.3 shows a schematic illustration of a polySiGe emitter. Four regions of the emitter can be identified, namely polySiGe grains, grain boundaries, the interfacial oxide layer and the single crystal silicon emitter. Hole transport in these regions is modelled using an effective recombination velocity approach, as originally proposed by Yu et al. [87] for polySi emitters.

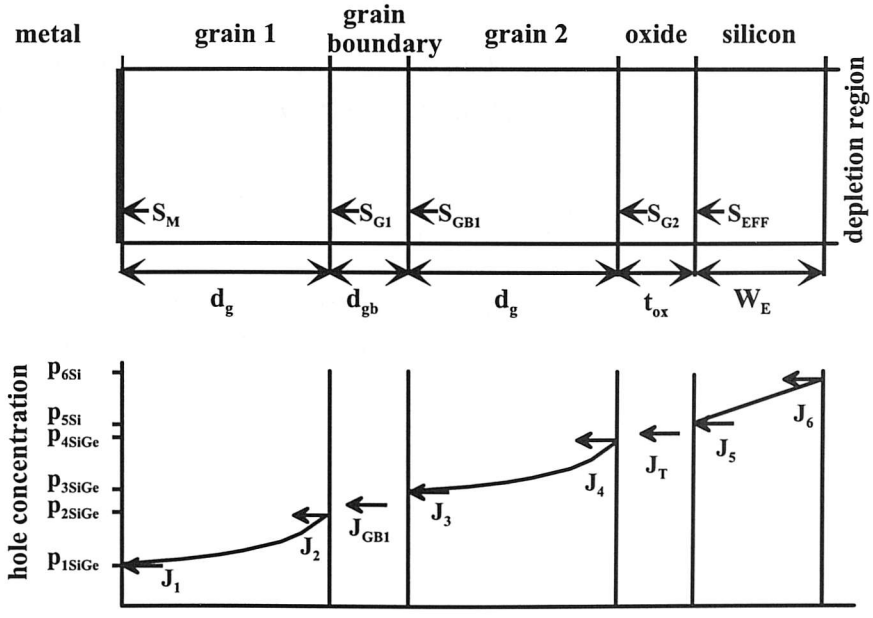


Figure 7.3: Schematic illustration of a polySiGe emitter showing the effective recombination velocities in the different regions of the emitter and the components of hole current

An effective recombination velocity is defined at each interface in figure 7.3. For example, the current density at the metal contact can be written as

$$J_1 = qS_M p_{1SiGe} \tag{7.1}$$

where S_M is the recombination velocity at the metal contact, J_1 is the hole current density and p_{1SiGe} is the hole concentration at the left side of the first polySiGe grain.

The hole current at either side of the first polySiGe grain can be derived by solving the continuity equation for holes

$$J_1 = q\left(p_{2SiGe}b_g - p_{1SiGe}a_g\right) \tag{7.2}$$

$$J_2 = q\left(p_{2SiGe}a_g - p_{1SiGe}b_g\right) \tag{7.3}$$

The parameters a_g and b_g depend on the physical properties of the grains and are given by

$$a_g = \frac{D_{pSiGe}}{L_{pSiGe}} \coth\left(\frac{d_g}{L_{pSiGe}}\right) \tag{7.4}$$

$$b_g = \frac{D_{pSiGe}}{L_{pSiGe}} \operatorname{csch}\left(\frac{d_g}{L_{pSiGe}}\right) \tag{7.5}$$

where d_g is the grain width, and L_{pSiGe} and D_{pSiGe} are the hole diffusion length and hole diffusivity in the polySiGe grain.

Equating equations 7.1 and 7.2 gives an equation for p_{1SiGe} which can then be substituted into equation 7.3 to give the current J_2

$$J_2 = q\left(a_g - \frac{b_g^2}{a_g + S_M}\right) p_{2SiGe} \tag{7.6}$$

A comparison with equation 7.1 shows that the effective recombination velocity at the right side of the first SiGe grain is

$$S_{G1} = a_g - \frac{b_g^2}{a_g + S_M} \tag{7.7}$$

The grain boundary is modelled by assuming that the grain boundary has a finite thickness d_{gb} and a mobility μ_{gb} that is different than the mobility in the grain. Recombination in the grain boundary is modelled at the interfaces between the grain boundary and the adjacent grains. The current density across the grain boundary is then

$$J_{GB1} = q\frac{D_{gb}}{d_{gb}}\left(p_{3SiGe} - p_{2SiGe}\right) \tag{7.8}$$

where D_{gb} is the hole diffusivity in the grain boundary.

Recombination at the grain boundary interfaces is modelled by the following equation

$$S_{GB} = \frac{N_{st}}{2} c_p \nu_{th} \tag{7.9}$$

where N_{st} is the trap density, c_p the trap capture cross-section and ν_{th} the thermal velocity.

Using equations 7.6 to 7.9, an equation can be derived for the current at the right side of the grain boundary J_3

$$J_3 = qS_{GB1}p_{3SiGe} \tag{7.10}$$

where

$$S_{GB1} = a_{gb} - \frac{b_{gb}^2}{a_{gb} + S_{G1}} \tag{7.11}$$

$$a_{gb} = \frac{D_{gb}}{d_{gb}} + S_{GB} \tag{7.12}$$

$$b_{gb} = \frac{D_{gb}}{d_{gb}} \tag{7.13}$$

The procedure used to derive the current at the right side of the first polySiGe grain can now be repeated to give the current at the right side of the second polySiGe grain J_4

$$J_4 = qS_{G2}p_{4SiGe} \tag{7.14}$$

where

$$S_{G2} = a_g - \frac{b_g^2}{a_g + S_{GB1}} \tag{7.15}$$

In general, there may be more than two grains in the polySiGe emitter, in which case, for n≥2, the effective recombination at the n_{th} grain is

$$S_{Gn} = a_g - \frac{b_g^2}{a_g + a_{gb} - \frac{b_{gb}^2}{a_{gb} + S_{G(n-1)}}} \tag{7.16}$$

The effect of the polySiGe layer can be explicitly highlighted by relating the hole concentration for a polySiGe grain p_{SiGe} to that for an equivalent polySi grain p_{Si}

$$p_{SiGe} = \frac{n_{iSiGe}^2}{n_i^2} p_{Si} = \left(\frac{N_{CSiGe} N_{VSiGe}}{N_{CSi} N_{VSi}} \right) \exp\left(\frac{\Delta E_G}{kT} \right) p_{Si} \tag{7.17}$$

where N_{CSiGe}, N_{VSiGe} are the effective densities of states in the conduction and valence band of SiGe, N_{CSi}, N_{VSi} are the equivalent in Si and ΔE_G the band gap difference between Si and SiGe. The effect of the polySiGe layer is illustrated in figure 7.4 which shows a graph of $S_{Gn}p_{SiGe}/p_{Si}$ as a function of the number of grains for various values of germanium content. In calculating this graph, the parameter values in [87] were used. For 0% Ge, the curve is identical to that obtained by Yu et al. [87], as indicated by the circular symbols. For a given number of grains, the effect of the germanium is to increase the value of $S_{Gn}p_{SiGe}/p_{Si}$. This trend can be understood from equation 7.17, which shows that p_{SiGe} increases strongly with Ge content. Figure 7.4 also shows that the number of grains has little effect once there are two or more grains in the polysilicon layer.

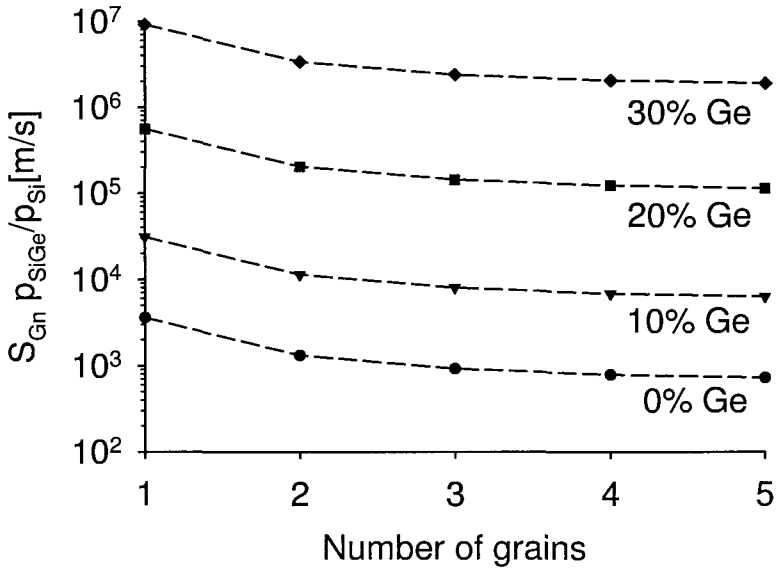


Figure 7.4: Illustration of the effect of the polySiGe emitter by plotting $S_{Gn}p_{SiGe}/p_{Si}$ as a function of the number of polySiGe grains for different Ge concentrations. The parameter values in [87] were used in the calculations.

Figure 7.5 illustrates the band diagram of the polySiGe/oxide/silicon interface. The bandgap in the polySiGe at the left side of the interfacial oxide is smaller than that in the single crystal Si at the right side, and this difference is represented by ΔE_G.

The hole current tunnelling density can be written as

$$J_T = qT_I N_{VSi}\left(\exp\left(\frac{E_{FP5}}{kT}\right) - \exp\left(\frac{E_{FP4}}{kT}\right)\right) \tag{7.18}$$

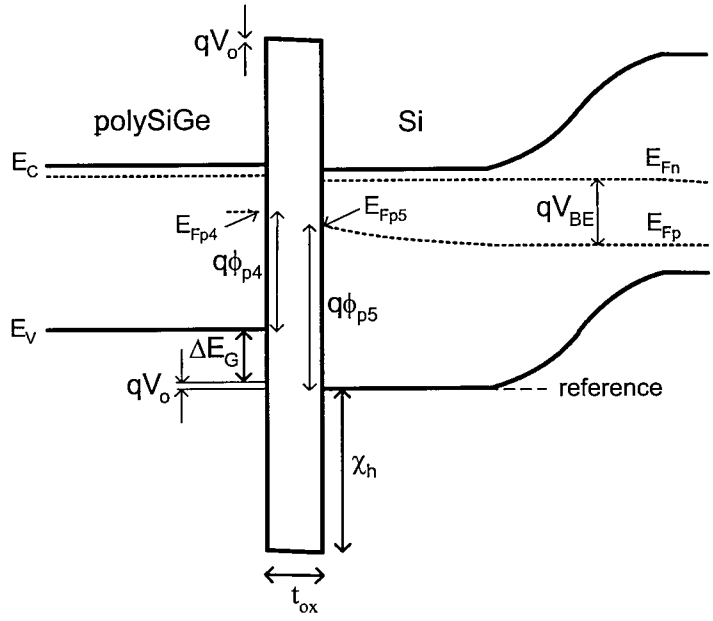


Figure 7.5: Band diagram of a polySiGe emitter showing the polySiGe/oxide/Si interface

where T_I is the tunnelling coefficient E_{Fp5} is the quasi Fermi level energy for holes on the right side of the oxide interface and E_{Fp4} the equivalent on the left side of the interface. Taking the valence band edge in the single crystal silicon as the zero energy reference and noting that the energy of holes increases downwards, we can write

$$E_{Fp5} = -q\phi_{p5} \tag{7.19}$$

$$E_{Fp4} = -q\phi_{p4} - \Delta E_G - qV_0 \tag{7.20}$$

where V_0 is the voltage drop across the interfacial oxide, which is neglected in the analysis below. The hole concentration can then be related to E_{Fp4} and E_{Fp5} using the following equations

$$p_{4SiGe} = N_{VSiGe} \exp\left(-\frac{q\phi_{p4}}{kT}\right) \tag{7.21}$$

$$p_{5Si} = N_{VSi} \exp\left(-\frac{q\phi_{p5}}{kT}\right) \tag{7.22}$$

Combining equations 7.18 to 7.22 gives

$$J_T = qT_I \left(p_{5Si} - Fp_{4SiGe}\right) \tag{7.23}$$

where

$$F = \frac{N_{VSi}}{N_{VSiGe}} \exp\left(-\frac{\Delta E_G}{kT}\right) \tag{7.24}$$

The current density J_5 at the edge of the polySiGe emitter is now given by

$$J_5 = J_T + qS_I p_{5Si} = qS_{EFF} p_{5Si} \tag{7.25}$$

where S_I models recombination at the polysilicon/silicon interface, and is given by an equation analogous to equation 7.9 and S_{EFF} is the overall effective surface recombination velocity for the polySiGe emitter, which is given by

$$S_{EFF} = S_I + \left(\frac{1}{T_I} + \frac{F}{S_I + S_{Gn}} \right)^{-1} \tag{7.26}$$

It is worth noting that holes tunnelling through the oxide become hot when they appear in the polySiGe grain, as they pick up kinetic energy of $\sim \Delta E_G$. The holes will quickly thermalise to the valence band edge and continue to diffuse towards the emitter contact. This effect is presented by a break in the hole quasi Fermi level in the SiGe grain, close to the oxide layer.

Figure 7.6 illustrates the variation of S_{EFF} with interfacial layer thickness t_{ox} for germanium contents of 0 to 35% in 5% steps.

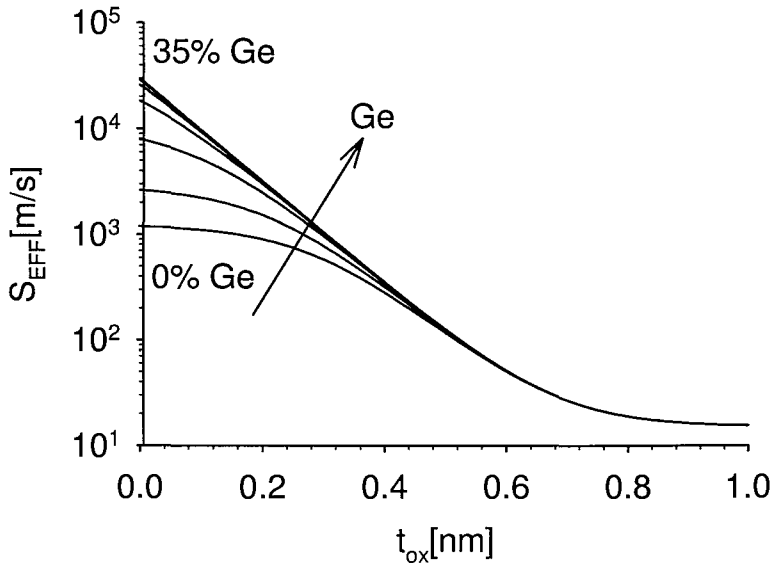


Figure 7.6: Calculated values of the effective surface recombination velocity S_{EFF} of the complete polySiGe emitter as a function of interfacial layer thickness t_{ox} for different Ge concentrations. The parameter values in table 7.1 were used in the calculations.

In calculating the curves in figure 7.6, the parameters in table 7.1 were used. It has been assumed that the density of states in the conduction band, hole diffusion coefficient and hole diffusion length are the same in SiGe as in Si [88]. Three regions

of the characteristic can be identified. For large values of interfacial layer thickness, T_I is small, and hence can be neglected with respect to S_I. The value of S_{EFF} therefore approaches the value of S_I at large values of interfacial layer thickness. In this situation, transport in the polySiGe emitter is dominated by recombination at the polysilicon/silicon interface. For intermediate values of interfacial layer thickness, T_I cannot be neglected, and since T_I varies exponentially with interfacial layer thickness [87]. S_{EFF} also varies strongly with interfacial layer thickness. In this situation, transport in the polySiGe emitter is dominated by tunnelling through the interfacial layer. For small values of interfacial layer thickness, T_I is large, and hence the value of S_{EFF} approaches the value of S_{Gn}. In this situation, the Ge content in the polySiGe emitter has a strong influence on S_{EFF}.

Parameter	**Name**	**Value**	**Unit**
D_{pSiGe}	diffusity of holes in polySiGe grains	3.34×10^{-4}	m^2/s
L_{pSiGe}	hole diffusion length in polySiGe grains	2.94×10^{-7}	m
d_g	width of a poly grain	1.25×10^{-7}	m
S_M	recombination velocity at the metal contact	1×10^4	m/s
S_{GB}	recombination velocity of grain boundary	75	m/s
S_I	oxide/silicon interface recombination velocity	15	m/s
d_{gb}	grain boundary width	2×10^{-9}	m
D_{gb}	grain boundary hole diffusity	5.2×10^{-6}	m^2/s
χ_h	potential barrier	1.5	eV
n_i	intrinsic carrier concentration in silicon	1.45×10^{16}	m^{-3}
A	emitter area	100×10^{-12}	m^2

Table 7.1: Parameter values used to calculate the theoretical values of effective recombination velocity S_{EFF} of the complete polySiGe emitter and base current I_B

Figure 7.6 also shows that the effect of the Ge on the value of S_{EFF} saturates above a Ge concentration of about 20%. This trend is shown more clearly in figure 7.7, where the value of S_{EFF} is plotted as a function of Ge content for different values of interfacial layer thickness t_{ox}. This figure shows that the value of S_{EFF} increases only slightly at high Ge contents. There is therefore little to be gained by using Ge contents in the polySiGe layer higher than 20%.

For simplicity, an equation for the base current can be derived [70] by assuming that the single crystal emitter is uniformly doped and transparent to minority carriers

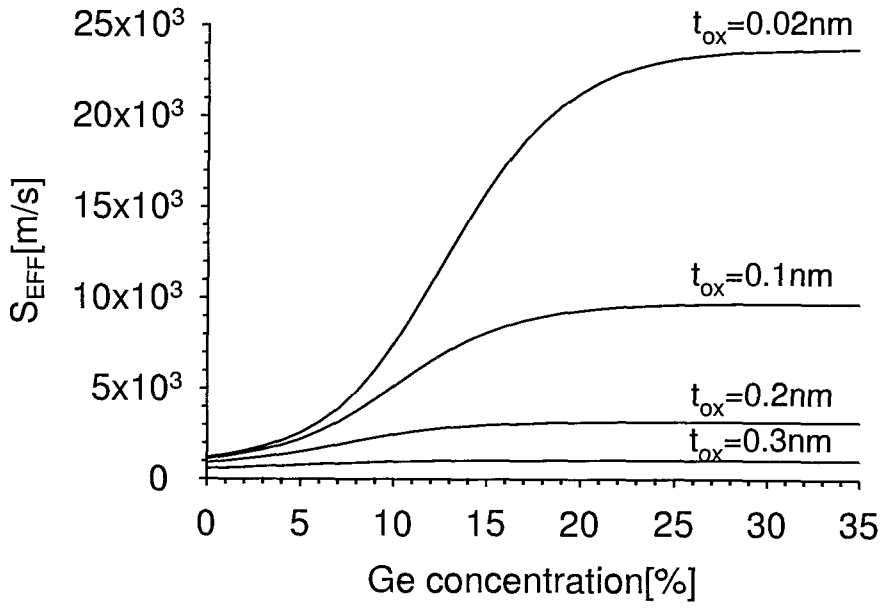


Figure 7.7: Calculated values of the effective surface recombination velocity S_{EFF} of the complete polySiGe emitter as a function of Ge concentration for different interfacial oxide thicknesses t_{ox}

(negligible recombination)

$$I_B = \frac{qAn_i^2}{\frac{N_{Deeff}W_E}{D_{pe}} + \frac{N_{Deeff}}{S_{EFF}}} \exp\left(\frac{qV_{BE}}{kT}\right) \tag{7.27}$$

where N_{Deeff} is the effective doping in the single crystal silicon emitter, W_E is the junction depth and D_{pe} is the hole diffusivity in silicon. This equation will be used to interpret the experimental results on transistors with polySiGe emitters.

7.3 Experimental Procedure

Silicon bipolar transistors were fabricated to experimentally determine the effect of germanium incorporation into the polysilicon emitter. Figure 7.8 shows a schematic cross-section of the manufactured bipolar transistors. The base was fabricated by implanting $2\times10^{13}cm^{-2}$ boron at 40keV through an 80nm thermal oxide layer. After annealing for 30 minutes at 950°C prior to emitter fabrication, the wafers were given an RCA clean, followed by a dip etch in buffered HF to remove any chemical oxide grown during the RCA clean. Immediately following this etch, a 250-290nm layer of in-situ phosphorus doped polycrystalline Si or SiGe was deposited in a low pressure chemical vapour deposition (LPCVD) system at a temperature of 540°C. The SiGe layers were deposited with Ge contents of 10 and 19%. The emitter was completed by annealing for 30s at 900°C to diffuse the phosphorus from the polycrystalline Si

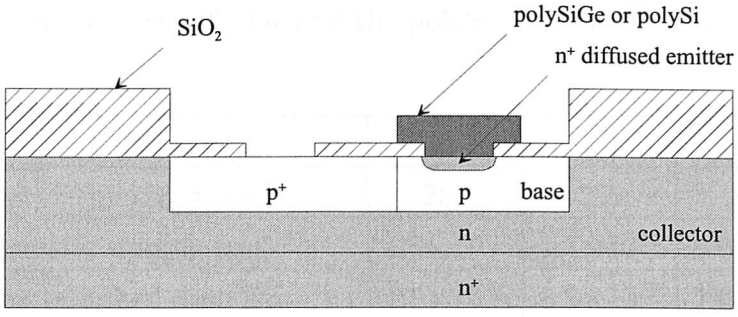


Figure 7.8: Cross-section of the manufactured bipolar transistor

or SiGe into the underlying single crystal Si. All measurements of the transistor characteristics were performed at a temperature of 25°C.

7.4 Results

Figure 7.9 shows secondary ion mass spectrometry (SIMS) plots through the emitter of the polySiGe transistor with 10% Ge annealed for 30s at 900°C. It can be seen that the germanium profile is approximately uniform throughout the 250nm polySiGe layer. The phosphorus profile in the polySiGe is similarly reasonably uniform with a concentration of $1.7\times10^{20}cm^{-3}$.

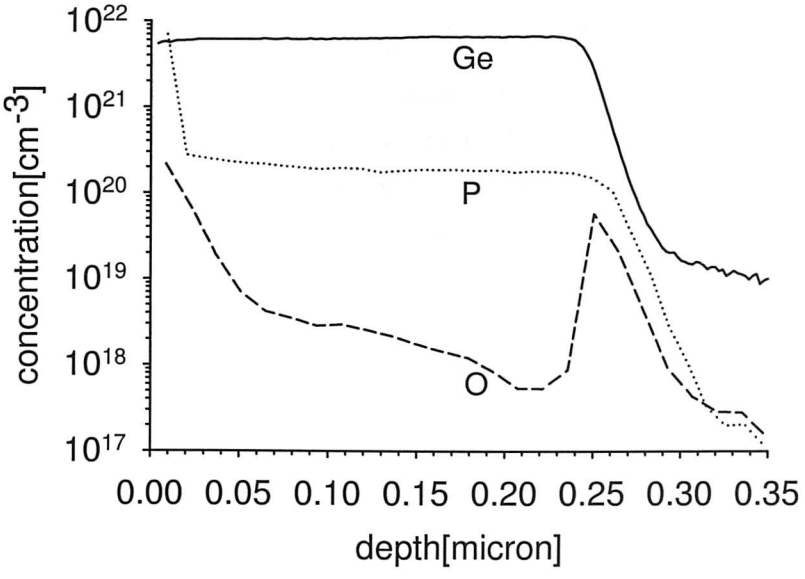


Figure 7.9: Measured germanium, phosphorus and oxygen SIMS profiles for bipolar transistors with polySi$_{0.9}Ge_{0.1}$ emitter given an anneal of 30s at 900°C

The oxygen profile in figure 7.9 shows a dose of $8.8\times10^{13}cm^{-2}$ at the interface between the polySiGe and the single crystal silicon. Similar results were obtained for

the polySiGe transistor with 19% Ge and the polySi control transistor, as summarised in table 7.2.

Ge content [%]	**0**	**10**	**19**
Poly layer thickness [nm]	250	250	290
Poly emitter doping [cm^{-3}]	1.5×10^{19}	1.7×10^{20}	6.0×10^{19}
Oxygen interface dose [cm^{-2}]	1.5×10^{14}	8.8×10^{13}	7.0×10^{13}
Interfacial layer thickness [nm]	0.031	0.018	0.015
W_E [nm]	30	50	40

Table 7.2: Summary of experimental data obtained from the SIMS measurements

The oxygen doses in the three samples lie in the range 0.7 to $1.5\times10^{14}cm^{-2}$, and there is no discernable trend in the oxygen dose with Ge content. The polySi and polySiGe layer deposition was performed one wafer at a time, and hence the variation in oxygen dose between the wafers is probably due to small differences in the timings of the wafer transfer into the deposition system. Table 7.2 also shows values of interfacial layer thickness, calculated assuming a uniform, stoichiometric silicon dioxide layer and a silicon atom concentration of $4.8\times10^{22}atoms/cm^3$ and the thickness of the single crystal portion of the emitter W_E extracted from the SIMS profiles.

Cross-Sectional Transmission Electron microscopy (TEM) was used to characterise the structure of the grains in the polySiGe and polySi layers. Figure 7.10 shows TEM cross-sections of a polySiGe emitter. No discernable difference was found in the structure of the grains in polySiGe and polySi layers. The grains in both materials were columnar in shape, with an average grain size of 125nm.

Figure 7.11 shows TEM cross-sections of a polySi emitter. The grain structure is similar in both cases, with large columnar grains in the top part of the layers and smaller grains adjacent to the interface.

Figure 7.12 shows Gummel plots for transistors annealed for 30s at 900°C with 10% and 19% polySiGe emitters and for a control transistor with a polySi emitter. The collector characteristics are ideal, with an ideality factor of 1.06 for all three devices. The base characteristics are near ideal, with ideality factors of 1.19, 1.13 and 1.13 at V_{BE}=0.6V for Ge contents of 0, 10 and 19%, respectively. The transistors with 10 and 19% Ge show increased base current at V_{BE}=0.6V compared with a transistor without Ge by a factor of 3.2 for 10% Ge and 4.0 for 19% Ge.

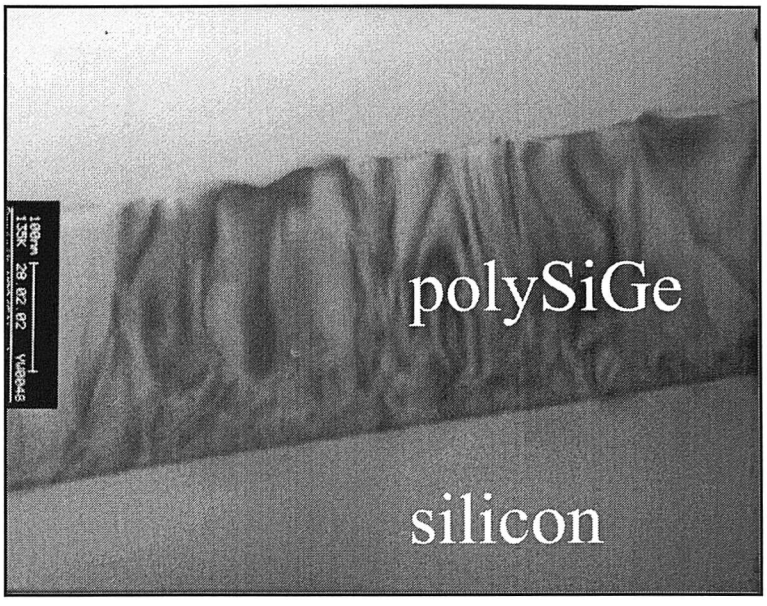


Figure 7.10: TEM cross-section of a polySi$_{0.90}Ge_{0.10}$ emitter annealed for 30s at 900^{o}C showing the polySiGe grains

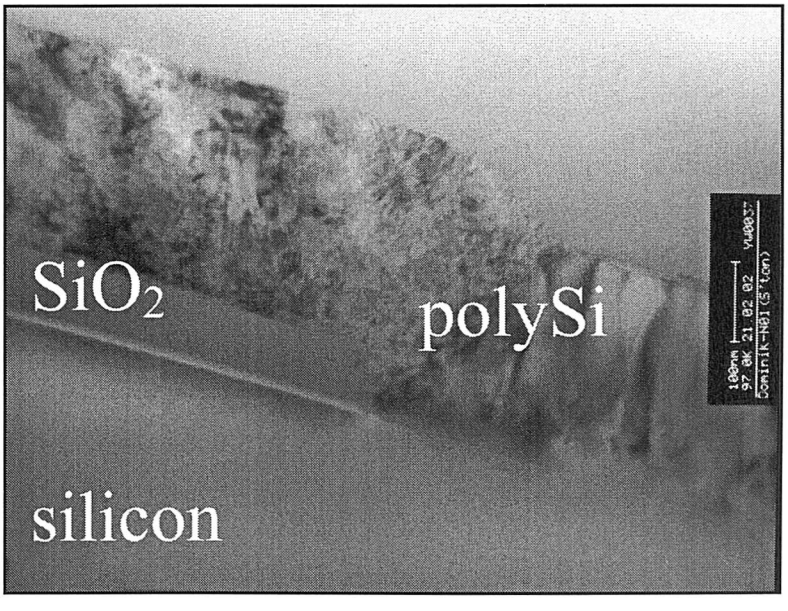


Figure 7.11: TEM cross-section of a polySi emitter annealed for 30s at 900^{o}C showing polySi over the emitter region

7.5 Discussion

The experimental results in figure 7.12 show that there is a large increase in base current when the germanium content of the polySiGe layer is increased from 0% to 10%, but a much smaller increase when the germanium content is increased from 10% to 19%. This result is in qualitative agreement with the theoretical curves in figure 7.7, which shows that the effect of the germanium on the base current saturates for germanium

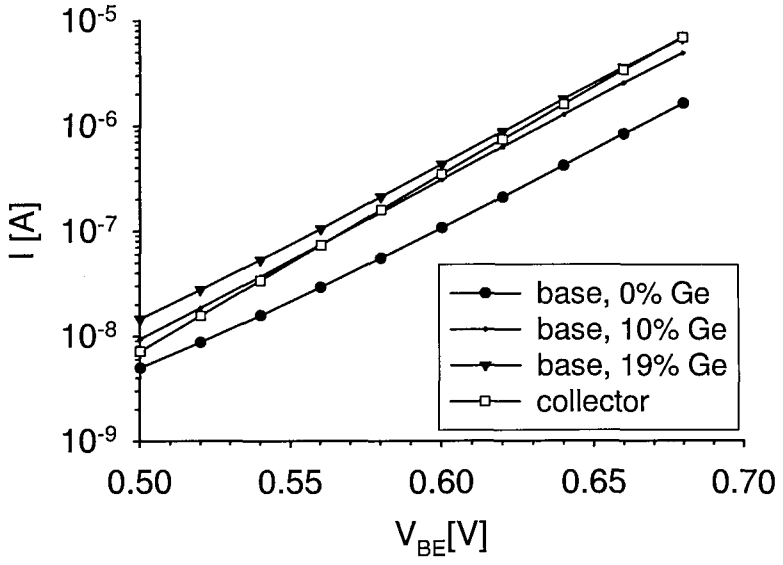


Figure 7.12: Measured Gummel plots for transistors with 0, 10 and 19% Ge in the polySiGe emitter, annealed at 900°C. The collector currents are identical and only one is shown.

concentrations above about 20%.

In order to quantitatively compare the experimental values of base current with calculated values, the small non-ideality in the base characteristics of figure 7.12 needs to be taken into account. To address this problem, the method of Hamel [89] has been used to correct for this non-ideality. This method uses an analysis to extract the underlying ideal component of the base current. The corrected base characteristics are shown in figure 7.13 and the corrected values base current at V_{BE}=0.6V are summarised in table 7.3. It can be seen that the corrected values of base current are a factor of 2-3 smaller than the measured values at V_{BE}=0.6V.

Equation 7.27 was used to calculate the base currents using the measured values of interfacial oxide thickness t_{ox} and emitter doping W_E in table 7.2. The average doping in the single crystal Si emitter was calculated from the SIMS profiles and the band gap narrowing model of del Alamo [90] used to calculate the effective doping N_{Deeff}. Calculated base characteristics are shown in figure 7.14.

Calculated values of base current at $V_{BE} = 0.6V$ are compared with the measured (corrected) values in table 7.3, where it can be seen that the agreement is within a factor of 1.1 for 0% Ge, 1.8 for 10% Ge and 1.1 for 19% Ge. This agreement is excellent considering the uncertainties of the parameter values in table 7.1.

Table 7.3 also summarises the calculated and measured (corrected) ratios of nor-

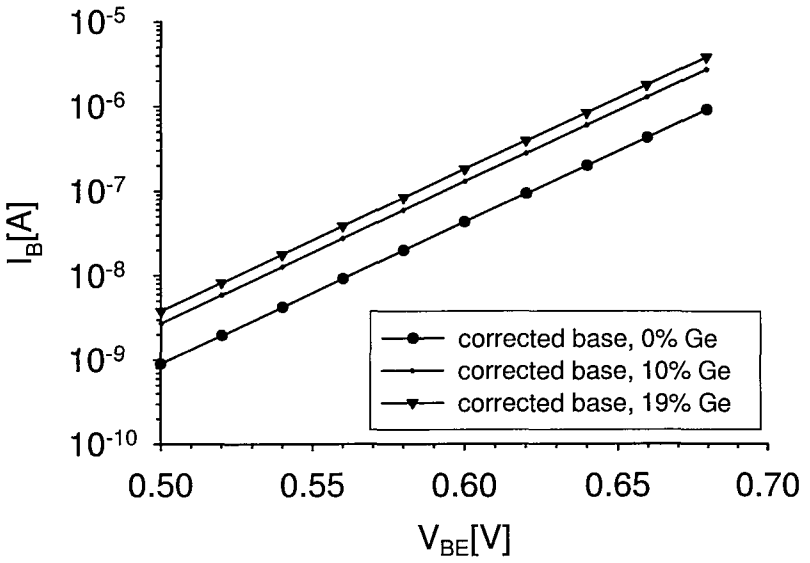


Figure 7.13: Base current I_B, corrected using the method of Hamel [89], as a function of base/emitter voltage V_{BE} for 0%, 10% and 19% Ge.

Ge content [%]	**0**	**10**	**19**
Measured I_B at V_{BE}=0.6V [A]	1.0×10^{-7}	3.0×10^{-7}	4.3×10^{-7}
Corrected [89] I_B at V_{BE}=0.6V [A]	4.2×10^{-8}	1.3×10^{-7}	1.8×10^{-7}
Calculated I_B at V_{BE}=0.6V [A]	3.8×10^{-8}	7.2×10^{-8}	1.6×10^{-7}
Corrected normalised $I_B(Ge)/I_B(0)$	1	3.2	4.0
Calculated normalised $I_B(Ge)/I_B(0)$	1	1.9	4.2

Table 7.3: Comparison of measured and calculated values of base current

malised base current, obtained by taking the ratio of the base current in the appropriate polySiGe transistor to that in the polySi transistor. The measured (corrected) ratios of 3.2 and 4.0 for 10 and 19% Ge, respectively, are in reasonable agreement with the calculated values of 1.9 and 4.2.

In polysilicon emitters, the interfacial layer has a strong effect on the current gain [91]. It is therefore important to understand how the interfacial oxide thickness influences the base current increase obtained when germanium is introduced into the polysilicon emitter. The opposite trends with germanium content and interfacial layer thickness are shown in figure 7.6 and this indicates that an interfacial layer thickness of less than about 0.3nm is needed if the germanium is to have a significant effect on the effective recombination velocity S_{EFF} and the base current. In practice, this could be achieved using an ex-situ HF etch in combination with polySiGe deposition in a cluster tool [92]. Even bigger effects could probably be achieved by breaking up

the interfacial layer using an interface anneal prior to polySiGe deposition [91] or by epitaxially regrowing the polySiGe during the emitter anneal

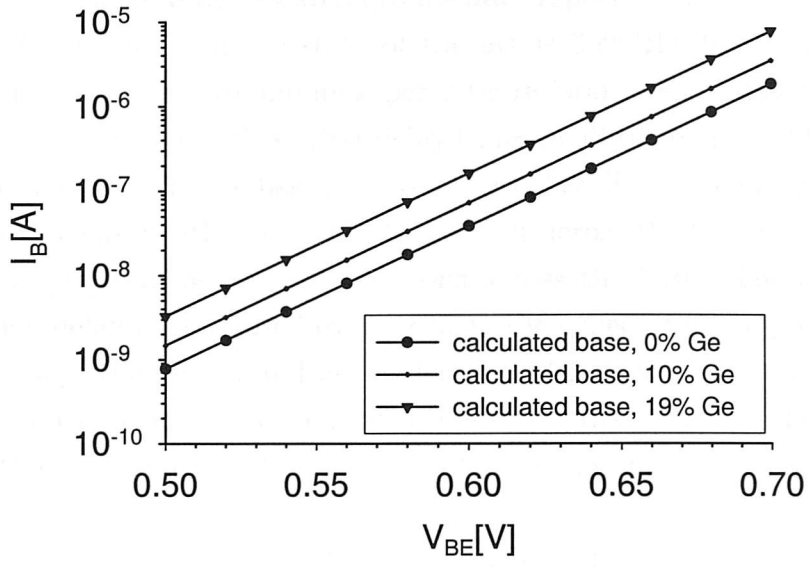


Figure 7.14: Calculated base currents I_B as a function of base/emitter voltage V_{BE} for 0, 10 and 19% Ge concentrations

7.6 Vertical MOSFET with polySiGe source

Figure 7.15 shows a schematic cross-section of the proposed polycrystalline SiGe source. The reduced band gap of the polySiGe layer will give a dramatic reduction in the gain of the parasitic bipolar transistor. The polySiGe source would have the additional advantage that a very shallow, well-controlled source junction could be created by diffusion from the polySiGe layer. This would give good control over the channel length.

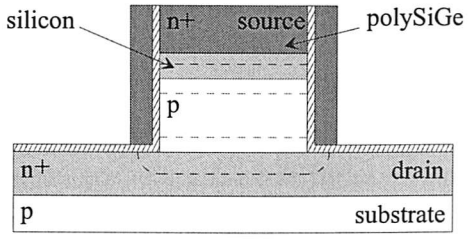


Figure 7.15: Polycrystalline SiGe source

7.7 PolySiGe emitter for gain control in SiGe HBTs

Over the last few years, the high frequency performance of SiGe HBTs has improved to such an extent that several research groups have reported values of f_T and/or f_{max} around 100GHz [93–97], and the state of the art is 300GHz [93]. To achieve this performance, it is necessary to minimise parasitic resistance and capacitance and optimise the vertical doping profile so that delay times in all the regions of the transistor are minimised, particularly the base and collector delay. The base delay is minimised by using a narrow basewidth and large Ge gradient across the base to create a built-in electric field [98] that accelerates electrons across the base. The collector/base depletion region delay is minimised by increasing the collector doping to decrease the collector/base depletion width and hence decrease the electron transit time. Unfortunately high collector doping concentrations have the disadvantage of degrading the common emitter breakdown voltage BV_{CEO} of the transistor.

The common emitter breakdown voltage BV_{CEO} of a bipolar transistor is strongly influenced by the common emitter current gain, as can be seen from the following equation [70]

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} \tag{7.28}$$

where BV_{CBO} is the common base breakdown voltage (i.e. the breakdown voltage of the collector/base junction), β is the common emitter gain and n is an empirical parameter that takes a value between 3 and 6. A gain of around 100 is needed for good circuit operation, but there is little advantage to be obtained from higher gains because of the degradation in BV_{CEO}. In SiGe HBTs, very high values of gain can be obtained, particularly when a high Ge concentration is used to give a large built-in electric field across the base. For example, Washio et al. [95] reported a gain of 1900 in a SiGe HBT with an f_{max} of 107GHz and an f_T of 90GHz. Huizing et al. [99] proposed that an epitaxial SiGe layer could be incorporated into the emitter to allow the base current to be tuned.

The work reported in this chapter shows that the gain of a bipolar transistor could be controlled by introducing Ge into the polysilicon emitter. This method has the advantage of allowing the gain to be controlled independently of the base profile and thereby allows the breakdown voltage BV_{CEO} to be optimised for a given f_T.

7.8 Summary

Parasitic transistor action can degrade vertical MOSFET performance. In order to address this problem a new vertical transistor design has been proposed with a polySiGe cap as the source. A theoretical expression has been derived for the effective surface recombination velocity of this polycrystalline SiGe source, and predicted values of parasitic base current compared with measured values on bipolar transistors with polycrystalline SiGe emitters. The measured results show an increase in base current by a factor of 3.2 for 10% Ge in the polySiGe emitter and by 4.0 for 19% Ge. The theory predicts that, for a given interfacial layer thickness, the base current initially increases with Ge content and then saturates for germanium contents of about 20%, a trend which agrees well with the experimental results. The size of the base current increase with Ge content depends on the thickness of the interfacial layer, with larger increases being obtained for thinner interfacial layers. The introduction of germanium into a polysilicon emitter therefore allows the base current, and hence the gain, to be controlled by means of the Ge content in the polySiGe emitter. This property is likely to be very useful in partially depleted vertical MOSFETs to suppress parasitic bipolar transistor action. Furthermore, this concept also provides a way of controlling the gain of a SiGe HBT and therefore of increasing the common emitter breakdown voltage BV_{CEO}.

Chapter 8

Conclusions

In this thesis several methods have been investigated to reduce parasitics in vertical MOS devices. These methods include a fillet local oxidation (FILOX) process to reduce overlap capacitance between the polysilicon gate track and the source, drain and substrate, optimisation of the pillar processing sequence, inclusion of a pillar top insulator and the incorporation of Ge into a polysilicon source.

First order calculations have been performed to compare the overlap capacitances of lateral and vertical transistors using 100nm industry design rules under the assumption of equivalent junction depths. For single gate vertical transistors incorporating the FILOX process, the gate/source overlap capacitance is 60% of that of a comparable lateral device and the gate/drain overlap capacitance is 40%. For surround gate transistors incorporating the FILOX the gate/source overlap capacitance is 5% of that of a comparable lateral device and the gate/drain overlap capacitance 20%.

The FILOX process has been simulated using calibrated values of nitride viscosity. It was found that a thick nitride fillet reduces the encroachment on the bottom of the pillar but has little influence on the encroachment on the pillar sidewall at the top of the pillar. Decreasing the pad oxide thickness for a given nitride thickness reduced the encroachment on the side of the pillar. Covering the pillar top with a nitride insulation layer completely suppresses the encroachment on the sidewall at the top of the pillar. Simulations showed that the stress in pillars with a nitride cap is lower than that in pillars with an oxide cap.

The FILOX process was used to fabricate pillar capacitors and a comparison made between capacitors with and without a nitride layer on the pillar top and with and without the FILOX oxide. Pillar structures with a nitride top showed a reduction of capacitance of 1.4 and structures incorporating the FILOX oxide a reduction of 4.0.

The fabricated structures were compared with simulated capacitors, and the oxide thickness on the pillar sidewall extracted. The simulated gate oxide on the pillar sidewall is 3.1nm thicker than that on horizontal surfaces because of the different orientations of the silicon. Measured and simulated values of sidewall gate oxide thicknesses agree within a factor of 1.18 for the FILOX capacitors. Kinks in the CV characteristics in inversion have been observed and explained by the formation of an inversion layer beneath the LOCOS field oxide.

Experimental results on fabricated single and surround gate transistors have been presented. The devices showed a subthreshold slope of 111 and 123mV/decade for single and surround gate transistors with a 3nm gate oxide thickness. These results compared favorably with reported vertical devices in the literature. A comparison of measured and simulated results for the single gate transistor showed good agreement. Vertical NOR and NAND gates have been proposed and shown to function correctly. A dielectric pocket concept has been proposed for vertical MOSFETs which has the potential to reduce short channel effects.

The use of a polySiGe source has been proposed to reduce parasitic bipolar transistor action in vertical MOSFETs. A theoretical model has been derived for the base current of the parasitic bipolar transistor in terms of an effective surface recombination velocity for the polycrystalline SiGe layer. The polySiGe source allows the parasitic base current, and hence the parasitic gain, to be controlled by means of the Ge content in the polySiGe layer. This property is likely to be very useful in fully depleted vertical MOSFETs to suppress parasitic bipolar transistor action. Furthermore, this concept also provides a way of controlling the gain of a SiGe HBT and therefore of increasing the common emitter breakdown voltage BV_{CEO}. Bipolar transistors have been fabricated with a polySiGe emitter (source) and values of base current measured for different Ge contents. It has been found that 19% Ge increases the base current (suppresses the gain) by a factor of 4.0. Measured and calculated values of ideal base current agree within a factor of 1.13 for a Ge content of 19%.

Chapter 9

Suggestions for future work

There are a number of areas from the work presented in this thesis where work might be carried out in the near future. These are summarised below.

- The fabricated capacitor batch includes several devices incorporating corners. Measurements of these structures should show the effects of corners.
- Further measurements on the vertical MOSFETs would allow the influence of channel length on on-current and threshold voltage to be determined. The leakage currents could be measured and their influence on the device performance investigated. The configuration of SOT and DOT could be investigated and a comparison made with examples in the literature. Further measurements on the fabricated logic gates could be carried out and their potential for high speed applications could be investigated. The functional 51 stage ring oscillators could be measured and compared with simulated results. RF measurements to show the maximum oscillation frequency and the cutoff could be extracted since special probe pads were included in the layout.
- Measurements of the common base breakdown voltage (BV_{CBO}) of both, control and SiGe HBTs could be carried out to show the increase of the common emitter breakdown voltage (BV_{CEO}) caused by the incorporation of SiGe in the poly emitter. Based on the polySiGe source idea a batch is currently being fabricated incorporating polySiGe sources into vertical transistors. This batch needs to be further processed and measured to show the reduction of parasitic capacitance caused by the incorporation of SiGe.

In the longer term work along the following lines would advance the state of the art:

- Realisation of transistors with dielectric pockets.

- Realisation of transistors with thin, fully depleted pillars to assess the improvements in short-channel effects that can be obtained from double and surround gates.

Appendix A

Simulation script files

The following Silvaco's Athena/Atlas simulation script files were used for the simulation presented. A detailed description of the syntax and models used can be found in [80, 100].

A.1 FILOX device simulations

See section 4.3 for details.

```
# file: thesis/filox/oxide/filox.in
# some variables...
# 50 -> 20nm
# 6 -> 5nm
# 2 -> 3nm
set padOxide = 6
# deposited nitride thickness...
set nitrideTh = 0.130
# nitride etch rate...
# 130nm -> 13
# 70nm -> 7
# 40nm -> 3.5
set nitrideEtch = 13
# pillar height...
# 230nm -> 21
# 80nm -> 9.01
set pillarHeight = 21

go athena

# define mash...
line x location=0.8             spacing=0.02
line x location=0.9             spacing=0.01
line x location=1.1             spacing=0.01
line x location=1.2             spacing=0.02

line y location=0.0 spacing=0.01
line y location=0.35 spacing=0.01

# initialise the wafer...
init silicon boron resistivity=0.75 orientation=100
# oxide grid (initial and subsequent)...
method gridinit.ox=0.005 grid.oxide=0.01 oxide.rel=0.02
```

```
# etch 230 nm pillar...
# first the photoresist...
deposit photores thick=0.1 div=5
etch photores left p1.x=1.000
# pillar etch...
rate.etch machine=pillar2 silicon n.m  rie isotropic=0.5 dir=10.00 chem=1 div=0.1
etch machine=pillar2 time=$"pillarHeight" minutes
# strip resist...
etch photores all
# etch off top peak (top 20nm only)...
etch silicon above p1.y=0.020
#tonyplot

# stress relieve oxide...
diffuse time=$"padOxide" temp=900 dryo2 pressure=1 hcl.pc=3
extract name="pad_sio2" thickness material="SiO^2" mat.occno=1 x.val=1.15

# deposit nitride and etch nitride fillet...
deposit nitride thickness=$"nitrideTh" div=14
rate.etch machine=fillet2 nitride n.m  rie isotropic=1 dir=10 chem=1 div=0.1
etch machine=fillet2 time=$"nitrideEtch" minutes
tonyplot

# etch pad oxide...
etch oxide dry thick=$"pad_sio2"/10000
tonyplot

# model parameter...
material oxide visc.0=5.1 visc.E=3.48 weto2
material nitride visc.0=2e3 visc.E=2.5625

#FILOX...
oxide stress.dep=t
method viscous

# step1....
diffuse time=0.5 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness1" thickness material="SiO^2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO^2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO^2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO^2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO^2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO^2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO^2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO^2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO^2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO^2" mat.occno=1 y.val=0.050
```

```
extract name="pad_sio2Y0075" thickness material="SiO~2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO~2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO~2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO~2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO~2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO~2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO~2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO~2" mat.occno=1 y.val=0.250
struct outf=filox1.str
#tonyplot -st filox1.str

# step2....
diffuse time=0.5 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness2" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO~2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO~2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO~2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO~2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO~2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO~2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO~2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO~2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO~2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO~2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO~2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO~2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO~2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO~2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO~2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO~2" mat.occno=1 y.val=0.250
struct outf=filox2.str
#tonyplot -st filox2.str

# step3....
diffuse time=1 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness3" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
```

```
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO^2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO^2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO^2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO^2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO^2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO^2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO^2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO^2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO^2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO^2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO^2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO^2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO^2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO^2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO^2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO^2" mat.occno=1 y.val=0.250
struct outf=filox3.str
#tonyplot -st filox3.str

# step4....
diffuse time=1 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness4" thickness material="SiO^2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO^2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO^2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO^2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO^2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO^2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO^2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO^2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO^2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO^2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO^2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO^2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO^2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO^2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO^2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO^2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO^2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO^2" mat.occno=1 y.val=0.250
struct outf=filox4.str
#tonyplot -st filox4.str

# step5....
diffuse time=1 temp=1000 weto2
# FILOX thickness...
```

```
extract name="FILOX thickness5" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO~2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO~2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO~2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO~2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO~2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO~2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO~2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO~2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO~2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO~2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO~2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO~2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO~2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO~2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO~2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO~2" mat.occno=1 y.val=0.250
struct outf=filox5.str
#tonyplot -st filox5.str

# step6....
diffuse time=1 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness6" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO~2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO~2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO~2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO~2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO~2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO~2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO~2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO~2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO~2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO~2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO~2" mat.occno=1 y.val=0.125
```

```
extract name="pad_sio2Y0150" thickness material="SiO~2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO~2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO~2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO~2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO~2" mat.occno=1 y.val=0.250
struct outf=filox6.str
#tonyplot -st filox6.str

# step7....
diffuse time=2 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness7" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO~2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO~2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO~2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO~2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO~2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO~2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO~2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO~2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO~2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO~2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO~2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO~2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO~2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO~2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO~2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO~2" mat.occno=1 y.val=0.250
struct outf=filox7.str
#tonyplot -st filox7.str

#step8....
diffuse time=3 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness8" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO~2" mat.occno=1 x.val=0.960
```

```
extract name="pad_sio2X0970" thickness material="SiO~2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO~2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO~2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO~2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO~2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO~2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO~2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO~2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO~2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO~2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO~2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO~2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO~2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO~2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO~2" mat.occno=1 y.val=0.250
struct outf=filox8.str
#tonyplot -st filox8.str

#step9....
diffuse time=4 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness9" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO~2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO~2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO~2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO~2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO~2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO~2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO~2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO~2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO~2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO~2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO~2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO~2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO~2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO~2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO~2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO~2" mat.occno=1 y.val=0.250
struct outf=filox9.str
tonyplot -st filox9.str
```

A.1.1 Extraction of stress

This script file was used to extract the maximum amounts of normal stress presented in table 4.3 and 4.4.

```
# v d kunz
# 05/12/2002
# directory:
#..students/vdk99r/thesis/filox/stress.in
##############################################################################
# simulation:
# - load in file
# - extract maximum stress
# - done
##############################################################################

# let's start...
go athena

# extract directly...
extract init infile="filox4_5_70.str"

# extract stress...
# nitride...
extract name="max_stress_xSi3N4" 2d.max.conc impurity="Stress X" material="Si~3N~4" datafile="stress.txt"
extract name="XstressX" x.pos datafile="stress.txt"
extract name="XstressY" y.pos datafile="stress.txt"

extract name="max_stress_ySi3N4" 2d.max.conc impurity="Stress Y" material="Si~3N~4" datafile="stress.txt"
extract name="YstressX" x.pos datafile="stress.txt"
extract name="YstressY" y.pos datafile="stress.txt"

# oxide...
extract name="max_stress_xSiO2" 2d.max.conc impurity="Stress X" material="SiO~2" datafile="stress.txt"
extract name="XstressX" x.pos datafile="stress.txt"
extract name="XstressY" y.pos datafile="stress.txt"

extract name="max_stress_ySiO2" 2d.max.conc impurity="Stress Y" material="SiO~2" datafile="stress.txt"
extract name="YstressX" x.pos datafile="stress.txt"
extract name="YstressY" y.pos datafile="stress.txt"

# silicon...
extract name="max_stress_xSiO2" 2d.max.conc impurity="Stress X" material="silicon" datafile="stress.txt"
extract name="XstressX" x.pos datafile="stress.txt"
extract name="XstressY" y.pos datafile="stress.txt"

extract name="max_stress_ySiO2" 2d.max.conc impurity="Stress Y" material="silicon" datafile="stress.txt"
extract name="YstressX" x.pos datafile="stress.txt"
extract name="YstressY" y.pos datafile="stress.txt"
# end
```

A.2 FILOX device simulations with top insulator

See section 4.6 for details.

```
# file: thesis/filox/nitride/rampnitride.in
# some variables...
# 50 -> 20nm
# 6 -> 5nm
# 2 -> 3nm
set padOxide = 50
# deposited nitride thickness...
```

```
set nitrideTh = 0.07
# nitride etch rate...
# 130nm -> 13
# 70nm -> 7
# 40nm -> 4
set nitrideEtch = 7
# pillar height...
# 230nm -> 21
# 80nm -> 9.01
set pillarHeight = 21

go athena

# define mash...
line x location=0.8             spacing=0.02
line x location=0.9             spacing=0.01
line x location=1.1             spacing=0.01
line x location=1.2             spacing=0.02

line y location=0.0 spacing=0.01
line y location=0.35 spacing=0.01

# initialise the wafer...
init silicon boron resistivity=0.75 orientation=100
# oxide grid (initial and subsequent)...
method gridinit.ox=0.005 grid.oxide=0.01 oxide.rel=0.02

# grow pad oxide...
diffuse time=50 temp=900 dryo2 pressure=1 hcl.pc=3
extract name="pad_sio2" thickness material="SiO~2" mat.occno=1 x.val=0.5

# deposit nitride...
deposit nitride thickness=0.130

# deposit SiO2...
deposit oxide thickness = 0.05

# etch oxide/nitride/oxide...
etch oxide left p1.x=1.0
etch nitride left p1.x=1.0
etch oxide left p1.x=1.0
tonyplot

# etch 230 nm pillar...
rate.etch machine=pillar2 silicon n.m  rie isotropic=0.5 dir=10.00 chem=1 div=0.1
etch machine=pillar2 time=$"pillarHeight" minutes
# strip resist...
etch photores all
tonyplot

# stress reliefe oxide...
diffuse time=$"padOxide" temp=900 dryo2 pressure=1 hcl.pc=3
extract name="pad_sio2" thickness material="SiO~2" mat.occno=1 x.val=0.85
tonyplot

# deposit nitride and etch nitride fillet...
deposit nitride thickness=$"nitrideTh" div=14
rate.etch machine=fillet2 nitride n.m  rie isotropic=1 dir=10 chem=1 div=0.1
etch machine=fillet2 time=$"nitrideEtch" minutes
tonyplot
```

```
# etch pad oxide...
etch oxide dry thick=$"pad_sio2"/10000
tonyplot

# model parameter...
material oxide visc.0=5.1 visc.E=3.48 weto2
material nitride visc.0=2e3 visc.E=2.5625

#FILOX...
oxide stress.dep=t
method viscous

# step1....
diffuse time=0.5 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness1" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO~2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO~2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO~2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO~2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO~2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO~2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO~2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO~2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO~2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO~2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO~2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO~2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO~2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO~2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO~2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO~2" mat.occno=1 y.val=0.250
struct outf=filox1.str
#tonyplot -st filox1.str

# step2....
diffuse time=0.5 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness2" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
```

```
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO^2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO^2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO^2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO^2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO^2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO^2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO^2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO^2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO^2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO^2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO^2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO^2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO^2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO^2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO^2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO^2" mat.occno=1 y.val=0.250
struct outf=filox2.str
#tonyplot -st filox2.str

# step3....
diffuse time=1 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness3" thickness material="SiO^2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO^2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO^2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO^2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO^2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO^2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO^2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO^2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO^2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO^2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO^2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO^2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO^2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO^2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO^2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO^2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO^2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO^2" mat.occno=1 y.val=0.250
struct outf=filox3.str
#tonyplot -st filox3.str

# step4....
diffuse time=1 temp=1000 weto2
```

```
# FILOX thickness...
extract name="FILOX thickness4" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO~2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO~2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO~2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO~2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO~2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO~2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO~2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO~2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO~2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO~2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO~2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO~2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO~2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO~2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO~2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO~2" mat.occno=1 y.val=0.250
struct outf=filox4.str
#tonyplot -st filox4.str

# step5....
diffuse time=1 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness5" thickness material="SiO~2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO~2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO~2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO~2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO~2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO~2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO~2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO~2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO~2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO~2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO~2" mat.occno=1 y.val=0.100
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extract name="pad_sio2Y0125" thickness material="SiO^2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO^2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO^2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO^2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO^2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO^2" mat.occno=1 y.val=0.250
struct outf=filox5.str
#tonyplot -st filox5.str

# step6....
diffuse time=1 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness6" thickness material="SiO^2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO^2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO^2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO^2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO^2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO^2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO^2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO^2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO^2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO^2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO^2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO^2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO^2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO^2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO^2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO^2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO^2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO^2" mat.occno=1 y.val=0.250
struct outf=filox6.str
#tonyplot -st filox6.str

# step7....
diffuse time=2 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness7" thickness material="SiO^2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO^2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.950
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extract name="pad_sio2X0960" thickness material="SiO^2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO^2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO^2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO^2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO^2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO^2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO^2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO^2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO^2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO^2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO^2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO^2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO^2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO^2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO^2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO^2" mat.occno=1 y.val=0.250
struct outf=filox7.str
#tonyplot -st filox7.str

#step8....
diffuse time=3 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness8" thickness material="SiO^2" mat.occno=1 x.val=1.15
# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO^2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO^2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO^2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO^2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO^2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO^2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO^2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO^2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO^2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO^2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO^2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO^2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO^2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO^2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO^2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO^2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO^2" mat.occno=1 y.val=0.250
struct outf=filox8.str
#tonyplot -st filox8.str

#step9....
diffuse time=4 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness9" thickness material="SiO^2" mat.occno=1 x.val=1.15
# vertical birds beak...
```

```
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO^2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO^2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO^2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO^2" mat.occno=1 x.val=0.930
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO^2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO^2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO^2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO^2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO^2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO^2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO^2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO^2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO^2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO^2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO^2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO^2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO^2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO^2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO^2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO^2" mat.occno=1 y.val=0.250
struct outf=filox9.str
tonyplot -st filox9.str
```

A.3 CV device/process simulations - calibration

See section 5.2.3 for details.

```
# v d kunz
# 06/01
# directory:
#..students/vdk99r/thesis/caps/adjust/topcap4nm.in
#################################################################################
# comment:
#       - this is the planar control device for edjustement of the cv's....
# - silicon/oxide/polysilicon/metal
#################################################################################
# variables...
# for gate oxide deposition...
#set oxThick=0.0048
# oxidation time for gate oxide...
# 4.8nm -> 50
# 3.9nm -> 33
set oxThick=33
# fixed charge (shifts the threshold voltage to more negative values) max at 5e12...
# good agreement with 7e10
set fixedCharge=0
# frequency...
# 1MHz -> 1e6
set frequency=1e6
```

```
# let's start...
go athena
# mesh def...
# for half of the structure only...

# define the mesh...
line x location=0.0 spacing=0.25
line x location=1.0 spacing=0.25

line y location=0.0             spacing=0.01
line y location=2.0             spacing=0.1

# define the wafer...
initialize silicon boron resistivity=0.75 orientation=100 two.d

# gate oxidation...
#deposit oxide thickness=$"oxThick"
diffuse time=$"oxThick" temp=800 dryo2 pressure=1
extract name="gate_sio2" thickness material="SiO~2" mat.occno=1 x.val=0.5

extract name = "top_sio2" thickness material="SiO~2" mat.occno=1 x.val=0.5

# deposit some polysi...
deposit polysilicon thick=0.2 phosphorus conc=5.0e18 divisions=1

# metal deposition...
deposit aluminum thickness=0.2

# define the electrical contact ...
electrode name=gate x=0.5 y=-0.3
electrode name=substrate backside

# threshold voltage...
extract name="thresholdVt" 1dvt ntype x.val=0.5 datafile="thresh.dat"

struct outfile=cap.str
tonyplot -st cap.str

#############################################################################
go atlas
#############################################################################
mesh infile=cap.str

interface qf=$"fixedCharge"

# models and methods...
#models mos print
models cvt consrh fermi

method newton carriers=2

# hf...
solve init
solve prev
#ramp up the gate voltage first...
solve vgate=0.0 vstep=0.25 vfinal=4.0 name=gate
log outf=cap_hf.log master
solve vstep=-0.1 vfinal=-4.0 name=gate ac freq=$"frequency" aname=gate
log outfile=tmp

tonyplot -st cap_hf.log -set hf.set
```

```
# lf...
#solve init
#solve prev
#ramp up the gate voltage first...
#solve vgate=0.0 vstep=0.25 vfinal=4.0 name=gate
#log outf=cap_lf.log master
#solve vstep=-0.1 vfinal=-4.0 name=gate ac freq=1e-4 aname=gate
#log outfile=tmp

# cv...
#tonyplot -overlay cap_hf.log cap_lf.log  -set hf.set
# conductivity
#tonyplot cap_hf.log  -set conduct.set
quit
```

A.4 CV device/process simulations - control

See section 5.4 for details.

```
# v d kunz
# 06/01
# directory:
#..students/vdk99r/thesis/caps/control/pillcap4nm.in
##############################################################################
# comment:
#       - this is the pillar device....
# - silicon/oxide/polysilicon/metal
##############################################################################
# variables...
set padOxide = 50
# etch time for pillar etch...
# 305nm -> 27
# 400nm -> 37
set pillarHeight = 37
# fixed charge (shifts the threshold voltage to more negative values) max at 5e12...
# good agreement with 7e10
set fixedCharge=7e10

# let's start...
go athena
# mesh def...
# for half of the structure only...
# define the mesh...
line x location=0.0 spacing=0.2
line x location=1.4             spacing=0.02
line x location=1.5             spacing=0.02
line x location=1.6             spacing=0.02
line x location=2.25 spacing=0.2

# draw linear scale until...
line y location=0.0 spacing=0.02
line y location=0.45 spacing=0.02
line y location=2.5 spacing=0.2

# define the wafer...
# initialize mesh(p-type substrate)...
initialize silicon boron resistivity=0.75 orientation=100 two.d
```

```
# first the photoresist...
deposit photores thick=0.1 div=5
etch photores left p1.x=1.500
# pillar etch...
rate.etch machine=pillar2 silicon n.m  rie isotropic=0.5 dir=10.00 chem=1 div=0.1
etch machine=pillar2 time=$"pillarHeight" minutes
# strip resist...
etch photores all
# etch off top peak (top 20nm only)...
etch silicon above p1.y=0.020

# stress relieve oxide...
diffuse time=$"padOxide" temp=900 dryo2 pressure=1 hcl.pc=3
extract name="pad_sio2" thickness material="SiO^2" mat.occno=1 x.val=1.15
etch oxide all

# gate oxidation...
diffuse time=50 temp=800 dryo2 pressure=1
extract name="gate_sio2_lat" thickness material="SiO^2" mat.occno=1 x.val=0.1
extract name="gate_sio2_vert" thickness material="SiO^2" mat.occno=1 y.val=0.2

# deposit some polysi...
deposit polysilicon thick=0.2 phosphorus conc=5.0e18 divisions=2

# deposit alu...
deposit aluminum thickness=0.3 division=5

# mirror...
#structure mirror right

# define the electrical contact ...
electrode name=gate x=0.5 y=-0.1
electrode name=substrate backside

# threshold voltage...
extract name="thresholdVt" 1dvt ntype x.val=2.0 datafile="thresh.dat"

struct outfile=cap.str
tonyplot -st cap.str

##############################################################################
go atlas
##############################################################################
mesh infile=cap.str

interface qf=$"fixedCharge"

# models and methods...
models mos srh print
method newton carriers=2

# hf...
solve init
solve prev
#ramp up the gate voltage first...
solve vgate=0.0 vstep=0.25 vfinal=4.0 name=gate
log outf=cap_hf.log master
solve vstep=-0.1 vfinal=-4.0 name=gate ac freq=1e6 aname=gate
log outfile=tmp
tonyplot cap_hf.log -set hf.set
```

```
# lf...
#solve init
#solve prev
#ramp up the gate voltage first...
#solve vgate=0.0 vstep=0.25 vfinal=4.0 name=gate
#log outf=cap_lf.log master
#solve vstep=-0.1 vfinal=-4.0 name=gate ac freq=1e-4 aname=gate
#log outfile=tmp

# cv...
#tonyplot -overlay cap_hf.log cap_lf.log  -set hf.set
# conductivity
#tonyplot cap_hf.log  -set conduct.set
```

A.5 CV device/process simulations - nitride top

See section 5.4 for details.

```
# v d kunz
# 06/01
# directory:
#..students/vdk99r/thesis/caps/nitridetop/pillinscap4nm.in
##############################################################################
# comment:
#       - this is the control device....
# - silicon/oxide/polysilicon
##############################################################################
# variables...
set padOxide = 50
set nitrideThick = 0.150
set padOxide2 = 0.063
# etch time for pillar etch...
# 305nm -> 27
# 320nm -> 28
set pillarHeight = 28
# fixed charge (shifts the threshold voltage to more negative values) max at 5e12...
# good agreement with 7e10
set fixedCharge=7e10

# let's start...
go athena
# mesh def...
# for half of the structure only...
# define the mesh...
line x location=0.0 spacing=0.2
line x location=1.2             spacing=0.02
line x location=1.5             spacing=0.02
line x location=1.6             spacing=0.2
line x location=2.2 spacing=0.2

# draw linear scale until...
line y location=0.0 spacing=0.02
line y location=0.38 spacing=0.02
line y location=2.5 spacing=0.1
```

```
# define the wafer...
# initialize mesh(p-type substrate)...
initialize silicon boron resistivity=0.75 orientation=100 two.d

# grow pad oxide...
diffuse time=50 temp=900 dryo2 pressure=1 hcl.pc=3
extract name="pad_sio2" thickness material="SiO^2" mat.occno=1 x.val=0.5

# deposit nitride...
deposit nitride thickness=$"nitrideThick"

# deposit SiO2...
deposit oxide thickness = $"padOxide2"

# etch oxide/nitride/oxide...
etch oxide left p1.x=1.5
etch nitride left p1.x=1.5
etch oxide left p1.x=1.5
# pillar etch...
rate.etch machine=pillar2 silicon n.m  rie isotropic=0.5 dir=10.00 chem=1 div=0.1
etch machine=pillar2 time=$"pillarHeight" minutes

tonyplot

# stress reliefe oxide...
diffuse time=$"padOxide" temp=900 dryo2 pressure=1 hcl.pc=3
extract name="pad_sio2" thickness material="SiO^2" mat.occno=1 x.val=1.15
etch oxide left p1.x=1.52
etch nitride left p1.x=1.52
tonyplot

# gate oxidation...
diffuse time=50 temp=800 dryo2 pressure=1
extract name="gate_sio2_lat" thickness material="SiO^2" mat.occno=1 x.val=0.1
extract name="gate_sio2_vert" thickness material="SiO^2" mat.occno=1 y.val=0.2

# deposit some polysi...
deposit polysilicon thick=0.2 phosphorus conc=5.0e18 divisions=2

# deposi t aluminum...
deposit aluminum thickness=0.3 division=5

# mirror...
#structure mirror right

# define the electrical contact ...
electrode name=gate x=0.5 y=-0.1
electrode name=substrate backside

# threshold voltage...
extract name="thresholdVt" 1dvt ntype x.val=2.0 datafile="thresh.dat"

struct outfile=cap.str
tonyplot -st cap.str

##############################################################################
go atlas
##############################################################################
mesh infile=cap.str

interface qf=$"fixedCharge"
```

```
# models and methods...
models mos srh print
method newton carriers=2

# hf...
solve init
solve prev
#ramp up the gate voltage first...
solve vgate=0.0 vstep=0.25 vfinal=4.0 name=gate
log outf=cap_hf.log master
solve vstep=-0.1 vfinal=-4.0 name=gate ac freq=1e6 aname=gate
log outfile=tmp
tonyplot -st cap_hf.log -set hf.set


# lf...
#solve init
#solve prev
#ramp up the gate voltage first...
#solve vgate=0.0 vstep=0.25 vfinal=4.0 name=gate
#log outf=cap_lf.log master
#solve vstep=-0.1 vfinal=-4.0 name=gate ac freq=1e-4 aname=gate
#log outfile=tmp

# cv...
#tonyplot -overlay cap_hf.log cap_lf.log  -set hf.set
# conductivity
#tonyplot cap_hf.log  -set conduct.set
quit
```

A.6 CV device/process simulations - FILOX

See section 5.4 for details.

```
# v d kunz
# 06/01
# directory:
#..students/vdk99r/thesis/caps/filox/pillinscap4nm.in
##############################################################################
# comment:
#       - this is the control device....
# - silicon/oxide/top insulator/filox/polysilicon/al
##############################################################################
# variables...
set padOxide = 50
set nitrideThick = 0.146
set padOxide2 = 0.064
# etch time for pillar etch...
# 305nm -> 27
# 320nm -> 28
# 460nm -> 40
set pillarHeight = 40

# fixed charge (shifts the threshold voltage to more negative values) max at 5e12...
# good agreement with 7e10
set fixedCharge=7e10
```

```
# let's start...
go athena
# mesh def...
# for half of the structure only...
# define the mesh...
line x location=0.0 spacing=0.2
line x location=1.2             spacing=0.02
line x location=1.5             spacing=0.02
line x location=1.6             spacing=0.02
line x location=2.25 spacing=0.2

# draw linear scale until...
line y location=0.0 spacing=0.02
line y location=0.5 spacing=0.02
line y location=2.0 spacing=0.1

# define the wafer...
# initialise mesh (p-type substrate)...
initialize silicon boron resistivity=0.75 orientation=100 two.d

# grow pad oxide...
diffuse time=50 temp=900 dryo2 pressure=1 hcl.pc=3
extract name="pad_sio2" thickness material="SiO~2" mat.occno=1 x.val=0.5

# deposit nitride...
deposit nitride thickness = $"nitrideThick"

# deposit SiO2...
deposit oxide thickness = $"padOxide2"

# etch oxide/nitride/oxide...
etch oxide left p1.x=1.5
etch nitride left p1.x=1.5
etch oxide left p1.x=1.5

# pillar etch...
rate.etch machine=pillar2 silicon n.m  rie isotropic=0.5 dir=10.00 chem=1 div=0.1
etch machine=pillar2 time=$"pillarHeight" minutes

# stress reliefe oxide...
diffuse time=$"padOxide" temp=900 dryo2 pressure=1 hcl.pc=3
extract name="pad_sio2" thickness material="SiO~2" mat.occno=1 x.val=1.15

# deposit nitride and etch nitride fillet...
deposit nitride thickness=0.07 div=14
rate.etch machine=fillet2 nitride n.m  rie isotropic=1 dir=10 chem=1 div=0.1
etch machine=fillet2 time=7 minutes

# etch off pad oxide...
etch dry oxide thick = $"pad_sio2"/10000

# model parameter...
material oxide visc.0=5.1 visc.E=3.48 weto2
material nitride visc.0=2e3 visc.E=2.5625
#FILOX...
oxide stress.dep=t
method viscous
diffuse time=10.5 temp=1000 weto2
# FILOX thickness...
extract name="FILOX thickness" thickness material="SiO~2" mat.occno=1 x.val=0.1
extract name="FILOX thickness" thickness material="SiO~2" mat.occno=1 y.val=0.15
```

```
etch nitride left p1.x=1.5

rate.etch machine=wetEtcher wet.etch oxide n.m isotropic=1.0
etch machine=wetEtcher time=20 min


extract name="FILOX thickness after wet etch" thickness material="SiO~2" mat.occno=1 x.val=0.1
extract name="FILOX thickness after wet etch" thickness material="SiO~2" mat.occno=1 y.val=0.15

tonyplot

# gate oxidation...
diffuse time=50 temp=800 dryo2 pressure=1
extract name="gate_sio2" thickness material="SiO~2" mat.occno=1 x.val

extract name = "Filox thickness after gate oxidation" thickness material="SiO~2" mat.occno=1 x.val=0.1
extract name = "Filox thickness after gate oxidation" thickness material="SiO~2" mat.occno=1 y.val=0.15

# deposit some polysi...
deposit polysilicon thick=0.2 phosphorus conc=5.0e18 divisions=5

# deposit aluminum...
deposit aluminum thickness=0.3 division=5

# mirror...
#structure mirror right

# define the electrical contact ...
electrode name=gate x=0.5 y=-0.1
electrode name=substrate backside

# threshold voltage...
extract name="thresholdVt" 1dvt ntype x.val=2.0 datafile="thresh.dat"

struct outfile=cap.str
tonyplot -st cap.str

###############################################################################
go atlas
###############################################################################
mesh infile=cap.str

interface qf=$"fixedCharge"

# models and methods...
models mos srh print
method newton carriers=2

# hf...
solve init
solve prev
#ramp up the gate voltage first...
solve vgate=0.0 vstep=0.25 vfinal=4.0 name=gate
log outf=cap_hf.log master
solve vstep=-0.1 vfinal=-4.0 name=gate ac freq=1e6 aname=gate
log outfile=tmp
tonyplot cap_hf.log -set hf.set

# lf...
#solve init
#solve prev
```

```
#ramp up the gate voltage first...
#solve vgate=0.0 vstep=0.25 vfinal=4.0 name=gate
#log outf=cap_lf.log master
#solve vstep=-0.1 vfinal=-4.0 name=gate ac freq=1e-4 aname=gate
#log outfile=tmp

# cv...
#tonyplot -overlay cap_hf.log cap_lf.log  -set hf.set
# conductivity
#tonyplot cap_hf.log  -set conduct.set
quit
```

A.7 Nitride and pad oxide etch for bird's beak extraction

See section 6.5.1 for details.

```
# v d kunz
# 08/04/2003
# directory:
#..students/vdk99r/thesis/filox/padetch.in
##############################################################################
# simulation:
# - load in file
# - remove pad oxide
# - list oxide thickness
# - done
##############################################################################

# let's start...
go athena

# init...
initialize infile="filox6_20_130.str"

tonyplot filox6_20_130.str

# remove nitride fillet...
strip nitride
extract name="FILOX thickness before wet etch" thickness material="SiO~2" mat.occno=1 x.val=1.199
# remove 20nm pad oxide...
rate.etch machine=wetEtcher wet.etch oxide n.m isotropic=1.0
etch machine=wetEtcher time=20 min
extract name="FILOX thickness after wet etch" thickness material="SiO~2" mat.occno=1 x.val=1.199

tonyplot

# vertical birds beak...
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.850
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.860
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.870
extract name="pad_sio2X0940" thickness material="SiO~2" mat.occno=1 x.val=0.880
extract name="pad_sio2X0950" thickness material="SiO~2" mat.occno=1 x.val=0.890
extract name="pad_sio2X0900" thickness material="SiO~2" mat.occno=1 x.val=0.900
extract name="pad_sio2X0910" thickness material="SiO~2" mat.occno=1 x.val=0.910
extract name="pad_sio2X0920" thickness material="SiO~2" mat.occno=1 x.val=0.920
extract name="pad_sio2X0930" thickness material="SiO~2" mat.occno=1 x.val=0.930
```

```
extract name="pad_sio2X0940" thickness material="SiO^2" mat.occno=1 x.val=0.940
extract name="pad_sio2X0950" thickness material="SiO^2" mat.occno=1 x.val=0.950
extract name="pad_sio2X0960" thickness material="SiO^2" mat.occno=1 x.val=0.960
extract name="pad_sio2X0970" thickness material="SiO^2" mat.occno=1 x.val=0.970
extract name="pad_sio2X0980" thickness material="SiO^2" mat.occno=1 x.val=0.980
extract name="pad_sio2X0990" thickness material="SiO^2" mat.occno=1 x.val=0.990
extract name="pad_sio2X1000" thickness material="SiO^2" mat.occno=1 x.val=1.000
# horizontal bird's beak...
extract name="pad_sio2Y0000" thickness material="SiO^2" mat.occno=1 y.val=0.000
extract name="pad_sio2Y0025" thickness material="SiO^2" mat.occno=1 y.val=0.025
extract name="pad_sio2Y0050" thickness material="SiO^2" mat.occno=1 y.val=0.050
extract name="pad_sio2Y0075" thickness material="SiO^2" mat.occno=1 y.val=0.075
extract name="pad_sio2Y0100" thickness material="SiO^2" mat.occno=1 y.val=0.100
extract name="pad_sio2Y0125" thickness material="SiO^2" mat.occno=1 y.val=0.125
extract name="pad_sio2Y0150" thickness material="SiO^2" mat.occno=1 y.val=0.150
extract name="pad_sio2Y0175" thickness material="SiO^2" mat.occno=1 y.val=0.175
extract name="pad_sio2Y0200" thickness material="SiO^2" mat.occno=1 y.val=0.200
extract name="pad_sio2Y0225" thickness material="SiO^2" mat.occno=1 y.val=0.225
extract name="pad_sio2Y0250" thickness material="SiO^2" mat.occno=1 y.val=0.250

# end
```

A.8 Vertical MOSFET device/process simulations

See section 6.5.5 for details.

```
# file: vmos.in
###############################################################################
############## let's do some process sims using ATHENA... ####################
###############################################################################
# GAI structure
# adjastable gate oxide thickness,
# drain voltage
# no FILOX

# some variables...
# pillar height...
set pillHeight = 0.310
set nitrideThick = 0.070
# 2.98nm gate oxide -> 8 min oxidation time
set gateOx = 5.25
# set max ramp votage for output characteristics...
set maxVDrain = 3.0

go athena

# define mesh...
line x loc=0.0 spac=0.100
line x loc=0.9 spac=0.010
line x loc=1.1 spac=0.010
line x loc=2.0 spac=0.100

line y loc=0.0 spac=0.005
line y loc=0.36 spac=0.005
line y loc=1.0 spac=0.100

# start off material...
```

```
# p-type wafer...
# start of with a boron doped wafer (17-33Ohm*cm).
initialize silicon orientation=100 boron resistivity=25 space.mul=2
# measure resistivity....
extract name="sheetRsubstrate" sheet.res material="silicon" mat.occno=1 \
x.val=0.500 region.occno=1 datafile="data.dat"

# p-well implant...
implant boron dose=5.0e14 energy=50 pears
# drive in...
diffuse time=10 temp=1100 dryo2 press=1.00
diffus time=30 temp=1100 nitro press=1.00
extract name="sheetRsubstrate after B implant" sheet.res material="silicon" mat.occno=1 \
x.val=0.500 region.occno=1 datafile="data.dat"

# strip all oxide...
strip oxide

# etch the pillar...
# left side...
etch silicon start x=0.0 y=0.0
etch continue x=1.0 y=0.0
etch continue x=1.0 y=$"pillHeight"
etch done x=0.0 y=$"pillHeight"

# measure resistivity....
extract name="sheetRbottom" sheet.res material="silicon" mat.occno=1 \
x.val=0.500 region.occno=1 datafile="data.dat"
extract name="sheetRtop" sheet.res material="silicon" mat.occno=1 \
x.val=1.500 region.occno=1 datafile="data.dat"
#tonyplot

# pad oxide...
diffuse time=50 temp=900 dryo2 press=1.00 hcl.pc=3
extract name="pad_sio2" thickness material="sio^2" mat.occno=1 x.val=0.1 junc.occno=1 datafile="data.dat"
#tonyplot -set dopec.set

# nitride spacers...
depo nitride thick=$"nitrideThick" divisions=8
etch nitride dry thick=$"nitrideThick"
# etch oxide (watch out Angstroem -> um cconversion)...
etch oxide dry thick=$"pad_sio2"/10000
#tonyplot -set dopec.set

# n-type implant...
implant arsenic dose=3.0e15 energy=50 tilt= 7 pearson
implant arsenic dose=3.0e15 energy=50 tilt= 0 pearson

#tonyplot -set dopec.set
# get rid of the nitride fillets...
strip nitride
strip oxide

# gate oxide...
#method gridinit.ox=0.002 grid.oxide=0.002
diffuse time=$"gateOx" temp=800 dryo2 press=1.00
#deposit oxide thickness=0.003
extract name="gateoxY" thickness oxide mat.occno=1 y.val=0.2
extract name="gateoxX" thickness oxide mat.occno=1 x.val=0.1
#tonyplot
```

```
# polysilicon gate fillets...
depo polysi arsenic thick=0.200  conc=5.0e+19 division=8
etch polysi dry thick=0.200

# Rapid Thermal Aneal...
method fermi compress
diffuse time=80/60 temp=1050  nitro press=1.0

# pattern s/d contact metal...
# bottom oxide removal...
etch oxide left x=0.5
# top oxide removal...
etch oxide right x=1.5
# contact...
deposit alumin thick=0.03 division=2

etch alumin start x=0.5 y=-0.4
etch continue x=1.5 y=-0.4
etch continue x=1.5 y=0.5
etch done x=0.5 y=0.5

###############################################################################
# Extract design parameters...
###############################################################################
# gate oxide thickness...
extract name="gateox" thickness oxide mat.occno=1 x.val=0.6 datafile="data.dat"
# extract final S/D Xj...
extract name="junction depth at pillar top" xj silicon mat.occno=1 x.val=0.100 junc.occno=1 datafile="data.dat"
extract name="junction depth at pillar bottom" xj silicon mat.occno=1 x.val=1.500 junc.occno=1 datafile="data.da

# extract the N++ regions sheet resistance...
extract name="n++ sheet resistance" sheet.res material="silicon" mat.occno=1 \
x.val=0.100 region.occno=1 datafile="data.dat"

# extract the sheet res under the spacer, of the implant region...
extract name="implant sheet resistance" sheet.res material="silicon" mat.occno=1 \
x.val=0.935 region.occno=1 datafile="data.dat"

# extract the surface concentration in the channel...
extract name="channel surface concentration" surf.conc impurity="Net Doping" \
material="Silicon" mat.occno=1 y.val=0.1 datafile="data.dat"

# extract a curve of resistance versus bias....
extract start material="polysilicon" mat.occno=1 bias=0.0 bias.step=0.2 bias.stop=$"maxVDrain" y.val=0.2
extract done name="sheet resistance versus bias at y=0.1" curve(bias,1dn.sheet.res \
material="silicon" mat.occno=1 region.occno=1) outfile="extract.dat"
# ...and plot...
#tonyplot extract.dat

# extract the long chan Vt...
extract name="1 dimensional threshold voltage (Vsubstrate=0.0V)" 1dvt ntype vb=0.0 \
qss=1e10 y.val=0.1 datafile="data.dat"

###############################################################################

# hmmm, a few electrodes could make things easier...
# drain on top...
electrode name=gate     x=0.900 y=0.20
electrode name=source   x=0.1
electrode name=drain    x=2.0 y=0.01
```

```
# source on top...
#electrode name=gate     x=0.900 y=0.20
#electrode name=source x=2.0 y=0.01
#electrode name=drain    x=0.1

# for both...
electrode name=substrate backside
structure outfile=mos.str

# plot the structure...
tonyplot mos.str -set mos.set

################################################################################
############## let's do some device sims using ATLAS... ########################
################################################################################
go atlas

# set workfunction of gate...
contact name=gate n.poly

# select models
# the following models are used...
# models conmob srh auger bgn fldmob print
# conmob -> concentration dependent mobility model
# srh -> shockley-reed hall recombination using fixed lifetimes
# bgn -> band gap narrowing
# fldmob -> lateral field dependent model
models yamaguchi srh fermi

# solving method...
method newton trap

log outf=tmp
# set all voltages to zero...
solve initial
# ramp gate voltage...
solve Vdrain=0.025
log outf=log0.log master
solve V1=0.0 electrode=1 Vstep=0.05 Vfinal=0.5
solve V1=0.5 electrode=1 Vstep=0.1 Vfinal=1.0
solve V1=1.0 electrode=1 Vstep=0.1 Vfinal=$"maxVDrain"
log outf=tmp
#tonyplot -set elec_conc.set

# set all voltages to zero...
solve initial
# ramp gate voltage...
solve Vdrain=0.01 electrode=3 Vstep=0.2 Vfinal=1.0
log outf=log1.log master
solve V1=0.0 electrode=1 Vstep=0.05 Vfinal=0.5
solve V1=0.5 electrode=1 Vstep=0.1 Vfinal=1.0
solve V1=1.0 electrode=1 Vstep=0.1 Vfinal=$"maxVDrain"
log outf=tmp

# plot resultant linear ID over linear VG threshold voltage curve
tonyplot -overlay log0.log log1.log -set vt.set
tonyplot -overlay log0.log log1.log -set st.set

################################################################################
# the next view lines plot ID versus VDS for three different VGS voltages...
################################################################################
```

```
# set all voltages to zero...
solve initial
# ramp drain voltage...
set tempVdrain = 2.0
solve V1=0.0 electrode=1 Vstep=0.2 Vfinal=$"tempVdrain"
log outf=ivdrain_log0.log master
solve Vdrain=0.0 electrode=3 Vstep=0.05 Vfinal=0.5
solve Vdrain=0.5 electrode=3 Vstep=0.1 Vfinal=1.0
solve Vdrain=1.0 electrode=3 Vstep=0.2 Vfinal=$"maxVDrain"
log outf=tmp

# set all voltages to zero...
solve initial
# ramp drain voltage...
set tempVdrain = 2.5
solve V1=0.0 electrode=1 Vstep=0.2 Vfinal=$"tempVdrain"
log outf=ivdrain_log1.log master
solve Vdrain=0.0 electrode=3 Vstep=0.05 Vfinal=0.5
solve Vdrain=0.5 electrode=3 Vstep=0.1 Vfinal=1.0
solve Vdrain=1.0 electrode=3 Vstep=0.2 Vfinal=$"maxVDrain"
log outf=tmp

# set all voltages to zero...
solve initial
# ramp drain voltage...
set tempVdrain = 3.0
solve V1=0.0 electrode=1 Vstep=0.2 Vfinal=$"tempVdrain"
log outf=ivdrain_log2.log master
solve Vdrain=0.0 electrode=3 Vstep=0.05 Vfinal=0.5
solve Vdrain=0.5 electrode=3 Vstep=0.1 Vfinal=1.0
solve Vdrain=1.0 electrode=3 Vstep=0.2 Vfinal=$"maxVDrain"
log outf=tmp

tonyplot -overlay ivdrain_log0.log ivdrain_log1.log ivdrain_log2.log -set iv.set

# that's it...
quit
```

Appendix B

Mask description

B.1 Vertical capacitors

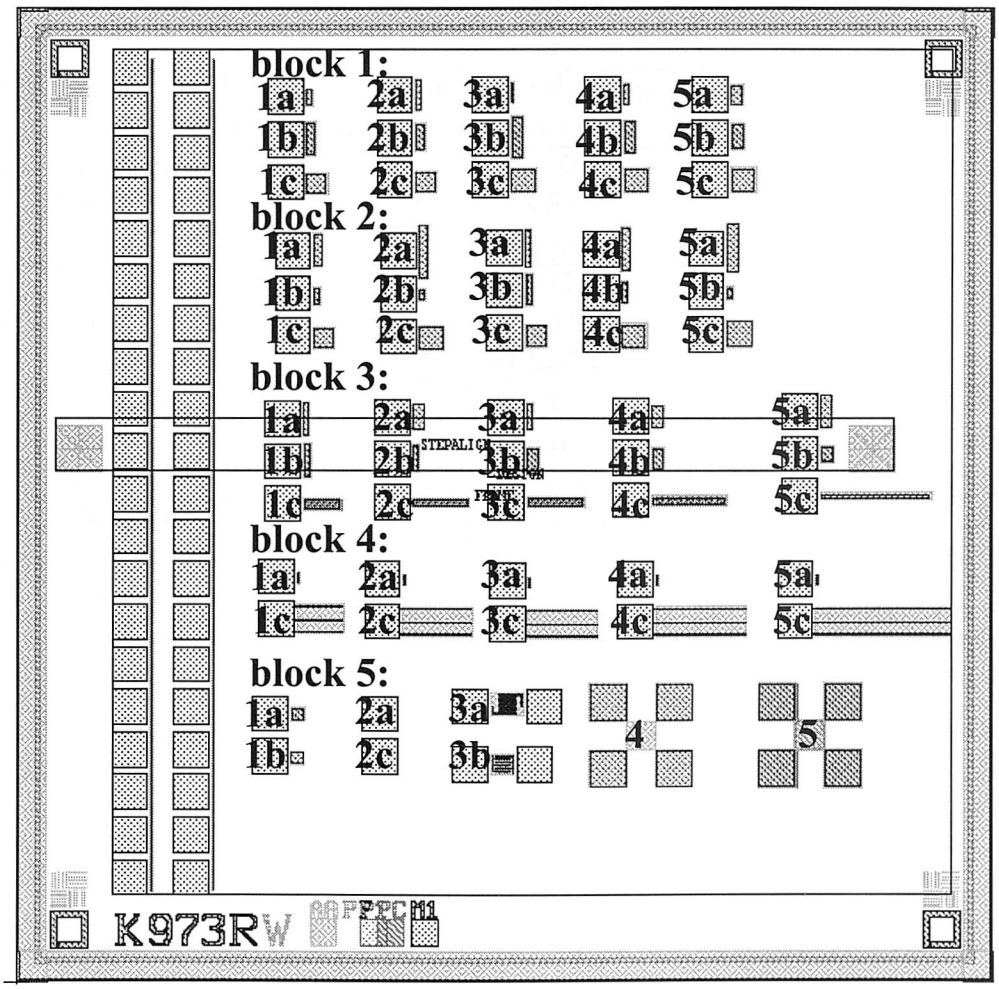

Figure B.1: Layout of one cell of the fabricated vertical capacitors. The device dimensions are listed in table B.1.

block 1	**type**	**dimensions**[μm] top/bottom	metal area[μm] $x_a \times x_b$	**description**
1a	bottom	-	20×53.8	capacitor on trench bottom
1b	top	-	30×108.66	capacitor on pillar top
1c	all	1.5/1.5	65.9×65.9	convex capacitor
2a	bottom	-	20×102.3	capacitor on trench bottom
2b	top	-	30×85.3	capacitor on pillar top
2c	all	1.5/3.0	67.8×67.8	convex capacitor
3a	bottom	-	10×66.8	capacitor on trench bottom
3b	top	-	40×133.7	capacitor on pillar top
3c	all	3.0/1.5	77.6×77.6	convex capacitor
4a	bottom	-	20×72.4	capacitor on trench bottom
4b	top	-	40×108.7	capacitor on pillar top
4c	all	3.0/3.0	76.1×76.1	convex capacitor
5a	bottom	-	40×66.8	capacitor on trench bottom
5b	top	-	40×83.5	capacitor on pillar top
5c	all	3.0/6.0	77.6×77.6	convex capacitor

block 2	**type**	**dimensions**[μm] top/bottom	metal area[μm] $x_a \times x_b$	**description**
1a	bottom	-	30×108.6	capacitor on trench bottom
1b	top	-	20×54.5	capacitor on pillar top
1c	all	1.5/1.5	65.9×65.9	concave capacitor
2a	bottom	-	30×178.3	capacitor on trench bottom
2b	top	-	20×33.45	capacitor on pillar top
2c	all	1.5/3.0	77.6×77.6	concave capacitor
3a	bottom	-	20×127.5	capacitor on trench bottom
3b	top	-	20×102.5	capacitor on pillar top
3c	all	3.0/1.5	67.8×67.8	concave capacitor
4a	bottom	-	30×144.6	capacitor on trench bottom
4b	top	-	20×72.5	capacitor on pillar top
4c	all	3.0/3.0	76.1×76.1	concave capacitor
5a	bottom	-	40×158	capacitor on trench bottom
5b	top	-	20×39.5	capacitor on pillar top
5c	all	3.0/6.0	84.3×84.3	concave capacitor

block 3	**type**	**dimensions**[μm] top/bottom	metal area[μm] $x_a \times x_b$	**description**
1a	bottom	-	20×108.5	capacitor on trench bottom
1b	top	-	20×108.65	capacitor on pillar top
1c	all	1.5/1.5	120×36.2	pillar capacitor
2a	bottom	-	40×87	capacitor on trench bottom
2b	top	-	20×86.9	capacitor on pillar top
2c	all	1.5/3.0	180×29	pillar capacitor
3a	bottom	-	20×87	capacitor on trench bottom
3b	top	-	40×86.9	capacitor on pillar top
3c	all	3.0/1.5	180×29	pillar capacitor
4a	bottom	-	40×72.2	capacitor on trench bottom
4b	top	-	40×72.2	capacitor on pillar top
4c	all	3.0/3.0	240×24.1	pillar capacitor
5a	bottom	-	40×108.7	capacitor on trench bottom
5b	top	-	40×54.3	capacitor on pillar top
5c	all	3.0/6.0	360×18.1	pillar capacitor

block 4	**type**	**dimensions**[μm] top/bottom	metal area[μm] $x_a \times x_b$	**description**
1a	bottom	-	10×34.7	capacitor on trench bottom
2a	bottom	-	10×34.7	capacitor on trench bottom
3a	bottom	-	10×34.7	capacitor on trench bottom
4a	bottom	-	10×34.7	capacitor on trench bottom
5a	bottom	-	10×34.7	capacitor on trench bottom

block 4	**type**	**dimensions**[μm] top/bottom	**nr. of pillars**	pillar length[μm]	**description**
1c	all	1.5/1.5	50	94.5	fillet capacitor
2c	all	1.5/3.0	50	94.5	fillet capacitor
3c	all	3.0/1.5	50	96	fillet capacitor
4c	all	3.0/3.0	50	96	fillet capacitor
5c	all	3.0/6.0	50	96	fillet capacitor

block 5	**type**	metal area[μm] $x_a \times x_b$	**description**
1a	top	41.6×41.6	capacitor on pillar top
1b	bottom	41.6×41.6	capacitor on trench bottom
2a	top	120×120	pad contact to pillar top
2b	bottom	120×120	pad contact to trench bottom
3a	test	-	test structure for metal step coverage
3b	test	-	test structure for metal separation

Table B.1: Layout description of fabricated vertical capacitors

B.2 Vertical MOSFETs

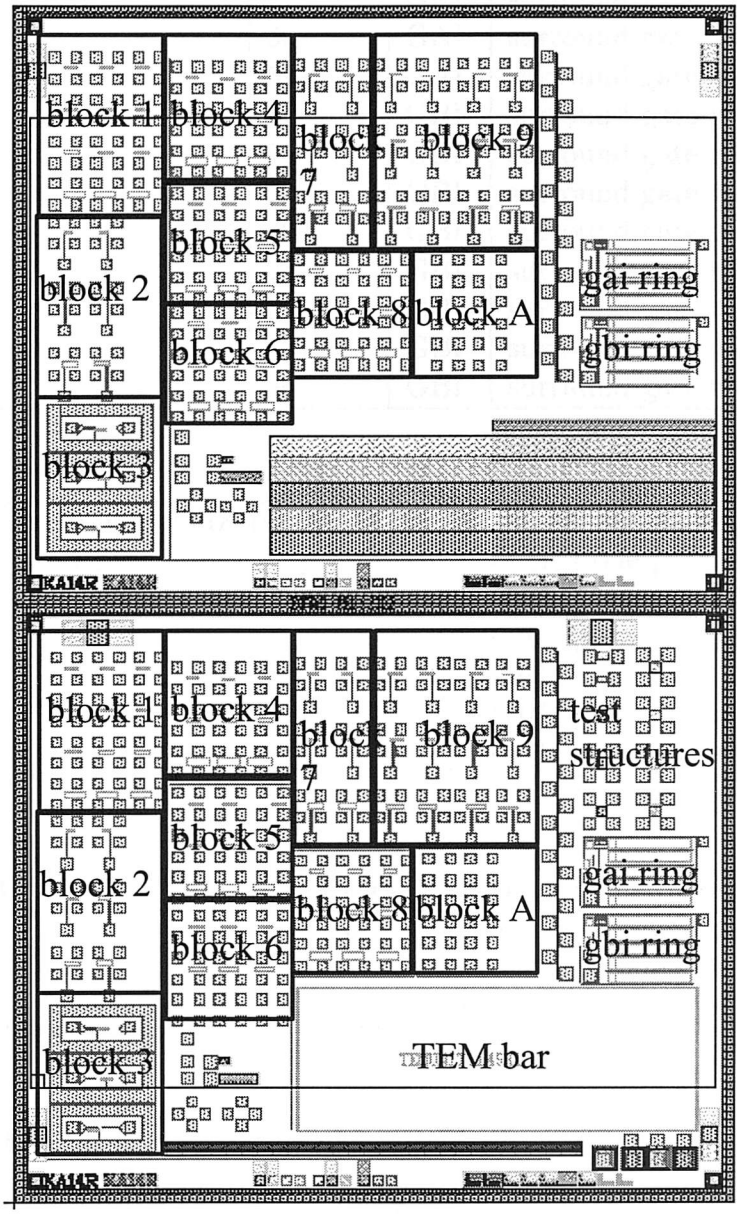

Figure B.2: Layout of two cells of the fabricated vertical MOS devices. The device dimensions are listed in table B.2.

block 1	feature size[μm]	W[μm]	type	description
1	1.5	27	GAI	surround gate with 1μm fin
2	1.5	27	GAI	surround gate with 1.5μm fin
3	2.0	36	GAI	surround gate with 2μm fin
4	2.0	60	GAI	surround gate with 1.5μm fin
5	1.5	27	GBI	surround gate with 1μm fin
6	1.5	27	GBI	surround gate with 1.5μm fin
7	2.0	36	GBI	surround gate with 2μm fin
8	2.0	60	GBI	surround gate with 1.5μm fin
9	1.5	24	GBI	surround gate with 1μm fin
10	1.5	24	GBI	surround gate with 1.5μm fin
11	2.0	32	GBI	surround gate with 2μm fin
12	2.0	56	GBI	surround gate with 1.5μm fin

block 2	feature size[μm]	W[μm]	type	description
1	1.5	13.5	GAI	one pillar NAND
2	2.0	18	GAI	one pillar NAND
3	4.0	30	GAI	one pillar NAND
4	1.5	60	GBI	one pillar NAND
5	2.0	18	GBI	one pillar NAND
6	4.0	30	GBI	one pillar NAND

block 3	feature size[μm]	W[μm]	type	description
1	1.5	24	GAI	surround gate for RF
2	1.5	24	GBI	surround gate for RF
3	1.5	22.5	GBI	surround gate for RF

block 4	feature size[μm]	W[μm]	type	description
1	1.5	24	GAI	minimum dimension surround gate
2	2.0	32	GAI	minimum dimension surround gate
3	4.0	52	GAI	minimum dimension surround gate
4	1.5	24	GBI	minimum dimension surround gate
5	2.0	32	GBI	minimum dimension surround gate
6	4.0	52	GBI	minimum dimension surround gate
7	1.5	22.5	GBI	minimum dimension surround gate
8	2.0	30	GBI	minimum dimension surround gate
9	4.0	48	GBI	minimum dimension surround gate

block 5	feature size[μm]	W[μm]	type	description
1	1.5	9	GAI	double gate
2	2.0	12	GAI	double gate
3	4.0	20	GAI	double gate
4	1.5	9	GBI	double gate
5	2.0	12	GBI	double gate
6	4.0	20	GBI	double gate
7	1.5	3	GBI	double gate
8	2.0	8	GBI	double gate
9	4.0	12	GBI	double gate

block 6	feature size[μm]	W[μm]	type	description
1	1.5	4.5	GAI	single gate
2	2.0	6	GAI	single gate
3	4.0	10	GAI	single gate
4	1.5	4.5	GAI	single gate
5	2.0	6	GAI	single gate
6	4.0	10	GBI	single gate
7	1.5	3	GBI	single gate
8	2.0	6	GAI	single gate
9	4.0	6	GBI	single gate

block 7	feature size[μm]	W[μm]	type	description
1	1.5	2×4.5	GAI	NOR gate
2	2.0	2×6	GAI	NOR gate
3	4.0	2×10	GAI	NOR gate
4	1.5	2×4.5	GBI	NOR gate
5	2.0	2×6	GBI	NOR gate
6	4.0	2×10	GBI	NOR gate

block 8	feature size[μm]	W[μm]	type	description
1	1.5	20	GAI	single gate
2	2.0	20	GAI	single gate
3	4.0	20	GAI	single gate
4	1.5	20	GBI	single gate
5	2.0	20	GBI	single gate
6	4.0	20	GBI	single gate
7	1.5	18.5	GBI	single gate
8	2.0	18	GBI	single gate
9	4.0	16	GBI	single gate

block 9	feature size[μm]	W[μm]	type	description
1	1.5	24	GAI	2 pillar NAND gate
2	2.0	32	GAI	2 pillar NAND gate
3	4.0	52	GAI	2 pillar NAND gate
4	1.5	24	GBI	2 pillar NAND gate
5	2.0	32	GBI	2 pillar NAND gate
6	4.0	52	GBI	2 pillar NAND gate
7	1.5	24	GAI	2 pillar NAND gate
8	2.0	32	GAI	2 pillar NAND gate
9	4.0	52	GAI	2 pillar NAND gate
10	1.5	24	GBI	2 pillar NAND gate
11	2.0	32	GBI	2 pillar NAND gate
12	4.0	52	GBI	2 pillar NAND gate

block A	feature size[μm]	W[μm]	type	description
1	2.0	42	GAI	surround gate
2	2.0	52	GAI	surround gate
3	2.0	62	GAI	surround gate
4	2.0	42	GBI	surround gate
5	2.0	52	GBI	surround gate
6	2.0	62	GBI	surround gate

test structures	description
1	poly series resistance
2	metal step coverage
3	metal separation
4	v.d.P: poly on LOCOS
5	v.d.P: GAI on pillar top
6	v.d.P: GBI on pillar top
7	v.d.P: substrate on pillar top
8	v.d.P: substrate on pillar bottom
9	v.d.P: GAI on pillar bottom
10	v.d.P: GBI on pillar bottom

Table B.2: Layout description of fabricated vertical MOSFETs

Appendix C

Batch listings

C.1 Batch listing for FILOX test batch

See section 4.2.

Editing k2217dt on 04-13-2003

B	R	G	No	1	2	3	4	5	6	ID	Description	Cou
										k2217dt	MR/DK - vLOCOS tests	
										r1	Front	
										g1	HEADER	
			1							G-S12	Title Page: 3 wafers, p-type, <100>, 10-33ohm.cm	16
			2							P-EM	Reticle Writing	0
			3							G-1P	Lithography Notes: optic litho, 1u	12
			4							G-1	wafers 1..3 were taken out of batch k2101... they were previously used for etch tests	0
			5							G-1	batch splits... wafer 1: 5nm pad oxide, 40nm nitride, vary oxide thickness wafer 2: 5nm pad oxide, 70nm nitride, vary oxide thickness wafer 3: 5nm pad oxide, 130nm nitride, vary oxide thickness	12
										com1a	some test...	
			6							W-C1	* RCA clean (WAFER 1..3)	12
			7							F12-0	*Furnace 12: Load in N2: 5nm oxide at 800degC	12
												0
			8							LN-0	* Deposit SIN4 40nm, @ 740degC DCS:NH4 1:4, 2.3nm/m (WAFER 1)	1
			9							D-0	Dry etch 40nm SI3N4 + pad oxide OPT80+CHF3+Ar to leave sidewall spacers please keep overetch to a min!!!! (WAFER 1)	1
			10							LN-0	Deposit SIN4 70nm, @ 740degC DCS:NH4 1:4, 2.3nm/m (WAFER 2)	1
			11							D-0	Dry etch 70nm SI3N4 + pad oxide OPT80+CHF3+Ar to leave sidewall spacers please keep overetch to a min!!!! (WAFER 2)	1
			12							LN-130	* Deposit Si3N4 130nm+-20nm @ 740degC DCS:NH4 1:4, 2.3nm/m. (WAFER 3)	1
			13							D-0	Dry etch 130nm Si3N4 + pad oxide OPT80+CHF3+Ar to leave sidewall spacers please keep overetch to a min!!!! (WAFER 2)	1
												12
			14							G-3	* Special instructions: cleave all three wafers in 4 parts for nitride	0
			15							W-C2	* Fuming Nitric acid clean, 2nd pot only (wafer 1..3)	0
												12
			16							W-C1	* RCA clean	0
			17							F5-9504G	950degC, 40nm+- 5nm, O2 + HCl (3 parts of wafer 1..3)	0
			18							W-C1	* RCA clean	1
			19							F5-0	950degC, 80nm+- 5nm, O2 + HCl (3 parts of wafer 1..3)	1
			20							W-C1	* RCA clean	0
			21							F5-0	950degC, 120nm+- 5nm, O2 + HCl (3 parts of wafer 1..3)	0
			22							W-C1	* RCA clean	0
			23							F5-00	950degC, 160nm+- 5nm, O2 + HCl (3 parts of wafer 1..3)	0
												0

Figure C.1: Listing for FILOX test structures

C.2 Batch listing for vertical capacitors

See section 5.2

Editing k2001s on 04-13-2003

B	R	G	No	1	2	3	4	5	6	ID	Description	Cou
										k2001s	DK - some cool caps (last changes 07.07.00)	
										r1	Front	
										g1	HEADER	
			1							G-S12	Title Page: 9 wafers, p on p+epi, <100>, 0.5-1.0ohm.cm + 1 check of the same	9
			2							P-EM	E-BEAM Mask/Reticle Writing	2
			3							G-1P	Lithography Notes: optic litho, 1u5	9
			4							G-1	batch splits... wafer 1..3: wafer - oxide - polysilicon - metal (reference wafers) wafer 4..6: wafer - oxide - nitride tops - polysilicon - metal wafer 7..9: wafer - oxide - nitride tops/fillets - polysilicon - metal wafer 10: testwafer for oxide	9
										com1a	ACTIVE AREA (WAFER 1..9)	
			5							W-C1	* RCA clean (WAFER 1..9)	9
			6							F5-9002P	* Pad oxidation: 900degC, 20nm+- 5nm, O2 + HCl (WAFER 1..9)	9
			7							LN-130	* Deposit Si3N4 130nm+-20nm @ 740degC DCS:NH4 1:4, 2.3nm/m. (WAFER 1..9)	9
			8							P-G1	* Photolith mask, K973 AA Light Field: nom. 1.1um resist (WAFER 1..9)	9
			9							P-RHBD	* Hardbake for dry etch (WAFER 1..9)	9
			10							D-NO1E	Etch Si3N4+PadSiO2. Anisot. L/F EBMF/OPTICAL resist OPT80+CHF3+Ar (WAFER 1..9)	9
			11							X-1	Measure specified areas on 12 wafers; flat, middle, curve.	9
			12							P-RS	* Resist strip (WAFER 1..9)	9
			13							W-C1	* RCA clean (WAFER 1..9)	9
			14							F6-W0060	* Hydrox oxidation: 1000degC, 600nm+-20nm, H2 + O2 (WAFER 1..9)	9
												0
			15							WH-2D2	Dip etch, 20:1 BHF 25degC. 30 seconds to remove any oxide on nitride (WAFER 1..3)	3
			16							WN-1	+ Strip/Wet etch Si3N4, Orthophosphoric acid 160degC (WAFER 1..3)	3
			17							WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic to remove 20nm pad oxide (WAFER 1..3)	3
			18							LO-0	LTO deposition: 50nm at 400degC SiH4 and O2 (WAFER 4..9) BEST EFFORT !!!	6
												0
										com2a	pillar definition and etch...	
			19							P-G1	* Photolith mask: K973 PL, Light Field: nom. 1.1um resist STANDARD (Wafer 1..9)	9
			20							G-2	* See Engineer: INSPECT	9
			21							P-RHBD	* Hardbake for dry etch (WAFER 1..9)	9
			22							G-2	* See Engineer for instructions about dry etch (WAFER 1..9)	9
												0
			23							D-0	Dry etch: etch 50nm LTO + 130nm Si3N4 + 20nm SiO2 use Si3N4 etch conditions for whole layers WAFER4..9	6
												0
			24							D-SP2S	Etch Poly/AmSi. Anisot. on oxides >15nm SYS90 HBr 2 step. (For LF patterns) ETCH 300nm deep (WAFER 1..9) this is a <si> etch not a poly etch	9
			25							P-RS	* Resist strip (WAFER 1..9)	9
			26							W-C2	* Fuming Nitric acid clean, 2nd pot only (WAFER 1..9)	9
			27							G-2	* See Engineer for instructions (WAFER 1..9)	9
										com3a	remove etch damage... (WAFER 1..9)	
			28							W-C1	* RCA clean (WAFER 1..9) + CHECK WAFER 10	10
			29							F12-00	800deg: 20nm SiO2 on Si, O2 (no HCL) (WAFER 1..9) + CHECK WAFER 10	10
			30							G-2	* See Engineer for instructions (WAFER 1..9)	9
										comba	nitride spacers... (WAFER 7..9)	
												0
			31							W-C1	* RCA clean (WAFER 7..9)	3
			32							LN-0	* Deposit SiN4 70nm @740degC DCS:NH4 1:4, 2.3nm/m (WAFER 7..9) BEST EFFORT !!!	3
			33							D-0	Dry Etch Si3N4 + pad oxide OPT80+CHF3+Ar TO LEAVE SIDEWALL SPACERS (WAFER 7..9) 5-10% overetch	3
			34							D-D60	* Descum: 3 min. SRS barrel O2 (WAFER 7..9)	3
			35							W-C1	* RCA clean (WAFER 7..9)	3
			36							F5-0	* Furnace 5: 950degC, 100nm +- 5nm, O2 + HCL (WAFER 7..9)	3
			37							WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic to remove oxide on nitride (WAFER 7..9) NOTE: MINIMISE previous STAGE OXIDE LOSS!!!	3

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B	R	G	No	1	2	3	4	5	6	ID	Description	Cou	C
			38							WN-1	+ Strip/Wet etch Si3N4, Orthophosphoric acid 160degC (WAFER 7..9) this stage is to remove the sidewall spacers only!!!	3	0
												0	0
			39							WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic to remove etch damage removal oxide (WAFER 1..9) + CHECK WAFER 10 check if WAFER 10 is hydrophobic!!!	4	0
										com4aa	we need some gate oxide over the pillars... (WAFER 1..9)		
			40							G-3	Special Instructions: DO 3 WAFERS at a time. furnace and poly deposition in one go!!! store wafers in nitrogen to stop contermination!!!	0	0
												0	0
			41							W-C1	* RCA clean (WAFER 1,4,7)	0	0
			42							F14-0	Furnace 14 - KOYO VERTICAL FURNACE (OXIDATION): 4nm SiO2 on Si, O2 (WAFER 1,4,7) at 800degC BEST EFFORT !!!	3	0
			43							LE-0	Low Pressure Epitaxy -> in-situ phosporus doped poly 1e19 at 650..670degC (WAFERS 1,4,7) 200nm thick	0	0
												0	0
												0	0
			44							W-C1	* RCA clean (WAFER 2,5,8)	0	0
			45							F14-0	Furnace 14 - KOYO VERTICAL FURNACE (OXIDATION): 8nm SiO2 on Si, O2 (WAFER 2,5,8) at 800degC BEST EFFORT !!!	9	0
			46							LE-0	Low Pressure Epitaxy -> in-situ phosporus doped poly 1e19 at 650..670degC (WAFERS 2,5,8) 200nm thick	0	0
												0	0
												0	0
			47							W-C1	* RCA clean (WAFER 3,6,9)	0	0
			48							F14-0	Furnace 14 - KOYO VERTICAL FURNACE (OXIDATION): 12nm SiO2 on Si, O2 (WAFER 3,6,9) at 800degC BEST EFFORT !!!	0	0
			49							LE-0	Low Pressure Epitaxy -> in-situ phosporus doped poly 1e19 at 650..670degC (WAFERS 3,6,9) 200nm thick	0	0
												0	0
										com4aaa	- Wafer 1..9: polysilicon deposition....		
			50							RA-2	RTA implant activation 20secs 1050degC	9	0
										metaldepo	- Wafer 1..9: metal deposition...		
			51							MS-0	Sputter 700nm Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED (WAFER 1..9)	9	0
			52							P-G2	* Photolith mask K973,(M1), Light Field: nom. 2.2um resist	9	0
			53							X-0	General inspection stage (WAFER 1..9)	9	0
			54							P-RHBW	* Hardbake for wet etch (WAFER 1..9)	9	0
										metaletch	- Wafer 1..9: metal etching		
			55							WM-A2	+ Wet etch Al, Orthophosphoric acid, 37degC, till clear. NO DEFRECKLE ETCH (WAFER 1..9)	9	0
			56							X-0	General inspection stage CHECK DENSITY OF Si GRAINYNESS (WAFER 1..9)	9	0
			57							P-RHBD	* Hardbake for dry etch (WAFER 1..9)	9	0
										com4ab	- Wafer 1..9: polysilicon etch...		
			58							D-SP2V	Etch Poly/AmSi. Anisot. on THIN gate ox, <15nm SYS90 HBr 3 step. (For LF patterns) note: gate oxide thickness 2nm and 4nm!!! -> short overetch	9	0
			59							P-RS	* Resist strip (WAFER 1..9)	9	0
										com5	Back contact (WAFER 1..9)		
			60							P-RF	* Frontspin resist (WAFER 1..9)	9	0
			61							P-RHBD	* Hardbake for dry etch (WAFER 1..9)	9	0
			62							D-SON1	BACK Strip: SiO2 _PolySi OPT80+ CF4+O2 (WAFER 1..9)	9	0
			63							WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic (WAFER 1..9)	9	0
			64							ME-AL10B	Evaporate pure Al 1000nm onto BACKS. WAFERS COULD BE Au CONTAMINATED (WAFER 1..9)	9	0
			65							P-RS	* Resist strip (WAFER 1..9)	9	0
			66							X-0	General inspection stage (WAFER 1..9)	9	0
			67							W-C3	* Fuming Nitric Acid clean, metallised wafers	0	0
			68							F9-H42	* Alloy/ Anneal: 30mins H2/N2 420degC 5'N2,30'H2/N2,5'N2.	9	0

Figure C.2: Listing for vertical capacitors

C.3 Batch listing for vertical MOSFETs

See section 6.3

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B	R	G	No	1	2	3	4	5	6	ID	Description	Cou
										k2101dt	DK - some ultracool vmos'	
										r1	Front	
										g1	HEADER	
			1							G-S12	Title Page: 12 wafers, p-type, <100>, 10-33ohm.cm + 4 check wafers of the same	160
			2							P-EM	Reticle Writing	0
			3							G-1P	Lithography Notes: optic litho, 1u	120
			4							G-1	batch splits... wafer 1..3: 50nm channel length; tox = 3/6/9nm (VLOCOS) wafer 4..6: 100nm channel length; tox = 3/6/9nm (VLOCOS) wafer 7..9: 150nm channel length; tox = 3/6/9nm (VLOCOS) wafer 10..12: 150nm channel length; tox = 3/6/9nm (no VLOCOS)	120
			5							G-1	wafer 13: test wafer to test pad oxide thickness for nitride spacers wafer 14..16: test wafer for silicon pillar etch	120
										com00	P-Well - all over the wafer...	
			6							W-C1	* RCA clean (WAFER 1..12) + test wafers #14-16	150
			7							IB-5045	* Implant Boron: 5E14 B+ 50 KeV (BIPOLAR Base implant) (WAFER 1..12,14-16)	150
			8							W-C1	* RCA clean (WAFER 1..12,14-16)	150
			9							F4-N10DI	* General Boron Drive-in 1100degC 10'dryO2,30'N2 (WAFER 1..12,14-16)	150
			10							WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic remove all oxide from the boron diffusion stage (WAFER 1..12,14-16)	150
										com1	pillar definition and etch	
			11							P-GS1	* STEPPER Photolith: reticle KA14R PL Light Field: nom. 1.1um resist STANDARD	150
			12							G-2	* See Engineer for instructions	150
			13							P-RHBD	* Hardbake for dry etch (WAFER 1..12,14-16)	150
												0
			14							D-SP2S	testwafers (WAFER 14..16): Etch Poly/AmSi. Anisot. SYS90 HBr 2 step. (For LF patterns) ETCH 300nm deethis is a <si> etch not a poly etch!!!	150
												0
			15							G-2	* See Engineer for instructions	150
												0
			16							D-SP2S	Etch Poly/AmSi. Anisot. SYS90 HBr 2 step. (For LF patterns) ETCH 250nm deep (WAFER 1..3) this is a <si> etch not a poly etch!!!	30
			17							D-SP2S	Etch Poly/AmSi. Anisot. SYS90 HBr 2 step. (For LF patterns) ETCH 300nm deep (WAFER 4..6) this is a <si> etch not a poly etch!!!	30
			18							D-SP2S	Etch Poly/AmSi. Anisot. SYS90 HBr 2 step. (For LF patterns) ETCH 350nm deep (WAFER 7..9) this is a <si> etch not a poly etch!!!	30
			19							D-SP2S	Etch Poly/AmSi. Anisot. SYS90 HBr 2 step. (For LF patterns) ETCH 350nm deep (WAFER 10..12) this is a <si> etch not a poly etch!!!	30
												0
			20							P-RS	* Resist strip (WAFER 1..12)	120
										com1a	ACTIVE AREA (WAFER 1..12)	
			21							W-C1	* RCA clean (WAFER 1..12,13,14)	120
			22							F5-9002P	* Pad oxidation: 900degC, 20nm+- 5nm, O2 + HCl (WAFER 1..12) and check wafer 13,14 !!!	130
			23							LN-130	* Deposit Si3N4 130nm+-20nm @ 740degC DCS:NH4 1:4, 2.3nm/m. (WAFER 1..12,14)	120
			24							P-GS1	* STEPPER Photolith: reticle KA14R AA Light Field: nom. 1.1um resist STANDARD Wafers 1-12,14	120
			25							G-2	* See Engineer for instructions	120
			26							P-RHBD	* Hardbake for dry etch (WAFER 1..12,14)	120
			27							D-NO1E	Etch Si3N4+PadSiO2. Anisot. L/F EBMF/OPTICAL resist OPT80+CHF3+Ar (WAFER 1..12,14)	120
			28							P-RS	* Resist strip (WAFER 1..12,14)	120
			29							W-C1	* RCA clean (WAFER 1..12,14)	120
			30							F6-W0060	* Hydrox oxidation: 1000degC, 600nm+-20nm, H2 + O2 (WAFER 1..12,14)	120
										com3b	nitride spacers... and vertical oxide...	
			31							WH-2D2	Dip etch, 20:1 BHF 25degC. 30 seconds to remove any oxide on nitride (WAFER 1..12,14)	120
			32							D-0	Dry Etch Si3N4 + pad oxide OPT80+CHF3+Ar TO LEAVE SIDEWALL SPACERS (WAFER 1..12,14) 5-10% overetch	120
			33							D-D60	* Descum: 3 min. SRS barrel O2 (WAFER 1..12,14)	120
			34							W-C1	* RCA clean (WAFER 1..12,14)	120
												0
			35							F6-0	* Furnace 6: Load in N2: 60nm @ 1000degC wafers #1-9,14	100
			36							W-C2	* Fuming Nitric acid clean, 2nd pot only wafers #10-12	0
												0

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B	R	G	No	1	2	3	4	5	6	ID	Description	Cou
										com3c	p+ bulk contact implants...	
			37							P-GS1	* STEPPER Photolith: reticle KA14R, PP Dark Field: nom. 1.1um resist STANDARD (WAFER 1..12)	12
			38							G-2	* See Engineer for instructions	12
			39							P-RHBI	* Hardbake for implant (WAFER 1..12)	12
												0
			40							IB-0	* Implant B+: 1E15 47keV (WAFER 1..9)	9
			41							IB-0	* Implant B+: 1E15 25keV (WAFER 10..12)	3
												0
			42							P-RS	* Resist strip (WAFER 1..12)	12
			43							W-C2	* Fuming Nitric acid clean, 2nd pot only (WAFER 1..12)	12
										com3dd	n+ source and drain implants for gate after implant transis...	
			44							P-GS1	* STEPPER Photolith: reticle KA14R, NGA Dark Field: nom. 1.1um resist STANDARD (WAFER 1..12)	12
			45							G-2	* See Engineer for instructions	12
			46							P-RHBI	* Hardbake for implant (WAFER 1..12)	12
												0
			47							IA-0	* Implant As+: 3e15 120keV implant direction: west (WAFER 1..9)	9
			48							IA-0	* Implant As+: 3e15 120keV impant direction: east (WAFER 1..9)	9
			49							IA-0	* Implant As+: 3e15 50keV implant direction: west (WAFER 10..12)	3
			50							IA-0	* Implant As+: 3e15 50keV impant direction: east (WAFER 10..12)	3
												0
			51							P-RS	* Resist strip (WAFER 1..12)	12
			52							W-C2	* Fuming Nitric acid clean, 2nd pot only (WAFER 1..12)	12
										com3	remove nitride fillets and stress relief oxide...	
			53							WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic --> to remove any access oxide on the nitride (WAFER 1..12) max 5 sec	12
			54							WN-1	+ Strip/Wet etch Si3N4, Orthophosphoric acid 160degC this is to remove the fillets and the nitride on top of the pillar (WAFER 1..12)	12
										com4aa	we need some gate oxide over the pillars... (WAFER 1..9)	
												0
			55							WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic --> about 40sec for 20nm stress relief oxide... (WAFER 1,4,7,10) + check wafer 13!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!	5
			56							W-C1	* RCA clean (WAFER 1,4,7,10 + check 13)	5
			57							F12-G0	* Gate oxidation 2: Temp = 900degC or less, < 10nm, O2 (+ HCl) 3nm SiO2 on Si, O2 (WAFER 1, 4, 7, 10 + check13) at 800degC BEST EFFORT !!!	0
			58							LE-0	Low Pressure Epitaxy -> deposit 200nm poly 5e19 at 650..670degC (WAFERS 1,4,7,10) and check wafer13!!!	5
			59							WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic --> about 40sec for 20nm stress relief oxide... (WAFER 2,5,8,11)	4
			60							W-C1	* RCA clean (WAFER2,5,8,11)	4
			61							F12-G0	* Gate oxidation 2: Temp = 900degC or less, < 10nm, O2 (+ HCl) 6nm SiO2 on Si, O2 (WAFER 2,5,8,11) at 800degC BEST EFFORT !!!	0
			62							LE-0	Low Pressure Epitaxy -> deposit 200nm poly 5e19 at 650..670degC (WAFERS 2,5,8,11)	4
			63							WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic --> about 40sec for 20nm stress relief oxide... (WAFER 3,6,9,12)	4
			64							W-C1	* RCA clean (WAFER3,6,9,12)	4
			65							F12-G0	* Gate oxidation 2: Temp = 900degC or less, < 10nm, O2 (+ HCl) 9nm SiO2 on Si, O2 (WAFER 3,6,9,12) at 800degC BEST EFFORT !!!	0
			66							LE-0	Low Pressure Epitaxy -> deposit 200nm poly 5e19 at 650..670degC (WAFERS 3,6,9,12)	4
												0
										com4aaa	- Wafer 1..12: polysilicon gate etch....	

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B	R	G	No	1	2	3	4	5	6	ID	Description	Cou
			67	☑						P-GS1	* STEPPER Photolith: reticle KA14R, P1 Light Field: nom. 1.1um resist STANDARD	12
			68	☑						G-2	* See Engineer: INSPECT	12
			69	☑						P-RHBD	* Hardbake for dry etch	12
			70	☑						D-SP2V	Etch Poly/AmSi. Anisot. on THIN gate ox, <15nm SYS90 HBr 3 step. (For LF patterns) WAFER1..12 Use ICP etcher **** leave poly fillets - stop on 2nm oxide****	12
			71	☑						P-RS	* Resist strip (WAFER 1..12)	12
			72	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only	12
										com0	n+ implant on gate before implant transis	
			73	☑						P-GS1	* STEPPER Photolith: reticle KA14R, NGB Dark Field: nom. 1.1um resist STANDARD (WAFER1..12)	12
			74	☑						G-2	* See Engineer: INSPECT	12
			75	☑						P-RHBI	* Hardbake for implant (WAFER1..12) please, please, please, hardbake the wafers foor 2h !!!!	12
												0
			76	☑						IA-0	* Implant As+: 3e15 90keV implant direction: west (WAFER1..9)	9
			77	☑						IA-0	* Implant As+: 3e15 90keV implant direction: east (WAFER1..9)	9
			78		☑					IA-0	* Implant As+: 3e15 50keV implant direction: west (WAFER10..12)	3
			79		☑					IA-0	* Implant As+: 3e15 50keV implant direction: east (WAFER10..12)	3
												0
			80	☑						P-RS	* Resist strip (WAFER1..12)	12
			81	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only (WAFER1..12)	12
										comu	remove poly silicon fillets (WAFER1..12)	
			82	☑						P-GS1	* STEPPER Photolith: reticle KA14R, PR Light Field: nom. 1.1um resist STANDARD	12
			83	☑						G-2	* See Engineer for instructions See Tony about next dry etch stage	12
			84	☑						P-RHBD	* Hardbake for dry etch	12
			85	☑						D-0	Dry etch: Use isotropic SF6 polySi etch in the OPT80+ To remove 200nm polysilicon fillets. No visible end point *****See engineer for nonstandard process - best effort***** please remember to stop in the thin gate oxide if possible	12
			86	☑						P-RS	* Resist strip	12
										backend	oxide depo and so on (WAFER1..12)	
			87	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only	12
			88	☑						LS-BO1	BPSG: Deposit 100nm undoped Silox + 500nm BPSG (4%P/*10%*B approx)	12
			89	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only	12
			90	☑						RA-1	RTA implant activation 10secs 1100degC (Std.CMOS S_D) - this is for annealing and reflow	12
			91	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only	12
			92	☑						P-GS1	* STEPPER Photolith: reticle KA14R,CW Dark Field: nom. 1.1um resist STANDARD	12
			93	☑						G-2	* See Engineer for instructions	12
			94	☑						P-RHBD	* Hardbake for dry etch (WAFER1..12)	12
			95	☑						D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar	12
			96	☑						P-RS	* Resist strip (WAFER 1..12)	12
			97	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only	12
										metaldepo	metal deposition... (WAFER1..12)	
			98	☑						WH-2D2	Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation)	12
			99	☑						MS-TA10	Sputter 1000nm Ti-Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED	12
			100	☑						P-GS2	* STEPPER Photolith: reticle KA14r; M1,Light Field: nom. 2.2um resist (For Si etch>1um or metal)	12
			101	☑						G-2	* See Engineer for instructions	12
			102	☑						P-RHBD	* Hardbake for dry etch	12
			103	☑						X-0	General inspection stage	12
										metaletch	metal etching (WAFER1..12)	
												0
			104	☑						D-MAT1	+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar (WHOLE 4" wfrs) WAFERS #1,4	12
			105		☑					P-RS	* Resist strip	0
			106		☑					MS-0	Add ARC to wafers #2,3,5-10,12	0
			107		☑					P-GS2	* STEPPER Photolith: reticle KA14r; M1,Light Field: nom. 2.2um resist (For Si etch>1um or metal)	0

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B	R	G	No	1	2	3	4	5	6	ID	Description	Cou
			108		☑					G-2	* See Engineer for instructions	0
			109		☑					P-RHBD	* Hardbake for dry etch	0
			110			☑				D-MAT1	+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar (WHOLE 4" wfrs)	0
												0
			111	☑						X-0	General inspection stage CHECK DENSITY OF SI GRAINYNESS	12
			112	☑						P-RS	* Resist strip	12
			113	☑						W-C3	* Fuming Nitric Acid clean, metallised wafers	12
			114	☑						F9-H42	* Alloy/ Anneal: 30mins H2/N2 420degC 5'N2,30'H2/N2,5'N2.	12

Figure C.3: Listing for vertical MOS transistors

Appendix D

Publications

D.1 Conference papers

- "Electrical Characteristics of Single, Double & Surround Gate Vertical MOSFETs with Reduced Overlap Capacitance", E. Gili, V. D. Kunz, C. H. de Groot, T. Uchino, D. onaghy, S. Hall, P.Ashburn, submitted for ESSDERC 2003
- "Reduction of parasitic capacitance in vertical MOSFET's by fillet local oxidation (FILOX)", C. H. de Groot, V. D. Kunz, T. Uchino, P. Ashburn, D. C. Donaghy, S. Hall, Y. Wang, P.L.F. Hemment, ULIS 2003
- "Modelling of gain control in SiGe HBTs and Si bipolar transistors by Ge incorporation in the polysilicon emitter", V. D. Kunz, C. H. de Groot, I. M. Anteney, A. I. Abdul-Rahim, S. Hall, P. Ashburn, Nanotechnology 2003, San Francisco
- "Application of Polycrystalline SiGe for Gain Control in SiGe Heterojunction Bipolar Transistor", V. D. Kunz, C. H. de Groot, S. Hall, I. M. Anteney, A. I. Abdul-Rahim, P. Ashburn, ESSDERC 2002
- "Investigating 50nm channel length vertical MOSFETs containing a dielectric pocket, in a circuit environment", D. Donaghy, S. Hall, V. D. Kunz, C. H. de Groot, P. Ashburn, ESSDERC 2002
- "Thermal Evaluation of a micromachined PCR chip", C. G. J. Schabmueller, A. G. R. Evans, G. Ensell, A. Brunschweiler, H. Sehr, T. E. G. Niblock, V. D. Kunz, M. Bu, Micromechanics Europe 2002
- "A 50nm channel vertical MOSFET concept incorporating a retrograde channel and a dielectric pocket", A. C. Lamb, L. S. Riley, S. Hall, V. D. Kunz, C. H. de Groot, P. Ashburn, ESSDERC 2001

D.2 Journal papers

- "Gain Control in SiGe HBTs by the Introduction of Germanium into Polysilicon Emitters", V. D. Kunz, C. H. de Groot, S. Hall, P. Ashburn, accepted for publication in IEEE Transactions on Electron Devices

- "Reduction of parasitic capacitance in vertical MOSFETs by spacer local oxidation", V. D. Kunz, T. Uchino, C. H. de Groot, P. Ashburn, D. C. Donaghy, S. Hall, Y. Wang, L. F. Hemment, accepted for publication in IEEE Transactions on Electron Devices

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