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UNIVERSITY OF SOUTHAMPTON

VLSI compatible parallel fabrication and  
characterisation of down-scaled multi-configuration  
Silicon quantum dot devices

by

Yun Peng Lin

A thesis submitted in fulfilment of the requirements for the  
degree of Doctor of Philosophy

in the  
Faculty of Engineering and Applied Science  
Department of Electronics and Computer Science

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UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF ENGINEERING AND APPLIED SCIENCES  
DEPARTMENT OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

By Yun Peng Lin

Electron spins in semiconductor quantum dots (QDs) have been increasingly shown in recent years to be a promising platform for realising the qubit – the basic unit of information in quantum computing. A crucial advantage of silicon QDs over alternative platforms is the potential for scalability in a quantum system to contain large numbers of qubits. Electron spins in Si-based QDs also have the benefit of a much longer spin coherence time relative to their extensively researched GaAs based counter parts – a prerequisite which gives the essential time needed for successful quantum gate operations and quantum computations.

In this work, we propose and realise the first very large scale integration (VLSI) compatible process capable of fabricating scalable repeatable QD systems in parallel using silicon on insulator (SOI) technology. 3D finite element method (FEM) capacitance and single electron circuit simulations are first utilised to demonstrate the suitability of our double quantum dot (DQD) design dimensions in supporting single electron operation and detection. Here, we also present a new method of detection for single electron turnstile operations which makes use of the periodicity present in the charge stability diagram of a DQD.

Through process optimisation, we fabricate 144 high density lithographically defined Si DQDs for the first time in parallel with 80% of the fabricated devices having dimensional variations of less than 5 nm. The novel use of hydrogen silsesquioxane (HSQ) resist with electron beam lithography (EBL) enabled the realisation of lithographically defined reproducible QD dimensions of an average of 51 nm with a standard deviation of 3.4 nm. Combined with an optimised thermal oxidation process, we demonstrate the precise fabrication of different QDs ranging from just 10.6 nm to over 20 nm. These are the smallest lithographically defined high density intrinsic SOI based QDs achieved to date. In addition, we demonstrate the flexibility of our fabrication process in its ability to realise a wide variety

of complex device designs repeatedly. A key advantage of our process is its ability to support the scalable fabrication of QD devices without significantly affecting fabrication turnover time.

Repeatable characteristic QD Coulomb oscillations and Coulomb diamonds signifying single electron tunnelling through our system are observed in electrical characteristics. Here we achieve precise independent simultaneous control of different QD's single electron occupation as well as demonstrate evidence suggesting charge detection between QD channels. The unmatched level of clarity observed within Coulomb blockade diamond characteristics at 4.2K enables observations of line splitting of our QD's excited states at this temperature, and readout of the spin orientation of sequential single electrons filling the QD. Through this spin readout, we gained an idea of the number of electrons stored on the QD and in turn, our ability to control the QD with precision down to the single electron limit.

Statistically, we realise a parallel fabrication yield of 69% of devices demonstrating the ability to switch on and off repeatedly at 4K cryogenic temperatures with no leakage and sufficient channel resistances for single electron turnstile operations. This is the highest achieved yield observed to date for fabrication of intrinsic SOI based QD systems.

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# Declaration of Authorship

I, Yun Peng Lin, declare that this thesis entitled “VLSI compatible parallel fabrication and characterisation of down-scaled multi-configuration Silicon quantum dot devices” and the work presented in it are my own, and have been generated by me as the result of my own original research. I confirm that:

This work was done wholly or mainly while in candidature for a research degree at this University;

Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;

Where I have consulted the published work of others, this is always clearly attributed;

Where I have quoted from the work of others, the source is always given, with the exception of such quotations, this thesis is entirely my own work;

I have acknowledged all main sources of help;

Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself; development of the device fabrication process was done by myself with collaborations from M. K. Husain and F. M. Alkhalil from the University of Southampton. Device low temperature electrical characterisations were primarily carried out by J. Perez-Baraza and N. Lambert from the University of Cambridge. We were jointly published for papers and conference publications for this work (included in the “List of Publications” section).

Parts of this work have been published in research journals as indicated in the “List of Publications” section provided with this manuscript.

Signed:

Dated:



# List of Publications

## Journal Publications

- [1] **Y. P. Lin**, J. I. Perez-Barraza, M. K. Husain, F. M. Alkhalil, N. Lambert, D. A. Williams, A. J. Ferguson, H. M. H. Chong and H. Mizuta, “VLSI compatible parallel fabrication of scalable few electron Silicon Quantum Dots”, *IEEE Transactions on Nanotechnology (TNANO)*, 12 (2013) 6
- [2] **Y. P. Lin**, M. K. Husain, F. M. Alkhalil, N. Lambert, J. Perez-Barraza, Y. Tsuchiya, A. J. Ferguson, H. M. H. Chong and H. Mizuta, “Design and fabrication of densely integrated silicon quantum dots using a VLSI compatible Hydrogen selsequioxane electron beam lithography process”, *Microelectronic Engineering*, 98 (2012) 386-390
- [3] F. M. Alkhalil, J. I. Perez-Barraza, M. K. Husain, **Y. P. Lin**, N. Lambert, H. M. H. Chong, Y. Tsuchiya, D. A. Williams, A. J. Ferguson, S. Saito and H. Mizuta, “Realisation of Al tri-gate single electron turnstile co-integrated with a close proximity electrometer SET”, *Microelectronic Engineering*, 111 (2013) 64-67

## Conference Oral Publications

- [1] **Y. P. Lin**, J. I. Perez-Barraza, M. K. Husain, F. M. Alkhalil, Y. Tsuchiya, N. Lambert, D. A. Williams, A. J. Ferguson, H. M. H. Chong and H. Mizuta, “Fabrication and characterisation of down-scaled multi-configuration Silicon quantum dot devices”, *2013 Symposia on VLSI Technology and Circuits: Silicon Nanoelectronics Workshop*, Rihga Royal Hotel, Kyoto, Japan, June 2013
- [2] **Y. P. Lin**, J. I. Perez-Barraza, M. K. Husain, F. M. Alkhalil, N. Lambert, D. A. Williams, A. J. Ferguson, H. M. H. Chong and H. Mizuta, “Single electron spin qubits in lithographically defined silicon quantum dots”, *IEEE 2012 12<sup>th</sup> International conference on nanotechnology*, International Convention Centre, Birmingham, U.K., August 2012
- [3] L. Boodhoo, **Y. P. Lin**, H. M. H. Chong, Y. Tsuchiya, T. Hasegawa and H. Mizuta, “Energy Energy Reversible Si-based NEMS Switch for Nonvolatile Logic Systems”,

[4] J. I. Perez-Barraza, N. Lambert, **Y. P. Lin**, F. M. Alkhalil, M. K. Husain, H. M. H. Chong, H. Mizuta, A. J. Ferguson, “Towards single spin readout in intrinsic silicon quantum dots”, *2012 Silicon quantum information processing meeting*, Warwick University, Coventry, U.K., September 2012

[5] F. M. Alkhalil, J. I. Perez-Barraza, M. K. Husain, **Y. P. Lin**, N. Lambert, D. A. Williams, A. J. Ferguson, H. M. H. Chong and H. Mizuta, “Realization of fully tunable FinFET Double Quantum Dots with close proximity plunger gates”, *IEEE 2012 12<sup>th</sup> International conference on nanotechnology*, International Convention Centre, Birmingham, U.K., August 2012

[6] M. K. Husain, **Y. P. Lin**, F. M. Alkhalil, H. M. H. Chong, Y. Tsuchiya, N. Lambert, A. J. Ferguson, and H. Mizuta, “Fabrication of Silicon-based single spin quantum devices using Hydrogen silsesquioxane electron beam resist”, *2011 37<sup>th</sup> International conference on micro and nano engineering*, The BCC Berliner Congress Center, Berlin, Germany, September 2011

[7] H. Mizuta, M. K. Husain, F. M. Alkhalil, **Y. P. Lin**, Z. Moktadir, S. Boden, Y. Tsuchiya, N. Lambert, A. J. Ferguson and H. M. H. Chong, “Silicon nanofabrication for QIP in Southampton” (Invited Talk), *U.K. Silicon QIP Meeting*, University of Cambridge, Cambridge, U.K., May 2011

## Conference Poster Publications

[1] **Y. P. Lin**, J. I. Perez-Barraza, M. K. Husain, F. M. Alkhalil, N. Lambert, D. A. Williams, A. J. Ferguson, H. M. H. Chong and H. Mizuta, “VLSI Compatible parallel fabrication of Si Quantum Dots”, *2012 Silicon quantum information processing meeting*, Warwick University, Coventry, U.K., September 2012

[2] **Y. P. Lin**, M. K. Husain, F. M. Alkhalil, J. I. Perez-Barraza, N. Lambert, A. J. Ferguson, H. M. H. Chong and H. Mizuta, “Single electron spin qubits in lithographically defined

silicon quantum dots”, *2012 International Seminar on Emerging Nanotechnology*, Shiinoki Cultural Complex, Kanazawa, Japan, March 2012

- [3] **Y. P. Lin**, M. K. Husain, F. M. Alkhalil, N. Lambert, A. J. Ferguson, H. M. H. Chong and H. Mizuta, “Design and fabrication of single electron spin qubits in lithographically defined silicon quantum dots”, *2011 quantum information processing and communication international conference*, ETH Zurich, Zurich, Switzerland, September 2011
- [4] M. K. Husain, **Y. P. Lin**, F. M. Alkhalil, H. M. H. Chong, Y. Tsuchiya, N. Lambert, A. J. Ferguson, and H. Mizuta, “Improved Silicon Quantum Dots Single Electron Transfer Operation with Hydrogen Silsesquioxane Resist Technology”, *2012 38<sup>th</sup> International conference on micro and nano engineering*, Centre de congrès Pierre Baudis, Toulouse, France, September 2012
- [5] F. Alkhalil, J. I. Perez-Barraza, M. K. Husain, **Y. P. Lin**, N. Lambert, H. M. H. Chong, Y. Tsuchiya, D. Williams, A. Ferguson and H. Mizuta, “Realisation of Al FinFET single electron turnstile co-integrated with a close proximity electrometer SET”, *2012 38<sup>th</sup> International conference on micro and nano engineering*, Centre de congrès Pierre Baudis, Toulouse, France, September 2012
- [6] F. Alkhalil, J. I. Perez-Barraza, M. K. Husain, **Y. P. Lin**, N. Lambert, H. M. H. Chong, Y. Tsuchiya, D. Williams, A. Ferguson and H. Mizuta, “Al FinFET single electron devices with close proximity Si plunger gates”, *Silicon Quantum Information Processing meeting*, University of Warwick, Coventry, U. K., September 2012
- [7] J. I. Perez-Barraza, **Y. P. Lin**, F. M. Alkhalil, N. Lambert, M. K. Husain, H. M. H. Chong, A. J. Ferguson and H. Mizuta, “Towards single spin readout in intrinsic silicon quantum dots”, *2012 Graduate school conference*, University of Cambridge, Cambridge, U. K., December 2011
- [8] F. M. Alkhalil, M. K. Husain, **Y. P. Lin**, H. M. H. Chong, A. J. Ferguson, Y. Tsuchiya and H. Mizuta, “Realization of an integrated double spin qubit device on ultra-thin silicon-on-insulator”, *2011 quantum information processing and communication international conference*, ETH Zurich, Zurich, Switzerland, September 2011



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*I dedicate this work to my parents Mr. Wei Lin and Mrs. Hong Guo for their invaluable support and guidance throughout my life.*

# Chapter 1

## Introduction

### 1.1 Overview of Research

Quantum information technology (QIT) is a radical new field which exploits the quantum properties of matter in order to perform computations and solve problems that were classically considered intractable. Motivated by the miniaturization and continual drive for performance of electronic devices, QIT has been shown to offer many advantages over classical computing. In 1997, Shor's algorithm [1] really put quantum computing on the world stage by demonstrating efficient prime factorization of integers,  $N$ , within time  $t \propto (\log N)^\alpha$  compared to the much longer time of  $t \propto e^{(\log N)^\alpha}$  on a classical computer. Further to this, Grover [2] formally proved in 1997 that search through unstructured search space could be sped up on a quantum computer. These results are a powerful indication that quantum computers are more powerful than any classical Turing machine.

The basic unit of information in quantum computing is the “qubit”. The difference between a qubit and a classical bit is that it's possible for qubits to form linear combinations or superpositions of its two possible states ( $|0\rangle$  or  $|1\rangle$ ). Quantum computation is then performed through a set of quantum gates which apply a unitary transformation  $U$  to a set of qubits in a certain quantum state  $|\psi\rangle$ . The resulting qubits in state  $|\psi'\rangle = U|\psi\rangle$  can then be measured. More importantly (just as in the classical case) one can find a set of universal quantum gates which can construct any desired computation [3]. Thus, the implementation of a set of universal gates is crucial in the realisation of a quantum computer. The ability to

construct such a set of gates that act only on one or two qubits at a time greatly reduces the complexity of the problem and avoids necessities of multi-qubit gates.

Since its birth, many experimental platforms have been proposed for the realisation of quantum computing. This ranges from manipulation of spins in cold trapped atoms and Josephson junctions to topological insulators and carbon nanotubes. However, the use of electron spins in solid state quantum dots (QD) has proven to be a natural candidate for realization of a qubit since electron spin is already a two level state (spin  $|\uparrow\rangle$  or  $|\downarrow\rangle$ ). A quantum dot is essentially an electron trap, capable of confining individual electrons in a structure of the order of tens of nanometres. At these dimensions, the electron energies become discrete levels and filling of these different energy states then become governed by rules from atomic physics (e.g. Hund's rule). Specifically within research on quantum dots, results have, to a large extent, demonstrated fulfilment of some of the fundamental requirements for realisation of a quantum computer. Notably the ability to store and initialise qubit states before each computation, manipulation of individual electron spin states via quantum gates, sufficient qubit isolation from its local environment to reduce the effects of spin decoherence and qubit readout to obtain the computation outputs. These five core criteria were first proposed in 2000 by DiVincenzo [4] and provide a checklist for the basic requirements of any physically realizable quantum computer. Crucially however, two additional criteria exist to ensure practicality – the device design must be scalable to allow for future multi qubit manipulation and there must be a method of faithfully transmitting qubits between specific locations. Both of these are challenging issues in most of the physical set-ups proposed so far.

A major drawback for electron spins in solid state quantum dots is their inevitable coupling to other degrees of freedom within the local environment. This includes the effects of spin-orbit and hyperfine interactions with the surrounding nuclei which work to induce a measurable decoherence effect on electron spins. In turn, this causes the lifetime of spin states to be finite and raises difficulties when trying to ensure sufficient qubit isolation in experimental setups; therefore, being able to probe the dynamics of individual spins in quantum dots repeatedly on a large scale and being able to present a statistical analysis of these characteristics is vital to determining whether it's a suitable platform for the realisation of quantum computing.

## 1.2 Motivation and Contributions

A variety of materials have been explored to find the best system for solid state quantum dots (QDs) - ranging from self-assembled InGaAs QDs to superconducting QDs and from P doped Si QDs to QDs in graphene nanoribbons. However, recently it seems that QDs formed in the two dimension electron gas (2DEG) layer of GaAs heterostructures have been most successful in demonstrating electron spin manipulation (See Chapter 3).

A major advantage in using GaAs is its direct band gaps which allow for easy optical manipulation of spin states. However, Si has recently attracted much interest due to its relatively smaller spin-orbit coupling and the appearance of isotopically pure Si materials which offer almost a spin-zero nuclear background. This significantly reduces the effects of contact hyperfine interactions for spin qubits in solid state QDs and can potentially lead to much longer electron spin decoherence time in comparison to that found in GaAs QDs (where confined electrons couple to  $\sim 10^6$  spin-3/2 nuclei through hyperfine interactions). This offers benefits to quantum computing in terms of allowing for longer gate operation times, greater fidelity in qubit state readout and longer qubit transport times between specific locations (allowing for sufficient qubit isolation from its local environment). In addition, being the long-time staple for the electronics industry, silicon has the benefit of being compatible with existing semiconductor device fabrication techniques. Lithographically defined Si based QDs with connecting nanowires bring further benefits by potentially offering greater scalability and compatibility with current very large scale integration (VLSI) techniques. It is therefore highly desirable to determine whether a process can be actually developed to fabricate scalable QDs which implements current silicon fabrication technologies. This in turn would help to further determine whether the Si based QDs are indeed a good candidate for quantum information processing.

In this work we aim to develop and realise for the first time a VLSI compatible process enabling the parallel fabrication of over 100 scalable complex QD systems on silicon on insulator (SOI). Our aims include the capability to fabricate versatile arrays of structurally different QD systems in parallel and to minimize turnover times given significant QD system design modifications. We start by exploring the fabrication of a number of different QD systems consisting of single spin turnstile devices (SSTDs) and double quantum dots (DQD) for individual single electron spin transfer along with a single QDs/single electron transistors (SET) for single electron charge and potential single electron spin transfer and readout.

Because our nanoscale system is lithographically defined in silicon via VLSI compatible processes, our platform crucially allows for scalability of the quantum system. To ensure an effective design with functional dimensionality, we first explore the feasibility of the proposal through an initial device design and mathematical analysis of the electrical characteristics of the SSTD. Finite element method is employed for a 3D capacitance analysis of our device, from which results are fed into a simulation of an equivalent circuit for the SSTD using the Monte Carlo simulator “SETSPICE” [5] which is based on the “orthodox theory” [6] of single electron tunnelling.

To then develop the fabrication process, we propose and implement the VLSI compatible fabrication process capable of realising over 100 complex QD devices in parallel for the first time via an EBL process. 4% hydrogen silsesquioxane (HSQ) resist is used with EBL for the first time to realise reproducible QD dimensions. The devices are then electrically characterised at milli-Kelvin temperatures to verify their single electron turnstile functionality, charge and single electron detection capabilities, and the ability to go down to the few electron limit in the QDs. In addition, we carry out a statistical analysis of the fabrication yield of each batch of devices.

### 1.3 Document Structure

This thesis explores an approach to develop for the first time a fabrication process which implements VLSI compatible techniques aimed at parallel fabrication of SOI based few electron QD systems on a large scale as a stepping stone towards future large scale manufacturing of quantum computing systems.

Chapter 1 outlines an overview of our field, highlighting the motivations behind our research and our intended contributions. Chapter 2 details the theory behind our research; the basics of a quantum dot, the functions of the single electron transistor and the characteristics of a coupled double quantum dot (DQD) system.

After this, I go on to summarize in Chapter 3 the most recent and important developments in solid state quantum dot research through a literature review and highlight the most important experimental methods relevant to our work. In Chapters 4 and 5, I outline our contributions to the field and present the design of our SOI based research device. 3D FEM based capacitance simulations of this design are then combined with Monte-Carlo single electron circuit simulations to allow structural analysis and dynamic simulations of device operations to

determine the feasibility of our design. The results from simulations as well as fabrication are presented along with recent measurements of device characteristics and performance. A wide variety of device designs are presented which demonstrates the most recent achievements in e-beam lithography, and the potential of our process to realise more sensitive, complex multi-configurational QD systems in parallel.

I conclude this report in Chapter 6, summarizing our findings, achievements and outlining potential directions for future work.

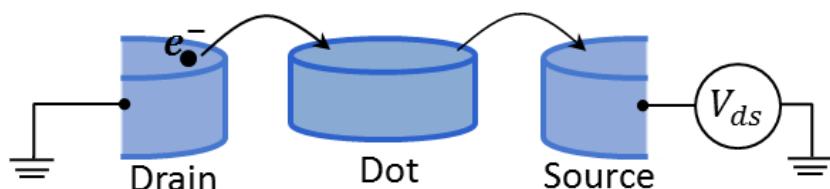


# Chapter 2

## A Theoretical Background

### 2.1 Basics of a quantum dot

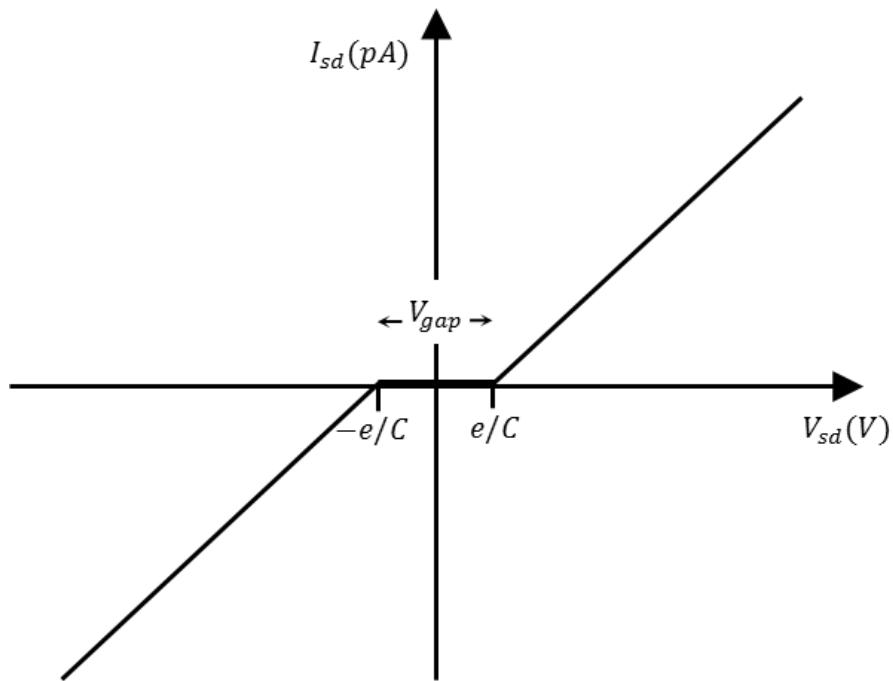
For nanoscale systems, electron transport is strongly influenced by the charging effects of even a single electron due to both the scale of the system and the small yet significant capacitances that exist. A quantum dot (QD) is such a nanoscale system where stored electrons' potential energies become discrete levels due to their very small size. In effect, a quantum dot is a three dimensional potential well where electrons can sequentially tunnel in to fill the quantized states and "charge" the quantum dot.



**Fig. 2.1(a)** Schematic of a nanoscale quantum dot connected to source and drain reservoirs via tunnel barriers (in this case a small air gap). These air gaps provide potential barriers to electron transport through the system and force electrons tunnelling through them when a non-zero source drain current,  $I_{ds}$ , is desired.

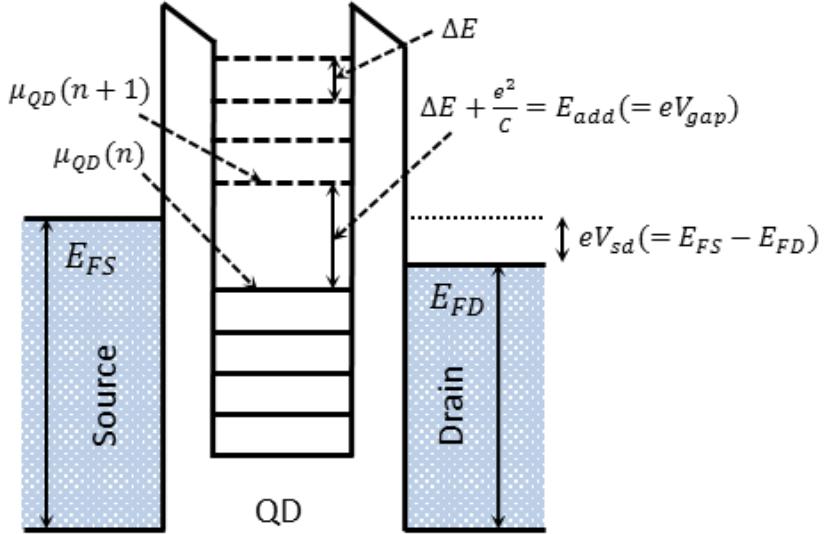
Conventionally, by connecting a conducting source and drain to the QD through electron tunnel barriers (See Fig. 2.1(a) for a schematic view), we can measure the electrical transport properties of such a system. For a spherical quantum dot, its capacitance can be approximated by  $C = 4\pi\epsilon a$  where "a" is the dot's radius and "ε" its permittivity. To observe single electron charging effects at temperature  $T$ , the charging energy of the dot,  $E_c = e^2/C$ , must exceed the thermal energy,  $k_B T$  (where  $k_B$  is the Boltzmann Constant), such that the thermal

energy  $k_B T \ll E_c \approx e^2/4\pi\epsilon a$ . This charging energy arises due to the effects of Coulomb repulsion between an extra electron on the QD and electrons on the source contact. In addition, to ensure a well-defined (constant) number of electrons on the dot, the tunnel barriers' resistance ( $R_t$ ) must be sufficiently large such that  $(C_t R_t)(E_c) > h$  (The energy-time uncertainty principle) where  $h$  is Planck's constant,  $C_t$  is the capacitance of the tunnel barrier and  $C_t R_t$  is the time taken by the electron to tunnel into or out of the dot with a charging energy of  $E_c$ . This in turn means  $R_t > h/e^2$  (for  $C = 4\pi\epsilon a$  and  $E_c = e^2/C$ ) where  $h/e^2$  is the “quantum resistance”.



**Fig. 2.1(b)** A schematic graph of the source to drain current,  $I_{sd}$ , through a quantum dot system as a function of source drain bias voltage  $V_{sd}$  at a temperature of 4.2K where single electron charging effects are dominant.

The expected current  $I_{sd}$  through a quantum dot as a function of source to drain bias voltage  $V_{sd}$  at a temperature of 4.2K is shown schematically in Fig. 2.1(b). In the quantum regime, conduction only occurs when  $V_{sd}$  is sufficiently high such that the electrons' energy at the contacts exceed the charging energy,  $E_c$ , of the dot.

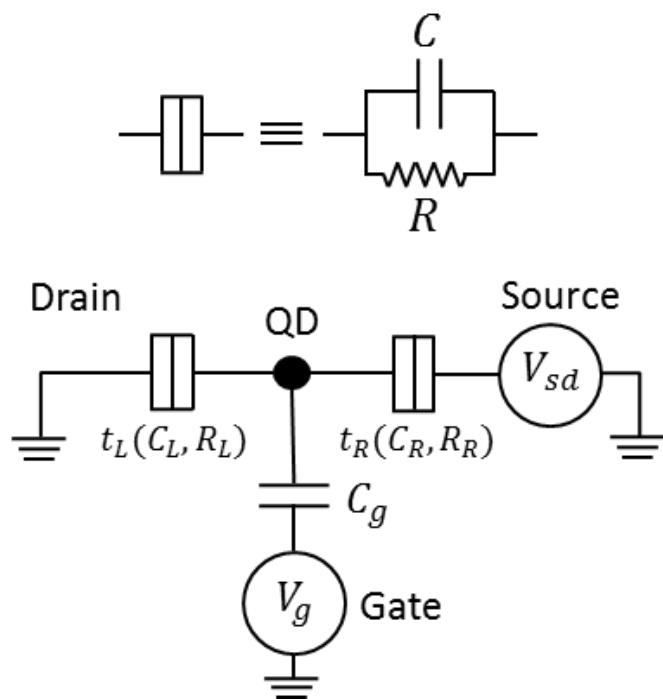


**Fig. 2.1(c)** Schematic energy level diagram of a quantum dot system like that in Fig. 2.1(a) set in the Coulomb blockade region where there are no single electron energy levels (horizontal black solid and dashed lines in the QD) aligned between the source and drain Fermi energies  $E_{FS}$  and  $E_{FD}$ . The horizontal solid and dashed lines represent occupied and unoccupied electron states respectively.  $\mu_{QD}(n)$  is the electrochemical potential of the state with  $n$  electron occupancy.

This is more clearly shown in an QD energy level diagram like that in Fig. 2.1(c) where the condition  $E_{FS} - E_{FD} > E_{add} (= \Delta E + E_c)$  must be satisfied for electrons to successfully tunnel through the potential barriers via quantum dot ( $E_{FS}$  and  $E_{FD}$  are the source and drain Fermi energies respectively,  $E_{add}$  is the difference in energy between the top most occupied and bottom most unoccupied QD electron state and  $\Delta E$  is the energy spacing between two discrete quantum energy levels). Since  $V_{sd} = (E_{FS} - E_{FD})/e$ , in the region  $-e/C < V_{sd} < e/C$  (assuming  $\Delta E \ll e^2/C$ ), the current is therefore expected to be especially small as  $V_{sd}$  cannot provide electrons with enough energy to overcome  $E_{add}$ . This region is called the “Coulomb blockade” region with the “Coulomb gap voltage” being  $V_{gap}$ . Only when a QD energy level lies between  $E_{FS}$  and  $E_{FD}$  can  $I_{sd}$  be non-zero.

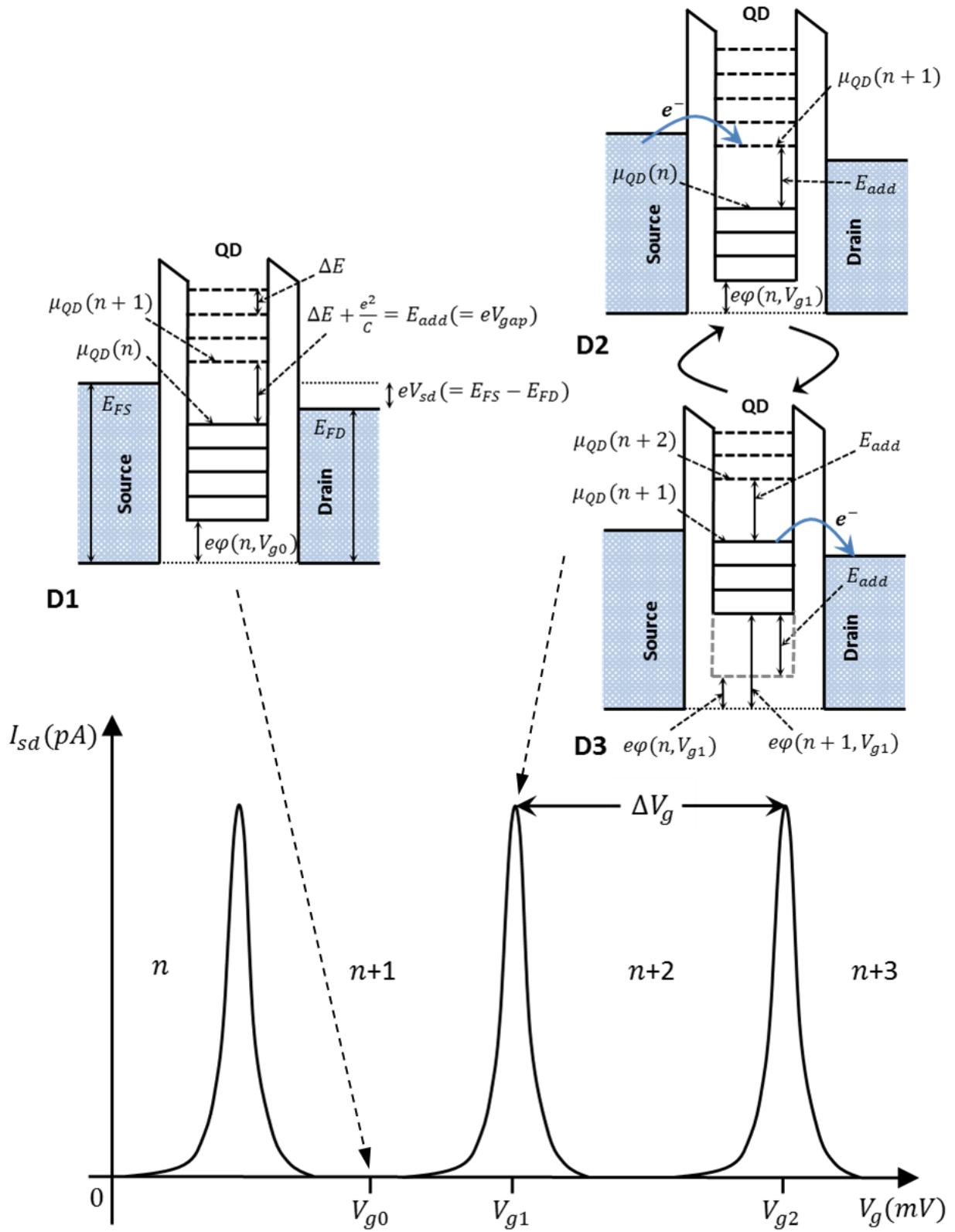
## 2.2 The Single Electron Transistor (SET)

A more useful implementation of the QD can be made by electrostatically coupling one or more “gate” electrodes which can be used to tune the electrostatic potential of the dot with respect to the reservoirs. Such a device (with one gate) known as the single electron transistor (SET) was originally proposed by [7] and can use the single electron charging effect to control the charging of the QD one electron at a time. A schematic circuit diagram of the device looks something like that in Fig. 2.2(a).



**Fig. 2.2(a)** Schematic circuit diagram of a single electron transistor (SET) – a quantum dot (QD) connected via tunnel barriers (“ $t_L$ ” and “ $t_R$ ”) to a source and drain contact and capacitively coupled (through capacitance  $C_g$ ) to a gate electrode. Tunnel barriers (“ $t_L$ ” and “ $t_R$ ”) are represented by a tunnel resistor (“ $R$ ”) and a tunnel capacitor (“ $C$ ”) connected in parallel (see inset above the circuit diagram)

By varying the voltage  $V_g$  applied to the gate electrode, we can gradually vary the electrochemical potential,  $\mu_{QD}$ , of electrons in the QD (See Fig. 2.1(c)) relative to that of the source and drain contacts to produce “Coulomb oscillation” characteristics in  $I_{sd}$  (the SET’s source to drain current). This characteristic (for  $-e/C < V_{sd} < e/C$ ; i.e. low source to drain bias voltage) is schematically drawn in Fig. 2.2(b). For the regions between Coulomb oscillation current peaks, the QD is in its “Coulomb blockade region” and has a stable/constant number,  $n$ , of occupying electrons. No current flows in this regime because there are no QD energy levels aligned between  $E_{FS}$  and  $E_{FD}$  for the electron to flow through.



**Fig. 2.2(b)** Characteristics of the source to drain current,  $I_{sd}$ , through a single electron transistor (SET) (Fig. 2.2(a)) showing distinct “Coulomb onscillations” as a function of gate voltage  $V_g$ . Inset: D1 shows the energy level diagram of the SET system when the QD is in its Coulomb blockade region (same as Fig. 2.1(c)). D2 and D3 shows the energy level diagrams of the two states that the SET system oscillates between when  $I_{sd}$  is at maxima and Coulomb blockade is lifted.

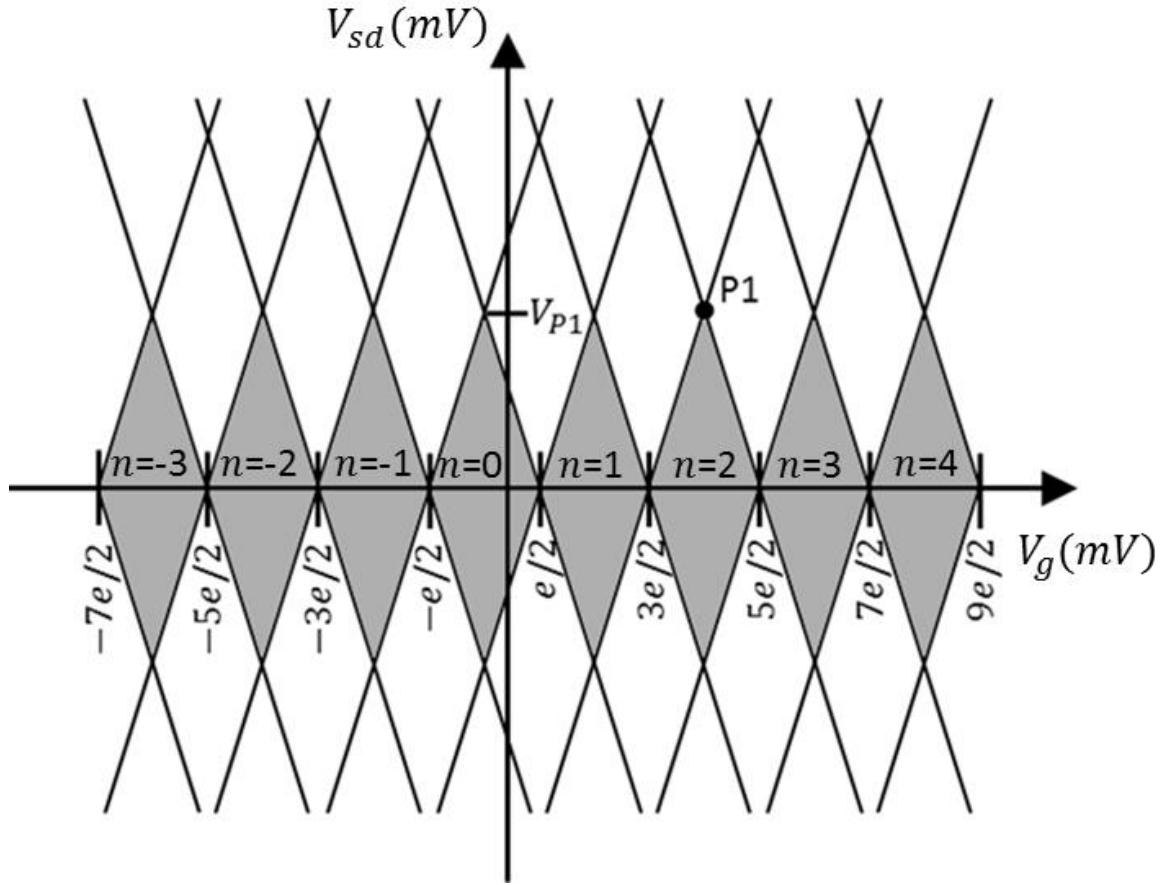
At the position of current peaks, an electron energy state is essentially aligned between  $E_{FS}$  and  $E_{FD}$  (with  $E_{FS} - E_{FD} > 0$ ). This therefore allows electrons to freely flow from source to drain through the QD and in turn lifting Coulomb blockade.

Each Coulomb oscillation peak separates two QD stable charge configurations which differ by one electron. The accompanying schematic energy diagrams (insets D1, D2 and D3) in Fig. 2.2(b) give a clear picture of the positions of the discrete QD electron energy levels relative to its environment at different points of the Coulomb oscillation characteristic. The electrochemical potential is given by [8] as

$$\mu_{QD}(n) = E_n + \varphi(n, V_g) = E_n + \frac{(n-n_0-0.5)e^2}{C} - e \frac{C_g}{C} V_g. \quad \text{Eqn. 2.2(a)}$$

This is defined as the minimum energy required for adding the  $n^{th}$  electron to the QD at a temperature of 0K measured relative to the bottom of the source's conduction band.  $E_n$  is the  $n^{th}$  discrete quantum single electron energy level (with separation  $\Delta E$ ) and  $\varphi(n, V_g)$  is the electrostatic potential of an electron in the QD measured from the base of the source's conduction band to the base of the QD's conduction band.  $n_0$  and  $n$  are respectively the stable excess number of electrons on the QD at  $V_g = 0V$  and  $V_g$ . It's useful to note that  $\mu_{QD}(n+1) - \mu_{QD}(n) = E_{add}$ .

This equation for  $\mu_{QD}(n)$  allows us to evaluate the periodicity of these Coulomb oscillations by allowing for calculations of the difference in  $V_g$  between two successive current peaks. We know that the QD differs by one stable electron between two successive current peaks and that the electrochemical potential is the same at each peak (since the lowest unoccupied QD state will be aligned between  $E_{FS}$  and  $E_{FD}$ ). Therefore, using  $\mu_{QD}(n, V_{g1}) = \mu_{QD}(n+1, V_{g2})$  (where  $V_{g1}$  and  $V_{g2}$  are the  $V_g$  values at two successive current peaks), we can obtain  $V_{g2} - V_{g1} = \Delta V_g = \frac{C}{eC_g} \left( \frac{e^2}{C} + \Delta E \right)$  using Eqn. 2.2(a).



**Fig. 2.2(c)** Schematic charge stability diagram of a SET as a function of the source to drain voltage,  $V_{sd}$ , and the side gate voltage  $V_g$ . Distinct “Coulomb blockade diamonds” can be seen where, in these grey diamond regions, the source to drain current,  $I_{sd} = 0A$ , due the QD being Coulomb blockaded. Elsewhere in the diagram,  $I_{sd} > 0A$ .

When  $I_{sd}$  is plotted as a function of both  $V_g$  and  $V_{sd}$ , periodic “Coulomb blockade diamond” patterns will form in the three dimensional plot. This effect is shown schematically in a charge stability diagram of “ $n$ ” electrons in the QD as a function of  $V_g$  and  $V_{sd}$  (See Fig. 2.2(c)). The parallelogram shaded areas (diamond shapes) represent regions where there is no available QD energy level between  $E_{FS}$  and  $E_{FD}$  for an electron to tunnel through (the “Coulomb blockade diamonds”). Therefore, Coulomb blockade exists in these areas at negligible thermal fluctuations (i.e. low temperatures such that  $T \ll E_c/k_B \approx e^2/4\pi\epsilon k_B a$ ). This is qualitatively explained via the energy level diagrams D1 in Fig. 2.2(b). For low levels of  $V_{sd}$  ( $\approx 0$ ),  $I_{sd}$  as a function of  $V_g$  is essentially the same as that in Fig. 2.2(b). As  $V_{sd}$  increases,  $E_{FS} - E_{FD}$  gets larger, and a QD energy level can lie between  $E_{FS}$  and  $E_{FD}$  for a larger range of  $V_g$  (See D2 in Fig. 2.2(b)). Therefore, the Coulomb blockaded regions decrease in size. At vertex (where  $V_{sd} = V_{P1}$  on Fig. 2.2(c)) of each diamond (e.g. point P1),

Coulomb blockade is fully lifted for all values of  $V_{sd} > V_{P1}$  because  $eV_{P1} = E_{add}$  (which means at least one QD electron energy level will always lie between  $E_{FS}$  and  $E_{FD}$ ). Therefore, we can deduce from a measurement of  $V_{P1}$  the separation in energy levels on the QD. This gives us insight into the QD's energy spectrum. In effect, Coulomb blockade diamonds form due to a combination of the reason for Fig. 2.1(b) and that for Fig. 2.2(b).

## 2.3 Orthodox theory of electron tunnelling through a SET

Currently, the most widely accepted theory for single electron tunnelling through a potential barrier is an “Orthodox” theory first developed by [6]. Since then, there has been much advancement in this field, including the addition of both single electron Coulomb charging effects and quantization effects [9] of a system. The main result from this theory is an expression derived in [10] of the tunnelling rate per unit time through the  $i^{th}$  tunnel barrier,

$$\Gamma_i^+ = \frac{1}{eR_i} \frac{\Delta E_i^+/e}{1 - \exp(-\Delta E_i^+/k_B T)}, \quad \text{Eqn. 2.3(a)}$$

where  $\Delta E_i^+$  is the change in the total electrostatic energy of the system as a result of tunnelling through the potential barrier, “+” (“-”) indicates an electron tunnelling across the barrier from left to right (right to left) and  $R_i$ ,  $e$ ,  $k_B$ ,  $T$  are respectively the tunnel resistance of the barrier, electron charge, Boltzmann's constant and temperature.

An even more practical result from the orthodox theory for electron tunnelling is the “master equation” derived in [10] of the probability,  $\rho_n(t)$ , of finding a SET in a charge state of “ $n$ ” at time “ $t$ ” for a given source drain bias  $V_{sd}$ ,

$$\begin{aligned} \frac{d\rho_n(t)}{dt} = & [\Gamma_L^-(n+1) + \Gamma_R^+(n+1)]\rho_{n+1}(t) + [\Gamma_L^+(n-1) + \Gamma_R^-(n-1)]\rho_{n-1}(t) \\ & - [\Gamma_L^-(n) + \Gamma_L^+(n) + \Gamma_R^-(n) + \Gamma_R^+(n)]\rho_n(t), \end{aligned} \quad \text{Eqn. 2.3(b)}$$

where “ $L$ ” and “ $R$ ” are the left and right tunnel barriers of the SET respectively. From this, we can then derive the currents  $I_L$  and  $I_R$  through the left and right barriers of the SET as,

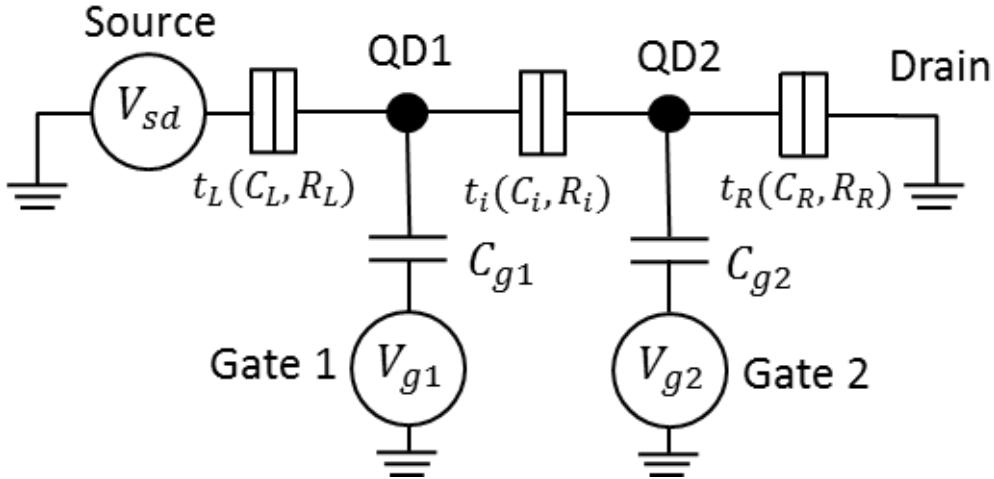
$$I_L = e \sum_n [\Gamma_L^+(n) - \Gamma_L^-(n)]\rho_n(t), \quad \text{Eqn. 2.3(c)}$$

$$I_R = e \sum_n [\Gamma_R^+(n) - \Gamma_R^-(n)]\rho_n(t). \quad \text{Eqn. 2.3(d)}$$

These are very powerful equations which allow us to directly simulate the current response of the SET. However, for more complex systems of greater than two potential barriers, the equations soon become complex and is more appropriately evaluated using, for example, a Monte Carlo simulator. In 1998, Hitachi Cambridge Laboratories [5] developed the “SETSPICE” Monte Carlo single electron circuit simulator which allows simulation of circuit characteristics that include numerous QDs and potential barriers. This uses Eqn. 2.3(a) to form statistical relations and simulate a large number of random tunnelling events. Through averaging of these events, variables of interest (e.g. current or electron occupation in QDs) can be estimated. In chapter 4, we use SETSPICE to simulate both the electrical characteristics of a single spin turnstile device circuit and also the dynamic detection of single electron turnstile operation in a DQD. Although SETSPICE uses the orthodox theory (which deals with a metallic system and neglects quantization effects), it can still qualitatively simulate our device characteristics which have dimensions that mean the quantization effects of our QDs are small compared to single electron charging effects.

## 2.4 Coupled double quantum dots (DQDs)

For electrons in double quantum dots (DQDs), an addition of one electron in one of the QD will electrostatically couple to the second QD and move the positions of its single electron energy levels (electrochemical potentials). In addition, depending on the inter-dot coupling (and inter-dot potential barrier), the single electron wavefunction can spread (de-localise) over the both QDs and electron spin entanglement may occur when both QDs are occupied by electrons. This “tunnel coupling” (which is a quantum effect that only occurs in the presence of strong inter-dot coupling and includes the effect of spin) should be distinguished from “electrostatic coupling” (which is the purely classical effect of electrostatic repulsion that occurs even when there is weak inter-dot coupling). A detailed treatment of the properties of electrons in weakly coupled DQDs is given in [11]. Below we outline the characteristics and behaviours of electrons in DQDs without going into depth on the details of derivations.



**Fig. 2.4(a)** Schematic circuit diagram of two quantum dots,  $QD_1$  and  $QD_2$ , connected respectively via tunnel barriers  $t_L$  and  $t_R$  to a source and drain contact and each capacitively coupled (through capacitance  $C_{g1,2}$  respectively) to a gate electrode. The inter-dot coupling is through tunnel barrier  $t_i$ . Each tunnel barrier is represented by a resistor of resistance  $R$  and capacitor of capacitance  $C$  connected in parallel (see Fig. 2.2(a))

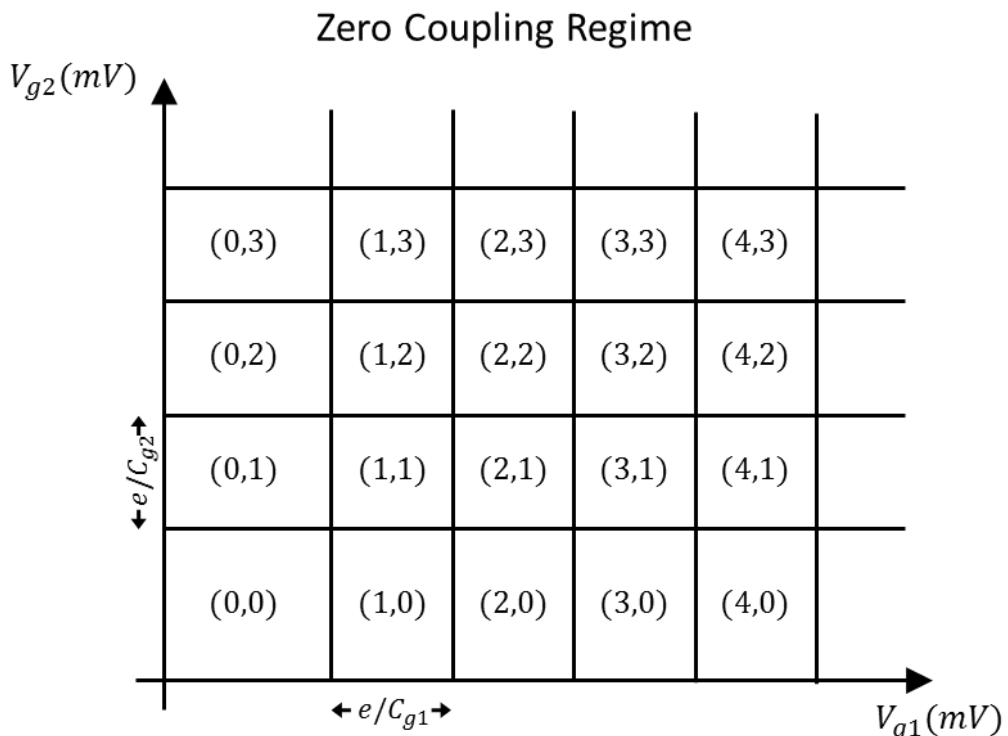
Fig. 2.4(a) shows a circuit schematic of two QDs ( $QD_1$  and  $QD_2$ ) electrostatically coupled respectively (via capacitances  $C_{g1}$  and  $C_{g2}$ ) to two gate electrodes with applied voltages  $V_{g1}$  and  $V_{g2}$ . Their electrochemical potentials  $\mu_1$  and  $\mu_2$  are therefore controlled independently by the gate voltages  $V_{g1}$  and  $V_{g2}$ . Connections of  $QD_1$  to the drain contact and  $QD_2$  to the source contact are via tunnel barriers  $t_L(R_L, C_L)$  and  $t_R(R_R, C_R)$  respectively (where  $R$  and  $C$  are the barriers' resistance and capacitance). The inter-dot coupling between  $QD_1$  and  $QD_2$  is dependent on the tunnel barrier  $t_i(R_i, C_i)$ . In this case, we have neglected the cross capacitances between different components of the device. Eqn. 2.4(a) and 2.4(b) below shows the explicit form of the respective electrochemical potentials in  $QD_1$  and  $QD_2$  (see [8] for their derivation),  $\mu_1(n_1, n_2)$  and  $\mu_2(n_1, n_2)$  (where “ $n_1$ ” and “ $n_2$ ” are the no. of electrons occupying  $QD_1$  and  $QD_2$ ),

$$\mu_1(n_1, n_2) = (n_1 - 1/2)E_{QD1} + n_2E_i + 1/e(C_{g1}V_{g1}E_{QD1} + C_{g2}V_{g2}E_i), \quad \text{Eqn. 2.4(a)}$$

$$\mu_2(n_1, n_2) = (n_2 - 1/2)E_{QD2} + n_1E_i + 1/e(C_{g1}V_{g1}E_i + C_{g2}V_{g2}E_{QD2}), \quad \text{Eqn. 2.4(b)}$$

where  $E_{QD1, QD2}$  are the charging energies of  $QD_1$  and  $QD_2$  respectively (See Chapter 2.1 or [8]),  $e$  is the charge on an electron and  $E_i$  is the electrostatic coupling energy defined as the change in electrostatic potential of one QD when an electron is added to the other QD.

For a source-drain bias of  $V_{sd} \ll (\frac{e}{C_1}, \frac{e}{C_2}, \frac{\Delta E}{e})$  (See Fig. 2.1(b) and [8]) where  $C_1 = C_{g1} + C_i + C_L$  and  $C_2 = C_{g2} + C_i + C_R$  (these are the total capacitances of  $QD_1$  and  $QD_2$  respectively) and  $\Delta E$  is the average energy spacing between two discrete quantum levels in  $QD_1$  and  $QD_2$  (see Fig. 2.1(c)), a schematic plot of the “charge stability diagram” of the DQD as a function of  $V_{g1}$  and  $V_{g2}$  (using Eqn. 2.4(a) and (b)) is shown in Fig. 2.4(b) in the limit of negligible inter-dot coupling (i.e.  $C_i \ll C_1$  and  $C_2$ ) . This condition ensures that we are in the very weak electrostatic coupling regime (no “tunnel coupling”) between  $QD_1$  and  $QD_2$  and that their respective electrochemical potentials  $\mu_1(n_1, n_2)$  and  $\mu_2(n_1, n_2)$  become  $\mu_1(n_1, n_2) = \mu_1(n_1)$  and  $\mu_2(n_1, n_2) = \mu_2(n_2)$  ; i.e. each QD’s respective electrochemical potential become independent of the electron occupation in the other QD.



**Fig. 2.4(b)** Schematic charge stability diagram for an uncoupled double quantum dot (DQD) as a function of side gate voltages  $V_{g1}$  and  $V_{g2}$  (See Fig. 2.4(a) for the system schematic circuit). The equilibrium electron occupation of  $QD_1$  and  $QD_2$  is depicted as  $(n_1, n_2)$  respectively.

The vertical and horizontal lines on Fig. 2.4(b) separates each square region of stable charge configuration on the DQD labelled  $(n_1, n_2)$ . Since we are in the limit of negligible inter-dot coupling,  $V_{g1}$  and  $V_{g2}$  thus only affect “ $n_1$ ” and “ $n_2$ ” respectively. No current flows in the body of the square regions of stable charge configuration because there are no QD energy levels (in either QD) aligned between  $E_{FS}$  and  $E_{FD}$  for the electron to flow through; i.e. “ $n_1$ ”

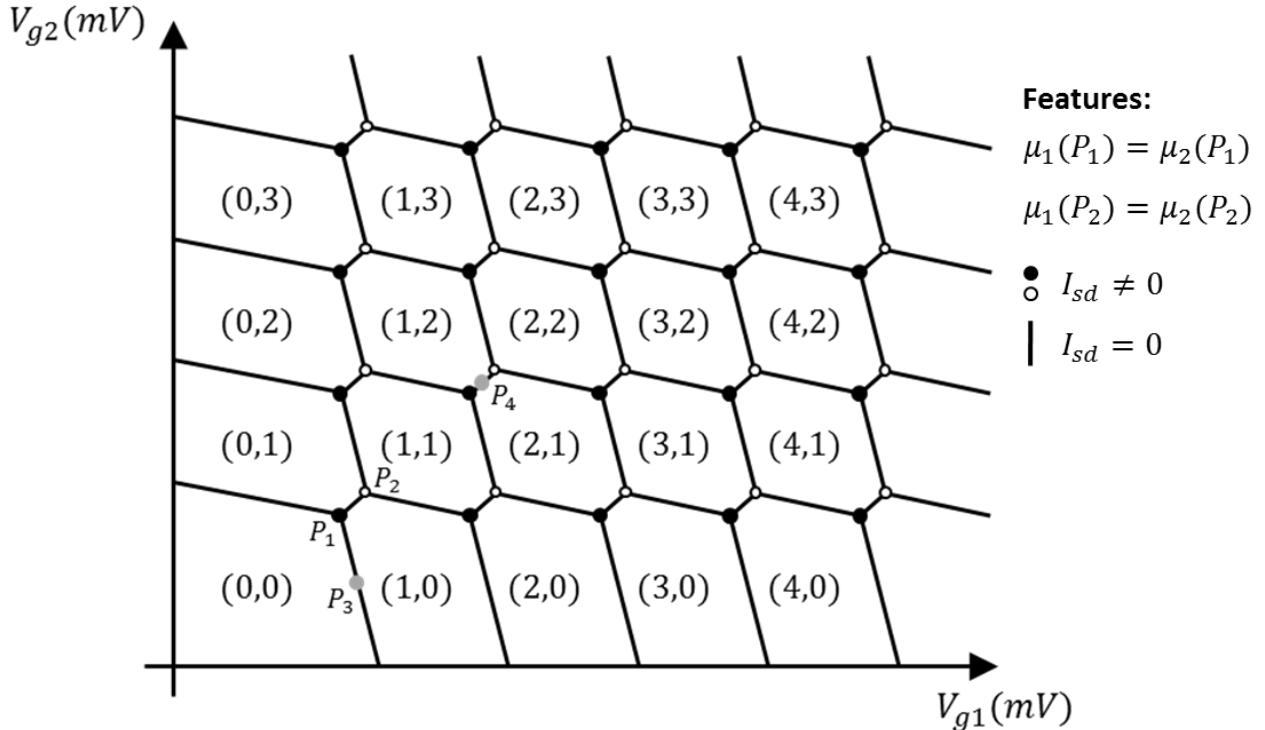
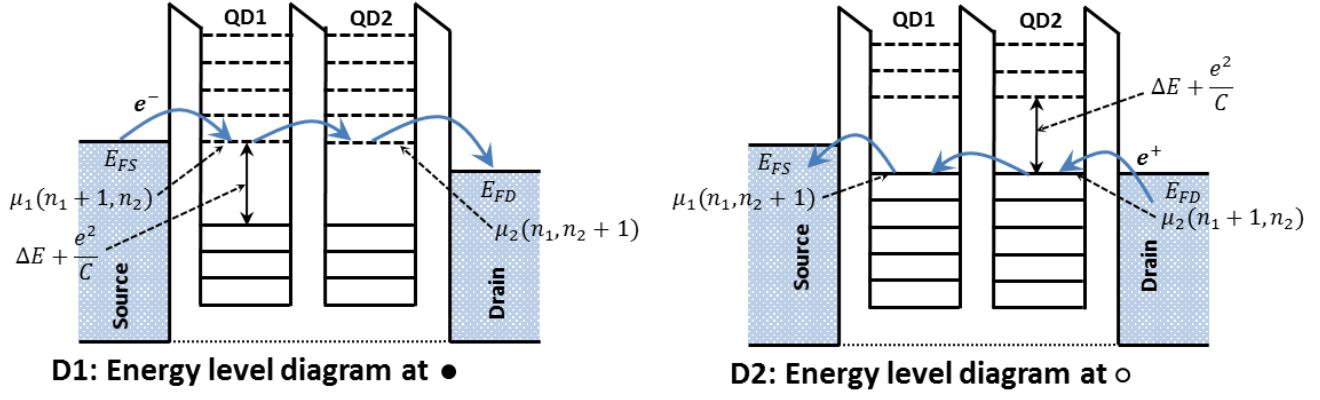
and “ $n_2$ ” are the largest numbers for which the electrochemical potentials satisfy  $\mu_1(n_1, n_2) < E_{FD}$  and  $\mu_2(n_1, n_2) < E_{FS}$  where (like before),  $E_{FD}$  and  $E_{FS}$  are respectively the Fermi energies at the drain and source contacts. Along the vertical lines,  $\mu_1$  lies between  $E_{FD}$  and  $E_{FS}$  and along the horizontal lines,  $\mu_2$  lies between  $E_{FD}$  and  $E_{FS}$ . At the points where the horizontal and vertical lines cross, the electrochemical potential of both QDs are aligned such that  $\mu_1(n_1) = \mu_2(n_2)$  and lie between  $E_{FD}$  and  $E_{FS}$ . These are the only points where there is a non-zero current from source to drain ( $I_{sd} \neq 0A$ ) through the DQD system.

When the two QDs are weakly coupled (i.e.  $C_i < C_1$  and  $C_2$ ), the Coulomb blockaded regions of charge stability (Square regions labelled “ $(n_1, n_2)$ ” on Fig. 2.4(b)) become hexagonally shaped and the boundaries become slightly tilted (See Fig. 2.4(c)). This is due to a finite “tunnel coupling” now present between the two QDs which in turn means  $\mu_1 = \mu_1(n_1, n_2)$  and  $\mu_2 = \mu_2(n_1, n_2)$ . The corners of each of the square regions on Fig. 2.4(b) also become split into two separate points (e.g. points  $P_1$  and  $P_2$  on Fig. 2.4(c)) each called a “triple point” since they’re now shared between three regions of charge stability (each labelled “ $(n_1, n_2)$ ”). This results in the “honeycomb” like pattern in Fig. 2.4(c).

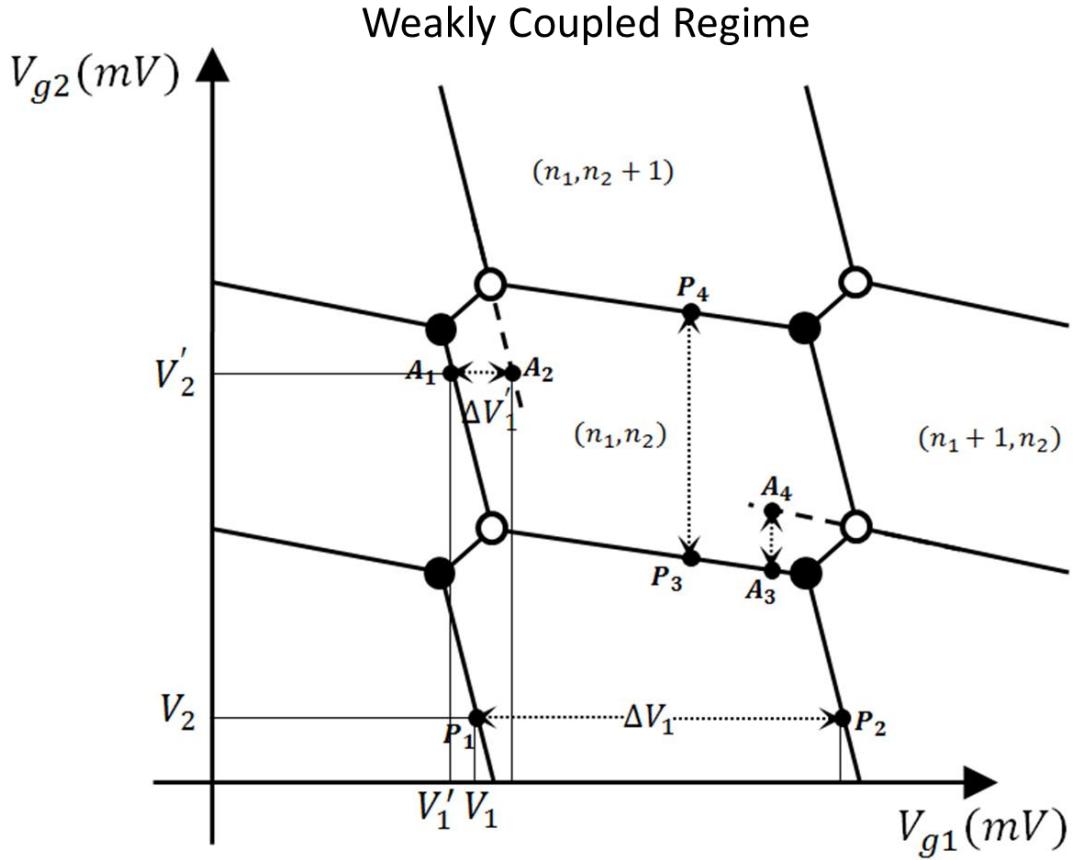
At the triple point  $P_1$ ,  $\mu_1(1,0) = \mu_2(0,1)$  and lies between  $E_{FD}$  and  $E_{FS}$  (see inset D1 on Fig. 2.4(c)). Since the coupling energy,  $E_i$ , is the same for both dots;  $\mu_1(1,1) - \mu_1(1,0) = \mu_2(1,1) - \mu_2(0,1)$ . Therefore, at point  $P_2$ ,  $\mu_1(1,1) = \mu_2(1,1)$  and also lies between  $E_{FD}$  and  $E_{FS}$  (See inset D2 on Fig. 2.4(c)). What this means is that Coulomb blockade is “lifted” at these triple points through electron tunnelling (black circles, e.g. point  $P_1$ ) and hole tunnelling (white circles, e.g. point  $P_2$ ) across the DQD system which in turn means  $I_{sd} \neq 0A$ . These transfer process are explained schematically via the energy level diagrams D1 and D2 on Fig. 2.4(c) (which are for general DQD electron occupation of  $n_1$  and  $n_2$ ). For point  $P_1$ , electron tunnelling occurs from source to drain as the QDs goes through the charge state sequence  $(0,0) \rightarrow (1,0) \rightarrow (0,1) \rightarrow (0,0)$ . Similarly, for point  $P_2$ ,  $I_{sd} \neq 0A$  because hole tunnelling occurs from drain to source as the QDs goes through the charge state sequence  $(1,1) \rightarrow (1,0) \rightarrow (0,1) \rightarrow (1,1)$ . Although we have concentrated only on the triple points between the  $(0,0)$  and  $(1,1)$  states, the processes described above apply for all triple points between any  $(n_1, n_2)$  and  $(n_1 + 1, n_2 + 1)$ . Elsewhere on the charge stability diagram (Fig. 2.4(c)),  $I_{sd} = 0A$  since the system is Coulomb blockaded; e.g. at point  $P_3$  (Grey circle) along the boundary of a hexagon, the electrochemical potentials of the two QDs aren’t aligned with each other, so no electron can tunnel through both QD systems. Similarly, at point  $P_4$  (Grey

circle) along the boundary joining  $P_1$  and  $P_2$ , the system is Coulomb blockaded again but this time despite the electrochemical potentials of the two QDs aligning with respect to each other, they aren't aligned with that of the source and drain so again  $I_{sd} = 0A$ .

### Weakly Coupled Regime



**Fig. 2.4(c)** Schematic charge stability diagram for a weakly electrostatically coupled double quantum dot (DQD) as a function of side gate voltages  $V_{g1}$  and  $V_{g2}$  (See Fig. 2.4(a) for the system schematic circuit). The equilibrium electron occupation of  $QD_1$  and  $QD_2$  is depicted as  $(n_1, n_2)$  respectively. A “honeycomb” like pattern can be clearly seen. The source to drain current is zero along the boundary and body of each hexagon. Current is only non-zero at the triple points shared between three hexagonal regions. Inset: D1 and D2 are schematic energy level diagrams representing the process for electron and hole flow through the DQD system at the triplet points (black and white circles respective) which allow for non-zero source to drain current.



**Fig. 2.4(d)** Schematic plot focused on a hexagonal cell of the charge stability diagram of a weakly electrostatically coupled DQD (See Fig. 2.4(c)).

Through analysing the periodicity that exists in a plot like Fig. 2.4(c), we can potentially extract the capacitance values that exist between different components of the device (See Fig. 2.4(a)). Fig. 2.4(d) shows a schematic plot focused on one of the charge stability hexagons in Fig. 2.4(c). The electrochemical potential of  $QD_1$  at points  $P_1$  and  $P_2$  of Fig. 2.4(d) are equal. Therefore, through Eqn. 2.4(a) and the condition  $\mu_1(n_1, n_2; V_1, V_2) = \mu_1(n_1 + 1, n_2; V_1 + \Delta V_1, V_2)$ , we can obtain the relation,

$$\Delta V_1 = e/C_{g1}. \quad \text{Eqn. 2.4(c)}$$

Similarly with  $QD_2$  and equating its electrochemical potential,  $\mu_2$ , at points  $P_3$  and  $P_4$  on Fig. 2.4(d), we can obtain the relation,

$$\Delta V_2 = e/C_{g2}. \quad \text{Eqn. 2.4(d)}$$

In addition, at points  $A_1$  and  $A_2$  on Fig. 2.4(d),  $QD_1$ 's electrochemical potential are also equal,  $\mu_1(n_1, n_2; V'_1, V'_2) = \mu_1(n_1, n_2 + 1; V'_1 + \Delta V'_1, V'_2)$ , and with Eqn. 2.4(a) gives,

$$\Delta V'_1 = \Delta V_1 C_i / C_2. \quad \text{Eqn. 2.4(e)}$$

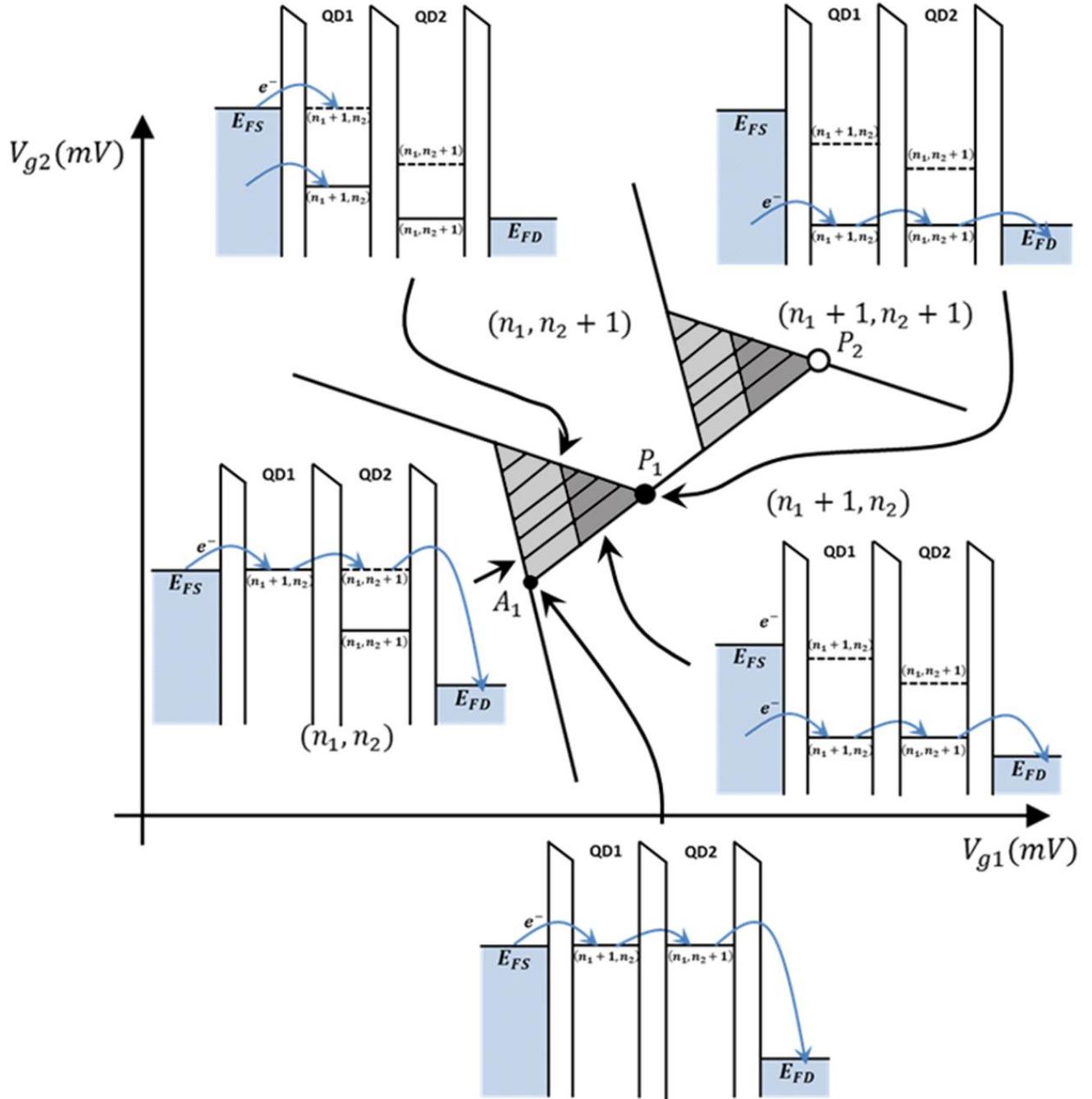
Again, through a similar method of equating  $\mu_2$  at points  $A_3$  and  $A_4$  on Fig. 2.4(d), we can obtain the relation,

$$\Delta V'_2 = \Delta V_2 C_i / C_1. \quad \text{Eqn. 2.4(f)}$$

We have so far analysed the characteristics of a DQD device in the limit of small source drain voltage  $V_{sd} \approx 0 \ll (\frac{e}{C_1}, \frac{e}{C_2}, \frac{\Delta E}{e})$ . When  $V_{sd}$  is increased, the triple points on Fig. 2.4(c) develop into triangular regions of finite conductance (See Fig. 2.4(e)) known as “bias triangles”. Here, two different types of electron tunnelling occur to allow for current through the DQD system. The first is *elastic* tunnelling which occurs only when the two QD’s energy levels are aligned (what we have discussed up till now) and lie between  $E_{FD}$  and  $E_{FS}$ . The second is *inelastic* tunnelling where there is an energy mismatch between the energy levels of the two QDs (but they still lie between  $E_{FD}$  and  $E_{FS}$ ). Due to the system having to conserve energy as a whole, energy exchange with the surrounding environment (through photon or phonon absorption or emission) needs to take place to compensate for the energy mismatch in levels. At cryogenic temperatures, the number of photons and phonons is negligibly small and thus makes inelastic tunnelling a second-order process which is much lower in magnitude than the elastic tunnelling rate. However, when elastic tunnelling can’t occur, inelastic tunnelling dominates.

We can understand electron transport in the bias triangle regions through an energy level analysis. The electron transport methods in the triangle originating from point  $P_1$  are analogous to that for  $P_2$  except transport there is via holes instead of electrons. Along the bottom right edge of the triangle with  $P_1$  (i.e. the edge connected to the line joining  $P_1$  and  $P_2$ ), elastic tunnelling occurs because  $\mu_1(n_1 + 1, n_2) = \mu_2(n_1, n_2 + 1)$ . Moving along a line of this same slope anywhere within the plot will not change the relative alignment of the levels in the two QDs however it will change their common alignment with respect to  $E_{FD}$  and  $E_{FS}$ . Only the ground state of the QDs (represented by the black lines on Fig. 2.4(e)) are involved here since they are aligned and elastic tunnelling is possible. The dashed lines represent excited states on the two quantum dots. These excited states arise mainly due to the presence of electron spin degrees of freedom and the Pauli Exclusion Principle which allow for potential non-degeneracy in spin states. They therefore provide a means for *inelastic* tunnelling from source to drain when the ground states of the QDs are not aligned between  $E_{FD}$  and  $E_{FS}$ .

## Weakly Coupled Regime with a larger source to drain bias



**Fig. 2.4(e)** Schematic plot of ‘bias triangles’ formed at the triple points of a charge stability diagram (See Fig. 2.4(c)) of a double quantum dot (DQD) system (See Fig. 2.4(a)) as a result of an applied source drain voltage  $V_{ds}$ . Within this bias triangle, conduction through the DQD system is energetically allowed at certain points. Insets show the energy level diagrams of electrons within each quantum dot and the corresponding method for electron transport at different points on the bias triangle (for triple point  $P_1$ ) where conduction is energetically allowed.

Along the left edge of the bias triangle, only  $\mu_2(n_1, n_2 + 1)$  changes (See Fig. 2.4(e)).  $\mu_1(n_1 + 1, n_2)$  stays constant and aligned with  $E_{FS}$ . At point  $A_1$  (lowest corner of the

triangle) elastic tunnelling occurs through the ground states since  $\mu_1(n_1 + 1, n_2) = \mu_2(n_1, n_2 + 1)$ . As we move up the left edge of the triangle,  $\mu_2(n_1, n_2 + 1)$  gets lowered and misaligned with  $\mu_1$  such that only inelastic tunnelling occurs and there is a significant drop in  $I_{sd}$  across the DQD. However, at a certain point,  $\mu_2$  will be pulled so low that an excited state for  $QD_2$  is dragged below  $E_{FS}$ . When this  $(n_1, n_2 + 1)$  excited state is aligned with the  $(n_1 + 1, n_2)$  ground state, elastic tunnelling can again occur and  $I_{sd}$  increases. At this point, moving into the triangle along a line parallel to the bottom right edge would result in these energy levels maintaining their alignment, giving a line of greater  $I_{sd}$ . Multiple excited states would give multiple such lines across the body of a bias triangle, and potentially reveal the energy spectrum of the quantum dot. Above the top corner of the triangle,  $\mu_2(n_1, n_2 + 1)$  falls below  $E_{FD}$  and the system is Coulomb blockaded.

Along the top edge of the bias triangle, only  $\mu_1(n_1 + 1, n_2)$  changes (See Fig. 2.4(e)).  $\mu_2(n_1, n_2 + 1)$  stays constant and aligned with  $E_{FD}$ . As we move down this edge,  $\mu_1$  is pulled lower with respect to  $E_{FS}$  and when an excited state for  $QD_1$  is also pulled below  $E_{FS}$ , there will be two paths available for electrons to tunnel from source to  $QD_1$ . A different  $I_{sd}$  will therefore result from this and will show up as indicated by the smaller grey triangle in the bias triangle.

It should be noted here that when a QD has two electrons occupying it, the spins of these electrons result in four possible spin states. One singlet state (anti-symmetric with respect to particle exchange),  $S(0,2)$ , and three triplet states  $T_+(0,2)$ ,  $T_0(0,2)$  and  $T_-(0,2)$ . These combined with the electrons' spatial wavefunctions and the Pauli Exclusion Principle give a set of overall wavefunctions describing the electron density in the QD and results in a series of discrete quantised energy levels. Due to the requirement of spin conservation, electron transport through the DQD system is governed by spin selection rules and may lead to a phenomenon called "Pauli spin blockade". This occurs when transport from  $QD_1$  to  $QD_2$  is blocked because an energy level (energetically accessible) in  $QD_2$  is inaccessible purely due to a required electron spin orientation. This effect is explored further in the literature review section below where we analyse experimental achievements in spin blockade detection. For a detailed explanation of quantum physics and single and triplet states please see [12]). Detailed reviews about single electron charging effects and quantum confinement effects in nanostructures can be found in [8], [13] and [14].



# Chapter 3

## An Experimental Review

### 3.1 Introduction

The potential to use individual electron spin states in a semiconductor quantum dot (QD) for quantum information processing has triggered a stream of experimental investigations in recent years to detect and manipulate single spins in the few electron limit.

Over the last few years, the bulk of the study has been focused on GaAs-based QD systems and it is within these where the essential requirements of controlling, measuring and manipulating single electron spin states have been demonstrated to a large extent. The reason behind this rapid advancement in GaAs as opposed to Si (which seems like a natural choice given its dominant use in the semiconductor industry) is partly due to the relative fabrication ease in creating very uniform and clean GaAs/AlGaAs heterostructures compared to in Si where there are a myriad of challenges when trying to remove charge traps, impurities and fixed charge effects which prohibit clean device operation. With these GaAs heterostructures, QDs could be defined via electrical gating of a 2 dimensional electron gas (2DEG) formed with lithographically defined gate electrodes. Lateral confinement of electrons (and thus formation of a QD) is then provided by applying negative voltages to gate electrodes which push electrons into small localized regions of the 2DEG and increases electron energy level spacing.

This platform was therefore a quick approach which enabled faster development of methods to understand single electron charge and spin dynamics in semiconductor QDs. The physics

behind many of the approaches developed however are entirely general and can be fully applied to new material systems.

Recently, through this progress on GaAs and the continual refinement of fabrication processes and advancements in Si fabrication methodologies, there has been significant development in the area of Si QDs with successes in both single electron charge and spin manipulation. As mentioned in Chapter 1, Si brings many advantages to the table by offering relatively smaller spin-orbit coupling and a spin-zero nuclear background which reduces the effects of hyperfine interactions for spin qubits compared to GaAs. One of the key challenges in working with Si however is due to its electrons' effective mass being relatively heavier than in GaAs. This in turn makes the confinement potential energy relatively smaller and to obtain quantum confined electronic states it is necessary to fabricate much smaller nano-devices and QDs. Refinement of fabrication techniques are thus key in paving the way towards future large scale fabrication of repeatable functioning silicon QD systems to ensure their practicality and usefulness. Recent advancements in electron beam lithography and fabrication methods are now enabling the realisation of ever smaller QD systems.

In the sections below, we go through a brief review of the experimental techniques developed for single electron manipulation in QDs and review recent advancements in Si based QD research, correlating them to our work. Crucially however, there has been a lack within literature of a more focused investigation into developing standardised processes or approaches which could enable fabrication of scalable QD systems with repeatable characteristics on a large scale. This is the focus of our work following this literature review.

### 3.2 Electron spin initialization and readout

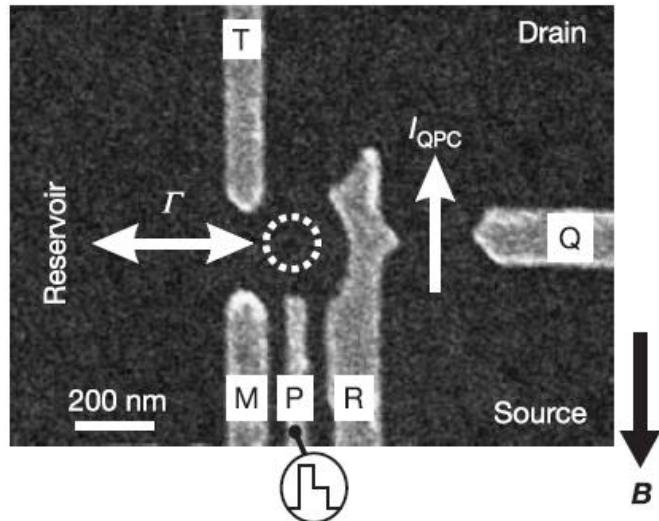
One of the core requirements in being able to realise quantum information processing is the ability to initialize and actually read qubit states. In the case of semiconductor QDs, this means being able to read the spin states of single electrons. Many techniques exist in performing electron spin readouts. Although direct detection of the small magnetic moment (on the order of  $\mu_B = 9.2741 \times 10^{-24} JT^{-1}$  [15]) of a single spin  $1/2$  is difficult, [16] managed to detect a single spin in  $SiO_2$  using magnetic resonance force microscopy (MRFM). Other proposals exist, including optical techniques which with ultrafast laser technology allows for clear advantages in the speed at which single spin states can be optically manipulated and detected. The ability to individually filter electron spins is fundamental for spin initialization

and readout. The sections below review previous work which have achieved purely electrical methods for readout and initialization of electron spins via spin filter methods. Electrical readout is preferred here due to its advantageous compatibility with existing signal processing methods and technologies. Additionally, we discuss the many different platforms explored, focusing on their device architectures and correlating this to our work.

### 3.2.1 Single shot electron spin readout

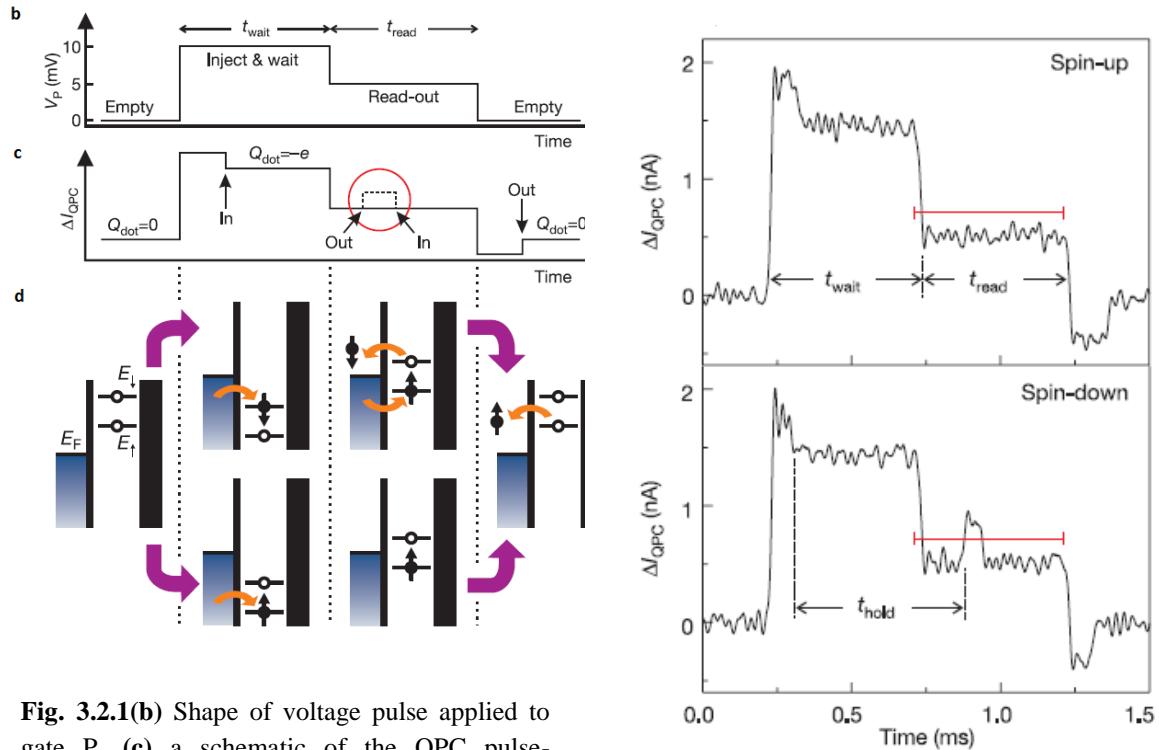
[17] was the first to demonstrate electrical single-shot measurements of an individual electron spin state in a GaAs quantum dot. A “spin to charge conversion” method [18] was used whereby information stored in electron spin degrees of freedom are transferred to orbital degrees of freedom. A scanning electron micrograph (SEM) of a device used in measurements by [17] is shown in the left figure in Fig.3.2.1(a). T, M, P, R and Q on the SEM in Fig. 3.2.1(a) are metallic gates deposited on the surface of a AlGaAs/GaAs heterostructure containing a 2 dimensional electron gas (2DEG) 90 nm below the surface with electron density  $2.9 \times 10^{15} m^{-2}$ . This type of 2DEG set up has become the convention in quantum dot research on GaAs and is present in many of the major works in this area which are reviewed in following sections. The top AlGaAs layer of the substrate creates the 2DEG in the underlying GaAs layer. Through applying negative voltages to the gates electrodes M, R and T, the 2DEG directly below the gates is depleted and this creates a potential minimum to form a quantum dot (dotted white circle in Fig. 3.2.1(a)).

The dot is then electrostatically coupled to a quantum point contact QPC which is operated as a charge detector. For a single electron trapped in the quantum dot, spin to charge conversion is possible when a magnetic field  $B$  is applied to split the single electron spin- $\uparrow$  and spin- $\downarrow$  states by the Zeeman energy,  $H_z = -gBe/m_e$  (where  $g$  is electron  $g$ -factor,  $e$  is the electronic charge and  $m_e$  the effective electron mass in GaAs). The dot potential is then tuned via gate P such that if the electron has spin- $\downarrow$  it will leave, whereas it will stay on the dot if it has spin- $\uparrow$  (i.e. the Fermi energy of the reservoir,  $E_F$ , sits between these two levels with  $H_z >$  Thermal energy) (see the 3<sup>rd</sup> column in Fig 3.2.1(b)). The QPC is set in the tunnelling regime (with conductance  $\sim e^2/h$ ) such that the current  $I_{QPC}$  through the QPC is very sensitive to electrostatic changes [19]. Measurement of the charge (and in turn the original spin state) on the dot is therefore done via recording changes in  $I_{QPC}$  (i.e. measuring  $\Delta I_{QPC}$ ).



**Fig. 3.2.1(a)** SEM of a single quantum dot GaAs heterostructure. [17]

Fig. 3.2.1(b), (c) and (d) below shows the 3 stage measurement procedure used: (1) empty the dot, (2) inject one electron with random spin and wait for time  $t_{wait}$  and (3) measure its spin state. The voltage pulses (three level pulse technique) applied to gate P (Fig. 3.2.1(b)) controls the 3 stages and shifts the dot's energy levels (Fig. 3.2.1(d)) respectively.



**Fig. 3.2.1(b)** Shape of voltage pulse applied to gate P. **(c)** a schematic of the QPC pulse-response if the injected electron has spin- $\uparrow$  (solid line) and spin- $\downarrow$  (dotted line: the only difference is during the readout stage). **(d)** The corresponding behaviour of energy levels of the quantum dot. [17]

**Fig. 3.2.1(e)**  $\Delta I_{QPC}$  versus time during measurement procedure [17]

The results (Fig. 3.2.1(e)) from  $\Delta I_{QPC}$  measurements clearly show the expected behaviour (Fig. 3.2.1(c)) and success in single electron spin readout. In addition, an exponential fit to a plot of the fraction of spin down electrons detected vs  $t_{wait}$  (sampling 625 traces for every  $t_{wait}$  value) showed, at a magnetic field of  $B = 8T$ , a single spin relaxation time of  $T_1 = (0.85 \pm 0.11)ms$  (this is the time  $t_{wait}$  it takes for the probability of detecting an electron spin down state to decay by  $e^{-1}$  compared to when  $t_{wait} = 0$ ). The probability of an electron occupying a spin- $\downarrow$  state is expected to decrease with  $t_{wait}$  because its spin- $\uparrow$  in this case will be lower in energy. Therefore, given enough time, electrons in the spin- $\downarrow$  state will tend to relax into the spin- $\uparrow$  state.

Despite the estimate of errors given for  $T_1$ , a central question is the reliability of the experimental results for single spin readout. This issue was briefly addressed in [17] where a value for the fidelity of measurement was evaluated to be  $\sim 0.93$  and  $\sim 0.72$  for spin- $\uparrow$  and spin- $\downarrow$  states respectively giving a measurement visibility in single-shot measurements of 65%. The authors also suggest that significant improvements to this visibility can be made by lowering the electron temperature (thus reducing thermal energy) and by making faster charge measurements.

This in turn leads to the major drawback of this energy selective readout (E-RO) technique in that it relies on a very large Zeeman splitting of the spin states and precise positioning of these levels with respect to the Fermi energy of the reservoir ( $E_F$ ). E-RO technique is therefore only effective at very low electron temperatures (where electron thermal energy  $\ll$  energy splitting between states) and high magnetic fields ( $B \geq 8T$  in [17] which are experimentally difficult to achieve. In addition, fluctuations in the electrostatic potential and background charge fluctuations can easily push the levels out of the readout configuration.

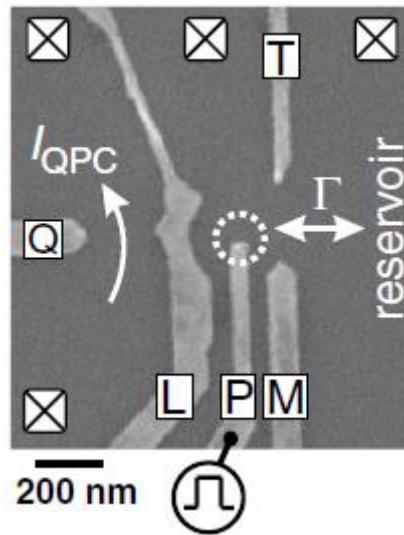
In terms of the device architecture, one of the greatest advantages is that it is relatively fast to fabricate, requiring only one layer of lithography to define the top metal gates. In addition, using an AlGaAs/GaAs heterostructure substrate utilises standardised industry based processes widely implemented and perfected in production of GaAs based transistors or lasers.

However, although such device designs enable rapid fabrication and progress to be made in exploring and understanding single electron charge and spin control mechanisms, the architecture does have its limitations. Primarily, the need for 4 gate electrodes as well as a

reservoir and drain required a total of 8 different voltage sources to form a single QD compared to only 3 required for conventional CMOS transistors. This significantly limits the future scalability in the quantum architecture when expanding to integrated multi-configurational QD systems for quantum information processing. In addition, the use of multiple metal gates dramatically increases the potential for leakage from gates to the GaAs substrate through the thin AlGaAs layer. This in turn could potentially limit the fabrication yield if large numbers of devices were fabricated in parallel.

### 3.2.2 Tunnel rate spin readout

To further the work by [17], Hanson et al [20] proposed spin readout which exploits the difference in *tunnel rates* instead of the energy difference between spin states and the electron reservoir in the presence of a magnetic field. They implemented a spin to charge conversion method much like [17] however this tunnel rate readout (TR-RO) is robust against charge noise and useable even when the electron temperature exceeds the energy splitting between the two spin states.

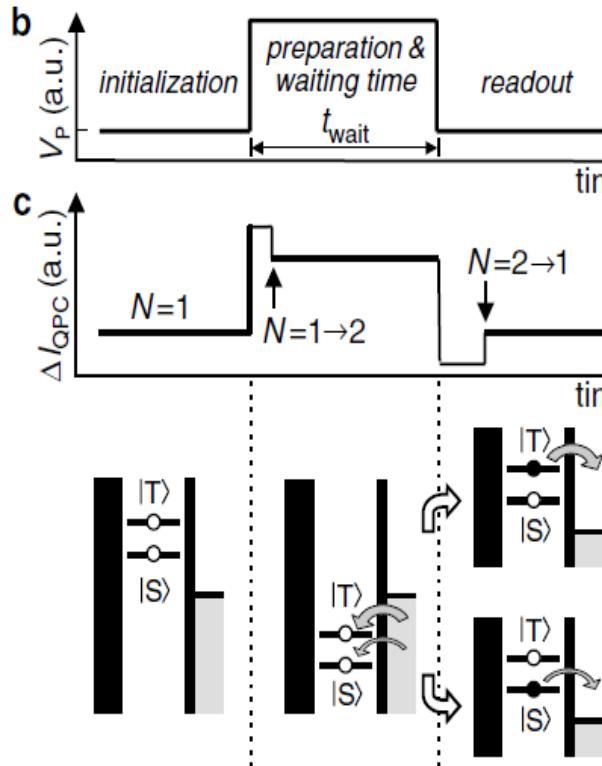


**Fig. 3.2.2(a)** SEM of a single quantum dot GaAs heterostructure [20]

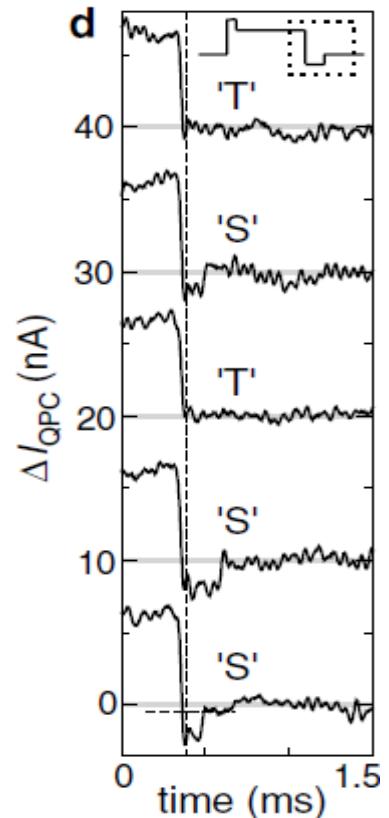
The spin-singlet ground state ( $|S\rangle$ ) and the spin-triplet state ( $|T\rangle$ ) of a two electron GaAs quantum dot (Fig. 3.2.2(a)) were used as qubits and a QPC as the detector. The tunnel rate from  $|T\rangle$  to the reservoir ( $\Gamma_T$ ) is greater than that from  $|S\rangle$  ( $\Gamma_S$ ) due to the first excited orbital state having more weight near the edge of the dot [21], i.e.  $\Gamma_T \gg \Gamma_S$ . Spin selective readout could then be carried out in a similar fashion to that on Fig. 3.2.1(b) except at the readout stage both spin states are pulsed above  $E_F$  (the Fermi energy of the reservoir) and

$t_{read}$  (readout time) is set such that  $\Gamma_T^{-1} \gg t_{read} \gg \Gamma_S^{-1}$ . Therefore, after time  $t_{read}$  an electron will have tunneled off the dot if the state was a  $|T\rangle$  but no tunnelling would have occurred if the state was a  $|S\rangle$ . Spin information could thus be converted to charge information. Fig. 3.2.2(b-d) below outlines the concept of the TR-RO technique.

Results (Fig. 3.2.2(d)) showed that the  $\Delta I_{QPC}$  trace for  $|T\rangle$  and  $|S\rangle$  were clearly distinguishable.  $\Gamma_T$  and  $\Gamma_S$  were tuned to  $2.5\text{kHz}$  and  $50\text{kHz}$  respectively and  $I_{QPC}$  was sent through an external  $20\text{kHz}$  low-pass filter such that tunnel events from  $|T\rangle$  were not resolved on the timescale shown but tunnelling from  $|S\rangle$  was. A value for triplet-to-singlet relaxation time of  $T_1 = (2.58 \pm 0.09)\text{ms}$  was also obtained which was more than twice the *single spin* relaxation time  $T_1 = (0.85 \pm 0.11)\text{ms}$  from [17]). Similarly, the fidelity of measurement for  $|T\rangle$  and  $|S\rangle$  were 96% and 85% respectively, giving a single-shot readout visibility of 81% which was again higher than that for split single electron spin states. A drawback of the TR-RO technique however is that it requires vastly different



**Fig. 3.2.2(b)** Shape of voltage pulse applied to gate P. (c) a schematic of the QPC pulse-response and below it the corresponding behaviour of energy levels of the quantum dot. [20]

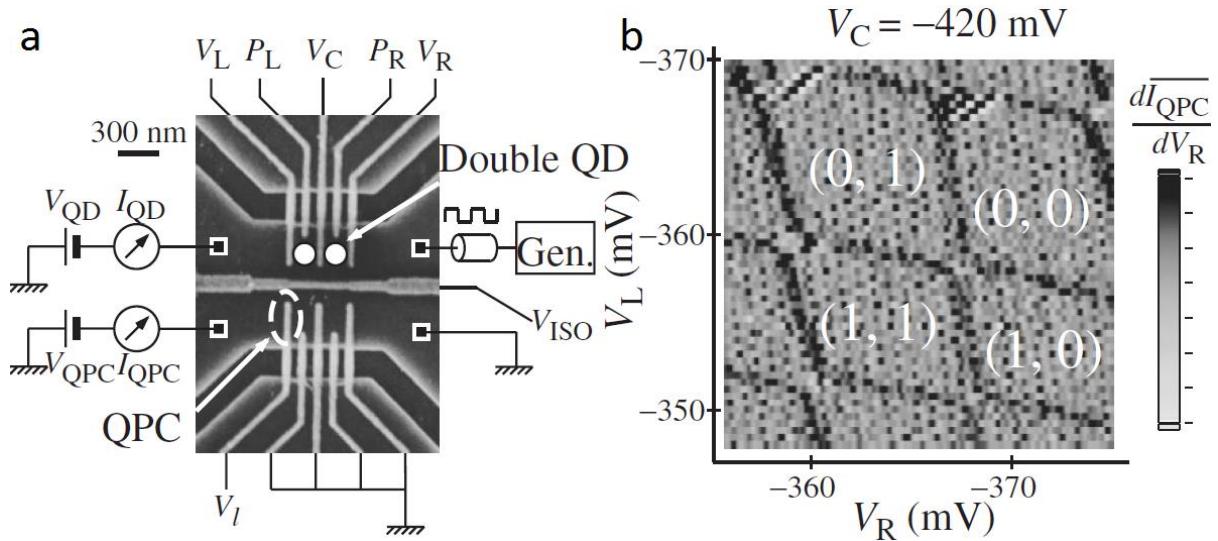


**Fig. 3.2.2(d)**  $\Delta I_{QPC}$  versus time during measurement procedure [20]

tunnelling rates for the rates for the two states, which is difficult to engineer for single electron quantum dots with spin- $\uparrow$  and spin- $\downarrow$  states which have the same orbital state. This work was taken further by [22] who showed a non-destructive measurement of electron spins with TR-RO technique for  $\Gamma_T = 200\text{kHz}$  and  $\Gamma_S = 10\text{kHz}$ . Two TR-RO measurement were taken in quick succession with a measurement pulses delay of  $60\mu\text{s} (< T_1)$ . A clear correlation between consecutive measurements were observed for both states with a conditional probability of 97% (84%) for a  $|T\rangle (|S\rangle)$  outcome in the second measurement given that the first measurement outcome was  $|T\rangle (|S\rangle)$ .

### 3.2.3 Real-Time Observation of charge states in a double quantum dot

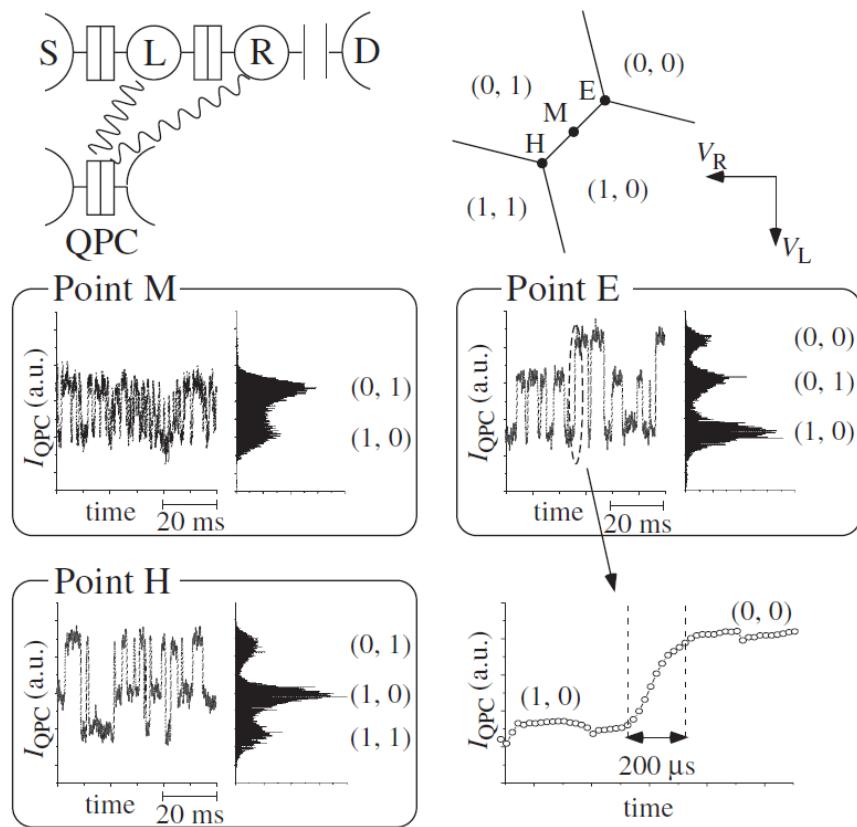
In [23], a work was presented which enabled time-resolved detection of single charges in a double quantum dot (DQD) by monitoring the time evolution of current  $I_{QPC}$  passing through a QPC near the DQD. They fabricated two symmetrically facing DQD devices defined by surface gates on a GaAs/AlGaAs heterostructure (see Fig. 3.2.3(a)) with a two dimensional electron gas below (2DEG). Two channels are defined by etched trenches and via applying a gate voltage  $V_{ISO}$ . The DQDs are defined on the channel via applying gate voltages to the lithographically defined side gates. Although one device is only used as a QPC to detect charge variations the other (which is implemented as a DQD), fabricating a



**Fig. 3.2.3(a)** SEM of a GaAs heterostructure forming a pair of symmetrically facing DQD. Schematic connections to source and drain are shown along with their applied voltages ( $V_{QD}$  and  $V_{QPC}$ ).  $V_L$ ,  $P_L$ ,  $V_C$ ,  $P_R$  and  $V_R$  are voltages applied to side gates electrostatically coupled to the QDs outlined by white circles on the SEM. **(b)** a plot of the conductance  $dI_{QPC}/dV_R$  through the DQD as a function of  $V_L$  and  $V_R$  displaying a clearly ‘honeycomb’ pattern (see Section 2.4) [23]

symmetric structure in this way allows for greater yield in the number of functioning devices after fabrication and also offers the ability to switch/reverse the device's function.

By tuning the QPC so that its conductance is  $\sim e^2/h$  resulting in maximum sensitivity to the DQD, the QPC conductance  $dI_{QPC}/dV_R$  displayed a clear “honeycomb” pattern (see Section 2.4) when  $V_R$  and  $V_L$  were swept from low to large voltages (See Fig. 3.2.3(b)). The body of each hexagonal shape in Fig. 3.2.3(b) represents a stable charge state  $(m, n)$  (where  $m$  and  $n$  are the excess no. of stable electrons in the left and right QDs respectively) of the DQD when current no longer flows due to the quantised nature of electronic states. This non-invasive measurement via the QPC allows for precise detection of DQD charge occupation even if direct current  $I_{DQD}$  through the DQD is immeasurably small.

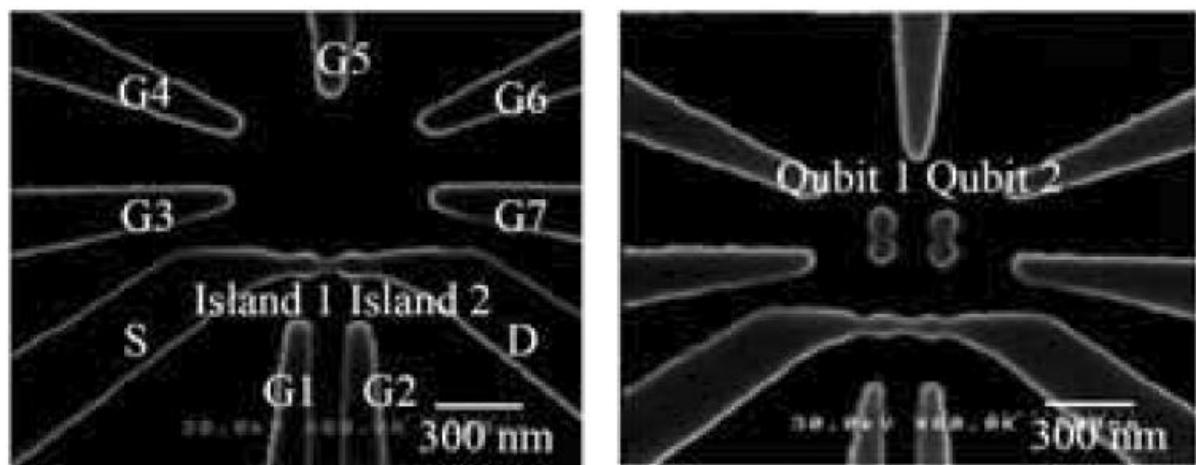


**Fig. 3.2.3(c)** Top left Diagram: A schematic circuit of the device with “L” and “R” being the left and right quantum dots (QDs), “S” and “D” being their source and drain contacts, and “QPC” being the quantum point contact detecting charge configuration in the QDs. Top right Diagram: a schematic of a section of the “honeycomb” pattern in Fig. 3.2.3(b)).The middle two and bottom left diagrams represent the response of  $I_{QPC}$  (the current through the QPC) as a function of charge states of the double quantum dots (L & R) at different points on the “honeycomb” pattern. The bottom right diagram is a close-up of the  $I_{QPC}$  response at point E [23]

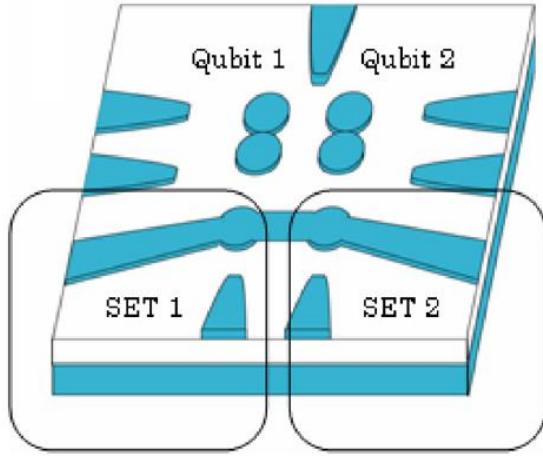
Fig. 3.2.3(c) shows the response of the  $I_{QPC}$  when the DQD is set to be at points “H”, “M” and “E” on the “honeycomb” pattern (top right diagram of Fig. 3.2.3(c)) where different charge states are degenerate (i.e. where the electrochemical potentials of the charge states are equal) and aligned between the source and drain Fermi levels such that current flows through the DQD system. The authors saw clear real time observations of changes in DQD charge states through the  $I_{QPC}$  response. Statistical analysis gave an estimate of transition times to be the order of milliseconds.

### 3.2.4 Charge state detection with a series connected Double Single Electron Transistor

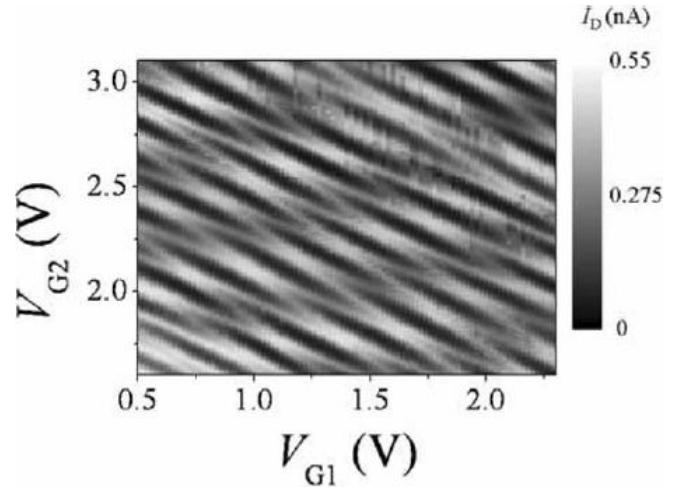
An alternative to the above methods of charge state detection of using a single electron transistor (SET) or a QPC is through the use of multiple single electron transistors (MSET). This has the advantage of being easily scalable with the increasing no. of qubits requiring detection and thus may offer a solution to the detection of integrated multiple qubit systems. [24] first proposed this readout technique by fabricating a lithographically defined double single-electron transistor (DSET) to detect the charge states of two isolated qubits. Fig. 3.2.4(a) shows SEM pictures of the P doped silicon on insulator (SOI) based DSETs, qubits and their electrostatically coupled side gates. Individual SETs 1 and 2 can be used to sense charge occupation in qubits 1 and 2 respectively (See Fig. 3.2.4(b) for device schematic view).



**Fig. 3.2.4(a)** SEMs of Phosphorus (P) doped silicon nanostructures (side gates and double single-electron transistor (DSET)) on insulating  $SiO_2$  (See Fig. 4.2.5(c)). Left: without qubits. Right: with qubits 1 and 2 [24]

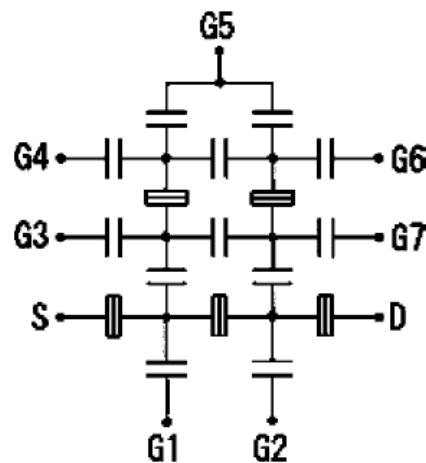


**Fig. 3.2.4(b)** Schematic bird's eye view of the nanoscale device structure. SET1 and SET2 make up the DSET. The rest makes up the qubits and their electrostatically coupled control gates. The blue layers are made from P doped Si. The white layer is a buried oxide layer (BOX) of  $SiO_2$  [24]



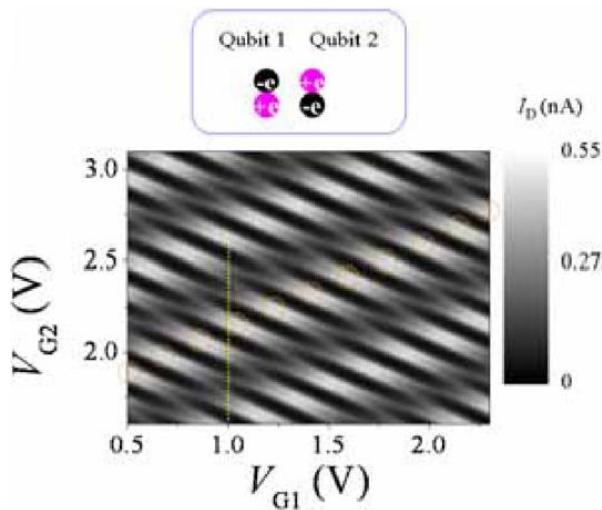
**Fig. 3.2.4(c)** Contour plot of the measured  $I_D$  as a function of side gate voltages  $V_{G1}$  and  $V_{G2}$  at a temperature of 4.2K and a source to drain bias through the DSET of  $500\mu V$  [24]

By measuring the current  $I_D$  through the DSET as a function of  $V_{G1}$  and  $V_{G2}$  (voltage applied to gates G1 and G2 respectively) clear evidence of the expected “honeycomb” pattern (See Section 2.4) was observed, thus indicating the presence of a DQD (Fig. 3.2.4(c)). From this, capacitances values between different components of the device were extracted and fed into a simulation of an equivalent DSET circuit (See Fig. 3.2.4(d)) using an “orthodox theory” [10] based Monte Carlo simulator “CAMSET” [25]. Simulations gave a charge stability diagram which matched that of Fig. 3.2.4(c).

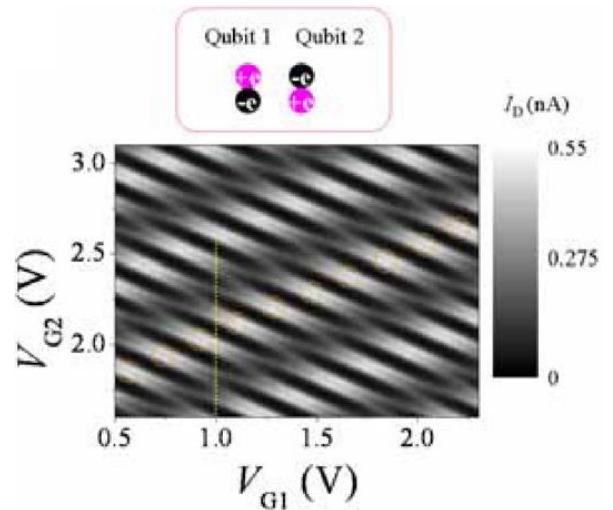


**Fig. 3.2.4(d)** Schematic of the equivalence circuit of the DSET device with two capacitively coupled qubits. Cross capacitances are not shown for clarity however were included in the simulations [24]

For the detection of qubit charge states, capacitance values between qubits and their control gates were evaluated via a simulator in which potential distributions were calculated by solving the three dimensional Poisson's equations with specific boundary conditions. CAMSET simulation of the full equivalent device circuit (See Fig. 3.2.4(d)) was then carried out with qubits 1 and 2 in different charge configurations. The response of  $I_D$  as a function of  $V_{G1}$  and  $V_{G2}$  was simulated for different qubit charge polarizations (See Fig. 3.2.4(e-f)) with  $-e$  and  $+e$  in either the top or bottom dot of each qubit. As can be seen, the current triple points (See section 2.4) in Fig. 3.2.4(f) were shifted towards the right bottom direction as compared with the same point in Fig. 3.2.4(e). This is expected for change in qubit configuration shown where qubit 1 couples much stronger to SET 1 than qubit 2 and vice versa. The results also show the current difference is of the order of several pA, which is clearly measurable experimentally. The authors also explored the potential for multi-qubit detection with a triple single electron transistor (TSET) and three qubits which produced encouraging results.



**Fig. 3.2.4(e)** Contour plot of the simulated  $I_D$  as a function of side gate voltages  $V_{G1}$  and  $V_{G2}$  at a temperature of 4.2K and a source to drain bias through the DSET of  $500\mu V$  for the charge polarizations shown in the inset figure [24]



**Fig. 3.2.4(f)** Contour plot of the simulated  $I_D$  as a function of side gate voltages  $V_{G1}$  and  $V_{G2}$  at a temperature of 4.2K and a source to drain bias through the DSET of  $500\mu V$  for the charge polarizations shown in the inset figure [24]

One of the key advantages of using these lithographically defined and etched QDs (Fig. 3.2.4(a)) over the GaAs 2DEG structures seen previously is the reduction in no. of gates or potentials needed to form a QD and conductance channel. From Fig. 3.2.4(b), it can be seen that only 3 gates are needed to create a single QD and form a SET as opposed to the 8 seen previously in section 3.2.1. This greatly benefits the future potential scalability of the

architecture where from Fig. 3.2.4(b), we can see that the DSET design could very easily be expand into a three or four QD system whilst only requiring 1 additional side gate for each additional QD. In addition, the etched lithographically defined structure allow for potential finFET [26] formation on the channels to create QDs. This would offer potentially greater levels of gating efficiency compared to the planar control gates for 2DEG structures seen previously due to the reduced gate delay time and increasing gating effectiveness of finFETs.

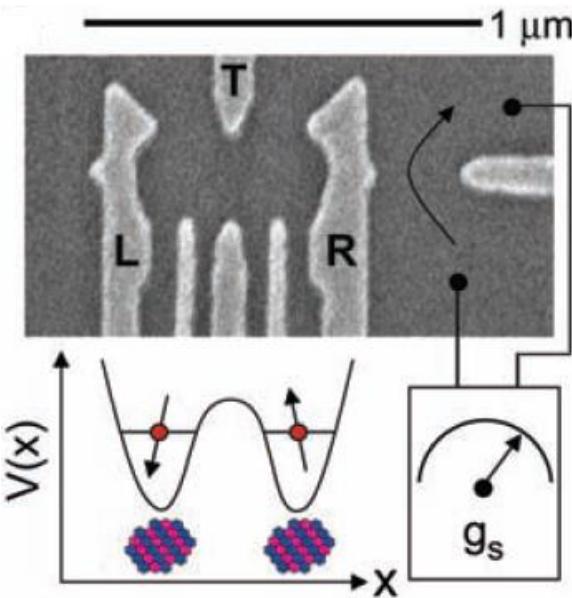
### 3.3 Coherent manipulation of coupled electron spins in QDs

In order to satisfy DiVincenzo's 4<sup>th</sup> criterion for realisation of a quantum computer, there has also been much work on exploring new ways to manipulate interactions between individual qubit states in both a controlled and precise manner to allow for the realisation of quantum gates operations. The sections below summarize some of the recent developments in the area of manipulating spin interactions as this is a very core and important area of research on QDs with successes that has attracted more interest into the field over the last few years. We also take a look at some of the platforms used that facilitated the methods enabling spin manipulation and discuss their attributes.

#### 3.3.1 *Spin Manipulation via the nuclear environment and exchange splitting*

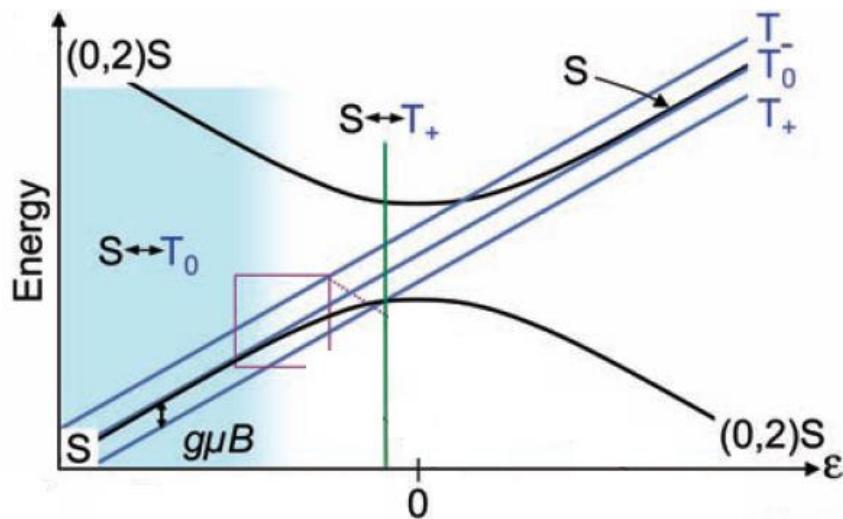
In 2005, [27] was the first to demonstrate coherent manipulation of coupled electron spins by using a GaAs double quantum dot (DQD) heterostructure (Fig. 3.3.1(a)) and through implementing GaAs' non-zero nuclear field and exchange energy splitting between spins. The GaAs based heterostructure device he used was similar to that used by [17] before (see section 3.2.1). Gates L and R (Fig. 3.3.1(a)) and their applied voltages  $V_L$  and  $V_R$  form the two quantum dots, couple each dot to their adjacent reservoirs and control their charge states. Interdot tunnelling (with a rate set by  $V_T$  applied to gate T) allows electron movement between dots when the detuning parameter  $\varepsilon = V_R - V_L$  is adjusted. A QPC to the right of the DQD serves as an electrometer with current  $I_{QPC}$  sensing the charge occupation of the adjacent quantum dots.

For manipulation of electron spins, Petta *et al* focused on transitions between the (1,1) and (0,2) charge states of the DQD (where for the state  $(n, m)$ ,  $n$  and  $m$  are the no. of extra

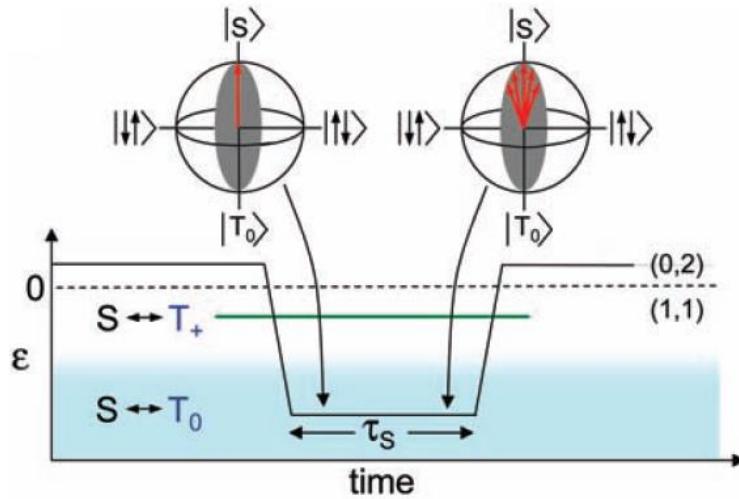


**Fig. 3.3.1(a)** an SEM of a GaAs heterostructure used by Petta *et al* consisting of a quantum point contact (QPC) and a double quantum dot (DQD) electrostatically defined by surface gates. Gates L and R control the electron occupation in the left and right quantum dots (QDs) respectively and gate T control the inter-dot coupling. The diagram below the SEM outlines the potential distribution across the system.  $g_s$  is the QPC's conductance. [27]

electrons occupying the left dot and right dot respectively). By sweeping from  $\varepsilon > 0$  to  $\varepsilon < 0$ , they pulsed the DQD charge state from (0,2) spin singlet state denoted “(0,2)S” to the (1,1) singlet,  $S$ , and triplet states  $T_-$ ,  $T_0$  and  $T_+$  (Fig. 3.3.1(b) shows this transition).

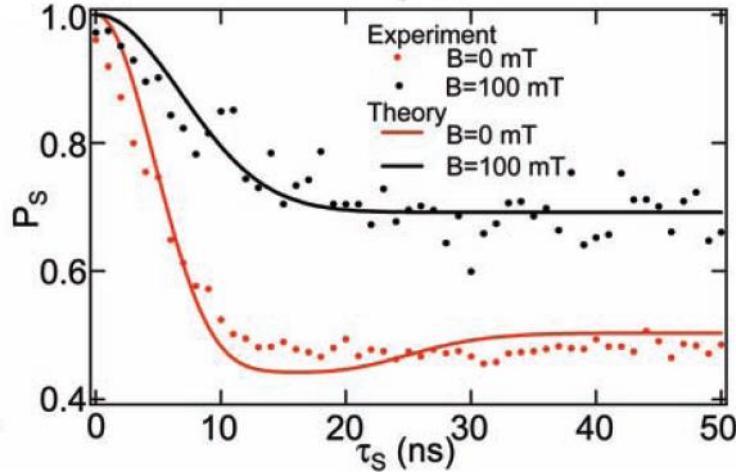


**Fig. 3.3.1(b)** Schematic graph of energy of various charge states as a function of the detuning parameter  $\varepsilon = V_R - V_L$  near the (1,1) to (0,2) charge state transition. (0,2)S is the spin singlet state when the DQD is in the (0,2) electron configuration.  $S$ , and  $T_-$ ,  $T_0$  and  $T_+$  are the singlet and triplet states respectively when the DQD is in the (1,1) electron configuration. A magnetic field is what splits the energy of the (1,1) triplet states ( $T_-$ ,  $T_0$  and  $T_+$ ) so that they become non-degenerate [27]



**Fig. 3.3.1(c)** Schematic of the pulse sequenced for  $\varepsilon$  (see Fig. 3.3.1(b)) used by Petta *et al* to evaluate the spin decoherence time  $T_2^*$ . The system is initialized in the  $(0,2)S$  state, and then transferred through a rapid adiabatic passage to the spatially separated  $S$  state (where the DQD is in the  $(1,1)$  charge configuration). At large  $\varepsilon < 0$  ( $\varepsilon = -6mV$ ),  $T_{\pm}$  states are non-degenerate to the  $S$  state due to a magnetic field, however, the  $T_0$  state mixes with the  $S$  state due to hyperfine fields driving rotations of spin about the x-axis of the Bloch sphere (the insets above the pulse sequence for  $\varepsilon$ ). After a separation time  $\tau_s$ , the state is projected back to the  $(0,2)S$  state [27]

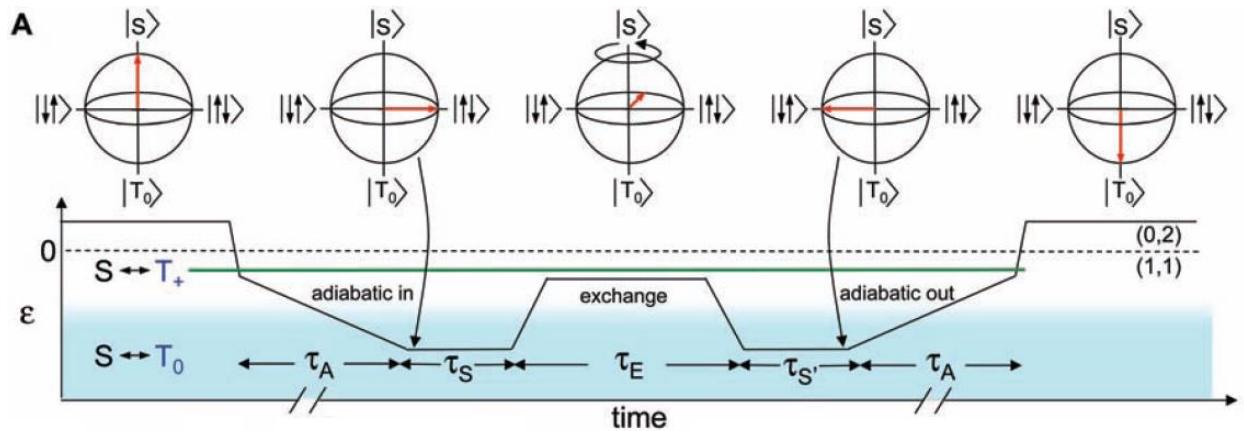
By using a cyclic pulse sequence (Fig. 3.3.1(c)) and sweeping via a rapid adiabatic passage [27] from the spin state  $(0,2)S$  to  $S$  and then projecting the resulting  $(1,1)$  spin state back to  $(0,2)S$ , a measurement of the  $(1,1)$  singlet,  $S$ , probability  $P_s$  was made (the  $(1,1)$   $T$  states are spin blockaded when pulsing back to  $(0,2)$  so electrons remain in the  $(1,1)$  configuration whereas the  $S$  state of  $(1,1)$  tunnel directly to the  $(0,2)S$  state). In this way, a spin to charge conversion of information is thus implemented allowing easy readout of spin information. Results showed  $P_s$  (Fig. 3.3.1(d)) decreasing with time  $\tau_s$  spent in the  $(1,1)$  configuration. This concurs with theoretical expectations that due to spin decoherence effects like hyperfine interaction (arising from electrons coupling to the background GaAs nuclear field  $B_{nuc}$ ) effectively mixing of the  $S$  and  $T_0$  and  $T_{\pm}$  states occurs at large  $\varepsilon < 0$  ( $\varepsilon = -6mV$ ) which in turn reduces  $P_s$ . A similar result was found in the presence of a magnetic field  $B$  which splits  $T_{\pm}$  states from  $T_0$  by the Zeeman energy. The spin decoherence time (time it takes for an electron spin to become decoherent in a GaAs environment) was evaluated to be  $T_2^* = 10 \pm 1\text{ns}$  (see (Fig. 3.3.1(d))) which is consistent with previous measurements [28]. However, this highlights the drawback that decoherence times are a major constraint on operation times when attempting to realise repeatable quantum gate operations on GaAs based proposals.



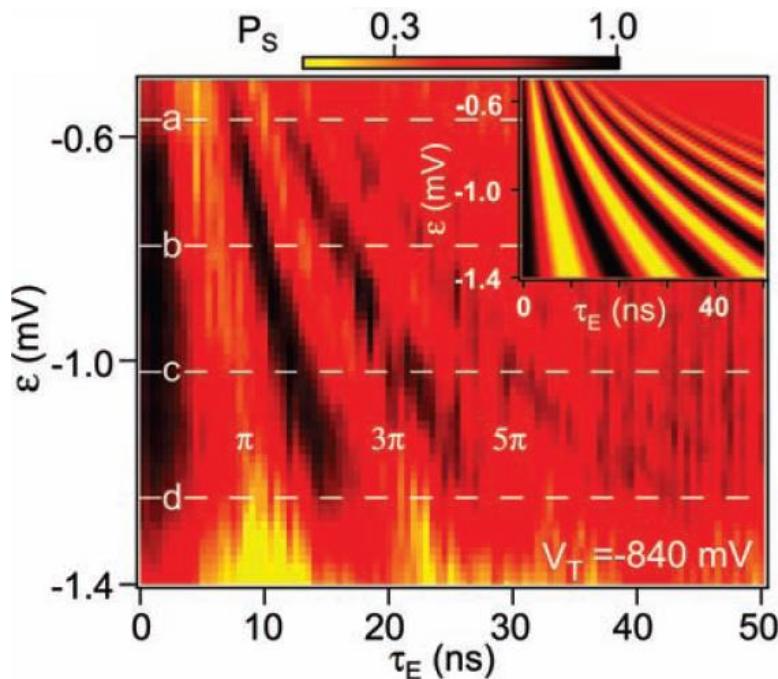
**Fig. 3.3.1(d)** Plot of the measurement probability  $P_s$  of the (1,1) singlet state  $S$  as a function of the electron separation time  $\tau_s$  (see Fig. 3.3.1(c)) with an external magnetic field of  $B = 100\text{mT}$  and  $B = 0\text{mT}$ . For  $\tau_s \ll T_2^*$ , the singlet state  $S$  does not have ample time to dephase and  $P_s \sim 1$ . For  $\tau_s \gg T_2^*$ , the singlet state  $S$  does have ample time to dephase and  $P_s \sim 0.7$  at  $B = 100\text{mT}$  and  $P_s \sim 0.5$  at  $B = 0\text{mT}$ . A fit from a semiclassical model of dephasing due to hyperfine coupling is also shown [27]

For coherent manipulation of spin states, Petta *et al* used the cyclic pulse sequence in Fig. 3.3.1(e) which allows for the demonstration of both spin SWAP operation [29] as well as Rabi oscillations [12] in the nuclear basis. For non-zero  $B$ , by first sweeping from  $(0,2)S$  through the  $S - T_+$  degeneracy (See Fig. 3.3.1(b)) via a rapid adiabatic passage and then using slow ramping of detuning (taking time  $\tau_A = 1\mu\text{s} > T_2^*$ ), the (1,1) system was initialized into the basis states of the nuclear field;  $|\uparrow\downarrow\rangle$  and  $|\downarrow\uparrow\rangle$ . Similarly, in reverse, spin readout was obtained from these nuclear states where  $|\uparrow\downarrow\rangle$  unloaded to  $S$  and  $|\downarrow\uparrow\rangle$  to  $T_0$ . Therefore, by measuring  $P_s$  they could obtain the fraction that was in state  $|\uparrow\downarrow\rangle$  before readout.

SWAP operation is possible in the nuclear basis via application of the exchange splitting  $J(\varepsilon)$  for time  $\tau_E$  which rotates the spin states in the nuclear basis about the  $z$  axis of the Bloch sphere (Fig. 3.3.1(e)) [29] by angle  $\phi = J(\varepsilon)\tau_E/\hbar$ . The exchange splitting  $J(\varepsilon)$  arises in the presence of inter-dot tunnelling between the  $S$  and  $T_0$  states of (1,1) due hybridising between (0,2) and (1,1) charge states. Spin state  $|\uparrow\downarrow\rangle$  is thus rotated into  $|\downarrow\uparrow\rangle$  if  $\phi = \pi$  constituting a spin SWAP operation. This would in turn result in a minima in the measured  $P_s(\varepsilon, \tau_E)$  since the system will be in the  $|\downarrow\uparrow\rangle$  state which unloads into a  $T_0$  state during readout (which is spin blockaded from tunnelling into the (0,2) $S$  state).



**Fig. 3.3.1(e)** Schematic of the pulse sequenced for  $\varepsilon$  (see Fig. 3.3.1(b)) used by Petta *et al* to demonstrate both spin SWAP operations and Rabi oscillations between two spin states. The Bloch spheres above this schematic show the orientation of the electron spins at different points on the sequence [27]

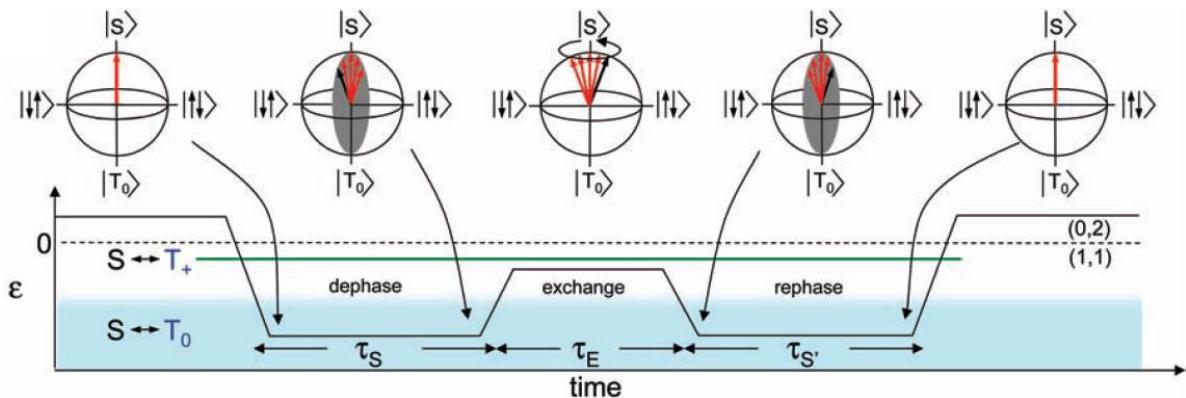


**Fig. 3.3.1(f)** Graph of  $P_s$  (the probability of a readout measurement of state  $S$ ) as a function of  $\varepsilon$  and  $\tau_E$  (see Fig. 3.3.1(e)) which shows clear evidence of Rabi oscillations between electrons occupying the  $|\uparrow\downarrow\rangle$  and  $|\downarrow\uparrow\rangle$  nuclear basis states [27]

The results in Fig. 3.3.1(f) above is a graph of  $P_s$  as a function of  $\varepsilon$  and  $\tau_E$  which shows clear evidence of Rabi oscillations between electrons occupying the  $|\uparrow\downarrow\rangle$  and  $|\downarrow\uparrow\rangle$  (or the measured  $(0,2)S$  and  $T_0$ ) states. One of the greatest advantages of this technique is that it is robust against nuclear interactions (such as spin-orbit or hyperfine interactions) as the electron is in the nuclear field's ground state during manipulation. Also, very fast  $\pi$ -pulses of up to 350ps could be obtained using this method. However, a major drawback is the time

$\tau_A = 1\mu\text{s}$  it takes to initialise spin states into the basis of the nuclear field. This severely limits the rate at which a SWAP operation and readout can occur.

In addition to demonstrating SWAP and Rabi oscillation, Petta *et al* showed further spin manipulation through a spin-echo technique which provides a means of refocusing the separated electron  $S$  state to undo dephasing due to local hyperfine fields. This technique has the great benefit of potentially prolonging the spin decoherence time which reduces a constraint on quantum gate operation times. The pulse sequence implemented here is shown in Fig. 3.3.1(g) where sweeping from the  $(0,2)S$  spin state to the  $S$  state and vice versa is once again done adiabatically. The  $S$  state at large  $\varepsilon < 0$  dephases for time  $\tau_S$  due to local hyperfine fields however, via applying a pulse of finite  $J(\varepsilon)$  for time  $\tau_E$  such that  $\phi = \frac{J(\varepsilon)\tau_E}{\hbar} = n\pi$  ( $n$  being any odd integer), the Bloch vector of the spin is rotated around the  $z$  axis by angle  $n\pi$  (essentially “reversed”) and the dephased  $S$  state can be refocused when it passes through another dephasing time of  $\tau_{S'} = \tau_S$  (Fig. 3.3.1(g)). This is very similar to spin echo refocusing techniques implemented in nuclear magnetic resonance [30].



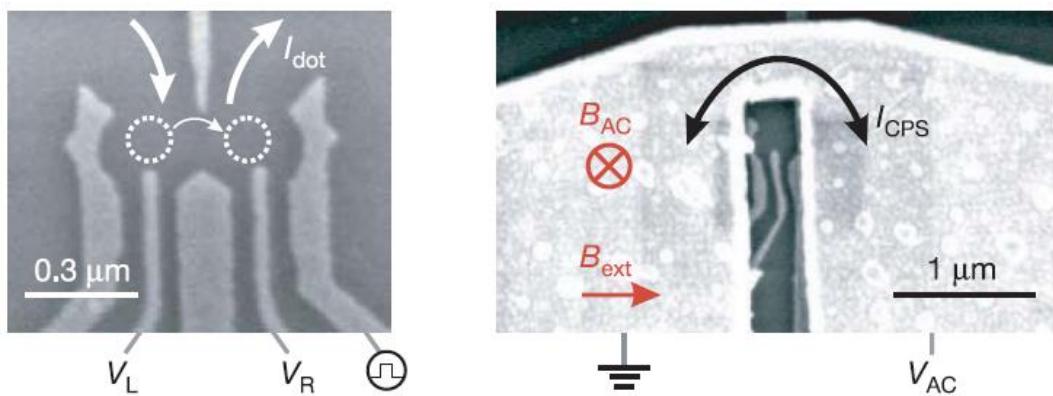
**Fig. 3.3.1(g)** Schematic of the pulse sequenced for  $\varepsilon$  (see Fig. 3.3.1(b)) used by Petta *et al* to demonstrate spin-echo technique. The method is similar to that in Fig 3.3.1(e) except the system is no longer initialized in the basis state of the nuclear field and there is no longer a slow ramping of detuning [27]

Results from spin-echo techniques of the measured singlet probability  $P_s(\varepsilon, \tau_E)$  clearly show periodic peaks (when  $\phi = n\pi$ ) in  $P_s$  as a function of  $\tau_E$  validating the use of the technique as a method for prolonging spin decoherence time. A lower bound of  $T_2 \geq 1.2\mu\text{s}$  was obtained which is more than  $10^2$  times larger than  $T_2^* = 10 \pm 1\text{ns}$  obtained without spin-echo techniques. Of course, if used on silicon based proposals this technique could potentially obtain even longer  $T_2$  times due to the zero nuclear spin of  $^{28}\text{Si}$ .

### 3.3.2 Driven coherent Rabi oscillations of a single electron spin via ESR and spin Blockade

Although [27] demonstrated a very novel use of the nuclear field as well as electron triplet and singlet states. Their methodology required the heavy use of the actual background nuclear field for demonstration of quantum SWAP and Rabi oscillations between two quantum states. This nuclear field inevitably results in undesirable decoherence effect on electron spins when the nuclear field is not implemented, therefore, a method which avoids use of this field completely is more desirable for manipulation of qubit states.

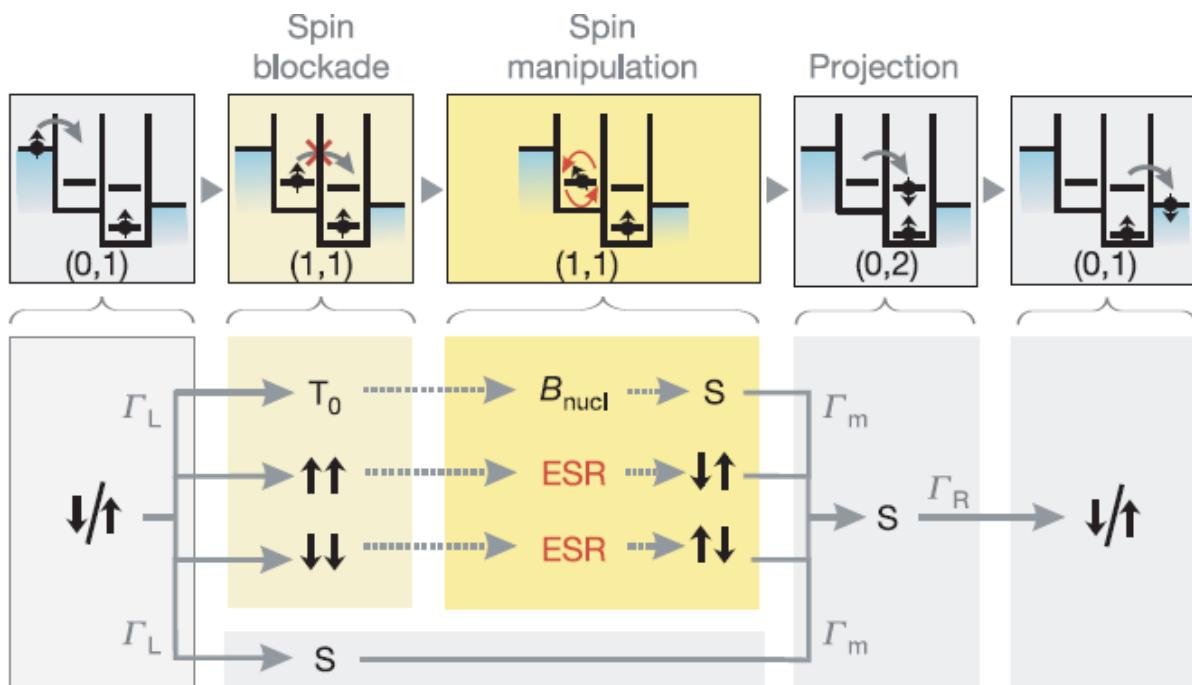
[31] demonstrated driven manipulation of a *single* electron spin confined in a GaAs DQD heterostructure (Fig. 3.3.2(a)) which doesn't explicitly use the nuclear field for spin manipulation and SWAP operations. This therefore makes it compatible with other materials like Si which have very low levels of nuclear spin-orbit coupling and hyperfine interaction. Here, coherent Rabi oscillations of a single electron spin in an electrostatically defined quantum dot was demonstrated using electron spin resonance (ESR) and spin blockade. In the (1,1) charge configuration of the DQD, applying an oscillating magnetic field  $B_{AC}$  (of frequency  $f_{AC}$ ) along with a perpendicularly oriented external constant magnetic field  $B_{ext}$  allows for controlled driven transitions of the electron spins via ESR when  $hf_{AC} = g\mu_B B_{ext}$  (where  $\mu_B$  is the Bohr magneton and  $g$  the electron spin  $g$ -factor).



**Fig. 3.3.2(a)** Left picture: SEM of a GaAs heterostructure used by Koppens *et al* consisting of a double quantum dot (DQD) formed in a 2 dimensional electron gas (2DEG) below the surface electrostatically defined by surface gates. Gates  $L$  and  $R$  (with applied voltages  $V_L$  and  $V_R$ ) control the electron occupation in the left and right quantum dots (QDs) respectively (outlined by dotted white circles). Right picture: SEM of the same GaAs heterostructure but now with an on-chip coplanar stripline (CPS) (with applied voltage  $V_{AC}$ ) deposited on top and centred on the left quantum dot [31]

$B_{AC}$  is generated by an on-chip coplanar stripline (CPS) separated from the surface gates and is centred such that  $B_{AC}$  is slightly stronger in the left dot than the right (See Fig. 3.3.2(a)). Therefore, electron spin transitions between spin  $\uparrow$  and spin  $\downarrow$  states in the left dot will occur at a faster rate than that in the right. The advantage of a DQD system over just a single dot is that spin-flips can be detected when electrons migrate from one dot to the other (through lifting of spin blockade) rather than between a single dot and a reservoir. Thus, there is no need to implement large Zeeman splitting needed to exceed the thermal energy of the electron reservoir (see Section 3.2.1) which in turn means operations can be performed at lower magnetic field and thus lower frequencies which are technically less demanding.

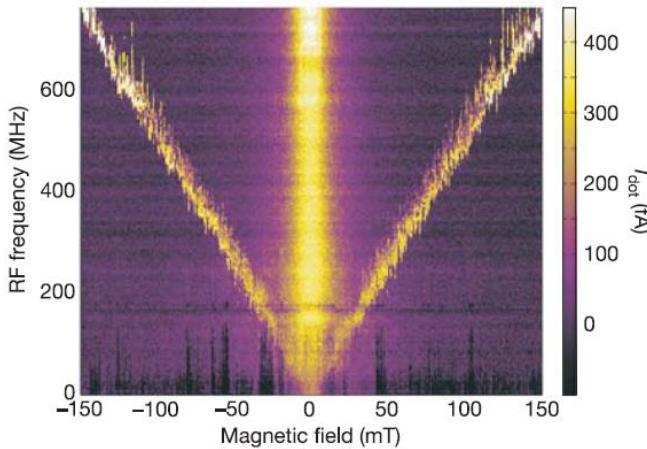
The gate voltages are tuned such that one electron always resides in the right dot. This ensures the spin blockade regime is accessed whereby if the electrons form a double dot singlet state  $S$  (i.e. in the (1,1) configuration), the left electron is then able move to the right



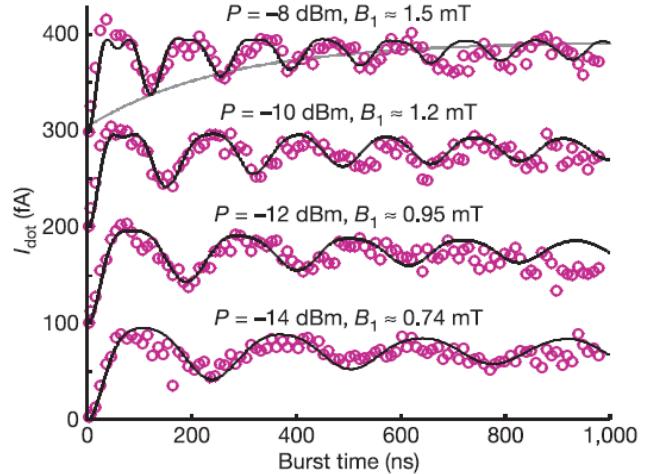
**Fig. 3.3.2(b)** Diagrams illustrating the transport cycle in the spin blockade regime. The top diagrams describe the cycle in terms of electron occupations  $(m, n)$  in the left and right dots respectively as  $(0,1) \rightarrow (1,1) \rightarrow (0,2) \rightarrow (0,1)$ . When an electron enters the left dot (with rate  $\Gamma_L$ ), the resulting  $(1,1)$  system formed can either be a spin singlet  $S(1,1)$  or a spin triplet  $T(1,1)$ . From  $S(1,1)$ , further current flow is possible via a transition to  $S(0,2)$  (the spin singlet state in the  $(0,2)$  charge configuration) with rate  $\Gamma_m$ . From  $T(1,1)$  however, current is blocked unless this state is coupled to  $S(1,1)$ . For the  $T_0$  triplet state, this coupling is provided by the inhomogeneous nuclear field in GaAs. For  $T_+$  and  $T_-$ , ESR causes a transition to a  $\uparrow\downarrow$  or  $\downarrow\uparrow$  state (where each arrow is an electron's spin) which is a superposition of  $T_0$  and  $S(1,1)$ . Therefore, through ESR, further current flow is possible at a rate determined by the Rabi oscillation frequency of ESR,  $f_{Rabi}$ , [31]

dot in the presence of non-zero source drain bias. If the (1,1) electrons form a double dot triplet state ( $T_0$ ,  $T_+$  and  $T_-$ ) the left electron cannot move to the right dot and is “spin blockaded” (See Fig. 3.3.2(b)). This is because the (0,2) singlet state,  $S(0,2)$ , is energetically accessible but the (0,2) triplet states are not. In the presence of a nuclear field  $B_N$ , hyperfine interactions result in admixing of  $T_0$  with  $S$  lifting of spin blockade. Application of a  $B_{AC}$  in resonance with  $B_{ext}$  (i.e.  $hf_{AC} = g\mu_B B_{ext}$ ) can also rotate the spin in the left or right dot from  $\uparrow\uparrow$  ( $T_+$ ) or  $\downarrow\downarrow$  ( $T_-$ ) (i.e. both electrons spin up or down respectively) to  $\uparrow\downarrow$  or  $\downarrow\uparrow$  at frequency  $f_{Rabi} = (g\mu_B B_{AC})/h$  lifting spin blockade periodically. In brief, spin blockade occurs when the system is in a  $T_+$  or  $T_-$  state and current flows through the double dot system when spin blockade is lifted. This only happens when the ESR condition ( $hf_{AC} = g\mu_B B_{ext}$ ) is satisfied.

The method proposed by the authors demonstrated clear evidence of ESR spin manipulation in semiconductor quantum dots (Fig. 3.3.2(c)). The graph plots the current ( $I_{dot}$ ) through the DQD system as a function of  $B_{ext}$  field strength and  $f_{AC}$  and shows clear linear dependence between  $f_{AC}$  and  $B_{ext}$  for the satellite peaks of maxima in  $I_{dot}$  (the diagonal lines of maxima in  $I_{dot}$ ) which agrees with expectations (i.e.  $hf_{AC} = g\mu_B B_{ext}$ ). This method was also taken



**Fig. 3.3.2(c)** A plot of  $I_{dot}$  (the measured current through the DQD system) as a function of the external magnetic field strength  $B_{ext}$  and  $f_{AC}$  (the RF frequency of the oscillating magnetic field of strength  $B_{AC}$ ) [31]



**Fig. 3.3.2(d)** Graph of  $I_{dot}$  (the measured current through the DQD system) as a function of the burst time  $t$  of the AC magnetic field of strength  $B_{AC}$ . Clear evidence of ESR and Rabi oscillations can be seen in the traces for  $I_{dot}$ . As the magnitude of  $B_{AC}$  decreases ( $B_1 = B_{AC}/2$ ),  $f_{Rabi}$  also decreases as expected. The purple circles each show a measurement data point. The solid lines are obtained from a numerical computation of the time evolution via a theoretical model [31]

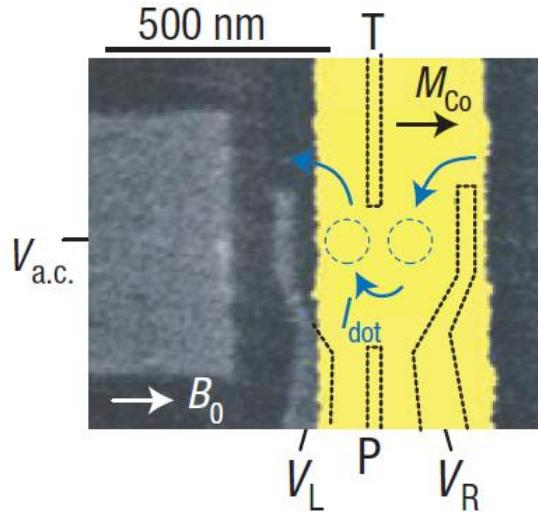
further by using short RF bursts of  $B_{AC}$  of time  $t$  instead of using a continuous *RF* magnetic field. In this way, the authors controlled the degree of single electron spin rotation whereby a rotation by angle  $(2n \pm 1)\pi$  ( $n$  being any integer) constitutes a spin flip whereas a  $2n\pi$  rotation gives no change in spin direction (the frequency of rotation being  $f_{Rabi} = (g\mu_B B_{AC})/h$ ). By first initialising the DQD in a spin blockade configuration and then applying short RF bursts of varying  $t$ , a plot of dot current  $I_{dot}$  vs  $t$  (See Fig. 3.3.2(d)) shows distinct Rabi oscillations in  $I_{dot}$  which is indicative of coherent electron spin rotations.

A major limitation in this method however is that the applied  $B_{AC}$  will always have an accompanying electric field which inevitably starts to hinder the experiment after some maximum  $B_{AC}$  value is reached. It is very difficult to remove this accompanying electric field from stripline excitation and this in turn limits the range of  $B_{AC}$  and the rate,  $f_{Rabi} = (g\mu_B B_{AC})/h$ , at which spin rotations can occur. Heating from the coplanar stripline is also a problem; high  $B_{AC}$  leads to significant heat dissipation close to the electron whose temperature must not exceed a few decikelvins for successful spin manipulation. In addition, the setup is not sufficient to allow for true single electron manipulation as both electrons have the same ESR frequency - we can't determine which electron was manipulated via ESR. In order to extend the work to achieve control of individual spins in two dots separately, a high  $B_{ext}$  gradient would be required across the two dots to successfully define different ESR resonant frequencies for them. Otherwise, *g*-factor engineering [32] could be used, however, both methods are experimental challenges in their own right.

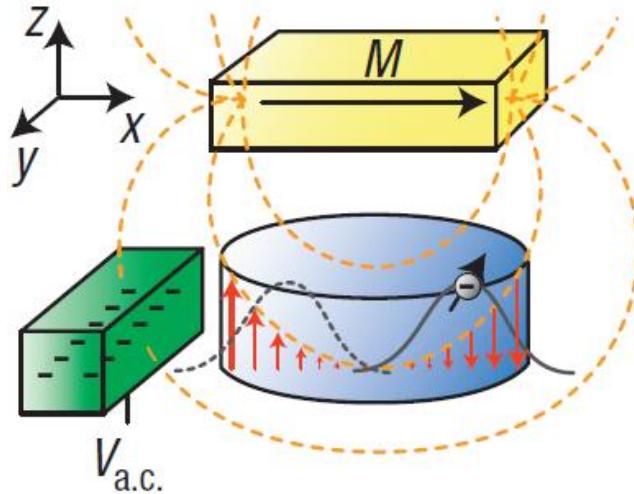
### 3.3.3 *Electrically Driven single-electron spin resonance in a Slanting Zeeman field*

The authors of [33] proposed a technique which offers individual electron spin manipulation through ESR but avoids having to artificially generate an oscillating magnetic field  $\tilde{\mathbf{B}}$  for operation. They implemented electric dipole induced spin [34] [35] (EDSR) driving individually addressable electron spin via mixing of electron spin and charge degrees of freedom in a controlled way in an engineered non-uniform magnetic field.

Oscillating electric fields  $E_{a.c.}$  are generated simply by exciting any gate electrode nearby a target spin. This is therefore much simpler than having to generate a  $\tilde{\mathbf{B}}$  field whilst ensuring minimal  $E_{a.c.}$ . The authors used a design consisting of the standard gate defined GaAs DQD



**Fig. 3.3.3(a)** SEM of a GaAs heterostructure consisting of a double quantum dot (DQD) formed in a 2 dimensional electron gas (2DEG) below the surface electrostatically defined by surface Ti-Au gates. Gates  $L$  and  $R$  (with applied voltages  $V_L$  and  $V_R$ ) control the electron occupation in the left and right quantum dots (QDs) respectively (outlined by dotted blue circles). The yellow strip on-chip covering the DQD represents the cobalt ferromagnetic strip used to generate a local static magnetic field gradient. This ferromagnet is uniformly magnetized by applying an in-plane magnetic field  $B_0$ . The large electrode to the left is the gate which couples to both dots and is used to produce an oscillating electric field of strength  $E_{a.c.}$  (of frequency  $f$ ) [33]



**Fig. 3.3.3(b)** Schematic diagram showing cobalt micromagnet (yellow rectangle on top), a single quantum dot (blue cylinder) and the electrode used to produce an oscillating electric field  $E_{a.c.}$  (green rectangle to the left) (see Fig. 3.3.3(a)). The magnetization  $M$  of the cobalt magnet produces a transverse magnetic field gradient across the quantum dot (red arrows) of strength  $\mathbf{B}_z = \mathbf{B}_z x \hat{z}$ .  $E_{a.c.}$  (driven by  $V_{a.c.}$ ) is then used to periodically displace the electron's wavefunction in this magnetic gradient to simulate an oscillating magnetic field  $B_{a.c.}$  [33]

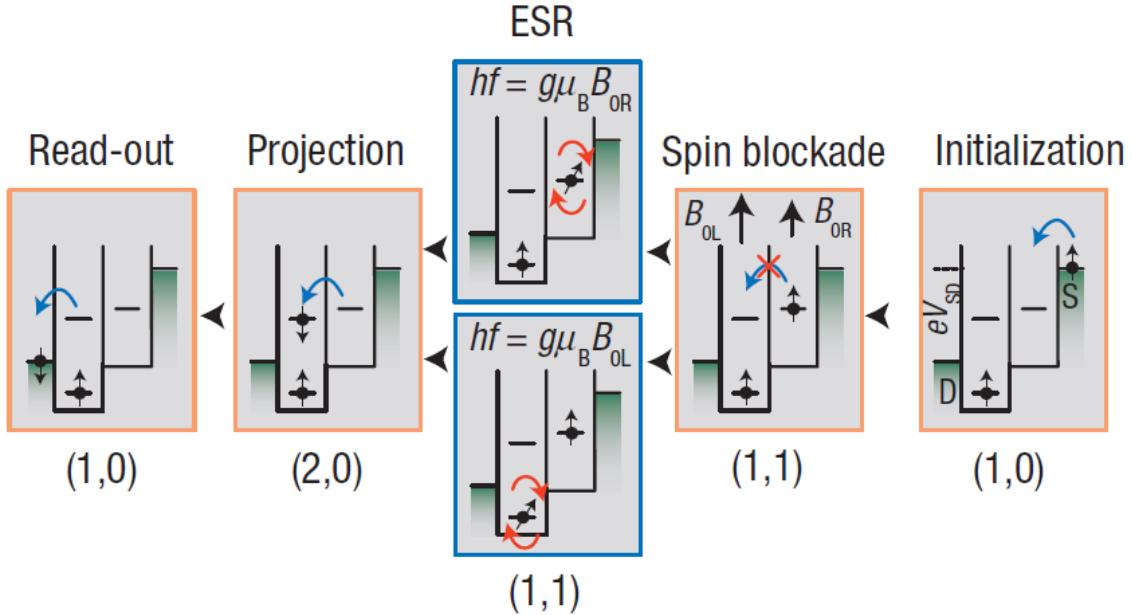
heterostructure (See Fig. 3.3.3(a)). The yellow strip covering the DQD represents the ferromagnetic strip (a micromagnet uniformly magnetised by an in-plane magnetic field  $B_0$ )

used to generate a static magnetic field gradient which in turn allows for different Larmor frequency,  $f_0$ , for spins in the two dots. The large electrode to the left on Fig. 3.3.3(a) represents the gate which couples to both dots and is used to produce  $E_{a.c.}$  (of frequency  $f$ ). Fig. 3.3.3(b) shows a schematic of the resulting magnetic field experienced by electrons in the DQD (positions outlined by the probability density drawn). In each dot, the spin will feel an upward magnetic field whenever it is displaced slightly to the left. Conversely, it experiences a downward field when displaced to the right.

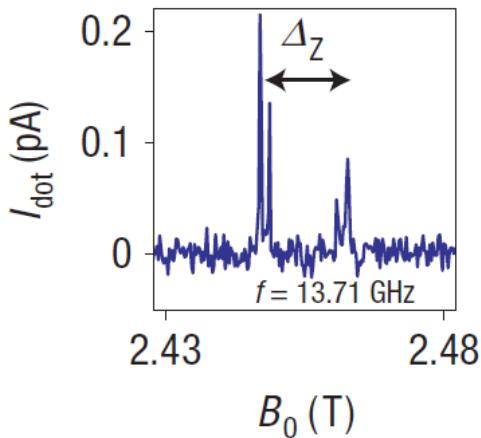
For single electron rotation and spin resonance, the author used a continuous wave (CW)  $E_{a.c.}$  to periodically displace electrons in each dot around their respective equilibrium positions. This results in a local effective oscillating magnetic field,  $B_{a.c.}$  (of frequency  $f$ ), for each electron spin which if driven at  $f_0$  of the target spin results in ESR. With the DQD operated in the Pauli spin-blockade regime (Fig. 3.3.3(c)), they measured and detected (via current through the DQD) individual selective coherent electron spin rotations and SWAP operations due to EDSR which are fundamental for the realization of a CNOT gate. The method of firstly initializing spin-blockade, manipulation and readout are near identical to that described in the previous section for [31]. Fig. 3.3.3(d) below shows results for current  $I_{dot}$  through the DQD system as a function of  $B_0$  for a constant  $f$ . The presence of two distinct peaks demonstrates differing Larmor frequencies for electrons residing in the left and right dot.

The author's design therefore offers the same level of integration as that in [31] but avoids the drawbacks and challenges of having to create an oscillating magnetic field. In addition, the use of a micromagnet may offer a simpler design when integrating quantum dots into multiqubit systems. However, having said this, restrictions are still present. Firstly, the problem of photon-assisted tunnelling (PAT) [18] arises when  $E_{a.c.}$  gets too large. This means at large  $E_{a.c.}$  (power  $\cong -20dBm$ ) PAT can excite right dot electrons from a (1,1) triplet state to a (2,0) triplet states (which were previously energetically inaccessible) thus undesirably lifting spin blockade. A possible solution to this is to operate deeper in the Coulomb blockade region of the stability diagram where energy levels have greater separation. This would mean stronger PAT is required to lift spin blockade and thus allow for both larger operating  $E_{a.c.}$  and faster spin-flip time. Another potential drawback is that random nuclear fields can act to shift the Larmor frequency of the quantum dots (See splitting of peaks in Fig. 2.3.3(d)) which impacts the repeatability of experiments. In addition, it is difficult to determine the precise magnitude of the induced  $B_{a.c.}$  since it depends on both the magnitude of  $E_{a.c.}$  as well as the

magnetic field gradient and rotation and the frequency of spin flips  $f_{rabi}$  (the Rabi frequency) accurately.

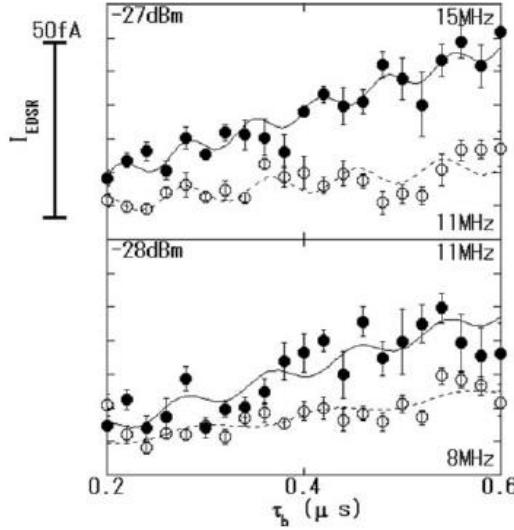


**Fig. 3.3.3(c)** Sequence of schematic energy level diagrams for the two quantum dots (see Fig. 3.3.3(a)) showing the steps used (from right to left) by Pioro-Ladriere *et al* to control the sequential flow of electrons through the DQD. The notation  $(n, m)$  indicates  $n$  and  $m$  electrons in the left and right QD respectively and arrows indicate the direction of electron spin. The system is driven through the cycle  $(1,0) \rightarrow (1,1) \rightarrow (2,0) \rightarrow (1,0)$ . Starting from the  $(1,0)$  configuration (initialization step), an electron tunnels from the source to form the  $(1,1)$  triplet  $T_+$  state. The electron in the right dot can't tunnel to the left dot because of the Pauli exclusion principle and transport is blockaded. With ESR, the electron spin in the right dot is reversed, allowing it to tunnel to the left dot to form a  $(2,0)$  state. One of these electrons then tunnels out to the drain to complete the cycle and allowing a non-zero source to drain current. [33]



**Fig. 3.3.3(d)** A plot of the measured current  $I_{dot}$  through the DQD system as a function of  $B_0$  for a constant  $f$  [33]

[36] furthered the work in [33] by experimentally demonstrating Rabi oscillations (See Fig. 3.3.3(e)) of leakage current  $I_{EDSR}$  through a DQD system. Instead of implementing a continuous wave  $E_{a.c.}$ , short bursts of time  $\tau_h$  were used instead to offer controlled spin rotation. Using a setup similar to that by Pioro-Ladriere *et al*, selective observation of Rabi oscillations for a single electron in each dot was achieved in the presence of a magnetic field gradient.

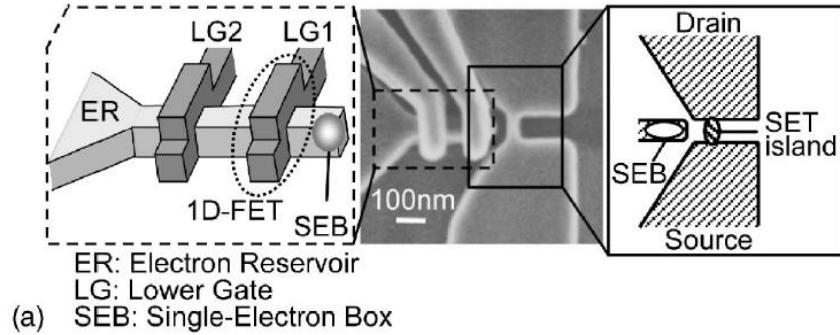


**Fig. 3.3.3(e)** A plot of the leakage current  $I_{EDSR}$  through a DQD system as a function of the burst time  $\tau_h$  of an oscillating electron field  $E_{a.c.}$  in the presence of a magnetic field gradient. Dark circles are data points for when spins in the left QD are addressed, and white circles for the right QD. As can be seen, the period of Rabi oscillations are different for the two QDs, which suggest individual addressability of single electron spins in the two QDs [36]

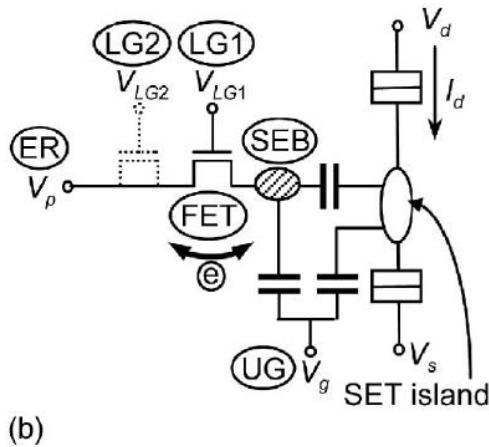
### 3.4 Single-electron transfer and multilevel memory

Although efforts to understand how to manipulate single spins in QDs is important for the future realisation of quantum information processing, there have also been diverse research into QDs for other applications which has been important in driving progress in this field.

The authors of [37] proposed a platform for the realisation of single electron turnstile operation in addition to a demonstration of a multilevel dynamic random access memory (DRAM) using a single electron box (SEB). This turnstile operation provided a crucial solution for the transportation of qubits between specific locations which is a desideratum for quantum communication [4]. A SEM image, schematic view and equivalent circuit of their device is shown in Fig. 3.4(a-b) respectively which consists of a single-electron transistor (SET), two field effect transistors (FET) and a SEB connected to an electron reservoir



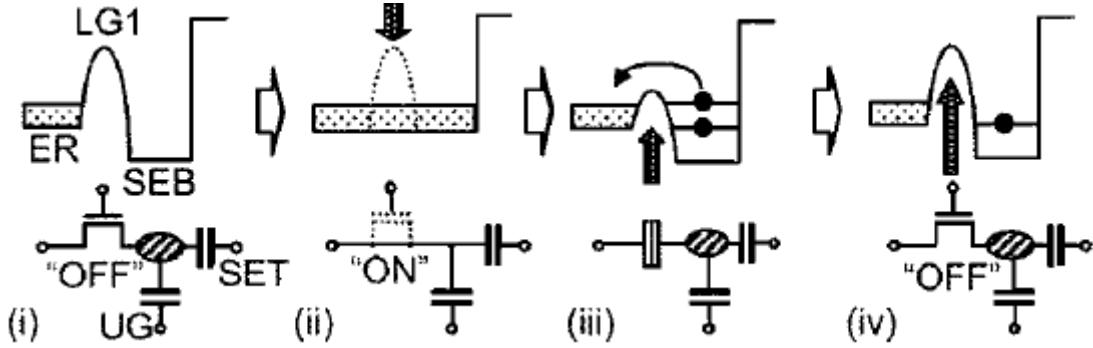
**Fig. 3.4(a)** SEM image (middle) and schematic view (left and right) of a multilevel memory device proposed by Nishiguchi *et al.* The device consists of a silicon nanowire protruding from an electron reservoir (ER) controlled electrostatically by two gates (LG1 and LG2) like two field effect transistors (FET). This allows a SEB to form at the end of the nanowire. A single electron transistor (SET) to the right of the device is used for detection of single electron occupancies in the SEB. Lighter regions represent the silicon based nanostructure and darker regions represent the insulating  $SiO_2$  substrate below. The entire SEM area is covered by an upper poly-Si gate used to induce an inversion layer in the intrinsic Si nanowire to allow for conduction [37]



**Fig. 3.4(b)** Equivalence circuit diagram of the multilevel memory device proposed by Nishiguchi *et al* (see Fig. 3.4(a)). The SET is used to count the number of electrons in the SEB (single electron box).  $V_p$  is the voltage applied to the ER and  $V_g$  is the voltage applied to the upper poly-Si gate [37]

(ER) fabricated on the same silicon-on-insulator (SOI) layer. A conducting upper gate (covering the entire area shown in the SEM) was used to induce an inversion layer in the SOI layer to allow for conduction and also controls the potential of the SET island. The two polycrystalline silicon (Poly-Si) conducting lower gates (LG1 and LG2) formed on the channel of the FET act to modulate potential barriers on the channel (when voltages are applied to them) and allow for single electron turnstile operation (See Fig. 3.4(c)). When the LG1 turns “ON”, electrons enter the SEB from the ER. Then, as LG1 turns “OFF” the potential barrier increases and the SEB gradually becomes electrically isolated from the ER

and stores some electron. The no. of electrons stored depends on the voltages applied to the upper gate ( $V_g$ ) and that applied to the ER ( $V_p$ ). The SET (which is strongly capacitively coupled to the SEB due to the small gap) can then act as an electrometer to measure the electron occupation of the SEB. LG2 was deemed non-essential for the operation and set to be “ON” by the authors.



**Fig. 3.4(c)** The sequence used for storing electrons in the SEB (left to right). Upper diagrams show the energy bands in the SEB and FET and the sequence of operations on potential applied to LG1 to allow single electron transfer to the SEB. Lower diagrams show equivalent circuits of this operation. Note that LG2 is always set in the “ON” state and only LG1 is operating [37]

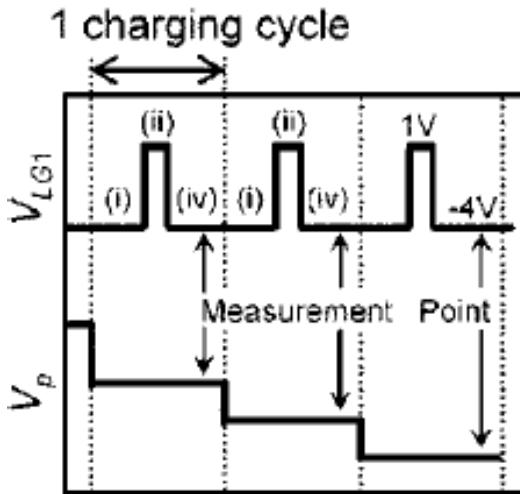
Turnstile operation was demonstrated at both 26K and crucially at room temperature. With a charging sequence shown in Fig. 3.4(d) (where (i-iv) are the steps on Fig. 3.4(c)), results (Fig. 3.4(e)) clearly showed successful single electron turnstile detection with  $I_d$  (the current through the SET) changing as a step function (electrons individually migrating into the SEB) as  $V_p$  decreases.

In terms of device design, one of the unique features of this work is the use of finFET gates [26] around an etched lithographically defined channel to define QDs/SEB. The fact that the Poly-Si finFET gate structures surrounds the etched SOI channel means it is able to control the SOI channel from three sides, increasing the effectiveness of finFET gates at pinching off the channel conductance. This offers potentially greater levels of gating efficiency compared to the previously seen planar control gates for 2DEG structures and is a main contribution factor which enabled observation of room temperature single electron turnstile operations. This is useful as it demonstrates a practical architecture for storing information via single electron charges avoiding the need for a low temperature setup.

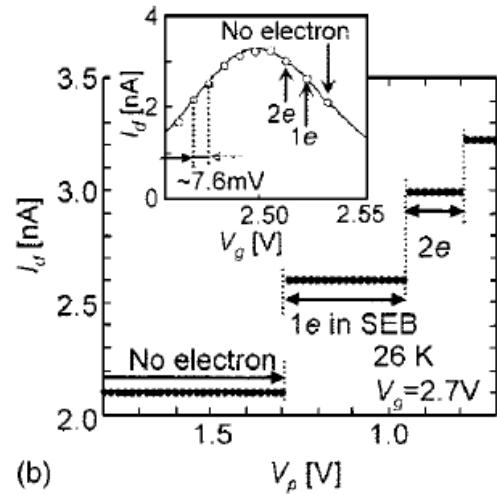
Another major benefit of this approach is that potential modulation by the FET can result in very long retention times of electrons in the SEB even at room temperature. In addition, high

speed operation can also be achieved with no repercussions for retention times. This is because with the FET in the “OFF” state, the SEB can be fully electrically isolated from the ER.

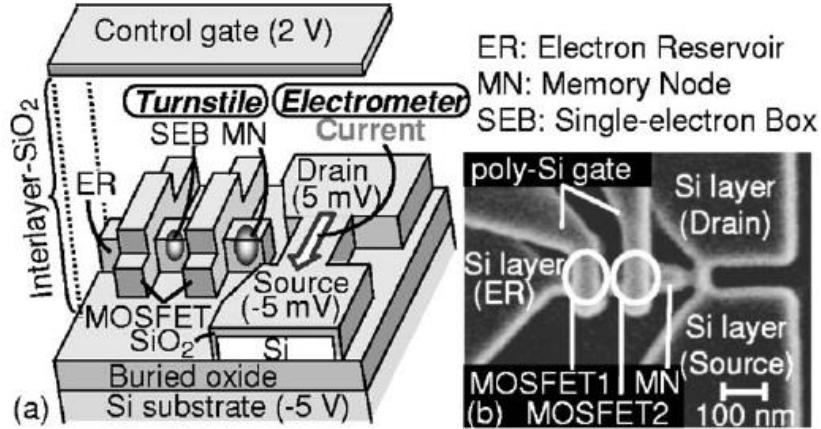
However the device design does have limitations. One of which is that there is a high potential for leakage between the Poly-Si finFET gates and the underlying silicon channel as only a very thin passivation  $\text{SiO}_2$  layer ( $<5$  nm thick) separates them. This could in turn lead to potentially lower working device yields when fabricating large numbers of these designs for memory storage.



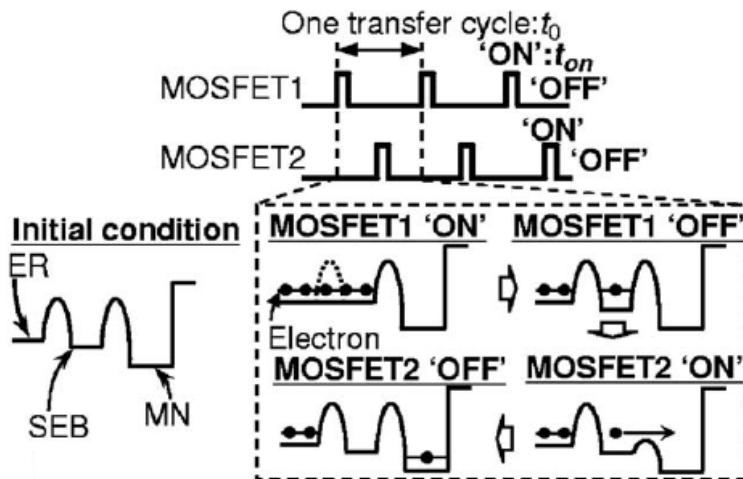
**Fig. 3.4(d)** The sequence of voltage applied to  $V_{LG1}$  and  $V_p$  to allow individual electrons to be added to the SEB. 1 charge cycle is equal to the cycle shown in Fig. 3.4(c), with steps (i), (ii), (iv) being the corresponding steps in Fig. 3.4(c). The “measurement points” are points where the current  $I_d$  through the SET is recorded (see Fig. 2.3(e)) [37]



**Fig. 3.4(e)** A plot of  $I_d$  (current through the SET) as a function of  $V_p$  (voltage applied to ER (see Fig. 2.4(b))) at a temperature of 26K,  $V_{LG1} = 3V$  and  $V_g = 2.7V$ . The inset shows the measured current  $I_d$  values (circles) fitted to a  $I_d - V_g$  characteristic (solid curve). Results clearly show successful single electron turnstile detection with  $I_d$  changing as a step function (electrons individually migrating into the SEB) as  $V_p$  decreases. [37]



**Fig. 3.4(f)** SEM image (right) and schematic view (left) of a silicon based multilevel memory device. The device consists of a nanowire protruding from an electron reservoir (ER) controlled electrostatically by two gates (LG1 and LG2) like two field effect transistors (FET). This allows a MN to form at the end of the nanowire and a SEB to form between the two gates. A single electron transistor (SET) to the right of the device is used as an electrometer for detection of single electron turnstile operation in the SEB and MN. Lighter regions represent the silicon based nanostructure and darker regions represent the insulating  $SiO_2$  substrate below. The entire SEM area is covered by an upper poly-Si gate used to induce an inversion layer in the intrinsic Si nanowire to allow for conduction [38]

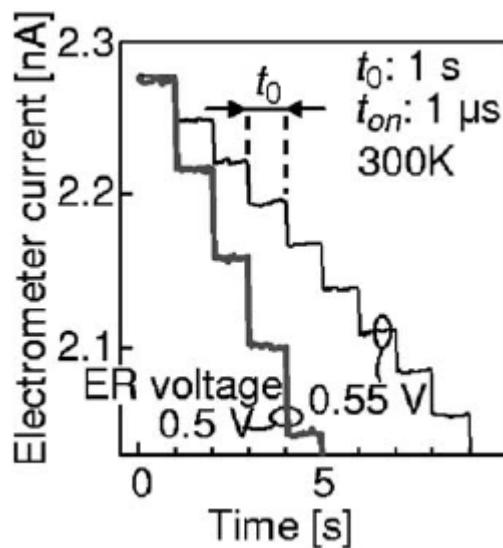


**Fig. 3.4(g)** The upper diagrams show the sequence of voltage applied to the gates of MOSFET1 and MOSFET 2 to allow single electrons to travel from the electron reservoir (ER) to the SEB or MN. MOSFET1 is first turned “ON” to allow electrons into the SEB. Then it turns “OFF” to trap an electron in the SEB. Then, MOSFET2 is turned “ON” to allow this single electron into the MN and finally turned “OFF” to trap this single electron in the MN [38]

In 2006, the authors [38] extended their approach by implementing LG2 in their device Fig. 3.4(a) and demonstrating selective single and double electron turnstile operation as well as realisation of a time division weighted sum circuit and a multilevel memory. An updated SEM image and schematic of their device (same as before) along with new notations is shown in Fig. 3.4(f). The authors used a charge transfer cycle (Fig. 3.4(g)) similar to before

but this time implementing two gates (MOSFET1 and MOSFET2), a SEB (single electron box) now between the gates and a memory node (MN) at the end of the channel. Electrons are transferred to the MN through the SEB via turning MOSFET1 and MOSFET2 “ON” and “OFF” as shown in (Fig. 3.4(g)) with each transfer cycle taking time  $t_0$ .

Results (Fig. 3.4(h)) clearly show the successful detection of turnstile operation at a temperature of 300K by the discrete changes in electrometer (SET) current which is capacitively coupled to the MN. The thin and bold lines are characteristics at ER voltages of 0.55 and 0.5V respectively which show a clear distinction between single electron and double electron transfer in each transfer cycle. Electron retention times in the MN of up to  $10^4$  seconds were demonstrated for a number of charge configurations.



**Fig. 3.4(h)** Measured changes in the electrometer current as a function of time when the transfer cycles (see Fig. 2.4(g)) were repeated at different electron reservoir (ER) voltages of 0.5V and 0.55V.  $t_{on}$  is the time it takes to switch a MOSFET “ON” or “OFF” [38]

### 3.5 Silicon Based Double Quantum Dot Structures

From our review so far of the important milestones in research on QDs, we can see that much progress has been made in single electron spin manipulation on GaAs based QD research to pave the way towards solid state realisation of quantum information processing capabilities. Critically however, the physics behind many of these approaches for spin manipulation are entirely general and can be fully applied to new material systems.

Silicon has recently attracted much interest because it is a material which brings many key advantages over GaAs in QD research. Firstly, intrinsic silicon offers smaller spin-orbit

coupling and the appearance of isotopically pure Si materials can offer almost a spin-zero nuclear background. This significantly reduces the effects of contact hyperfine interactions for spin qubits in solid state QDs and can potentially lead to much longer electron spin decoherence time in comparison to that found in GaAs QDs (where confined electrons couple to  $\sim 10^6$  spin-3/2 nuclei through hyperfine interactions). This offers benefits to quantum computing by allowing for greater fidelity in qubit state readout, longer gate operation times, and longer qubit transport times between different locations without decoherence. Additionally, being the long-time staple for the electronics industry, silicon has the benefit of being compatible with existing semiconductor device fabrication techniques.

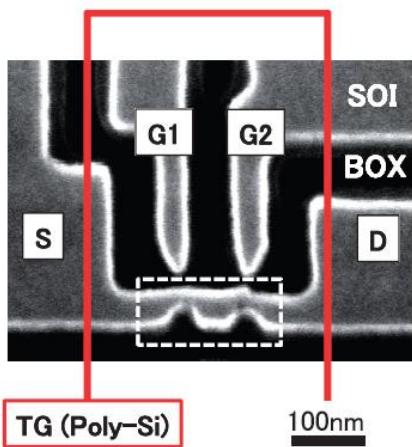
Below we take a look at some of the most recent progress on intrinsic Si QDs, the different platforms explored and highlight some of the key advantages intrinsic Si QDs offer over their GaAs counterparts. Crucially, we focus on intrinsic Si rather than highly doped Si (see section 3.2.4) platforms because the intrinsic property allows the potential for control over QD occupations down to the single electron limit and thus enables single electron spin manipulations. Working with intrinsic Si however does have its challenges. Realising intrinsic Si QDs requires a greater level of complexity in device fabrication because extra gates would be needed to control the materials conductance via an inversion layer of carriers at lower temperatures. This in turn adds to the challenge of ensuring a contaminant and trap free interface between different lithographic layers in the device architecture.

### 3.5.1 *Series coupled lithographically defined Double Quantum Dots*

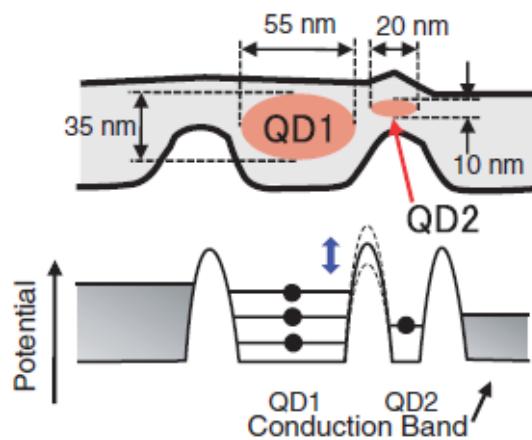
In 2009, [39] reported successful characterisation measurements of one of the first lithographically defined series coupled intrinsic silicon double quantum dot structures. Fig. 3.5.1(a) shows an SEM image of the silicon DQD device coupled to two side gates (G1 and G2) lithographically defined on the same SOI (silicon on insulator) layer. “S” and “D” are the source and drain and a conducting Poly-Si top gate “TG” (Outlined on Fig. 3.5.1(a)) was used to induce inversion carriers in the SOI thus allowing conduction through the DQD. The two channel constrictions (dashed rectangle on Fig. 3.5.1(a)) and two side gates were patterned by electron beam lithography on a 60 nm thick SOI layer. A gate oxide of about 30 nm was formed via thermal oxidation for 30 min at 1273K which ensured the channel constrictions were less than 10 nm and that the gap between side gates and nanowire was filled with  $SiO_2$ . One quantum dot formed between the two constrictions and the other (smaller QD) formed

on the right constriction which has a bump. This resulted in the formation of an asymmetric DQD schematically shown in Fig. 3.5.1(b).

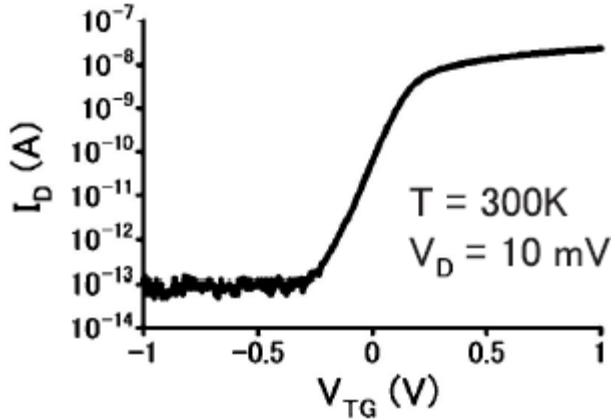
This accidental formation of a QD highlights one of the key challenges in working with Si in that electrons have a higher effective mass than in GaAs. Because the electron confinement potential energy required is relatively smaller than GaAs, smaller QDs are therefore needed when working with Si in order to obtain single electron quantum confined electronic states. This in turn means even more precise lithography is needed if systems are to expand to future, more complex multi-configuration QD systems.



**Fig. 3.5.1(a)** SEM image of a silicon double quantum dot (DQD) (see Fig. 3.5.1(b)) connected via tunnel barriers to a source and drain contact and electrostatically coupled to two side gates (G1 and G2) lithographically defined on the same SOI (silicon on insulator) layer. Lighter regions represent the silicon based nanostructure and darker regions represent the insulating  $SiO_2$  layer below. The red line indicates the approximate position of a Poly-Si top gate (TG) deposited to induce an inversion layer in the underlying Si channel [39]



**Fig. 3.5.1(b)** Top diagram: Schematic view of the region outlined by a dotted rectangle in Fig. 3.5.1(a). The approximate positions of the two quantum dots ( $QD_1$  and  $QD_2$ ) are indicated. Bottom diagram: a schematic potential profile across the DQD system [39]

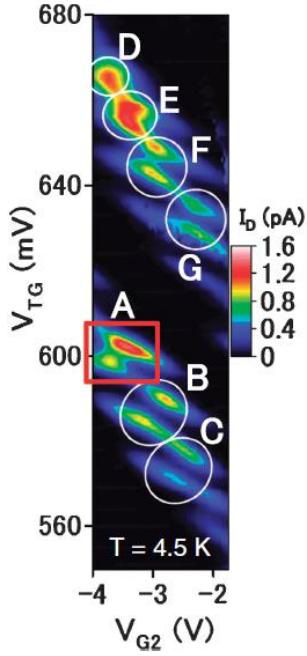


**Fig 3.5.1(c)** Plot of the measured source to drain current,  $I_D$ , through the DQD system as a function of  $V_{TG}$  (voltage applied to the Poly-Si top gate) at room temperature [39]

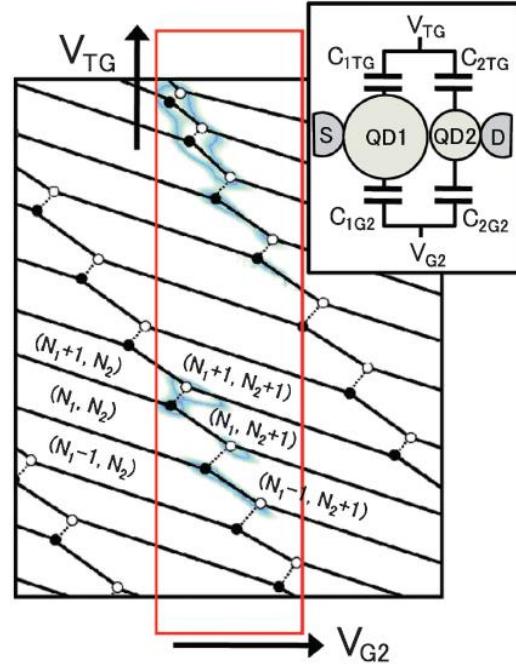
A plot of drain current ( $I_D$ ) through the DQD as a function of the voltage applied to the top gate ( $V_{TG}$ ) (Fig. 3.5.1(c)) with 10mV applied to the drain ( $V_D$ ) showed expected characteristic of a standard Si MOSFET. Fig. 3.5.1(d) shows the contour plot of  $I_D$  as a function of the voltage applied to G2 ( $V_{G2}$ ) and  $V_{TG}$  at 4.2K. Clear evidence of bias triangles and a honeycomb pattern of  $I_D$  could be seen with a finite bias voltage of  $V_D = 500\mu V$ . These form only at the charge triple points (see Section 2.4) where the electrochemical potentials of the DQDs align with that of the leads and current is allowed. Fig. 3.5.1(e) shows a schematic of the underlying honeycomb pattern in the contour plot of  $I_D$  with the red rectangle representing results in Fig. 3.5.1(d).  $(N_1, N_2)$  denotes the stable charge configuration of the quantum dot with  $N_1$  and  $N_2$  confined electrons in  $QD_1$  and  $QD_2$  respectively. In addition, the authors evaluated the capacitance between QDs and side gates from the periodicity in Fig. 3.5.1(d) which confirmed the validity of the estimated sizes of the DQD shown in Fig. 3.5.1(b).

One of the most important highlights of this work by [39] is the use of a top gate as well as side gates to control both the SOI channel conductance as well as single electron occupation in the QDs to demonstrate single electron turnstile operation. The advantage of this device architecture is the ability to fabricate and define both the QD structures as well as their controlling side gates in one lithographic step. This reduces the fabrication process complexity whilst also minimising the potential for leakage between QDs and their respective side gates. In turn, this could enable a potentially higher functional device yield than the 2DEG architectures seen previously when fabricating large numbers of devices. The etched

lithographically defined structures also allows for scalability in the QD architecture, enabling many of the advantages discussed previously in section 3.2.4.



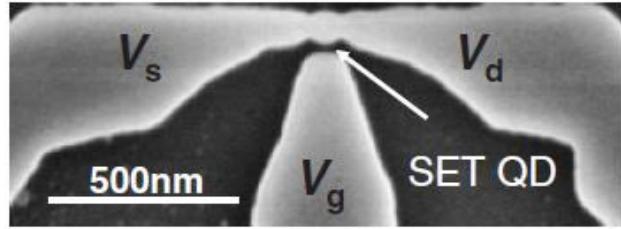
**Fig 3.5.1(d)** Contour plot of the measured source to drain current,  $I_D$ , through the DQD system as a function of  $V_{TG}$  and  $V_{G2}$  (the voltage applied to gate G2) at a temperature of  $T = 4.5K$  and a source to drain bias voltage of  $V_D = 500\mu V$  [39]



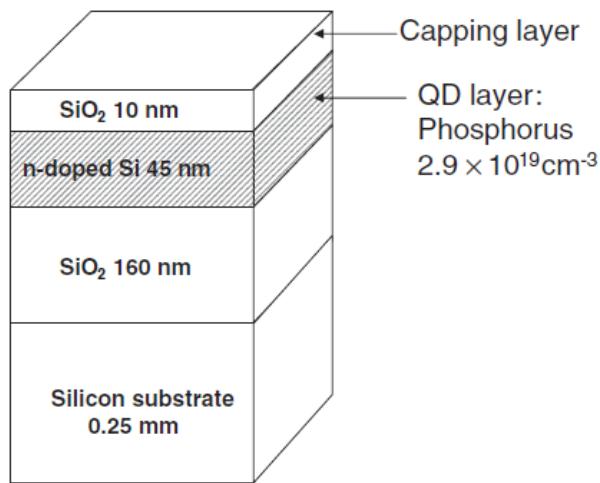
**Fig 3.5.1(e)** Schematic honeycomb pattern (see Section 2.4) expected to appear in a plot of  $I_D$ , as a function of  $V_{TG}$  and  $V_{G2}$  for a DQD device. The region outlined by the red rectangle corresponds to the experimental result. The inset is an equivalent circuit of the DQD capacitively coupled to  $V_{TG}$  and  $V_{G2}$  [39]

### 3.5.2 Parallel coupled lithographically defined Double Quantum Dots

A similar quantum dot device to that above but with parallel coupled quantum dots was realised by [40] on highly phosphorus doped SOI. Electron beam lithography and reactive ion etching were used to pattern a single island nanostructure (quantum dot) (Fig. 3.5.2(a)) on highly doped n-type SOI wafers. “S”, “D” and “G” represent the source, drain and side gate respectively with their applied voltages being “ $V_s$ ”, “ $V_d$ ” and “ $V_g$ ”. Fig. 3.5.2(b)) shows a schematic of the stratigraphic structure of the device. A post oxidation technique was used to confine the electron wavefunction to below 50 nm and a 10 nm capping  $SiO_2$  layer was deposited on top of the nanowires (n-doped Si) to avoid damage during fabrication processes.



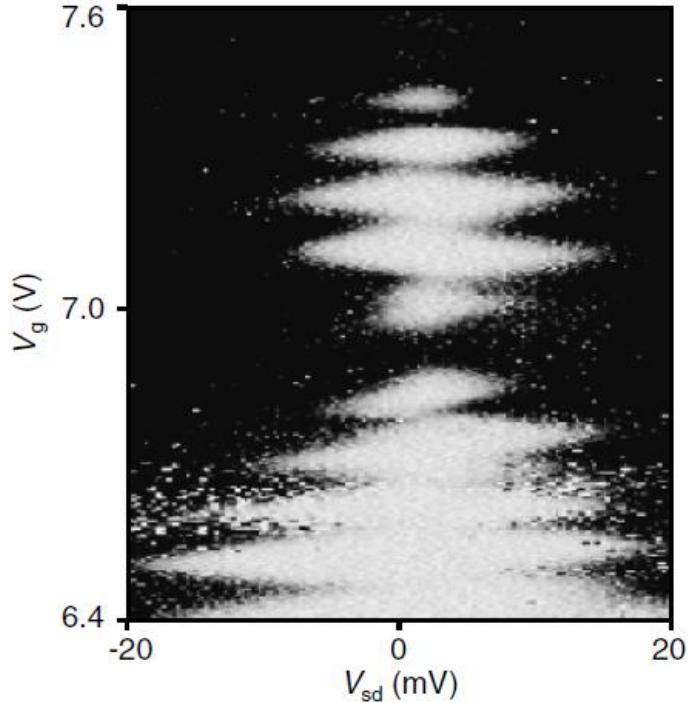
**Fig. 3.5.2(a)** SEM image of a silicon quantum dot (QD) connected via tunnel barriers to a source and drain contact (with applied voltages  $V_s$  and  $V_d$ ) and electrostatically coupled to a side gate (with applied voltage  $V_g$ ) lithographically defined on the same SOI (silicon on insulator) layer. Lighter regions represent the n-doped silicon based nanostructure and darker regions represent the insulating  $SiO_2$  layer below [40]



**Fig. 3.5.2(b)** Schematic diagram of the cross section of the wafer used to make the device in Fig. 3.5.2(a). The material thicknesses of each layer are indicated. [40]

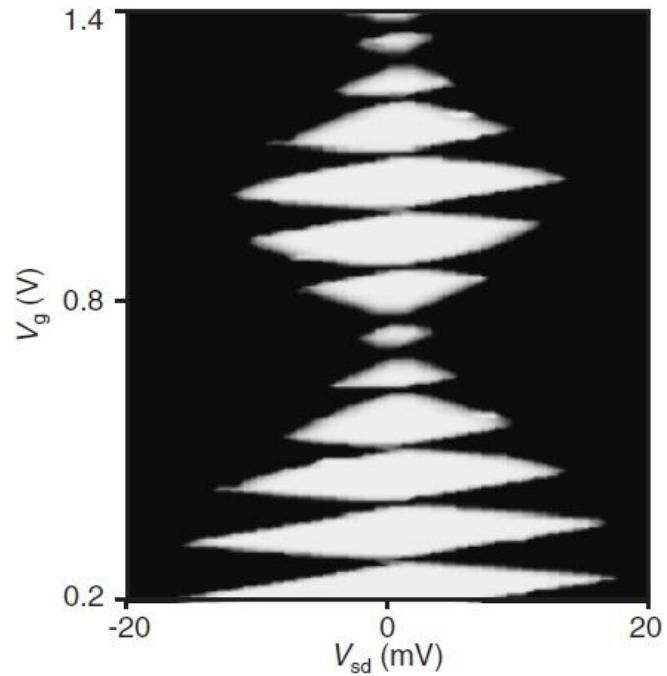
By plotting the measured variation in differential conductance  $dI_{sd}/dV_{sd}$  of the single island nanostructure versus  $V_{sd}$  ( $= V_s - V_d$ ) and  $V_g$  (Fig. 3.5.2(c)), the authors observed clear evidence of Coulomb blockade (see Section 2.1). The black and white regions respectively represent the Coulomb blockade and conducting regions. It can be clearly seen that the diamond shaped Coulomb blockade regions are modulated by a yet larger Coulomb oscillation as  $V_g$  is varied. A low temperature complementary metal oxide semiconductor (LTCMOS) integrated circuit provided power and measurement capabilities for the device. This phenomenon was explained via simulations based on the orthodox model [6] for a parallel coupled DQD and solving the master equation [10] numerically which gave results that matched experiment Fig. 3.5.2(d). A similar simulated series coupled DQD however produced differing results. A schematic diagram of the simulated parallel DQD circuit as well as the DQD structure is shown in Fig. 3.5.2(e-f) respectively. This assumed a parallel coupled system of quantum dots in which coupling from  $QD_2$  to the side gates is five times stronger

than that from  $QD_1$ . As can be seen from Fig. 3.5.2(d), the periodicity of simulated Coulomb diamonds (large and small) and gradual change in their lateral size agrees well with empirical results (Fig. 3.5.2(c)) and is due to parallel conduction through the QDs differently coupled to the gate electrode.

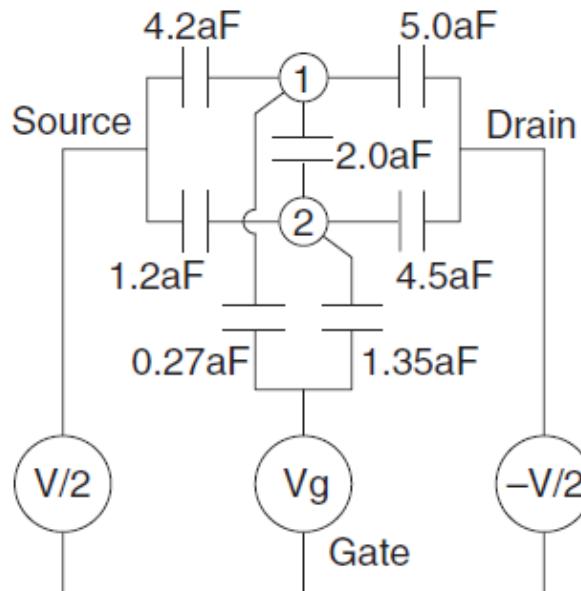


**Fig. 3.5.2(c)** Grey-scale plot of the “Coulomb diamonds” (see Section 2.4) pattern that appears when the measured differential conductance  $dI_{sd}/dV_{sd}$  through the single island nanostructure is plotted as a function of  $V_g$  and  $V_{sd}$ . Darker regions indicate higher levels of  $dI_{sd}/dV_{sd}$ . In the white regions, the system is in a Coulomb blockaded state [40]

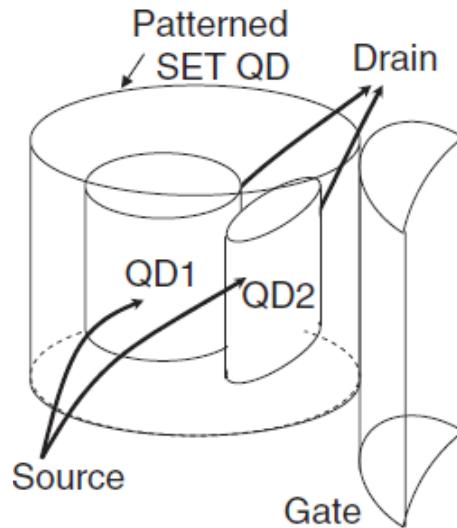
This work also highlights the difficulty in successfully fabricating lithographically defined single quantum dots in a controlled way whilst avoiding the formation of unexpected quantum dots. From Fig. 3.5.2(a), a constriction island of much smaller than  $\sim 80$  nm is required for a single quantum dot to form as intended. In this respect, the use of a non-doped Si QD with a top gate electrode (like [39]) seems to be a better approach for realizing disk-like QDs in the few electron regime since it allows flexibility in tuning the QD potential and the inversion layer in intrinsic silicon. Channel constrictions also require suitable pattern dimensions to avoid undesired QD formation during the post lithography pattern dependant oxidation process (PADOX) [41].



**Fig. 3.5.2(d)** Grey-scale plot of the “Coulomb diamonds” (see Section 2.4) pattern that appears when the simulated differential conductance  $dI_{sd}/dV_{sd}$  through the single island nanostructure is plotted as a function of  $V_g$  and  $V_{sd}$ . Darker regions indicate higher levels of  $dI_{sd}/dV_{sd}$  [40]



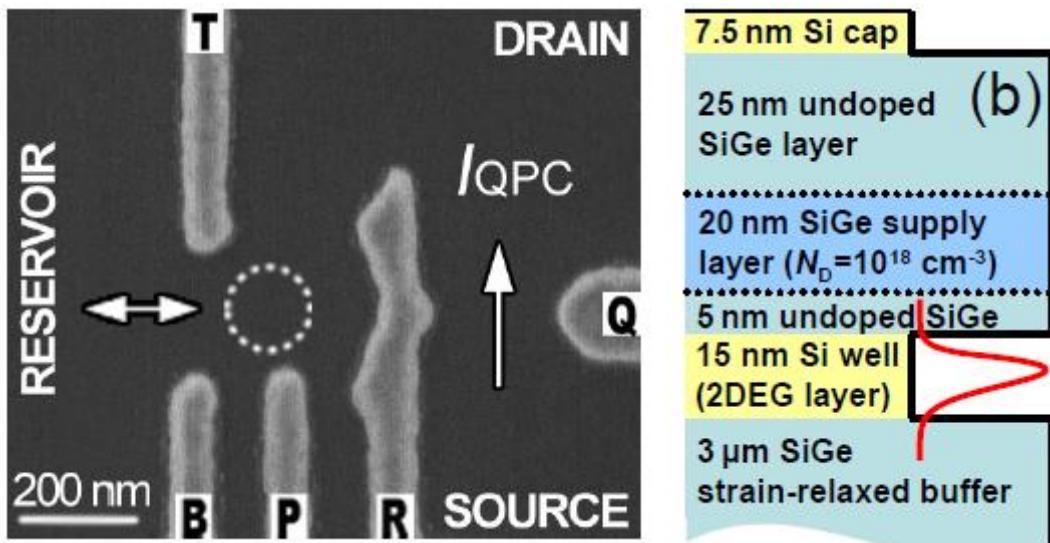
**Fig. 3.5.2(e)** Schematic circuit diagram of the DQD (labelled 1 and 2) coupled in parallel. The system parameters are indicated. [40]



**Fig. 3.5.2(f)** Schematic diagram outlining the possible configuration of  $QD_1$  and  $QD_2$  (the two quantum dots) within the silicon single island nanostructure in Fig. 3.5.2(a) [40]

## 3.6 Electron Spin manipulation in Silicon Quantum Dots

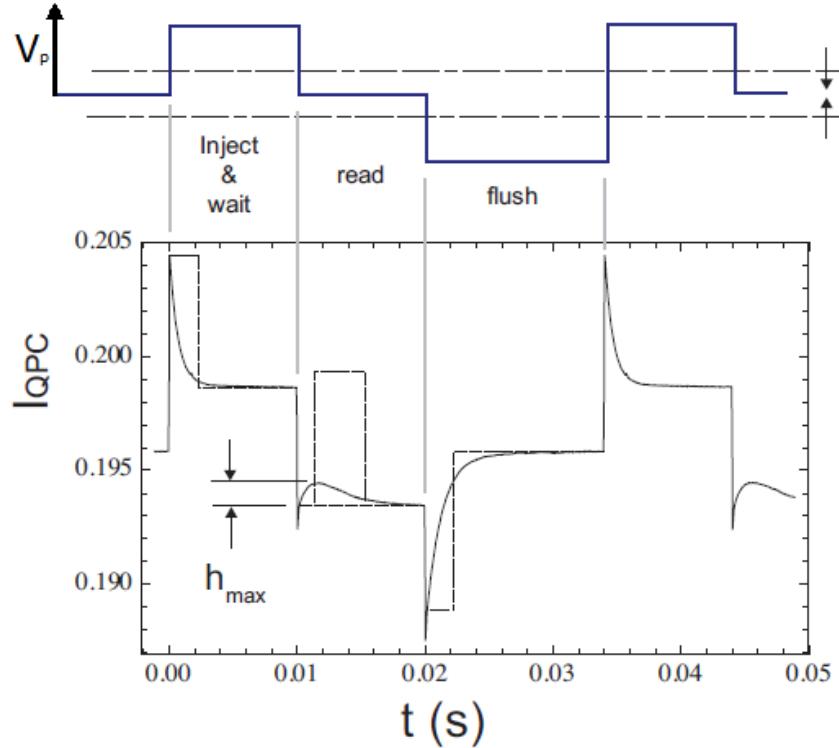
### 3.6.1 Spin relaxation time



**Fig. 3.6.1(a)** Left: SEM image of a  $Si/SiGe$  heterostructure used by Hayes *et al* consisting of a quantum point contact (QPC) and a quantum dot (QD) (outlined by the dotted white circle) electrostatically defined by surface gates. Gate P controls the electron occupation in the QD. The QD is formed in a two dimensional electron gas (2DEG) below the surface. Right: Schematic diagram of the cross section of the wafer used to make the  $Si/SiGe$  heterostructure. [42]

More recently, the work by [42] reported the first direct observation of Zeeman splitting and measurement of electron spin relaxation time in a Si-based quantum dot. Their system and

method was very much a replica of that by [17] (See Section 3.2.1) except they used a *Si/SiGe* heterostructure with surface gates “T”, “B”, “P” and “R” (See Fig. 3.6.1(a)) electrostatically defining a quantum dot in the 2 dimensional electron gas (See right of Fig. 3.6.1(a) for structure) below.



**Fig. 3.6.1(b)** Top: the three step (Inject & wait, read and flush) sequence for the potential  $V_P$  applied to gate “P” (originally proposed by [17]) used to allow measurements of the spin relaxation time  $T_1$  for an electron in a QD (see Section 2.2.1). The first step loads an electron into the QD with either spin- $\uparrow$  (ground state) or spin- $\downarrow$  (excited state) and then waits. If the electron is in the excited state, and survives the wait-time without decaying to the ground state, the second step removes it from the dot and reloads another from the reservoir into the ground state. The third step flushes the ground state electron off the dot so that the cycle can be repeated. Bottom: A trace of  $I_{QPC}$  (the current through the quantum point contact) as a function of time. The dashed lines are an artistic rendition of instantaneous values of  $I_{QPC}$  that occur during a typical cycle, the solid curve is an actual time-averaged of 1000 of these events [42]

Through applying an external magnetic field and a three-step voltage sequence  $V_P$  to gate “P” (See top of Fig. 3.6.1(b)) like that used by [17] (See Section 2.2.1), the response of the quantum point contact current  $I_{QPC}$  (which is electrostatically coupled to the quantum dot) showed clear evidence of electron spin readout and Zeeman splitting (See bottom of Fig. 3.6.1(b)) as the quantum dot’s electron occupation changed. A value for the spin relaxation time (see Section 2.2.1) of  $T_1 = 164\text{ms}$  was evaluated for a magnetic field of 1.5T. This is

more than twice that observed previously by [17] for single electron spins in a GaAs environment. Similar work was carried out by [43] using a  $Si/SiO_2$  based QD who reported  $T_1 \approx 10ms$  for an external magnetic field of  $B = 4T$  and a dependence of  $T_1^{-1} \propto B^7$ .

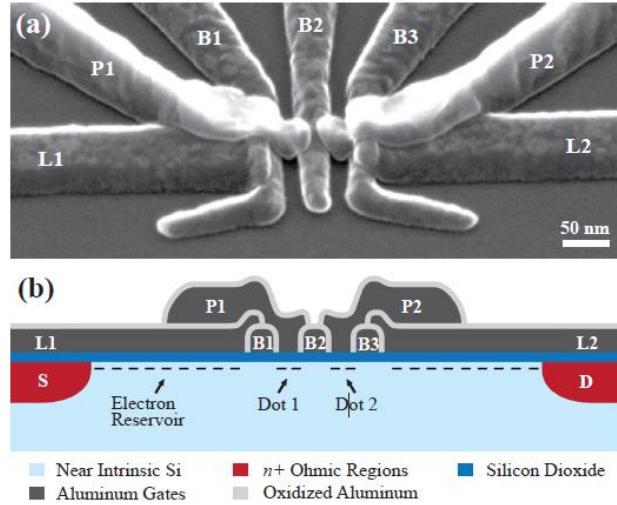
Recently, there has also been a rise in interest in selectively phosphorus implanted silicon devices. One of the longest recently observed spin relaxation time for a single electron between its  $|\uparrow\rangle$  and  $|\downarrow\rangle$  states was evaluated by [44] who successfully made a single-shot readout of a single electron spin bound to an implanted P donor in silicon. Again a similar method to that originally used by [17] was implemented to obtain relaxation time of  $T_1 = 6 \pm 2s$  with a fidelity of better than 90% for a magnetic field of  $B = 1.5T$  at a temperature of  $T \approx 40mK$ . In addition, a dependence of  $T_1 \propto B^5$  was found. This highlights the benefit of this alternative platform in that P donors in silicon can offer long electron spin lifetimes and coherence due to its long lived nuclear spin.

### 3.6.2 *Pauli-Spin Blockade*

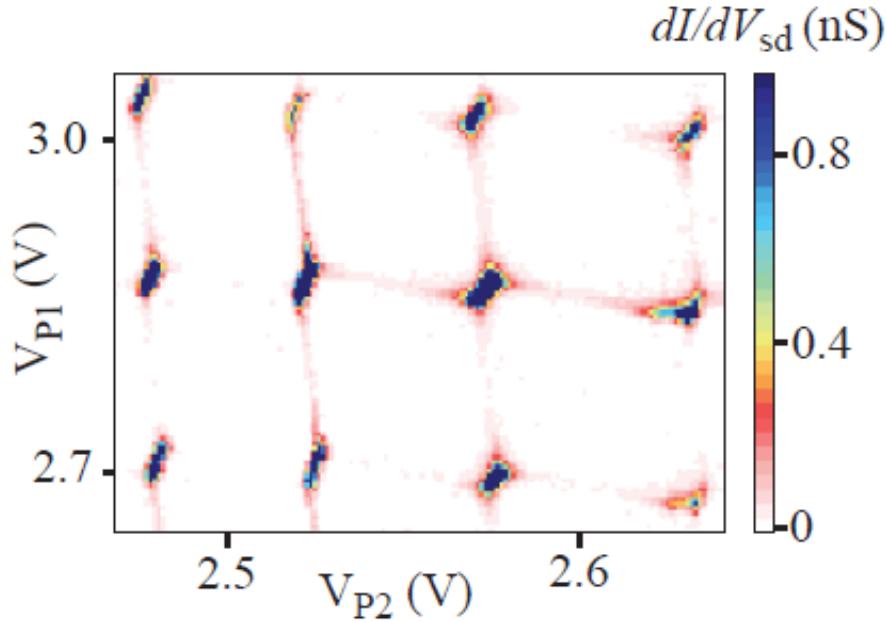
Recently, [45] managed to demonstrate the observation of Pauli spin blockade (See Section 3.3 for previous work on GaAs) in a highly tuneable silicon double quantum dot (DQD). They presented an engineered Si-DQD offering high levels of control over individual dot occupancies or inter-dot coupling. The use of a silicon MOS structure which utilizes an  $Al - Al_2O_3 - Al$  multi-gate stack allowed for quantum dots of  $\sim 30nm$  to form in the accumulation layer of electrons under the thin  $SiO_2$  when lead gates L1 and L2 were positively biased (See Fig. 3.6.2(a)).

A honeycomb pattern of the differential conductance  $dI/dV_{sd}$  through the DQD was successfully observed as gates P1 and P2 which controlled the quantum dots' potential were swept from low to high voltages (See Fig. 3.6.2(b)). With the application of a DC source-drain bias  $V_{sd}$ , the triple points of larger  $dI/dV_{sd}$  in Fig. 3.6.2(b) extended to form triangular shaped conducting regions (See Section 2.4 for theory). As can be seen from Fig. 3.6.2(c), the authors observed clear evidence of a suppression of current at one bias polarity ( $V_{sd} = 2.5mV$ ) compared to the other ( $V_{sd} = -2.5mV$ ). The non-zero current in the body of the triangular regions (for  $V_{sd} = -2.5mV$ ) indicate that electrons can tunnel freely from the  $S(0,2)$  singlet state to the  $S(1,1)$  singlet state (where  $(m,n)$  is the effective electron occupancy of the DQD and “S” and “T” represent singlet and triplet states). The opposite bias polarity ( $V_{sd} = 2.5mV$ ) however sees this current suppressed due to spin blockade. The

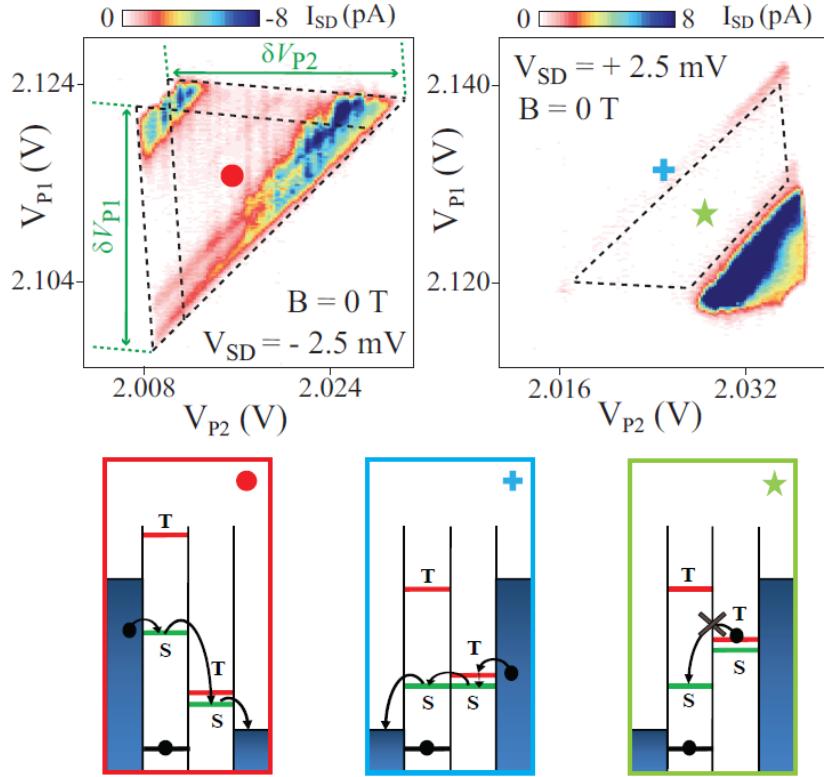
energy level diagrams in Fig. 3.6.2(c) explain more clearly what happens at particular points (indicated by the circle, cross or star) on the bias triangles.



**Fig. 3.6.2(a)** Top: SEM image of an engineered silicon metal-oxide semiconductor (MOS) structure utilizing an  $Al - Al_2O_3 - Al$  multi-gate stack that enables a double quantum dot (DQD) to be defined in an underlying electron reservoir (ER) layer, each with independent gate control (via gates P1 and P2) together with gate-tunable inter-dot coupling (via gate B2). Bottom: Schematic diagram of the cross section of the device. The red areas are the  $n^+$  source (S) and drain (D) contacts formed via diffused phosphorus [45]



**Fig. 3.6.2(b)** Measured differential conductance,  $dI/dV_{sd}$ , through the DQD from source to drain as a function of  $V_{P1}$  and  $V_{P2}$  (the respective voltages applied to gates P1 and P2). The conditions for the other gates were  $V_{L1} = V_{L2} = 3V$ ,  $V_{B1} = 0.76V$ ,  $V_{B2} = 1.2V$ ,  $V_{B3} = 1V$  and  $V_{sa} = 0V$ . [45]



**Fig. 3.6.2(c)** Top: Measured source to drain current,  $I_{sd}$ , as a function of  $V_{P1}$  and  $V_{P2}$ . The lead and barrier gate voltages were fixed at  $V_{L1} = V_{L2} = 3.2V$ ,  $V_{B1} = 0.656V$ ,  $V_{B2} = 1.176V$ ,  $V_{B3} = 0.940V$ . For  $V_{sd} = -2.5mV$  (top left graph), the ground state and excited states of a full bias triangle are shown (see Section 2.4). The current flows freely at the  $S(0,2) - S(1,1)$  ( $S$  being the singlet state and  $(n, m)$  indicating  $n$  and  $m$  electrons in the left and right QDs) transition as illustrated by the energy level diagram marked with a red dot. For  $V_{sd} = +2.5mV$  (top right graph), the current between the singlet ( $S$ ) and triplet states ( $T$ ) is fully suppressed by spin blockade (green star box) except on the bottom (blue cross box) of the bias triangle. The blue cross box shows how a leakage current may arise due to relaxation from a  $T$  into a  $S$  state [45].

Despite the success of this device architecture in being able to demonstrate very clear control over DQD single electron occupations, the  $Al$  -  $Al_2O_3$  -  $Al$  multi-gate stack does give rise to concerns over the yield of the fabrication process. The existence of a number of thin  $Al_2O_3$  layers between  $Al$  gates in addition to the thin  $SiO_2$  layer between the silicon and  $Al$  gates means there has an even greater potential for leakage between different device components when compared to the GaAs 2DEG device structures seen previously in section 3.2.1. In addition, the existence of multi-gate stacks means a number of distinct lithography steps is needed to define the conductance channel, QD and gates which lengthen the fabrication turn-over time when compared to the single lithography step used in the process in section 3.5.1.



# Chapter 4

## VLSI compatible parallel fabrication of scalable down-scaled multi-configuration Silicon quantum dot devices

### 4.1 Introduction

The previous chapter presented an overview of recent research within the area of solid state quantum dots (QD) which have led to advancements that are paving the way towards real world realisation of quantum information processing. In addition to reviewing the key methods developed to initialise, readout and manipulate single or coupled electron spins, sections 3.4-3.6 also demonstrated how silicon as a material platform has gained much traction in recent years and the factors which could potentially result in it becoming a platform of choice for realisation of a solid state qubit. This is not least because of silicon's potential for supporting much greater spin relaxation times ( $T_1 = 6 \pm 2s$  [44]) and having a much lower nuclear spin density compared to GaAs but also because many of the techniques for spin manipulation discovered using GaAs systems (see Section 3.3) are directly transferable to other material systems.

In addition, being the staple for the electronics industry, silicon has the advantage of being compatible with a diverse array of well-established device architectures and fabrication techniques as well as being compatible with very-large-scale integration (VLSI) processes. More specifically, the realisation of lithographically defined QDs (see Sections 3.4-3.5) is particularly important as it provides greater levels of scalability than some of the other

systems explored for QD systems (see discussion in sections 3.2.4 and 3.5.1). The use of in-plane Si side gates for electrostatic control of a QD's single electron occupation and the potential to realise this using a single step lithography process provides a faster means of device fabrication which could directly benefit future large scale production. This also has the added benefit of minimizing any potential for leakage between lithographically defined structures compared to the use of Al control gates.

In this work, we propose and implement the first VLSI compatible fabrication process for the parallel realisation of an array of different and scalable lithographically defined QDs systems on an intrinsic SOI (silicon on insulator) platform. A core focus of this work is enabling the fabrication of QD systems on a large scale and is an area of investigation which is missing from current literature. This work hopes to pave the way towards future realisation of large scale integrated single electron spin qubits. Considering the many potential improvements (see Section 1.2 and 3.4-3.6) intrinsic silicon may offer in comparison to GaAs, we aim to offer a fundamental platform which can be built upon to realise repeatable spin qubits and single spin turnstile operation across different scalable QD (see Section 3.4) systems whilst minimizing the potential for leakage between device components.

To reach these goals, we first undertake simulation of one of our many device designs to verify the dimensionality of our system in being able to support single electron detection and turnstile operation. Here, we also propose a novel method for single electron detection making use of the periodicity in voltage space present in the charge stability diagram of a DQD. After successful real world fabrication and measurements, we then characterise the fabrication yield and device performance whilst also exploring the limitations and benefits of our fabrication capability and process.

## 4.2 Design and dynamic simulation of symmetric Si-based double quantum dot transistors with in-plane side gates

To determine the feasibility of our device design, a 3D capacitance simulation using COMSOL Multiphysics® was first combined with Monte Carlo single-electron circuit simulations to model the dynamic detection of single spin turnstile operation across a DQD. 3D structural data of a DQD pair and multiple gate electrodes are precisely input into COMSOL's finite element method-based capacitance simulator in which potential

distributions are calculated. The capacitances between each component in the device can then be extracted and fed into the well tested single-electron circuit simulator SETSPICE.

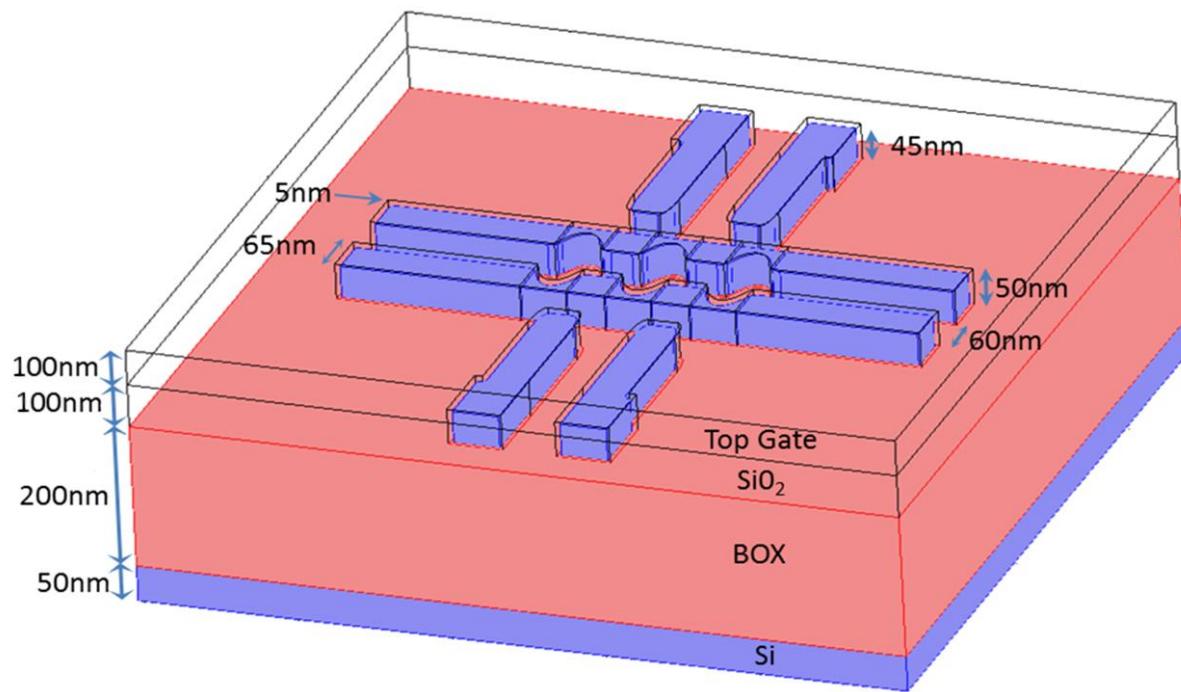
#### 4.2.1 3D design and capacitance simulation methodology

Fig. 4.2.1(a) shows a 3D structural schematic of our symmetric DQD device designed in COMSOL's electrostatics application mode with dimensions optimized after feedback from multiple fabrication trial runs (see Section 4.3). Only the 3D structures in close proximity to the QDs are shown in Fig. 4.2.1(a). Tapered connections (see Section 4.3) to larger contact pads (which are needed for connecting to measurement equipment) are not shown as the effects from these would be approximately the same across all device scale components and thus result in negligible discrepancies between these components.

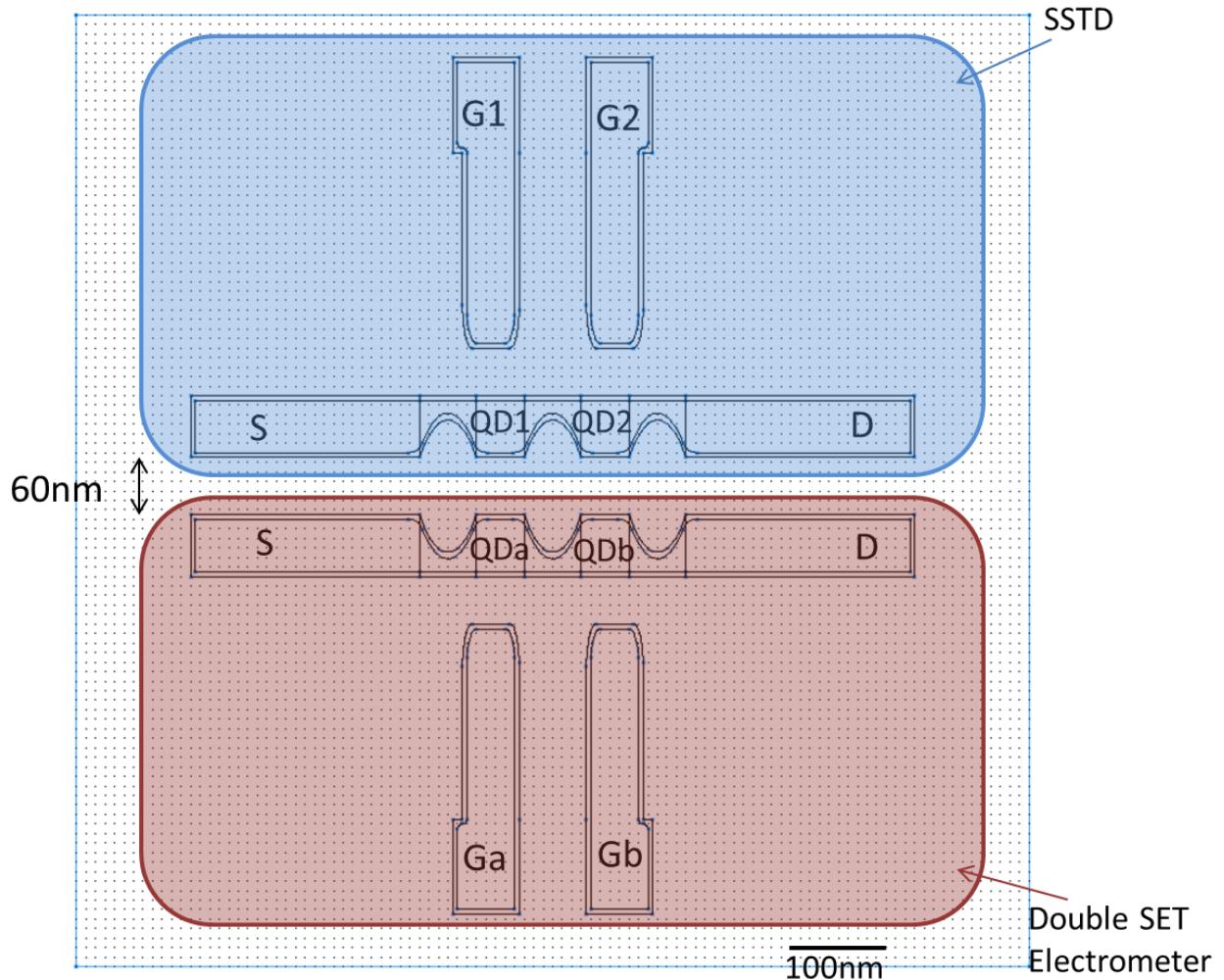
The device consists of a pair of DQD “transistors” etched into the uppermost silicon layer (blue) of the SOI wafer (See Fig. 4.2.1(a)). This is designed to be 50 nm thick initially (a thickness shown to offer single electron confinement) but with post lithography oxidation during fabrication will be reduced to a thickness of ~45 nm with ~5 nm of  $\text{SiO}_2$  passivating the surface [39]. The 200 nm thick “BOX” layer is the insulating  $\text{SiO}_2$  layer (red) of the SOI wafer and underneath this is the thick base Si substrate layer (modelled as ~50 nm thick). Each “DQD transistor” contains a DQD connected in series to a source “S” and drain “D” and coupled electrostatically to two in plane side gates which independently control the potential of each QD. This can be seen more clearly in Fig. 4.2.1(b) which shows a 2D top down view of the nanostructure in Fig. 4.2.1(a). Here the QDs are labelled  $QD_{1,2}$  and  $QD_{a,b}$  with their respective side gates being  $G_{1,2}$  and  $G_{a,b}$ . Each QD (~55 nm  $\times$  55 nm  $\times$  45 nm in size on Fig. 4.2.1(b)) is defined lithographically between two channel constrictions (which form quantum tunnel barriers under operation) on a 55 nm wide Silicon channel (dimensions take the 5 nm thermal oxide into account). Silicon is semi-conducting therefore a metal top gate with an appropriate applied voltage needs to be deposited above this in the real device to induce an inversion layer in the Si nanowires to allow for conduction through our device. To prevent leakage through this top gate, the nanowires and DQD are designed to be imbedded in a deposited insulating 100 nm thick  $\text{SiO}_2$  layer.

The device is designed such that one of the DQD transistors (bottom on Fig. 4.2.1(b)) can act as an electrometer used to detect changes in charge configuration in the other DQD. The top DQD transistor on Fig. 4.2.1(b) can thus be operated as a “single spin turnstile device”

(SSTD) in a similar way to [38]. The only difference being that here our side gates can control the electrochemical potentials of the quantum dots in addition to being able to tune the channel constrictions to form the desired tunnel barriers for turnstile operation. This design offers both scalability in the number of QDs present as well as doubling the yield in QD device fabrication since only one DQD transistor is operated as a turnstile. The electrometer does not require perfect formation of a double QD (DQD) for good sensitivity as a charge detector; therefore, functionality can be interchanged between the two DQDs depending on fabrication results.



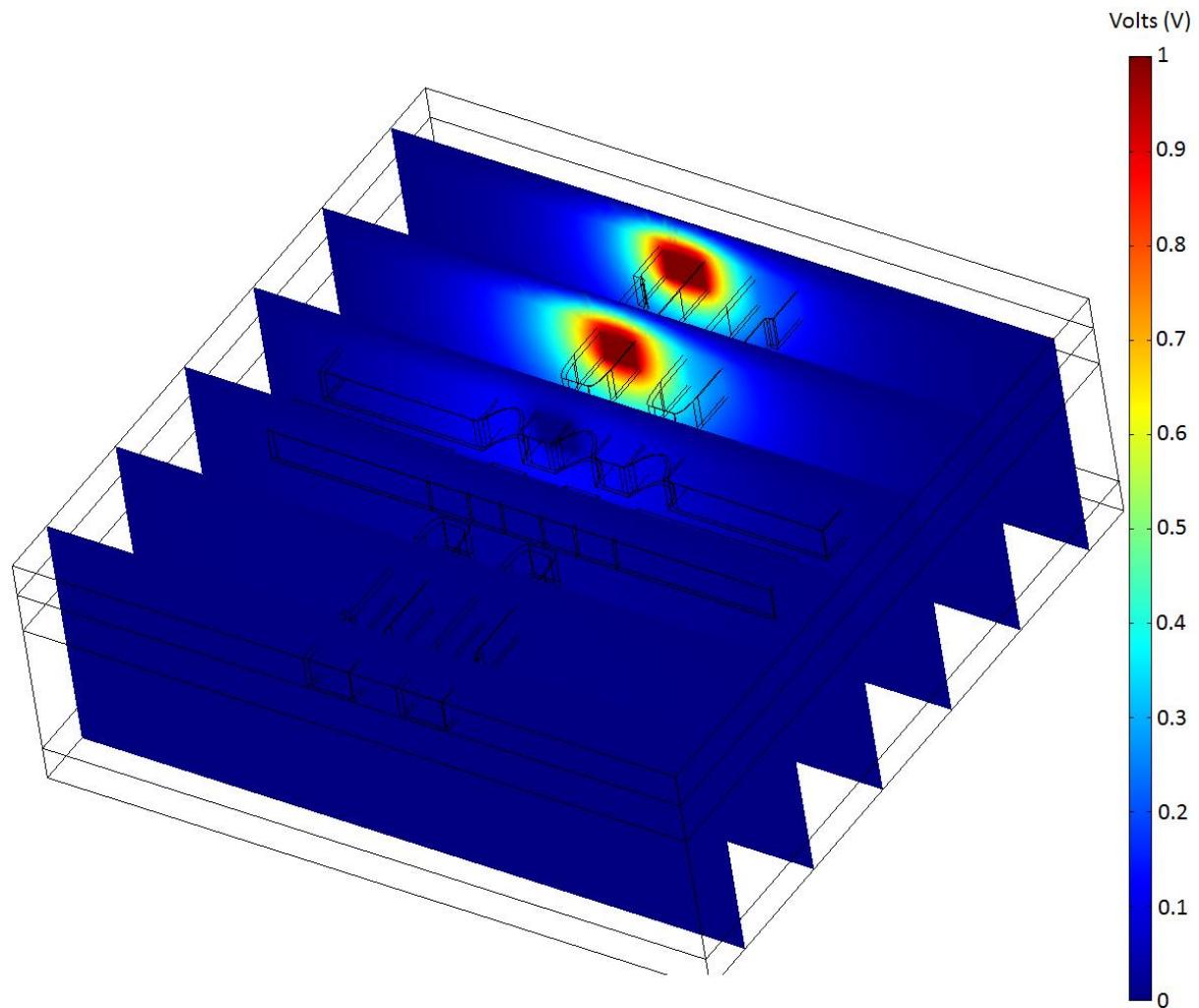
**Fig. 4.2.1(a)** Schematic 3D model of a SOI based DQD design to offer single electron detection and turnstile operation done using COMSOL Multiphysics®. The interlayer  $\text{SiO}_2$  layer in which the SOI structure is embedded and the Al top gate deposited directly above this is not shaded in for clarity.



**Fig. 4.2.1(b)** A schematic top-down 2D view of the SOI based DQD design for single electron detection and turnstile operation (same as in Fig. 4.2.1(a))

After structural specifications were set, 3D capacitance simulations were performed with COMSOL to extract the inter-part capacitance between different components of the device. To find the capacitance between any two components, 1V is first applied to one component and the other component is grounded; i.e. if we want the capacitance between  $QD_1$  and  $G_1$ , we would apply 1V to all the surfaces which define  $G_1$  in COMSOL and ground all the surfaces which define  $QD_1$  (or vice versa). Then, after solving Maxwell's equations, COMSOL allows for integration over all the surfaces which define  $QD_1$  to give us the charge  $Q$  induced on the surface of  $QD_1$  and through the use of  $Q = CV$  with  $V = 1V$  gives us the inter-part capacitance  $C$  between  $QD_1$  and  $G_1$ . Throughout this process all other surfaces of the structure were set to have continuity boundary conditions except for the outermost boundaries that define the whole system which were also grounded. Fig. 4.2.1(c) below shows the potential distribution of our system after solving Maxwell's equations when 1V is

applied to  $G_1$  with  $QD_1$  grounded. Similar processes were carried out for the other inter-part capacitances of our system.



**Fig. 4.2.1(c)** cross-sectional plots of the potential distribution around the system solved using Maxwell's equations after 1V is applied to  $G_1$  and  $QD_1$  grounded.

#### 4.2.2 Capacitance simulation results

Variable	Capacitance/aF
$C_{G1-S}$	3.01
$C_{G1-Sub}$	11.34
$C_{G1-QD1}$	3.70
$C_{G1-QD2}$	2.16
$C_{G1-G2}$	9.56
$C_{G2-QD2}$	3.71
$C_{G2-QD1}$	2.17
$C_{G2-D}$	3.01
$C_{G2-Sub}$	11.39
$C_{QD1-Sub}$	6.96
$C_{QD2-Sub}$	6.95
$C_{QD1-QD2}$	2.96
$C_{QD1-QD1}$	1.86

Variable	Capacitance/aF
$C_{G2-S}$	3.01
$C_{G2-Sub}$	11.34
$C_{G2-QD2}$	3.70
$C_{G2-QD1}$	2.16
$C_{G2-G1}$	9.56
$C_{G1-QD2}$	3.71
$C_{G1-QD1}$	2.17
$C_{G1-D}$	3.01
$C_{G1-Sub}$	11.39
$C_{QD2-Sub}$	6.96
$C_{QD1-Sub}$	6.95
$C_{QD2-QD2}$	1.86
$C_{QD2-QD1}$	2.96

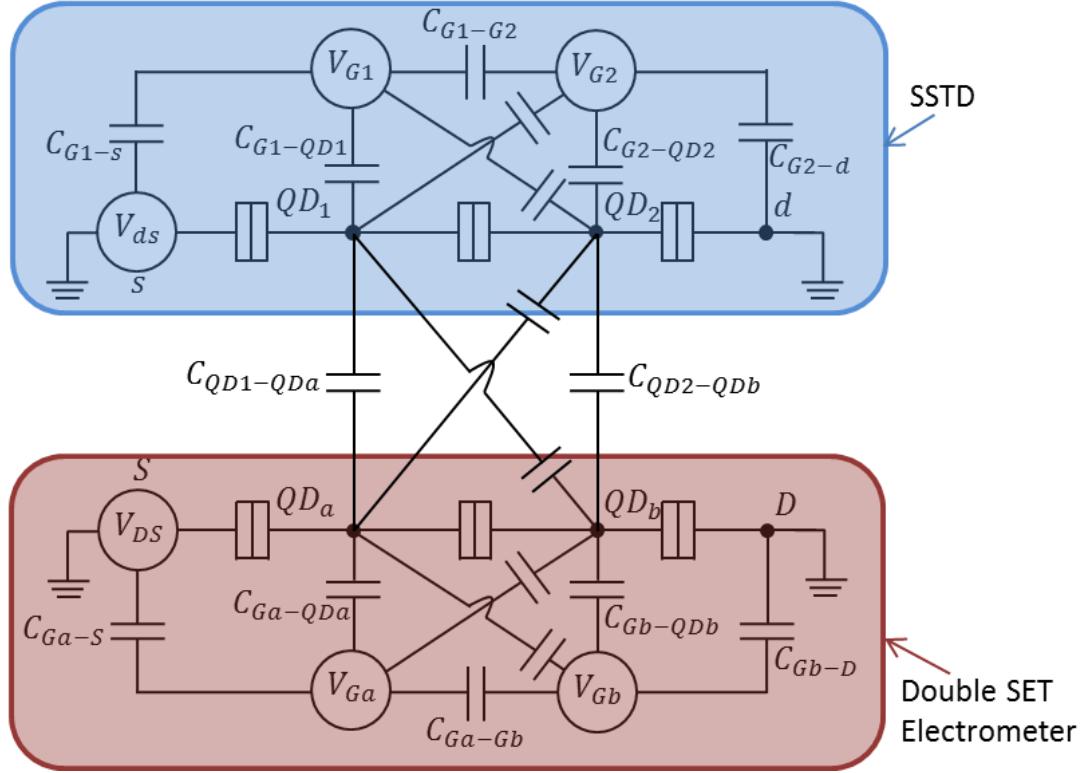
**Table 4.2.2(a)** Tables showing the extracted inter-part capacitances between different components of our device obtained using COMSOL (see Fig. 4.2.1(b) for component names)

In Table 4.2.2(a) I summarize the extracted inter-part capacitances of our system. The subscripts of each capacitance label refer to the different components of the system labelled in Fig. 4.2.1(b). The subscript “Sub” refers to the lowest Si substrate layer shown on Fig. 4.2.1(a). The values agree with the expectation that inter-part capacitance is in general less for components with greater separation and smaller surface areas.

#### 4.2.3 Equivalent circuit and device simulation methodology

A well tested Monte-Carlo based single-electron circuit simulator SETSPICE (see Section 2.3 or [5] was used for dynamic circuit simulations which is capable of numerically solving the ‘master equation’ [10] which describes the rate of change of probability,  $\rho_n(t)$ , of finding a single quantum dot in a charge state of ‘ $n$ ’ at time ‘ $t$ ’ (see Section 2.3). An equivalent circuit of our device (see Fig. 4.2.3(a)) is first designed and then input via programming into the SETSPICE simulator. Simulations are then run which can output the current and voltage values at each of the nodes of the circuit. As can be seen from Fig. 4.2.3(a), the inter-part capacitances between all device components were extracted from COMSOL and implemented in the circuit schematic. As COMSOL cannot simulate tunnel barriers (the

channel constrictions), these were all defined to have an appropriate resistance and capacitance of  $500 \text{ k}\Omega$  and  $4 \text{ aF}$  respectively. All components of the circuit were capacitively coupled (using the simulated values) to ground (which was taken as the lowest Si substrate layer in Fig. 4.2.1(a)) however this is not shown on Fig. 4.2.3(a) to avoid cluttering the key aspects of the circuit schematic.

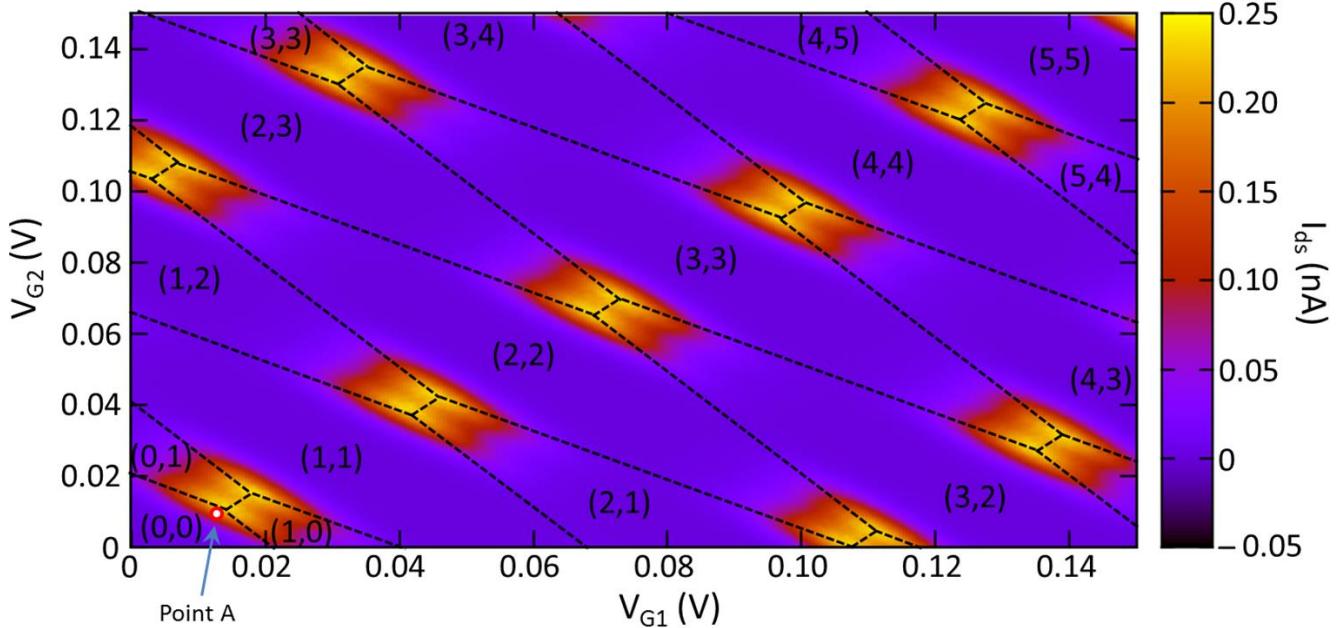


**Fig. 4.2.3(a)** Equivalent circuit diagram of the device shown in Fig. 4.2.1(a) and (b).  
Respective capacitance values are shown in Fig. 4.2.2(a).

Simulations of the device when only operating one of the DQD transistors (e.g. just the SSTD) gave the characteristic DQD charge stability diagram. A clear honeycomb pattern was seen when the source to drain current through the DQD,  $I_{sd}$ , was plotted as a function of voltages  $V_{G1}$  and  $V_{G2}$  applied to side gates G1 and G2 respectively (see Fig. 4.2.3(b)). The source to drain voltage was set to  $V_{ds} = 1\text{mV}$  (the reason why there are small bias triangles present at the triple points) with an operation temperature of  $4.7\text{K}$ . The electrometer in this case had a source to drain bias voltage of  $V_{DS} = 0\text{V}$  with side gate voltages  $V_{Ga} = V_{Gb} = 0\text{V}$ . The wire frame on Fig. 4.2.3(b) outlines the approximate shape of the charge stability diagram of the DQD and  $(n, m)$  labels the DQD electron configuration where  $n$  and  $m$  are the number of electrons in  $QD_1$  and  $QD_2$  respectively.

To undertake single electron turnstile operation, we sweep  $V_{G1}$  and  $V_{G2}$  across an appropriate path on Fig. 4.2.3(b) to get a sequence of desired configuration  $(n, m)$  of electrons in the DQD. To offer detection of the values of  $(n, m)$ , multiple methods were explored including

that suggested by [24] (see Section 3.2.4). Simulated results using this method however didn't allow for the level of control needed for detection of turnstile operation due to the gates  $G_1$  and  $G_2$  coupling too strongly to  $QD_a$  and  $QD_b$  and affecting their potential just as much as the charge states of  $QD_1$  and  $QD_2$ .



**Fig. 4.2.3(b)** A plot of the simulated source to drain current  $I_{ds}$  through a DQD as a function of side gate voltages  $V_{G1}$  and  $V_{G2}$ . The wire frame highlights the honeycomb pattern and outlines the approximate shape of the charge stability diagram of the DQD (see Section 2.4)

Therefore, alternative methods were explored. The most promising results were obtained with a more dynamical approach which allowed for time dependent non-invasive detection of charge states. This means true single electron detection that does not affect the charge state of the SSTD and allows for detection even if the current through the SSTD is immeasurably small, which is likely if we are in the single electron limit.

To achieve this, the electrometer (see Fig. 4.2.1(b)) is set to a point in its charge stability diagram (same as Fig. 4.2.3(b) except the horizontal and vertical axis would be  $V_{Ga}$  and  $V_{Gb}$ ) close to a triple point (e.g. point A) between three regions of charge stability (see Section 2.4 for theory) such that electrometer current  $I_{DS}$  is just before its peak value and can increase slightly with  $V_{Ga}$  and  $V_{Gb}$  (this ensures a large signal to noise ratio).  $V_{G1}$  and  $V_{G2}$  are then swept at a constant rate through a straight line in voltage space (i.e. anywhere across Fig. 4.2.3(b)) allowing for turnstile operation in the DQD of the SSTD. Due to the capacitive coupling between the DQD of the SSTD and the DQD of the electrometer, the source to drain current  $I_{DS}$  through the DQD of the electrometer should be sensitive to changes in charge state of the DQD of the SSTD. Therefore plotting  $I_{DS}$  as a function of increasing (decreasing)

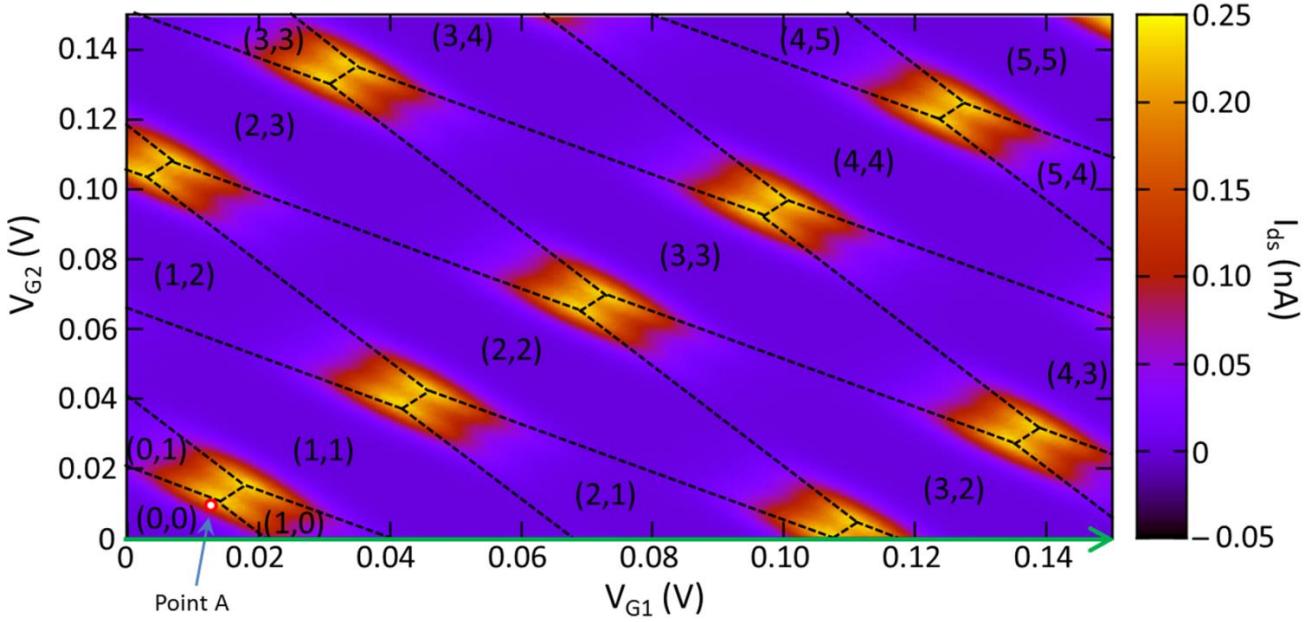
$V_{G1}$  and  $V_{G2}$  should show periodic decreases (increases) in  $I_{DS}$  due to periodic increases (decreases) in the number of electrons on the DQD of the SSTD. Essentially, we use the electrometer much like how a quantum point contact is used for charge detection (see Section 3.2 or e.g. [17]). The reason why our electrometer is a DQD transistor instead of a simpler single electron transistor (SET) (see Section 2.2) is that a symmetric design like this (see Fig. 4.3.1(b)) allows for greater fabrication yield in functioning devices. Therefore, in practice, if one DQD transistor doesn't function as expected, it can be used as the electrometer and the good transistor gets used as the SSTD; i.e. the operation of the two can be interchanged.

Below I present and analyse some simulation results on the detection of single electron turnstile using the above method when sweeping  $V_{G1}$  and  $V_{G2}$  across a path on Fig. 4.2.3(b).

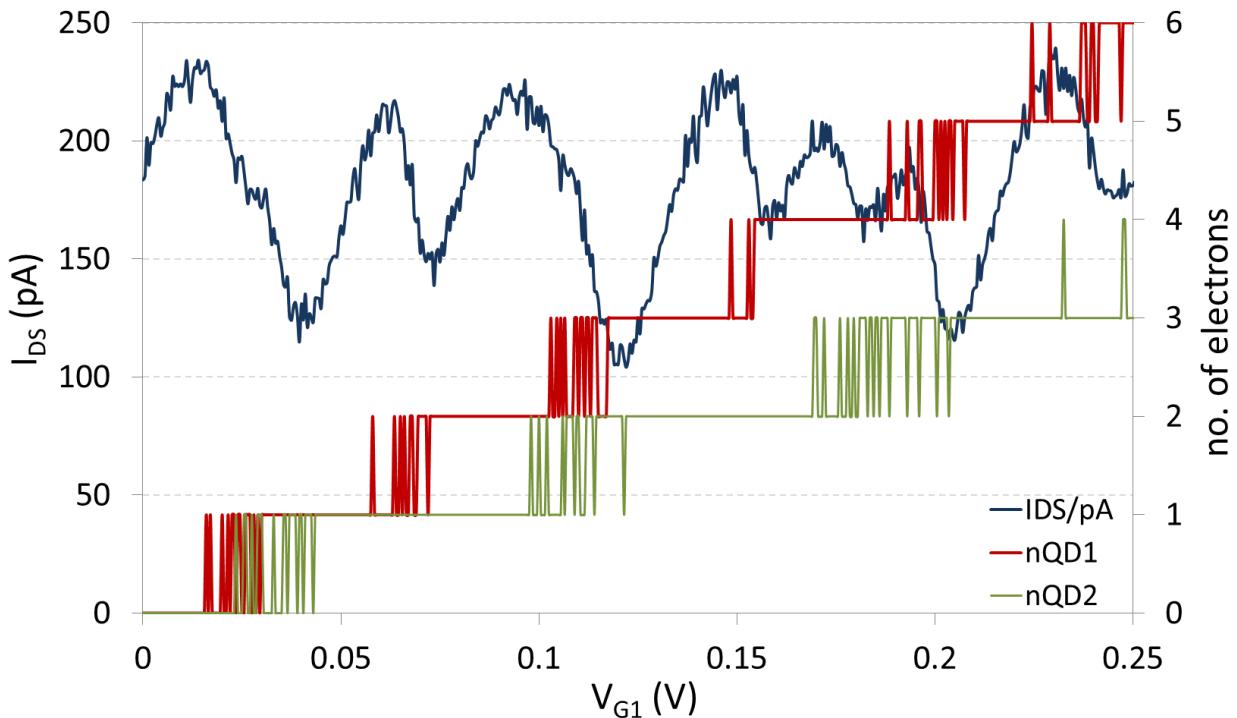
#### 4.2.4 Single electron turnstile detection simulation results and analysis

By setting the electrometer to an equivalent point to point A on Fig. 4.2.4(a) on its own charge stability diagram ( $V_{Ga} = V_{Gb} = 11.5mV$ ), and sweeping  $V_{G1}$  from  $0mV$  to over  $500mV$  (the path outlined by the green arrow on Fig. 4.2.4(a)), we can pulse the DQD of the SSTD through the charge configurations crossed by the green arrow on Fig. 4.2.4(a). Operating the system at  $4.7K$  with a source to drain bias of  $V_{ds} = 1mV$  and  $V_{DS} = 1mV$  for both the SSTD and electrometer respectively, a plot of the electrometer current  $I_{DS}$  as a function of  $V_{G1}$  (see Fig. 4.2.4(b)) clearly shows distinctive negative shifts in the magnitude of this current when the electron occupation of the DQD of the SSTD increases. Places where  $I_{DS}$  increases are due to the capacitive coupling to  $V_{G1}$  which is increasing at a steady rate and thus increases the potential at the DQD of the electrometer.

A key question however is how to distinguish whether a shift in  $I_{DS}$  is due to electrons transferring to  $QD_1$  or  $QD_2$ . As can be seen from Fig. 4.2.4(b), we can use the magnitude of shift in  $I_{DS}$  to clearly distinguish between whether a single electron was added to the DQD or two electrons at the same time (difference between the 1<sup>st</sup> and 2<sup>nd</sup> shift which are a double electron and single electron transfer respectively). However, we can not use this same technique when distinguishing between a single electron transfer in  $QD_1$  or  $QD_2$  as the magnitude of shift in  $I_{DS}$  when an electron is added to  $QD_1$  is the same as that when an electron is added to  $QD_2$ . In addition, looking at Fig. 4.2.4(b), this shift in  $I_{DS}$  seems to be different in magnitude for different values of  $V_{G1}$  which is possibly due to the non-linear nature of the charge stability diagram (Fig. 4.2.4(a)).



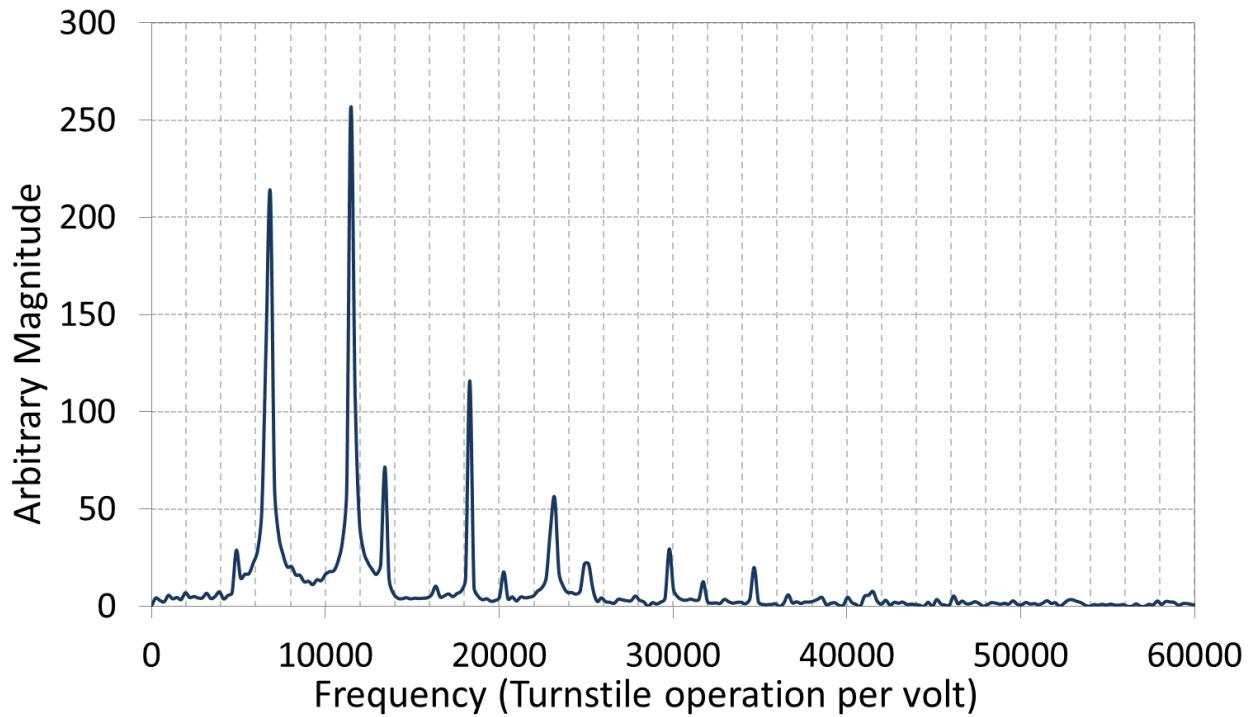
**Fig. 4.2.4(a)** A plot of the simulated source to drain current  $I_{DS}$  through a DQD as a function of side gate voltages  $V_{G1}$  and  $V_{G2}$ . The wire frame outlines the approximate shape of the charge stability diagram of the DQD (see Section 2.4). The green arrow shows the direction of sweeping of  $V_{G1}$  in the simulation of turnstile detection.



**Fig. 4.2.4(b)** A plot of the electrometer current  $I_{DS}$  (blue trace) as a function of  $V_{G1}$  (the side gate voltage of the SSTD).  $V_{G2} = 0\text{mV}$  and  $V_{Ga} = V_{Gb} = 11.5\text{mV}$ . The red and green trace respectively give the number of electrons present in  $QD_1$  and  $QD_2$  of the SSTD as a function of  $V_{G1}$ .

A possible solution to this however is to exploit the periodicity in changes in  $n_{QD1}$  and  $n_{QD2}$  (no. of electrons in  $QD_1$  and  $QD_2$  respectively) as a function of  $V_{G1}$  (see Fig. 4.2.4(b)). This is due to the periodicity that exists in the charge stability diagram of a DQD (e.g. Fig. 4.2.4(a)) and will be present as long as we go in a linear path in any direction in the space provided by

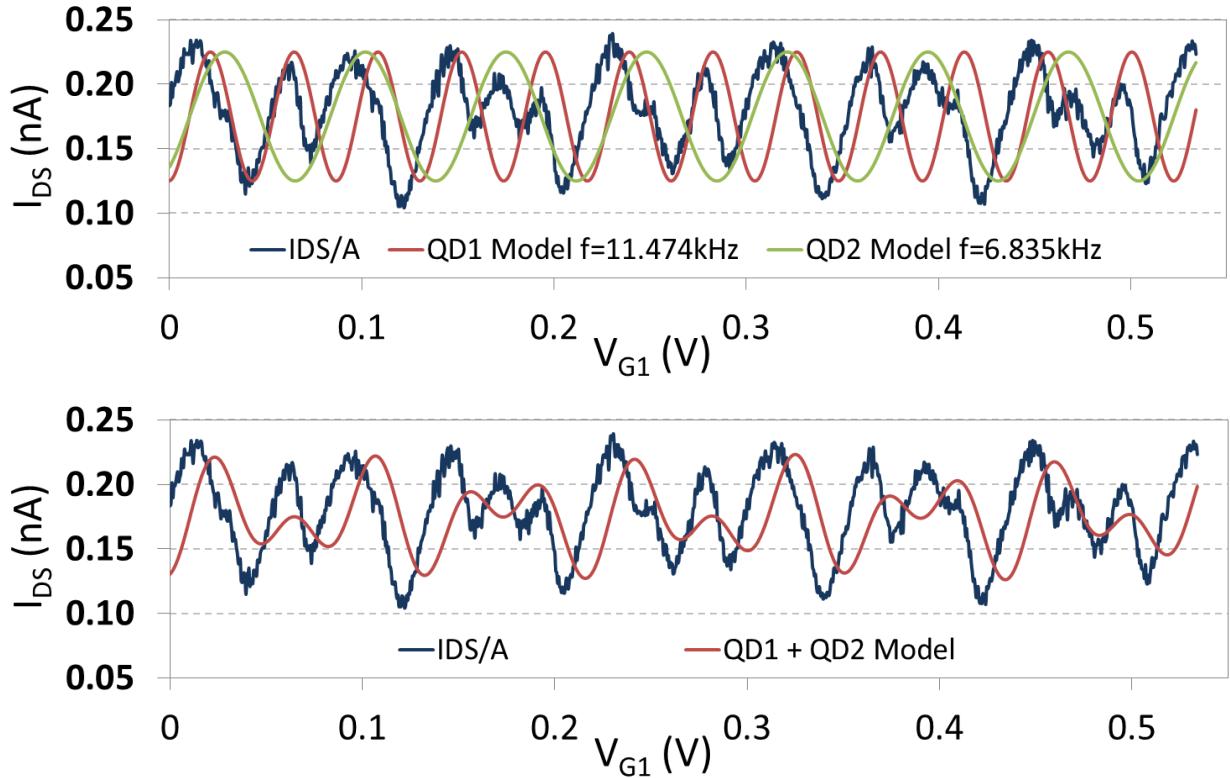
$V_{G1}$  and  $V_{G2}$  (Fig. 4.2.4(a)). Therefore, by Fourier transforming the signal of  $I_{DS}$  in Fig. 4.2.4(b), we can extract two frequency peaks corresponding to the addition of electrons in  $QD_1$  and  $QD_2$ . This is presented in Fig. 4.2.4(c) which is a Fourier transform of  $I_{DS}$ . It must be noted that frequency here is in voltage space, so corresponds to the number of transitions per volt. Two distinct peaks are present at lower frequencies which correspond to the turnstile operation per unit volt in  $QD_1$  and  $QD_2$  respectively. The lower frequency corresponds to transitions in  $QD_2$  as transitions here are at a slower rate than in  $QD_1$  (the higher frequency) because we are only sweeping across  $V_{G1}$  (see Fig. 4.2.4(a)). This is also a result of the fact that  $QD_1$  has greater capacitive coupling to G1 than  $QD_2$  (see Fig. 4.2.2(a)).



**Fig. 4.2.4(c)** A plot of the Fourier transform of the electrometer current  $I_{DS}$  (blue trace in Fig. 4.2.4(b)). The two dominant (largest amplitude) frequencies correspond to the rate of turnstile operations in  $QD_1$  (higher frequency) and  $QD_2$  (lower frequency). The naturally larger peak at 0 frequency due to the offset of  $I_{DS}$  from zero was removed.

By fitting sinusoidal functions with the two dominant frequencies in Fig. 4.2.4(c) to the trace for  $I_{DS}$  (see Fig. 4.2.4(d)), we can determine which of the shifts in magnitude of  $I_{DS}$  corresponds to a transition in the number of electrons in  $QD_1$  or  $QD_2$ . The peaks of these sine functions are fitted to match the position at which transitions take place (i.e. the peaks are fitted to the points when  $I_{DS}$  is decreasing). By comparing Fig. 4.2.4(c) with Fig. 4.2.4(b), we can clearly see that the sine functions are successful in associating periodic decreases in current with the correct increase in electron in  $QD_1$  or  $QD_2$ . This method should be robust regardless of what linear path we take in voltage space on Fig. 4.2.4(a) and thus allows for

the dynamic detection of single electron turnstile operation in a DQD. Part of this work was presented orally at the 37th International conference on micro and nano engineering in 2011 and in the 2013 IEEE Transactions on Nanotechnology (See List of Publications).



**Fig. 4.2.4(d) Top:** A plot of the electrometer current  $I_{DS}$  (blue trace in Fig. 4.2.4(b)) as a function of  $V_{G1}$  (the side gate voltage of the SSTD) with two sinusoidal functions fitted (for turnstile operations in  $QD_1$  and  $QD_2$ ) to the dominant frequencies in Fig. 4.2.4(c). This allows us to determine which shifts in the magnitude of  $I_{DS}$  corresponds to turnstile operations in  $QD_1$  (red) or  $QD_2$  (green). **Bottom:** The same plot as the top graph, except the two sinusoidal functions have been added together to more clearly show the matching of periodic single electron transitions to shifts in the electrometer current  $I_{DS}$ .

### 4.3 A VLSI compatible parallel fabrication process

The simulations in the previous sections gave a promising indication of the feasibility of our designed platform and its ability to support both single electron turnstile operation as well as single electron detection. In order to realise our designed system and develop the device fabrication process, we firstly reviewed the advantages and characteristics of different device architectures previously explored in the literature (see Chapter 3). Through this, key features and designs were identified which would form the fundamental criteria of our fabrication approach. Crucially this needs to support:

- A scalable device architecture
- VLSI compatible processes

- Parallel fabrication of a large number of QD systems
- Rapid chip turnover and fabrication time
- Scalability in the no. of fabricated devices with minimal effect on the fabrication turnover time
- A high device fabrication yield
- Repeatable device dimensionality and performance

As mentioned in this chapter's introduction in Section 4.1, by using lithographically defined Si QDs, we can capture the benefit of greater scalability versus conventional 2DEG device structures (Sections 3.2 and 3.3) as well as benefit from silicon's low-spin nuclear background and smaller spin orbit coupling to allow for greater fidelity in single spin manipulations.

Taking these criteria into account and through process optimisation, we propose the first very large scale integration (VLSI) compatible electron beam lithography (EBL) process using HSQ resist for the parallel fabrication of reproducible intrinsic Si based QD transistors with potential for scalability in the quantum architecture. A schematic process flow diagram is outlined in Fig. 4.3(a). Nine major steps with five being lithography related are needed to fabricate our intrinsic Si DQDs devices. Only one lithography step needed for the SOI device component definition. To start, alignment marks are first defined on a SOI sample. A  $\text{SiO}_2$  mask is then deposited above the position of the nanostructure region for each device to act as a doping mask during a phosphorosilica spin on dopant process. This maintains the region's intrinsic Si property whilst the rest of the SOI is heavily phosphorus doped. E-beam lithography with HSQ resist and reactive ion etching (RIE) then defined our device structure in the SOI. The devices are oxidized briefly to form a  $\text{SiO}_2$  outer layer which both passivates the surface and reduces our QD dimensions. A top gate oxide is then deposited above this to form a layer which prevents leakage to the Al top gate.

In the sub-sections below, we go into more detail on each step of the fabrication process, giving the reasons behind their implementation and provide analysis on the pros and cons of each approach.

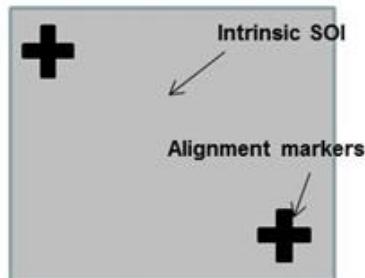
#### 4.3.1 *Chip and Mask Design*

In order to create a standardised scalable fabrication process, a chip and lithography mask design must first be created to define not only the layout of devices but also core features which make each chip self-sufficient.

## Fabrication Process Flow Diagram

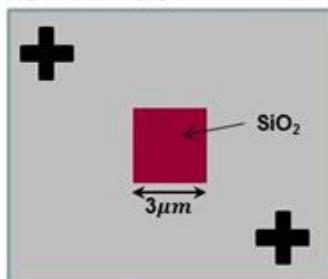
### Step 1

- Define and reactive ion etch (RIE) alignment markers into 50nm thick SOI by EBL and ZEP520 resist



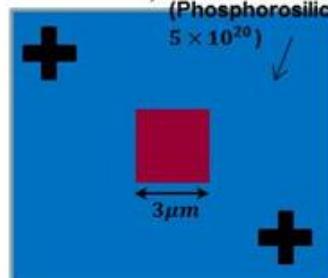
### Step 2

- PECVD of 100nm multilayer  $\text{SiO}_2$  as P-dopant diffusion mask (for nanowire region) using photolith. and RIE



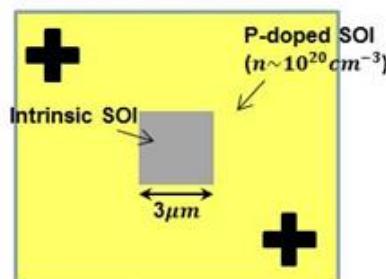
### Step 3

- Spin-on-dopant + Thermal Drive-in at  $950^{\circ}\text{C}$  (P-dopant, resultant  $n \sim 10^{20} \text{ cm}^{-3}$ )
- Spin-on-dopant (Phosphosilicafilm  $5 \times 10^{20}$ )



### Step 4

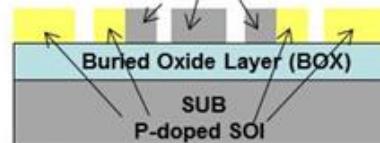
- Removal of spin-on-dopant &  $\text{SiO}_2$  diffusion mask by 20:1 BHF Wet Etch for 5min



### Step 5

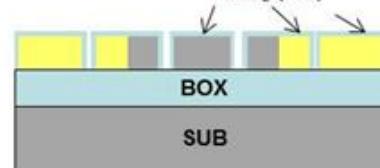
- HSQ resist spin & EBL to define nanostructure
- Post bake HSQ @  $250^{\circ}\text{C}$  for 4m30s
- RIE of SOI based with  $\text{SF}_6 / \text{O}_2$
- 20:1 BHF wet removal of HSQ resist

Intrinsic SOI with nanoscale device pattern



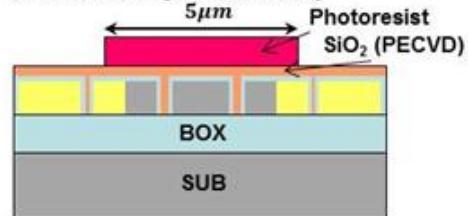
### Step 6

- Dry thermal oxidation ( $950^{\circ}\text{C}$ ) for formation of 20nm  $\text{SiO}_2$  surface oxide and reduce QD size to  $<35\text{nm}$
- $\text{SiO}_2$  (OX)



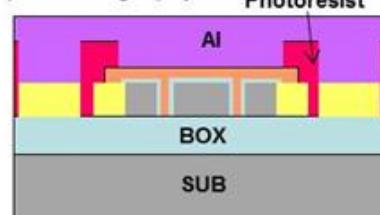
### Step 7

- PECVD 100nm of interlayer  $\text{SiO}_2$
- Define structure with photolith. and RIE with  $\text{CHF}_3/\text{Ar}$  chemistry



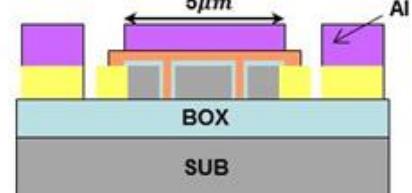
### Step 8

- Evaporate 200nm Al and define top gate & probe contact pads via photolithography

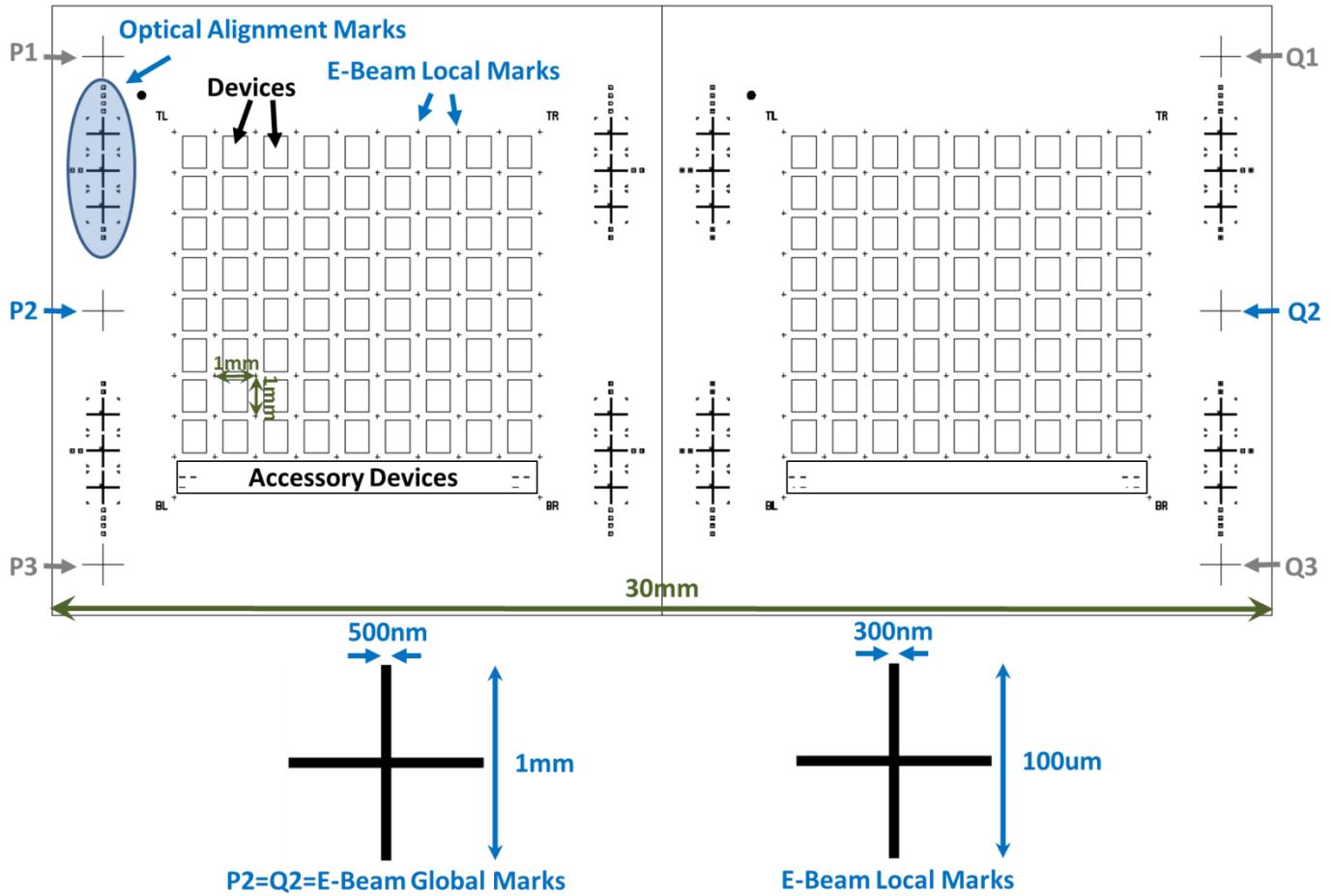


### Step 9

- Lift off photoresist
- RTA of Al contact layer at  $350^{\circ}\text{C}$



**Fig. 4.3(a)** Schematic diagram of our VLSI compatible process for the fabrication of high density quantum devices. The schematic diagram in each step focuses on one device out of an array across a chip. Steps 1-4 have top down schematic views whereas steps 5-6 have cross sectional schematic views for greater clarity.



**Fig. 4.3.1(a)** Schematic chip sized design and layout

Fig. 4.3.1(a) shows the design of our proposed chip including the devices and alignment mark layout needed for device fabrication. An important feature of the design is that it is scalable so that the number of devices on each chip can be expanded to increase chip capacity or each chip can be arrayed across a whole wafer with ease without affecting detailed device level design. This can then tailor and maximize fabrication output to differing demands without significantly affecting the fabrication time – a key benefit of the process we develop capable of parallel fabrication. Here (Fig. 4.3.1(a)), each chip, and thus each fabrication run will complete two chips worth of devices, each containing 72 devices.

Three sets of optical alignment marks and one set of e-beam alignment marks are used to align the four lithography steps. Each time a layer is created the corresponding alignment marks are altered (either covered by material or etched) and therefore an alternative set is needed for the next step. Each device can be a maximum of 1 mm in size and surrounded by 4 local e-beam marks at the corners (device positions approximately outlined by the array of rectangles in Fig. 4.3.1(a)). The e-beam alignment we developed uses both the coarse alignment marks P2 and Q2 as well as fine local alignment marks which are key to achieving a lithographical misalignment error of below 5 nm.

The chip design is such that nanostructures of devices can be altered and tailored to future requirements whilst still being compatible with the larger structures and our fabrication methodology.

To ensure each chip can be self-sufficient, one of the unique features about this chip design is the array at the bottom of each containing “Accessory Devices” which can be used to not only characterise the substrate, but also fabrication results and lithographical misalignment. This enables us to extract information which is key when trying to understand the performance of devices on a particular chip or identifying ways in which the fabrication methodology can be improved. These include (Fig. 4.3.1(b)):

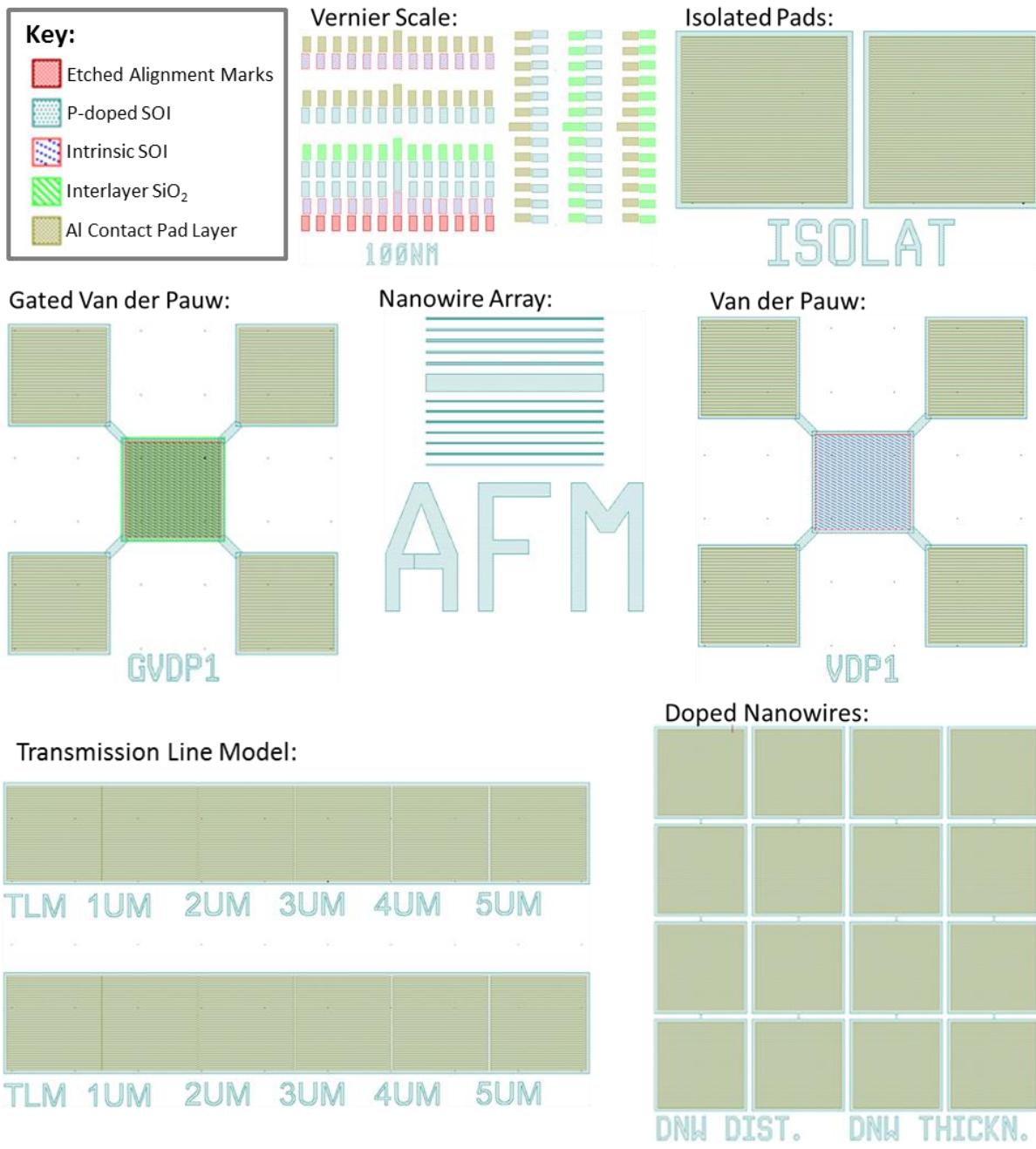
- Vernier scale (4 at each corner of a chip) allows us to identify and measure the degree misalignment or rotation when performing different lithography fabrication steps with a resolution of 100 nm.
- Isolated SOI pads to check for leakage through the BOX and the underlying Si substrate
- Nanowires array to characterise the depth of etching by AFM
- Van der Pauw (VdP) and gated VdP devices to be used with a 4 point probe measurement to characterize our spin-on-doping process and the effectiveness of the Al top gate
- Doped/intrinsic nanowires of varying thickness and length between contact pads for further doping and SOI conductance characterisations
- Transmission line model (TLM) devices for resistivity characterisations

These accessory devices are designed such that they are fabricated in parallel with our QD systems. For any device however, lithographical misalignment is a major challenge which severely limits the resolution of device lithography. For each lithographical step in the process therefore, we have designed such that there is accommodation for a misalignment of 1  $\mu\text{m}$  between steps. This is empirically the minimum degree of error for optical alignment during photolithography with our system which is an EVG620T Automated Mask Alignment System®<sup>1</sup>. This is also the reason why different device lithography layers of the accessory devices in Fig. 4.3.1(b) are seen to be slightly different sizes.

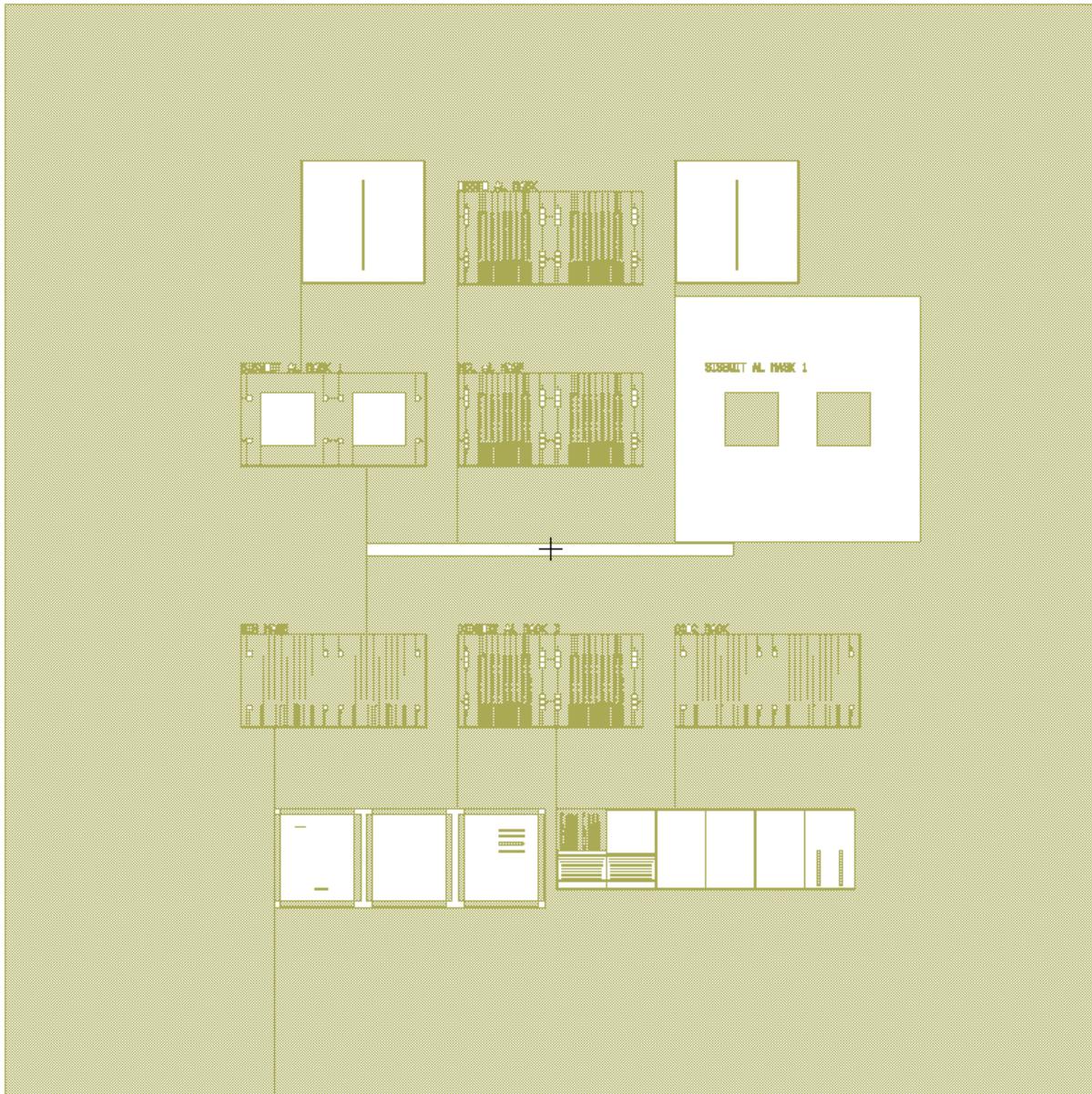
Fig. 4.3.1(c) shows the overall macro-level layout of our 7” photolithography mask. Because we are using 3.5 cm square samples, the 7” mask contains all the mask designs needed for each photolithographic step of our device fabrication process. To define a particular lithography design, we simply align the sample below the required window with the correct design and expose.

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<sup>1</sup> [http://www.evgroup.com/en/products/lithography/mask\\_aligners/evg620semiauto/](http://www.evgroup.com/en/products/lithography/mask_aligners/evg620semiauto/)



**Fig. 4.3.1(b)** Schematic 2D top down views of the “Accessory Devices” used for fabrication process characterisations. Different layers of each device are defined via a corresponding step in Fig. 4.3(a) and are labelled in the key.



**Fig. 4.3.1(c)** The 7" photolithography mask design used for our fabrication process. It's segmented into a number of distinct 3.5x3.5 cm areas (the approximate size of our samples used for each batch of device fabrication) which contain lithographical masks for each fabrication process step requiring photolithography.

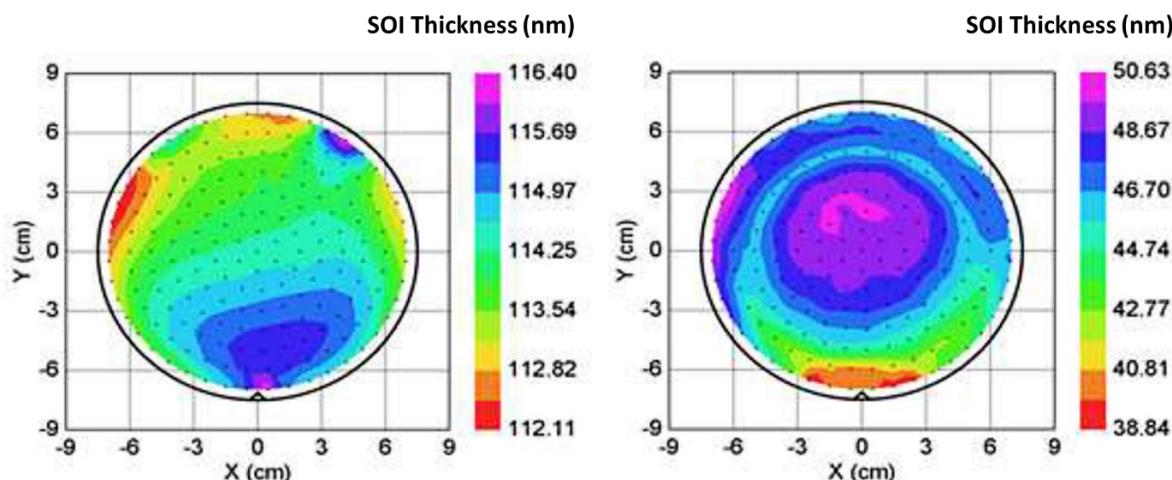
#### 4.3.2 *Sample Preparation and SOI Thinning*

Our SOI wafers are brought commercially (from Soitec®) cut along the  $<100>$  crystal plane with a 100 nm thick top Silicon layer on a 200 nm buried  $\text{SiO}_2$  layer (BOX) over a 0.5 mm thick silicon substrate. In order to reach the specifications needed so that our devices can be made to support single electron operations, the top SOI thickness needs to be first thinned to 50 nm or less. This can be done via various different approaches however we decided on thermal oxidation as it is a contaminant free process which doesn't damage the wafer surface or change the SOI to  $\text{SiO}_2$  interface. Thermal oxidation can be via either a wet or a dry

process depending on if the oxidizing ambient includes steam water vapour (wet) or O<sub>2</sub> gas. The process in which silicon undergoes at high temperatures (approx.  $\geq 800$  °C) is:



After oxidation, the grown SiO<sub>2</sub> layer can then be removed via wet etching in a mixture of ammonium fluoride buffered hydrofluoric acid (BHF) to leave a thinned SOI of the desired thickness. In our process, we decided on a commercially available 20:1 mixture of BHF to give a controlled SiO<sub>2</sub> etch rate of  $\sim 0.5$  nm/s. This allows for accuracy over not only removal of unwanted SiO<sub>2</sub> after SOI thinning but also gives us sufficient control such that the BOX of the SOI is not etched too significantly that it would affect device performance.

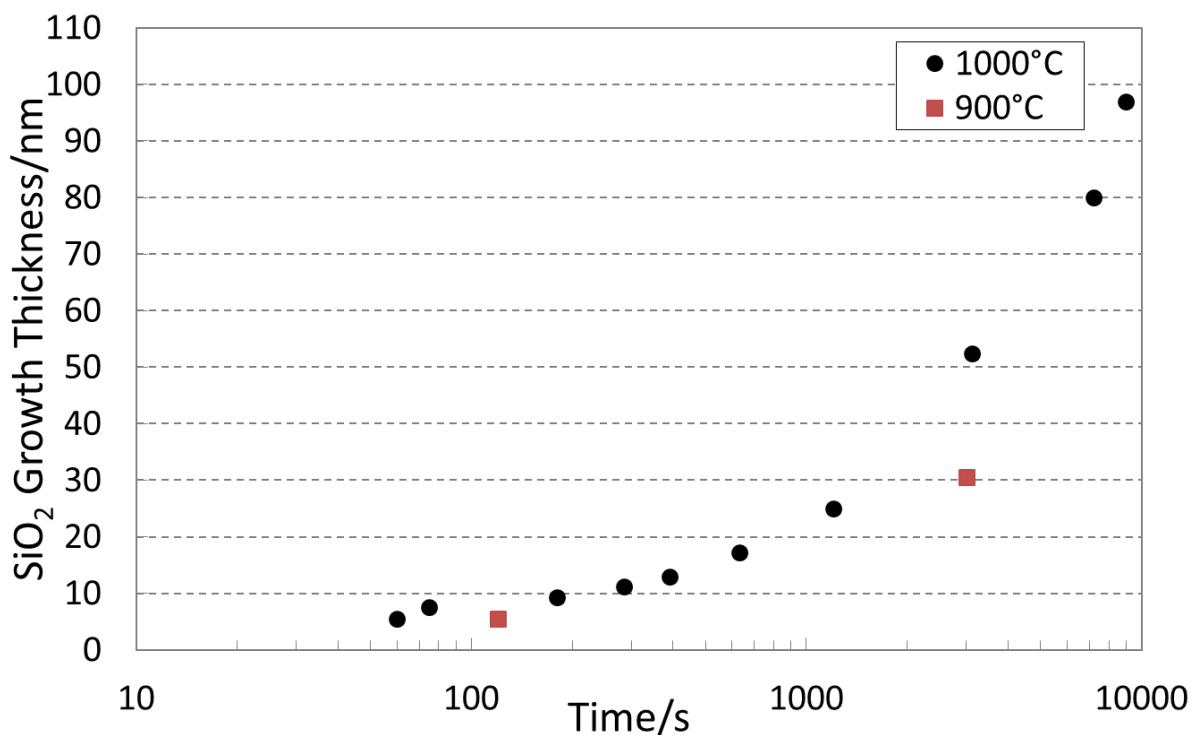


**Fig. 4.3.2(a)** Ellipsometry measurement of the top silicon layer's thickness profile across an SOI wafer before (left) and after (right) thinning via wet thermal oxidation at 1000 °C and BHF removal of the grown SiO<sub>2</sub>. Measurement measured across 133 points distributed across the wafer with a mean squared error of 4.31 nm.

One of the main advantages of using wet oxidation is that it is a much faster process for oxidizing silicon compared to dry oxidation. With our Tempress® horizontal ambient oxidation furnace system, a simple 50 min oxidation run resulted in 53 nm of SiO<sub>2</sub> grown from Si via dry oxidation compared to 165 nm grown via wet oxidation at 1000 °C. Given that the time required to grow SiO<sub>2</sub> from Si increases more than exponentially with thickness (see Fig. 4.3.2(b)), it is therefore much more time efficient to implement wet oxidation when aiming to achieve bulk SiO<sub>2</sub> growth.

However, although achieving a practical and minimal fabrication turnover time is a key objective of this work, implementing wet oxidation does have drawbacks. One of the key weaknesses of wet oxidation is the inability to precisely control the rate of oxidation across

the face of a 6" SOI wafer. Given the much faster vapour based reaction, slight discrepancies in vapour pressure due to convection across the wafer surface will result in very different oxidation rates. This reduces the thickness uniformity of the  $\text{SiO}_2$  grown and in turn, the uniformity of the SOI we are trying to thin. Fig. 4.3.2(a) shows an example of ellipsometry measurements of the thickness profile of the top Si layer of a SOI wafer before and after thinning via a wet oxidation process at 1000 °C (followed by BHF removal of the grown  $\text{SiO}_2$  layer). As can be seen, the process nearly tripled the difference in SOI thickness across the wafer from just  $\sim 4$  nm to nearly 12 nm. This would severely limit the repeatability of our fabrication process and affect our aims of a uniform SOI thickness of 50 nm for QD operations. Dry oxidation was therefore preferred over wet oxidation because it produced thickness profiles that had discrepancies of  $< 2$  nm before and after SOI thinning with an oxidation time that was only 2 hrs and 30 min in total.



**Fig. 4.3.2(b)** Table of data for our dry thermal oxidation process near our target thickness

Fig. 4.3.2(b) shows a graph of our oxidation calibration curve for SOI at 1000 °C and 950 °C for the gas flows setup we used. A temperature of 1000 °C was chosen for the actual thinning because it thinned the SOI to the required thickness in a practical amount of time whilst not straying too far from 950 °C which produces the best quality thermal  $\text{SiO}_2$ . Overall, the process was fully optimised to focus on precise control of the thermally grown oxide thickness, reproducibility across multiple runs, increasing the uniformity of SOI wafer profile

and minimizing SOI surface roughness. This was achieved after extensive testing and characterization including optimisation of the heating profile of the furnace system which uses two heating steps - the first to ramp the temperature rapidly followed by a second heating stage with a slow temperature ramp to the target oxidation temperature to reduce shock to the wafer and ensure temperature stability. Other optimisation parameters included process gas flows, process partial pressure, boat insertion speeds and N<sub>2</sub> gas flow during boat insertion.

Table 4.3.2(c) shows how much the SOI is thinned by for a given SiO<sub>2</sub> growth thickness. This gives the following approximate relationship (near the approximate thickness of thinning we want to achieve) between SiO<sub>2</sub> growth thickness, *t*, and the amount the SOI is thinned, *d*, by:

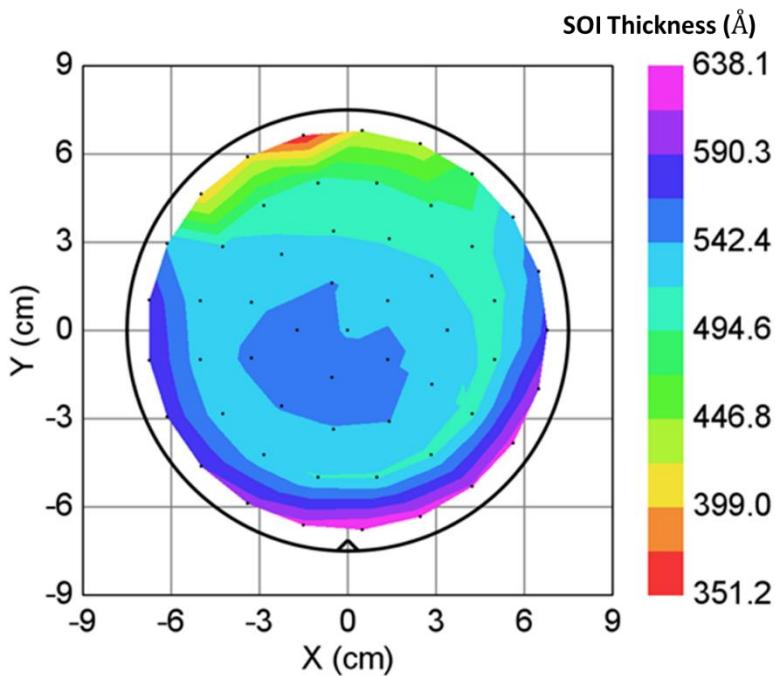
$$d = 0.46t$$

It was found that 70-80 nm of thermal oxide growth thinned SOI by ~37 nm. Therefore, the SOI was oxidized for 2 hrs 30 min to be thinned to 50-55 nm. Fig. 4.3.2(d) shows an ellipsometry measurement of the thickness uniformity of a particular SOI wafer after the dry oxidation SOI thinning process and 20:1 BHF wet etch removal of the grown SiO<sub>2</sub>. A variation of only 5 nm (the same as that originally before thinning) over the majority of the wafer area should be sufficient to ensure repeatability and not affect device performance too much.

Atmosphere	Temperature (°C)	Time	SiO <sub>2</sub> Thickness (nm)	SiO <sub>2</sub> Thickness Range (nm)	SOI Thinned by (nm)
Gas: O <sub>2</sub> Flow Rate: 5 slm	1000	20m	22	21-22	11
	1000	2hrs	80	79-81	37
	1000	2hr30min	97	96-98	45

**Table 4.3.2(c)** Table of data for our dry thermal oxidation process near our target thickness. The O<sub>2</sub> gas flow rate is in units of standard litres per minute (slm).

In addition, a variation of less than 5 nm across a 6" wafer means we can practically thin down to SOI thicknesses of only 10 nm or below. This enables an alternative approach to QD device fabrication via direct milling with a helium-ion microscope and could produce even smaller, sub 10nm DQD structures compared to that achievable via e-beam lithography. Currently, He-ion milling can “etch” 8 nm into silicon. With a milling resolution of down to 3 nm, this has the potential to realise room temperature DQDs. A more detailed discussion into this topic can be found in section 6.2.3.



**Fig. 4.3.2(d)** Ellipsometry measurement of the thickness profile across an SOI wafer after thinning via dry thermal oxidation at 1000 °C. Measurement measured across 54 points distributed across the wafer with a mean squared error of 4.22 nm.

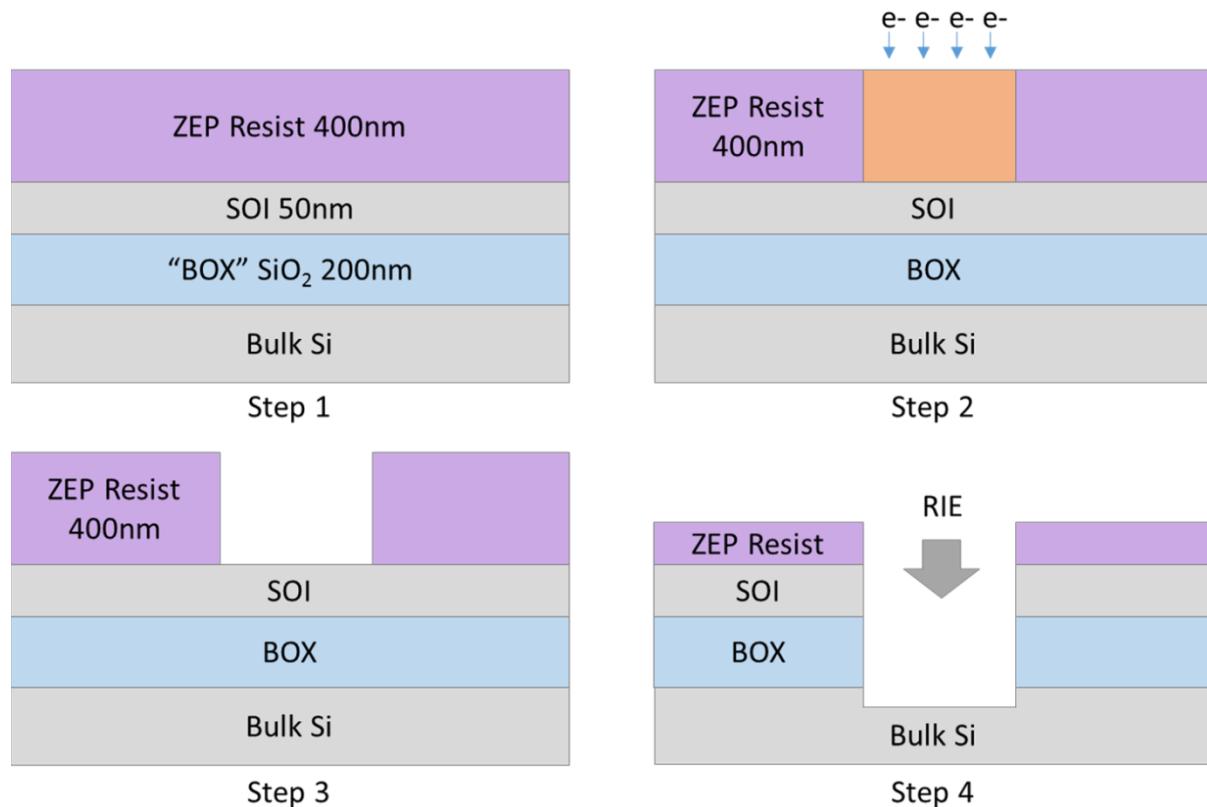
### 4.3.3 Interlayer Alignment Marks

One of the most crucial components of the device fabrication process is the ability to define precise alignment marks in a contaminant free way since so many lithography steps in the fabrication process rely on these marks for accurate alignment. Nano and micron scale alignment marks are required for accurate e-beam and optical alignment of all 5 lithography steps. To eliminate unwanted displacement between different alignment marks, all alignment marks are defined in one step. Therefore, e-beam lithography must be utilised to write all alignment marks in one go, including the sub 1  $\mu\text{m}$  e-beam alignment marks as shown in 4.3.1(a). This is because photolithography techniques are limited by the wavelength of the light source used for exposure which effectively translates to a lithography resolution down to only  $\sim 1 \mu\text{m}$  (insufficient for our needs). EBL on the other hand is capable of resolutions down to 4 nm sized spots depending on the manufacturer and has thus become a widely used tool for fabrication of solid state QDs.

For use with e-beam lithography, metal alignment marks are commonly used as this gives a high signal to noise contrast compared to silicon during e-beam reflection. However, as our devices need to be defined in clean intrinsic silicon and later processing steps require high temperature environments, potential metal ions on the surface of our SOI can dope/contaminate the material to produce unwanted effects on single electron spin operations

(e.g. nuclear spin of dopants can reduce relaxation times for single electron spins). Therefore, a different approach is needed to make alignment marks.

The use of etched alignment marks provides an effective alternative. The advantage here is its smaller line edge roughness compared to metal marks, which are often defined via a lift off process. This should mean greater accuracy in the e-beam alignment of our device structures. Since SOI has silicon and  $\text{SiO}_2$ , RIE with two different gas chemistries are needed for a high selective anisotropic etch. A key challenge is ensuring good material contrast so the marks can be detected by the e-beam system. This means alignment marks need to be etched through the BOX layer and into the Si substrate. Therefore, a way of realising this pattern is via firstly using e-beam to define the pattern in positive resist on SOI and then to transfer this pattern via reactive ion etching to the SOI substrate (see Fig. 4.3.3(a)). A core advantage here is the transfer from resist to substrate is a process that can be performed in parallel across a scalable number of devices.



**Fig. 4.3.3(a)** Schematic step by step process flow diagram for the definition of etched alignment marks. Step 1 is to cover the SOI substrate with ZEP® resist. Step 2 is to expose the alignment marks pattern onto the ZEP® resist. Step 3 is the removal of exposed resist via use of a developer (ZED-N50) and step 4 is to transfer this pattern into the SOI substrate via reactive ion etching (RIE).

There are currently only a limited number of electron sensitive resist with resolutions high enough to support few nm level e-beam lithography. The commonly used resist include

PMMA, MMA (and their bilayer varieties), ZEP520, UVN30 and the more recently developed HSQ (the latter two being negative type e-beam resists).

Through comparing these different resist types and extensive experimentation, we decided on “ZEP520” (manufactured by ZEONREX electronic chemicals) which is a high resolution electron sensitive positive resist to define our alignment mark designs. We chose ZEP520 not only because of its high resolution<sup>2</sup> at a thickness of 400nm but also because of its hardness after baking and high etching resistance against reactive ion etch gases used to etch silicon and SiO<sub>2</sub>. The alternative positive resist to this includes MMA/PMMA resist types but these are found to be much softer after post lithography baking and prone to deformation during RIE processes. Following the manufacturer’s guidance, the resist is first spun on the clean SOI sample at 3370 rpm and hard baked at 180°C for 3 min to give a ~400 nm thick layer.

To expose the resist and define our alignment mark pattern, an e-beam lithography exposure is needed which works by irradiating the resist with an electron beam to transfer energy to the intended areas (very similar to photolithography except in that case photons are performing the energy transfer). This causes chemical changes in the exposed resist area which then affects the solubility of the exposed resist compared to the un-exposed resist area in an optimised chemical solution (for ZEP520 this “developer” is the commercially available ZED-N50® solution). The amount of e-beam irradiation (referred to as the exposure electron dose with units  $\mu\text{Ccm}^{-2}$ ) is thus a key parameter which gives us control over the dimensions and repeatability of our process for defining patterns.

With our JEOL JBX 9300FS electron beam direct write lithography system, we undertook extensive beam and dose optimisation to conclude with an optimal base dose of 450  $\mu\text{Ccm}^{-2}$  and a beam spot size of 25 nm. Through adjustment of various e-beam parameters including beam accelerating voltage, aperture and current, this optimisation was focused not only to give sufficient precision in alignment mark definition, but also to minimise the time taken to expose each chip. This is critically important if the process is to be scaled up or down in the future without drastically affecting the exposure time. With our setup, only 5 minutes is needed to expose the alignment marks for the chip shown in Fig. 4.3.1(a).

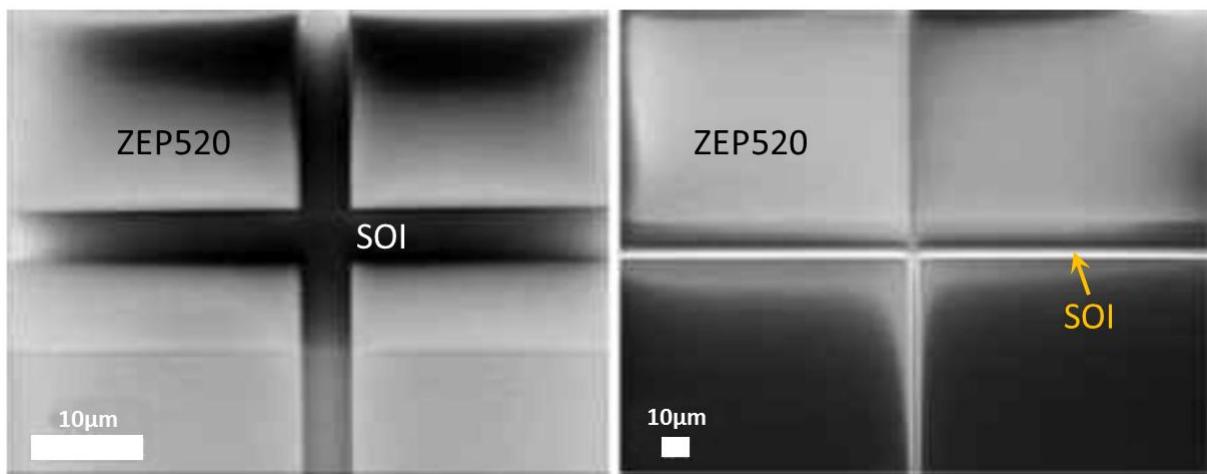
A further challenge with e-beam lithography is the problem of electron backscattering from the sample substrate due to the high electron energies used in the lithography process. This in turn results in scattered exposure of areas of the resist we don’t want to expose which is in proximity to the required pattern. To reduce this proximity effect, proximity error correction

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<sup>2</sup> [http://www.nanolithography.gatech.edu/ZEP520\\_literature\\_3.pdf](http://www.nanolithography.gatech.edu/ZEP520_literature_3.pdf)

was employed to firstly fracture the alignment mark design into smaller areas and then assign different constant dose levels to these fractured areas based on a Gaussian approximation of electron backscattering effects (the base dose mentioned previously is that with which the e-beam system takes as reference for proximity error correction). For a given area of a pattern therefore, one would expect the dose to be reduced at the centre and higher at the edges (see section 4.3.5 below for a more extensive discussion). This can therefore effectively reduce the proximity effect and limit electron exposure only to those areas we want to expose.

After exposure, the resist is then developed in ZED-N50 developer for 2 min and IPA for 1 min. Fig. 4.3.3(b) shows a SEM image of the global and local alignment e-beam marks (see Fig. 4.3.1(a)) after e-beam exposure and development of ZEP520 resist.



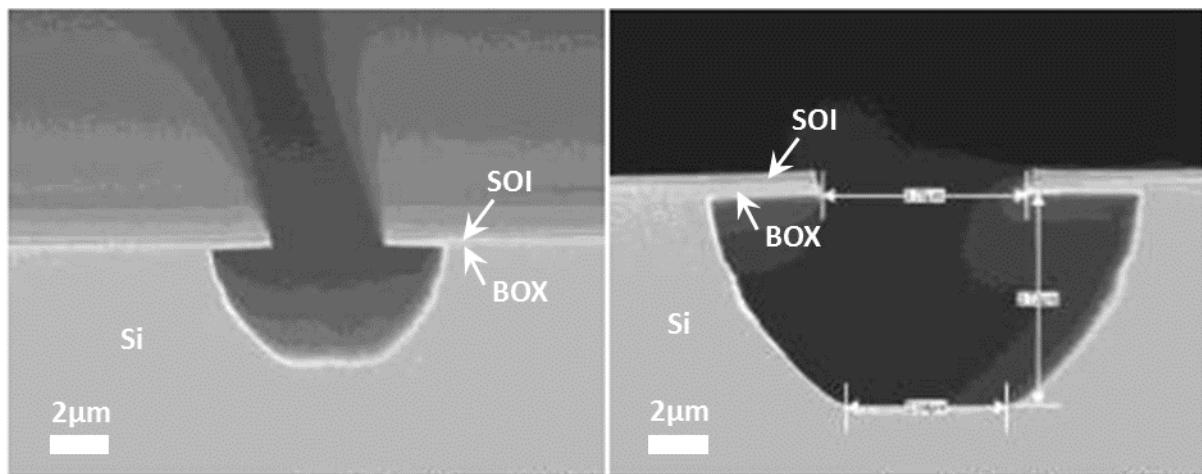
**Fig. 4.3.3(b)** Global (Left) and local (Right) e-beam alignment marks (as defined previously in Fig. 4.3.1(a)) patterned on ZEP520 resist with an e-beam dose of 450  $\mu\text{Ccm}^{-2}$ .

To transfer the alignment mark pattern into the SOI, two reactive ion etching processes needed to be developed which must not only deep etch ( $\sim 700\text{nm}$ ) through the Si and  $\text{SiO}_2$  layers of the SOI but also minimize the etching of the thin 400nm ZEP520 resist in addition to ensuring vertical side walls on the etched alignment marks. This was a key challenge in the alignment mark definition process. The system we used to develop this process was the Oxford Instruments RIE 80+.

To ensure a high etching selectivity of Si and  $\text{SiO}_2$  against ZEP520 resist, we started firstly with the standard RIE gas flow mixture of  $\text{SF}_6/\text{O}_2$  and  $\text{CHF}_3/\text{Ar}$  to etch Si and  $\text{SiO}_2$ . In terms of the  $\text{SiO}_2$  dry etching process, because the BOX is only 200nm in thickness whereas our required etch depth is 700nm, this meant we could still etch relatively vertical alignment mark side walls even if the BOX layer was etched isotropically as long as the Si etch process was anisotropic. Focusing on process development in this way was an essential step which

allowed us to achieve our target etching depth because it allows us to focus on realising a high etch selectivity of  $\text{SiO}_2$  against ZEP520 resist. This was achieved by altering the standard  $\text{CHF}_3/\text{Ar}$  gas flow ratio from 3:1 to etching purely with  $\text{CHF}_3$ . The removal of Ar, a noble gas, from the process effectively removed the mechanical part of the etching process to leave only  $\text{CHF}_3$  which reacts with  $\text{SiO}_2$  to form a chemical etch. This dramatically improved the etching selectivity from  $\sim 1:1$  to  $4:1$  for  $\text{SiO}_2$  against ZEP520 resist. However, the result is also accompanied by a much slower, but necessary,  $\text{SiO}_2$  etch rate of 6.6nm/min (full process parameters are detailed in Table 4.3.3(d)).

In addition, because the etching is set to occur at a relatively low RF power of only 50W (again to limit any mechanical etching of the ZEP520 resist), this meant it was difficult to maintain a constant DC bias in the RIE chamber to maintain the 50W power. Instead of the standard quartz bottom electrode (which becomes more insulating at low RF power levels with time), this was replaced with a higher conductance graphite plate to maintain the low RF power and a sufficient DC bias. Changing the setup in this way was a pivotal step to furthering our process optimisation to produce a novel low power  $\text{SiO}_2$  etch process using a graphite base plate with pure  $\text{CHF}_3$  chemistry.



**Fig. 4.3.3(c)** SEM of a failed isotropic etch of a global e-beam alignment mark (as defined previously in Fig. 4.3.1(a)) into SOI.

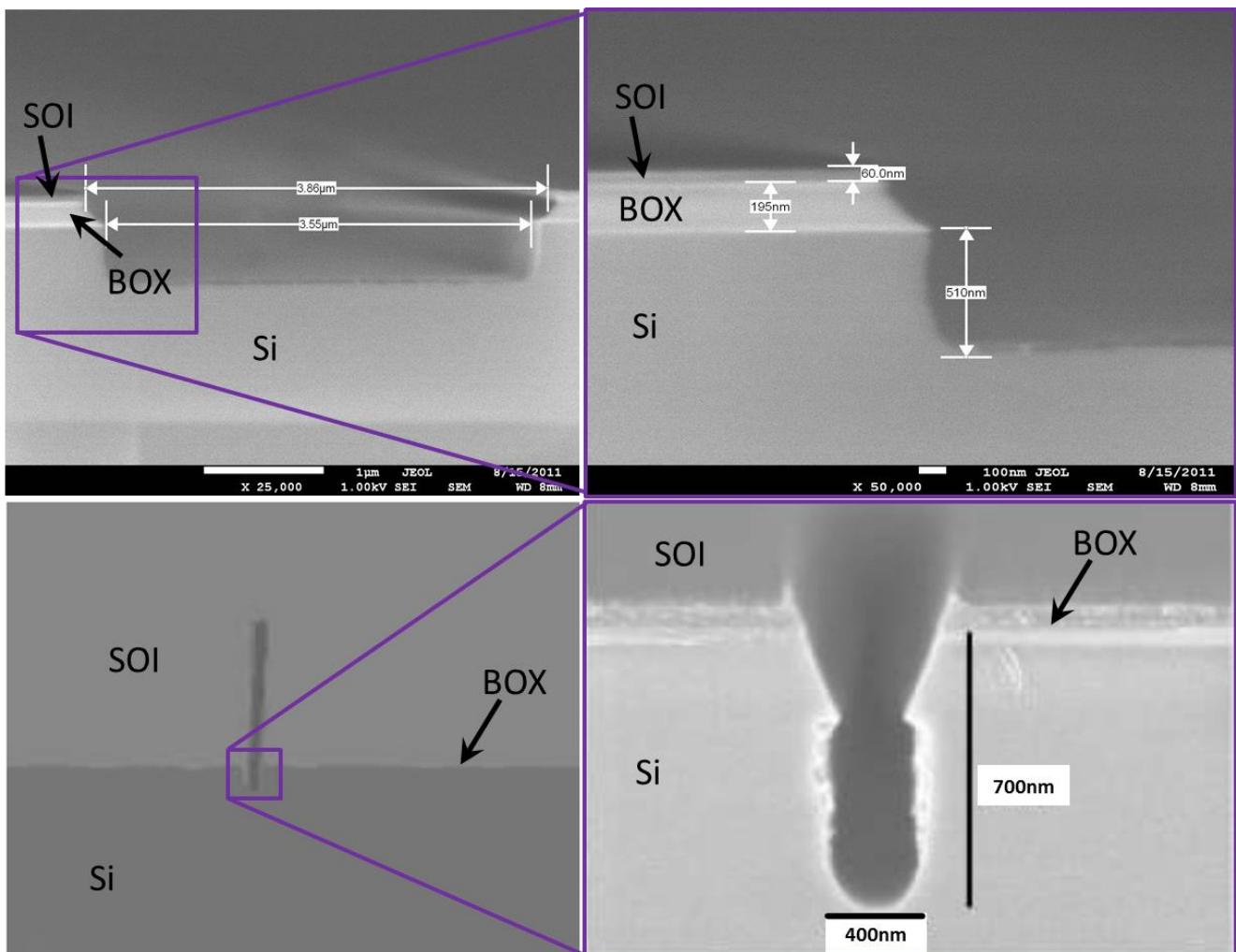
For the Si etching, we firstly decided to use a  $\text{SF}_6/\text{O}_2$  gas flow ratio of 5:1 with total gas pressure of 50mTorr and an RF power of 50W. The low RF power and  $\text{O}_2$  levels were chosen to provide the highest possible etching selectivity between Si and ZEP520 resist. This process resulted in a Si etch rate of 170nm/min with a Si:ZEP520 etching selectivity of 7:1 which was more than enough to ensure we could reach the target 700nm deep etch target. However, through detailed characterisation, it was found that the low RF and  $\text{O}_2$  levels resulted in an

etch that was too isotropic in nature (see SEM result in Fig. 4.3.3(c)) to be used repeatedly for e-beam lithography.

Through extensive RIE recipe optimisation and calibration, the conditions given in Table 4.3.3(d) were seen to give the best etching results. This sacrificed the high etching selectivity we achieved before but in return enabled an anisotropic Si etch with near vertical side walls which had acceptable etching selectivity relative to ZEP520. In combination, the Si and SiO<sub>2</sub> etching recipes for alignment mark definition is sufficient to produce an etch of > 700nm. The complete process of etching SOI, BOX and the Si substrate only consumes around 220nm of ZEP520 resist to produce alignment marks of around 700nm deep. SEM images of the deep etched alignment marks (After removal of the residual ZEP520 resist) are shown in Fig. 4.3.3(e). To remove any residual ZEP520 resist, the sample is plasma ashed with O<sub>2</sub> gas and then cleaned using fuming nitric acid and semiconductor industry standard RCA clean.

	Si Etch Recipe	SiO <sub>2</sub> Etch Recipe
<b>SF<sub>6</sub> Gas Flow Rate (sccm)</b>	18	0
<b>O<sub>2</sub> Gas Flow Rate (sccm)</b>	13.5	0
<b>CHF<sub>3</sub> Gas Flow Rate (sccm)</b>	0	12
<b>Ar Gas Flow Rate (sccm)</b>	0	0
<b>Coil RF Power (W)</b>	160	50
<b>Pressure (mTorr)</b>	30	30
<b>Strike Pressure (mTorr)</b>	0	0
<b>Table Type</b>	Quartz	Graphite
<b>Table Temperature (°C)</b>	20	20
<b>Etch Rate - (nm/s)</b>	3.13	0.11
<b>Etch selectivity to ZEP</b>	3:1	4:1

**Table 4.3.3(d)** Reactive Ion Etching plasma and chamber condition to etch and transfer the ZEP alignment mark pattern into SOI. The gas flow rate are in units standard cubic centimetres per minute (sccm).



**Fig. 4.3.3(e)** SEM of etched global (Top) and local (Bottom) e-beam alignment marks using the RIE recipe in Table 4.3.3(d).

To date, this process has produced many samples (over 60) with alignment marks without ever causing e-beam lithography alignment issues during latter device fabrication steps. The marks exhibit distinct contrast under an e-beam and are easily detectable by the automated e-beam alignment mark sensor system even at low signal to noise ratio. More importantly, because of the smaller line edge roughness produced by the dry etch process, results show that the etched marks are capable of producing alignment errors less than 10 nm across all devices on a chip. The total process time is also very practical given the scalable and parallel nature of the process, with only 33 min needed to etch the resist pattern into the SOI substrate.

#### 4.3.4 Spin-on-doping

To enable conductivity through the SOI, it needs to be selectively n-doped such that the centre of each device (where the nanostructure lies) is left intrinsic. Conventionally, ion implantation provides a precise method for selective doping, however, we propose the use of

a novel spin-on-dopant process which achieves the desired result whilst being more economical and offering a much faster turnaround time. This is mainly due to the scarcity of ion implantation facilities which, if used, will take around 3 weeks due to the queue of jobs present.

In order to selectively dope the SOI, we must first start by defining a doping “mask” which covers the centre of each device where we want to maintain the SOI’s intrinsic properties. The most widely used dopant masking material in the VLSI industry are  $\text{Si}_3\text{N}_4$  and  $\text{SiO}_2$  [47]. Both materials were explored but  $\text{SiO}_2$  was chosen for our purposes due to the ease in its deposition, etching and patterning as well as its effective properties in being an impurity diffusion barrier material.

A 100 nm thick  $\text{SiO}_2$  layer is deposited via plasma enhanced chemical vapour deposition (PECVD) on our SOI in three 33 nm thick layers. This multilayer structure is used to minimise pinhole formation between  $\text{SiO}_2$  layers, which is common for PECVD [46]. Pinholes are problematic because they allow parts of the intrinsic nanostructure region to be potentially doped. By depositing in three steps, the reactants are purged away from the sample surface between each deposition step so that subsequent depositions will cover any pinholes formed. Table 4.3.4(a) shows our conditions for the PECVD of  $\text{SiO}_2$ . The oxide deposits via a chemical reaction between  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  in the gas phase under RF power.

SiO <sub>2</sub> Deposition Recipe	
SiH <sub>4</sub> Gas Flow Rate (sccm)	12
N <sub>2</sub> Gas Flow Rate (sccm)	38
N <sub>2</sub> O Gas Flow Rate (sccm)	12
No. of Steps	3
Step Time (s)	36
RF Forward Power (W)	20
LF Forward Power (W)	0
Pressure (mTorr)	1000
Table Temperature (°C)	350
Deposition Rate - (nm/s)	0.926

**Table 4.3.4(a)** PECVD plasma and chamber condition to deposit 100 nm of  $\text{SiO}_2$  to be used as a doping diffusion mask.

After  $\text{SiO}_2$  deposition, photolithography is then used with AZ2070 negative photoresist to define a 3  $\mu\text{m}$  box at the centre of each device using our photolithography mask (see Fig. 4.3.1(c)). The resist is spun on the sample at 6000  $\text{rpm}$  and hard baked at 110°C for 1 min

to give a  $> 7 \mu\text{m}$  thick layer. This provides for a sufficiently thick sacrificial etching mask when transferring the pattern by RIE into SOI. After alignment using the alignment marks defined previously and a  $5.5 \text{ sec}$  exposure, the resist is baked at  $110^\circ\text{C}$  for  $1 \text{ min}$  and developed in AZ726MIF for  $90 \text{ secs}$ .

	<b>SiO<sub>2</sub> Etch Recipe</b>
<b>CHF<sub>3</sub> Gas Flow Rate (sccm)</b>	12
<b>Ar Gas Flow Rate (sccm)</b>	38
<b>Coil RF Power (W)</b>	200
<b>Pressure (mTorr)</b>	30
<b>Strike Pressure (mTorr)</b>	50
<b>Table Temperature (°C)</b>	20
<b>Etch Rate - (nm/s)</b>	0.41

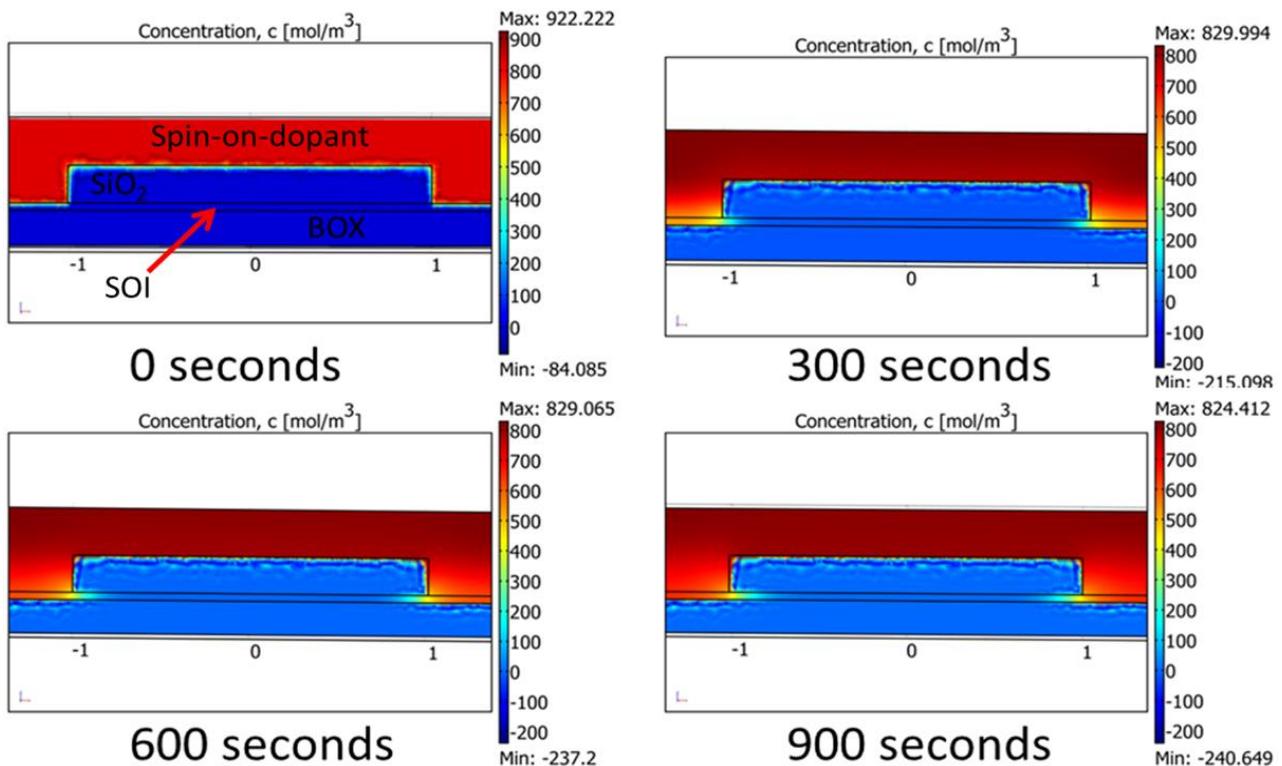
**Table 4.3.4(b)** RIE plasma and chamber condition to etch and transfer the AZ22070 doping mask pattern into SiO<sub>2</sub>.

RIE then transfers the doping mask pattern into the SiO<sub>2</sub> layer via the conditions shown in Table 4.3.4(b) which is optimised to give an anisotropic etch that produces vertical sidewalls. RIE is used rather than a wet etching process with hydrofluoric acid because it allows for an anisotropic etch which can more accurately retains the dimensions of the resist pattern. Wet etching tests revealed that removing the excess SiO<sub>2</sub> surrounding the doping masks would actually undercut the resist pattern and etch the SiO<sub>2</sub> directly below this up to a distance of  $20\mu\text{m}$ , which would significantly change the thickness of a  $3 \mu\text{m}$  wide SiO<sub>2</sub> doping box. However, a disadvantage of RIE is that the etch time must be controlled accurately. If the sample is etched longer than necessary, the boxes may be over etched and the pattern transferred into the SOI. This creates a problem for later lithography steps as any non-uniformity in the SOI will affect the uniformity of resist coating (especially important for the nanoscale device patterning using HSQ resist). Any excess AZ2070 resist is then removed with acetone and IPA along with a FNA and RCA clean before the doping process.

For doping, we use a commercially available  $3 \times 10^{20}$  phosphorosilicafilm<sup>3</sup> manufactured by emulsitone as the n-type phosphorus dopant source. This contains  $3 \times 10^{20}$  phosphorus dopants per cm<sup>3</sup> and is spun onto the sample at  $2000 \text{ rpm}$  and baked at  $110^\circ\text{C}$  to give a uniform dopant layer of around  $1 \mu\text{m}$  (determined by ellipsometry characteristics). This pre-drive in baking essentially hardens the resist by removing excess solvent content to provide a uniform distribution of dopants across the sample and ensure reproducibility across runs. With

<sup>3</sup> [http://www.emulsitone.com/psif5x10\\_20.html](http://www.emulsitone.com/psif5x10_20.html)

reference to the material's technical data sheet and taking into account our target doping depth and SOI thickness, we decided to thermally drive the dopants into the SOI for 15 min in a  $N_2$  atmosphere at 950 °C. What is crucial here is that we must not thermally drive dopants for too long or else this will dope too deep into the SOI and lead to significant electrical leakage through the BOX layer during device operations. COMSOL finite element based mass diffusion simulations were therefore utilised to ensure a controlled dopant drive in process. Via entering our SOI dimensions using empirical diffusion coefficient of phosphorus in both Si and  $SiO_2$  [48], simulations indicated that a 15 min drive in should dope the SOI to a concentration of  $\sim 10^{19}/cm^3$  without causing any significant doping in the  $SiO_2$  BOX layer. This would in turn mean that the SOI should offer enough conductance even at low temperatures for device operations without any potential leakage through the BOX layer. Fig. 4.3.4(c) shows our simulated result. A doping mask of 2  $\mu m$  was used here (instead of our fabricated 3  $\mu m$ ) and dopant diffusion of up to 200 nm under the doping mask is observed. It is expected that some doping will occur in the SOI under the doping mask due the diffusive nature of the process, however, 200 nm is much smaller than the size of our doping box (3  $\mu m$ ) and thus should not affect the desired intrinsic property of the fabricated QDs (which are only 50 nm in size and located in the centre of the intrinsic region).



**Fig. 4.3.4(c)** COMSOL finite element based simulation of phosphorus dopant diffusion/concentration in SOI at 950 °C after 0, 300, 600 and 900 seconds. The bar to the right indicates the phosphorus concentration in the structure in  $mol/m^3$ . The maximum of which is equivalent to a phosphorus concentration of  $\sim 3 \times 10^{20}/cm^3$ .

Therefore, dopant drive in was carried out at 950 °C for 15 min in a N<sub>2</sub> atmosphere. 4-point probe measurements indicated a sheet resistance on average of 17mΩ/■ which corresponded to a doping concentration of  $\sim 10^{19}/cm^3$  – verifying the simulation results and expectations. One of the main advantages of this novel spin-on-doping process is its ability to reduce the turnover time for the SOI doping process from an average of 3 weeks for conventional ion-implantation to just 15 minutes for dopant drive in. Altogether, the processing time from doping mask formation to dopant drive-in takes just a few hours and a major advantage here is the process is designed to be scalable without affecting fabrication time.

Finally, to remove the excess phosphorosilicafilm after annealing, the material datasheet recommended the use of a HF wet etch. We found after numerous trials that the excess phosphorosilicafilm can easily be removed along with the SiO<sub>2</sub> doping mask boxes in a BHF 20:1 mixture for 10 min to leave a selectively doped SOI substrate ready for device lithography.

#### 4.3.5 *SOI QD Device lithography and definition*

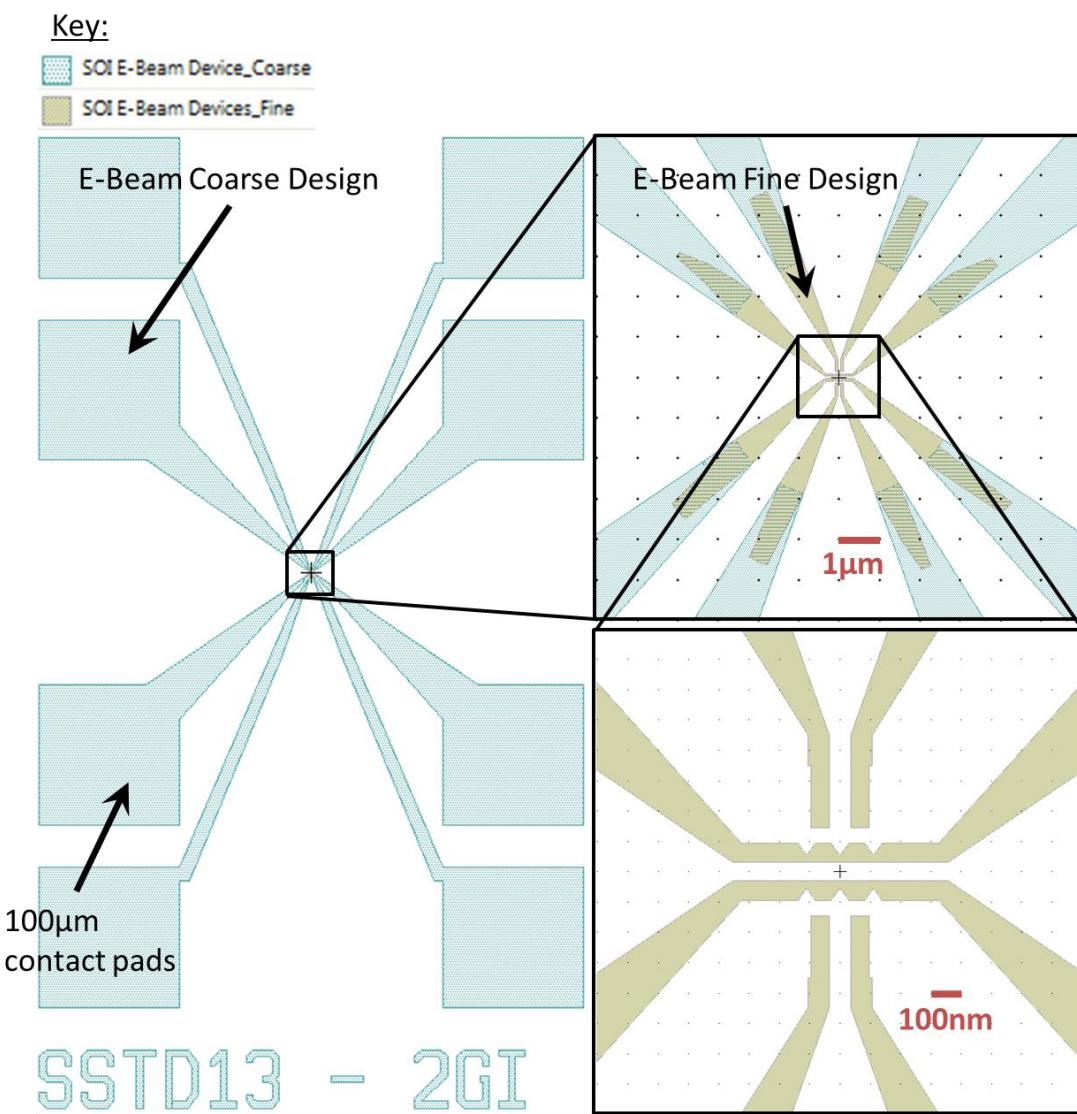
For precise nm-scale definition of our QD system, we again utilise an e-beam lithography process much like that used in section 4.3.3 for alignment marks. However, because we want to pattern the SOI to leave the QD device design (See Fig. 4.2.1(a)), a negative tone electron sensitive resist is used because in this case the total area under exposure will be smaller than if a positive tone resist is utilised. This is important because the e-beam system is a direct write lithography system where the resolution is dependent on the spot size and write time dependent on the time it takes for the beam spot to cover the entire area of the device pattern. This essentially means the write time will scale proportionately with the total area of the exposed pattern and is unlike photolithography where exposure of the resist is done in parallel via use of a photolithography mask.

The key challenge of keeping the e-beam lithography write time down to a minimum is not only because this is a key objective of this work but also because such e-beam systems are often costly to operate. Therefore, minimizing the exposure time is economically preferred.

Fig. 4.3.5(a) shows a schematic of our device design. This has the same dimensions and features as that simulated previously (Fig. 4.2.1(a)) in section 4.2. Again, one of the main advantages of this design is it offers the potential for greater yield in QD device fabrication since only one DQD transistor is operated as a turnstile where as the other as an electrometer. The electrometer does not require perfect formation of a double QD (DQD) for good

sensitivity as a charge detector; therefore, functionality can be interchanged between the two DQDs depending on fabrication results (increasing device yield).

Each of the devices will sit within a  $1 \times 1$  mm region enclosed by the e-beam local alignment marks (Fig. 4.3.1(a)) and is repeated across a chip to enable parallel fabrication of a scalable number of devices. One of the advantages of this approach is it easily enables the parallel fabrication of a large number of different QD systems. Only the designs in this step of the fabrication process need to be changed (the QD layout and contact pads designs) with the others the same to result in fabrication of a large array of devices with completely different layouts and functionalities.



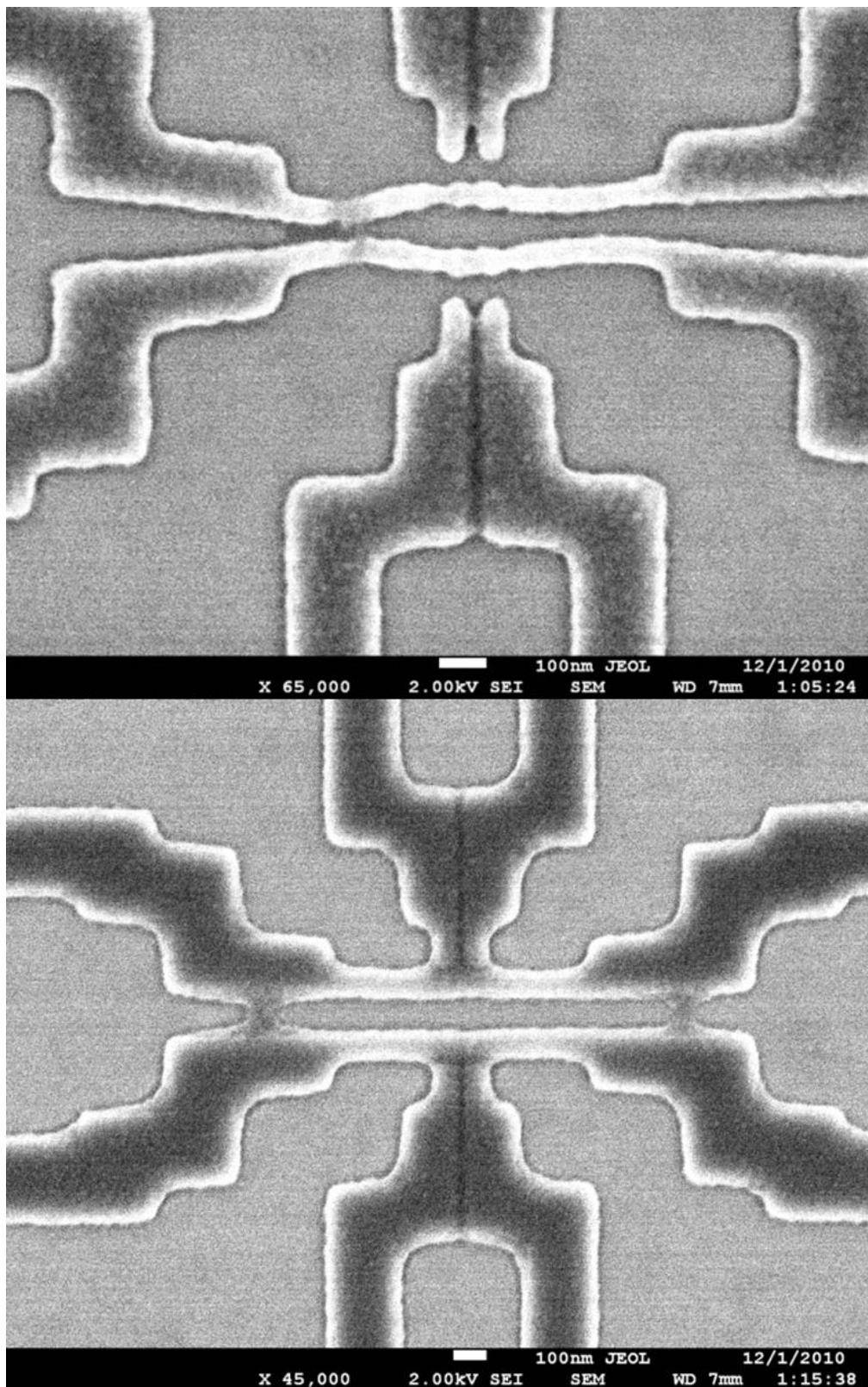
**Fig. 4.3.5(a)** 2 dimensional top down diagram of the SOI device design. The brown nanostructure region is exposed via a fine EBL beam condition whereas the larger cyan regions are exposed via a coarse EBL beam condition. There is an area of overlap between the coarse and fine designs to account for any beam drift and alignment error.

In order to define the 65 nm wide QDs and channels, a 4 nm e-beam spot size (the minimum possible) had to be used to achieve a high enough resolution to accurately define the QD and channel constriction shapes smoothly and with low line edge roughness. This is absolutely critical to ensure repeatable device performance and clear QD characteristics since a small bump due to rough lithography on a channel could mean the accidental formation of unintended QDs as seen previously in [39]. However, smaller spot sizes inevitably results in longer exposure times for a given pattern since the time it takes a 4 nm spot to write the whole design (Fig. 4.3.5(a)) including the 100×100 um large contact pads will be longer than that for e.g. a 25 nm e-beam spot. Trials shows that to write 72 devices on a chip using a single “fine” beam condition (with spot size 4 nm) would take at least 12 hours to complete. This severely limits the potential scalability of the fabrication approach and thus an alternative method was needed.

Since we only require precise definition for the QD and nearby nanoscale device components, we explored a novel method of using two different beam condition in the same exposure to minimize the e-beam exposure time. This however added to the complexity of the e-beam process since the exposure needed to be stopped half way through for manual calibration of a change in e-beam condition. This in turn affected the e-beam coordinates and thus the local alignment marks (4 near the corners of each device) defined previously were utilised. Performing the e-beam exposure in this way could therefore reduce the exposure time and also ensure accurate alignment between the nanoscale “fine” device patterns exposed with the “fine” beam condition and coarse bond pads and taper designs with the “coarse” beam condition (see Fig. 4.3.5(a)). An overlap was designed between the fine designs and coarse designs (as well as enough spacing between the tapers to ensure they didn’t overlap if misaligned) to ensure any e-beam misalignment was accounted for. After extensive refinement of the designed pattern and e-beam conditions, trials showed that with this new approach, e-beam exposure time could be reduced to just 5 hours needed to expose 144 devices (2 chips worth of devices) with less than 5 nm in alignment error observed reproducibly between the two exposure conditions. This also demonstrates the effectiveness and reliability of our process in section 4.3.3 for alignment mark definition in SOI.

In order to define the device patterns, the selectively doped SOI had to be first covered with e-beam sensitive resist. The two main types of negative tone e-beam sensitive resist are the commercially available UVN30 and hydrogen silsesquioxane (HSQ) resist with the former being the more economical choice. Extensive dose tests to realise our patterns using UVN30 were attempted. However, results showed the exposed resist patterns displayed significant

signs of merging at the critical dimensions of 50 nm and which varied significantly from the design (Fig. 4.3.5(b)).



**Fig. 4.3.5(b)** SEM of a UVN30 exposure of a preliminary device designs on Si at  $50\mu\text{C}/\text{cm}^2$  (top) and  $100\mu\text{C}/\text{cm}^2$  (bottom) The top SEM shows signs of pattern drift whereas the bottom shows severe resist merging between critical features.

HSQ resist was therefore chosen instead because of its capabilities in realising sub 10 nm [50] pattern definition and very small line edge roughness. This makes it particularly useful for precisely [49] patterning QDs whilst minimizing the possibility of forming unintentional QDs (unlike the work by [39] in which ZEP520 resist was used for device lithography). In addition, one of the key features of HSQ is that it becomes an  $\text{SiO}_2$  like material after curing which gives it a high etching resistance that is especially useful for direct transfer of the pattern into thin SOI. This offers a competitive advantage over positive resist alternatives such as poly methylmethacrylate (PMMA) where nanostructure fabrication requires an additional lift off process which often suffers from significant line edge roughness and is used widely for work on GaAs based QDs (Elzermann *et al* (2004)).

As mentioned previously in section 4.3.3, for exposure of large areas and especially where very fine nanoscale patterns are in close proximity of larger micron scale patterns, a high energy e-beam will result in significant electron backscattering from the SOI substrate to expose unintended areas. To maintain the same e-beam exposure dose across the whole device design whilst minimizing unintended electron proximity exposure, proximity error correction (PEC) was employed to ensure the same Gaussian distribution of doses is experienced around each point of the exposed pattern. Firstly the device design is fractured into smaller areas and then assigned different constant dose levels to these fractured areas based on a Gaussian approximation of electron backscattering effects. For a given large area of a pattern therefore, one would expect the dose to be relatively uniform and reduced at the centre and much higher at the edges with a more complex distribution. This can therefore effectively avoid overexposure in any part of the design, reducing proximity effect exposures and limit electron exposure only to those areas we want to expose. Fig. 4.3.5(c) shows an example of a design similar to that in Fig. 4.3.5(a) which has been fractured and assigned different e-beam doses intensities based on results from proximity error correction calculations. After PEC, the calculated design and dose distribution information is directly input into the e-beam system for exposure.

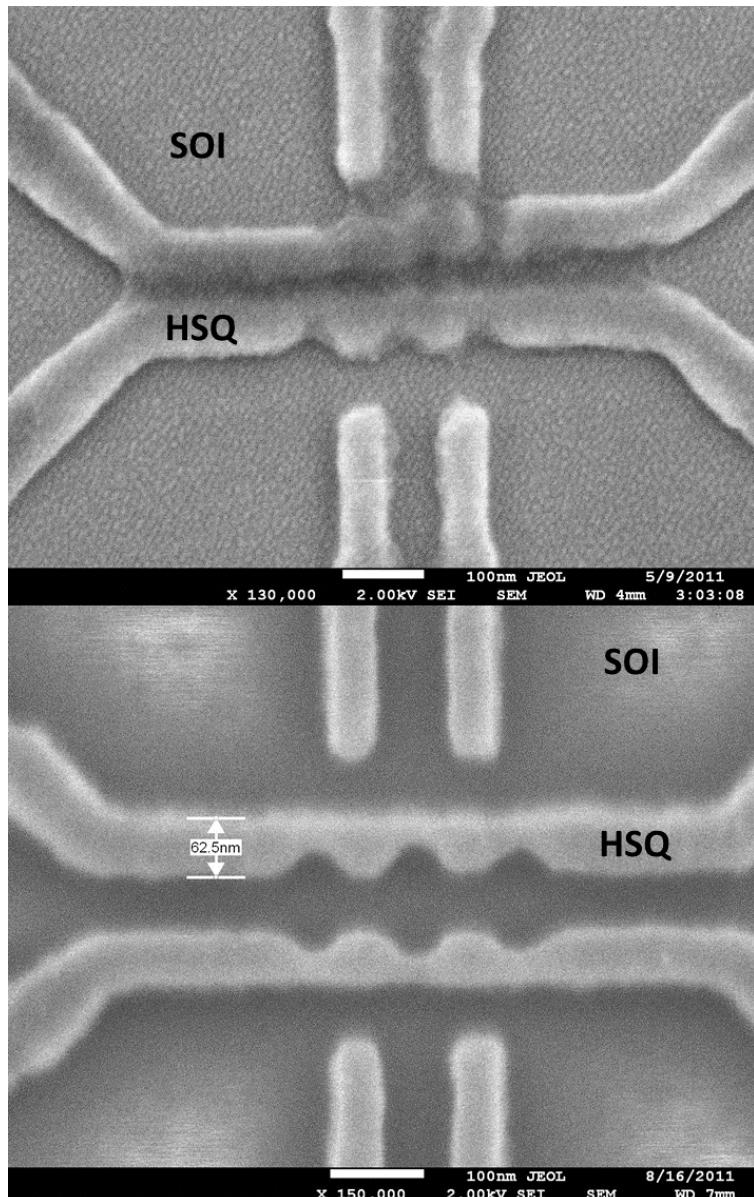


**Fig. 4.3.5(c)** An example of a device layout after proximity error correction (PEC) simulations. Each block of colour corresponds to a specific exposure intensity calculated depending on the proximity effects of exposures around it.

Fig. 4.3.5(d) below shows an example of an e-beam exposure of our device design in HSQ after resist development with the same e-beam conditions with and without proximity error correction. It can be clearly seen that the effects of electron backscattering is prominent here causing significant resist merging without the use of proximity error correction. The DQDs at the top of Fig. 4.3.5(d) are in the reverse direction to that in the bottom image as both designs were attempted, however the top design was chosen because it gave the best exposure repeatability and largest useable dose range.

To prepare our chip for exposure, the SOI is first dehydrated for 30 min at 210 °C. HSQ is then spun on the sample at 5000 rpm and baked at 80 °C for 4 min to become ready for exposure. This creates around a 50 nm thick HSQ resist layer, which through trials and extensive e-beam dose testing, has been found to give the required repeatable device dimensions with sufficient lithography resolution as well as being thick enough to allow for RIE transfer of the device pattern in to the SOI.

EBL dose tests of HSQ spun on SOI substrates revealed that doses of 625  $\mu\text{C}/\text{cm}^2$  and 1250  $\mu\text{C}/\text{cm}^2$  gave the best realisation of the coarse and fine device patterns on HSQ. In general, doses within the range 600 to 700  $\mu\text{C}/\text{cm}^2$  for coarse patterns (1200  $\mu\text{C}/\text{cm}^2$  to 1400  $\mu\text{C}/\text{cm}^2$  for fine patterns) gave repeatable patterns with very good definition which closely matched the design in Fig. 4.3.5(a). The exposed device patterns closely match the design in Fig. 4.3.5(a) with a dimensional variation of <10 nm. For doses higher than 1400  $\mu\text{C}/\text{cm}^2$ , the effects from back scattering of electrons becomes a problem even with PEC and caused severe merging of the resist pattern after development between nanoscale device structures. Dose tests on both bulk Si and SOI were done, with noticeable differences when changing substrates (SOI exposures require slightly higher dose).



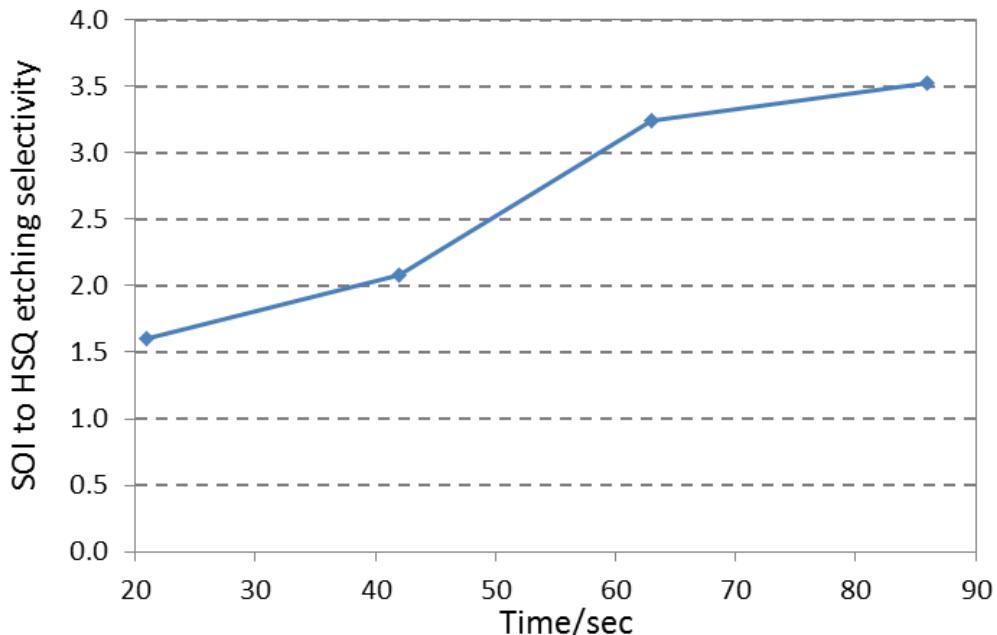
**Fig. 4.3.5(d)** SEM image of an e-beam exposure on HSQ of the nanostructure of our device design on SOI at  $1250\mu C/cm^2$  without proximity error correction (PEC). The grainy texture visible in the SEM is due to the sample being coated by 1 nm of gold to provide greater imaging contrast under the SEM. Bottom: SEM image of a successful e-beam exposure on HSQ of the nanostructure of our device designs with PEC. The top and bottom designs have the QDs inverted in orientation.

After exposure, the sample is developed in commercially available Microposit® MF319 developer for 100 secs, and then hard baked at 250 °C for 4 min 30 secs to become a SiO<sub>2</sub> like layer. This can then be used as an etching mask during a RIE process with an Oxford Instruments RIE80+ system to transfer the resist based device pattern into SOI. Table 4.3.5(e) shows the RIE conditions and Fig. 4.3.5(f) shows a plot of the etching rate. Ellipsometry and profilometer measurements were used throughout the etching process to accurately determine the etch depth and the thickness of material remaining for a given time. From Fig. 4.3.5(f) we

can clearly see that the SOI to HSQ etch selectivity is always above 1 which ensures that we can fully transfer the device pattern into the SOI without any risk of the HSQ running out.

	Si Etch Recipe
SF <sub>6</sub> Gas Flow Rate (sccm)	36
O <sub>2</sub> Gas Flow Rate (sccm)	36
Coil RF Power (W)	100
Pressure (mTorr)	30
Strike Pressure (mTorr)	50
Table Temperature (°C)	20
Etch Rate - (nm/s)	1.34

**Table 4.3.5(e)** RIE plasma and chamber condition to etch and transfer the HSQ device pattern into SOI.

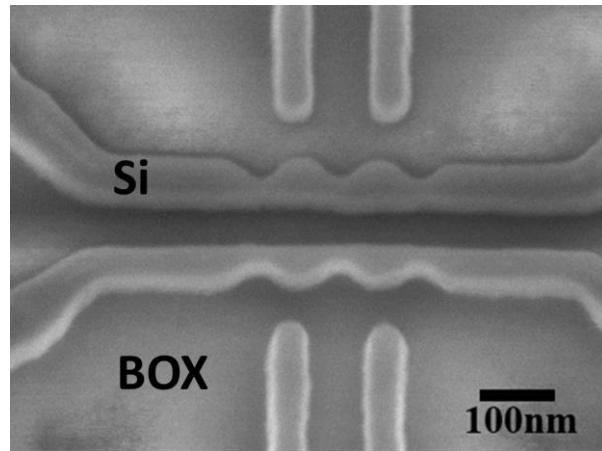


**Fig. 4.3.5(f)** RIE etching rate of SOI to HSQ as a function of the total etching time. As can be seen, this is not constant and varies significantly with time.

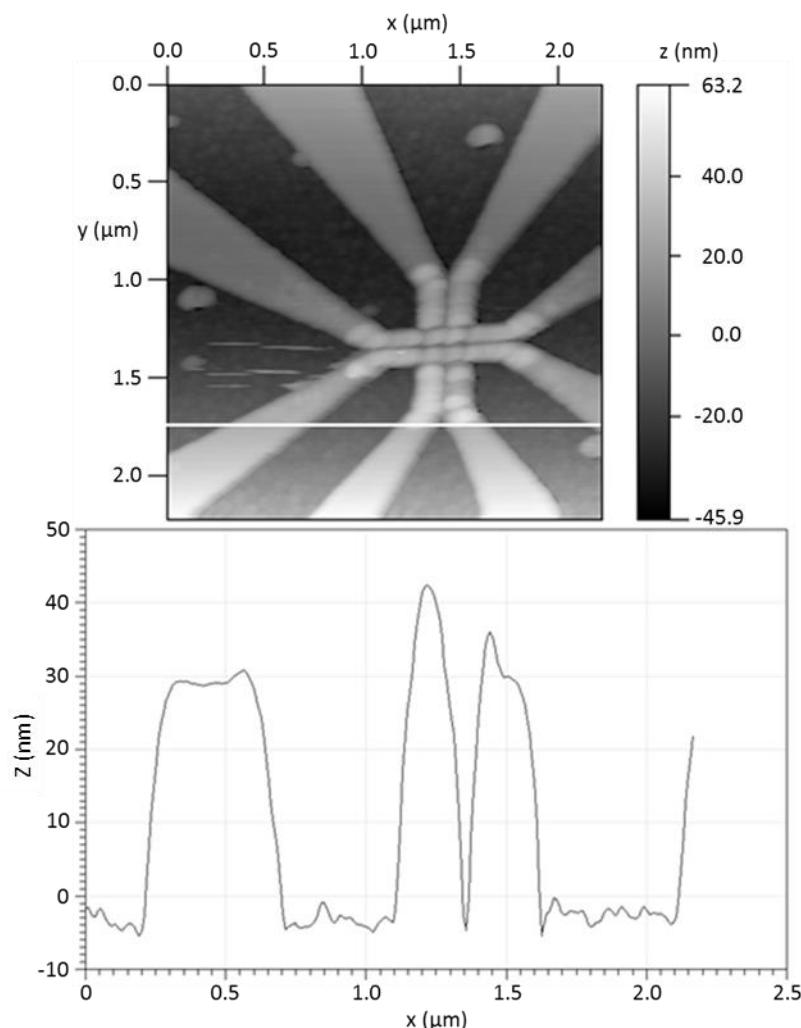
After RIE, the HSQ is removed in a BHF 20:1 mixture at a rate of ~1 nm/sec. Given the etching rate and selectivity however, this means the time to remove any left over HSQ in BHF 20:1 is around 20 seconds and must be controlled precisely. Prolonged etching could remove a significant proportion of the 200 nm buried oxide (BOX) layer of our SOI and potentially suspend the SOI QDs structures.

Fig. 4.3.5(g) shows a tilted SEM of a device etched into SOI after HSQ removal via BHF. The etched nanostructures are observed to have clearly defined vertical sidewalls with <1% dimensional deviation from the resist pattern. Fig. 4.3.5(h) shows a tapping mode atomic

force microscopy (AFM) scan of the nanostructure with Al-G tips where we obtain sub-nm accuracy in determining the etching depth. The profile across the white line on Fig. 4.3.5(h) shows that the side walls of the nanostructure are  $> 80^\circ$  (here approximately a 30nm thick SOI sample was used) - sufficient for defining our QD system.



**Fig. 4.3.5(g)** 20° Tilted SEM of the nanostructure of our device nanostructure etched into SOI.



**Fig. 4.3.5(h)** Top: AFM image of etched devices in SOI. The scan area focuses on the nano-scale pattern. Bottom: A plot of the variation of height across the white line drawn on the AFM image (Top). A clear step of  $\sim 30\text{nm}$  is seen.

#### 4.3.6 SOI Device Oxidation

Following a pattern transfer into SOI, the SOI based devices are then oxidised for 10 min 30 secs to form a  $\sim$ 17 nm  $SiO_2$  layer around the device structure, helping to reduce charge traps caused by any surface imperfections. We decided for this to be thicker than that originally simulated in section 4.2 because smaller QDs will offer more distinct and better single electron control. This has the added benefit of reducing our QDs from 65 nm to  $\sim$ 48 nm and constrictions from 25 nm to just 7-10 nm. The thermal oxidation condition is the same as that used in section 4.3.2 for SOI thinning (see Fig. 4.3.2(b)).

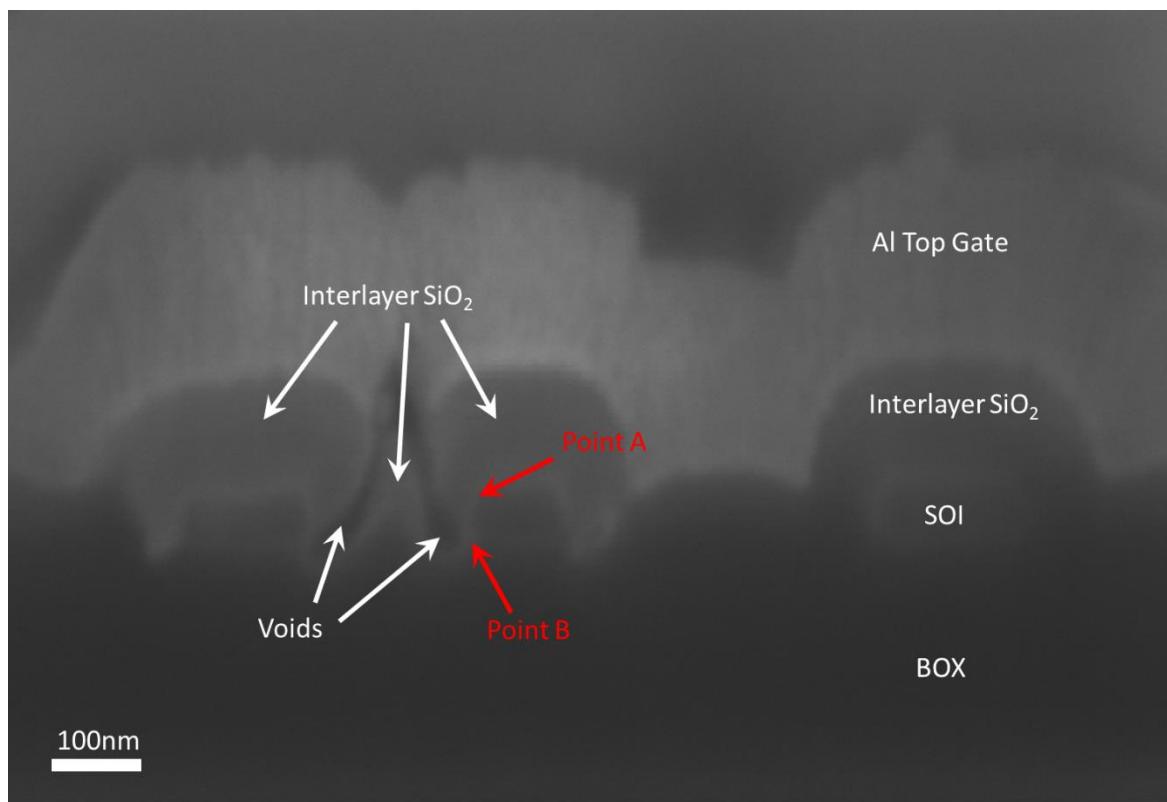
One of the concerns during this process is that because of the high temperature (1000 °C) used for oxidation, phosphorus dopants previously driven into the SOI might diffuse extensively into the intrinsic Si QDs channel. However, simulations from section 4.3.4 showed that even after a 15 min anneal, phosphorus dopants could only diffuse 200 nm into the intrinsic region. Therefore a 10 min 30 sec oxidation of the SOI should not cause significant dopant diffusion into the intrinsic region.

#### 4.3.7 Interlayer Oxide Formation

In order to operate the intrinsic QD device, a top gate is needed to apply enough of an electric field to form an inversion layer in the intrinsic SOI nanostructures to bias them into conductance. To prevent leakage to this conducting top gate, a 100 nm thick interlayer  $SiO_2$  layer must be first deposited above the device. A similar PECVD process to that described in section 4.3.4 is used to deposit this. This is then patterned with photolithography using AZ2070 resist in much the same way as the dopant diffusion mask in section 4.3.4 using our photolithography mask (see Fig. 4.3.1(c)). We define a 10  $\mu m$  box shape in the AZ2070 resist above the nanostructure and intrinsic region of each device and transfer this pattern into the interlayer  $SiO_2$ . The pattern transfer is done via RIE using exactly the same process as that used in section 4.3.4 to define the dopant diffusion mask. This is necessary so that a 5  $\mu m$  Al top gate can then be deposited above the same region of each device to enable device operations without any significant potential for leakage or screening between device side gates and QD operations.

Although at first glance the process seems like it should be identical to that developed previously for the dopant diffusion mask, one of the key challenges observed after various trials was the removal of voids which often formed between the QD channels (see Fig. 4.3.7(a)). Via using the standard  $SiH_4$  and  $N_2O$  gas under RF power to generate a chemical

reaction which deposited the interlayer  $\text{SiO}_2$ , it was observed that deposition wasn't isotropic enough to fill the gaps. Furthermore, it can be clearly seen from Fig. 4.3.7(a) that  $\text{SiO}_2$  growth seems to be faster around protruding corners (e.g. point A in Fig. 4.3.7(a)) rather than in the depressed corners (e.g. point B in Fig. 4.3.7(a)). A possible explanation for this could be that because the deposition occurs at relative high temperatures ( $350\text{ }^\circ\text{C}$ ) and RF power, the  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  gases therefore have greater mean free path and average velocity. This results in a lower probability for  $\text{SiO}_2$  nucleation to occur in depressed corners because the gases molecules have simply too much kinetic energy to react in such a small volume of space. Point A on the other hand has a much better chance of  $\text{SiO}_2$  formation because of the volume of free space around it. Therefore, extensive process optimisation was required in order to achieve  $\text{SiO}_2$  growth with better conformity around all surfaces (horizontal and vertical) of the substrate to ensure any voids were filled.



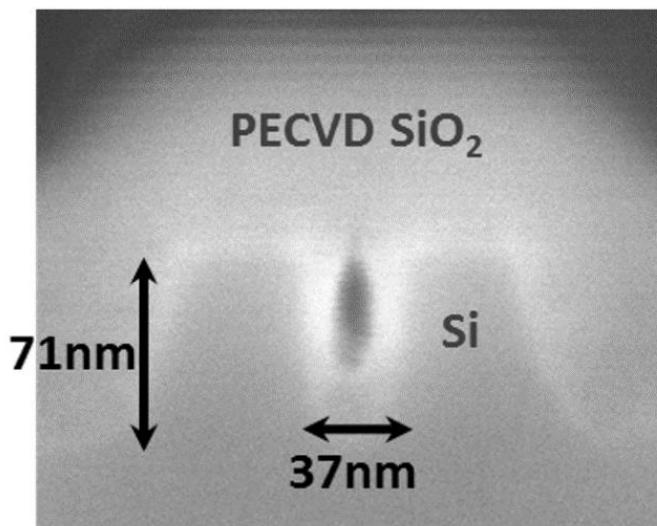
**Fig. 4.3.7(a)** A cross-sectional SEM image of a nanoscale SOI channel after interlayer  $\text{SiO}_2$  and top gate deposition. Voids can be clearly seen between gaps where SOI channels are in close proximity to one another.

Through reference to our Oxford Instruments RIE80+ system's specifications, we decided to explore and migrate the PECVD deposition process from a gas based to a liquid based tetraethyl orthosilicate (TEOS) source to achieve better conformity. Through extensive optimisation of the TEOS system, power and the PECVD chamber conditions, we found that the setup in Table 4.3.7(b) produced the best conformity around our QD nanoscale SOI

channels. Fig. 4.3.7(c) shows an SEM cross-sectional image of a deposition of  $\text{SiO}_2$  using this optimised PECVD process on two 65 nm wide channels etched  $\sim$ 70nm deep into bulk Si.

SiO <sub>2</sub> TEOS Deposition Recipe	
<b>TEOS Valve</b>	Open
<b>O<sub>2</sub> Gas Flow Rate (sccm)</b>	500
<b>Chamber Pressure (mTorr)</b>	500
<b>RF Forward Power (W)</b>	40
<b>RF Power Pulse Time (s)</b>	12
<b>LF Forward Power (W)</b>	40
<b>LF Power Pulse Time (s)</b>	8
<b>Table Temperature (°C)</b>	350
<b>Deposition Rate - (nm/s)</b>	0.703

**Table 4.3.7(b)** TEOS PECVD source, plasma and chamber conditions which gave maximum conformity during  $\text{SiO}_2$  deposition.

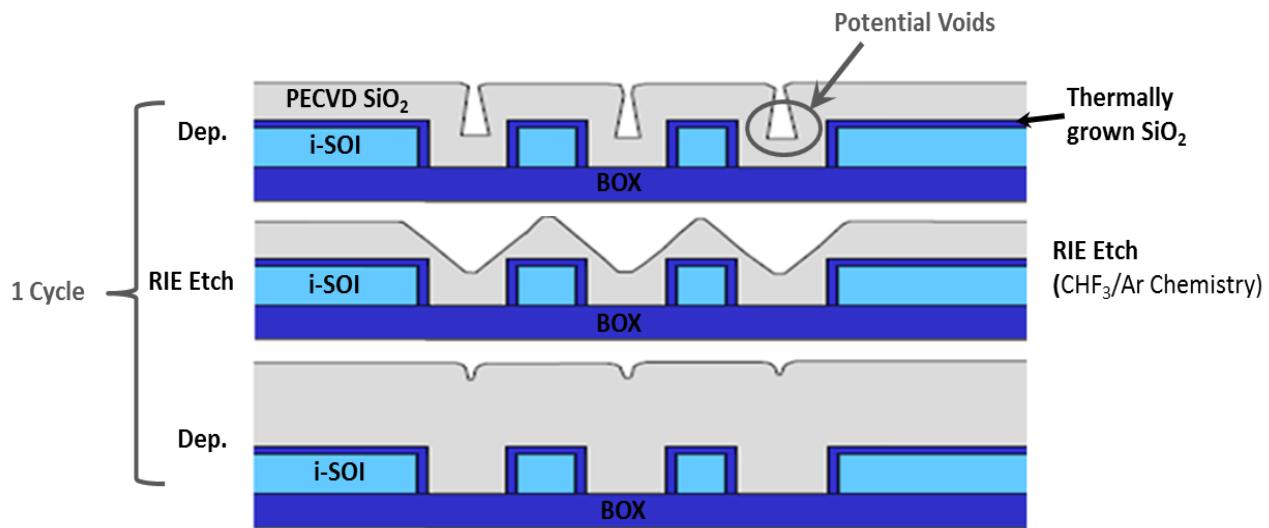


**Fig. 4.3.7(c)** Cross-sectional SEM image of  $\text{SiO}_2$  deposited via TEOS PECVD (with the conditions in Table 4.3.7(b)) above two 65 nm wide Si channels with a 37 nm lateral separation. The clear presence of a void can be seen between the two Si channels.

From Fig. 4.3.7(c), we can clearly see that despite an increased level of conformity compared to that previously achieved using the  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  gas sources, voids were still present between the two Si channels. Here we only used a separation of 37 nm between the two channels to ensure that the deposition would completely fill gaps in our actual QD structures.

Therefore, to remove the void formed between our QD channels, we developed an “etch back process” of repeatedly performing  $\text{SiO}_2$  deposition and etching cycles in order to effectively “round” the corners of the nano-channel structure such that sequential TEOS PECVD

deposition would fill the gaps. Fig. 4.3.7(d) shows a schematic for a cycle of our “etch back process” and what it aims to achieve. The  $\text{SiO}_2$  etching steps are performed via RIE with the same conditions as that shown previous in Table 4.3.4(b).



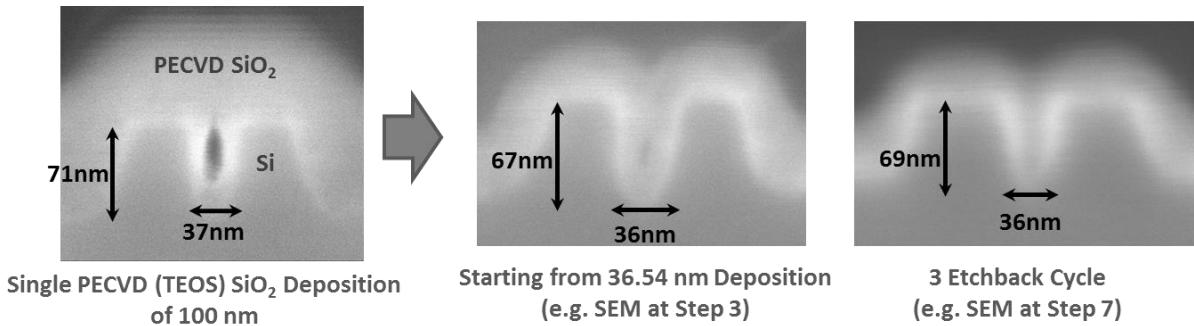
**Fig. 4.3.7(d)** A schematic diagram of the etch back process to remove voids formed during PECVD TEOS deposition of  $\text{SiO}_2$ . Step 1 is to deposit  $\text{SiO}_2$  to the point where voids are beginning to form. Step 2 is to then dry etch this freshly deposited  $\text{SiO}_2$  such that the void/gap opening is widened. Step 3 is a repeat deposition which will now begin to fill the void previously formed because the gap is now more open.

Through extensive experimentation, results showed that the following deposition and etching cycles in the etch back process gave the most repeatable and reliable results. Altogether 3 deposition and etch back cycles are needed to completely remove any voids formed for our given device dimensions.

### Etch Back Process

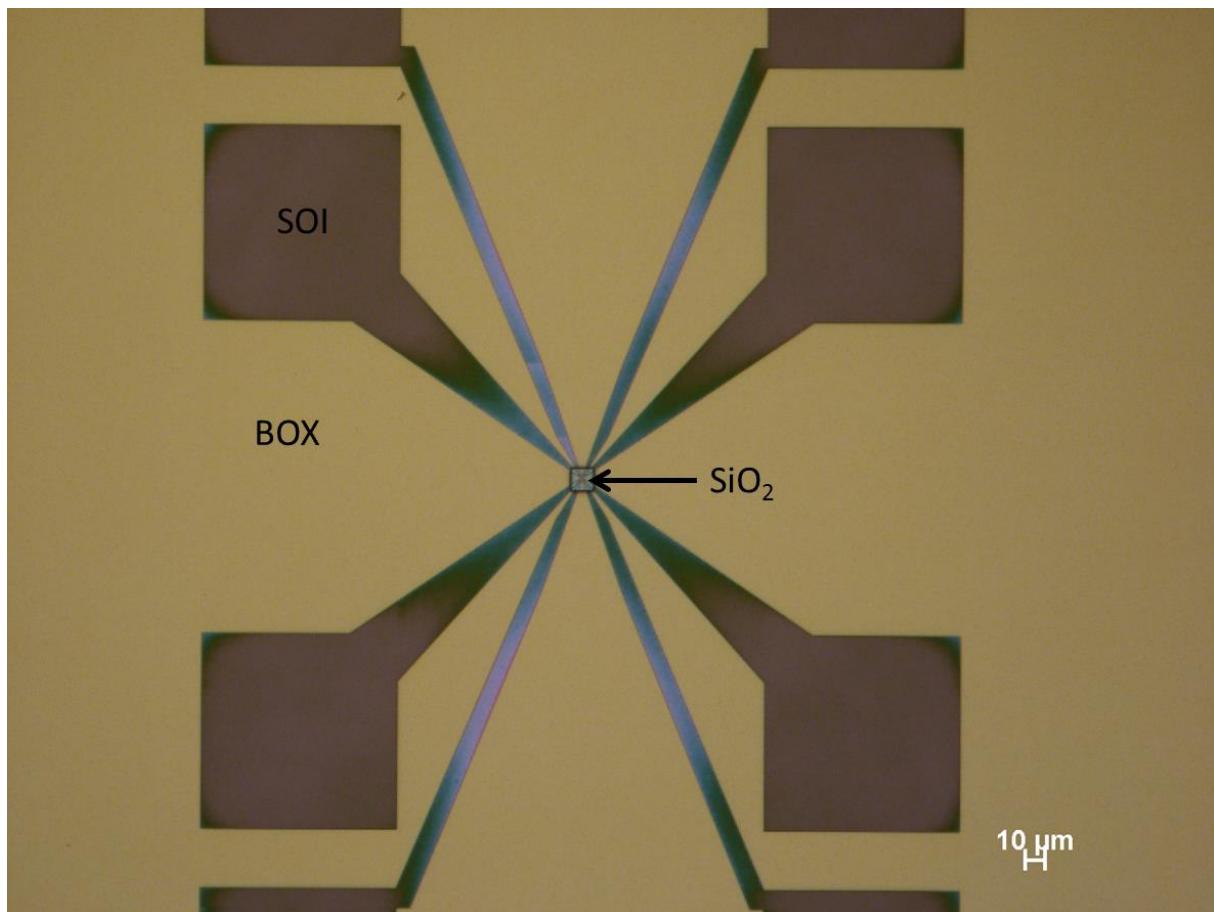
1. Deposit  $\sim 35$  nm of TEOS  $\text{SiO}_2$  ( $\sim 1$  m 7 secs deposition)
2. Etch back  $\text{SiO}_2$  until 15 nm thick ( $\sim 53$  secs etch)
3. Deposit TEOS  $\text{SiO}_2$  until  $\text{SiO}_2$  is  $\sim 35$  nm thick ( $\sim 40$  secs deposition)
4. Etch back  $\text{SiO}_2$  until 20 nm thick ( $\sim 36$  secs etch)
5. Deposit TEOS  $\text{SiO}_2$  until  $\text{SiO}_2$  is  $\sim 50$  nm thick ( $\sim 57$  secs deposition)
6. Etch back  $\text{SiO}_2$  until 30 nm thick ( $\sim 49$  secs etch)
7. Deposit TEOS  $\text{SiO}_2$  until  $\text{SiO}_2$  is  $\sim 130$  nm thick ( $\sim 3$  min 5 secs deposition)

Ellipsometry and profilometer measurements must be used throughout the etching process to accurately determine the etching depth and thickness. Fig. 4.3.7(e) below shows a sequence of SEM images (at different steps in the etch back process) which present the progress of our etch back process in completely removing any void formations between the nano channel.



**Fig. 4.3.7(e)** The figure demonstrates the effectiveness of our etch back process in reducing the size of voids formed between nanowire channels in close proximity. The left most SEM image is a cross-section of two Si channels with a separation of 37 nm laterally demonstrating the clear presence of a void formed after a single PECVD (TEOS)  $\text{SiO}_2$  deposition of 100 nm. The two SEM images to the right of the arrow demonstrate the progress at different steps in our etch back process in removing the void formed in the left most SEM image.

Following the application of this optimised interlayer  $\text{SiO}_2$  deposition process for device fabrication, the deposited interlayer  $\text{SiO}_2$  is then coated with a layer of photolithographically patterned AZ2070 resist to define a 10  $\mu\text{m}$  box shape above the nanostructure and intrinsic region of each device (see section 4.3.4 for details). This pattern is then transferred into the interlayer  $\text{SiO}_2$  via RIE (same process as in section 4.3.4). Again, ellipsometry and profilometer measurements can be used throughout the etching process to accurately determine the etching depth and thickness to make sure the BOX layer and SOI are not over etched. However it is important to point out the etching depth must now take into account the thermal oxide grown around the SOI in order to achieve good Ohmic contact in the future when Al is deposited above the SOI contact pads (see Fig. 4.3.5(a)). Any residual AZ2070 resist after the RIE pattern transfer can be easily removed by  $\text{O}_2$  plasma ashing with an FNA and RCA wet clean to ensure a contaminant free surface. An optical image of the etched 100 nm thick interlayer  $\text{SiO}_2$  square before resist removal via oxygen plasma ashing is shown in Fig. 4.3.7(f). As can be seen, optical alignment once again gives an error of around 1  $\mu\text{m}$  which must be taken into account in the designs and essentially limits our ability to reduce the dimensions of any one particular design layer of the device.



**Fig. 4.3.7(f)** Optical image of the device before metallisation, centred around the etched 100 nm thick interlayer  $\text{SiO}_2$  10  $\mu\text{m}$  square pattern (with resist on top).

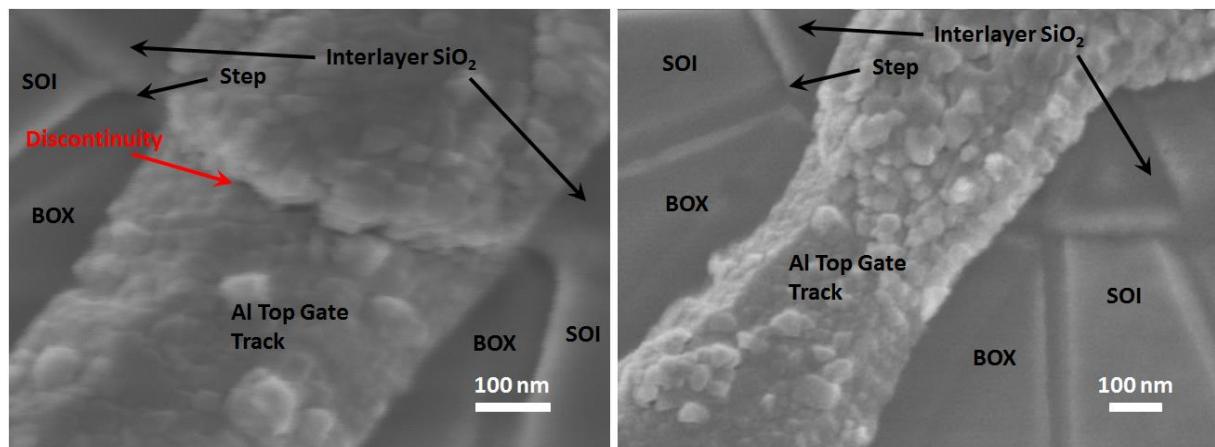
#### 4.3.8 Contact Metallisation

The final step of the fabrication process is to metalize the contact pads with aluminium such that they can be wire bonded to measurement equipment for electrical characterisations. This is performed in parallel across the sample in a single step along with the deposition of the 5  $\mu\text{m}$  aluminium top gate above the interlayer top gate  $\text{SiO}_2$  (which is above the intrinsic SOI device nanostructure region). Ideally, we would like aluminium tracks to be precisely deposited on the doped silicon tracks all the way as close as possible to the 5  $\mu\text{m}$  top gate (but not touching it), however, this is not possible due to photolithography having an alignment error of  $\sim 1\text{--}2\mu\text{m}$ . Therefore, the aluminium tracks stop  $\sim 12\ \mu\text{m}$  away from the nanostructure, and are  $\sim 3\ \mu\text{m}$  wide to account for these alignment errors should they arise.

The Al contacts go up to 12  $\mu\text{m}$  away from the device nanostructure to minimize the device's source to drain resistance as much as possible. This increases the possibility of carrying out RF characterisations of the device operations (which provides for a faster method of device measurement compared to DC) as it increases the cut-off frequency of the structure to become potentially compatible with our RF reflectometry [51] measurement equipment.

To carry out the Al deposition, we firstly use the same photolithography techniques as that in sections 4.3.4 and 4.3.7 to align the designed Al contact pad and top gate patterns to the SOI devices. However unlike before where a negative tone resist (AZ2070) was used, here we use the commercially available Microposit® S1813 positive tone resist (where the exposed areas are removed after development). This is first spun on the sample at 5000RPM, baked at 95 °C for 1 min and then exposed for 1.9 seconds with a contact force of 1 Bar. Post exposure, the sample is developed in MF319 developer for 25 seconds to remove the resist where it has been exposed. This leaves the device contact pads, tapers and top gate design clear of resist.

The sample is then dipped in to 20:1 BHF for a few seconds to remove any native oxide formed on the SOI structures and placed immediately into the vacuum chamber of an evaporator for Al deposition. We use the Leybold® Lab 700H vertical evaporator system for evaporation (and in turn deposition) of Al via an e-beam heating gun. The process works by firstly melting then evaporating a solid Al source via e-beam. The deposition rate can be controlled by adjusting the power of the e-beam gun. The evaporated Al then deposits onto our sample at a target rate of 2.5 Å/s to form a 180 nm layer. The deposited Al needs to be this thick because it must cover the vertical step imposed by the thickness of the interlayer  $\text{SiO}_2$ . Trials showed that an Al deposition of 150 nm or less demonstrated discontinuity in the operation of the top gate. The left figure in Fig. 4.3.8(a) shows an SEM image of a 140 nm thick deposited Al top gate layer which showed signs of discontinuity at the step presented by the interlayer  $\text{SiO}_2$ . The right figure in Fig. 4.3.8(a) shows an SEM image of a 180 nm thick Al layer without any signs of discontinuity at the same step presented by the interlayer  $\text{SiO}_2$ .

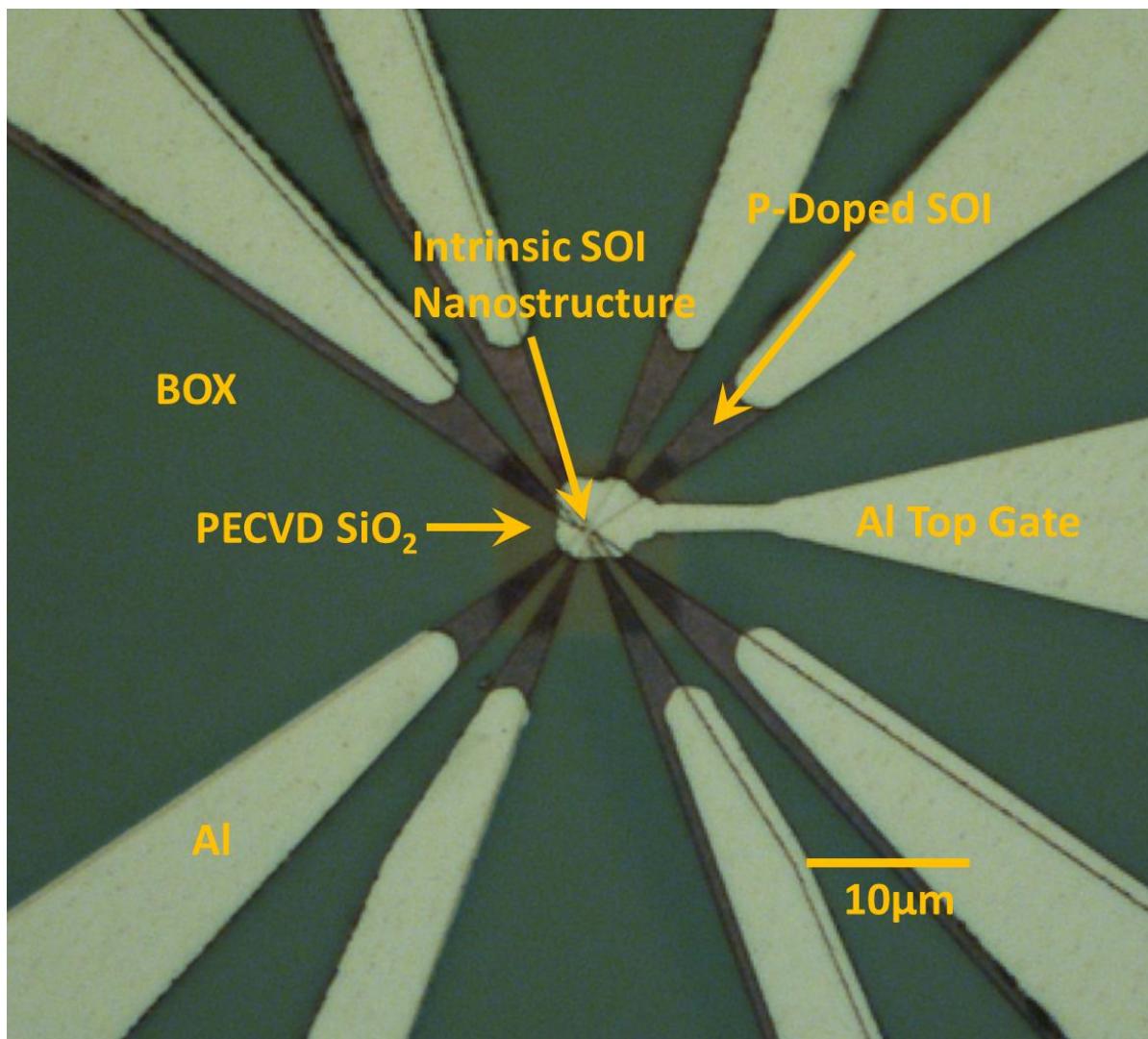


**Fig. 4.3.8(a)** Left: SEM of a 140 nm Al layer deposited on the SOI substrate and interlayer  $\text{SiO}_2$  showing a discontinuity. Right: SEM of a 180 nm thick Al layer over the same device structure without signs of discontinuity at the interlayer  $\text{SiO}_2$  step.

The sample is then immersed in acetone for 5 hours to remove the S1813 resist and any Al deposited above the S1813 resist is lifted off such that only the desired areas (i.e. the Al

deposited directly on the device's contact pads, tapers and to form the top gate) are left. The Al is annealed in an RTA (rapid thermal annealer) in  $N_2$  atmosphere at 350 °C for 15 min to form good Ohmic contact between the aluminium and SOI. This alloys the Al with Si and further reduce any potential contact resistance.

Fig 4.3.8(b) shows an optical image of a finalised device after contact metallisation and top gate formation. This gives an indication of the level of alignment accuracy achieved between 4 layers of lithography – as can be seen, there's around 1  $\mu m$  misalignment between each layer which is unavoidable with photolithography.



**Fig. 4.3.8(b)** Optical image of a finished device after metallisation, centred around the top gate.

## 4.4 Simulation and Fabrication Conclusions

Fig. 4.4(a) shows a chip scale photo and a device array photo of result of our fabrication process in being able to realise 144 QD devices in parallel – a key advantage of our approach in being compatible with conventional CMOS and VLSI fabrication techniques. Out of a total of 144 exposed devices, a high fabrication yield was achieved with over 80% of the QDs in a chip having dimensional variations of less than  $\pm 5$  nm compared to the design. The average realised QD dimension was 61 nm across 144 devices with a standard deviation of 3.4 nm. To our knowledge, this is the first successful attempt at obtaining such high density and high resolution lithographically defined quantum devices in parallel in such large numbers with repeatable device dimensionalities on SOI using HSQ.

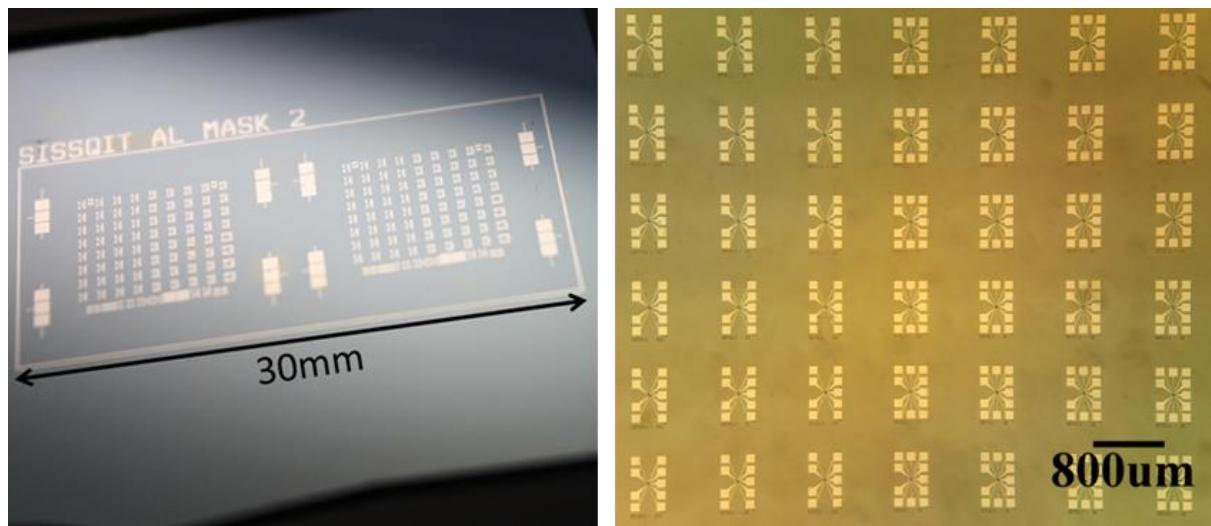
Another unique feature offered by our process is flexibility to be able to realise a range of different QD systems in parallel with only changes to one step of the fabrication process. Trials showed a variety of different nanostructure designs can be realised repeatedly (Fig. 4.4(b)) with completely different QD operations possible without significantly affecting the fabrication turnover time. Further to this, a key advantage of the device architecture used is that of in-plane Si side gates. This not only minimizes device lithography to a single process, but offers systems which have a minimal potential for leakage between control gates which therefore increases fabrication yield.

Our fabrication method also enables a high level of scalability in the device architecture where, as can be seen from Fig. 4.4(b), a QD can be easily added to the QD channel through addition of a constriction, QD and a single side gate. Overall, given the availability of tools and fabrication systems needed, the whole fabrication process requires only a 2 week turnaround time for the fabrication of over 100 QD systems with repeatable dimensions.

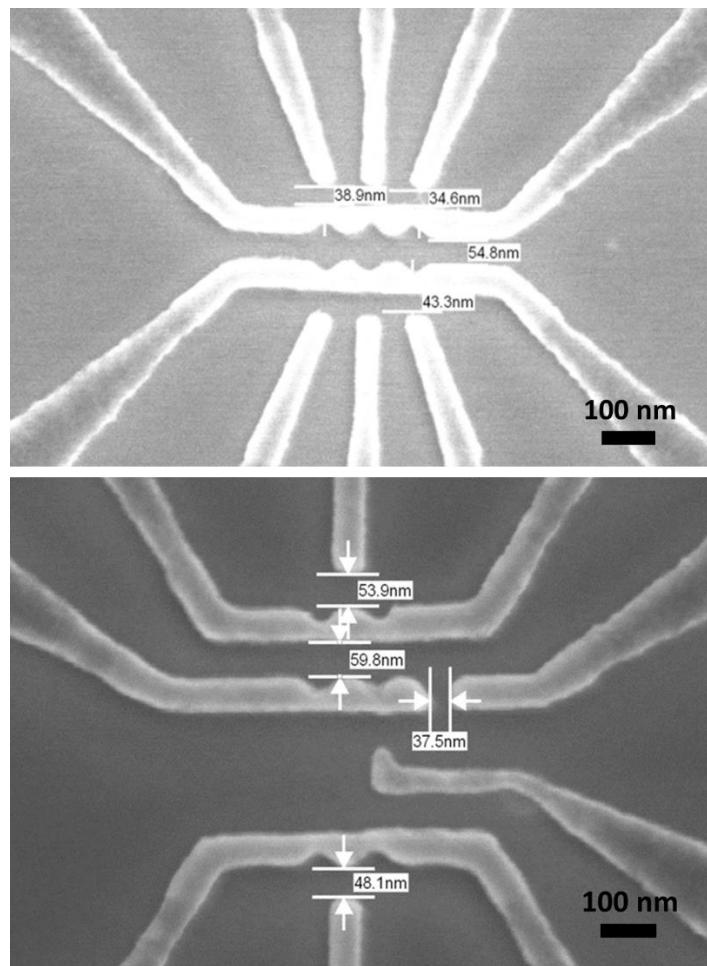
These results demonstrate the consistency of our proposed novel process and paves the way towards true single electron occupation and manipulation in potentially scalable intrinsic Si QDs. This work also provides the required reproducibility and flexibility which can potentially support the realisation of future systems of more integrated and complex design for quantum information processing.

In addition to the novel fabrication methodologies proposed, we also introduced a new method of charge detection for single electron turnstile operations through simulations which make use of the periodicity present in the charge stability diagram of a DQD. The results from this work have impacted the field through various publications in journals as well as in a

number of different conferences both orally and via poster. This can be found in the list of publications at the start of this thesis.



**Fig. 4.4(a)** Left: Optical photo of a finished device after metallisation. Right: Photo taken via an optical microscope of the device array present on each finalised chip. Here devices with different designs were arrayed and fabricated.



**Fig. 4.4(b)** Top: SEM of a dual DQD device nanostructure with three side gates for more sensitive constriction control. Bottom: SEM of a multi-QD device optimised for our project partners from Hitachi Cambridge Laboratories.



# Chapter 5

## Electrical characterisations and fabrication process improvements

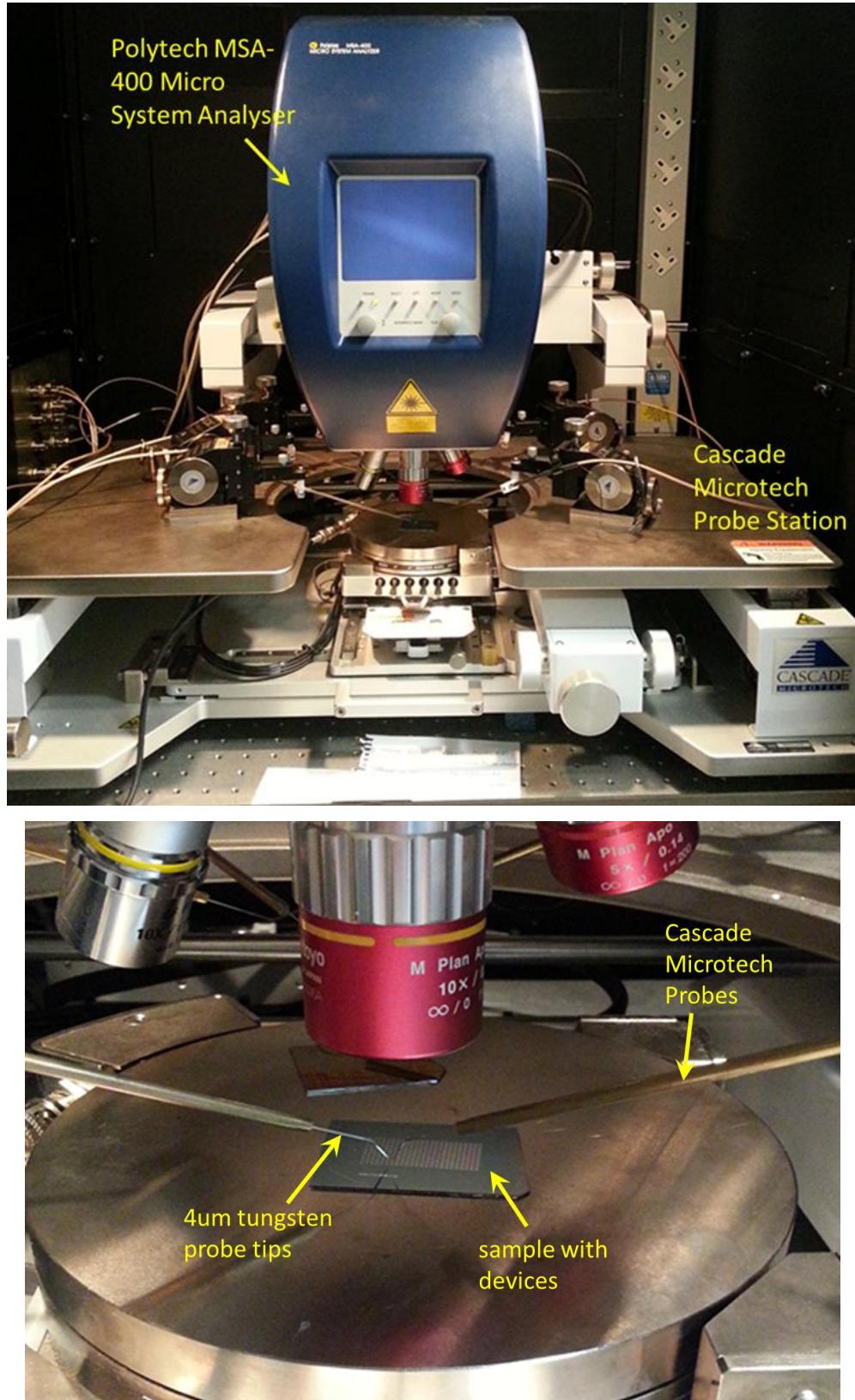
### 5.1 Introduction

In order to gain an effective understanding of the viability of our fabrication process and device design in realising repeatable single electron manipulations, electrical characterisations must be performed. To undertake this, we carried out both room temperature and cryogenic electrical measurements of our fabricated devices to study both device performance from a statistical point of view as well as the response of the best devices at low temperatures. Feedback from this can then be used to formulate improvements to the fabrication process to further enhance device performance.

### 5.2 Characterisations of a single electron transfer device

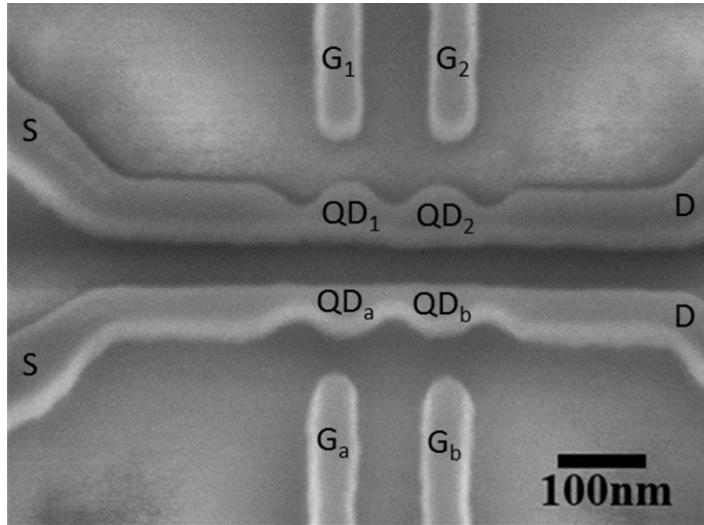
#### 5.2.1 *Room Temperature Characterisation*

Initial measurements and characterisations of our DQD device was carried out at room temperature using a Polytech MSA-400 micro system analyser and on a Cascade Microtech probe station connected coaxially to an Agilent B1500A parameter analyser. The equipment was setup on an optics table with intelligent tuneable vibration dampening technology to reduce electrical noise during measurement. Fig. 5.2.1(a) shows photos of our room temperature measurement setup. Samples were placed in a dark cupboard and 4  $\mu\text{m}$  wide tungsten probe tips were used for measurement to obtain good Ohmic contact with each device's Al contact pads.



**Fig. 5.2.1(a)** Top: Photo of our measurement facility setup used for room temperature measurements of our device characterisations. Bottom: A photo of the setup during measurement using tungsten probe tips to connect the device to measurement equipment.

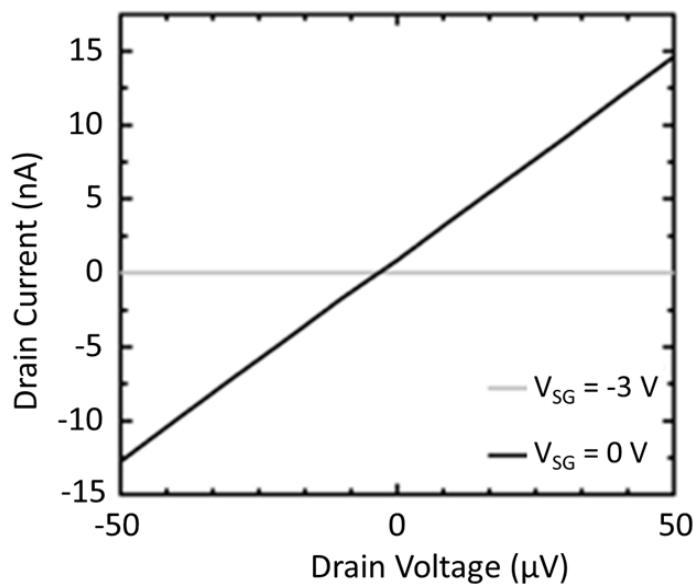
Fig. 5.2.1(b) shows a SEM of one of our fabricated dual DQD devices under measurement (before top gate and interlayer  $\text{SiO}_2$  formation) with the labelled device components.



**Fig. 5.2.1(b)** SEM image of a fabricated dual DQD device before device top gate and interlayer  $\text{SiO}_2$  formation.  $\text{QD}_{1,2,a}$  and  $b$  label the QDs of each DQD structure and  $\text{G}_{1,2,a}$  and  $b$  are their respective closest side gates for electrostatic control of single electron occupation. S and D label the source and drain of the DQD channels.

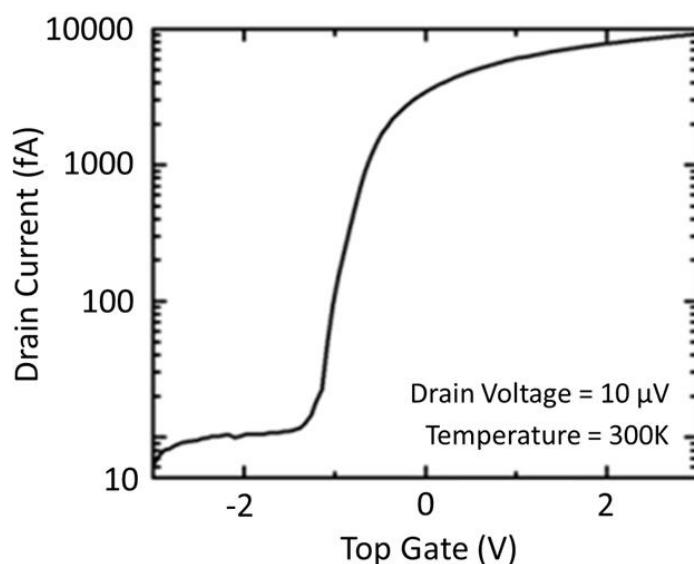
Using our room temperature measurement setup, Fig. 5.2.1(c) shows a plot of the measured source to drain current,  $I_{\text{DS}}$ , through one of the DQDs of a particular device (see Fig. 5.2.1(b)) at a temperature of 300 K as a function of the applied source to drain voltage,  $V_{\text{DS}}$ , at two different gate biases (for the closest side gates for the DQD). A source to drain resistance of  $\sim 50 \text{ k}\Omega$  was observed with a clear distinction between when a single voltage of  $V_{\text{SG}} = 0 \text{ V}$  and  $-3 \text{ V}$  was applied to all gates (all side gates and the top gate). Here, the behaviour is analogous to that of a semiconducting MOSFET on/off, where the silicon DQD channel is turned on and off respectively for the two gate voltages. Preliminary electrical characterisation also showed minimal leakage current through the BOX between the SOI and the Si substrate as well as a clear Ohmic contact between the Al contact pads and the SOI. In addition, the interlayer  $\text{SiO}_2$  which is deposited between the side gate, source, drain and top gate have a breakdown voltage of  $> 22 \text{ V}$ , well above the operating voltages of the device. This demonstrates one of the key benefits of an SOI based approach in eliminating the potential for leakage between device components compared to the more conventional 2DEG QD structures which require numerous Al gates for operation. This also significantly improves the potential in obtaining higher yields in the parallel fabrication of devices.

Through extensive electrical characterisations across a chip, it was found that over 70% of DQD channels could have their conductance successfully and distinctively switched on and off. With the channel conducting, channel resistances were observed to be between the ranges of 50-200  $\text{k}\Omega$  across the chip. This is of a sufficient resistance to allow for observations of single electron turnstile operations across a QD at cryogenic temperature.



**Fig. 5.2.1(c)** DQD source to drain current,  $I_{DS}$ , as a function of source to drain voltage,  $V_{DS}$ , with voltages  $V_{SG}=0$  V and -3 V applied to all side gates and top gate.

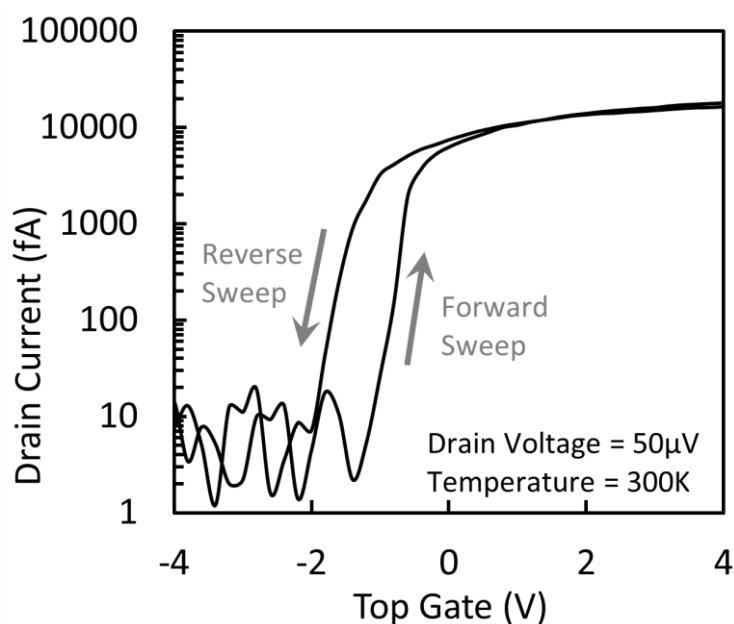
Fig. 5.2.1(d) shows the electrical measurements of a particular DQD channel's source to drain current  $I_{DS}$  at a temperature of 300 K as a function of the applied top gate voltage  $V_{TG}$  at a source to drain voltage,  $V_{DS} = 10 \mu$ V. Characteristic MOSFET behaviour was observed with all other side gates grounded. The top gate here is effective in turning the source to drain channel off with a high electron mobility here of  $4800 \text{ cm}^2/\text{Vs}$ . In addition, a threshold voltage of around -1V was observed which matches expectations given the temperature (this becomes positive at cryogenic temperatures). Via similar characterisations across the chip, around 70% of devices tested demonstrated similarly consistent top gate control over the DQD's channel conductance, with electron mobility ranging from  $1900 \text{ cm}^2/\text{Vs}$  to  $4800 \text{ cm}^2/\text{Vs}$ .



**Fig. 5.2.1(d)** DQD source to drain current,  $I_{DS}$ , as a function of top gate voltage,  $V_{TG}$ , with all other gates grounded at a drain voltage,  $V_{DS}=10 \mu$ V.

This effective top gate control over the DQD's channel conductance provides evidence that our fabrication process is reliable in producing the required high quality thermal  $\text{SiO}_2$  and PECVD deposited interlayer  $\text{SiO}_2$  with high enough dielectric constants. In addition, the quality of the oxide also means a lower probability for any electrical leakage to occur between device components during measurements at lower temperatures.

However, although we had an effective device top gate, we did observe hysteresis in the measured drain current when repeating forward and reverse sweeps of the top gate voltage. This can be clearly seen in an example measurement in Fig. 5.2.1(e). In addition, across the fabricated chip, it was observed that the threshold voltage at which the top gate could turn the DQD channel on ranged between -2 and 2 V (the device measured in Fig. 5.2.1(d) had a threshold voltage of around -1V). This suggested the presence of both moving and fixed trapped charges in the device structure respectively, which most likely originated in the interface between the different layers of the device during lithography and also within PECVD of the interlayer  $\text{SiO}_2$ . This is despite attempts to ensure a clean interface via the use of FNA, RCA and BHF sample cleaning where possible in the fabrication process.



**Fig. 5.2.1(e)** DQD source to drain current,  $I_{DS}$ , as a function of top gate voltage,  $V_{TG}$ , swept in the forward and reverse voltage directions with all other gates grounded at a drain voltage,  $V_{DS}=50 \mu\text{V}$ . Clear evidence of hysteresis can be observed which is due to the presence of floating charges in the device structure.

Despite these observations however, fixed charges which shift the threshold voltage between devices shouldn't affect QD device single electron operations too much at cryogenic temperatures as these charges are fixed. In addition, although moving trapped charges will result in noise during measurements, they do have a tendency to freeze out and become fixed

during cryogenic temperature measurements (which is what is observed in following section 5.2.2). Given the accuracy in QD lithography using HSQ and the thermal  $\text{SiO}_2$  growth process afterwards, we expect the trapped charges to be limited to structures external to the SOI QDs and should mean QD operations are relatively free of any potential charge traps which can increase the possibility of forming unexpected QDs.

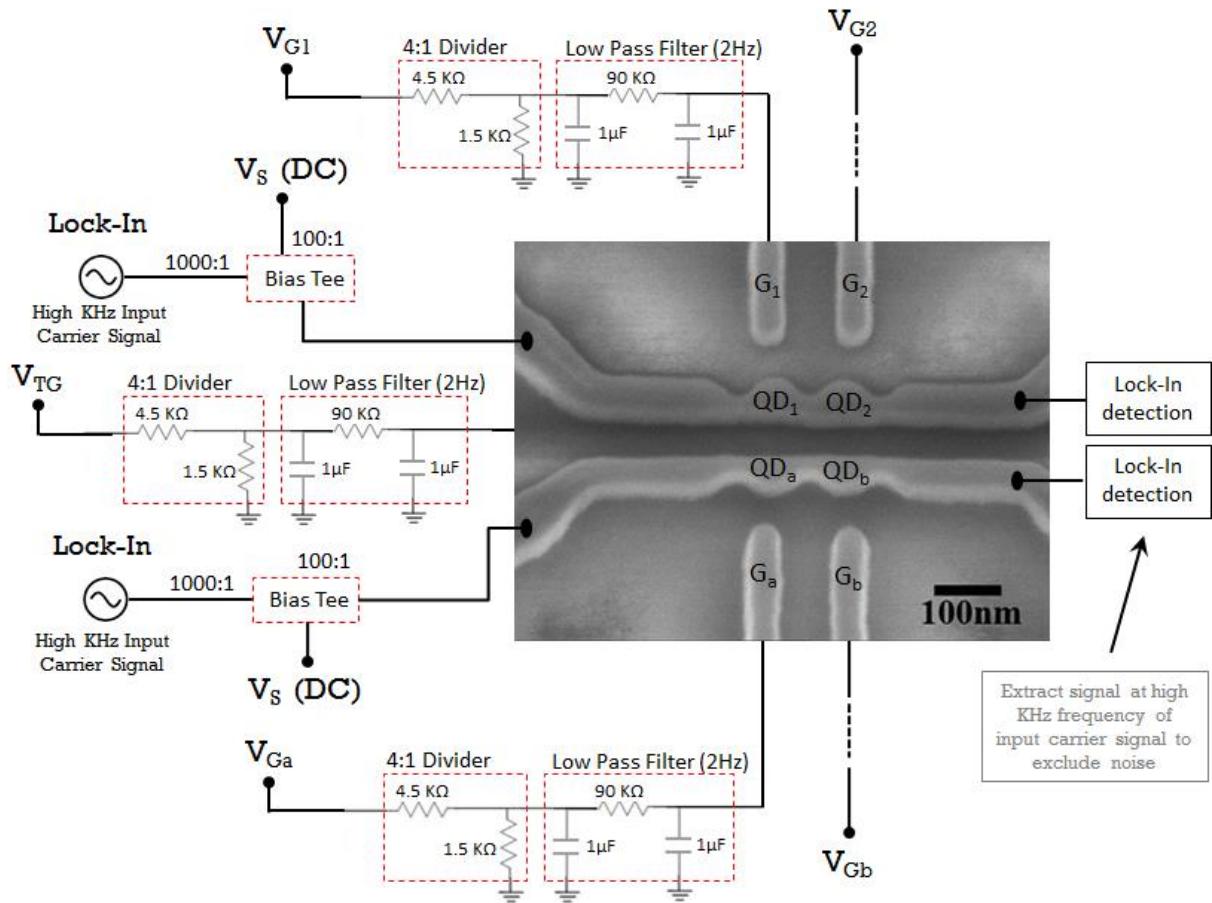
### 5.2.2 *Cryogenic Temperature Characterisation*

In order to determine the ability of our dual DQD devices in supporting single electron manipulations, low temperature measurements must be performed. Due to the absence of required equipment in the University of Southampton, measurements were taken in our project partner's laboratory in the University of Cambridge.

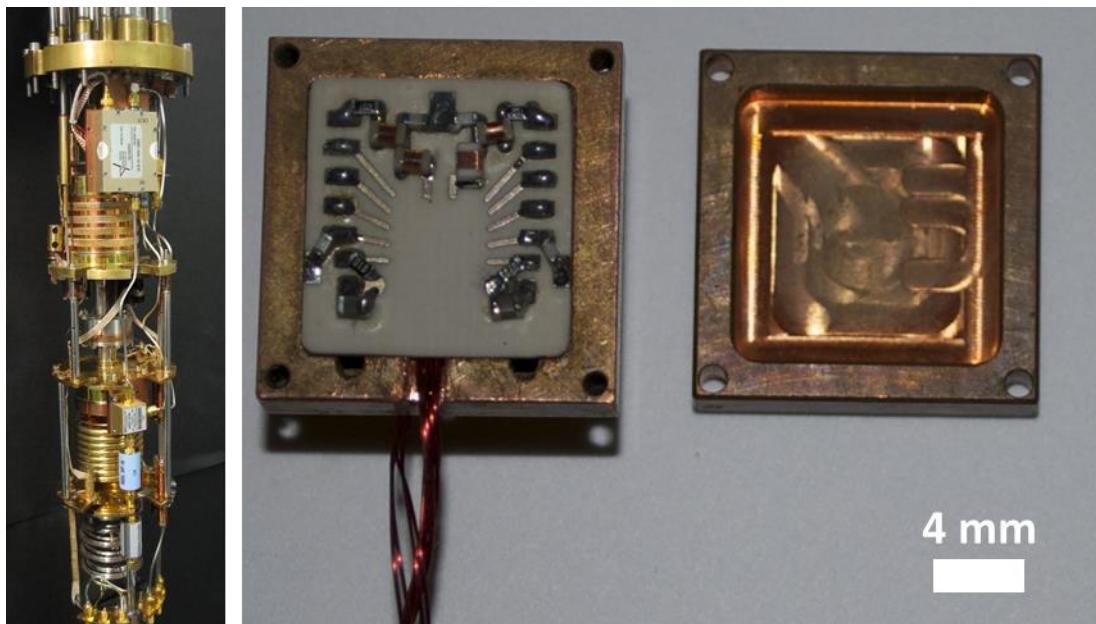
Here, a custom-made helium-3 fridge system was used with DC lines connected to RC  $\pi$  low pass filters ( $3 \text{ dB}$  cutoff for frequencies  $> 1 \text{ kHz}$ ) and voltage dividers to perform low temperature measurements of our DQD devices. Measurement equipment included HP 34401A multimeters, SRS SR570 low noise current pre-amps, Keithley 2400 source meters and a Stanford SR830 DSP lock-in amplifier. Fig. 5.2.2(a) shows a diagram of the device connections to the equipment used when performing low temperature measurements of a DQD.

In order to mount our devices onto the fridge system, each chip had to be cut into  $4 \times 4 \text{ mm}$  pieces (with 16 devices on each piece) in order to fit onto the custom made sample holder for the low temperature setup (see Fig. 5.2.2(b)). The sample pieces are stuck on the holder and each device is sequentially wire bonded onto the tracks on the holder which then connect via a coaxial cable to the measurement setup. Fig. 5.2.2(b)) also contains a photo of the custom made Helium-3 fridge system dipstick onto which the sample holder is connected.

Via use of this system, a repeat of the measurement (Fig. 5.2.1(c)) in the previous section at a temperature of  $80 \text{ mK}$  with the source to drain voltage,  $V_{\text{DS}}=1 \text{ mV}$ , and applied side gate voltages of  $V_{\text{SG}}=-4 \text{ V}$  and  $4 \text{ V}$  (Fig. 5.2.2(c)) was made. Rather than a smooth transition like that seen in Fig. 5.2.1(c) from an off to an on state for the channel conductance, we observed oscillating peaks in drain current,  $I_{\text{DS}}$ , as a function of applied top gate voltage,  $V_{\text{TG}}$ . Given the noticeable periodicity in the consecutive peaks, these correspond to the characteristic Coulomb oscillations through the DQD system (previously explained for SETs in section 2.2) and signify consecutive single electron transfers through the QDs. Measurement at two different applied side gate voltages showed distinctive shifts in the pattern of these Coulomb

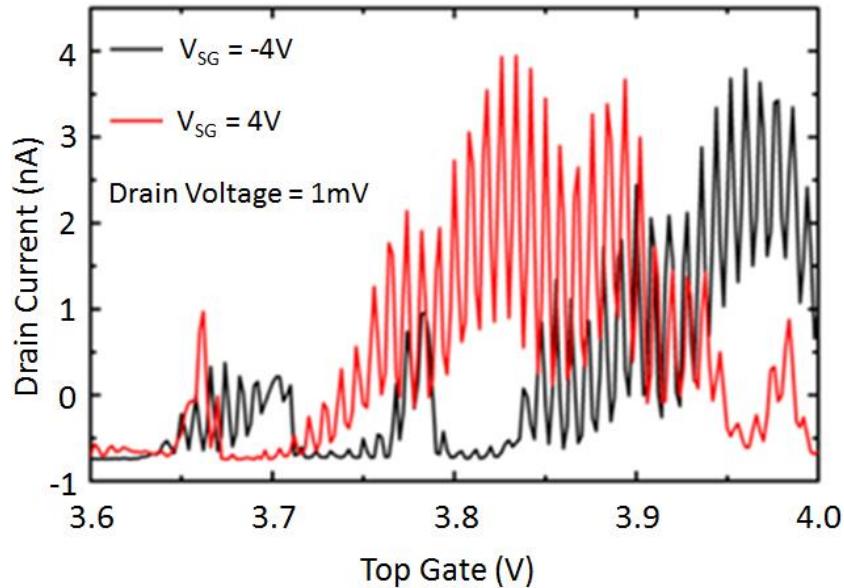


**Fig. 5.2.2(a)** A diagram of the device connections, filters and voltage dividers which were used to perform low temperature measurements of our device. The capacitance and resistance values of the filters were set depending on the resistance of the DQD channel of the device.  $V_{G2}$  and  $V_{Gb}$  are connected to the device gate electrodes by the same divider and filter setup as  $V_{G1}$  and  $V_{Ga}$  respectively.

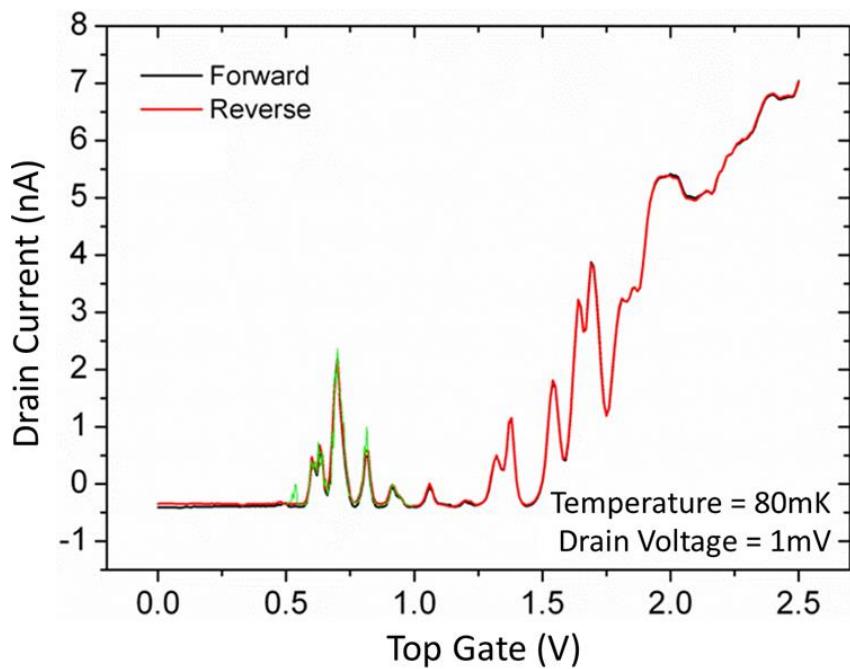


**Fig. 5.2.2(b)** Left: A photo of our custom made helium-3 fridge system dipstick. Right: A photo of the sample holder used to perform low temperature measurements of our devices.

oscillations which displayed the same periodicity. This supports the thought that single electrons are in fact being transferred in and out of the QDs rather than through some kind of charge trap. The periodicity here gives us some idea of the charging energy of each QD for our given fabricated QD dimensions.



**Fig. 5.2.2(c)** DQD source to drain current,  $I_{DS}$ , at a drain voltage  $V_{DS}=1$  mV as a function of top gate voltage,  $V_{TG}$ , with voltages  $V_{SG}=4$  V and  $-4$  V applied to side gates (and all other gates grounded) at a temperature of 80 mK.

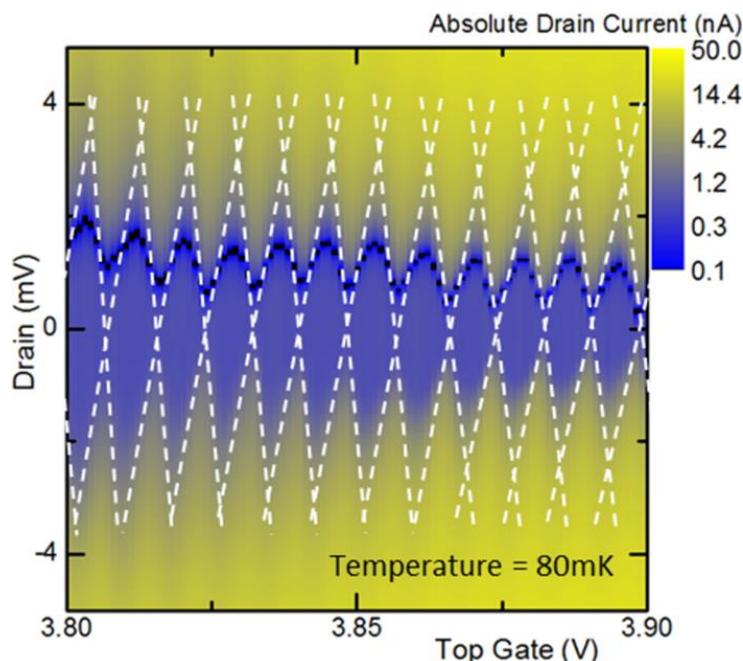


**Fig. 5.2.2(d)** DQD source to drain current,  $I_{DS}$ , at a drain voltage  $V_{DS}=1$  mV as a function of top gate voltage,  $V_{TG}$ , with all other side gates grounded at a temperature of 80 mK. Forward and reverse sweeps of the top gate voltage is seen to demonstrate no hysteresis in the observed drain current.

Through sweeping the top gate in forward and reverse directions for the same measurement (using a different DQD channel), practically no hysteresis was observed (see Fig. 5.2.2(d)).

This is in contrast to the observed hysteresis seen previously in Fig. 5.2.1(e) and indicates the freezing out of mobile charges which were present at room temperatures. This means that our device will be capable of supporting Coulomb oscillation and single electron turnstile measurements which will not drift in voltage space with time which is often a problem with devices with mobile charges.

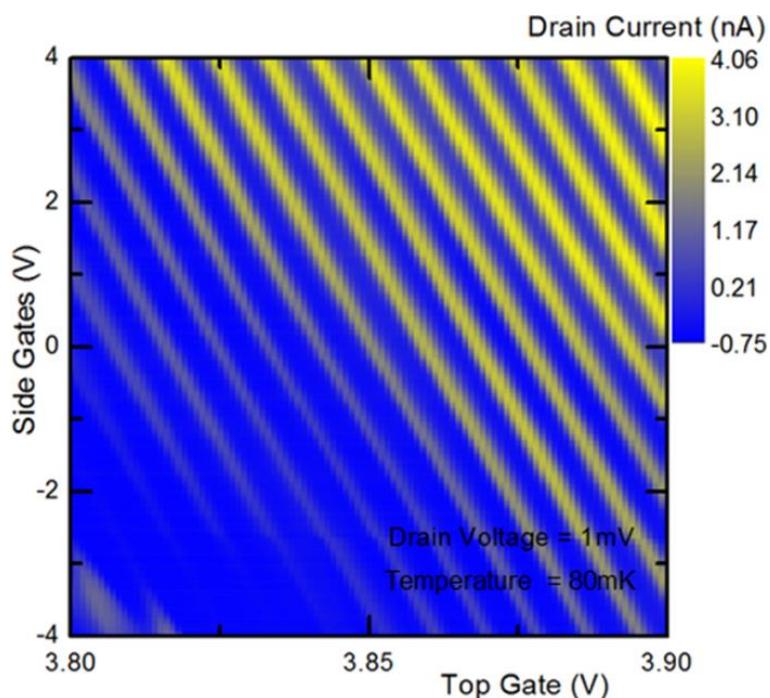
Fig. 5.2.2(e) shows a contour plot of the drain current,  $I_{DS}$ , of the same DQD channel measured as a function of the applied source to drain voltage,  $V_{DS}$ , and applied top gate voltage,  $V_{TG}$ , at a base temperature of 80 mK. Diamond shaped Coulomb blockade regions can be clearly seen in contrast to the conducting regions, where current through the DQD is low due to Coulomb blockade (section 2.3). By approximating the DQD as two QDs of dimensions  $a = 25$  nm and assuming spherical QDs, their capacitance can be approximated by  $C = 4\pi\epsilon a$  where  $\epsilon$  is the permittivity of silicon. The charging energy of each QD is then given by  $E = e^2/C \approx 2$  meV. Given that  $V = E/e$ , we therefore expect  $V_{DS} \approx 2$  mV to be the point beyond which Coulomb blockade is fully lifted for all values of  $V_{TG}$ . This agrees with Fig. 5.2.2(e) where the vertex of the largest Coulomb blockade diamond is at  $V_{DS} \approx 2$  mV and verifies the approximation that the QDs are  $\sim 25$  nm in size. This particular device therefore had slightly smaller QDs than our expectations from the fabrication process of 42 nm, and might be due to the PADOX effect [41] where different nanostructure geometries significantly affect the rate of oxidation.



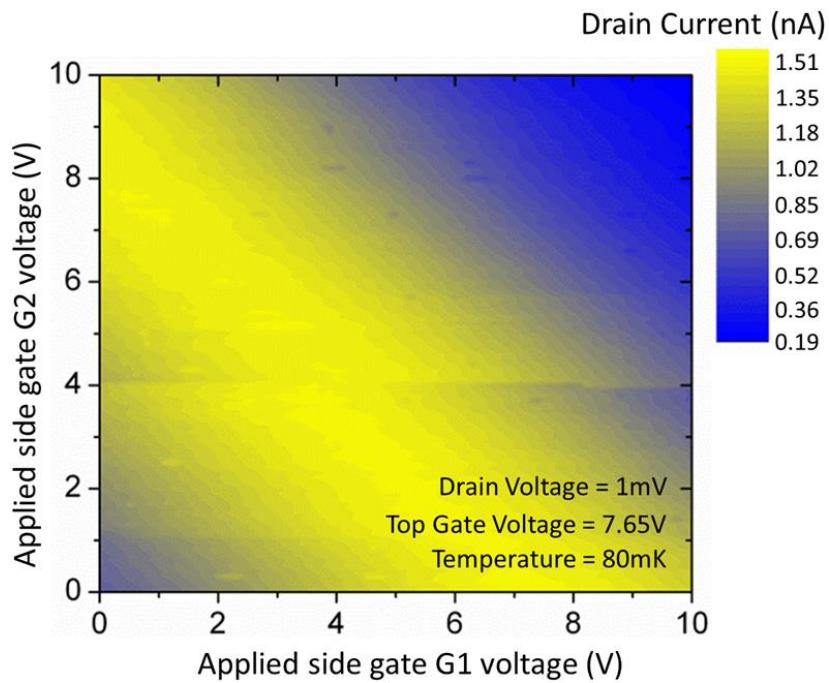
**Fig. 5.2.2(e)** Contour plot of the absolute DQD source to drain current,  $I_{DS}$ , as a function of top gate voltage,  $V_{TG}$ , and applied drain voltage,  $V_{DS}$ , at a base temperature of 80 mK. Dotted white lines approximately outline the Coulomb diamonds.

Fig. 5.2.2(f) shows a contour plot of the drain current,  $I_{DS}$ , at a base temperature of 80 mK as a function of the applied top gate voltage,  $V_{TG}$ , and a voltage  $V_G$  applied to the two closest side gates of the DQD with a source to drain voltage,  $V_{DS} = 1$  mV. Again, like before only a single DQD channel in our dual DQD device was measured here. Effective control across multiple Coulomb oscillations with both the top gate and side gates signifies consecutive single electron tunnelling and blockade events through the DQD system (section 2.2).

Although single electron turnstile operations were successfully observed for a number of DQD devices, one of the particular weaknesses observed with our fabricated devices was however that there was always insufficient electrostatic coupling from the two nearest side gates to the two respective QDs of the DQD. A contour plot of  $I_{DS}$  at a base temperature of 80 mK as a function of voltages applied to the two nearest side gates  $V_{G1}$  and  $V_{G2}$  with  $V_{DS}$  at 1 mV showed insufficient control of the electron occupation within the DQD (Fig. 5.2.2(g)). Sweeping the applied side gate voltages from 0 to 10 V only managed to sweep the QD's single electron occupation across one Coulomb oscillation. This meant that we were unable to effectively control the single electron occupations individually within each QD of the DQD to produce characteristic charge stability diagram of a DQD (see Fig. 2.4(c) and section 2.2). This suggests further optimisation was needed in the device design and fabrication process to enable control of individual QD electron occupations down to the single electron limit.



**Fig. 5.2.2(f)** Contour plot at a base temperature of 80 mK of the DQD source to drain current,  $I_{DS}$ , as a function of top gate voltage,  $V_{TG}$ , and applied side gate voltage,  $V_G$ , with all other gates grounded at  $V_{DS}=1$  mV.



**Fig. 5.2.2(g)** Contour plot at a base temperature of 80 mK of the DQD source to drain current,  $I_{DS}$ , as a function of the applied side gate voltage,  $V_{G1}$  and  $V_{G2}$ , at a source to drain voltage of 1 mV.

### 5.3 Measurements Conclusions

Further to the fabrication conclusions in section 4.4, preliminary electrical characterisations demonstrated repeatable consistent control of the intrinsic DQD channel current via a metal top gate. Clear MOSFET on/off control was observed for over 70% of tested devices with a peak observed electron mobility of up to  $4800 \text{ cm}^2/\text{Vs}$ . In addition, successful repeatable Coulomb oscillations and Coulomb diamonds (see section 2.2) signifying single electron transport and storage are observed in the electrical characteristics of a number of Si DQDs at a base temperature of 80 mK. Here, little hysteresis was observed during forward and reverse sweeps of the top gate control of DQD channel conductance which resulted in stable single electron Coulomb oscillation measurements that did not drift with time. From the measurement data of a DQD device, the charging energy of each QD was extracted to give QD dimensions of  $\sim 25 \text{ nm}$ . Effective control across multiple Coulomb oscillations with both the top gate and side gates signifies single electron tunnelling. The combination of the above measurements and the fabrication results provides an effective indication on the viability of our fabrication process and DQD system for single electron manipulation.

However, despite the clear observation of single electron turnstile operations in a number of devices, measurements did indicate a few weaknesses in the performance of fabricated devices. Firstly, the side gates were insufficiently coupled to the DQD to effectively control

the QDs' individual electron occupation and reduce the electron occupancy down to the single electron limit. In addition, single electron turnstile operation in one DQD system had no measureable effect on the current through the other, suggesting further design optimisation is needed for charge detection. Adjustments in the form of closer DQD to DQD separations and reduced side gate to DQD distances could have helped to improve device characteristics and measurement results. Another factor which affected sensitivity between side gates and QDs could be that the 17 nm SiO<sub>2</sub> which is formed around the device structure from thermal oxidation may be too much. A pattern dependent oxidation processes [41] means that different parts of our device oxidises at different rate and the tip of the effective side gate may be further than we expect from the QDs. In addition, the device's interlayer SiO<sub>2</sub> between the SOI structure and Al top gate may not be thick enough and some Al is actually protruding in between the nanowires and side gates. This would effectively screen any electrostatic interactions we want to apply and reduce the control of side gates and DQD to DQD sensitivity. Despite all this however, many of the parameters mentioned are adjustable during the fabrication process and can be pragmatically optimised through experimentation.

One of the other aims of our device measurement was to obtain RF characterisations of the device as this provides for a much faster means of device measurement. However, through measurement, it was found that the size of the top gate and its capacitance to the source was unfortunately too large to allow for any RF electrometry measurements as potential RF signals at our operating frequency of 200 MHz to 3GHz would leak from the source into the top gate. This can be solved via implementing a smaller top gate and intrinsic SOI nanostructure region to maximize the cut off frequency of the device. However, current photolithography based fabrication steps prevent this due to a minimum 1  $\mu$ m alignment error present for lithography.

The advantage of RF measurement techniques [51] is that in combination with a SET, they offer much higher sensitivity in single electron turnstile detection compared to D.C. measurements. In addition, using RF to realise single-shot measurements of the qubits suppresses unwanted back-action from the electrometer and improve decoherence time of the qubits.

Therefore steps within the proposed fabrication process need to be further improved to overcome many of the issues to do with device performance. These are explored and addressed in the next section.

## 5.4 Fabrication process improvements and further optimisations

The previous sections discussed some of the issues in device performance associated with our approach to VLSI fabrication of SOI based DQDs. Although results were encouraging and demonstrated the viability of our platform in potentially enabling single electron spin manipulations on a large scale, much could be done to the design and fabrication to improve device performance and electrical characteristics. The section below presents our most recent work towards the achievement of this goal followed by further measurement results.

### 5.4.1 *Lithography updates*

In order to increase the chance of performing RF reflectometry characterisations of our device (which allows for quicker characterisations of single electron operations than D.C.), the top gate dimensions need to be reduced (and in turn, the intrinsic SOI region of the device) to minimise its capacitive coupling to the DQD's source and maximise the device's cut-off frequency. Since the dopant diffuses up to 200 nm under the dopant diffusion mask, the minimum size that this mask can be is around 1  $\mu\text{m}$  to ensure both QDs within each DQD are intrinsic in nature. As mentioned previously, photolithography restricts the minimum top gate and doping mask sizes because interlayer alignment has a minimum error of 1  $\mu\text{m}$ . Therefore, in order to overcome this, we proposed that all photolithography based processes be transferred to e-beam lithography processes. This would enable a huge advancement in the reduction of device lithography alignment error from 1  $\mu\text{m}$  to a minimal 5 nm and in turn, allow for much smaller device dopant diffusion mask, interlayer  $\text{SiO}_2$  and top gate designs as well as greater accuracy in the alignment of Al contact pads and tracks.

To enable this process transfer, we had to use a different type of negative tone resist to AZ2070 that was electron sensitive. We therefore migrated to a UVN30 resist based process for defining the dopant diffusion mask and interlayer  $\text{SiO}_2$ . This was chosen because it is an economical alternative to HSQ resist and also provides a thicker sacrificial resist layer during pattern transfer process. However, through numerous exposure trials, UVN30 resist was observed to have very poor adhesion with  $\text{SiO}_2$  due to our small dopant diffusion mask designs. Therefore this presented a challenge when trying to reproduce an accurately aligned pattern transfer process after resist development. The reason behind this was because  $\text{SiO}_2$  has a relatively hydrophilic surface whereas the UVN30 resist was much more hydrophobic. Therefore a mismatch in surface energy meant that any water vapour condensation on the  $\text{SiO}_2$  surface just before coating with UVN30 would result in poor adhesion between the two.

This was observed despite multiple attempts to extensively dehydrate the sample surface before resist coating using both ovens and hot plates.

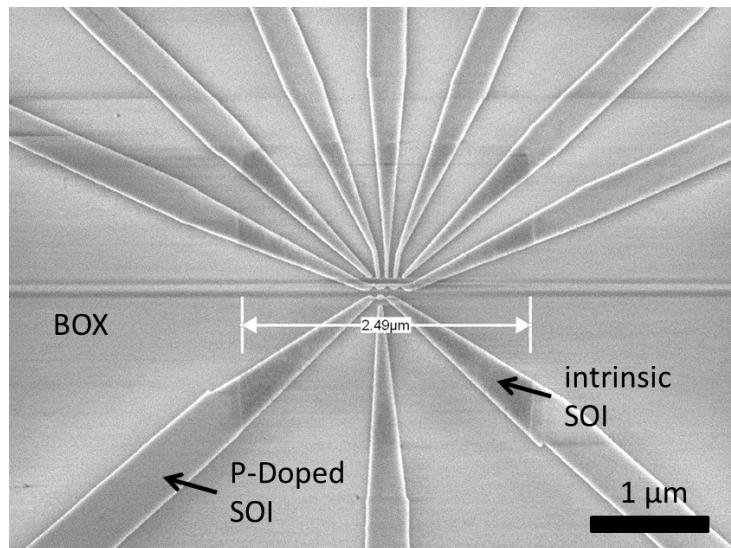
To overcome this issue, a novel hexamethyldisilazane (HMDS) vapour coating process for UVN 30 resist was developed. HMDS is a widely used alkylsilane resist adhesion promotor. It reacts with water on a sample surface, producing gases NH<sub>3</sub>, oxygen, and inert hexamethyldisilazane compounds. This reaction effectively removes OH groups on the surface to create a chemically pure dehydrated surface. The HMDS then reacts with O<sub>2</sub> to form trimethylsilyl (Si(CH<sub>3</sub>)<sub>3</sub>) oxide species that are chemically bound to cover the sample surface. The result of these two reactions is a hydrophobic sample surface with a surface energy comparable to the resist surface energy, leading to excellent resist adhesion to the oxide sample surface [47].

HMDS is most often applied by liquid coating and thus priming a sample before resist coating. However results showed that this didn't improve the adhesion between UVN30 and the sample surface after lithography and development. Therefore, instead we vapour coated our sample for 3 min (via using enclosed beakers) after sample dehydration and PECVD of SiO<sub>2</sub> on our sample (see section 4.3.4 for preceding fabrication steps). This was seen to give far superior adhesion of UVN30 resist to SiO<sub>2</sub> with every single dopant diffusion mask for each device observable after e-beam lithography and resist development.

After HMDS coating, UVN30 negative electron sensitive resist is then spun on the sample at 4000 rpm and baked at 110 °C for 1 min to form an ~300 nm layer (which is a sufficiently thick mask during RIE to etch around 100 nm of SiO<sub>2</sub> for the dopant diffusion mask and 130 nm for the interlayer device SiO<sub>2</sub>). After e-beam exposure of the 1 μm dopant diffusion mask pattern with a dose of 56 μC/cm<sup>2</sup> (spot size of 25 nm), the resist is baked at 110 °C for 1 min and developed in microposit® MFCD-26 developer for 1 min. The fabrication then follows the same as that in section 4.3.4. This process also replaces the lithography step for defining the device interlayer SiO<sub>2</sub> in section 4.3.7.

The only disadvantage of this transfer to an e-beam process is the write and exposure time which takes 1 hour longer than photolithography. However, the better alignment accuracy obtained (which potentially increases fabrication yield) as well as the potential time saved during measurement via the possibility of RF characterisations significantly outweighs this. Fig. 5.4.1(a) shows an SEM of the degree of alignment between the intrinsic SOI region and the etched device (a more advanced design is used (see section below) as a result of improvements to the device lithography process). The intrinsic SOI region here was designed

to be  $\sim 2.5 \mu\text{m}$  - a number of different sized doping masks were used to allow for the parallel fabrication of devices with different levels of doping and top gate sizes. As can be seen, the level of alignment here is extremely accurate with the nanostructure right at the centre of the intrinsic region as designed. It's also interesting to note that the intrinsic SOI region can be seen to be a different shade of grey compared to the phosphorus doped SOI due to their differences in conductance.



**Fig. 5.4.1(a)** SEM of an etched device nanostructure. There is a clear contrast between the  $2.49 \mu\text{m}$  wide intrinsic SOI square and the doped SOI device tapers. This contrast is an indication of the different levels of phosphorus doping in the SOI.

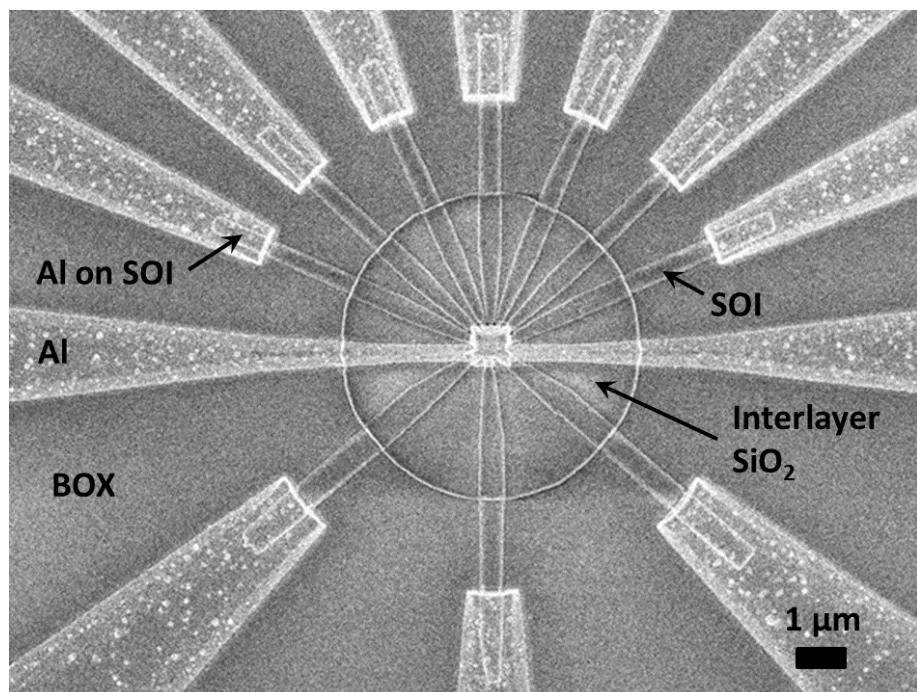
In order to transfer the lift off process to define the top gate and device's metallised contacts to an e-beam process (replacing the photolithography process in section 4.3.8), we decided to used PMMA/MMA (Para-Methoxymethamphetamine/methyl methacrylate) bilayer positive electron sensitive resist because of the relatively greater resist thickness this provides to make the lift off process more reliable and quicker to perform.

For this, the sample is first dehydrated at  $210^\circ\text{C}$  for 30 min and then coated with PMMA resist spun at 5000 rpm and baked at  $150^\circ\text{C}$  for 70 secs. MMA resist is then spun on this at 5000 rpm and baked at  $180^\circ\text{C}$  for 70 secs. As this forms a 350 nm thick layer, it is sufficient to lift off around 180 nm of Al in acetone or NMP (N-Methyl-2-pyrrolidone).

However, it was observed that deposited Al thicknesses of greater than 200 nm was difficult to lift off. This there does means that our top gate with a thickness of 180 nm will limit the gate oxide thickness to around 130 nm, or else there is increased risk that the track (which steps up from the BOX to the top of the gate oxide) from the top gate to the contact pad may break and fail from electron-migration effects [52].

To further increase the potential for RF characterisations, we changed the exposure method for the SOI device structure from both a fine and coarse beam condition exposure (originally to expose the device nanostructure and coarse patterns respectively) to a fine beam only exposure (Fig. 5.4.1(b)). This means that only the designs for the nanostructure and nearby tapers are exposed and etched into the SOI.

The advance here is that it reduces both the e-beam write time as well as the source to drain resistance of the device. This allows 144 devices to be written in just 55 min and therefore reduced costs arising from e-beam usage time. The nanostructure is enlarged to overlap with the aluminium layer to form good Ohmic contact with the overall source to drain resistance being lower than before.

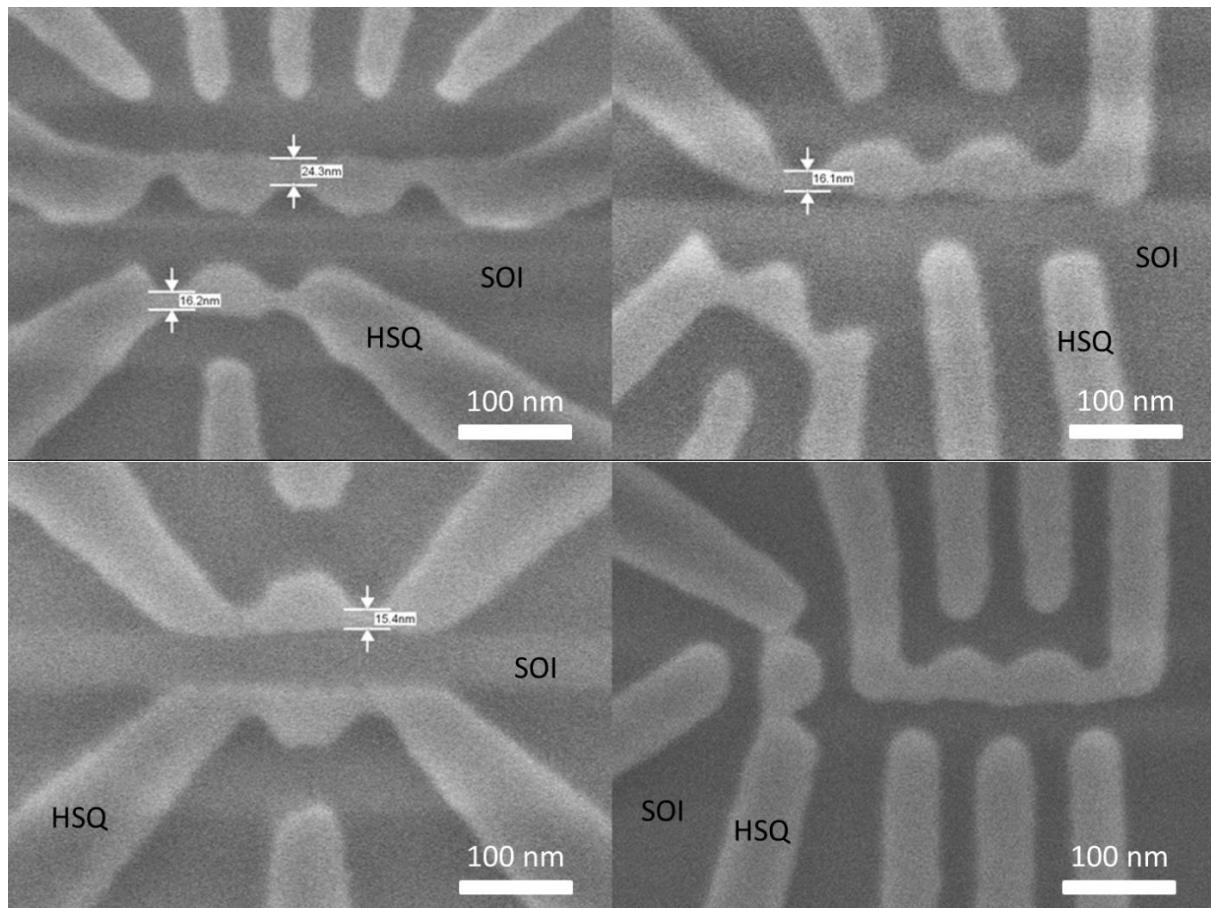


**Fig. 5.4.1(b)** SEM of a finalised device with only the nanostructure and nearby tapers defined for the SOI layer. The top gate and intrinsic SOI region here is only around 1  $\mu\text{m}$  in size.

#### 5.4.2 Device lithography updates

To address the issue of inadequate device sensitivity and ineffective side gate control, we migrated to using HSQ with a 2% concentration rather than 4% to allow for even higher realisable resolutions in e-beam lithography. The resist coating process is the same as in section 4.3.5 except due to the lower HSQ concentration, a resultant 25 nm layer is spun on the sample. This is still an acceptable thickness for RIE pattern transfer into the SOI given the etching selectively shown previously in section 4.3.5.

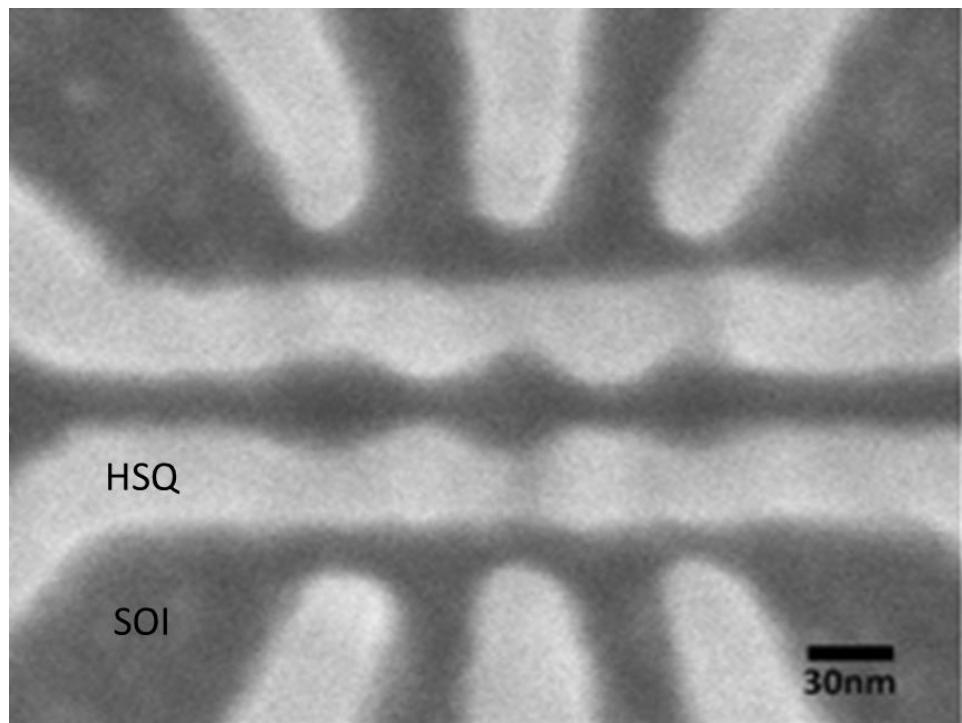
With this new resist, extensive dose testing demonstrated a significant increase in the density of structures we could achieve in addition to reduced dimensionality of device components. The accurate realisation of updated designs with up to 5 side gates was achievable and with down to 14 nm realisation in QD to side gate separation distances (See Fig. 5.4.2(a-b)). A range of e-beam doses between  $2600\mu\text{C}/\text{cm}^2$  to  $3200\mu\text{C}/\text{cm}^2$  was found to be able to accurately realise these more complex nanoscale device patterns. These should enable greater capacitive coupling between DQDs and between DQD and side gates to allow greater control (via more side gates) and detection of single electrons within a QD.



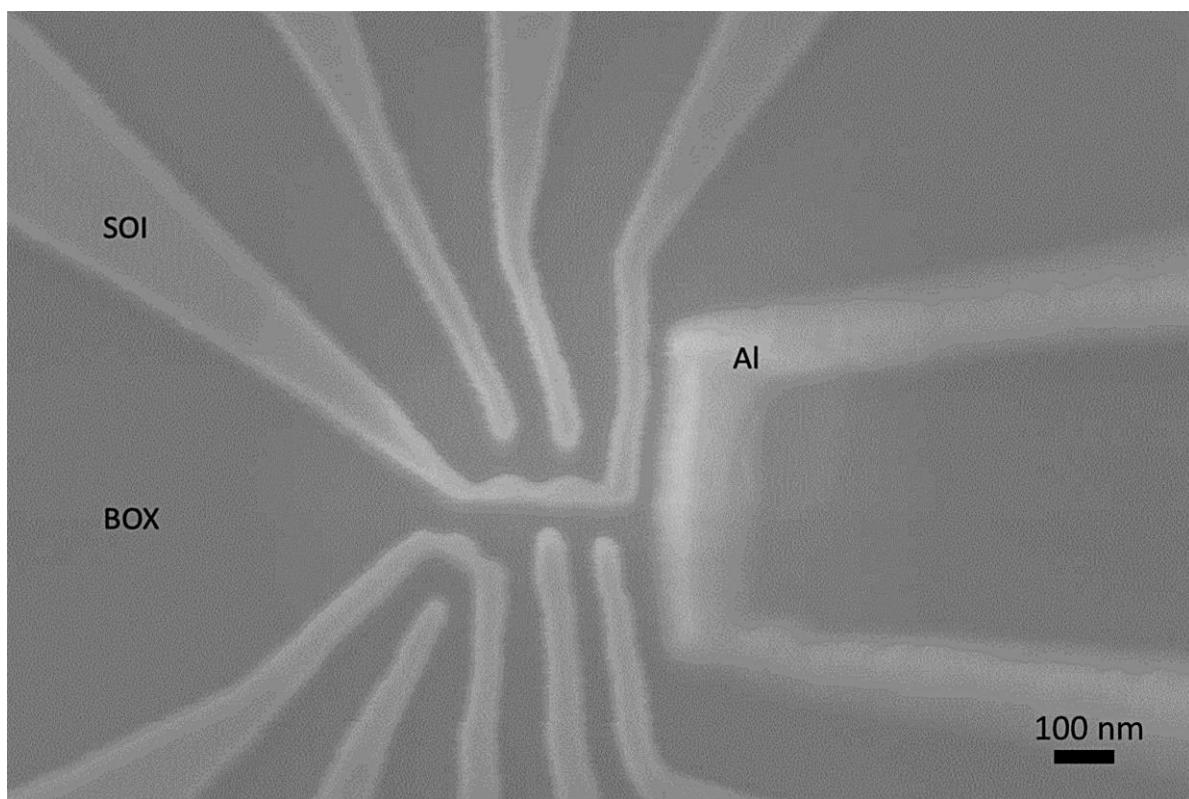
**Fig. 5.4.2(a)** SEM of a few successful HSQ e-beam exposure of DQD nanostructure with increased design density on SOI at a dose of  $2600\mu\text{C}/\text{cm}^2$ .

Due to the increased lithography capability of the new process, Fig. 5.4.2(c) below shows a recent SEM of a nanostructure design with room for the potential deposition of an aluminium stripline to the right of the DQD (The same SOI device design as that shown in the top right corner of Fig. 5.4.2(a)) as well as deposition of a potential nanomagnet to the left for integrated spin qubit operations. The hope here is to enable the generation of oscillating magnetic fields via an A.C. current through the stripline in order to demonstrate coherent

rotation and control of single electron spins. Simulations of the potential performance of this stripline was carried out with the details contained in Appendix A.



**Fig. 5.4.2(b)** SEM of a successful HSQ e-beam exposure of DQD nanostructure with three side gates on SOI at a dose of  $2600\mu\text{C}/\text{cm}^2$ . The DQD to side gate distance is down to 14 nm.



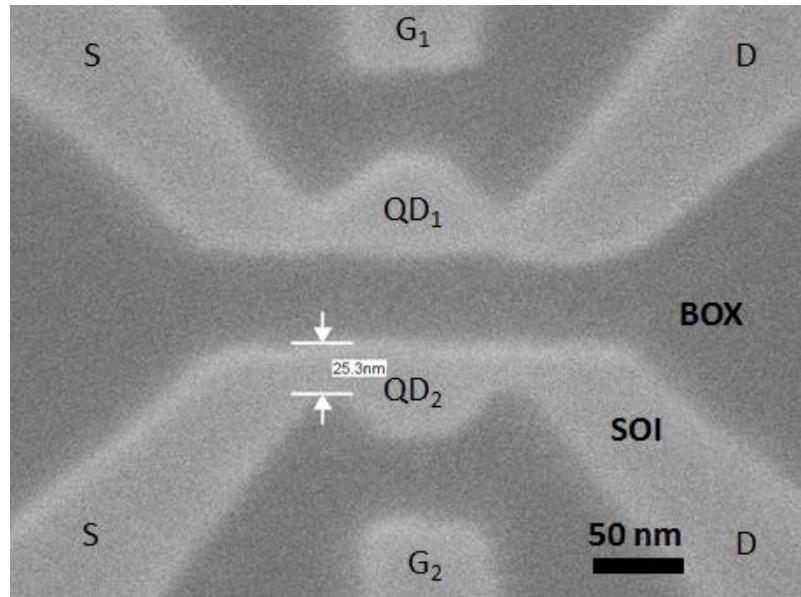
**Fig. 5.4.2(c)** SEM of a device nanostructure before top gate formation with an aluminium stripline to the right of the DQD.

## 5.5 Device characterisations of an updated process

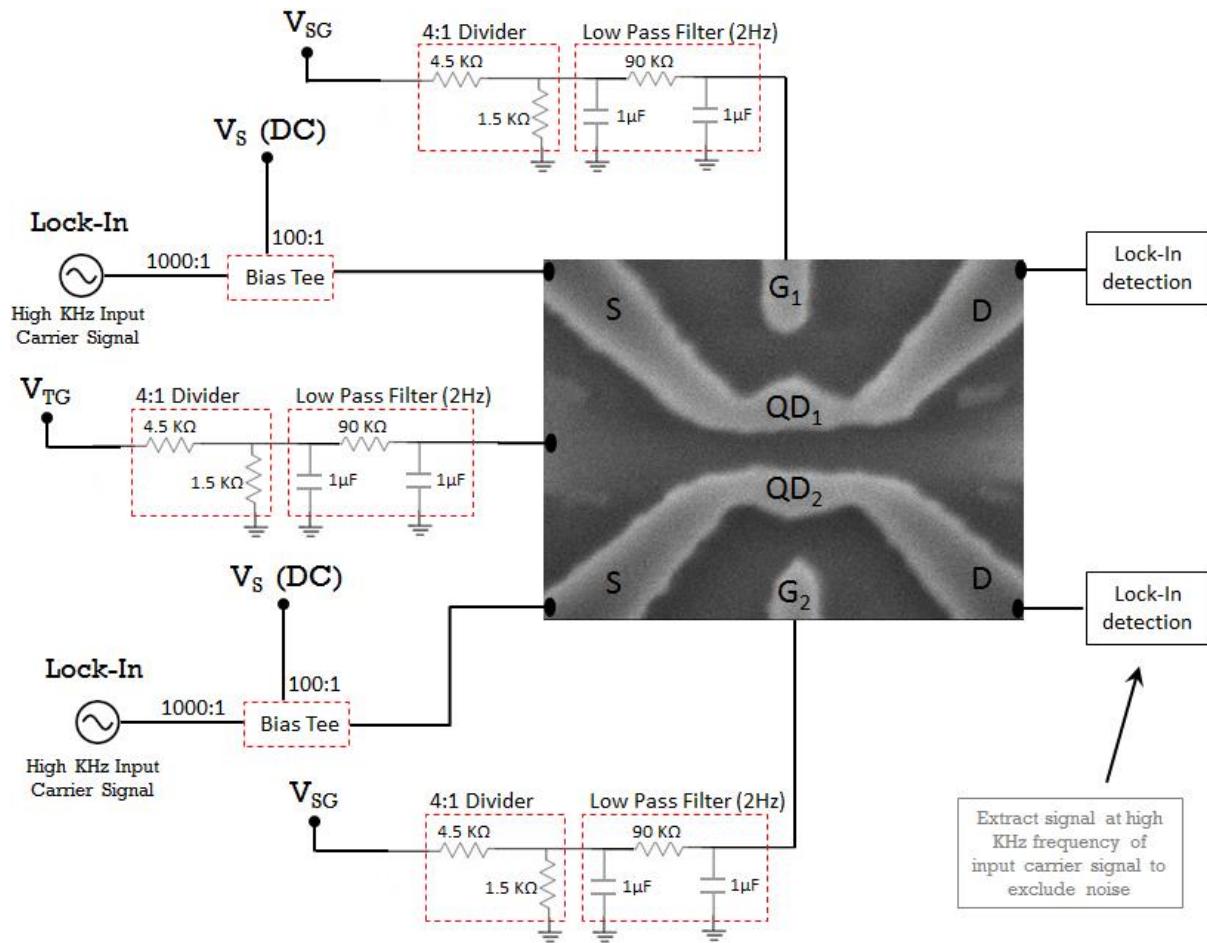
With the updates to our proposed fabrication process, electrical characterisations of the newly fabricated devices were then performed in order to measure the improvements in device performance as well as fabrication results. Room temperature measurements demonstrated similar characteristics to that observed previously in section 5.2.1 however cryogenic electrical measurements demonstrated noticeable improvements to device sensitivity and performance. Below we concentrate on measurements of one device design out of the number of different designs fabricated (see Fig. 5.4.2(a)) to understand fundamental device performance improvements and the future potential of our fabrication process in realising repeatable single electron qubit operations.

### 5.5.1 Dual QD Device Characterisations

The devices which measurements were concentrated on started with the simplest dual single QD design (Fig. 5.5.1(a)) with an aim of understanding the fundamental device performance before moving onto more complex QD structures. The same measurement setup to that in section 5.2.2 was utilised with the device connected as shown in Fig. 5.5.1(b).

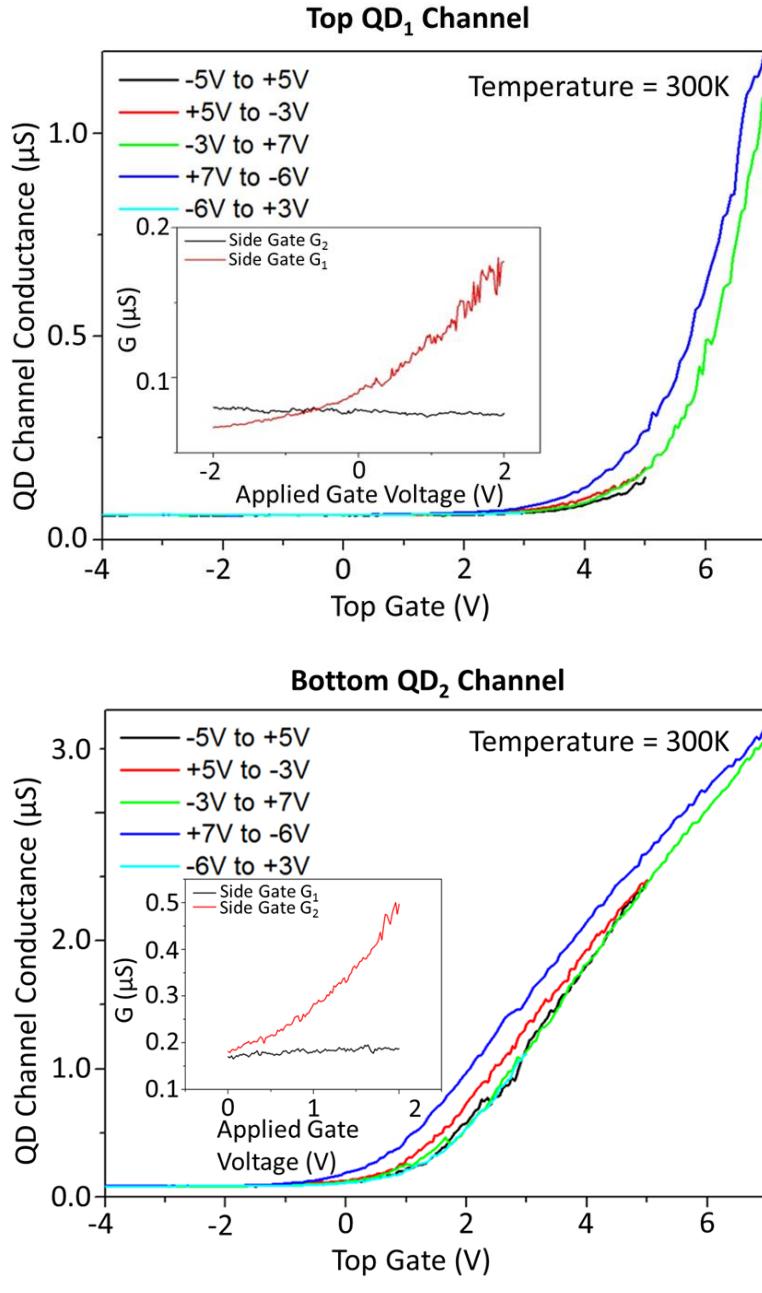


**Fig. 5.5.1(a)** SEM image of a fabricated dual QD device before device top gate and interlayer SiO<sub>2</sub> formation. QD<sub>1</sub> and <sub>2</sub> label the QDs of each channel and G<sub>1</sub> and <sub>2</sub> are their respective closest side gates for electrostatic control of single electron occupation. S and D label the source and drain of the QD channels.



**Fig. 5.5.1(b)** A diagram of the device connections, filters and voltage dividers which were used to perform low temperature measurements of our device. The capacitance and resistance values of the filters were set depending on the resistance of the QD channel of the device.

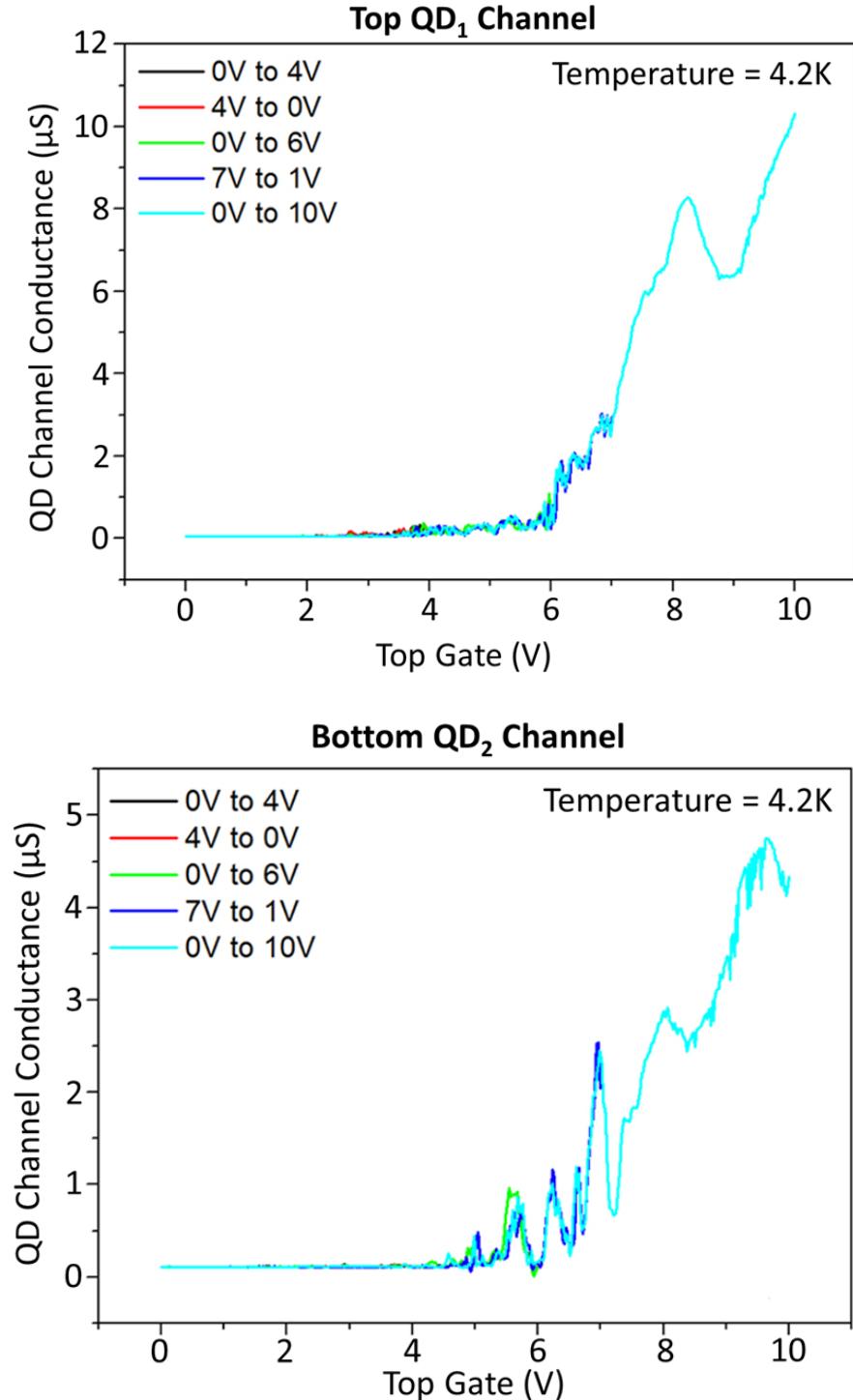
Via use of the above measurement setup, measurements were performed on a number of devices fabricated across a chip. Room temperature characterisations of the device conductance,  $G$ , as a function of the applied top gate voltage,  $V_{TG}$ , demonstrated clear repeatable control over the QD channel conductance for both the top and bottom channel of the device. The top gate was clearly able to turn the QD channel conductance on and off at operating voltages. Fig. 5.5.1(c) shows such a measurement for the top and bottom channel of a particular device over a range of different sweeps of the  $V_{TG}$ . It can be seen that the threshold voltage shifts slightly for  $V_{TG}$  sweeps across different voltage ranges and this is again most likely due to the floating charges discussed previously in section 5.2.1 which is causing the hysteresis. The threshold voltage is also slightly different between the top and bottom channels due to fixed charges present during deposition of the interlayer  $\text{SiO}_2$  layer.



**Fig. 5.5.1(c)** Top: The channel conductance,  $G$ , of the top QD (QD<sub>1</sub>) of our device as a function of applied top gate voltage,  $V_{TG}$ , through different voltage range sweeps with all other device components grounded at room temperature. The insert shows the response of the same channel conductance as a function of the applied voltage to side gates G<sub>1</sub> and G<sub>2</sub>. Bottom: The same as the top graph except the data is for the bottom QD of our device (QD<sub>2</sub>).

What is important here however is the smaller graph contained within the characteristics for the top and bottom channels which shows the response of the respective channel's conductance as a function of the applied side gate voltages to G<sub>1</sub> and G<sub>2</sub>. These characteristics demonstrate a clear improvement in the sensitivity of the QD channel conductance to the applied side gate voltages over the previously fabricated devices in section 5.2. The advantage here is the ability to now individually control single electron turnstile operations and Coulomb oscillations across the two QDs using the side gates rather than the top gate. Additionally, it

can be seen from the smaller plots in Fig. 5.5.1(c) that there is minimal cross effect between a QD channel and its non-corresponding side gate (e.g.  $G_2$  and  $QD_1$ ). This means we can accurately control a QD's single electron occupation using its closest side gate without worrying about any significant cross capacitive coupling to the other channel – simplifying controlled device operations.

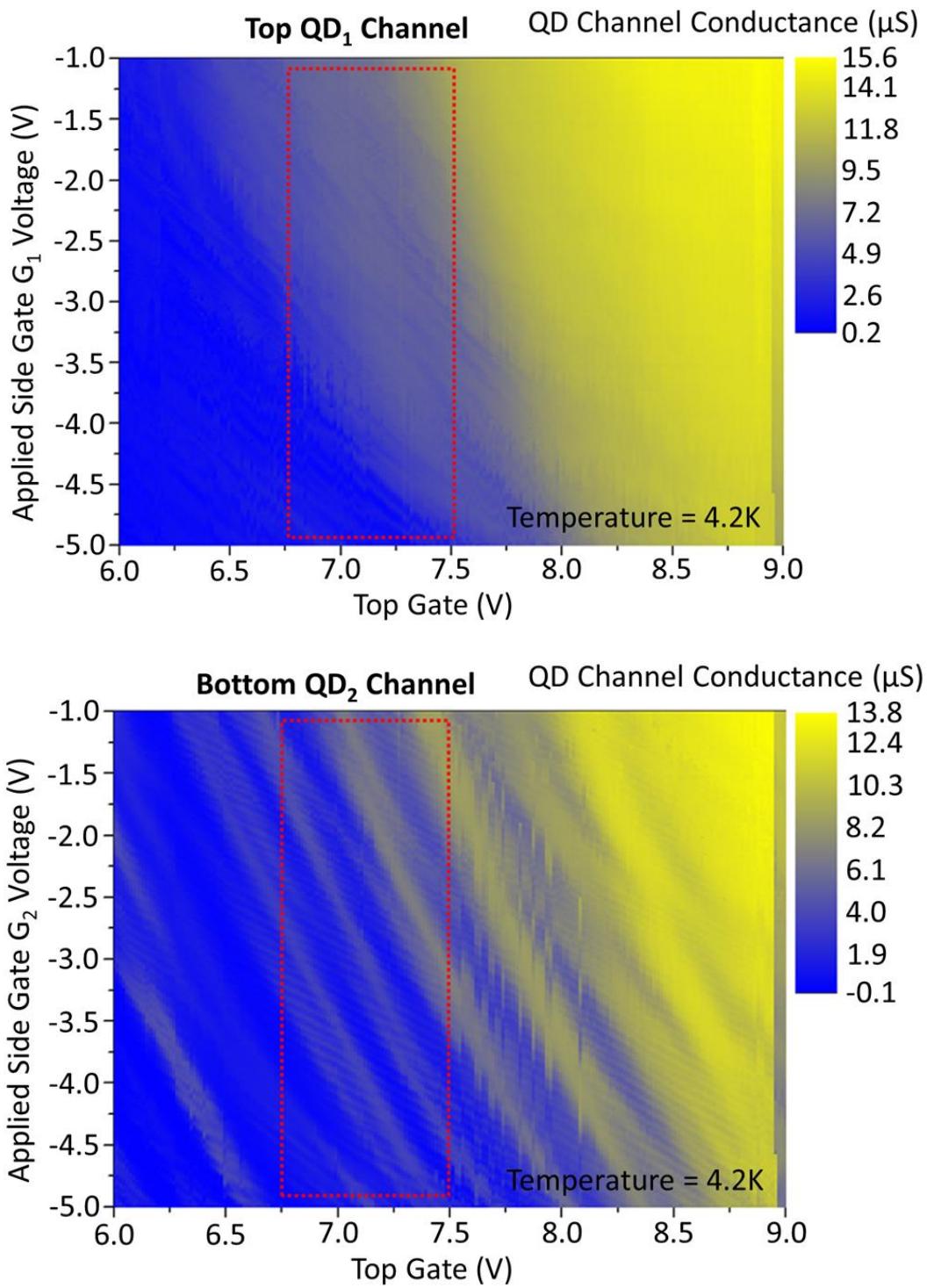


**Fig. 5.5.1(d)** Top: The channel conductance,  $G$ , of the top QD ( $QD_1$ ) of our device as a function of applied top gate voltage,  $V_{TG}$ , through different voltage range sweeps with all other device components grounded at 4.2K. Bottom: The same as the top graph except the data is for the bottom QD of our device ( $QD_2$ ).

A repeat of the measurement in Fig. 5.5.1(c) at a cryogenic temperature (see Fig. 5.5.1(d)) of 4.2K with all side gates grounded demonstrated a clear reduction in the shifting of the top gate threshold voltage and hysteresis which was observed at room temperature when sweeping across different top gate voltage ranges. This concurs with the measurements observed previously in section 5.2.2 and indicates the freezing out of mobile charges which were present at room temperatures. This means that our device will be capable of supporting stable Coulomb oscillation and single electron turnstile measurements which will not drift in voltage space with time which is often a problem for QD devices.

It can be seen from Fig. 5.5.1(d) however that near the threshold voltage, numerous oscillations in the QD channel conductance can be seen and these are due to parasitic QDs formed in the source/drain leads as the 2DEG of the device begins to get induced by the top gate. These are sample dependent since they are mainly determined by traps/defects at the Si/SiO<sub>2</sub> interface, however mostly disappear when operating at higher top gate voltages.

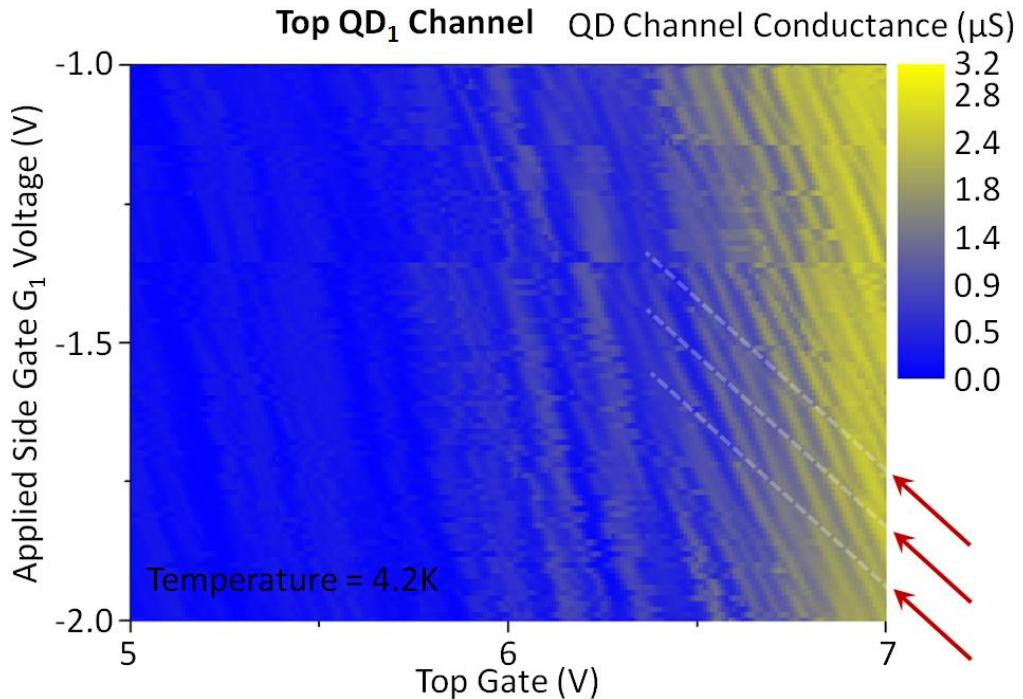
By plotting each device's top and bottom QD channel conductance (QD<sub>1</sub> and QD<sub>2</sub>) as a function of both their respective applied side gate voltage, V<sub>G1</sub> and V<sub>G2</sub>, and top gate voltages, V<sub>TG</sub>, we can obtain a plot similar to that previously in Fig. 5.2.2(f) of the Coulomb oscillations through each of the QDs of the device. This can be seen in Fig. 5.5.1(e) for QD<sub>1</sub> and QD<sub>2</sub> of the fabricated dual QD devices where with this particular device the threshold voltage was similar for both channels such that they could both simultaneously display single electron transport. The results show simultaneous individual effective control of the QD single electron occupations via their respective side gates. However, as observed earlier in Fig. 5.5.1(d), the presence of parasitic dots is clearly present in the operational regions where Coulomb oscillations are observable where we have gradual shifts in the QD channel conductance. Ideally we would wish to operate at sufficiently high V<sub>TG</sub> such that there is a homogeneous 2DEG in the SOI structure however the effect of the side gates decrease for higher values of V<sub>TG</sub>. This therefore indicates the need to realise devices with smaller channel constrictions than that fabricated in Fig. 5.5.1(a) to allow for device operations with a more homogeneous SOI 2DEG. In addition, the operational region outlined by the dotted red box in Fig. 5.5.1(e) seemed to vary from device to device depending on the density of trapped charges within the device structure. This leads to difficulties in successfully demonstrating detection of single electron turnstile operations from one QD of the other as the two QD channels of each device may not be simultaneously in the operational region for Coulomb oscillation to be detectable (since we only have one top gate controlling both channels).



**Fig. 5.5.1(e)** Top: The channel conductance,  $G$ , of the top QD (QD<sub>1</sub>) of our device, as a function of applied top gate voltage,  $V_{TG}$ , and applied voltage,  $V_{G1}$ , to side gate G<sub>1</sub> at 4.2K. The dotted red box approximately outlines the operational region in voltage space in which Coulomb oscillations can be clearly detected. Bottom: The same as the top graph except the data is for the bottom QD channel of our device (QD<sub>2</sub>). The top and bottom QD device channels are measured simultaneously to produce the two graphs.

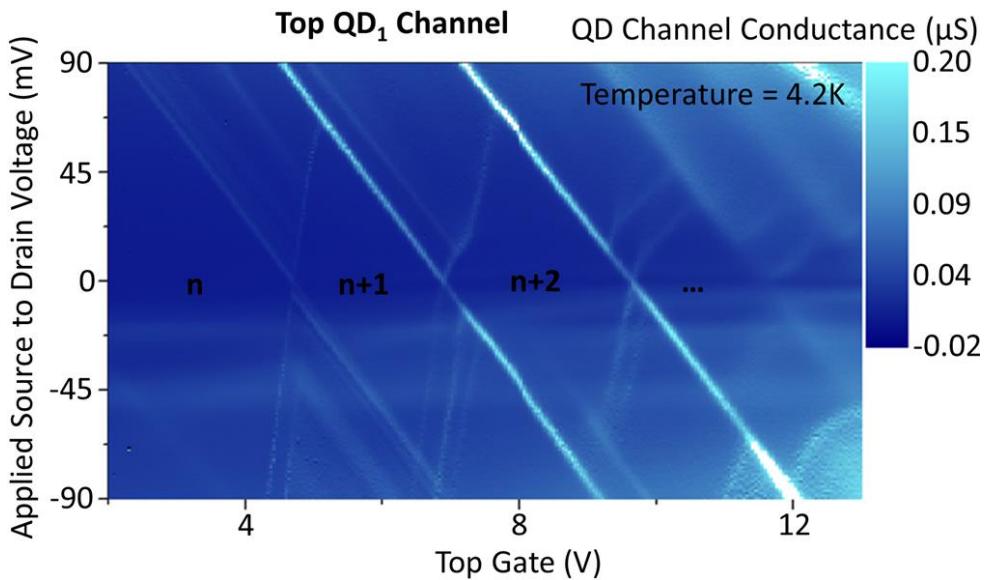
We did however observe some evidence of charge detection which may be from one QD channel of single electron turnstile operations in the other. This can be seen in Fig. 5.5.1(f) where by simultaneously sweeping the applied voltages on the top gate,  $V_{TG}$ , and side gates

$G_1$  and  $G_2$  to control Coulomb oscillations in  $QD_1$  and  $QD_2$ , we see periodic shifts in the Coulomb oscillations through  $QD_1$  as they occur in  $QD_2$ . The periodicity of this shift matches the periodicity observed in the Coulomb oscillations in  $QD_2$  given their dimensional separations and the expected capacitive coupling between the two QDs. The graph is slightly noisier than those in Fig. 5.5.1(e) because the measurement here was performed prior to the use of filters in the experimental setup in Fig. 5.5.1(b).



**Fig. 5.5.1(f)** A plot of the channel conductance,  $G$ , through the top QD ( $QD_1$ ) of our device, as a function of applied top gate voltage,  $V_{TG}$ , and applied voltage,  $V_{G1}$ , to side gate  $G_1$  at 4.2K. Here, the bottom QD device channel ( $QD_2$ ) had a sweeping voltage,  $V_{G2}$ , applied to its respective side gate,  $G_2$ , at same time to induce single electron turnstile operations through  $QD_2$ . The observed periodic shifts (red arrows and dotted white lines) in the Coulomb oscillations through  $QD_1$  in the graph suggest detection of sequential single electrons tunnelling onto  $QD_2$ .

One of the key advantages of our fabrication process is the ability to accurately control the QD dimensions not only by e-beam lithography, but also via adjusting the thickness of the thermal oxide grown around the lithographically defined SOI QDs. One example of this is an instance where a chip of devices was fabricated with around a 17 nm thick  $SiO_2$  thermally grown around the SOI devices. This led to the realisation of extremely small QDs with characteristics that demonstrate a level of clarity within Coulomb blockade diamonds not seen before in literature on SOI based QDs at a temperature of 4.2K. Fig. 5.5.1(g) shows one such example where a single QD ( $QD_1$ ) channel's conductance,  $G$ , is plotted as a function of the applied top gate voltages,  $V_{TG}$ , and source to drain voltage,  $V_{SD}$ , with all other side gates grounded at a temperature of 4.2K.

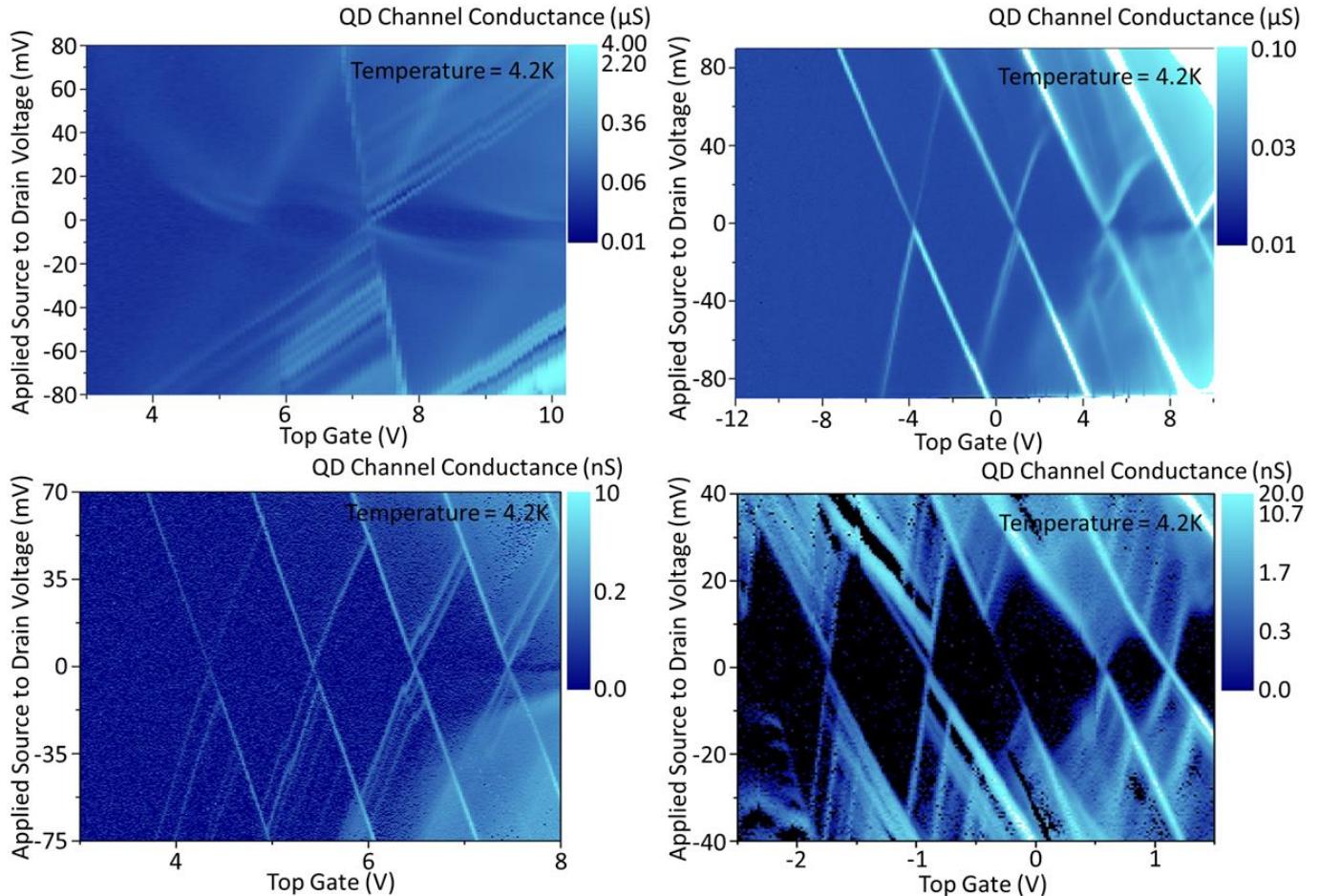


**Fig. 5.5.1(g)** A plot of the channel conductance,  $G$ , through the top  $QD_1$  of our device, as a function of applied top gate voltage,  $V_{TG}$ , and applied source to drain voltage,  $V_{SD}$ , at 4.2K with all other side gates grounded.

From Fig. 5.5.1(g), we can clearly see the presence of distinct Coulomb blockade diamonds (see section 2.2 for theory) much like that observed previously in section 5.2.2 and in Fig. 5.2.2(e). A core improvement in this result however is the clarity of the Coulomb diamonds which can be observed. More importantly, the Coulomb diamonds are very clearly defined with sharp corners unlike the previous result in Fig. 5.2.2(e), which indicates very clean and noise free single QD characteristics. “ $n$ ” in Fig. 5.5.1(g) represents the number of electrons stored within the QD when transport through it is blocked due to Coulomb blockade. The widening of the Coulomb blockade diamond peaks in  $V_{SD}$  (at the electron occupation “ $n$ ”) gives us an encouraging indication that we’re in the very low few electron occupation region of the QD. This is key to paving the way towards precise control of single electron spin manipulations in intrinsic SOI based QDs. An importance milestone achieved here is our ability to control the QD’s single electron turnstile operations in a very precise and defined manner via using either the top gate or side gates due to the size of the Coulomb diamonds in voltage space (which is a result of the small dimension of the QD). In fact, across a fabricated chip, many devices were observed to demonstrate similar characteristics with our fabrication process. A few of these are shown in Fig. 5.5.1(h).

A result imposed by the use of very small QDs however is the increase in channel resistance which was observed to increase from an expected few  $100\text{K}\Omega$  to over  $10\text{ M}\Omega$  which limits our ability to perform RF reflectometry device characterisations. Through an analysis similar to that used in section 5.2.2 by measuring the applied source to drain voltage at the vertex of the largest Coulomb blockade diamond to extract the charging energy of the QD and

assuming a spherical QD capacitor model, we demonstrated the fabrication of a number of QDs ranging from just 10.6 nm to over 20 nm. This can be controlled precisely via both the e-beam lithography of the SOI device structures as well as in the thermal dry oxidation of devices to reduce their size.



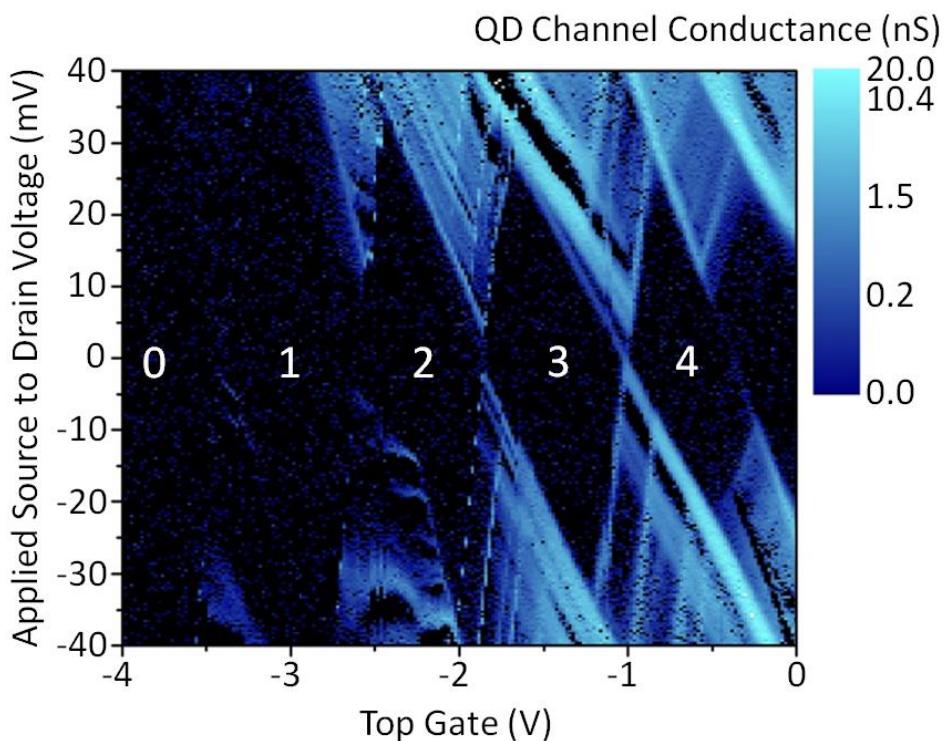
**Fig. 5.5.1(h)** Plots of the channel conductance,  $G$ , through the top  $\text{QD}_1$  of our designed device, as a function of applied top gate voltage,  $V_{\text{TG}}$ , and applied source to drain voltage,  $V_{\text{SD}}$ , at 4.2K with all other side gates grounded for 4 different fabricated QD devices.

An additional but very important point of interest in the characteristics shown in Fig. 5.5.1(g) and in Fig. 5.5.1(h) is the clear presence and observation of a number of distinct electron excited states of the QD (see section 2.2 and 2.4 for theory) which provide clear evidence that we are in the few electron regime. The excited states are the extra lines in the conducting regions which are parallel to the edges of the Coulomb blockade diamonds. As expected, it can be seen that the number of excited states visible increases for an increased electron occupation in the QDs where the separation in excited state energy levels are wider (in voltage space) for lower QD electron occupations. These excited states have noticeably lower QD single electron charging energy differences than the shift of a full Coulomb blockade

diamond and represents potential electron transport through the QD via additional energy vacant states available as a result of many different multi-electron spin degrees of freedom.

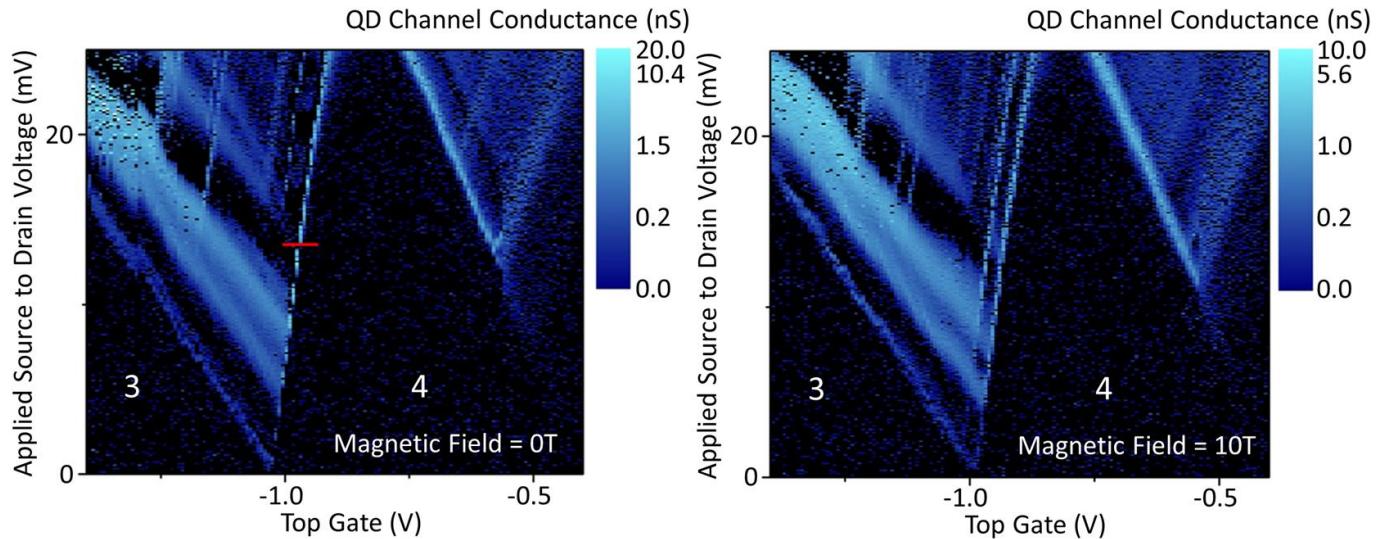
Taking measurements a step further, we investigated the performance of our device under an external magnetic field in an attempt to split many of the excited spin states observed in the Coulomb blockade diamond characteristics of single QD channels. This not only gives us a better understanding of the spin degrees of freedom present in our observed characteristics but also allows us to characterise the dependence of excited spin states on changes in the external magnetic field. This in turn allows us to both identify the spin orientation of electrons within the QDs as well as gain a better idea of the number of electrons actually occupying it.

Fig. 5.5.1(i) shows a plot of the same characteristics for a different QD channel as that demonstrated previously in Fig. 5.5.1(g) and Fig. 5.5.1(h) however this time we label the Coulomb blockade diamonds with what subsequent results in Fig. 5.5.1(j) to Fig. 5.5.1(l) indicate to be no. of electrons occupying the QD.

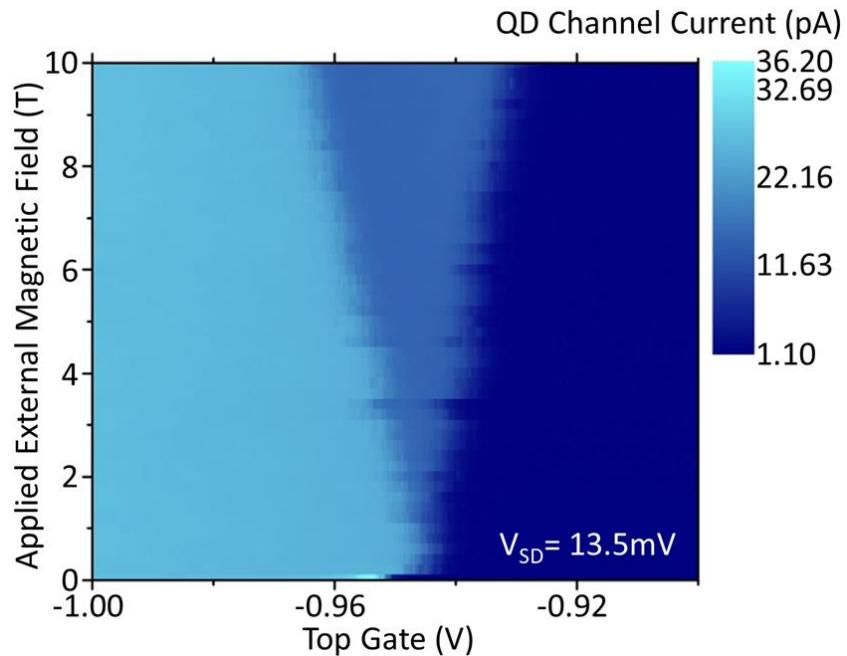


**Fig. 5.5.1(i)** A plot of the channel conductance,  $G$ , through the top QD<sub>1</sub> of a device, as a function of applied top gate voltage,  $V_{TG}$ , and applied source to drain voltage,  $V_{SD}$ , at 4.2K with all other side gates grounded. The white numbers are what subsequent measurements indicate to be the number of electrons present within the QD when transport through it is blocked due to Coulomb blockade (i.e. within each Coulomb blockade diamond).

Through applying an external magnetic field,  $B$ , line splitting of the excited states could be clearly seen as degenerate electron spin states become split into states of different energies. This therefore offers an increased no. of distinctive states of different energy which could facilitate single electron transport through a QD. Fig. 5.5.1(j) shows a magnified plot of Fig. 5.5.1(i) around the 3-4 electron occupation transition of the QD with clear signs of line splitting as a magnetic field is applied.

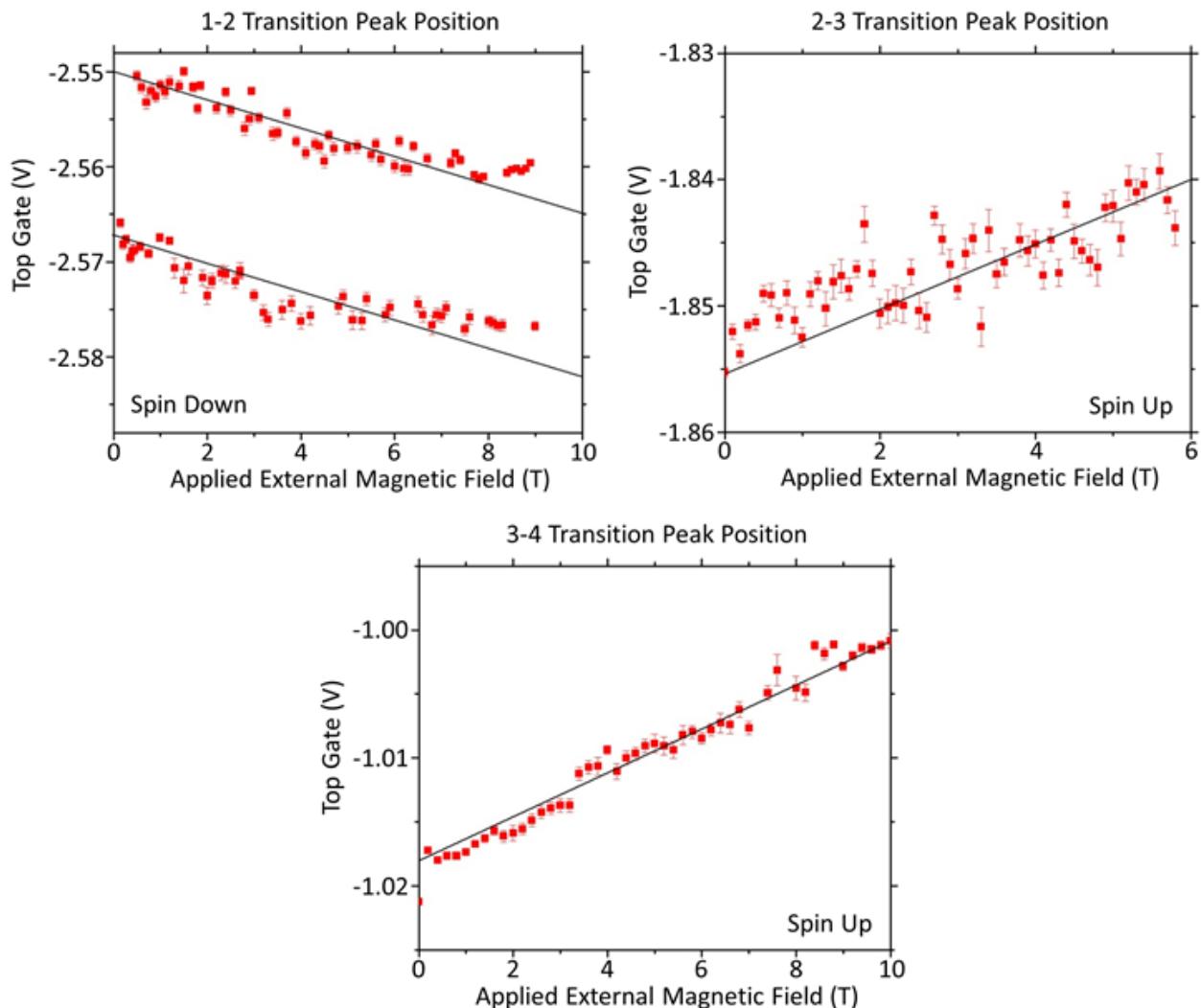


**Fig. 5.5.1(j)** A magnified plot of Fig. 5.5.1(i) around the 3-4 electron QD occupation transition with (Right) and without (Left) an applied external magnetic field,  $B$ .



**Fig. 5.5.1(k)** A plot of the QD channel current,  $I_{SD}$ , across the red line in the left graph of Fig. 5.5.1(j) as a function of the applied external magnetic field,  $B$ , at a temperature of 4.2K. The applied source to drain voltage,  $V_{SD}$ , was 13.5mV.

A plot of the QD channel current across the position of the red line in the left graph of Fig. 5.5.1(j) as a function of the applied external magnetic field,  $B$ , demonstrates the gradual splitting of degenerate electron spin states as an external magnetic field is increased. This is shown in Fig. 5.5.1(k). It is through comparing the gradient of these transitions with that expected from theory that we can gain a better idea of the precise number of electrons present within the QD.



**Fig. 5.5.1(l)** A plot of the value of the applied top gate voltage,  $V_{TG}$ , which gave the peak positions of the 1-2, 2-3 and 3-4 Coulomb blockade diamond transitions as a function of the applied external magnetic field,  $B$ , at 4.2K. The solid black line in each plot outlines the expected relationship from theory ( $\pm 58\mu\text{eV/T}$  for each electron in the QD) given the spin orientation of the last electron to fill the state (which is stated on each plot).

Through analysing the shifts in peak positions of the QD Coulomb blockade diamonds through transitions between the 1-2, 2-3 and 3-4 electron occupation as a function of  $B$ , we obtained the following relationships shown in Fig. 5.5.1(l). The solid black line in each plot outlines the expected relationship from theory ( $\pm 58\mu\text{eV/T}$  for each electron in the QD) given the spin orientation of the last electron to fill the state. The 1-2, 2-3 and 3-4 transitions have

2, 3 and 4 electrons in the QD respectively and the relationships from theory would therefore be expected to be  $\pm 1.16\text{meV/T}$ ,  $\pm 1.74\text{meV/T}$  and  $\pm 2.32\text{meV/T}$  respectively (2, 3 and 4 times that for a single electron).

Given the very good correlation between the observed measurements and theory, the results in Fig. 5.5.1(l) provide an encouraging indication that the electron occupation in our QD are what was labelled in Fig. 5.5.1(i). Therefore, from the results in Fig. 5.5.1(l), we can define the electron spin loading of the first four electrons into the QD as  $\downarrow, \downarrow, \uparrow, \uparrow$  where  $\downarrow$  represents a spin down electron and  $\uparrow$  represents a spin up electron. We were not able to measure the 0-1 electron occupation transition of the QD due to the low measurable current however know this is always a spin down electron (since it always occupies the ground state). The reason why the second electron to enter the QD is a spin  $\downarrow$  is because of the presence of the magnetic field,  $\mathbf{B}$ . In this case, the  $\mathbf{B}$  field interacts with the spin magnetic moment, to produce a “normal Zeeman effect” which shifts the energy states by splitting the energy degeneracy of the spin states. The shift in energy due to this effect is,  $\Delta E = \frac{e}{2m}(\mathbf{L} + 2\mathbf{S}) \cdot \mathbf{B}$ , where  $\mathbf{L}$  is the orbital angular momentum,  $\mathbf{S}$  is the spin angular momentum and  $e$  and  $m$  are the charge and mass of an electron. In the case of a  $\downarrow, \downarrow$  spin configurations (which is one of the triplet states), the total spin angular moment would be  $S = (2 \times -1/2)\hbar = -\hbar$ . For the singlet state  $(\downarrow, \uparrow)$ ,  $S = (-1/2 + 1/2)\hbar = 0$ . Therefore, when these values are inserted into the equation for  $\Delta E$ , the  $\downarrow, \downarrow$  spin configurations provides a lower Zeeman energy shift and is lower in energy because  $\mathbf{L}$  and  $\mathbf{B}$  are the same in both cases. Without the presence of the  $\mathbf{B}$  field, the spin singlet state  $\downarrow, \uparrow$  would be the preferred spin configuration for the first two electrons to enter the QD. In addition, the agreement seen in Fig. 5.5.1(l) between measurements and theoretical expectations indicate that any valley splitting [53] for the electron states of our QDs are smaller than Zeeman splitting induced by the external magnetic field.

These results therefore give us an effective indication of our abilities to control the electron occupation of our fabricated QDs with precision down to the single electron limit for future capabilities in enabling single electron spin manipulations.

## 5.6 Updated process and measurements conclusions

The results from the previous section demonstrated significant advancements in device performance and single electron control in QDs over devices which were fabricated prior to the fabrication process updates. Further to the conclusions outlined previously in section 5.3, many of the issues in device performance associated with our prior approach to VLSI fabrication of SOI based DQDs have been resolved.

Devices now demonstrate effective control over single electron turnstile operations through QDs via using both the electrostatically coupled side gate as well as top gate. This resolves the problem of insensitive side gates observed with devices measured in section 5.3 and enables the independent control of single electron turnstile operations in more than one QD simultaneously. Furthermore, devices characteristics demonstrated a high level of repeatability and stability over time with no sign of drifting in voltage space. This indicated the freezing out of any mobile charges (which were observed at room temperatures) at cryogenic temperatures and is the result of the cleanliness achieved with our fabrication process. In addition, devices which were seen to have two QD channels demonstrating Coulomb oscillations over the same range of applied top gate voltages exhibited signs of detection by one QD channel of the single electron turnstile operations in the other.

However, due to the presence of fixed charges within the devices structures, it was difficult to find devices where both QD channels displayed Coulomb oscillations over the same top gate voltage range in order to demonstrate reproducible charge detection abilities across a chip. This is because the presence of fixed charges in the device structures shifted the threshold voltage for the SOI QD channels by up to 1-2V. This therefore presents a potential area of further work to reduce the level of contamination within the fabrication process to enable cleaner devices free from contaminants and trapped charges.

One of the major points of interest highlighted by the device characterisations was the observation of our fabrication process' ability to realise very small intrinsic Si QDs down to just 10.6 nm. The advantage of this is the unmatched precision in the level of control this enables for control of single electron occupations of the QD at a temperature of 4.2K. It also allows us to very precisely analyse the excited states of electrons occupying QDs in great detail and observe the variations in these excited states with the application of an external magnetic field. This demonstrates a level of clarity within Coulomb blockade diamond characteristics not seen before in literature on SOI based QD. The results here also demonstrate the level of control in QD dimensionality our fabrication process is able achieve, not only through the precision offered by our updated HSQ based e-beam device lithography process but also through optimised control of thermal oxidation around the device structures to reduce QD dimensions. Through characterisations of multiple devices, we demonstrated the fabrication of a number of QDs ranging from just 10.6 nm to over 20 nm.

In addition, clear evidence of splitting of the degenerate QD excited states (due to electron spin degrees of freedom) was observed when devices were measured under an external magnetic field. The level of control in single electron turnstile operations enabled us to

characterise, through magnetic field dependent measurements, the spin orientation of electrons tunnelling into the QD. This spin readout gave us an indication of the number of electrons stored on the QD and in turn, our ability to control the QD with precision down to the single electron limit.

Furthermore, one of the achievements through our updated device lithography process is the ability to realise a variety of complex even higher density QD systems than before. Process optimisation enabled the realisation of DQD structure with up to 5 in plane side gates for independent control of both the QD tunnelling barriers and the QD's single electron occupations. This offers an even greater level of precision and control in QD characteristics which, combined with the parallel and repeatable nature of our fabrication process, offers a fundamental platform for detailed exploration into Si QD characteristics and spin manipulations.

Out of the samples we tested, the best measurement yield we obtained was 69% of all devices fabricated in parallel. This value represents the percentage of QD devices channels that could be switched on and off repeatedly at 4K cryogenic temperatures with a sufficient channel resistances to be able to detect single electron turnstile operations and observe QD Coulomb oscillations characteristics. The devices would've also had to show no observable leakage between any of the device components at the expected operating voltages. As a significant amount of time is required to characterise each device, a statistical analysis of the performance of each device across a chip in terms of their ability to support single electron turnstile operations in a noise free environment was unfortunately not available at the time of submission. However given the parallel nature of our fabrication process and the fully SOI based nature of our device design, the reduced potential for leakage as a result and repeatability observed should mean many of the device structures are capable of supporting single electron operations.

We also attempted RF reflectometry readout of the QD devices however, through measurement, our RF setup showed no clearly detectable resonance with the device when switched on or off. Further investigation may be needed however it may be that the size of the top gate needs to be reduced further to reduce its capacitance to the QD channel's source and drain.

Overall, the combination of the above measurements and fabrication results provides for an effective indication of the ability of our fabrication process to realise and accurately control the dimensions of diversely different, repeatable QD systems in parallel. Importantly, the

realised QD systems demonstrate the required ability to precisely control single electron QDs occupations such that our fabrication process can act as a fundamental platform to further investigations into single electron spins and their manipulations in Si on a large scale. Efforts are currently underway to characterise the more complex DQD device structures (see Fig. 5.4.2(a)) which will hopefully enable the demonstration of dynamic detection of single electron spin relaxation times and spin manipulations from devices fabrication by our VLSI compatible process. The results from the current electrical characterisations presented in section 5.5.1 are currently being submitted for journal publication.

# Chapter 6

## Conclusion and further work

### 6.1 Conclusions

The suitability of SOI as a platform for quantum information processing was investigated in this study. A literature review revealed that a major benefit of silicon based QDs over their conventional GaAs based counterparts is their much longer single electron spin relaxation time  $t_1$  (more than three orders of magnitude larger than in GaAs (see Sections 3.6 and 3.2)). Having an almost spin-zero nuclear background, silicon offers significantly reduced effects compared to GaAs from contact hyperfine interactions and spin-orbit coupling. This clearly brings benefits quantum computing by allowing for longer gate operation times and greater fidelity in qubit state readout.

In addition, as the long-time staple for the electronics industry, silicon is compatible with existing semiconductor device fabrication and VLSI techniques. These are highly transferable to the fabrication of spin qubits and makes SOI a practical platform to pave the way for future large scale integration of quantum information processing systems.

Preliminary designs of our SOI based device consist of a symmetric pair of lithographically defined DQDs with in-plane side gates where one set of DQDs (denoted the “SSTD”) is used for single electron spin turnstile operation and the other (denoted the “electrometer”) acting as an electrometer for single electron detection. Structural analysis and dynamic simulation of these operations were performed by combining 3D FEM based capacitance simulations and Monte-Carlo single electron circuit simulation. The results presented showed that our system is capable of its intended operation and suitable as a preliminary design to be built on in the near future for more complex single spin manipulation. We presented a new method of detection of single electron turnstile operation which makes use of the periodicity present in

the charge stability diagram of a DQD and allows for separate detection of electron configurations in each QD of the DQD despite the symmetric nature of our design. An advantage of this symmetry is of course the potential for higher yield during fabrication due to the ability to interchange the operations of the SSTD and electrometer.

In addition, we successfully implemented and optimised a VLSI compatible fabrication process allowing for the large scale parallel fabrication of over 100 devices. These are scalable intrinsic silicon based high density DQD systems realised using HSQ resist and electron beam lithography (Lin *et al* (2012)). The implementation of HSQ resist allowed for repeatable lithographically defined SOI Si QDs of  $\sim 50$  nm and nanowire channel constrictions of just  $\sim 25$  nm. This is smaller than that in previous work [40], [39] and increases the potential for true single electron QD occupation and manipulation. The resultant high density nanostructures are well-defined and within variations of less than  $\pm 5$  nm from the design for over 80% of the 144 devices fabricated in parallel. This demonstrates the repeatability of our fabrication process where the average realised QD dimension was 61 nm with a standard deviation of 3.4 nm. One of the great advantages of our process is the rapid turnover time achieved where due to the scalable nature of the process, parallel fabrication of larger numbers of devices does not significantly affect fabrication turnover time. In addition, the use of a single step lithography process to define both QD structures and their respective individual control gates allows for a reduction in fabrication time compared to GaAs device systems where multiple lithography steps are needed to define the metal control gates [31].

Preliminary electrical characterisations demonstrated repeatable consistent control of the intrinsic DQD channel current via a metal top gate. Clear MOSFET on/off control was observed for over 70% of tested devices with a high electron mobility of up to  $4800 \text{ cm}^2/\text{Vs}$ . In addition, successful repeatable Coulomb oscillations and Coulomb diamonds (see section 2.2) signifying single electron transport and storage are observed in the electrical characteristics of Si DQDs when controlled with the metal top gate at a base temperature of 80 mK. Here, little hysteresis was observed during forward and reverse sweeps of the top gate control of DQD channel conductance with stable single electron Coulomb oscillation measurements that did not drift with time. This demonstrates the level of stability our devices offer in single electron manipulations achieved through our fabrication process.

From measurement data the charging energy of each QD was extracted to give QD dimensions of  $\sim 25$  nm. Effective control across multiple Coulomb oscillations with the top gate signifies single electron tunnelling and provides evidence of the viability of our system for single electron manipulation. However, despite these successes, measurements did

identify some weaknesses to do with our device performance. The most important of which was the insufficient sensitivity of Si in-plane side gates in individually controlling the single electron occupation of QDs.

Many of these issues in device performance were however resolved when we introduced further advancements and optimisation of the fabrication process. A migration to the use of 2% HSQ has allowed for unparalleled increase in empirical resolution of our e-beam exposure of device structures. This has enabled the parallel fabrication of more advanced DQD structures with up to 5 side gates for even greater single electron control. Further to this was the migration of all lithography steps to e-beam based processes to minimize the potential for alignment errors. This led to significant size reductions in many device components including the top gate which increases the potential for electrical characterisations via RF reflectometry methods [51]. Trials showed that through the updated process, a variety of different, more complex QD device designs can be realised repeatedly, demonstrating the consistency of the process and paving the way towards true single electron occupation and manipulation in intrinsic Si QDs.

Electrical characterisations demonstrated effective individual and simultaneous control of single electron turnstile operations through QDs via the use of side gates. Further to this, observations suggest the capability of charge detection by one QD channel in close proximity to another. One of the major points of interest observed was our fabrication process' ability to realise very small intrinsic Si QDs down to just 10.6 nm. This dimension of QDs offer an unmatched precision in the level of control of single electron occupations of the QD. It also enables precise analysis of the excited states of electrons occupying QDs in great detail and their variations with the application of an external magnetic field. This demonstrates a level of clarity within Coulomb blockade diamond characteristics not seen before in literature on SOI based QD at a temperature of 4.2K. Through the application of an external magnetic field, clear evidence of splitting of the degenerate QD excited states was observed from which we extracted the spin orientation of electrons tunnelling into the QD. This spin readout gave us an indication of the number of electrons stored on the QD and in turn, our ability to control the QD with precision down to the single electron limit.

These results demonstrated the level of control in QD dimensionality our fabrication process is able to achieve, not only through precision offered by our updated HSQ based e-beam device lithography process but also through optimised control of thermal oxidation around the device structures to reduce QD dimensions. Through characterisations of multiple devices,

we demonstrated the fabrication of a number of QDs ranging from just 10.6 nm to over 20 nm.

Out of the samples we tested, the best measurement yield we obtained was 69% of all devices fabricated in parallel. This value represents the percentage of QD devices channels that could be switched on and off repeatedly at 4K cryogenic temperatures with a sufficient channel resistances to be able to detect single electron turnstile operations and observe QD Coulomb oscillations characteristics. The devices would have also had to show no observable leakage between any of the device components at the expected operating voltages.

The combination of the above measurements and fabrication results provides an effective indication and evidence of the viability of our fabrication process and resultant diverse QD systems in enabling future advancements in the area of large scale parallel fabrication of repeatable integrated QD structures which are capable of supporting single spin qubit operations towards quantum information technology.

To further the impact of this work, the results of our versatile fabrication process have branched out to other fields of research, for example where the fabrication technology has been utilised to realise energy reversible Si-based NEMS switch for nonvolatile logic systems (See list of publications).

## 6.2 Directions for Future Work

As the core of this work was to produce a fundamental platform and standardised process which future research can use to further the area of Si based quantum information research, there are many channels for future work which could lead to interesting and novel insights. A few possible directions are discussed here.

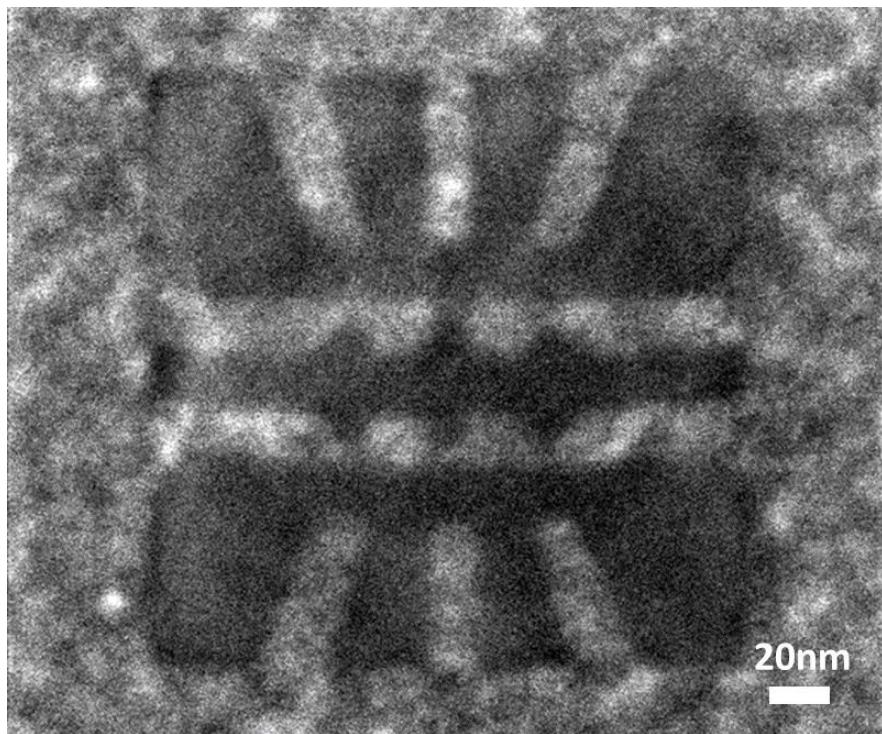
### 6.2.1 *Characterisation of more complex DQD systems*

The devices produced in this work consisted of more than just the selection of devices measured. Measurement of some of the more complex DQD devices which were shown in 5.4.2(a) could lead to more interesting results and novel ways of electron spin manipulation. In fact, efforts are currently underway to characterise the more complex DQD devices fabricated which will hopefully enable the demonstration of dynamic detection of single electron spin relaxation times and spin manipulations from devices fabrication by our VLSI compatible process.

### 6.2.2 *Integration of nano-magnet and on-chip waveguide*

For future research, the device design can be modified to include a nanoscale magnet and an on-chip waveguide to access and control the spin states of electrons in the Si QD system. This was already explored by the device design shown previously in Fig. 5.4.2(c). Methods which could be implemented to enable spin manipulation and dynamic detection of spin dependent transport can then largely be based on transferable methods developed through previous experiments performed on QDs fabricated from GaAs (see Section 3.2-3.3). Electrical measurements of single electron spin states can be performed through a spin-to-charge conversion method much like that used by [17]. In this way, the spin relaxation time  $t_1$  for a single spin in an SOI QD can be measured. In order to measure the spin decoherence time  $t_2$ , electron spin resonance (ESR) can be used much like that in [31] or [33] through the use of a nanomagnet (producing a magnetic field gradient) and controlled by the on-chip waveguide. Spin readout can then once again be via a spin-to-charge conversion method to allow electrical detection.

### 6.2.3 *He-ion fabrication of ultra-small QDs*



**Fig. 6.2.3(a)** A He-ion microscope image of a tri-gate dual DQD device design pattern etched 7 nm deep via direct milling into Si.

With our optimised thermal dry oxidation process demonstrating an oxidation variation of below 5 nm across a 6" wafer, this means we can practically thin SOI down to thicknesses of

only 10 nm or below. With the advancement of helium-ion milling techniques [54], this enables an alternative approach to QD device lithography as direct milling has been demonstrated to be able to etch around 10 nm of SOI without significant contamination. Given the even greater lithographical precision of He-ion microscopes (with milling resolutions of down to 3 nm) compared to e-beam, it may be possible to produce smaller (sub 15 nm) lithographically defined QDs on the ultra-thin SOI. Trials with the He-ion milling facility at the University of Southampton demonstrated the ability to lithographically define QD structures in Si that are only 15 nm in dimension (see Fig. 6.2.3(a)). This coupled with our precise oxidation process developed could lead to the potential realisation of QD operations at higher temperatures.

#### *6.2.4 Radio-Frequency dependent characterisations of SOI QD conductance*

Despite reductions in top gate dimensions as a result of our updated fabrication process, our radio-frequency (RF) setup showed no clearly detectable resonance with the device when switched on or off. This suggests a need for further process optimisation as the enablement of RF characterisations brings major benefits in terms of much faster measurement speeds compared to D.C. and much higher measurement sensitivity. In addition, using RF to realise single-shot measurements of the single electron spins suppresses unwanted back-action from the electrometer and improves decoherence time of the qubits.

#### *6.2.5 Further process optimisation*

The presence of fixed charges in the device structures presented a major challenge in the control of QD channel in proximity by a single top gate. The removal of fixed charges and contaminants during the fabrication process is key to enabling repeatable dynamic single electron charge detection between two QD channels in proximity. This is a major area where further optimisation could lead not only to improved device performance but also the fabrication yield.

# Appendix A

## Aluminium Stripline Simulation

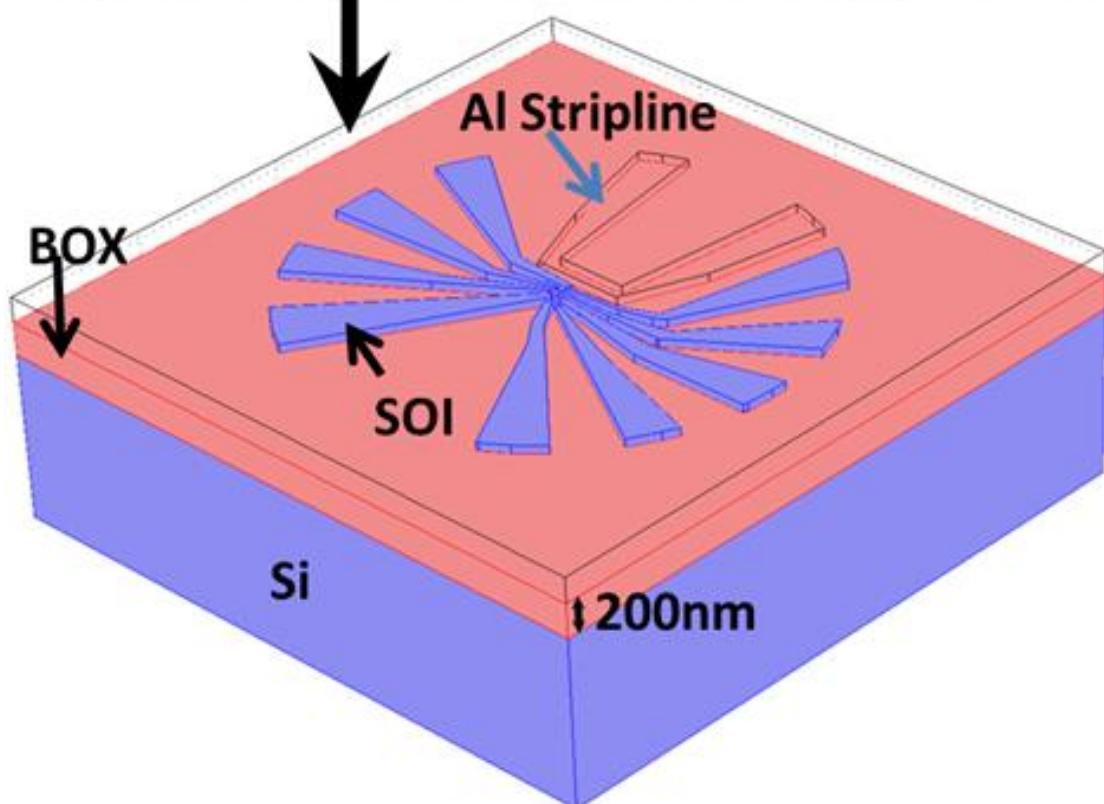
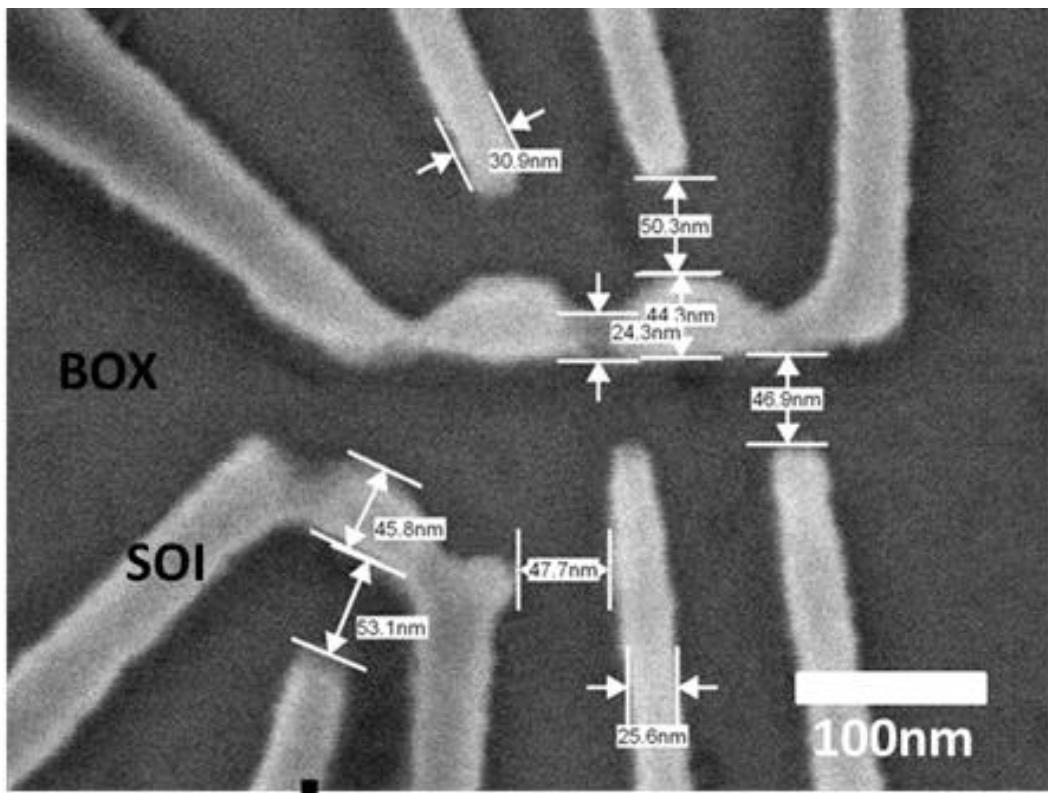
To gain insight into the effectiveness of our aluminium stripline design and its ability to generate microwaves with minimal electric field fluctuations at the position of our QDs, we undertook classical COMSOL current based simulations.

Device geometries (see Fig. 5.4.2(c)) and relevant material properties were input into COMSOL's 3D time harmonic electromagnetic module much like in section 4.2. This is shown in Fig. A.1 where the device consists of a DQD electrostatically coupled to a SET with an on-chip Al stripline.

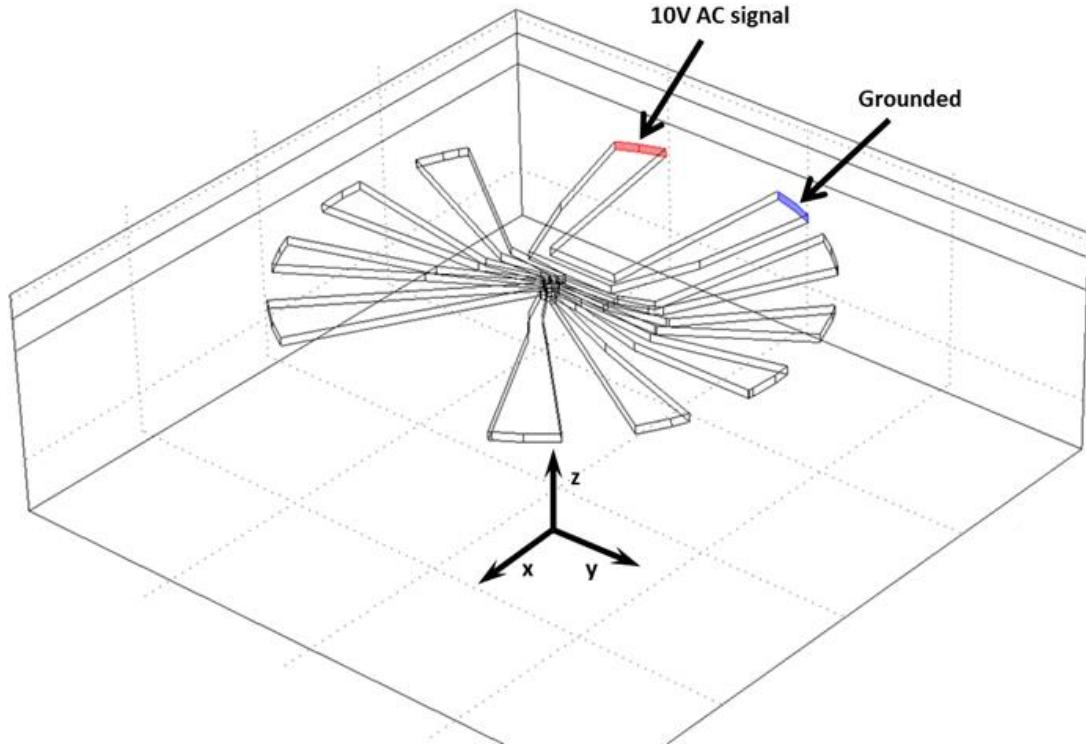
The stripline near the DQD is designed to have a 100x100 nm square cross section, is 1  $\mu\text{m}$  long and 200 nm away from the centre of the nearest QD. These dimensions were chosen based on the results from previous experiments by [44] who worked with phosphorus dopants and discussions with their fabrication team.

In order to manipulate single electron spins and generate detectable Rabi oscillation we need to induce A.C. magnetic fields of a few mT [31] at the position of the QD whilst minimising the electric field. By applying an A.C. sinusoidal source to drain signal (see Fig. A.2) of 10 V, simulations suggest that we can induce an oscillating magnetic field perpendicular to the plane of the device (i.e. the z direction),  $B_z$ , of amplitude 500 mT (see. Fig. A.3) at the position of the nearest QD of the DQD.

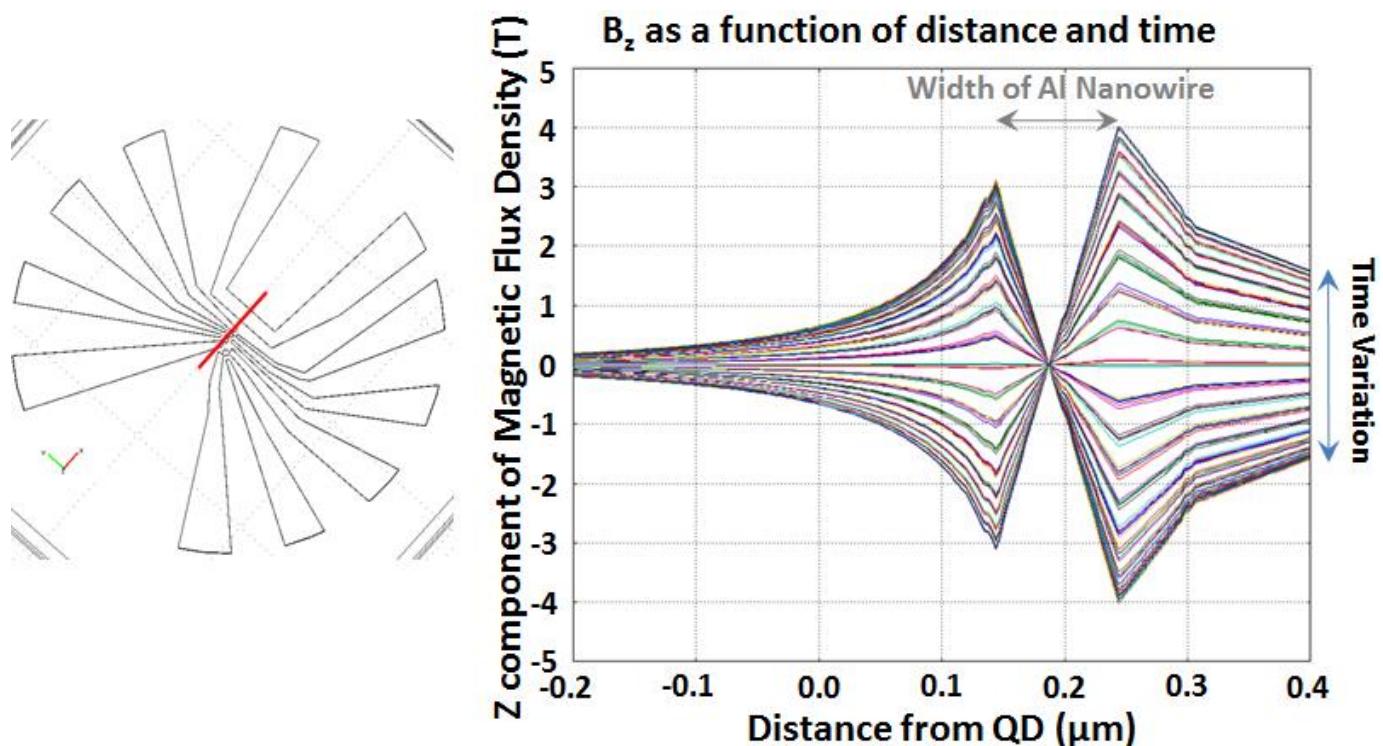
This translates to 5 mT of magnetic field,  $B$ , at the position of the nearest QD for an applied stripline source to drain signal,  $V$ , of 100 mV (since  $B \propto V$ ). This is a more realistic source to drain voltage used in practice and should induce a current of  $\mu\text{A}$  which in turn should not incur significant effects on QD's single electron operation due to Joule heating of the stripline.



**Fig. A.1** Top: SEM of the device nanostructure before Al stripline deposition. Bottom: The corresponding device nanostructure with the local tapered design and stripline input with the correct geometries into COMSOL.



**Fig. A.2** 3D schematic showing the boundary conditions set for the source and drain of the Al stripline. The other boundaries of the devices are set to continuity boundary conditions with the correct material properties of relative permeability, permittivity and conductivity for Si, SiO<sub>2</sub> and Al.



**Fig. A.3** Left: a top down view of the device design in COMSOL. The red line indicates the length and position of the cross-sectional plot for the graph to the right. Right: A plot of the z component (perpendicular to the plane of the device) of the magnetic field in the plane of the device at different times (time here is arbitrary as solutions are steady state based). The length of the plot is indicated by the red line in the left figure. As expected from classical electromagnetism,  $B_z$  decreases with  $1/x$  outside the stripline and is linearly proportional to  $x$  within the stripline.

From these simulations, the x and y component of the magnetic field,  $B_x$  and  $B_y$  respectively, were found to be  $B_x = 0.25$  mT and  $B_y = 3.75$  mT at the position of the nearest QD to the stripline with  $V=10$  V. This translates to negligible field magnitudes when a  $V=100$  mV signal is applied across stripline source and drain.

These steady state classical simulations therefore suggest that the dimensions and position of the aluminium stripline are sufficient to produce the required magnetic field at the position of the DQD. However, to analyse stationary modes of the electric and magnetic field at these positions and to minimise the electric field component (since an oscillating electric field will result in the electron oscillating and forming an unwanted dipole), more involved RF based simulations need to be performed to better understand the microwave physics and the effects of geometry on electric and magnetic field uniformity.

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