

A Distributed Amplifier System for Bilayer Lipid Membrane (BLM) Arrays With Noise and Individual Offset Cancellation

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Abstract—Lipid bilayer membrane (BLM) arrays are required for high throughput analysis, for example drug screening or advanced DNA sequencing. Complex microfluidic devices are being developed but these are restricted in terms of array size and structure or have integrated electronic sensing with limited noise performance. We present a compact and scalable multichannel electrophysiology platform based on a hybrid approach that combines integrated state-of-the-art microelectronics with low-cost disposable fluidics providing a platform for high-quality parallel single ion channel recording. Specifically, we have developed a new integrated circuit amplifier based on a novel noise cancellation scheme that eliminates flicker noise derived from devices under test and amplifiers. The system is demonstrated through the simultaneous recording of ion channel activity from eight bilayer membranes. The platform is scalable and could be extended to much larger array sizes, limited only by electronic data decimation and communication capabilities.

Index Terms—Bilayer lipid membrane, current amplifier, discrete-time amplifier, electrophysiology, ion channel recording, low noise, microfluidic device, parallel BLM recording, sensor array.

I. INTRODUCTION

ION CHANNEL proteins play a pivotal role in a wide variety of physiological processes and in several chronic diseases, and are consequently of considerable interest to the pharmaceutical industry. Electrophysiology is the gold standard for investigating the function of channel proteins and their modulation by pharmaceutical drugs, particularly at the single-channel level, but it is also a laborious process with very low throughput. It involves placing an electrode on either side of a membrane and measuring the current flow through the ion channels in the

membrane. Currents are typically between 1 and 150 pA per channel. The key challenge is to obtain a ‘Gigaseal’ configuration where the two aqueous compartments are electrically insulated from each other by a stable cell membrane or lipid bilayer. This is difficult to achieve, rendering conventional electrophysiology a laborious process with a notoriously low throughput.

When considering strategies to increase throughput, it is necessary to distinguish between the two main electrophysiology methods: 1) patch clamp [1], [2] and 2) bilayer lipid membranes (BLM) [3]. In patch clamp, a glass pipette, containing an electrode connected to an amplifier, is tightly pressed against a cell membrane forming a seal with Gigaohm resistance. The opening of the pipette is rather large ($\sim 2 \mu\text{m}$ diameter) and consequently the clamped membrane patch typically contains many ion channels, resulting in electrical characterization of channel populations rather than single-channel recordings [1].

Several companies have commercialized patch clamp systems that automate cell and pipette manipulation, but they do not substantially increase the capacity for ion channel screening [4]. To increase throughput, emphasis has been placed on the development of microfluidic planar-array based patch clamping, in which cells are sucked onto an aperture in a chip rather than onto the end of a glass pipette. Commercial parallel platforms require significant investment ($> \$100 \text{ k}$ per instrument), due in part to the high cost of connecting each well to its own amplifier. Furthermore, these systems are not configured for electrophysiology at a single channel level [4].

Electrophysiology using artificial bilayer lipid membranes is in principle easier to automate than patch clamp because it does not involve the manipulation of delicate cells. In a conventional BLM setup, a protein-free lipid bilayer is suspended in a vertical aperture of $\sim 150 \mu\text{m}$ diameter made in a hydrophobic plastic such as Teflon or Delrin (Fig. 1). The aqueous chambers on both sides of the aperture are electrically insulated from each other when the bilayer is present ($\sim 50 \text{ G}\Omega$ resistance) and with an electrode in each chamber, the current flowing through ion channels can easily be measured using an amplifier such as ID 526 BLM amplifier (Industrial Developments Bangor, Bangor, UK) as shown in Fig. 1. The main advantage of suspended bilayers is that their very low leakage current enables recording of single ion channels [3]. This yields more detailed electrophysiological data than recordings on the entire channel population of a clamped membrane [1].

Manuscript received March 26, 2014; revised June 08, 2014 and July 12, 2014; accepted July 24, 2014. This work was supported by the Engineering and Physical Sciences Research Council (U.K.) through Grant EP/H044795/1 and by EU and National funds (IT) under the ENIAC-JTI project LAB4MEMs. This paper was recommended by Associate Editor A. Mason.

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Digital Object Identifier 10.1109/TBCAS.2014.2346402

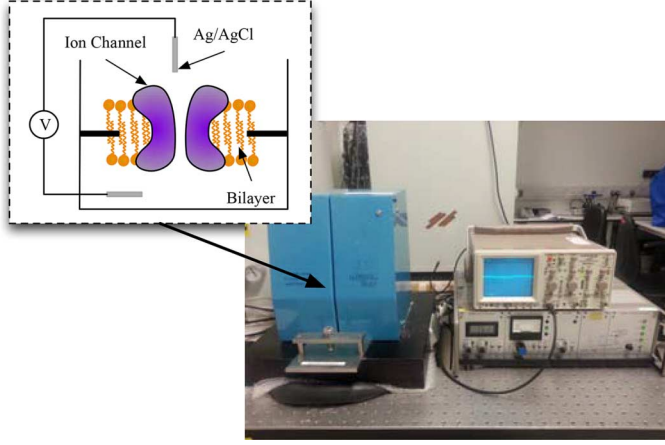


Fig. 1. Conventional BLM setup using a commercial amplifier platform.

However, the low throughput of conventional BLM systems is due to the fact that suspended lipid bilayers are difficult to form, and once formed, easily break when channel-containing liposomes are added to one of the aqueous chambers. In conventional bilayers, the apertures are made in Teflon or Delrin [5] by a laser or mechanical drill, which results in a large aperture ($>100 \mu\text{m}$). Also commercially available bilayers cups (e.g., Warner instruments) made from polysulfone have apertures that are larger than $150 \mu\text{m}$. The large diameter aperture makes it difficult to form bilayers, which break easily. In addition, leakage currents may exist due to poor clamping or bonding of apertures between separate reservoirs [6].

A variety of approaches have been explored to facilitate bilayer formation and stability. All of these use a horizontal bilayer rather than the classical vertically suspended bilayer because the horizontal format can in principle be scaled up. For a vertical bilayer architecture, each bilayer needs a compartment/cup on each side of the aperture. Bilayer formation protocols do not allow these cups to be smaller than approximately 5 mm. In contrast, for a horizontal bilayer architecture, each bilayer can have a microfabricated aqueous compartment on one side [6]–[8] while tens to hundreds of these bilayers can share the same aqueous top compartment, allowing sufficient space for bilayer formation protocols, without compromising the footprint of an individual bilayer site.

Very stable bilayers can be deposited on a horizontal solid or nanoporous substrate, but these supported bilayers tend to suffer from leakage currents and/or from a limited ion reservoir beneath the bilayer, which limits their use for single-channel electrophysiology. Instead, most studies have focused on optimizing the formation of bilayers suspended across a horizontal aperture. Several groups have explored variations in the aperture itself (material, thickness, diameter, geometry) and also in novel microfluidic delivery methods for the lipid/solvent mixture from which the suspended bilayer is formed (e.g., [9]–[13]).

In the last years, substantial progress in the routine formation of stable on-chip bilayers for single-channel recordings has been made [5]. The present state of the art is the sequential recording of 96 droplet-in-oil bilayers [6] and the simultaneous formation with subsequent serial or sequential recording of 12–16 individual horizontally suspended bilayers [7], [14].

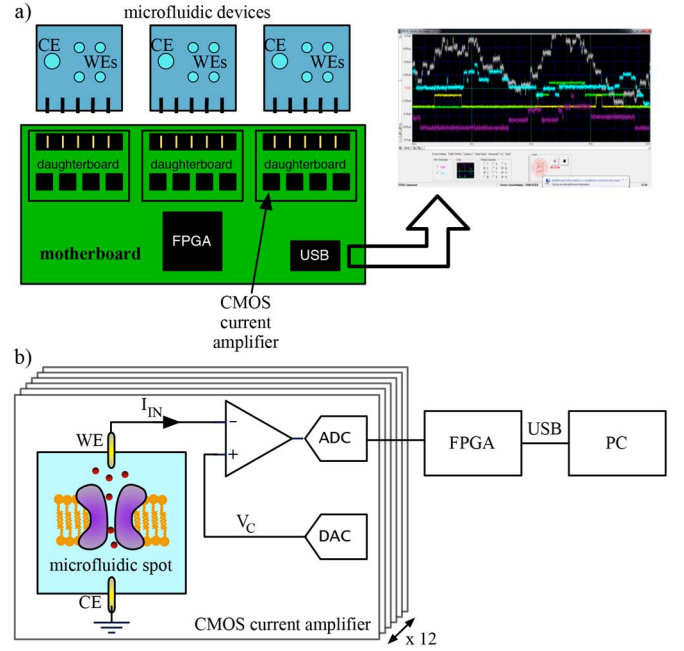


Fig. 2. (a) Description of the parallel acquisition system, showing microfluidic devices, daughter-boards and mother-board. (b) Workflow of the system highlighting the array structure. The CMOS current amplifier stimulates the BLM with a voltage V_C and reads the flowing current. The current is digitized and sent to FPGA for data processing.

The step change required to realize high-throughput, truly parallel/simultaneous single-channel electrophysiology with on-chip BLM systems is to make all the bilayers electrically independent, which requires that each bilayer is connected to its own amplifier.

This paper presents a novel system where electronics and microfluidics are coupled together to create a compact architecture for truly parallel single-channel BLM recording. The system is able to form and read from 12 BLMs concurrently, keeping each bilayer electrically independent from all others. In Section II the proposed platform is described and in Section III the CMOS current amplifier is presented, while Section IV explains the structure of the microfluidic components. Finally, bilayer formation, ion channel incorporation and parallel ion channel current recording are reported in Section V.

II. PARALLEL PLATFORM

A. System Overview

In this paper we describe a novel system for parallel BLMs formation and recording. The system is based on a low-cost hybrid technology that integrates disposable microfluidic devices with CMOS low-noise current amplifiers on a single platform, offering a fully scalable acquisition system for BLM arrays.

The parallel system consists of the following several different parts as illustrated in Fig. 2:

1—Microfluidic chips supporting suspended BLMs for ion channel recording with embedded Ag/AgCl electrodes and pads for electrical interconnection.

2—An array of custom-made low-noise CMOS amplifiers for ion-channel current amplification. Each IC includes a charge

sensitive amplifier (CSA) and a delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC), outputting a single-bit stream.

3—A digital control unit implemented in a Field Programmable Gate Array (FPGA) performing data filtering and system control [15].

4—A custom-made Graphical User Interface (GUI) used for data visualization and storage.

The system works as follow: each CMOS current amplifier stimulates the corresponding BLM with a voltage stimulus V_C ; then the CMOS frontend reads, amplifies and digitizes the ionic current flowing through the ion channels in a single lipid membrane. Digital data coming from all the CMOS amplifiers is collected and processed by the FPGA. Then, the FPGA communicates with the PC via a USB link (Fig. 2).

Digital control circuitry and analog readout circuitry are placed on two separate PCBs, named motherboard and daughterboard, respectively. The motherboard consists of the FPGA, power supply control circuits, connectors for daughterboards, and USB controller for data communications with the PC. Every daughterboard includes four low-noise current amplifiers implemented in $0.35\ \mu\text{m}$ CMOS technology. The microfluidic devices are made on a glass substrate and are $15 \times 15\ \text{mm}$ in dimension. Each microfluidic chip has four apertures for BLM formation, with four Ag/AgCl electrodes used as working electrodes (WEs) and a common reference electrode used as counter electrode (CE). The fluidic devices are connected to the daughterboard via Samtec™ single row connectors. This arrangement of the overall system ensures better shielding from electromagnetic interference, prevents exposure of the electronics to any reagents, and allows simple and fast replacement of microfluidic devices.

The system is flexible and scalable and is designed for maximum versatility; the FPGA can manage up to 1500 channels simultaneously [15]. Different kinds of fluidic devices can be accommodated, either for manual or automated BLM formation [5]. The aforementioned approach, where a readout circuit is in close proximity to the microfluidic substrate, is particularly suitable for BLM readout for the following reasons: 1) since noise is correlated to the input stray capacitance, the closer the readout the lower the noise [16], [17]; 2) due to the low current regime and timing requirements, single-BLM signal multiplexing should be avoided, since this will reduce performance. Thus, it is crucial to place the electronic conversion as close as possible to each BLM, provided that exposure of electronics to reagents such as buffer solution is avoided.

Photographs of the system are shown in Fig. 3. The motherboard is housed in a metal box for shielding against spurious coupling of digital signals. The system accommodates three daughterboards and three microfluidic devices, providing concurrent acquisition of 12 channels. The CMOS current amplifier works in both single supply mode and dual supply mode. It acquires current signals over four selectable bandwidths: 625 Hz, 1.25 kHz, 5 kHz and 10 kHz, and two input ranges: $\pm 200\ \text{pA}$ and $\pm 20\ \text{nA}$.

B. System Scalability

Each acquisition channel is amplified and digitized by a dedicated circuit (as explained in Section III). All the digital

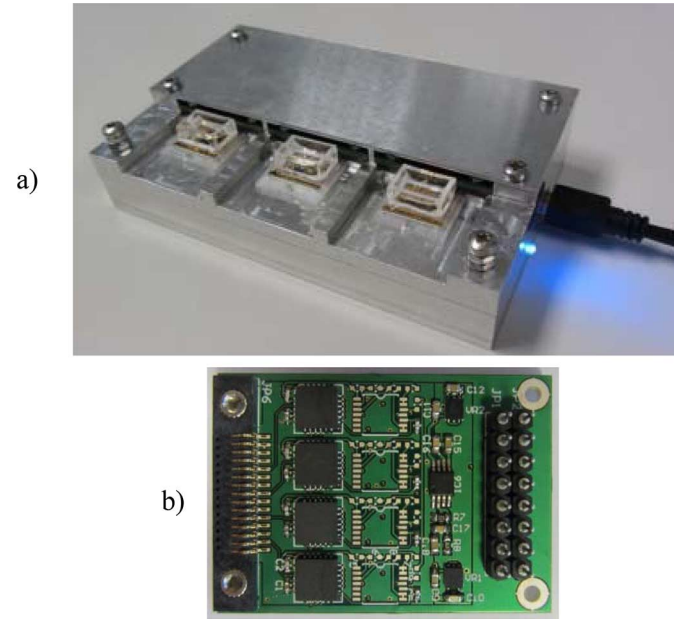


Fig. 3. (a) Photograph of the 12-channel parallel acquisition system. (b) Photo of a single daughterboard including 4 CMOS current amplifiers.

data are acquired and processed by FPGA, which decimates data at the proper frequency based on the selected oversampling ratio (OSR) before delivering the information to a PC via USB link. The FPGA implements a two stages decimator filter, transforming the 1-bit $\Delta\Sigma$ output stream to a 16-bit data stream [15].

The architecture has been designed to allow scaling up to a very large number of data channels that can all be processed in parallel. Scaling limits are imposed by the performance of the FPGA and maximum capacity of the data transfer link, while the analog section could be easily scaled by increasing the number of ICs. For instance, a commercial FPGA (i.e., Xilinx Virtex VI® XC6VSX475T) offers up to 2.016 DSP slices operating at 600 MHz, where each slice can process a single channel. Assuming an acquisition channel operating at 10 kHz with 16bit resolution, for each data sample transferred through a USB 2.0 full-speed (12 Mb/sec) data link it is possible to deliver up to 30 channels simultaneously. Upgrading to a USB 2.0 high-speed (480 Mb/sec) data link increases the number of channels up to 1.500 channels. Using Ethernet link operating at Gbps data rate, the maximum number of channels could increase up by a further order of magnitude.

The hardware setup reported in this manuscript is a proof-of-concept limited to 12 channels that can be concurrently acquired, but could be scaled up to 30 channels. Scaling to a higher number of channels requires changing the data transfer link from USB 2.0 full-speed to USB 2.0 high-speed or USB 3.0.

III. CMOS LOW-NOISE CURRENT AMPLIFIER

A. General Architecture

A block schematic of the architecture tailored to reduce both noise and offset, is shown in Fig. 4. Current acquisition and amplification is made with a discrete-time charge-sensitive

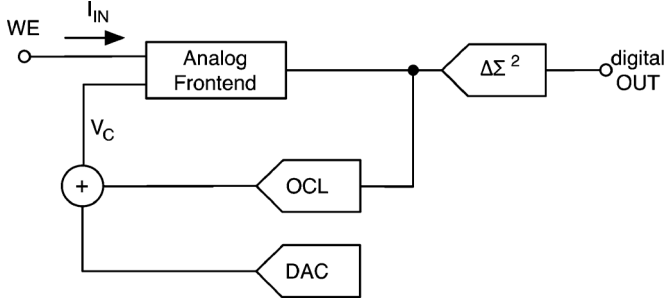


Fig. 4. Block scheme of the low-noise CMOS current amplifier, with the OCL block for compensation of the offset generated at the electrode-electrolyte interface and DAC for generation of V_C stimulus.

amplifier (DT-CSA) that integrates the input current over fixed periods of time, termed integration phases. A low-pass filter is added after the CSA to band-limit the system and lower the noise [19]. A CDS scheme is used to further reduce offset and the noise of the CSA [18], [20]. A delta-sigma ADC digitizes the signal into a high frequency single-bit data stream. A second-order low-pass delta-sigma ADC is used to keep the quantization noise below the thermal noise and minimize the effects of limit cycles [21]. A 10-bit DAC generates the stimulus voltage V_C , which is applied to the BLM through the CSA virtual short-circuit. The offset correction loop checks the analog output against a reference value to compensate for any electrode-electrolyte offset. The offset correction loop is activated at the system startup, while it is switched off during current acquisition with the final offset compensation value stored inside the digital offset correction loop (OCL).

The current acquisition based on integration-differentiation scheme has proven to achieve both low noise levels and high bandwidths [16], [17]. DT-CSA has shown to be slower than continuous-time CSA, however it has better noise performance at lower bandwidths [16].

One of the main problems in bioelectronics amplifiers is the low-frequency noise of the CMOS amplifier [17]. There are two main techniques to reduce such noise: chopping and correlated double sampling (CDS) [18]. The proposed system employs a novel complementary-clocked-parallel CDS based on the scheme presented in [20]. The aim of this novel scheme is to maximize the active time allowing the application of different stimulus signal V_C to each ion channel, made possible by virtual short-circuit at the CSA input. Maximizing the active time is fundamental to increasing the equivalent trans-resistance R_{eq} of the system and thus lowering the noise. As reported in [16] the input-referred noise is approximately given by

$$\overline{i_N^2}(f) \approx \frac{16}{3} \frac{C_T}{R_{eq}} \frac{kT}{C_O} \quad (1)$$

where C_T is the total capacitance facing to the input node, k is the Boltzmann constant, T is the temperature in Kelvin degrees, C_O is the capacitance at CSA output and R_{eq} is given by

$$R_{eq} = \frac{T_{INT}}{C_F} \quad (2)$$

where C_F is the CSA feedback capacitance and T_{INT} is the active time used for integrating the input signal. The proposed scheme lowers the input referred rms noise at 1 kHz by about 50% (from 200 fArms to 100 fArms) with respect to the original scheme presented in [20]. Results are shown in Section III-D.

Application of different stimulus signal is fundamental for the array approach; in this way each BLM can be treated as a separate site and different tests can be done at the same time. However, applying V_C to CSA positive input causes output signals to be referred to V_C , which is time variant. Hence, a subtraction step is needed before analog-to-digital conversion; this compensation is performed by the CDS scheme.

Another very important problem is cancellation of the voltage offset that can be generated at the electrode-electrolyte interface since it affects the current measure and thus the total accuracy. A high offset voltage (hundreds of mV) creates a high offset current, limiting the acquisition range or even causing saturation of the current amplifier. To cope with interface offset in an array platform, we developed a digital offset correction loop (OCL) integrated in each CMOS amplifier. A detailed description of the functionality of these blocks is presented in the next section.

B. Analog Frontend

A detailed scheme of the analog frontend is shown in Fig. 5. The system works in time frames of period T_S . Each time frame is divided into three phases: a reset phase, a noise-sampling phase and an integration phase. To maximize the integration phase, two CDS stages have been designed working in a complementary clocked parallel way. While CDS1 follows the integral of the input current, CDS2 transfers the result of the previous integration phase to the S&H circuit, and vice versa the following time frame (Fig. 6) where switches S5 and S9 clock the two CDS circuits at the sampling frequency $f_S = 1/T_S$. This solution requires the CDS stages to be well matched, otherwise an undesired square-wave at half of the sampling frequency will appear at the S&H output.

A detailed description of the system workflow during time frame 1 is as follow. During the reset phase, switches S1, S2, S3 and S4 are closed, resetting the charge stored in feedback capacitances of both the CSA and the sample and hold (S&H). The use of two switches to reset each stage reduces the charge injection because they are connected to the reference node that has a low impedance. We set the reset period to 200 ns, the minimum time needed to reset the capacitors.

The noise-sampling phase starts after the reset phase. During this phase CDS1 follows the CSA output, while CDS2 starts to transfer the value stored into its capacitors to the S&H. At the end of the noise-sampling phase, S6 opens sampling the noise, the op-amp offset and the charge injection on capacitor C_2 of CDS1. This phase cannot be too short because it must sample the noise with sufficient accuracy [21]. At the same time, it cannot be too long otherwise the integration phase would be significantly reduced. To cope with this trade-off we opted for a constant noise-sampling phase lasting 6.4 μ s based on empirical analysis.

The integration phase is the most important because it is the only one concerning the input signal; hence it must last as long as possible to minimize loss of data. During the integration

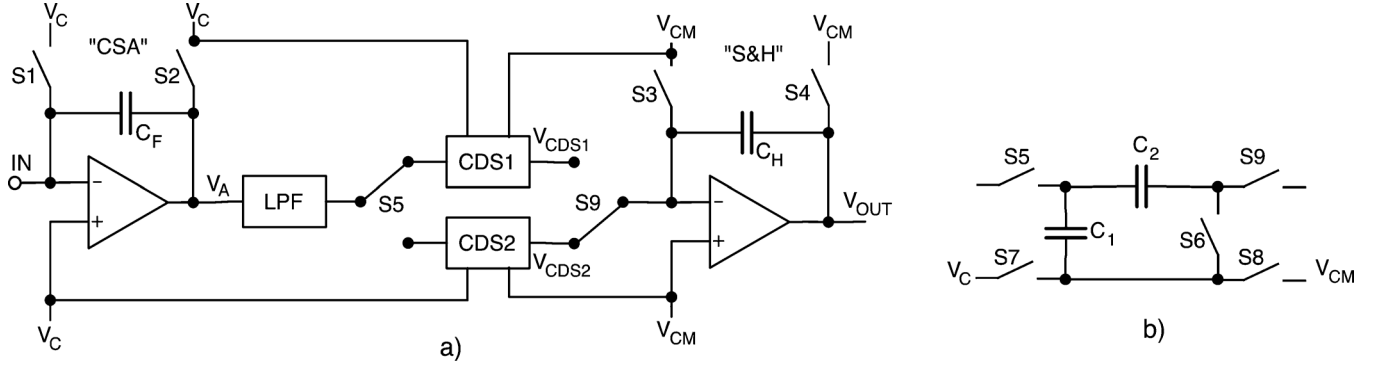


Fig. 5. (a) Schematic of the analog frontend showing the reset solution, the LPF, and two CDS stages realizing the complementary-clocked-parallel architecture governed by switches S5 and S9. (b) Detailed architecture of a single CDS stage. Switch S6 is used to sample the noise into capacitor C_2 [20]. Switches S7 and S8 are used to subtract V_C from the input signal and refer it to V_{CM} .

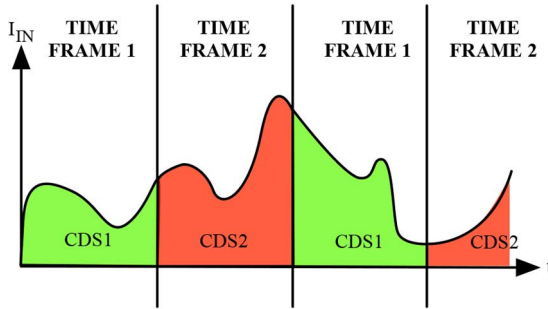


Fig. 6. Division of the acquisition time into frames. The integrated input current is processed by CDS1 in time frame 1 while it is processed by CDS2 during time frame 2. This is the principle behind complementary-clocked-parallel CDS.

phase the CSA integrates the input current and CDS subtracts the pre-stored noise sample. At the end of this phase the voltage at the output of CDS1 (or CDS2 in time frame 2) is given by

$$\begin{aligned} V_{CDS1}(t_1) &= \frac{1}{C_F} \int_{\text{frame1}} I_{IN}(t) dt - V_{n1} + V_C, \\ V_{CDS2}(t_3) &= \frac{1}{C_F} \int_{\text{frame2}} I_{IN}(t) dt - V_{n2} + V_C \end{aligned} \quad (3)$$

where I_{IN} is the input current, V_{n1} and V_{n2} are the pre-stored noise samples and V_C is the stimulus signal. This voltage is temporally stored in the $C_2 - C_1$ series capacitors and is transferred to S&H during the integration phase of the next time frame. Before transferring can take place V_{CDS1} must be referred to V_{CM} , i.e., the common-mode voltage of the $\Delta\Sigma$ converter. To achieve this two alternating switches have been added as shown in Fig. 5(b). During the integration period switch S7 is closed, referring all the internal voltages to V_C as in (1). Then S7 opens and S8 closes before the CDS transfers the charge to the S&H circuit, hence V_{CDS1} (or V_{CDS2} in time frame 2) becomes

$$\begin{aligned} V_{CDS1}(t_2) &= \frac{1}{C_F} \int_{\text{frame1}} I_{IN}(t) dt - V_{n1} + V_{CM}, \\ V_{CDS2}(t_4) &= \frac{1}{C_F} \int_{\text{frame2}} I_{IN}(t) dt - V_{n2} + V_{CM}. \end{aligned} \quad (4)$$

The workflow starts again in the next time frame after swapping CDS1 with CDS2 (Fig. 7). The output voltages at S&H during the first and second frames can be described as

$$\begin{aligned} V_{OUT1}(t_2) &= V_{CDS1}(t_2) - V_C + V_{CM}, \\ V_{OUT2}(t_4) &= V_{CDS2}(t_4) - V_C + V_{CM}. \end{aligned} \quad (5)$$

Due to the high number of switches, noise and charge injection of the switches in the CDS scheme become significant. Therefore, we designed complementary switches with dummy structures optimized for voltages around V_{CM} [22]. Moreover, the digital clocking signals were designed to realize a back-sampling technique, providing a further reduction of the charge injection [23].

C. Offset Compensation Loop

The junction potential in a BLM setup is due to the electrode-electrolyte interface and is typically in the order of tens to hundreds of millivolts. Such a high offset voltage generates a large offset current that limits the acquisition range or even causes saturation of the CSA. To cope with the junction potential offset in an array platform, we developed a digital OCL integrated in each current amplifier. Note that this current offset could not be canceled out by CDS, which cannot discern between signal and current offset. The OCL is composed of a comparator, an up/down counter and a 10-bit digital-to-analog converter (DAC) with a full range of 200 mV to compensate standard offset values with a minimum step of 200 μ V (Fig. 8). The OCL compares the S&H output with V_{CM} , which is the reference voltage corresponding to zero input current. If the S&H output is higher than V_{CM} , then the OCL increases its output until the input current is nulled, and vice versa [24]. The digital counter is refreshed at low frequency, 150 Hz, to meet all the bandwidth limitations imposed by the electrochemical system. A switched-capacitor analog adder adds the offset compensation output to the desired stimulus voltage, which is generated by another DAC.

The offset correction loop is activated at system startup; and is switched off during current acquisition with the final offset compensation value stored into the DAC inside the OCL.

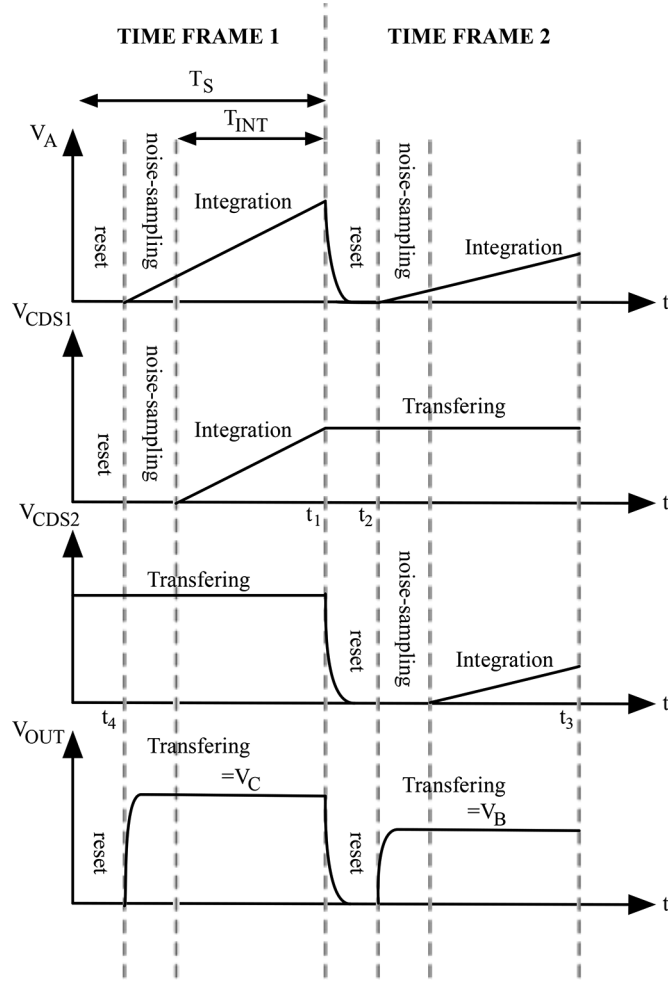


Fig. 7. Time frame subdivision phases. Each time frame lasts T_S and is divided into three phases: a reset phase, a noise sampling phase and the integration phase. The graph also explains the complementary clocked behaviour of the two CDS stages. While CDS1 is in noise sampling-phase or integration phase, CDS2 transfers the result of the previous integration phase to the output, and vice versa.

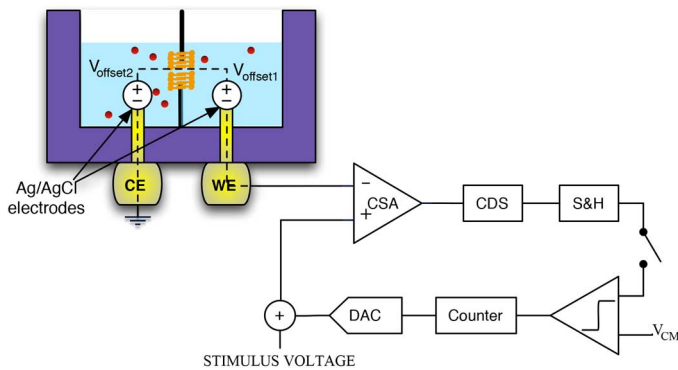


Fig. 8. Scheme of offset compensation loop. The OCL compensates for offset voltages generated at the electrode-electrolyte interfaces, both at CE and WE. Offset compensation is active at system startup. The OCL compares S&H output with V_{CM} and adjust the positive input of the CSA to eliminate the junction offsets.

D. Experimental Measurements

The measured input referred noise spectra for the four preset acquisition bandwidths are shown in Fig. 9. The lowest noise of

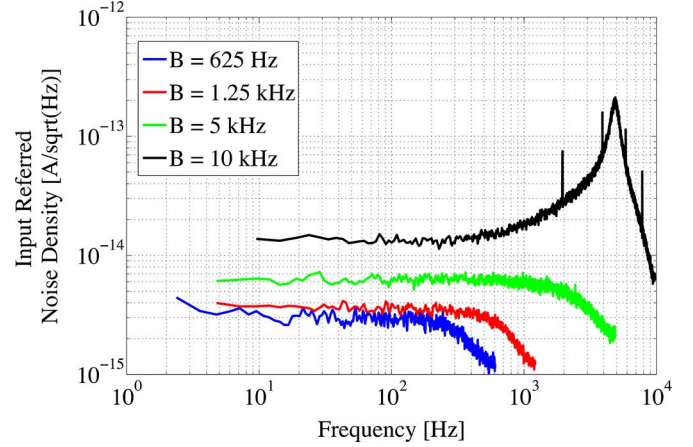


Fig. 9. Measured noise spectra for the 200 pA input range.

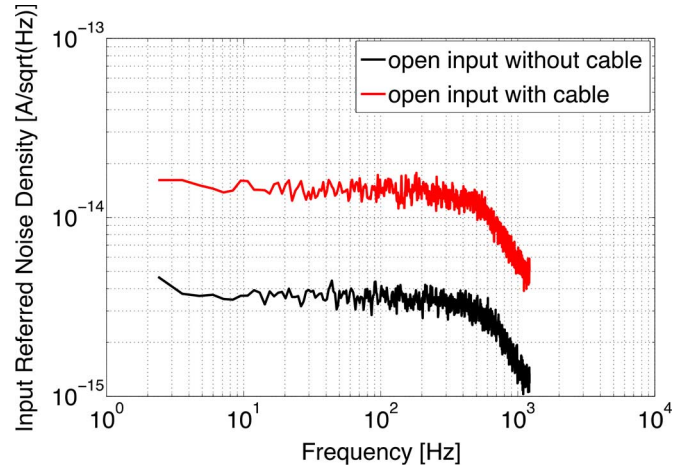


Fig. 10. Effect of a 5 cm cable at the input on the input referred noise density. Measurements were performed at 1.25 kHz on a single amplifier in open-circuit input condition. The presence of the 5 cm coaxial cable increases the input referred noise since it raises the input capacitance and collects EMI noise.

70 fA_{rms} is achieved with the 200 pA range and 625 Hz bandwidth. Note that bandwidth reduction has two effects on noise; it reduces the equivalent noise bandwidth and lowers the noise density at the same time. In fact, DT-CSA is the best solution for low-frequency current acquisition [16]. The spike in the 10 kHz noise spectrum is related to digital signal coupling [20]. The measured spectra were obtained with an open-input condition; for higher input capacitances the noise increases [16]. The integration of microfluidics with microelectronics also allows the input parasitic capacitance to be limited, since no extra connections with wires or cables are needed [25]. A low input capacitance is fundamental for low noise performance since the input-referred noise power is proportional to the input capacitance [16]. For instance, the use of 5 cm coaxial cable increases the rms noise at 1.25 kHz bandwidth from 130 fA to 470 fA, as shown in Fig. 10.

The overall gain of the amplifier (i.e., the equivalent trans-resistance R_{EQ}) suffers from CMOS process variation and this leads to differences in the gain of individual bilayer recording channels. However, this error can be easily corrected using software calibration. Apart from this issue, the CMOS current

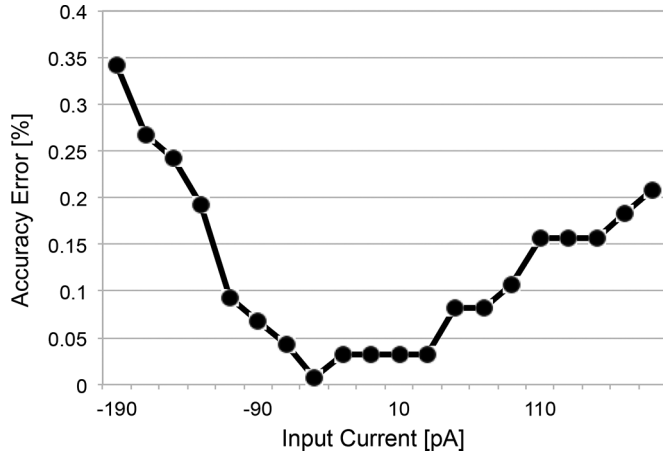


Fig. 11. Accuracy error over the entire input range.

TABLE I
PERFORMANCE OF THE CMOS CURRENT AMPLIFIER

Parameter	Value
Technology	0.35 μ m
Area	5mm ²
Total power consumption	40mW
Supply voltage	3.3 \pm 1.65V
Bandwidths	625Hz, 1.25kHz, 5kHz, 10kHz
Ranges	\pm 200pA, \pm 20nA
r.m.s. Noise @625Hz	70fA
r.m.s. Noise @1.25kHz	130fA
r.m.s. Noise @5kHz	425fA
r.m.s. Noise @10kHz	1.2pA

amplifier shows a maximum accuracy error of only 0.35% (Fig. 11). Measurements were taken with a Keithley 6514 electrometer connected in series with the CMOS current amplifier.

IV. MICROFLUIDIC DEVICE

To enable parallel recording within a compact platform, we designed a microfluidic device with a dimension of 15 \times 15 mm to hold four separate BLMs, each with its own integrated Ag/AgCl electrodes and a common Ag/AgCl electrode as shown in Fig. 13-a. Each daughter board is connected to the four BLM recording sites via contact pads on the edge of the microfluidic chip, and as depicted in Fig. 3 it can record current from 12 bilayers simultaneously. As described in [8], four microcavities, each consisting of a bottom electrode chamber and a top aperture layer were fabricated on a glass substrate using two layers of dry-film resist [26].

The bottom chambers are 150–200 μ m in diameter and approximately 55 μ m deep. The gold electrode tracks inside these chambers were electroplated with silver to produce micro-electrodes with a thickness of 5–6 μ m. These were chlorinated by immersion in FeCl₃ solution. These large Ag/AgCl electrodes enable long-term electrophysiological recording without electrode degradation [7]. A second layer of dry-film resist covers this cavity to define an aperture of 20–100 μ m diameter for the suspended bilayer.

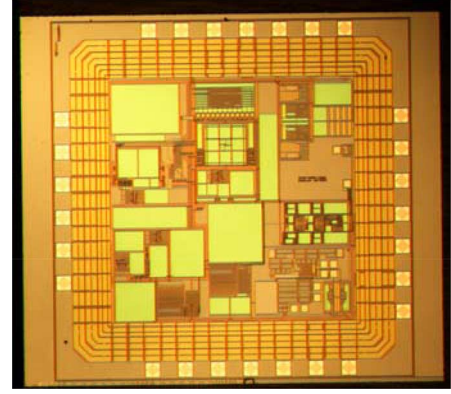


Fig. 12. Microphotograph of the chip.

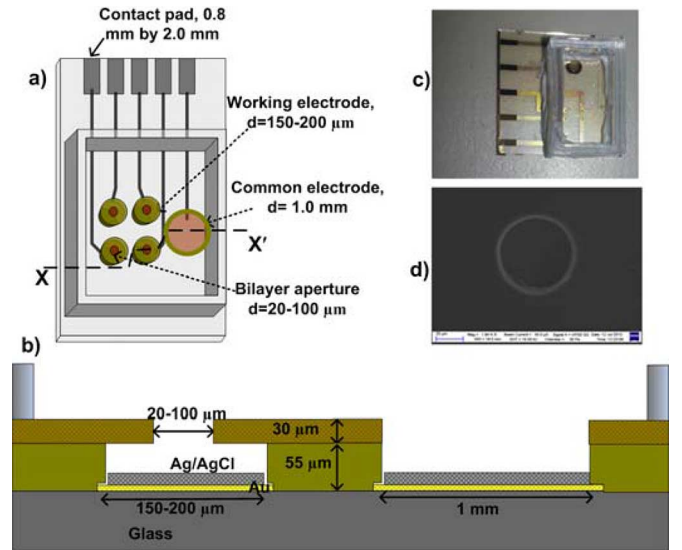


Fig. 13. (a) Top view of the microfluidic chip, showing four separate BLM working electrodes for current recording with contact pads. (b) Cross section (X-X') of the micro-electrode cavity chip showing (left) one working electrode (150–200 μ m) with the aperture for the BLM and (right) the common electrode (not to scale). (c) An image of the bilayer chip (15 \times 15 mm) with four bilayer apertures. (d) SEM image of a 50 μ m aperture.

Each microfluidic device contains four separate working electrodes (WEs) at the bottom of the four aperture-covered microcavities, and also a common reference electrode (CE) [Fig. 13(a)] connecting to the top aqueous compartment defined by an acrylic chamber, as shown in Fig. 13(c). Note that all the electrodes are on the same plane as depicted in Fig. 13(b). The CMOS current amplifiers are positioned directly next to the microfluidic device when plugged into the daughter board via the Samtec™ single row connector. This makes the overall system very compact (11.4 \times 7 \times 1.2 cm) compared to the systems that use off-the-shelf recording systems, which are tens of cm wide and deep [7], [14], [27], [28].

V. MEASUREMENT RESULTS

A. Bilayer Formation and Stability

The top aqueous compartment of the microfluidic device was filled with buffer solution (1 M KCl, 10 mM HEPES, pH 7.4) and the device was placed in a desiccator under mild vacuum to

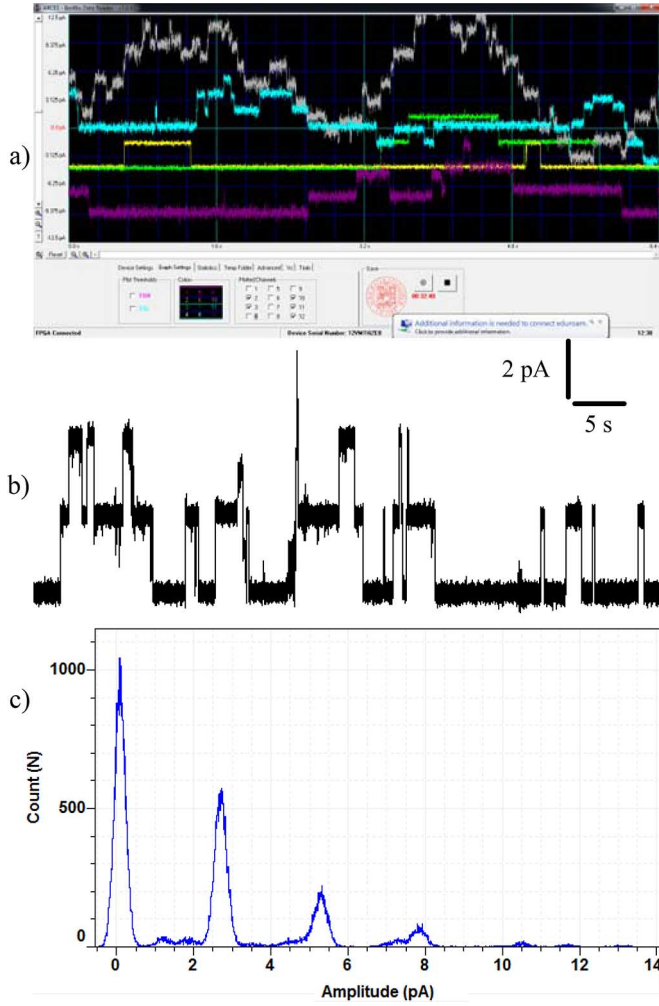


Fig. 14. (a) Screen shot of the display interface with five channels showing gramicidin A activity. (b) Segment of a current trace from one amplifier, after filtering at $f_c = 625$ Hz (c) current histogram for a 60 sec trace. The diameter of each bilayer aperture was $75 \mu\text{m}$ and a $+100$ mV potential was applied across the bilayers. The oversampling frequency was 1.25 MHz and data were filtered at 625 Hz using the FPGA built-in digital filter.

draw the buffer into the bottom compartment. The device was then connected to a daughterboard and bilayers were formed by painting a 20 mg/ml solution of phospholipid in decane over the apertures. The measured capacitance of a bilayer suspended across a $75 \mu\text{m}$ aperture was typically 15 – 20 pF, with a background capacitance of 2 – 3 pF. For a $50 \mu\text{m}$ aperture the capacitance was 10 – 15 pF. These bilayers were stable for several days; up to 10 days for a $20 \mu\text{m}$ aperture, as evaluated by continuous measurement of current (100 mV potential) and checking intermittently the bilayer capacitance.

B. Parallel Ion Channel Recording

To validate the system performance 12 channels were concurrently acquired using 3 microfluidic devices. Two microfluidic devices (8 ch) were used to observe the activity of the peptide ion channel gramicidin A, and one device (4 ch) was used to observe the protein ion channel α -hemolysin (α -HL).

Gramicidin A: A 50 pg/ml solution of gramicidin A was added to the top aqueous compartment, resulting in ion channel current steps in five of the eight painted bilayers. A screen shot

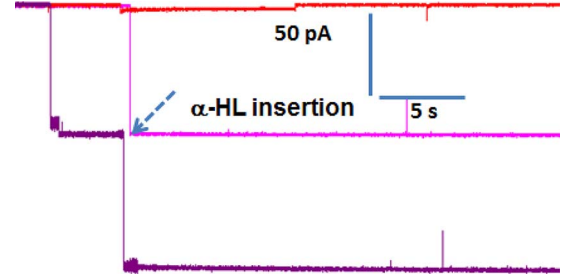


Fig. 15. The α -HL current steps @ -50 mV. The purple trace shows two α -HL current steps while the pink trace shows one current step. 1 M KCl, $f_s = 1.25$ MHz, the aperture diameter is $75 \mu\text{m}$.

of the user interface displaying the independent current signals from five bilayers out of eight with gramicidin A activity is shown in Fig. 14(a). Fig. 14(b) shows a gramicidin A current trace from a particular channel in more detail. This was filtered at 625 Hz, while Fig. 14(c) shows a current histogram of a trace that was not filtered.

The measured ion channel current steps were ~ 2.6 pA, which closely matches literature values for gramicidin A (for $+100$ mV potentials and 1 M KCl) [1]. The figure also shows that the current noise is as small as 0.5 pA p-p (0.18 pA rms) at 625 Hz, highlighting the advantage of the integrated amplifier-microfluidics approach of the platform. The current histogram for a 60 sec trace, shown in Fig. 14(c), consists of peaks at current values that are multiples of 2.6 pA, obtained from several gramicidin A channels that are open at the same time. It should be noted that for some of the amplifiers, the characteristic current amplitude of a gramicidin A channel deviated from literature values. This is related to some variability in gain between different amplifiers and can be corrected with the software, as described in Section III-C.

α -Hemolysin: To demonstrate the capability of the system to record larger current steps, a $2.5 \mu\text{g/ml}$ solution of the protein α -HL was added to the top aqueous compartment. Within 10 minutes, three of the four aperture-suspended bilayers showed current steps indicative of the insertion of one or two α -HL nanopores. Fig. 15 shows current traces from three amplifiers, recorded at a potential of -50 mV, with current steps of ~ 70 pA to ~ 150 pA. A small number of current steps was expected because α -HL does not exhibit a transition between a closed and an open state. The magnitude of the current step is in reasonable agreement with literature values for α -HL in 1 M KCl solution [11], [29], [30] demonstrating that the platform is suitable to record larger currents (>100 pA) from nanopores as well as smaller currents (<20 pA) from ion channels.

C. β -Cyclodextrin Blocking

In order to show the system performance with faster dynamics, blocking events by beta cyclodextrin (β -CD) in a α -HL nanopore has been demonstrated. Initially the bottom cavity was filled with 1 M KCl buffer solution with $100 \mu\text{M}$ β -CD. After bilayer formation α -HL was added from the top side and the resulting channel current steps with β -CD induced transient channel closures, measured at $+50$ mV, are shown in Fig. 16. The extent and the duration of channel blocking events and the

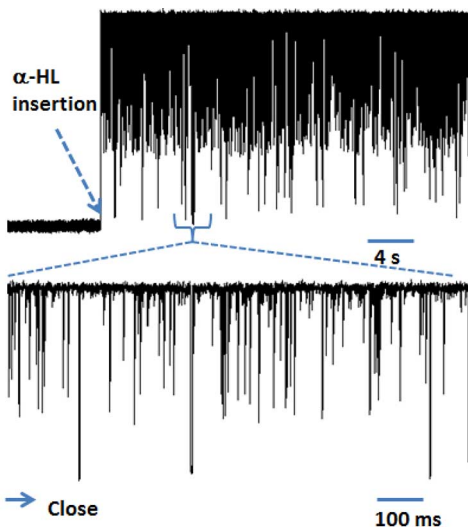


Fig. 16. The α -HL blocking by β -CD at @+50 mV. 1 M KCl, 100 μ M β -CD, fs = 1.25 MHz, and fc = 1.25 kHz, the aperture diameter is 75 μ m.

TABLE II
COMPARISON WITH STATE-OF-THE-ART PARALLEL PLATFORM FOR
BIM RECORDING

	Channels	Success Rate	Aperture Size [μm]	BLM capacitance [pF]	Embedded electronics	Max. Bandwidth [kHz]	rms Noise @ 1k Hz open input [fA]	rms Noise @ 1k Hz with BLM [fA]
	12	66%	20 - 100	15 - 20	Yes	10	100	240
[5]	12	-	200	-	Yes	4	200	4000
[6]	96	46%	30	-	No	-	-	-
[25]	8	-	15	6 - 25	Yes	1MHz	320	2280
[31]	12	90%	30	-	No	-	-	1000
[32]	64	-	-	-	Yes	20	-	-
[33]	48	-	-	-	No	20	1600	-
[34]	1	-	-	-	No	20	173	-
[35]	1	-	-	-	No	100	15	-

frequency with which these occur can be easily identified from the processed data and agree with the literature [5].

D. State-of-the-Art Comparison

Table II compares the performance of our system with state-of-the-art parallel BLM platforms. To our knowledge, there are few parallel architectures for BLM recording reported in the literature in [5], [6], [25] and [31]. Among these, only

[25] integrates microfluidics and electronics in the same system. However, our integrated platform has the best noise performance. To further understand the performance of the system, Table II compares our system also with state-of-the-art commercial instruments. Ionflux-HT offers the highest throughput with 64 parallel channels, but our system could be scaled to 64 channels or more. The Axon Axopatch 200B is the benchmark instrument for low-noise current acquisition with only 15 fArms noise at 1 kHz. Our system is noisier than Axon but offers parallel acquisition of ion-channel activity.

VI. CONCLUSION

We have described a parallel 12-channel system capable of recording from single ion channels. The system uses a commercial FPGA for digital processing, a custom-made CMOS amplifier for low-noise current acquisition and novel disposable microfluidic chips for BLM formation. Modularity of the platform permits easy parallelization, enabling high-throughput BLM recording. The CMOS low-noise current amplifier is based on a novel noise cancellation technique which very effectively eliminates flicker noise derived from devices under test and from the amplifiers. Input-referred noise is as low as 70 fArms at 625 Hz (100 fArms in 1 kHz) and maximum acquisition bandwidth is 10 kHz. The microfluidic device, made on a glass substrate, is only 15 mm by 15 mm, accommodates 4 bilayers and integrates in a very simple way with the recording electronics.

Ion channel recording with either gramicidin A or α -hemolysin has been obtained, demonstrating the ability of the system to concurrently record from different kinds of ion-channels. In proof of principle experiments, eight bilayers out of 12 demonstrated protein insertion, representing a success rate of 66%.

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