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UNIVERSITY OF SOUTHAMPTON

FACULTY OF PHYSICAL AND APPLIED SCIENCE

School of Electronics and Computer Science

# A STUDY ON THE EFFECTS OF VARIABILITY ON PERFORMANCE OF CNFET BASED DIGITAL CIRCUITS

By

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A thesis submitted for the degree of Doctor of Philosophy

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ABSTRACT

FACULTY OF PHYSICAL AND APPLIED SCIENCE

SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

**A STUDY ON THE EFFECTS OF VARIABILITY ON PERFORMANCE OF CNFET BASED DIGITAL CIRCUITS**

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With the continuous trend of reducing feature sizes, and employing continuously smaller components on integrated circuits, new challenges arise on the way of silicon CMOS circuits and devices. Emerging "nanodevices" promise the possibility of increased integration density and reduced power consumption. The emerging and new devices, partially due to their extremely small dimensions, show large variations in their behaviour. The variation shown by these devices affects their reliability and the performance of circuits made from them. The Carbon Nano-Tube (CNT) is one such device which is also the device of choice in this work. This work is concerned with building reliable systems out of these unreliable components. The work was done in HSPICE with the help of the Stanford CNFET model. Logic gates are implemented using CNT Field Effect Transistors (CNFETs) which are in turn made from CNTs with different physical attributes. Given a CNT manufacturing process, there exists a mean and standard deviation (STD) for the diameter distribution of the manufactured CNTs which depend on the accuracy of the manufacturing process

In the first part of this work, CNTs with different mean diameters and standard deviations (STD) in their diameter distribution are considered. Simulation results show that logic gates made from CNTs with larger mean and smaller STDs in their diameter distribution show less variation in their timing behaviour (propagation delay, rise and fall times) and a promise of more reliable operation.

Alternative structures were then explored in the form of multiplexers and XOR gates. It is shown that these structures have the advantage over the gates studied previously in that they exhibit similar rise and fall transition times and hence are better suited to CNFET-based circuit design.

The next stage of this work involves implementation and simulation of a memory structure (SRAM). Parameters such as Static Noise Margin (SNM), leakage power and read/write delays were studied and the effects of CNT diameter variation on them examined.

The next contributions of this work are empirical models developed for a library of CNFET-based logic gates/circuit structures. The models can predict both the mean and standard deviation (STD) in various circuit performance parameters of a given CNFET-based logic gate/SRAM given the mean and STD of the diameter of CNTs used in their manufacture. The aim is, given a target reliability specification (timing requirements, power, speed, etc.), for various logic gates, and larger circuit components, to come up with a design strategy to suggest what physical properties the nano-device of choice should have to meet the target specification or vice versa. Best-case CNT diameter mean and STD selection scenarios are proposed to minimise circuit parameter variations.

In the last part of this work, the effects of doping fluctuations in the source/drain regions of the CNFETs on the performance of logic gates made from them are studied. The work concludes that if doping concentration is kept above 1%, variation in doping concentration has a minimal effect on performance parameters.

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# Chapter 1 Introduction

## 1.1 Motivation

Silicon device scaling in future faces limitations. As the silicon industry moves into the 45nm node and beyond, increasing technology challenges will be imposed by silicon CMOS device scaling. Among the most important obstacles against further device scaling is the performance variation introduced by increased process variations as feature sizes shrink and the standby power dissipation [1]. Increased device density and device parametric variation, rising sub-threshold leakage current and gate tunnelling current and higher device temperatures all contribute to the power problem. As CMOS approaches the 25nm node, stochastic threshold variation caused by dopant implant position in ultra-small inversion regions [2] will give rise to more than 100mV of threshold variation. The timing behaviour of devices is also greatly affected by spatial and temporal process parameter tolerance and voltage and temperature variation. Continued channel length reduction is prevented by the limitation to reduce gate insulator thickness. This leads to a lack of control over static leakage, short channel effects and drain voltage induced barrier lowering.

Short channel effects occur in devices where the channel length is of the same order of magnitude as the source/drain region depths. This can have a number of consequences including velocity saturation, drain-induced barrier lowering (DIBL) and charge sharing. Velocity saturation occurs when the carriers in a short channel device become velocity saturated due to the high electric field in the channel region. As the applied electric field is increased beyond the point of velocity saturation, carrier velocity no longer increases as carrier energy is lost through increased lattice collisions. DIBL is also an issue; as the source and drain get closer, they become electrostatically coupled, so that the drain bias can affect the potential barrier to carrier flow at the source junction. This leads to an increase in both off-current and sub-threshold slope. As a result, threshold voltage is reduced.

In a short channel device, a large proportion of the electric field lines associated with the depletion region is terminated on the source and drain junctions. This 2 dimensional sharing of the depleted substrate charge between the source, drain and gate terminals dramatically affects device

behaviour. As channel length shrinks, increased charge sharing from source/drain degrades the controllability of gate voltage over channel current. The reduced control of the gate over the channel depletion region in turn reduces the threshold voltage. The threshold voltage is the minimum value of gate to source voltage which is required to allow current to flow (refer to section 2.2).

Floating body effects are observed in silicon on insulator devices. Holes generated by impact ionisation in an n-type device accumulate in the body. The collection of these carriers increases the body potential and lowers the threshold voltage of the device. This phenomenon can however arise in any MOS device with the body floating.

Three primary approaches for addressing these challenges are put forward [1, 3]:

- Extending silicon scaling through innovations in materials and device structure;
- Expanding the level of integration through 3-dimensional structures comprised of silicon through-via holes and chip stacking in order to enhance functionality and parallelism;
- Exploring post-silicon CMOS innovation with new nano-devices based on distinctly different principles of physics, new materials, and new processes, such as spin-dependent electronics (spintronics) [4], carbon nanotubes, nanowires [5], or molecular systems which utilise the molecular electrostatic potentials and vibrational states of molecules to perform logical operations and transmit signals [6].

The issue of power consumption could be addressed by reducing the operating voltage albeit increasing delay [7]. Supply voltage reduction mitigates active as well as static power, but low voltage operation requires adding complexity in supply distribution and modulation [1]. If however, the issue of power consumption can be managed, it is variability that becomes the ultimate challenge in the way of scaling [1]. What the optimal device/technology of the future will be, depends to a great extent on how critically its performance varies with process variations.

Emerging and future devices exhibit dimensions in the order of the de-Broglie wavelength of electrons [8]. These include single electron transistors [8], electrons confined to sufficiently small dimensions and allowed to tunnel to metallic leads; silicon nanowires [5] which are extremely thin silicon wires that form a transistor’s channel; graphene sheet transistors [9] which utilise the very fast carrier transport of monolayer graphene; and carbon nanotubes (CNTs) [10]. The extremely

small scales mean that the behaviour of these devices is no longer governed by the classical laws of physics; rather it is dictated by quantum physics [10]. As quantum physics is probabilistic in nature, these new devices in most cases are likely to be very unpredictable and unreliable. Any electronic system based on these devices will in turn be prone to noise and disturbances such Single Event Upsets (SEUs). At the nanoscale SEUs can be caused by thermal noise as well as radiated particles. A foreign particle can cause a register on a digital integrated circuit to accidentally change its state. Thermal noise at room temperature could prevent the output of a combinational block to be sampled correctly by the subsequent register, at the rising or falling edge of the clock.

Some key advantages of employing CNTs over silicon for building transistors include:

- High carrier mobility
- High current density
- High gate capacitance
- Compatibility with high-k gate dielectrics

Disadvantages include issues with reliability and mass production. It is difficult to produce significant amounts of semi-conducting CNTs without the presence of unwanted metallic CNTs.

Appropriate circuit design methods and process development strategies have to be devised in order to tackle the abovementioned issues on power dissipation and variability. This work concentrates on the CNT as one of the most promising of emerging nanodevices. Though holding a great promise for future electronics, CNTs are extremely prone to various sources of variations. As the electrical characteristics of CNTs are directly related to their physical structure, atomic structural changes can translate into significant variation in their electronic behaviour. This work aims to facilitate CNT-based design in the presence of CNT diameter and doping variations. To achieve this, an exhaustive study is carried out to examine the effects of CNT physical characteristics variations on circuit performance variables. The effect of CNT diameter variations on performance parameters (delay, power consumption, etc.) of various logic and memory structures is studied in depth. Through various simulation strategies, an optimum CNT mean diameter for use in CNT-based logic design is put forward for the first time. Further, novel mathematical models for the prediction of delay behaviour of CNT-based circuits in the presence of diameter variations are developed.

## 1.2 The Carbon Nanotube

A CNT is a hollow cylinder constructed by rolling up a sheet of graphene. Graphene is a single atomic layer of graphite which in turn is a crystalline form of carbon. Its conducting properties are determined by the nature of the electronic states near the Fermi energy ($E_F$) which is the energy of the highest occupied electronic state at absolute zero. All bonds in a CNT are satisfied and the surface is atomically smooth, hence, there is no scattering of carriers by surface states and the roughness that plagues conventional FETs at high voltages is also absent [11]. With their ultra-long mean-free paths (~ μm) for elastic scattering, CNTs are good candidates for use in electronics [12-15]. The quasi-ballistic nature of carrier movement in a CNT [12] means that electrons are confined in the radial and circumferential directions and are only free to move along the direction of the tube axis [16], hence only forward and backward scattering due to electron-phonon interactions are possible for carriers. This gives CNTs unique electrical properties. CNTs' electrical conductivity can be varied by doping them with impurity atoms. In this way both p-type and n-type CNTs can be obtained which then enables the creation of complementary logic structures such as those adopted in conventional CMOS design. In graphite (and hence in CNTs) the atoms of carbon are very closely packed in the basal planes, the distance between their centres (nearest neighbour distance) being only 1.42 Å, which is even closer than in diamond. One consequence of this small nearest-neighbour distance is that impurity species are unlikely to enter the covalently bonded in-plane lattice sites substitutionally [17] but rather occupy some interstitial position between the graphene layer planes which are bonded by a weak van der Waals force. The only impurity atom that can easily do this is boron, hence, CNTs are usually doped using boron atoms; however, alkali metals and halogens such as bromine and iodine are also used. CNTs can exhibit either semiconducting or metallic behaviour depending on their chiral angle. The conductivity and robustness of metallic nano-tubes make them suitable for future interconnects. As for the semiconducting CNTs, they exhibit the desired properties for making field effect transistors. The restricting issue here is to selectively separate metallic and semiconducting CNTs. A number of methods have been proposed for the separation of metallic and semiconducting CNTs including [18, 19]. In [20] a new method for separation of metallic and semiconducting CNTs proposes selective suspension in aqueous sodium dodecyl sulphate according to electronic

structure. A recent work by IBM [21] utilises this separation technique and achieves a high-density integration of CNTs allowing wafer-scale integration using highly purified CNTs.

Continuous films of Single Walled Carbon Nanotubes (SWCNTs) can be produced by dielectrophoretic deposition onto interdigitated electrode arrays. SWNCTs produced this way possess a significantly different degree of alignment with respect to the electric field. The dependence of SWCNT alignment on the electric field allows the separation of metallic and semiconducting SWCNTs using electrode-less dielectrophoresis through nanopores.

Another technological challenge is the capability to precisely place CNTs on wafer. The inability to absolutely control the alignment of CNTs under the metal gate affects the functionality of CNT-based cells. Current technology cannot eliminate all misaligned CNTs at the physical level; hence, this problem is normally addressed at the design level. This means that the layout of these standard cells must incorporate fault tolerant techniques and be designed robust enough to overcome probable misalignments at the physical level.

Electrophoresis has been employed for separating CNTs according mainly to their electrical properties (metallic or semiconducting) together with length and diameter. Charged macromolecules are commonly separated by electrophoresis using gel in an electric field. To be able to process the CNTs in the gel, they would have to be individually dispersed with the aid of a surfactant such as sodium dodecylsulfonate. The metallic/semiconducting separation using this technique utilises different polarisable characters between them under an electric field. Dielectrophoresis was first used for the alignment and purification of CNT bundles in isopropyl alcohol [22, 23]. It was extended to separation of individually dispersed CNTs.

CNTs, due to their advantages over other new devices, amongst which are their very high performance and integration capabilities are emerging as the dominant future nano-electronic device. Actual CNT samples are usually found in one of two forms: Multi-Wall Carbon Nanotubes (MWCNTs) or Single Wall Carbon Nanotubes (SWCNTs).

*1.2.1 SWCNT*

SWCNTs are carbon nano-tubes made of a single layer of graphene. SWCNTs can be produced by laser vaporisation method or the carbon arc method in the presence of metal catalysts such as the transition metals Fe, Co, or Ni [17]. Typical SWCNT diameters range from 1 to 3 nanometres (nm) [17] and the chiral angle ranges from 0 to 30 degrees. Two of the most important physical properties of CNTs are their diameter and the chiral angle. The vectors $a_1$ and $a_2$ shown in fig. 1.1 are unit vectors and $n$ and $m$ are integers. $C_h$ is the axis along which the graphene sheet is rolled up to form the CNT and is called the chiral vector. The chiral angle of a nanotube is defined as the angle between the vector $C_h$ and the vector $a_1$. Although graphene is a zero band-gap semiconductor, SWCNTs can be metals or semiconductors with different size energy gaps, depending on the diameter and chirality of the tubes, i.e. on the indices $(n,m)$. Generally $(n,n)$ tubes are metals, also known as armchair CNTs; $(n, m)$ tubes with $n\text{-}m = 3j$, where $j$ is a nonzero integer, are very tiny band-gap semiconductors and all others are large band-gap semiconductors. $(n, 0)$ tubes are zigzag and $(n,m)$ tubes are chiral. Zigzag and chiral CNTs are metallic when $(n\text{-}m)/3$ is an integer and semiconducting otherwise. Energy band gap is important as it determines the ease with which charge carriers can move from one energy band to the other and hence determines the conductivity of the material. A smaller band gap means that a transistor made of CNTs with larger diameters can exhibit higher on-currents

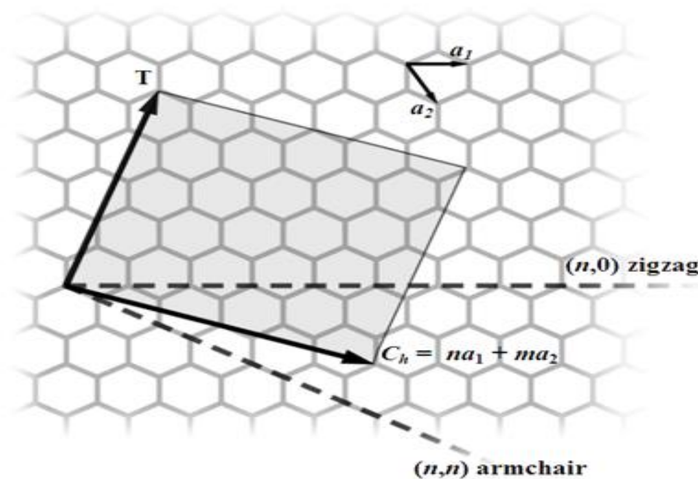


**Figure 1.1: The honeycomb lattice of a CNT [19]**

*1.2.2 MWCNT*

A MWCNT consists of a nested coaxial array of SWCNTs separated from one another by approximately 0.34nm, the interlayer distance of graphite. Unlike SWCNTs which require a catalyst for their growth MWCNT production requires no catalyst [17]. In [24] it has been shown that interlayer coupling has little effect on the electronic properties of individual SWCNTs. Thus, two coaxial zigzag CNTs that would be metallic as SWCNTs yield a metallic double-wall tube. Semiconducting tubes behave similarly. They also showed that coaxial metallic-semiconducting and semiconducting-metallic tubes retained their respective characters when interlayer interactions were introduced suggesting that double walled CNTs could be used as insulated nanowires. Subsequent works [25, 26] considering a double-wall CNT consisting of two metallic SWCNTs looked at the effect of changing the relative position of one tube with respect to the other found that in certain configurations the interlayer interactions can cause both SWCNTs to become semiconducting. These experiments underline the fact that further work needs to be done to determine the electronic properties of multi-wall zigzag and chiral CNTs.

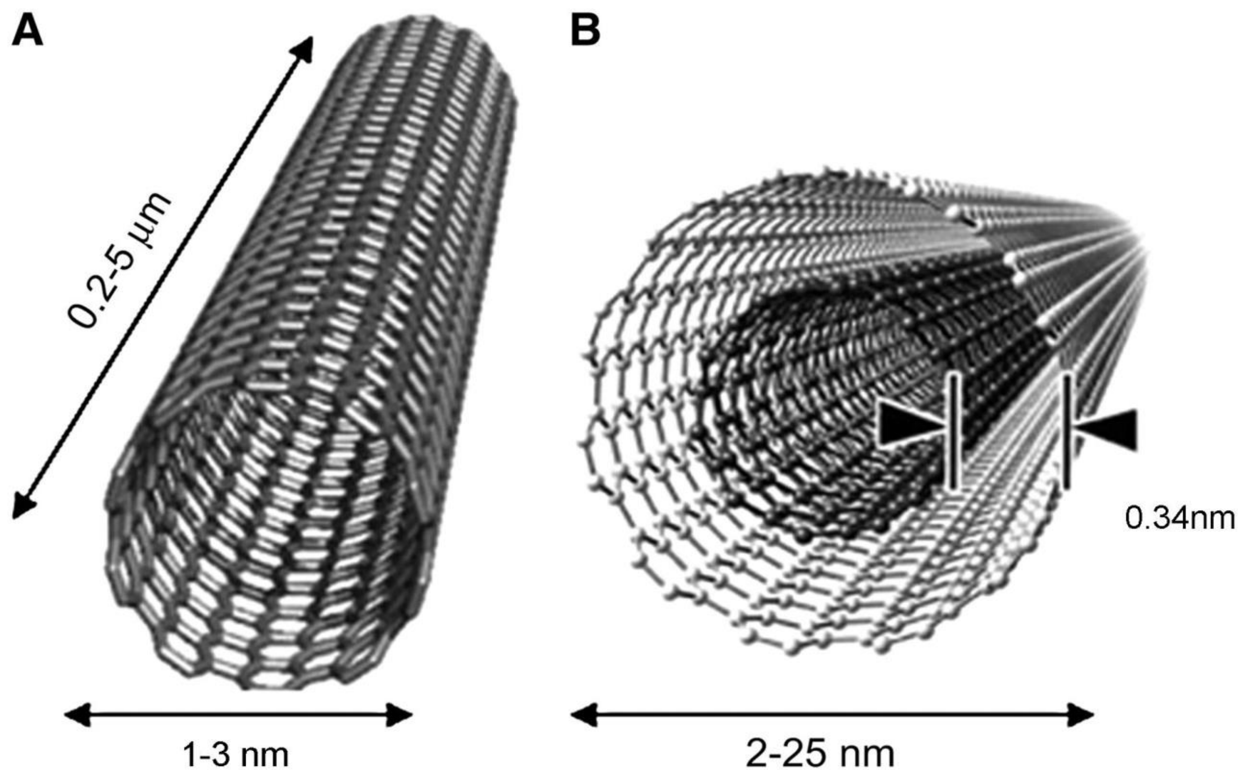


**Figure 1.2: Structure of SWCNT (A) and MWCNT (B)**

## 1.3 Applications of Carbon Nanotubes

The potential of CNTs for developing high-speed and power-efficient logic applications is vast [21]. Ensembles of nano-tubes have been used for field emission based flat-panel displays [17], composite materials with improved mechanical properties and electromechanical actuators [17]. Bulk quantities of CNTs have been suggested to be useful as high capacity hydrogen storage media [17]. Nanotubes have also been used for field emission sources, tips for scanning probe microscopy and nano-tweezers [17]. Nano-tubes have significant potential as the central elements of nano-electronic devices such as field effect transistors [17]. These CNT based transistors have been utilised recently to implement various electronic structures such as logic gates and memory structures. Intercalated CNTs could also be used in super high capacity batteries.

CNTs have been shown to have potential benefits in medicine too. SWCNTs with a diameter of 1.4nm have shown potential for targeted delivery of radionuclides to cancer cells in the field of nuclear medicine [27].

Since CNT electronic properties are strong functions of atomic structure, mechanical deformations or chemical doping can induce strong changes in conductance. Such changes can be easily detected by electron current signals making CNTs suitable for VLSI application as extremely small sensors sensitive to their chemical and mechanical environments [28].

## 1.4 Thesis Outline

This work is motivated by the need for nano-electronic circuitry, such as logic and memory structures, based on CNTs to operate in spite of the inherent variations which exist due to the nature and size of these nanodevices. As variations in structural properties of CNTs can cause significant variation in the electrical properties of these devices, it is envisaged that any electronic component based on these nano-devices would be prone to variations in circuit speed and power consumption. Therefore there is a need for the circuit designer to be able to predict the performance of a design based on the CNT structural properties and their variations.

Chapter 2 gives an overview of the various techniques for the fabrication of CNTs together with their advantages and disadvantages. The doping of CNTs is also discussed together with the types

and properties of field-effect transistors (FETs) that can be made using CNTs. Various existing models for CNFETs are then discussed together with their strengths and shortcomings. Construction of logic structures from CNFETs is then discussed and the design challenges are identified.

In Chapter 3, the electrical behaviour of basic CNT-based logic gates is studied through Monte Carlo and parametric simulations. It is shown that time delay and power consumption of NOT, NAND and NOR gates are direct functions of variation in CNT diameter. As the first contribution of this work, a CNT diameter threshold is suggested in order to keep delay variation to a minimum. This threshold diameter is valid for all the logic gates studied in this chapter. The second contribution of this chapter is in the form of mathematical models developed for the prediction of mean and STD in propagation delay based on given CNT diameter mean and STD for the various logic gates.

In Chapter 4 more complex logic structures i.e. multiplexers and XOR gates are studied under the presence of CNT diameter variations. It is suggested that the use of the specific structures for multiplexers and XOR gates detailed in this chapter would be advantageous for CNT-based design as the structures discussed exhibit similar rise and fall times. Propagation delay, fall/rise time and power consumption of these structures are examined. It's found that time delay rises sharply below a CNT diameter of 0.85nm, a threshold consistent with that observed in Chapter 3. The chapter further examines power consumption, delay and energy variations in the presence of CNT diameter mean and STD variation. Finally mathematical models based on Response Surface Methodology technique have been developed to model and predict the mean propagation delay and STD in propagation delay of the multiplexers and the XOR gates based on CNT diameter mean and STD.

Chapter 5 is concerned with the performance of a CNT-based SRAM cell. SRAM performance parameters such as delay, Static Noise Margin (SNM), Write Margin (WM) and standby leakage power are studied in the presence of CNT diameter variations. It is observed that read and write delay are reduced with larger CNT diameters and that delay values show a sharp rise below a CNT diameter of 0.85nm. It is further revealed that as SNM depends on threshold voltage, and threshold voltage is determined by CNT diameter, diameter variations cause significant variation in SRAM SNM. As far as leakage is concerned, standby leakage power rises sharply above a CNT diameter of 1.5nm, but below this value it is relatively constant. Predictive statistical models are developed

for the various performance parameters of the SRAM discussed in this chapter and shown to be reliable and accurate through the adjusted $R^2$ measure.

Predictive models for mean propagation delay and Standard Deviation (STD) in propagation delay are developed in this work. These models will work as guidelines for the logic designer to forecast the performance of a design based on the mean and STD in distribution of fabricated CNT diameters given by a certain technology.

Contributions of this work are:

- The Stanford CNFET model has been modified to allow for easier and fault-free simulations of semi-conducting CNT diameter variations.
- A comprehensive study on the effects of CNT diameter variations on various circuit performance parameters such as delay characteristics and power consumption is carried out.
- A relation is proposed by which a minimum mean CNT diameter can be chosen to ensure minimum delay variation for various CNT-based logic gates.
- A CNT-based SRAM is designed and simulated. The effects of CNT diameter variations on the delay characteristics, stability metrics and power consumption of the SRAM cell have been studied.
- Predictive models have been developed to relate the various CNT-based circuit performance metrics to CNT diameter and variations in CNT diameter.
- Effects of doping fluctuations on CNT-based logic gates have been studied.

# Chapter 2 Literature Review

## 2.1 Background

Carbon filaments having diameters of less than 10nm were first prepared in the 1970s through the synthesis of vapour grown carbon fibres by the decomposition of hydrocarbons at high temperatures in presence of transition metal catalyst particles of less than 10nm in diameter [29, 30]. However, it was the publication of Ijima's work in 1991 [31] that launched the field of Carbon Nanotubes.

Three principal techniques for synthesis of SWCNTs exist

- Laser ablation [32]
- Electric arc discharge [33, 34]
- Chemical Vapour Deposition (CVD) [35, 36]

Laser ablation and arc-discharge techniques involve the condensation of hot gaseous carbon atoms generated from the evaporation of solid carbon. The downside of these two techniques is the large amount of energy consumption and the sophisticated equipment required [35, 36]. Also both these techniques are limited in the volume of sample they can produce in comparison with the size of the carbon source. Furthermore, more impurities accompany the CNTs generated in the form of amorphous carbon and catalyst particles because of the high temperature nature of the heat source. Laser ablation and arc discharge produce mainly MWCNTs which are poorly aligned as a result of limited control over the synthesis techniques.

The prominent industrial approach for CNT synthesis is CVD. The technique is the irreversible deposition of a solid form of a gas or mixture of gases through a heterogeneous chemical reaction. The growth process can be controlled either by diffusion or by surface kinetics. CVD is the preferred technique for fabrication of thin layers of metals, insulators and semiconductors on various substrates [37-39]. CVD has the highest yield out of the other synthesis techniques and produces the lowest impurity CNTs at moderate temperatures. Also because of the equilibrium nature of the chemical reactions involved, CVD provides better growth control. Finally, CVD has

the capability to control the size, shape and alignment of the CNTs through patterning of the catalysts on the substrate's surface [40].

Both SWCNTs and MWCNTs can be doped by either electron donors or electron acceptors [40]. Performance improvement especially in the on state of CNFETs by chemically doping the CNT to n-type has been demonstrated experimentally [41]. As-grown p-type CNT devices have been converted to n-type devices by controlled doping [42, 43]. Doped CNTs exhibit high on currents [42, 43]. To obtain MOSFET-like contacts in a 50 nm CNT, a doping concentration value of ($5\times10^{-3}$) or higher dopants per atom is required [44].

CNTs can exhibit ambipolar behaviour. Ambipolar conduction is characterized by a superposition of electron and hole currents. Ambipolar behaviour has been reported in carbon nanotube field effect transistors (CNFETs) [10]. As opposed to unipolar silicon CMOS devices whose p-type or n-type behaviour is determined during fabrication, the polarity of ambipolar devices can be switched from n-type to p-type by changing the gate bias [45]. The electrostatic field applied at the back gate of the CNT-to-metal contacts is responsible for controlling the device polarity. Because CNT ambipolarity can be controlled in-field, this property of CNT devices can be utilized for building libraries of complex logic gates that efficiently embed XOR functions [46]. However ambipolar behaviour is unsuitable for CMOS as the switching activity of ambipolar devices cannot be controlled in the same way as the switching of unipolar devices can.

## 2.2 CNT Field Effect Transistors (CNFETs)

CNTs have been used to build Carbon Nanotube Field Effect Transistors (CNFETs). As described earlier, a CNT has an atomic and electronic structure that gives it unique advantages as a FET channel. These include low scattering of carriers and long mean free paths [14]. Its small diameter enhances the gate's ability to control the potential of the channel [11].

The first CNFETs were fabricated in 1998 [47, 48]. These were based on individual CNTs. Since then CNFETs have been shown to be suitable for the fabrication of circuits, sensors and NanoElectroMechanical Systems (NEMS) [48-50]. A primary advantage of CNFETs over silicon MOSFETs is their much lower capacitance value (roughly 0.05 aF/nm) which alleviates the power dissipation problem that limits the scaling of MOSFETs [11]. CNFETs can be used in conjunction with high-k gate dielectric material; also, in MOSFET-like CNFETs, the gate and source/drain can

be separated by the length of the source/drain extension region which greatly reduces the parasitic capacitance. Dynamic switching of a device takes energy of ½ $CV^2$ where $C$ represents capacitance and $V$ is the voltage.

During the fabrication of a CNFET, parallel CNTs are grown on or transferred to a silicon oxide substrate [52]. The regions of the CNTs under the gate are undoped. The conductivity of these undoped regions is controlled by the gate. The source and drain regions of the CNTs are heavily doped. The gate, source and drain contacts and interconnects are defined by conventional lithography. In this way, a large proportion of the existing design and manufacturing structure for FET-based large-scale electronics systems can be utilized [53].

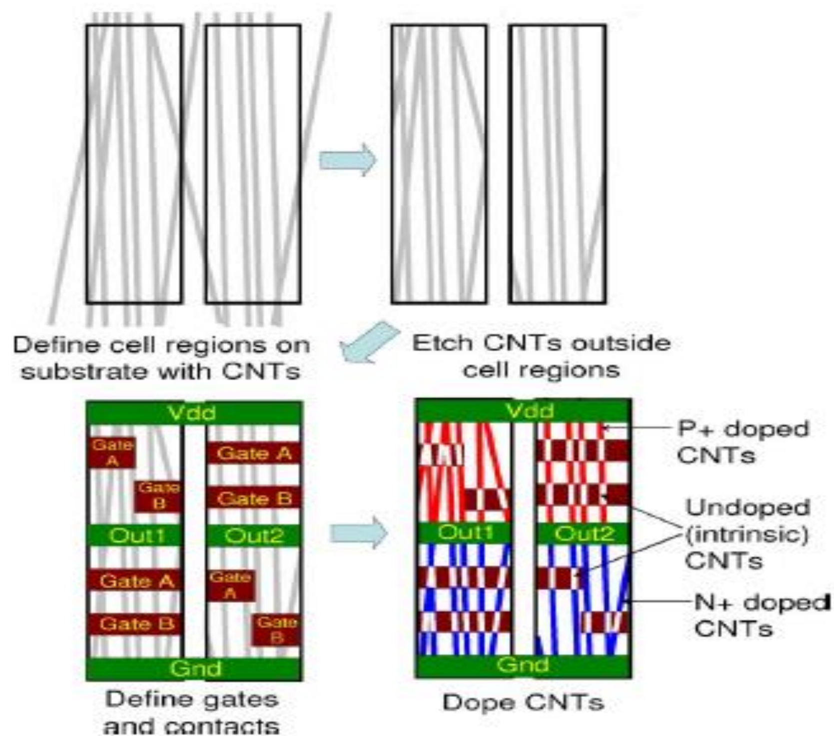


**Figure 2.1: CNFET circuit fabrication process [53]**

The process of manufacturing CNFET circuits involves growth or transfer of semiconducting CNTs on a substrate. The regions of logic cells are defined using lithography, and CNTs outside these cell regions are etched away. The gate and contact regions are subsequently defined using lithography and CNTs outside these regions are etched away. The next step involves p-type doping of CNT regions which correspond to PFET transistors, while lithographically masking the NFET regions. Then CNT regions corresponding to NFET transistors are doped n-type, while masking

the PFET regions. The CNT regions under the gates remain undoped as they are masked during the doping steps in this self-aligned process. Interconnects are defined using lithography at the final stage of the process.

**Figure 2.2: CNFET cross section [54]**

The fundamental operation of the CNFET is similar to conventional silicon devices. They are normally 3 terminal devices which employ semiconducting CNTs acting as the conducting channel between the source and drain contacts. The metal gate is used to electrostatically turn the device on or off (fig. 2.4).

Two alternative device configurations are prominent:

- Schottky Barrier (SB) FET [55]
- MOSFET-like FETs [56, 57].

In SB-CNFETs, metal source/drain contacts are directly connected to the gate controlled CNT channel [58] and hence a Schottky barrier is formed at the junction of CNT and Source/Drain contact (fig. 2.3). Compact models for SB-CNFETs have been reported [59]. SB-CNFETs show ambipolar behaviour [60] which is undesirable as far as complementary logic design goes because it contributes to higher leakage [60] as a parasitic current due to holes can flow easily. The SB contact reduces the ON current by reducing the effective voltage across the channel, thus lowering the $I_{on}/I_{off}$ ratio [61].

In MOSFET-like CNFETs, the ungated portions of the structure are doped and thus the structure behaves similarly to CMOS transistors (fig. 2.3). MOSFET-like CNFETs show unipolar behaviour and as far as fabrication is concerned they are easier to make (fig. 2.3).

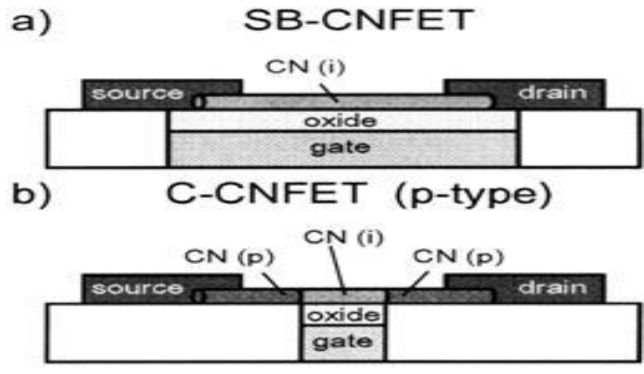


**Figure 2.3: (a) gating occurs over entire nano-tube channel. (b) p/i/p doping profile exists along the tube in a MOSFET-like CNFET. Only the intrinsic portion of the nano-tube is gated [58]**

Fig. 2.4 shows the cross section of the channel region in a CNFET. In this figure, 'd' denotes the diameter of a CNT and '*h*' is the distance between the metal gate and the centre of a CNT. 's' is inter-CNT separation. '$C_{gc}$' is gate to channel capacitance. $C_{gc_m}$ and $C_{gc_e}$ denote the gate capacitance to middle and edge CNT channels respectively.

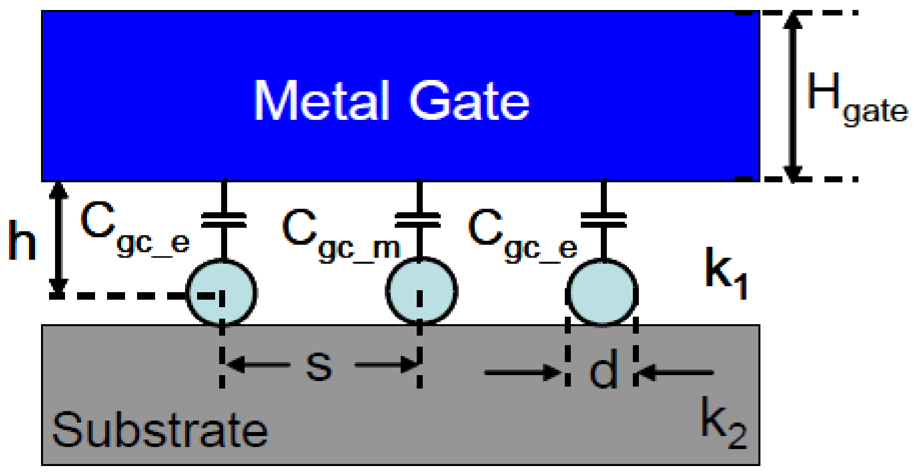


**Figure 2.4: Cross section of a CNFET**

The intrinsic CNTs act as the undoped channel region of the CNFET. The other regions are heavily doped and act as the source/drain extension regions and/or interconnect between two adjacent devices. In the limit of near-ballistic transport, the drive current highly depends on $C_{gc.}$ As a MOSFET-like CNFET, the structure shown in fig. 2.4 operates on the basis of barrier height modulation by application of a gate potential. The current of a CNFET depends on the number, position and the spacing of CNTs under the gate.

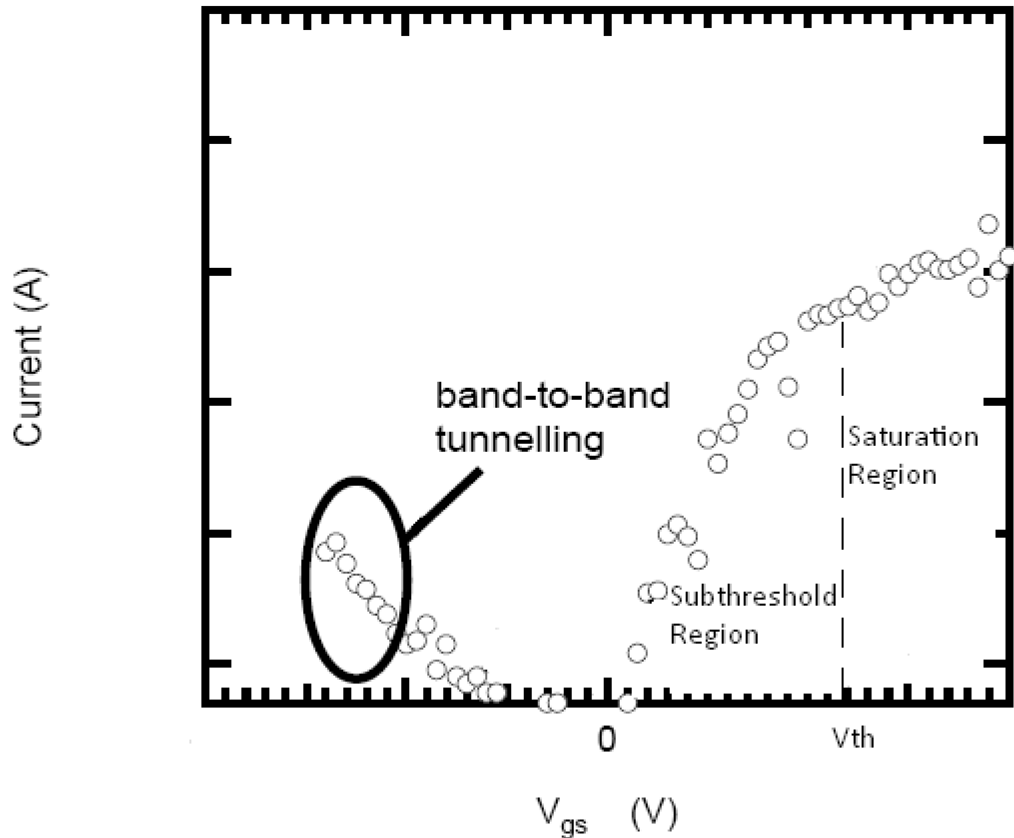


**Figure 2.5: Transistor sub-threshold plot showing drain current against voltage [45]**

Plot of fig. 2.5 shows a plot of drain current versus gate to source voltage for a CNFET. The transition from the ON state to the OFF state is gradual. Current rises exponentially before threshold voltage ($V_{th}$) is reached. This current is essentially the channel-source PN junction current. An important consideration from this observation is that a low threshold voltage is desired for high ON current; however, as it can be observed from the plot, to keep OFF current to a minimum, a high $V_{th}$ is required. The slope of the plot in the sub-threshold region is called the sub-threshold slope. A steep sub-threshold slope indicates faster switching for the device.

## 2.3 Existing CNFET Models

Many of the developed CNFET models are numerical, involving self-consistent equations which circuit solvers like SPICE are not able to handle. As these models show the essential physics of an individual CNFET, they are not suitable from a circuit designer's point of view and for logic level simulations. To evaluate the potential of CNFET-based structures to replace silicon CMOS technologies in digital circuits, a semi-empirical SPICE model for CNTFET logic is proposed in [63]. Another circuit-compatible model of ballistic CNTFETs is proposed in [56]. Both of these models are used for single-walled semiconducting CNTs. Compact models are circuit models which are sufficiently simple to be incorporated in circuit simulators and at the same time are accurate enough to give circuit designers useful simulation outcomes.

Other models aiming to evaluate semiconducting CNFET potential performance at device level for digital logic applications have also been developed [10, 11]. These models exhibit promising dc performance over silicon CMOS. The issue with all the CNFET models discussed so far is that they use one or more lumped static gate capacitances. In this way the model assumes that the temperature difference inside the "lump" is negligible thereby simplifying the complex differential heat equations needed to be solved by the model. This simplification reduces the accuracy and reliability of these models. Further, the carrier transport model used in these compact models, assumes ideal ballistic transport. These simplifications render the evaluation of the transient response and device dynamic performance questionable. Models of [10,11] are difficult to implement in circuit simulators such as HSPICE as a result of the intensive calculation effort required to solve the integral function used in these models. The model implemented in [8] employs a polynomial fitting approach, thereby improving the run time over [64, 65] but as far as a comprehensive evaluation of the CNFET performance goes, especially for considering variability with different device parameters, the same approach renders the model inconvenient. The typical CNFET gate structure consists of gate oxide on top of silicon dioxide insulating bulk. However the models in [63-65] all use a coaxial or planar gate structure.

In [66] a non-iterative physics based CNT transistor compact model is presented. This model is scalable to key process and design parameters including diameter and chirality. However this model is directed mainly towards CNTs as interconnects and Schottky-barrier transitors.

FETToy is another compact model developed for calculating the I-V characteristics of CNFETs [67]. This is a set of MATLAB scripts which assumes a cylindrical gate geometry for the CNFETs. Further, only the lowest energy sub-band is considered which hinders the accuracy of the model by ignoring the effects of other sub-bands (specifically considering the second sub-band could increase accuracy significantly). FETToy assumes ballistic transport which renders the model too optimistic meaning the results can be too optimistic.

A numerically efficient CNFET model for HSPICE has been developed by the University of Southampton [68]. This model is accurate and efficient in comparison with existing models such as FETToy, however its accuracy is hindered by failing to consider sub-band effects which have an effect on current. This model still needs to be further matured to represent a realistic CNFET with all the non-idealities present including the channel length dependence of current drive, contacts resistance, geometry dependence of the gate to channel capacitance and the interconnect wiring capacitance.

None of the models discussed here account for having multiple CNTs under one gate and the effect that this would have on the effective gate capacitance due to charge screening effect which is how charge carriers in adjacent CNTs compete for the electric field of the metal gate. These models do not incorporate the non-idealities that are common place in CNFET-based devices.

The Stanford CNFET model which is used in this work is presented in [54, 69]. It is a MOSFET-like CNFET compact model. The Stanford CNFET model is a universal circuit compatible model implemented in HSPICE and accounts for various non-idealities such as scattering in the channel region, the screening effect by the parallel CNTs for CNFETs with multiple CNTs, hence more than one CNT under the gate of each device can be modelled.

The model describes unipolar MOSFETs with semiconducting SWCNTs as channels and is based on a quasi-ballistic transport model. It includes an accurate description of the capacitor network in a CNFET.

Other non-idealities including the parasitic capacitance between the gate and the source/drain formed by multiple 1D nanotubes, the gate-to-gate and gate-to-contact-plug capacitances, the access resistance of the source/drain extension regions, the Schottky-barrier resistance at the metal-CNT contact interfaces and the band-to-band leakage current are all accounted for by the model.

By incorporating a full transcapacitance network, the Stanford model produces better predictions of the dynamic performance and transient response. The model's accuracy and ability to be implemented in HSPICE have contributed to its selection for use in this work.

This model has been modified in this work to allow for a study of CNT diameter variation and its effects on circuit performance. The HSPICE code for this is given Appendix B. The model only accepts semiconducting CNTs, a reasonable assumption given recent works in [18-20].

## 2.4 CNFET-based Logic Structures

Two scenarios have been suggested under which logic circuits can be constructed using CNTFETs [70]:

1) Transposing existing CMOS-based logic functions directly to CNFET technology. Non-volatile memories [71] and logic gates [72] have been constructed this way.
2) Properties explicit to CNFETs are exploited allowing the implementation of completely new logic functions, inaccessible to MOSFET-based circuits. As an example, the band gap and hence the threshold voltage is inversely proportional to the CNT diameter. This allows for circuit branches with different switching levels to be constructed.

So far, simple circuits such as inverters [57, 73] and ring oscillators [73, 74] have been successfully fabricated. Oscillators are composed of an odd number of pairs of inverters made by appropriate doping of the CNTs.

Several works have been published on the performance comparison of various CNFET-based structures against that of conventional MOSFET-based designs. In [75], designs for different logic gates (NOT, NAND and NOR) are simulated under the same minimum gate length and different operational conditions. This work reports that the power-delay product and the leakage power for the CNFET based gates are lower than the MOSFET based logic gates by 100 to 150 times, respectively.

In [76, 77] designs for ternary logic inverters using CNFETs have been put forward. These works exploit the dependency of the threshold voltage on CNT diameter in a CNFET to design ternary logic inverters. Multiple-valued logic circuits are of interest due to their capability to increase information content per unit area.

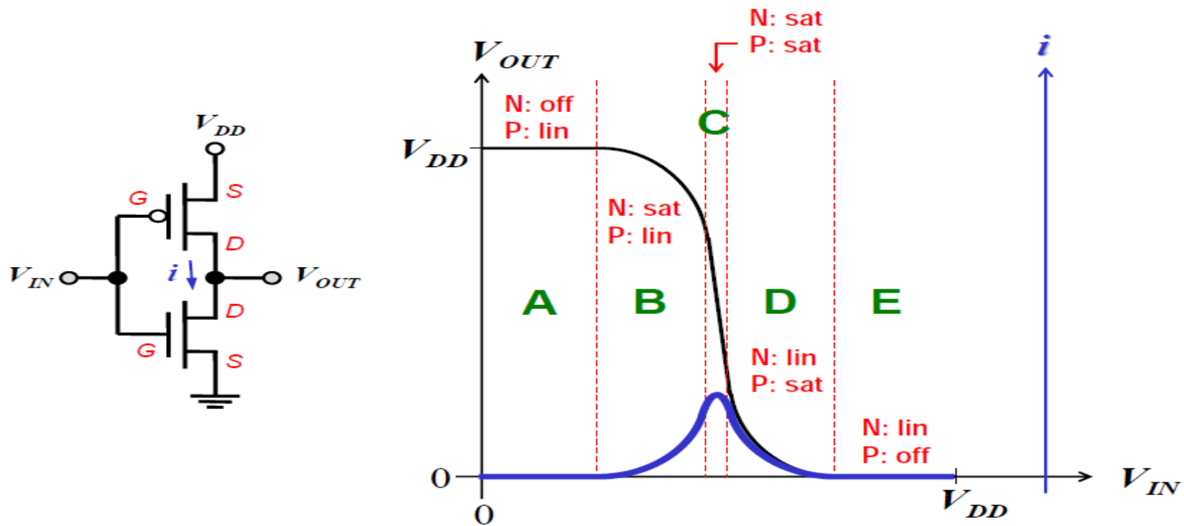


**Figure 2.6: Inverter Transfer Characteristics**

Fig. 2.6 depicts the transfer characteristics of an inverter and current flow during the switching process. The figure shows the different operational regions of the inverter for when the transistors are linear, saturated or cut-off. In region A, the nFET is off so the pFET pulls the output to $V_{DD}$. In region B, the nFET is starting to turn on as $V_{IN}$ exceeds the threshold voltage, $V_{th}$. As electron and hole mobility is assumed equal, $V_{th}$ for both nFET and pFET is also assumed to be equal here. Both transistors are saturated in region C. for the nFET $V_{th}$ is smaller than $V_{IN}$ and for the pFET $V_{IN}$ is smaller than $V_{th} + V_{DD}$ If transistors were ideal, region C would only last as long as $V_{IN} = V_{DD}/2$ and the slope of the transfer curve would be $-\infty$ corresponding to an infinite gain. As transistors in reality are not ideal, there exists a finite output resistance and hence a finite slope and a wider C region. In region D, the pFET is partially ON (saturated). In region D, the pFET is OFF, hence the linear nFET can pull the output down to ground. As $V_{IN}$ passes through voltages 0 and $V_{DD}$ both transistors are momentarily ON which results in a current being drawn from the power supply.

The use of SWCNFETs in SRAM design has been investigated in [78-80]. As the threshold voltage of the CNFET can be easily controlled by changing the chiral vector of the CNTs, a dual-diameter CNFET SRAM cell configuration with different threshold voltages is designed in [78], which is made possible by using different diameters for the P-type and N-type CNTs in the cell. The work of [79] explores the performance of a CNFET-based 6T SRAM cell and compares it with that of the conventional CMOS cell at a deep submicron 32nm technology node. The work reports that

due to inherent characteristics of CNFET, such as good gate controllability, drive current and immunity to short channel effect, the CNFET cell outperforms in leakage power, write margin, speed and read Static Noise Margin (SNM) as compared with the CMOS cell. It is also reported that the CNFET- based SRAM cell has more stable SNM against temperature variations.

## 2.5 Charge Transport in CNFETs

Charge carriers in CNTs are confined within the atomic plane of graphene. The quasi-1D structure of CNTs means that carrier motion in CNTs is strictly restricted. The only direction in which carriers can move is along the tube axis. This results in the prohibition of all wide angle scatterings. Only forward scattering and backscattering due to electron phonon interactions are possible for carriers in CNTs.

Various works have reported that CNTs exhibit ultra-long elastic scattering mean-free path (MFP) of ~1μm [12, 13]. This long MFP suggests near-ballistic transport in CNTs. This near-ballistic transport can be achieved under low voltage bias in CNTs [12, 13].

SB-CNFETs exhibit ambipolar behaviour. MOSFET-like CNFETs on the other hand exhibit unipolar behaviour by suppressing either electron or hole transport with heavily doped source/drain. The gate source bias modulates the non-tunnelling potential barrier at the channel region and thereby controls the conductivity of the device. Figs. 2.7 and 2.8 depict the energy band diagram for a MOSFET-like CNFET. Four different Fermi levels are shown in fig. 2.8. These are both input and output Fermi levels for the source and the drain.

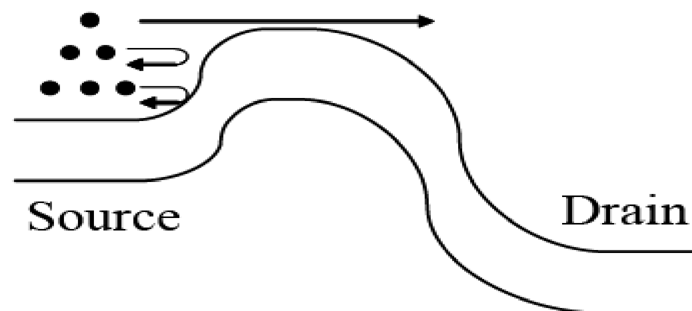


**Figure 2.7: Energy-band diagram for a MOSFET-like CNFET**

As 1-D devices, the drive current of CNFETs in the limit of near-ballistic transport highly depends on the gate to channel capacitance. In the case of having multiple CNTs under the gate of a CNFET,

the parallel CNTs have a screening/imaging effect on the actual potential profile in the gate region, thereby affecting the capacitance.

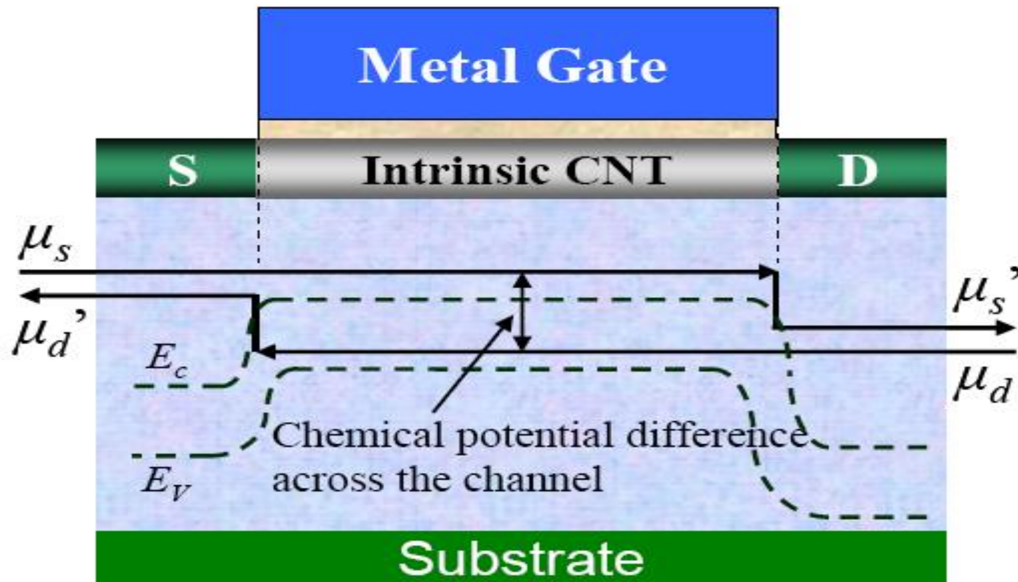


**Figure 2.8: Fermi level profiles for ballistic transport [54]**

In fig. 2.8, the chemical potential represents the Fermi level in the device. The potential can be either electrostatic potential or chemical potential (Fermi level). In the case of 1D devices, the Fermi level potential does not necessarily follow the electrostatic potential around the contacts especially for devices that are connected serially without an intermediate electron reservoir provided by a metal contact, hence, the chemical potential needs to be considered for describing the behaviour of these devices. $\mu_s$ and $\mu_d$ are the source Fermi level and the drain Fermi level respectively, while $E_c$ and $E_v$ are the conduction and valence bands.

For the high doping level of CNFETs considered in this work (1%), the first two sub-bands of the doped source/drain region are assumed to be degenerated while only the first sub-bands of the intrinsic channel region is degenerated at on-state. Sub-bands are degenerate if the Fermi level is above the first conduction band of the CNT and the sub-bands are populated in by charge carriers. The high doping level here also has the effect of suppressing the SB resistance and making the metal/CNT contact essentially ohmic through tunnelling.

## 2.6 CNFET-based Design Challenges

Controlled doping in nanoscale devices is difficult, and fluctuations in the number and position of the dopants can have a profound effect on device performance. CNFETs, along with other post-silicon device candidates suffer from extreme amounts of statistical variation in device behaviour, leading to a lack of robustness. Innovations in design, test and verification methodologies must accompany advances in manufacturing technology to address the reliability issue [81].

### 2.6.1 Sources of Variation

Various sources of variation exist when dealing with CNT-based circuits:

- Variations in CNT diameter,
- Chirality variation (leading to metallic or semiconducting CNTs),
- Doping variations,
- Variation in CNT alignment under the gate,
- Mispositioned CNTs

Diameter and doping variations in CNTs cause drain current variations whilst metallic and mispositioned CNTs affect the functionality of the gates. This work is concerned with CNT diameter variations and source/drain doping fluctuations which cause drain current variations.

A CNFET NAND cell layout overlaid on an SEM image of CNTs is shown in Figure 2.8a. The misaligned CNT in Fig. 2.8a causes Vdd to output short in this NAND cell because the portion of this CNT between Vdd and output is entirely p-doped. A misaligned CNT may also cause an incorrect logic function implementation as illustrated in Fig. 2.9b.

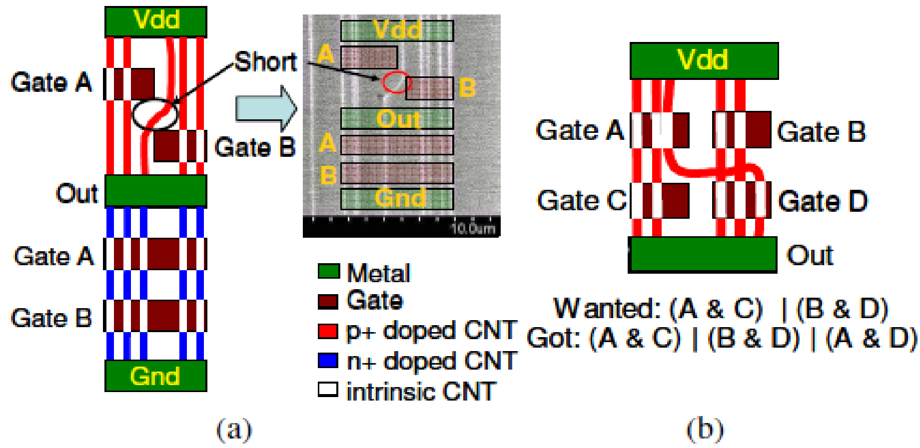


**Figure 2.9: (a) Short inside NAND gate caused by misaligned CNT. (b) Incorrect logic function due to misaligned CNT [81]**

CNTs can exhibit either semiconducting or metallic behaviour depending on their diameter and chiral angle (chirality) [17]. The diameter of nanotubes can be controlled to some extent but there is no control over the chiral angle of CNTs. The band gap energy of CNTs is inversely proportional to their diameter. As the energy band gap affects current through a CNT, the diameter and chiral angle are determining factors with regards to its current-voltage characteristics. Chirality is difficult to control during manufacturing, this results in conducting (metallic) nanotubes and defective CNTFETs similar to stuck-on (SON or source-drain short) faults, as encountered in classical MOS devices [82].

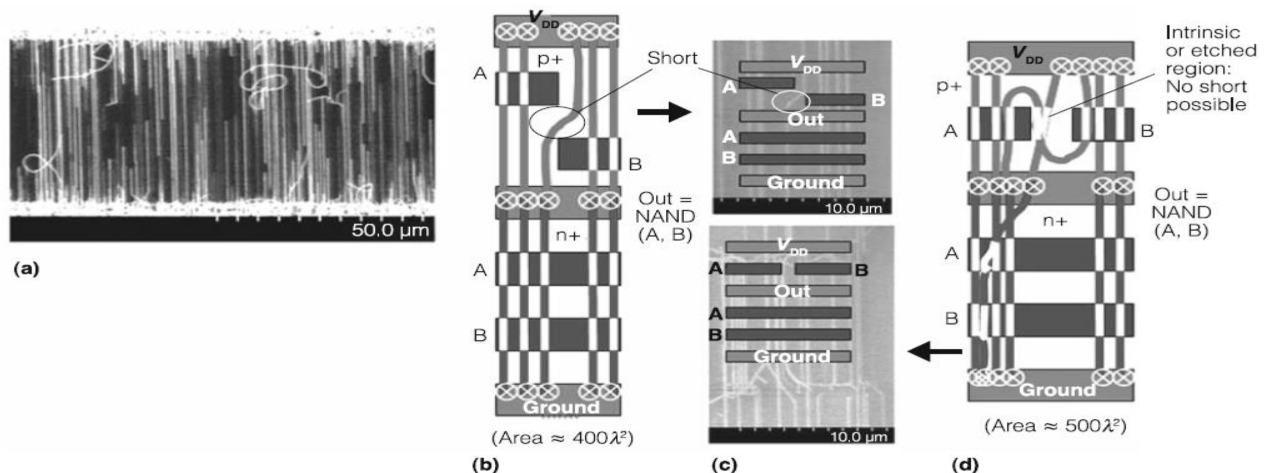


**Figure 2.10: CNT issues: largely aligned CNTs with misaligned CNTs (a), layout of misaligned-CNT-vulnerable NAND gate (b), SEM image of CNTFET overlaid with gates (c), misaligned-CNT-immune CNTFET-based NAND gate (d) [80]**

Misaligned CNTs and metallic CNTs in CNFETs are two of the main challenges in the way of progress in nano-scale technologies. As figures 2.10(b) and 2.10(c) show, misaligned CNTs cause shorts and incorrect logic functions [49]. Design techniques to build CNFET-based circuits while ensuring functional immunity to misaligned CNTs have been put forward in [53, 81, 83]. Also, semiconducting CNTs are required for CNTFETs; metallic CNTs create source-drain shorts resulting in excessive leakage and severely degraded noise margins [80]. No known CNT growth technique guarantees the total absence of metallic CNTs. Therefore, metallic CNT removal techniques are necessary [52]. Unfortunately, such removal techniques alone are imperfect and insufficient; hence, co-optimization of processing techniques for metallic CNT removal together with CNFET-based circuit design is necessary. The impact of the presence of metallic CNTs in logic circuits has been studied [84-86]. Design and processing guidelines that enable design of CNFET-based digital circuits in presence of metallic CNTs are introduced in [87].

The challenges mentioned in this section along with the lack of control of the current technology on CNT physical characteristics, highlight the importance of low cost variation tolerant design techniques which, when applied to designs impose minimal changes on design methodologies Although various CNFET models and logic structures do exist, there is no systematic study on the performance of CNT-based logic structures in the presence of the specific variation sources mentioned in this section.

In standard cell design techniques, cells are pre-designed. For the purpose of timing analysis of circuits made from these pre-designed cells, the designer needs to know how much delay each cell would introduce into the circuit. Since delay is a variable of technology, a predictive model for the prediction of delay is required. The same is true for the case of power consumption as energy usage of electronic components is an increasingly important aspect of design as sizes get smaller. This work represents a proposal for a guideline for effective CNT-based electronic design.

Lithography could also be an issue. Line-edge roughness (LER) is a random fluctuation in the width of a resist feature. The amplitude of LER can be a significant fraction of the overall resist feature width at small feature dimensions. LER is a key factor hindering the advancement of lithography to nanoscale dimensions; however this is mainly a challenge for CMOS.

# Chapter 3 CNT Based Logic Gates in the Presence of CNT Diameter Variation[1]

The electronic properties of carbon nanotubes (CNTs) are directly related to CNT physical characteristics. The main structural properties of a CNT affecting its electrical behaviour are diameter and chirality. As the energy band gap of a CNT is inversely proportional to its diameter, changes in CNT diameter translate into changes in electrical current through the CNT. As manufacture of CNTs with exact unified diameters is not achievable with current technology, CNFET-based electronics design and circuitry is prone to electric current variation. The variation in current through different CNFETs causes an avalanche of other variations such as variation in propagation delay and power consumption.

The ability to cope with these variations adds further weight to the proposition for CNFET as replacement for current silicon CMOS technology. In this chapter the performance of various logic gates in the presence of CNT diameter variations is studied. For the purpose of simulating the CNFET-based logic gates, the Stanford CNFET model is used [54, 68]. Logic gates (NOT, NAND and NOR) are studied and parameters (propagation delay, rise time, fall time and power consumption) are examined in the presence of CNT diameter variations. The CNT-based logic gates are designed and implemented in HSPICE. Parametric and Monte Carlo simulations are then carried out to obtain timing and power consumption characteristics.

Predictive models for the prediction of mean worst case propagation delay and also Standard Deviation (STD) in propagation delay based on given CNT mean diameter and STD have been developed in this chapter. Also two models for the prediction of mean power consumption and STD in power consumption of the logic gates given CNT diameter mean and STD have been developed.

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[1] Most of the contents of this chapter are taken from the paper "Effect of Variability in SWCNT-Based Logic Gates", by Hamed Shahidipour et. al. Refer to appendix A.

## 3.1 Simulation Methodology

### *3.1.1 CNFET Structure Used*

For this work a MOSFET-like CNFET structure is used as this type of device behaves in a similar fashion to CMOS FETs, exhibits unipolar behaviour and is easier to fabricate [56, 57]. The CNFET model developed by Stanford University [54] is utilised. The model implements a circuit-compatible compact model for CMOS-like single-walled (SW)-CNFETs and is implemented in HSPICE. The model is superior to previous compact models as it accounts for scattering in the channel region, the resistive source/drain, the Schottky barrier resistance and the parasitic gate capacitances. Also by addition of a full trans-capacitance network it produces better predictions of the dynamic performance and transient response. Previous models used one or more lumped static gate capacitances and an ideal ballistic transport model in which it is assumed that no scattering occurs in the channel region and all carriers emitted from the source reach the drain [56, 63-65]. The model has been calibrated against experimental CNFET data to within 90% accuracy [88]. The CNFET structure used in this work is shown in figure 3.1. The section of the SWCNT under the gate is intrinsic. For doped source/drain extension regions doping level is taken as 1% of the total number of carbon atoms which is above the first conduction band of the SWCNT. Carrier mobility in CNTs is $10^4$ $cm^2/V{\cdot}s$. The model assumes equal electron and hole mobility in CNTs. The mean free path (MFP) in the intrinsic section of the CNTs under the gate is 200nm. MFP in the doped CNT regions is 15nm throughout the work.

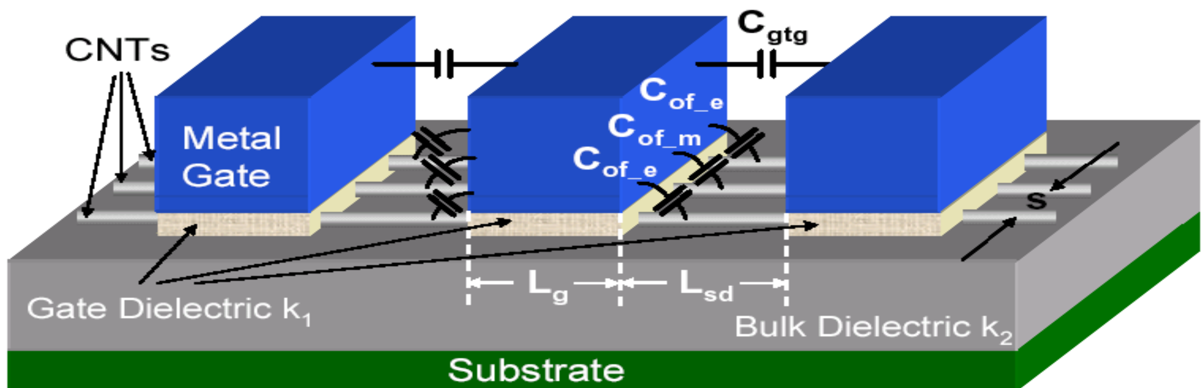


**Figure 3.1: CNFET with multiple CNTs [54]**

As mentioned earlier on, work in this chapter concentrates on the CNFET circuit performance benchmarked with the standard digital library cells such as the NOT, NAND and NOR gates. CNFET circuit performance analysis is extended to more complicated circuit structures such as multiplexers and memory modules.

Three SWCNTs per CNFET have been used in the simulations. Having more than one SWCNT per transistor has the potential advantage of improving current drive, however extra CNTs occupy extra space and impose an area cost on the transistor. Having 3 CNTs at a typical diameter of 1.5nm, with an in inter-CNT spacing of 20nm, requires a gate width of 48nm. Adding any extra CNTs would add an extra area cost in terms of the spacing required between the CNTs and the diameter of the CNT itself.

The effect of chirality variation at low-voltage operation (as is the case in most digital applications) is negligible on device electrostatics [90]; hence, in this work CNT diameter variations are considered for analysing the performance of CNFET-based logic gates and other circuit structures under process parameter variations.

As long as CNT diameter is less than 3 nanometres (nm) (which is typical for CNT devices) and the transistor is taken to be a short-channel device (less than 100nm) only the first conduction/valence bands have a significant effect on the current with a power supply of less than 1V [54, 91]. A physical channel length of 32nm is assumed together with an oxide thickness of 4 nm. This channel length is short enough for the device to be assumed short channel and long enough for the model to be able to correctly simulate the device. The model cannot simulate CNFETs with channel lengths under 10nm correctly. The physical metal gate width is assumed to be 48nm. This physical width affects the parasitic capacitance but the on-current depends on the actual *effective* gate width which is determined by the number of CNTs under the gate and the spacing between them. A power supply voltage of 0.9V is used in accordance with the ITRS roadmap for 32nm technology [3]. 10,000 samples were taken and Monte Carlo iterations were run for each mean CNT diameter ($D_{\mu}$) and CNT diameter standard deviation ($D_{\delta}$) considered. All simulations are run for the 32nm technology node. The performance parameters considered are propagation delay, rise time, fall time and power consumption. The following definitions of delays are used [62]:

*Propagation delay*: maximum time from the input crossing 50% to the output crossing 50%. This has been taken as the high to low output transition for NAND gates and low to high output transition for NOT and NOR gates.

*Rise time*: time for a waveform to rise from 10% to 90% of its steady-state value

*Fall time*: time for a waveform to fall from 90% to 10% of its steady-state value

Propagation delay and hence the device speed strongly depend on the parasitic gate capacitance, including the outer fringe gate capacitance ($C_{of}$) and the gate to gate (source/drain) coupling capacitance ($C_{gtg}$) (Fig. 3.1). The parallel conducting channels have screening/imaging effect on the actual potential profile in the gate region, and therefore affect the capacitance. For devices at 32nm node, as is the case in this work, $C_{gtg}$ is around 11 aF. The gate to channel capacitance ($C_{gc}$) strongly depends on the device geometry and both $C_{gc}$ and $C_{of}$ are affected by screening of neighbouring CNTs especially if CNTs are closely spaced thereby providing large current drive per unit device width.

### *3.1.2 Statistical Simulation Strategy*

The most commonly used statistical CNT diameter models adopt a Gaussian distribution [91]. If the rate of carbon feeding is fixed at any given growth condition there is an optimal diameter of nano-particles that nucleate nanotubes [92]. Any smaller diameter nano-particle cannot nucleate as it is “overfed” with carbon feedstock and any nano-catalysts with larger diameters are inactive as they’re “under-fed”. Assuming that the process of defining the catalyst particle size can be optimized to give a narrow allocation around a specified mean diameter, for large numbers of fabricated CNTs it can expected that the spread in diameter to follow a normal (Gaussian) distribution. A Gaussian distribution is also reported by other groups [92-95]. A positive distribution is considered as the diameter of a CNT always has a positive value.

As there is an inherent uncertainty in the diameter of CNTs produced during fabrication, a Monte Carlo (MC) approach is used with a normal distribution of CNT diameters for the simulations. MC simulations were performed to analyse how mean CNT diameter ($D_{\mu}$) and diameter STD ($D_{\delta}$) variation affect the mean and STD of the various performance parameters. 10,000 different

samples (logic gates) were assumed and for each run the diameter distribution properties were varied in the range 1.01 nm to 1.71 nm for mean diameter and 0.04 to 0.2 nm for standard deviation. Only semi-conducting CNTs are considered. Five different samples for mean diameter were taken into account. For each mean diameter sample, 5 categories of standard deviation in the range 0.04nm to 0.2nm were considered (as shown in table 3.1).

To be consistent with the work of [96], different values for mean diameters in the range 1.01 nm to 1.71 nm were taken into account. Considering the inaccuracy of fabrication techniques, a standard deviation from the mean in the range of 0.04nm to 0.2nm [96] was introduced for each mean diameter value.

HSPICE scripts are used to measure the average power consumption of the various logic gates simulated. This is done by measuring the average power drawn from the voltage source $V_{DD}$ throughout the operation of the circuit when input voltage waveforms are applied. This period also covers any switching of the circuits and thereby the dynamic power used by the circuit. The procedure for measuring the average power consumption of the circuits is shown in sample HSPICE scripts in appendix B.

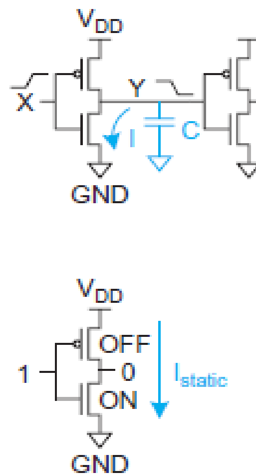


**Figure 3.2: Inverter showing current and capacitance during switching [62]**

Sources of power dissipation are dynamic power dissipation and static power dissipation. In CNFET-based circuitry, dynamic power dissipation is due to charging and discharging load capacitances as the gate switches and also the short circuit power due to short circuit current while

both pFET and nFET stacks are partially ON [62]. Static power dissipation arises from sub-threshold leakage through OFF transistors and gate leakage through gate dielectric [62].

The top part of fig. 3.2 shows an inverter with a connected load. The capacitance C in the figure represents the load capacitance due to the fan out. When the circuit is actively switching, the power consumed to charge and discharge the capacitor C is the dynamic power. When the gate is not switching, a current, $I_{static}$ is leaked through between power and ground due to the OFF transistor. This leakage gives rise to leakage power. In these simulations, the instantaneous and average power delivered by the voltage source is measured as the power consumption of the circuit. Power consumption measured in the simulations includes both the dynamic (switching + short circuit power) and the static (sub-threshold leakage + gate leakage) components.

*3.1.3 Parametric Analysis*

Parametric simulations were performed to study how diameter variation affects the performance parameters of the various logic gates considered such as delay characteristics and power consumption.

Parametric simulations were run for the various logic gates considered in this study. In the parametric analysis, the diameter of the CNTs used in the fabrication of each logic gate were swept linearly from a minimum CNT diameter of 0.6nm (the smallest physically achievable diameter) to a maximum diameter of 2nm in a transient analysis using HSPICE. Performance parameters such as propagation delay, rise time, fall time and the power consumed for each diameter case were then recorded.

The complete circuit consists of a 2-input logic gate together with 2 CNFET-based inverters in series which introduce a skew in the ideal input signal at each input thereby providing non-ideal conditions for the simulations, and 4 CNFET-based inverters in parallel as the fan-out of the NAND gate as is the case in standard practice (fig. 3.3). The fanout-of-4 (FO4) inverter delay is the delay of an inverter driving a load capacitance that has four times the inverter's input capacitance [97]. The FO4 metric is not substantially changed by process technology or operating conditions. The test circuit structure of fig. 3.3 is used in all the logic gates simulations in this work.

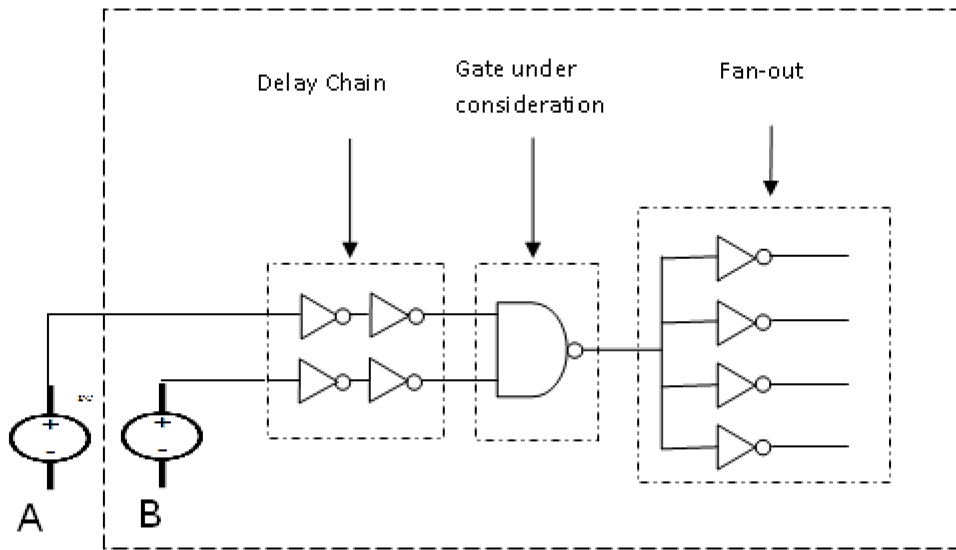


**Figure 3.3 Test Circuit**

## 3.2 Simulation RESULTS

### *3.2.1 NAND Gate*

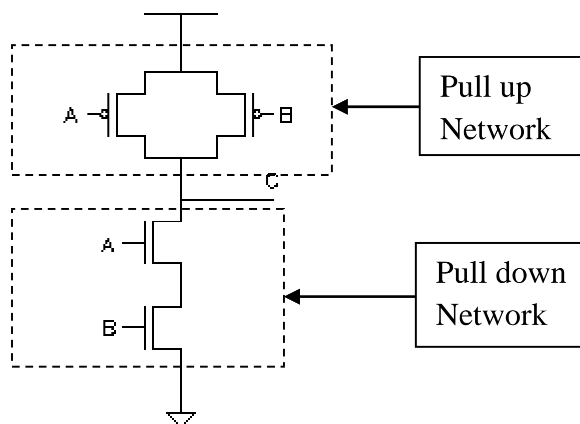


**Figure 3.4: Schematic of the simulated NAND gate**

The performance of a CNFET based NAND gate is analysed. The circuit consists of a 2-input NAND gate (composed of two P-type CNFETs and two N-type CNFETs) together with fan-in and fan-out as described in section 3.1.3. The input waveforms shown in Fig. 3.4 were given as the inputs to the NAND gate. The output waveform is v(c2) in the bottom of fig. 3.5:

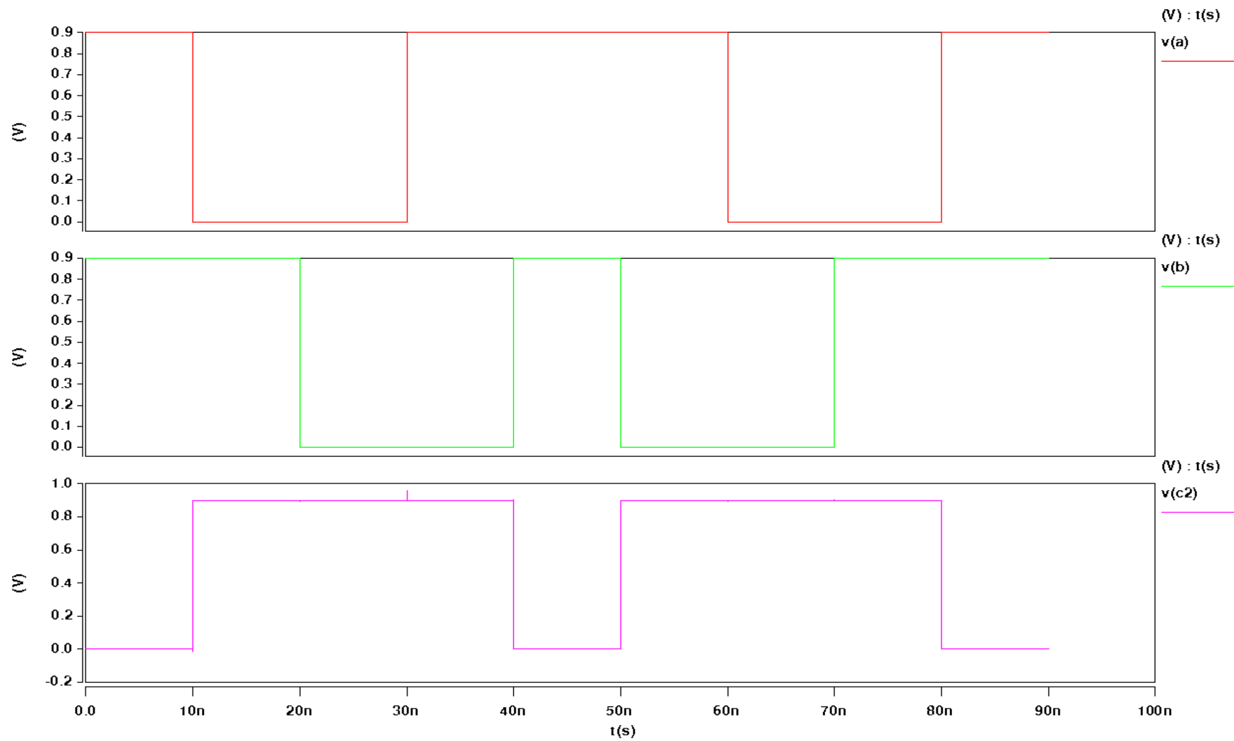


**Figure 3.5: Gate Input/Output waveforms**

Fig. 3.6 shows a falling edge of the output waveform of the NAND gate (v(c2) in fig. 3.5) in more detail in a smaller time frame.

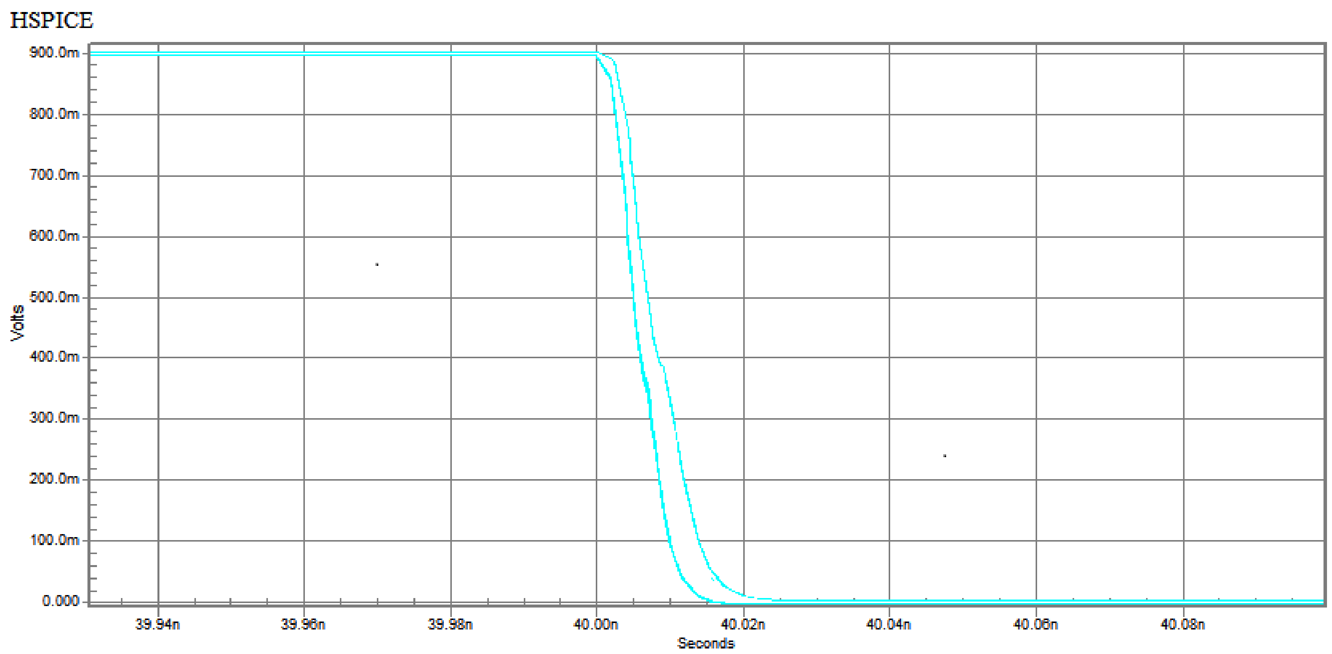


**Figure 3.6: NAND waveform showing part of the output waveform falling edge**

During each low to high output transition the load is charged through the PMOS transistors drawing a certain amount of energy from the power supply. It is discharged during the high to low output transition and the stored energy is dissipated through the NMOS transistors.

The input waveforms and the time duration are chosen so that the analysis covers the different behavioural regimes of the gates. The two signals cover the cases where both inputs to the gate *A* and *B* are high (at Vdd = 0.9V); where *A* is low (at 0 Volts) and *B* is high, also when input *A* is high and input *B* is low and finally when both inputs *A* and *B* are low; this covers the full logic input combination for the 2-input NAND gates. The input signals are almost ideal so that rise and fall times are ~0, however the fan-in inverters in the test circuit are there to introduce the necessary skew in the rise/fall times of the input signals.

The two P-type CNFETs (PCNFETs) are connected to the supply voltage Vdd. As P-type transistors close when their gate signal is low, the two parallel PCNFETs imply that if either or both inputs *A* and *B* are low, then the gate output is high (at Vdd). NCNFETs behave in the opposite way as they close when the signal on their gate is high, hence, the two series NCNFETs provide a connection to ground only when both *A* and *B* are high.

*3.2.1.1 Timing Behaviour*

When both A and B are high, the two PCNFETs are off and the two NCNFETs are both on, providing a connection to ground, hence output is zero (low). The two series NCNFETs here offer greater resistance in the path of current and fall time is expected to take longer than when current would be passing through one transistor only. When both A and B are low, the two PCNFETs are on and the two NCNFETs are off. Gate output here would be high. The path offered to current through the parallel pull-up network of the PCNFETs has half the resistance of a single transistor and rise time is expected to be faster than the fall time for the NAND gates.

The case for worst case delay happens when one input (*A* in Fig. 3.5) is high and the other input (*B* in Fig. 3.5) changes from low to high. While *B* is still low, the PCNFET connected to *A* is off and the other PCNFET connected to *B* is on. The NCNFET connected to *A* is on and the NCNFET connected to *B* is off. Under this condition the output terminal is charged through the PCNFET connected to *B* to approximately Vdd. In this case the drain regions of the on-NCNFET are also

charged to Vdd. When *B* changes from low to high, the on PCNFET turns off and the off NCNFET turns on. Now the two series NCNFETs are on and the output terminal of the NAND gate discharges to ground, but the charge previously stored at the drain region of the NCNFET connected to *A* must also be discharged at the same time. This discharge takes place through the NCNFET connected to the *B* input and hence the discharge of the NAND gate's output terminal must wait until this is done.

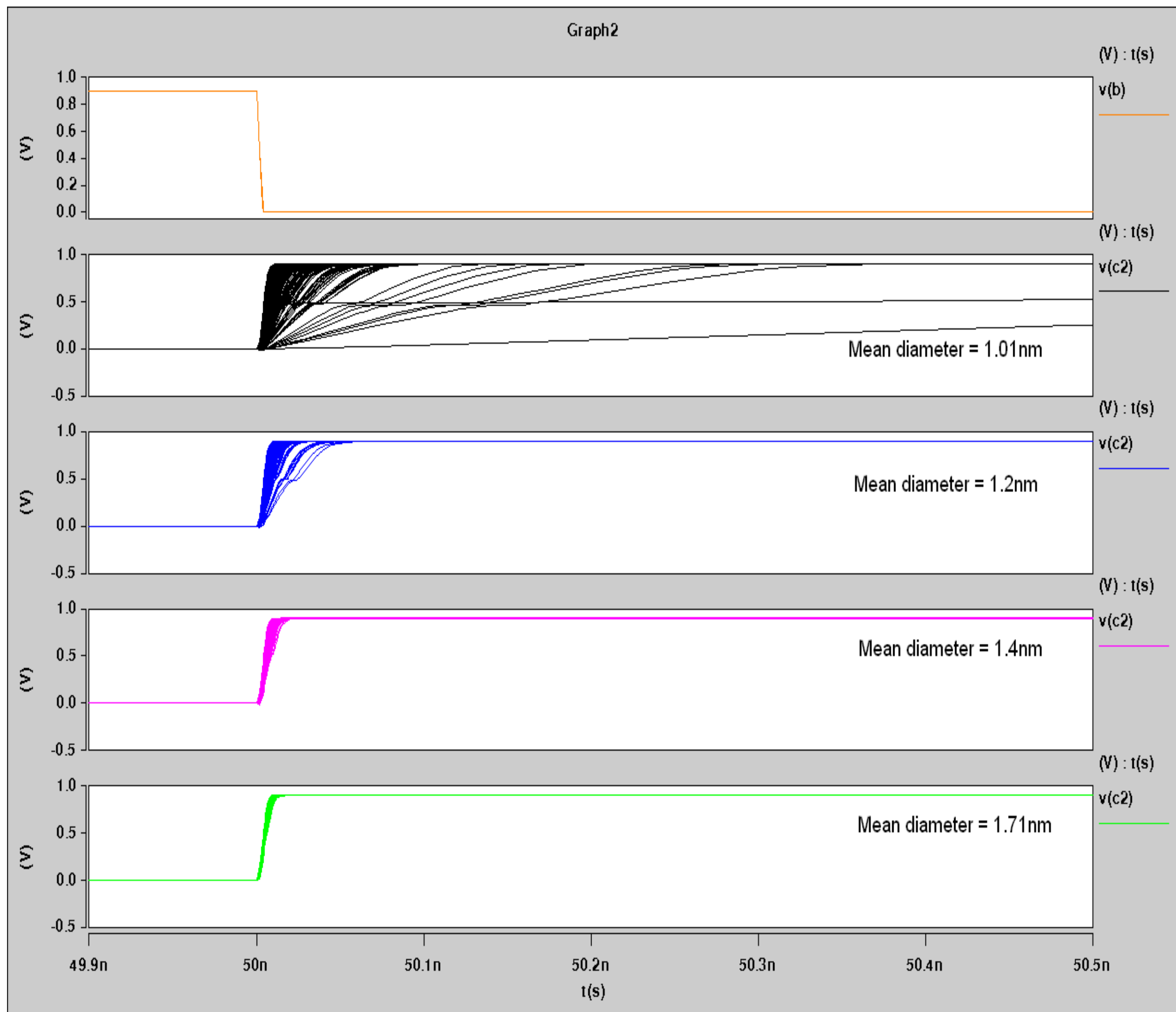


**Figure 3.7: Variation in NAND Gates Delay with different CNT diameters**

Fig. 3.7 shows output voltages obtained from 10000 Monte Carlo simulation iterations of NAND gates with various CNT mean diameters for a given input voltage. It can be seen from the plots that for NAND gates employing larger diameter CNTs, variation in output voltage becomes smaller.

As the band gap of a carbon nanotube is inversely proportional to its diameter [97-104], CNTs with larger diameters have smaller band gaps. A smaller band gap means that a transistor made of CNTs with larger diameters can exhibit higher on-currents. CNTs with smaller diameters have higher source/drain resistance which can be explained by the fact that at small diameters only the first sub-band is degenerate (zero bandgap, i.e. the subbands are populated by charge carriers) [69].

From figure 3.6 it can be observed that at smaller diameters, the effects of diameter variations as a process parameter are more profound. By varying the diameter the band gap of the CNT is modified. Assume two sets of CNTs. One set has a mean diameter of 1.01nm and the other set has a mean diameter of 1.71nm. Assume also a STD of 0.2 nm. The 3 sigma point of the distribution is taken (according to the empirical rule this covers over 99.7% of the values drawn from the normal distribution) into account, so that this STD roughly translates into an 11.7% deviation from mean diameter in the case of 1.71nm mean, but the same STD implies almost a 20% deviation for the 1.01nm CNTs. Hence, a diameter change of 0.2nm causes greater band gap variation for CNTs with small mean diameters compared with those with larger mean diameters.

**Table 3.1: NAND Gates delay behaviour**

| Mean Diameter(nm) | Diameter STD (nm) | Mean Delay $T_d$ (ps) | Min. Delay (ps) | Max. Delay (ps) | $\Delta T_d$ (ps) |
|---|---|---|---|---|---|
| **1.01** | 0.04 | 7.44 | 5.75 | 10.31 | 4.56 |
| | 0.08 | 7.62 | 4.56 | 26.69 | 22.13 |
| | 0.12 | 8.15 | 3.43 | 49 | 45.57 |
| | 0.16 | 8.97 | 3.03 | 55.41 | 52.38 |
| | 0.2 | 9.63 | 2.81 | 54.82 | 52.01 |
| **1.2** | 0.04 | 6.09 | 4.79 | 7.33 | 2.54 |
| | 0.08 | 6.11 | 3.62 | 9.72 | 6.1 |
| | 0.12 | 6.18 | 3.21 | 19.49 | 16.28 |
| | 0.16 | 6.35 | 2.99 | 53.81 | 50.82 |
| | 0.2 | 6.71 | 3 | 60.11 | 57.11 |
| **1.4** | 0.04 | 4.85 | 3.71 | 5.93 | 2.22 |
| | 0.08 | 4.85 | 3.33 | 7.07 | 3.74 |
| | 0.12 | 4.88 | 3.12 | 9 | 5.89 |
| | 0.16 | 4.95 | 3.1 | 13.9 | 10.8 |
| | 0.2 | 5.06 | 3.1 | 38.63 | 35.53 |
| **1.5** | 0.04 | 4.19 | 3.59 | 5.21 | 1.62 |
| | 0.08 | 4.25 | 3.38 | 6.18 | 2.8 |
| | 0.12 | 4.33 | 3.19 | 7.68 | 4.49 |
| | 0.16 | 4.42 | 3.15 | 10.19 | 7.04 |
| | 0.2 | 4.53 | 3.15 | 19.3 | 16.15 |
| **1.71** | 0.04 | 3.66 | 3.44 | 4.03 | 0.59 |
| | 0.08 | 3.68 | 3.38 | 4.88 | 1.51 |
| | 0.12 | 3.73 | 3.37 | 5.94 | 2.56 |
| | 0.16 | 3.8 | 3.37 | 7.01 | 3.64 |
| | 0.2 | 3.9 | 3.22 | 9.05 | 5.83 |

**Table 3.2: NAND Gates Rise/Fall Times Variation**

| Mean Diameter(nm) | Diameter STD (nm) | Max Rise/Fall (ps) | Min. Rise/Fall(ps) | $\Delta T_d$ (ps) |
|---|---|---|---|---|
| **1.01** | 0.04 | 14.58 | 6 | 8.58 |
| | 0.08 | 39.98 | 5.36 | 34.62 |
| | 0.12 | 71.17 | 4.1 | 67.07 |
| | 0.16 | 79.54 | 4.04 | 75.5 |
| | 0.2 | 79.88 | 4.044 | 75.84 |
| **1.2** | 0.04 | 11.9 | 5.56 | 8.34 |
| | 0.08 | 14.96 | 4.72 | 10.24 |
| | 0.12 | 30.75 | 4.56 | 26.19 |
| | 0.16 | 83.51 | 4.51 | 79 |
| | 0.2 | 93.27 | 4.513 | 88.76 |
| **1.4** | 0.04 | 10.9 | 4.81 | 6.09 |
| | 0.08 | 12.22 | 4.63 | 7.59 |
| | 0.12 | 14.72 | 4.61 | 10.12 |
| | 0.16 | 22.33 | 4.59 | 17.74 |
| | 0.2 | 63.28 | 4.59 | 58.7 |
| **1.5** | 0.04 | 10.28 | 4.65 | 5.63 |
| | 0.08 | 11.54 | 4.63 | 6.91 |
| | 0.12 | 13.08 | 4.58 | 8.5 |
| | 0.16 | 16.76 | 4.57 | 12.19 |
| | 0.2 | 32.27 | 4.57 | 27.7 |
| **1.71** | 0.04 | 8.33 | 4.38 | 3.95 |
| | 0.08 | 9.89 | 4.38 | 5.51 |
| | 0.12 | 11.74 | 4.38 | 7.36 |
| | 0.16 | 12.95 | 4.38 | 8.57 |
| | 0.2 | 15.46 | 4.38 | 11.08 |

Table 3.1 shows the propagation delay of NAND gates of 10000 Monte Carlo iterations with various CNT mean and STD in diameter. Mean Delay represents the average propagation delay value for the 10,000 NAND gates within each category. As an example from table 3.1 the mean propagation delay of NAND gates with a CNT diameter of 1.01nm and a STD in diameter distribution of 0.04nm is 7.44ps. The delay values were measured in HSPICE. Sample codes are provided in Appendix B.

Min. Delay and max. delay in table 3.1 represent the minimum propagation delay and the maximum propagation delay observed respectively within the total 10,000 NAND gates considered within a particular category; hence, from table 3.1 the minimum propagation delay observed for any NAND gate within the category of 1.01nm mean and 0.04nm STD in diameter is 5.75ps and the maximum propagation delay observed for any of the NAND gates within the same category is 10.31ps giving a propagation delay variation $\Delta T_d$ of 4.56ps.

Table 3.2 shows the worst case variation in fall times ($t_f$) or rise times ($t_r$) for 10,000 Monte Carlo iterations of the NAND gates with various mean and STD values for CNT diameter. Maximum and Minimum values for rise time and fall time are found and shown in the table. Then a worst case delay variation $\Delta T_d$ is obtained by finding the difference between maximum and minimum rise/fall time. This worst case rise/fall time variation is plotted in the 3D plot of fig. 3.6.

It is observed from tables 3.1 and 3.2 that with increasing mean CNT diameter and decreasing CNT diameter STD the worst case variation in timing behaviour $\Delta T_d$, which is defined as the difference between maximum delay and minimum delay observed in the logic gates, decreases consistently. According to the tables 3.1 and 3.2, the only exception to this is when mean CNT diameter of 1.01nm and 1.2nm are compared for the STD case of 0.2nm. For this case $\Delta T_d$ in propagation delay of NANDs employing 1.01nm diameter CNTs with a STD of 0.2nm is about 52ps while that of NAND gates employing 1.2nm mean diameter CNTs is around 57ps. This discrepancy could simply be the result of the large STD value used in the Monte Carlo simulations which can result in some CNT diameters which deviate significantly from the mean. This further underlines the need for technologies which can provide smaller STDs from the mean to guarantee more consistent timing behaviour.

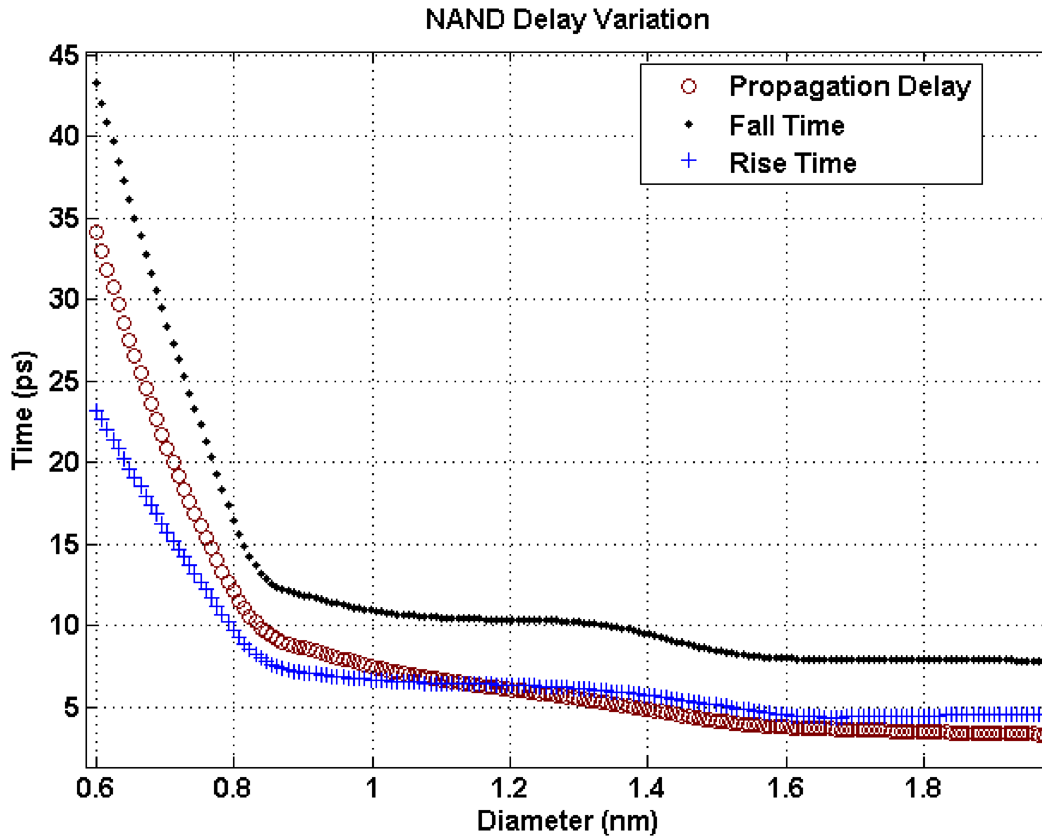


**Figure 3.8: NAND Gates Time Delay with respect to CNT Diameter Variation**

Figure 3.8 is obtained based on the results of the parametric simulation of the NAND gates. In this parametric simulation CNT diameter is swept from a minimum of 0.6nm to a maximum 2nm while recording the performance parameters. The graph shows the behaviour of the various delay metrics of the NAND gates with respect to changing CNT diameter. The graph shows that rise time takes shorter than fall time but the trend of timing delay is similar for propagation delay, rise time and fall time in that delay behaviour is comparatively static above a CNT diameter of 1nm but as diameter is reduced below ~0.85nm a dramatic change in timing behaviour is observed and timing delay of the NAND gates becomes increasingly larger.

As the doping level is the same for all CNTs in the simulations (1%) regardless of their diameter, the Fermi level for all the doped CNTs here is almost constant. As CNT band gap is inversely proportional to CNT diameter, reducing the diameter increases the band gap. Reducing CNT diameter further, there comes a point when the constant Fermi level no longer lies above the sub-

bands. Fewer degenerate sub-bands mean higher source/drain resistance and reduced current drive. The reduced current drive in turn causes a larger delay which is why a sudden increase in delay time is observed in fig. 3.8.

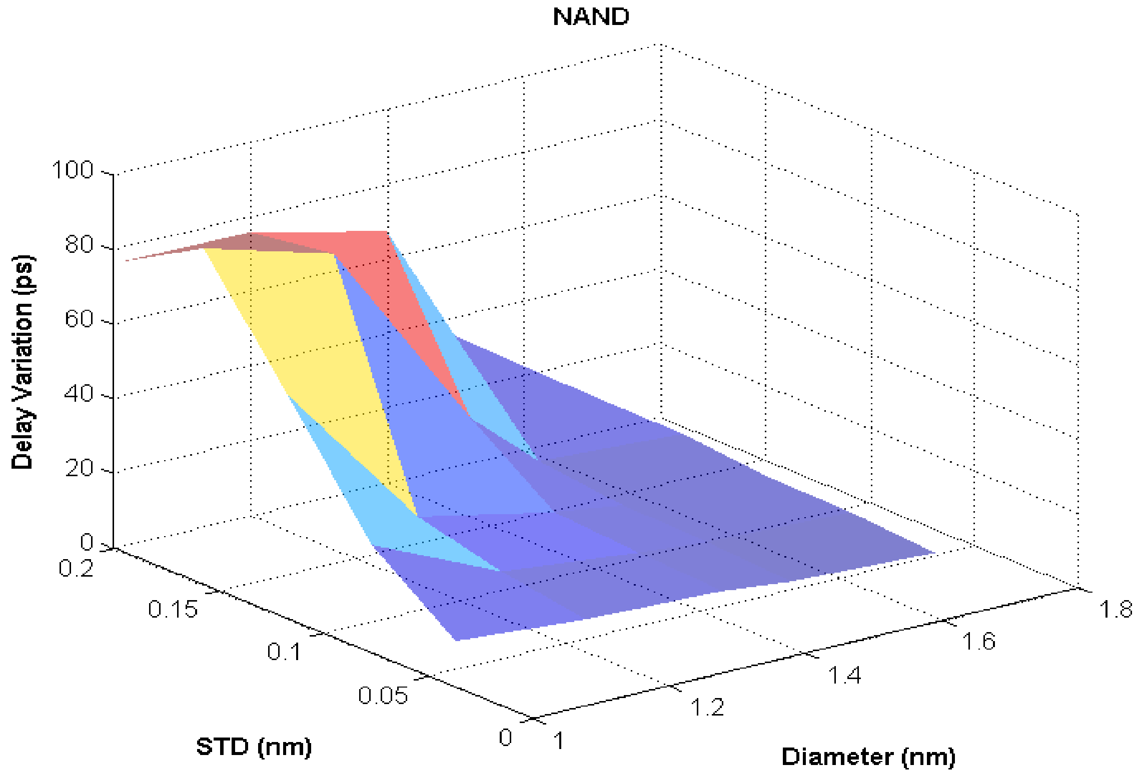


**Figure 3.9: NAND Gates delay variation with respect to change in CNT mean diameter and STD**

In fig 3.9, mean CNT diameter and STD in CNT diameter are plotted on the X and Y axes respectively. The gates delay variation is plotted on the Z axis. Delay variation here is defined as the difference between maximum rise/fall time and minimum rise/fall time of the NAND gates. The plot shows that the logic gates delay variation rises significantly when smaller CNT mean diameters are employed in the design of the gates. The variation in delay peaks when the small mean CNT diameter is combined with larger STDs of CNT diameter. It can be observed from fig. 3.8 that delay variation ranges from around 4ps at larger mean diameters with smaller STDs to over 80ps at small mean diameters with large STDs.

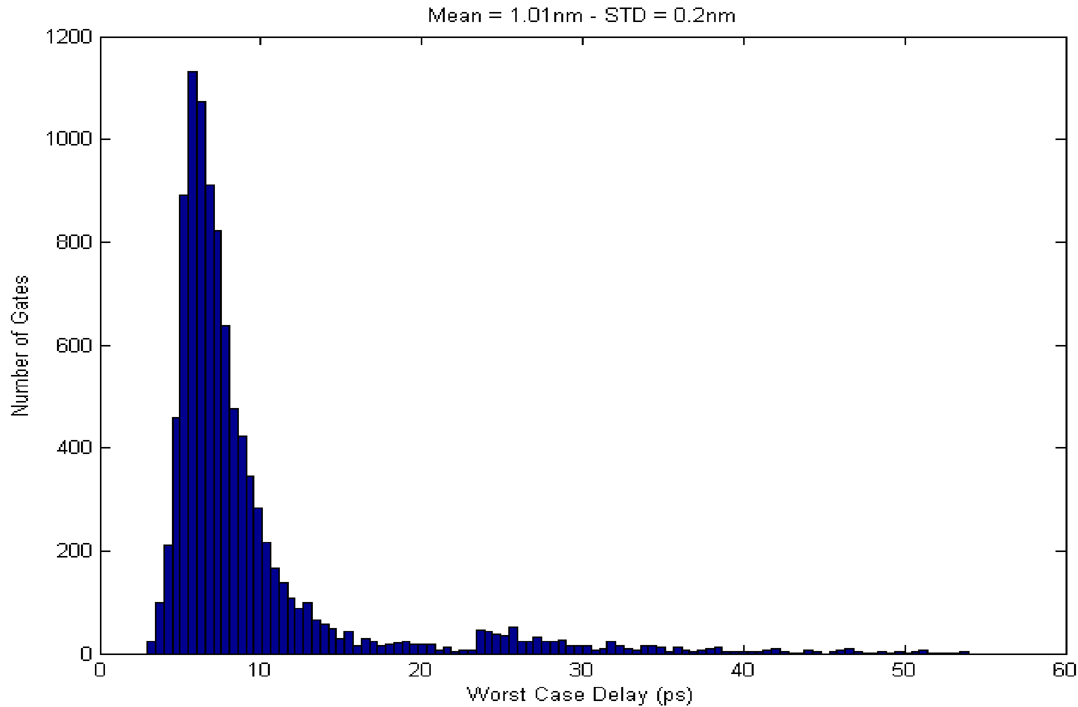


**Figure 3.10: Worst Case Delay for 1.01nm Mean and 0.2 STD in Diameter**

At a STD of 0.2nm, gates employing CNTs 1.01nm in mean diameter, show a mean propagation delay of 9.63 ps and $\Delta T_d$ of around 52ps. This variation is clearly very large, over 5 times bigger than the actual mean delay of the gates as the minimum and maximum delay values are 2.81ps and 54.82ps respectively.

If it is assumed however that a manufacturing process is accurate enough to give CNT diameters within a standard deviation of 0.04nm, based on these results it can be expected to achieve a mean delay of about 7.44ps and a $\Delta T_d$ of 4.56 picoseconds. This shows a huge improvement in delay variation compared to the 0.2nm STD case.

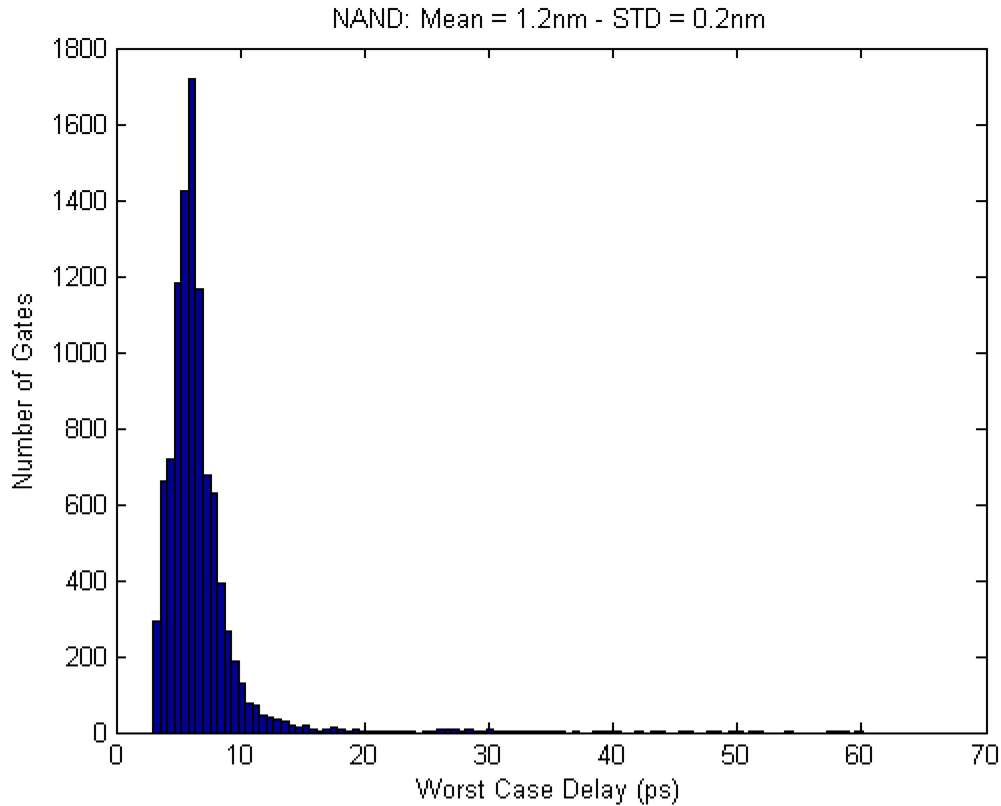


**Figure 3.11: Worst Case Delay for 1.2nm Mean and 0.2 STD in Diameter**

As can be seen from Fig. 3.11, gates with a CNT mean diameter of 1.2nm at 0.2nm standard deviation have a mean propagation delay of about 6.7 picoseconds and $\Delta T_d$ of 57.11 ps. This is a variation over 8 times larger than the mean delay value for the NAND gates, a figure which is unacceptable.

The same gates with a STD in CNT diameter of 0.04nm give a figure of 6.09ps as mean delay and a $\Delta T_d$ of around 2.5ps. Again a huge improvement can be seen with a smaller STD value.

As CNTs with larger diameters deliver more current, each CNFET made from them and hence, the whole logic gate has a higher current drive compared with gates made of smaller diameter CNTs. This total increase in current drive translates into improved timing characteristics. The distribution graphs also show that variation in propagation delay decreases for gates made of CNFETs with larger CNT diameters.

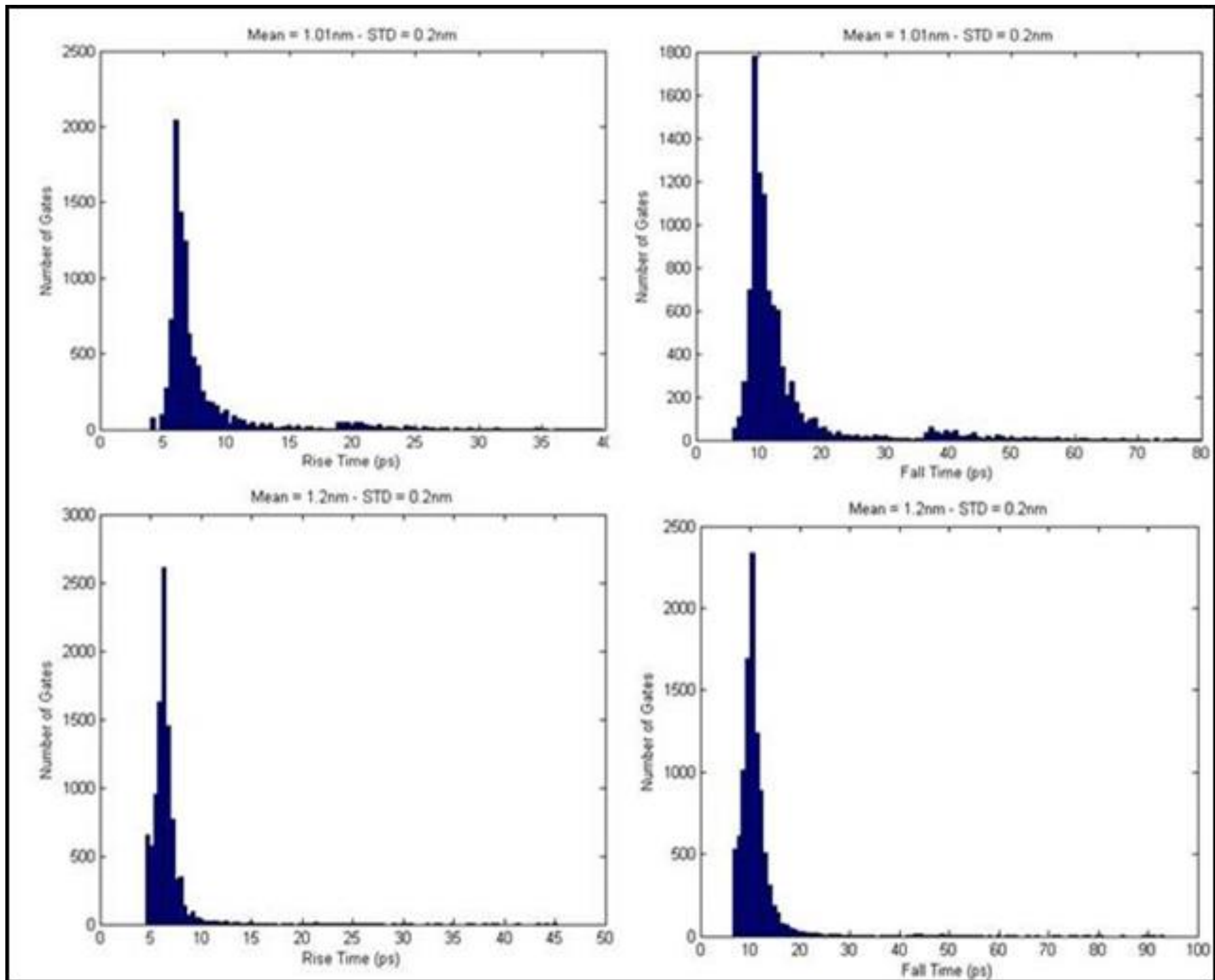


**Figure 3.12: Rise & Fall times for NAND Gates with 1.01nm & 1.2nm mean CNT diameter and 0.2nm STD in diameter**

Fig. 3.12 depicts histograms for the rise and fall times of NAND gates employing CNTs with mean diameter of 1.01nm and 1.2nm, all at a diameter STD of 0.2nm. The number of NAND gates is shown on the y axis (out of a total of 10000 NAND gates) and timing behaviour is on the x axis. The histograms for the 1.01 nm mean diameter case show a wider spread revealing higher variability compared to a larger mean diameter of 1.2nm.

*3.2.1.2 Power Consumption*

The results of the Monte Carlo simulations for power consumption of the NAND gates are shown in table 3.3.

**Table 3.3: NAND Gates Power Consumption**

| Mean Diameter(nm) | Diameter STD (nm) | Mean Power(nW) | Min. Power (nW) | Max. Power(nW) | ΔP (nW) | PDP ($*10^{-20}$ J) | PDP Variation ($*10^{-20}$ J) |
|---|---|---|---|---|---|---|---|
| **1.01** | 0.04 | 4.7 | 4.62 | 4.85 | 0.23 | 34.968 | 1.0488 |
| | 0.08 | 4.7 | 4.48 | 4.95 | 0.47 | 45.814 | 10.4 |
| | 0.12 | 4.7 | 4.38 | 5.38 | 1 | 38.305 | 45.57 |
| | 0.16 | 4.69 | 4.36 | 5.96 | 1.6 | 42.069 | 83.808 |
| | 0.2 | 4.7 | 4.36 | 6.99 | 2.63 | 45.261 | 136.786 |
| **1.2** | 0.04 | 5.17 | 5.08 | 5.39 | 0.31 | 31.485 | 0.7874 |
| | 0.08 | 5.18 | 5 | 5.82 | 0.82 | 31.6498 | 5 |
| | 0.12 | 5.19 | 4.9 | 6.33 | 1.44 | 32.074 | 23.44 |
| | 0.16 | 5.21 | 4.8 | 7.46 | 2.67 | 33.083 | 135.7 |
| | 0.2 | 5.23 | 4.78 | 7.32 | 2.54 | 35.093 | 145.06 |
| **1.4** | 0.04 | 5.73 | 5.51 | 6.07 | 0.56 | 27.7905 | 1.24 |
| | 0.08 | 5.73 | 5.36 | 6.64 | 1.28 | 27.7905 | 4.8 |
| | 0.12 | 5.74 | 5.28 | 7.55 | 2.27 | 28.011 | 13.37 |
| | 0.16 | 5.76 | 5.2 | 7.77 | 2.57 | 28.512 | 27.8 |
| | 0.2 | 5.78 | 5.13 | 7.76 | 2.63 | 29.2468 | 93.44 |
| **1.5** | 0.04 | 5.99 | 5.75 | 6.5 | 0.76 | 25.0981 | 1.23 |
| | 0.08 | 5.99 | 5.55 | 7.23 | 1.68 | 25.4575 | 4.7 |
| | 0.12 | 6 | 5.42 | 7.85 | 2.43 | 25.98 | 10.91 |
| | 0.16 | 6.02 | 5.36 | 7.79 | 2.43 | 26.6084 | 17.11 |
| | 0.2 | 6.05 | 5.27 | 7.8 | 2.52 | 27.4065 | 40.7 |
| **1.71** | 0.04 | 6.46 | 6.1 | 7.66 | 1.56 | 23.6436 | 0.92 |
| | 0.08 | 6.57 | 6 | 7.85 | 1.86 | 24.1776 | 2.8086 |
| | 0.12 | 6.62 | 5.79 | 9.11 | 3.32 | 24.6926 | 8.5 |
| | 0.16 | 6.62 | 5.66 | 7.89 | 2.21 | 25.156 | 8.044 |
| | 0.2 | 6.6 | 5.52 | 8.52 | 3 | 25.74 | 17.49 |

The results are the average power consumption by the gates over the entire waveform period (0 to 90ns) as measured in HSPICE (the relevant code is presented in Appendix B). The first observation from the table is that for a particular CNT mean diameter, the effect of diameter STD variation on average power consumption is small; that is for any mean diameter and any fabrication process with any STD accuracy, mean power consumption remains the same. For example, NAND gates employing CNTs of average diameter 1.5nm, have a mean power consumption of 6 nanoWatts (nW) for all the STDs considered within the range of 0.04nm to 0.2nm.

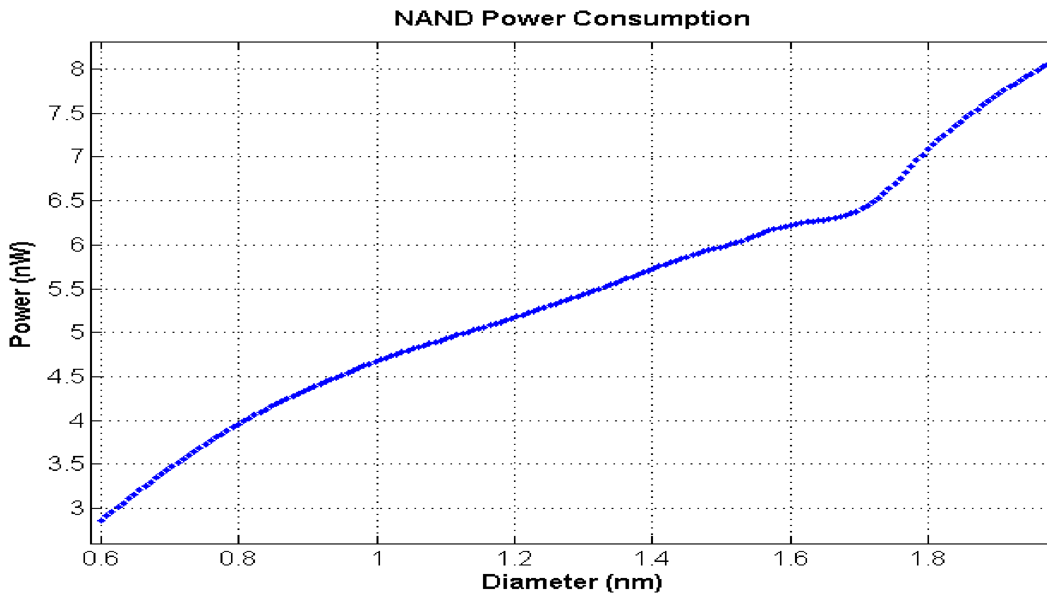


**Figure 3.13: NAND Gates Power Consumption**

Results also reveal that even though mean power consumption is unaffected by diameter STD, variation in power consumption is indeed hugely affected by CNT diameter STD. NAND gates with a mean CNT diameter of 1.01nm and with a STD of 0.04nm show a variation in power consumption of 0.23nW. This is a variation of less than 5% of average power consumption and perhaps tolerable. But for the same mean diameter and a lager STD of 0.2nm, variation in power consumption is 2.63nW. This is variation amounting to 56% of the average power consumption and clearly poses a problem.

Considering CNTs with mean diameters of 1.71nm, NAND gates show a variation in power of 1.56nW (24% of average power) at STD of 0.04nm and a variation of 3nW (45% of average power) at STD of 0.2nm. Given a fixed STD of 0.04nm, mean CNT diameters of 1.2nm, 1.4nm and 1.5nm give variations in power consumption of ≈ 6%, 10% and 13% of the average power consumption

respectively (table 3.4). Fig. 3.13 shows the results of the parametric simulation of NAND gates power consumption. The figure shows that mean power consumption increases with CNT diameter. As diameter increases band gap decreases and more current flows through the CNFET. Increased drive current translates into increased power consumption as supply voltage is fixed. This is why higher average power consumption is observed for NAND gates employing CNTs with larger diameters. Fig. 3.14 shows that for all mean diameters at a larger STD of 0.2nm, variation in power consumption remains almost the same; suggesting that a technology which provides a STD of 0.2nm, is less dependent on large or small diameter CNTs as far as power variation is concerned as variation in power consumption remains greater than 40% for any mean diameter chosen. Further, fig 3.13 also suggests a sharper rise in power consumption as diameter increases beyond ~1.7nm.

**Table 3.4: %age Variation from the mean of NAND Gates Power Consumption with mean Diameter**

| Mean Diameter (nm) | % Variation (STD = 0.04nm) | %Variation (STD = 0.2nm) |
|---|---|---|
| 1.01 | 5 | 56 |
| 1.2 | 6 | 49 |
| 1.4 | 10 | 46 |
| 1.5 | 13 | 42 |
| 1.71 | 24 | 45 |

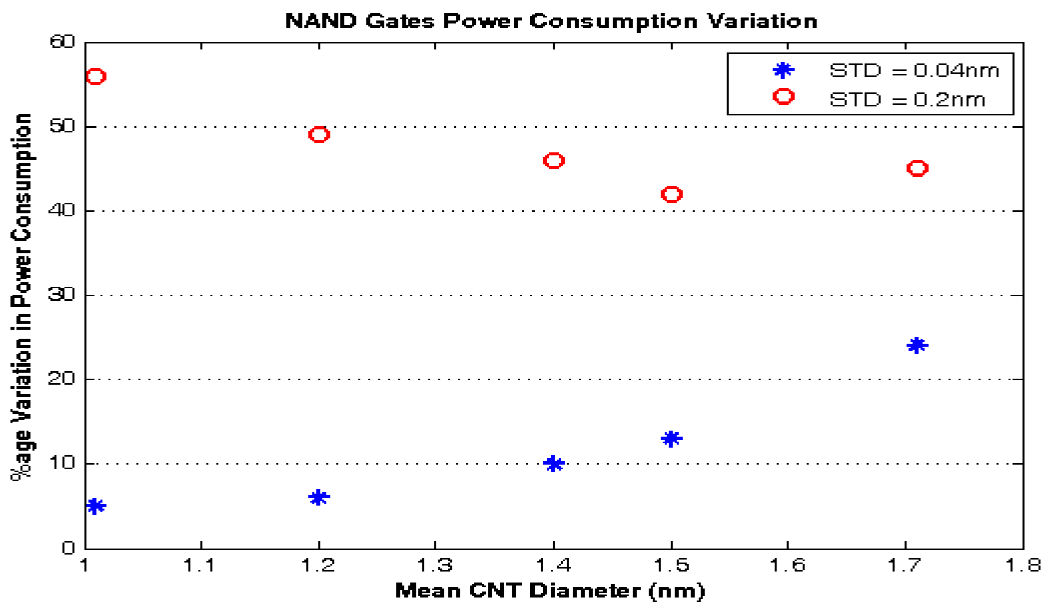


**Figure 3.14: Variation in NAND Gates Power Consumption**

*3.2.1.3 Power-Delay Product*

As low operation power is desired together with small time delays, the Power-Delay Product (PDP) is a good measure of device performance. It is the product of propagation delay of the logic gates with the power consumed per logic gate and represents the energy efficieny of the gates. PDP variation in this work is defined as the product of $\Delta P$ and $\Delta T_d$.

Table 3.3 shows figures obtained for the PDP of the NAND gates. The PDP values show insignificant changes from one CNT diameter STD to the next for a given mean diameter. In moving from one CNT mean diameter to the next however large changes in PDP are apparent. As mean CNT diameter increases, PDP values become smaller suggesting that greater energy efficiency is obtained for NAND gates utilizing CNTs with wider diameters.

Looking at variation in the PDP values (table 3.3) it is observed that the *variation* in PDP is greatly affected by diameter STD. PDP variation is obtained by finding the product of propagation delay variation and power consumption variation ($\Delta P$) defined as the difference between maximum power consumption of the gate and the minimum power consumption of the gate. This significant variation in PDP from one diameter STD to the next however is mainly a result of significant changes in propagation delay variation through different diameter STDs which weighs heavily on PDP variation.

It can be concluded that if manufacturing accuracy can allow for a CNT diameter STD of less than 0.12nm, a similar pattern of variation in PDP is seen for all the mean diameters considered. If technology does allow control of diameter to finer STDs such as 0.04nm, then as far as power consumption alone is concerned, it would be advisable to choose smaller CNT mean diameters in designs to avoid excessive variation in power consumption. However, as propagation delay plays a great role in any logic circuit design, a judgement on the ultimate CNT diameter of choice should also consider delay and PDP variations. Hence, provided that a STD of less than 0.12nm can be guaranteed, larger CNT diameters provide better delay behaviour and PDP as far as variation is concerned and also show acceptable power consumption variation compared with smaller diameter CNT NAND gates.

*3.2.2 NOR Gate*

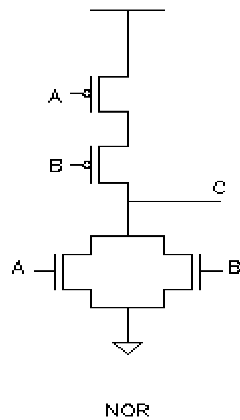


**Figure 3.15: NOR gate schematic**

This section shows analysis of the performance of a CNFET-based NOR gate. The complete circuit consists of a 2-input NOR gate (composed of 2 PCNFETs and 2 NCNFETs) together with 2 CNFET-based inverters in series which introduce a skew in the ideal input signal at each input, and 4 CNFET-based inverters in parallel as the fan-out of the NOR gate as is the case in standard practice. All the circuit and simulation conditions are as described for the NAND gate in the previous section.

*3.2.2.1 Timing Behaviour*

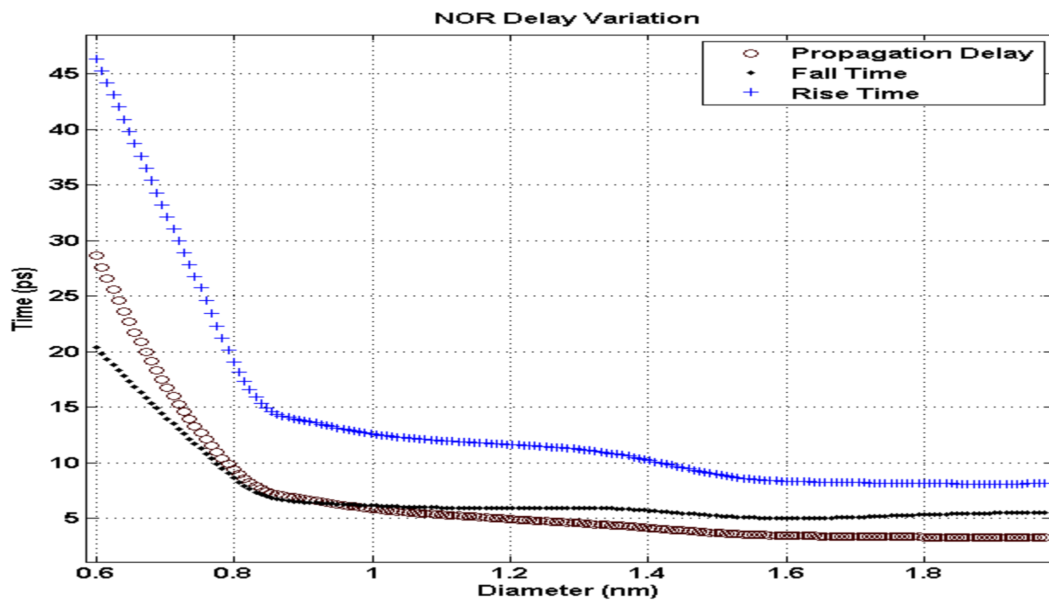


**Figure 3.16. NOR Gate Delay Variation with respect to CNT Diameter Variation**

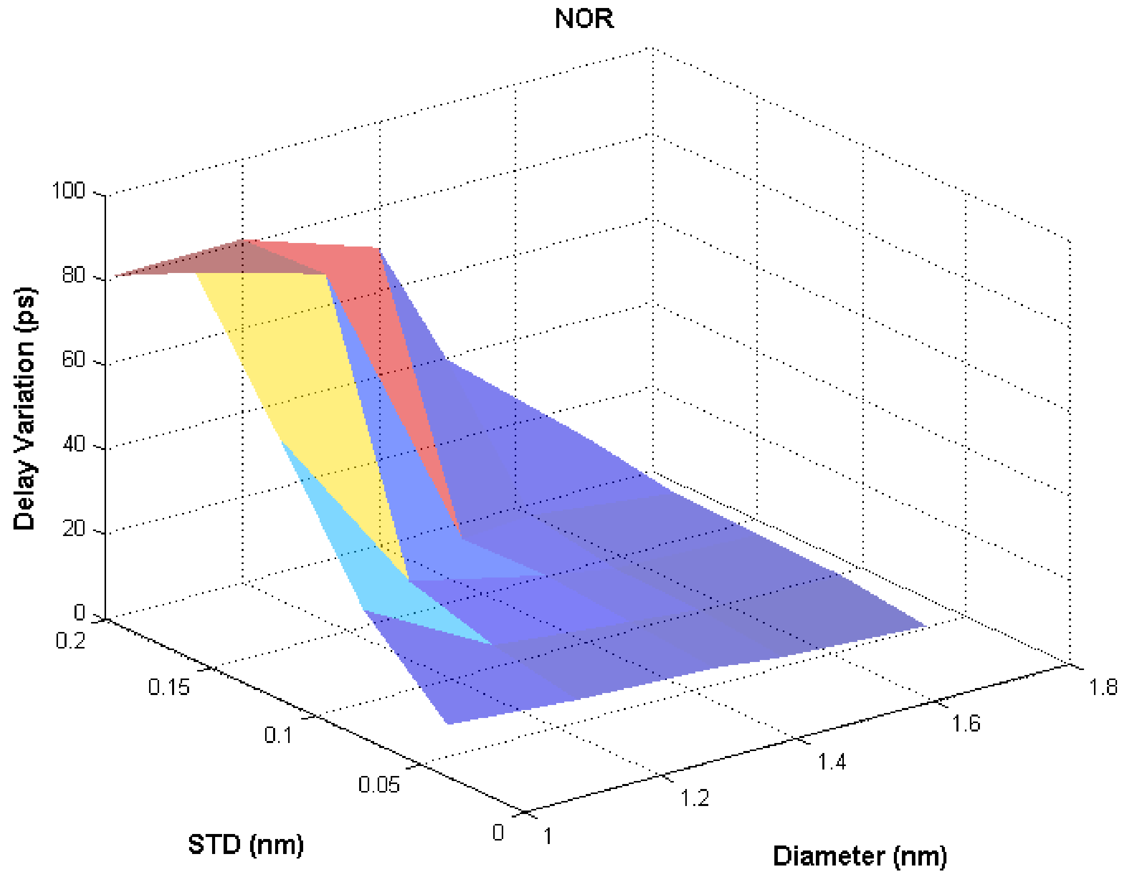


**Figure 3.17. NOR Delay Variation with change in CNT Diameter & STD**

Figure 3.17 shows that for the NOR gates, again delay variation rises significantly at smaller mean diameters and greater STD values. Fall time is reached faster than rise time for the NOR gates. Similar to the structure of the pull up network in a conventional CMOS NOR gate, the pull up network of the CNT-based NOR gate in this work consists of 2 PCNFETs in series. The pull down network is made of 2 NCNFETs in parallel. Carriers experience less resistance through the 2 parallel n-type transistors of the pull-down network and fall time is shorter than rise time. As far as delay variation is concerned a great variation for diameters smaller than around 0.85nm is observed in fig. 3.16.

The delay behaviour and maximum variation in fall/rise times are shown in tables 3.5 and 3.6 respectively. It is observed that variation in delay is most in smaller CNT mean diameters and more stability is achieved with larger CNT mean diameters.

Table3.5: NOR Gates delay behaviour

| Mean Diameter(nm) | Diameter STD (nm) | Mean Delay $T_d$ (ps) | Min. Delay (ps) | Max. Delay (ps) | $\Delta T_d$ (ps) |
|---|---|---|---|---|---|
| **1.01** | 0.04 | 6.14 | 4.78 | 8.37 | 3.59 |
| | 0.08 | 6.29 | 3.84 | 20.97 | 17.13 |
| | 0.12 | 6.68 | 3.03 | 37.82 | 34.79 |
| | 0.16 | 7.3 | 2.82 | 42.49 | 39.67 |
| | 0.2 | 7.8 | 2.72 | 42.21 | 39.49 |
| **1.2** | 0.04 | 5.13 | 4.1 | 6.19 | 2.08 |
| | 0.08 | 5.17 | 3.31 | 8.34 | 5.04 |
| | 0.12 | 5.23 | 3.05 | 15.69 | 12.64 |
| | 0.16 | 5.38 | 2.92 | 43.69 | 40.78 |
| | 0.2 | 5.67 | 2.42 | 48.12 | 45.7 |
| **1.4** | 0.04 | 4.32 | 3.49 | 5.16 | 1.66 |
| | 0.08 | 4.33 | 3.24 | 6.18 | 2.95 |
| | 0.12 | 4.37 | 2.49 | 7.81 | 5.33 |
| | 0.16 | 4.43 | 2.49 | 11.76 | 9.27 |
| | 0.2 | 4.53 | 2.57 | 32.19 | 29.62 |
| **1.5** | 0.04 | 3.9 | 3.4 | 4.76 | 1.46 |
| | 0.08 | 3.95 | 2.69 | 5.7 | 3.01 |
| | 0.12 | 4 | 2.65 | 6.75 | 4.1 |
| | 0.16 | 4.08 | 2.65 | 8.86 | 6.21 |
| | 0.2 | 4.16 | 2.55 | 16.45 | 13.9 |
| **1.71** | 0.04 | 3.45 | 2.79 | 3.8 | 1.01 |
| | 0.08 | 3.45 | 2.52 | 4.56 | 2.04 |
| | 0.12 | 3.47 | 2.69 | 5.49 | 2.81 |
| | 0.16 | 3.54 | 2.69 | 6.51 | 3.81 |
| | 0.2 | 3.63 | 2.73 | 8.32 | 5.59 |

Table 3.6: NOR Gates Rise/Fall times Variation

| Mean Diameter(nm) | Diameter STD (nm) | Max Rise/Fall (ps) | Min. Rise/Fall(ps) | $\Delta T_d$ (ps) |
|---|---|---|---|---|
| **1.01** | 0.04 | 16.43 | 5.46 | 10.97 |
| | 0.08 | 44.1 | 4.91 | 39.19 |
| | 0.12 | 74.28 | 4.27 | 70.01 |
| | 0.16 | 84.92 | 4.23 | 80.69 |
| | 0.2 | 84.42 | 4.06 | 80.36 |
| **1.2** | 0.04 | 12.9 | 5.32 | 7.58 |
| | 0.08 | 16.09 | 4.54 | 11.55 |
| | 0.12 | 14.8 | 4.47 | 10.33 |
| | 0.16 | 86.08 | 4.36 | 81.72 |
| | 0.2 | 94.8 | 4.36 | 90.44 |
| **1.4** | 0.04 | 11.83 | 4.87 | 6.96 |
| | 0.08 | 12.93 | 4.77 | 8.16 |
| | 0.12 | 15.61 | 4.7 | 10.91 |
| | 0.16 | 22.98 | 4,69 | 18.29 |
| | 0.2 | 65.13 | 4.71 | 60.43 |
| **1.5** | 0.04 | 11.06 | 4.81 | 6.25 |
| | 0.08 | 12.41 | 4.78 | 7.63 |
| | 0.12 | 13.87 | 4.78 | 9.09 |
| | 0.16 | 17.12 | 4.78 | 12.34 |
| | 0.2 | 33.21 | 4.17 | 29.04 |
| **1.71** | 0.04 | 8.61 | 4.97 | 3.64 |
| | 0.08 | 10.5 | 4.96 | 5.54 |
| | 0.12 | 12.28 | 4.96 | 7.32 |
| | 0.16 | 13.55 | 4.95 | 8.6 |
| | 0.2 | 16.02 | 4.96 | 11.06 |

### *3.2.2.2 Power Consumption*

**Table 3.7: NOR Power Consumption**

| Mean Diameter(nm) | Diameter STD (nm) | Mean Power(nW) | Min. Power (nW) | Max. Power(nW) | ΔP (nW) | PDP ($*10^{-20}$ J) | PDP Variation ($*10^{-20}$ J) |
|---|---|---|---|---|---|---|---|
| **1.01** | 0.04 | 4.61 | 4.53 | 4.72 | 0.19 | 28.3054 | 0.6821 |
| | 0.08 | 4.62 | 4.42 | 4.9 | 0.48 | 29.0598 | 8.22 |
| | 0.12 | 4.62 | 4.33 | 5.29 | 0.95 | 30.8616 | 33.05 |
| | 0.16 | 4.62 | 4.32 | 5.9 | 1.58 | 33.726 | 62.6786 |
| | 0.2 | 4.63 | 4.32 | 6.87 | 2.55 | 36.114 | 100.7 |
| **1.2** | 0.04 | 5.08 | 4.98 | 5.29 | 0.32 | 26.0604 | 0.6656 |
| | 0.08 | 5.09 | 4.94 | 5.7 | 0.77 | 26.3153 | 3.88 |
| | 0.12 | 5.1 | 4.86 | 6.35 | 1.49 | 26.673 | 18.83 |
| | 0.16 | 5.12 | 4.78 | 7.35 | 2.57 | 27.5456 | 104.8 |
| | 0.2 | 5.14 | 4.76 | 7.3 | 2.54 | 29.1438 | 116.078 |
| **1.4** | 0.04 | 5.59 | 5.4 | 6.05 | 0.66 | 24.1488 | 1.0956 |
| | 0.08 | 5.61 | 5.26 | 6.72 | 1.46 | 24.2913 | 4.307 |
| | 0.12 | 5.64 | 4.36 | 7.75 | 3.39 | 24.6468 | 18.0687 |
| | 0.16 | 5.67 | 4.22 | 7.96 | 3.74 | 25.1181 | 34.67 |
| | 0.2 | 5.71 | 5.09 | 7.95 | 2.85 | 25.8663 | 84.42 |
| **1.5** | 0.04 | 5.93 | 5.05 | 6.5 | 1.45 | 23.127 | 2.11 |
| | 0.08 | 5.94 | 5.45 | 7.18 | 1.73 | 23.463 | 5.2073 |
| | 0.12 | 5.96 | 5.35 | 7.71 | 2.37 | 23.84 | 9.717 |
| | 0.16 | 5.99 | 5.28 | 8 | 2.72 | 24.4392 | 16.89 |
| | 0.2 | 6.02 | 5.25 | 8.01 | 2.76 | 25.0432 | 38.36 |
| **1.71** | 0.04 | 6.71 | 6.28 | 7.5 | 1.23 | 23.1495 | 1.24 |
| | 0.08 | 6.74 | 5.9 | 8.1 | 2.2 | 23.253 | 4.488 |
| | 0.12 | 6.75 | 5.66 | 8.15 | 2.48 | 23.4225 | 6.9688 |
| | 0.16 | 6.74 | 5.66 | 8.14 | 2.58 | 23.8596 | 9.8298 |
| | 0.2 | 6.69 | 5.54 | 8.15 | 2.26 | 24.2487 | 12.6334 |

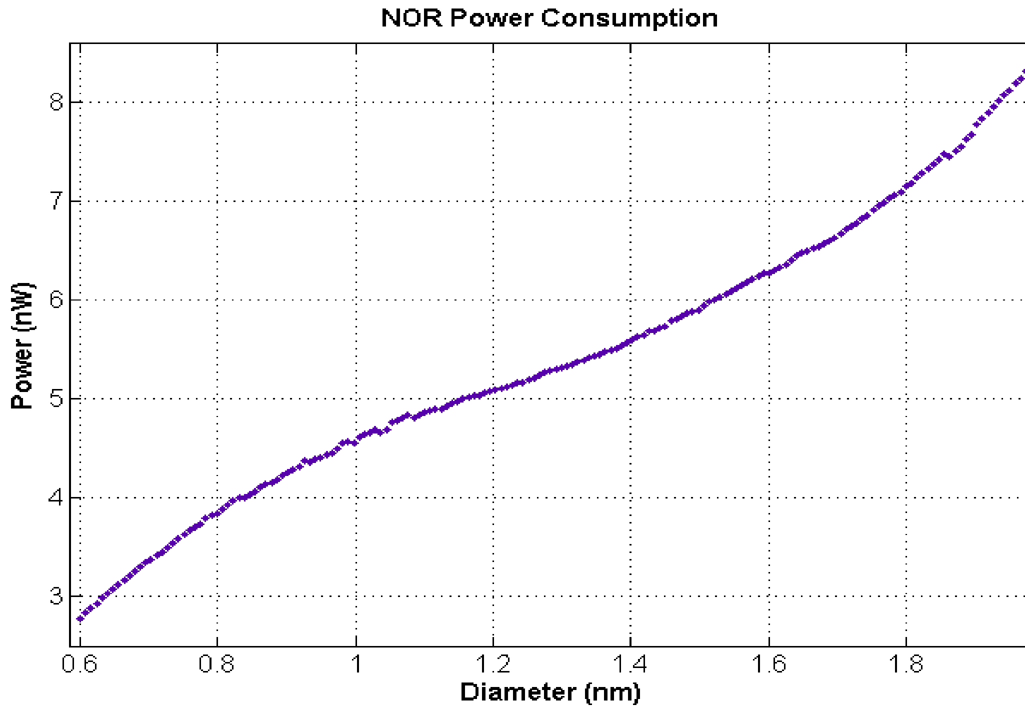


**Figure 3.18: NOR Gates Power Consumption**

Power consumption of the NOR gates and its variation follows the same trend as that of the NAND gates described in the previous section. Power consumption rises with increasing CNT diameter as more drive current is provided.

**Table 3.8: Variation of NOR Gates Power Consumption with mean Diameter**

| Mean Diameter (nm) | % Variation (STD = 0.04nm) | %Variation (STD = 0.2nm) |
|---|---|---|
| 1.01 | 4 | 55 |
| 1.2 | 6 | 49 |
| 1.4 | 12 | 50 |
| 1.5 | 24 | 46 |
| 1.71 | 18 | 34 |

Percentage variation of power is smaller at small mean diameters and STDs. Power consumption varies from 4% to 24% of the total power consumption of the gates depending on mean diameter

for a STD of 0.04nm (Table 3.8). The conclusion to be made from table 3.8 is that larger CNT diameters and smaller diameter STDs ensure less variation in power consumption. However referring to table 3.7 and Fig. 3.18, it can be seen that larger diameters translate into higher power consumption; hence there is a trade-off between higher power consumption and less variation in power consumption which should be met according to the desired design.

As with the case of the NAND gates studied in section 3.2.1, provided that a STD in diameter of smaller than 0.12nm can be achieved, larger mean CNT diameters perform better in terms of delay and PDP variation.

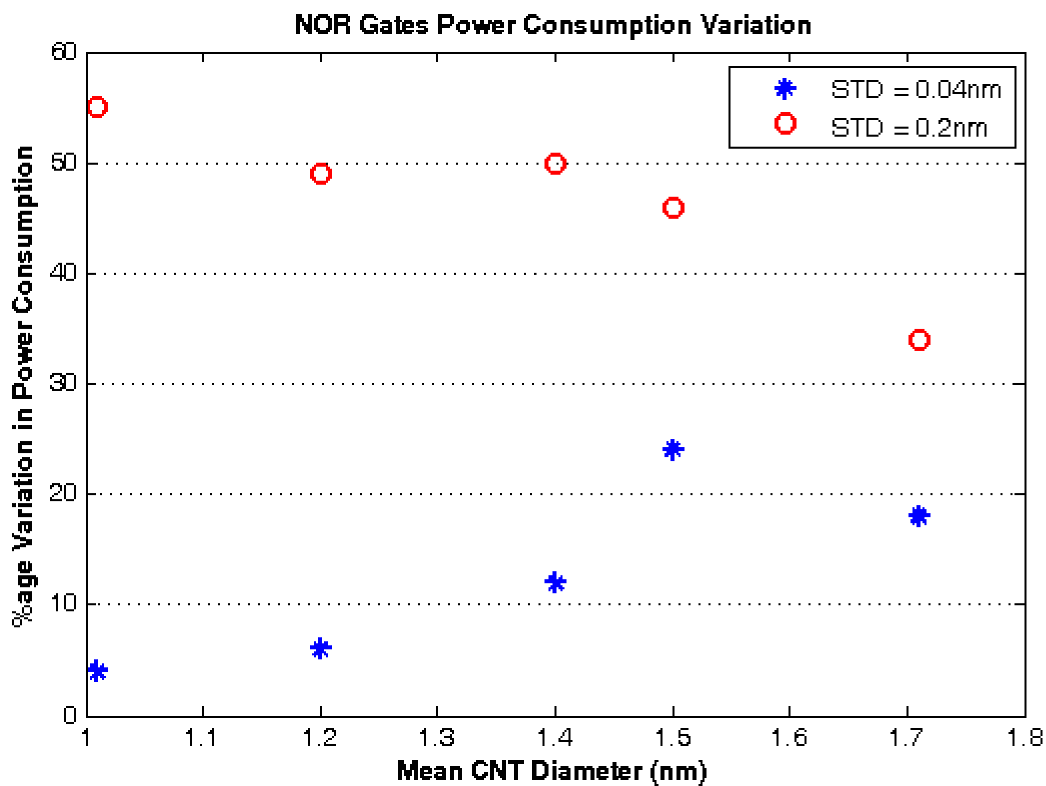


**Figure 3.19: Variation in NOR Gates Power Consumption**

*3.2.3 NOT Gate*

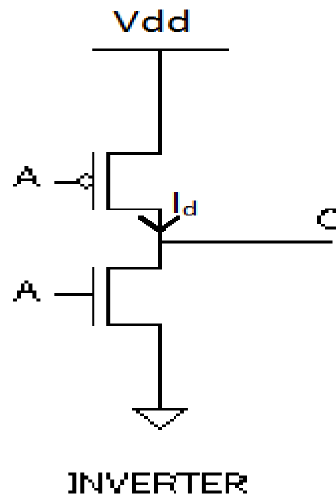


**Figure 3.20: Inverter Schematic**

NOT gates have been implemented and simulated. All simulation conditions are as for NAND and NOR gates described in previous sections. Timing characteristics and power consumption of the gates are studied in this section.

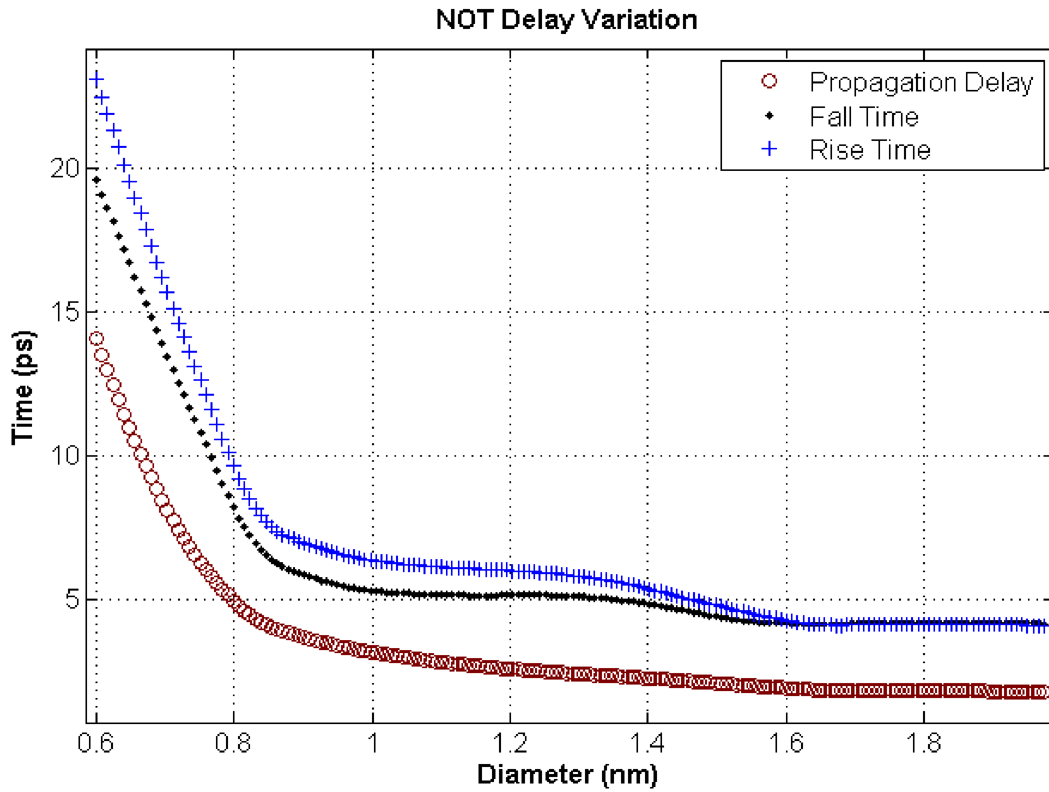


**Figure 3.21: NOT Gates Timing Behaviour**

### *3.2.3.1. Timing Behaviour*

Table 3.9 shows the time-delay behaviour of the NOT gates simulated.

**Table 3.9: NOT Gates Delay Behaviour**

| Mean Diameter(nm) | Diameter STD (nm) | Mean Delay $T_d$ (ps) | Min. Delay (ps) | Max. Delay (ps) | $\Delta T_d$ (ps) |
|---|---|---|---|---|---|
| **1.01** | 0.04 | 3.78 | 2.9 | 5.27 | 2.37 |
| | 0.08 | 3.88 | 2.36 | 12.08 | 9.72 |
| | 0.12 | 4.12 | 1.91 | 23.28 | 21.37 |
| | 0.16 | 4.49 | 1.76 | 26.29 | 24.53 |
| | 0.2 | 4.78 | 1.7 | 26.09 | 24.39 |
| | 0.04 | 3.04 | 2.47 | 3.7 | 1.23 |
| | 0.08 | 3.07 | 2.01 | 5.04 | 3.03 |
| | 0.12 | 3.11 | 1.86 | 9.35 | 7.49 |

| 1.2 | 0.16 | 3.21 | 1.78 | 25.58 | 23.8 |
|---|---|---|---|---|---|
| | 0.2 | 3.39 | 1.72 | 28.51 | 26.79 |
| 1.4 | 0.04 | 2.52 | 2.07 | 2.98 | 0.91 |
| | 0.08 | 2.53 | 1.93 | 3.55 | 1.62 |
| | 0.12 | 2.55 | 1.85 | 4.59 | 2.74 |
| | 0.16 | 2.58 | 1.83 | 7.08 | 5.25 |
| | 0.2 | 2.64 | 1.74 | 17.97 | 16.23 |
| 1.5 | 0.04 | 2.27 | 2.01 | 2.72 | 0.71 |
| | 0.08 | 2.3 | 1.91 | 3.19 | 1.28 |
| | 0.12 | 2.33 | 1.88 | 3.9 | 2.02 |
| | 0.16 | 2.37 | 1.8 | 5.26 | 3.46 |
| | 0.2 | 2.43 | 1.79 | 9.44 | 7.65 |
| 1.71 | 0.04 | 2.02 | 1.92 | 2.19 | 0.27 |
| | 0.08 | 2.03 | 1.85 | 2.6 | 0.75 |
| | 0.12 | 2.05 | 1.83 | 3.07 | 1.24 |
| | 0.16 | 2.09 | 1.83 | 3.65 | 1.82 |
| | 0.2 | 2.14 | 1.83 | 4.64 | 2.81 |

**Table 3.10: NOT Gates Rise/Fall times Variation**

| Mean Diameter(nm) | Diameter STD (nm) | Max Rise/Fall (ps) | Min. Rise/Fall(ps) | $\Delta T_d$ (ps) |
|---|---|---|---|---|
| **1.01** | 0.04 | 8.29 | 4.63 | 3.66 |
| | 0.08 | 20.24 | 4.09 | 16.15 |
| | 0.12 | 35.74 | 3.43 | 32.31 |
| | 0.16 | 39.9 | 3.33 | 36.57 |
| | 0.2 | 40.08 | 3.29 | 36.79 |
| **1.2** | 0.04 | 6.54 | 4.48 | 2.06 |
| | 0.08 | 8 | 3.69 | 4.32 |
| | 0.12 | 15.53 | 3.52 | 12 |
| | 0.16 | 40.41 | 3.48 | 36.93 |
| | 0.2 | 45.21 | 3.41 | 41.8 |

| | | | | |
|---|---|---|---|---|
| **1.4** | 0.04 | 6.15 | 3.99 | 2.16 |
| | 0.08 | 6.57 | 3.86 | 2.7 |
| | 0.12 | 7.62 | 3.78 | 3.84 |
| | 0.16 | 11.59 | 3.76 | 7.83 |
| | 0.2 | 29.96 | 3.67 | 26.29 |
| **1.5** | 0.04 | 5.72 | 4.02 | 1.7 |
| | 0.08 | 6.35 | 3.93 | 2.43 |
| | 0.12 | 6.95 | 3.89 | 3.06 |
| | 0.16 | 8.61 | 3.82 | 4.79 |
| | 0.2 | 16.08 | 3.81 | 12.27 |
| **1.71** | 0.04 | 4.65 | 4.05 | 0.6 |
| | 0.08 | 5.44 | 4 | 1.44 |
| | 0.12 | 6.23 | 3.97 | 2.26 |
| | 0.16 | 6.8 | 3.96 | 2.84 |
| | 0.2 | 8 | 3.96 | 4.04 |

Tables 3.9 and 3.10 reveal that an increase in mean diameter together with a decrease in diameter STD, significantly lowers the worst case time-delay variation.

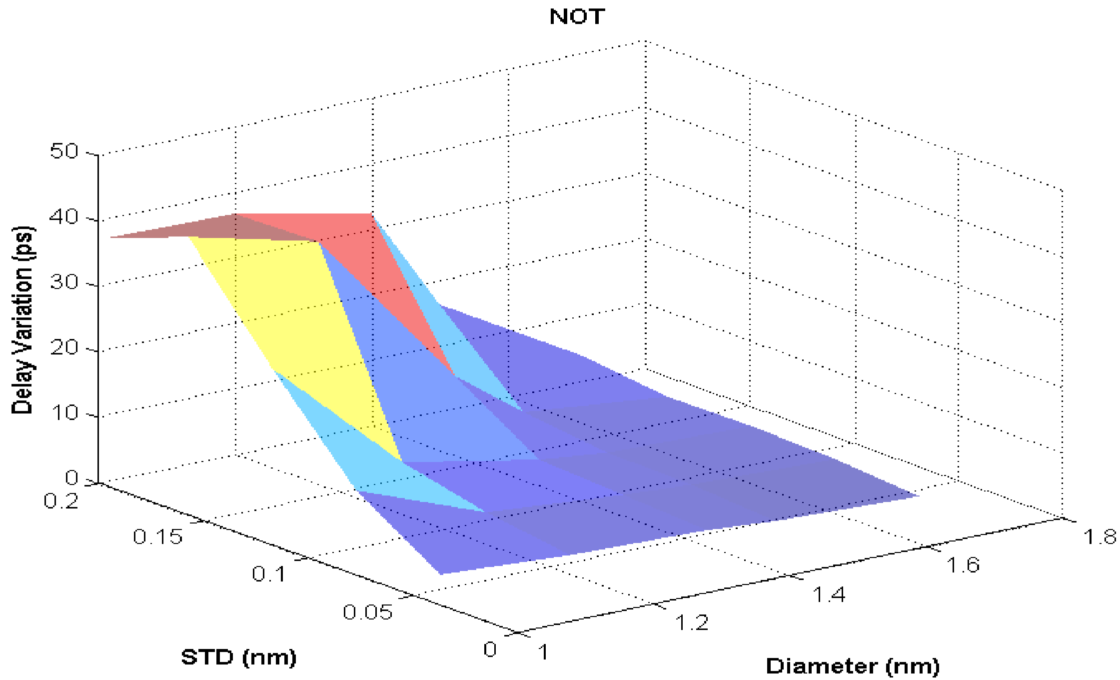


**Figure 3.22: NOT Gates Delay Variation with CNT Diameter Mean & STD**

Figure 3.22 shows variation in time delay of an inverter with respect to CNT mean diameter and STD. It can be observed from the plot that for smaller STDs, variation in delay is relatively small at ~13%. As STD increases delay variation also increases. The variation in delay becomes very significant for bigger STDs and smaller CNT mean diameters. Results show that there is greater delay variation at smaller diameters of CNTs. As the energy band gap of a CNT is inversely proportional to its diameter [93], CNTs with larger diameters have smaller energy band gaps. A smaller energy band gap means that a transistor made of CNTs with larger diameters can exhibit higher on-currents and hence shorter delay times. CNTs with smaller diameters have higher source/drain resistance which can be explained by the fact that at small diameters only the first sub-band is degenerate [74]. Fig. 3.20 shows the timing characteristics of the simulated inverters. The fall and rise times show very similar behaviour and are close to each other. This is due to the equal electron and hole mobility in CNTs [54]. It is observed from fig. 3.21 that below a diameter of around 0.85nm delay dependency on diameter increases resulting in a rapid rise in delay variation.

*3.2.3.2 Power Consumption*

**Table 3.11: NOT Gates Power Consumption**

| Mean Diameter(nm) | Diameter STD (nm) | Mean Power(nW) | Min. Power (nW) | Max. Power(nW) | ΔP (nW) | PDP ($*10^{-20}$ J) | PDP Variation ($*10^{-20}$ J) |
|---|---|---|---|---|---|---|---|
| **1.01** | 0.04 | 6.6 | 4.26 | 8.34 | 4.08 | 24.95 | 9.67 |
| | 0.08 | 6.61 | 5.29 | 8.6 | 3.31 | 25.65 | 32.17 |
| | 0.12 | 6.62 | 4.59 | 9.62 | 5.04 | 27.27 | 107.7 |
| | 0.16 | 6.62 | 4.28 | 10.19 | 5.91 | 29.72 | 144.97 |
| | 0.2 | 6.64 | 4.52 | 10.35 | 5.83 | 31.74 | 142.19 |
| **1.2** | 0.04 | 7.32 | 6.06 | 9.35 | 3.29 | 22.25 | 4.05 |
| | 0.08 | 7.3 | 4.06 | 9.41 | 5.34 | 22.41 | 16.18 |
| | 0.12 | 7.31 | 5.52 | 10.34 | 4.82 | 22.73 | 36.1 |
| | 0.16 | 7.33 | 3.22 | 12.04 | 8.82 | 23.53 | 209.92 |
| | 0.2 | 7.35 | 3.97 | 10.34 | 6.37 | 24.92 | 170.65 |
| **1.4** | 0.04 | 7.96 | 5.99 | 9.63 | 3.64 | 20.06 | 3.31 |
| | 0.08 | 7.98 | 7.58 | 11.31 | 3.73 | 20.19 | 6.04 |
| | 0.12 | 8 | 6.49 | 10.12 | 3.63 | 20.4 | 9.95 |
| | 0.16 | 8.04 | 7.23 | 10.32 | 3.09 | 20.74 | 16.22 |
| | 0.2 | 8.08 | 6.48 | 10.31 | 3.83 | 21.33 | 62.16 |
| **1.5** | 0.04 | 8.35 | 6.59 | 11.07 | 4.48 | 18.95 | 3.18 |
| | 0.08 | 8.37 | 6.99 | 9.73 | 2.74 | 19.25 | 3.51 |
| | 0.12 | 8.39 | 7.73 | 11.22 | 3.49 | 19.55 | 7.05 |
| | 0.16 | 8.42 | 6.7 | 10.33 | 3.63 | 20 | 12.56 |
| | 0.2 | 8.45 | 6.88 | 10.84 | 3.96 | 20.53 | 30.29 |
| **1.71** | 0.04 | 9.14 | 8.67 | 9.98 | 1.31 | 18.46 | 0.35 |
| | 0.08 | 9.16 | 8.34 | 10.51 | 2.17 | 18.6 | 1.63 |
| | 0.12 | 9.19 | 8.11 | 10.56 | 2.45 | 18.84 | 3.04 |
| | 0.16 | 9.18 | 8 | 10.56 | 2.55 | 19.19 | 4.64 |
| | 0.2 | 9.14 | 7.93 | 10.56 | 2.63 | 19.56 | 7.39 |

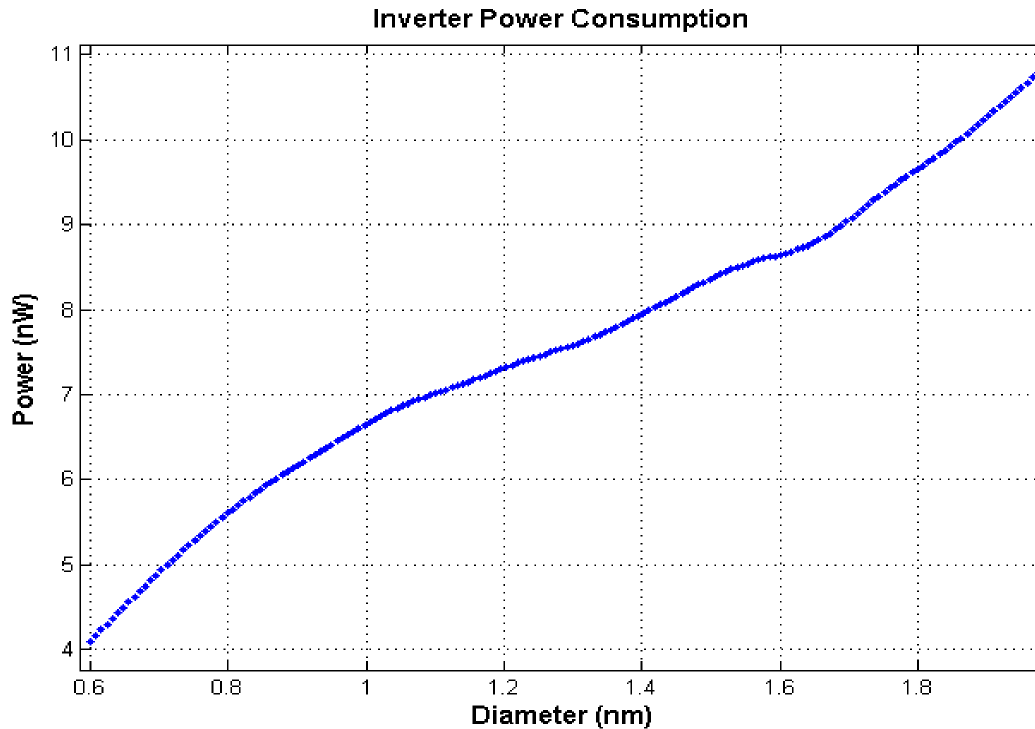


**Figure 3.23: NOT Gates Power Consumption**

Fig. 3.23 shows the rise in power consumption with increasing CNT diameter due to the decreased band gap. Table 3.14 reveals that variation in power consumption decreases with increasing CNT diameter. So for the NOT gates again the same behaviour is observed as that for NOR and NAND gates. The trade-off of power consumption versus variation in power consumption has proven to be a common feature for all the logic gates studied so far. According to table 3.14, if a design needs minimum power variation, the largest diameter considered in the simulations (1.71nm) would be the ideal choice as this introduces a variation of 14% of the total power consumption for the case of STD = 0.04nm, and a variation of 29% for a STD of 0.2nm; figures which are by far better than the existing variation in smaller mean diameters.

The PDP values do not show very significant changes with changing diameter compared with the actual variation in the PDP from one diameter to the next. For the mean diameter of 1.71nm PDP changes from a minimum of $18.46e^{-20}$J to a maximum of $19.56e^{-20}$J. Considering all the mean diameters and the STD values, PDP only changes in the range of $18.46\text{-}^{e-20}$ to $31.74^{e-20}$J. Variation in PDP however, increases significantly from less than $1e^{-20}$J to over $200e^{-20}$J for different diameter

STD especially at smaller CNT mean diameters, again suggesting the use of larger mean CNT diameters if variation is to be kept at a minimum.

**Table 3.14 Variation of NOT Gates Power Consumption with mean Diameter at STD of 0.04nm and 0.2nm**

| Mean Diameter (nm) | % Variation (STD = 0.04nm) | %Variation (STD = 0.2nm) |
|---|---|---|
| 1.01 | 62% | 88 |
| 1.2 | 45% | 87 |
| 1.4 | 46% | 47 |
| 1.5 | 54% | 47 |
| 1.71 | 14% | 29 |

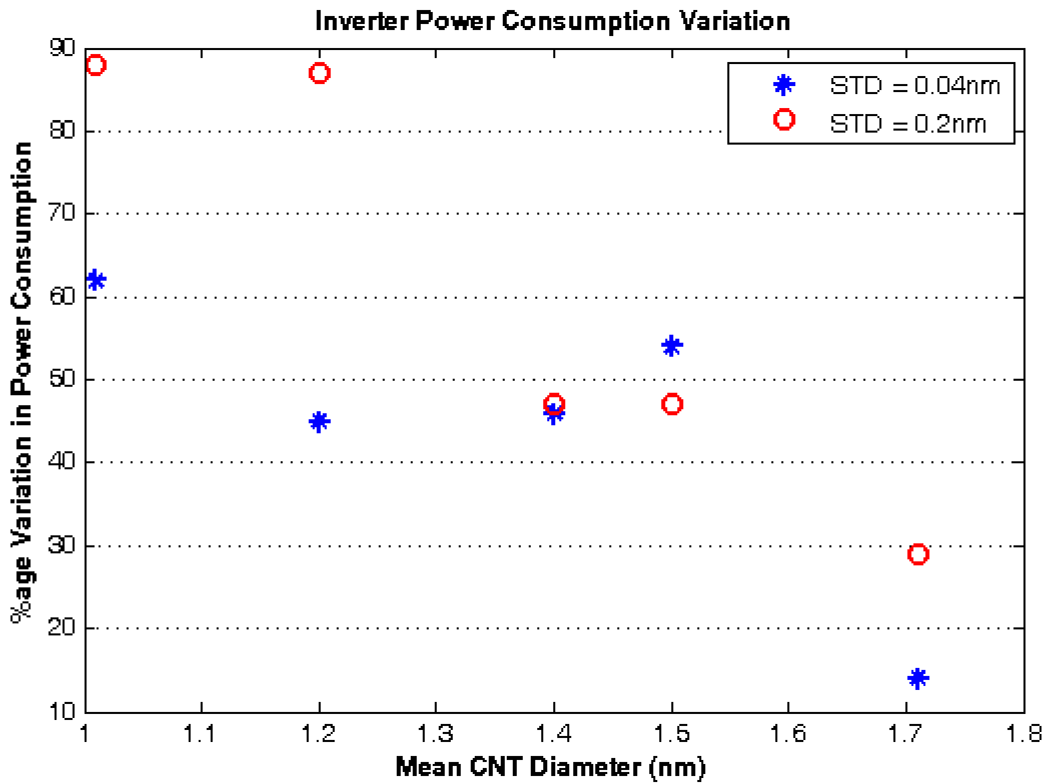


**Figure 3.24: Variation in Inverters Power Consumption**

## 3.4 Modelling of Delay

In this section the development of predictive models based on the simulation results obtained so far is detailed. The results of the extensive and costly HSPICE Monte Carlo simulations are used in this section to develop mathematical models based on Response Surface Methodology which would be able to predict circuit performance parameters based on a given CNT diameter distribution. Modelling of the various circuit performance parameters is needed for the design process. The predictive models developed in this section are facilitators for the CNT design process. The models developed are used to predict the propagation delay mean and STD of the various logic gates considered in the presence of CNT diameter variations.

### *3.4.1 Response Surface Methodology*

Response Surface Methodology (RSM) regression technique has been applied to devise a predictive model for the behaviour of the logic gates studied in this work. RSM in general is a collection of mathematical and statistical techniques useful for developing, improving and optimizing processes [105]. RSM is particularly useful in situations where several input variables potentially influence some performance measure or quality characteristic of the process. The performance measure or quality characteristic is called the *response* and the input variables are called the *independent variables*. For the case of two independent variables, the first order model is:

$$\eta = \beta_0 + \beta_1 x_1 + \beta_2 x_2 \quad (3.1)$$

Where $x_1$ and $x_2$ are the independent variables and the response $\eta$ depends on these variables. $\beta_0$, $\beta_1$ and $\beta_2$ are the model parameters which are estimated by the regression process. Equation (3.1) is also called a *main effects model* as it only includes the main effects of the two variables $x_1$ and $x_2$. To account for any interaction between the variables, the model can be modified to become:

$$\eta = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{12} x_1 x_2 \quad (3.2)$$

The interaction between the two variables renders the response function more complicated and often the first order model is inadequate for more complicated problems, hence, a second order model becomes necessary. With two variables, the second order model becomes:

$$\eta = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{11} x_1^2 + \beta_{22} x_2^2 + \beta_{12} x_1 x_2 \quad (3.3)$$

The second order model is widely used in RSM as it is very flexible and can take a variety of functional forms, so it will be a good approximation to the true response surface. Also it is easy to estimate the β parameters using the least squares method in the second order model. Furthermore there is considerable practical experience indicating that second-order models work well in solving real response surface problems.

*3.4.2 Model Verification*

To verify and test the obtained model for accuracy the $R^2$ measure is used. The $R^2$ is a measure of the amount of reduction in the variability of the response η obtained by using the independent variables $x_1$ and $x_2$. The value for $R^2$ always lies in the range $0 \leq R^2 \leq 1$. An $R^2$ value close to 1 usually indicates high accuracy and a value close to 0 usually indicates low accuracy of the model; however, a large $R^2$ value does not necessarily imply that the model is an accurate one as adding a variable to the model will always increase $R^2$ regardless of whether the additional variable is statistically significant or not, hence even a model with a large $R^2$ value could yield poor estimates of the mean response.

To overcome this limitation of the $R^2$, in this work the *adjusted* $R^2$ value is used:

$$R^2_{adj} = 1 - \frac{n-1}{n-p}(1 - R^2) \quad (3.4)$$

Where $R^2_{adj}$ is the adjusted $R^2$ value, $n$ is the number of observations and $p$ is the number of regression coefficients.

Generally, the adjusted $R^2$ will not always increase as variables are added to the model; in fact, if unnecessary terms are added, the value of $R^2_{adj}$ will often decrease.

*3.4.3 Model of Mean Propagation Delay of Logic Gates*

To develop the statistical model, consider the fact that the variables are CNT diameter mean $D_\mu$ and STD $D_\delta$. The ranges of mean propagation delay and mean CNT diameter are much bigger than the STD of diameter. Also the effect of $D_\delta$ on the response variable, that is, mean propagation delay in this case, is less than that of $D_\mu$; hence, the log transformation is used to improve the accuracy of the model [106]. The logarithm used is the natural logarithm with the constant *e* as its base.

For the purpose of predicting the mean worst-case propagation delay of the NAND gates with any CNT diameter mean and STD, a second-order model is developed given by:

$$Log\left(Pd_\mu\right) = \beta_0 + \beta_1 Log\left(D_\mu\right) + \beta_2 D_\sigma + \beta_{12} D_\sigma Log\left(D_\mu\right) + \beta_{11}(Log\left(D_\mu\right))^2 + \beta_{22} {D_\sigma}^2 \quad (3.5)$$

Where $Pd_\mu$ is mean of worst-case propagation delay; $D_\mu$ is mean CNT diameter and $D_\sigma$ is CNT diameter STD. Hence, Log $D_\mu$ is replaced as $x_1$ in equation 3.4 and Log $D_\delta$ is replaced as $x_2$ in the equation.

By performing multiple linear regressions the coefficients for all the logic gates studied are found and presented in table 3.12:

**Table 3.12: Coefficients for prediction of mean propagation delay and $R^2_{adj}$ values for the RSM Models**

| | $\boldsymbol{\beta_0}$ | $\boldsymbol{\beta_1}$ | $\boldsymbol{\beta_2}$ | $\boldsymbol{\beta_{12}}$ | $\boldsymbol{\beta_{11}}$ | $\boldsymbol{\beta_{22}}$ | $\boldsymbol{R^2_{adj}}$ |
|---|---|---|---|---|---|---|---|
| **NAND** | 2.0138 | -1.5457 | 0.5899 | -2.3203 | 0.5261 | 3.2421 | 0.99294 |
| **NOR** | 1.81 | -1.25 | 0.56 | -2.28 | 0.48 | 3.11 | 0.9949 |
| **NOT** | 1.33 | -1.55 | 0.6 | -2.2 | 0.85 | 2.89 | 0.99584 |

The $R^2_{adj}$ values of the regressions are also found and presented in table 3.15. The $R^2_{adj}$ allows for the degrees of freedom associated with the sums of the squares. An $R^2_{adj}$ value of 0.99294 for the model of NAND gates therefore suggests that this is a reliable and accurate model for the prediction of mean worst case propagation delay of the NAND gates based on the MC simulation results as 99.294% of the samples can be explained reliably by the model.

*3.4.4 Model of STD in Propagation Delay of Logic Gates*

Based on the Monte Carlo simulation results, a statistical model can also be developed for prediction of STD in worst case propagation delay using the RSM regression model. CNT diameter STD has a considerable effect on the logic gates' delay STD; hence, to achieve good regression results, the log transformation is used:

$$Log\ (Pd_\sigma) = \gamma_0 + \gamma_1 Log(D_\mu) + \gamma_2 \log(D_\sigma) + \gamma_{12} Log(D_\sigma) Log(D_\mu) + \gamma_{11} \left(Log(D_\mu)\right)^2 + \gamma_{22} (Log(D_\sigma))^2 \quad (3.6)$$

The values for the coefficients of this model together with the $R^2_{adj}$ values are presented in table 3.13.

**Table 3.13: Coefficients for prediction of STD in propagation delay and $R^2_{adj}$ values for the RSM Models**

| | $\gamma_0$ | $\gamma_1$ | $\gamma_2$ | $\gamma_{12}$ | $\gamma_{11}$ | $\gamma_{22}$ | $R^2_{adj}$ |
|---|---|---|---|---|---|---|---|
| NAND | 5.82 | -5.54 | 2.74 | -1.16 | -1.86 | 0.23 | 0.95566 |
| NOR | 4.95 | -5.45 | 2.23 | -0.84 | -0.19 | 0.14 | 0.96328 |
| NOT | 5.19 | -5.84 | 2.86 | -1.02 | -1.26 | 0.26 | 0.97879 |

## 3.5 Discussion

The simulation results show that delay variations in all CNFET-based gates considered depend on both CNT mean diameter and STD. As an illustrative example in fig. 3.23 multiple Probability Density Function (PDF) curves are depicted for propagation delay of NAND gates with a CNT mean diameter of 1.71nm and various STDs, normally distributed in the range of 0.04nm to 0.2nm. It can be observed that as STD increases, the distribution of possible propagation delay values rises. The same PDF plots for smaller CNT mean diameters show far greater variations in propagation delay (Fig. 3.25), an expected result as the same STD values for smaller CNT mean diameters translate into greater deviations from the smaller mean diameters compared with larger mean diameters and hence greater drive current and delay variations.

The results show that inverter delay variation shows a 9 times improvement as mean diameter is increased from 1.01nm to the maximum mean diameter of 1.71nm. In the cases of NAND and

NOR gates delay variation shows an improvement by a factor of almost 7, suggesting that employing CNTs with larger diameters will minimize delay variations.

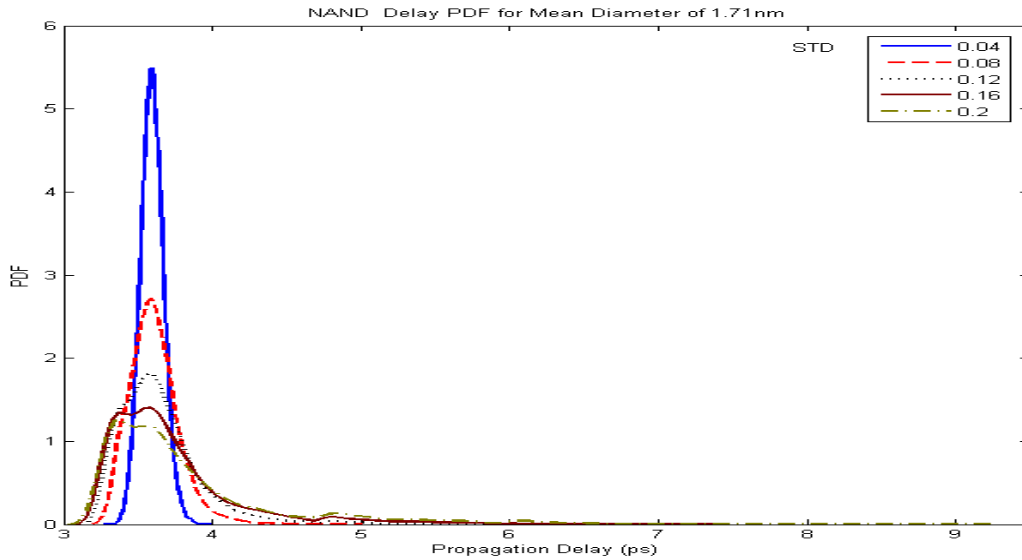


**Figure 3.25: PDF of Propagation delay of NAND Gates with various STD**

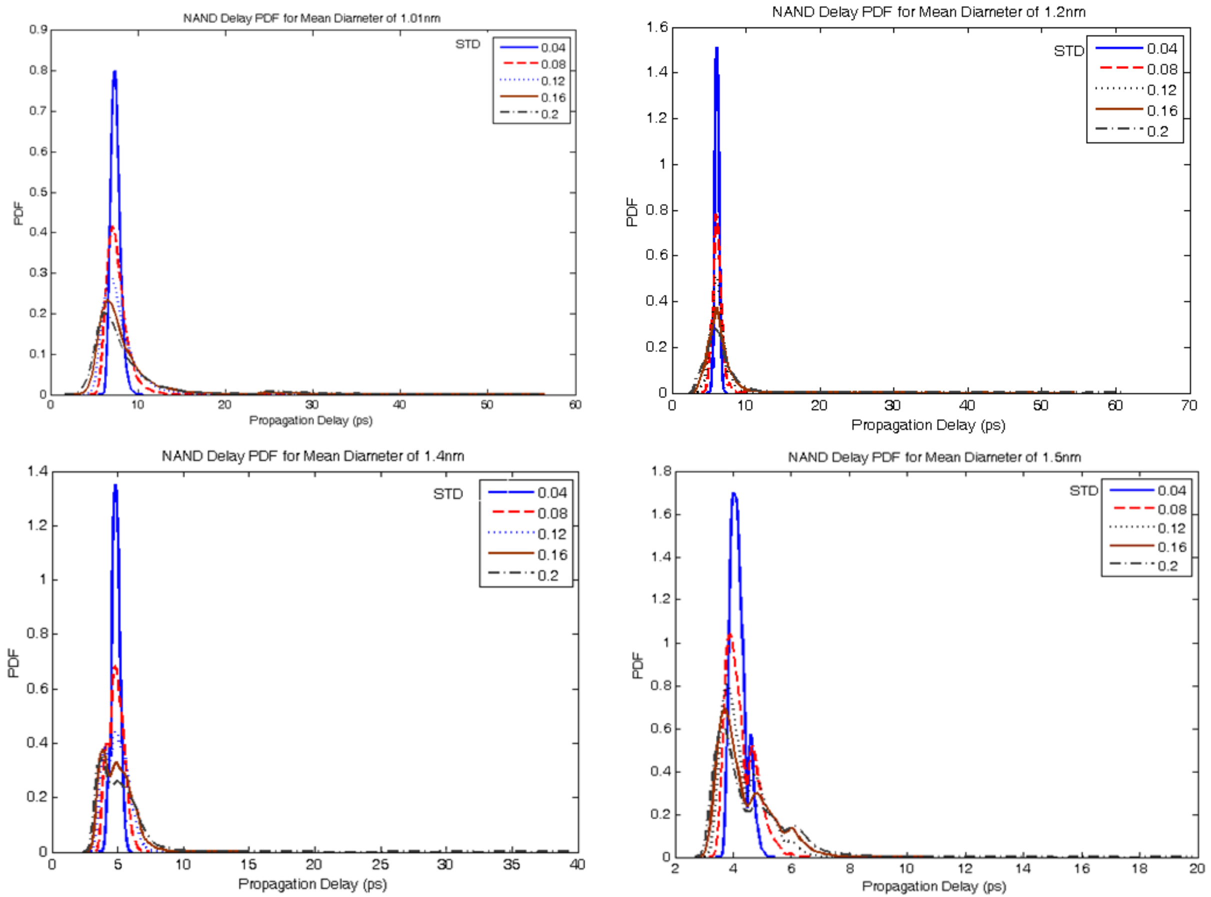


**Figure 3.26: PDF of Propagation Delay of NAND Gates with Various Mean Diameter & STDs**

Results for all simulated gates as seen in Figs. 3.8, 3.16 and 3.21 show that for all cases diameter should be kept above 0.85nm to ensure more consistent timing characteristics; hence:

$$D_{\mu} - \Delta D \geq 0.85nm \quad (3.7)$$

where, $D_{\mu}$ is mean CNT diameter and $\Delta D$ is diameter variation given by:

$$\Delta D = D_{\mu} x, \quad (3.11)$$

$x$ being a process-dependent constant defining the manufacturing tolerance (deviation from the mean) for fabrication of CNTs.

Thus, for consistent timing behaviour:

$$D_{\mu} \geq \frac{0.85nm}{1 - x} \quad (3.8)$$

For instance, assuming a process with a 30% manufacturing tolerance [10], for reliable timing operation a mean diameter is required defined by (3.8):

$$D_{\mu} \geq \frac{0.85nm}{1 - 0.3} \cong 1.2nm \quad (3.9)$$

## 3.6 Conclusion

It has been shown that larger CNT diameters and smaller STDs provide more reliable timing operation and faster delay times. A relation by which a minimum mean diameter can be chosen to ensure minimum delay variation for various CNT-based logic gates has been proposed. In order to propose an optimum CNT diameter for logic design a trade-off between fast operation and power consumption should be taken into account.

The work has shown that to keep power consumption minimum, smaller CNT diameters are desirable. However, smaller CNT diameters also have the highest variation in power consumption. Minimum power consumption variation is achieved by employing larger CNT diameters and smaller diameter STDs. This presents a three-way trade-off involving not only minimum power consumption and delay (variation), but also minimum power consumption and minimum variation in power consumption. Therefore, the designer should consider all the aspects of design and to use these guidelines accordingly based on the desired specification: speed, power consumption and robustness to variability.

# Chapter 4 Complex Logic Structures

To have a better understanding and a more conclusive study of CNFET-based structures it is necessary to investigate more complex structures which employ higher numbers of CNFETs.

Two very widely used structures in electronics are the multiplexer and the XOR gate. Multiplexers are employed heavily in telecommunications while XOR gates are utilised to implement binary addition in computers as an example.

Equal electron and hole mobility in SWCNT-based transistors translate into significant differences in rise and fall times of certain logic gates made such as NAND and NOR. One possible way around this problem could be the use of logic structures with an equal number of transistors (CNFETs) in their pull-up and pull-down networks for the design of CNT-based circuit structures. In this chapter multiplexer and XOR structures employing the same number of CNFETs in the pull-up as that of the pull-down network are proposed which are expected to exhibit relatively symmetric rise and fall times compared to structures which do not have this property.

The parameters rise time, fall time, propagation delay and power consumption for a multiplexer and an XOR structure are studied through simulations using HSPICE. The CNFET model used and the simulation conditions are identical to the conditions for other logic gates described in Chapter 3.

Further, predictive models for the prediction delay behaviour with respect to CNT diameter mean and standard deviation have been developed.

## 4.1. Multiplexer

The design of fig. 4.1 implements a restoring, inverting multiplexer. The design is in essence two tri-state inverters connected together. Apart from being restoring, the design has the advantage that the select (en1) and its complement (enb1) are mutually exclusive, thereby providing a simplified pull-up network. This approach to multiplexer design is also faster and more compact in comparison to other approaches (e.g. transmission gate approach or compound gates approach) because it requires less internal wiring. For the purpose of simulations, each transistor has 3 CNTs under the gate to improve current drive. The HSPICE code developed for simulation of this structure and to measure timing and power behaviour is provided in Appendix B.

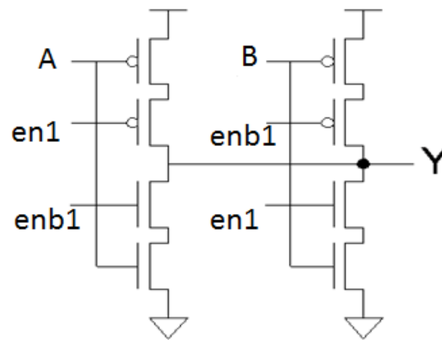


**Figure 4.1: Inverting Multiplexer**

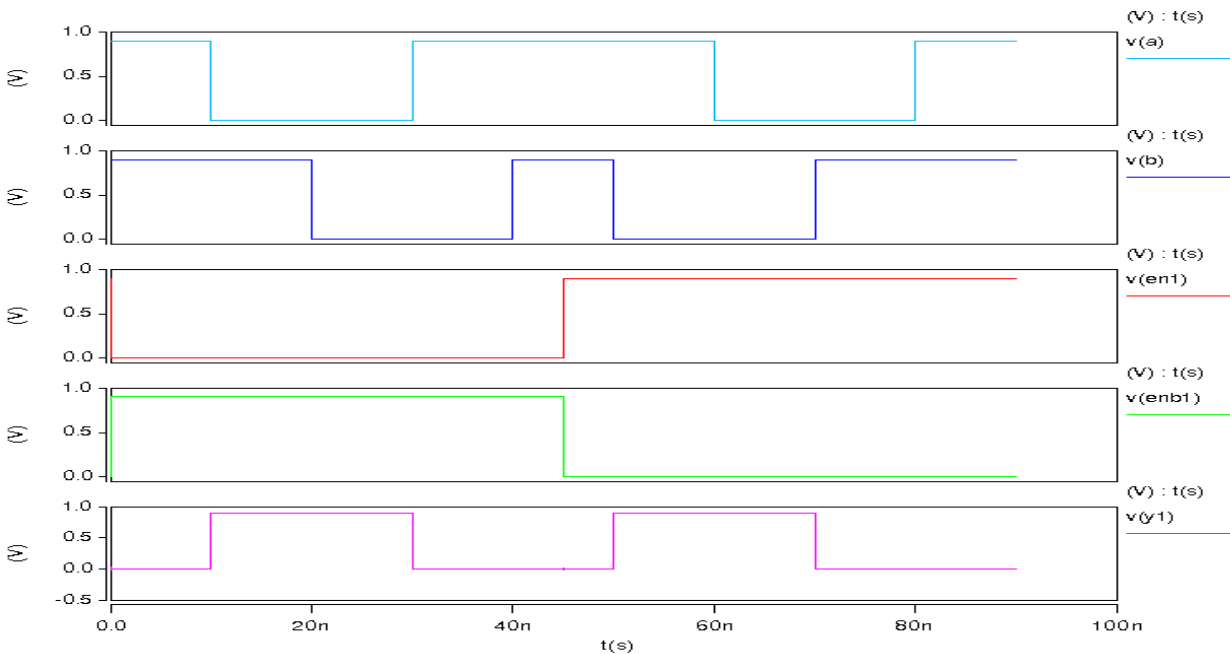


**Figure 4.2 Multiplexer input/output waveforms**

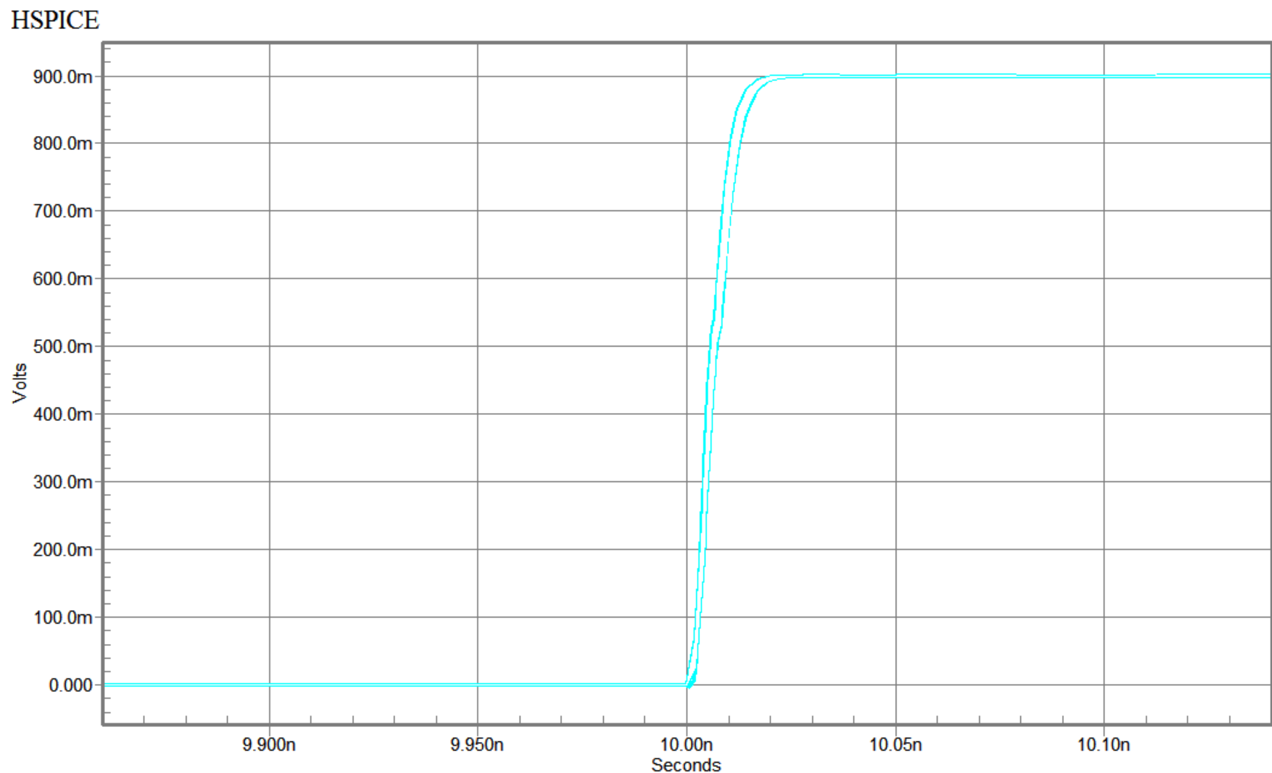


**Figure 4.3: Multiplexer output waveform showing a rising edge**

In fig 4.1, A and B represent the input voltages and en1 and enb1 represent the control voltage and its complement respectively. Y is the output of the inverting multiplexer. The details of the connections can be found in the netlist of Appendix B. The input/output waveforms to the multiplexer gates are shown in fig. 4.2. Fig. 4.3 shows a rising edge of the output waveform of the multiplexer (y1 in fig. 4.2) in more detail in a much smaller time window. MC simulation results for delay behaviour of the multiplexers are shown in tables 4.1 and 4.2. Power consumption of the gates together with power delay product (PDP) values and PDP variation (discussed in section 4.1.1) are shown in table 4.3.

**Table 4.1 Multiplexer Delay Behaviour**

| Mean Diameter(nm) | Diameter STD (nm) | Mean Delay $T_d$ (ps) | Min. Delay (ps) | Max. Delay (ps) | $\Delta T_d$ (ps) |
|---|---|---|---|---|---|
| **1.01** | 0.04 | 18.92 | 14.21 | 26.17 | 11.96 |
| | 0.08 | 19.43 | 9.81 | 48.01 | 38.28 |
| | 0.12 | 20.45 | 8.27 | 132.9 | 124.63 |
| | 0.16 | 22.19 | 7.08 | 149 | 141.92 |
| | 0.2 | 23.71 | 6.77 | 148.1 | 141.33 |
| **1.2** | 0.04 | 14.1 | 9.94 | 18.36 | 8.42 |
| | 0.08 | 14.03 | 8.2 | 23.22 | 15.02 |
| | 0.12 | 14.13 | 7.04 | 39.49 | 32.45 |
| | 0.16 | 14.51 | 6.44 | 133.3 | 126.86 |
| | 0.2 | 15.28 | 6.46 | 149.3 | 142.84 |
| **1.4** | 0.04 | 9.55 | 8.07 | 12.71 | 4.64 |
| | 0.08 | 9.82 | 6.94 | 16.53 | 9.59 |
| | 0.12 | 10.1 | 6.4 | 20.74 | 14.34 |
| | 0.16 | 10.46 | 6.61 | 29.72 | 23.11 |
| | 0.2 | 10.85 | 6.62 | 95.61 | 88.99 |
| **1.5** | 0.04 | 8.57 | 7.76 | 10.95 | 3.19 |
| | 0.08 | 8.75 | 6.56 | 14.26 | 7.71 |
| | 0.12 | 8.9 | 6.43 | 17.36 | 10.93 |
| | 0.16 | 9.12 | 6.32 | 23.26 | 16.94 |
| | 0.2 | 9.4 | 6.32 | 38.83 | 32.51 |
| **1.71** | 0.04 | 7.37 | 6.49 | 8.22 | 1.73 |
| | 0.08 | 7.35 | 6.34 | 9.21 | 2.87 |
| | 0.12 | 7.41 | 6.32 | 12.52 | 6.2 |
| | 0.16 | 7.53 | 6.32 | 15.59 | 9.27 |
| | 0.2 | 7.74 | 6.32 | 19.88 | 13.56 |

The following definitions of delays were used when doing measurements in HSPICE:

*Propagation delay*: maximum time from the input crossing 50% to the output crossing 50%. This has been taken as the high to low output transition for NAND gates and low to high output transition for NOT and NOR gates.

*Rise time*: time for a waveform to rise from 10% to 90% of its steady-state value

*Fall time*: time for a waveform to fall from 90% to 10% of its steady-state value

Table 4.1 shows the delay behaviour of simulated multiplexers. It can be observed that variation in delay increases with increasing standard deviation and reduced CNT diameter. At a CNT mean diameter of 1.71nm a variation of only 1.73ps can be observed for the multiplexers with a STD of 0.04nm. Compare this with a variation of 11.96ps for a CNT diameter of 1.01nm with the same STD value. If it is assumed that a CNT manufacturing process can only guarantee a 0.2nm STD from the mean diameter, again larger CNT diameters prove superior in terms of timing behaviour reliability as can be observed from tables 4.1 and 4.2. In this case the minimum CNT mean diameter of 1.01nm results in a delay deviation of 141ps as opposed to 13.56ps for the larger mean diameter of 1.71nm.

Table 4.2 details the worst case rise/fall delay behaviour of the simulated multiplexers. Smaller mean diameters show the most desirable characteristics in terms of speed and delay variation.

**Table 4.2: Multiplexer Worst Case Rise/Fall Delay Variation**

| Mean Diameter(nm) | Diameter STD (nm) | Max Rise/Fall (ps) | Min. Rise/Fall(ps) | $\Delta T_d$ (ps) |
|---|---|---|---|---|
| **1.01** | 0.04 | 46.01 | 27.68 | 18.33 |
| | 0.08 | 82.2 | 19.65 | 62.55 |
| | 0.12 | 221.5 | 17.15 | 204.35 |
| | 0.16 | 243.8 | 16.76 | 227.04 |
| | 0.2 | 252.1 | 16.28 | 235.82 |
| **1.2** | 0.04 | 35.77 | 19.88 | 15.89 |
| | 0.08 | 42.39 | 17.29 | 25.1 |
| | 0.12 | 63.51 | 16.58 | 46.93 |
| | 0.16 | 224.5 | 16.02 | 208.48 |
| | 0.2 | 244.2 | 16.04 | 228.46 |
| **1.4** | 0.04 | 26.95 | 17.23 | 9.72 |
| | 0.08 | 32.67 | 16.72 | 15.95 |
| | 0.12 | 38.85 | 15.97 | 22.88 |
| | 0.16 | 52.87 | 16.03 | 36.84 |
| | 0.2 | 159.7 | 16.04 | 143.66 |
| **1.5** | 0.04 | 23.21 | 16.94 | 6.27 |
| | 0.08 | 29.52 | 16.28 | 13.24 |
| | 0.12 | 33.83 | 16 | 17.83 |
| | 0.16 | 41.73 | 15.94 | 25.79 |
| | 0.2 | 62.26 | 15.94 | 46.32 |
| **1.71** | 0.04 | 19.36 | 17.99 | 1.37 |
| | 0.08 | 20.32 | 15.95 | 4.37 |
| | 0.12 | 26.89 | 15.94 | 10.95 |
| | 0.16 | 32.52 | 15.94 | 16.58 |
| | 0.2 | 37.97 | 15.94 | 22.03 |

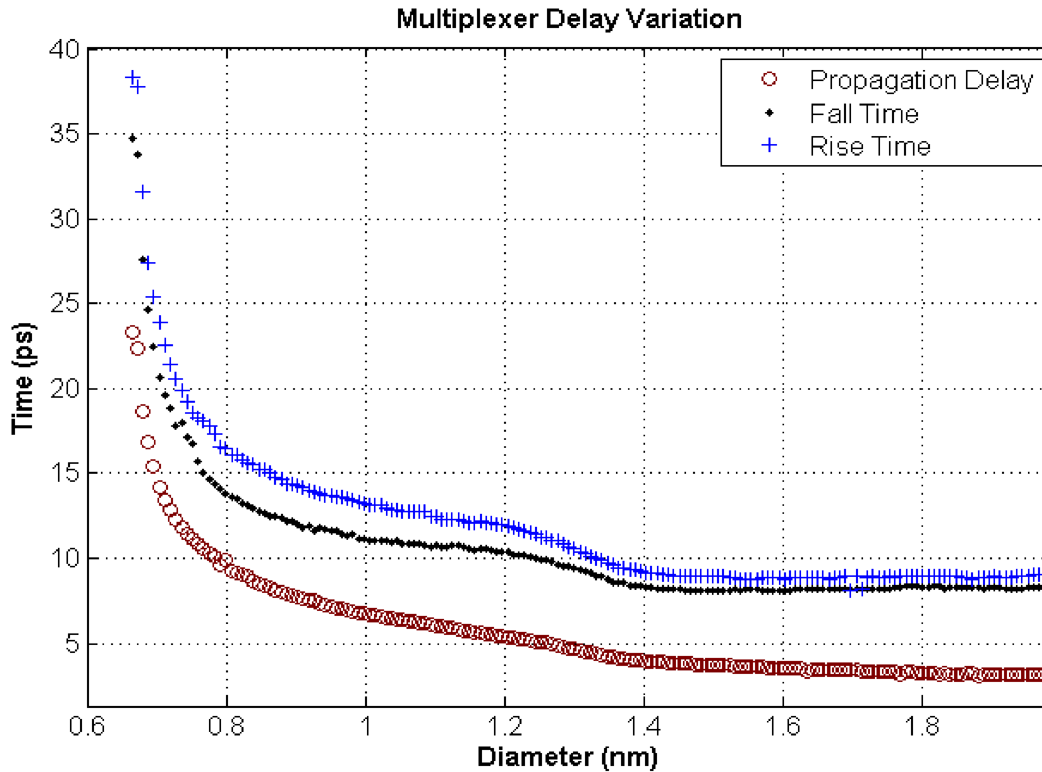


**Figure 4.4: Multiplexer Timing Behaviour based on CNT Diameter**

Fig. 4.4 shows the results of the parametric simulation of the multiplexers. In the parametric simulation, CNT diameter is swept from 0.6nm to 2nm and the various delay metrics are measured. Two main points can be derived from fig. 4.4. The first point of observation is that propagation delay, rise time and fall time all rise sharply as diameter is reduced below ~0.85nm. On the other hand as CNT diameter increases past the 0.85nm mark, time delay is steadily reduced.

As CNT diameter increases, energy band gap is decreased thereby allowing more charge carriers to contribute to conduction and more on-current to flow as explained in Chapter 1; increasing on current through the CNTs means that delay is steadily reduced until reaching equilibrium at diameters larger than ~1.6nm for a fixed voltage of 0.9V.

The second point of observation is that fall time and rise time are very similar, confirming that utilizing structures with an equal number of CNFETs in series in their pull-up and pull-down network would yield to similar rise and fall times due the equal mobility of electrons and holes in CNTs.

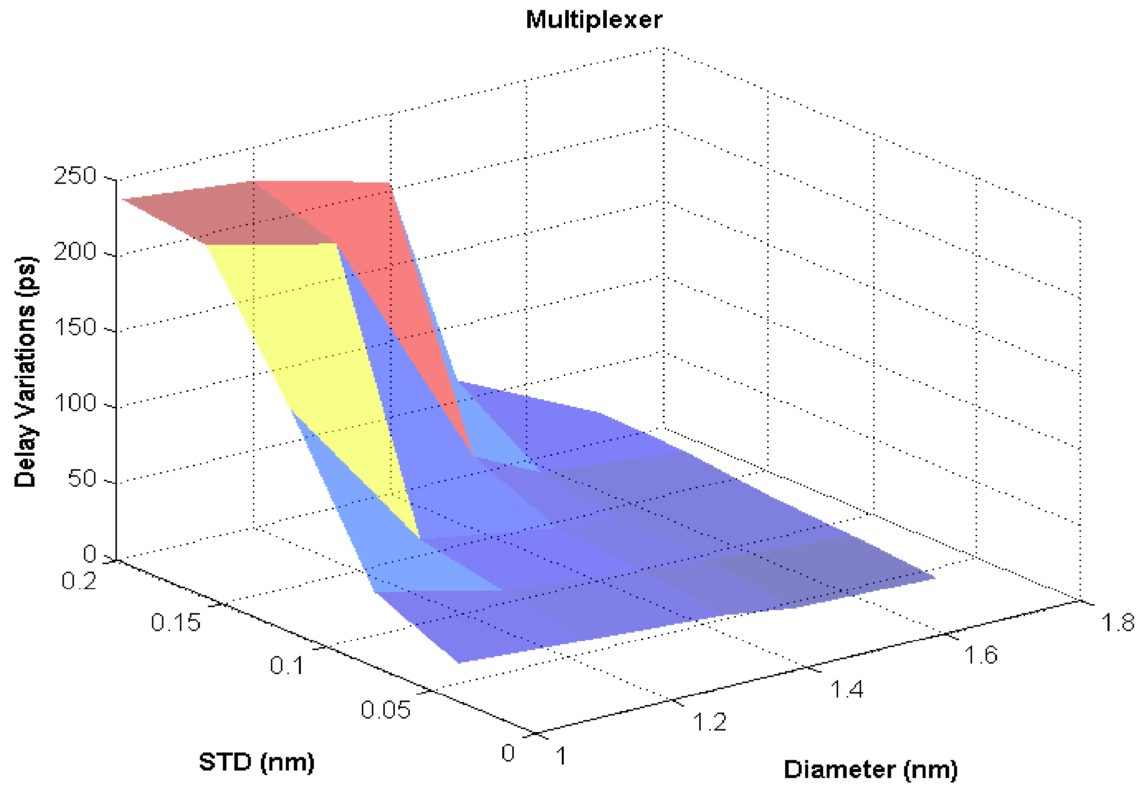


**Figure 4.5 Multiplexer Delay variation based on CNT Diameter Mean & STD**

Fig. 4.5 is obtained from the Monte Carlo simulation results of 10000 multiplexers. It shows the multiplexers worst case delay variation, defined as the difference in maximum rise/fall time and minimum rise/fall time, plotted against CNT mean diameter and STD in CNT diameter. The variation in multiplexer delay peaks when the small mean CNT diameter is combined with larger STDs of CNT diameter.

**Table 4.3: Multiplexers Power Consumption**

| Mean Diameter(nm) | Diameter STD (nm) | Mean Power(nW) | Min. Power (nW) | Max. Power(nW) | ΔP (nW) | PDP ($*10^{-20}$ J) | PDP Variation ($*10^{-20}$ J) |
|---|---|---|---|---|---|---|---|
| **1.01** | 0.04 | 5.14 | 4.59 | 6.06 | 1.46 | 97.25 | 17.46 |
| | 0.08 | 5.15 | 3.99 | 6.17 | 2.19 | 100.06 | 83.83 |
| | 0.12 | 5.15 | 4.505 | 6.05 | 1.55 | 105.32 | 193.18 |
| | 0.16 | 5.15 | 4.42 | 6.51 | 2.09 | 114.28 | 296.61 |
| | 0.2 | 5.15 | 4.37 | 7.78 | 3.41 | 122.11 | 481.94 |
| **1.2** | 0.04 | 5.65 | 5.87 | 5.54 | 0.33 | 79.67 | 2.78 |
| | 0.08 | 5.66 | 5.48 | 6.27 | 0.78 | 79.41 | 11.72 |
| | 0.12 | 5.67 | 3.95 | 6.98 | 3.03 | 80.12 | 98.32 |
| | 0.16 | 5.69 | 5.09 | 8.34 | 3.26 | 82.56 | 413.56 |
| | 0.2 | 5.71 | 4.13 | 8.23 | 4.09 | 87.25 | 584.22 |
| **1.4** | 0.04 | 6.17 | 5.95 | 6.83 | 0.88 | 58.92 | 4.083 |
| | 0.08 | 6.18 | 8.82 | 7.33 | 1.51 | 60.69 | 14.48 |
| | 0.12 | 6.2 | 5.33 | 8.81 | 3.48 | 62.62 | 49.9 |
| | 0.16 | 6.23 | 5.66 | 9.16 | 3.5 | 65.17 | 80.89 |
| | 0.2 | 6.28 | 5.45 | 9.14 | 3.69 | 68.14 | 328.37 |
| **1.5** | 0.04 | 6.46 | 6.18 | 7.03 | 0.85 | 55.36 | 2.71 |
| | 0.08 | 6.48 | 6.01 | 8.16 | 2.15 | 56.7 | 16.58 |
| | 0.12 | 6.51 | 5.47 | 8.75 | 3.27 | 57.94 | 35.74 |
| | 0.16 | 6.56 | 5.86 | 9.2 | 3.35 | 59.83 | 56.75 |
| | 0.2 | 6.64 | 5.7 | 9.21 | 3.52 | 62.42 | 114.44 |
| **1.71** | 0.04 | 7.31 | 5.14 | 8.48 | 3.34 | 53.87 | 5.78 |
| | 0.08 | 7.37 | 5.28 | 9.26 | 3.97 | 54.17 | 11.39 |
| | 0.12 | 7.41 | 6.27 | 11.16 | 4.89 | 54.91 | 30.32 |
| | 0.16 | 7.4 | 6.11 | 9.32 | 3.21 | 55.72 | 29.76 |
| | 0.2 | 7.36 | 5.64 | 9.32 | 3.68 | 56.97 | 49.9 |

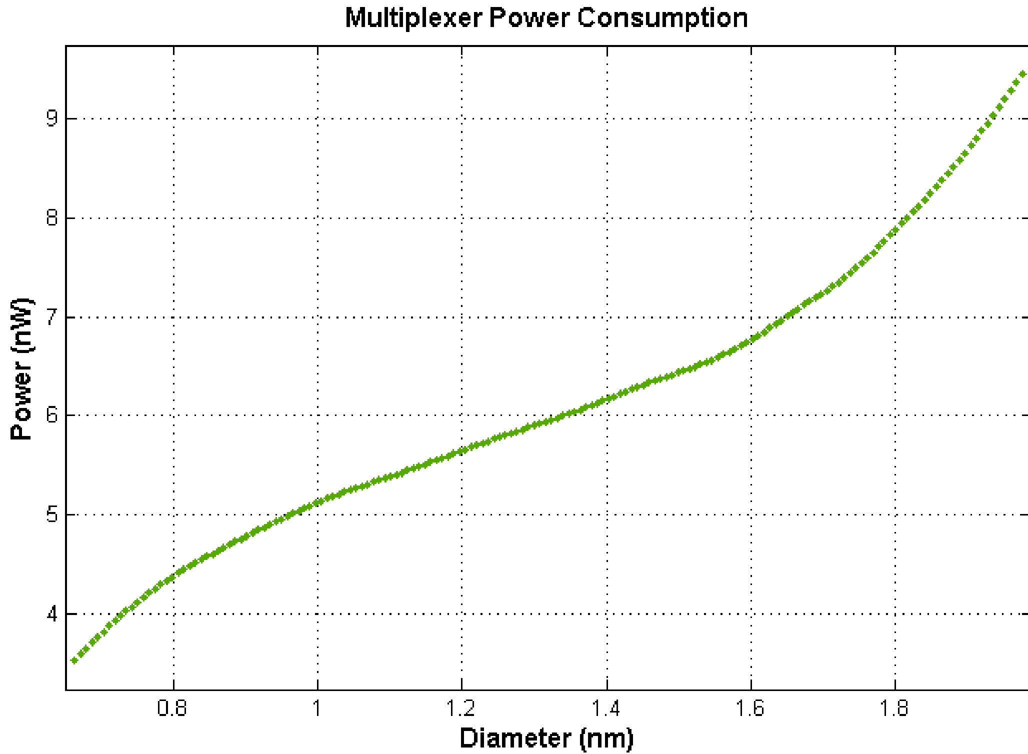


**Figure 4.6: Multiplexer Power Consumption**

Table 4.3 shows the results of Monte Carlo simulation of the multiplexers for power consumption parameters. Mean power consumption is not greatly affected by CNT diameter STD within the same mean diameter group. As mean CNT diameter is increased, a slight increase in power consumption is also observed.

Fig. 4.6 shows the results of a parametric simulation of the multiplexers. Again, CNT diameter is swept from a minimum of 0.6nm to a maximum of 2nm. The rise in power consumption with increasing CNT diameter is due to the decreased energy band gap. As CNT diameter increases, energy band gap is reduced thereby requiring less energy for charge carriers to flow and allowing for greater current. This increased current in turn causes power consumption to rise. The figure shows a sharper rise in power consumption as CNT diameter is increased beyond 1.6nm, the same effect was also observed for the other logic gates studied in chapter 3.

Variation in power consumption however, decreases with increasing CNT diameter according to table 4.3. Table 4.4 shows percentage variation in power consumption for the multiplexers.

**Table 4.4: Percentage Power Consumption Variation for Multiplexers**

| Mean Diameter (nm) | % Variation (STD = 0.04nm) | %Variation (STD = 0.2nm) |
|---|---|---|
| 1.01 | 28% | 66% |
| 1.2 | 6% | 72% |
| 1.4 | 14% | 59% |
| 1.5 | 13% | 53% |
| 1.71 | 46% | 50% |

### *4.1.1 Power-Delay Product*

Table 4.3 lists values for power-delay product representing the energy efficiency of the multiplexer. As discussed in chapter 3, PDP is the product of power and propagation delay of the multiplexers. PDP variation in this work is defined as the product of $\Delta P$ and $\Delta T_d$. PDP values show modest changes as CNT diameter STD is changed within a mean diameter group. For small CNT diameters PDP values are larger in comparison with values for larger CNT mean diameters. Variation in PDP is extreme for smaller CNT mean diameters and is greatly dependent on diameter STD. For larger CNT diameters of 1.4nm, 1.5nm and 1.71nm PDP values show little difference and are generally similar, further underlining the trade-off between time delay and power consumption as larger CNT diameters mean smaller delays but at the same time they lead to greater power consumption. This leads to the conclusion that to achieve better PDP values, diameters larger than 1.2nm are required. This result is in agreement with the choice of diameter put forward at the end of chapter 3 of this work.

## 4.2. XOR Gate

In this section the simulation results of CNFET-based XOR gates are studied. The structure of the implemented gate is shown in fig. 4.7. This structure is commonly used in standard cell design. The pull up network consists of 4 p-type CNFETs and the pull-down network has 4 n-type CNFETs.

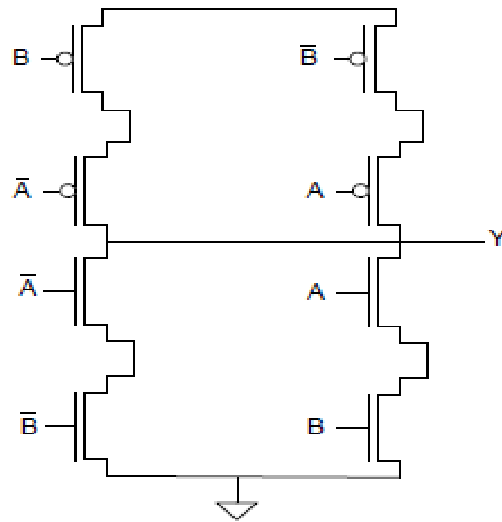


**Figure 4.7: The implemented XOR gate**

Table 4.5 shows the delay behaviour of the simulated XOR gates based both on parametric and Monte Carlo simulation results. Monte Carlo simulations were done with 10,000 iterations for each mean CNT diameter considered.

Table 4.5: XOR Gates Delay Behaviour

| Mean Diameter(nm) | Diameter STD (nm) | Mean Delay $T_d$ (ps) | Min. Delay (ps) | Max. Delay (ps) | $\Delta T_d$ (ps) |
|---|---|---|---|---|---|
| **1.01** | 0.04 | 19 | 14.4 | 26.72 | 12.32 |
| | 0.08 | 19.46 | 9.82 | 47.01 | 37.19 |
| | 0.12 | 20.43 | 8.26 | 132.1 | 123.84 |
| | 0.16 | 22.12 | 7.08 | 160.3 | 153.22 |
| | 0.2 | 23.46 | 6.46 | 154.1 | 147.64 |
| **1.2** | 0.04 | 14.015 | 9.65 | 17.82 | 8.17 |
| | 0.08 | 14 | 8.19 | 23.86 | 15.67 |
| | 0.12 | 14.12 | 7.03 | 37.12 | 30.09 |
| | 0.16 | 14.49 | 6.44 | 138.5 | 132.06 |
| | 0.2 | 15.25 | 6.46 | 157.1 | 150.64 |
| **1.4** | 0.04 | 9.54 | 7.81 | 12.95 | 5.14 |
| | 0.08 | 9.8 | 6.94 | 16.2 | 9.26 |
| | 0.12 | 10.08 | 6.4 | 21.53 | 15.13 |
| | 0.16 | 10.38 | 6.31 | 31.65 | 25.34 |
| | 0.2 | 10.74 | 6.32 | 99.28 | 92.96 |
| **1.5** | 0.04 | 8.7 | 7.49 | 10.47 | 2.98 |
| | 0.08 | 8.73 | 6.55 | 13.85 | 7.3 |
| | 0.12 | 8.88 | 6.43 | 17.35 | 10.92 |
| | 0.16 | 9.1 | 6.32 | 23.34 | 17.02 |
| | 0.2 | 9.39 | 6.32 | 36.7 | 30.38 |
| **1.71** | 0.04 | 7.35 | 6.49 | 8.21 | 1.72 |
| | 0.08 | 7.34 | 6.33 | 9.2 | 2.87 |
| | 0.12 | 7.39 | 6.21 | 12.51 | 6.3 |
| | 0.16 | 7.52 | 6.31 | 15.6 | 6..29 |
| | 0.2 | 7.72 | 6.31 | 20.25 | 13.94 |

Table 4.6: XOR Gates Worst Case Rise/Fall Times Variation

| Mean Diameter(nm) | Diameter STD (nm) | Max Rise/Fall (ps) | Min. Rise/Fall(ps) | $\Delta T_d$ (ps) |
|---|---|---|---|---|
| 1.01 | 0.04 | 45.76 | 27.78 | 17.98 |
| | 0.08 | 83.1 | 19.74 | 63.36 |
| | 0.12 | 216.8 | 17.14 | 199.66 |
| | 0.16 | 251.8 | 16.77 | 235.03 |
| | 0.2 | 243.2 | 16.04 | 227.16 |
| 1.2 | 0.04 | 34.3 | 19.29 | 15.01 |
| | 0.08 | 41.79 | 17.29 | 24.5 |
| | 0.12 | 64.29 | 16.58 | 47.71 |
| | 0.16 | 224 | 16.01 | 208 |
| | 0.2 | 249.4 | 16.04 | 233.86 |
| 1.4 | 0.04 | 27.28 | 17.23 | 10.05 |
| | 0.08 | 32.37 | 16.7 | 15.67 |
| | 0.12 | 38.41 | 15.97 | 22.44 |
| | 0.16 | 52.21 | 15.93 | 36.28 |
| | 0.2 | 157.3 | 15.93 | 141.37 |
| 1.5 | 0.04 | 22.19 | 16.73 | 5.46 |
| | 0.08 | 29.2 | 16.27 | 12.93 |
| | 0.12 | 33.89 | 16 | 17.9 |
| | 0.16 | 41.98 | 15.94 | 26.04 |
| | 0.2 | 61.74 | 15.93 | 45.81 |
| 1.71 | 0.04 | 19.3 | 16.07 | 3.23 |
| | 0.08 | 20.12 | 15.93 | 4.19 |
| | 0.12 | 26.33 | 15.92 | 10.41 |
| | 0.16 | 31.98 | 15.92 | 16.06 |
| | 0.2 | 37.57 | 15.9 | 21.67 |

Propagation delay and its variation for the gates are shown in table 4.5. Consistent with the results obtained for all the CNFET-based structures considered so far, larger CNT diameters offer the best case choice for minimisation of delay. A mean diameter of 1.71nm and a STD of 0.04nm give a variation of 1.72ps compared to a variation of 12.32ps for a mean diameter of 1.01nm.

The situation is the same for worst case rise and fall time variation. Again larger CNT mean diameters and smaller STDs offer the fastest and most reliable operations in terms of delay as can be observed from table 4.6 and fig. 4.8.

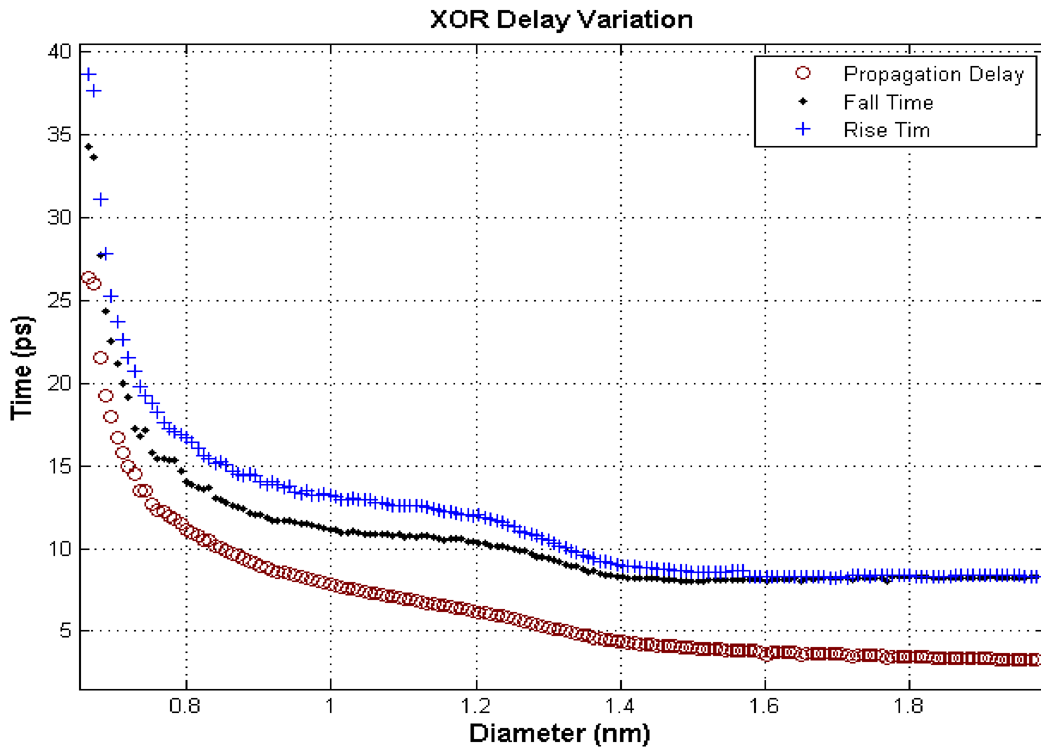


**Figure 4.8: XOR Timing Behaviour according to CNT Diameter**

Fig. 4.8 highlights the achievement of similar fall and rise times that were targeted at the start of this section. Due to the equal number of transistors in the pull-up and pull-down networks, fall time and rise time are now very close to each other. It is observed from the figure that delay rises sharply below the same CNT diameter of ≈ 0.85nm as observed for previously considered structures.

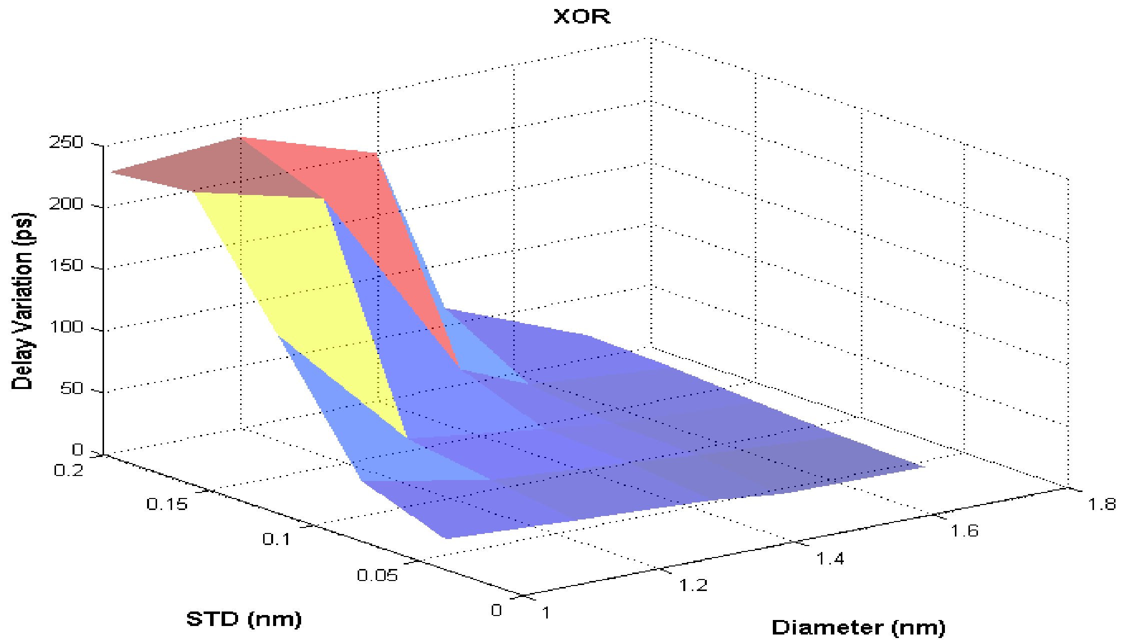


**Figure 4.9: XOR Delay Variation based on CNT Diameter Mean & STD**

Fig. 4.9 plots the results of Monte Carlo simulations for 10,000 XOR gates with varying CNT mean diameter and STD. As STD increases, delay variation becomes larger. The variation in delay becomes quite significant for bigger STDs and smaller CNT mean diameters.

**Table 4.7 XOR Gates Power Consumption**

| Mean Diameter(nm) | Diameter STD (nm) | Mean Power(nW) | Min. Power (nW) | Max. Power(nW) | ΔP (nW) | PDP ($*10^{-20}$ J) | PDP Variation ($*10^{-20}$ J) |
|---|---|---|---|---|---|---|---|
| **1.01** | 0.04 | 9.71 | 8.5 | 11 | 2.51 | 184.49 | 30.92 |
| | 0.08 | 9.7 | 8.38 | 11.24 | 2.86 | 188.76 | 106.36 |
| | 0.12 | 9.7 | 8.65 | 11.17 | 2.53 | 198.17 | 313.32 |
| | 0.16 | 9.69 | 8.6 | 11.2 | 2.6 | 214.34 | 398.37 |
| | 0.2 | 9.71 | 8.79 | 13.38 | 4.59 | 227.8 | 677.67 |
| **1.2** | 0.04 | 10.7 | 9.55 | 11.69 | 2.14 | 149.96 | 17.48 |
| | 0.08 | 10.7 | 9.86 | 11.6 | 1.74 | 149.8 | 27.27 |
| | 0.12 | 10.72 | 9.9 | 12.78 | 2.88 | 151.37 | 86.66 |
| | 0.16 | 10.74 | 9.75 | 13.99 | 4.24 | 155.62 | 559.93 |
| | 0.2 | 10.77 | 9.74 | 14.73 | 4.99 | 164.24 | 751.69 |
| **1.4** | 0.04 | 11.66 | 11.32 | 12.27 | 0.95 | 111.24 | 4.88 |
| | 0.08 | 11.67 | 10.89 | 13.48 | 2.59 | 114.37 | 23.98 |
| | 0.12 | 11.7 | 10.6 | 15.26 | 4.66 | 117.936 | 70.51 |
| | 0.16 | 11.74 | 10.53 | 15.55 | 5.02 | 121.86 | 127.21 |
| | 0.2 | 11.8 | 10.47 | 15.54 | 5.07 | 126.73 | 471.31 |
| **1.5** | 0.04 | 12.2 | 11.71 | 13.09 | 1.38 | 106.14 | 4.11 |
| | 0.08 | 12.2 | 11.41 | 14.34 | 2.93 | 106.51 | 21.39 |
| | 0.12 | 12.24 | 11.22 | 15.22 | 4 | 108.69 | 43.68 |
| | 0.16 | 12.28 | 11.1 | 15.7 | 4.6 | 111.75 | 78.29 |
| | 0.2 | 12.33 | 10.88 | 15.71 | 4.83 | 115.78 | 146.74 |
| **1.71** | 0.04 | 13.64 | 11.94 | 15.15 | 3.21 | 100.25 | 5.52 |
| | 0.08 | 13.6 | 11.94 | 15.85 | 3.91 | 99.82 | 11.22 |
| | 0.12 | 13.66 | 11.89 | 15.92 | 4.03 | 100.95 | 25.39 |
| | 0.16 | 13.62 | 11.65 | 15.92 | 4.27 | 102.42 | 26.86 |
| | 0.2 | 13.55 | 11.5 | 15.92 | 4.42 | 104.61 | 61.61 |

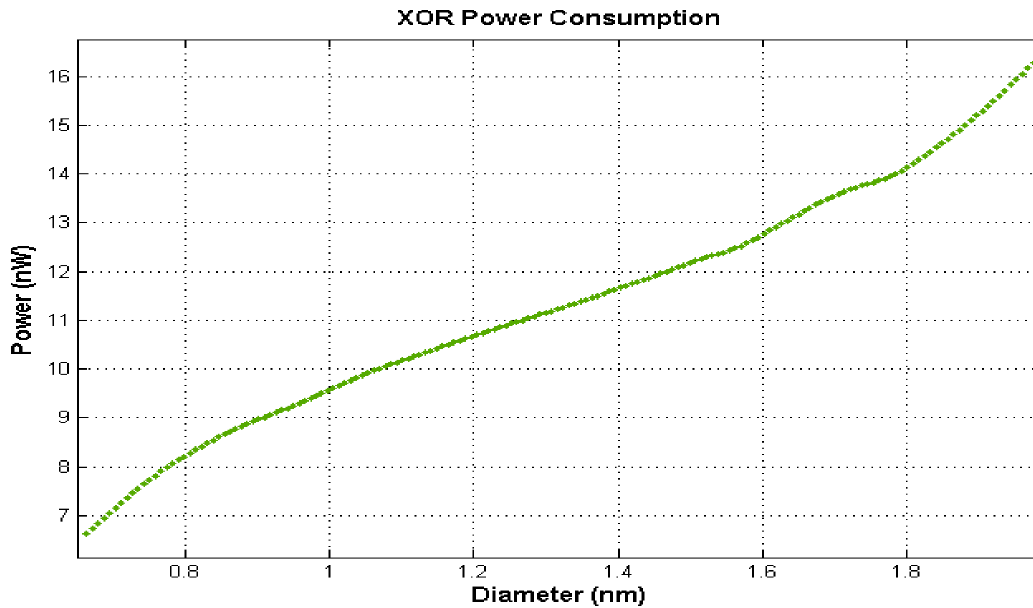


**Figure 4.10: XOR Gates Power Consumption**

Table 4.7 and fig. 4.10 show the rise in power consumption of the XOR gates with increasing CNT diameter due to the decreased energy band gap. The sharper rise in power consumption beyond a CNT mean diameter of 1.6nm is also observed for the XOR gates. Variation in power consumption however, decreases with increasing CNT diameter according to table 4.7. Results reveal that for a design requiring minimum power variation, the largest diameter considered in the simulations (1.71nm) would be the ideal choice as this introduces the least variation in total power consumption. PDP and PDP variation behaviour for XOR gates is similar to that of multiplexers discussed before, section 4.1.1. Table 4.8 shows percentage variation in power consumption.

**Table 4.8 Percentage Power Consumption Variation for XOR Gates**

| Mean Diameter (nm) | % Variation (STD = 0.04nm) | %Variation (STD = 0.2nm) |
|---|---|---|
| 1.01 | 26% | 47% |
| 1.2 | 20% | 46% |
| 1.4 | 8% | 43% |
| 1.5 | 11% | 39% |
| 1.71 | 23% | 33% |

## 4.3 Modelling of Delay

Response Surface Methodology (RSM) regression technique has been applied to model the behaviour of the multiplexers and XOR gates considered in this chapter. This technique has been discussed in detail in Chapter 3, section 3.4.

*4.3.1 Mean Propagation Delay Model*

For the purpose of predicting the mean worst-case propagation delay of the multiplexers with any CNT diameter mean and STD, a second-order model is developed given by:

$$Log\left(Pd_{\mu}\right) = \beta_0 + \beta_1 Log\left(D_{\mu}\right) + \beta_2 D_{\sigma} + \beta_{12} D_{\sigma} Log\left(D_{\mu}\right) + \beta_{11}\left(Log\left(D_{\mu}\right)\right)^2 + \beta_{22} {D_{\sigma}}^2$$

Where $Pd_{\mu}$ is mean of worst-case propagation delay; $D_{\mu}$ is mean CNT diameter and $D_{\sigma}$ is CNT diameter STD. By performing multiple linear regressions the coefficients are found as presented in table 4.9.

The adjusted $R$-squared ($R^2_{adj}$) of this regression is 0.9913. This value suggests that this is a reliable and accurate model for the prediction of mean worst case propagation delay of the multiplexers based on the MC simulation results as 99.13% of the samples can be explained reliably by the model.

**Table 4.9 Coefficients for mean propagation delay predictive model and $R^2_{adj}$ values**

| | $\boldsymbol{\beta_0}$ | $\boldsymbol{\beta_1}$ | $\boldsymbol{\beta_2}$ | $\boldsymbol{\beta_{12}}$ | $\boldsymbol{\beta_{11}}$ | $\boldsymbol{\beta_{22}}$ | $\boldsymbol{R^2_{adj}}$ |
|---|---|---|---|---|---|---|---|
| **MUX** | 2.07 | -1.94 | 0.36 | -1.41 | 0.88 | 2.91 | 0.9913 |
| **XOR** | 2.07 | -1.94 | 0.33 | -1.39 | 0.87 | 3 | 0.99175 |

*4.3.2 Propagation Delay STD Model*

Based on the Monte Carlo simulation results, a statistical model can also be developed for prediction of STD in worst case propagation delay using the RSM regression model. CNT diameter STD has a considerable effect on the delay STD of both multiplexers and XOR gates; hence, to achieve good regression results, the log transformation is used:

$$Log\,(Pd_\sigma) = \gamma_0 + \gamma_1 Log(D_\mu) + \gamma_2 \log(D_\sigma) + \gamma_{12} Log(D_\sigma) Log(D_\mu) + \gamma_{11}\left(Log(D_\mu)\right)^2 + \gamma_{22}(Log(D_\sigma))^2$$

Where $Pd_\sigma$ is the STD of worst case propagation delay.

The coefficients of the model are presented in table 4.10.

**Table 4.10 Coefficients for STD in propagation delay and $R^2_{adj}$ values**

| | $\gamma_0$ | $\gamma_1$ | $\gamma_2$ | $\gamma_{12}$ | $\gamma_{11}$ | $\gamma_{22}$ | $R^2_{adj}$ |
|---|---|---|---|---|---|---|---|
| **MUX** | 5.42 | -3.84 | 2.55 | -0.71 | -3.66 | 0.21 | 0.98641 |
| **XOR** | 5.61 | -3.84 | 2.75 | -0.59 | -3.98 | 0.26 | 0.98645 |

## 4.3 Conclusion

The structures studied in this section show similar rise and fall times suggesting that multiplexers and XOR gates can be advantageous as building blocks of CNFET-based logic structures. The propagation delay of the gates increases with reducing diameter and timing variation is also greater in gates composed of smaller diameter CNTs. Such structures can be used with larger diameter CNTs in the design of CNFET-based logic for the purpose of reliability and practicality. Results obtained in this section are homogenous with those obtained for basic logic gates studied in the previous section and show better PDP values and improvement in PDP variation for larger CNT mean diameters.

# Chapter 5 CNT Based Static Random Access Memory in the Presence of CNT Diameter Variations[2]

In the previous chapters, CNT-based logic structures were simulated so that the performance of various logic gates could be analysed in the presence of CNT diameter variations and predictive models could be developed to facilitate the design process of these logic gates.

In this chapter, the study is extended to memory and a CNFET-based Static Random Access Memory (SRAM) is designed and implemented. Parametric and Monte Carlo simulations are then carried out in the presence of CNT diameter variations to examine the performance and stability of the implemented SRAM cell. Performance parameters such as read/write delays, Static Noise Margin (SNM), Write Margin (WM) and standby leakage power are studied.

Based on the simulation results, an ideal threshold for CNT diameter selection is put forward and a mathematical model for the prediction of the various SRAM performance parameters are developed.

[2] Parts of this work are taken from the paper "Effects of CNT Diameter Variability on a CNFET-Based SRAM", by Hamed Shahidipour et. Al, Refer to Appendix A.

## 5.1 SRAM

Random Access Memory (RAM) is a type of volatile memory which data only as long as power is applied. Static Random Access Memory (SRAM) uses feedback to maintain its state and can be thought of as two cross-coupled inverters. During start-up, a small voltage difference on one of the floating inverters outputs is driven positively within the loop to force the SRAM to go to a 1 or a 0.

A memory array contains $2^n$ words each containing $2^m$ bits with each bit stored within a memory cell; the simplest form of this is shown in fig. 5.1. The layout diagram of the SRAM is shown in fig. 5.2. The address is utilized by the row decoder for activating one of the rows by asserting the wordline. The cells on this wordline drive the bitlines during a read operation.

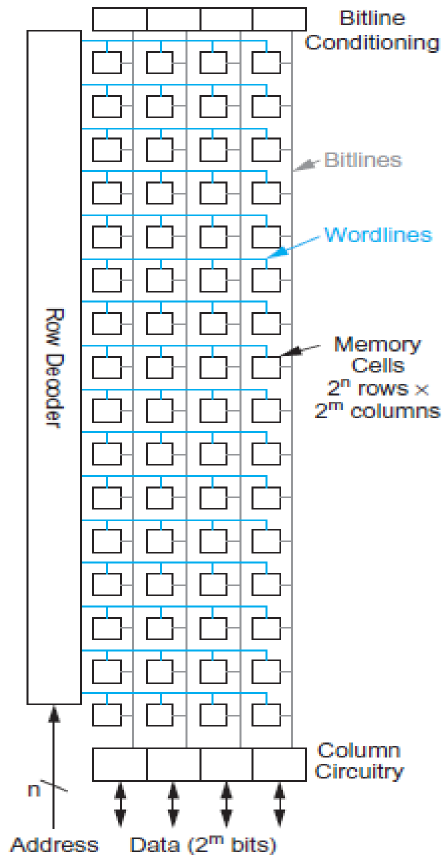


**Figure 5.1: Simple memory array architecture [62]**

SRAM is faster and easier to use in comparison with Dynamic RAM (DRAM). SRAM is the most commonly used form of on-chip memory. The 6T SRAM is commonly used and is superior

to other SRAM structures due to its superior robustness, low power operation and short access time [107].

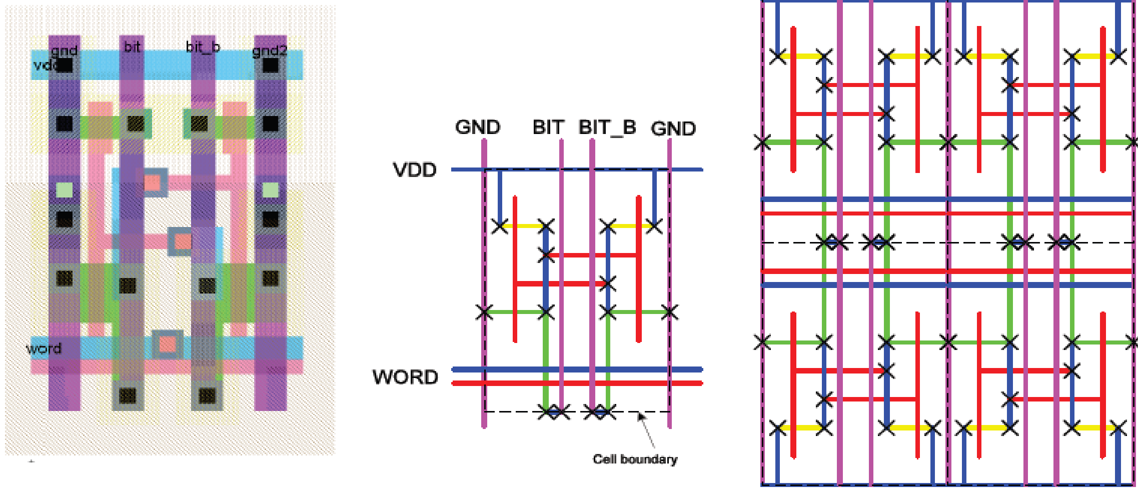


**Figure5.2: SRAM Layout [62]**

The cell contains a pair of cross-coupled inverters and an access transistor for each bitline. True and complementary versions of the data are stored on the cross-coupled inverters. Disturbances caused by leakage or noise are corrected by the positive feedback. The cell is activated when the wordline (WL) is raised and is read or written through the bitlines (BL and BL-B). BL and BL-B are used for writing the desired value and its complement respectively. Write operation takes place by driving the value to be written and its complement onto the bitlines, followed by raising WL.

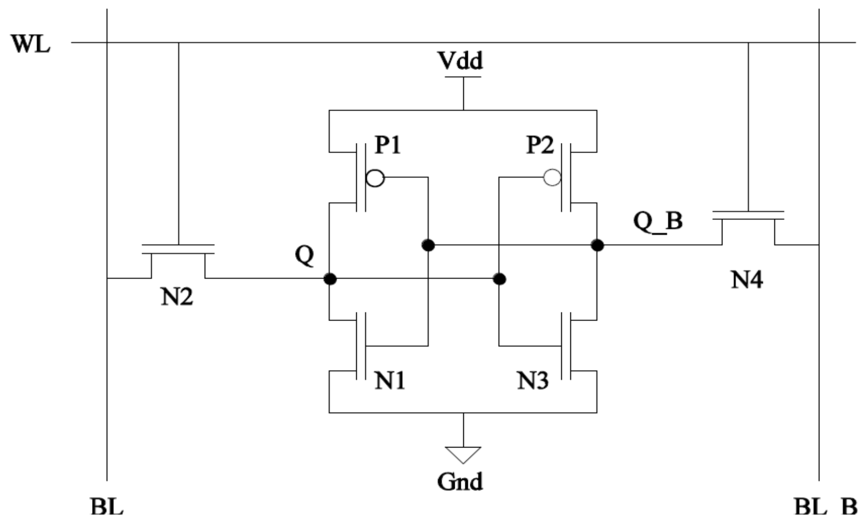


**Figure 5.3: Schematic of 6T SRAM**

## 5.2 Simulation Methodology & Performance Measurement

Most of the simulation methodology follows that used for logic gates in the previous chapters. A MOSFET-like CNFET structure is considered utilising SWCNTs. Three CNTs per CNFET have been used in the simulations. The doping level of the source/drain extension regions is taken as 1%. Sample HSPICE codes used for measurements are given in Appendix B.

The main challenges in SRAM design are minimizing size and ensuring that the transistors involved in holding the state of the cell are weak enough to be overpowered during a write operation and strong enough not to be disturbed during a read operation. Also to achieve good layout density, all the transistors in the SRAM cell must be small. For this reason the weakest transistors in the design (P1 and P2) have only one CNT under the gate. Adding further CNTs requires a wider gate area, hence increasing the area cost of the entire SRAM cell. The physical metal gate width of a CNFET is assumed to be 48nm. This width affects the parasitic capacitance but the on-current depends on the actual "effective" gate width which is determined by the number of CNTs under the gate and the spacing between them. A power supply voltage of 0.9V is used in accordance with the ITRS roadmap for 32nm technology [3]. 10,000 samples were taken and MC iterations were run for each $D_{\mu}$ and $D_{\delta}$ considered. All simulations are run for the 32nm technology.

Cell stability is important as it determines the soft error rate - the rate at which corruptions of the data stored in the memory cell occur - and the sensitivity of the memory to process tolerances and operating conditions. An important measure of the stability of SRAM cells is the Static Noise Margin (SNM), discussed in sections 5.2.5 and 5.3.2. Further, an SRAM cell needs to be sufficiently stable during the read operation but at the same time it needs to be easy to write to during write operation as well. Write margin is a measure for the writeability of the SRAM (discussed further in sections 5.2.6 and 5.3.3). Read and write delays are a measure of the speed of the memory cell and hence important performance parameters for the SRAM.

For read stability N1 must be stronger than N2 (fig. 5.3) [62]. Also, to satisfy writeability P2 must be weaker than N4 [62]. To have higher drive current and hence "stronger" CNFETs more CNTs are put under the gate of the transistor. Hence, N1 & N3 employ 3 CNTs under the gate; N2 & N4 have 2 CNTs and P1 & P2 employ 1 CNT under the gate. Centre to centre CNT spacing ($S$) is 20

nanometres (nm) since at this spacing the charge screening effect of CNTs and its effect on drive current and SRAM performance are negligible [69].

*5.2.1 Read Operation*

Read operation is achieved by precharging the two bit lines high and then allowing them to float. When WL is raised, BL or BL_B pulls down indicating the data value. Fig. 5.4 shows the waveforms for read operation of the 6T SRAM as 0 is read onto BL. When WL is raised, BL should be pulled down through N1 and N2. As BL is being pulled down node Q tends to rise (this is seen in fig. 5.4). Q is held low by N1 but raised by current flowing in from N2. N1 must be stronger than N2 to preserve the state of Q. To satisfy read stability the transistors should be ratioed so that node Q remains below the switching threshold of the P2/N3 inverter. This ratio is typically > 1.28 for CMOS.

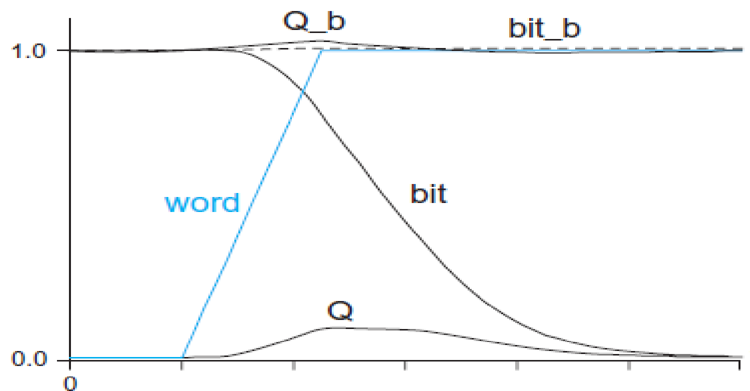


**Figure 5.4: Read Operation for 6T SRAM [62]**

*5.2.2 Read operation measurements*

Two capacitors C1 and C2 and two PCNFETs are used to precharge BL and BL_B to 1 for the read operation (fig 5.5). C1 and C2 are charged when the signal precharge is high (fig. 5.5). Both C1 and C2 are taken to be 100fF [79]. Fan-in inverters are also used for WL and precharge. Q and Q_B are initialized to 1 and 0 respectively. Read delay is defined as the time required for developing a 100mV differential voltage between BL and BL_B after WL (fig. 5.5) reaches 50% of its final swing [109]. As the worst-case stability condition for the SRAM configuration occurs when the cell is accessed for read operation, read SNM is the focus in this work.

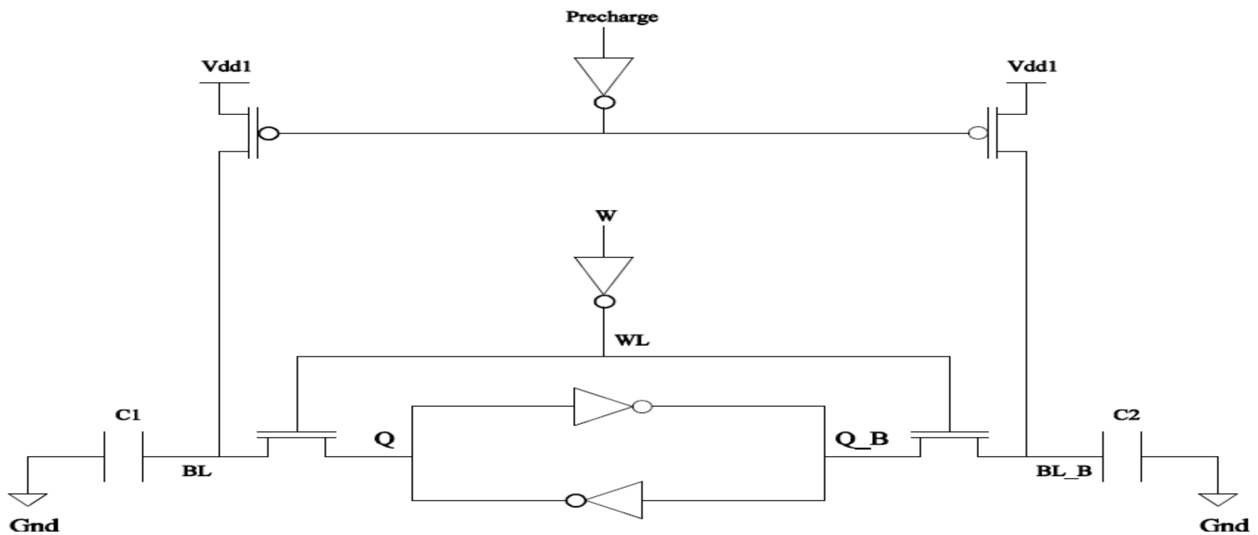


**Figure 5.5: Read Operation Circuitry**

### *5.2.3 Write Operation*

Fig. 5.6 shows the write operation of the SRAM as a 1 is written to the cell. BL is precharged high and left floating. The only way the cell can be written to is by forcing Q_b low through N4 as Q cannot be forced high through BL on account of N1 being chosen stronger than N2 to satisfy read stability. As P2 will try to pull Q_b high, P2 should be chosen weaker than N4 so that Q_b can be pulled sufficiently down. This constraint is called writeability. As Q_b falls low, N1 is turned OFF and P1 is turned ON, hence pulling Q high.

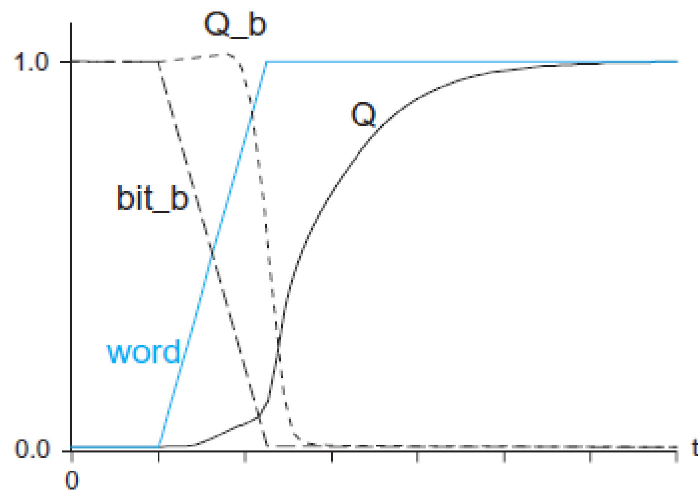


**Figure 5.6: Write Operation for 6T SRAM [62]**

### *5.2.4 Write operation measurements*

To investigate the effect of diameter variation on SRAM performance, a simplified circuit, bypassing the peripheral circuitry usually involved in write operation, is utilized by imposing the voltage on the bitlines (fig. 5.7). Fan-in inverters are put in front of BL, BL_B and WL to introduce skew in the ideal input signal. These inverters all have 3 CNTs under the gate. The SRAM cell is initialized to store a 1 by setting Q to 1 and Q-B to 0.

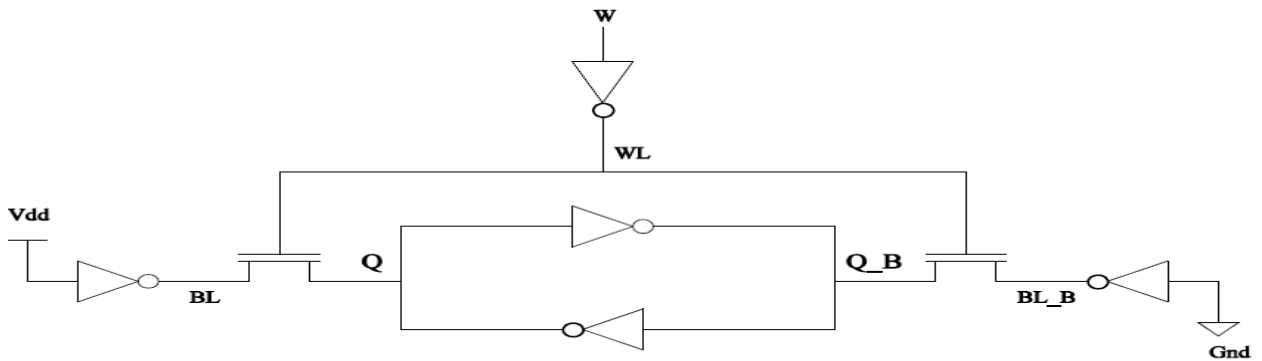


**Figure 5.7: Write Operation Circuitry**

Write delay [60] is defined as the time from the 50% activation of WL to the time the internal nodes Q and Q_B (fig. 5.7) reach 50% of their final value [109].

### *5.2.5 SNM measurement*

There are various sources of disturbances such as alpha particle emissions from chip packaging materials and cosmic rays that can affect the normal operation of SRAM cells temporally leading to data errors. The more disturbances an SRAM cell can tolerate, the more stable it is. With technology scaling and reduced power supply voltages SRAMs become more susceptible to static noise i.e. external noise or offsets and mismatches due to process variation and changes in operating conditions.

Various methods exist to define the stability of the SRAM cell. SNM is the most important of these metrics [111]. The SNM is defined as the maximum value of DC noise voltage tolerated without changing the stored bit [111]. Usually SNM can be obtained graphically by obtaining the voltage

transfer characteristics (VTC) of the cross-coupled inverters in the SRAM cell. As the inverters used in this work are identical, the VTC is mirrored across the imaginary line passing through the origin at 45 degrees from the horizontal (fig 5.8). SNM is determined by the length of the side of the largest square that can be drawn between the curves.

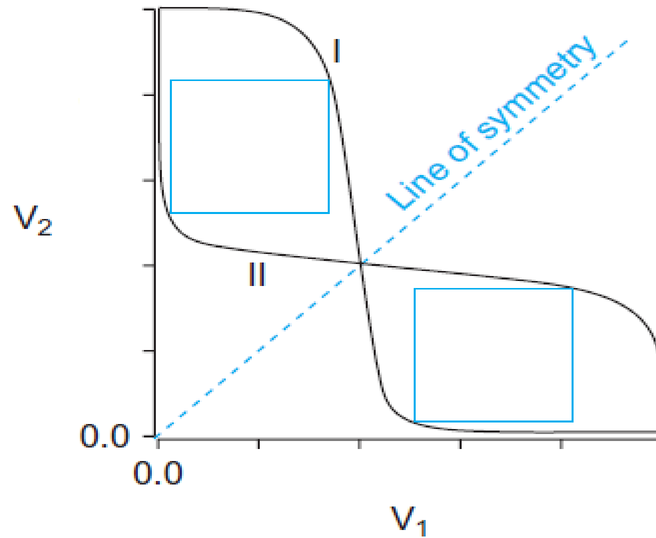


**Figure 5.8: Butterfly Diagram indicating SNM [62]**

As the SRAM cell is most vulnerable during read operation, SNM is measured under the read situation. As 10,000 Monte Carlo iterations are taken during the simulations, the circuit of fig. 5.8 is used for obtaining SNM.

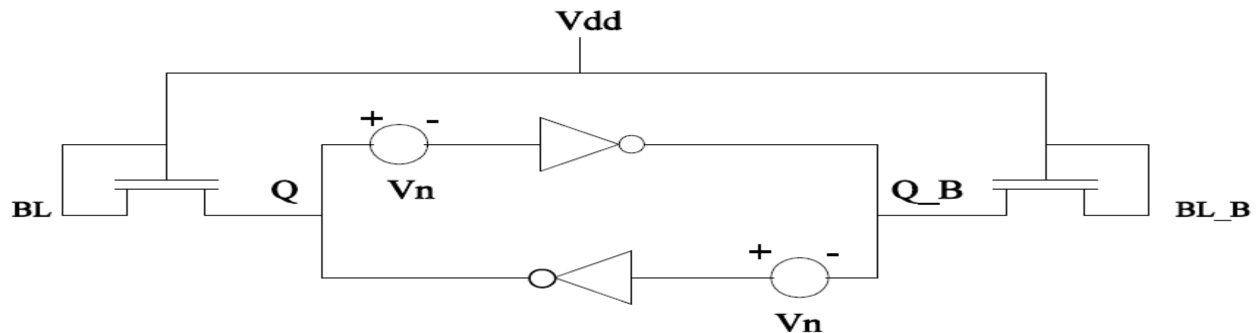


**Figure5.9: Circuit schematic for SNM simulation**

Two identical noise sources Vn are applied at both internal nodes Q and Q_B. BL, BL_B and WL are all connected to Vdd for the purpose of measuring SNM during read operation. Q is initialized to 1 and Q_B to 0. Both noise sources are then swept from 0 to Vdd. The value of Vn represents the SNM voltage when the value of Q drops to 50% of Vdd.

*5.2.6 Write Margin Measurement*

Write margin represents the writeability of the SRAM cell. It is defined as the maximum voltage on the bitline needed to flip the cell content during a write operation. During the write operation one of the bitlines needs to be discharged low (ideally 0). In most cases the cell can tolerate the non-zero low level on the bitline and complete a successful write operation. Write margin determines this tolerance of the SRAM cell.

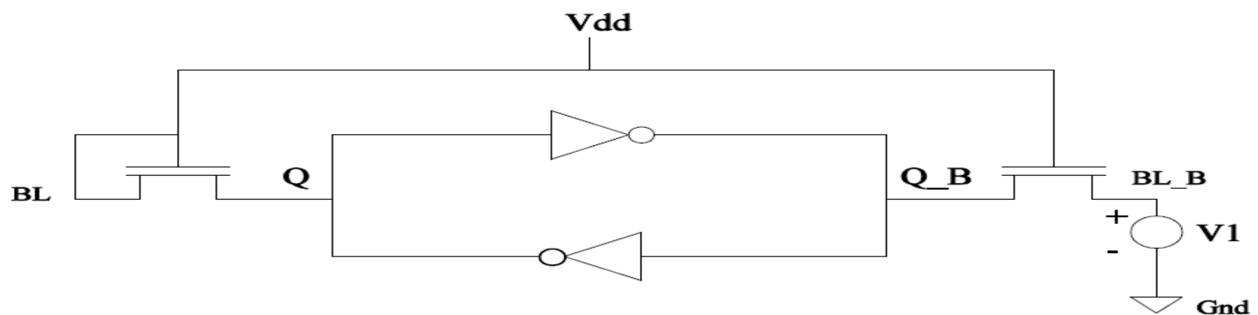


**Figure 5.10: Circuit Schematic for Write Margin Simulation**

For the simulations WL and BL are both connected to Vdd. A DC voltage source V1 is inserted between BL_B and ground. Q and Q_B are initialized to 0 and 1 respectively. V1 is swept from Vdd to 0. Write margin is the V1 value that flips the state of the SRAM cell.

*5.2.7 Standby Leakage Power Measurement*

The main components of leakage power in conventional CMOS design are:

- Reverse gate leakage power – due to tunnelling of electrons through the gate oxide
- Sub-threshold leakage power - due to sub-threshold currents. This is of significant importance as with each new technology node, transistor threshold voltages fall, hence leakage currents increase contributing greatly to leakage power.
- Drain-induced barrier lowering – depth of junction depletion layer increases as reverse bias voltage across drain to body PN junction increases.

As the CNFET structure used in this work is MOSFET-like, the sources of leakage power are the same as for MOSFETs and the CMOS SRAM leakage model is valid for CNFET-based SRAMs.

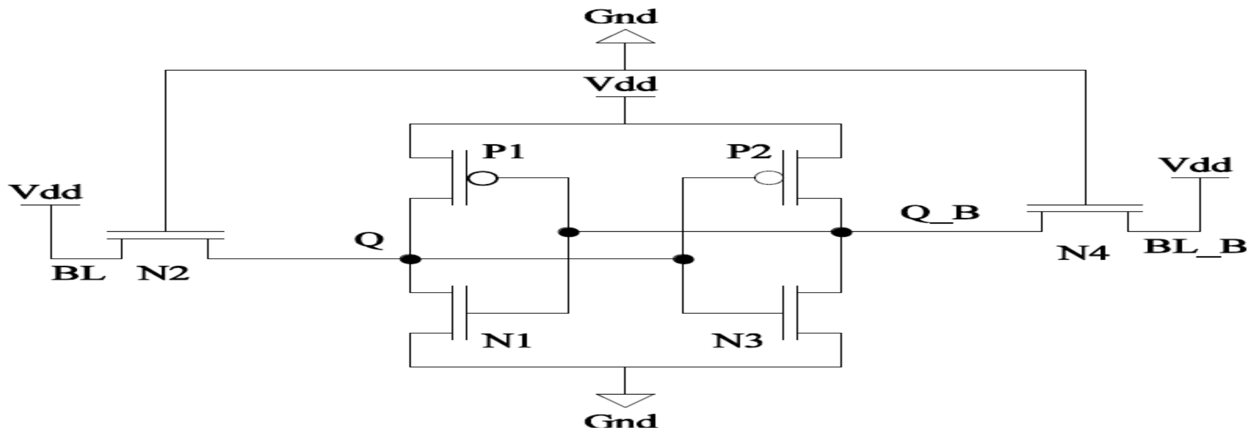


**Figure 5.11: Circuit Schematic for Standby Leakage Power Simulation**

Circuit of fig. 5.11 is devised for measuring the standby leakage power of the SRAM cell. To turn off the access transistors WL is connected to ground. To mimic the conditions of the SRAM cell at standby where BL and BL_B are both precharged high, ready for read or write operation, BL and BL_B are connected to Vdd. Once Q is initialised to 1 and Q_B to 0, simulations are carried out for finding the standby leakage power of the SRAM cell defined as the average power consumption of Vdd during simulations. All transistors contribute to the gate tunnelling leakage. N4, P2 and N1 contribute to the sub-threshold leakage [112].

## 5.3 Simulation Results

### *5.3.1 Read/Write Delay*

As touched upon in 5.2.2, read delay is defined as the time required for developing a 100mV differential voltage between BL and BL_B after WL (fig. 5.5) reaches 50% of its final swing. Fig. 5.5 shows the implemented circuit for measuring read delay. The short script below is a part of the HSPICE code used for measuring read delay:

```
vprecharge precharge 0 pwl 0n 0 0.1n 0 0.1000001n 0.9 5n 0.9 5.000001n 0 15n 0

Vw w 0 pwl 0n 0.9 5.1n 0.9 5.1000001n 0 15n 0

.TRAN .1n 15n sweep monte = 10000
```

```
.measure tran read_delay trig V(wl) val=0.45 rise=1 targ V(bl bl_b) val=0.1 rise=1
```

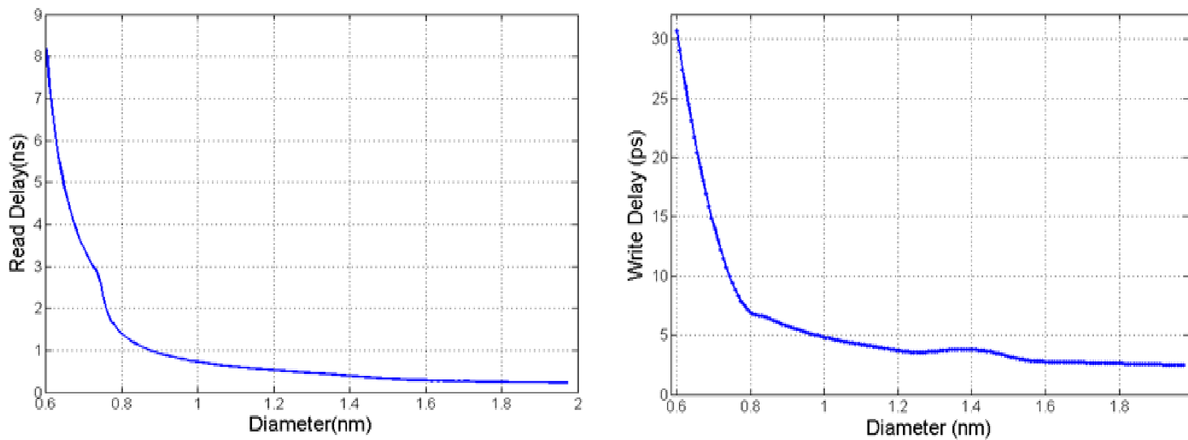


**Figure 5.12: Dependence of SRAM Read & Write Delay on CNT diameter**

Fig. 5.12 shows the relationship between read and write delays with different values of diameter respectively. Both delays decrease as diameter increases. As energy band gap ($E_g$) of a CNT is inversely proportional to its diameter ($D$) [13], increasing $D$ will cause a decrease in $E_g$ and hence a smaller energy barrier in way of flow of charge, which allows for larger on-currents of CNFETs; thus reducing delay. It can be observed from fig. 5.12 that the delay increases rapidly below $D$ of around 0.85nm. It is interesting to note that in previous chapters for the study of logic gates it was also observed that the $D$ at which variations in timing delays greatly increased was the same value of 0.85nm.

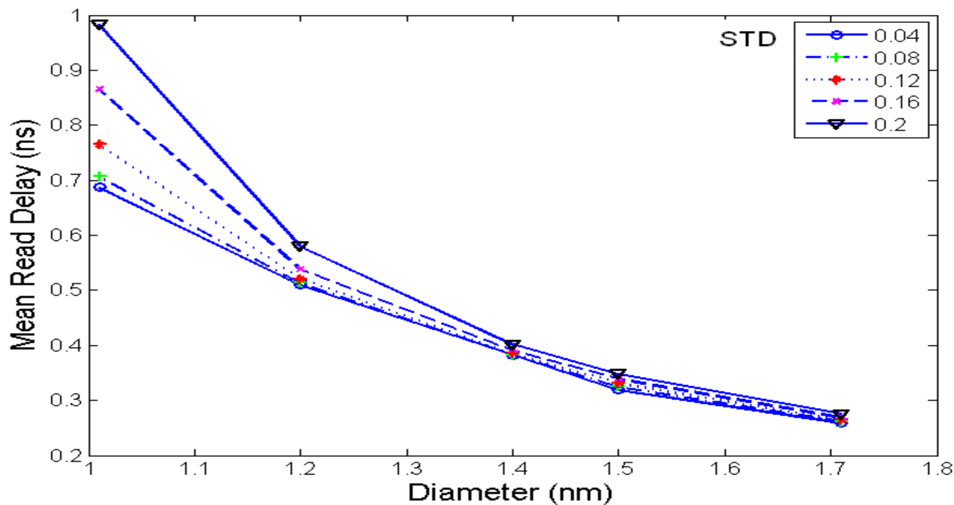


**Figure 5.13: Variation of Mean Read Delay with diameter Mean and STD**

Figs. 5.13 and 5.14 depict the dispersion of mean read/write delay values with $D_\mu$ and various $D_\delta$. It is observed that mean read/write delay increases with $D_\mu$ and fixed $D_\delta$. As equal $D_\delta$ values translate into different percentage change in different $D_\mu$, the coefficient of Variation (CV) was taken into account. CV is the ratio of STD over mean (μ) and is a normalized measure of dispersion which is comparable among different mean distributions.

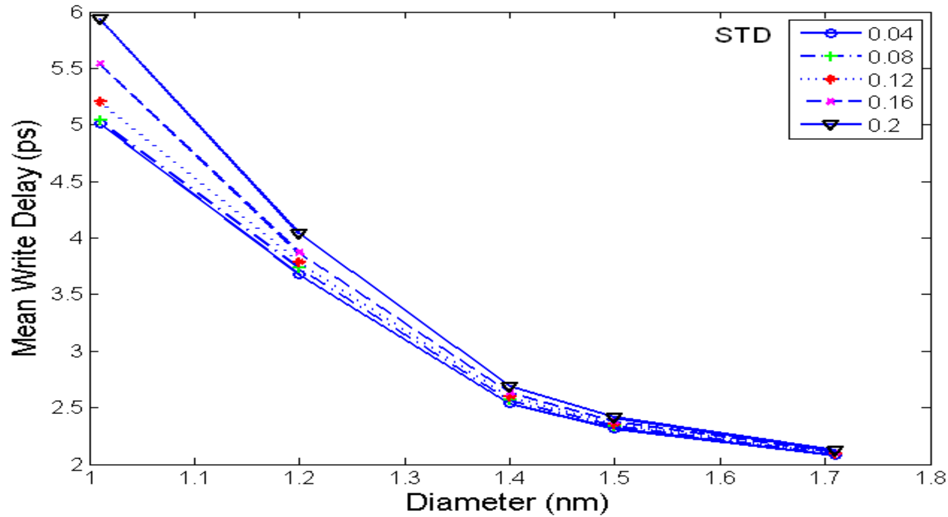


**Figure 5.14: Variation of Mean Write Delay with diameter Mean and STD**

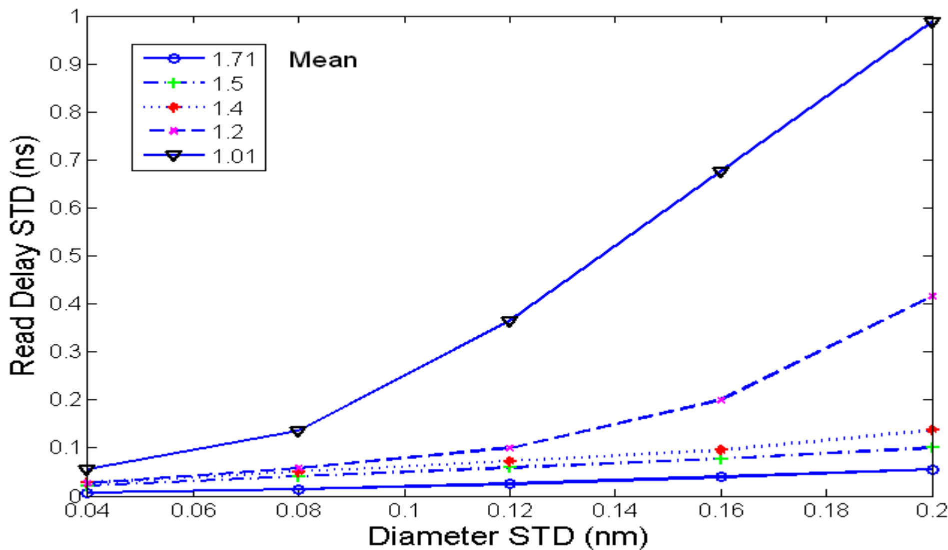


**Figure 5.15: Read Delay STD vs. CNT diameter Mean and STD**

Results reveal that both read and write delays show the least amount of variation at maximum CNT diameter mean ($D_\mu$) of 1.71nm as this is where the smallest value for CV is obtained. In figs. 5.15 and 5.16 STDs of read and write delays are plotted against $D_\delta$ respectively. It can be observed

that at smaller $D_{\mu}$, diameter standard deviation ($D_{\delta}$) variations cause far greater deviations in delay values. For instance at $D_{\mu}$ of 1.01nm, a $D_{\delta}$ of 0.2nm causes a read delay STD of 1ns, but the same $D_{\delta}$ for a $D_{\mu}$ of 1.71nm, only gives a 0.05ns STD in read delay. This result suggests higher reliability in terms of read/write delay variations with larger $D$.

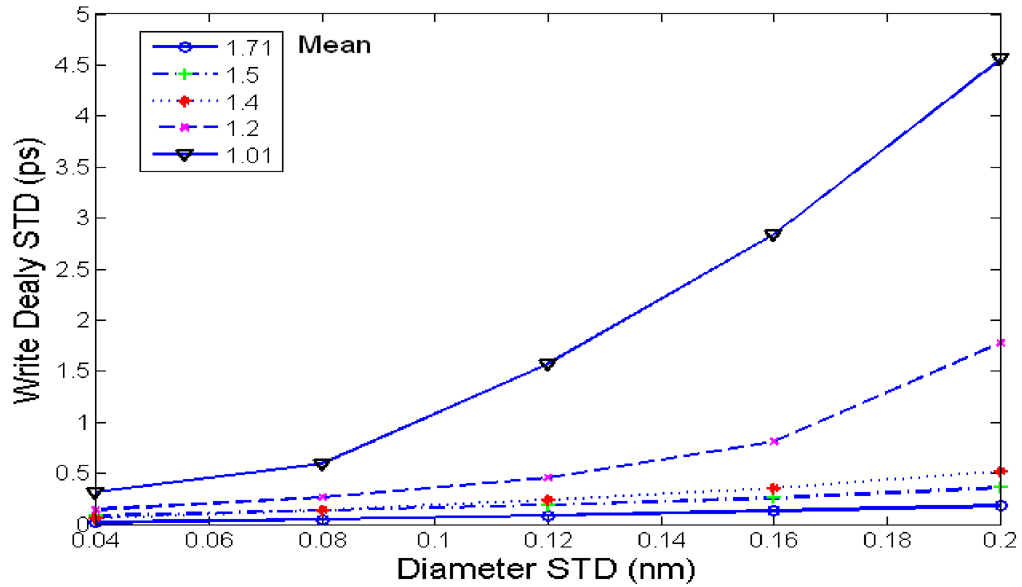


**Figure 5.16: Write Delay STD vs. CNT diameter Mean and STD**

*5.3.2 Static Noise Margin*

An important measure of the stability of SRAM cells is SNM [110]; defined as the maximum value of DC noise voltage tolerated without changing the stored bit [111]. A large SNM is desired to ensure stability of SRAM. Fig. 5.17 shows that SNM remains almost constant at the high value of ~270mV for $D \leq 0.85$nm. Above 0.85nm SNM worsens almost linearly with $D$ increasing; although even for larger CNT diameters, SNM of CNFET-based SRAMs is superior to that of CMOS implementations [91].

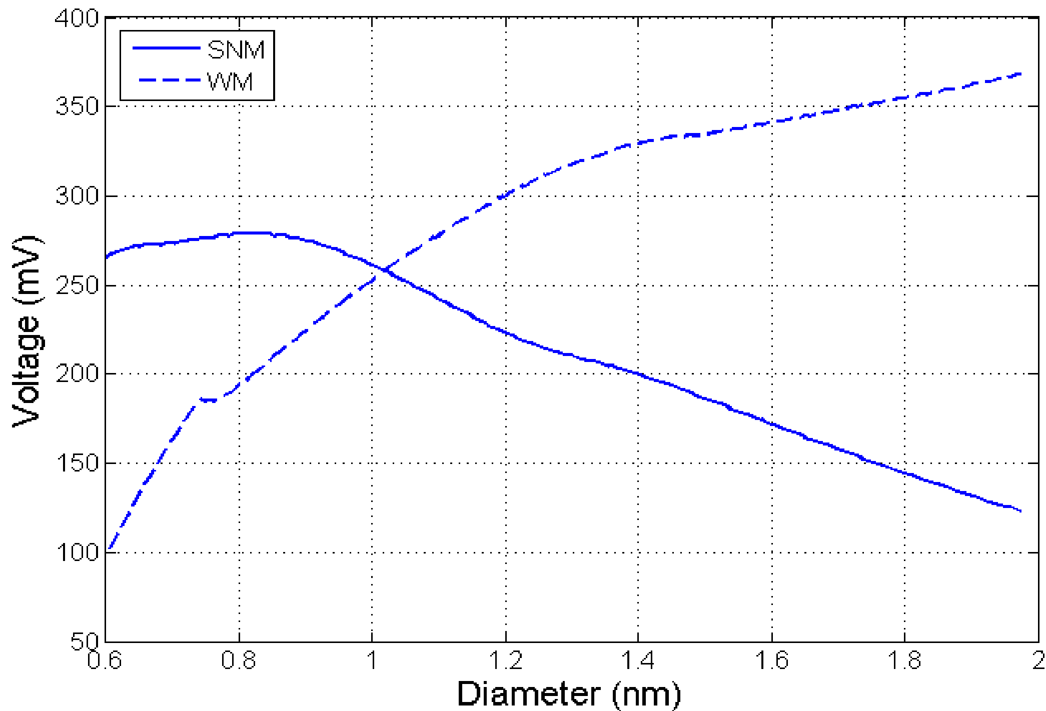


**Figure 5.17: Effect of CNT diameter change on SRAM SNM and WM**

SNM depends on three factors [113]: threshold voltage (refer to section 2.2), power supply and Cell Ratio (CR). With the CNFET-based SRAM, CR can be considered as the ratio of the number of CNTs in the drive transistors to that of access transistors; 3/2 in this case. Power supply is fixed in

the simulations; Threshold voltage ($V_{th}$) is the only remaining factor which could cause variation in SNM. $V_{th}$ is given by [113]:

$$V_{th} = \frac{\sqrt{3}}{3}\frac{aV_{\pi}}{eD} \tag{5.1}$$

Where $a = 2.49$Å, the carbon to carbon atom distance, $V_{\pi} = 3.033$eV, the carbon π-π bond energy in the tight binding model, $e$ is the unit electron charge and $D$ is CNT diameter.

It can be seen from (5.1) that $V_{th}$ is inversely proportional to $D$, meaning $D$ can be the only cause of SNM variations here. Thus, the decrease of SNM with increasing $D$ in Fig. 5.17 is explained through the dependence of $V_{th}$ on the inverse of $D$. SNM is proportional to $V_{th}$ [112]; as $D$ increases, $V_{th}$ decreases, causing SNM to decline.

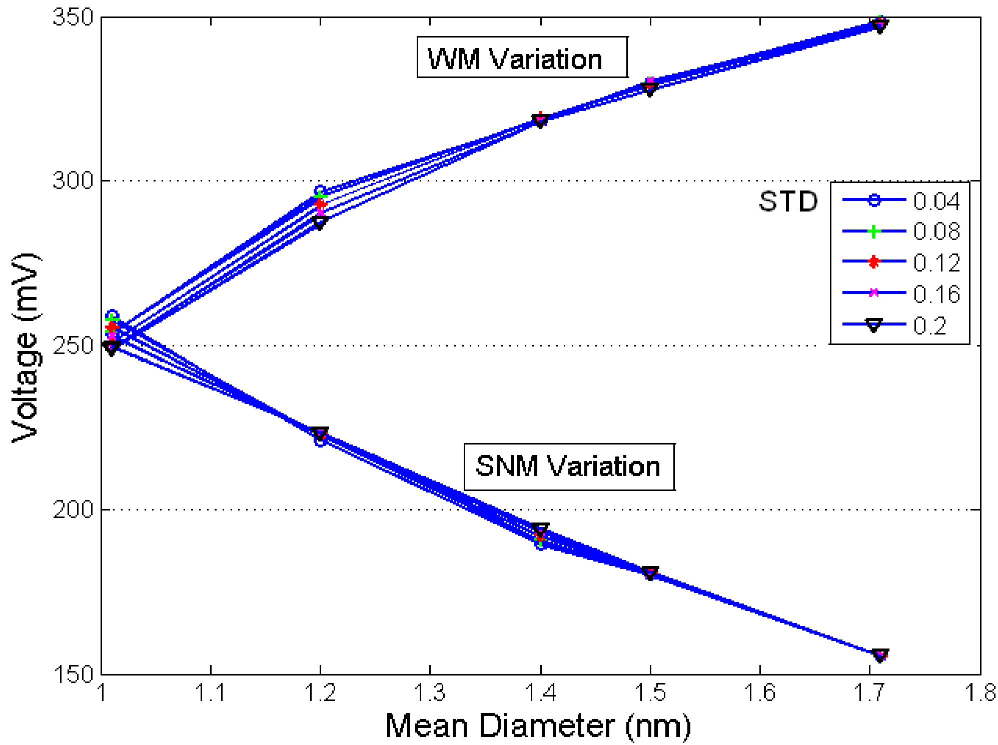


**Figure 5.18. Variation of mean SNM and WM vs. diameter Mean & STD**

Fig. 5.17 shows that below a $D$ of ~0.85nm, there is little change in SNM. There is even a slight decrease in SNM with decreasing $D$. It was found that there is a slight variation in CR at these small diameters (CR increases from ~1.48 at $D \approx 0.6$nm to ~ 1.49 at $D \approx 0.8$nm and stabilizes at this value

for larger $D$). This slight change in CR can be accredited to minute current changes due to CNTs being close to each other which could have a very slight effect on current at these very small CNT diameters; hence, the slight rise in SNM can be explained by the fact that SNM rises with increasing CR [112]. There is little change in mean SNM with $D_\delta$ especially when $D$ is large. For a $D_\mu$ of 1.01nm and in the range of $D_\delta$ considered, SNM only varies by ~10mV throughout. This change for $D_\mu$ > 1.5nm is ~ 0 (Fig. 5.18). STD change in SNM with various $D_\mu$ and $D_\delta$ is shown in Fig. 5.18. It is clear that the change in STD of SNM with $D_\delta$ is roughly constant for all $D_\mu$.

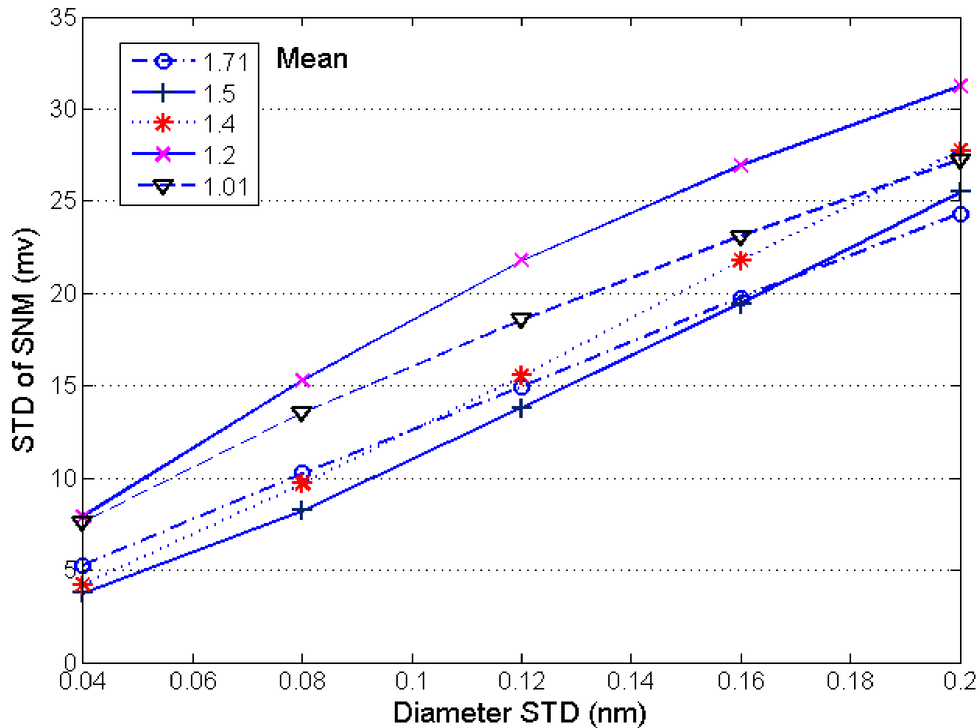


**Figure 5.19. STD of SNM vs. diameter Mean & STD**

*5.3.3 Write Margin*

WM and SNM are often trade-off parameters in SRAM design. The higher the SNM, the more difficult it is to write data into the cell (lower WM). A high WM is desired as it can improve write

delay and ensure correct data is being written. Further as a high write margin suggests that the bitline does not need to be discharged fully to 0, a high WM can guarantee reduced power consumption during write operation. A cell is written to by precharging one bitline to Vdd and discharging the other to ground, with the wordline at Vdd. WM is the highest acceptable voltage on this low bitline. WM is inversely proportional to the pull-up ratio (PR) of the SRAM cell and $V_{th}$. PR is defined as the drive current ratio of pull-up transistors over that of access transistors. The simulation results have shown that PR is almost constant; hence WM variation is dominated by $V_{th}$. As $D$ increases, $V_{th}$ is lowered, causing WM to rise as seen in Figs. 5.18 and 5.20. STD of WM rises as $D_{\delta}$ increases with a fixed $D_{\mu}$ (fig. 5.20). The minimum variation in WM is observed with the largest $D_{\mu}$ of 1.71nm.

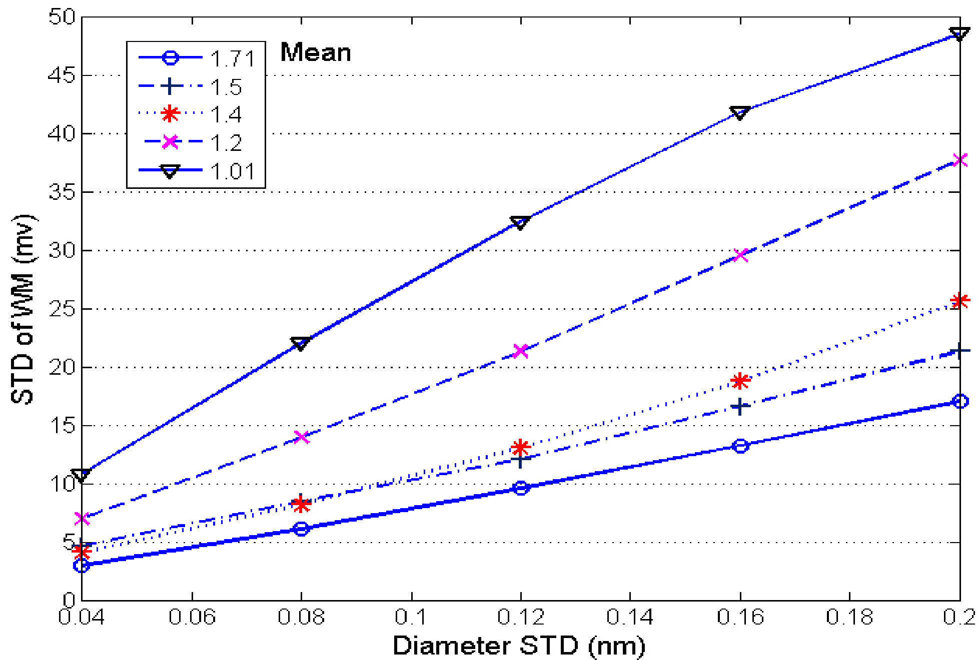


**Figure 5.20. STD of WM vs. diameter Mean & STD**

*5.3.4 Standby Leakage Power*

SRAMs as memory arrays occupy a significant area on a chip. This means that standby leakage power of SRAMs could dominate that of the entire chip and contribute to the total power

consumption of the whole chip. Fig. 5.21 shows the impact of increasing CNT diameter on the standby leakage power of the SRAM cells. Leakage power rises with increasing CNT diameter. The leakage power is composed of two components of gate leakage and sub-threshold leakage. Sub-threshold leakage current is the current that flows through the channel when the transistor is in the sub-threshold region, i.e. $V_{gs}$ is smaller than $V_{th}$. Sub-threshold leakage dominates the total leakage power especially in CNFTETs with high 'K' dielectrics which are used in this work. Further, the sub-threshold current is largely influenced by the threshold voltage, i.e. low threshold voltage results in high sub-threshold off current. As threshold voltage is inversely proportional to CNT diameter according to (5.1), sub-threshold leakage will rise with diameter increasing which dominates the whole standby leakage power trend.

It can be observed from the graph of figure 5.21 that standby leakage power starts to rise significantly above a CNT diameter of around 1.5nm. This suggests that in order to keep the leakage power of the SRAM cells down, it is wise to use CNTs with diameters below 1.5nm.

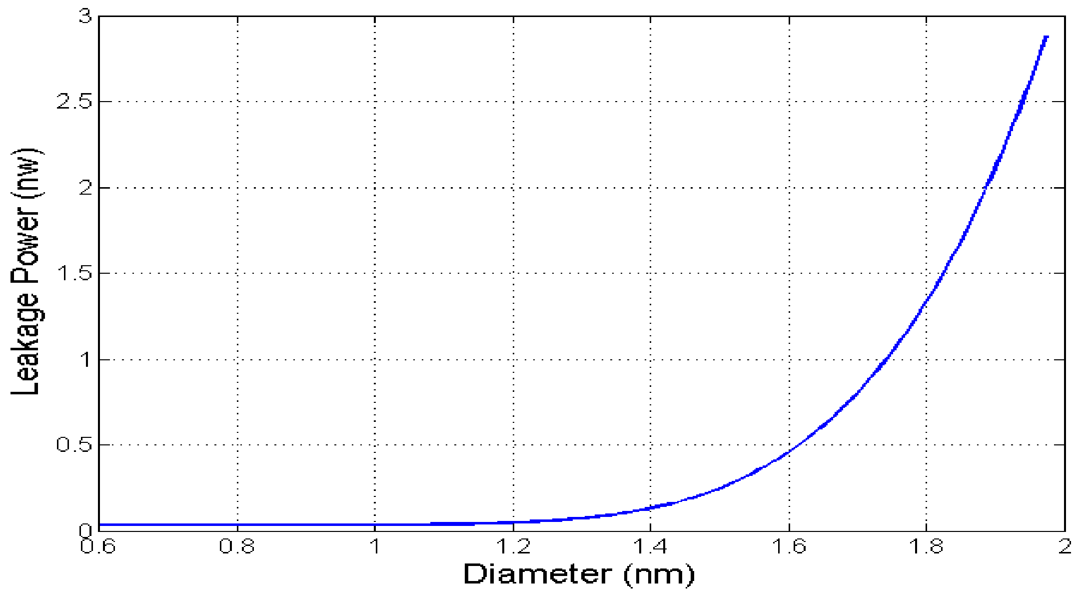


**Figure 5. 21: Standby Leakage Power vs. CNT Diameter**

Fig. 5.22 graphically describes the relationship between the mean leakage power and mean CNT diameter with various diameter STDs. The figure shows that at larger CNT mean diameters, as STD in variation is mean leakage power is more significant with changing diameter STD. Fig. 5.23 shows the relationship between STD of leakage power and the STD of CNT diameter with

various mean diameters. It is observed from Fig. 5.23 that most variation in leakage power occurs at larger CNT diameters. Smaller CNT mean diameters show the least variation in leakage power with changing diameter STD.

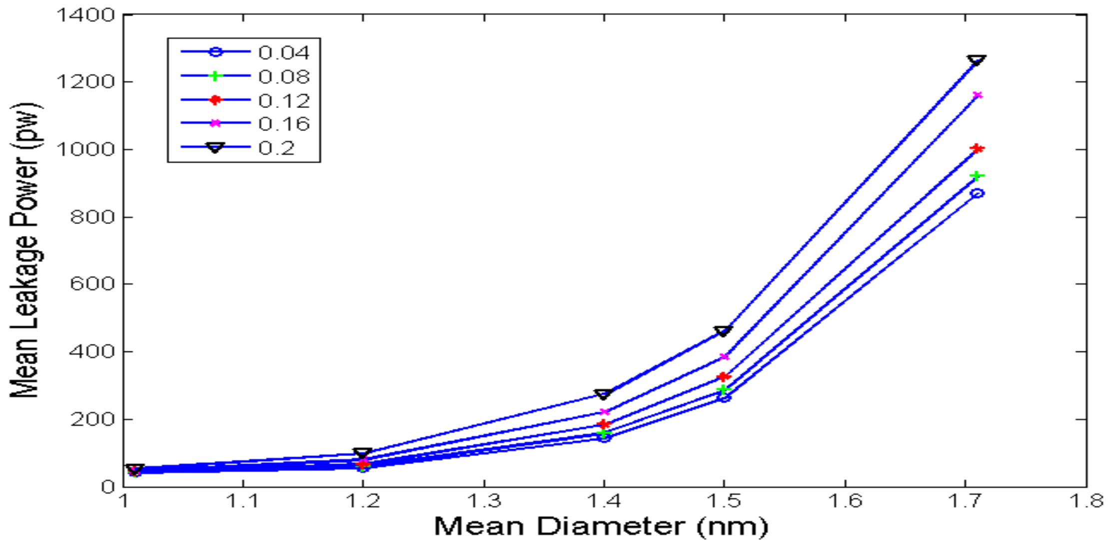


**Figure 5.22: Variation of Mean Leakage Power with Diameter Mean & STD.**

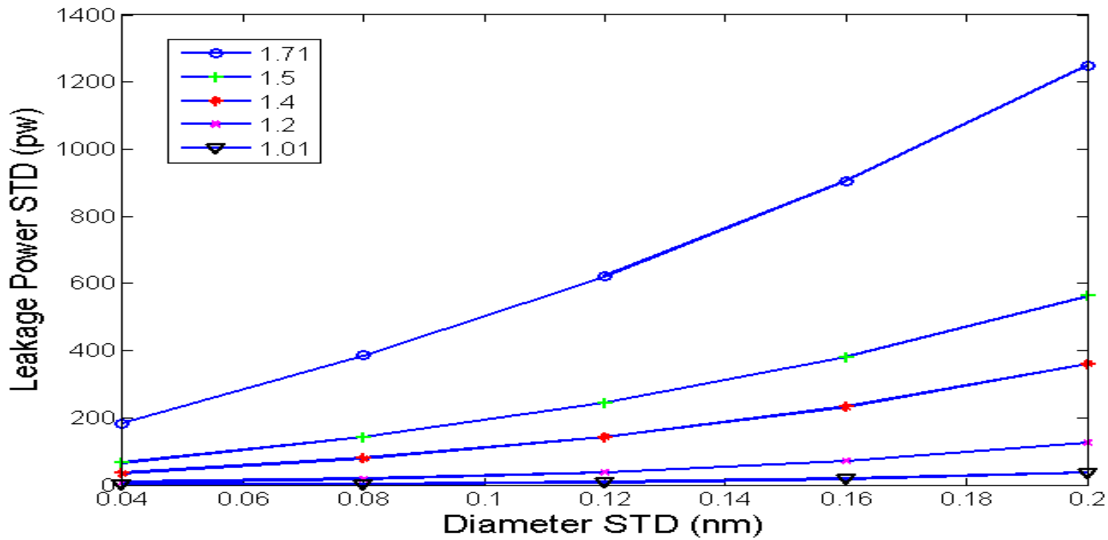


**Figure 5.23: Variation of STD in Leakage Power with Diameter Mean & STD**

## 5.4 Modelling of SRAM Performance Parameters

The Response Surface Methodology (RSM) regression technique has been applied to model the various performance parameters of the SRAM. The variables considered are CNT diameter mean and STD. The technique has been discussed in detail in chapter 3.

The ranges of mean read delay and mean CNT diameter are much bigger than the STD of the diameter. Also the effect of diameter STD on the response variable, i.e. mean read delay in this case, is less than that of mean diameter; hence, the log transformation is used to improve the accuracy of the model [58]. For the purpose of predicting the mean read delay of the SRAM cell with any CNT diameter mean and STD, a second-order model is developed given by:

$$Log\left(Rd_{\mu}\right) = \beta_0 + \beta_1 Log\left(D_{\mu}\right) + \beta_2 D_{\sigma} + \beta_{12} D_{\sigma} Log\left(D_{\mu}\right) + \beta_{11}\left(Log\left(D_{\mu}\right)\right)^2 + \beta_{22} {D_{\sigma}}^2 \quad (5.2)$$

Where $Rd_{\mu}$ is mean read delay, $D_{\mu}$ is mean CNT diameter and $D_{\sigma}$ is CNT diameter STD. By performing multiple linear regressions the coefficients are found and presented in table 5.1. Models for other SRAM parameters, i.e. mean write delay ($Wd_{\mu}$), mean SNM ($SNM_{\mu}$), mean Write Margin ($WM_{\mu}$) and mean leakage power ($LP_{\mu}$) have been developed. For each of these parameters, the model of equation 5.2 is used in the same manner as for $Rd_{\mu}$and the coefficients calculated. The $R^2_{adj}$ value is also calculated as a measure of the accuracy of each of the models. All the coefficients and the $R^2_{adj}$values are presented in table 5.1.

**Table 5.1: Statistical Model coefficients for mean values of various SRAM performance parameters**

| | $\boldsymbol{\beta_0}$ | $\boldsymbol{\beta_1}$ | $\boldsymbol{\beta_2}$ | $\boldsymbol{\beta_{12}}$ | $\boldsymbol{\beta_{11}}$ | $\boldsymbol{\beta_{22}}$ | $\boldsymbol{R^2_{adj}}$ |
|---|---|---|---|---|---|---|---|
| $\boldsymbol{Rd_{\mu}}$ | -0.03792 | -2.044 | 0.7851 | -3.4624 | 0.69 | 4.5447 | 0.99464 |
| $\boldsymbol{Wd_{\mu}}$ | 1.6273 | -2.4669 | 0.432 | -1.767 | 1.5196 | 2.3603 | 0.98952 |
| $\boldsymbol{SNM_{\mu}}$ | 5.5601 | -0.7597 | 0.0751 | 0.4056 | -0.4131 | -0.1944 | 0.99816 |
| $\boldsymbol{WM_{\mu}}$ | 5.5383 | 0.9022 | -0.1242 | 0.3296 | -0.609 | -0.2216 | 0.99721 |
| $\boldsymbol{LP_{\mu}}$ | 3.6113 | 1.3196 | -0.1087 | 2.1148 | 8.1569 | 10.4792 | 0.99508 |

Based on the Monte Carlo simulation results, a statistical model can also be developed for prediction of STD in read delay using the RSM regression model. Figure 5.14 shows that CNT

diameter STD has a considerable effect on SRAM read delay STD; hence, to achieve good regression results, the log transformation should be used:

$$Log\,(Rd_\sigma) = \gamma_0 + \gamma_1 Log(D_\mu) + \gamma_2 \log(D_\sigma) + \gamma_{12} Log(D_\sigma) Log(D_\mu) + \gamma_{11} \left(Log(D_\mu)\right)^2 + \gamma_{22}(Log(D_\sigma))^2 \quad (5.3)$$

Where $Rd_\sigma$ is the STD of read delay.

The coefficients of equation (5.3) are found and presented in table 5.2.

Statistical models for other SRAM performance parameters, i.e. Write Delay STD ($Wd_\sigma$), STD of SNM ($SNM_\sigma$), STD of Write Margin ($WM_\sigma$) and STD of standby Leakage Power $LP_\sigma$ have also been developed in the same manner of equation (5.3). Coefficients of these models together with the $R^2_{adj}$ values are presented in table 5.2.

**Table 5.2: Model coefficients for STD values of various SRAM performance parameters**

| | $\gamma_0$ | $\gamma_1$ | $\gamma_2$ | $\gamma_{12}$ | $\gamma_{11}$ | $\gamma_{22}$ | $R^2_{adj}$ |
|---|---|---|---|---|---|---|---|
| $Rd_\sigma$ | 4.3919 | -7.1956 | 3.2504 | -1.3864 | -0.9813 | 0.307 | 0.96023 |
| $Wd_\sigma$ | 6.0086 | -7.3406 | 3.4096 | -0.8517 | -0.0786 | 0.3676 | 0.97592 |
| $SNM_\sigma$ | 4.577 | 0.5249 | 0.6768 | -0.5493 | 0.0193 | 0.0321 | 0.93506 |
| $WM_\sigma$ | 5.8403 | -2.3199 | 1.219 | 0.1841 | 0.7763 | 0.0496 | 0.99051 |
| $LP_\sigma$ | 9.0271 | 5.3656 | 4.1661 | -2.2235 | -3.468 | 0.3911 | 0.99781 |

## 5.5 Conclusion

The performance of a CNFET-based SRAM in the presence of CNT diameter variations due to manufacturing inaccuracy has been analysed. In terms of read and write delays, results suggest that larger $D_{\mu}$ and smaller $D_{\delta}$ are optimal as they result in the least read/write delays and also less variation in mean and STD of delays, meaning more reliable circuit operation in terms of timing characteristics. Improved SNM is provided with smaller $D$ but smaller $D$ also means lower WM; hence, there's a trade-off involving circuit speed and WM on one side and SNM on the other. As a general rule, considering $D_{\delta}$ which is always present during CNT synthesis, it can be suggested that $D_{\mu}$ should be kept above 1nm but not larger than 1.5nm. This shows good agreement with the results obtained for leakage power of the SRAM as leakage power rises significantly above CNT diameter of ~ 1.5nm.

# Chapter 6 Conclusions

This work concerned a study of the performance of CNT-based electronic circuits in the presence of process parameter variations. CNT diameter variations are one of the main sources of variation which can cause CNFET drain current variations and hence irregular time and energy consumption behaviour. This thesis then proposed guidelines for effective variation-tolerant CNT-based logic design. Towards this end mathematical models were developed based on the simulated data that can model and predict the behaviour of CNFET-based structures according to a predefined CNT diameter distribution.

## 6.1 Conclusions and Contributions

In chapter 3 the effects of diameter variations on basic logic structures (NOT, NAND and NOR) were examined using Monte Carlo simulations. It was shown that due to technology limited control over nanoscopic CNT diameters and the CNT energy band gap direct dependence on CNT diameter, this lack of control can cause significant performance variability in CNT logic behaviour. It was found that variation in propagation delay decreases as the diameter of CNTs was increased. Parametric simulation results revealed a rapid increase in delay dependency on CNT diameter below a threshold of 0.85nm.

The results of the parametric simulations reveal that mean power consumption increases with mean CNT diameter. This is because as diameter increases the energy band gap of the CNT decreases allowing for more drive current at the same supply voltage. Results obtained further suggest that for any particular CNT mean diameter, the effects of diameter STD variation on average power consumption are negligible. This would suggest that for any mean diameter and any fabrication process with any STD accuracy, mean power consumption of the logic gates remains the same. However, variation in power consumption is greatly affected by STD of CNT diameter. The conclusion made was that larger CNT diameter and smaller diameter STD ensure less variation in power consumption; however larger diameters also translate into higher power consumption; hence a trade-off between higher power consumption and less variation in power consumption exists in CNFET based design.

Energy usage of the logic gates was measured using the Power Delay Product (PDP). For a given CNT, mean diameter changes in STD do not seem to affect the average PDP values significantly suggesting more robust operation in the presence of diameter STD variations. However with a change in mean CNT diameter, PDP varies more significantly. This result gives the designer more freedom to choose a CNT diameter for better tuning towards energy efficiency without having to consider uncertainties that may arise due to the technology lack of control over CNT diameter STD. Although no significant change is observed in mean PDP with changing STD the variation in PDP (difference from maximum to minimum) is greatly affected by diameter STD. This work further shows that greater energy efficiency is obtained for logic gates utilizing wider CNT diameters. The conclusion made was that provided that a diameter STD of < 0.12nm can be achieved, larger mean CNT diameters perform better in terms of time delay and PDP variation.

A relation was proposed by which a minimum mean diameter can be chosen to ensure minimum delay variation for various CNT-based logic gates. In order to propose an optimum CNT diameter for logic design, a trade-off between fast operation and power consumption should be taken into account:

$$D_{\mu} \geq \frac{0.85nm}{1-x}$$

Finally statistical models for the prediction of mean propagation delay and STD in propagation delay based on CNT diameter mean and standard deviation were developed using RSM regression technique. The developed models were verified and tested for accuracy using the $R^2$ measure, exhibiting excellent accuracy.

In chapter 4, more complex logic structures are studied. In this chapter it is suggested that as electrons and holes have the same mobility in CNTs, the multiplexer and XOR gate structures proposed in this chapter which employ an equal number of CNFETs in their pull up and pull down networks could be better suited as the building blocks of CNT-based electronic design due to the fact that they would be expected to exhibit similar rise and fall times.

In this chapter it has been shown that in accordance with the simpler logic gates studied, larger CNT diameters and smaller STDs provide multiplexers and XOR gates with more reliable timing operation and faster delay times. This work has shown that to keep power consumption minimum,

smaller CNT diameters are desirable. However, smaller CNT diameters also have the highest variation in power consumption. Minimum power consumption variation is achieved by employing larger CNT diameters and smaller diameter STDs. This presents the CNT logic designer with a three-way trade-off involving not only minimum power consumption and delay (variation), but also minimum power consumption and minimum variation in power consumption. Here again as for the previous logic gates considered propagation delay, rise time and fall time all increase sharply as diameter is reduced below ~0.85nm. On the other hand as CNT diameter increases past the 0.85nm mark, propagation delay is steadily reduced.
PDP values for the multiplexers and XOR gates show modest changes as CNT diameter STD is changed within a mean diameter group, typically less than $10e^{-20}$ J for larger CNT mean diameters. For small CNT diameters PDP values are larger in comparison with values for larger CNT mean diameters. Variation in PDP is extreme for smaller CNT mean diameters and is greatly dependent on diameter STD. For larger CNT diameters (>1.4nm) PDP values show little difference and are generally similar, further underlining the trade-off between propagation delay and power consumption as larger CNT diameters mean smaller delays but at the same time they lead to greater power consumption. This leads to the conclusion that to achieve better PDP values, diameters larger than 1.2nm are required. This result is in agreement with the choice of diameter put forward at the end of chapter 3 of this work.
Mathematical models were then developed for the prediction of mean and STD in propagation delay of the structures based on the diameter distribution profile of the CNTs utilized within the CNFETs.
Chapter 5 contained details of the design and simulation of a CNT-based SRAM cell. The SRAM cell was studied in the presence of CNT diameter variations and the various performance parameters such as SNM, read/write delay, write margin and standby leakage power were examined.

Both read and write delays decrease as CNT diameter increases, which is as a result of increased current drive as the energy band gap of a CNT is inversely proportional to CNT diameter. Both delays show the least variation with larger CNT diameters suggesting the highest reliability with larger diameter values.

The SNM value on the other hand worsens with larger CNT diameters showing an almost linear correlation with CNT diameter; an observation which was explained by showing the dependence of threshold voltage of the CNFET on CNT diameter. It was also shown that the change in STD of SNM with diameter STD is almost constant for all mean diameters.

The simulations detailed in this chapter also show that the variation in write margin is independent of the pull-up ratio of the transistors and hence only depends on CNT diameter through threshold voltage. WM rises with CNT diameter and minimum variation in WM is observed at larger diameters.

As far as standby leakage current is concerned, sub-threshold leakage is the dominant factor. As sub-threshold leakage rises with increasing diameter the standby leakage power of the SRAM rises rapidly at CNT diameters of 1.5nm and above.

Statistical models for mean and STD of SNM, WM, read/write delay and standby leakage power have been developed based on the obtained simulation results.

Generally larger mean diameter and smaller STD in CNT diameter are desired as far as propagation delay is concerned. Improved SNM is provided with smaller CNT diameters but smaller diameters also means lower WM; hence, there is a trade-off involving circuit speed and WM on one side and SNM on the other. As a general rule, considering diameter STD ($D_{\delta}$) which is always present during CNT synthesis, it can be suggested that mean diameter ($D_{\mu}$) should be kept above 1nm but not larger than 1.5nm. This shows good agreement with the results obtained for leakage power of the SRAM as leakage power rises significantly above CNT diameter of ~ 1.5nm.

**Table: 6.1 Summary of Design Rules**

| **Logic gates time delay** | $D$ >0.85nm |
|---|---|

| Average Power Consumption | Unaffected by diameter variation |
| --- | --- |
| PDP Efficiency | Utilize larger CNT mean diameters |
| PDP Variation | For minimized PDP variation, $D_\delta$ <0.12nm should be utilized |
| Power consumption Variation | Smaller diameter CNTs recommended to obtain less variation in power provided $D_\delta \leq$ 0.04nm |
| | Considering propagation delay, power consumption and PDP together, provided that $D_\delta$ <0.12nm, larger CNT diameters advisable. |
| **SRAM** | For reliable SNM $D \leq$ 0.85nm. |
| Standby Leakage Power | $D$ <1.5nm for min. leakage power |
| | Considering all aspects of SRAM design 1nm< $D_\mu$ <1.5nm |

## 6.2 Future work

This work can be improved further by a thorough examination of more complex logic functions and memory structures.

Another challenging way to carry this work forward would be to integrate the spread of propagation delays (worst-case propagation delay, rise/fall time, etc.) into a library of logic gates which would then become a useful platform for synthesis.

This work has only considered 2-input logic structures. A study with higher input structures (i.e. 4 input logic gates) would be useful, as stacking and the ensuing body effect will become involved. As the body effect is concerned with changes in the threshold voltage and $V_{th}$ in CNTs is directly related to CNT diameter this would be a particularly interesting study to carry out. To improve sub-threshold behaviour modelling, consideration of the surface potential lowering and the subsequent current increase caused by carrier pile up in the nFET/pFET channel region is necessary. This is analogous to the floating body effect as observed for SOI MOSEFT and depends

on the doping profile of the drain junction. Having a gradual doping profile can alleviate this effect by relaxing the potential drop over a longer distance.

Ensuring that CNTs are positioned in a straight line under the gate between the source and drain is a very difficult task. In most cases multiple CNTs are present under each CNFET gate and in all likelihood they are not completely in parallel with each other. This could then prevent the CNTs under the same gate from being in common-mode and experience varying voltage changes along their lengths hence changes in capacitance can occur. Being able to address this problem would be a major breakthrough in the area of CNFET design.

Also as CNTs in practice are often not aligned in a straight line and not parallel to each other, the length of the CNT under the gate can vary. This means that a constant channel length cannot be assumed and channel length variations become an issue.

A study of CNFET logic performance in the presence of various sources of variations at different technology nodes could be the next step towards future work.

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# Appendix A: Publications

1. Hamed Shahidipour, Arash Ahmadi and Koushik Maharatna, "Effect of Variability in SWCNT-Based Logic Gates", in *Proc. International Symposium on Integrated Circuits*, 2009.

2. Hamed Shahidiour, Yue Zhong, Arash Ahmadi and Koushik Maharatna, “Effects of CNT Diameter Variability on a CNFET-Based SRAM”, *IEEE Asia Pacific Conference on Circuits and Systems,* 2010.

# Appendix B: Sample HSPICE Codes

CNFET model sample code:

```
.LIB CNFET

.PROTECT

.OPTIONS PARHIER=LOCAL

.OPTIONS EPSMIN=1E-99

.OPTIONS EXPMAX=37

.INC 'PARAMETERS.lib'

.PARAM Lgate = 'MIN(Lg,Lgmax)'

*********************************************************************

* The Gate-CNT coupling capacitance

********************************************************************

.param indices = myindices1

* The diameter of the CNT

.PARAM dia='a*indices/pi'

* The radius of the CNT.

.PARAM rad='dia/2'

* Oxide thickness

.PARAM Hei='Tox+rad'

* The inverse of the capacitance with the uniform Kgate dielectric material

.PARAM RCo='log(2*Hei/dia + SQRT(POW(2*Hei/dia,2)-1))'

* The inverese of the effects due to the image charge

.PARAM RCimg='beta*log(2*Hei/(3*dia) + 2/3)'

* The inverse of the capacitance with infinite spacing between CNTs

.PARAM RCinf='RCo+RCimg'

* The potential due to the adjacent CNT

.PARAM Vadjc='0.5*log((POW(Pitch,2)+2*(Hei-rad)*(Hei+SQRT(POW(Hei,2)-
POW(rad,2))))/(POW(Pitch,2)+2*(Hei-rad)*(Hei-SQRT(POW(Hei,2)-POW(rad,2)))))'

* The potential due to the image charge of the adjacent CNT

.PARAM Vadji='0.5*beta*log((POW(Hei+dia,2)+POW(Pitch,2)) /
(9*POW(rad,2)+POW(Pitch,2)))*TANH((Hei+rad)/(Pitch-dia))'

* The total potential contributed by the adjacent CNT and its image charge

.PARAM RCadj='Vadjc+Vadji'
```

NAND Gate Sample HSPICE Code:

```
.param mymean = '1.2592e10 * 1.5e-9'
.param mysigma = '1.2592e10 * 0.04e-9 *3'
.param model2diam = 1.5e-9

.PARAM myindices = agauss(mymean,mysigma,3)
.param myindices1 = myindices
.param myindices2 = myindices1
.param myindices3 = myindices2
.param myindices4 = myindices3


***********************************************************************
* Define power supply

VDD Vdd 0 DC 0.9
Vdd1 Vdd1 0 DC 0.9    *separating gate supply and the load supply to get proper current reading
VA A 0  PULSE  0.9 0 10n 0.004n 0.004n 19.996n 50n
VB B 0  PWL 0N 0.9 20n 0.9 20.004N 0 40.000001N 0 40.004N 0.9 50.000002N 0.9 50.004N 0 70.000003N
0 70.004N 0.9 90N 0.9
******************Inverter subcircuit**********************************
.subckt NOT3 OUT IN Vdd1

XCNTmodel2 OUT IN 0    0    NCNFETmodel2 tubes = 3
XPNTmodel2 OUT IN Vdd1 Vdd1 PCNFETmodel2 tubes = 3
.ends
*******************NAND Subcircuit*************************************
.subckt nand2 IN1 IN2 C Vdd
*  D   G  S    B

X1 C   IN1  Vdd Vdd   PCNFET tubes = 3
X2 C   IN2  Vdd Vdd   PCNFET tubes = 3
X3 C   IN1  N34 0     NCNFET tubes = 3
X4 N34 IN2  0   0     NCNFET tubes = 3
.ends
***********************************************************************

x0 A   B  C2   Vdd nand2


*******************************************************************************************
x6 OUT2 C2  Vdd1    not3
x7 OUT2 C2  Vdd1    not3
x8 OUT2 C2  Vdd1    not3
x9 OUT2 C2  Vdd1    not3

.TRAN .1n 90n sweep monte = 10000


*****Get rise/fall time in range 10% to 90% of Vdd @ junction of NAND gate with Inverters*****

.measure tran risetime trig V(C2) val=0.1 rise=1 targ V(C2) val=0.81 RISE=1
.measure tran falltime trig V(C2) val=0.81 fall=1 targ V(C2) val=0.1 fall=1

******Get propogation delay of circuit************************************
.measure tran mydelay1 TRIG V(A) val = 0.45 FALL = 1 TARG V(C2) VAL = 0.45 RISE = 1
.measure tran mydelay2 TRIG V(A) val = 0.45 RISE = 2 TARG V(C2) VAL = 0.45 fall = 2
.measure tran mydelay3 TRIG V(B) val = 0.45 RISE = 1 TARG V(C2) VAL = 0.45 fall = 1
.measure tran mydelay4 TRIG V(B) val = 0.45 FALL = 2 TARG V(C2) VAL = 0.45 RISE = 2

**********************Show power dissipation*****************************
.measure pwr AVG P(VDD) FROM 0NS TO 90NS

.END
```

Multiplexer Sample HSPICE Code:

```
.param mymean = '1.2592e10 * 1.5e-9'
.param mysigma = '1.2592e10 * 0.04e-9 *3'
.param model2diam = 1.5e-9

.PARAM myindices = agauss(mymean,mysigma,3)
.param myindices1 = myindices
.param myindices2 = myindices1
.param myindices3 = myindices2
.param myindices4 = myindices3

VDD Vdd   0 DC 0.9
Vdd1 Vdd1 0 DC 0.9    *separating the gate supply and the load supply to get proper current
reading

VA    A    0   PULSE  0.9 0   10n 0.004n 0.004n 19.996n 50n
VB    B    0   PWL 0N 0.9 20n 0.9 20.004N 0 40.000001N 0 40.004N 0.9 50.000002N 0.9 50.004N 0
70.000003N 0 70.004N 0.9 90N 0.9
VEN1  EN1  0   PULSE  0.9 0   0n 0.004n 0.004n 45n 90n
VENB1 ENB1 0   PULSE  0   0.9 0n 0.004n 0.004n 45n 90n

******************Multiplexer subcircuit**********************************
.subckt mux  D0 D1 S SB OUT1 Vdd
*    D    G   S    B
XP1 N12   D0  Vdd  Vdd PCNFET tubes = 3
XP2 OUT1  S   N12  Vdd PCNFET tubes = 3
XP3 N34   D1  Vdd  Vdd PCNFET tubes = 3
XP4 OUT1  SB  N34  Vdd PCNFET tubes = 3
XN5 OUT1  SB  N56  0   NCNFET tubes = 3
XN6 N56   D0  0    0   NCNFET tubes = 3
XN7 OUT1  S   N78  0   NCNFET tubes = 3
XN8 N78   D1  0    0   NCNFET tubes = 3
.ends
**************************************************************************

x0 A B EN1 ENB1 Y1  Vdd mux

******************Inverter subcircuit**********************************
.subckt NOT3 OUT IN Vdd1

XCNTmodel2 OUT IN 0    0    NCNFETmodel2 tubes = 3
XPNTmodel2 OUT IN Vdd1 Vdd1 PCNFETmodel2 tubes = 3
.ends
***********************************************************************

x1 OUT2 Y1  Vdd1    not3
x2 OUT2 Y1  Vdd1    not3
x3 OUT2 Y1  Vdd1    not3
x4 OUT2 Y1  Vdd1    not3

.TRAN .1n 90n sweep monte = 10000
*****Get rise/fall time in range 10% to 90% of Vdd @ junction of Mux gate with Inverters*******

.measure tran risetime trig V(Y1) val=0.1 rise=1 targ V(Y1) val=0.81 RISE=1
.measure tran falltime trig V(Y1) val=0.81 fall=1 targ V(Y1) val=0.1 fall=1

******Get propogation delay of circuit************************************
.measure tran mydelay1 TRIG V(A) val = 0.45 FALL = 1 TARG V(Y1) VAL = 0.45 RISE = 1
.measure tran mydelay2 TRIG V(A) val = 0.45 RISE = 1 TARG V(Y1) VAL = 0.45 fall = 1
.measure tran mydelay3 TRIG V(B) val = 0.45 FALL = 2 TARG V(Y1) VAL = 0.45 RISE = 2
.measure tran mydelay4 TRIG V(B) val = 0.45 RISE = 2 TARG V(Y1) VAL = 0.45 FALL = 2

***********************Show power dissipation******************************
.measure pwr AVG P(VDD) FROM 0NS TO 90NS

.END
```

SRAM Read Delay Measurement Sample HSPICE Code:

```
.lib 'CNFET.lib' CNFET
.lib 'CNFETmodel2.lib' CNFETmodel2

*Some CNFET parameters:
.param Ccsd=0      CoupleRatio=0
.param m_cnt=1     Efo=0.6
*****changed here
.param Wg=48e-9        Cb=40e-12
.param Lg=32e-9    Lgef=100e-9
.param Vfn=0       Vfp=0
.param m=19        n=0
.param Hox=4e-9    Kox=16

 ******************************
 ******************************
.param mymean = '1.2592e10 * 1.01e-9'
.param mysigma = '1.2592e10 * 0.08e-9 *3'
.param model2diam = 1.01e-9

.PARAM myindices = agauss(mymean,mysigma,3)
.param myindices1 = myindices
.param myindices2 = myindices1
.param myindices3 = myindices2
.param myindices4 = myindices3
*******************************************************************
* Define power supply
VDD Vdd   0 DC 0.9
Vdd1 Vdd1 0 DC 0.9

.global vdd vdd1 0
******************Inverter subcircuit**********************************
.subckt inv OUT1 IN1 vdd

XCNT OUT1 IN1 0   0   NCNFET tubes = 3
XPNT OUT1 IN1 Vdd Vdd PCNFET tubes = 1
.ends

******************2nd model Inverter subcircuit*********************************
.subckt inv_ld OUT2 IN2 vdd1

XCNTmodel2 OUT2 IN2 0    0    NCNFETmodel2 tubes = 3
XPNTmodel2 OUT2 IN2 Vdd1 Vdd1 PCNFETmodel2 tubes = 3
.ends

*******************************************************************************************
x1 q_b q vdd  inv
x2 q  q_b vdd inv
xcnt1 bl wl q 0 NCNFET tubes = 2
xcnt2 bl_b wl q_b 0 NCNFET tubes = 2
x5 wl w vdd1 inv_ld
c1 bl 0 100f
c2 bl_b 0 100f
xpnt1 bl pl vdd1 vdd1 PCNFETmodel2 tubes = 3
xpnt2 bl_b pl vdd1 vdd1 PCNFETmodel2 tubes = 3
x6 pl precharge vdd1 inv_ld

.ic q = 0.9 q_b=0 bl=0 bl_b=0

vprecharge precharge 0 pwl 0n 0 0.1n 0 0.1000001n 0.9 5n 0.9 5.000001n 0 15n 0
Vw w 0 pwl 0n 0.9 5.1n 0.9 5.1000001n 0 15n 0
.TRAN .1n 15n sweep monte = 10000
.measure tran read_delay trig V(wl) val=0.45 rise=1 targ V(bl bl_b) val=0.1 rise=1
.measure readpower max P(VDD) FROM 0NS TO 15NS

.END
```

SRAM Write Margin Measurement Sample HSPICE Code:

```
*For optimal accuracy, convergence, and runtime
***************************************************
.options POST
.options AUTOSTOP
.options INGOLD=2     DCON=1
.options GSHUNT=1e-12 RMIN=1e-15
.options ABSTOL=1e-5  ABSVDC=1e-4
.options RELTOL=1e-2  RELVDC=1e-2
.options NUMDGT=4     PIVOT=13
.options runlvl=0

.param   TEMP=27
***************************************************
*Include relevant model files
***************************************************
.lib 'CNFET.lib' CNFET
.lib 'CNFETmodel2.lib' CNFETmodel2

*******************************
.param mymean = '1.2592e10 * 1.5e-9'
.param mysigma = '1.2592e10 * 0.04e-9 *3'
.param model2diam = 1.01e-9

.PARAM myindices = agauss(mymean,mysigma,3)
.param myindices1 = myindices
.param myindices2 = myindices1
.param myindices3 = myindices2
.param myindices4 = myindices3


*********************************************************************
* Define power supply

VDD Vdd 0 DC 0.9

.global vdd 0
*****************Inverter subcircuit*********************************
.subckt inv OUT1 IN1

XCNT OUT1 IN1 0   0   NCNFET tubes = 3
XPNT OUT1 IN1 Vdd Vdd PCNFET tubes = 1
.ends

x1 q_b q  inv
x2 q  q_b inv
xcnt1 q vdd vdd 0 NCNFET tubes = 2
xcnt2 q_b vdd bl_b 0 NCNFET tubes = 2
v1 bl_b 0 0.9
.NODESET q = 0 q_b=0.9

.dc v1 0.5 0 10m sweep monte=10000

*****Get the write delay of SRAM*******

.measure dc wm find V(bl_b) when v(q_b)=0.45

.END
```