Resistive Open Faults Detectability Analysis and Implications for Testing Low Power Nanometric ICs

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***Abstract*—Resistive open faults (ROFs) represent common manufacturing defects in integrated circuit (IC) interconnects and result in delay faults that cause timing failures and reliability risks. The non-monotonic dependence of ROF-induced delay fault on supply voltage (V_{DD}) poses a concern on whether single-V_{DD} testing would suffice low power nanometric designs. Our analysis shows multi-V_{DD} test could be required depending on test speed selection. This knowledge can be exploited in small delay fault testing to reduce chances of test escapes while minimizing cost.**

***Index Terms*—Resistive Opens, Low Power Design, Variability, Detectability, Multi-V_{DD} Test, Small Delay Faults**

I. Introduction

RESISTIVE open faults (ROFs) represent degradation in conductivity within a circuit's interconnects, due to inevitable manufacturing failures in current and emerging technologies [1], [2]. Such faults cause performance failures and reliability risks whose magnitude is not only *voltage-sensitive* but also influenced by the electrical characteristics of driving and driven CMOS networks [3]–[5]. The resulting impact (delay faults) can be detected in silicon by at-speed tests or faster-than-at-speed tests depending on whether the accumulative delay of the infected path exceeds the delay of the longest path of the design [6], [7]. The investigation of optimal fault detectability dependence on V_{DD} gains attention due to test escapes minimization interest especially for low power designs employing dynamic voltage scaling [8]. Previous research [4], [9], [10] suggested testing at the highest voltage level, but have not shown whether testing at the highest voltage level would always yield optimal detectability.

Consequently, the work reported here attempts to answer whether multi-V_{DD} testing is required when a range of supply and threshold voltages is provided. The ultimate goal is to evaluate the viability of multi-V_{DD} testing for future nanometric ICs designed for low power and subject to variability. This is carried out by performing accurate circuit-level simulations for benchmark designs using nanometric technological models. Our analysis shows that determining whether multi-V_{DD} is required is test speed dependent especially for faster-than-at-speed testing.

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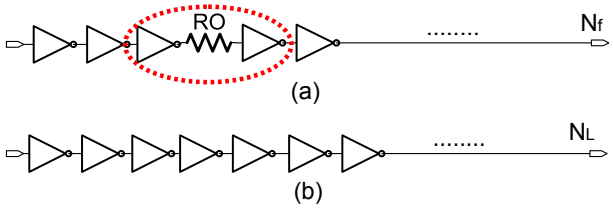


Fig. 1. Inverter Chain Example: (a) Faulty path with marks around the faulty segment, (b) Long path

This brief is organized as follows: a qualitative analysis on the voltage-detectability dependencies is presented in Section II. Fault detectability results using benchmark circuits simulation is explained and discussed in Sections III and IV. Concluding remarks are given in Section V.

II. Fault Detectability Dependencies

To qualitatively analyze the detectability dependency on the supply voltage and its implication on test, inverters chains, as shown in Fig. 1, are considered. The figure shows a chain with resistance RO emulating the lump resistance of an open fault and interconnect. A longer path with stages N_L is introduced to provide test clock period values. It is assumed that this long path is the longest in a given set of paths and not necessarily the longest in the circuit so to enable generalization for at-speed and faster-than-at-speed testing cases.

The propagated fault effect through the faulty path can only be detectable if the detectability defined as the ratio of the delay of the sensitized faulty path (t_{Df}) to the test clock period (TCP) is ≥ 1. Therefore,

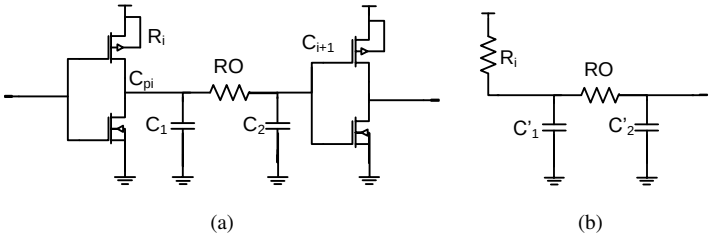
$$\text{Detectability} = \frac{t_{Df}}{TCP} \geq 1. \tag{1}$$

The test clock period will be equalized here to the propagation delay of the long path. Assuming the path has N_L number of logic stages with equal propagation delay per stage, this yields:

$$\frac{t_D(RO) + t_D(N_f - 1)}{TCP} = \frac{t_D(RO) + t_D(N_f - 1)}{t_D(N_L)} \geq 1 \tag{2}$$

Where, $t_D(RO)$ is the delay exclusively contributed by the faulty segment; $t_D(N_f - 1)$ is the delay of the path without the faulty segment; and $t_D(N_L)$ is the delay of the longest path. For further analysis of the delay contributed by the fault, an expanded schematic of the faulty segment in Fig. 1a is plotted in Fig. 2. In Fig. 2a, the parasitic capacitances of the driving

and driven transistors are lumped in capacitors C_{pi} and C_{i+1}, whereas the interconnect parasitic capacitances are represented by C_1 and C_2. For rising transition at driven CMOS network, the faulty segment can effectively be reduced to an equivalent π model as shown in Fig. 2b.



(a) (b)

Fig. 2. Faulty segment: (a) Driving and driven gates, (b) Equivalent π-model Circuit

An approximate expression for the delay contributed by the faulty segment can be obtained as follows:

$$t_D(RO) = K_c \times (R_i(C_1^{'} + C_2^{'}) + RO \times C_2^{'}) \tag{3}$$

K_c is a delay constant for this π-modeled RC circuit. R_i is the average channel resistance calculated as the ratio between channel voltage to current as in Equation (4):

$$R_i = \frac{V_{DD}}{K_r(V_{DD} - V_t)^{\alpha}} \tag{4}$$

Where K_r is a transconductance parameter related to the transistor channel size and α is a technology-dependent coefficient. The propagation delay of an inverter chain with equal delay stages can generally be obtained by multiplying the number of logic gates (N) by the gate delay as in Equation (5):

$$t_D(N) = N \times \left(\frac{(C_1^{'} + C_2^{'})V_{DD}}{K_t(V_{DD} - V_t)^{\alpha}} \right) \tag{5}$$

Where K_t is a parameter related to the transistor channel size and C is the capacitance of the driven gate. Substituting Equation (5) into Equation (2) yields the following equations:

$$t_D(RO) + (N_f - 1) \times \left(\frac{(C_1^{'} + C_2^{'})V_{DD}}{K_t(V_{DD} - V_t)^{\alpha}} \right) \geq N_L \times \left(\frac{(C_1^{'} + C_2^{'})V_{DD}}{K_t(V_{DD} - V_t)^{\alpha}} \right) \tag{6}$$

$$t_D(RO) \geq (N_L - N_f + 1) \times \left(\frac{(C_1^{'} + C_2^{'})V_{DD}}{K_t(V_{DD} - V_t)^{\alpha}} \right) \tag{7}$$

Using $t_D(RO)$ from Equation (3):

$$K_c(R_i(C_1^{'}+C_2^{'})+RO\times C_2^{'}) \geq \frac{(N_L - N_f + 1)(C_1^{'} + C_2^{'})V_{DD}}{K_t(V_{DD} - V_t)^{\alpha}} \tag{8}$$

Substituting R_i and making simple manipulations yields:

$$RO \geq \frac{(N_L - N_f + 1)(C_1^{'} + C_2^{'})V_{DD} - K_f(C_1^{'} + C_2^{'})V_{DD}}{K_c K_t C_2^{'}(V_{DD} - V_t)^{\alpha}} \tag{9}$$

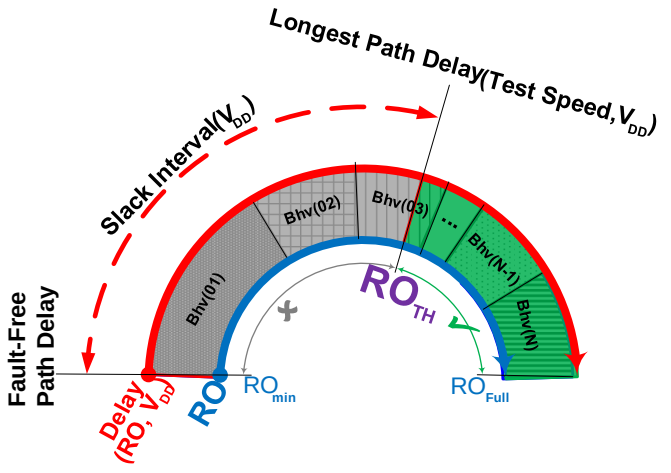


Fig. 3. Graphical Illustration for RO_{TH} Dependence on Longest Path Delay, Fault-free Slack Interval and the Corresponding Delay Behavior at RO_{TH}

Replacing K, $K^{'}$ and C_f by K_r, K_c, K_t and $(C_1^{'} + C_2^{'})/C_2^{'}$ reduces the formula to:

$$RO \geq \frac{(N_L - N_f + 1)C_f V_{DD} - K^{'} C_f V_{DD}}{K(V_{DD} - V_t)^{\alpha}} \tag{10}$$

For paths with large slack interval, the approximation holds $(N_L - N_f)C_f V_{DD} \gg (1 - K^{'})C_f V_{DD}$ which yields,

$$RO \gtrapprox \frac{(N_L - N_f)C_f V_{DD}}{K(V_{DD} - V_t)^{\alpha}} \tag{11}$$

C_f can be considered here as layout and fault location dependent parameter shaping the relative total segment capacitance $(C_1^{'} + C_2^{'})$ to the portion driven by fault $(C_2^{'})$. In nanometric designs, α is almost 1 due to velocity saturation effects, therefore, the minimum detectable fault, the open resistance detection threshold RO_{TH}, can be written as:

$$RO_{TH} \propto \frac{(N_L - N_f)C_f}{(1 - \frac{V_t}{V_{DD}})} \tag{12}$$

The formula in (12) qualitatively captures the main detectability dependencies of ROF. It suggests that the detection threshold is proportional to the slack interval lenght of affected path (i.e. $(N_f - N_L)$) which in turn depends on test speed. In other words, the detectability is improved by increasing the test speed so as to minimize slack interval while using the lowest V_t and highest V_{DD}. This formula agrees with the literature [4], [5], [9]. However, the exact relationship requires the consideration of input slope dependent inverter-output voltage evolution waveform [11] incorporating short-channel effects in CMOS triode, saturation [12] and sub-threshold regions [13], the voltage-dependent transition slope effect [14], voltage-dependent CMOS diffusion capacitances and layout-dependent coupling capacitances [3], as they strongly impact the average channel resistance in Equation 4 and the effective capacitance in Equation 12.

To explain the above-mentioned voltage-detectability dependencies more accurately, the model in [15] can be used as in Fig. 3. The figure depicts a generalized faulty path delay behavior for different RO values shown along the inner circular

axis (RO_{min} - RO_{Full}) and corresponding delay on the outer circular axis with respective increasing or decreasing behaviors (Bhv(01), Bhv(02),...,Bhv(N)). For RO values greater than RO_{TH} the fault is detectable, otherwise, the fault remains undetectable. By increasing the test speed to capture small delay faults, the delay behavior with V_{DD} of the longest path and the corresponding faulty path given the slack interval can become different thereby coverage maximization might imply different V_{DD} selection.

Consequently, detectability dependencies on V_{DD} based on test speed can be hypothesized. The remainder of this brief explains the method used to evaluate this likelihood, and the results obtained in detail.

III. Empirical Analysis

In this empirical analysis, the V_{DD} value that provides optimal detectability, inferred from RO_{TH}, is obtained from exhaustive parametric circuit-level simulations. The value for RO_{TH} is computed using the delay information of the faulty path at all resistance values (ROs) and that of the test clock period. To explain the hybrid numerical-circuit simulation method in determining the RO_{TH}, a path delay example is considered in Fig. 4. In this figure, the path delay values at discrete RO values labelled as cross and square marks for two different V_{DD} values is shown. The discrete values of open resistances used in the simulation were [50, 1k, 10k, 50k, 100k, 500k, 1M, 5M, 10M]. The value of 50 Ω, denoting the minimum open resistance RO_{min}, is arbitrarily selected to account for the parasitic interconnect resistance, whereas the rest were selected in a semi-logarithmic manner to mimic the distribution reported in [1]. Other values for resistances were also used and similar results were observed. SPLINE interpolation is used to obtain a continuous delay waveform for the entire RO axis. RO_{TH} is obtained by finding the intersection between the test clock period (TCP) and faulty path delay at different V_{DD}.

Once all resistance detection thresholds are known then the V_{DD} that provides the best detectability can be identified by searching all V_{DD} and test patterns for the minimum RO_{TH} and reporting the corresponding V_{DD} value. This procedure is repeated for all faults (ROFs) in each design. The considered faults are the inter-cells faults (not covering the intra-cell locations), however, due to the ATPG's capability to generate transition test patterns [16], the final number of faults are less. Finally, the selected voltages are reported.

The detectability was evaluated at-speed and faster-than-at-speed. In at-speed tests, the test clock period, TCP was determined in each simulation by finding the longest path delay obtained for each V_{DD} and V_t. In faster-than-at-speed tests, TCP values were identified by finding shorter path delays at different percentiles of the path delay population and test results that sensitize larger paths are discarded. This percentile is called here the test clock period percentile ($TCPP$) which describes the percentage of paths which are considered in the analysis, sorted in ascending order according to the delay of the path, compared to the total number of paths. For example, 100% $TCPP$ means that the test clock period is equivalent to the longest path delay. Whereas, 75%, 50%, and 25% mean that the test clock period is equal to the respective lower percentiles of the longest path delay.

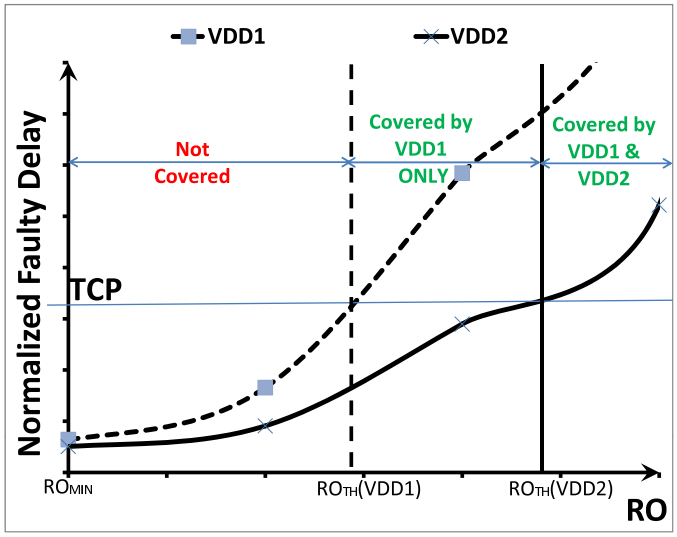


Fig. 4. RO_{TH} Computation Using SPLINE Interpolation for Faulty Path Delay at V_{DD1} (solid lines) and V_{DD2} (dashed lines) Supply Voltages

TABLE I
Transistor Models and Respective V_{DD} and V_t Settings

Tech	V_{DD}			Standard V_t		High V_t	
	H	M	L	$\|Vtn\|$	$\|Vtp\|$	$\|Vtn\|$	$\|Vtp\|$
130nm	1.20	1.00	0.80	0.28	0.27	0.39	0.41
32nm	0.90	0.80	0.70	0.51	0.37	0.63	0.58
16nm	0.70	0.65	0.59	0.48	0.43	0.68	0.69

The simulation was carried out on a representative set of benchmark circuits [17]–[19] using 130nm, 32nm and 16nm technology models (from Silterra and the Berkeley Predictive Technology Models (BPTM) [20] for Hi-K/metal gate/strained Si technologies respectively). The corresponding V_{DD} and V_t values used are given in Table I, whereby the highest V_{DD} value, the median V_{DD} value and the lowest value are denoted as V_{DDH}, V_{DDM} and V_{DDL} respectively. For the 16nm transistor model, the values imply that the design operates in the near and sub-threshold regions to give some insights on fault detectability in such an operating environment. Finally, to mimic the effect of process variability in this analysis, the test clock period was scaled by 125% at each V_{DD} to account for worst case delay spread as shown in previous literature [10], [21].

IV. Results and Discussion

Results were obtained for variety of circuits (c17, s27, b01, c432, c499, c880, c1355, c1908, c2670, c3540 and c6288), portions of them were published elsewhere [22], show consistent observations. However due to space limit and analysis accuracy, only very accurate results for small circuit simulations showing optimum voltage selection at different speeds for 130nm, 32nm and 16nm technologies are given in

TABLE II
OPTIMAL V_{DD} SELECTION FOR AT-SPEED AND FASTER-THAN-AT-SPEED TESTS FOR 130NM, 32NM AND 16NM TECHNOLOGIES

Technology		130nm			32nm			16nm		
Ckt	**TCPP**	V_{DDH}	V_{DDM}	V_{DDL}	V_{DDH}	V_{DDM}	V_{DDL}	V_{DDH}	V_{DDM}	V_{DDL}
c17	100	9	0	0	9	0	0	9	0	0
	75	**4**	**3**	**0**	9	0	0	9	0	0
	50	7	0	0	9	0	0	9	0	0
	25	5	0	0	5	0	0	5	0	0
s27	100	14	0	0	14	0	0	14	0	0
	75	13	0	0	14	0	0	14	0	0
	50	11	0	0	**13**	**0**	**1**	**13**	**0**	**1**
	25	8	0	0	**10**	**0**	**1**	**7**	**1**	**0**
b01	100	40	0	0	40	0	0	22	0	0
	75	40	0	0	40	0	0	16	0	0
	50	**29**	**0**	**2**	**32**	**5**	**3**	11	0	0
	25	**16**	**0**	**2**	23	0	0	5	0	0
MultiVDD Tests		**25%**			**25%**			**16%**		

Table II. Even though the worsen variability impact at reduced V_{DD} is considered here (unlike in [22]), the results show that up to 25% of the cases are optimally detected at reduced V_{DD}, thus suggesting multi-V_{DD} testing scheme for these particular runs. Without considering the variability, the percentage was even more (60%), substantiating Rosselló et al findings in [10].

Upon investigating the cases motivating multi-V_{DD} test scheme, it is found that almost all of those cases (including those not reported here) occurred when tests were made at faster-than the nominal speed. This can be explained by the change of longest path delay behavior and that of the faulty path with V_{DD} as follows. Due to path delay ranking dependence on V_{DD}, the longest path delay behavior at particular percentiles exhibit weaker delay ratio at V_{DDM} and V_{DDL} compared to that at V_{DDH} of other percentiles. Reducing the test speed causes consequent slack interval reduction thereby allowing new manifestation of faulty path delay behavior (as demonstrated earlier in Fig. 3). Whenever the behavior of corresponding RO range exhibits increased delay ratio at V_{DDM} and V_{DDL} (decreasing or mid-bump behavior patterns) compared to that at V_{DDH}, V_{DDM} and V_{DDL} cause earlier fault detection compared to V_{DDH} thereby making them more optimal for test. For example, when running the test for c17 circuit synthesized on 16nm technology at the speed of the 40^{th} percentile, three faults were optimally tested at V_{DDM}, however, it returns back to zero when test speed is set at 50^{th} and 25^{th} percentiles due to change of new longest path delay behavior and that of the faulty path at given slack interval. Remarkably, such speed-dependent detectability was not observed and deemed unlikely to manifest in design-blocks that uses single Hight-V_t library or totally operate in near/sub-threshold regions due to the observed absence of path delay ordering dependence on V_{DD} possibly due to the consistent dramatic monotonic increase of delay at reduced V_{DD} for all path delay population.

In summary, optimal V_{DD} selection for testing resistive open faults shows speed-dependency in multi-V_{DD} and multi-V_t designs. The probability of this dependence is higher for faster-than-at-speed tests compared to at-speed, and in multi-V_{DD}/multi-V_t designs compared to those operating in sub-threshold or using single high V_t design. This knowledge can be incorporated in test speed selection that minimizes cost without compromizing quality.

To incorporate this knowledge in test generation framework, a path-aware test pattern generator such as [23] can be used. To reduce time consuming circuit-level simulation per standard cell, each ROF can be simulated at cell level with various combinations of driving strengths and capacitive loads. A database of the resulting additional delays incorporated in statistical timing analysis per standard cell such as [24] can be then used for any circuit to calculate the RO_{TH} for any given slack interval and V_{DD} value. Additionally to improve test quality, layout and switching dependent induced noise from neighbouring networks such as in [3] can be considered. Due to the possible voltage variation due to ground bounce and IR drop, test generation robustness can be enhanced by exploiting the "don't care" pattern so that its impact is reduced [25]. Finally, to distinguish between delay faults due to variability and that due to ROF, the transition-dependent ROF-induced delay behavior explained in [15] can be exploited.

V. CONCLUSION

The optimal detectability of resistive open faults exhibits test speed-dependency in multi-V_{DD} and multi-V_t nanometric designs. This dependency may suggest a multi-V_{DD} test scheme depending on the exact test speed selection. This is due to the speed-dependent delay-voltage behavior of the longest path and the faulty-size dependent delay behavior of faulty paths. This knowledge can be exploited in small delay test pattern generation by carefully selecting the test speed such that single or minimum number of V_{DD} levels is required for optimal fault coverage so to minimize possibilities of test escapes while maintaining low test cost.

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