Multi-layer graphene FET compact circuit-level model with temperature effects

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***Abstract*—This paper presents a circuit-level model of a dual-gate bilayer and four layer graphene field effect transistor (GFET). The model provides an accurate estimation of the conductance at the charge neutrality point (CNP). At the CNP the device has its maximum resistance, at which the model is validated against experimental data of the device off-current for a range of electric fields perpendicular to the channel. The model shows a good agreement for validations carried out at constant and varying temperatures. Using the general Schottky equation, the model estimates the amount of bandgap opening created by the application of an electric field. Also the model shows good agreement when validated against experiment for the channel output conductance against varying gate voltage for both a bilayer and four layer graphene channel.**

I. Introduction

The physical and electrical properties of graphene have motivated a significant amount research into its behaviour. Due to the absence of sufficient bandgap opening [1] only a small on-off current ratio is achievable thus limiting digital logic applications. However, this does not exclude analog and RF applications, as there has been extensive research into graphene FET radio frequency performance [2], [3], [4]. Equally, RF models have been published with good f_{MAX} and f_T performance for some devices [5], [6], [7], [8], [9].

In addition to the growing research into RF performance, there have been a number of experimental results on the characterization of graphene transistors with respect to the drain DC current transport characteristics [10], [11], [12], [13]. The availability of experimental data as well as the need to design circuits have led to an extensive research into compact models which supplements the RF models [11], [14], [15], [16], [17], [18], [19].

These models use the drift equation to model the transport characteristic for both small signal and large signal. Also some of the models report closed form analytical equations for the three regions of operation namely triode, saturation and ambipolar saturation regions [14].

In this paper, we propose a compact model based on a recent work [14] on the development of graphene FET for SPICE implementations. Compared to existing models, this work introduces an interlayer capacitance which is used in calculating the channel surface potential and the channel resistance at the charge neutrality point (CNP). The interlayer capacitance has been used in determining the layer asymmetry and consequently estimating the bandgap opening [20], [21]. Some models [11], [14], [15] use a linear relationship with the back-gate to calculate the threshold voltage (that is the top-gate voltage at the CNP). Although this method proves a simple way to estimate the threshold voltage and it is accurate for single layer graphene FET, an experiment [10] shows that a linear relationship can deviate substantially for back-gate voltages further away from the back-gate voltage at the Dirac point. In this work, an equivalent circuit is proposed to calculate the threshold voltage. Also, so far no existing SPICE related graphene FET model has incorporated temperature effects. In this work, we develop a model that determines the channel resistance dependence on temperature.

The main contribution of this paper is a general graphene FET model that can be used for an arbitrary number of graphene layers, N. The model has been validated against experimental data for $N = 2$ and $N = 4$. Other improvements of the earlier model [14] are: an accurate estimation of the conductance of the channel at the Dirac point, an accurate determination of the threshold voltage and an analytical equation that models the channel resistance dependence on temperature from which an estimate of the bandgap opening is calculated.

This paper is organized as follows: Section II derives the surface potentials of the top and bottom layers which determines the quantum capacitance and the gate capacitances, section III evaluates the electric field dependent bandgap, section IV validates the model against experiment for both bilayer and four-layer graphene FET and section V concludes the paper.

II. Capacitance Model

Fig. 1(a) shows the layout of a bilayer graphene FET. The layout investigated in this paper consist of both a top-gate and a back-gate responsible for the perpendicular electric field the channel. The channel is sandwiched between both the top-gate and back-gate dielectrics.

Fig. 1(b) shows an equivalent circuit for a bilayer graphene FET. Single layer samples of graphene have been reported to have a measured quantum capacitance [22] which is a function of the surface potential [23]. The proposed model uses a quantum capacitance for each layer namely $C_q(\varphi_{s1})$ and $C_q(\varphi_{s2})$ as shown in Fig. 1(b). Both quantum capacitances are separated by an interlayer capacitance, C_o. In this paper

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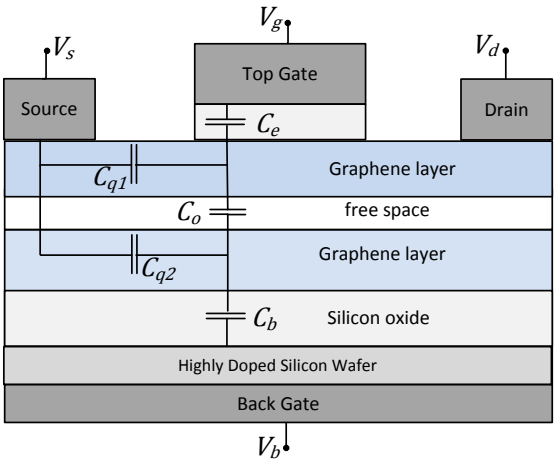
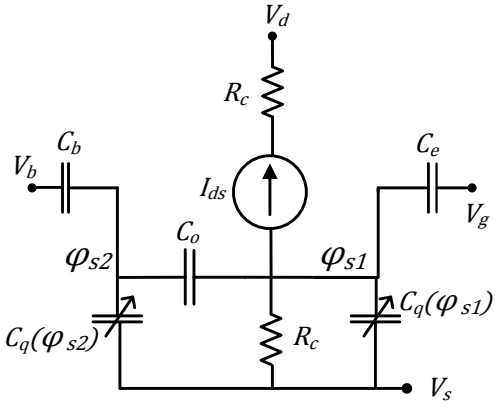


(a) Bilayer graphene transistor layout



(b) The transistor layout and proposed equivalent circuit

Fig. 1. Schematic of the graphene bilayer transistor

the layers are indexed relative to the top-gate, with the closest layer as 1, 2 for the next layer and so forth.

A. Surface potential

For the top-layer, the quantum capacitance varies by its surface potential, φ_{s1}, by

$$C_{qvar}(\varphi_{s1}) = q^2 \frac{2}{\pi} \frac{q|\varphi_{s1}|}{(\hbar v_f)^2} \tag{1}$$

where v_f is the Fermi velocity [24], electronic charge q and the reduced Plank's constant $\hbar$. When $\varphi_{s1} = 0$ the channel has been reported to have a charge density, n_0 [25], [26]. Taking n_0 into consideration, at $\varphi_{s1} = 0$ the resulting capacitance is

$$C_{qmin} = \frac{q^2\sqrt{n_0}}{\sqrt{\pi}\hbar v_f} \tag{2}$$

From the Drude model the charge density in the channel is $n = \sqrt{n_0^2 + n_*^2}$ where n_* is the charge density caused by the gate potential. Hence, the quantum capacitance of the layer is

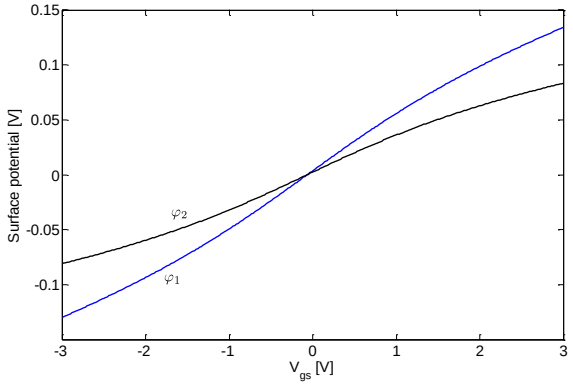


Fig. 2. The surface potential φ_{s1} and φ_{s2} of the layers as a function of V_{gs} at $V_{bs} = 50V$.

$$C_q(\varphi_s) = \frac{C_{qmin}^2 + 2(C_{qvar}(\varphi_s)/2)^2}{\sqrt{C_{qmin}^2 + (C_{qvar}(\varphi_s)/2)^2}} \tag{3}$$

From the capacitance model in Fig. 1(b) the surface potentials can be solved, giving that C_e is the capacitance due to the dielectric between the top-gate and the channel, C_b is the capacitance between the channel and the back-gate, V_d, V_g, V_s and V_b are the drain, top-gate, source and back-gate voltages respectively. Therefore, the surface potential of the second layer is

$$\varphi_{s2} = \frac{1}{C_o}\Big[-C_e(V_{gs} - V_{gs}^0) + \varphi_{s1}(C_e + C_o) + \varphi_{s1}\sqrt{(C_{qvar}(\varphi_{s1})/2)^2 + C_{qmin}^2}\Big] \tag{4}$$

where V_{gs}^0 is the top-gate-to-source Dirac point voltage and V_{bs}^0 is the back-gate-to-source Dirac point voltage. Equally, the first layer's surface potential is

$$\varphi_{s1} = \frac{1}{C_o}\Big[-C_b(V_{bs} - V_{bs}^0) + \varphi_{s2}(C_e + C_o) + \varphi_{s2}\sqrt{(C_{qvar}(\varphi_{s2})/2)^2 + C_{qmin}^2}\Big] \tag{5}$$

Fig. 2 (see parameter values in test case A of Table I) shows the behavior of the surface potential of both layers as a function of V_{gs} for $V_{bs} = 50V$. Positive values of φ_{s1} indicates the Fermi level is in the conduction band, negative values indicates the Fermi level is in the valence band and a zero value indicates a charge neutrality point [27].

B. Effective gate capacitance

Since the top-gate capacitance is comparable to the quantum capacitance, to accurately model the capacitance between V_g and V_s the quantum capacitance has to be taken into consideration. This gives and effective capacitance, C_{top}, as

$$C_{top} = \frac{C_e(C_oC_q(\varphi_{s2}) + (C_o + C_q(\varphi_{s2}) + C_b)C_q(\varphi_{s1}))}{C_oC_q(\varphi_{s2}) + (C_o + C_q(\varphi_{s2}) + C_b)(C_q(\varphi_{s1}) + C_e)} \tag{6}$$

C. Threshold voltage

Eqns. (5) and (4) are the surface potential of both layers and are a function of the V_{gs}. At charge neutrality, $\varphi_{s1} = 0$ and the value of V_{gs} which satisfies this condition is referred to as the threshold voltage, V_o.

$$V_o = V_{gs}^0 - \varphi_{s2}\frac{C_o}{C_e} \tag{7}$$

III. Bilayer gap using electric field

The device bandgap greatly influences the channel conductivity, in the bilayer graphene the electric field opens the bandgap by creating an asymmetry between the layers [21].

A. Off-current electric field dependence

Considering the bilayer graphene with interlayer capacitance, C_o, the excess charge density on the first layer is Q_{s1} and the excess density of the second layer is Q_{s2}. The excess charge is considered at charge neutrality.

$$Q_{s1,2} = \frac{\varphi_{s1,2}}{2}C_{qvar}(\varphi_{s1,2}) \tag{8}$$

Here, it is assumed that the transistor does not have multiple top-gates therefore at charge neutrality $\varphi_{s1} = 0$ and the corresponding change in potential energy between the layers is

$$U_{s2} = \frac{\varphi_{s2}^2}{6}C_{qvar}(\varphi_{s2})) \tag{9}$$

The charge distributed throughout the layer gives rise to the electric field between the layers and the resulting change in potential energy determines the asymmetry between the layers [21].

Introducing the bare asymmetry [21], [20] for a non zero density the total potential energy is

$$U_s = \frac{\varphi_{s1}^2}{6}C_{qvar}(\varphi_{s1})) + U_{s2} \tag{10}$$

It should be noted that U_{s2} is constant in eqn. (10) while φ_{s1} changes by the action of the top-gate voltage.

Considering a parallel plate capacitor of capacitance C_b between the second layer and the back-gate. Carriers on the second layer facing the back-gate gives rise to a potential energy, $1/2C_bV_E^2$. Where V_E is the potential difference as a result of a uniformly distributed charge. It is assumed that a uniform electric field exist between the metallic back-gate and the second layer. Therefore relating with eqn.(9)

$$V_E = \sqrt{\frac{2U_s}{C_b}} \tag{11}$$

For a given temperature, V_E being a reflection of the bandgap opening should satisfy the relationship $R_q \propto \exp(V_E/V_T)$. So the channel resistance at zero density, when the channel experiences charge neutrality, for a given back-gate voltage is

$$R_q = R_s^0 \exp(V_E/V_T) \tag{12}$$

Where R_s^0 is the resistance at intrinsic state, that is at charge neutrality condition with zero bandgap opening and V_T is a constant voltage. Based on the Drude model used in characterising graphene devices

$$R_s^0 = \frac{1}{qn_o\mu} + 2R_c \tag{13}$$

Where R_c is the series resistance, q is the electronic charge, n_o is the minimum charge density and μ is the mobility.

B. Off-current Temperature dependence

Although published results of the off-current, I_{off}, supports an exponential relationship with the gate voltage [10], it deviates from the relationship $I_{off} \propto \exp(q\phi_{barrier}/K_BT)$ which suggests that a small bandgap opened. Rather the relationship $I_{off} \propto \exp((T_o/T)^n)$ has been reported [13] in which $n = 1/3$. The exponent parameter $n = 1/3$ may be due to the presence of localized impurities in the bandgap.

Aside graphene, in other semiconducting materials the temperature dependence has equally been modeled using the exponent $n = 1/3$ in the Steinhart and Hart equation [28] and also using the exponent $n = 1/4$ in the Hoge-3 equation [29]. In modeling I_{off} by $\exp((T_o/T)^n)$ it is reported [13] that both fitting parameters T_o and n decrease by decreasing the electric field.

However, in our model we introduce a reference temperature, T_{ref} such that $I_{off} \propto \exp((T_o(1/T - 1/T_{ref}))^n)$ where $n = 1/3$. Using this modification, although T_o still decreases by decreasing electric field the exponent fitting parameter n remains constant.

A factor R_T is thereby multiplied to eqn. (12) to capture the resistance's dependence on temperature

$$R_T = \exp\left(\left(\frac{T_o(T_{ref} - T)}{TT_{ref}}\right)^{1/3}\right) \tag{14}$$

Eqn. (14) holds as long as the condition $T \leq T_{ref}$ is satisfied. For validations with experiment in this paper, T_{ref} set at room temperature gives a good agreement. Hence, the off-current is

$$I_{off} = V_{ds}/R_q \tag{15}$$

To calculate the drain current away from the charge neutrality point, a root of the squares of both the off-current, I_{off} and the drift current, I_{ds*} [14].

$$I_{ds} = \sqrt{I_{off}^2 + I_{ds*}^2} \tag{16}$$

C. A Multi layer channel

In the case where the channel has more than two layers, the electric field will be determined by the excess charge density of the layer furthest from the top-gate. Thus eqn. (11) becomes

$$V_E = \sqrt{\frac{\varphi_{sm}^2 C_{qvar}(\varphi_{sm}) + \varphi_{s1}^2 C_{qvar}(\varphi_{s1})}{3C_b}} \tag{17}$$

Where m is the index number of the furthest layer. Equally, applying the temperature factor R_T in eqn. (14) to eqn. (17) results in

$$R_q = R_T R_s^0 \exp\left(\frac{V_E}{V_T}\right) \tag{18}$$

Eqn. (18) can be used to calculate the total drain current using both eqn. (15) and eqn. (16). For a semiconductor with appreciable bandgap and sharply defined energy bands, the off-current has a exponential relationship with T^{-1}. In this paper, the bandgap opening is estimated relative to the general Schottky barrier equation, $exp(\Delta E/2K_BT)$, where ΔE is the bandgap and K_B is the Boltzmann's constant.

$$\Delta E = 2K_BT\left(\left(\frac{T_o(T-T_{ref})}{TT_{ref}}\right)^{1/3} + \frac{V_E}{V_T}\right) \tag{19}$$

IV. Experimental Validation

The proposed model is validated for both a bilayer and a four-layer graphene FET against published experimental data.

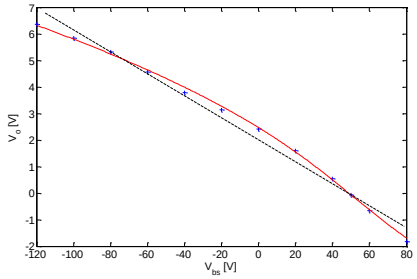
A. Bilayer FET validation

To validate the model against the experiment test cases A, B, C of three different transistors are used. For all three transistors a measured threshold voltage and the channel conductance dependence on V_{bs} is validated against the proposed model. Also a measured channel resistance dependence on temperature is validate against the model for test case C. Table I shows the model parameters of the transistors in all cases.

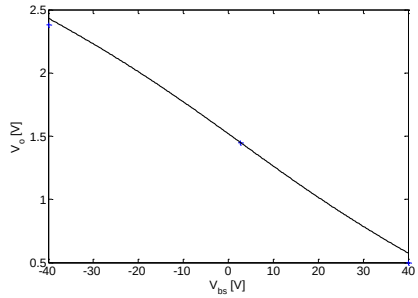
TABLE I
Model parameters for bilayer graphene FET

Model parameter	Test A	Test B	Test C
Ref	[10]	[11]	[13]
$L(\mu m)$	3	1	8
$W(\mu m)$	1.6	2.1	1
$t_{ox}(nm)$	10	15	15
$t_{il}(nm)$	0.335	0.335	0.335
k_2	3.9	3.9	3.9
$V_{gs}^0(V)$	-0.066	1.45	-0.195
$V_{bs}^0(V)$	50	2.7	0
$H_{sub}(nm)$	300	285	285
$R_s^0(K\Omega)$	8.08	12.88	1.23

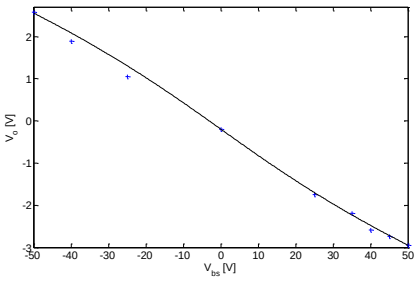
Test cases B transistor uses HfO_2 as the top-gate dielectric and SiO_2 as back-gate dielectric (k_2 is the dielectric constant), test case C uses only SiO_2 dielectrics and test case A uses a stack of HfO_2 on a derivative of polyhydroxystyrene. An interlayer separation, t_{il}, of $0.335nm$ between the top and bottom layer in the graphene channel is assumed. This is consistent with experiment and theory [20], [30], [31] for Bernal stacking structure of two layer graphene. Thus, C_o, has a capacitance of $2.64\mu Fcm^{-2}$ using a dielectric constant of 1.



(a) The threshold voltage, V_o, against V_{bs} for the Experimental data (+) [10], the proposed model (solid line) and the best fit of a straight line (dash lines)



(b) The threshold voltage, V_o, against V_{bs} for the Experimental data (+) [11], the proposed model (solid line)



(c) The threshold voltage, V_o, against V_{bs} for the Experimental data (+) [13] and the proposed model (solid line)

Fig. 3. The threshold voltage between the experimental data and the model for test case A, B and C respectively

For a given V_{bs} the threshold voltage is dependent on the device capacitances. Various threshold voltages are extracted from experimental data [10], [11], [13] and plotted against the model as shown in Fig. 3. Model parameters used can be seen in Table I. For all test cases as shown in Fig. 3(a), Fig. 3(c) and Fig. 3(b) a good fit against experimental data is attained with $C_e \approx 133nFcm^{-2}$, $C_e \approx 319nFcm^{-2}$ and $C_e \approx 130nFcm^{-2}$ respectively.

It has been reported that the threshold voltage against V_{bs} is a straight line graph with the slope being the ratio of the gate capacitances [11]. In comparison with a straight line that best fits the threshold voltages, Fig. 3(a) shows large deviations from the experimental data, which indicates that although a linear representation of the threshold voltage against V_{bs} is a quick way to estimate the threshold voltage it may not be sufficient in some cases. However, both a best fit straight line and the model give a good agreement against the experiment for Fig. 3(c). As such the technique presented here proves to be a consistent way of calculating the threshold voltage.

A threshold voltage model has equally been reported elsewhere [18]. There a fitting parameter is used along with a polynomial of the effective back-gate voltage, whereas in the proposed model the threshold voltage is calculated from the equivalent capacitance model and only C_e is adjusted to fit the experiment. As such C_e has a value smaller than the theoretically expected value based on its dielectric geometry and theoretical dielectric constant. However, there is a recent published report of a measured top-gate capacitance used on graphene channel appearing to be lower than the theoretically expected value [11].

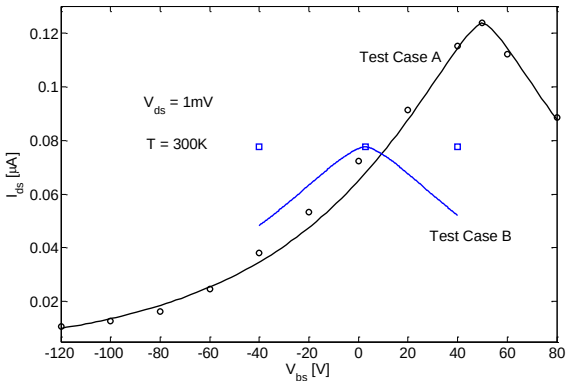


Fig. 4. A plot of the device off-current against V_{bs} for $V_{ds} = 1mV$ shows the proposed model against experimental data for both case A (experimental data (○) [10]) and case B (experimental data (□) [11]) at room temperature

Fig. 4 shows the channel conductance of V_o against V_{bs}. Both test case A and B are measured at room temperature with $V_{ds} = 1mV$.

The model shows a good agreement against experiment [10] for test case A with $V_T = 1.75V$, $C_e \approx 133nFcm^{-2}$, $T = 300K$, $n_0 = 1.2 \times 10^{16}m^{-2}$ and an intrinsic resistance, $R_s^0 = 8.08K\Omega$. The current characteristics depicts that the device is in intrinsic state for $V_{bs} = 50V$. At this value of V_{bs} the device has a zero bandgap. From the surface potential characteristics shown in Fig. 2 both φ_{s1} and φ_{s2} are both zero at the threshold voltage.

For test case B the model show a good agreement with the transistor measurements at $V_{bs} = 2.7$ using the following fitting parameters; $V_T = 2.0V$, $C_e \approx 319nFcm^{-2}$, $T = 300K$, $n_0 = 1.0 \times 10^{16}m^{-2}$ and an intrinsic resistance, $R_s^0 = 12.88K\Omega$. For the other two measured points there is

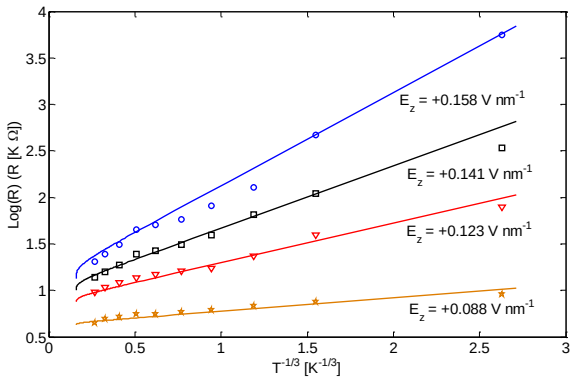


Fig. 5. A logarithm of the channel resistance against inverse cube root of the temperature for a range of perpendicular electric fields ($(V_{bs} - V_{gs})/(t_{ox} + H_{sub})$ where t_{ox} and H_{sub} are the thickness of the top-gate and back-gate dielectric). The experimental data [13] is plotted against the model shown in a solid line using parameters of test case C in table I

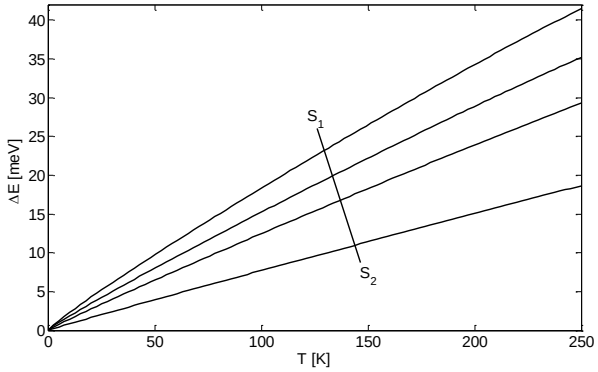


Fig. 6. Energy bandgap created by varying the temperature for the following electric fields $0.158Vnm^{-2}$, $0.141Vnm^{-2}$, $0.123Vnm^{-2}$ and $0.088Vnm^{-2}$ (top to bottom of cross section S_1 to S_2).

a deviation between the model and the measured data. The measured data shows an equal resistance for all three points, a behaviour consistent with single layer graphene FETs where there is no bandgap opening due to electric field.

For the device in test case C, Fig. 5 shows a temperature analysis of the device channel resistance for various electric fields. The proposed model shows a good agreement against experimental data using a reference temperature, $T_{ref} = 300K$, $C_e \approx 130nFcm^{-2}$, $V_T = 1.1V$, $n_0 = 1 \times 10^{16}m^{-2}$ and $R_s^0 = 1.23K\Omega$.

By decreasing the electric field the fitting parameter T_o equally decreases. T_o relates with surface potential at the threshold voltage by a phenomenological equation.

$$T_o = T_\alpha \exp\left(\frac{\eta\varphi_{s2}}{\varphi_\alpha}\right) \tag{20}$$

where η, T_α and φ_α are characteristic, temperature and voltage fitting constants respectively.

Eqn. 20 has the following values, $1.0K$, $0.3K$, $0.076K$ and $0.003K$ corresponding to an electric field ($(V_{bs} - V_{gs})/(t_{ox} +$

H_{sub}) where t_{ox} and H_{sub} are the thickness of the top-gate and back-gate dielectric) of $0.158Vnm^{-2}$, $0.141Vnm^{-2}$, $0.123Vnm^{-2}$ and $0.088Vnm^{-2}$ respectively. As the device tends towards its intrinsic state the T_o tends towards zero. Equally, the channel resistance temperature dependence increases by increasing electric field.

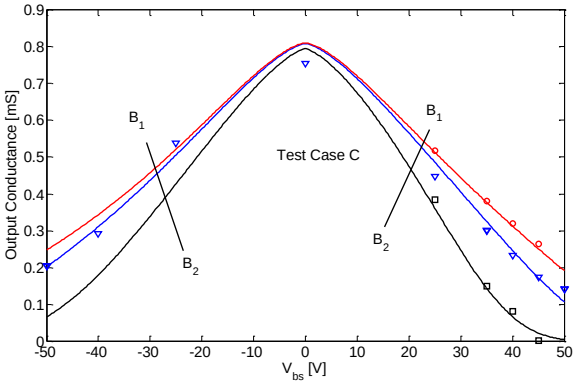


Fig. 7. A plot of the device charge neutrality conductance against V_{bs} for test case C. cross-section B_1 to B_2 (top to bottom) shows the proposed model against experimental data [13] at a temperature of 53K (○), 4.2K (▽) and 0.055K (□)

Fig. 7 the measured channel conductance at threshold voltage against V_{bs} is validated against the proposed model for test case C. The validation is done for three operating temperatures, 53K, 4.2K and 0.055K respectively. The model show a good agreement against measured data for all operating temperatures. Fitting parameters used for the electric field relation to temperature in eqn. (20) are, $T_\alpha = 6 \times 10^{-7}K$ and $\varphi_\alpha = 0.0086V$. For positive values of φ_{s2}, $\eta = 1$ gives a good fit and for negative values of φ_{s2}, $\eta = 0.8$ gives a good fit.

In mapping the modeling equation against that of the Schottky barrier general equation, an estimate of the bandgap created is deduced. Fig. 6 shows an increasing bandgap by increasing temperature, as well as a bandgap of less than $50meV$ at room temperature which confirms the dependence of the resistance on the $\exp(T^{-1/3})$ factor. The rising bandgap against increase in temperature accounts for why the transistor shows a small current ratio between operating at room temperature and low temperatures. Between $300K$ and $53K$ only a very slight increase in the maximum resistance is observed especially under low electric field. It is expected that towards $0K$ the device bandgap approaches zero.

The output conductance, g_{ds}, is defined as the variation in the drain current for a small variation in the drain-source voltage while keeping the gate-source voltage constant. Model parameters used in test case B in Table I show a good agreement against experimental data for $C_e \approx 319nFcm^{-2}$, $R_s^0 \approx 12.88K\Omega$ and $n_0 = 1 \times 10^{16}m^{-2}$.

In Fig. 8 g_{ds} is plotted for a range of V_{gs} with $V_{bs} = 40V$ and $V_{ds} = 0V$. For the best fit against the experimental data, $R_c = 1000\Omega$ and $\mu = 3000cm^2/Vs$ for hole conduction and

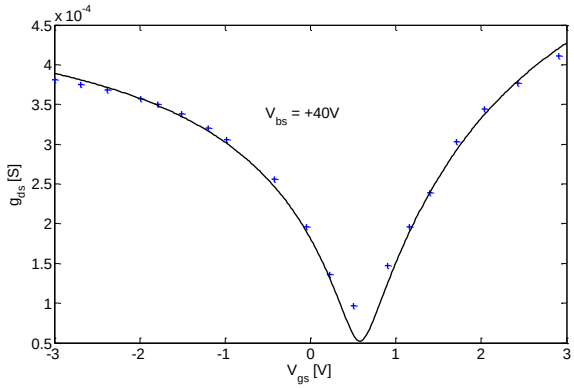


Fig. 8. Characteristics of the channel output conductance against the top-gate voltage for $V_{bs} = 40V$(Experimental data(+) [11], proposed model(–))

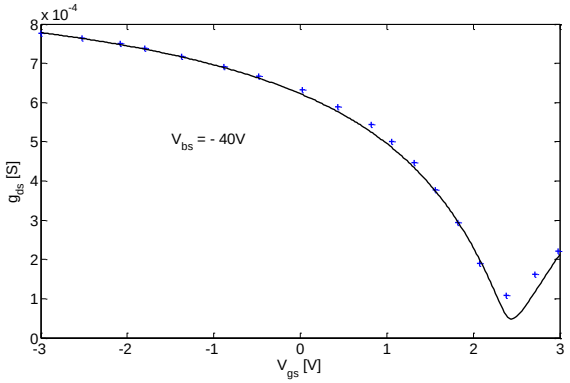


Fig. 9. Characteristics of the channel output conductance against the top-gate voltage for $V_{bs} = -40V$(Experimental data(+) [11], proposed model(–))

$R_c = 700\Omega$ and $\mu = 2700cm^2/Vs$ for electron conduction.

In Fig. 9 g_{ds} is plotted for a range of V_{gs} with V_{bs} = -40V and $V_{ds} = 0V$. For the best fit against the experimental data, $R_c = 515\Omega$ and $\mu = 4400cm^2/Vs$ for hole conduction, and $R_c = 300\Omega$ and $\mu = 2700cm^2/Vs$ for electron conduction.

B. four-layer graphene validation

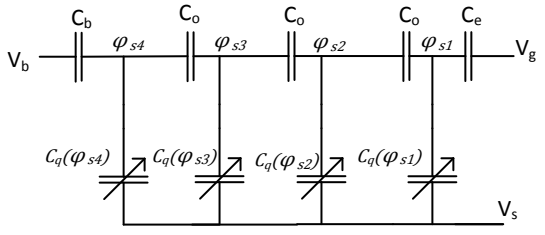


Fig. 10. Capacitance model for a four-layer graphene channel

This paper shows the model for both a bilayer and a four layer graphene FET. To extend the model to a many layer graphene transistor each layer is modeled by a quantum

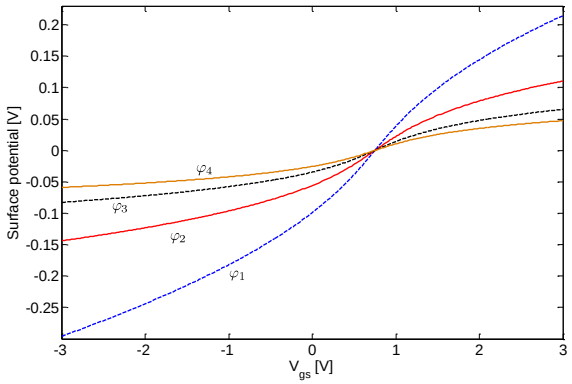


Fig. 11. Surface potential of the respective layers in a four-layered graphene channel for a sweep of the top-gate voltage while maintaining the back-gate voltage at the back-gate-to-source voltage at the Dirac point

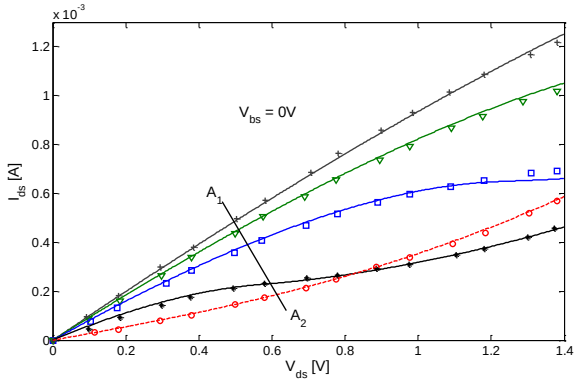


Fig. 12. Experimental data [12] versus the proposed model (–) for negative I_{ds} vs negative V_{ds} characteristics at V_{bs}= 0V. V_{ds} is varied from 0 to -1.4V for top-gate voltages of -1.25V, -0.75V, -0.25V , 0.25V and 0.75V (from top to bottom between cross-section A_1 and A_2)

capacitance C_q and separated from the next layer by an interlayer capacitance, C_o.

In the capacitance model for a four-layer graphene channel shown in Fig. 10, it is assumed that all layers are equally spaced with an interlayer thickness, t_{il}, of $0.355nm$.

TABLE II
MODEL PARAMETERS FOR FOUR-LAYER GRAPHENE FET

Model parameter	Parameter value
Ref	[12]
$L(\mu m)$	10
$W(\mu m)$	5
$t_{ox}(nm)$	40
$t_{il}(nm)$	0.355
k_1	17.0
k_2	3.9
$V_{gs}^0(V)$	0.75
$V_{bs}^0(V)$	0
$H_{sub}(nm)$	500
$R_s^0(K\Omega)$	3.7

Using model parameters in Table II for a DC sweep of the top-gate voltage Fig. 11 shows the surface potential of each of the four-layers. In this case the back-gate voltage is biased at the back-gate-to-source Dirac point voltage, such that there is a zero bandgap at the threshold voltage. Therefore, the surface potential of all layers is zero at the threshold voltage.

Fig. 12 shows the variation of the drain current against changes in the drain voltage. The model is validated against experimental data [12] for $V_{bs} = 0V$ and V_{gs} of -1.25V, -0.75V, -0.25V , 0.25V and 0.75V. Parameters shown in Table II gives a good fit against experiment using the following fitting parameters, $n_0 = 0.5 \times 10^{16} m^{-2}$, $V_T = 3.0V$, $C_e \approx 376nFcm^{-2}$, $R_c = 390\Omega$, $E_c = 15KV/cm$, hole carrier mobility $\mu = 13,000cm^2/V.s$ and alternate carrier mobility $\mu_n = 2900cm^2/V.s$. The dielectric constant of HfO_2 used is 17 [32].

Fig. 13 shows the variation of the drain current against changes in the top-gate for $V_{ds} = 0.1V$. The model gives the best fit against experimental data [12] for $R_c = 290\Omega$ and

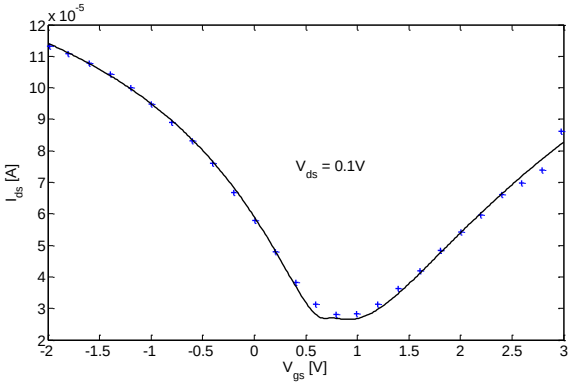


Fig. 13. Characteristics of the channel Drain current against the top-gate voltage for $V_{ds} = 0.1V$(Experimental data(+) [12], proposed model(–))

$\mu = 7000cm^2/V.s$ for hole conduction and $R_c = 200\Omega$ and $\mu = 3200cm^2/V.s$ for electron conduction.

V. CONCLUSION

In this paper we present a circuit-level model that describes a dual-gate multi-layered graphene transistor. The model has been verified against published experimental data [10], [11], [12], [13] for both a bilayer and a four-layered graphene transistor and shows a good agreement. The validation against experimental data was done for both the channel output conductance, the drain current characteristics for changes in the drain voltage and the device off-current for a range of back-gate voltages.

In the proposed model, surface potentials of all the layers are calculated for the bilayer and four-layer transistor. Each layer is represented by a quantum capacitance that is a function of its surface potential.

Equally, the model uses the proposed equivalent circuit in calculating the threshold voltage. The model shows a good agreement for extracted experimental data of the threshold voltage for a range of V_{bs}. It is observed that although linear

function of V_{bs} with the ratio of the gate capacitances being the slope provides a quick method of evaluating the threshold it may be insufficient in some cases. The method presented here proves to be accurate for the cases validated. By this method, the top-gate capacitance is also numerically calculated as it is the only parameter used to fit the model against experiment. Supported by a recent published report [11] of a measured top-gate capacitance being smaller than the expected theoretical value, this technique proves a suitable way of calculating the top-gate capacitance.

The proposed model implements the transistor as having a channel resistance which is modulated by the gate bias using charge density and an off-current resistance in parallel to this resistance which shows an exponential relationship with the surface potential. The off-current resistance is the maximum channel resistance and it determines the device off-current. The model's estimated off-current shows a very good agreement against experimental data [10], [13].

At a constant temperature the channel resistance shows a exponential relationship with the surface potential by varying the perpendicular electric field. The fitting parameter used ranged between $1V$ and $3V$ for both the bilayer and the four layer channel.

For a constant electric field and a varying the operating temperature, the proposed model uses an $\exp(T^{-1/3})$ temperature dependence of the channel resistance. The model uses a fitting parameter, T_o, which decreases by decreasing the electric field. Also an increase in the channel resistance to temperature dependence is observed for an increase in the electric field.

Using the Schottky barrier general equation, the proposed model estimates the amount of bandgap opening for a given back-gate voltage. The results agree with known theory of a bandgap opening by the presence of a perpendicular electric field. Also the model reveals an increase in the bandgap by increasing the operating temperature, whereby a zero bandgap is estimated towards 0K. An increasing bandgap account for the small current ratio by varying the temperature. From $300K$ to $52K$ the device shows only a slight increase in resistance.

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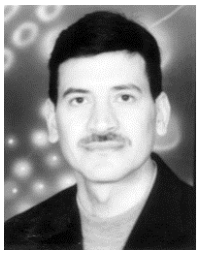

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