A novel top-down fabrication process for $Ge_2Sb_2Te_5$phase change material nanowires

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***Abstract*—A novel e-beam free, top-down spacer etch process was used to fabricate sub-hundred nanometer $Ge_2Sb_2Te_5$ phase change nanowires. Naowires with a cross-section dimension of 50 nm × 100 nm (width × height) were obtained and phase change functionality demonstrated.**

Keywords-phase change materials; nanowire; spacer etch

I. INTRODUCTION

Phase change random access memory is considered as one of the most promising candidates for next generation non-volatile solid-state memory due to its outstanding performance, which includes non-volatility, high scalability, high speed, low power, low cost, and compatibility with CMOS process [1].

Nanowires-based technology is a powerful approach to assemble memory devices in ultra-small scales for their sub-lithographic size and unique geometry. It provides the potential for high scaled phase change memory devices and multilevel memory applications. Single-crystal nanowires based on different phase change materials such as GeTe [2-6],GeSb [7], $Ge_2Sb_2Te_5$ [8-11], $Ge_1Sb_2Te_4$ [12] and In_2Se_3 [13] have been previously synthesized and demonstrated a nano-second level switching time at very low powers, suggesting that the nanowires could be ideal for data storage devices.

Up to now, most of the methods used to synthesis phase change nanowires are based on bottom-up technology such as thermal evaporation method under vapor-liquid-solid (VLS) mechanism [3, 9, 10, 12, 14] and metal organic chemical vapor deposition (MOCVD) [13]. However, this technology suffers from, disadvantages such as poor nanowire diameter/position control, non-COMS-compatibility and poor reproducibility. On the contrary, a top-down technology offers better control over the fabrication process and is highly reproducible and CMOS-compatible. The top-down fabrication is also more favorable in manufacturing. The conventional way for top-down nanowire fabrication by e-beam lithography induces a high cost with low efficiency. In this work, we propose to use a spacer etch process to fabricate phase change nanowires. This spacer etch is a novel technique and can be used as a low-cost alternative to e-beam lithography for sub-hundred nanometre nanowire fabrication. Unlike bottom-up technology, it is compatible with current CMOS process and the geometry and location of the nanowires can be precisely controlled.

II. EXPERIMENTAL SECTION

The overall fabrication processes is described in Fig. 1(a)-1(e). A 400 nm thermal SiO_2 was first grown on a pre-cleaned Si wafer [Fig. 1(a)]. This layer was then patterned with a photolithography process using a pre-designed mask [Fig.1(b)] and was followed by a reactive ion etching of the SiO_2 to create a trench with a depth of 100 nm [Fig. 1(c)]. The photolithography was carried out using an EVG620TB with a

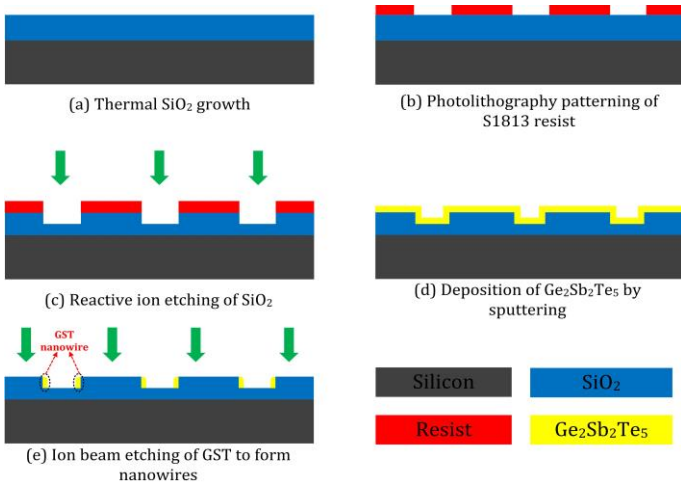

Figure 1. Fabrication process of spacer etch $Ge_2Sb_2Te_5$ nanowire.

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positive resist S1813. The etching was performed by a RIE80+with CHF_3 and Ar.

After resist stripping, an amorphous $Ge_2Sb_2Te_5$(GST) layer with a thickness of 100 nm was deposited on the etched SiO_2 by RF sputtering in a Nano 38 system (Kurt J. Lesker, USA) from targets of the composition $Ge_2Sb_2Te_5$ at a power of 45W [Fig. 1(d)]. The SiO_2 trenches created in the previous process serve as a step for the following spacer etch. The GST nanowire can then be obtained by an anisotropic etching process. Ion beam etching was chosen in this work to etch the GST as it provides high uniformity and repeatability. The nature of the process and its non-selectivity results in the GST at the SiO_2 step forming the desired nanowire [Fig. 1(f)]. In this work, the nanowires were formed using Ionfab ion beam etcher by Oxford Instrument Plasma Technology. The etch condition was set to with a RF power of 700 W, a beam current of 300 mA, beam voltage of 500 V and an acceleration voltage of 400 V.

To characterize the electrical behaviour of the nanowire, TiN electrodes were deposited and patterned on the two sides of the SiO_2 trench by photolithography and lift-off processes using a negative AZ2070 resist. The electrical characterization was carried out with a Cascade probe station and Agilent B1500A semiconductor device analyser.

III. Results and Discussion

Fig. 2(a) shows a cross-section SEM image of a sample after GST film deposition over the SiO_2 step. The GST layer can be identified on top of the thermal oxide layer and is about 110 nm in thickness. The GST film thickness on the sidewall was measured to be 50 nm and is reduced due to the non-conformity of the sputtering process. This region of the GST will eventually form the spacer nanowire after etching.

Fig. 2(b) shows the cross-section SEM image of the sample after 30 seconds etch. A clear decrease of the GST layer thickness can be observed. Additional etching of 20 seconds further decreased the film thickness while the GST along the sidewall remained untouched as shown in Fig.2(c).After another 30 seconds etch, the GST on the planar surface has been completely removed [Fig. 2(d)], leaving a GST nanowire along the SiO_2 step. The dimension of the nanowire was measured to be 50 nm × 100 nm (width × height) which match the GST film thickness on the sidewall and the SiO_2 trench depth, respectively, indicating that the nanowire dimensions can be precisely controlled by the fabrication process. The nanowire height is determined by the height of SiO_2 step and can be controlled during the RIE process. The nanowire width is tuneable through the thickness of the deposited GST layer. The nanowire length is determined by the length of SiO_2 trench. In an actual device, the active nanowire length is then determined by the distance between two electrodes.

The continuity of the nanowires was investigated by observation under optical microscope. Fig. 3 shows the optical Nomarski micrographs of spacer etched GST nanowires. A clear contrast can be observed between the SiO_2trenchs and the GST nanowires adjacent to their boundaries. All nanowires appear to be continuous with no evidence of breaks.

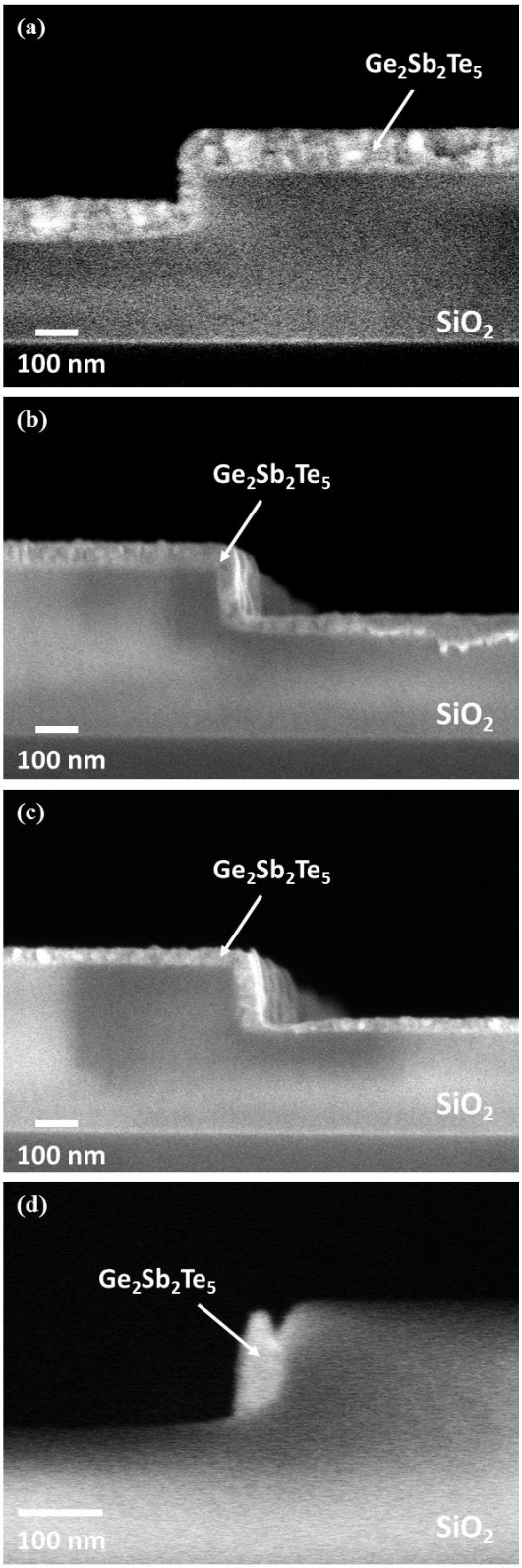

Figure 2.Cross-section SEM images of samples (a) before GST spacer etch, (b) after a 30 seconds etch, (c) after a 50 seconds etch and (d) after a 80 seconds etch.

Fig. 4(a) shows the top-view SEM of a nanowire device which contains 16 GST nanowires with an active length of 16 μm. Fig. 4(b) shows zoomed in SEM image of the device where the GST nanowire can be clearly observed. The width of the nanowire measured from this top-view SEM is 48 nm which matches the data obtained from the cross-section SEM. It is worth mentioning that the nanowire shows some roughness which is attributed to the roughness of the SiO_2 trench. This could be further improved through the photolithography process.

The potential degradation of the GST material during the ion beam etching process was monitored by electrical characterizations on devices. The devices were first measured in amorphous (as-deposited) state and then in crystalline state after annealing them in N_2 atmosphere at 200℃ (above the crystalline temperature of GST) for 5 minutes. The I-V characteristic is shown in Fig. 5 where a resistance ratio of 1.60×10^{3} can be observed between the amorphous and crystalline states. The resistivities were measured to be 0.54 Ω·m for the amorphous state and 3.37×10^{-4} Ω·m for the crystalline state. Both data are in a reasonable agreement with the references [15], indicating that the property of GST has not deteriorated during etching.

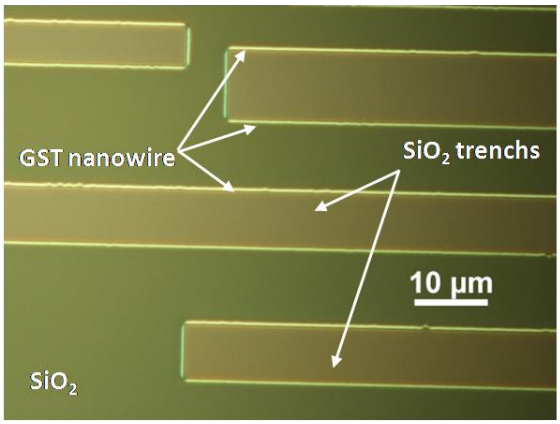

Figure 3.Nomarski optical micrograph of spacer etch GST nanowire.

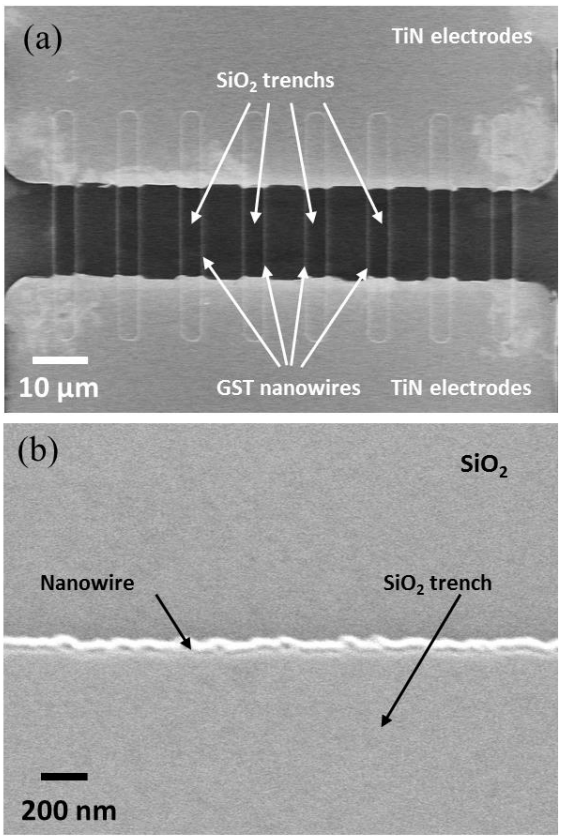

Figure 4. Top-view SEM images of (a) a spacer etch GST nanowire device which contains 16 GST nanowires with an active length of 16 μm and (b) a single spacer etch GST nanowire.

IV. Conclusion

In this work, a novel e-beam free top-down process to fabricate GST nanowires is presented. Sub-hundred nanometer GST nanowires have been obtained through an anisotropic ion beam etching of a GST layer deposited on SiO_2 trenches. The dimensions (height, width and length) of the nanowire can be precisely controlled through the fabrication process. The phase change properties of the GST material remains after fabrication as evidence by electrical measurement.

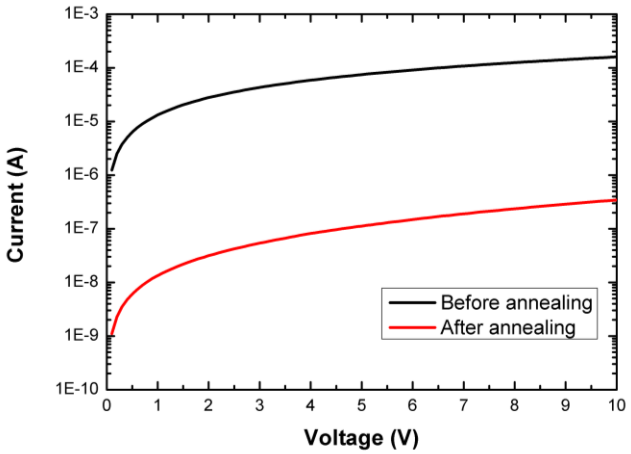

Figure 5. I-V characteristic of spacer etch GST nanowire before and after annealing.

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