Effects of Surface Passivation on Top-Down ZnO Nanowire Transistors

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Introduction: ZnO nanowire field effect transistors (NWFETs) can be fabricated using bottom-up or top-down approaches. Even though bottom-up devices may have better electrical characteristics; their orientation, dimensions and addressability are difficult to achieve. Therefore, top-down fabrication method is favorable for producing controlled nanowire dimensions and location. In a back gate FET configuration, the nanowire channel is exposed to the atmospheric environment. The surface charges between insulator, air and nanowire channel can deplete the channel surface to lower the output drain current and affect the electrical performances such as threshold shift – making the device to behave like enhancement mode [2]. This has also been observed in silicon-based nanowire FET [3]. It has been shown that passivation of ZnO TFT and bottom-up ZnO nanowire can improve electrical performance such as transconductance and mobility [4]. However, there is still little work done in the electrical performance of top-down spacer fabrication method ZnO nanowire under unpassivated and passivated conditions. In this work, we will investigate the effect of surface passivation of ZnO nanowire channel with Al_2O_3 using atomic layer deposition method and the electrical characteristics comparison to an unpassivated FET device.

Fabrication: The ZnO NWFET is fabricated using our top-down spacer method [2], [3], which uses standard photolithography; remote plasma atomic layer deposition (RPALD) and anisotropic dry etch. RPALD process is conducted at 900 cycles, with each cycle consisting of 50 ms diethyl zinc (DEZ) precursor dose time, a 4 s Ar purge , a 2.65 s oxygen plasma, and a final 4 s Ar purge. The deposition temperature is done at 190 ºC and the RF power and pressure were set at 100 W and 15 mtorr respectively. The deposited ZnO layer thickness is 76 nm and was measured using an ellipsometer. The natural n-type carrier concentration is 1×10^{18} cm^{-3} and measured using a Hall Effect system. We use anisotropic inductively coupled plasma (ICP) etcher and CHF_3 gas chemistry to remove the ZnO layer. Figure 1 (a) shows the top view microscope image of the ZnO NWFET with the source drain connection; and Figure 1(b) shows the cross section scanning electron micrograph of the ZnO nanowire. Then thermal ALD is used to deposit a layer of 18 nm thick Al_2O_3 over the ZnO nanowires at temperature of 200 ºC. The aluminum layer is formed using trimethyl-aluminum (TMA) precursor and distilled ionized water is used for the oxidation process. Finally, aluminum lift-off process is used to form ohmic contact at the source and drain region. The fabricated NWFETs have channel length of 8.6 µm, thickness of 80 nm and width of 20 nm. The electrical I-V characterization of the ZnO NWFETs is done using Agilent B1500A semiconductor parametric analyzer.

Results: Figure 2(a) shows the I_dV_d characteristics for un-passivated device with output drain current I_d = 0.18 µA; whereas the passivated device has I_d = 0.4 µA when mesured at V_d = 1 V and V_g = 20 V. Figure 2(b) shows that threshold voltage shift before and after passivation from V_T = 6.5 V to V_T = -10 V. The unpassivated NWFET initially exhibits enhancement mode operation and after passivation it reverts to the expected depletion mode, since the ZnO n-channel has a concentration of 1×10^{18} cm^{-3}. The I_d increase after passivation is confirmed analytically using the linear region equation $I_d = C_{NW}\,\mu_{FE}\,(V_g - V_T)V_D / L^2$, [5], where the ($C_{NW}$ = 0.92 fF) is considered to be the capacitance of the dual nanowire, L is the length of the channel and μ_{FE} is the field effect mobility. The extracted field effect mobility from the transconductance before and after passivation is 18.0 cm^2/V.s and 15.0 cm^2/V.s respectively. The passivation process has improved the output drain current and lowers the threshold voltage to the expected depletion mode operation. Further work will includes effect of passivation layer against threshold voltage and drain current output and investigation of subthreshold characteristics due to surface charges and roughness. The top-down passivated ZnO NWFET has the potential application biosensing application.

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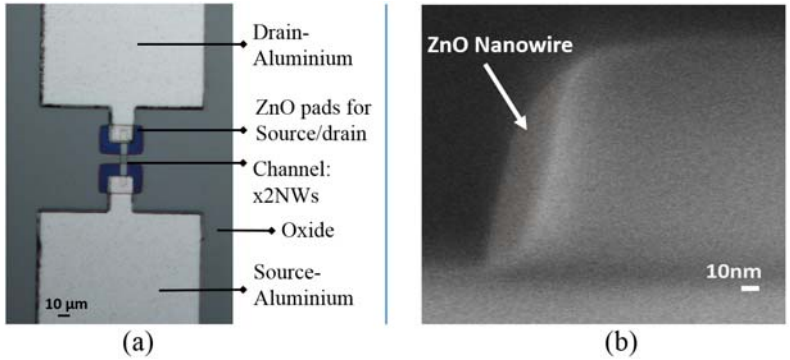

Figure 1: NWFET device structure (a) schematic of fabricated device (b) Cross-sectional SEM image of ZnO nanowire.

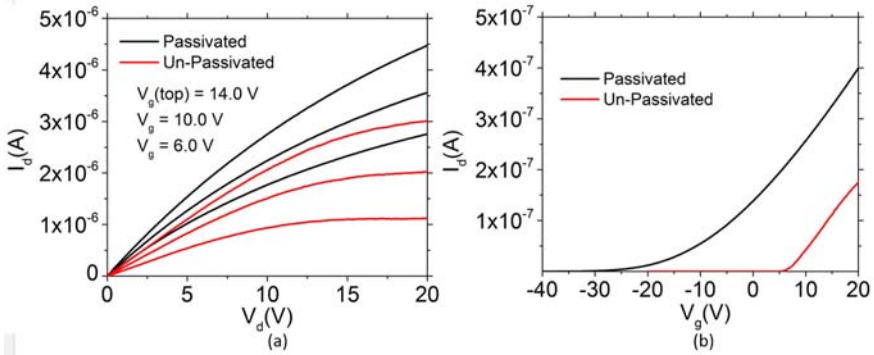

Figure 2: Passivated verses un-passivated (a) I_dV_d (b) I_dV_g characteristics with V_d = 1.0 V.