Fabrication and Characterisation of Suspended Oxidised Silicon Nanowire Channels for Near Zero Leakage Logic Switches

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Background

Leakage current in complementary metal-oxide-semiconductor (CMOS) technology below the 45nm feature scale is expected to lead to increased power dissipation. To maintain previous performance increase rates, metal-oxide-semiconductor field effect transistor (MOSFET) technology scaling is still continuing. Due to increased power dissipation, MOSFET fabrication is driving towards innovations in materials and new device structures for logic circuits [1]. In this paper, a suspended silicon nanowire very low leakage current switch fabrication process is presented for potential integration with existing CMOS processes. Device I-V characteristics demonstrate near zero leakage current and an on/off ratio in excess of 10^5.

Method

In this work, operation of the suspended silicon nanowire switch achieves very low leakage current and high on/off ratio. This is owing to the triple layer SiO_2/air/SiO_2 insulation between source-drain and double side gate design. This configuration is made possible due to a double suspension fabrication process. Electrostatic switch-off is illustrated in fig. 1b, and electromechanical pull-in and destruction are demonstrated by ramping a single side gate voltage from 0 V to 75 V (fig. 2). The devices are fabricated with silicon-on-insulator (SOI) substrates. Device layer is phosphorus doped, with a concentration of $\sim 1 \times 10^{19}\, cm^{-3}$. Nanoscale features are patterned using hydrogen silsesquioxane electron beam lithography to achieve channel widths of around 42 nm on 50 nm thickness SOI. Reactive ion etching (RIE) is used to etch device features using sulphur hexafluoride (SF_6) and oxygen (O_2) chemistry. The silicon nanowire channel is suspended using hydrofluoric (HF) acid vapour phase under-etching of the 200 nm thick buried oxide (BOX) layer. The device is insulated by growing a 12 nm thermal oxide layer on the channel and two side gates. ~600 nm thick sacrificial layer of amorphous silicon (a-Si) is then deposited by plasma enhanced chemical vapour deposition (PECVD) to protect the suspended silicon nanowire channel during metallisation. Aluminium contact pads are evaporated onto photo-lithographically patterned AZ2070 photoresist and subsequently a lift-off procedure is performed overnight using n-methyl-2-pyrrolidinone (NMP). The final stage is then to re-release the nanowire for suspension, this is realised using a highly selective cycled xenon difluoride (XeF_2) vapour phase etch of the a-Si layer [2].

Results

Fig. 1b shows the nanowire threshold voltage of -1.8 V under drain voltage of 0.1 V. Electrostatic switch-off shows depletion mode characteristics of the device. At -3.5 V the channel current is 8.56 pA, resulting in an on/off ratio in excess of 10^5. Electrical isolation is maintained until an individual gate voltage of 39 V, when electromechanical pull-in occurs resulting in complete device destruction, also creating a conduction path through both ~12 nm oxide layers between the source and gate electrodes (inset fig. 2).

Conclusions

Suspended silicon nanowire devices with 42 nm wide channels have been fabricated and tested. Electrical isolation results in near zero leakage current operation. Electromechanical pull-in and destruction tests have been performed to measure maximum operational gate voltage range to the point of device destruction.

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[1] ITRS 2013 Edition, *Emerging Research Devices Chapter*. 2013
[2] Kourosh Khosraviani and Albert M Leung 2009 *J. Micromech. Microeng.* **19** 045007

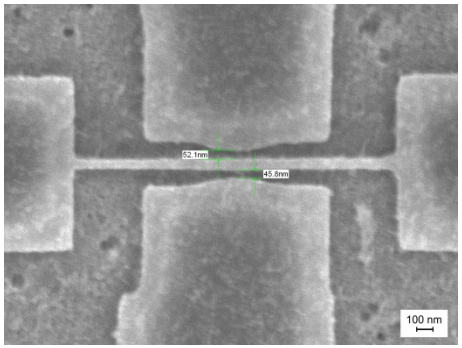

Fig. 1a: Scanning electron micrograph of suspended silicon nanowire conducting channel with 46 nm and 52 nm air gaps between channel and gate electrodes

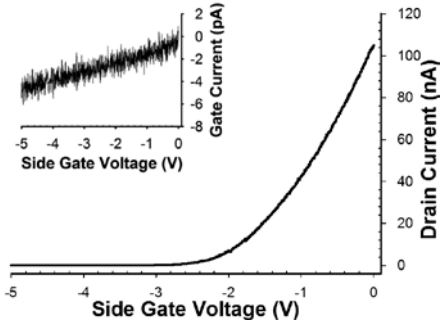

Fig. 1b: 0 V to -5 V gate voltage showing source-drain current electrostatic switch-off (main) and very low gate leakage current (inset). Source-drain voltage held at 0.1 V.

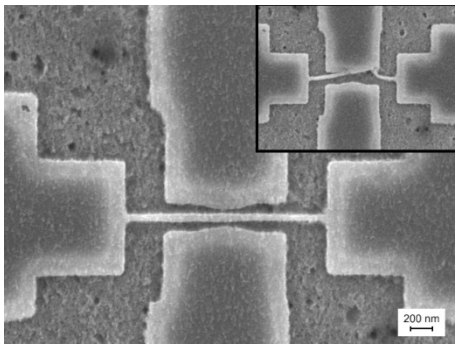

Fig. 2a: Scanning electron micrographs of suspended silicon nanowire before pull-in/destruction testing (main) and after (inset)

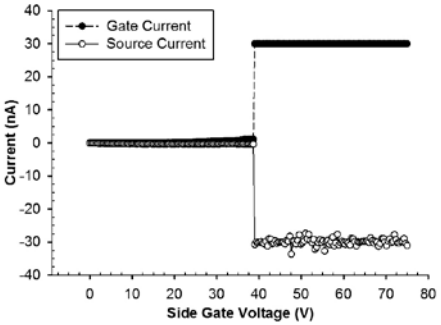

Fig. 2b: I-V behavior of the suspended silicon nanowire during mechanical destruction test. The current is limited to 30 nA. Electromechanical pull-in is clearly observed.