Silicon carrier depletion modulator with 10Gbit/s driver realized in high-performance photonic BiCMOS

D. J. Thomson[1], H. Porte[2], B. Goll[3], D. Knoll[4], S. Lischke[4], F. Y. Gardes[1], Y. Hu[1], G. T. Reed[1], H. Zimmermann[3], L. Zimmermann[4]

1 - Optoelectronics Research Centre, University of Southampton, Southampton, Hampshire, SO17 1BJ, UK
2 - PHOTLINE Technologies, ZI Les Tilleroyes – Trépillot, 16 rue Auguste Jouchoux, 25000 Besançon - France
3 - Vienna University of Technology, EMCE, Gußhausstr. 25/354, A-1040 Vienna, Austria
4 - IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

d.thomson@soton.ac.uk

Abstract max 150 (150) words:

Optical modulators based upon carrier depletion have proven to be an effective method to achieve high speed operation in silicon. However, when incorporated into Mach-Zehnder Interferometer structures they require electronic driver amplifiers to provide peak to peak drive voltages of a few volts in order to achieve a large extinction ratio. For minimal performance degradation caused by the electrical connection between the driver and the modulator monolithic integration in the front end of the process is the preferred integration route. The formation of electronic driver amplifiers in BiCMOS is advantageous over CMOS in terms of achievable performance versus cost. In this work the first monolithic photonic integration in the electronic front-end of a high-performance BiCMOS technology process is demonstrated. Modulation at 10Gbit/s is demonstrated with an extinction ratio >8dB. The potential scalability of both the silicon photonic and BiCMOS elements make this technology an attractive prospect for the future.

Abstract max 500 (420) words:

Optical modulators based upon the plasma dispersion effect have proven to be an effective method to monolithically achieve high speed modulation in silicon. More specifically those which use carrier depletion in a reverse bias pn junction positioned to interact with the propagating light provide the best trade-off of performance and fabrication simplicity. Mach-Zehnder Interferometer versions of these devices which incorporate carrier depletion phase modulators into both waveguide arms offer a wide optical bandwidth, thermal stability, low chirp, reasonable tolerance to fabrication variations and no photon cavity lifetime limitation as compared to resonant based devices. Such modulators require electronic driver amplifiers to provide peak to peak drive voltages of a few volts in order to achieve a large extinction ratio from devices on the order of a mm in length. The formation of electronic driver amplifiers in BiCMOS is advantageous over CMOS in terms of achievable performance versus cost. BiCMOS technology achieves a higher figure of merit (maximum oscillation frequency × breakdown voltage) compared to CMOS and also requires lower specification lithography, which is also capable of forming the photonic elements, leading to high performance at lower chip cost. The integration of the optical modulator and the drive amplifier is a process required to fulfil a number of applications. Different methods for integration have been proposed and demonstrated, however, the frontend integration of silicon photonics and electronics which involves the fabrication of electronic components such as transistors and photonic components such as optical waveguides side by side on the same substrate, allows for higher performances to be reached over alternative approaches since degradation due to bond pads and bond wires is avoided. In this work the first monolithic photonic integration in the electronic frontend of a high-performance BiCMOS technology is demonstrated combining the carrier depletion MZI modulator and push-pull driver amplifier. Photonic SOI is not suitable for BiCMOS devices due to the incompatibility with the collector fabrication and the higher thermal resistance compared to the bulk silicon normally used in BiCMOS. A method for producing localised regions of photonic SOI embedded in a bulk silicon substrate was therefore developed to

enable the frontend integration of photonics and BiCMOS electronics. Tuning of the modulator operating point is achievable using a phase tuning element also based upon carrier depletion. Modulation at 10 Gbit/s is demonstrated with an extinction ratio of approximately 8dB at the quadrature operating point. The total on chip optical loss is 13dB which can be reduced dramatically through design improvements which are described within the text.

Keywords: SiGe, Integration, Modulator, Silicon modulator, Driver, BiCMOS, Front end, Silicon photonics

1. Introduction

Optical modulators formed in the silicon photonics platform have attracted significant research interest worldwide owing to the motivation of silicon photonics in low cost photonic component/circuit fabrication and the possibility to directly integrate with electronics. Standalone devices have gone through a period of rapid development in the previous decade with device speeds now exceeding 40Gbit/s [1-3]. There are several different types of silicon optical modulator that have demonstrated a high performance. One approach has involved the incorporation of other materials onto the silicon waveguide including III-V based compounds [4], germanium [5], graphene [6] and polymer [7]. The most common high performance devices are based upon the plasma dispersion effect and use the depletion of free carriers from a pn junction positioned to interact with the propagating light in order to achieve modulation [8]. To convert between phase and intensity modulation carrier depletion phase modulators are typically incorporated into Mach-Zehnder Interferometer (MZI) structures in order to exhibit a wide optical bandwidth, thermal stability, low chirp, reasonable tolerance to fabrication variations and no photon cavity lifetime limitation as compared to resonant based devices. Such modulators typically require electronic driver amplifiers to provide peak to peak drive voltages on the order of a few volts in order to achieve a large extinction ratio. The electrical connections used between the driver and the modulator can significantly degrade performance at high speed therefore motivating the integration of these components in close proximity.

Different integration routes are possible including wire bonding, flip chip bonding and monolithic integration. The bond wires and bond pads used in the first two of these approaches can introduce parasitics which can again degrade and limit the overall performance of the device. Monolithic photonic integration in the frontend of a silicon IC technology involves fabricating photonic devices such as modulators side by side with electronic elements such as transistors. This approach allows for the shortest possible electric interconnects between the electronic and photonic elements minimising any performance degradation. The electrical connections can also be produced with high accuracy minimising any time synchronisation issues of the drive signals to the two MZI arms. A further motivation for this integration route are the prospects of sharing process steps of the modulator and electronics particularly in the metallisation stages which can reduce the overall cost of fabrication. Frontend integration of photonics and electronics has been pursued by several groups, however, this has been based on CMOS (complementary metal oxide semiconductor) technologies [9-12]. In this work a new approach to frontend photonic electronic integration is demonstrated with the integration of a MZI based modulator in the frontend of a high performance BiCMOS (bipolar and CMOS) technology. Photonic SOI is not suitable for BiCMOS devices due to the incompatibility with the collector fabrication and the higher thermal resistance compared to the bulk silicon normally used in BiCMOS. A method for producing localised regions of photonic SOI embedded in a bulk silicon substrate was therefore developed to enable the frontend integration of photonics and BiCMOS electronics [13].

The advantages of BiCMOS are in achievable performance versus cost. High performance BiCMOS is commonly used in broadband applications, especially high-speed photonics. The key figure of merit is maximum oscillation frequency × breakdown voltage. This figure of merit of bipolar transistors is higher than in comparable CMOS processes, so there is increased design flexibility and overall simpler analogue design at high speed (compared to CMOS with issues of leakage, transistor nonlinearity and low supply voltage). On the other hand, chip area in a highly scaled CMOS process

is very costly, which prohibits frontend integration of larger photonic devices in such technologies. This tradeoff is much less critical for high performance BiCMOS, which only requires 248nm lithography instead of 193nm lithography (as used for highly scaled CMOS). Photonic BiCMOS is thus particularly interesting for broadband applications without the very large volume behind advanced CMOS. In this paper experimental results from a first fabrication run of the co-integration of a BiCMOS foundry technology (SG25H3) to integrate a SiGe complementary output RF driver amplifier with a dual-drive carrier depletion Mach-Zehnder modulator is presented. 10Gbit/s modulation is achieved from a MZI with 2mm long phase modulators in either arm with an extinction ratio in excess of 8dB.

2. Driver design and Technology

The electronic driver is designed in IHP SG25H3 technology to drive the modulator in push-pull configuration. The schematic of the driver and the simulated eye diagrams at a data rate of 10Gb/s are shown in figure 1.

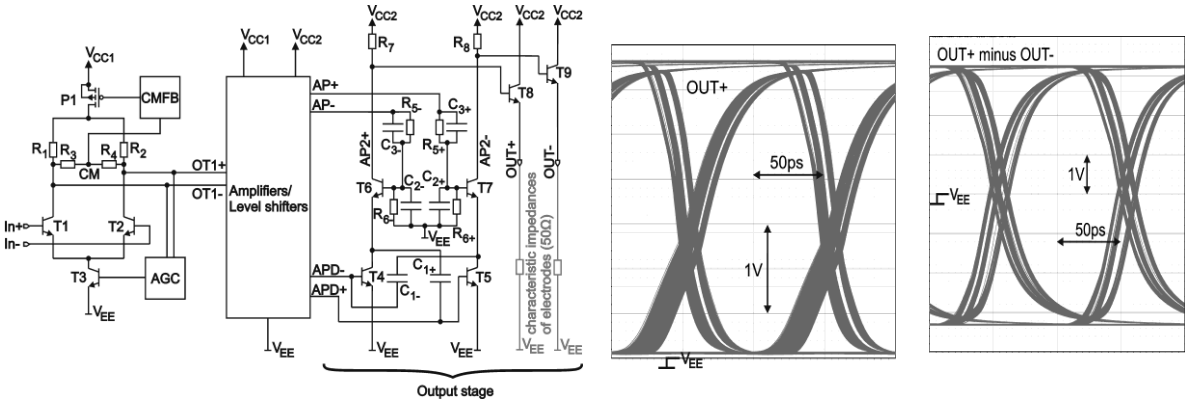

Figure 1 - Simplified schematic of the electronic driver (left) and simulated eye diagrams (right) of one single ended output OUT+ (0V to 2.8V) and the whole differential output (Vpp=5.6V) for 50mVpp at the input (10Gb/s)

The driver contains a differential amplifier (T1-T3, P1, R1-R4) for pre-amplification. The input common-mode voltage at In+/In- is ≈1.25V. A common-mode feedback circuit (CMFB) is implemented to set the optimal operation point. The input data signal is overlaid to the input common-mode voltage and can be applied either only at a single input (e.g. In+) or at both inputs (In+ and In+) as a fully differential signal. For high input amplitudes, an automatic gain control (AGC) is implemented for reduction of the voltage gain. Additional amplifiers and level shifters generate two data signals (AP+/AP- and APD+/APD-) at different common-mode voltage levels to drive transistors T6 in series to T4 (T7 and T5 resp.) with the help of RC-networks to overcome the limits set by the collector-emitter breakdown voltage BVCE0≈2.2V of these fast transistors. Transistors T8 and T9 with lower speed but higher BVCE0 drive the electrodes of the modulator with a characteristic impedance of 50Ω. The driver uses two supply voltages (VCC1=2.5V and VCC2=4.2V). So a maximum output differential voltage of Vpp=5.6V can be achieved. Measurements have shown that the driver has a maximum AC gain of 40dB (f-3dB=7.5GHz).

The global photonic BiCMOS flow is schematically depicted in figure 2. The process steps within the pink box describe the standard IHP SG25H3 BiCMOS process. Three photonic modules are then introduced into the process flow at different stages. Photonic SOI, with a silicon layer thickness of 220nm is not fit for integration with high-performance bipolar transistors. This is mainly due to incompatibility with collector fabrication and the higher thermal resistance compared to bulk silicon substrates that are normally used for high-performance BiCMOS processes. The collector fabrication involves producing a buried n+ layer below the n-well layer, however, the silicon overlayer of photonic SOI is too thin to achieve this. Furthermore, the buried oxide layer of photonic SOI is too thick (2µm) and therefore prevents effective heat dissipation from the high-speed bipolar circuits,

strongly limiting high-speed performance. For this reason a process for combining local-SOI areas with bulk-Si areas was developed.

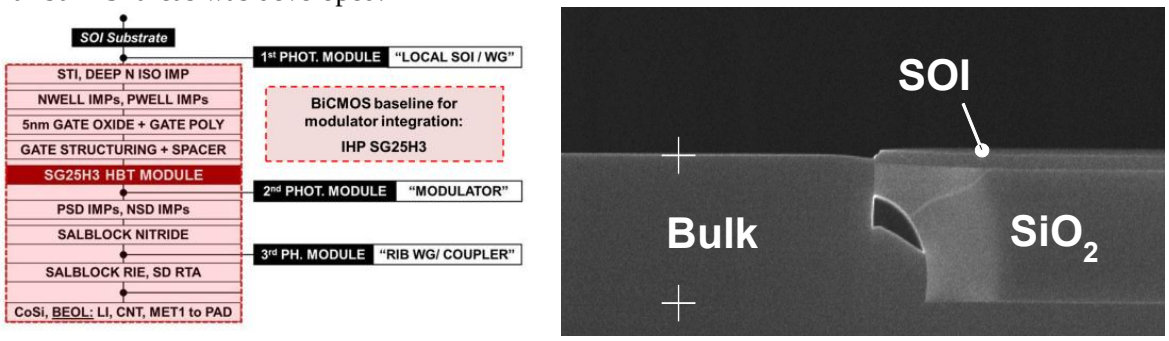

Figure 2 - Photonic BiCMOS global flow (left) and local-SOI cross section [13] *(right)*

The starting substrate is photonic SOI, which is etched down to the handle wafer and then locally regrown by Si-epitaxy, finishing with polishing to obtain surfaces at the same height for local-SOI and for bulk silicon. A cross sectional SEM image of the wafer showing the transition between a bulk and a local SOI region is also shown in figure 2. The left hand side of the image shows the regrown and planarised bulk region of the wafer whilst the right hand side of the image shows the local SOI region. This local SOI process describes the first photonic module which is inserted in the BiCMOS flow. After this the BiCMOS process steps of shallow trench isolation (STI) and deep n-well layer formation for the vertical isolation of nMOSFETs are performed (DEEP N ISO IMP). The CMOS wells are then formed (NWELL IMPs and PWELL IMPs) followed by the gate oxidation (5nm GATE OXIDE), gate polysilicon deposition (GATE POLY), gate structuring (GATE STRUCTURING) and gate spacer etching (SPACER). A series of process steps are then performed for the heterojunction bipolar transistor (HBT) fabrication, more details of which can be found in [14]. The second photonic module is then inserted in the process flow which involves the ion implantation steps and an intermediate waveguide etch-depth to fabricate the frontend structure of the silicon photonic modulator. The electrode is later fabricated using standard backend metalisation. Source/drain implantations (PSD IMPs and NSD IMPs), application of a silicide blocking layer then take place (SALBLOCK NITRIDE). The third photonic module is then performed involving a one mask step which is applied for etching shallow trenches in the top-Si layer of the SOI regions to form low-loss waveguides simultaneously with grating coupler structures. The process is then completed with patterning of the silicide blocking mask (SALBLOCK RIE), source drain annealing (SD RIE), colbalt salicidation (CoSi), a local interconnect process (BEOL:LI), contact definition (CNT) and structuring of 5 metal layers and a passivation layer (MET1 to PAD).

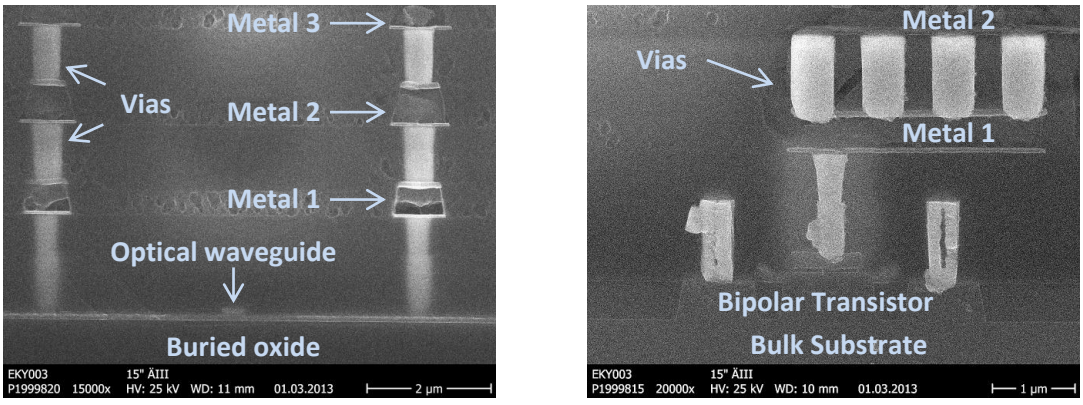

Figure 3 – Cross sectional diagrams of the phase shifter with metal layers 1-3 (left) and SG25H3 bipolar transistor (right)

Annotated cross-sectional SEM images of the photonic device and high performance bipolar transistors on the same wafer are shown in figure 3. In the image on the left of figure 3 a cross section

through the high speed optical phase modulator is shown along with three metal layers of its electrodes. In the right of figure 3 the cross section of a bipolar transistor can be seen. Preliminarily investigations comparing the electronic yield on local-SOI and on baseline bulk wafers using typical monitors (such as 4k & 12k HBT arrays) produced the same figures [13].

3. Photonic circuit layout

The photonic circuit is formed in the local SOI regions on the wafer. These have a silicon overlayer of 220nm thickness and buried oxide layer of thickness 2µm. High speed optical modulation is achieved via the plasma dispersion effect, using the depletion of free carriers from a reverse biased pn junction to electrical control the density of free carriers in interaction with the propagating mode and ultimately changing the phase of the modulating light. A cross-section of the semiconductor section of the phase shifter design is shown in figure 4. The device in based on waveguides of height 220nm, slab height 100nm and a rib width of 400nm. The rib region and slab to one side are doped p-type and the slab to the other side is doped n-type, therefore creating a pn junction at one edge of the waveguide rib. In order to obtain efficient modulation with this configuration the p-type region is doped with a lower concentration than the n-type region, so that the depletion extends mainly into the waveguide with a reverse bias applied. Highly doped p and n-type regions that are used to form ohmic contacts to the device electrodes are positioned in the slab at a distance of 500nm and 600nm away from the rib edges respectively.

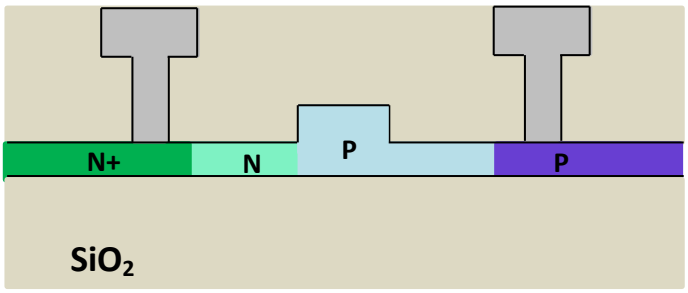

Figure 4 – Cross sectional diagram of the phase modulator element.

The modulator is fabricated using a self-aligned process similar to the one described previously [15]. The modulator electrodes are formed in the standard BiCMOS backend with the coplanar waveguides formed on top metal 2 which is 3um thick, with connections down to the phase modulator made with the lower metal layers and intermediate vias. The phase modulators of 2mm in length are placed in MZI to convert between phase and intensity modulation. The configuration of the MZI is shown in figure 5.

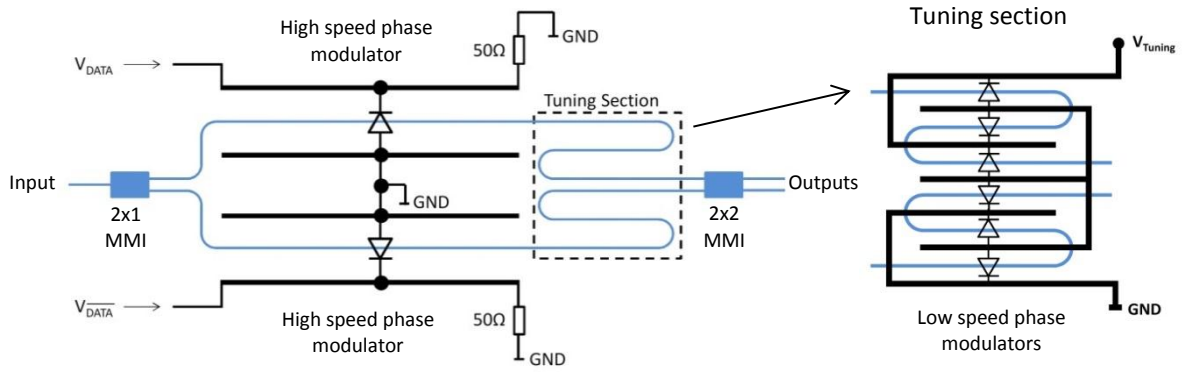

Figure 5 – Diagram of the Mach Zehnder Interferometer configuration including detail of the tuning section.

A symmetrical MZI is used to give a broad operating wavelength range and thermal stability. A 2x1 MMI is used to split the input light into the two optical arms. Low loss and precise splitting has been

demonstrated using this structure separately [16]. The high speed phase modulators are incorporated into both arms of the MZI in order to balance the optical loss and to therefore produce a large extinction ratio. This configuration also allows for dual-drive operation for which a lower drive voltage is required. Furthermore low chirp has been demonstrated in this configuration [15]. Low speed phase modulators of length 2.55mm are included in both arms to allow the operating point to be adjusted electrically. The low speed phase modulators consist of the same PN junction as used for the high speed phase modulators however the n+ and p+ regions are separated from the waveguide edge by 1µm in order to reduce the optical loss. To save space these low speed tuning sections are folded inside the MZI structure as shown in figure 5. A 2x2 MMI is then used to recombine the light from the two MZI arms. The 2x2 MMI will theoretically position the modulator operating point at quadrature without tuning and will also provide a second output for monitoring purposes without incurring loss on the main output. Note that even slight differences in the actual waveguide dimensions across the device change the phase relationship at the start of the 2x2 MMI and mean that in practice, the tuning section is essential to operate the modulator correctly. An optical microscope image of the final fabricated device during testing is shown in figure 6.

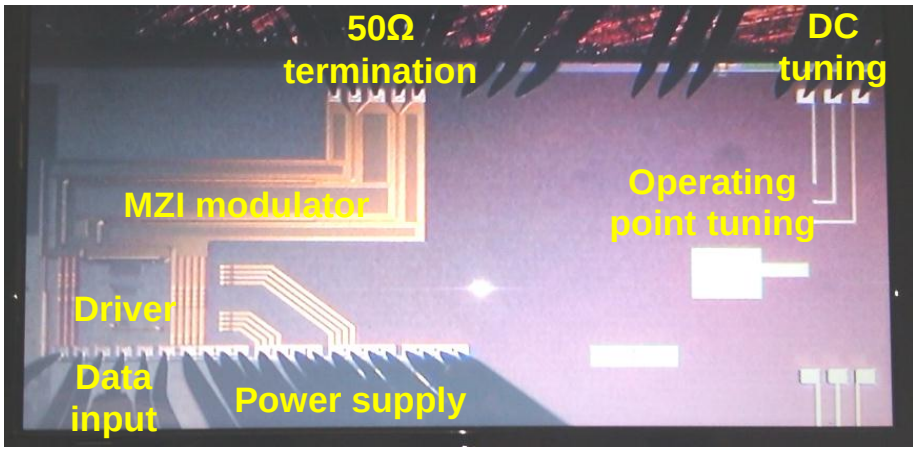

Figure 6 – Optical microscope image of the full device under test.

4. Experimental results and discussion

The different photonic elements of the device are first characterised to assess their contribution to the optical loss of the device. A number of test structures have been included on the fabricated dies to enable this. For the waveguide and doping loss, the cut back method is used where the optical loss through different lengths of waveguide is examined. The MMI and bend loss structures include a different number of bends/MMIs. Surface grating couplers are used to couple light at a wavelength of approximately 1550nm into and out of both the test structures and the full devices. The results of the optical measurements on the test structures are shown in figure 7.

The optical loss of the passive waveguide is ~0.4dB/mm. Subtracting this loss from the measurement of the waveguides with doping gives a phase modulator loss of ~3.3dB/mm comprising ~1dB/mm loss due to the n and p-types regions and ~2.2dB/mm loss due to the highly doped n and p-type contact regions. The 2x1 and 2x2 MMI losses are ~0.2dB/MMI and ~0.7dB/MMI respectively. The bend loss is 0.03dB/90°bend for each of eight bends in the full MZI structure.

The DC tuning sections in each arm are electrically connected in a back to back diode configuration as depicted in figure 5. Continuous DC tuning from -10V to 10V is therefore possible covering almost a complete cycle of the MZI response as can be seen in black line of figure 8 which shows the averaged optical output power from the device during modulation with the voltage across the DC tuning section varied. The -3dB level (quadrature) is indicated by the blue line. It can be seen that quadrature operation is achieved at approximately -2V or +7V. To confirm that the modulator is operated at quadrature with +7V applied across the DC tuning section the output power from the device against time was observed on a digital communications analyser (DCA).

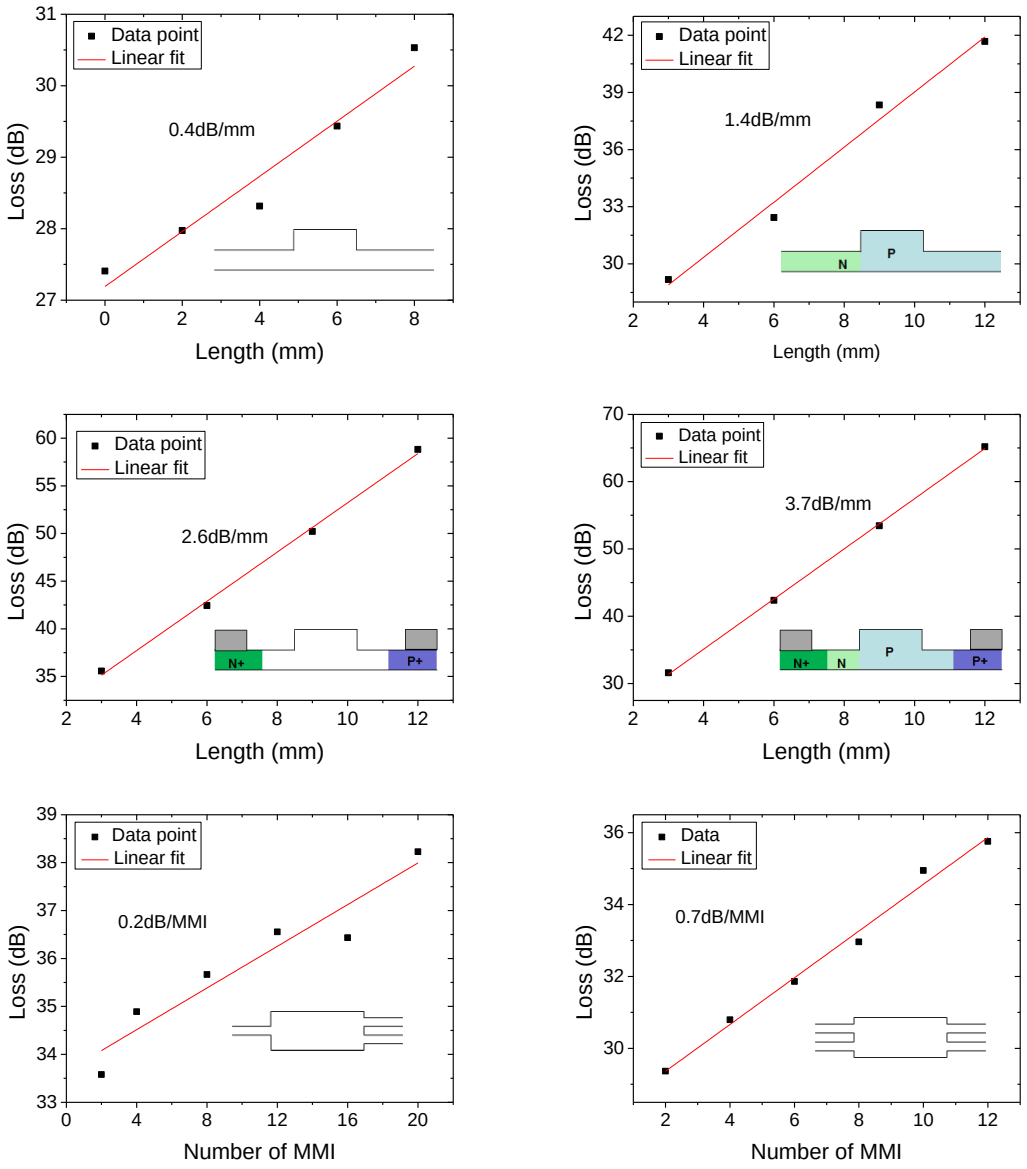

Figure 7 – Characterisation of the different elements in the photonic circuit. Top left shows the optical loss of the passive rib waveguides. Top right shows the optical loss of the passive waveguides and the low doped n and p-type regions. Middle left shows the optical loss of the passive waveguides and the highly doped regions. Middle right shows the loss of the full high speed phase shifter sturcture inculding passive waveguide loss. Bottom left and bottom right show the optical loss of the 2x1 and 2x2 MMI respectively.

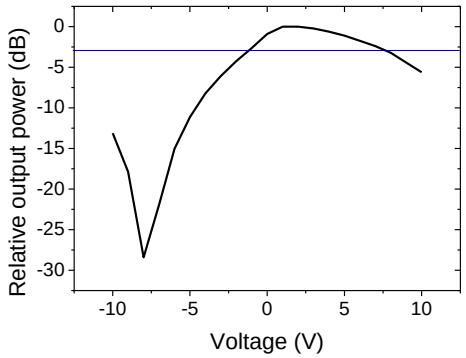

Figure 8 – Average optical output power during modulation with different voltages applied across the DC tuning section.

The output of the modulator with +5V, +7V and +9V applied across the modulator is shown in figure 9. The solid and dashed brown line indicates the minimum and maximum output power levels of the modulator respectively. It can be seen that with +7V across the tuning section the modulator is positioned in the middle of the optical power range (quadrature).

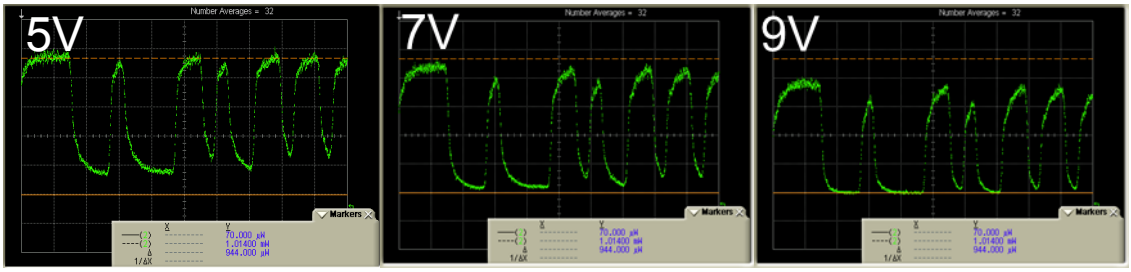

Figure 9 – DCA screen images of the modulator output with different DC voltages applied across the tuning element.

The DC performance of the high speed phase modulator element is assessed in isolation by testing a stand-alone 1mm long asymmetric Mach-Zehnder Modulator fabricated on the same chip. The phase shift and phase efficiency versus reverse bias voltage are shown in the left and right graphs of figure 10 respectively. Over the operating range of the driver output (0 to ~3V) a phase efficiency of approximately 2.3V.cm results.

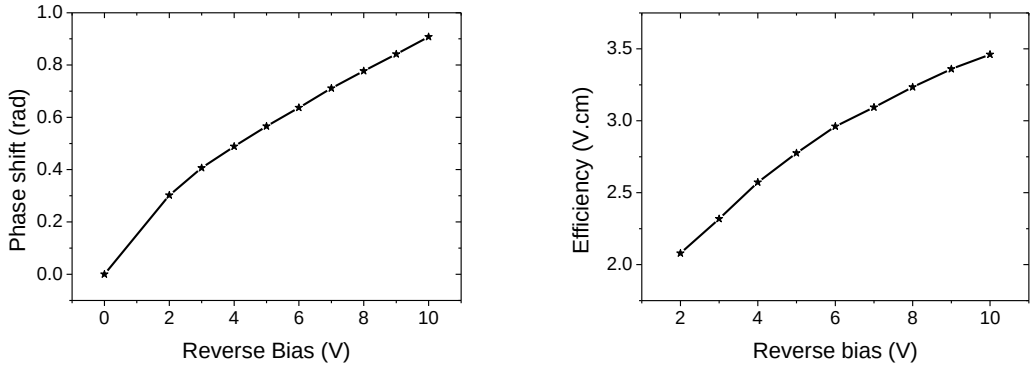

Figure 10 – Phase shift achieved on a 1mm long modulator versus applied reverse bias voltage (left) and resultant phase efficiency (right)

As can be seen in the optical microscope image of figure 6 the input RF signal, 50ohm termination and DC power supply for the driver and tuning section are applied to the device using custom made probes with both DC and RF tips supplied by TPC technoprobe. High speed testing is performed by applying a 240mVpp PRBS data stream and DC power to the driver. The RF signal with a 1.25V DC bias level is applied to one input of the driver. A 1.25V DC level is applied to the other input. Two DC levels of 2.5V and 4.2V are used to power the driver. Light of wavelength 1540nm is passed to the device from a tunable laser and polarisation controller to the input grating coupler via an optical fibre. Light is then collected from the device and is passed to an EDFA again via a grating coupler and optical fibre. The EDFA is used to boost the optical output signal. A band-pass optical filter is then used to reduce noise from surrounding wavelengths before the light is passed to a DCA for measurement. The optical eye diagram from the modulator is shown in figure 11. It can be seen that 10Gbit/s modulation is achievable. The eye diagram is obtained with a +7V tuning voltage so that the device is operated at the quadrature point as discussed previously. Subtracting the noise generated in the EDFA from the one and zero power levels gives an extinction ratio of approximately 8.4dB.

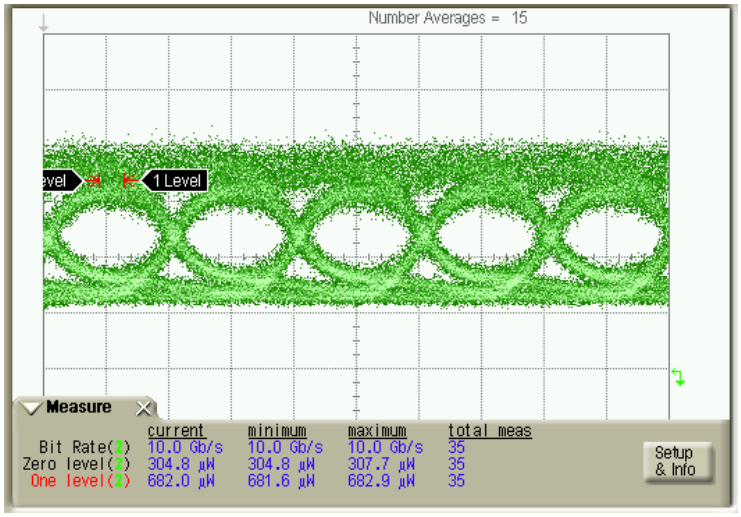

Figure 11 – Output optical eye diagram from the modulator at 10Gbit/s.

The total on-chip loss of the device is approximately 13dB. The main contributions of the optical loss in the device are: 2mm high speed phase shifter (7.2dB), 2.55mm tuning section (3.6dB), 2x1 MMI splitting (0.2dB), 2x2 MMI combining (0.7dB), and additional passive waveguide loss (0.8dB). Significant reductions in the device loss are achievable through simple design changes. Our analysis suggests that a slight increase of the p+ and n+ region separations can be made to reduce loss by ~4dB whilst maintaining high speed operation. If thermal tuning was employed instead of the depletion configuration currently used the loss can be reduced by a further ~3dB (at the expense of an increase in tuning power). In total it is expected that on-chip insertion loss can be reduced to approximately 5dB. It should be noted that the speed of 10Gbit/sec is limited by the transistor speed in SG25H3 with $f_T \approx 120$GHz. Operation at speeds up to 40Gbit/s is achievable by using SG25H1 where much faster transistors are available with fT/fmax = 180/220 GHz. No issues are anticipated in following the photonic BiCMOS integration approach demonstrated in this paper for SG25H1 since the electronic technologies differ only in the bipolar module, and local-SOI does not affect the performance of the HBT. Furthermore MZM modulators operating at >25Gbit/sec were already realized in Innovations for High Performance Microelectronics (IHP) technology [15]. Furthermore similar modulators have been reported at 50Gbit/s [1]. There is therefore huge potential to scale the performance of silicon photonics-BiCMOS integration to much higher speeds in the future.

5. Summary

A new approach involving the monolithic front-end integration of a silicon photonics with BiCMOS has been demonstrated. To enable this integration local SOI regions have first been realised on the wafers. This allows for the electronic elements to be fabricated in bulk silicon (as required for optimal performance) side by side with the photonics elements which must be formed in thin SOI. A dual-drive modulator driver amplifier has been designed and fabricated using the standard steps of the BiCMOS foundry technology (SG25H3). A high speed carrier depletion based silicon MZM has been formed alongside the driver using additional photonic modules incorporated into the BiCMOS flow. Electrical connections between the two elements are made using the standard metallisation layers of the BiCMOS backend process. 10 Gbit/s modulation has been demonstrated from the integrated driver-modulator as targeted by the design. An extinction ratio in excess of 8dB with an optical loss of 13dB is observed. The optical loss and device speed can be significantly improved through design changes to the modulator and choice of the SG25H1 process for the driver in the future.

6. Acknowledgements

We gratefully acknowledge partial support by European Commission, project HELIOS (FP7-224312), by German Ministry of Research and Education (BMBF), project SASER, and by an EPSRC funded project in the UK, "UK Silicon Photonics".

7. References

[1] - D. J. Thomson, F. Y. Gardes, J-M. Fedeli, S. Zlatanovic, Y. Hu, B. P. -P. Kuo, E. Myslivets, N. Alic, S. Radic, G. Z. Mashanovich and G. T. Reed, IEEE Photonics Technology Letters, **24**, 234-236, (2012).
[2] - X. Xiao, H. Xu, X. Li, Z. Li, T. Chu, Y. Yu, and J. Yu, Opt. Express, **21**, 4116-4125, (2013).
[3] - P. Dong, L. Chen, and Y-K. Chen, Opt. Express, **20**, 6163-6169, (2012).
[4] - Y. Tang, J. D. Peters and J. E. Bowers, Optics Express, **20**, 11529-11535, (2012).
[5] - D. Feng, S. Liao, H. Liang, J. Fong, B. Bijlani, R. Shafiiha, B. J. Luff, Y. Luo, J. Cunningham, A. V. Krishnamoorthy, and M. Asghari, Optics Express, **20**, 22224-22232, (2012).
[6] - M. Liu, X. Yin, E. Ulin-Avila, B. Geng, T. Zentgraf, L. Ju, F. Wang and X. Zhang, Nature, **474**, 64–67, (2011).
[7] - L. Alloatti, D. Korn, R. Palmer, D. Hillerkuss, J. Li, A. Barklund, R. Dinu, J. Wieland, M. Fournier, J. Fedeli, H. Yu, W. Bogaerts, P. Dumon, R. Baets, C. Koos, W. Freude, and J. Leuthold, Optics Express, **19**, 11841-11851, (2011).
[8] - G. T. Reed, G. Z. Mashanovich, F. Y. Gardes and D. J. Thomson, Nature photonics, **4**, 518 – 526, (2010).
[9] - B. Analui, D. Guckenberger, D. Kucharski, A. Narasimha, IEEE J. Solid State Circuits, **41**, 2945-2955, (2006).
[10] - S. Assefa, S. Shank, W. Green and M. Khater, in Proc. IEEE International Electron Device Meeting IEDM, 809-11, (2012).
[11] – J. S. Orcutt, B. Moss, C. Sun, J. Leu, M. Georgas, J. Shainline, E. Zgraggen, H. Li, J. Sun, M. Weaver, S. Urošević, M. Popović, R. J. Ram, and V. Stojanović, Opt. Express, **20**, 12222-12232, (2012).
[12] – B. G. Lee, A. Rylyakov, W. M. J. Green, S. Assefa, C. W. Baks, R. Rimolo-Donadio, D. Kuchta, M. Khater, T. Barwicz, C. Reinholm, E. Kiewra, S. Shank, C. Schow, and Y. A. Vlasov, Proceedings of OFC, PDP5C, (2013).
[13] - D. Knoll, H. H. Richter, B. Heinemann, S. Lischke, Y. Yamamoto, L. Zimmermann and B. Tillack, ECS Transactions, **50**, 297, (2013).
[14] - B. Heinemann, R. Barth, D. Knoll, H. Rucker, B. Tillack, W. Winkler, Third International SiGe Technology and Device Meeting, (2006).
[15] - D. J. Thomson, F. Y. Gardes, S. Liu, H. Porte, L. Zimmermann, J-M Fedeli, Y. Hu, M. Nedeljkovic, X. Yang, P. Petropoulos and G. Z. Mashanovich, IEEE Journal of Selected Topics in Quantum Electronics, **9**, 3400510, (2013).
[16] - D. J. Thomson, Y. Hu, G. T. Reed, and J-M. Fedeli, IEEE Photonics Technology Letters, **22**, 1485-1487, (2010).