Electrical transport properties of isolated carbon nanotube/Si heterojunction Schottky diodes

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A detailed study of the electrical transport properties of Pd contacted carbon nanotube (CNT)/Si heterojunctions is presented. The CNT with a diameter ranging from 1.2 to 2.0 nm on *n*-type Si substrates showed rectifying behavior with the ideality factor of 1.1-2.2 and turn on voltage of 0.05-0.34 V. The current-voltage characteristics of the CNT/n^+-Si diodes were investigated in the temperature range from 50 to 300 K. The transition from thermionic emission to tunneling process was seen in the forward current around 150 K and the Schottky barrier height at Pd/CNT interface is estimated to be 0.3-0.5 eV.

(Received on 30-Sep-2013 # L13-09320)

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Intense research on nanotechnology for future electronics based on "More than Moore" and "Beyond complementary metal-oxide-semiconductor (CMOS)" approaches is currently underway. In both cases, heterogeneous integration is essential to utilize the CMOS platform. Carbon nanotube (CNT) is one of the most attractive building blocks for nanodevices due to its excellent electrical, optical, thermal, and mechanical properties. The CNT has spurred research into many practical applications including nanoelectronic devices,[1,2] biosensors,[3] and via interconnects.[4] Recently, a high performance CNT/Si solar cell with power conversion efficiency of 15% has been reported.[5] This device is ready for integrating the existing Si solar cells which hold a dominant share of the market and an even higher efficiency could be achieved by fabricating multi-junction solar cells. The CNT/Si heterojunction has attracted great interest not only for solar cells[5-7], but also for photodetectors[8-10] in the wide wavelength ranging from ultraviolet to near-infrared. For these applications, single walled CNT (SWNT) could provide even higher performance due to the strong absorption at the wide wavelength range. The absorption peak is controlled by changing the direct band-gap, which depends on the diameter of the SWNT. In addition, multiple electron-hole pairs associated with the higher subbands at low temperatures could enhance the device performance.[11] While the SWNT/Si heterojunction could play a crucial role in the CNT based devices, the measurements of electrical transport properties on the heterojunctions between isolated SWNT and Si have yet not been made because most of the work has been done by using CNT composite film[5,6,10] or multiwalled CNTs.[8,9]

Figure 1 shows an outline of the CNT/Si diode fabrication process. A heavily doped *n*-type Si (0.02 Ω·cm) was employed as a substrate. After a standard cleaning process, a 55-nm-thick SiO_2 layer was thermally grown as an isolated layer. The SiO_2 wafers were cut into 8×10 mm pieces and the samples were soaked with acetone and isopropyl alcohol for cleaning. Metal

catalyzed CVD growth was employed to prepare CNTs. The substrate was dipped in ferric nitrate solution for 1 min and rinsed with hexane. The solution was prepared by dissolving 1.5 mg of the ferric nitrate salt in 5 ml of isopropyl alcohol and sonicated for 20 minutes. The CNT growth was carried out using CVD in a hot-wall reactor at atmospheric pressure. CNTs were grown at 850 °C for 20 min using a mixture of methane (1000 sccm) and H_2 (300 sccm) immediately after a pre-anneal in H_2 (1000 sccm) at 900 °C.[12] Figure 1(a) illustrates the schematic of a Si/SiO_2 substrate after CNT growth. The Pd contacts (thickness: 150 nm, area: 100×100 μm) were formed using direct write laser lithography and lift-off at arbitrary position as shown in Fig. 1(b). Pd films were deposited by the direct current magnetron sputtering system. Pd is an appropriate choice for CNT devices because it delivers ohmic contact for p-type conduction due to its high work function and has the technological advantage of favorable wetting between Pd and CNT.[13] Next, the SiO_2 layer near the contacts was etched with buffered hydrofluoric (BHF) acid through a photoresist mask. A precise alignment of the window patterns to the contacts is not required because both Pd and CNT are tolerant against BHF acid. Only the SiO_2 layer in the unprotected region is etched away. As a result, a part of the CNT dropped as low as the Si surface as illustrated in Fig. 1(c). At the same time, unnecessary CNTs in the window are washed away. This process allows us to connect CNTs with the Si substrates over a large area with an oxide-free interface. The CNTs adhered to Si substrate via van der Waals forces. Finally, the Al film (thickness: 100 nm) was deposited by sputtering on the back side of the Si substrate as a back contact. Figure 1(d) shows a field emission scanning electron microscope (FE-SEM) image of the fabricated device. It is clearly seen that an isolated CNT bundle has formed a contact with the Si substrate. Typically one or two CNTs hang over the gap

between the top contact and the Si substrate. For comparison, similar devices were fabricated on a heavily doped *p*-type Si (0.005 Ω·cm).

The area density of CNTs was analyzed using six FE-SEM images from different parts of the sample and evaluated as 2.4 ± 0.3 CNTs/μm^2. As-grown CNTs were also characterized by means of a micro Raman spectroscopy with He-Ne laser (λ = 632.8 nm, power = 12 mW). All samples clearly showed the radial breathing mode (RBM), indicating that SWNTs are present. The lack of D-band peak indicates that synthesized SWNTs have a low defect density. The diameter of SWNTs is estimated at 1.2-2.0 nm from the RBM peaks. Thicker nanotubes may exist but the notch filter of our Raman system prevents the measurement for lower wave numbers.

Electrical measurements have been made on 51 functional devices in total and the yield of working device is 73%. The cause of the device failure is mainly associated with open circuits due to the lack of CNTs between Pd contact and Si substrate. Figure 2(a) shows typical *I-V* characteristics of CNT/Si heterojunctions. Forward bias is defined as positive voltage applied to the CNT. The device fabricated on a heavily doped *n*-type Si substrate exhibits rectifying behavior with an ideality factor (*n* value) of 1.2. The current at forward bias is more than three orders of magnitude larger than the current at reverse bias. On the contrary, the device fabricated on a heavily doped *p*-type Si substrate exhibits quasiohmic behavior with resistance of around 500 kΩ at high bias voltage. The conductance at negative bias is slightly larger than the one at positive bias, suggesting that the hole density in p^+-Si is larger than that in CNT. The observed quasiohmic behavior in these measurements is consistent with the previous results on the multi-walled CNT/p^+-Si heterojunctions.[14] The inset shows the photovoltaic effect of the CNT/n^+-Si diode, indicating a fill factor (FF) of 0.33 and an open-circuit voltage of 64 mV. The conversion

efficiency of the CNT/n^+-Si diode is estimated to be 2.4% taking into account the effective device area. Figure 2(b) shows *I-V* characteristics for ten typical CNT/ n^+-Si diodes. The forward current at 1 V ranges from 0.3 to 2.3 mA, the ideality factor ranges from 1.1 to 2.2, and the reverse current at -1 V ranges widely from 6.6×10^{-8} to 1.1×10^{-4} A. The reverse current at $V_f < 0$ is mainly determined by the Schottky barrier height. The injection of electrons from the Pd electrode to the CNT depends on the bandgap of CNT.[15] Simulations reported in the literature[16] predict an increase in leakage current by four orders of magnitude when the bandgap of CNTs is reduced from 0.9 to 0.45 eV. The variation of CNT diameter obtained from our Raman measurements suggests that the bandgap ranges from 0.45 to 0.75 eV. Thus, variations in CNT diameter can explain most of the reverse current variability, particularly when the uncertainty in CNT diameter distribution from Raman and TEM measurements is considered.

Figure 3(a) shows the temperature dependence of *I-V* characteristics of the CNT/n^+-Si diode in the temperature range from 50 to 300 K. The turn on voltage decreases with increasing temperature. The measured lower turn on voltage less than 0.5 V at room temperature indicates that this device is a Schottky diode. In order to investigate the current transport mechanism of the CNT/n^+-Si diode, an Arrhenius plot at forward bias voltage of 0.4 V is shown in Fig. 3(b). The barrier height of Φ_B is given by $-q(\Phi_B - V/n)/k$, where q is the electron charge, k is the Boltzmann constant, V is the forward bias voltage, and n is the ideality factor. From the measured slopes above 200 K and their corresponding ideality factors, the barrier height is estimated to be 0.3-0.5 eV. The band diagram under forward bias in the inset shows that the fabricated device has two barriers. One is the Schottky barrier at the Pd/CNT interface and the other is the conduction band discontinuity at the CNT/n^+-Si heterojunction interface. In the band diagram, CNT is an intrinsic semiconductor with band gap of 0.6 eV and electron affinity of 4.5

eV and work function of Pd is 5.2 eV. The band diagram indicates that the Pd electrodes deliver a good ohmic contact to CNTs for holes but not for electrons. Consequently, the rectifying behavior of the fabricated device is associated with the Pd/CNT interface rather than the CNT/n^+-Si interface. Thus the estimated barrier height is attributed to the Schottky barrier at the Pd/CNT interface. These values are in good agreement with the previously reported values measured by various techniques.[17] As for the CNT/p^+-Si device, although the discontinuity in valence band edges ΔEv exists at CNT/p^+-Si interface, the thermionic emission process is the dominant transport mechanism at room temperature, giving rise to the ohmic behavior.

Figure 3(b) shows the transition from a negative slope to a positive slope at 130 K. The other samples also show the same transition around 150 K. In general, the tunneling current has a weaker temperature dependence compared to the thermionic emission current and consequently the tunneling process dominates at low temperatures. Thus, the tunneling through the barrier at the heterojunction interface is the most likely process to explain the negative activation energy at low temperatures. The discontinuity in conduction band edges ΔEc can be calculated from the electron affinity difference between CNT and n^+-Si and it ranges from 0.45 to 0.7 eV. A similar transition between thermionic emission and tunneling was reported by Appenzeller *et al.* in Ti contacted CNTFETs.[18] They mentioned that the tunneling probability was enhanced in a CNT due to a smaller effective mass of narrow gap semiconductor.

In summary, we have fabricated Pd contacted CNT/Si heterojunctions. The heterojunctions on the n^+-Si substrates showed rectifying behaviour with ideality factors ranging from 1.1 to 2.2. The *I-V* characteristics of the CNT/n^+-Si diodes have been investigated in the temperature range from 50 to 300 K. The transition from the thermionic emission to the tunneling process was seen in the forward current around 150 K. From the temperature

dependence of the forward current, the barrier height at Pd/CNT interface is estimated to be 0.3-0.5 eV.

The authors would like to acknowledge EPSRC for supporting this work. Electrical measurements were carried out under the cooperative research project program of the Research Institute of Electrical Communication, Tohoku University.

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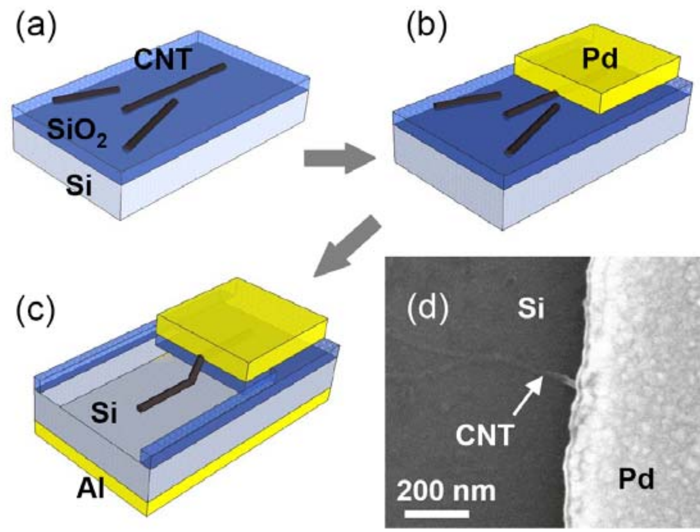


Figure 1 Schematic drawing of the fabrication steps of the CNT/Si heterojunction. (a) CVD growth of CNTs on Si/SiO_2 substrate. (b) After the direct write laser lithography, a Pd layer was sputtered for an electrode and followed by a lift-off process. (c) CNT/Si heterojunction was formed after the SiO_2 wet etch through the patterned photoresist. Al electrode was formed on the back side. (d) FE-SEM image after the formation of CNT/Si heterojunction.

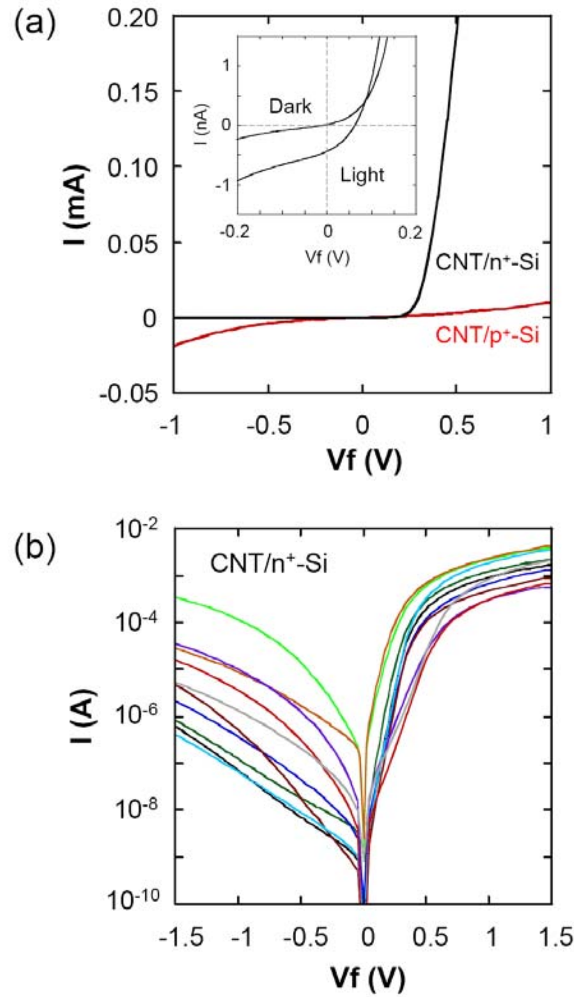
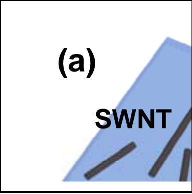


Figure 2 (a) Typical *I-V* characteristics of the CNT/Si heterojunctions. The CNT/n^+-Si device showed rectifying behavior with an ideality factor with 1.2, while the CNT/p^+-Si device showed quasiohmic behavior. The inset shows *I-V* characteristics of the CNT/n^+-Si diode with and without illumination. The photocurrent measurements were carried out using a halogen lamp with 8.6 mW/cm^2 as a light source. (b) Ten typical *I-V* characteristics of CNT/n^+-Si diodes.



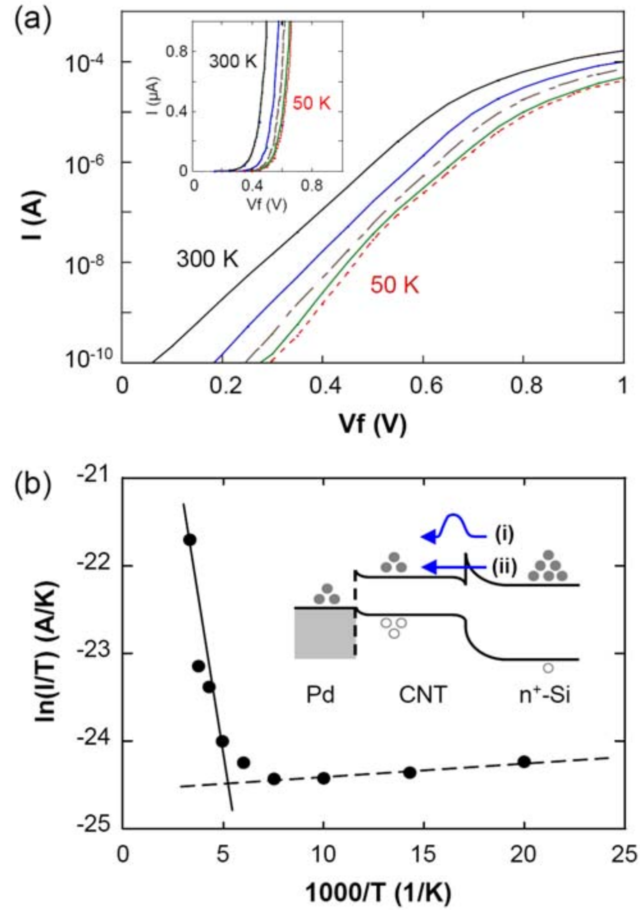


Figure 3 (a) *I-V* characteristics of the CNT/n^+-Si diode measured for different temperatures (50, 133, 200, 267, 300 K). The inset shows temperature dependence of the turn on voltage. (b) Arrhenius plot of the CNT/n^+-Si diode at $V_f = 0.4$ V. The inset shows the energy band diagram of CNT/n^+-Si diode. The panel (i) and (ii) show thermionic emission process and tunneling process, respectively.