UNIVERSITY OF SOUTHAMPTON

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

FAST CHARGING TECHNIQUES AND COMPACT INTEGRATED IMPLEMENTATIONS FOR ELECTROCHEMICAL DOUBLE LAYER CAPACITORS IN PORTABLE APPLICATIONS

By: Rareş Andrei Bodnar

Supervisor: Prof. William Redman-White

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Abstract

The widespread increase in the range and types of portable electronic devices in the past decades has resulted in higher requirements for energy storage and conversion modules. Most of these devices use rechargeable batteries as energy storage elements. No matter what type of batteries are used (Ni-Cd, Ni-MH, Li-Ion, etc.) they all have one serious drawback in common, in terms of charging time. Electrochemical double layer capacitors (EDLCs) also known as ultracapacitors or supercapacitors seem to have overcome this disadvantage, at the cost of lower energy storage capacity.

This work aims to explore the design of fast and compact integrated charging techniques for ultracapacitors using the AC mains network as the source. The main constraints that arise are the power dissipation on-chip and in the magnetic components due to the large amount of energy that has to be transferred in a very short time interval. Two other limitations come from the EDLC side due to the device parasitics and the widely varying voltages over the operational envelope. This will impose the need for a flexible control system providing high efficiency over the whole output voltage range.

The structure of this thesis comprises five main parts: literature review, behavioural modelling of the control system (including matlab simulations); implementation of the device with discrete components; design of an analogue circuit implementation and design of a mixed signal circuit implementation. As ultracapacitors represent one of the newest solutions in the field of electrical energy storage there are very few designs for chargers from the mains network. Therefore the literature review will also examine the properties and the modelling of EDLCs, as well as the choice of converter topologies available and the characteristics of the magnetic devices required for the system. The behavioural model of the control module gives a preview of the system parameters, while the design chapter introduces a series of new control techniques. The simulations and measurements of the breadboard circuit come as a first confirmation of the design approach and make it a viable starting point for an IC implementation. The analogue IC design presents the integration of the algorithms in a medium-voltage process using the current mode approach, as a demonstrator for a fully monolithic high-voltage IC. Once the functionality of the system is demonstrated at IC level, the mixed-signal system aims to optimize the device and provide a broader flexibility for the system parameters and control algorithms.

List of publications

1. Rares Bodnar, William Redman-White, “A 250W/30A Fast Charger for Ultracapacitors with Direct Mains Connections”, European Conference on Circuit Theory and Design, pp. 813-816, Aug 2011

2. Rares Bodnar, William Redman-White, “High-Accuracy Current Memory in HV CMOS Technology”, IEEE Transactions on Circuits and Systems 60-II(6), pp. 321-325, 2013

3. Rares Bodnar, William Redman-White, “An Integrated Ultracapacitor Fast Mains Charger with Combined Power/Current Optimisation”, European Solid State Circuits Conference, Sept 2013

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Chapter 1 INTRODUCTION

1.1 Motivation

The main limitations of battery powered electrical and electronic devices have been the energy storage capacity and the charging time. Electrochemical Double Layer Capacitors (EDLCs) seem to be a very good solution for the second problem thanks to the high charge / discharge currents. Recent research has demonstrated that the energy storage density of the EDLCs can reach half the value of the Li-Ion batteries, while the output power is at least two orders of magnitude higher [4]. As most of the chargers for rechargeable batteries are powered from the mains network, the need for a compact and low cost adapter for ultracapacitors is more than obvious.

One of the main problems regarding the fast charging of energy storage devices is the conductors connecting the charger with the battery or EDLC. As we are aiming to deliver large amounts of energy in a very short time, the resulting currents will be very high (tens of amps), this considering that he nominal voltage of most of these devices is relatively low (between 2.5V and 30-40V when a practical number of cells are connected in series). The wires required to connect the adapter and the battery or capacitor would be very thick, heavy and difficult to manipulate. There are two obvious solutions for this problem: increase the nominal voltage of the energy storage unit by stacking multiple devices in series or design a compact charger that could be embedded inside the energy storage device. The first option requires an additional voltage balancing block which becomes more complicated as the number of the elements increases. Also, as most portable devices require low voltages, thus an additional step-down converter would be required which would bring the efficiency down, while the costs and size of the system would increase. The second alternative has the advantage of transferring the energy to the complete device (i.e. batteries and charger together) at relatively high voltage / low current (230 VAC) and making the conversion to high currents / low voltages locally. As a result, the need for designing a very compact and light charger seems essential in order to solve the fast charging problem.

1.2 Research Goals and Contributions

One of the main goals of this research is to design and implement AC-DC converters as fast chargers for electrochemical double layer capacitors. This includes a detailed analysis of the capacitors and magnetic components at high frequencies; development and demonstration of the control module, starting with Matlab modelling, breadboard circuit implementation, design of custom magnetic components, current-mode analogue IC architecture, circuit design, layout, verification, evaluation and mixed signal system design. Several key research contributions which address these goals are highlighted below:

- Design of an adaptive current control technique that balances the losses on-chip and in the magnetic components, providing a high power throughput at the same time
- Development of two self oscillating regulation algorithms customized for EDLC charging, compatible with loads starting from short circuit up to 16.2V
- Current mode control by sensing the output current in the primary side of the transformer, thus eliminating the need of series current sense resistor in the secondary circuit.
- The system generates a DC current with constant ripple that minimizes the load power dissipation and enhances the lifetime of the EDLC
- Introduced a novel high precision CMOS current memory suitable for high voltage process
- Demonstrated an enhanced version of the Traff current comparator with faster response time and lower quiescent current consumption

Chapter 2 LITERATURE REVIEW

2.1 EDLC overview

The EDLC effect was firstly observed in 1954 by General Electric researchers during their experiments with capacitors using porous carbon electrodes [1]. Although the mechanism was not fully understood it was clear the source of the very large capacitance was the porous surface of the carbon electrodes. The main drawbacks of the capacitor at that time were "the large size of the capacitor" (due the fabrication limitations) and the maximum voltage drop between the electrodes, 2.5V.

The first commercial version of EDLC was introduced by Standard Oil of Ohio in 1966, but it was marketed as "supercapacitor" only in 1978 by NEC. The main application for ultracapacitors at that time was as backup power for computer memories. In 1991 NEC reported the first modern supercapacitor based on an activated carbon electrode, the technology that is also currently used for the manufacturing of EDLCs [2]. The market started expanding at the beginning of the 1990's when several companies like EPCOS, Maxwell Technologies, Panasonic, Nesscap, etc. started manufacturing ultracapacitors for commercial use.

Ultracapacitors currently available on the market are using activated carbon electrodes and still present the two disadvantages highlighted by Becker in 1954, i.e. low energy density and low voltage. Of course the storage capacity of EDLCs has improved over the decades, but similar progress has also been achieved in the competing technologies (i.e. Li-Ion, Ni-Ca, Ni-MH, etc.). The drawback of the moderate energy density (around 6Wh/kg for activated carbon electrodes) can be eliminated by using even more porous electrode materials, according to recent studies. The first competitor is Graphene, a material that presents excellent surface area due to its multiple layers. A novel EDLC based on chemically modified Graphene, made of 1-atom thick sheets of carbon, is presented in [3]. Researchers from MIT have presented an even better solution for the electrode material in the form of a matrix of vertically aligned carbon nanotubes [4]. Based on this technology MIT aims to reach an energy density higher than 60Wh/kg (half of the commercial Li-Ion batteries) and a power density greater than 100kW/kg (three orders of magnitude higher than present batteries). The third alternative for activated carbon electrodes is carbon aerogel, material that also provides a very high surface area.

2.1.1 Structure of the EDLC

The energy storage mechanism of the ultracapacitors is based on the double layer effect, discovered by H. von Helmholtz in 1853 [7]. According to his model, when two electrodes with different potentials are immersed into an ionic solution, the ions from the electrolyte migrate at the interface between the electrode and the solution. A first order approximation of the capacitance is given by equation 2.1.

$$C_{EDLC} = \frac{\varepsilon A'}{d} \qquad (2.1)$$

Where ε is the permittivity, A' is the overall area of the electrodes and d is the distance between electrodes.

Therefore, when the permittivity and the distance are fixed, the only way to raise the specific capacitance is to increase the area but that will lead to bigger devices. Ultracapacitors achieve a very large electrode area without increasing the overall device size by covering the electrodes with a thin layer of activated carbon, as depicted in figure 2.1.

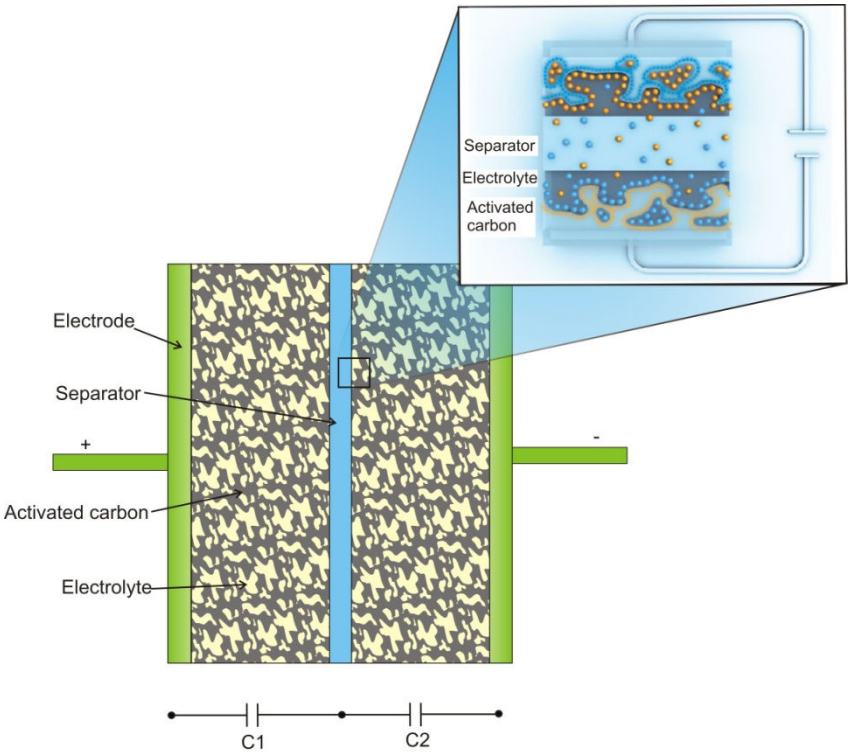


Figure 2. 1. Structure of the ultracapacitor

A separator plate, also coated with activated carbon, is introduced between the two electrodes. The resulting structure is equivalent to two capacitors connected in series that can withstand double the voltage of the individual capacitors. Even with this architecture the nominal voltage of the EDLCs is low (2.5V – 2.7V) due to the properties of the electrolyte and the carbon.

2.1.2 Tradeoffs and comparison with other energy storage technologies

Even though it is an electrochemical device, the storage and the release of the electrical charge takes place without any chemical reactions, thus the instantaneous power available is mainly limited by the equivalent series resistance (ESR) of the capacitor. A second benefit derived immediately from the high instantaneous power of EDLCs is the reduced charging time.

Also, because it involves no chemical reactions, the charge-discharge process is highly reversible. The number of charge-discharge cycles can reach up to the order of one million without any memory effects or degradation of the properties.

The main drawbacks of ultracapacitors are the low voltages of the cells (2.5V to 2.7V), high-self discharge rate (compared with conventional electrochemical batteries) and the output voltage variation with the instantaneous value of the stored energy. The low voltage of the units requires series connections in order to obtain higher voltages. As a result of different discharge rates between cells, voltage balancing circuits are needed to ensure the charge in each cell is equivalent over many cycles.

The fact that the output voltage is not constant during the discharge process has two consequences: firstly additional converter circuits are required to provide a constant output voltage; and secondly, it is not practical to use all of the stored energy. The second issue is not as bad as it might seem due to the quadratic proportionality between the energy and the output voltage. In this way an EDLC fully charged at a nominal voltage of 2.7V and then discharged to 0.8V leaves only 8.8% of the total energy unused.

A summary of the EDLC tradeoffs is presented in the following.

Advantages:

- High specific power
- High charge / discharge current (up to hundreds of Amperes)
- Rapid charging
- Increased lifetime (up to one million cycles)
- Low ESR
- Broad operating temperature range: -40ºC to +65ºC
- Low cost per cycle

Disadvantages:

- Low nominal voltage per cell (2.5V to 2.7V)
- Low energy density
- High self-discharge rate (compared with electrochemical batteries)
- Output voltage varies with the energy stored

Before going further it is important to have an overview of the current battery technologies that ultracapacitors are competing with. Table 2.1 summarises these parameters.

	Lead - Acid	Ni-Cd	Li-Ion	EDLC
Energy capacity	~35Wh/kg	~50Wh/kg	120Wh/kg	~6Wh/kg
Life-cycle (nameplate cycles)	~500	~1200	~4,000	1,000,000

Table 2. 1. Comparison of the parameters for energy storage devices

2.1.3 EDLC characterisation and modelling

As the aim of this project is to reduce the charge time of the ultracapacitors to a minimum, it is important to evaluate and model the behaviour of the ultracapacitors under various operating conditions. Most of the traditional electrolytic capacitor parasitics can be represented using the basic model presented in figure 2.2. The equivalent series resistance (ESR) is very small (of the order of mΩ) and it is composed of the electrode resistance, electrolyte resistance and the contact resistance. On the other hand the equivalent parallel resistance (EPR) is very large and represents the self-discharge rate of the capacitor.

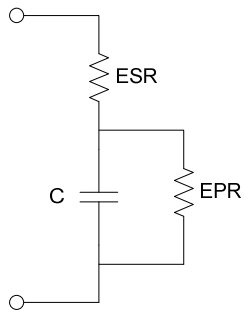


Figure 2. 2. Basic model of a capacitor

Laboratory charge and discharge tests for ultracapacitors show a series of effects that are not included in the basic model of the capacitor. Figure 2.3 shows the step response of a EDLC when subjected to a 3.5A load current. It can be observed that the output voltage presents an exponential response as a result of the high freqeuncy components of the rising and falling edge. For an electrolytic capacitor the terminal voltage would show a square-wave shape with amplitude determined by $\Delta V_{OUT} = \Delta I_{LOAD} \times ESR$.

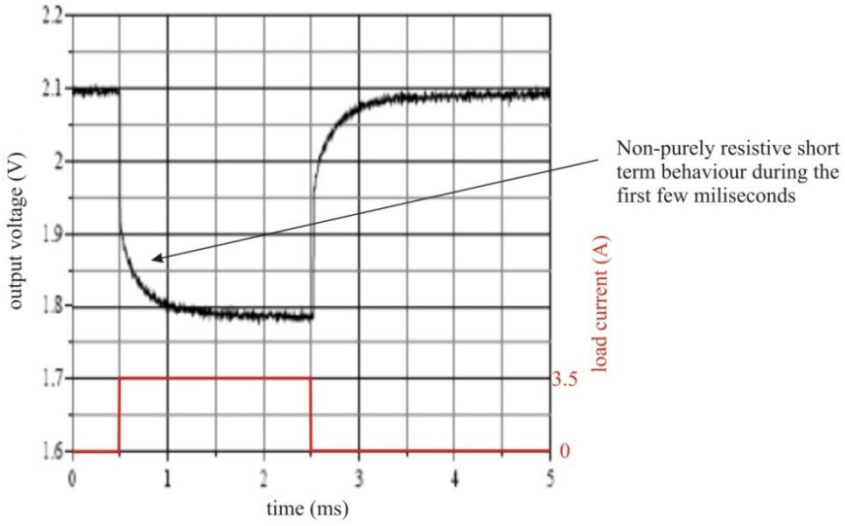


Figure 2. 3. Single pulse discharge of a 10F cell [9]

Two other non-ideal behaviours can be observed during the long transient measurements, presented in figure 2.4. The first one is the variable slope of the output voltage when charged with a constant current. This indicates the presence of a variable capacitance component that is function of the cell voltage. A better view of the variation of the nominal capacitance with the output voltage can be observed in figure 2.5 for a full charge process. The second effect is the charge redistribution after the input current is removed. This behaviour can be explained by considering the porous nature of the electrodes and the ions diffusing inside the spiral wound capacitor.

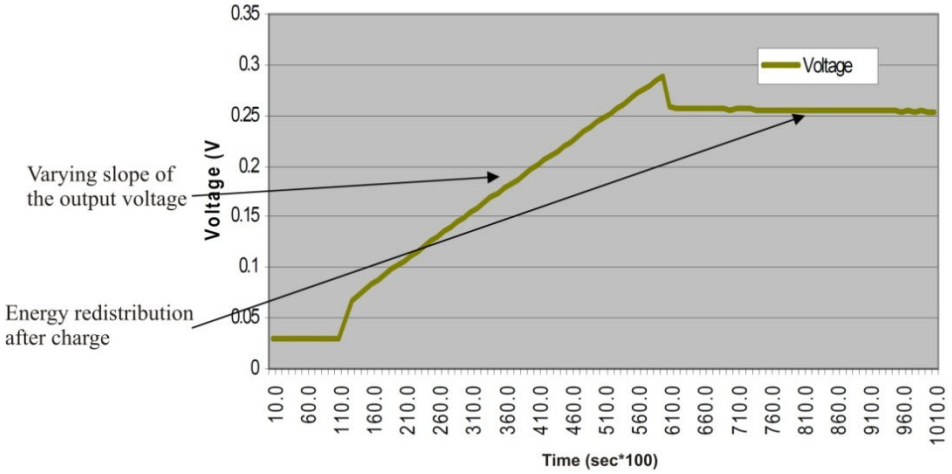


Figure 2. 4. 100 Amps constant current charge pulse [9]

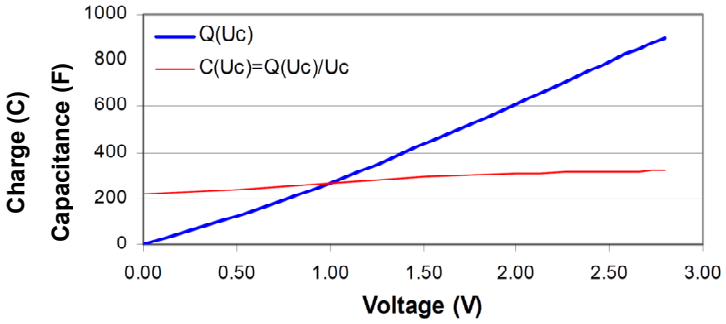
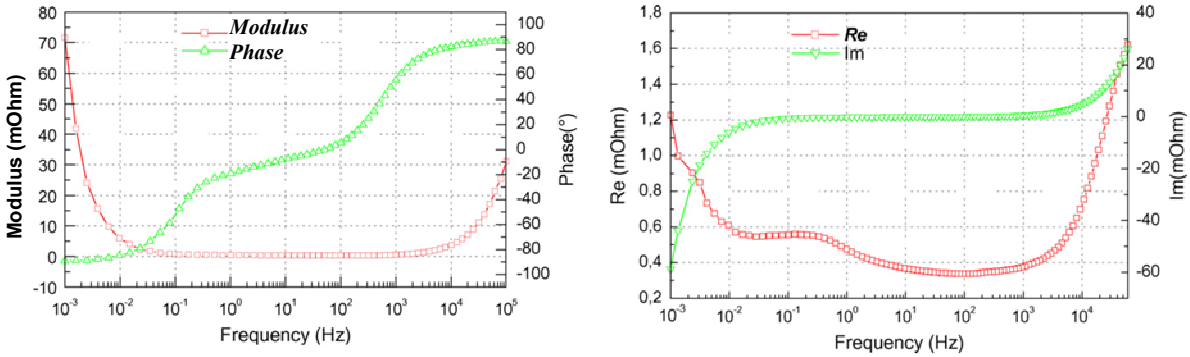


Figure 2. 5. Charge and Capacitance vs. Terminal Voltage [9]

A very comprehensive set of impedance spectroscopy tests are presented in [10]. The measurements have been done for a 2600F/2.5V ultracapacitor in the [1mHz; 60kHz] frequency range.Figure 2.6 a) presents the modulus and the phase versus frequency, while figure 2.6 b) depicts the real and imaginary parts versus frequency.



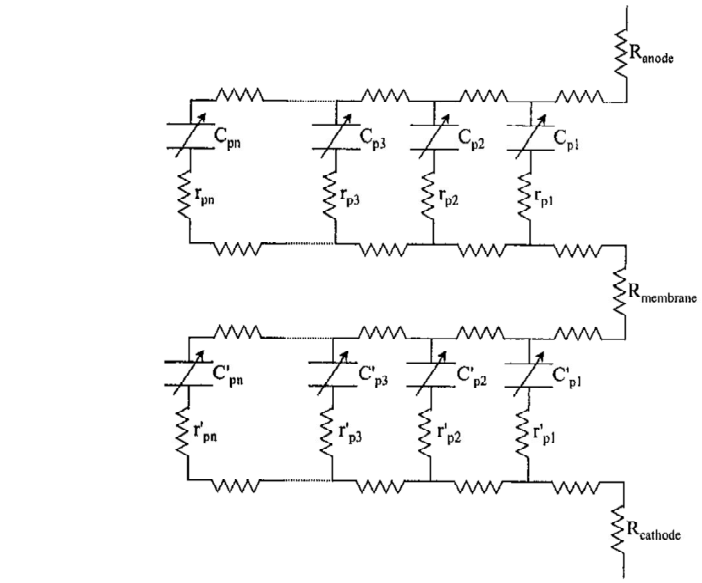
a) **b)**

Figure 2. 6. a) Modulus and phase of the ultracapacitor impedance;
b) Impedance real and imaginary parts vs. frequency [10]

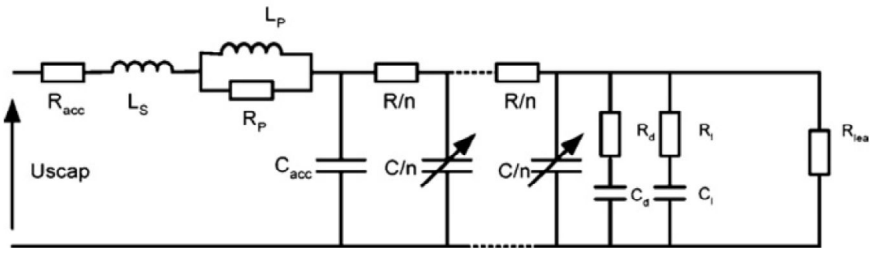
Three main aspects can be observed in the spectroscopy tests. First for very low frequencies (<10mHz) the behaviour of the EDLC is mainly capacitive and the magnitude is relatively high. Second, in the medium frequency range [10mHz; 1kHz] the behaviour becomes resistive with a minimum magnitude of 0.27mΩ. Finally for frequencies over 5kHz, the phase shift is above +80º (inductive behaviour) as the impedance real part increases with frequency [10].

Several electrical models have been presented [9-13] and all the opinions seem to converge towards the transmission line electrical model. As the EDLC has a very complex behaviour, the modelling also depends on manufacturing technology, the purpose of the application and measurement conditions. The architecture presented in figure 2.7 a) is very close to the physical construction of the ultracapacitors and the analysis presented in [13] is an

excellent starting point. The general model presented in [10] (figure 2.7 b) provides a very useful description for very low and high frequencies, introducing the inductive (L_S) component for high frequencies.



a)



b)

Figure 2. 7. Electrical models for EDLC; a) double transmission line [13], b) single inductive line [10]

The voltage dependence of the capacitance has been modelled in both topologies by the variable capacitors. The charge redistribution at low frequencies and the leakage current are represented by the resistor introduced in series with the transmission line. Values of the components are determined by measurements under different conditions and identification of the values with the components of the model. For the 2600F ultracapacitor tested in [10] the following values were obtained: R_{acc}=0.27mΩ, L_S=50nH, C_{acc}=200F, C=1900 + 360×V, R=0.54mΩ (see figure 2.7 b).

2.1.4 EDLC applications

The very high specific power and reduced charging time make the EDLC very suitable for short-term energy storage. There are two main directions of interest. The first one comes from the automotive, industry while the second one targets the energy storage for portable

devices. Transportation engineering has been using ultracapacitors for regenerative braking, electromagnetic valve control, electric power steering, augmentation of the electrical system for loads that require large transient currents (i.e. electric power steering, electric air compressor, etc) [15] and start-stop engines. Also, EDLCs represent a very promising solution for the Hybrid Electric Vehicle (HEV), relieving the load on the battery during high power requirements. A good alternative for public transportation is presented in [14] by an electric bus that is entirely powered by inductively charged ultracapacitors.

Portable devices have a major limitation due to the increased charging time of the batteries. Also, batteries cannot deliver high instantaneous power levels, and because of this many devices have to be powered from the mains, event hough the overall energy consumption could be supplied by batteries (UltraCut cordless tubing cutter) [56]. The toy industry is also a significant target as most children cannot wait 90 minutes or more for the batteries to recharge. Cordless hand tools are also in the same group, as batteries are recharged several times a day, leading to the need of spare batteries to compensate for the slow charging cycle.

Other applications include the storage of energy generated from green energy sources [16], regenerative power elevators [17], pallet trucks, etc.

2.2 Project guidelines

As presented in the introduction, in a first instance, the aims of the project are to design a very fast charger that could push to the limit the power delivered to ultracapacitors from an AC mains supply.At a first view the idea of charging an ultracapacitor seems trivial. Previously reported devices focus on the charging of high voltage capacitors for aerospace and industrial applications such as X-ray imaging, lasers, RF generation, etc. The main problem of the capacitors is that the output voltage starts from zero volts, condition equivalent to output terminals short circuit. As the final implementation of the design is a fast and compact IC driver, the main restriction is imposed by the losses on-chip and in the magnetic components. Therefore the system has to provide high efficiency regardless of the output voltage. The high-frequency model of the ultracapacitors also sets strict limitations on the output current transients in order to limit the self heating of the capacitors.

As the nominal voltage of the EDLCs is relatively low (≈2.7V) several cells are connected in series to achieve a higher voltage. For this implementation we will consider the case of six capacitors connected in series, with a total voltage of 16.2V.The maximum power delivered by the device was set to 250W and the output current limited to 30A, values that

will allow a compact size of the magnetic components and reasonable power dissipation for a monolithic IC.

Another design limitation derives from the thickness of the wires between the charger and the capacitor pack. The energy dissipated in the wires is$P_{wire} = I_{out}^2 R_{wire}$. To achieve low heating of the cable we must therefore use short and thick wires. If the waveform of the output current has high frequency AC components we must also consider the skin effect, which will further increase the power dissipation. The minimum copper wire diameter recommended for 30A DC current is 2.6mm. The power dissipation for a one meter long cable (d=2.6mm) is approximately 6.3W ($R_{wire/1m}$=7mΩ). Clearly the overall cable diameter would be over 1cm including the insulation, a fact that would make the handling of the charger difficult. As a solution, we aim for a very compact device that could be integrated with the capacitor pack and thus reduce the length of the conductors to a minimum.

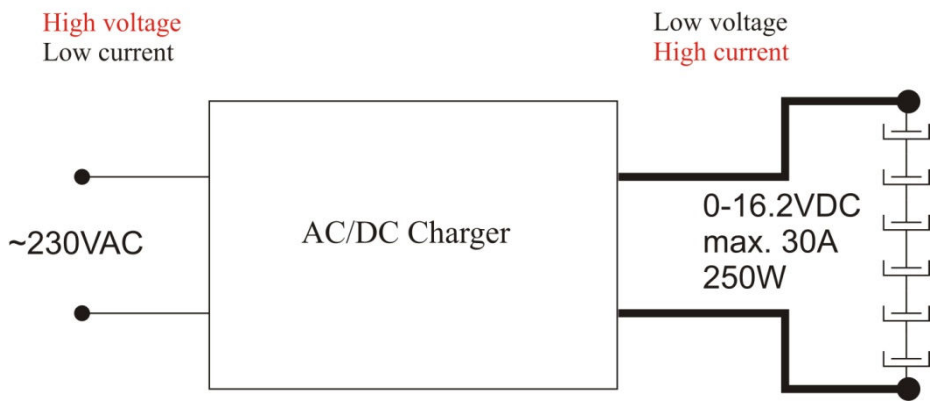


Figure 2. 8. Block diagram of the charger concept

2.3 Market status

Very few papers have been presented so far on the topic of charging ultracapacitors from the mains network (230VAC). Several reports present chargers powered by a DC voltage source [18], battery, fuel cell or photovoltaic cell [19],[20]. A high power charger powered from the mains network is presented in [21]. This device includes an adaptive control system that maximizes the output current, but comes with the drawback of large volume and need of water cooling.

A compact low power mains charger is described in [22]. The device is based on the flyback converter architecture with self oscillating control system, shown in figure 2.9. The control system allows an efficient management of the power throughput, but the main

limitation of the architecture still remains the output power and the pulsating waveform of the output current. The flyback topology has the main benefit of being a very low cost solution and it is suitable to provide an output power up to about 200W in a practical compact implementation. The limitation of the output power comes from the fact that the transformer doesn't transfer the energy directly to the output and operates only in the first quadrant of the magnetic hysteresis.

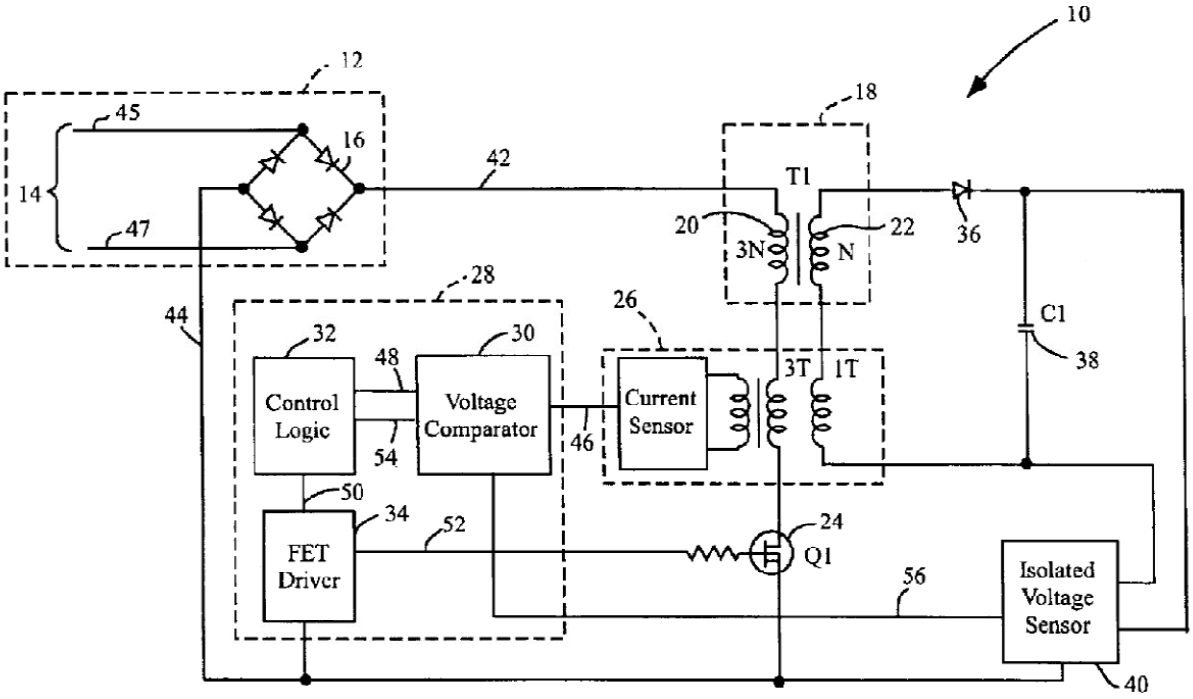


Figure 2. 9. Structure of the self-oscillating flyback charger [22]

2.4 Converter architectures

As we have seen in chapter 2.2 one of the main tasks of the charger is to perform the conversion from high voltage and low current to low voltage and high current. This leads us to the choice of an insulated converter configuration (i.e. based on a magnetic transformer). If we were to use a non-insulating topology like the Buck converter then peak magnitude of the input and output current pulses would become equal. Hence the conversion would involve very short and high amplitude current pulses being drawn from the mains network. The isolated topology is preferred from a safety perspective as it provides galvanic insulation between the mains AC network and the low voltage output of the converter.

If we continue with the example of the buck converter, where the inductor current equals the output current, the peak input current is also equal to the output current. Therefore if I_{OUT} = 30A the peak input current would also be approximately 30A and the instantaneous

power drawn from the mains reaching up to 9.6kW (depending on the value of the sinusoidal voltage at the moment when the switch is turned on). It is clear that such high current pulses would cause serious damage even to an industrial mains network. The duty cycle of the converter (V_O/V_I) would also be very small (<5%) due to the very small conversion ratio.

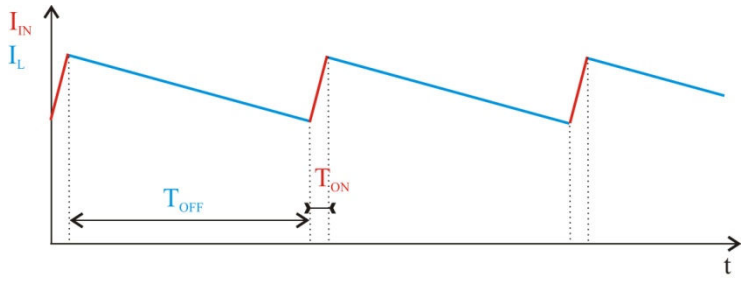


Figure 2. 10. Buck converter current waveforms

Depending on their magnetic cycle, the insulated converter topologies can be divided into two categories, asymmetrical and symmetrical. An insulated converter is called asymmetrical if the magnetic operating point remains in the same quadrant of the B-H loop. All the other isolated converters are called symmetrical.

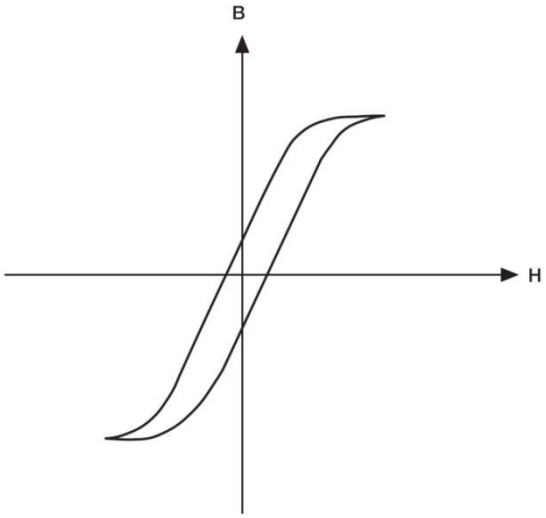


Figure 2. 11. B-H plot of the symmetrical converters

The class of asymmetrical converters is comprised of four main topologies: flyback, two-switch flyback, forward and two-switch forward, see figure 2.12 a, b, c and d, respectively.

The flyback converter (figure 2.12.b) is well known for its simplicity, reduced part-count and basic control logic. The low-cost attribute has made this configuration a favourite for low power applications. During the ON-time of the switch, the energy is stored in the magnetic core of the transformer through the primary winding. The energy is transferred to

the output by the secondary winding during the OFF cycle. As the energy transfer is made in two steps, rather than direct transfer during the ON cycle, this topology is suitable for low power applications, up to 200W.

The two-switch flyback converter (figure 2.12.b) adds a high-side switch and two clamping diodes for the protection of the switches during the OFF-time. The non-dissipative clamping of the voltage across the switches allows higher switching frequencies and a better efficiency than the single switch flyback.

The forward converter (figure 2.12.c) can be considered the ideal alternative for applications that require medium power levels, due to the higher maximum duty cycle. In this case the transformer consists of three windings, primary, secondary and demagnetizing winding. The energy is transferred directly from V_{IN} to the output during the ON-time of the switch. When the switch is turned OFF the output inductor current is freewheeling through diode D2 and the energy stored in the core is returned to the input by the demagnetizing inductance in series with diode D3. The voltage drop on the switch during the demagnetization time is double the input voltage plus the voltage spike due to the leakage inductance of the primary.

The double-switch forward configuration includes a second high-side switch and two clamping diodes. The voltage drop on the two switches equals the input voltage and no additional snubber / clamping circuit is required.

Symmetrical converters have the main benefit of a higher duty cycle and a better usage of the transformer. The OFF-time can be reduced as the energy stored in the core doesn't have to be discharged during this interval. Hence the minimum OFF-time is determined by the switching times and the leakage inductance. The most common structures in this case are the push-pull, half-bridge and full-bridge converters.

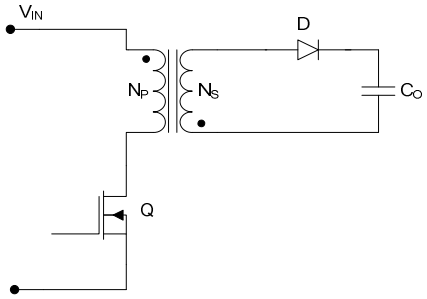
All the above topologies have in common the output inductor which provides a DC current to the load and forces the current through the secondary to a high value when the switches are turned on. This way, the current in the primary winding is composed of the magnetizing current (determined by the B-H loop) and the output current reflected in the primary. Therefore the energy transferred mostly depends on the output current and duty-cycle.

The push-pull (figure 2.12 e) requires only two low-side switches, but has a four-winding transformer and it also requires damping of the voltage spikes generated by the leakage inductance. During the ON-time the two switches are alternately turned on. A dead-

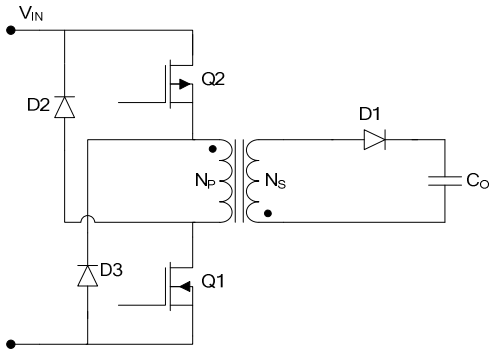
time is required between the ON time of the individual switches to avoid cross-conduction and the discharge of the leakage inductance of the primary windings. The benefit of using only two low-side switches is slightly lessened by the requirement to handle the voltage drop during OFF time that goes up to twice the input voltage plus the leakage inductance spike.

The drawbacks of two primary windings and high voltage switches are eliminated by the half-bridge converter (figure 2.12 f). The cost of this is a high-side switch and two large capacitors in series that fix the mid-point so that the voltage drop on both switches during OFF-time is $V_{IN.}$

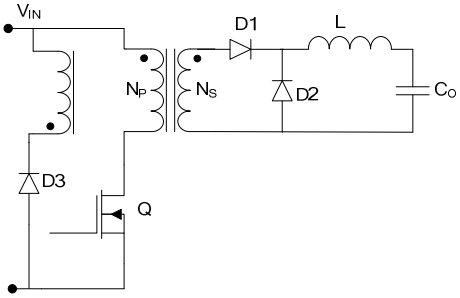
The full bridge converter (figure 2.12 g) doubles the power delivered by the half bridge but it also doubles the switching and conduction losses of the transistors. Due to the use of two high-side switches, an IC driver can be difficult to implement. On the other hand a better usage of the transformer is achieved and the duty cycle can go to higher values than previous solutions. Figure 2.13 presents a comparison of the optimal power range of the topologies presented above, suitable from the efficiency and converter size perspective.



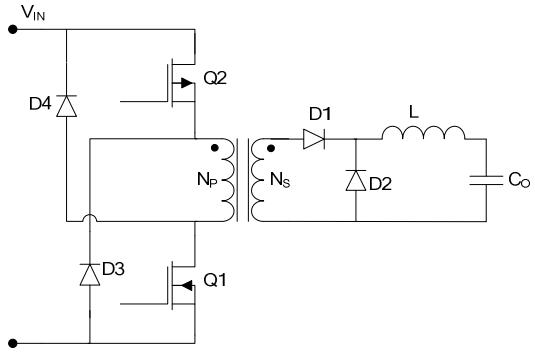
a) Flyback



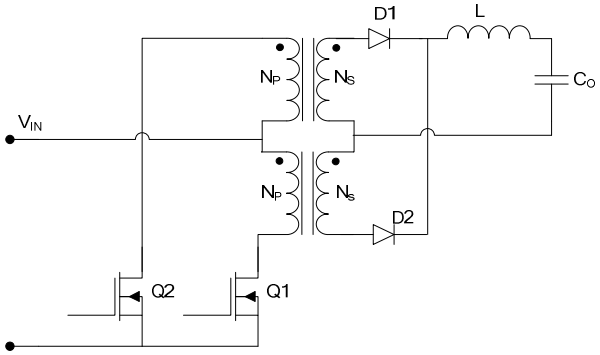
b) Two-switch flyback converter



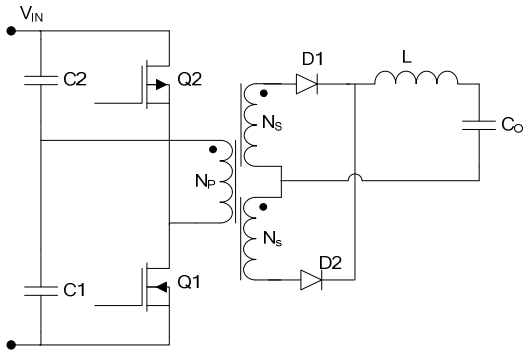
c) Forward converter



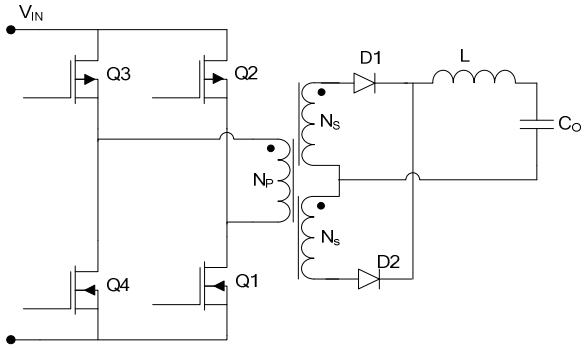
d) Two-switch forward converter



e) Push-pull converter



f) Half-bridge converter



g) Full-bridge converter

Figure 2. 12. Insulated converter architectures

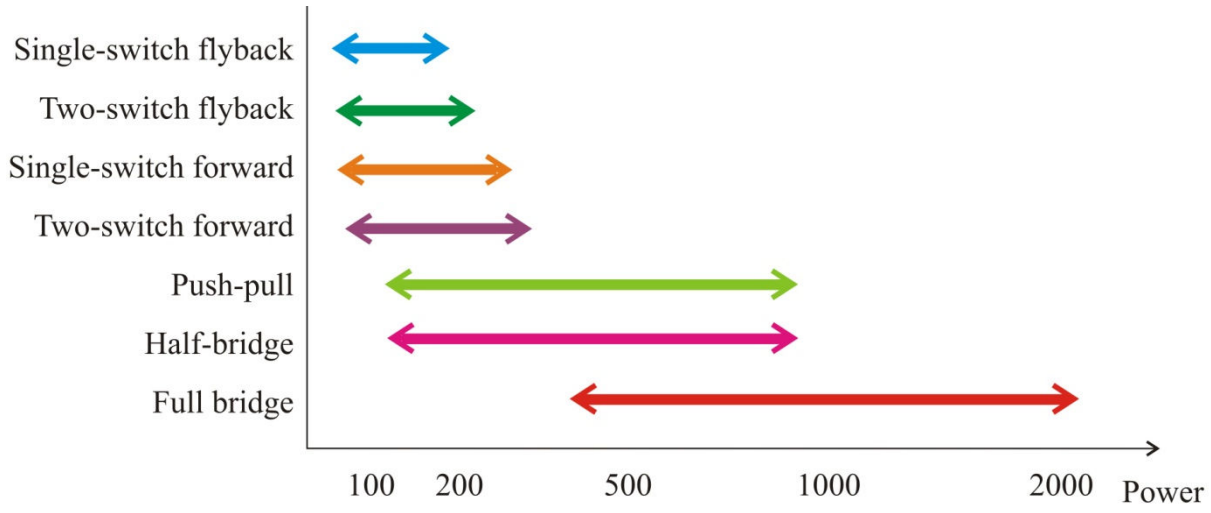


Figure 2. 13 Optimal power range chart for the insulated converter topologies

2.4.1 This work's architecture choice

After comparing the tradeoffs between the above topologies, we have selected the push-pull converter topology as the main focus of the subsequent design study for the following reasons:

- DC output current – allows the operation of the converter at the high frequencies regardless of the inductive behaviour of the EDLC
- Only two low side switches required – internal or external HV devices can be driven easily by a IC driver and will provide a low power dissipation on chip
- Medium output power
- The ratio between the input and output voltage of the transformer(N_P/N_S) will be large and therefore the output current reflected in the primary will be small, thus low conduction losses in the primary windings and switches

The drawbacks of this architecture are:

- Two primary windings – larger transformer and higher copper losses
- Complex control system and accurate timing of the switching transistors to avoid flux imbalance

2.5 Detailed description of the push-pull converter

The name of the push-pull converter comes from the magnetic cycle of the transformer, depicted in figure 2.14. When switch Q1 is on and Q2 is off (see figure 2.15.a) the core magnetic flux density (B) and the magnetic field intensity (H) are increasing and the operating

point of the transformer moves from point B to A (red path). In the same way, when Q1 is off and Q2 is on, the input voltage pulls-down the operating point from A to B (green path).

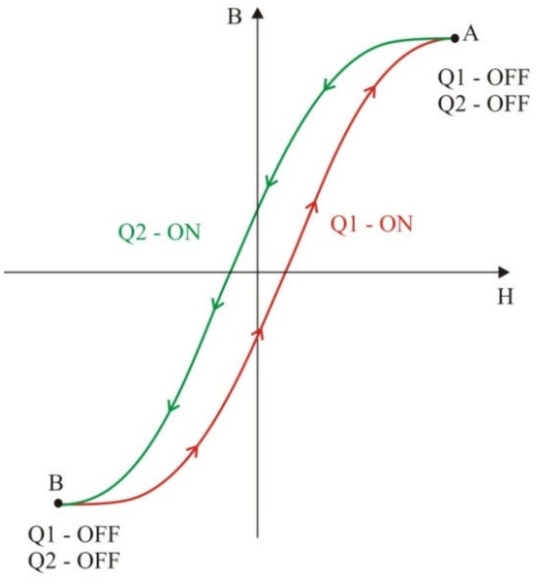
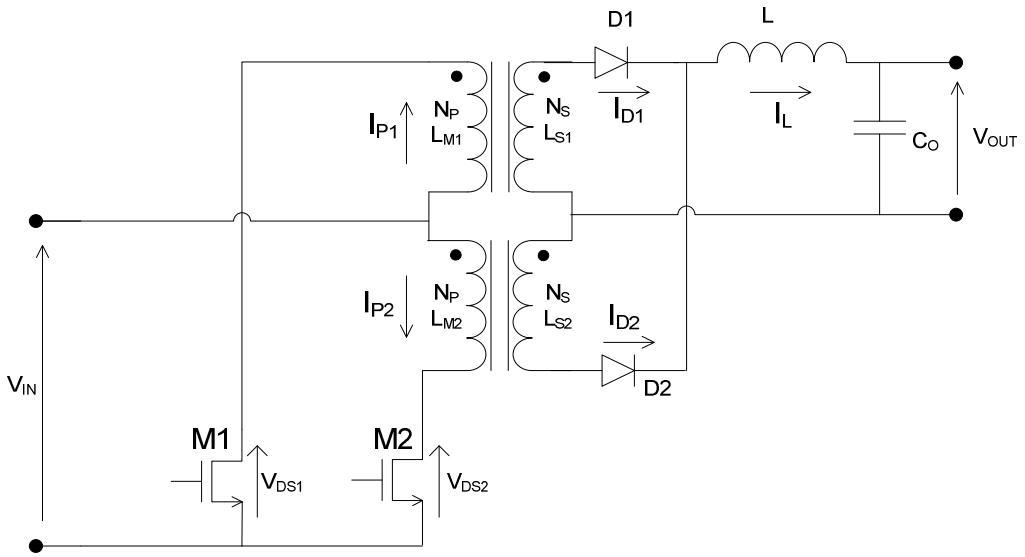
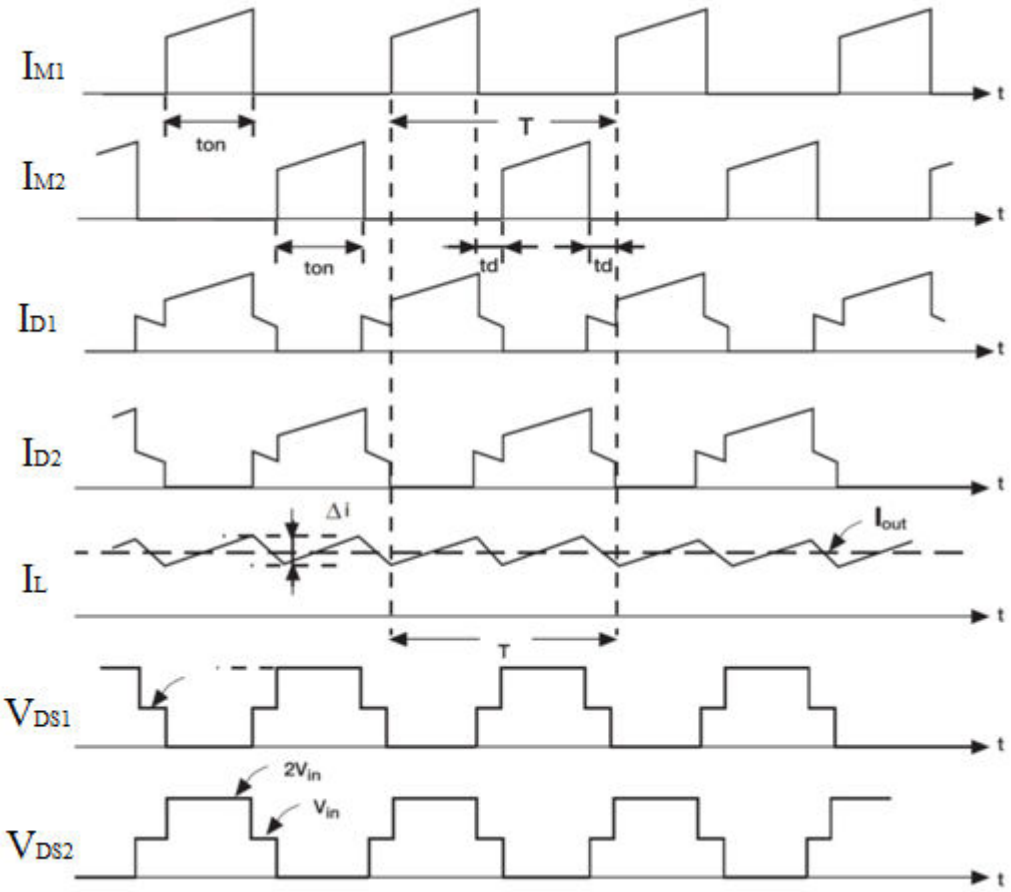


Figure 2. 14. B-H plot for the push-pull converter

Figure 2.15 a) and b) present the detailed schematic of the push-pull converter and the corresponding waveforms, respectively. Each operating cycle of the converter comprises of four successive phases: 1: Q1 – on, Q2 – off; 2: Q1 – off, Q2 – off (dead time); 3: Q1 – off, Q2 – on; 4: Q1 – off, Q2 - off (dead time). During each phase only two windings of the transformer are driving the current.



a)



b)

Figure 2. 15. a) Schematic of the push-pull converter b) waveforms for the push-pull converter

During phase 1 the input voltage drops over the primary winding L_{M1}. The magnetic flux induced in the primary generates a voltage pulse in the secondary windings with an amplitude set by the input voltage and the transformer winding ratio (Np/Ns). Diode D2 is forward biased and the entire load current passes through winding L_{S2} and D2. Diode D1 is reversely biased and no current passes through L_{S1} and D1. The unused primary winding, L_{M2} outputs a voltage equal with the voltage drop on L_{M1}, and forces the potential in the drain of M2 to approximately $2V_{IN}$.

During phase 2 and 4, as both switches are OFF, the current through the primary windings is zero and the voltage drop on both transistors is equal to V_{IN}. On the secondary side the output inductor forward biases D1 and D2, with the current through each diode and secondary winding being half of the inductor current. As the currents in the secondary windings are in opposite senses, the magnetization forces of the two windings cancel and the magnetic operating point remains fixed (points A and B on figure 2.14). The voltage drop on

the secondary windings is very small, determined by the product between the current and the wire resistance.

Phase 3 is similar to 1, but in this case the current in the primary side is driven by M2 - L_{M2}, and in the secondary by L_{S1} - D1- L. The voltage drop on the output inductor during phase 1 and 3 is given by equation 2.2.

$$V_{L0} = (V_{IN} - V_{DSON})\frac{N_P}{N_S} - V_O - V_D \qquad (2.2)$$

Where V_{IN} is the input voltage, V_{DSON} is the voltage drop on the switch when on, N_P and N_S are the primary and secondary number of turns respectively, V_O is the output voltage and V_D is diode forward voltage drop.

The output current during the on phases (phase 1 and 3) is:

$$I_O(t) = I_{Lmin} + V_{LO}\frac{t}{L} \qquad (2.3)$$

Where *t* is the time from the moment Q1 or Q2 is turned on, I_{Lmin} is the output current at the beginning of the phase and *L* is the inductance of the output inductor.

The current through the primary windings during phase 1 and 3 is composed of the magnetizing current (given by the B-H loop) and the secondary current reflected in the primary (with a ratio of N_S/N_P). Figure 2.16 presents the dependency of the magnetizing current on the magnetic cycle of the transformer. The equation of the primary current during the on phase is:

$$I_P(t) = \frac{1}{L_{Pm}}\int_0^t V_{IN}\,dt + I_O(t)\frac{N_S}{N_P} \qquad (2.4)$$

Where L_{Pm} is the magnetizing inductance of the primary windings (L_{M1} and L_{M2} in figure 2.15 a).

Under steady-state conditions and with a pure capacitive load for the converter, the rise of the output voltage during ON and OFF phase is:

$$\Delta V_O = \frac{1}{C_O}\int_0^{t_{ON/OFF}} I_L dt$$

or
$$\Delta V_O = \frac{I_{Lmin}+I_{Lmax}}{2} \times \frac{t_{ON/OFF}}{C_O} \qquad (2.5)$$

Where I_{Lmax} is the current at the beginning of the phase and C_O is the output capacitance.

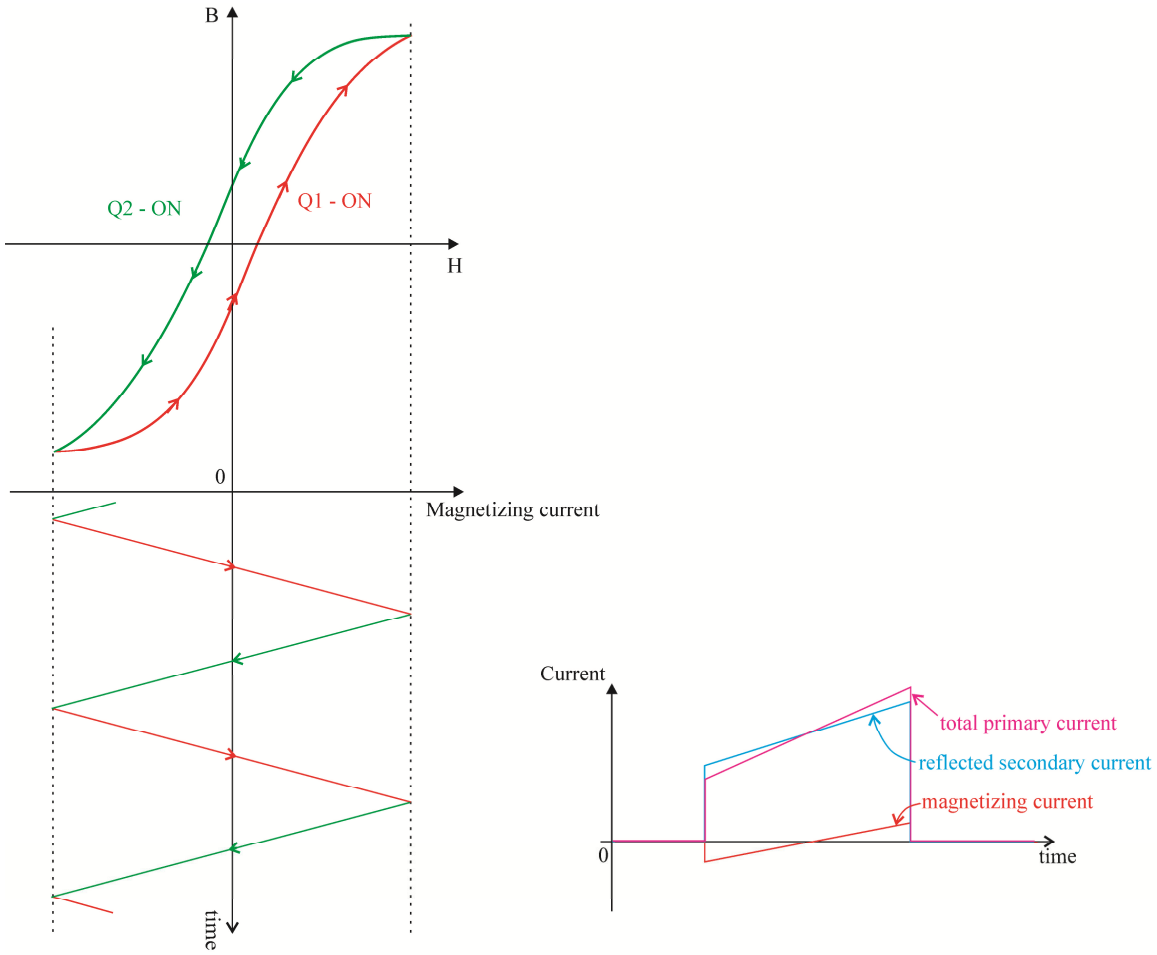


Figure 2. 16. Waveforms of the magnetizing and primary winding currents

During the OFF phases (phase 2 and 4) the fall of the output current is given by:

$$I_O(t) = I_{Lmax} - \frac{1}{L}\int_0^t (V_O + V_D)\, dt \qquad (2.6)$$

where all the symbols have the same meaning as above.

2.6 Sources of losses in the push-pull converter

All the components of the converter, except the capacitive load (considered ideal in this case) dissipate energy during the operation of the converter. As mentioned before, one of the benefits of the push-pull topology is that it has only two low-side switches and therefore reduced power dissipation. In the following discussion we will analyse the losses and the parameters that influence them.

The main sources of losses are:

- Power switches
  - Conduction losses
  - Switching losses

- Transformer
    - Wire losses
    - Core losses
- Diodes
    - Conduction losses
- Output inductor
    - Wire losses
    - Core losses

As the final design is aimed to be implemented in a monolithic driver using a high voltage CMOS process, the power switches can be implemented as MOSFETs or IGBTs. As we are aiming for high duty cycles and therefore reduced switching times, we have decided to use field effect transistors. In order to model the conduction losses the FET can be seen as a voltage controlled resistor, with the control voltage given by the gate-source voltage (V_{GS}). For the analysis of the switching losses we have to look at the parasitic model of the MOSFET, figure 2.17.

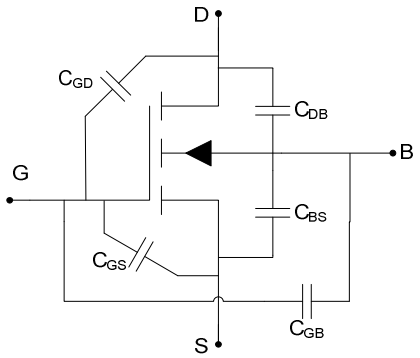


Figure 2. 17. MOSFET parasitic model

In terms of switching losses the parasitic capacitances of interest are C_{GS}, C_{GD}, C_{DS} and $C_{DB.}$ The gate-drain capacitance is of particular interest because it has to be discharged and charged by the driver from approximately 310V to $-V_{GS}$ at the beginning and the end of phases 1 and 3, respectively.

The wire losses in the transformer can also be split in two categories: DC current loss and AC current loss. The wire losses due to AC current will increase with the frequency and magnetic field due to the skin effect and proximity effect, respectively. The skin effect is the tendency of the high frequency currents to flow in the thin outer skin of the conductor. Figure 2.18 illustrates the distribution of the current in the wire due to the skin effect.

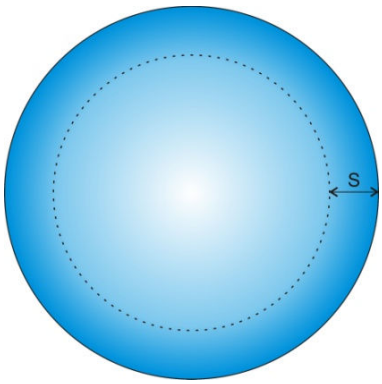
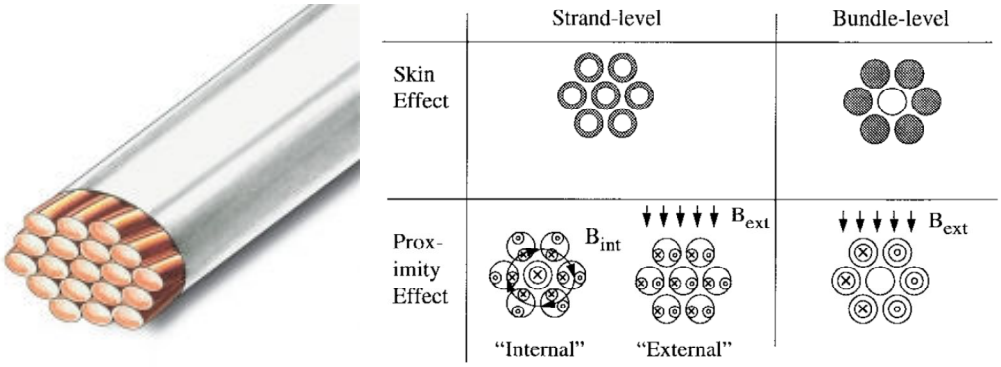


Figure 2. 18. Current distribution in the conductor due to the skin effect

Proximity effect is the tendency of current to flow in different concentrated distributions due to the presence of magnetic field generated by nearby conductors. Both skin effect and proximity effect can be attenuated by the use of stranded litz wire. This type of wire is usually used within the frequency range 10kHz to 1MHz. Litz (contraction from Litzendraht) wire consists of thin strands of insulated wire held together by outer covering insulation, see figure 2.19. The two effects can be further divided into strand-level and bundle-level effects [23],[24], as depicted in figure 2.19 b.



a) **b)**

Figure 2. 19.a) Litz wire structure; b) Skin and proximity effects in litz wire [24]

The pattern of the litz wire must ensure that each strand is subjected to the same external and internal magnetic field to minimize the proximity effect.

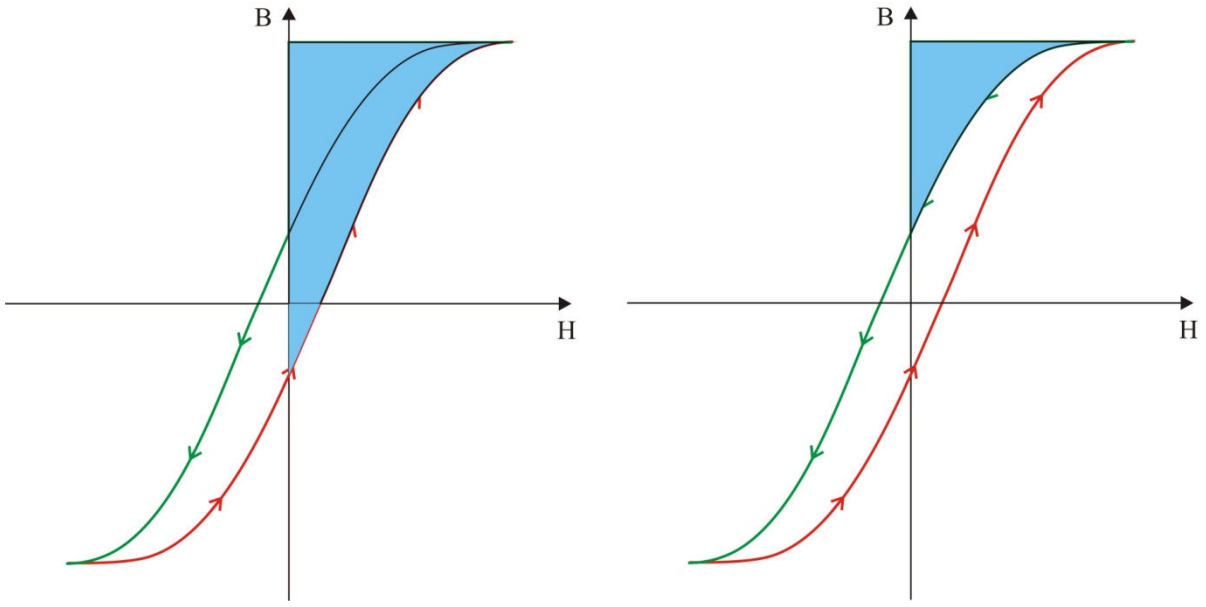
Skin depth is defined as the distance below the surface where the current density has dropped to 1/e, or 37%, of its value at the surface of the conductor. The relation between skin depth and frequency for a copper wire at 70ºC is [23]:

$$S = \frac{76}{\sqrt{f}} \qquad (2.7)$$

where S is the skin depth in mm and f is the frequency in Hertz.

The skin depth at 200kHz is S=0.16mm, therefore the litz wire single-strand radius must be smaller than this value.

The core losses in the transformer are determined by the area of the hysteresis loop. Figure 2.20 gives a representation of the energy consumed to establish the field and the energy released by the collapse of the field. Because the loss is proportional to an area it should be roughly proportional to the square of the maximum flux density. In practice the energy dissipated depends on the material, and for iron it will reduce to $B^{1.6}$ while for ferrite it will raise to $B^{2.5\text{-}2.7}$. The value for a specific material is called the Steinmetz exponent. Also the core losses will increase with the operating frequency; for ferrite this increase goes with about the 1.6^{th} power of the operating frequency, for ferrite cores [23]. It should be noted that there is no dependency between the core loss and the reflected current; it is only a function of the maximum flux swing and the frequency.



a) blue area = energy required to establish field b) Blue area = energy released by the field collapse

Figure 2. 20.Energy consumed and released by the magnetic field

The conduction losses in the diodes can be estimated easily, as the average diode current is equal with half of the DC output current. In our case if we have a constant current of 30A and a forward voltage drop of approximately 0.5V (high current Schottky diode), so the average power dissipation is 7.5W per device. Reverse recovery losses are negligible, compared to the conduction loss for the range of switching frequencies (up to approx. 200kHz).

In the output inductor the main source of loss is the resistance of the wire. If we continue the analysis started before (I_{OUT} = 30A) and a winding resistance of 50mΩ, the

average power dissipated would be 45W. Such a value would be unacceptable in a practical design, and therefore thick wires should be used to reduce the winding resistance to be of the order of 1mΩ to 3mΩ. Core losses can almost be ignored as they are determined by the AC component of the output current (in our case approximately 1A). The same argument holds for the energy dissipated in the wire due to the AC component of the current.

2.7 Power factor correction for nonlinear loads

A nonlinear load is a device that produces a non-sinusoidal load current when powered from the mains AC network. In our case in order to obtain a DC supply at the input of the converter we must use a rectifying bridge and a large capacitor. As shown in figure 2.21, the bridge will draw current from the network only when the input voltage exceeds capacitor voltage. The output ripple will be given by the load current and the value of the capacitor. As the load current is fixed, the only way to reduce the ripple of the output voltage is to increase the size of the capacitor. The cost of a well stabilized rectified voltage comes in terms of high amplitude current pulses drawn from the AC supply network.

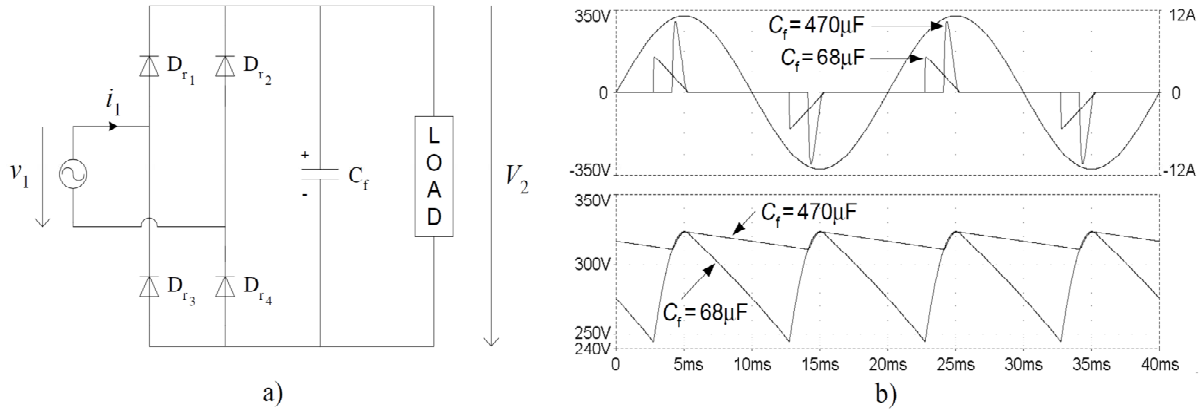


Figure 2. 21. Diode bridge rectifier: a) Schematic; b) Line voltage and line current (upper plot) and output voltage (lower plot), with V_1=230V_{RMS} and constant power load P=200W [25]

The short current pulses contain frequency components that are multiples of the mains network frequency. Figure 2.22 presents the spectrum of the harmonics generated by the current pulses, for the typical worst case values of the line: R_{line}=0.4Ω and L_{line}=800µH. The current harmonics produce a series of undesirable effects in the distribution network and home appliances [25]:

- Additional losses and overheating of: transformers, power cables, AC machines and shunt capacitors
- Reduced power factor, hence less power available from the power outlet having a certain apparent power rating

- Electrical resonances in the power system
- Distortion of the line voltage, as shown in figure 2.22 b.
- Excessive current in the neutral conductor for three-phase, four-wire systems.

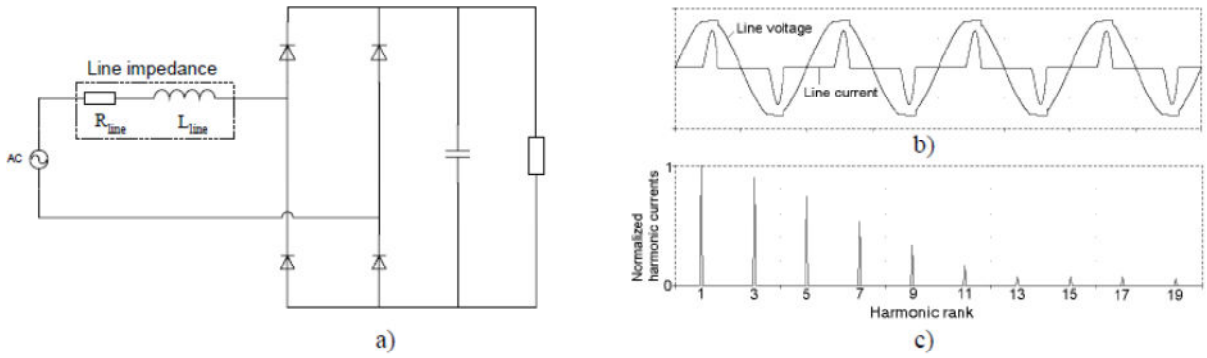


Figure 2. 22. Single phase diode rectifier: a) Schematic; b) Typical line current and voltage waveforms; c) Odd line current harmonics normalized to the fundamental [25]

Due to the previously mentioned negative effects the European Committee for Electrotechnical Standardization – CENLEC has introduced the EN61000-3-2 standard. The standard requires that all switched-mode power supplies with an output power over 75W must include as a minimum a passive power factor correction circuit (PFC). A passive filter is usually implemented as an LC filter, in different configurations. Passive PFC circuits provide a typical efficiency around 96%, while the active ones are limited to approximately 94%. On the other side passive PFC require an inductor much larger than the active ones. Figure 2.23 presents the main types of passive PFC. As the aims of this project do not include the design and optimisation of the PFC, a standard passive circuit will be used.

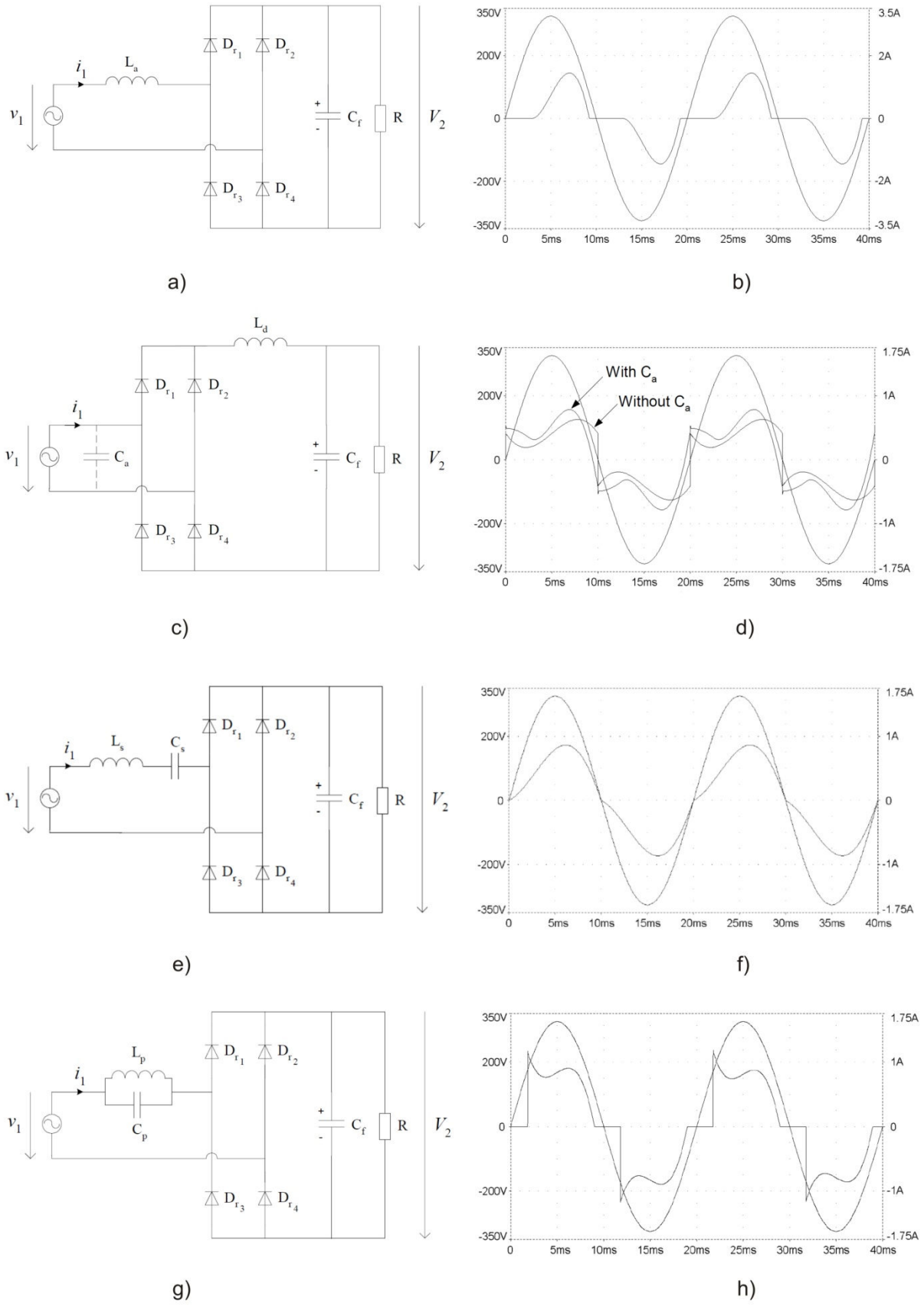


Figure 2. 23. Rectifier with AC-side inductor: a) Schematic; b) Line voltage and current waveforms Rectifier with DC-side inductor: c) Schematic; d) Line voltage and current waveforms Rectifier with series resonant band-pass filter: e) Schematic; f) Line voltage and current waveforms Rectifier with parallel resonant band-stop filter: g) Schematic; h) Line voltage and current waveforms [25]

Chapter 3 SYSTEM LEVEL CHARGER STUDY

3.1. System architecture

The structure of the EDLC charger can be divided in three blocks: rectifying and PFC block,push-pull converter power stage and the control module. As stated in the requirements chapter the system is intended to be implemented as a monolithic chip. Figure 3.1 identifies the individual parts of the system and the devices that are going to be integrated on chip.

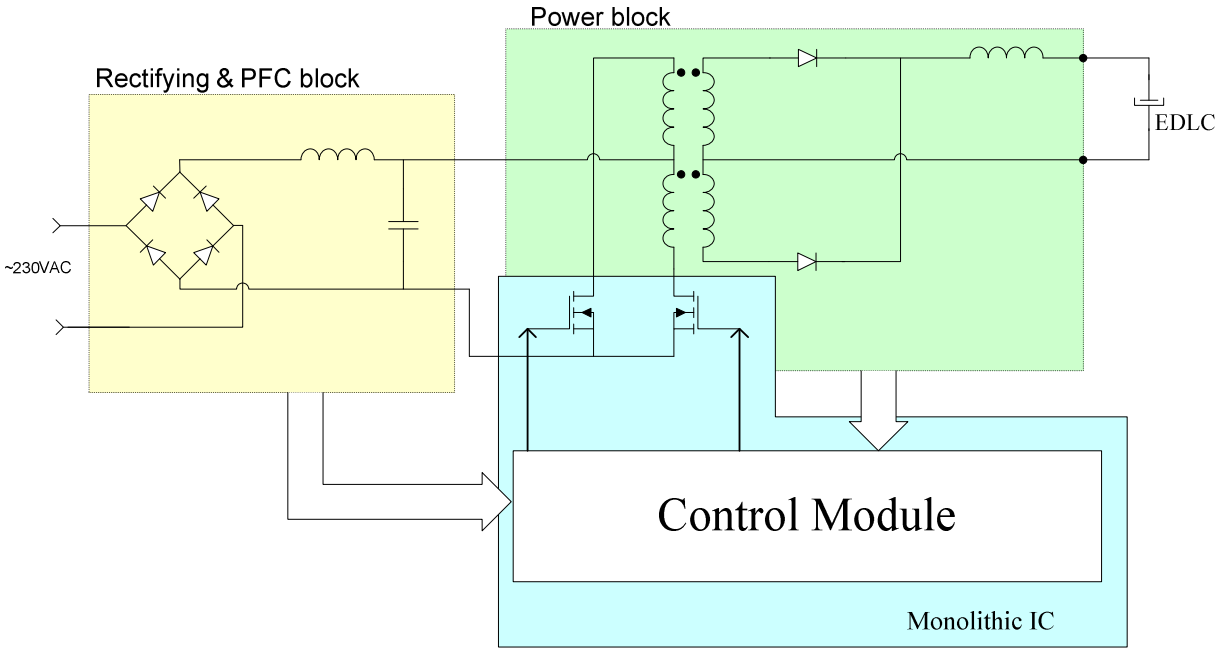


Figure 3. 1. Architecture of the EDLC charger

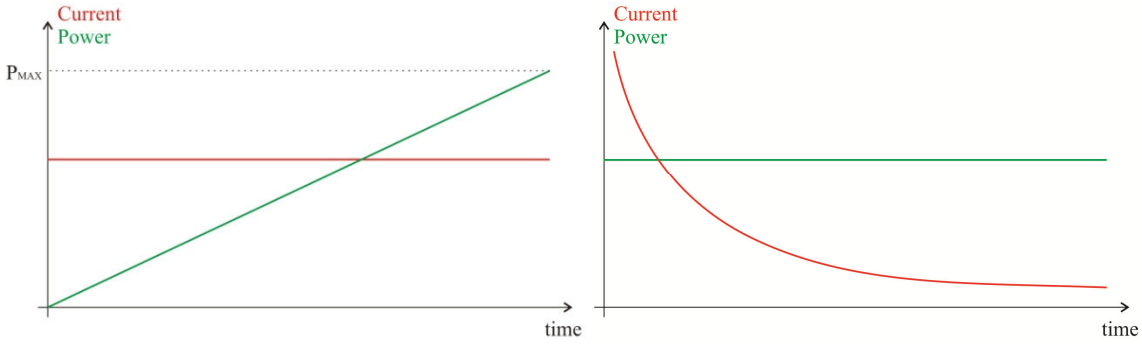
3.2. Control module strategies

Traditional AC/DC converters can be divided into three categories according to the type of control system: constant voltage (most frequent), constant current or constant power. The algorithm for regulating the output voltage (with current limitation) cannot be implemented in this case for the following reasons:

- This algorithm provides a regulated output voltage, instead of constant current or constant power, while in our case the output voltage varies broadly.
- This type of converter requires a minimum output voltage even in current limitation mode. When the output voltage is 0V, the voltage drop on the output inductor during the off time is approximately 0.5V. Thus the OFF time would be very long (tens of

microseconds), a value which would limit the operating frequency of the device to tens of kilohertz.

The constant current topology gives a fast charging process but the constraint in this case is the size of the converter. Figure 3.2 a) depicts the graph of the current and output power in this case. It can be observed that the converter delivers the maximum power only at the end of the charging cycle. Due to this the whole converter must be sized to deliver P_{MAX} (during the whole charging process) while the average power delivered is $P_{MAX}/2$. Larger transistors have to be used for the power switches, a fact that will lead to higher switching losses and low efficiency over most of the operating range. As these losses are constant during the charging process, the efficiency of the converter will be very low during the first 20-30% of the charging cycle. The magnetic components have to be larger as well, leading to a heavier and larger charger overall.



a) **b)**

Figure 3. 2. Output current (red line) and power (green line) waveforms for: a) constant current algorithm b) constant power algorithm

The final control algorithm is the constant power. In this case the current that would have to be delivered when V_O = 0V is infinite, see figure 3.2 b). The very high current requires a large output inductor, thick wires for the winding of the transformer secondary and inductor and also very large rectifying diodes at the output. On the other hand the output current at the end of the charging process would drop to low values.

The control algorithm for this design aims to combine the constant power and constant current topologies. Figure 3.3 presents the profile of the current and power for the proposed implementation. In order to boost the efficiency and reduce the size of the components, an adaptive frequency and duty-cycle regulation algorithm is used. A fast feed-forward loop is used to stabilize the current against input voltage fluctuations and a slow feedback loop used for the computation of the switch off time (dependent on the output voltage).

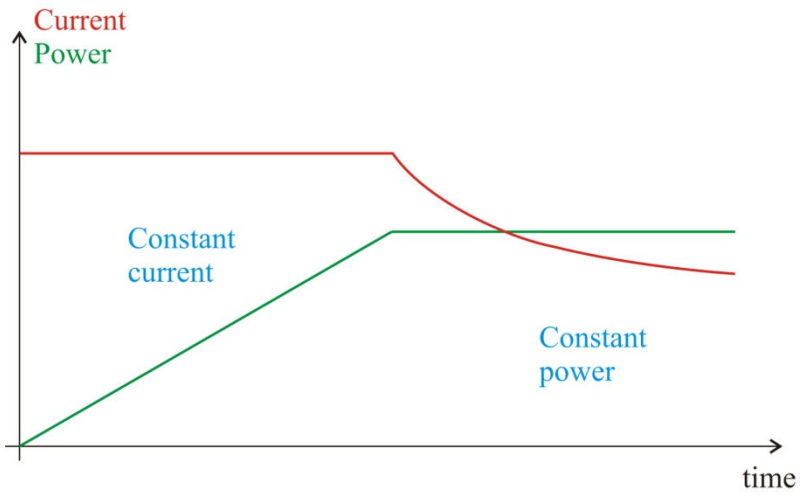


Figure 3. 3. Graph of the output current and power of the hybrid control logic

The main advantages of the hybrid control system are:

- Fast charging process
- Reduced size of the converter
- Reduced power dissipation / high efficiency
- Quasi-constant ripple of the output current
- Low cost

On the other hand the converter requires complex control circuitry tolerant of the variation of the components, temperature and input voltage.

3.2.1 Current – mode control module

As the converter needs to regulate the output current, a sense resistor has to be introduced in the current path in order to evaluate its magnitude. In a traditional implementation this resistor would be placed in series with the load, on the high side. The limitation that arises in this case is the galvanic insulation between the primary and secondary sides of the transformer. To facilitate this, the output current is monitored from the primary side and scaled by the transformer ratio. This can be achieved in two ways: using an additional transformer winding dedicated for the measurement of the current or by introducing a sense resistor in series with the main switches. The second option has been selected for the ease of simplicity, accuracy and reduced size of the transformer. The sense resistor is placed in the between the source of the switches and ground, as depicted in figure 3.4.

The current mode monitoring also helps with one of the problems that can appear in the operation of the push-pull converter, i.e. flux imbalance in the magnetic core of the transformer. This effect is usually determined by slightly unequal ON times of the main switches and leads to the 'staircase' saturation of the core. This problem is avoided by continuously evaluating of the current in the primary windings while the switches are on.

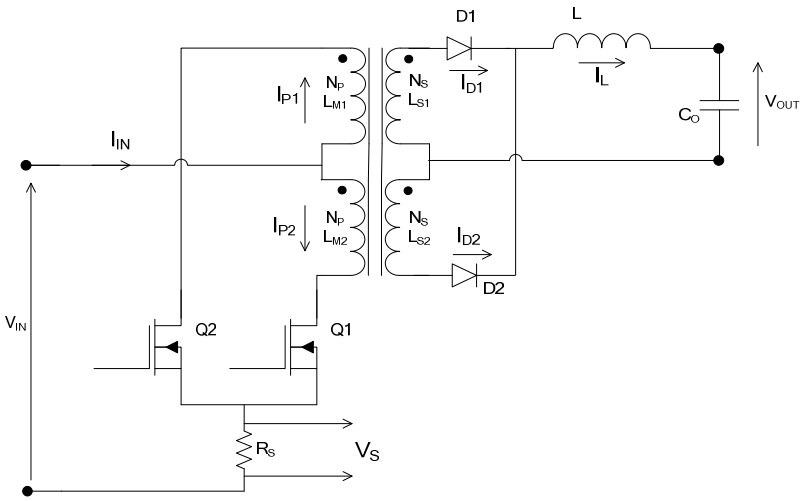


Figure 3. 4. Current-mode topology of the push-pull converter

As it has been previously shown, the primary current consists of the sum between the magnetization current of the primary winding and the output current reflected in the primary. The weakness of the current mode duty cycle regulation comes from the fact that the output current can not be evaluated while the switches are both off. Thus a regulation algorithm has been developed to overcome this limitation. Figure 3.5 shows the typical waveforms of the input and output current.

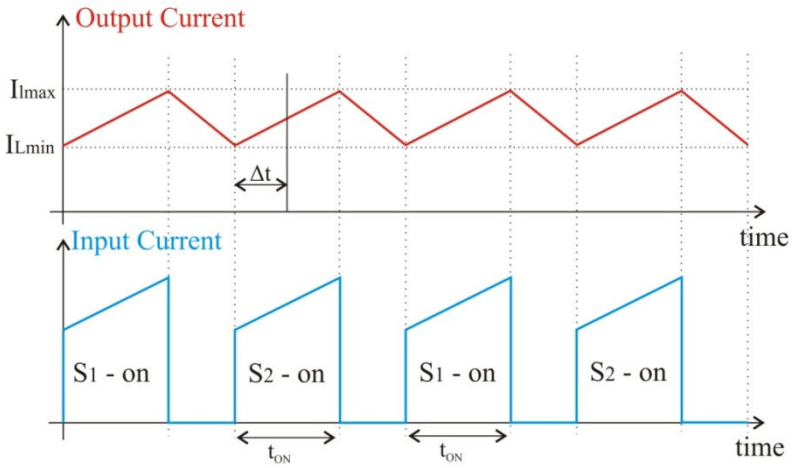


Figure 3. 5. Typical waveforms of the output current (upper plot) and input current (lower plot)

In order to avoid the saturation of the core, it is required to have equal on times for the push cycle (M1 – ON) and pull cycle (M2 – ON). This is achieved by measuring the voltage drop on R_S (see figure 3.4) and comparing it with a reference threshold value.

As we have shown before, during the ON cycles the input current can be written as:

$$I_{IN}(\Delta t) = I_M(\Delta t) + I_0(\Delta t)\frac{N_S}{N_P} \tag{3.1}$$

where I_M is the magnetizing current and I_O is the output current, see figure 3.5.

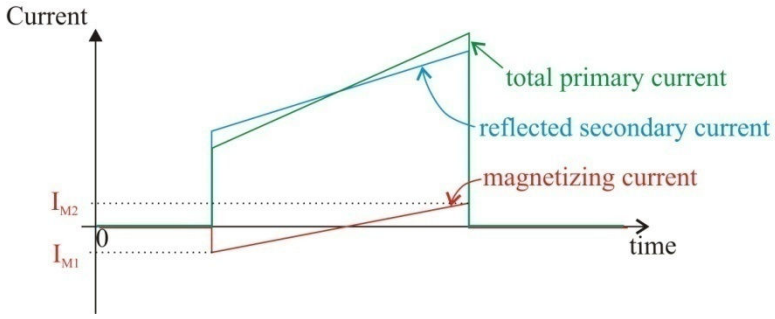


Figure 3. 6. Structure of the primary current

As the duration of the successive on cycles is constant, the magnetizing current at the end of the on phase (I_{M2} – figure 3.6) has to be equal to the modulus of the magnetizing current at the beginning of the cycle (I_{M1} – figure 3.6). The difference between I_{M2} and I_{M1} is equal to:

$$I_{M2} - I_{M1} \cong \frac{1}{L_{M1,2}} \int_0^{ton} V_{IN}\,dt \tag{3.2}$$

Because $I_{M2} = -I_{M1}$ and the input voltage can be assumed constant, under steady state operation, the value of the magnetizing current at the end of the cycle can be expressed as:

$$I_{M2} \cong \frac{V_{IN}}{2L_{M1,2}} t_{ON} \tag{3.3}$$

Thus the equation of the output current is:

$$I_0(t_{ON}) = \frac{N_P}{N_S}\left(I_{IN}(t_{ON}) - \frac{V_{IN}}{2L_{M1,2}} t_{ON} \right) \tag{3.4}$$

$$I_0(t_{ON}) = \frac{N_P}{N_S}\left(\frac{V_S(t_{ON})}{R_S} - \frac{V_{IN}}{2L_{M1,2}} t_{ON} \right) \tag{3.5}$$

where t_{ON} is the on time duration, $L_{M1,2}$ is the magnetizing inductance of the primary windings and V_S is the voltage drop on current sensor R_S.

It can be observed from equation (3.4) or (3.5) that the precise value of I_{OUT} can be obtained from the value of the input current (or the voltage drop on R_S). The second term of equation (3.4) and (3.5) can be obtained by scaling and integrating the input voltage over the length of the ON cycle. In this way the value of the output current also becomes immune to the fluctuations of the input voltage over successive cycles.

3.3 Matlab modelling of the converter

Before going further to the design of the control module it is very useful to simulate a behavioural model of the converter and extract the range of values for the main parameters such as: frequency, on time, off time, average input current, AC and RMS currents of the primary windings, power dissipation, etc. This modelling is performed from a quantitative point of view as we are interested in the evolution of certain figures during the charging process rather than the precise value. Therefore variations of 5-10% can be expected to appear between the results below and the practical ones, due to parasitics, but the trends visible are still valuable. Besides the evaluation of these parameters, the behavioural modelling has the benefit of short time simulations and allows the sweep of values in order to achieve optimum performance.

The modelling of the converter is made under the following premises:

- Output power is limited to 250W
- Output current is limited to 30A
- The ripple of the output current is constant
- The Volt x microsecond product for the transformer is limited to 742.5Vμs (equivalent to ΔB=200mT), to avoid the overheating or saturation of the core. This translates into a maximum ON time of 2.25μs when V_{IN} = 330V.
- Minimum OFF time 250ns – required for discharging the leakage inductance.
- Parameters of the transformer: ratio of turns N_P/N_S=28/2, magnetizing inductance $L_{M1,2}$ = 2.16mH. The detailed design procedure of the transformer is attached in appendix 1.
- Input voltage range (rectified voltage): 280 – 330V

The values of the maximum output power and current have been selected for the purpose of compact magnetic components and switching losses that would allow the

integration of the power switches. These values can be scaled up or down depending nature of the application.

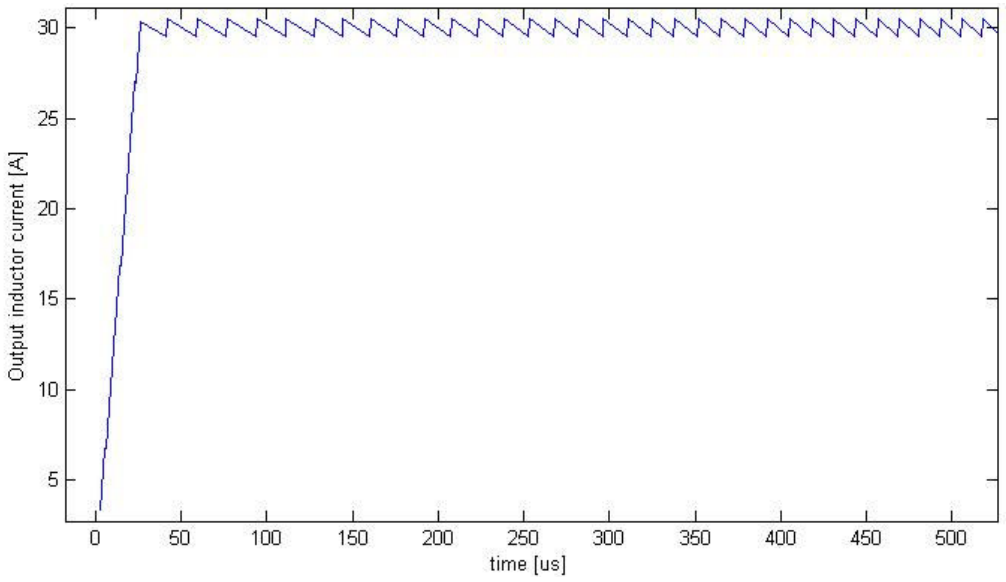
Two types of simulations have been performed; a transient simulation based on the equations characterising the converter; and a frequency oriented analysis based on the analytical derivation of the frequency and duty cycle equations. The Matlab files are attached in appendix 2 and 3, respectively.

TRANSIENT SIMULATION

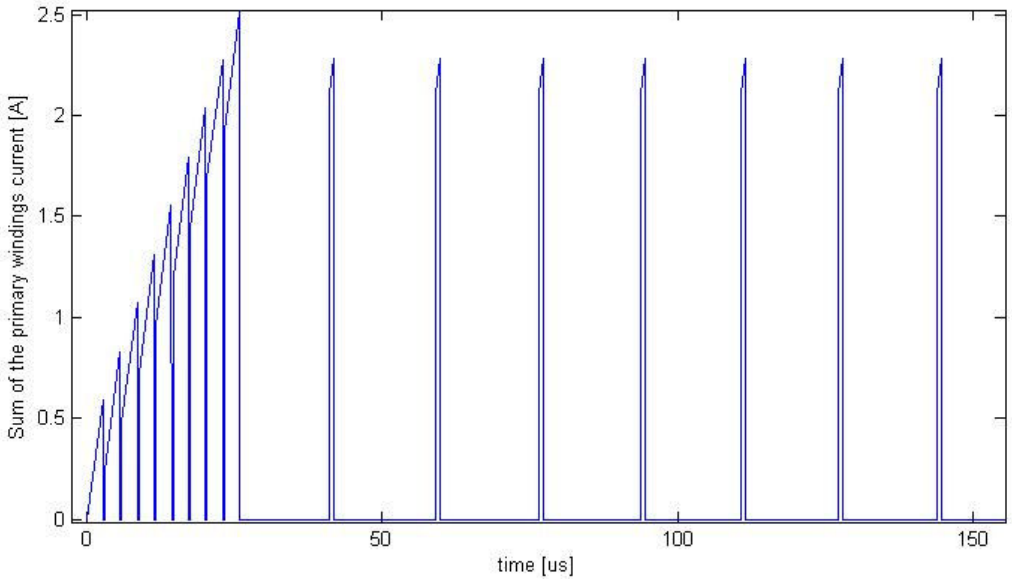
The operation of the control logic is based on a self oscillating topology. According to this, considering the given pattern of the output current I_{Oref} and the maximum current ripple ΔI_O, the switches will operate as follows: turn OFF when the output current reaches the value $I_{Oref} + \Delta I_O/2$ and back ON when the current drops to $I_{Oref} - \Delta I_O/2$.

The following simulations were made considering the worst case input voltage scenario, i.e. when Vin = 280VDC. Also, a small value of the output load capacitor (C_O=30mF) has been used to decrease the number of computations and memory required for a full charging cycle. The absolute values of the observed parameters remain the same as for a large output load.

Circuit start-up (L_O=15µH)



a)



b)

Figure 3. 7. Transient behavioural simulation:
a) output current b) input current (zoomed in to show the start-up behaviour)

The nominal output current is reached in a very short time interval (approx. 40μs) due to the adaptive duty cycle algorithm. Notice the amplitude and the sharp edges of the input current pulses, which will influence significantly the requirements for the power factor correction circuit.

Full charging cycle – output current (L_O=15μH)

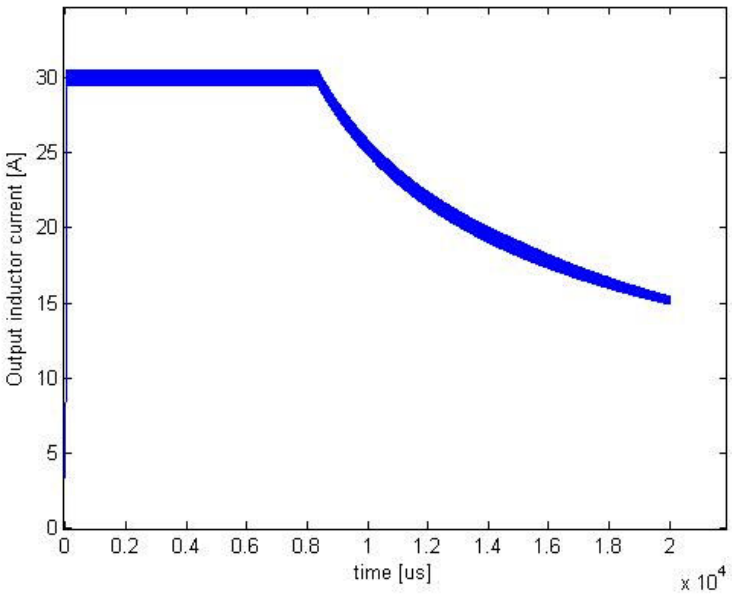


Figure 3. 8 Output current waveform – transient behavioural simulation

SWITCHING ANALYSIS

Under steady state conditions the ripple of I_O for two consecutive ON and OFF cycles has to be constant:

$$\Delta I_O = \left(V_{IN}\frac{N_S}{N_P} - V_O - V_D\right)\frac{\Delta t_{ON}}{L_O} \tag{3.6}$$

$$\Delta I_O = (V_O + V_D)\frac{\Delta t_{OFF}}{L_O} \tag{3.7}$$

where Δt_{ON} and Δt_{OFF} are the ON and OFF times respectively, and all the other symbols have the same meaning as above.

From (3.6) and (3.7) we can deduce the ratio between Δt_{ON} and Δt_{OFF}:

$$r = \frac{\Delta t_{ON}}{\Delta t_{OFF}} = \frac{V_O + V_D}{V_{IN}\frac{N_S}{N_P} - V_O - V_D} \tag{3.8}$$

The duty cycle for a switch is:

$$D = \frac{t_{ON}}{2(t_{ON} + t_{OFF})} = \frac{r}{2(1+r)} \tag{3.9}$$

The frequency of the switches and transformer can be expressed as:

$$f = \frac{1}{2(t_{ON} + t_{OFF})} \tag{3.10}$$

$$f = \frac{1}{2t_{OFF}(1+r)} \quad \text{[Hz]} \tag{3.11}$$

The switching frequency of the converter (actuation of the two switches together) is two times the frequency of the individual switches and the transformer.

Based on (3.6) and (3.7) the frequency can be written as:

$$f = \frac{(V_O + V_D)\left(V_{IN}\frac{N_S}{N_P} - V_O - V_D\right)}{2\Delta I_0 L_0 V_{IN}\frac{N_S}{N_P}}$$

The flux density swing is:

$$\Delta B = \frac{V_{IN}}{N_P A_e} t_{ON} \quad \text{[Tesla]} \tag{3.13}$$

DC current in each of the secondary windings:

$$\bar{I}_{sec} = I_O D + 2\frac{I_O}{2}(0.5 - D) = \frac{I_O}{2} \tag{3.14}$$

As the DC component of the magnetizing current is zero, the DC current for a primary winding is:

$$\bar{I}_{pri} = DI_O \frac{N_S}{N_P} \tag{3.16}$$

Secondary winding RMS current:

$$I_{RMS\_sec} = \frac{I_O}{\sqrt{0.5}} \tag{3.17}$$

Primary winding and switch RMS current:

$$I_{RMS\_pri} = \frac{\bar{I}_{pri}}{\sqrt{D}} \tag{3.18}$$

Primary and secondary winding AC current:

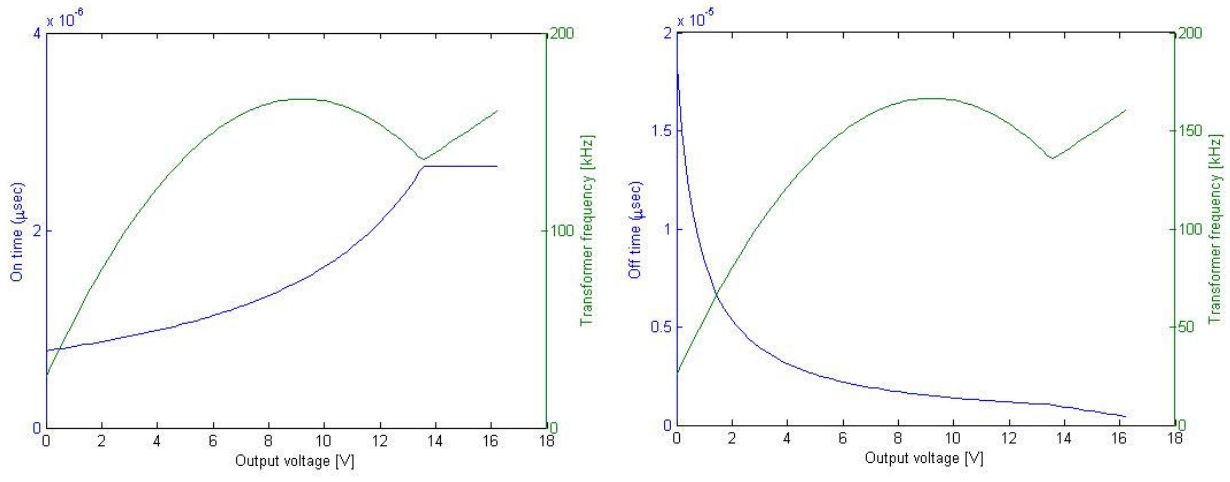
$$I_{AC} = \sqrt{I_{RMS}^2 - \bar{I}^2} \tag{3.19}$$

Skin effect penetration depth:

$$S = \frac{76}{\sqrt{f}} \text{ [mm]} \tag{3.20}$$

The benefit of low power dissipation of the control algorithm can be observed from the frequency waveform (see figure 3.9). The control logic will always operate at the minimum frequency required, depending on the input and output voltage, thus minimizing the switching and AC losses. Figure 3.9 and 3.10 present the operating frequency of the converter and the ON/OFF time for V_{IN}=280V and 330V, respectively. All the parameters presented in the following are regarded as a function of the output voltage, rather than time, as the duration of the charging cycle depends on the dimension of the load. The rise of the frequency at the end of the charging process is due to the limited Vμs product of the transformer.

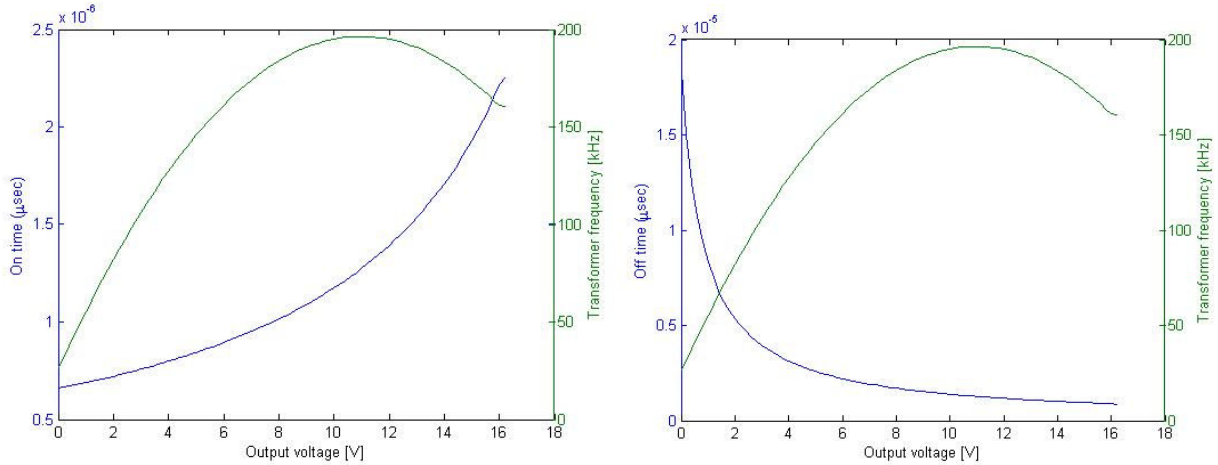
Operating frequency, ON and OFF time (L_O=15μH, V_{IN}=280V)



a) **b)**

Figure 3. 9. Transient behavioural simulation (V_{IN}=280V):
a) on cycle duration (blue), transformer frequency (green);
b) off cycle duration (blue), transformer frequency (green)

Operating frequency, on and off time (L_O=15µH, V_{IN}=330V)

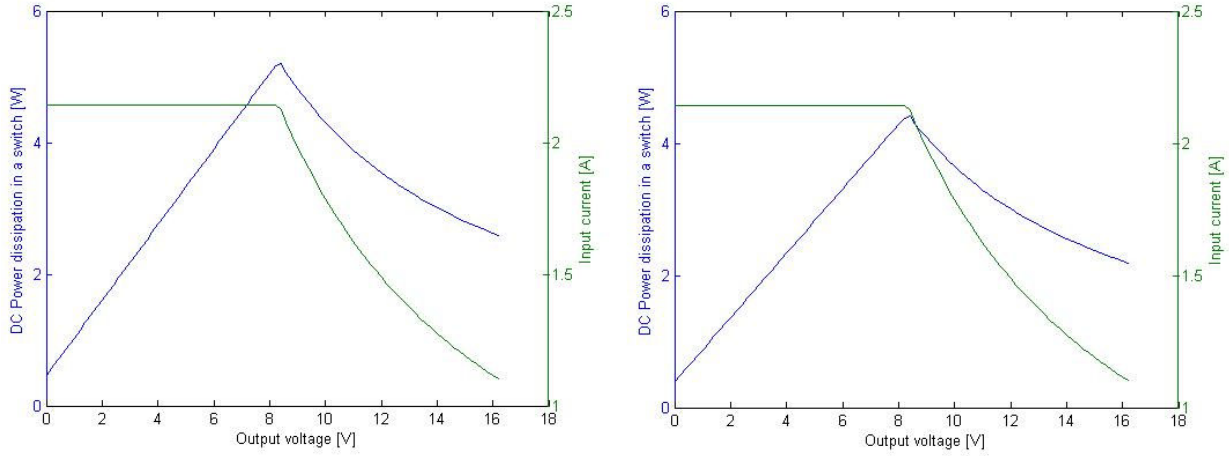


a) **b)**

Figure 3. 10 Transient behavioural simulation (V_{IN}=330V): transformer frequency (green); a) on cycle duration (blue), transformer frequency (green); b) off cycle duration (blue), transformer frequency (green)

As it has been seen before, the main source of power dissipation, and the most important from the point of view of this project, is the DC conduction loss of the power switches. Of course, the current-voltage overlap and the gate charge losses will also play an important role, but they are expected to be less than the conduction losses. Additionally, the parasitic leakage inductance of the transformer will have to be discharged every cycle, increasing the AC power losses. Figure 3.11 a) and b) presents the variation of the time averaged conduction losses per switch for R_{DSON}=5Ω.

DC average power loss in a switch with R_{DSON} = 5Ω



a) **b)**

Figure 3. 11 Conduction losses in a switch device with proposed Ron; a) V_{IN}=280V; b) V_{IN}=330V

The graphs for the rest of the parameters enumerated above, for V_{IN}=280V and V_{IN}=330V, are attached in appendix 4. This second, more accurate modelling of the control system is required to confirm the results of the switching modelling and for the sizing of the switches, the wire used for the transformer winding and the power dissipation for the power devices. The detailed Matlab file is attached in appendix 3.

3.4 Control module architecture

Now that the assumptions for the control algorithm have been validated, the next step is to look at the system implementation. As depicted in figure 3.12 the control circuitry for the self-oscillating converter can be divided in three individual parts: ON time block, OFF time block and switch control logic block. The first one extracts and monitors the value of the output current when the switches are on and signals when the output current has reached the upper limit. The OFF time block estimates the dead time duration and generates a pulse when the output current is expected to reach the lower limit. The switch control logic retains the status of the system (i.e. switch ON/OFF, push/pull transistor ON, normal operation / over-current mode, etc.) and generates the control signals for the switches.

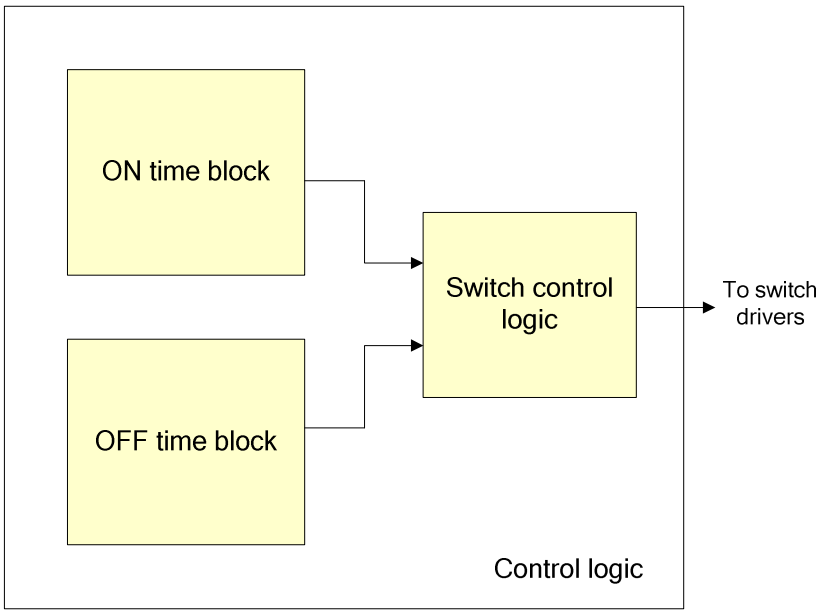


Figure 3. 12. Block diagram of the control logic

3.5 ON time block

The main tasks of the ON time circuit are:

- Generate the profile for the reference output current (see figure 3.3)
- Estimate the magnetizing current
- Extract the value of the output current
- Compare the output current with the reference value and then turn off switches
- Monitor the Vμs product and turn off switches when the maximum is exceeded
- Over-current protection

Figure 3.13 presents the structure of the ON time block. Two main parts can be distinguished: the constant power block, and the output current extraction block. The first one generates the reference value for the output current by dividing the maximum power P_{MAX} by the output voltage and clamps the value to I_{MAX}.

The output current block measures the voltage drop on the current sensing resistor (R_S see figure 3.4) subtracts the magnetization current and multiplies the result with a constant proportional to the winding turns ratio. The resulted voltage (proportional to the inductor current - I_L) is compared with the reference (given by the constant power block $-I_{REF}$) and when exceeded it generates a pulse.

The magnetizing current is also compared with a constant reference in order to limit the Vμs product and avoid very large losses in the transformer core.

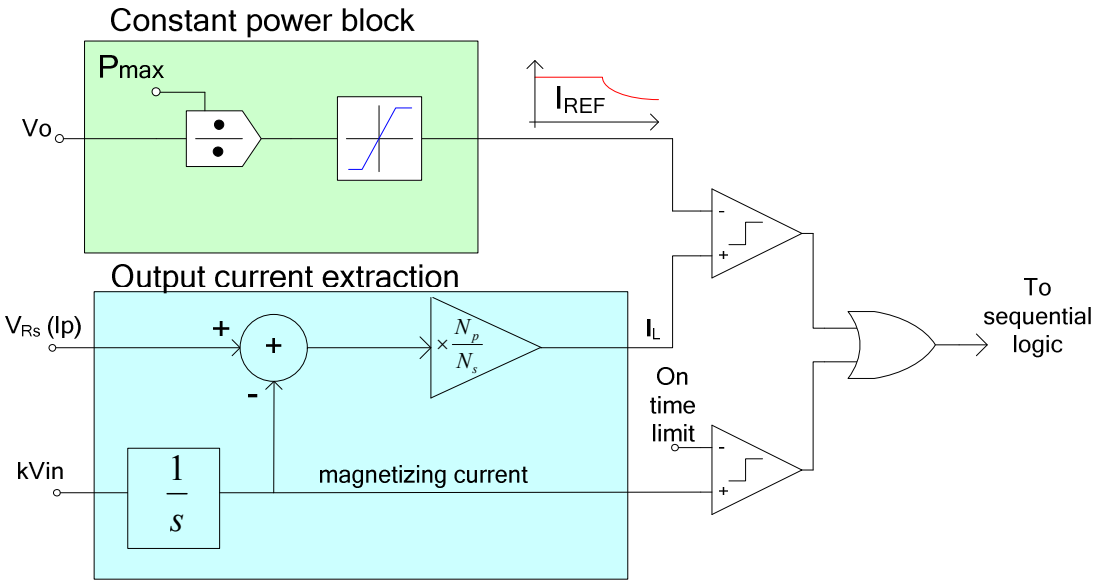


Figure 3. 13 Block diagram of the on time module

3.6 OFF time block

As mentioned before, the main drawback of the push-pull topology is that the output current cannot be evaluated when the switches are off. This disadvantage can be compensated for by using an estimation algorithm. The benefit of having an EDLC as load is that its impedance varies slowly, thus the ON and OFF cycles duration will have a slow variation as well. We have designed two algorithms for the estimation of the dead time: input current sampling and ON time integration. The aim of both algorithms is to estimate the value of the output current at the end of the off phase, subtract it from a prescribed value and minimize the difference (error).

3.6.1 Input current sampling algorithm

The principle used for the estimation of the OFF time is explained using the waveforms and the block diagram depicted in figure 3.14 a) and b), respectively. At the beginning of each on cycle the value of the primary winding current is sampled (time t_2 and t_5). This value is then scaled by the ratio of the transformer windings. The difference between the sampled value and the output current reference (I_O-$\Delta I_O/2$) forms the error signal. This value is added to the voltage corresponding to the previous time base (ΔT). This way, if the error is positive (i.e. if the current at the beginning of the ON cycle is larger than the reference) the new time base voltage will increase and the next OFF time will be longer ($\Delta T+T_X$ from t_3 to t_5). If the error is negative (i.e. if the current at the beginning of the ON cycle is smaller than the reference) the time base will decrease and the OFF time will be shorter.

Thanks to this, the OFF time spreads over a large interval allowing the implementation of the variable frequency topology. The maximum value of the error scaling constant, P is limited to ensure the stability of the system and to avoid large short term variations of the OFF time that would induce flux imbalance in the core.

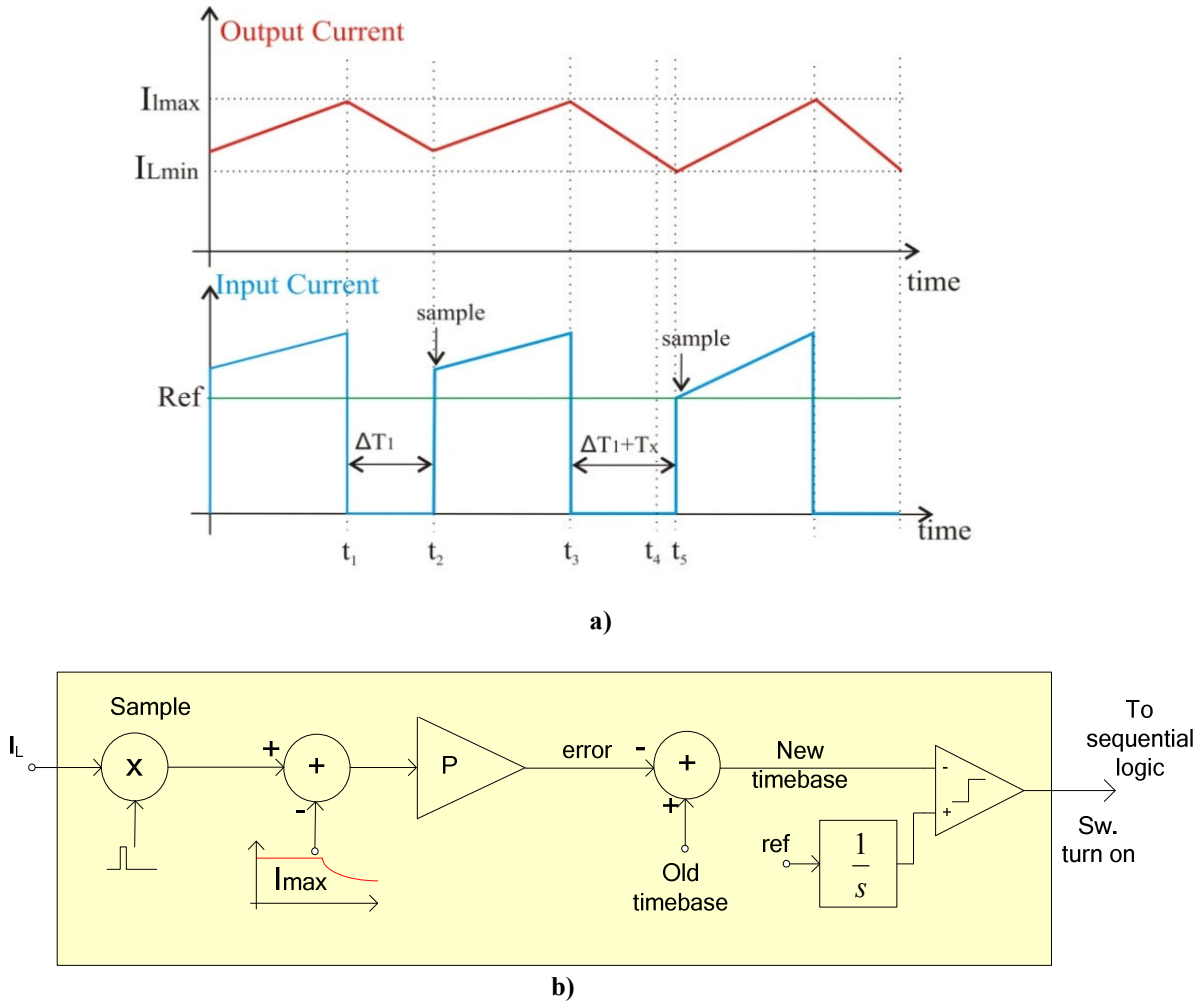
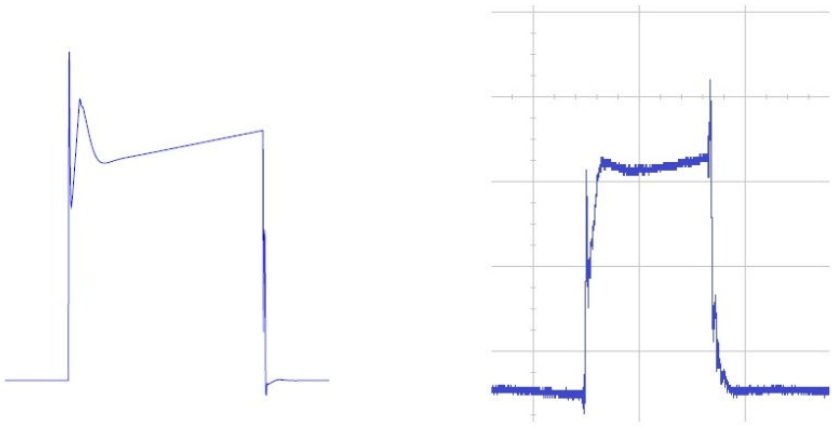


Figure 3. 14. Diagram of the OFF time block: a) waveforms; b) block diagram

DOUBLE SAMPLING CIRCUIT

The principle presented above suffers from the effects of the parasitics of the transformer and main switches. When one of the switches turns on, the measured current at that instant is altered by: the current in the leakage inductance of the inactive primary winding, the snubber current of the active primary winding and gate charge displacement through C_{GS} of the MOSFET. Figure 3.15 presents the simulated and measured (for the breadboard presented in chapter 4) waveforms of the tail current.



a) b)

Figure 3. 15 Sense resistor current waveform; a) simulation result b) breadboard circuit measurement

To compensate for these sources of error we have designed a double sampling circuit that returns an accurate value of the current at the moment when the switches are turned on. The algorithm relies on the constant slope of the input current during the ON phase. The input current is sampled twice at precise moments of time ΔT_1 and $2\Delta T_1$ and the initial value is obtained by extrapolation, respectively, see figure 3.15.

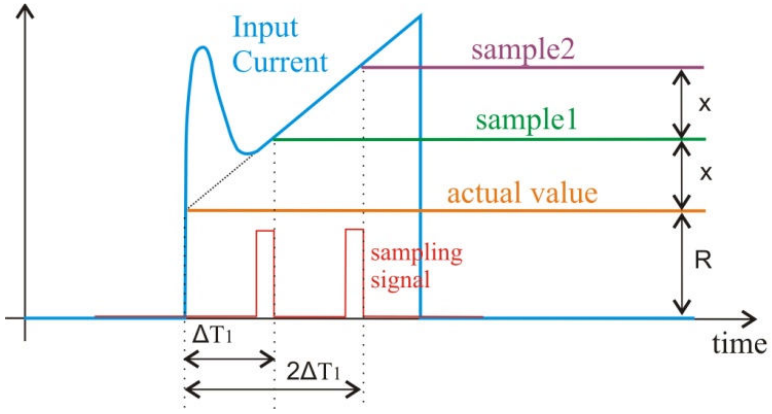


Figure 3. 16 Double sampling circuit waveforms

The value of the input current at the beginning of the on cycle is:

$$I_{initial} = sample1 - (sample2 - sample1)$$

$$I_{initial} = 2\,sample1 - sample2 \qquad (3.21)$$

The exact value of ΔT_1 is not critical, as it just has to be longer than the duration of the overshoot and short enough to allow the double sampling to occur during the minimum duration of the ON phase. The important aspect is that the second sampling event takes place at exactly $2\Delta T_1$. The circuit implementation of the double sampling algorithm is attached in appendix 8.

3.6.2 ON time integration algorithm

This implementation eliminates the need to sample the input current and relies instead on the expression for the ON time. This algorithm is also based on the assumption of a slow change in the load voltage due to the large capacitive load (>20mF). In the following we will provide a quantitative explanation of the algorithm, while the practical implementation is presented in the next chapter. The principle of the algorithm is explained based on the waveform and block diagram from figure 3.17 and 3.18, respectively. As we have seen in the Matlab modelling of the system, the duration of the ON time is a function of V_{IN} and V_O during the charging process. Therefore in the following we will assume that the ON time value is known, with a value that will be called '*ON time reference*'.

The duration of each ON cycle is measured and subtracted from the *ON time reference* resulting in an error, *err*. If the value of the error is positive then the ON cycle was too short and the level of the output current at the beginning of the cycle, I_{MIN1}, was too high. Therefore the duration of the previous OFF cycle was not long enough and must be increased. The error is then scaled by a proportionality constant, K and added to the duration of the previous OFF time. In this way at the beginning of the next ON phase, the output current will have a lower value and the error between the *ON time reference* and the actual ON time will decrease until the two values coincide. The algorithm also has the benefit that a higher limit can be imposed for the ON time duration, for the operation region where this is limited by the maximum flux density (or the V×μs product). The derivation of this limit and the practical implementation are presented in the next chapter.

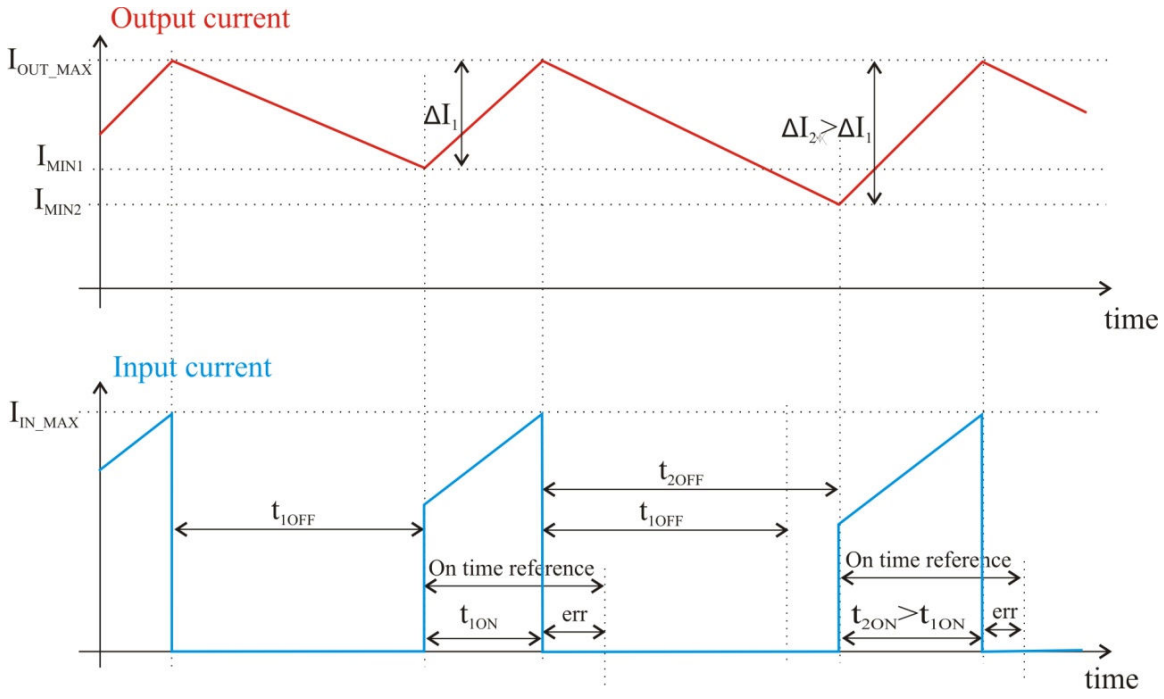


Figure 3. 17 ON time integration algorithm waveforms

The value of the *ON time reference* is obtained from the ON cycle equation (3.7):

$$\Delta I_O L_O = \int_0^{Ton} V_{in} \frac{N_S}{N_P} - (V_o + V_D) dt \qquad (3.22)$$

where ΔI_O is the ripple of the output current, L_O is the value of the output inductor and the other terms have the same significance as above.

Thus the error value becomes:

$$err = \Delta I_O L_O - \int_0^{Ton} V_{in} \frac{N_S}{N_P} - (V_o + V_D) dt \qquad (3.23)$$

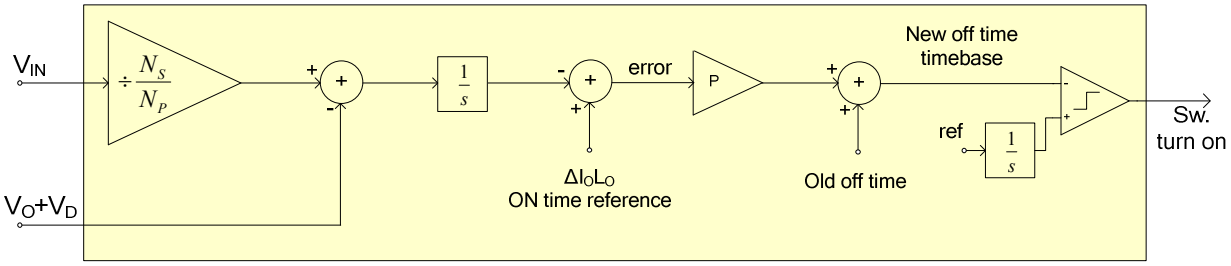


Figure 3. 18 Diagram of the OFF time block for the ON time integration algorithm

Chapter 4

IMPLEMENTATION OF THE CHARGER WITH DISCRETE COMPONENTS

4.1 Control module - ON time block

As stated at the beginning, the first implementation of the proposed charger architecture is with discrete components, in order to validate the control algorithm and check the practical self heating of the devices (mainly the magnetic components and the power switches). In the following sections we are going to give a brief presentation for each of the blocks presented above.

CONSTANT POWER BLOCK – CURRENT REFERENCE

The current reference is generated by dividing the specified maximum power of the device with the instantaneous output voltage and clamping the result to a value that will correspond to the maximum output current ($I_{OUT(MAX)}$ = 30A). Figure 4.1 depicts the simplified diagram of the circuit, while the full schematic is attached in appendix 5. Figure 4.2 presents the waveform of I_{REF} versus the output voltage.

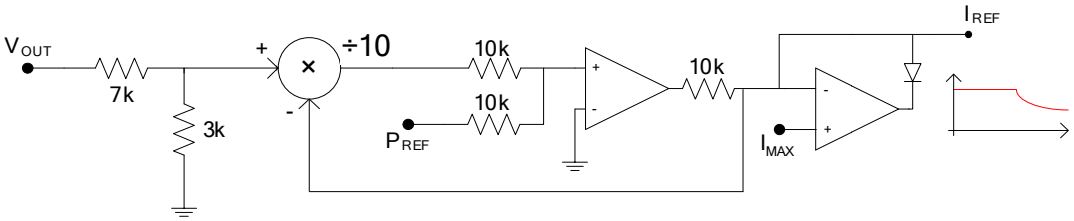


Figure 4. 1. Current reference block

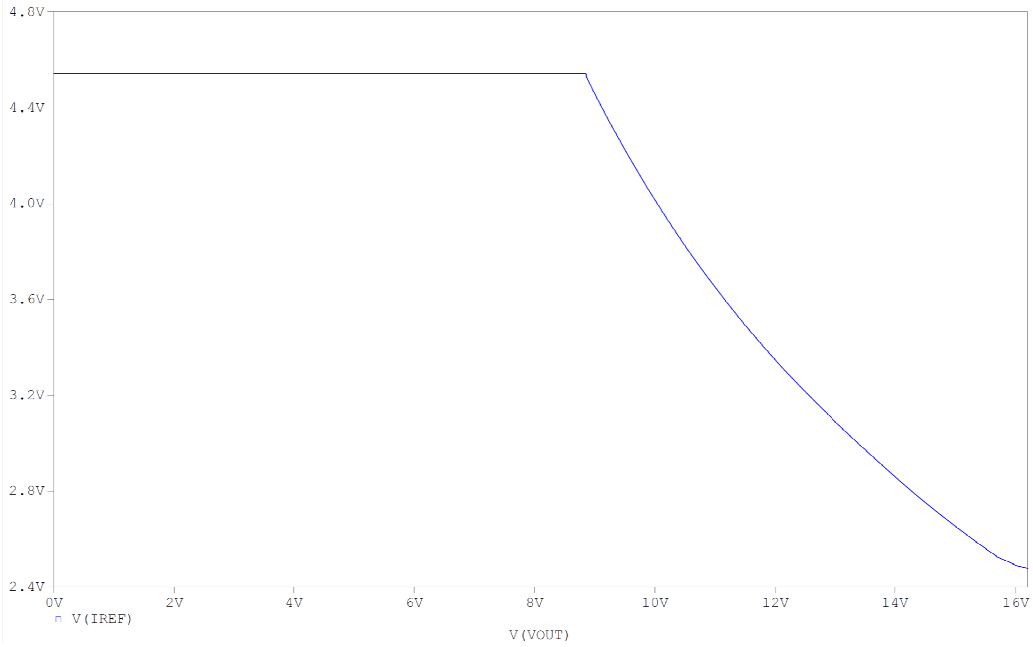


Figure 4. 2 Current reference vs. output voltage

OUTPUT CURRENT BLOCK

According to equation (3.5), during the ON phase, the output current can be derived from the value of the primary winding current by subtracting the magnetizing current of the primary and multiplying the result by N_P/N_s. The diagram of the circuit that estimates the value of the output current is depicted in figure 4.3.

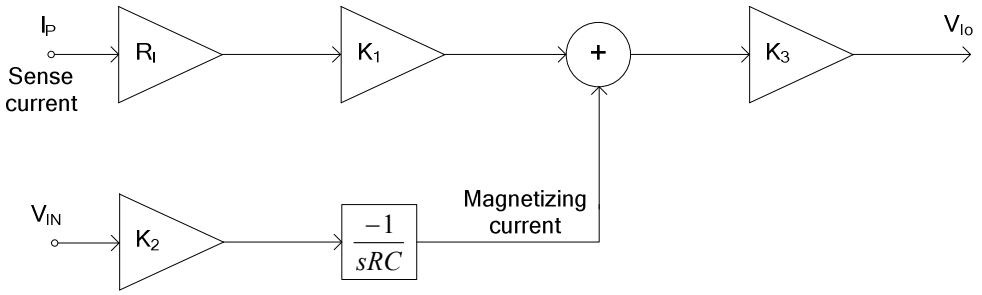


Figure 4. 3 Functional diagram of the output current block

The equation of the output signal (corresponding to the estimated output current), V_{Io}, is:

$$V_{Io}(t) = \left(i_P(t) R_I K_1 - \frac{K_2}{2RC} V_{IN} t \right) K_3 \tag{4.1}$$

While the actual output current can also be written as:

$$I_0(t_{ON}) = \left(i_P(t_{ON}) - \frac{V_{IN}}{2L_{P1,2}} t_{ON} \right) \frac{N_P}{N_S} \tag{4.2}$$

Comparing the two equations above, we can make the following identification of the coefficients:

$$R_I K_1 = \frac{2K_2 L_{P1,2}}{RC} \tag{4.3}$$

For $R_I K_1 = 1/4$, $L_{P1,2}$=2.16mH, C=1nF and R=51KΩ we obtained K_1=4.9 and K_2=5.9e-3, K_3=1.4.

Overall the ratio between V_{Io} and I_O is:

$$\frac{V_{Io}}{I_O} = \frac{1}{40} \tag{4.4}$$

The practical implementation of the output current block is included in appendix 6.

4.2 Control module – OFF time block

OFF TIME BLOCK - INPUT CURRENT SAMPLING ALGORITHM

The OFF time block is the most complex part of the circuit, estimating the moment when the output current has reached the value I_{O_Ref} - $\Delta I_O/2$. As mentioned before, this approach is only possible for loads that have a slow variation of their impedance when charged with constant current, as the EDLC. Figure 4.4 shows the diagram of the block. The circuit works as follows (also see chapter 3.6.1):

- The voltage that corresponds to the minimum output current (I_{Ref} - $\Delta I_o/2$) is subtracted from the signal representing the output current (V_{Io}), resulting in an error signal.
- The error signal is multiplied with the proportionality constant and added to the previous value of the time-base.
- The new value of the time-base is sampled on capacitor $C_{sample1}$ at the beginning of the ON phase, thus generating the new time-base to be integrated during the next OFF time.
- At the beginning of the OFF phase (after the output of the buffer *Buff1* has settled) the new time-base is sampled over capacitor $C_{sample2}$. This value will be added to the error signal generated at the beginning of the next ON time, and the process repeats.

The new time-base control value is converted into a time interval with the aid of the resettable integrator and a comparator. Thus when voltage ramp generated by the integrator exceeds the value of the new time-base, the comparator generates a pulse that turns on the switches.

As the time-base magnitude can reach very low values, an additional comparator establishes the minimum OFF time. This time has to be long enough to allow the circuit to settle and the new time-base to be sampled over $C_{sample2}$. The detailed schematic of the OFF time estimation block is given in appendix 7.

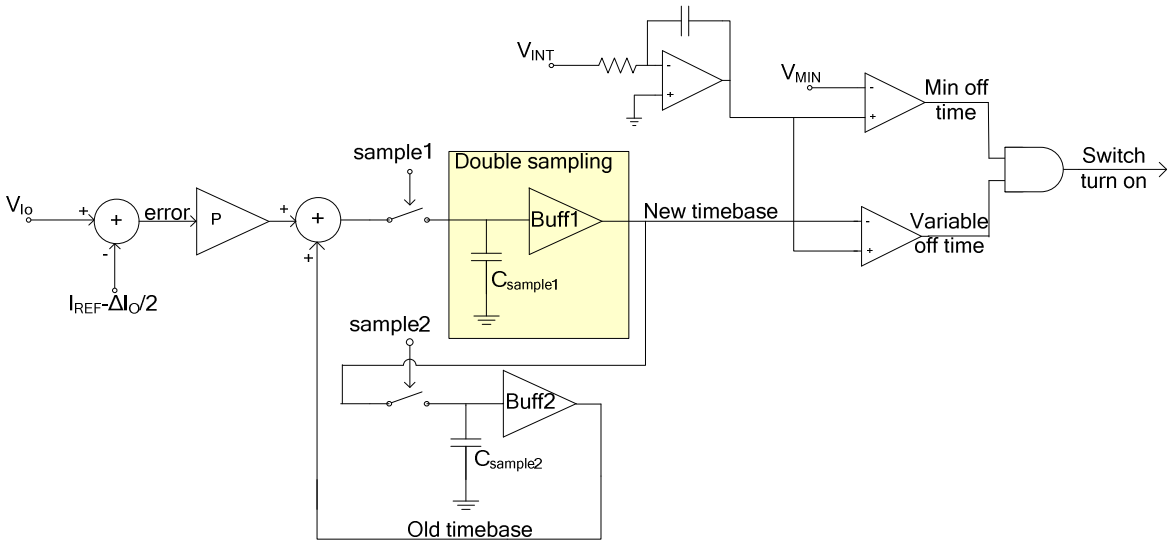


Figure 4. 4 Off time block - input current sampling algorithm

The choice of the sampling switches is one of the main limiting factors of the circuit. The switches must present the following properties in operation: low charge injection, low clock feed-through, low switching delays, low ON resistance, low leakage current and high operating voltage. For the discrete components implementation, the low charge injection and clock feed-through switches have a have a voltage range typically limited between 0V and 5V. As it can be observed from appendix 4, the OFF time varies between 18µs down to 460ns. In practice the maximum OFF time has to be even larger so that the converter can recover from over-current situations swiftly.

Thus if 5V corresponds to 18µs off time, for 460ns the time-base control variable should be 127mV. The error generated by the charge injection, offset of the buffers, integrator errors could alter the OFF time value significantly. This can result in oscillations of the output current, flux imbalance in the transformer and additional losses.

The solution in this case is a variable slope of the integrator output voltage. In this way, the integration of the same time-base value can result in two different time intervals depending on the integrated voltage, see figure 4.5.

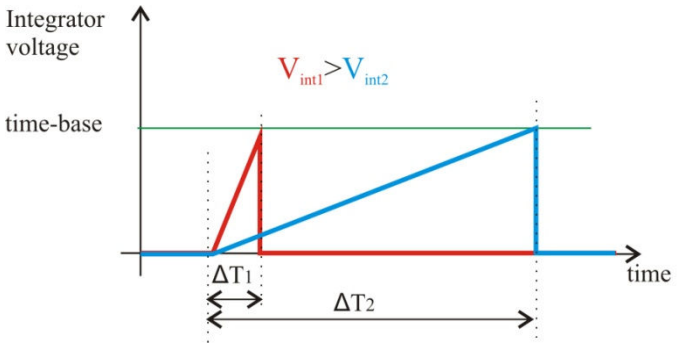


Figure 4. 5 Waveforms for the variable slope integrator

In order to have a minimum time-base control value of 2.5V and reduce the circuit level errors, the slope of the integrator would have to be 20 times higher when V_O=16.2V than when V_O=0V. Therefore the input voltage of the integrator (V_{INT}, see figure 3.17) would have to represent the corresponding dependence on the output voltage. This can be seen as a linear predistortion (as function of V_O) introduced in the integrator input signal to compensate for the wide variation of the OFF time duration versus V_O (see figures 3.9 and 3.10).

For the values of the components presented in the appendix 7 the equation of V_{INT} is:

$$V_{INT} = \frac{-9.5}{16.2} V_O - 0.5 \qquad (4.6)$$

OFF TIME BLOCK - ON TIME INTEGRATION ALGORITHM

The second implementation of the OFF time estimation block eliminates the need of sampling the input voltage of the converter and brings an improved stability to the control loop at the cost of less accurate control of the output current ripple. The difference between the two algorithms is in the way the error signal is computed (see figure 3.14). Therefore in the following we will focus only on that part of the circuit which is different, and assume the rest is the same as for the 'input current sampling' algorithm.

As presented before, the value of the error that will update the value of the previous OFF cycle duration is:

$$err = K\left[\Delta I_O L_O - \Delta t_{ON}\left(V_{IN}\frac{N_S}{N_P} - (V_O + V_D)\right)\right] \qquad (4.7)$$

The transfer function for the circuit presented in figure 4.6 is:

$$err = K_1 V_{ref2} - \frac{2\Delta t_{ON}}{RC}\left(V_{IN} K_0 \frac{R_3+R_4}{R_4} - V'_O \frac{R_3}{R_4}\right) \qquad (4.8)$$

Where: $K_1 = \frac{2R_8}{(R_7+R_8)}$, $K_0 = \frac{R_2}{R_1+R_2}$, $V'_O = V_O + V_D$ and $R_9 = R_{10}$

Equation (4.8) can be rewritten as:

$$err = K\left\{\frac{K_1}{K} V_{ref2} - \Delta t_{ON}\left[V_{IN} K_0\left(1 + \frac{R_4}{R_3}\right) - V'_O\right]\right\} \qquad (4.9)$$

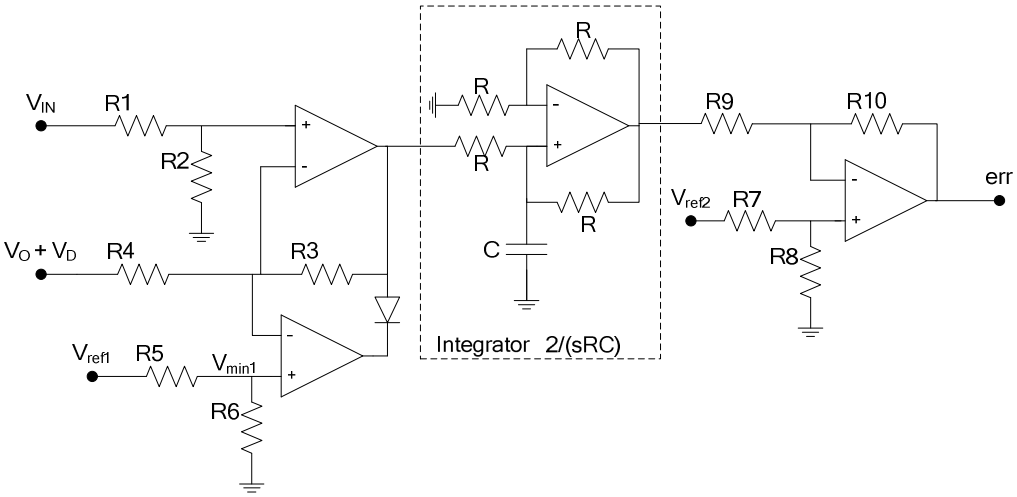


Figure 4. 6 Simplified schematic of the OFF time block – ON time integration algorithm

If we identify the scale parameters from (4.7) and (4.9) we obtain the following:

$$K_0\left(1+\frac{R_4}{R_3}\right)=\frac{N_S}{N_P} \tag{4.10}$$

$$K=\frac{2}{RC}\frac{R_3}{R_4} \tag{4.11}$$

$$K_1V_{ref2}=K\Delta I_O L_O \tag{4.12}$$

The values of the components are found by following these steps:

1. Set the range of the output (err signal). This value coincides with K_1V_{ref2}

$$K_1V_{ref2}=4V \tag{4.13}$$

If we set the value of V_{ref2}=5V then K_1=0.8

2. Determine value of K, R_3 and R_4

Based on (4.12) $K=\frac{K_1V_{ref2}}{\Delta I_O L_O}={}^{8}/_{3}\times 10^5$ (for ΔI_O=1A and L_O=15µA).

If we impose the integration components R=22kΩ and C=100pF and using equation (4.11) we obtain the ratio ${}^{R_3}/_{R_4}=K\frac{RC}{2}\cong {}^{1}/_{3.41}$, thus we chose R_3 = 2kΩ and R_4=6.8kΩ.

3. Determine R_1 and R_2

From (4.10) and definition of K_0, we obtain: $\frac{R_2}{R_1+R_2}=\frac{R_3}{R_3+R_4}\frac{N_S}{N_P}=\frac{1}{61.6}$.

We choose R_2=1kΩ and R_2=60.6kΩ

MAXIMUM FLUX DENSITY LIMIT

As we have seen before, the flux density swing is limited by the value of the losses in the core, in our case ΔB_{MAX}=200mT. In our case, this limit is introduced by controlling the duration of the ON cycle. The equation of ΔB is:

$$B = \frac{1}{N_P A_e} \int_0^{t_{ON}} V_{IN} dt \qquad (4.14)$$

Where N_P is the number of turns of the primary winding and A_e is the area of the core.

For constant values of V_{IN}, equation (4.14) can be rewritten as:

$$t_{ON} = \Delta B \frac{N_P A_e}{V_{IN}} \qquad (4.15)$$

Therefore the maximum value of t_{ON} is:

$$t_{ON\_max} \cong \frac{700 \mu Vs}{V_{IN}} \qquad (4.16)$$

As the value of t_{ON} is limited to a maximum value, we have to introduce a minimum value for the term $V_{IN} \frac{N_S}{N_P} - (V_O + V_D)$ in equation (4.7), otherwise the error would be always positive above the t_{ON_max} point. In order to allow the error to be bipolar, we have to impose the following condition:

$$\Delta t_{ON\_max} \left(V_{IN} \frac{N_S}{N_P} - (V_O + V_D) \right) \geq \Delta I_O L_O \qquad (4.17)$$

If we use the notation for the value $V_{IN} \frac{N_S}{N_P} - (V_O + V_D) = V_{IN\_min}$, then equation (4.17) becomes:

$$V_{IN\_min} = \frac{\Delta I_O L_O}{\Delta t_{ON\_max}} \qquad (4.18)$$

The value of V_{IN_min} corresponds to the signal at the input of the integrator in figure 4.6. Hence this equates to:

$$\frac{R_3}{R_4} \left(V_{IN} K_0 \left(1 + \frac{R_4}{R_3} \right) - V'_O \right) \geq V_{IN\_min} \qquad (4.19)$$

or

$$V_{min1} = V_{IN\_min} \frac{R_3}{R_4} = \frac{R_3}{R_4} \frac{\Delta I_O L_O}{700 \mu Vs} V_{IN} \qquad (4.20)$$

The resulting values for the components are: R_5=158kΩ, R_6=1kΩ and $V_{ref1}=V_{IN\_min}$.

4.3 Leakage inductance and snubber circuit

Under ideal circumstances it is assumed that the entire magnetic flux from a primary winding of the transformer is coupled to the secondary windings. In practice, a small fraction of the flux does not link to the secondary windings, by "leaking" into the air. The leaking flux leads to a *leakage inductance* distributed throughout the windings of the transformer. For simplicity, the leakage inductance can be represented as a lumped inductor for each winding, connected in series, as depicted in figure 4.7. The size of the leakage inductance is proportional to the number of turns of the winding, and hence for a step-down transformer, the leakage inductances in the secondary will be much smaller than in the primary.

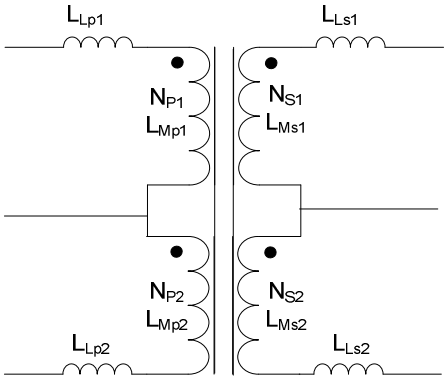


Figure 4. 7 Equivalent transformer circuit

The magnitude of the leakage inductance for each winding is not easy to calculate as it depends on the thickness of the insulation between the windings and the winding geometry. The actual leakage inductance can be determined by direct measurements. This is achieved by measuring the winding inductance with the remaining windings short-circuited. The leakage inductance for a good transformer should be no more than 4% of its magnetizing inductance [23]. The value of the L_L can be reduced by using a long centre leg core and less winding layers or by interweaving the primary and the secondary windings [36].

Two main consequences derive from the presence of this non-ideal behaviour. The slew rate of the rising and the falling edge of winding current will be limited to the value: $dI/dt = V_w/L_L$, where V_w is the voltage drop across the winding and L_L is the leakage inductance. The second effect is on the high voltage side and is specific to the push-pull topology. When one of the switches turns off, the leakage inductance will generate a voltage spike at the drain terminal of amplitude: $V_s = V_{supply} + L_L\, dI/dt$. In addition to the voltage spike, ringing is also created by excitation of the LC network composed of the leakage inductance and the MOSFET parasitic capacitances. It is normally important to minimise such

ringing with some additional damping. The waveform depicted in figure 4.8 corresponds to a converter with a snubber network, and hence no ringing is indicated.

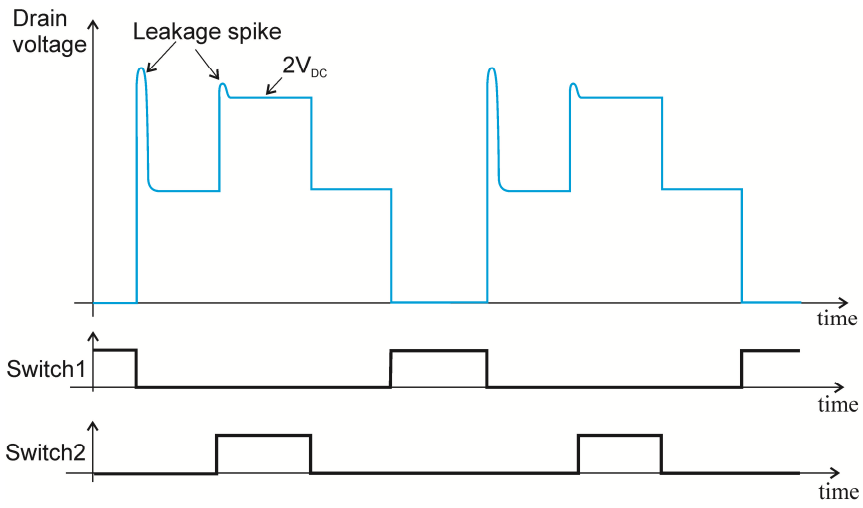


Figure 4. 8 Drain voltage spike due to the leakage inductance

As mentioned before, the main drawback of the push-pull converter is that when off, the switches have to be able to withstand double the input voltage. As it can be seen from figure 4.8, the amplitude of the leakage spike can require an even larger $V_{DS\text{-}OFF}$ value. Thus additional snubber and clamping circuits must be added in order to reduce the voltage stress on the MOSFETs.

The trade-off for the attenuation of the spikes comes from the following considerations. In the first instance, one can be tempted to reduce the value of dI/dt, but that would result in a very large current-voltage overlap loss. On the other hand, the amplitude of the spikes can be reduced by using a large snubber capacitor, but this case would increase the loss in the snubber circuit. The third option is to use a clamping circuit, but this would extend the duration of the spike and reduce the slope of the falling current through the leakage inductance.

SNUBBER NETWORK

The basic purpose of the snubber circuit for the push pull converter is to absorb the energy from the leakage inductance and damp any oscillation at the drain of the MOSFET, when that node of the circuit presents high impedance. The voltage snubber is composed of an energy storage capacitor connected in parallel with the switch, a resistor and/or a diode, depending on the nature of the circuit.

In the case of converters with alternating switches, such as the push-pull converter, a snubber which controls the voltage at turn off will create a current pulse in the switch at turn on [37]. This is due to the change of the potential of the transformer terminal that is left in a high impedance state, and the current required to charge the parasitic capacitances. For this design, the simple RC snubber proved to be the most suitable choice, resulting in a good balance between losses, damping and recovery time. The simple RC snubber is presented in figure 4.9.

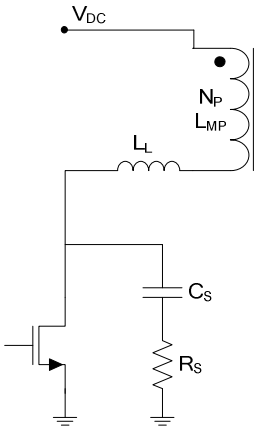


Figure 4. 9 Simplified primary side circuit with snubber network

The ringing will be critically damped if the value of the resistor is equal with the characteristic impedance of the resonant circuit, $R_S = \sqrt{L_L/C_{tot}}$ [37],[38]. The size of the capacitor has to be larger than the equivalent circuit capacitance to reduce the overshoot and ringing. The parasitic circuit capacitance is mainly determined by the output capacitance of the MOSFET. The size of C_S is usually selected in the range of two to four times this value [23],[37]. Care must be taken not to increase C_S too much as it will lead to significant losses.

4.4 Simulation results and measurements for the breadboard circuit

This section focuses on various transient simulations and measurements of the charger as a whole. The purpose of these is to validate the operation of the control algorithm and power block. Also, the measurements will help to highlight any non ideal behaviour of the components (i.e. tracks HF impedance, switching delays, etc.) and their influence on the overall behaviour of the device.

First we will look at the device start-up under different conditions and afterwards at the long transient simulations for a full charge cycle. Due to the very long duration of the charging process compared with the switching period, plots of the full charge process with large specified load capacitors are not very informative. Hence the measurements will only

focus on the regulation of the OFF time block at start-up. Considering the complexity of the system, a transient simulation for a real charge cycle would require a very long time and it would result in a large data file. As a consequence, we have simulated full charging process with a reduced 10mF load. This represents a more difficult scenario for the control system, as the variation of the load voltage is much faster, with the charging time being approximately 5.6ms. Based on this value, we can estimate the charging time for an array of six 350F ultracapacitors to be approximately 35.5 seconds, while energy transferred to the capacitor array is 2.13Wh (for the non-scaled load).

System start-up

Three main intervals can be observed during the converter start-up, see figure 4.10:

- The output current is less than 30A (10µs to 400µs). During this interval, the OFF time-base decreases until I_{OUT} reaches the maximum value. The switch ON time will be limited by the maximum Vµs product to avoid the saturation of the transformer.
- The output current exceeds 30A, but the time-base has a low value (400µs to 480µs). During this time interval the OFF time estimation loop will regulate the duration of the OFF time, until steady state conditions are met.
- Normal operation region (480µs onwards). After 480µs the output current reaches the nominal value and the OFF cycle time-base value settles. The ON time is set by the value of $I_O+\Delta I_O/2$ and the OFF time is set by the estimation loop.

The simulation for the circuit start-up has been repeated for the maximum input voltage, V_{IN}=330V. In this simulation we have introduced an additional stress test for the control loop. The test consists of shorting the voltage corresponding to the OFF cycle to ground (at 1.05ms, see figure 4.11). This shows the stability of the loop and the capability to deal with external interferences. Figure 4.12 presents the measured waveforms for the input current and OFF time-base voltage of the breadboard circuit for V_{IN}=330V, demonstrating the operation of the OFF time estimation algorithm in practice.

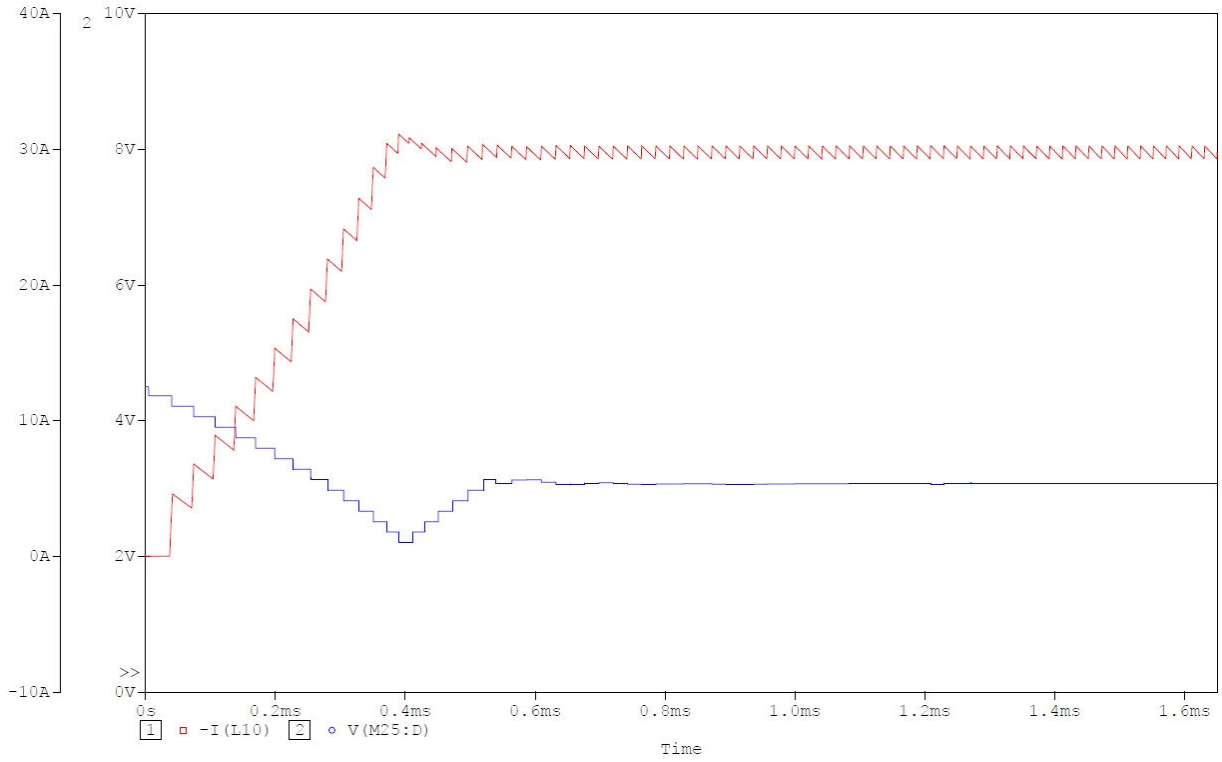


Figure 4. 10. Charger start-up for V_{IN}=280V;

red – output inductor current; blue - *OFF* time-base waveform

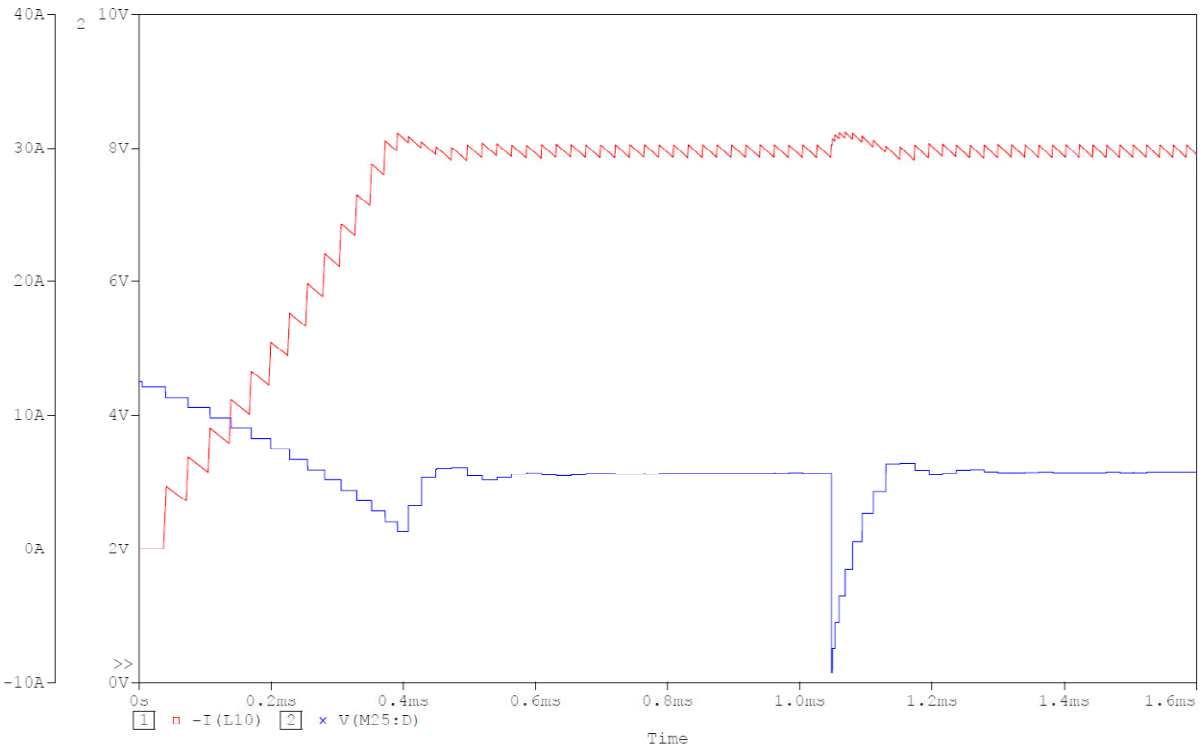


Figure 4. 11. Charger start-up for V_{IN}=330V;

red – output inductor current; blue – *OFF* time-base waveform

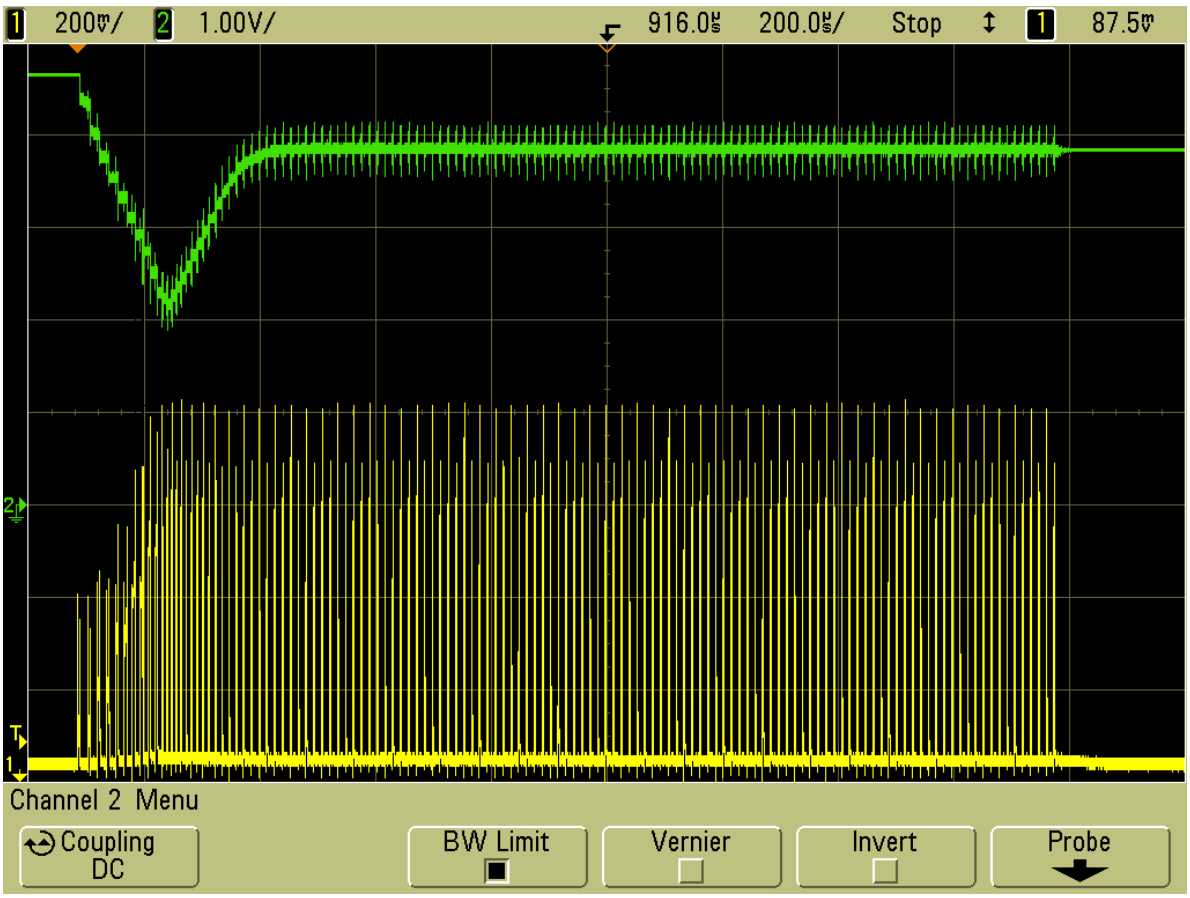


Figure 4. 12. Measured waveform of the primary current (yellow) and the voltage corresponding to the *OFF* time (green)

Capacitor full charge for variable/fluctuating input voltage

The long transient simulations must include a variable input voltage as an equivalent for the ripple of the voltage after the power factor correction block and voltage fluctuations in the mains network. Therefore we have considered a 500Hz sinusoidal waveform with a DC component of V_{DC} = 305V and AC equal to V_{AC} = 25V, in order to cover the full input range of the converter. A 500Hz AC input signal has been used in order to verify the immunity of the regulation algorithm to higher order harmonics. The simulation result shows a very good rejection of the supply fluctuations thanks to the fast feed forward loop that compensates the changes of the supply voltage.

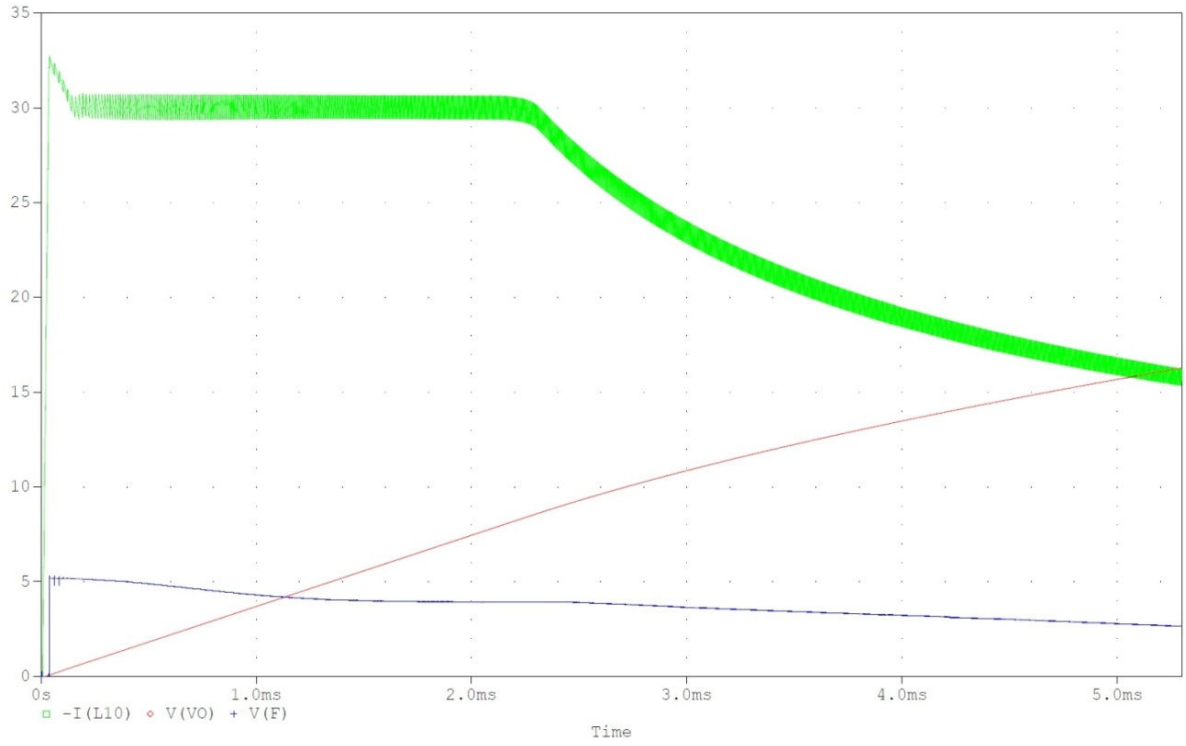


Figure 4. 13 Full charging cycle of the ultracapacitor waveforms:
green – output current; red – output voltage; blue – time-base voltage

The circuits presented in this chapter together with the simulations and the measurements represent an important milestone towards the design of an integrated circuit implementation. As a first stage, this chapter demonstrates the validity of current-mode charger architecture and the operation of the novel control algorithm. The breadboard implementation of the circuit allowed us to test the circuit step-by-step, increasing gradually the duration of the start-up cycle, thus reducing the hazards that can result from working with high voltage. Another major aspect that has been verified by the circuit measurements is the power dissipation in the transformer and switches. Special care must be taken with the self heating of the transformer as it can lead to a short circuit in the primary windings. The accuracy of the current ripple and the *OFF* time estimation loop can be further improved in the IC version. An improved accuracy can lead to even higher operating frequencies and thus smaller dimensions of the transformer core.

Chapter 5
INTEGRATED CIRCUIT DESIGN – ANALOGUE APPROACH

5.1 System architecture

One of the main aims of this project is to reduce the size the converter to a minimum so that it can be embedded with the EDLC pack. Also, it has to represent a feasible solution from a manufacturing point of view and therefore we have decided to realise it as monolithic circuit in a high voltage process, in the first instance. The control module is implemented in analogue mode for the following reasons: We are aiming for a one chip solution and the size of MOSFETs and the parasitic capacitances in the target HV process are very large (even for the low voltage devices), hence a mixed-signal approach would not be feasible from the area and speed point of view. Also, the minimum duration of the ON cycle goes down to values of 400ns, and therefore the period of the clock would have to be below 10ns in order to achieve a decent accuracy. As the propagation delay for flip-flops in a coarse HV CMOS technology (>1µm geometry) is of the order of nanoseconds, the implementation of the complete control loop would not be viable. Also, it would be difficult to build a robust oscillator with a frequency of 100MHz in such a process. The medium and high voltage technologies offer good fully isolated NPN transistors, allowing some of the signal manipulation for the algorithms to be performed in translinear multiplier/divider blocks, greatly simplifying the overall circuit complexity.

One of the main problems of switched-mode power supplies is the noise generated by the main switches and the drivers. This could easily alter the internal signals by raising the ground potential or by capacitive coupling. The current-mode design approach is being used in order to alleviate these effects and simplify the summation circuits. The drawback in this case comes from the fact that additional circuitry is required to convert the input values (voltages) into currents. Nevertheless, the circuit will include a small amount of digital circuitry to hold the system state, but this will operate at a much lower frequency and it will be asynchronous.

For the first iteration of the charger design we are going to use the "ON time integration" algorithm. Based on the algorithms and diagrams presented in Chapter 3, together with the breadboard circuit in Chapter 4, we have developed the abstract block diagram of the analogue control circuitry (see Figure 5.1). The equations in the diagram represent the signals from the power block, and based on these, we are going to set the scaling factors for each signal and determine their magnitude in the integrated circuit.

The main difference between the above diagram and the ones presented in Chapter 3 is the integrator in the feedback loop. In this case we have used a single integrator both for the integration of the ON and the OFF time. In this way, any integration error is introduced on both signals and therefore cancels itself over a complete switching period.

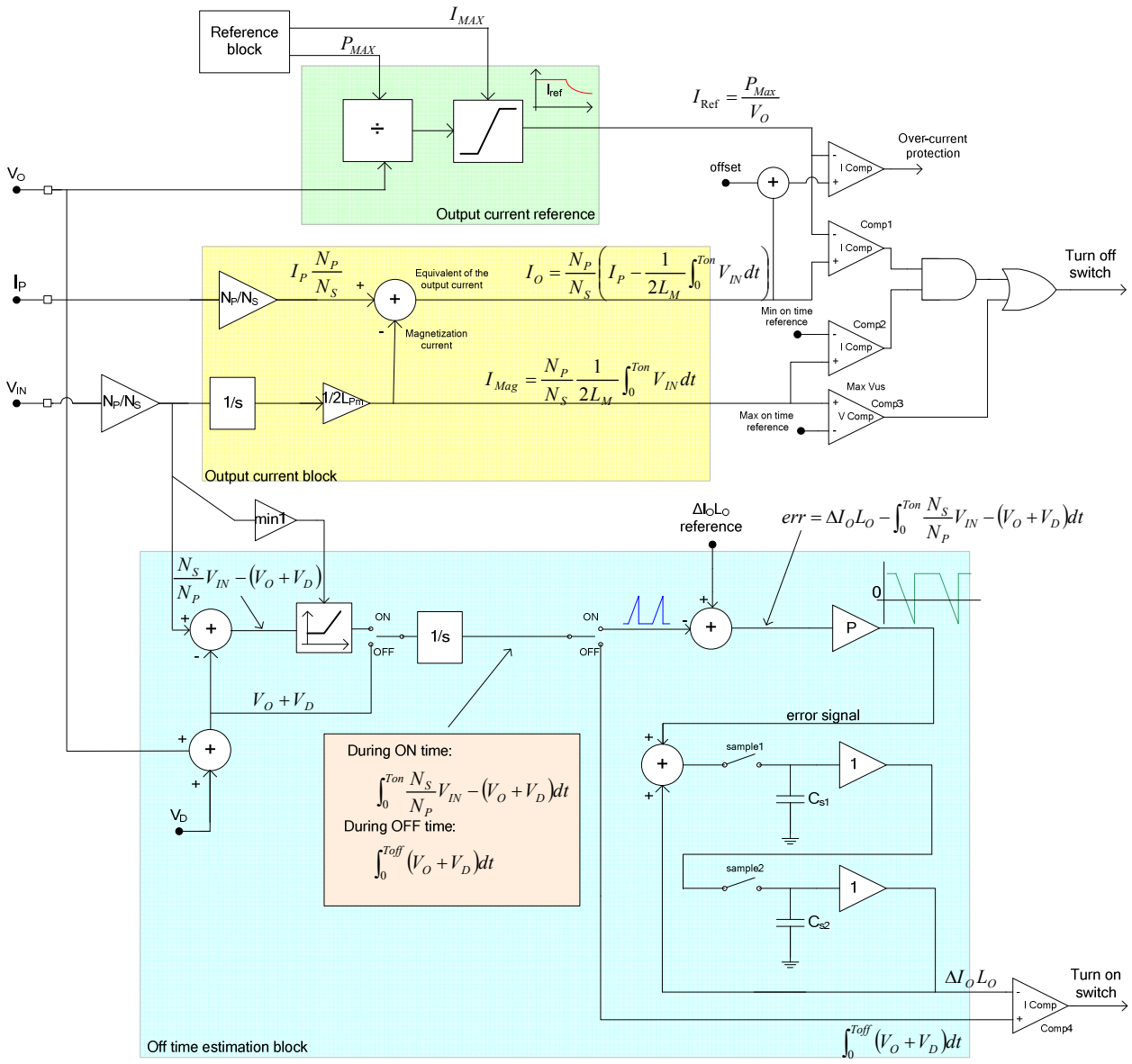


Figure 5. 1. Abstract block diagram of the control circuitry

As the control circuitry is implemented in an analogue current mode, the three input signals (scaled mains voltage, scaled output voltage and the voltage drop on the sense resistor) need to be converted into currents.

The detailed circuit level diagram of the control circuitry is presented in Figure 5.2. The reference for the divider representing P_{MAX} and the current clamping to I_{MAX} are provided by an external bandgap voltage reference and V-I converter. A minimum value limitation has to

be imposed to the current that translates the charger output voltage V_{OUT}, to avoid the division by very small values. The voltage reference also generates the signal corresponding to the voltage drop on the output diode (V_D) in the *OFF time* estimation block.

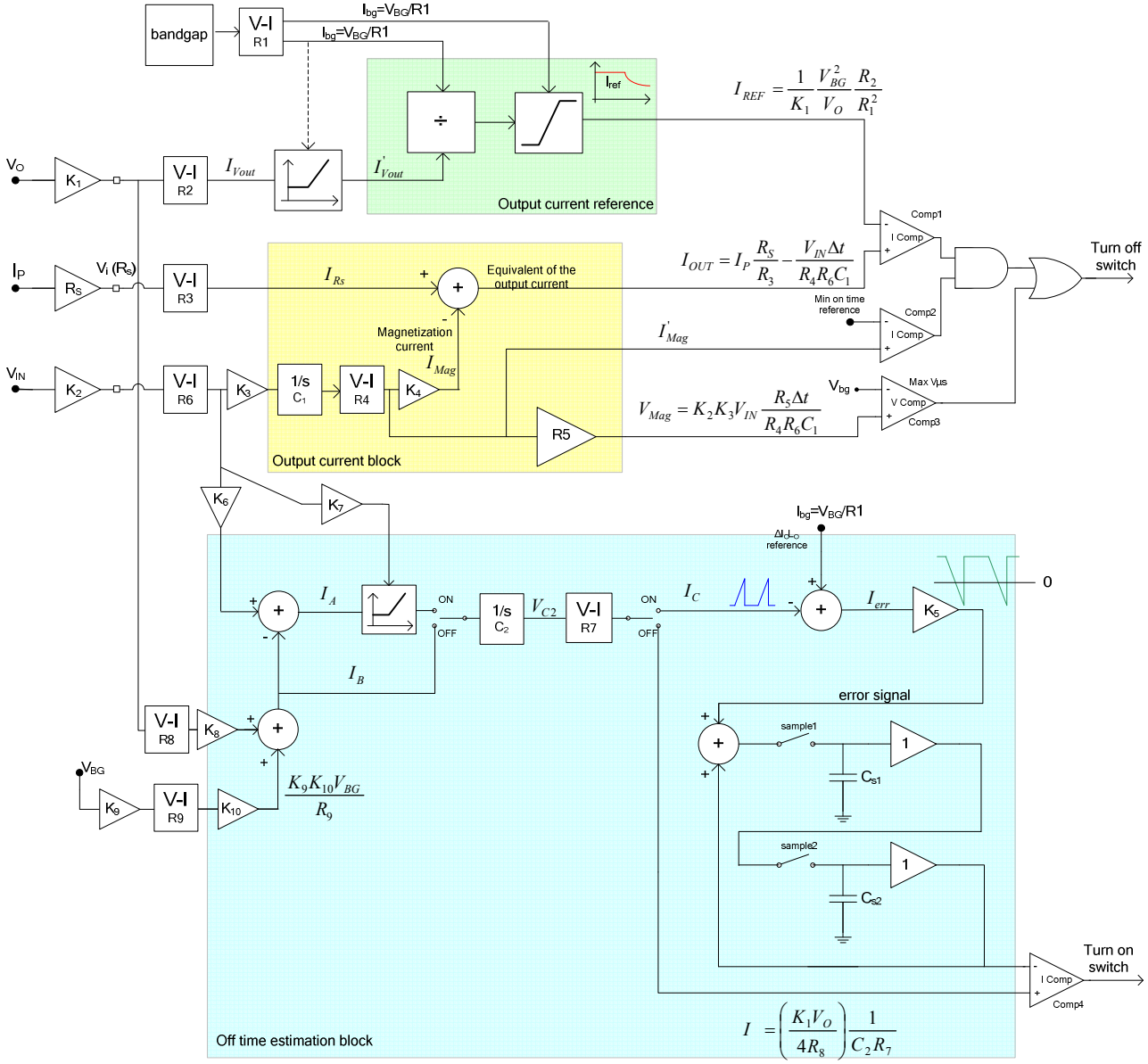


Figure 5. 2. System block diagram with circuit level scale factors

Target Foundry Access Change

Because of commercial decisions in the foundry company, the ability to fabricate the design in the ultra-HV technology was withdrawn part way through the project, and the design work did not proceed as far as tape-out. As a consequence, the whole design had to be transferred to a bulk CMOS medium voltage technology from AMS Microsystems. Since this technology has a maximum voltage capability of 50V, the design strategy was changed to include the use of external HV switch transistors, leaving only medium voltage driver circuits

on the die. Hence the following chapters are organised as follows. The next chapter looks at the design specific to the NXP EZ-HV technology and the way the technology limitations have been overcome. In the following chapter, the design presentation continues with the blocks that have been adapted to the AMS process, and the novel circuitry developed for this specific process and system integration.

5.2 Monolithic design for ultra high voltage technology (650V)

The technology intended for this IC version of the design is the NXP EZ-HV process [60]. This is a single metal, SOI process with power MOSFETs, IGBTs and JFETs suitable for operating voltages up to 650V. Besides the high voltage N-channel MOSFET there are also available a medium and a low voltage double diffused MOS transistors. The technology also offers two vertical NPN transistors for low and medium voltages, derived from the NDMOS transistor with separate source and body. Two types of PMOS devices are available for high-side applications, the tradeoffs being made between threshold voltage, β and matching.

5.2.1 Voltage-to-current converter

The V-I converter is one of the circuits that will influence strongly the behaviour of the power converter with its accuracy. Besides that, it should also have a very good immunity to temperature, low offset, large input voltage range and high input impedance. The standard implementation of a V-I (op-amp, source follower and resistor) is impractical in this case due to the projected area of a suitable op-amp in this technology, and parasitics that incur a limited bandwidth. An attractive alternative option in this case is a topology based on the translinear principle for bipolar transistors [35].

Before going further in the circuit analysis, we should look at the parameters of the NPN transistors in the HV-SOI process being used. The selected technology contains only a low and a medium voltage lateral NPN, with a typical β_F=45. Both are derived from layouts normally used for the NMOS devices. The theory of translinear circuits assumes that the current gain of the transistors is large enough so that the base currents can be ignored. Clearly this is not the case in this technology, and special attention must be paid to this aspect. Another source of errors is the Early effect, but in our case it will have a small contribution as the Early voltage is above 300V (ΔV_{CE}=1V introduces an error of 0.33%) . Nevertheless, we will try to bias the collector-base junctions at the same voltage to minimise any impact.

The translinear circuit principle also assumes a high linearity between the value of $\log(I_C)$ and V_{BE} over many decades. Practical measurements and simulations of the bipolar transistors show that at high collector currents, the base current is high as well, and it causes a voltage drop ΔV_{Rb} on the extrinsic (or lateral) base resistance (R_b) [26],[27]. As a result, the collector current increases linearly after a certain point and the V_{be} becomes a mixture of linear and logarithmic terms:

$$V_{BE} = V_T ln \frac{i_C}{I_S} + \frac{R_b i_C}{\beta} \qquad (5.1)$$

Figure 5.3 presents the plot of $\frac{d(\ln(I_C))}{d(V_{BE})}$ versus V_{BE} for a low voltage transistor with emitter area A_E=40x40µm^2. It can be observed that for current values above 25mA the slope of the plot decays considerably. Hence for good linearity, the design of the circuit should ensure that the unit collector current does not exceed this value.

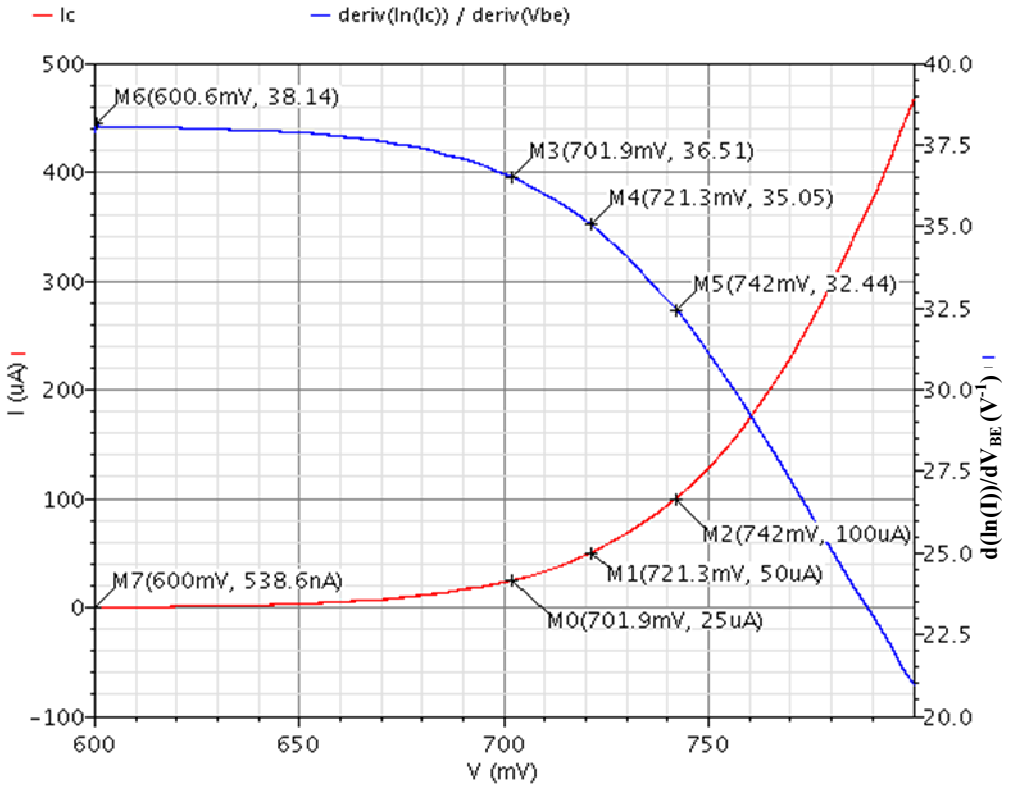


Figure 5. 3. High collector current effect: (blue) - $d(\ln(I_C)) / d(V_{BE})$; (red) – Collector current

Considering the above limitations we can distinguish three circuits that would comply with our requirements [26],[28],[29]. Even though the performance of the first circuit is below the one presented in [29], we have selected it for the reduced number of bipolar transistors (see figure 5.4) as being more suitable for such a coarse geometry process. Having only four devices that determine the performance of the circuit allows us to get good matching and base

current compensation, and thus we can diminish the effects of low β_F. The circuit is based on the translinear cross-quad pair and can be implemented either with NPN or PNP transistors.

Due to the cross-quad arrangement of the transistors the collector currents are equal (for $Q_1 - Q_3$ and $Q_2 - Q_4$) while the base-emitter voltages cancel:

$$I_{C1} = I_{C3} \quad \text{and} \quad I_{C2} = I_{C4} \tag{5.2}$$

$$\rightarrow \; I_{C1}I_{C4} = I_{C2}I_{C3} \tag{5.3}$$

As I_C is an exponential function of V_{BE}, for equal emitter areas this can be translated into base-emitter voltages as:

$$V_{BE1} + V_{BE4} = V_{BE2} + V_{BE3} \tag{5.4}$$

Therefore the emitter of Q_3 will have the same potential as the emitter of Q_4, hence creating a virtual ground. At low frequencies the input impedance is:

$$r_{IN} = \frac{4V_T}{\beta I_0} \tag{5.5}$$

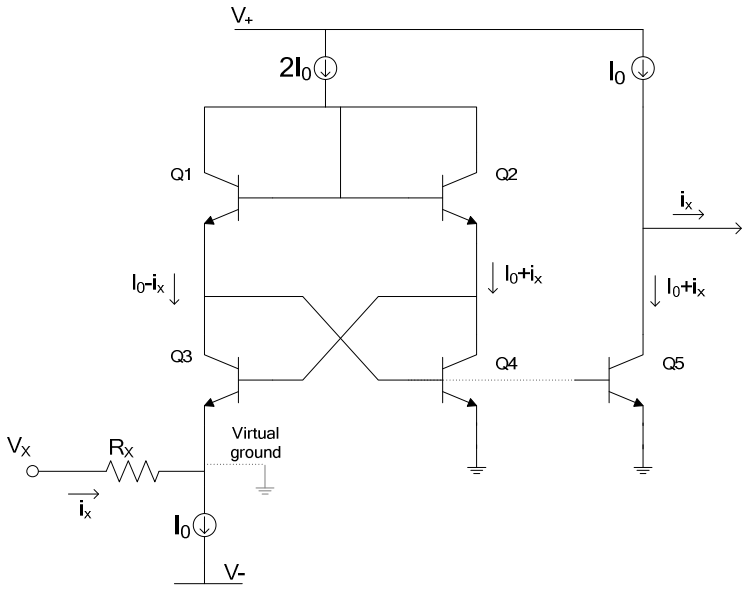


Figure 5. 4 Voltage-to-current converter core

In the current HV technology for I_0=100µA the input resistance is about 23Ω (emitter area A_E=40x40µm^2). The problem of the input resistance is mainly the variation with temperature and collector current. The entire input resistance (including the error) can be neglected for large values of R_X. The output of the circuit is available as a differential voltage in translinear form or as single ended mirrored current, as depicted in figure 5.4. A cascode transistor can be added on top of Q_5 (biased from the base of $Q_{1,2}$) to match the collector voltage of Q_5 with Q_4 and increase the output impedance.

For high β_F and large ratios between I_0 and i_x the base currents cancel each other: $I_{B1} \approx I_{B4}$ and $I_{B2} \approx I_{B3}$. Thus the collector currents obey the equation (5.2). Unfortunately this is not the case with the current technology and we must introduce special circuitry to compensate these currents. The reason for which the bias current (I_0) can not be made very large with respect to the input current i_x is because of the collector current spreading resistance. Four transistors have been connected in parallel to alleviate this and improve the matching of the bipolar devices.

The error resulting from the base current is compensated with the aid of additional circuitry, depicted in figure 5.5. Transistors Q_1' and Q_2' are matched with Q_1 and Q_2, respectively, and have been introduced for the purpose of measuring the equivalent base current for the two branches. The base current of Q_2 is subtracted with the aid of MOS transistors M_2, M_3 and M_4. Also, the base current of Q_4 is injected through M_5. The circuit used for the base current compensation of Q_1 and Q_3 is similar to the one for Q_2 and Q_4.

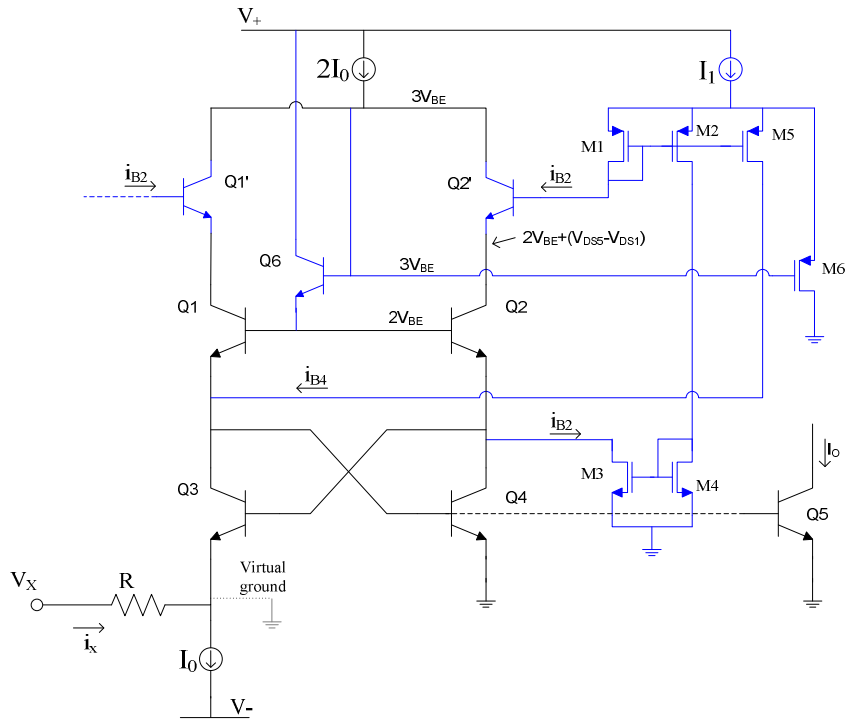


Figure 5. 5. Voltage-to-current conversion circuit including the base current compensation

The high-side current mirror (I_1) cannot be connected straight to V_{DD} as it would set the collector voltage of Q_2 to a potential $V_{DD} - (V_{Tp} + V_{DSat1} + V_{BE})$. The role of M_6 connected as source follower is to provide a collector-base voltage for Q_1 and Q_2 independent of the power supply. Thus the collector potential of Q_1 and Q_2 is always held at approximately $2V_{BE}$. The bias current I_1 has to be slightly larger than the current $4I_0/\beta_{min}$in order to supply the base currents for Q_2', Q_2, Q_4, and Q_5. Transistor Q_6 has been introduced to ensure a constant bias

for the collectors of Q_1' and Q_2' ($3V_{BE}$). The complete schematic of the V-I conversion circuit is attached in appendix 9.

5.2.2 Current divider

The output current reference block is composed of two parts, a current divider and a limiting circuit. The divider is required to operate only in the first quadrant, thus a basic translinear-loop circuit has been used to achieve this function. Even though translinear signal processing is generally considered obsolete in modern CMOS processes and replaced by digital techniques, the isolated NPN transistors available in medium and high voltage technologies make it a clear choice in this case. Taking into account the issues for the bipolar devices mentioned in the previous section (low β and significant collector current spreading resistance), the selected circuit uses only four transistors [26],[30], see figure 5.6. The base-emitter voltages of the four transistors build a translinear-loop, thus we can write the following equation for the collector currents:

$$\frac{I_1 I_2}{A_1 A_2} = \frac{I_3 I_4}{A_3 A_4} \tag{5.6}$$

In order to reduce the errors introduced by the mismatch we will start by setting all the emitter areas equal (A_1=A_2=A_3=A_4). Therefore the value of the output current, I_4 becomes:

$$I_4 = \frac{I_1 I_2}{I_3} \tag{5.7}$$

In our case, I_3 represents a current proportional to the output voltage, while the product I_1I_2 is the equivalent of the maximum power delivered by the charger. The value of I_4 will give the reference for the output current of the converter.

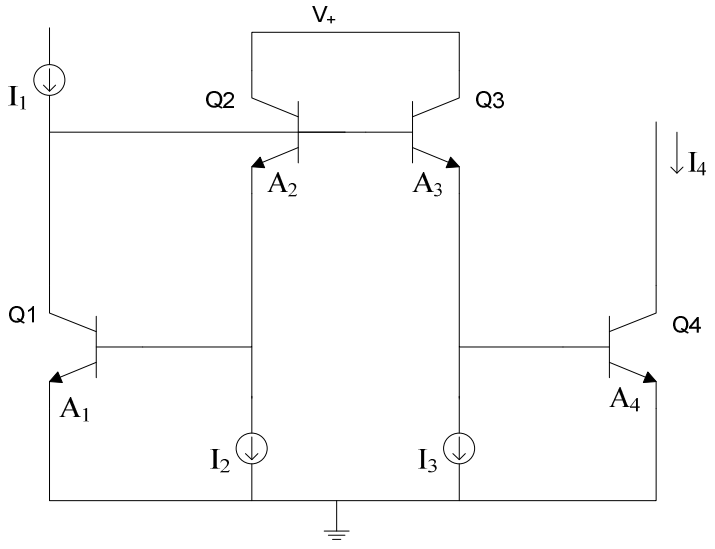


Figure 5. 6 The core of the TL multiplier/divider

Three main sources of errors have to be considered in this case: base currents, collector current spreading resistance and the Early effect. As the circuit is not symmetrical, for low β transistors the accuracy will be low even if the values of the collector currents are close. Therefore the need for a base current compensation circuit is imperative. The collector-base voltage of Q_1 is fixed to a certain value ($2V_{BE}$ in this case), while V_{CB4} will be determined by the circuit connected to the output, and hence a considerable error is introduced by the Early effect, as the supply voltage is 14V (ΔV_{CE} can reach values in the region of 10V, resulting an error of 3.3% for V_E=300V). The errors introduced by the Early effect for Q_2 and Q_3 can be neglected as they cancel each other. If the areas of the transistors are not sized appropriately, then for large ratios between collector currents the associated increase of the base resistance will also introduce large errors, (see figure 5.3).

The base current compensation circuit is very similar to the one used for the V-I conversion (see figure 5.6). In order to simplify the circuit we have set I_1=I_2, and hence the entire base current injected by Q_2 flows in the base of Q_1. Thus the collector currents of Q_1 and Q_2 are equal to I_1 and I_2 without the need for any additional circuitry. However, we still we need to introduce transistors Q_6 and M_1 to ensure the matching of the collector potentials between Q_2 and Q_3.

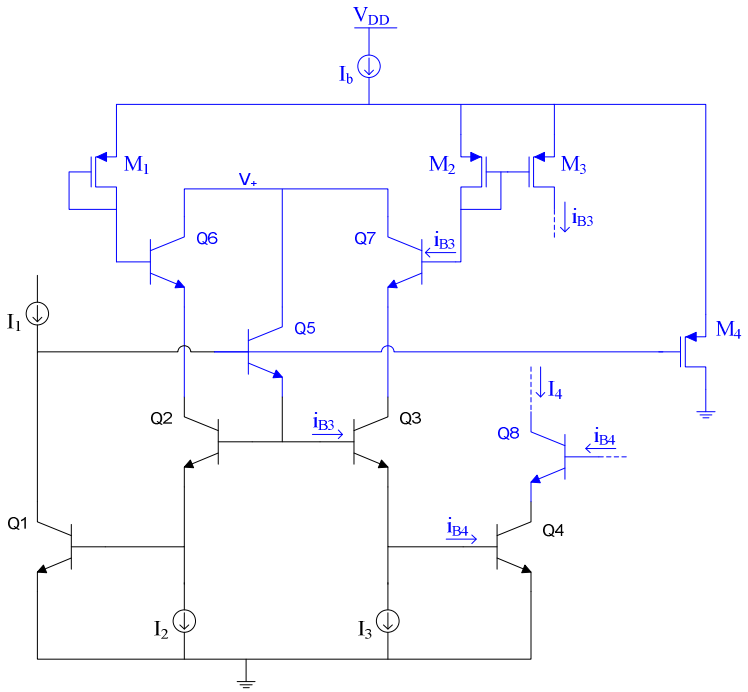


Figure 5. 7 Divider circuit including the base current compensation

As we have seen before, the value of I_4 has to be limited to the equivalent of 30A (output inductor current), and thus we have added a current limiting circuit at the output. Also, a limiting circuit for the minimum value of I_3 must be added to prevent the division by

zero or small values. The operation of the limiting circuit and the schematic of the divider circuit are presented in appendix 10.

5.2.3 Current sampling circuit

The current sampling circuit can be considered the core circuit of the off time estimation block. Its accuracy is very important as it will determine the stability of the feedback loop. The principle of current memories has been used over the years for dynamic current mirrors, switched current circuits [30-35], DAC trimming and amplifier offset cancellation. Figure 5.6 presents the simplest forms of a sampled current cell and it works as follows. During phase Φ_1 (S_1 and S_2 closed, S_3 open) transistor M1 is diode-connected and the drain current is the sum of the bias current I_0 and input current *i*. Capacitor C is charged to a voltage required to hold the total drain current. On phase Φ_2, (S_1 and S_2 open, S_3 closed) the capacitor C keeps the gate voltage constant and M1 behaves as a current source, holding the drain current constant to the value sampled in phase Φ_1, forcing the output current $i_{out} = -i$.

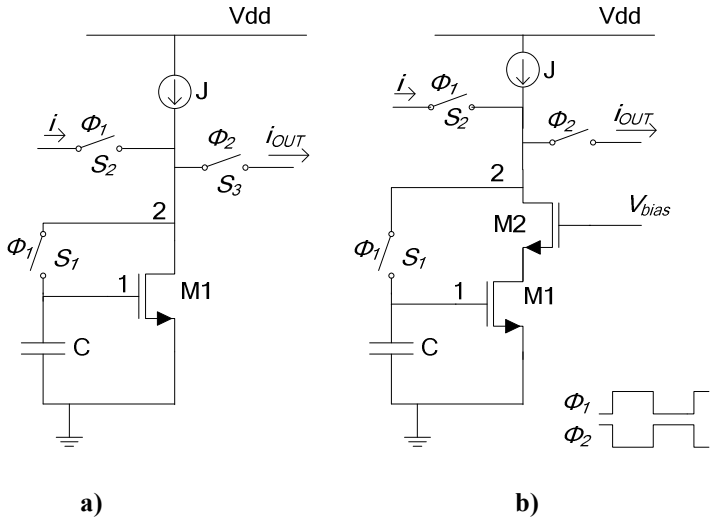


Figure 5. 8 a) Simple current sampling cell; b) Cascoded current sampling cell

When implemented in a standard CMOS technology there are five main limitations for the accuracy:

1. Channel length modulation: The drain voltage of M1 can change between the sample and hold phases. For a settled input signal, the value of V_{DS} during Φ_1 is equal to the gate voltage. On phase $\Phi_2$the drain voltage of M1 will be dictated mainly by the conditions in the output circuit. Thus the variation of the drain-source voltage will lead to a drain current error:$I_\varepsilon = \lambda(V_{DS1} - V_{DS2})$.

2. Charge fed through C_{DG} of M1: The variation of the drain potential of M1 will inject a certain charge through C_{DG} of M1, altering the sampled gate voltage and hence the drain current.

3. Switch inversion layer charge injection and clock feedthrough (CFT): When the sampling switch MOSFET (S1) is turned off the charge in its inversion layer will split between the drain and the source. This charge will alter the gate voltage by ΔV and hence alter the drain current by $I_\varepsilon = g_{m\_M1}\Delta V$. As the g_m for a saturated device is approximately a function of $\sqrt{I_{DS}}$ (in typical operating regions) the absolute error will be a function of the signal.

The parasitic capacitance between the gate and source (node 1) of the switch MOSFET is also coupling into the sampling capacitor the digital signal driving the gate of the switch. Hence when an NMOS switch is turned off it will reduce the voltage stored in a sampling capacitor by a factor: $\Delta V_{sample} = \Delta V_{sw\_gate} {C_{gs\_sw}}/{(C + C_{gs\_sw})}$. Where ΔV_{sw_gate} is the amplitude of the digital signal driving the switch gate C_{gs_sw} is gate-source capacitance of the switch and C is the sampling capacitor. This source of error can be assumed constant and therefore compensated by the feedback loop in the current system.

4. Finite resistance of the cascode transistor: Cascoding is one technique commonly used to address the effects of channel length modulation in this cell, as shown in figure 5.8 b. If there is a large variation in the output node potential (of the order of 5-8V is expected in this application) between the sample and hold state, then due to the finite output impedance of M2, the drain voltage of M1 will also change by up to a few hundred millivolts. Even though this variation will not produce a large error by means of channel length modulation of M1, it will inject a charge into C through the C_{DG} of M1. As the resulting error is a function of the g_m of M1, and hence is signal current dependent, it cannot be compensated afterwards. This error is accentuated in the HV processes due to the large overlap capacitance and higher supply voltage, which leads to a larger swing at the current summing node (2).

5. Settling time in sample state: The large swing of node 2 (figure 5.8 b) has another consequence at the moment of transition from hold to sample state. Even if switch S_1 is turned on with a certain delay after the actuation of S_2 and S_3, node 2 can still have a high potential compared with node 1, depending of the ratio between the values of the previously sampled current and the new input current. The parasitic capacitance of node 2 will produce a considerable alteration of the voltage of node 1, at the moment when S_1 is turned on; thus increasing the settling time of the circuit. As result, even if the variation between consecutive

samples is small, the sampling speed will be affected. The capacitance of node 2 is the result of the overlap capacitance of three transistors and the associated tracks, hence it will be larger for circuits sampling high currents. This problem will particularly affect circuits with multiplexed inputs or outputs, having more switches connected in parallel.

The following paragraphs present the existing methods to overcome the above mentioned limitations together with a novel circuit aimed to improve the performance of the current memory.

The channel length modulation and the Miller charge feed-through can be overcome by using a cascode transistor (see figure 5.8 b) or forcing the drain voltage during the two cycles to a specific value [31]. The constant bias for the cascode presents the risk of pushing the sampling transistor into triode operation for large values of the signal. One way to avoid this is to force the memory transistor to operate in triode region for the whole input range. The constant g_m of M1 turns the clock feedthrough charge into a constant current error, which can be subtracted afterwards. The trade-off in this case consists in the limited input signal range, due to the large V_{GS} of M1 incurred by the triode region operation.

The charge injection and clock feedthrough can be reduced by using half-sized dummy switches operated in anti-phase with the main switch, or by using a capacitive divider [32]. This compensation method relies on the assumption that the charge in the inversion layer is divided equally between the source and the drain, when the switch turns off. Usually when the speed of the circuit is not a constraint, the size of the switch is made minimum size in order to reduce the amount of charge in the channel. The usage of the dummy devices imposes the constraint on the sampling switch of being at least twice the minimum allowable device width.

Many of the above sources of errors can be diminished by increasing the size of the sampling capacitor, but this will result in longer settling times and larger die area.

The topology presented in the following discussion aims to overcome the foregoing limitations and reduce the errors specific to the HV technology (i.e. large overlap capacitance and the finite output impedance of the cascode combined with the large swing of the node). The circuit is presented in figure 5.9 and it operates as follows. Transistor M_1' (matched with M_1) provides a copy of the sampled current. The op-amp regulates the gate voltage of M_2'so that the drain and the gate voltages of M_1' are equal. As transistors M_2 and M_2' are matched the source potential of M_2 during phase Φ_2 is maintained at the same value as in phase Φ_1 when M_1 was connected as a diode. In this way, we ensure a constant voltage for the drain of M_1 during both phases, eliminating the effects of channel length modulation, Miller

capacitance feed-through and switch S_1 drain-to-source charge feed-through. The variation of M1 drain potential is reduced by a factor of:

$$\frac{\Delta V_{DS\_M2}}{\Delta V_{DS\_M1}} = A_{OA}\left(g_{m2}r_{DS2} + \frac{r_{DS2}}{r_{DS1}} + 1\right) \qquad (5.8)$$

As the attenuation of the drain potential fluctuation between phases is aimed to be in the region of 60dB, a single stage transconductor with wide bandwidth can be used. The benefits of enhancing the output resistance using an op-amp have been initially presented in [41]. In this case, the non-inverting input of the amplifier is biased from a constant voltage; hence the range of the input current is limited and the potential of node (2') changes between stateΦ_1 and Φ_2.

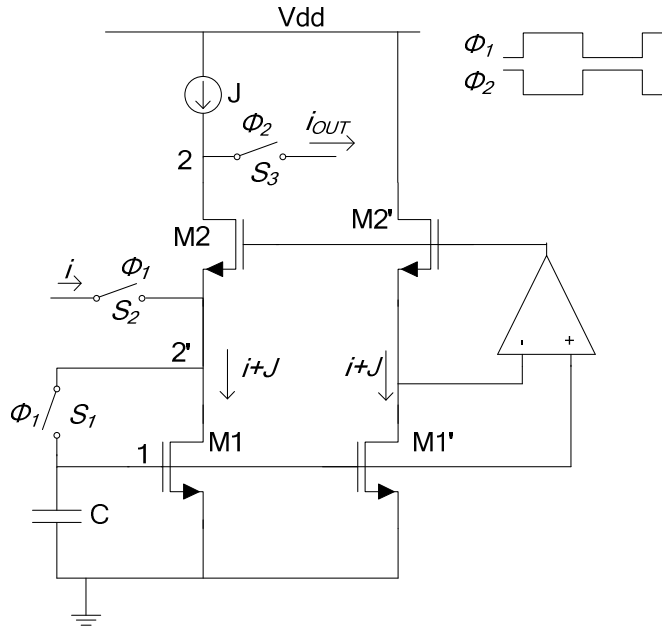


Figure 5. 9 Modified cascoded current mirror

Besides the error cancellation capability, the circuit also adds the benefit of ensuring that M1 operates in the saturation region, regardless of the input current. Also, as the potential of node (2') is held constant and equal to node (1), it will result in a better symmetry for the division of the injected charge due the switch turn off [42].

Due to the connection of switch S_1 below the drain of M2, the sampling switch is fully isolated from the swing of node 2. Hence reducing the charge fed through from node 2 (through the C_{DS} of the switch) at the transition of this node from high impedance to low impedance (hold to sample phase), resulting in a faster settling time.

The circuit presents two feedback loops in parallel, comprising M1 – op-amp – M2, and op-amp - M2' (and r_{DS1}). During the sampling state (when S_1 and S_2 are closed), the first loop

forms a positive feedback path, while the feedback in the second loop remains negative. Because M1 is diode connected, the positive loop gain is $A_{OA}g_{m2}/(g_{m1}+g_{m2})$, (neglecting body bias effects). On the other side, the negative feedback loop presents a gain of $A_{OA}r_{DS1}/(1/g_{m2}+r_{DS1})$ which is larger and hence will dominate the overall response, ensuring the stability of the complete circuit.

Several simulations have been conducted to demonstrate the operation of the circuit. First, statistical simulation (based on the variance data from the foundry) analyses the influence of the mismatch and process parameter variation (see figure 5.10). The input current is swept from 50µA to 300µA, with a step of 25µA. The range of the sampled current extends above 300µA with an error below ±0.1%.

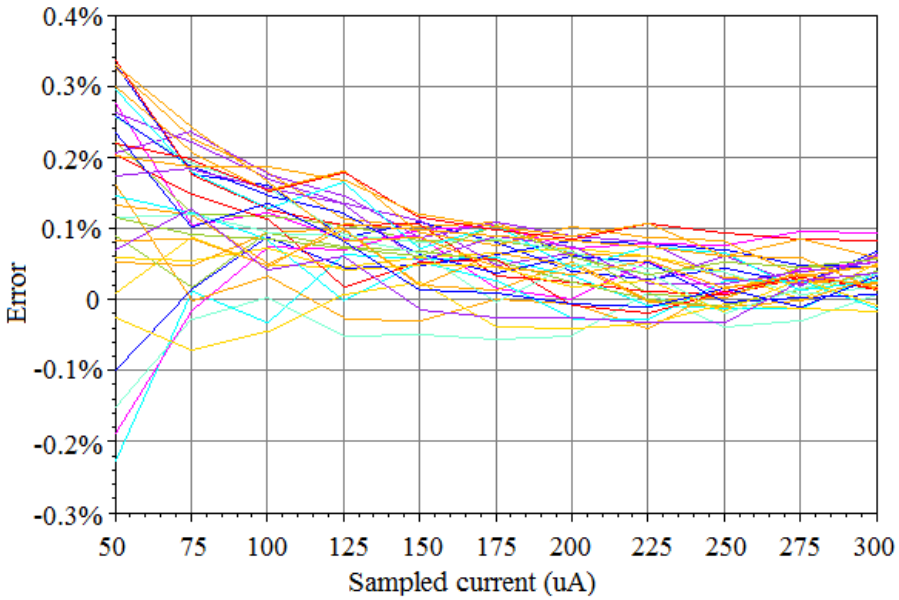


Figure 5. 10Monte Carlo Simulation of the current sampling circuit

To demonstrate the immunity of the sampled current to the supply voltage we have simulated the operation of the circuit for supply voltages between 10V and 14V (figure 5.11). Comparing the statistical (figure 5. 10) and the nominal (for multiple Vdd values) simulations we can observe that for small currents the mismatch between M1 - M1' and M2 – M2' dominates the sampling error. As the threshold voltage of the MOSFETs is in the region of 3.5 - 4V in this HV technology, then for lower supply voltages and high currents the amplitude of the error tends to increase slightly due to the reduced headroom for the cascode devices. The reduced headroom affects the V_{DS} of the cascode devices forcing their operation towards triode region and hence reducing the cascode output impedance.

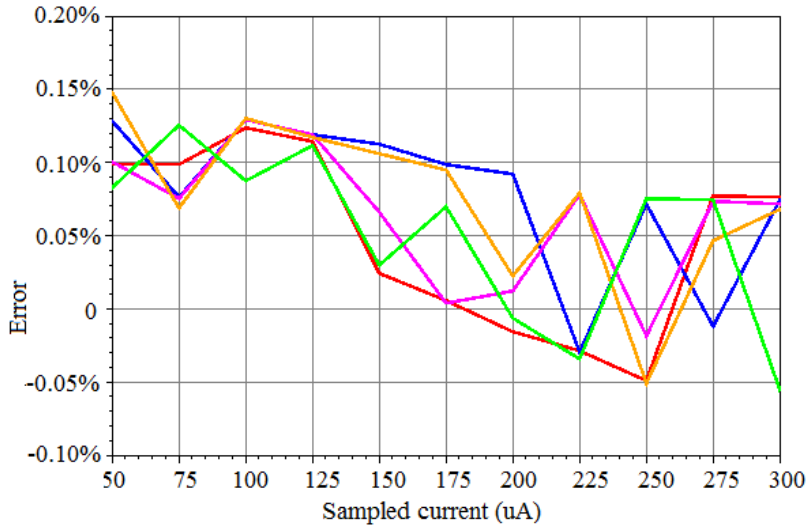


Figure 5. 11 Nominal simulation for the absolute error with multiple V_{DD} values: (blue – V_{DD} = 14V; magenta - V_{DD} = 13V; yellow - V_{DD} = 12V; red - V_{DD} = 11V; green - V_{DD} = 10V)

Figure 5.12 shows the comparison between the settling time of the proposed servo cascode cell and the constant bias memory (figure 5.8 b). In this case the bias current (*J*) is set to 100µA and the sampled current alters between 80µA and 90µA. During the sampling phase, the settling time for both circuits is determined by the ratio g_{m1}/C. Hence, in order to reduce the settling time further it is necessary to either increase the g_m of M1 or reduce the size of the sampling capacitor (figure 5.8 and 5.9). The main tradeoff in both cases would be a larger current sampling error due to the increased sensitivity to switch charge injection.

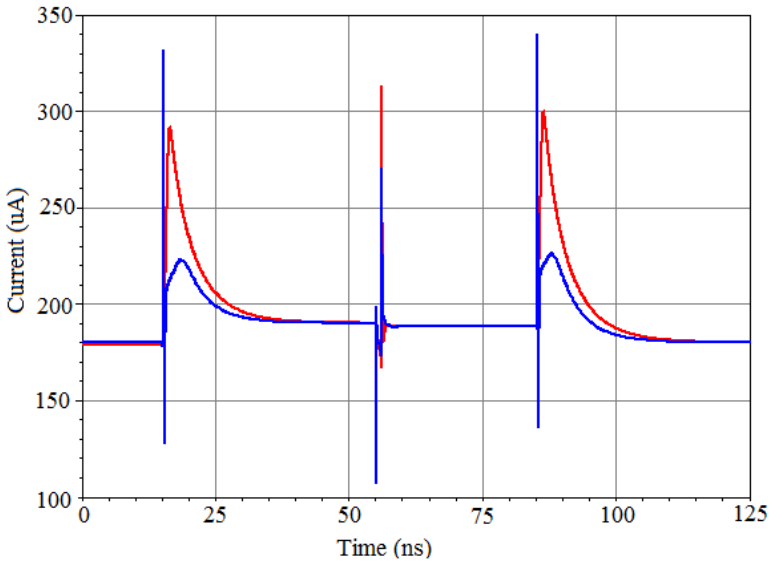


Figure 5. 12 Transient simulation for the settling time of the sampled current current (blue – servo cascode cell; red – constant bias cascode cell)

Two-step current sampling circuit

In the circuit in figure 5.9 the main source of errors comes from the poor compensation of the switch charge injection. The most effective way of removing this error is to replace the saturated transistor M1 with a device that has a transconductance that is independent of the sampled current. The constant transconductance will convert the quasi-constant charge injected in capacitor C into a constant current error (independent of the signal) that can be compensated by offset cancellation techniques. The constant g_m transconductor can be achieved by source degeneration, triode region operation [31], two step sampling [35],[41],[44] or with a constant g_m circuit. The source degeneration and the triode region operated transistor come with some limitations on the input signal range. The two-step sampling technique was first presented in [43], providing an efficient first order error cancellation at the cost of only a few extra devices. The drawbacks in this case are the large transients resulted when switching between the NMOS and PMOS current samplers and the difficulty of cascoding. The S^2I circuit shown in [41] employs NMOS devices both for the coarse and the fine sampling cells. In this case the clock feedthrough (CFT) compensation is made by using a larger switch for the coarse sampling cell and a minimum size switch for the fine sampling one. In this way a fast settling time is achieved, and the final error due to CFT is determined by the minimum size sampling switch. The circuit presented in [44] is a significant improvement from the accuracy point of view, but it requires multi-step sampling and multiple stages, and hence has some speed penalty.

To address these issues, a new error cancellation scheme has been developed based on an NMOS two step topology, similar to the one in [41]. The actuation of the switches in this case is made by non-overlapping clock signals and the CFT error is signal independent. As the cell is used in combination with the servo cascode described above, it also fully cancels the channel length modulation and C_{DG} charge injection errors.

The principle of the two step non-overlapping coarse and fine sampling is described using the diagram from figure 5.13. The sampling phase, Φ_1 is split into two sub-phases for coarse and fine sampling, Φ_{1a} and Φ_{1b}, respectively. During Φ_{1a} the fine sampling block operates as a current source (in hold state), set to a value equal to the bias current (J), while the coarse sampling block (in sample state) draws the whole input current. At the end of the first sub-phase and the beginning of the second one, the two sampling blocks change states (fine sampling block goes into sample mode and the coarse sampling goes into hold state). Hence, the current in this sub-phase for the coarse block will be the previously sampled input current minus a small sampling error i-ε_1. Thus the current to be sampled by the fine

sampling cell is $J+\varepsilon_1$. As the sampling error of the coarse block (ε_1) is very small in comparison with the bias current (J), the fine sampling block can be considered to have a constant g_m. Therefore when the circuit turns from phase Φ_{1b} to Φ_2 (when both sampling blocks are in hold state) switch charge injection will generate a constant error (ε_{ct}), that can be compensated in subsequent manipulations, if required.

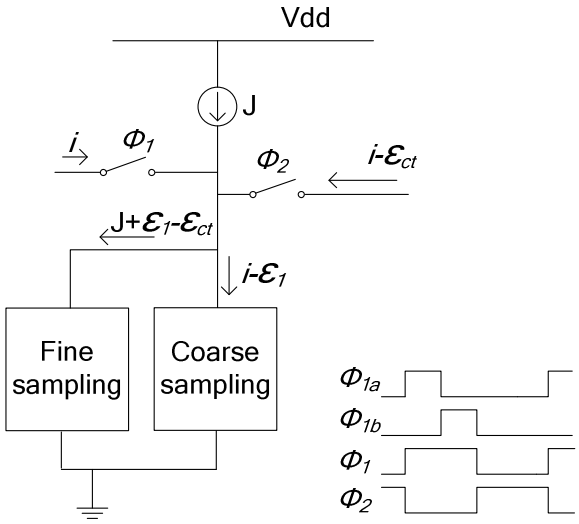


Figure 5. 13 Double sampling circuit – block diagram

The CMOS implementation of the foregoing principle is presented in figure 5.14. The coarse sampling is done by transistor M3 (during Φ_{1a}) while the fine sampling is performed by transistor M1 (during Φ_{1b}).

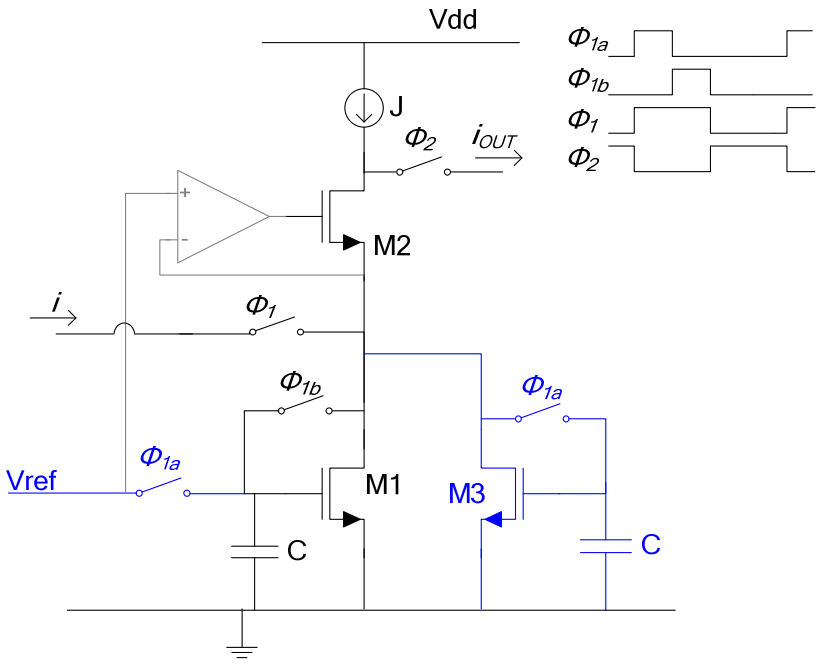


Figure 5. 14 Two step sampling circuit diagram and control signals

During the first sub-phase (Φ_{1a}) transistor M1 is connected as a current source with a drain current approximately equal to the bias current J (see figure 5.15 a). The entire input current will be forced into the drain of the diode connected transistor, M3. At the end of Φ_{1a} the input current is sampled with M3, resulting a drain current of $I_C = i - \varepsilon_1$.

In sub-phase Φ_{1b} transistor M3 is drawing the current sampled in the previous phase and M1 is diode-connected (see figure 5.15 b). Because the sampling error for M3 is small, the drain current of M1, $I_F = J + \varepsilon_1$ will be very close to the value of the bias current, *J*. Therefore the transconductance of M1 can be assumed to be constant. For a constant g_m of M1, the resulting clock feedthrough error (ε_{ct}) will also be constant and easy to compensate at a system level, if required.

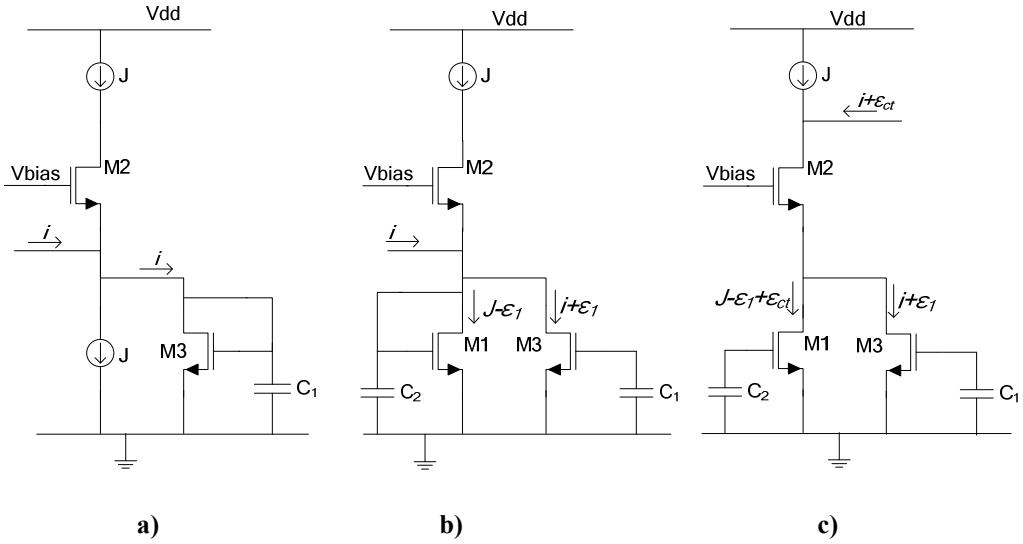


Figure 5. 15 Detailed operation of the current memory
a) state Φ_{1a}; b) state Φ_{1b}; c) state Φ_2

Statistical simulations have been conducted for the circuit above with the servo cascode circuit using foundry model variance data. The maximum variation of the error current ($\Delta\varepsilon_{ct}$) for signals between 50µA and 300µA is 44nA. Thus the differential error between subsequent current samples is between 880ppm (for *i*=50µA) and 146ppm (for i=300µA). Figure 5.16 presents the absolute error of the circuit equipped with a simple PMOS current sampler for offset compensation. The relative error between different circuits sampling the same current is below ±46nA within the entire operating range.

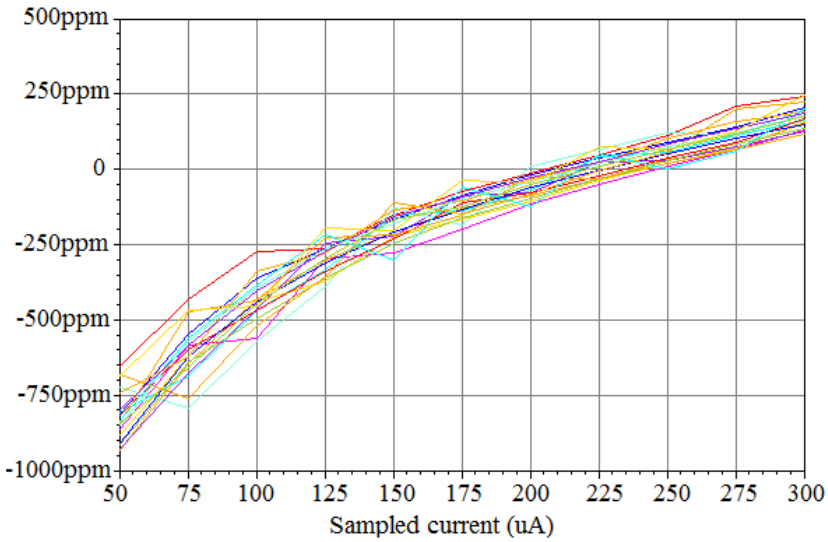


Figure 5. 16. Monte Carlo simulation for the absolute error of the double sampling circuit in ultra-HV technology

5.3 Monolithic driver design in medium voltage technology (50V)

As mentioned before, due to commercial impediments, the design had to be transferred to a publicly accessible multi project wafer (MPW) process. Because a 650V BiCMOS process was not available for fabrication, the power MOSFETs had to be implemented off-chip. Hence the integrated circuit implementation of the analogue system was comprised of the control circuitry and output drivers, while discrete components were be used for the power switches. With these constraints, the design was migrated to a 0.35µm bulk CMOS process with a maximum drain-source voltage of 50V. The process has been adapted from the standard 3.3V CMOS technology by adding 20V and 50V CMOS compatible DMOS devices, fabricated in a deep n-well. This feature also allowed the development of the isolated low voltage MOSFETs and most importantly, a vertical NPN transistor. The presence of the bipolar transistors is very useful as it facilitates the transfer of the translinear divider circuit from the previous technology. The process also features lateral and vertical PNP bipolar transistors, four metal layers (with thick top metal), polysilicon-insulator-polysilicon (PIP) capacitors (0.86fF/µm^2) and high value polysilicon resistors.

5.3.1 System integration

The same IC architecture has been preserved as for the ultra-HV process in order to ensure good immunity to switching noise, simplicity of the summation circuits and for a good reuse of the circuitry already developed. It was also intended that the design could be easily

re-worked for a fully integrated implementation should an ultra-HV process become available again at a later stage.

The first change made, with regard to the previous (for the ultra-HV process) topology, is the V-I conversion circuit. In this case, it is more feasible to implement this circuit using a more conventional op-amp with source follower loop. The main limitation arises from the input range of these V-I converters (there were no serious restrictions in the previous UHV design). As we will see later, due to the variation of the resistors value over process corners, the input range of the V-I circuits is between 0 and 1.35V. As a consequence, the V_{OUT} and V_{IN} signals have to be scaled to fit in this range. Further, as the low-voltage core transistors and pads for the current technology can tolerate a maximum of 3.3V, the scaling has to be done off-chip by resistive means.

One of the main problems of integrated circuits that are using resistors and capacitors is the absolute variation of these components between wafer lots in manufacture. In the case of the Austria Microsystems H35 process, we can observe a tolerance of ±20% and ±10% in the case of polysilicon resistors and capacitors, respectively. For this reason a method of compensation becomes imperative. This is achieved in our case by two means: architecture level compensation and resistive/capacitive trimming.

The architecture level compensation of the errors introduced by the absolute value resistor variation is achieved by ensuring that all channels are affected by the error in the same proportion. Assuming that the products C_1R_4 and C_2R_7 (see figure 5.17) are constant, the equation of each signal from the inputs of the current comparators can be expressed as $f\left(\frac{1}{R_i}\right)$ or $f\left(\frac{R_i}{R_j^2}\right)$. In both cases the rank of the denominator is greater by one than the rank of the nominator, in terms of R_{POLY}. This way both inputs of the current comparators will be affected by the resistor variation in the same proportion, resulting in a full error cancellation.

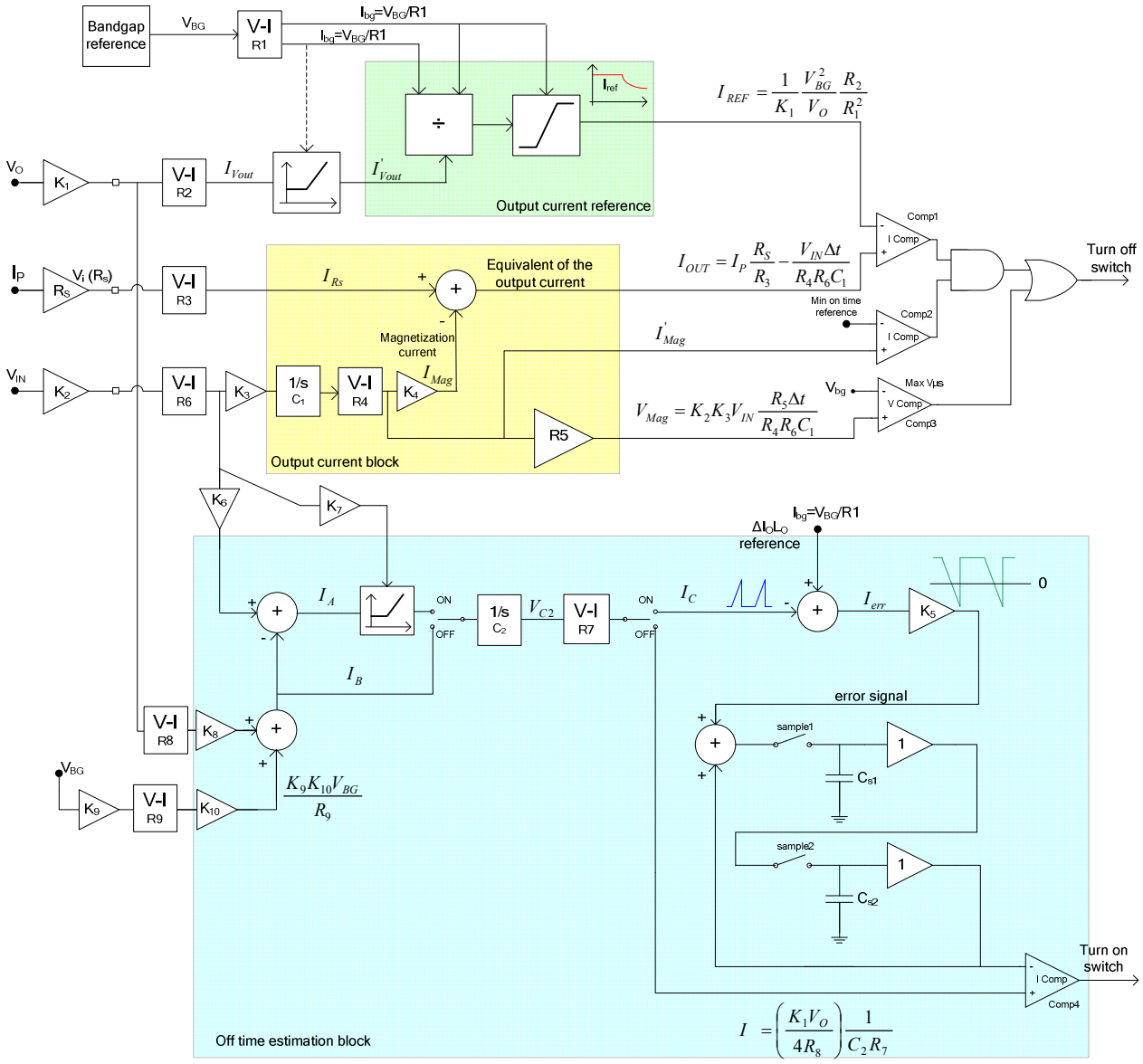


Figure 5. 17. Detailed block diagram of the control circuitry with physical component scale factors

The resistive and capacitive trimming is split into two categories, coarse and fine trimming. The coarse trimming is made with the aid of resistors to bring the signals within the optimal range of operation (linearity) of the circuits. This type of trimming allows us to reduce the absolute tolerance of the signals from ±20% to ±2.5%. This is mainly required due to the reduced range of linearity of the divider circuit. The fine tuning is achieved with the aid of the capacitors of the two integrators. As we have said before, the products C_1R_4 and C_2R_7 are assumed to be constant and this is achieved by fine capacitive tuning, as we will see in the following paragraphs.

The derivation of the scaling parameters starts from the power block, with the value of the sense resistor. As the maximum value of the output current is 30A and the ratio of the transformer windings is N_P/N_S=28/2, this translates into a primary current of approximately

2.15A plus the magnetizing current. The circuit should also be able to accommodate output over-current situations of up to 2A above the nominal maximum. Hence the maximum current expected in the sensing resistor is 2.5A. Considering the input range of the V-I converter of up to 1.35V, this translates in to a maximum value of R_S=0.54Ω. The trade off in setting the sense resistor value comes from the following aspects: A large value of the resistor is desired as it will lead to a good signal to noise ratio, but if the resistor is made too large it will consume too much from the V_{GS} of the power switches, leading in a higher ON resistance. In this case a value of 1.35V for the source of the power MOSFETs is easy to tolerate, and hence a value close to the maximum is selected: R_S=0.5Ω. The equation that describes the slope of the current in the primary winding of the transformer is:

$$\frac{dI_P}{dt} = \frac{V_{IN}}{L_{Pm}} + \frac{V_{IN}}{L_O}\left(\frac{N_S}{N_P}\right)^2 - \frac{(V_O+V_D)}{L_O}\frac{N_S}{N_P} \qquad (5.9)$$

Hence, the minimum slope (V_{IN}=280V and V_O=16.2V) of the voltage on the sensing resistor is dV_{Rs}/dt=73.27mV/µs, and the maximum slope (V_{IN}=330V and V_O=0V) is dV_{Rs}/dt=132.034mV/µs.

The values of R_1 and R_2 are determined by the linearity considerations of the divider circuit. In order to obtain a good operation of the divider, the collector current density of the bipolar transistors should in the same range for all devices. In this case the divider must provide a good accuracy for values of V_{OUT} between P_{MAX}/I_{MAX} and V_{OUT_max}, which is between 8.33V and 16.2V, respectively. For the V_{OUT} values below that, the converter operates in current limitation mode and the result of the divider is ignored. From the simulations of the divider the best linearity region is observed between 80µA and 185µA. The two reference inputs of the divider must be centrally placed in this interval, with a reference value in the middle of this range. Considering a bandgap voltage V_{BG}=1.25V and R_1=10KΩ, we obtain a reference current I_{BG}=125µA.

As the maximum input voltage of the V-I converter is 1.35V, the scaling factor K_1 results as: $K_1 = {V_{OUT\_max}}/{1.35V} \rightarrow K_1 = 1/12$. In consequence we obtain R_2=7666.66 and the interval for I'_{Vout} is from 90.5µA to 176µA.

In figure 5.17, the output signal of the divider can be expressed as:

$$I_{REF} = \frac{V_{BG}^2}{K_1 V_O}\frac{R_2}{R_1^2} \qquad (5.10)$$

Comparing the coefficients of this equation with its equivalent from figure 5.1, results in:

$$K\frac{P_{Ref}}{V_O} = \frac{V_{BG}^2}{K_1 V_O}\frac{R_2}{R_1^2} \tag{5.11}$$

Where *K* is the scaling factor between the system level and circuit level block diagram:

$$K = \frac{1}{K_1}\frac{R_2}{R_1^2}\frac{V_{BG}^2}{P_{Ref}} \tag{5.12}$$

The scaling factor *K* is used directly to determine the value of R_3 by comparing the equations of I_{Rs} from figures 5.1 and 5.17:

$$I_P\frac{R_S}{R_3} = KI_P\frac{N_P}{N_S} \tag{5.13}$$

$$R_3 = \frac{R_S}{K}\frac{N_P}{N_S} \;\rightarrow\; R_3 = 6211\Omega \tag{5.14}$$

Magnetization current

As the scaled input voltage (K_2V_{IN}) is only used at the input of the integrators, the value of the scaling factor K_2 should result in a small input current for the integrators, and also a good signal to noise ratio. As a consequence we have selected the value of K_2=1/471, which results in a maximum scaled voltage K_2V_{IN}=700mV, for V_{IN}=330V. The equation of the magnetization current in figure 5.1 is (system level):

$$I_{Mag} = K\frac{N_P}{N_S}\frac{1}{2L_M}\int_0^{Ton} V_{IN}dt \tag{5.15}$$

Its circuit equivalent from figure 5.17:

$$I_{Mag} = K_2K_3K_4\frac{1}{R_4R_6C_1}\int_0^{Ton} V_{IN}dt \tag{5.16}$$

From the equation above, results:

$$K_3K_4\frac{1}{R_4R_6C_1} = \frac{K}{K_2}\frac{N_P}{N_S}\frac{1}{2L_M} \tag{5.17}$$

Due to the layout constraints for accurate scaling in practical current mirrors, the value of K_3 has to be made: K_3=2/5. The product R_6C_1 is limited in value by the input range of V-I circuit. Hence we must determine the voltage at the output of the integrator as a function of maximum ON time. For a resettable integrator we can define the peak voltage as:

$$V_{C\_max} = \frac{1}{C}\int_0^{Tmax} i\,dt \tag{5.18}$$

In our case the current can be approximated as constant, thus equation 5.18 becomes:

$$V_{C1\_max} = \frac{I_{C1}}{C_1}T_{ON\_max} \tag{5.19}$$

The duration of the ON cycle is limited by the maximum flux density swing, ΔB_{MAX}:

$$T_{ON\_max} = \frac{\Delta B_{MAX} N_P A_e}{V_{IN}} \quad (5.20)$$

As a consequence, based on equations (5.18), (5.19) and (5.20) the maximum integrator voltage for constant $V_{IN}$is:

$$V_{C1\_max} = \frac{K_2 K_3}{C_1 R_6} \Delta B_{MAX} N_P A_e \quad (5.21)$$

Further, the minimum value of the R_6C_1 product is:

$$(R_6 C_1)_{min} = \frac{K_2 K_3}{V_{C1\_max}} \Delta B_{MAX} N_P A_e \quad (5.22)$$

For ΔB_{MAX}=200mT, N_P=28, A_e=1.25*10^{-4}, V_{C1_max}=1.35V and imposing R_6=50KΩ we obtain C_1=8.5pF. Based on these values and the equation (5.16) we can obtain the ratio R_4/K_4:

$$\frac{R_4}{K_4} = \frac{2K_2 K_3}{K} \frac{N_S}{N_P} \frac{L_M}{R_6 C_1} \quad (5.23)$$

Thus for K_4=1/4 we obtain R_4=29787Ω.

Comparator *Comp3* from figure 5.1 and 5.17 has the purpose of limiting the duration of the ON cycle, and the value of R_5 will have to be chosen to set this limit. The equation of the signal from the positive input of Comp3 is:

$$V_{Mag} = K_2 K_3 V_{IN} \frac{R_5 \Delta t}{R_4 R_6 C_1} \quad (5.24)$$

As the threshold of the comparator is set to the bandgap voltage (V_{BG}), this value must be reached by V_{Mag} for $\Delta t = T_{ON\_max}$ (described in equation 5.20):

$$V_{BG} = K_2 K_3 \frac{R_5}{R_4 R_6 C_1} \Delta B_{MAX} N_P A_e \quad (5.25)$$

$$R_5 = \frac{V_{BG} R_4 R_6 C_1}{K_2 K_3 \Delta B_{MAX} N_P A_e} \quad (5.26)$$

For the values presented above, we obtain R_5=26876Ω.

Off time estimation block

A new scaling parameter, K' will be introduced in the following instead of K, in order to obtain integer ratios for the current mirrors. The equation of signal I_A from figure 5.17 is:

$$I_A = \frac{K_2 K_6}{R_6} V_{IN} - \left(\frac{K_1 K_8}{R_8} V_O + \frac{K_9 K_{10}}{R_9} V_{BG} \right) \quad (5.27)$$

Identifying this equation with its equivalent from Figure 5.1, results

$$\frac{K_2 K_6}{R_6} V_{IN} - \left(\frac{K_1 K_8}{R_8} V_O + \frac{K_9 K_{10}}{R_9} V_{BG} \right) = K' \left[\frac{N_S}{N_P} V_{IN} - (V_O + V_D) \right] \quad (5.28)$$

Hence the formula for K' becomes:

$$K' = \frac{K_2 K_6}{R_6} \frac{N_P}{N_S} \tag{5.29}$$

The value of K_2 is set based on the size of capacitor C_2 and the input range of the V-I circuit. As mentioned above, the value of K_2 is aimed to be a ratio of two integer numbers for best scaling. After successive iterations for the values of K_6, C_2, K_8 and R_7, we have imposed K_6=2. The value of the ratio R_8/K_8 is obtained by identifying the coefficients of the variable V_{OUT} from equation 5.28:

$$\frac{R_8}{K_8} = \frac{K_1}{K'} \tag{5.30}$$

Hence for K_8=1/4, and R_8=17522Ω.

The signal corresponding to the output Schottky diode voltage drop is considerably smaller than the one generated by the V-I with R1 from the top of the diagram, and therefore a separate V-I and scaling block will be required for generating this reference. Identifying the coefficients for the variables V_D and V_{BG} from equation 5.28 results in:

$$\frac{K_9 K_{10}}{R_9} V_{BG} = K' V_D \tag{5.31}$$

Considering the expression of K' from equation 5.30 results:

$$K_9 K_{10} = K_1 K_8 \frac{V_D}{V_{BG}} \frac{R_9}{R_8} \tag{5.32}$$

For a forward voltage drop on the diode V_D≈0.6V (measured in the breadboard circuit I_O=16.5÷30A) and by setting the value of R_9 to 50KΩ, we obtain K_9K_{10}=1/32.4. As the scaling factor K_{10} is implemented at the circuit level by a current mirror and K_9 by a resistive divider, it is preferred to have an integer ratio for K_{10}. Hence the following values have been selected: K_9=1/4.67 and K_{10}=1/6.

The value of the capacitor of the integrator in the *OFF time* block has to be chosen once again considering the input range of the V-I circuit. Thus, during the *ON time* the maximum voltage from the output of the integrator is:

$$V_{C2\_peak\_ON} = \frac{K'}{C_2} \int_0^{Ton} \frac{N_S}{N_P} V_{IN} - (V_O + V_D) dt \tag{5.33}$$

Based on equation 3.22, we can express V_{C2} as a function of $\Delta I_O L_O$:

$$V_{C2\_peak\_ON} = \frac{K'}{C_2} \Delta I_O L_O \tag{5.34}$$

During the *OFF time* the peak value on the capacitor is:

$$V_{C2\_peak\_OFF} = \frac{K\prime}{C_2}\int_0^{Toff}(V_O + V_D)dt \qquad (5.35)$$

Based on equation 2.6, we obtain an equation similar to 5.34 for the *OFF time*:

$$V_{C2\_peak\_OFF} = \frac{K\prime}{C_2}\Delta I_O L_O \qquad (5.36)$$

As expected, the peak voltage of the integrator is equal for the ON and OFF cycles, corresponding to the integration in the current domain of the output inductor with a positive or negative slope, respectively. Thus for a peak value of 1.35V and $\Delta I_O L_O$=15*10^{-6}, the minimum size of C_2 is 11.8pF. A value of C_2=12pF has been selected in practice.

Resistor R_7 provides the scaling of the signal from the output of the integrator in order to match the reference from the subsequent subtraction operation. Based on equation 3.32 and Figure 5.1, the expression of the error signal at the system level is:

$$err = \Delta I_O L_O - \int_0^{Ton} V_{in}\frac{N_S}{N_P} - (V_o + V_D)dt \qquad (5.37)$$

At the circuit level the reference is provided by the output of the V-I (R1), derived from the bandgap voltage reference:

$$I_{err} = \frac{V_{BG}}{R_1} - \frac{1}{R_7 C_2}\int_0^{Ton}\left[\frac{K_2K_6}{R_6}V_{IN} - \left(\frac{K_1K_8}{R_8}V_O + \frac{K_9K_{10}}{R_9}V_{BG}\right)\right]dt \qquad (5.38)$$

Identifying the coefficients in the two equations above, results in:

$$R_7 = K_1K_8\frac{R_1}{R_8C_2}\frac{\Delta I_O L_O}{V_{BG}} \qquad (5.39)$$

For the numerical values mentioned above we get R_7=11890Ω.

5.3.2 Voltage-to-current converter

The V-I converter is one of the circuits whose accuracy will influence strongly the behaviour of the converter system. In addition to a good basic precision, it should also have a low offset, linear transfer function, low offset drift with temperature and large input voltage range. Two categories of circuits satisfy these requirements: V-I circuits using the translinear principle for bipolar transistors and the ones based on an operational amplifier or transconductor. For the system implementation using the Austria Microsystems H35 technology we used the op-amp/transconductor based circuit, due to the reduced area of the amplifier and good matching of the MOSFETS. Three types of circuits can be distinguished in this category, as depicted in Figure 5.18.

The first circuit (Figure 5.18 a) is the most popular; the bandwidth is mainly limited by the OTA, there are no significant matching limitations and it has an open-drain output which allows easy subtraction of the signals. When the output load is a current mirror, the input voltage is limited to approximately half of the supply voltage, as we will see in the following discussions. The second circuit (Figure 5.18 b) brings the benefits of a larger input range and multiple (scaled) outputs at the cost of the reduced accuracy of the current mirror required. The resistor and the high-side MOSFET combine together to form the output stage of the amplifier. Hence the value of the output current will affect the stability, gain and the bandwidth of the overall amplifier configuration. The third circuit (Figure 5.18 c) compensates for the stability and low gain drawbacks of the previous circuit by introducing a bias current, but it also requires a second current mirror and hence more random mismatch. The error caused by channel length modulation in the current mirrors of the circuits in Figure b) and c) is not considered here, as it is easy to remove with the aid of cascode transistors.

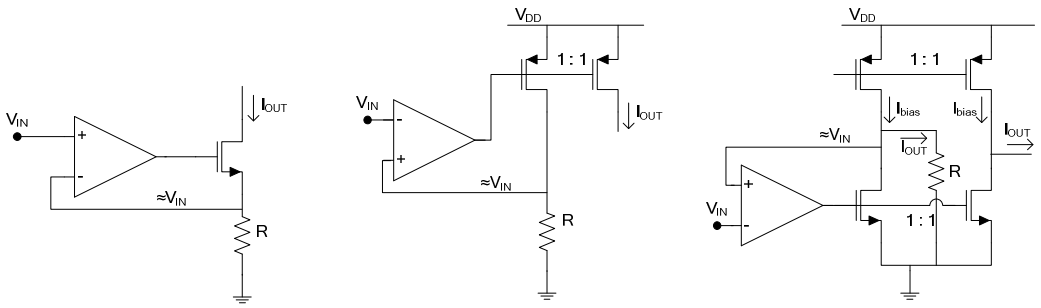


Figure 5. 18. OTA based voltage to current converters

Due to the accuracy considerations we have selected the topology from Figure 5.3 a) for the implementation of the V-I circuits. In the following discussion we give more details of the circuit and the limiting parameters. Some of the V-I circuits employed need to have multiple current outputs and therefore a current mirror is required at the output of the circuit. The complete circuit with the current mirror is presented in Figure 5.19. From the point of view of the voltage drop on the resistor, the maximum input voltage of the circuit can be expressed as:

$$V_{IN\_max} = V_{DD} - \left(V_{Tp} + V_{DSATp}\right)_{M2} - V_{DS\_M1} \qquad (5.40)$$

For good matching, the current mirrors should have a large saturation voltage (V_{DSAT}). A minimum V_{DSAT} of approximately 0.4V has been selected for the current mirrors. Also, a drain-source voltage of about 0.2V should be allowed for M_1 to be in strong inversion. Hence for V_{DD}=3.3V and V_{Tp}=0.7V the maximum input voltage of the V-I circuit is $V_{IN\_max} \approx$ 2V. On

the other hand, the input range must also be considered from the point of view of the gate potential of M_1:

$$V_{IN\_max} = V_{OTA\_max} - (V_{Tn} + V_{ov})_{M1} \quad (5.41)$$

Where V_{OTA_max} is the maximum output range of the OTA and V_{ov} is the overdrive voltage of M_1. Considering that in the target technology an isolated MOSFET can be used for M_1 , we can ignore the body effect. Therefore for V_{OTA_max}=2.9V, V_{Tn}=0.6Vand V_{ov}=0.3V we obtain the same input range, $V_{IN\_max} \approx$ 2V.

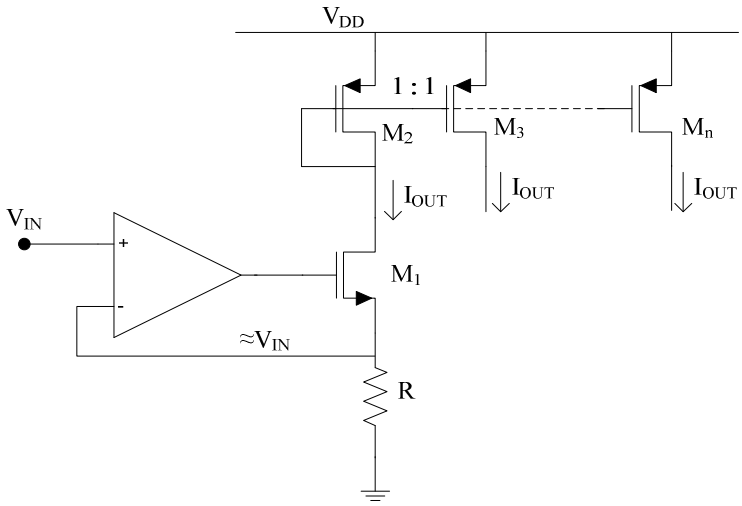


Figure 5. 19. Diagram of the V-I circuit including the output current mirror

5.3.3 Resistor and capacitor trimming

The resistor trimming is an important aspect because even though it performs a coarse operation in absolute terms, it needs to maintain a small relative mismatch between the resistors. Resistor trimming has found various applications, starting from op-amp offset trimming [57], bandgap reference trimming [58], filter tuning [59], etc. From the topology point of view, three main types of resistive trimming suitable for the above V-I circuit can be considered. Figure 5.20 presents these circuits showing 2-bit trimming for illustration. In the first circuit (Figure 5.20 a), the binary trimming has the benefit of ease of simplicity and reduced number of components. The drawback in this case is that the ON resistance of the switches adds to the main resistance. Further, for an n-bit trimming circuit we can reach the situation where the equivalent resistance is: $R_E = R_0 + nR_{SW}$; where R_{SW} is the ON resistance of each switch. As stated before, we are interested in the ratios of the resistors, rather the absolute values. In this case, the parasitic switch resistance will behave as an offset and alter the ratio between resistors. The switch resistance shows a larger temperature

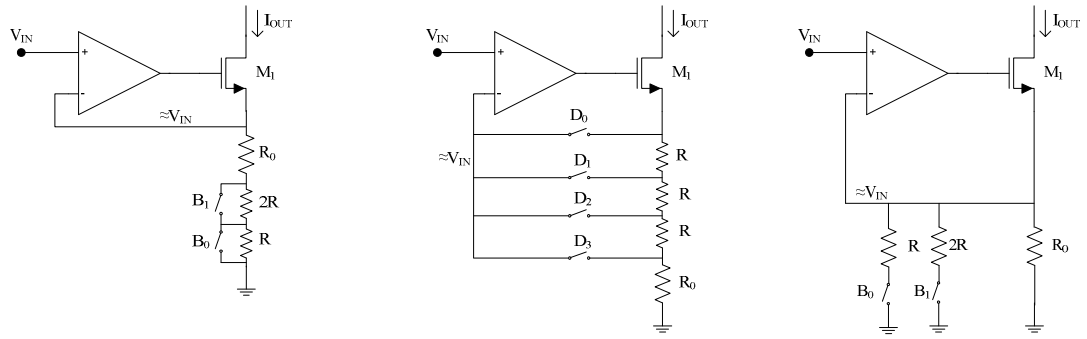
coefficient compared with polysilicon resistors, and therefore the offset due to R_{SW} will have a strong temperature dependence.

The second circuit (Figure 5.20 b) manages to overcome the drawback of the previous circuit at the price of extra circuitry and lower input voltage range. The extra circuitry comes in the form of more switches and a decoder, as in this case the control signals for the switches come in unary format rather than binary. The input range of the V-I reduces because in the worst case scenario, we will have switch D_3 turned on and the voltage at the source of M_1 is:

$$V_{S1} = V_{IN}\left[1 + (2^n - 1)\frac{R}{R_0}\right] \qquad (5.42)$$

It should also be take into consideration that the maximum potential of the source of M_1 is not a function of the number of bits used for trimming (n), but rather a function of the resistor absolute variation.

The third circuit (Figure 5.20 c) is a trade-off between the previous two. This topology uses parallel trimming and binary weighted encoding for the control of the switches. Hence the resistors R and 2R will have values larger than R_0, so that when one of the switches is closed the equivalent resistance to be equal to the nominal value. It should be noted that even though the output current passes through the switches, the switch resistance will be negligible compared with the large value of the trimming resistor. Also, all of the switches are connected to ground. In this way the switch ON resistance will not be suffer from body effect. The drawbacks of this configuration consist of the very large area required by the trimming resistors and their capacitance to the substrate.



a) **b)** **c)**

Figure 5. 20. Resistive trimming architectures

Considering features of the circuits presented above and the trimming range required, we have selected the circuit from Figure 5.20 b). In the following we derive the value of the trimming resistors and the base resistor, R and R_0 respectively.

The resistor string placed on top of the core resistor can be replaced by a more complex digital to analogue converter (DAC), if extra resolution is required (i.e. string DAC). The principle of the resistor trimming is to split the large span of the resistor value into 2^n equal intervals. First, we assign a value R_0+kR to each subinterval so that the resulting values correspond to a much smaller trimmed interval centred on the nominal value of the resistor (R_{NOM}). Where parameter k is defined as: $k \in [0; 2^n - 1]$. The principle is presented graphically in Figure 5.21. Above the axis, the span of the absolute resistor value $[R_{MIN};R_{MAX}]$ is represented along with the subintervals this range is divided into. The quantization interval is determined as:

$$q = \frac{R_{MAX} - R_{MIN}}{2^n} \tag{5.43}$$

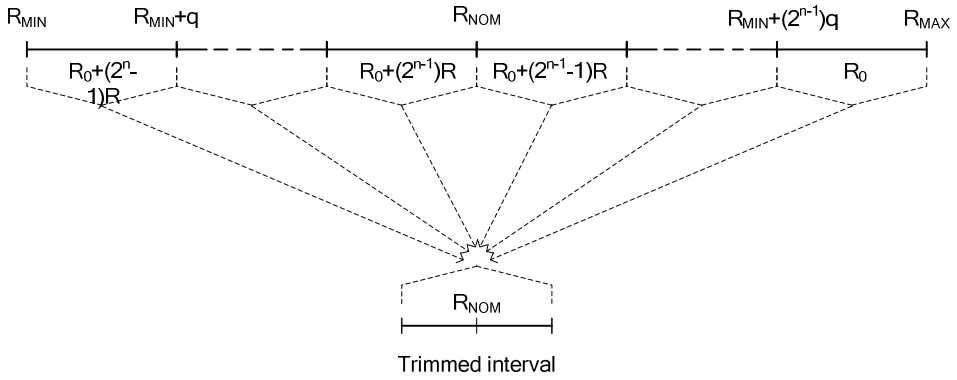


Figure 5. 21. Series resistor trimming principle

In order to determine the value of R_0 we need to look at the last interval on the right side of the segment. This segment is the most significant, as all the others must be translated into a trimmed smaller interval, centred on R_{NOM}. Hence the centre value of this subinterval ($R_{MAX} - q/2$) multiplied by the tolerance scale factor will correspond to R_{NOM}. In other words, this central value can be considered as corresponding to a resistor with a nominal value R_{NOM}, whose value has increased due to random process variation to $R_{MAX} - q/2$; this results in a multiplication factor of $\frac{R_{MAX} - q/2}{R_{NOM}}$. At the circuit level, the equivalent resistance for this interval is the base resistor R_0. Therefore if we multiply R_0 with $\frac{R_{MAX} - q/2}{R_{NOM}}$ it must be equal with R_{NOM} :

$$R_0 \frac{R_{MAX} - q/2}{R_{NOM}} = R_{NOM} \tag{5.44}$$

Where R_{MAX} / R_{NOM} is the maximum tolerance of the resistor.

As a consequence, the value of R_0 is expressed as:

$$R_0 = \frac{R_{NOM}^2}{R_{MAX} - {}^{q}/_{2}} \tag{5.45}$$

To determine the value of the incremental resistors (R) we need to look at the interval from the left side of the axis. This interval is centred around the value $R_{MIN} + q$ and has a corresponding value in the trimmed circuit of $R_0+(2^n-1)R$. Based on the principle described before the multiplication factor with regard to the nominal value of this interval is: $\frac{R_{MIN}+{}^{q}/_{2}}{R_{NOM}}$. Further we can write the equation that makes the correspondence between intervals:

$$[R_0 + (2^n - 1)R]\frac{R_{MIN}+{}^{q}/_{2}}{R_{NOM}} = R_{NOM} \tag{5.46}$$

And the equation for the value of the incremental resistor is:

$$R = \frac{\frac{R_{NOM}^2}{R_{MIN}+q/2} - R_0}{2^n - 1} \tag{5.47}$$

In the current case the polysilicon resistor has a nominal value of R_{NOM}=50Ω/□, a minimum value of R_{MIN}=40Ω/□ and a maximum value of R_{MAX}=60Ω/□. The aim of the trimming circuit is to reduce the tolerance from ±20% to approximately ±2.5%. Hence a 3 bit (8 intervals) trimming circuit is employed. In the following we are going to express all the figures normalised to R_{NOM}=50Ω. The quantization interval is q=2.5Ω, the value of the base resistor is R_0=43.478Ω and the value of the unit resistor is R=2.45Ω. In order to obtain the practical circuit values for a specific value of the resistor, R_x, the values of R_0 and R are multiplied by the ratio R_X/R_{NOM} .

The input range of the V-I circuit can be determined now, based on equation 5.33:

$$V_{IN\_MAX} = \frac{V_{S\_MAX}}{1+(2^n-1)\frac{R}{R_0}} \tag{5.48}$$

Where the highest potential in the source of M_1 (Figure 5.20 b) is V_{S_MAX}=2V, as demonstrated before. Thus the input range of the V-I circuit is limited to 1.43V. However in the design we will use the value V_{IN_MAX}=1.35V in order to preserve a safety margin.

Capacitor trimming

The trimming scheme for the capacitors is simpler as the size of the capacitors is large, input currents are small, the width of the transistors used as trimming switches is reduced and therefore only a little parasitic capacitance is added. The configuration used in this case is a parallel binary trimming. The schematic diagram for a 3-bit circuit example is shown in Figure 5.22.

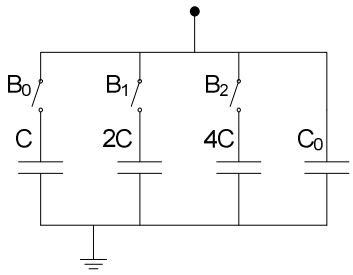


Figure 5. 22. Capacitor binary weighted trimming circuit

The equations for the value of C_0 and C are similar to the ones used for resistor trimming. For the current technology, in the case of the double polysilicon capacitor, the typical, minimum and maximum values are C_{NOM}=0.86fF/μm^2, C_{MIN}=0.78fF/μm^2 and C_{MAX}=0.96fF/μm2, respectively. In practical terms, the process variation is approximately ±10%. As we are looking for a trimmed accuracy below ±0.25%, the trimming circuit will require 6 bits, and so the values of C_0 and C are 0.7714fF/μm^2 and 2.782aF/μm^2 respectively. The practical circuit values for a specific value of a capacitor, C_X, are obtained by scaling these figures in the same manner as for the resistors.

Calibration of the on-chip resistors and capacitors is a standard procedure, extensively discussed in the literature [59],[61],[62],[63]. In this project the absolute skew of the resistors and capacitors is evaluated by manual measurement, mimicking the industrial test and calibration procedure. Reference devices (resistor and capacitor), connected to external pins have been placed within proximity (<500μm) of the critical circuit resistors and capacitors. Thus the gradient of the absolute values at die level can be neglected. The value of these components is measured manually in order to determine the deviation of the process from the nominal values. The trim codes are the calculated and loaded into the registers to compensate for the resistor and capacitor skew.

5.3.4 Continuous time current divider

The divider is required to operate only in the first quadrant, thus in the current technology it can be implemented using a circuit similar to the one presented in chapter 5.2.3. If the circuit needs to be implemented in a technology that does not include bipolar transistors, the alternative PWM mode CMOS divider described in chapter 5.3.5, can be used. The translinear divider was adapted for the AMS 0.35μm HV-CMOS technology, and a simplified method for the cancellation of the base current and biasing of collector voltages has been introduced.

As demonstrated before, the value of the output current for the circuit in figure 5.23 can be expressed as (if the emitter areas are equal):

$$I_4 = \frac{I_1 I_2}{I_3} \tag{5.49}$$

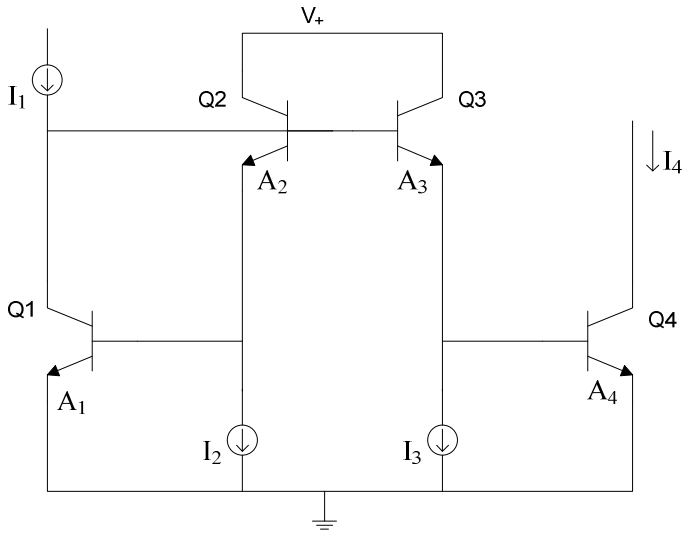


Figure 5. 23 The core of the TL multiplier/divider

Three main sources of errors have to be considered in this case: base currents, the Early effect and collector current spreading. For low β transistors the base currents cannot be neglected, thus equation 5.49 becomes:

$$I_{C4} = \frac{[I_1 - (I_{B1} + I_{B2})](I_2 - I_{B2} + I_{B1})}{(I_3 - I_{B3} + I_{B4})} \tag{5.50}$$

The base current compensation circuit is presented in Figure 5.24 a) and it works as follows: The current sources I_2 and I_3 have been moved to the high-side and replaced with two diode-connected MOSFETS, M_2 and M3, respectively. This arrangement has the benefit that under DC conditions the collector currents of Q_2 and Q_3 are always equal to I_2 and I_3, respectively. Also, all the current sources are on the high side, and thus better matching is achieved, as the signal does not have to be mirrored around the ground rail. The sizing of M_2 and M_4 must take into account the minimum possible collector-emitter ($V_{CE2\_MIN} \approx 0.4V$) voltage required for M_2 to remain saturated

$$V_{DSat\_M2} \geq V_{CE2\_min} + V_{BE1\_max} - V_{T\_M2} \tag{5.51}$$

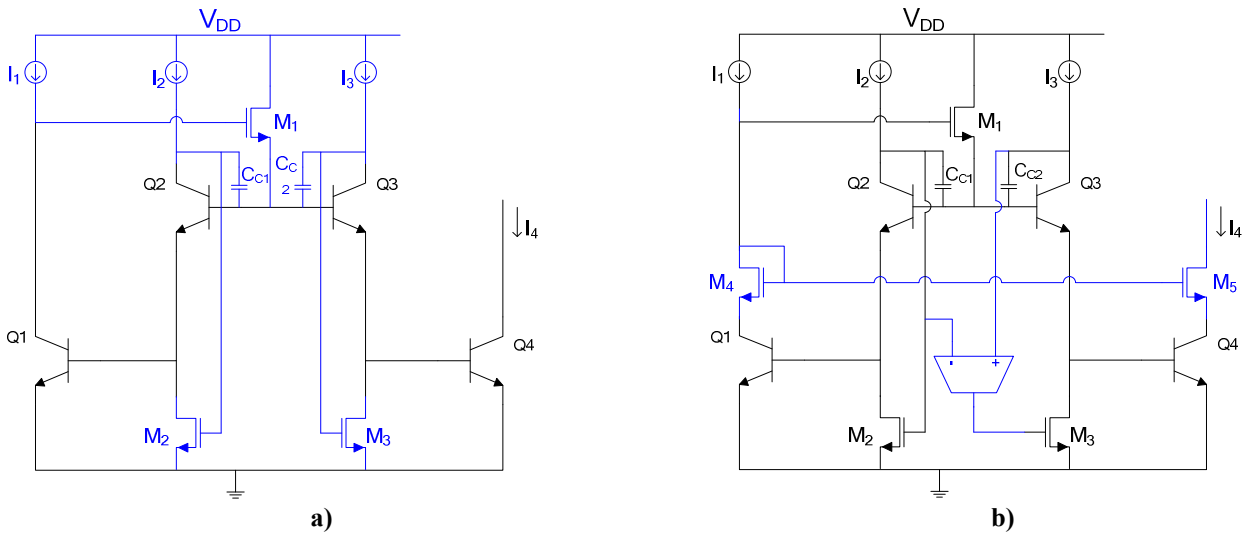


Figure 5. 24. Divider circuit: a) Base current compensation circuit; b) Early effect compensation

A small compensation capacitor, C_C is required to ensure the stability of the circuit. In order to ensure the matching between I_{C1} and I_1 we have introduced M_1 to supply the bias for the bases of Q_2 and Q_3, respectively.

The g_m of M_2 and M_3 has to be reduced in order to bias the collectors of Q_2 and Q_3 to a minimum of approximately $2V_{BE}$ (at 27° C). This low g_m value will lead to a considerable potential difference between the collectors of Q_2 and Q_3 when the collector currents are different. Hence, the error due to the Early effect in the two branches will increase. In order to avoid mismatches between the collector potentials of the two devices, we have also introduced an amplifier based loop for the gate biasing of M_3. The schematic of the modified circuit is presented in Figure 5.24 b). The transconductor driving the gate of M_3 ensures that regardless the current of I_2 and I_3, the collector potentials of Q_2 and Q_3 will be equal. For the other two branches (Q_1 and Q_4) a CMOS cascode is employed. Transistors M_4 and M_5 will have large transconductance and output resistance, such that little potential difference will result between the collector of Q_1 and Q_4.

One of the conditions required to ensure the linearity of the circuit is that transistors Q_1 to Q_4 are biased in the same current region. In order to determine the optimum operating range for the divider, the value for both I_1 and I_2 has been set to 125µA and current I_3 has been swept from 70µA to 200µA. Figure 5.25 presents the relative error and the output current. It can be observed that the error is kept to a minimum for I_3 between 90µA and 180µA, corresponding to a variation of V_{OUT} between approximately 8.33V and 16.2V (the region where the charger operates in power limitation mode).

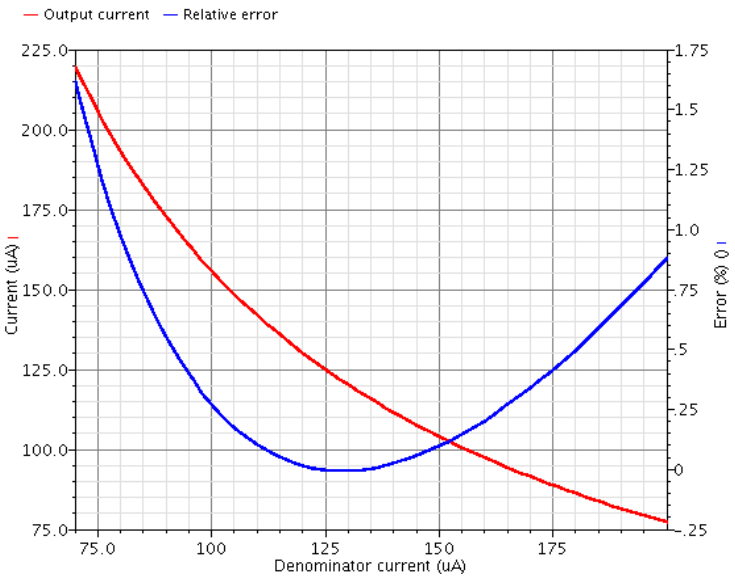


Figure 5. 25 Relative error and output current of the divider circuit

The nominal error in this region of operation is below 0.5%. The statistical simulation (for random mismatch and process variation) shows a maximum error of 1% for a 3σ interval. It should be observed that the error drops to zero when the divider branches are balanced (i.e. equal bias currents for Q_1 to Q_4).

The stability of the circuit has been analyzed by breaking the loop made of OTA, M_3 and Q_3 (Figure 5.24 b) and sweeping the value of C_{C2} until a phase margin over 65º was achieved over all corners. Figure 5.26 shows the settling of the circuit for a step of 40µA, denominator current.

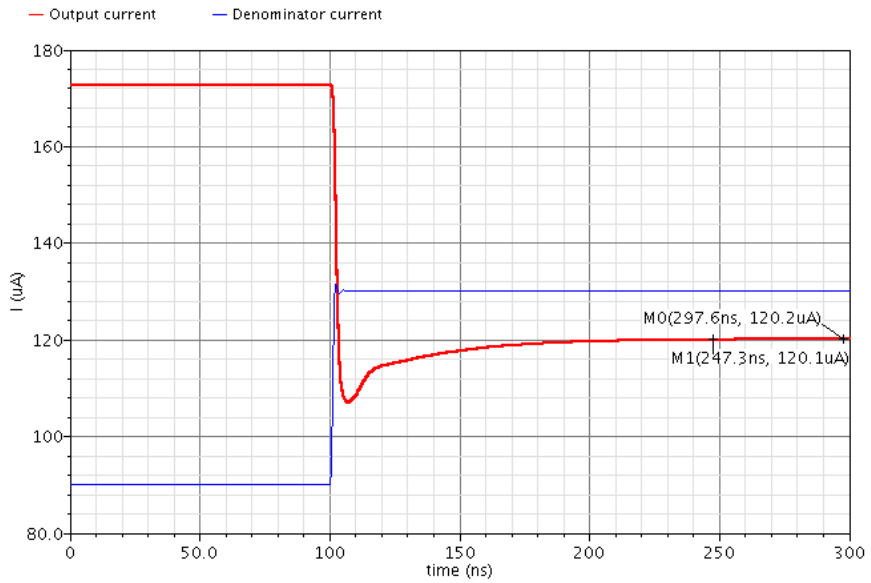


Figure 5. 26 Step response of the divider circuit

The settling time to 0.1% of the final value is 147ns, hence even if transient pulses are induced by the switching of the power MOSFETs, the circuit will settle before the minimum ON or OFF times are reached.

5.3.5 Sampled CMOS current divider

The availability of the vertical NPN transistor was made possible in this process due to the presence of the deep N-well, required for the HV MOSFETs. Hence, for the analogue system implementation, the translinear divider circuit has been used. Unfortunately, many low voltage standard CMOS processes do not include good NPN transistors and the implementation of the translinear divider is not possible. As this project is aimed as a generic solution for EDLC chargers, we have also built an alternative divider circuit that overcomes this impediment and does not require any bipolar transistors.

The operating principle of the circuit [39] is based on a current-to-time domain conversion with the aid of two resettable integrators and a comparator. The circuit is presented in Figure 5.27 and operates as follows. After the reset signal becomes inactive, the voltage on capacitor C_1 starts to increase proportionally to the current I_1:

$$V_{C1} = \int_0^t \frac{I_1}{C_1} dt \tag{5.52}$$

At moment t_1 the voltage drop on V_{C1} becomes equal with V_{T1} and switch S_1 is turned OFF. Considering that the current is constant and the voltage drop across the capacitor is zero after reset, the time required for the capacitor voltage to reach value V_{T1} is:

$$\Delta t_1 = V_{T1} {}^{C_1}/_{I_1} \tag{5.53}$$

At the same time, the integrator made from the current source I_2 and C_2 will develop an output voltage:

$$V_{C2} = \Delta t_1 {}^{I_2}/_{C_2} \tag{5.54}$$

$$V_{C2} = \frac{I_2}{I_1}\frac{C_1}{C_2} V_{T1} \tag{5.55}$$

Hence the voltage at the output of the circuit is proportional to the ratio between currents I_2 and I_1. The delay block has been introduced to create a time interval between t_1 and t_2 when the result of the division is held constant for the subsequent circuits. Also this delay ensures that there is time for a full discharge of the capacitors between time t_2 and t_3.

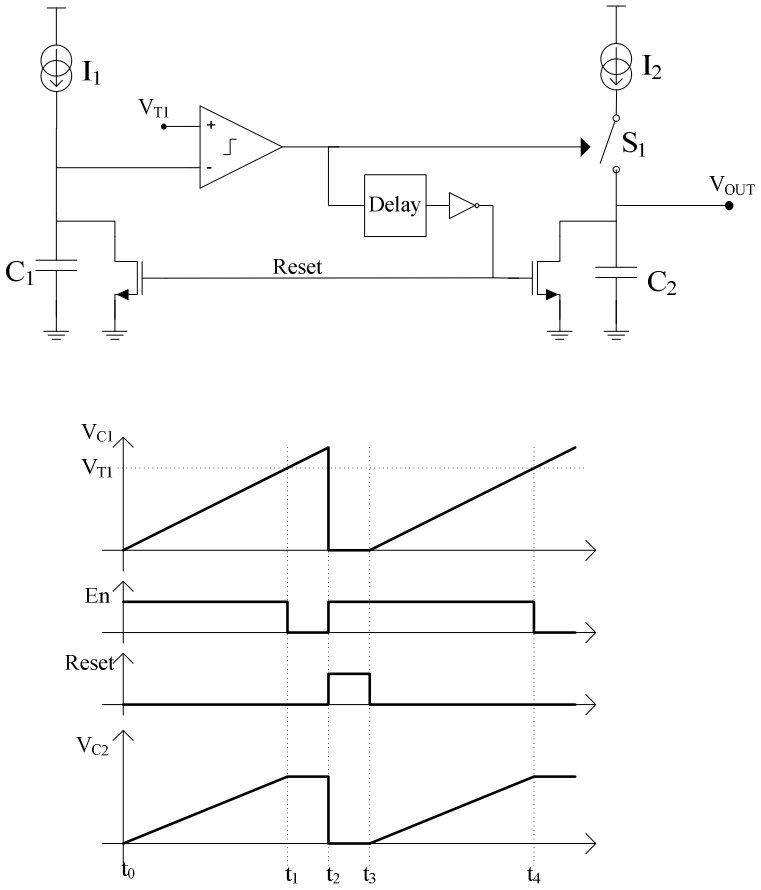


Figure 5. 27 Circuit diagram and signal waveforms of the divider

The main possible sources of errors of this circuit include: The delay and input impedance of the comparator; charge injection from switch S_1; the input impedance of the load circuit; and incomplete resetting of the capacitor charge. On the other hand, the circuit has the significant advantage of making trimming very easy through the voltage V_{T1}. Also, the sizes of the capacitors appear as a ratio in the expression of the output voltage, and hence the circuit will not be affected by the variation of the absolute value of the capacitors or parasitic capacitances.

In the current IC system architecture, the circuit has the drawback of having the result available at discrete moments of time and therefore it requires synchronisation with the rest of the circuit. As the integration time is dependent on the current I1, this might be difficult to achieve. The solution in this case could be the use of a track and hold circuit at the output or by using two multiplexed capacitors for C_2. The second option provides a better accuracy and therefore it was preferred.

Figure 5.28 presents the simulation results for the circuit with two multiplexed output capacitors (for C_2) and an auto-zero output buffer. The main source of error in this case is the charge injection of the switches and delay of the comparator. The mismatch between the

capacitors and the current mirrors can be easily cancelled by trimming. The total systematic error of the circuit is approximately 0.17%. Taking into consideration the mismatch of the components, the untrimmed circuit shows a maximum error of 0.54% (C_1=C_2=10p).

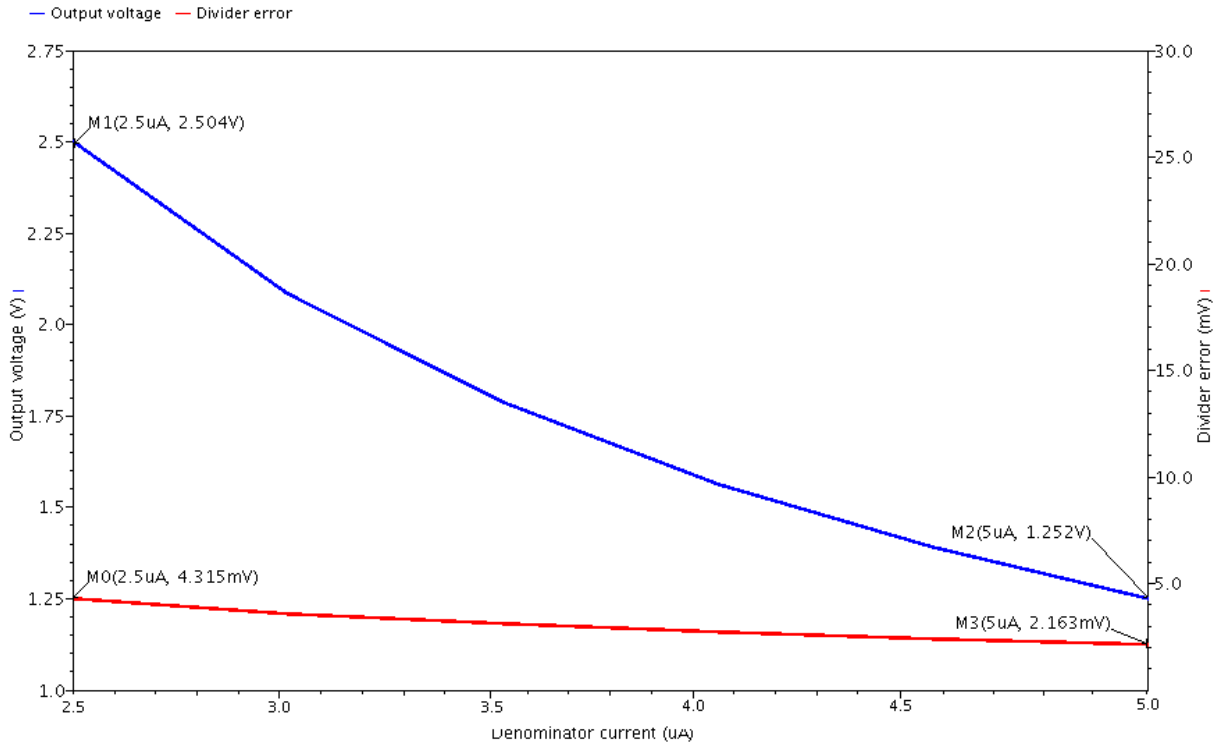


Figure 5. 28 Absolute error and output voltage of the sampled divider circuit

5.3.6 Current comparator

The current comparator is another key block of the circuitry as it determines the moments when the switches are going to be turned ON or OFF. An ideal current comparator would show very low input impedance, very small propagation delay, very short recovery time, low input offset, low input referred noise and low power consumption. One of the topologies that sits at the origin of the high speed current comparators is the one presented by Traff in 1992 [45].

The circuit, shown in figure 5.29, is based on a CMOS inverter with two source followers feeding back to the input of the circuit. When the input current is positive or negative transistors M3 or M4 are driving the input current, respectively. In this way, the circuit shows a low input impedance. When the input current drops to small values, M3 and M4 turn off and the whole circuit behave like an inverter with high input impedance. The speed of the inverter is set by the ratio $g_{m1,2}/C_{PAR}$ (where C_{PAR} is the parasitic capacitance of the output). For a good sizing of the MOSFETs, when the input current is zero the potential of the input node with respect to ground should be approximately $V_{DD}/2$. In this way, for a zero

input current, the pair M1 – M2 will show a very large g_m and therefore provide a fast decision.

As with most the high-speed circuits, the trade-off comes between the speed and the current consumption. For both positive and negative currents, the deviation of the potential of the input node from approximately $V_{DD}/2$ should be minimal, so that only a small charge is absorbed by the input for fast transients; and hence ensuring a fast response of the circuit. On the other hand, the inverter will have a large and poorly defined quiescent current if its input is biased close to half of the supply voltage.

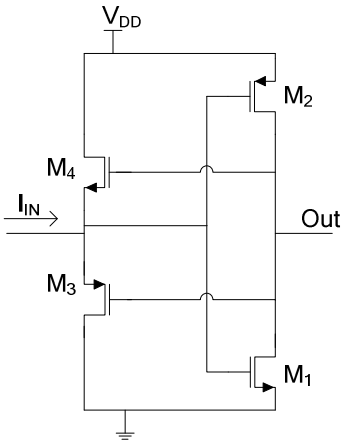


Figure 5. 29 Schematic of the Traff comparator

Figure 5.30 shows the simulation results for the comparator circuit implemented in the AMS-HV 0.35μm process, for a triangle wave input current. The first plot shows the drain current of M4 and the source current of M3. These two MOSFETs operate as complementary source followers, M4 sourcing the current for negative input signals and M3 sinking the current for positive values.

The second plot presents the voltage swing of the input node. For large input current signals the voltage variation at this node is very small, hence showing the low impedance input. When the input signal drops close to zero, the two source follower transistors (M3 and M4) are cut-off and the node goes into high impedance, producing a larger swing at the input node. This feature of the comparator ensures very small input offset, with the only source of error being the leakage currents of M3 and M4 (usually very small if correctly sized). Also, in the second plot we have the presented the supply current of the circuit. It should be noted that when the input signal approaches the zero value, the supply current of the inverter starts to increase, leading to a higher transconductance and faster decision. The third plot shows the output signal and the digital reconstructed output signal. In this design example, the

propagation delay from the zero crossing moment of the input current to the edge of the digital output is approximately 10ns.

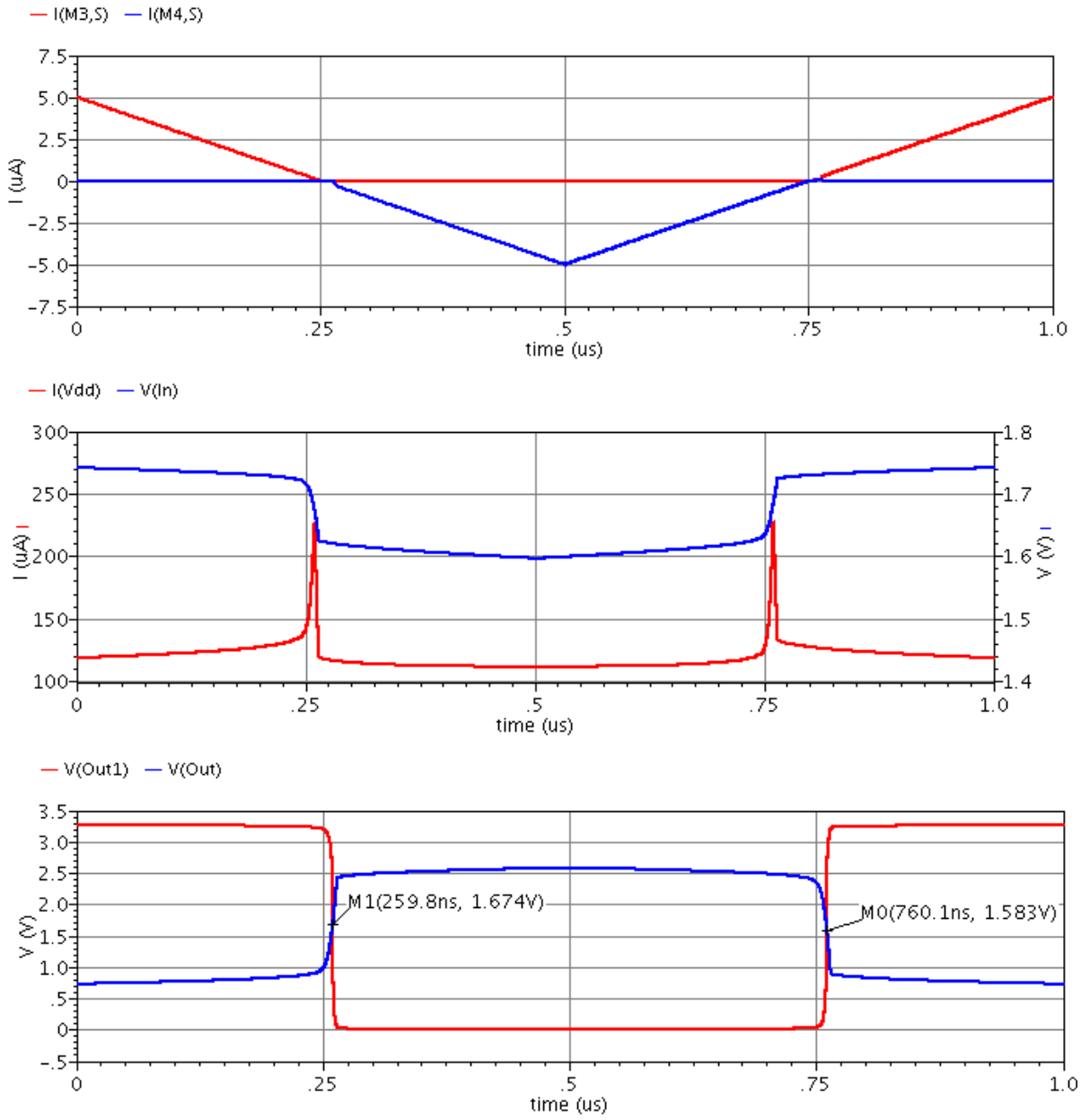


Figure 5. 30 Waveforms of the current comparator signals; first plot: I_{SD_M3} (red) and I_{SD_M4} (blue); second plot: voltage of the input node (blue), supply current (red); third plot: output signal (blue) and after one inverter (red)

As mentioned before, there is a trade-off between the current consumption and speed of the comparator. In the previous example, the quiescent current consumption of the comparator is approximately 115µA. This might not represent a problem for a circuit that has only a few of these comparators or is not intended for a device with low power consumption. Numerous applications need to continuously monitor a large number of signals and react immediately, and hence the current consumption, speed and die area all become important aspects.

Several articles have been presented that aim to reduce the power consumption or improve the response time. The circuits proposed in [46]-[49] have demonstrated higher speed at the expense of larger power consumption and the need for several inverter stages to obtain rail-to-rail outputs, adding to die area and increasing the likelihood of switching current transients on the power rails. The topology presented in [46] also requires a twin-well CMOS process (for isolated transistors) and very accurate current sources. The circuit in [48] requires a capacitor with an area comparable with that required for the transistors, as well as five extra inverters, out of which two are in the feedback loop in order to boost the gain and reduce the swing of the input. The circuit presented in [49] shows very low power consumption at the expense of a high impedance input that swings rail-to-rail. A direct consequence of this is that direct current subtraction at the input of the comparator is more difficult to achieve. Further, large excursions at this point often lead to poor recovery time when used with a transconductance input stage to provide a voltage input interface.

The circuit presented in figure 5.31 aims to reduce the inverter cross-current by introducing an extra source follower for each transistor of the previous implementation. Two additional current sources (I_{B1} and I_{B2}) are required in the circuit for biasing M3 and M4. The purpose of M9 and M10 is to ensure the biasing of M8 and M10 with a very small current and prevent transistors M5 and M6 from going into deep sub-threshold, hence speeding up the turn-on of the input source followers.

For ease of understanding we will consider the circuit starting from a steady state where the input current is positive and transistors M1, M3, M5, M7 and M10 are all turned on, with M5 sourcing the input current. On the high-side M2, M4, M6, M8 and M9 are all turned off. The equilibrium between the input and the output is determined by:

$$V_{T5} + V_{DSat5} + V_{T7} + V_2 = V_{T3} + V_{DSat3} + V_{GS1} \qquad (5.56)$$

The drain current of M7 is very small, and hence V_{DSAT7} can be neglected. It should be noted that I_{B1} should be selected in such a manner to maintain the V_{GS} of M1 close to the V_T level. The same applies for I_{B2} when M1 is off. The quiescent current / speed of the inverter can be tuned during a pre-calibration phase. In this way the circuit can improve its accuracy during critical operating cycles and reduce its current consumption during the non-critical times.

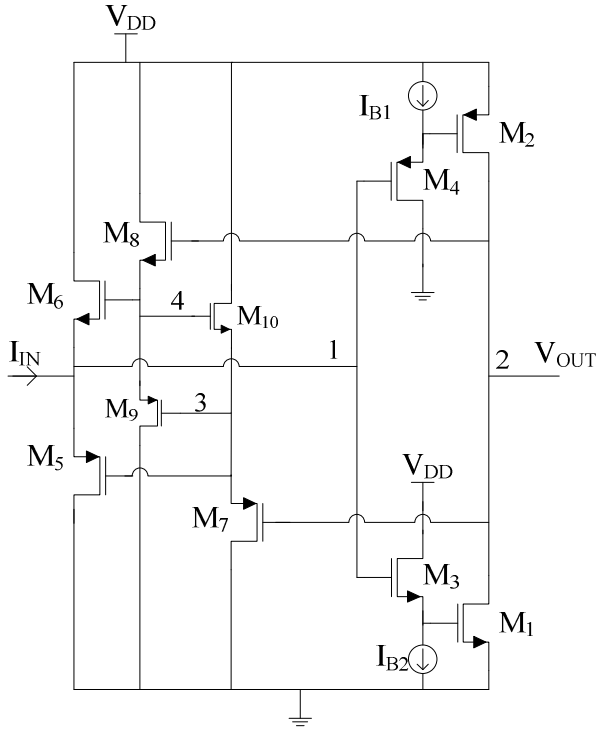


Figure 5. 31. Improved current comparator

As the input signal drops, V_{DSAT_M5} falls as well, pulling node 1 down. As the gate of M1 and M2 are biased by source followers with constant current, these nodes will follow the input node precisely. This allows transistor M2 to partially turn on and boost the combined transconductance of M1 and M2. When the input signal current drops to zero, M5 fully turns off leaving the input in a high impedance state. From this point until M6 turns on, all the input current is charging/discharging the parasitic capacitances of the input. As the output node goes up, transistor M7 also turns off, followed by the turn on of M8 and M6. If M7 and M8 would have been biased by constant current sources they would follow the swing of the output node. But the pair M9 and M10 keeps nodes M3 and M4 within a close range (approx. V_T) of each other. Even though the gate-source voltage of M7 and M8 is taking a large voltage when these devices are on, M9 and M10 are blocking any DC current through these devices. Figure 5.32 shows the main waveforms of the optimised circuit for a signal current with small amplitude. The sizes of the transistors used were the same for M_1, M_2, M_5 and M_6. The propagation delay for the new circuit is approximately 5-6ns, while the Traff circuit requires 10ns in the same technology for the same input current swing. Maximum current consumption is significantly reduced in the new circuit, approximately 25µA compared with 115µA for the Traff circuit for the same test conditions. For variations of the supply voltage of ±10% the current increases by up to 6µA and the propagation delay variation is up to 1ns.

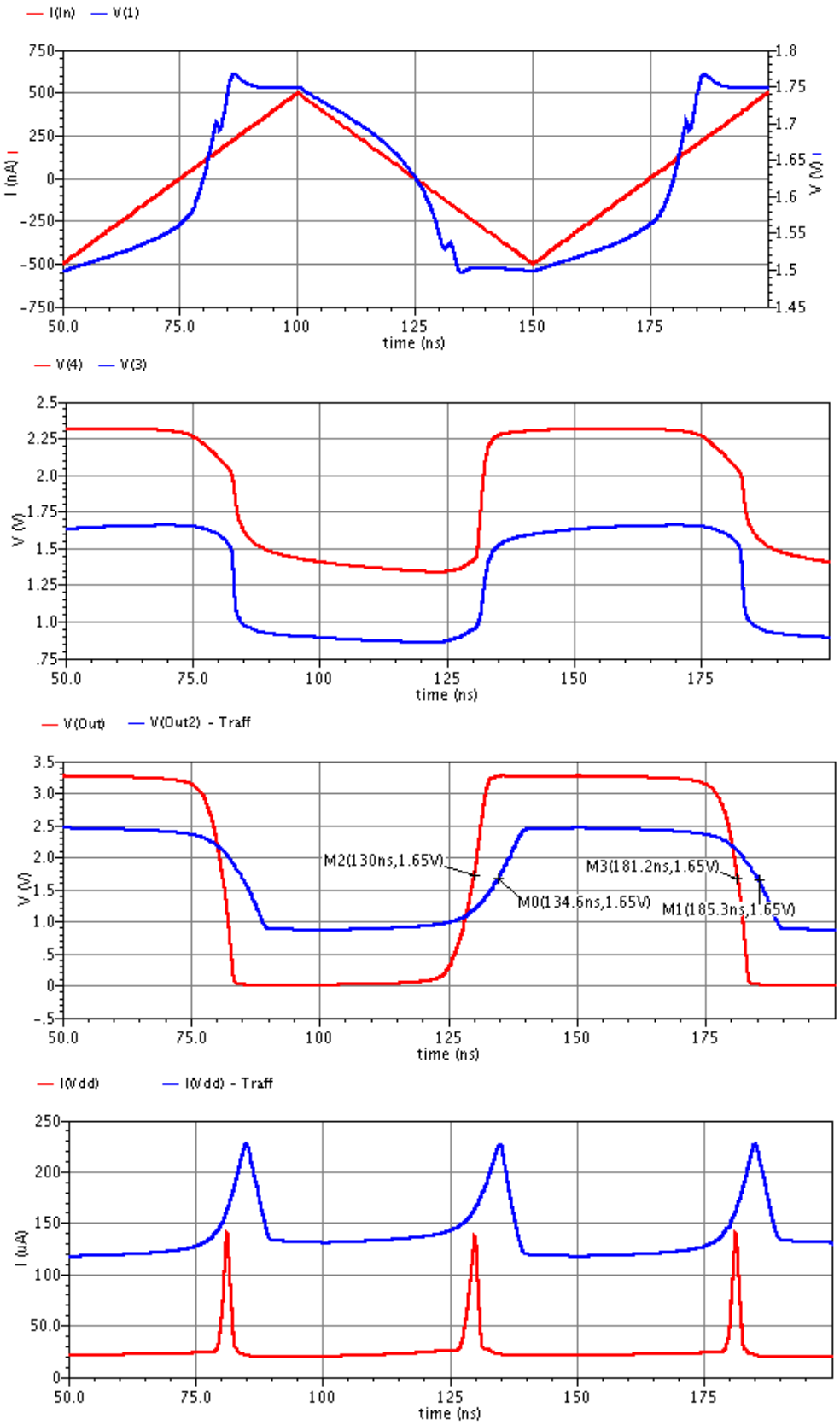


Figure 5. 32 Improved comparator simulation waveforms; First plot: input current (red), input node voltage (blue); Second plot: potential of nodes 3 (blue) and 4 (red); Third plot: output signal, new comparator (red) and Traff circuit (blue); Fourth Plot: current consumption, new comparator (red) and Traff circuit (blue)

5.3.7 OFF-time regulation – current sampling loop

As mentioned before, the accuracy of the OFF time estimation block is critical for good regulation of the output current ripple. For this analogue implementation the main sources of errors originate from the summing nodes, the integrator functions and from sampling noise. In order to improve the accuracy of the circuit, it has been an aim to reduce the number of summing nodes to a minimum. Figure 5.29 shows the OFF time estimation block with the current sampling loop highlighted by an orange background.

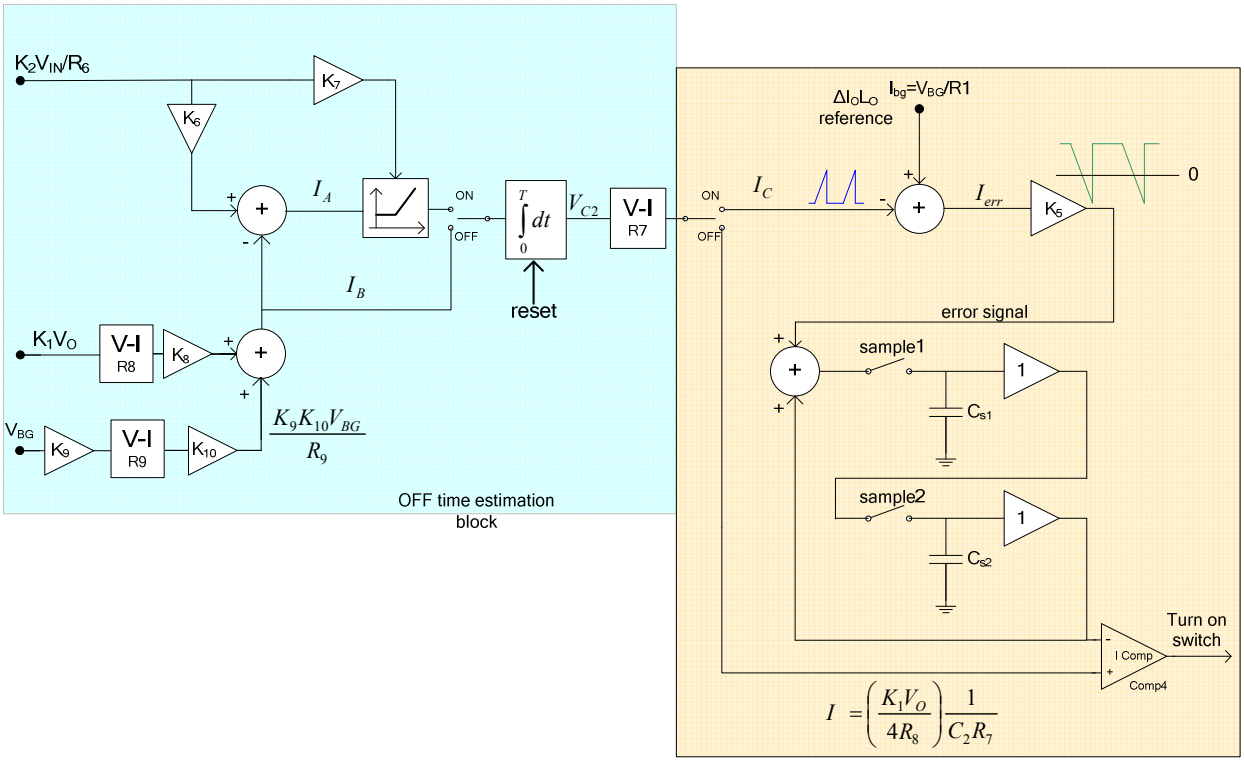


Figure 5. 33 Current sampling loop (orange background) – block diagram

A careful look at the sampling loop shows that it can be split in two parts: the summing/scaling circuitry and a comparator on one side, and the two current sampling blocks on the other. Hence, all the current summing and scaling circuitry has been combined at a single node that is connected to the output of the integrator, the input of the current sampler and the input of the current comparator. In this way, the number of stages and the sources of errors are reduced significantly. The circuit implementation of the loop is depicted in figure 5.34. The current comparator is implemented using the topology presented before; hence it has only one input signal in the form of the difference between value of the previously sampled current and the integrator output.

The lumped summing node, found on the left-hand-side of the diagram, has a dual function: during the ON phase it generates the error signal for the new time-base signal (the

difference between the reference current and the integrator output signal); while during the OFF phase it generates the input signal for the comparator (the difference between old time-base and the integrator output signal).

The scaling operation (K_5) is not achieved in a direct form with the aid of a current mirror because the error signal is bipolar and a simple current mirror could not supply negative currents. This could be overcome by adding a DC current bias that is subtracted afterwards, but it would represent an extra source of error and it would also limit the negative swing of the error. As a consequence, in order to achieve a scaling factor of $1/K_5$ we have multiplied the old time-base current and the sampling load by K_5. Hence the new time-base will be:

$$I_{NEW\_TB} = \frac{K \times I_{OLD\_TB} + I_{ERROR}}{K} \qquad (5.56)$$

This operation is achieved with the aid of current mirror M4 – M6, and the two matched diode-connected sampling transistors M1 and M3. For the current implementation, a scaling factor of five has been chosen for stability reasons. Hence the aspect ratio between M4 – M6 and M1 – M3 is 1 : 5 and 1 : 4, respectively.

The first sampling block made from M1 and C1 stores the value of the new time-base at the end of the ON phase, and then during the OFF phase it feeds it into the second sampling block (M2 and C2). This current is then fed back to the input with the aid of mirror M4 – M5.

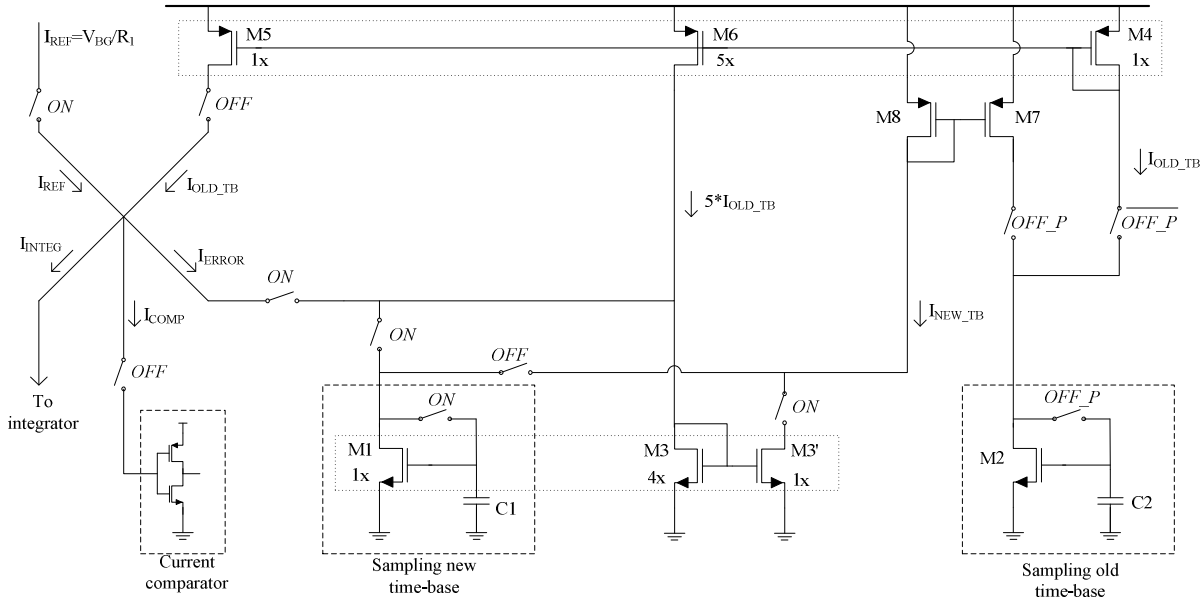


Figure 5. 34 Current sampling loop – schematic diagram

One other option for the second current sampling cell is to implement it on the supply rail, using PMOS transistors (instead of the pair M7 – M8). This case would have required

very good regulation of the supply rail and low coupling of the transistor gate and capacitor plates to ground. Considering the high switching noise in the system the first structure has been used.

The waveforms for the main figures of the simplified current sampling loop are presented in figure 5.31. During the ON phase (t_1 to t_2 and t_4 to t_5) the output of the lumped summing node (error signal) is scaled and added to the previous time-base, generating the new time-base. At the end of the ON cycle (determined by the ON time monitoring block) the value of the new time-base is sampled using the first current sampling cell (M1 and C1). During the OFF phase the output of the summing node is fed to the current comparator. At the moment when the difference between the old time-base and the integrator signal drops to zero the comparator generates a pulse that activates the ON phase.

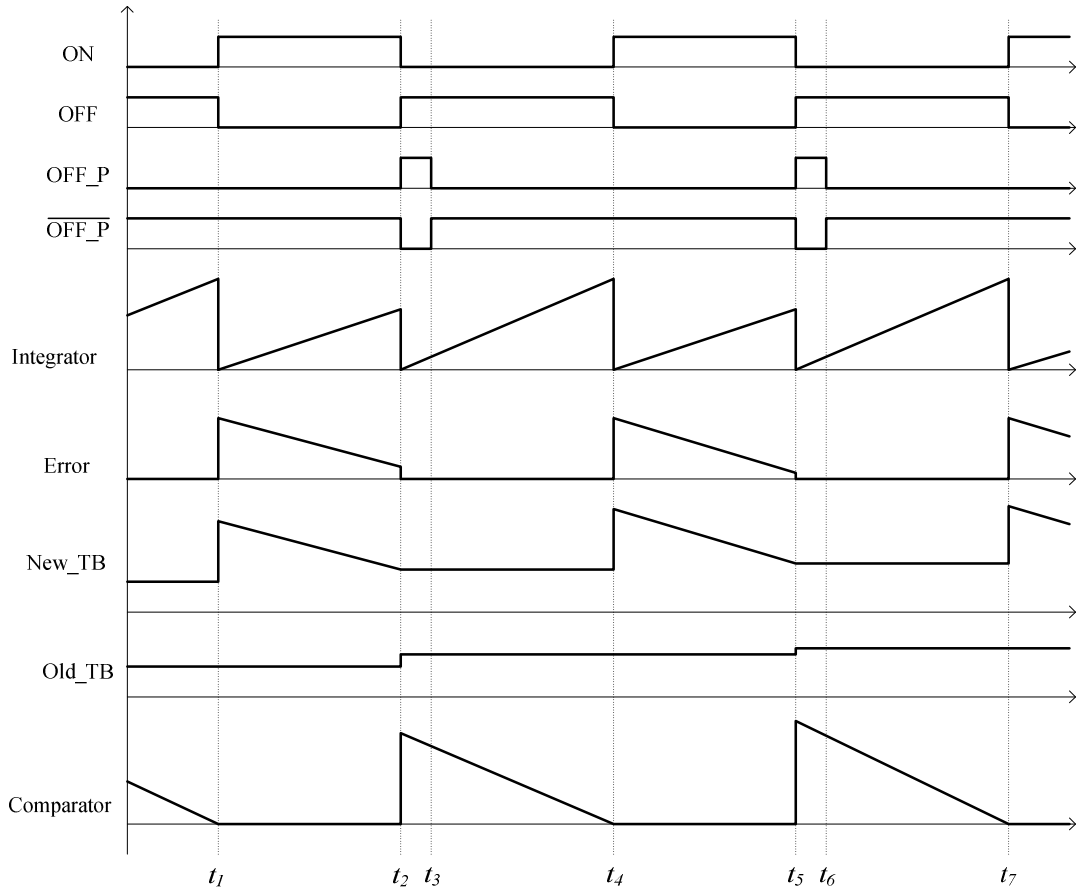


Figure 5. 35. Waveforms of the signals for the current sampling loop

The sampling of the time-base in the second memory cell (M2 and C2) is done in a short time interval (*OFF_P*) at the beginning of the OFF phase. This interval is set slightly shorter than the minimum OFF time to allow the settling of the comparator input signal. The reason that this interval has to be shorter than the minimum OFF time is because the updated value of the current memory will determine the duration of the OFF cycle. As this time

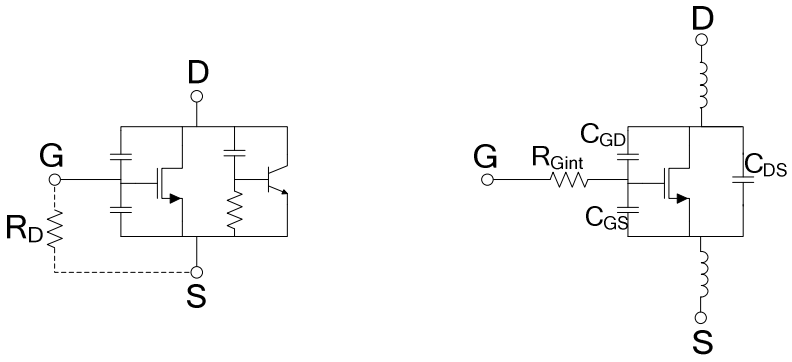
interval is below approximately 200ns, a fast settling of the signal is required in the second current memory. Hence a pre-charging current source (M3') is added (during the ON-phase) for the current mirror M7 – M8. In this way, regardless of how large the gate area of the pair M7 - M8 is (and large devices are required for good matching), the gate potential of the current mirror will be approximately constant. As a consequence, the settling time is only dependent of the second current memory time constant.

5.3.8 Power MOSFETs driver

Even though the actuation of the power MOSFETs might seem a trivial aspect, a closer look will reveal a series of tradeoffs that will determine the performance of the system. The starting point for the design of any driver is the characterisation of the load impedance. In our case it is a large field effect transistor with an inductive load.

Two models of the power MOSFET must be taken into consideration when designing the driver. The first one (Figure 5.36 a) is useful mainly from the perspective of the dv/dt induced breakdown characteristic. Due to the abrupt rising edge of the drain voltage, the parasitic bipolar transistor (present in power MOSFETS) can turn on, leading to oscillations in the drain potential. The second aspect comes from the HF output impedance of the driver. Again, when the transistor is turned OFF and the drain potential increases (due to the activation of the other switch), the charge fed through the Miller capacitance can raise the gate potential if the high frequency output resistance of the driver and associated tracks is not lower than the impedance of the gate capacitance. The track impedance will increase with frequency due to the skin effect and possible track (including on/off chip tracks) parasitic inductance. On the other hand, the impedance of the power MOS gate-source capacitance will drop at higher frequencies. In the current case, the dV_{DS}/dt is limited by a snubber circuit, therefore contributing to the stability of the switches.

Figure 5.36 b) presents the switching model of the power MOSFET. The gate-source capacitor is mainly caused by the gate electrode overlapping with the source diffusion and channel region. The gate-drain capacitance, also referred as Miller capacitance, is the result of the overlap between the gate and drain drift region. Even though it is a small capacitance, its value is multiplied by the voltage gain of the switch, due to the Miller effect. As a consequence, C_{GD} is the main factor limiting the switching speed of the MOSFET. Another important parasitic factor is the gate mesh resistance. This includes the parasitic resistance associated with the distribution of the gate signal from the pad to the gate (i.e. bondwire, metal tracks, polysilicon, etc.).



a) b)

Figure 5. 36 Parasitic model of the MOSFET;
a) dv/dt model, b) switching model

SWITCHING PROCEDURE

The switching procedure will be analysed for the MOSFET without source resistance and with a clamped inductive load. The test circuit is presented in figure 5.37. The drain and source inductance have been omitted in this circuit as the following analysis is aimed at low and medium frequencies, and these components affect only the HF behaviour of the circuit. The driver supply is V_{DD} while the supply voltage of the switch is V_{HV} (the rectified mains voltage in our case). The internal resistance of the driver is symbolised by R_{dr} (assumed constant for the moment). The driver is connected to the power switch through a discrete resistor R_{Gext}, to limit the driver current.

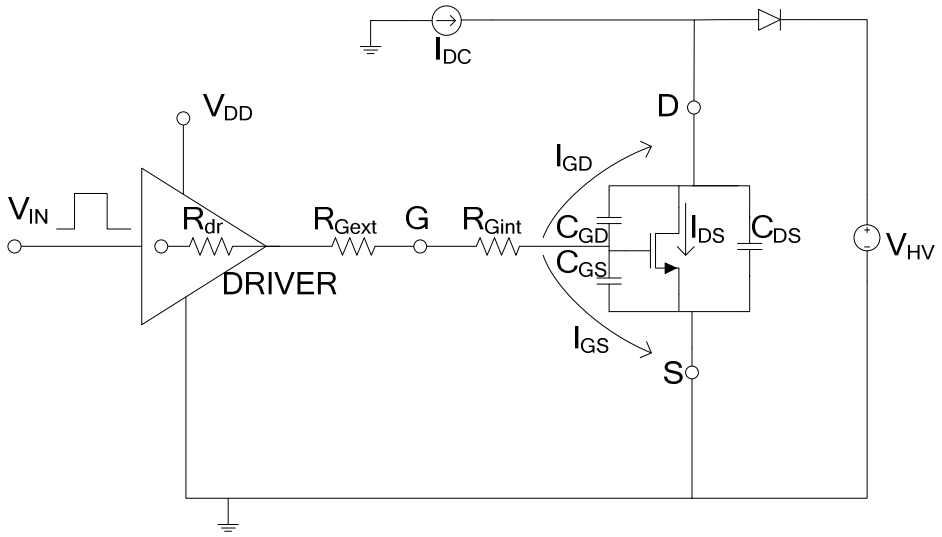


Figure 5. 37. Power MOSFET switching circuit

TURN-ON PROCEDURE

The turn-on procedure is explained with the aid of the schematic and waveforms from figure 5.38 a) and b). Four different intervals can be identified during the turn-on sequence of the power MOSFET. The step signal is applied at the input of the driver at the moment t_0. Ignoring the propagation delay of the driver, the gate voltage increases exponentially with a time constant $T1=(R_{DR}+R_{Gext}+R_{Gint})\times(C_{GS}+C_{GD})$. Until the moment t_2 when the gate voltage reaches the threshold voltage of the power MOSFET, the drain potential and current remain constant. As V_{GS} increases above V_T the drain current starts to increase, but the drain voltage is initially approximately constant, and hence the transistor enters the saturation region. At the moment t_3, the drain current reaches the value of the inductor current (symbolised here by I_{DC}) and the MOSFET starts to pull down its drain potential. Between the instants t_3 and t_4, the gate voltage stays nearly constant, with all the gate current being fed into C_{GD} until V_{DS} drops to the minimum value. This interval is called the Miller plateau as V_{GS} remains constant. Once V_{DS} has decayed and the Miller capacitance has been charged, the gate voltage starts to increase, following a simple exponential charging profile with a time constant similar to T1. The difference in this case is that the drain N-drift region has expanded due to the fall of the drain potential and C_{GD} has increased significantly, resulting in a longer time constant [50]-[55].

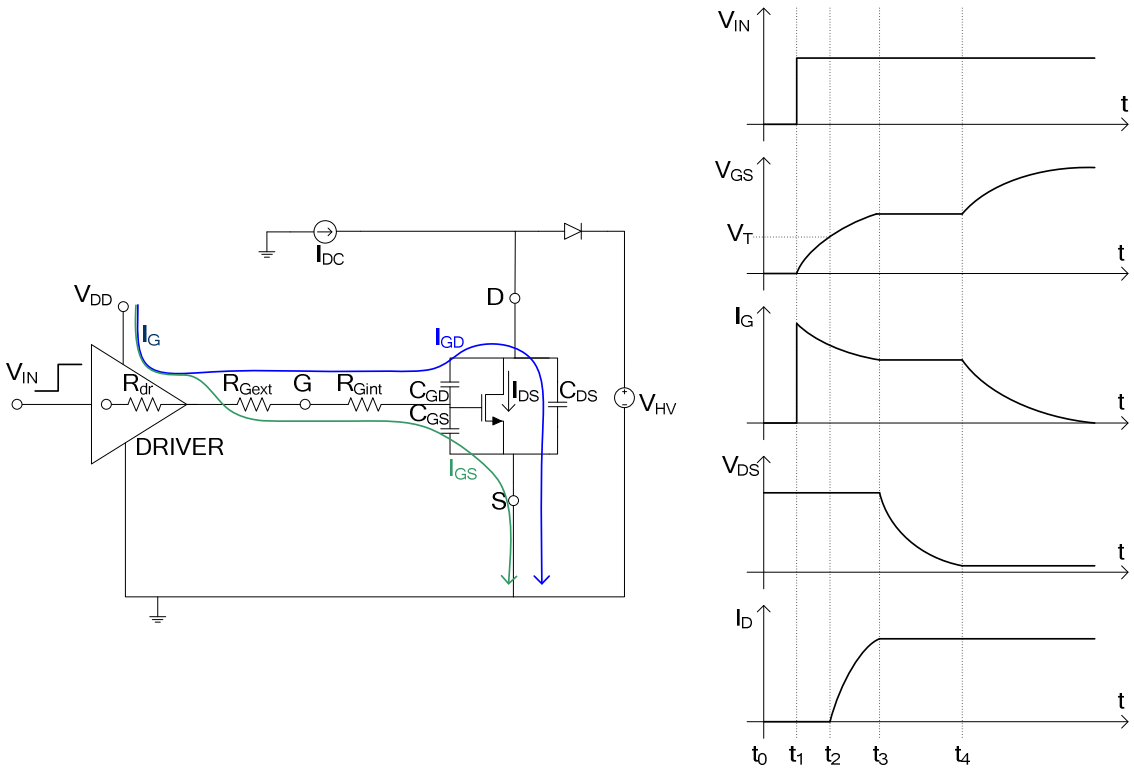


Figure 5. 38. Power MOSFET turn-on procedure;
a) circuit schematic and gate currents; b) main signals variation

The value of the Miller plateau is specified in the datasheet of the transistor and can be approximated using the device transconductance:

$$g_{fs} = {}^{dI_D}/_{dV_{GS}} \tag{5.57}$$

As a consequence, the maximum current of the transistor operating in saturation is:

$$I_D = \left(V_{GS\_Miller} - V_T\right) \times g_{fs} \tag{5.58}$$

The approximate value of the Miller plateau is thus:

$$V_{GS\_Miller} \cong V_T + {}^{I_D}/_{g_{fs}} \tag{5.59}$$

It should be also observed that from the power dissipation point of view that the most critical region during transistor turn-on is between t_2 and t_4, when it operates in saturation.

TURN-OFF PROCEDURE

The turn-off process is described with the aid of figure 5.39 a) and b). It can be considered a mirrored version of the turn-on procedure, and hence if the driver output resistance is the same as for turn-on it should return similar time constants. At the instant t_1, the input signal of the driver goes low. At the same moment, the gate current ramps up to the maximum value $I_{dr\_max}=V_{dr\_max}/(R_{dr}+R_{Gext}+R_{Gint})$, where V_{dr_max} is the maximum achievable output swing of the driver. Between t_1 and t_2 the gate voltage will fall exponentially with a time constant equal to T1, as in the turn-on sequence. It should be noted that C_{DG} has a large value during this interval due to the low V_{DS}. The variation of V_{DS} is minor in this region as the transistor is still operating in triode region. At the instant t_2, the transistor enters the saturation region and the drain potential begins to rise steeply. During this interval the gate voltage remains essentially constant (following the Miller plateau again), with the entire gate current flowing in the drain-gate capacitance. The drain current stays approximately constant up to the moment t_3, when V_{DS} reaches the maximum value. Between t_3 and t_4 the drain current fully turns off. The gate voltage also falls exponentially from the Miller plateau value to V_T. The time constant expression is as before, but in this case the numerical value is less as C_{DG} is smaller due to the large V_{DS}. After the moment t_4 , the transistor can be considered turned off and V_{GS} keeps falling until the gate capacitance is fully discharge [50]-[55].

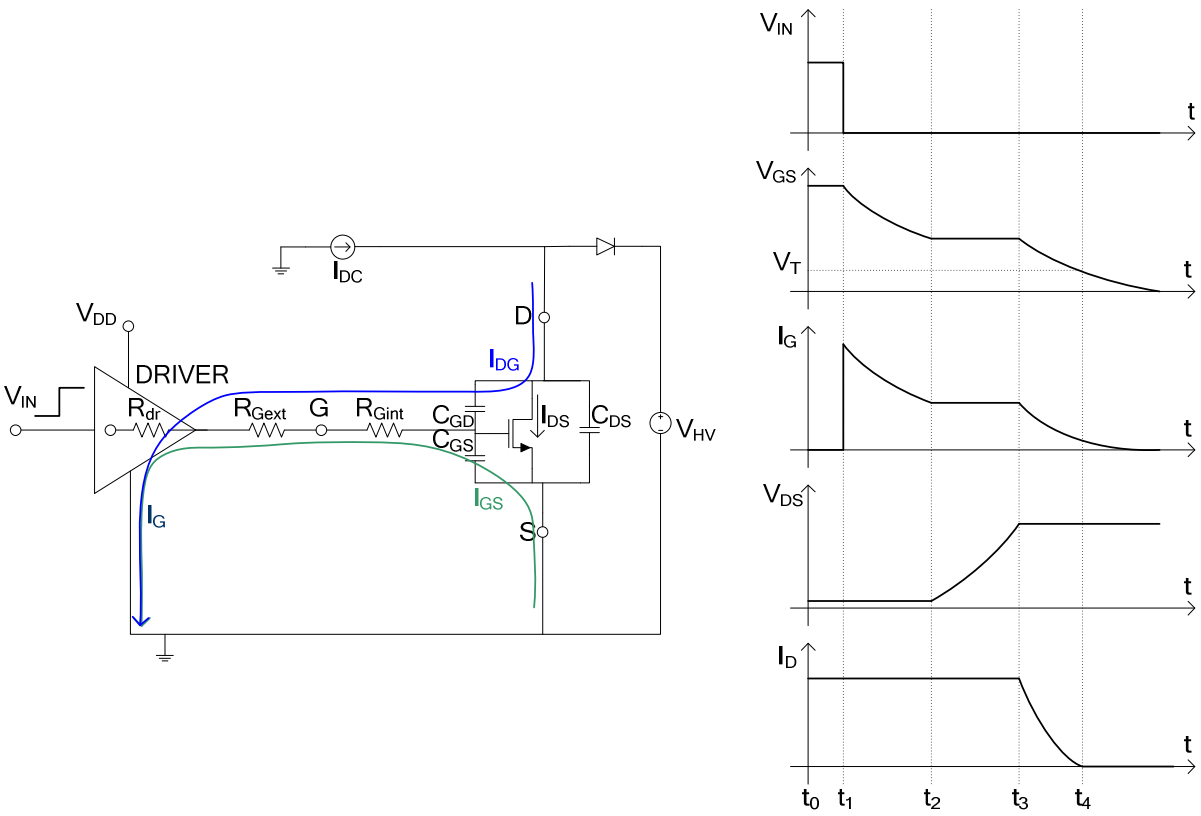


Figure 5. 39. Power MOSFET turn-off procedure;
a) circuit schematic and gate currents; b) Variation of main signals

DRIVER CIRCUITRY

The MOSFET driver can be seen from a behavioural point of view as a current amplifier with a level shifter at the output to meet the required output range.

In the previous analysis it has been assumed that the driver output resistance is constant for the turn on and turn off process. In practice this can depend on the architecture of the output stage of the driver. For the monolithic driver implementation (analogue mode) the final stage of driver has been implemented using an isolated NMOS for the high side (see figure 5.40) due to its reduced ON resistance at maximum gate bias (11.9kΩ×µm width) compared with a PMOS device (11.9kΩ×µm width). The drawback of having an n-type MOSFET on the high-side is that its source potential is given by the output voltage of the driver. Thus when the power switch is turned on, the high-side transistor of the driver sources the entire switch gate current and the overdrive of the high-side transistor drops as V_{GS_switch} increases. If the supply voltage of the driver is large enough, this is not a problem as it will run out of head room long after the power switch is turned on. On the other hand, it is not recommended to have V_{GS_max} too large, as it will increase the switching losses due to extra charge being

sourced in the gate of the switch, and the R_{DS_ON} of the power MOSFET stops decreasing above a certain value of V_{GS} (usually 10-14V).

The power MOSFETs selected for this application (SPA02N80C3) have the following parameters: V_T=3V, $V_{PLATEAU}$=5.5V, Q_G=12nC, R_{Gint}=1.2Ω, R_{DS_ON}=2.7Ω, V_{DS_MAX} =800V, V_{GS_MAX}=20V, under the following conditions of T_J=25ºC, V_{DS}=640V, I_D=2A, V_{GS_ON}=10V. As the Miller plateau voltage is low compared with the nominal V_{GS_ON}, a high-side NMOS proves to be a suitable solution for the driver. However, it should be expected that the settling time after t_4 (figure 5.38) will increase considerably due to the low overdrive of the high-side driver NMOS in that region.

Figure 5.40 presents the schematic of the output driver. At the input of the circuit a chain of inverters is followed by a level shifter that interfaces the signal from the low voltage (3.3V) circuitry to the high voltage (15-20V) domain. The chain of inverters connected to the output of the level shifter increase the current drive capability of the signal (similarly to the previous inverters), in order to match the gate capacitances of M1 and M2 (figure 5.40).

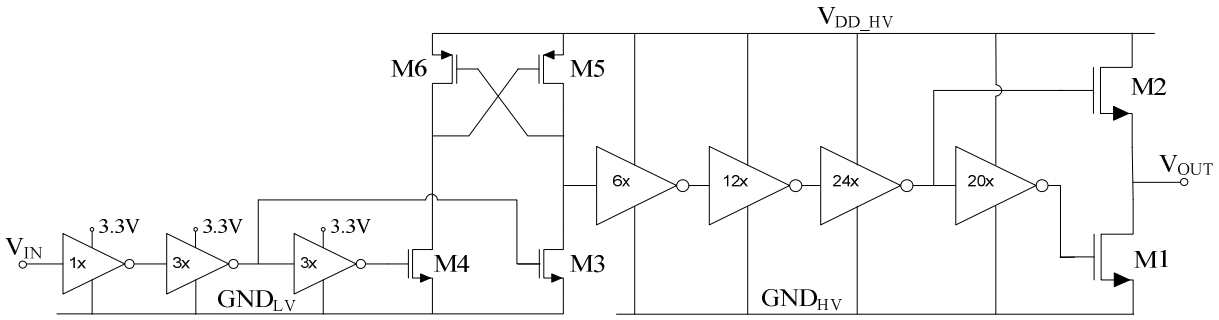


Figure 5. 40. Circuit diagram for the switch driver

The timing diagrams presented before have critical importance in the sizing of the driver and estimation of the converter power dissipation and efficiency. Primarily, the sizing of M1 and M2 is done in such a manner so that the switching time is reduced to a minimum. From that point of view one should be tempted to make those devices as large as possible. But other tradeoffs come from the large die area and the current density of the bonding pads and tracks.

The electromigration current limit of a standard pad in this technology is approximately 200mA. Each driver is connected to the power switch using two bonding pads. As the technology design rules for the electromigration limit (1.07mA/μm) refers to the DC current, the pulsed current limitation for the pads can be estimated at 300mA and the fusing current to approximately ten times the electromigration limit (i.e. 2A). The circuit aims to drive the gate

of the power switch up to approximately 12-15V. Looking at the diagrams from figures 5.38 and 5.39, it can be observed that the maximum gate current is achieved at moment $t_1$and is equal to:

$$I_{G\_MAX} = {V_{DR\_MAX}}/{(R_{DR} + R_{Gext} + R_{Gint})} \quad (5.60)$$

Based on the equation above and a maximum gate swing of 15V, the minimum total resistance between the gate and the driver is set to approximately 25Ω. In order to allow some flexibility for the design the on-chip resistance of the driver has been set to 10Ω, out of which 3Ω are for resistance of the tracks, bonding pads and wires, etc. The rest of approximately 12Ω is to be assigned to R_{Gext}.

All the high voltage NMOS transistors have to be isolated from the substrate in order to reduce the noise injected into the substrate at the moment of switching. The nominal values of the ON resistance for the NMOS and PMOS devices are 8.8kΩ*µm and 19kΩ*µm. The resulting width of M1 is approximately 1300µm, for 7Ω ON resistance. To ensure a safety margin, the width of M1 has been set to 1500µm. As M2 suffers from a lower overdrive voltage (due to the variable source potential) the width of this device was set to 1800µm to achieve the same ON resistance.

The connection between the high-voltage ground and the low-voltage ground is made off-chip, to reduce the coupling of the switching noise. Transistors M3 and M4 (figure 5.40) are implemented using thin-oxide HV transistors with low-voltage V_{GS_MAX} (3.3V) and high-voltage V_{DS_MAX} (20V). Transistors M5 and M6 are thick gate oxide HV PMOS transistors as the swing of the gate is equal with the HV supply.

Figure 5.41 presents the layout of the driver and the interfacing to the bonding pads. The main concern in the layout of the drivers is the minimisation of the current path for the output MOSFETs (M1 and M2, figure 5.40). To achieve this, transistors M1 and M2 have been placed at a minimum distance from the pads.

The arrangement of the bonding pads also took into consideration the minimum loop length requirement for the output signals: the output pads are placed in the middle, V_{DD_HV} pad is on the left side (close to M2) and GND_{HV} is located on the right side (close to M1). The electrostatic discharge (ESD) protection is placed in between the IO pads and V_{DD_HV} together with a ground pad to minimise the loop for ESD currents. The second driver is generated as a mirrored version (to the left) of the first one, with the two blocks sharing the GND_{HV} (in the middle).

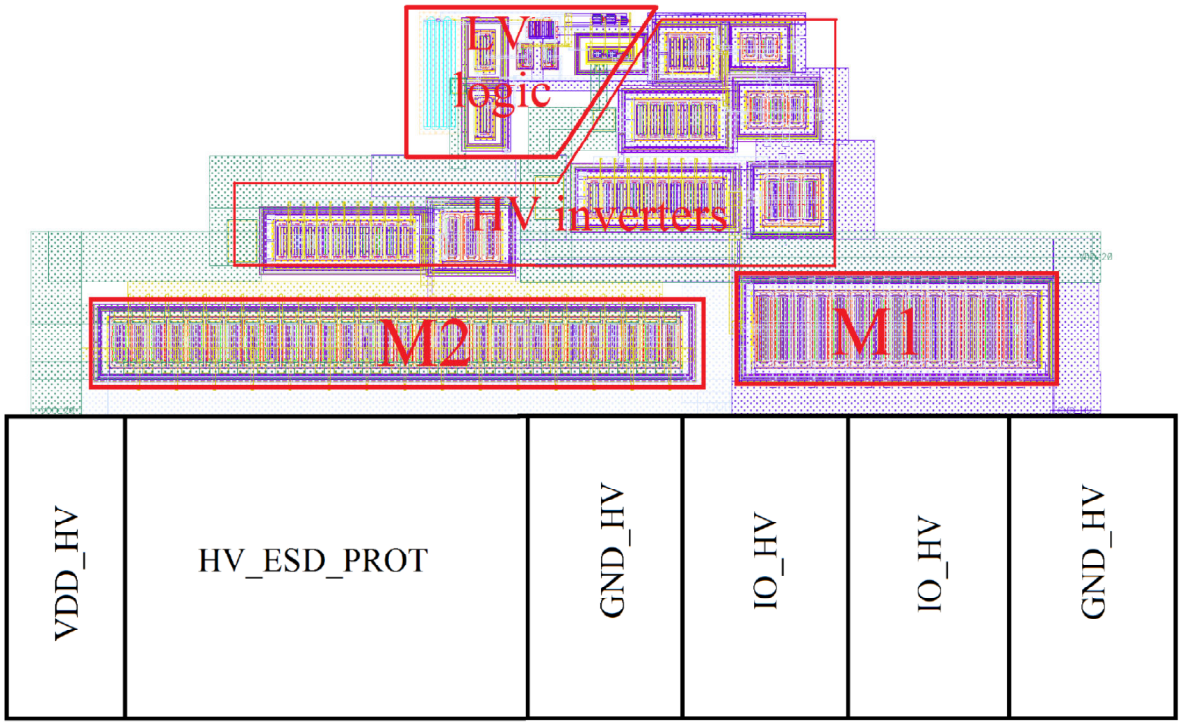


Figure 5. 41. Driver layout and placement of the bonding pads

As can be seen in figure 5.41, a wide area of the drivers' layout is occupied by the isolation (deep n-tub) of the drivers, HV inverters and metal tracks. In order to reduce the area and improve the transient behaviour for the second iteration, in the mixed-signal implementation (chapter 7) the final stage of the driver has been designed with a PMOS transistor on the high-side (Figure 5.42). This configuration saves an HV inverter stage and simplifies the routing and the placement of the blocks. On the other hand, it requires a larger inverter to drive both M1 and M2 and the width of the PMOS is set 2.2 times larger than M1, i.e. 3300µm.

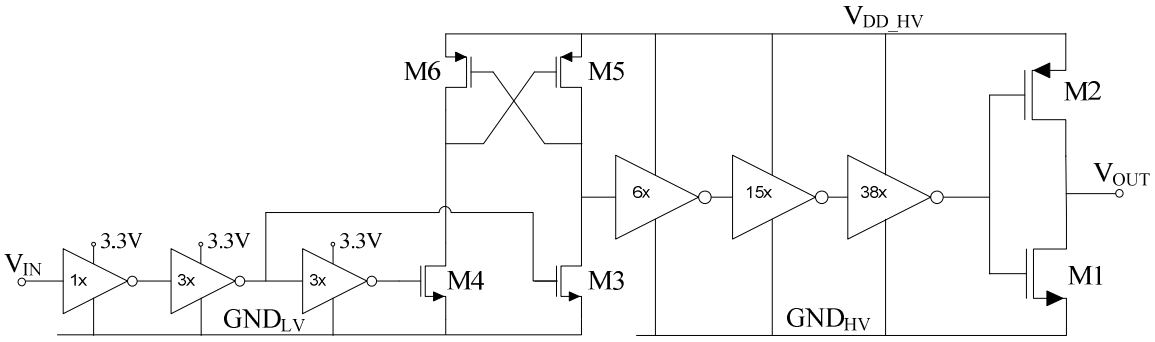


Figure 5. 42. Circuit diagram of the driver for the mixed-signal charger implementation

Figure 5.43 presents the layout and the bonding pads placement for the second version of the driver circuit. M1 and M2 are placed as before and right on top of them sits the 38x inverter, driving their gates. The placement of the devices is more compact in this case and

the routing is more efficient (no routing channels are required for the wide metal tracks). The bonding pads are placed similarly to the previous circuit, but in this case the ESD protection circuit is placed in between the two driver blocks. The second driver is placed on the right hand side of the one illustrated (oriented with the GND pad towards the ESD protection circuit). The dimensions of the first and second driver designs (including the pad wiring) are 735µm × 275µm and 567µm × 195µm respectively. The gaps on the sides of the first driver layout are filled with decoupling capacitors. Even though the active area is larger in the second implementation, the net area is still slightly lower compared with the first design (Fig. 5.40 and 41).

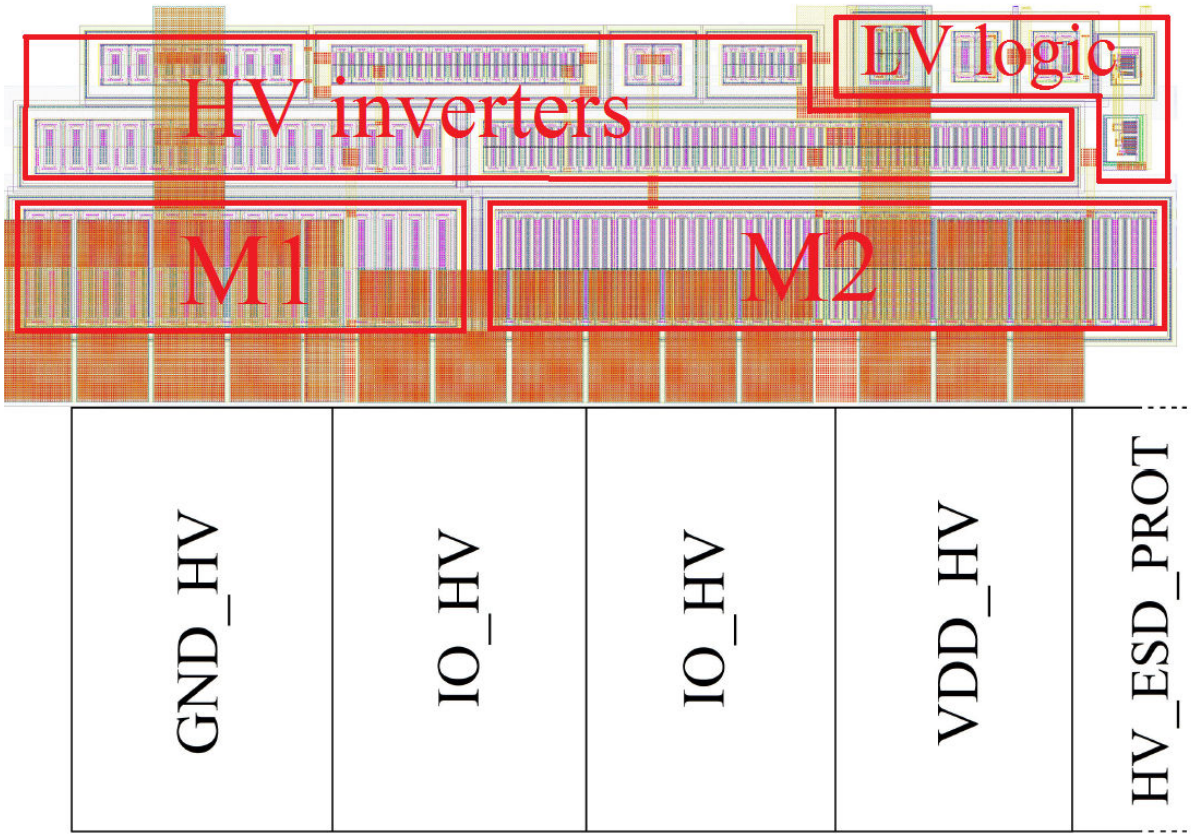


Figure 5. 43. Driver layout and placement of the bonding pads for the mixed-signal architecture

The above considerations for gate voltage profile (see Fig. 5.38 and 5.39) and driver design have been validated through circuit simulation and measurement. Figure 5.44 presents the simulated gate-source voltage waveform, for the first driver implementation (Fig. 5.40). The measurement result is presented in figure 6.10). The simulation has been done under the following conditions: The driver supply voltage V_{Driver}=15V, the drain-source voltage of the discrete power switches is 300V, 16Ω discrete gate resistors are used and inductive load for the switch. The effective turn- and turn-off (until the end of the Miller Plateau) of the switches takes approximately 50ns.

During the turn-on process, due to the use of the high-side NMOS transistor the slope of the gate voltage decays above the Miller plateau due to the increasing ON resistance of the high-side transistor of the driver circuit. This does not represent a problem as the power FET is fully turned ON at the end of the Miller plateau and from this point the increasing value of V_{GS} will only contribute to a lower R_{DS_ON} value.

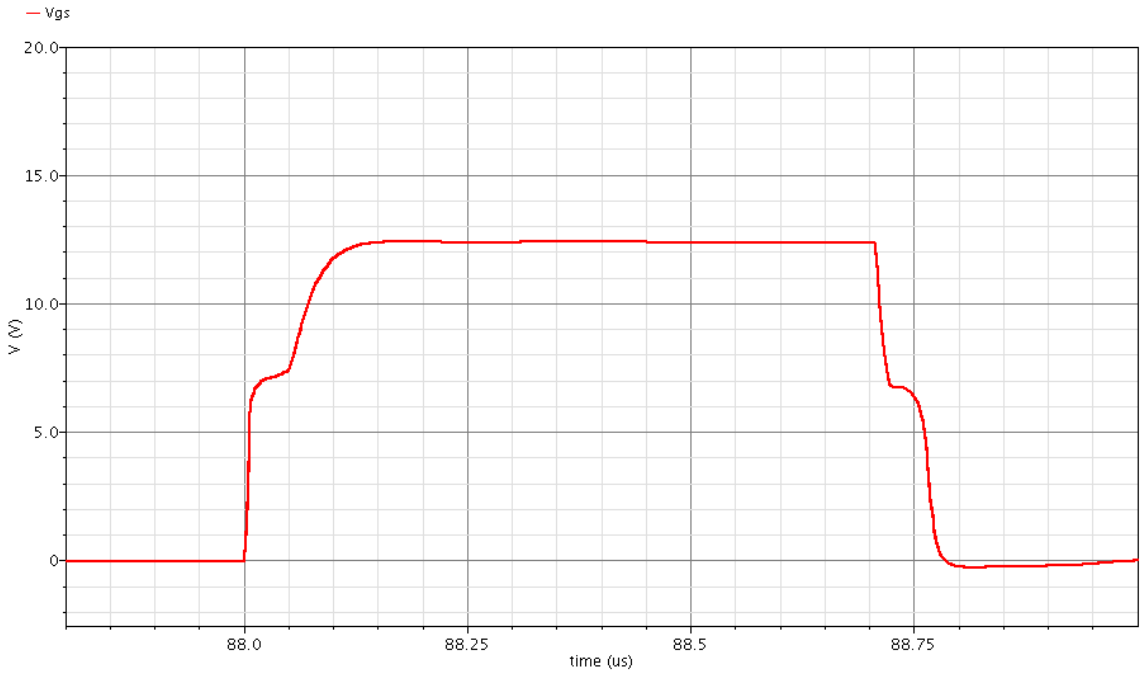


Figure 5. 44 Gate to source voltage waveform simulation
(V_{DD_driver}=15V, V_{DD_switch}=300V and R_{sw_gate}=16Ω)

5.3.9 IC floor plan

The floor plan of the integrated circuit must take into consideration the requirements of the system and individual sub-blocks. From the top level, the IC can be divided into three parts: low voltage analogue circuitry, digital block and high voltage (HV) drivers. Each of the three sections must have separate supply rails to avoid the coupling of the switching noise into the analogue signals (from digital block and drivers) and thus into the analogue blocks. Table 5.1 presents the list of pins used and their functionality.

The implementation of the system in a bulk CMOS process requires that all parts share the same substrate. The switch drivers will introduce high energy transients at the moment of the switching (due to very short current pulses of up to 600mA) that can couple through the substrate to the low voltage circuits, if not well isolated. To achieve this goal, isolated N-MOSFETs have been used for the drivers and driver pads. Also, a spacing of 400µm has been

introduced between the driver final stage and analogue circuitry, also serving to reduce any temperature gradient present in the analogue blocks that could affect the translinear functions.

The placement on the bonding pads has been done in such a manner to minimise the unwanted coupling between adjacent bonding wires, pins and tracks. Figure 5.45 presents the chip floor plan and pad ring while figures 5.47 and 5.48 show the full chip layout and die photomicrograph. The HV drivers and pads have been placed on the bottom side of the die. All the HV pads are isolated from the bulk substrate and have negligible resistance between the bondpad and I/O pin. The pinout of the chip also isolates the HV pins (on the right side, numbered from 3 to 11) and allows minimum length for the bondwires.

Pin name	Domain	Type	Description
AVDD	Analogue	Power	3.3V supply for analogue blocks
AGND	Analogue	Power	Ground rail for the analogue blocks
VRs	Analogue	Input	Current sense resistor voltage
Vin	Analogue	Input	Scaled value of the rectified input voltage
Vout	Analogue	Input	Scaled value of the output voltage
Vref	Analogue	Input	1.25V reference voltage
Rref	Analogue	Test	Polysilicon test resistor
Cref1	Analogue	Test	Test capacitor top plate
Cref2	Analogue	Test	Test capacitor bottom plate
DVDD	Digital	Power	3.3V Supply for the digital block
DGND	Digital	Power	Ground rail for the digital block
nEN	Digital	Input	Circuit enable (active low)
RegIn	Digital	Input	Trim circuitry register input
Clk	Digital	Input	Clock for the trim register
nReset	Digital	Input	Reset signal (active low)
SW1lv	Digital	Output	Power switch 1 low voltage output
SW2lv	Digital	Output	Power switch 2 low voltage output
VDDHV	Driver	Power	10-20V supply for the output driver
GNDHV	Driver	Power	Ground rail for the output driver
SW1	Driver	Output	Driver 1 output
SW2	Driver	Output	Driver 2 output

Table 5. 1. Pin list for the analogue implementation of the circuit

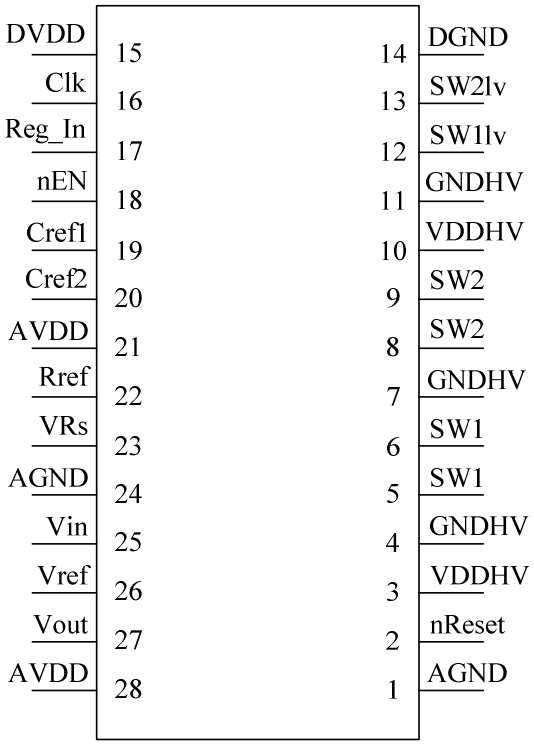


Figure 5. 45. Integrated circuit pinout

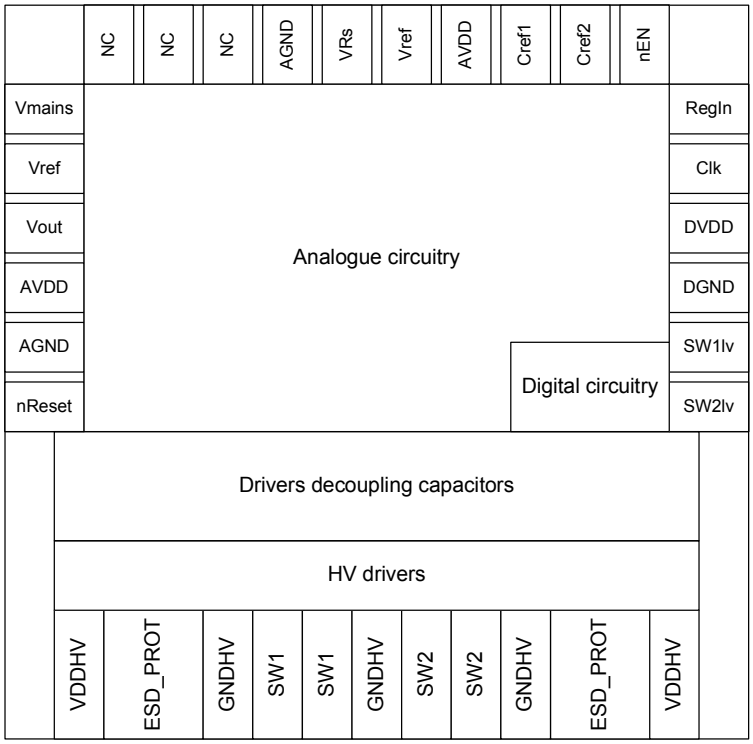


Figure 5. 46. IC floor plan and pad ring

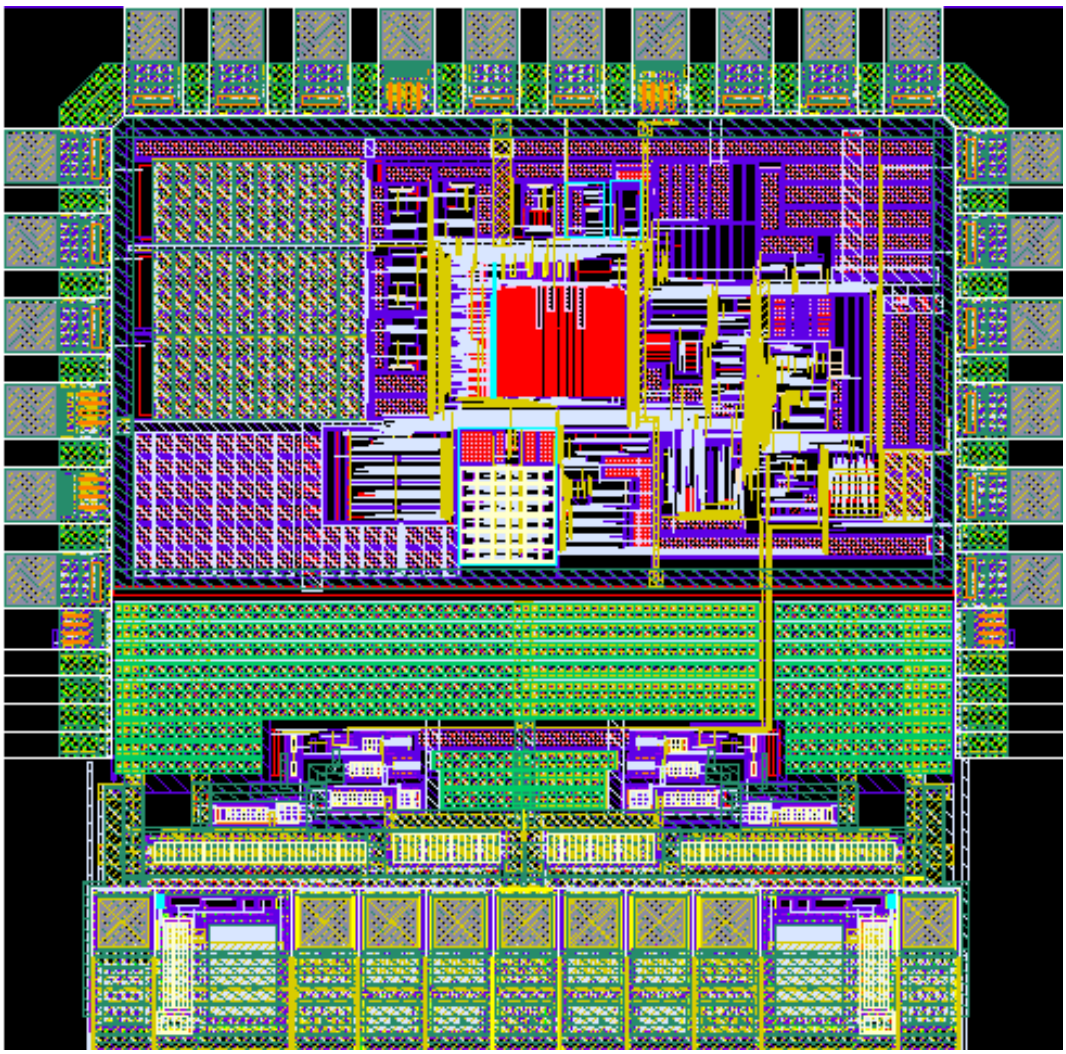


Figure 5. 47. Full chip layout plot

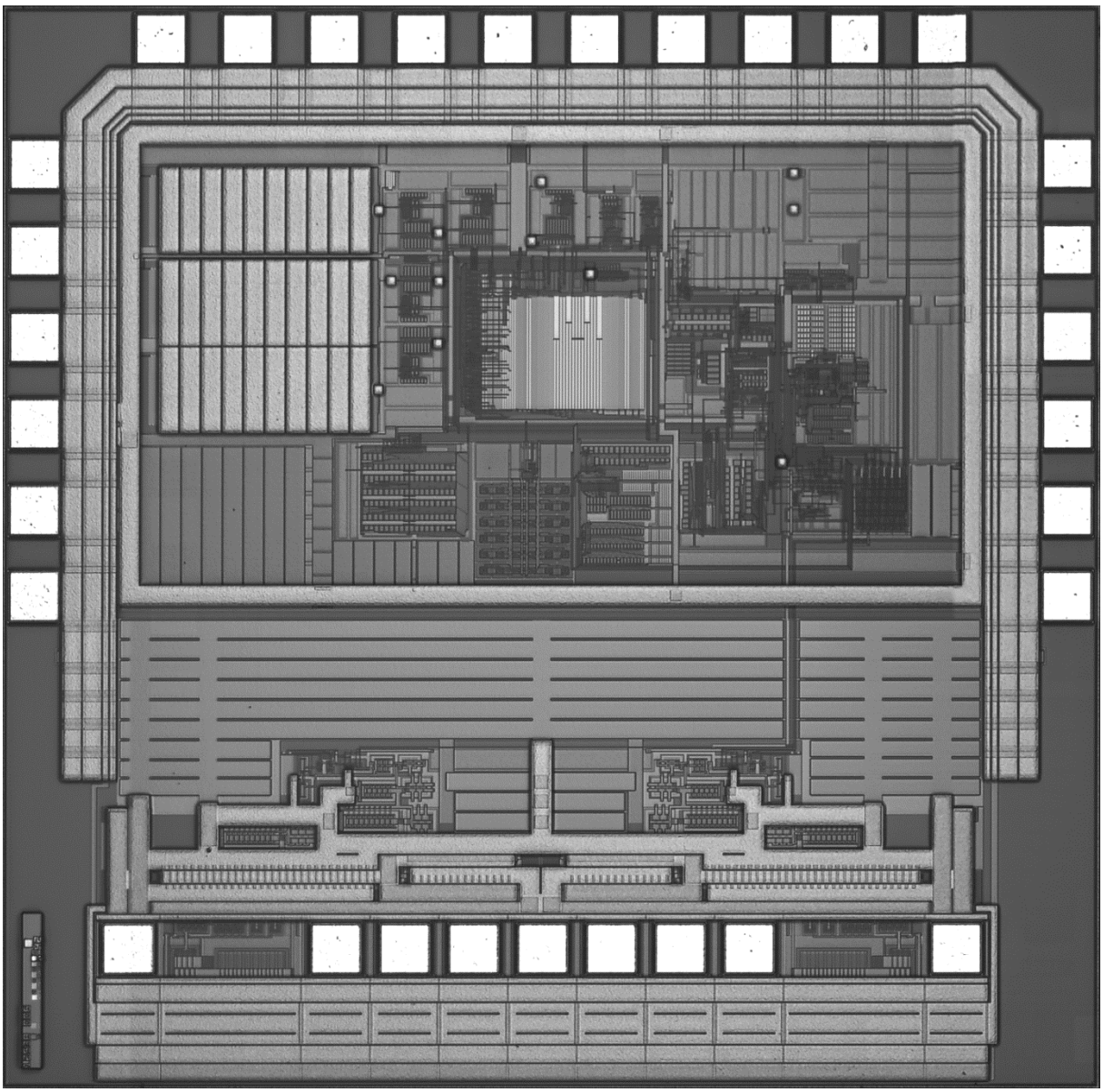


Figure 5. 48. Analogue charger IC photomicrograph

Chapter 6
SIMULATION AND MEASUREMENTS RESULTS ANALOGUE MONOLITHIC DRIVER

This chapter presents the system level simulations and measurements of the circuitry described in Chapter 5. The design of each sub-circuit has been verified pre- and post-layout, over the process corners and temperature. Further, statistical simulations for device mismatch in conjunction with absolute process variation have been carried out.

The design, simulation and layout processes of the circuit have been completed using the Cadence IC 6.1.3 suite (Virtuoso, Spectre and Assura). Due to the practical limitations of the simulator, a simplified model of the transformer has been used for the long transient simulations (over 1ms). The simplified behavioural model of the magnetic components allows a shorter simulation time and a better verification of the integrated circuit over the operating corners. A more complex model of the transformer (including leakage inductance and the snubber circuit) has been simulated separately, for shorter intervals and at several different operating points.

The simulation and measurement results are also presented in parallel to validate the design, showing the behaviour of the main signals that can be probed through non-invasive methods. In some other cases, a better insight of the circuitry can be achieved only by simulation, and hence comparative measurement data are not present in every case.

6.1 Testbench circuit

The simplified circuit diagram of the simulation and measurement testbench for the complete charger is presented in figure 6.1. The main challenge from the system perspective is the realisation of a low-impedance and stable ground plane. When the power MOSFETs switch, a large current spike is injected into the ground plane through the gate of the MOSFETs. Compared with the amplitude of the drain current, the amplitude of this transient current is lower, but the high frequency harmonics can lead to oscillations in the gates of the switches, thus resulting in spurious on/off transitions of the switches that can result in larger oscillations with the leakage inductance of the transformer primary. To avoid this, a shunt capacitor (C_S) has been connected in parallel with the sense resistor, allowing the HF harmonics to bypass the sense resistor, and thus minimising the HF impedance to ground from the source of the switches. Also, the HV ground and the low-voltage analogue ground

have been star-point connected at the bottom terminal of the sense resistor. The star-point connection allows the analogue ground of the IC to be connected to a stable ground point, without transient voltage drops on the tracks/wires due to the MOSFET switching. Care must be taken with the sizing of C_S, as large values can lead to time constants (R_SC_S) that alter the amplitude of the voltage drop on R_S (corresponding to the primary current) that is sampled. Considering that the minimum allowed *ON time* is approximately 700ns, the time constant R_SC_S should be at least five times below this value, resulting in C_S=270nF (R_S=0.5Ω).

A photo of the testbench breadboard is shown in figure 6.2. The system has been split into two parts, low voltage (left-hand-side board) and high voltage (right-hand-side) board. Extra capacitive decoupling (C_F =50uF) has been added to the output of the charger to remove the voltage spikes generated at the switching moments. This also contributes to the attenuation of the output current high frequency ripple, leading to even lower heating of the EDLC cells. In a future implementation of the charger, a larger output inductor ripple could be investigated, with partial attenuation by capacitive means. This would lead to smaller magnetic components and a lighter charger.

As the measured skew of the resistors and capacitors values of the evaluated ICs was very small, the circuit behaviour was nominal with the default trim codes and no digital trimming of the components was required.

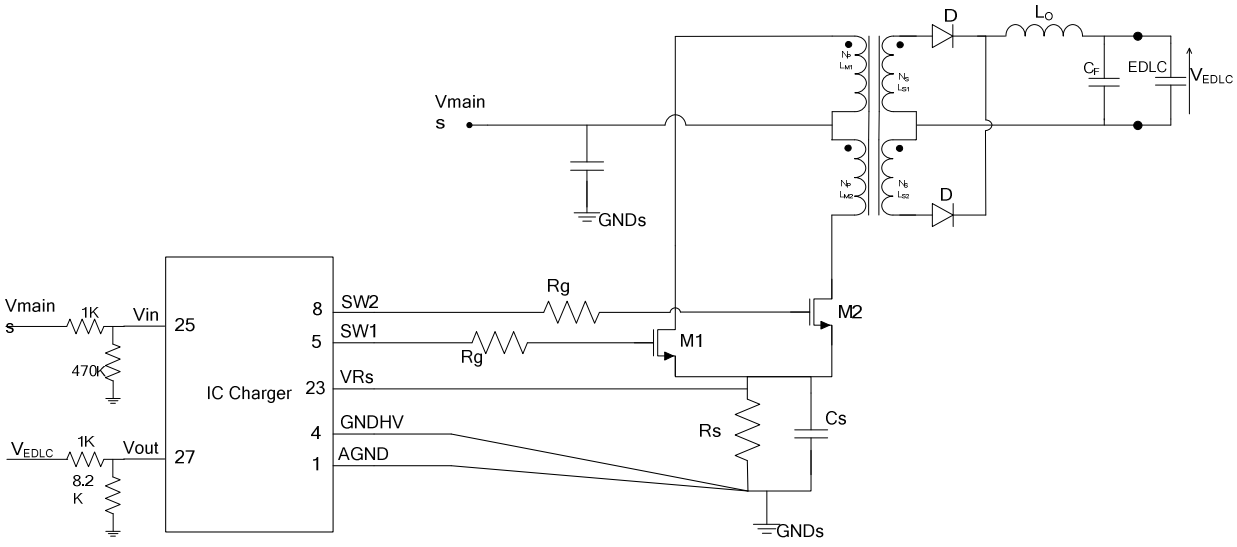


Figure 6. 1. Simplified diagram of the testbench circuit

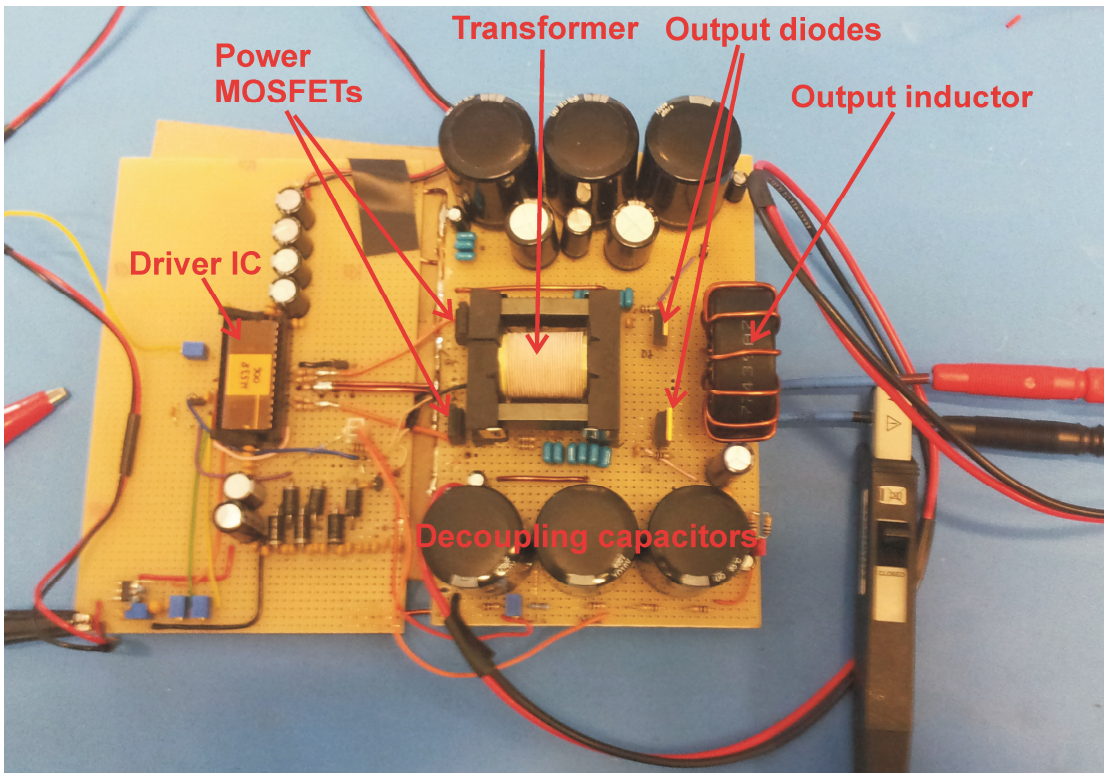


Figure 6. 2. Photo of the testbench breadboard

6.2 Simulation and measurements results

The start of the charging cycle is the most critical part of the converter operation, as it must reach the steady-state within a minimum time, while preserving the stability of the feedback loop. Figure 6.3 and 6.4 show the simulation and measurement of the start-up sequence. The profile of the measured output current matches very well the simulation result. The difference between the ripple of the two waveforms is due to the non-ideal behaviour of the ultracapacitor, element that is considered ideal in the simulation. It can be observed that the input inductance is filtering the load current, also helped by the discrete capacitor (50µF) place in parallel with the ultracapacitor. The spikes on the sense resistor voltage in the measurement plot are mainly due to the fact that the bandwidth of the oscilloscope ground is limited by the lead series inductance. Thus, the oscilloscope could not track the high frequency transients of the system ground. To demonstrate this, the sense resistor voltage has been measured in a differential manner by probing the ground plane separately and subtracting it from the sense resistor signal. The result is showed in figure 6.7, demonstrating the absence of the spikes in this case.

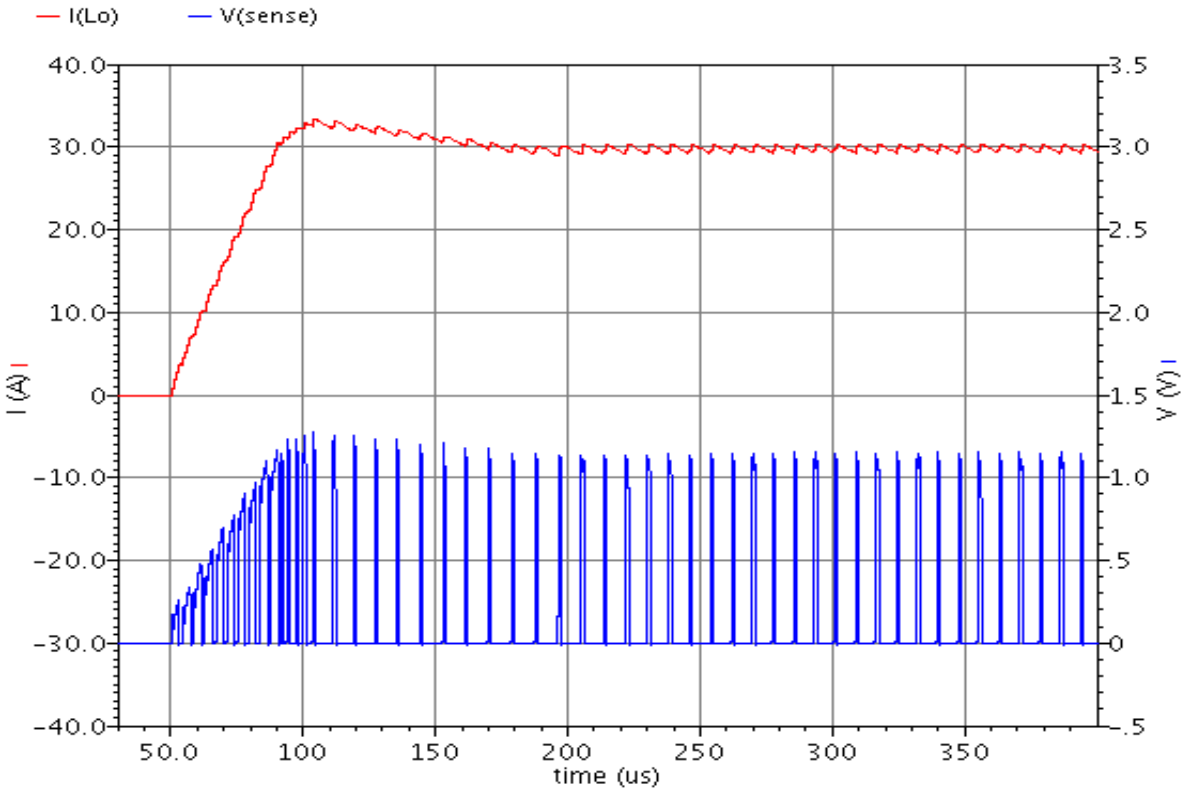


Figure 6. 3. Simulated start-up cycle; output current (red / top), sense resistor voltage (blue / bottom)

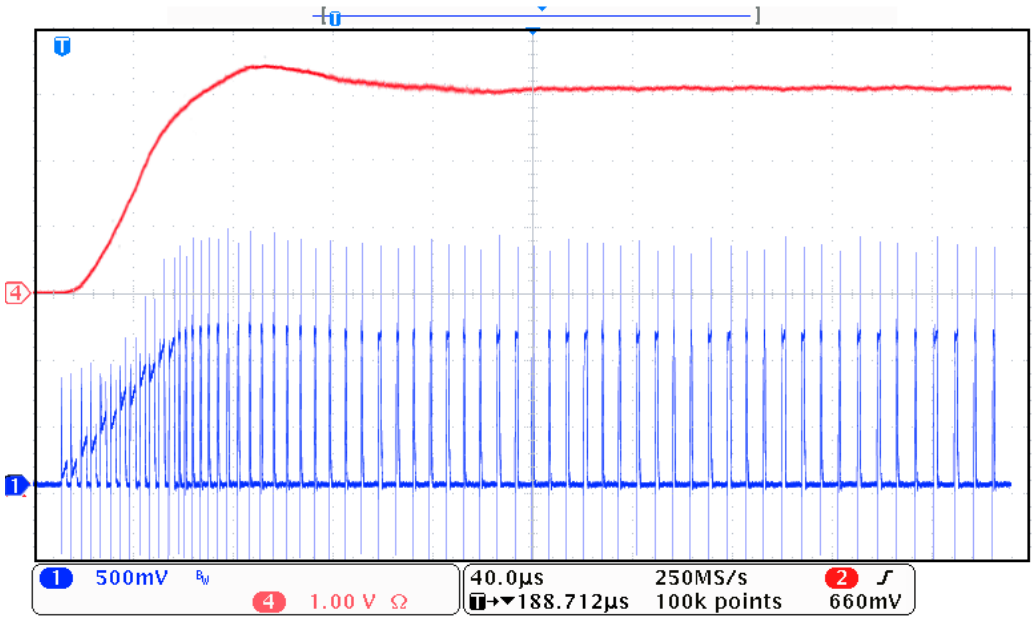


Figure 6. 4. IC measurement of the start-up cycle; output current (red/top), sense resistor voltage (blue/bottom)

Figure 6.5 presents the waveforms (simulation results) of the transformer primary and secondary winding currents. It should be noticed that the ratio of the output currents is constant during the OFF phase, hence the magnetic operating point of the transformer core is maintained constant. The overshoot of the input currents is reduced compared with the one

observed in the measured circuit, as the leakage inductance and snubber circuit were not included in the long transient simulations, due to simulator and model limitations.

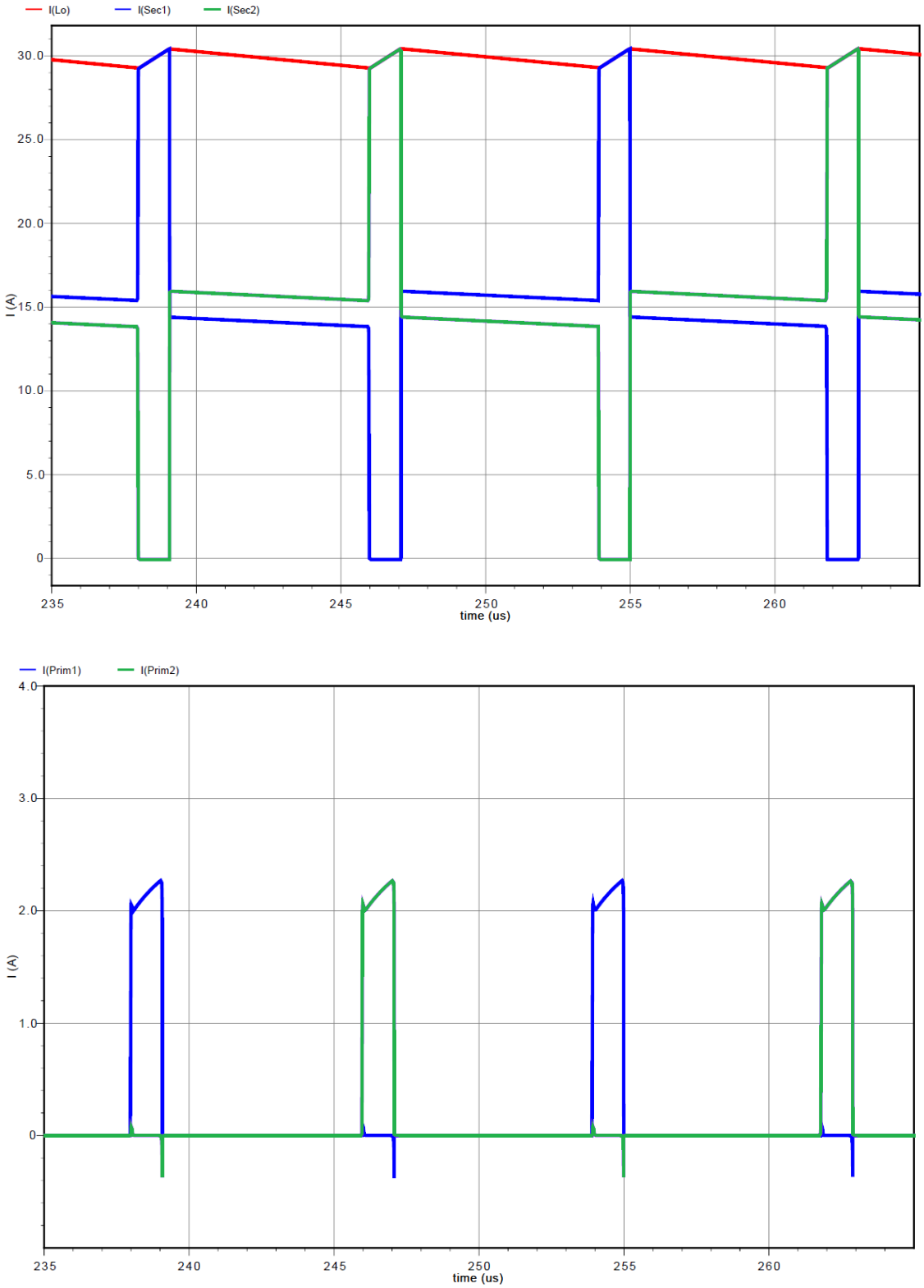


Figure 6. 5. Simulated transformer currents;
top diagram: output current (red), secondary 1 current (blue), secondary 2 current (green);
bottom diagram: primary 1 current (blue), primary 2 current (green)

Figure 6.6 shows the variation of the current corresponding to the OFF phase duration (sample old time-base block) with respect to the waveform of the output current. After approximately 105µs the output current reaches the overcurrent threshold and a large increment is added to the duration of the OFF phase. This allows the system with a large time constant to respond quickly when the output current exceeds the acceptable range.

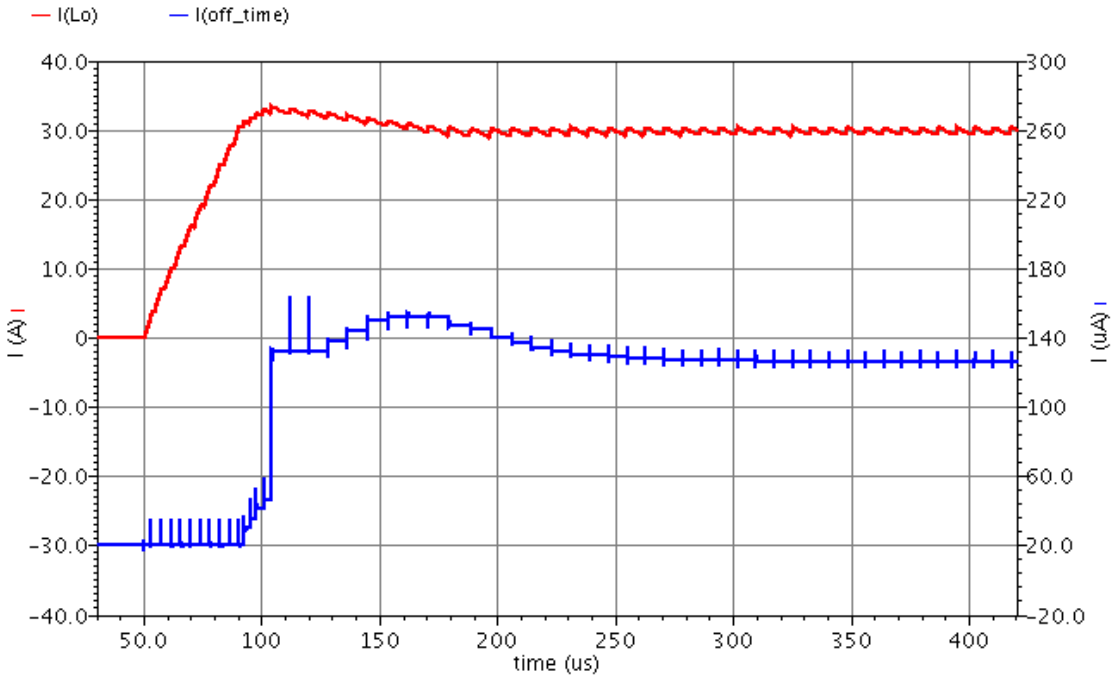


Figure 6. 6. Off time regulation: output current (red/top), voltage corresponding to the off cycle duration (blue/bottom)

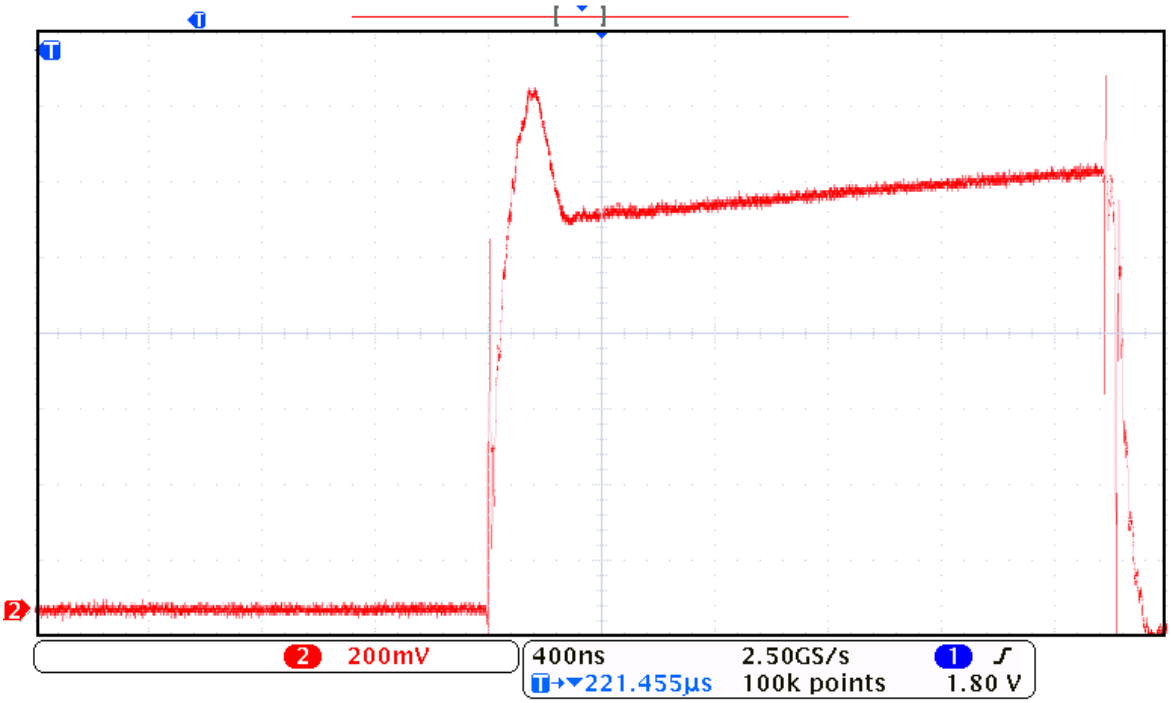


Figure 6. 7. Measurement of voltage drop on the sense resistor for a single HV switch phase, under steady-state conditions

Figure 6.7 shows the voltage drop on the sense resistor generated by a single pulse of the primary side current, under steady state operation of the converter. The overshoot with limited slew-rate from the beginning of the current pulse is generated by the leakage inductance together with the snubber circuit.

Figure 6.8 shows the measured waveforms of the power MOSFETs' drain-source voltages with the snubber circuit included. It should be noted the overshoot duration (approximately 300ns) matches the current overshoot duration, shown in figure 6.7.

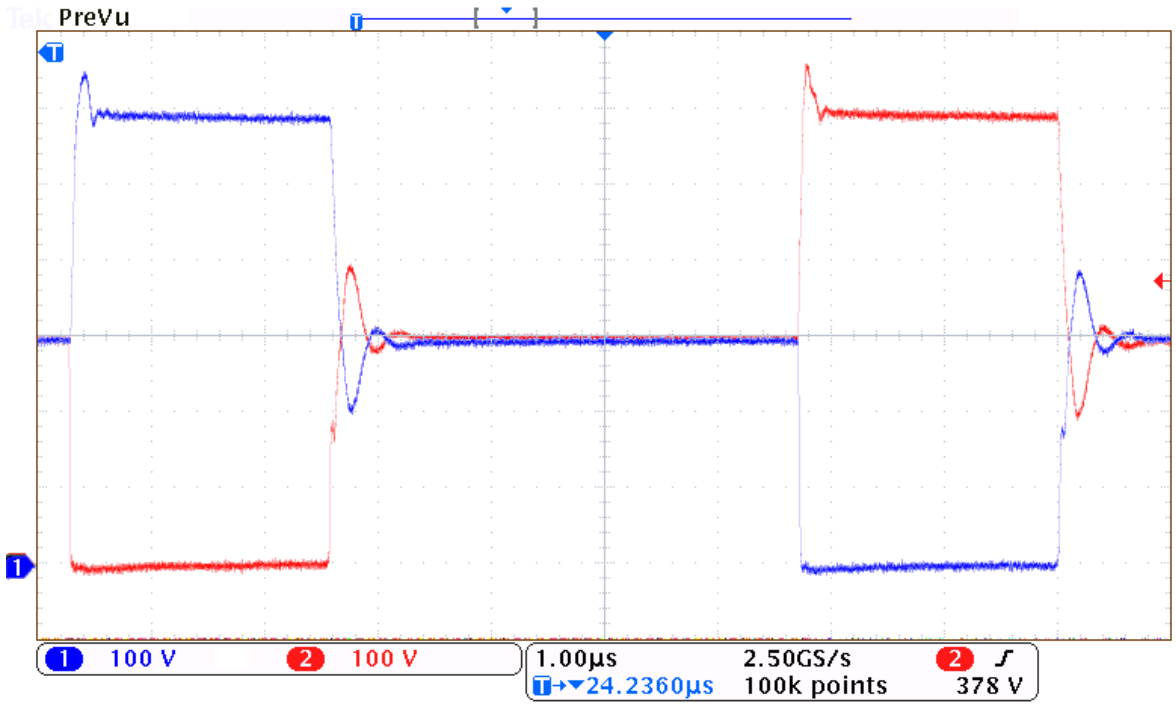


Figure 6. 8. Circuit measurement of the power MOSFETs drain-source voltage

Figures 6.9 and 6.10 present the simulation and measurement waveforms of the power switches gate voltage. The simulation and measurement have been done under the following conditions: Driver supply voltage V_{Driver}=15V, drain-source voltage of the discrete power switches is 300V and 16Ω discrete gate resistors are used. The effective switch turn-on and turn-off (until the end of the Miller Plateau) duration (approx. 50ns) is equal for the simulation and measurement waveforms.

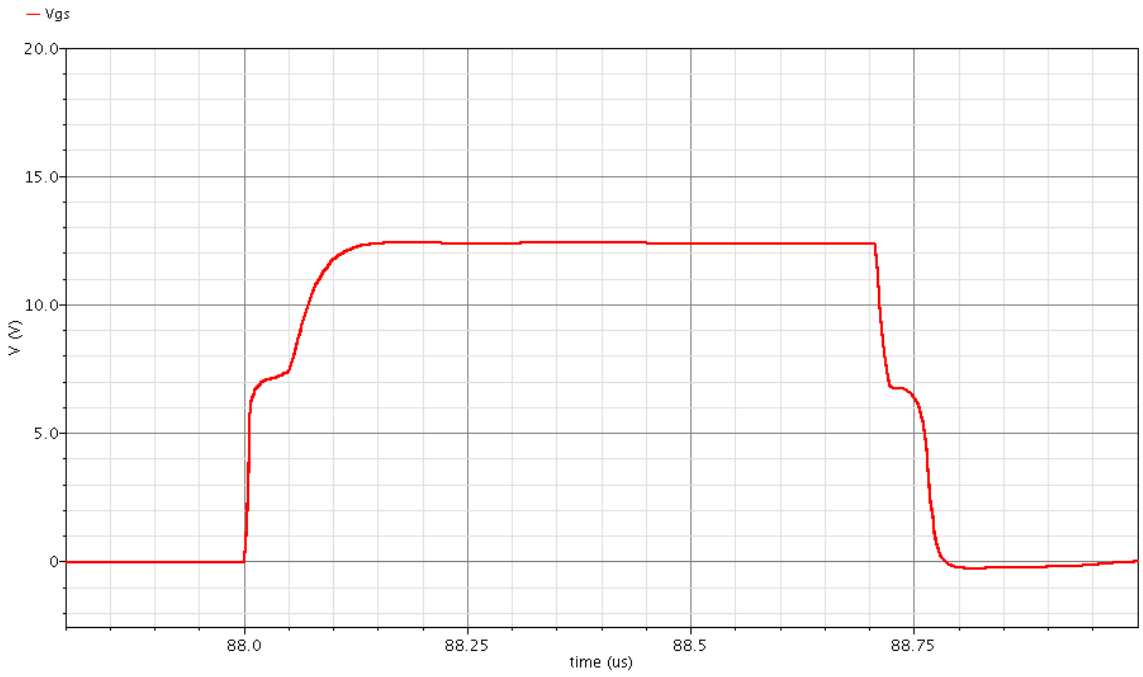


Figure 6. 9 Simulation waveform of the power MOSFET gate voltage (R_G=16Ω)

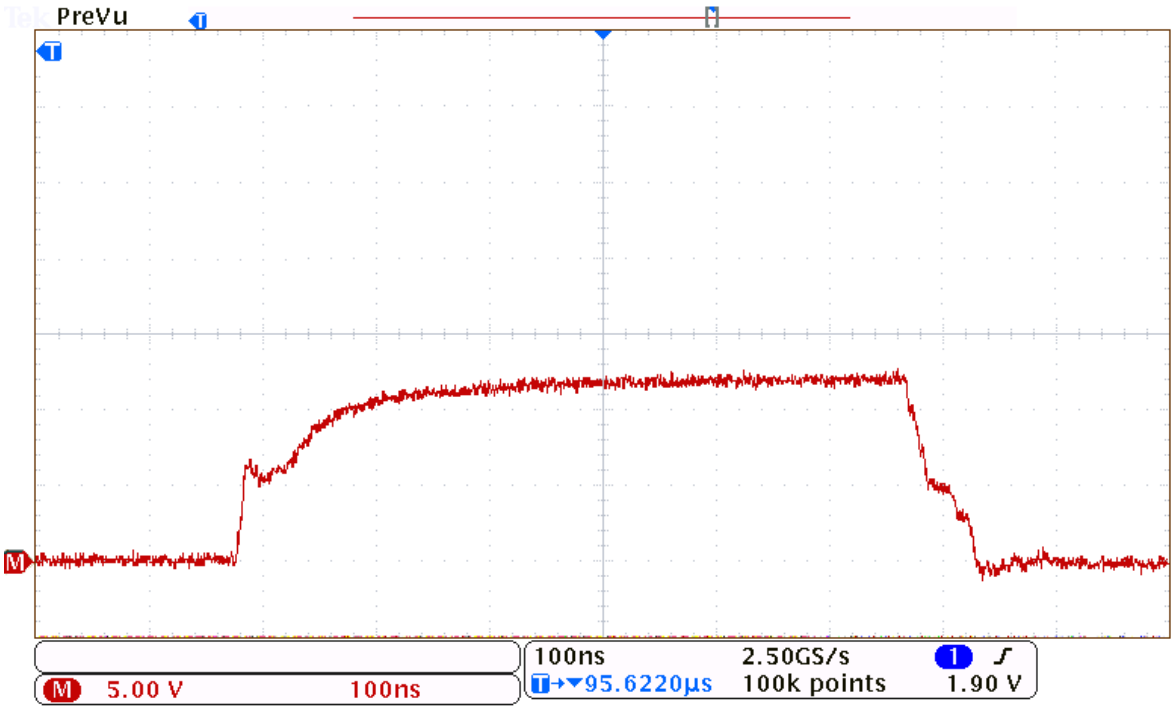


Figure 6. 10. Circuit measurement of the power MOSFET gate voltage (R_G=16Ω)

The full charging cycle has been tested using a string of six EDLCs (350F each). Figure 6.11 shows the variations of the output current, voltage and power. The output voltage increases from 0 to 16.2V in approximately 38s. In chapter 4.4 the total charging time was estimated to be 35.5s, but due to the variable capacitance of the EDLC C=f(Vout), the

charging time is increased slightly. The total energy transferred to the load is 2.13Wh, with an average output power of 210W over the full charging cycle. The average current consumption of the low voltage circuitry is 2mA, while the drivers are absorbing between 9mA and 18mA depending on the instantaneous duty cycle.

The efficiency plot of the system is shown in Fig 6.12. The modest value of the efficiency when the output is below 1.5V is due to the low output power (less than 45W) versus the nearly constant power consumption in the control part. Correlating Fig 6.10 with 6.11, it can be observed that the output voltage reaches the 2V level after less than 2 seconds (partially helped by the impedance of the load); hence the 65% efficiency level is reached after less than 2 seconds from start (5% of the total charging time) with the test load. The peak efficiency operation (above 80%) is reached when the circuit operates in constant output power mode (after 13 seconds for this load). The maximum efficiency level is reached at the end of the charging cycle (approximately 88%). The drop in the input current in the latter part of the charging cycle is due to the lower switching frequency in this region, in accordance with the Matlab estimates from chapter 3.3, Fig. 3.9 and 3.10. The heating of the EDLC casing during a full charging cycle was approximately 7ºC, starting from room temperature.

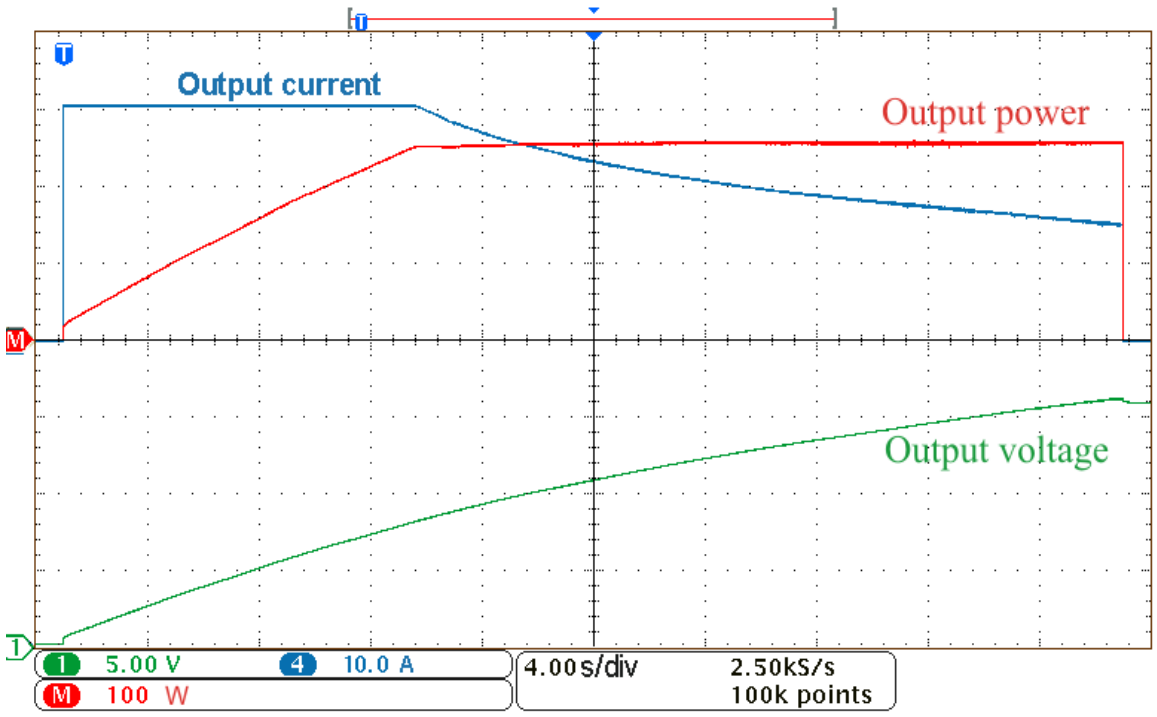


Figure 6. 11. Measurement of the full charging cycle for a string of six EDLCs (350F each)

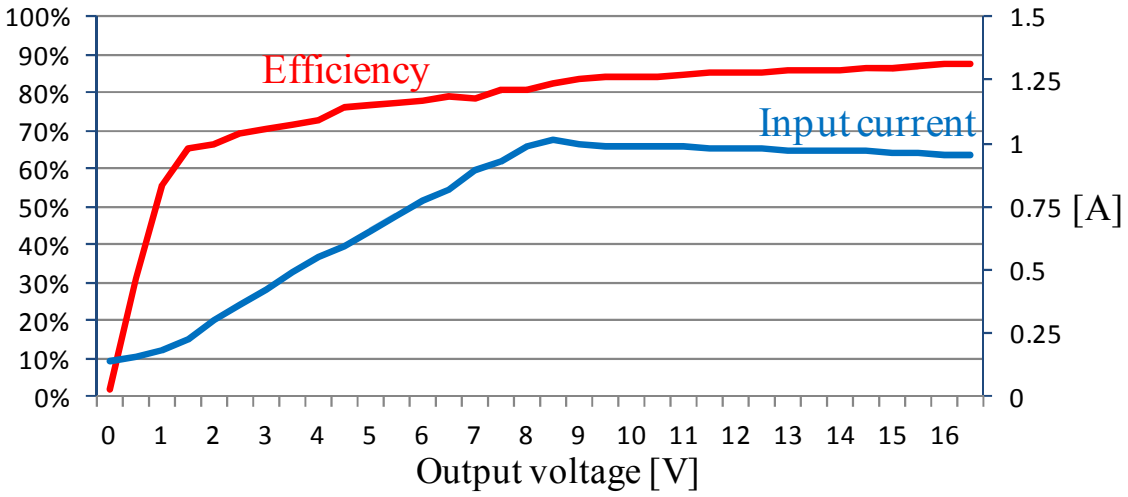


Figure 6. 12. Efficiency and input current plot

Chapter 7
INTEGRATED CIRCUIT DESIGN – MIXED SIGNAL APPROACH

The analogue monolithic driver, presented in the previous two chapters, has been designed as an architectural demonstrator for low-cost high voltage smart power IC processes where the implementation of even moderately complex digital circuits is not feasible due to the long channel length of the available FETs. This chapter looks at the design of a mixed signal integrated circuit that can be used in more modern medium voltage processes (ie. 0.35µm or 0.18µm, V_{DS_max}≈50V). As mentioned before, the high voltage (V_{DS_max}≈800V) technology allows the integration of the power switches on chip. By contrast, while the integration in a medium voltage process means the power switches must be external, a mixed signal implementation in a medium voltage process gives greater flexibility in the choice of the algorithm, better noise immunity and lower die area. In this particular case, the main reason behind developing the mixed signal system is the flexibility of the algorithm. This will allow further optimisation of the charger size, weight and efficiency. In the absence of high frequency thermal model for ultracapacitors the heating of the ultracapacitors cannot be estimated for high frequency and large ripple current. The analogue charger implementation has demonstrated a low heating of the ultracapacitors. Thus it is expected for the ultracapacitor pack to tolerate a larger ripple of the current in exchange for smaller magnetic components. The flexibility of a mixed signal implementation allows simple trimming of the output current ripple, in order to establish the best trade-off between frequency, magnetic components size and heating of the ultracapacitors. Hence, this design should be seen as a platform that is easy to customize and can operate over a wider range compared with the analogue version.

7.1 System architecture

The system can be divided in two parts, from the signal speed point of view. The fast block includes the current monitoring during the ON time, switch turn OFF and over-current protection. The low frequency block consists of the OFF time estimation block and the reference generator for setting the profile of the output current over the charging cycle. The circuitry handling slowly varying signals can be implemented using digital logic. Figure 7.1 presents the system diagram with the fast continuous-time block highlighted in yellow and the low speed mixed signal circuitry in blue. The function of the digital block is to estimate the OFF time duration, generate the input code for the digital divider as a function of V_{OUT}, set

the minimum/maximum ON time duration and drive the control signals for the analogue blocks. For flexibility reasons, the digital block was intended to be implemented off-chip using an FPGA, thus allowing the use of different digital algorithms with the same analogue silicon, and easy trimming of the system scaling constants.

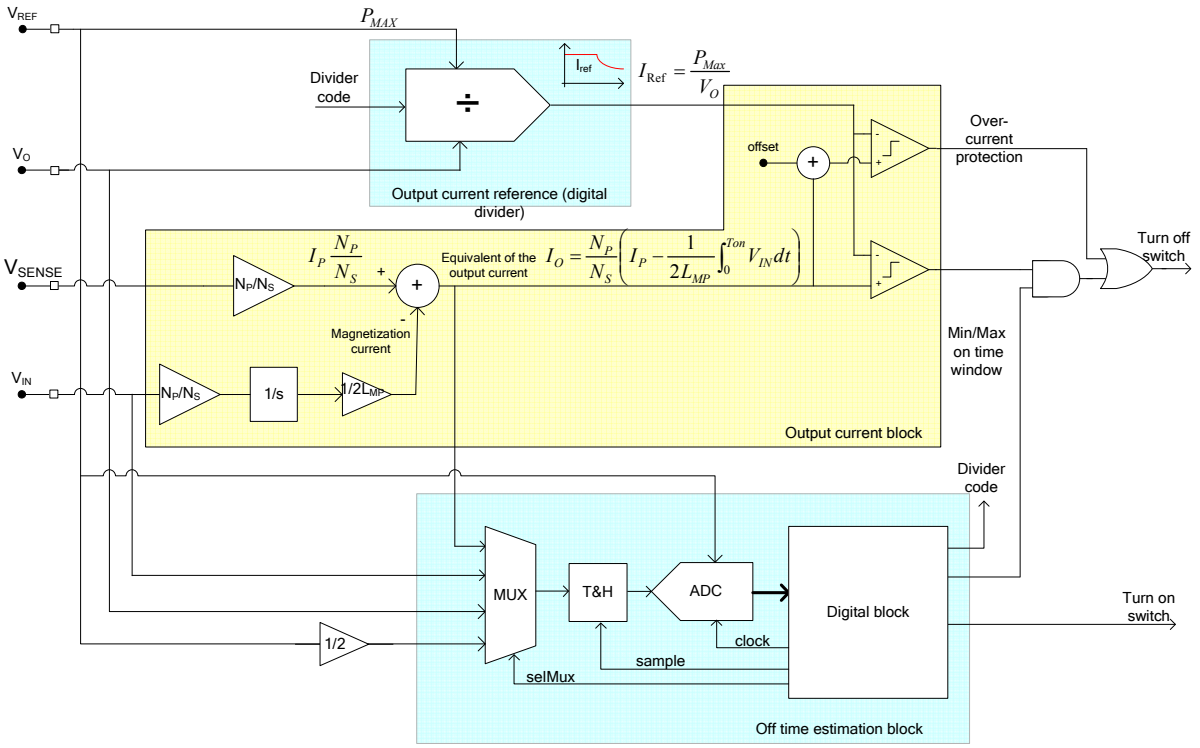


Figure 7. 1. Mixed signal implementation - block diagram

The analogue block, which monitors the value of the output current during the ON time, operates in a similar manner to the analogue implementation described in chapter 5, but due to the reduced complexity it was implemented in voltage mode. The input values that determine the duration of the OFF time (V_{IN}, V_O and V_{IN}) are multiplexed, sampled and then digitized with the aid of a fast 8 bit analogue to digital converter (ADC). For ADC testing and calibration purposes, the reference signal can be selected at the input of the multiplexer, as well as the normal signal path. The operation of the algorithm for the *'ON time integration algorithm'* is described with the aid of the waveform diagrams shown in figure 7.2.

As the integration of the ON time is made in the digital domain it requires the sampling and digitization of the input current value at the end of each ON phase. Hence the OFF time block performs two tasks during each ON cycle: first, the integration of the previously acquired value, and in the second half, the sampling of the primary current. The track and hold block turns to sample mode as soon as the ADC conversion is complete (time t_2) and

switches back to hold mode at the end of the *ON cycle* (time t_3). During the ON time, the digital block integrates a signal corresponding to the voltage drop on the primary winding, according to equation (7.1):

$$V_P = \int_0^{Ton} \frac{N_S}{N_P} V_{IN} - (V_O + V_D) dt \qquad (7.1)$$

With the equivalent in the digital domain:

$$V_P[N] = \frac{N}{f_{clk}} \left(\frac{N_S}{N_P} V_{IN} - (V_O + V_D) \right) \qquad (7.2)$$

Where f_{clk} is the clock frequency and N is the number of clock cycles counted from the beginning of the *ON phase*.

Once the digitisation of the sense voltage (corresponding to the primary current) is complete, the digital block computes the new OFF time duration in a similar manner to the analogue circuit. First, the error is calculated between the integrated primary voltage drop during the ON time ($V_P[N]$) and the reference value according to the system level continuous time equation:

$$err = \Delta I_o L_o - \int_0^{Ton} \frac{N_S}{N_P} V_{IN} - (V_O + V_D) dt \qquad (7.3)$$

The error is then scaled and added to the previous OFF cycle duration. If the over-current comparator output is high, the duration of the OFF cycle is reset to maximum value. Also if the sampled value of the primary current is larger than the reference for the end of the cycle, the error scaling factor will increase such that a steady-state condition is reached within the minimum number of cycles. Once the ADC has finished the conversion (time t_4), the sampling block starts tracking the scaled value of V_{IN} or V_{OUT} (alternating every OFF cycle) and samples it at the end of the OFF cycle (time t_5). The cycle repeats as for the previous ON/OFF cycle.

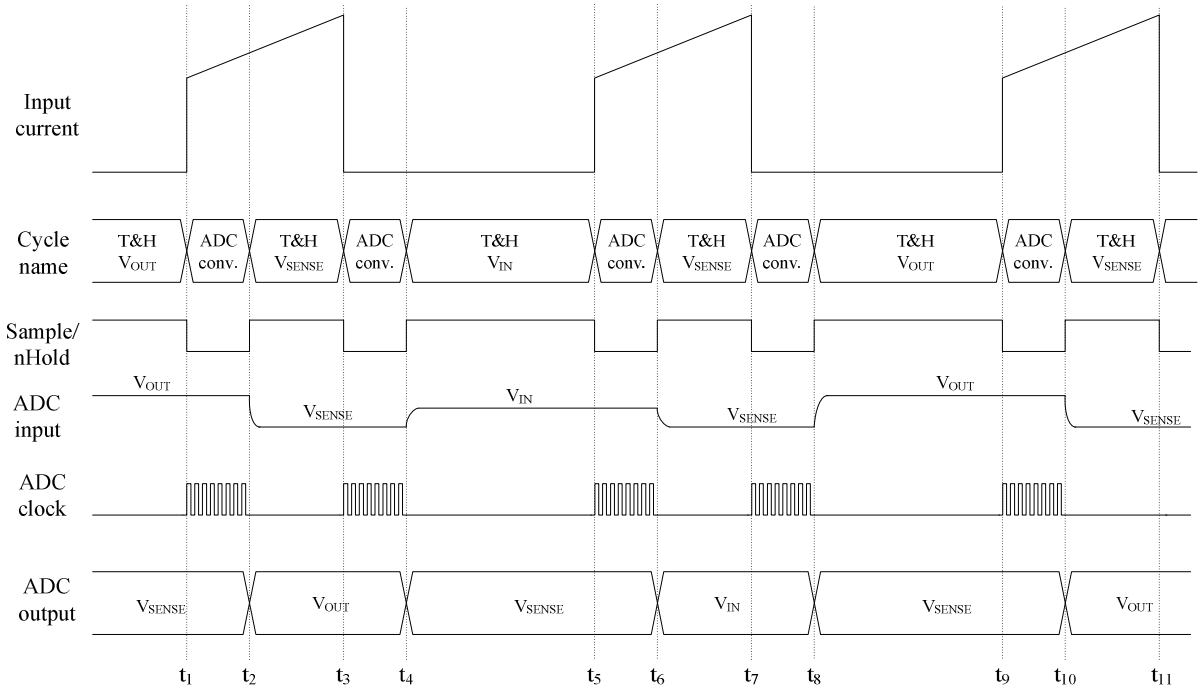


Figure 7. 2. Waveforms for the operation of the 'ON time integration' algorithm

The implementation of the ‘Input current sampling’ algorithm (chapter 3.6.1), with double sampling, is achieved by sampling the input current twice during the ON cycle. This double sampling procedure sets the maximum duration of the analogue to digital conversion. Depending on the parasitic inductance of the transformer primary side and snubber circuit, the input current is expected to settle within 400-500ns. Figure 7.3 presents the characteristic waveforms for the operation of the algorithm. The sampling of the input current is made at moments t_2 and t_3 (t_6 and t_7, t_{10} and t_{11}, respectively). The input current is not sampled at the end of the cycle anymore, but if the end value is required it can be extrapolated. Signal filtering can be added easily using a PID algorithm, if needed.

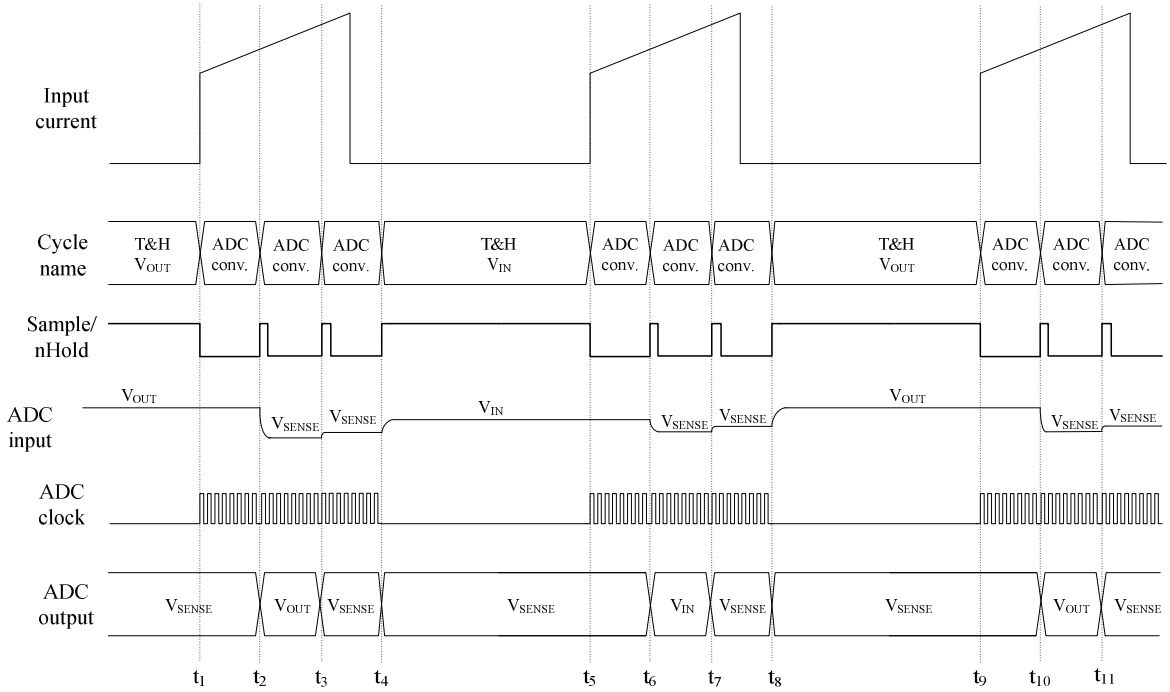


Figure 7. 3 Characteristic waveforms for the 'Input current sampling' algorithm

7.2 Mixed signal voltage divider

Two types of architectures stand out as potential candidates for the efficient implementation of the voltage divider in a mixed signal system. The first one is a digital divider combined with a digital to analogue converter (DAC) and the second is a DAC in divider configuration. The second option was selected in this case as it requires the same analogue circuitry as the first but no digital divider.

The operating principle of the DAC in divider configuration is based on a DAC-amplifier loop where the reference voltage of the DAC is driven by the output of the amplifier, as depicted in figure 7.4. The amplifier will adjust the DAC reference voltage such as the DAC output matches the voltage at the non-inverting input of the amplifier.

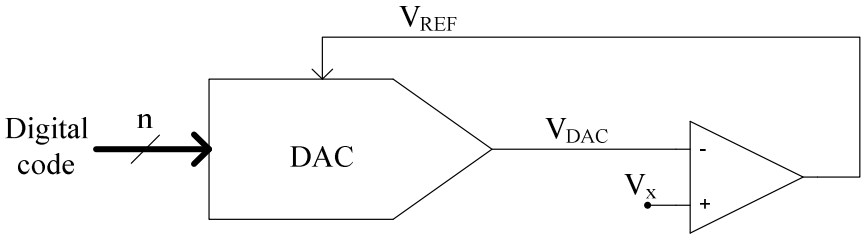


Figure 7. 4. Block diagram of the DAC divider

The DAC output voltage is determined by the following expression:

$$V_{DAC} = V_{REF}\left(\frac{b_{n-1}}{2^1} + \frac{b_{n-2}}{2^2} + \cdots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\right) \qquad (7.4)$$

For an ideal amplifier (with infinite gain) $V_{DAC}=V_X$, hence V_{REF} can be expressed as:

$$V_{REF} = \frac{V_X}{\left(\frac{b_{n-1}}{2^1}+\frac{b_{n-2}}{2^2}+\cdots+\frac{b_1}{2^{n-1}}+\frac{b_0}{2^n}\right)} \qquad (7.5)$$

As a consequence, the regulated reference voltage of the loop serves as the output figure determined by the ratio between V_X and the digital code of the DAC. Two architectures have been derived from the above topology and a R-2R DAC. A third implementation is derived from a voltage to current converter together with the above topology.

Current mode R-2R divider

This circuit is based on the current mode R-2R divider, depicted in Fig. 7.5. In this converter the operational amplifier drives a current through rail A of the R-2R ladder such that the potential of rail A matches the one of rail B.

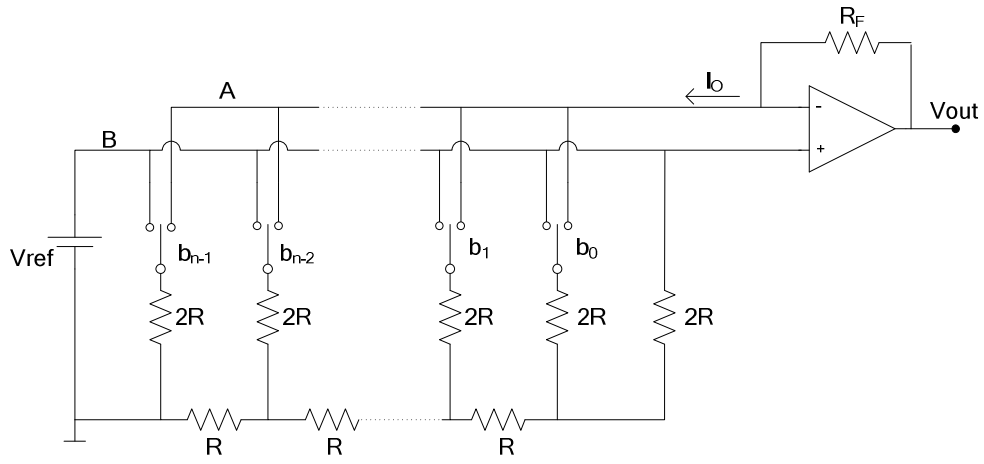


Figure 7. 5. R-2R digital to analogue converter

The total current through rail A is:

$$I_O = \frac{V_{ref}}{R}\left(\frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \cdots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\right) \qquad (7.6)$$

The output voltage of the converter results as:

$$V_{out} = V_{ref} + V_{ref}\frac{R_F}{R}\left(\frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \cdots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\right) \qquad (7.7)$$

In most cases R_F=R and expression (7.7) becomes:

$$V_{out} = V_{ref}\left(1 + \frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \cdots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\right) \qquad (7.8)$$

The circuit presented in figure 7.6 operates in a similar manner to the one above. The operational amplifier OA1 controls the DAC current through rail A and ensures that the potential of rail A and B is equal (V_A=V_B). The current mirror M1-M2 feeds a scaled version of the DAC current into resistor R_O. The amplifier OA2 sets the potential of rail B such that I_1R_1=V_1. The value of the output voltage results as follows:

$$I_{DAC} = \frac{V_A}{R}\left(\frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \cdots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\right) \quad (7.9)$$

$$V_1 = kI_{DAC}R_1 \quad (7.10)$$

$$V_1 = k\frac{R_1}{R}V_B\left(\frac{b_{n-1}}{2} + \frac{b_{n-2}}{4} + \cdots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\right) \quad (7.11)$$

$$V_B = \frac{R}{kR_1}\frac{V_1}{\left(\frac{b_{n-1}}{2}+\frac{b_{n-2}}{4}+\cdots+\frac{b_1}{2^{n-1}}+\frac{b_0}{2^n}\right)} \quad (7.12)$$

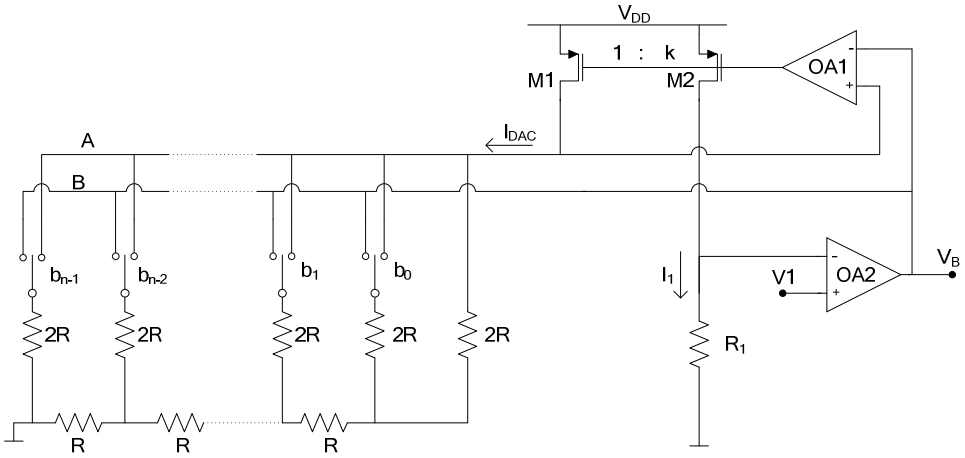


Figure 7. 6. Diagram of the R-2R divider

The parasitic capacitances of the R-2R network can affect the stability of the loop. This can be resolved by introducing a Miller compensation capacitor between the non-inverting input of OA2 and rail B, and setting the dominant pole of the loop.

A main feature of this topology is that the switches are toggling between nodes with the same potential. Thus the voltage drop on the switches will be constant and the parasitic resistor capacitances will not displace charge when the code is changing, increasing the speed of the circuit.

Voltage mode R-2R divider

This second possible divider architecture (Fig 7.7) is derived directly from the principle depicted in Fig 7.4 and implemented with the aid of an R-2R divider.

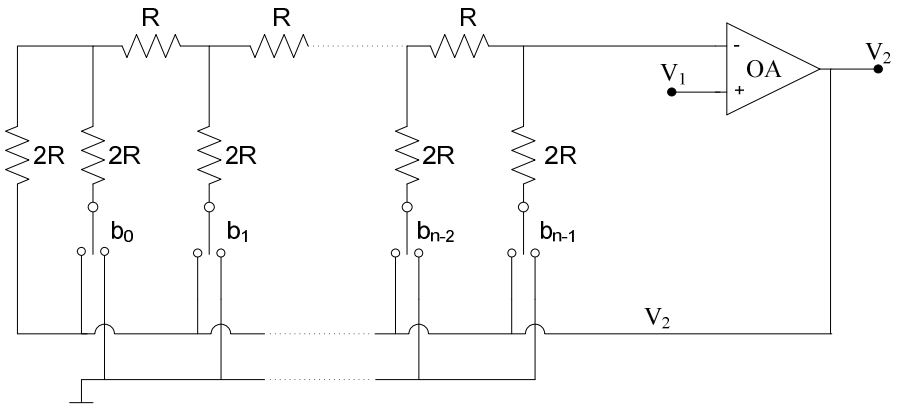


Figure 7. 7 Voltage mode R-2R divider

The voltage from the output of the amplifier is a function of $V_1$and the digital code, as follows:

$$V_2 = \frac{V_1}{\frac{b_{n-1}}{2^1}+\frac{b_{n-2}}{2^2}+\cdots+\frac{b_1}{2^{n-1}}+\frac{b_0}{2^n}} \tag{7.13}$$

The value of the divider LSB is determined as:

$$LSB \cong \frac{2^{-n}}{V_1\left(\frac{b_{n-1}}{2^1}+\frac{b_{n-2}}{2^2}+\cdots+\frac{b_1}{2^{n-1}}+\frac{b_0}{2^n}\right)^2} \tag{7.14}$$

$$LSB \cong \frac{1}{2^n}\frac{V_2^2}{V_1}$$

A dynamic value of the LSB is achieved this way, with smaller steps for lower values of the output signal. Thus, the quantization error is proportional to the Output signal^2.

This architecture shows a significant drawback, compared with the previous one, arising from the fact that the switches are not switching between nodes with equal potentials. Thus, the ON resistance will depend on the position of the switch. As the number of switches is limited, the size is not an impediment and the ON resistance can be made small enough to become negligible compared with the R-2R ladder resistors.

On the other hand, the second implementation benefits from simplicity and higher accuracy, dependent only of the R-2R ladder and the amplifier offset and gain. For this reason the second circuit was the selected option.

As the required bandwidth of the divider is low, the settling time is not a critical constraint and the resistor size can be large (i.e. R=50kΩ). Miller compensation (C=1pF) was used for the operational amplifier to set the dominant pole of the loop and ensure stability.

For the current application the range of the denominator corresponds to an output voltage variation from 8.33V to 16.5V. Thus the range of the denominator (digital code) must

be a ratio greater than 2 between the start and the end of the code range (i.e. 120 to 250). Voltage V_1 is set by the reference voltage (1.25V) and the resulting output range of the divider is 2.66V down to 1.28V. Figure 7.8 shows the output voltage, division error and the variation of the LSB over the range. The sizing of the resistors and switches was made such that the total nonlinearity is kept bellow 1LSB and the DNL is less than 0.5LSB.

The layout of the DAC divider is presented in Figure 7.9. Extra decoupling capacitors have been added to remove noise coupled from the supply. Additional filtering has also been added to the output of the divider to remove glitches.

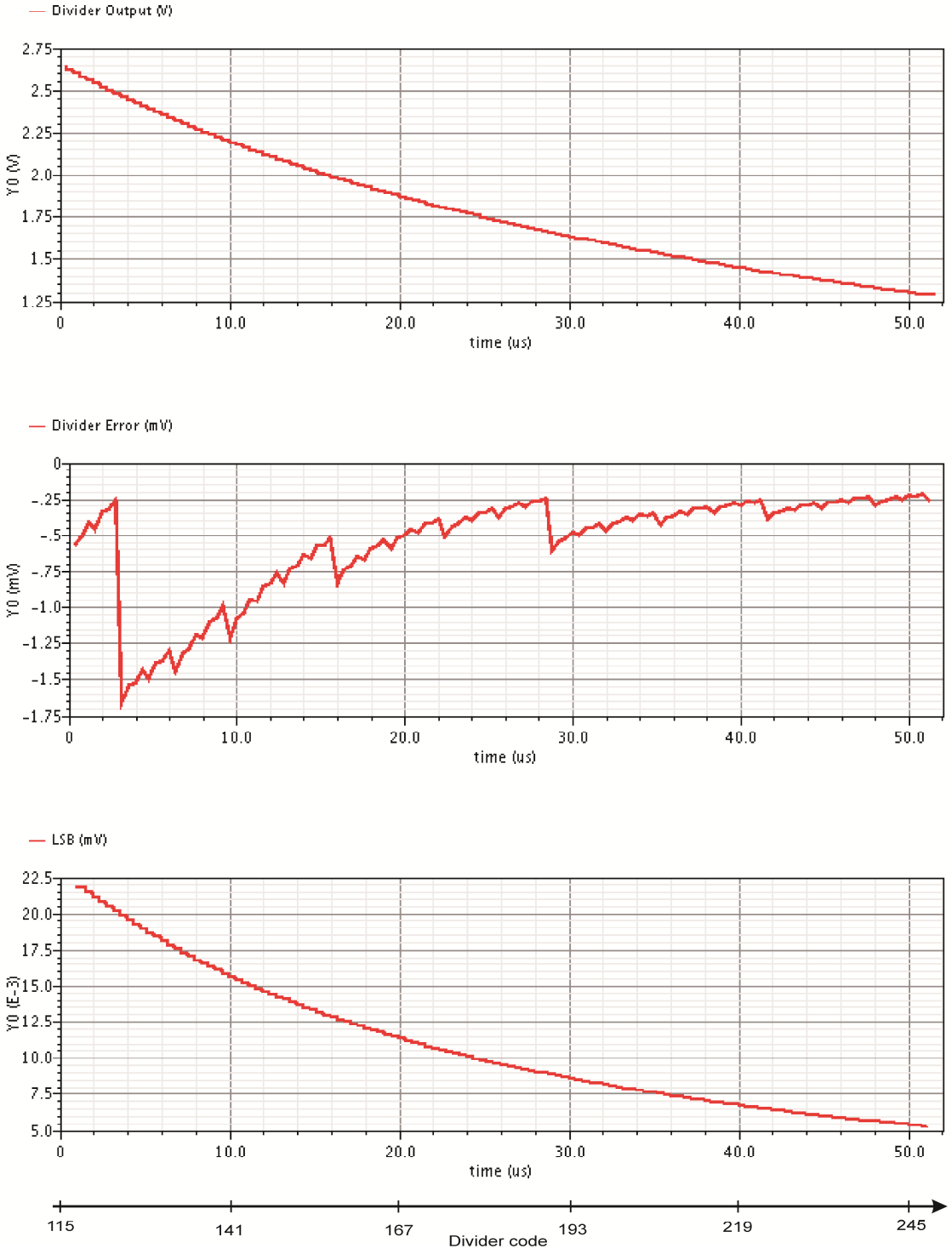


Figure 7. 8 Digital divider output waveforms for denominator range from 120 to 250; output voltage (top), divider error (middle) and LSB size (bottom)

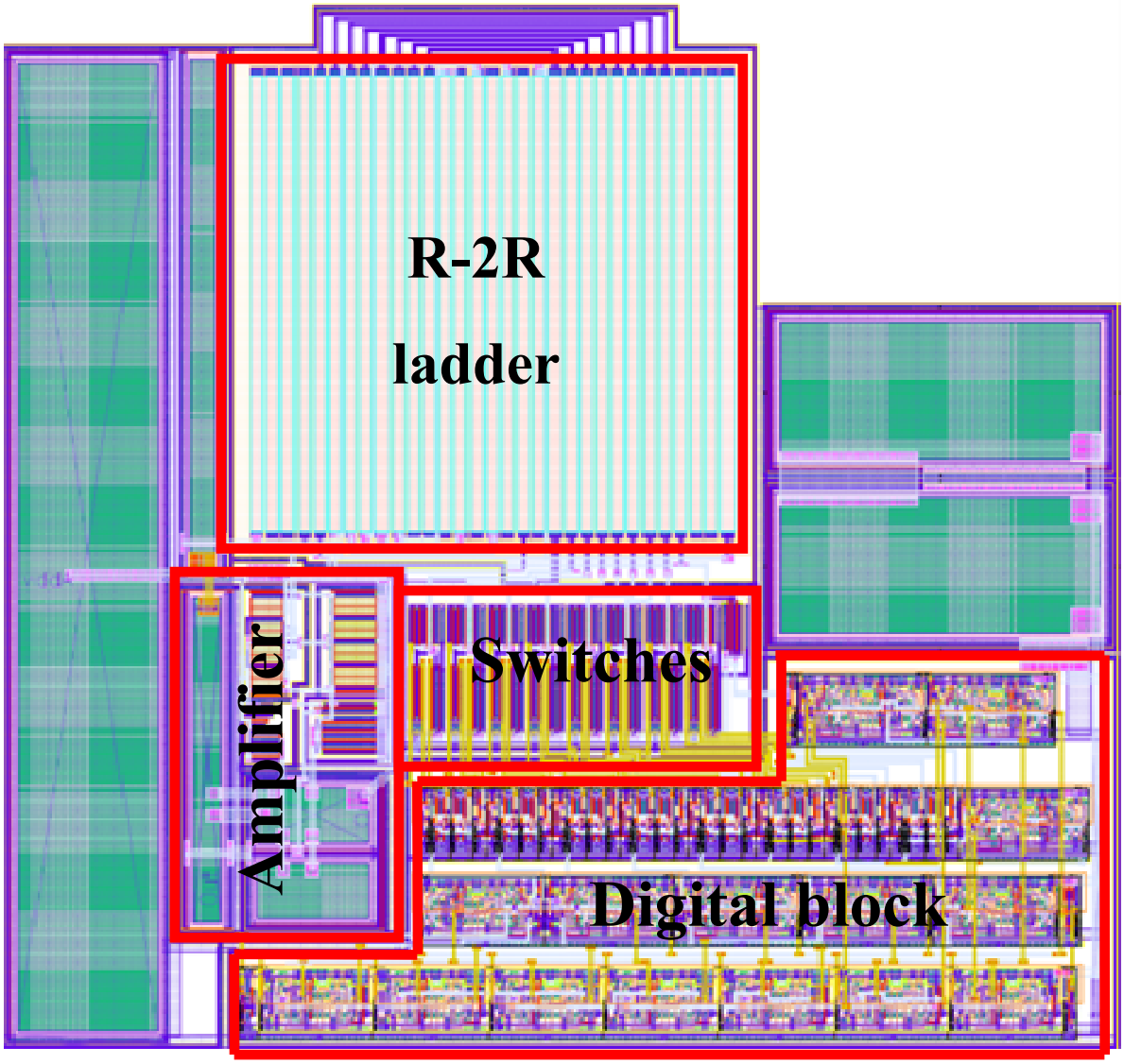


Figure 7. 9 R-2R divider layout

7.3 Successive approximation register analogue-to-digital converter

The analogue to digital converter (ADC) has been introduced for the digitisation of the signals that determine the duration of the OFF time. The resolution, DNL and INL are set by the overall system requirements. The most stringent property of the system is the absolute value of the output current, with a maximum allowable error of 1%. This error is comprised of the quantisation error and ADC nonlinearity. Considering a maximum nonlinearity of 1LSB, the resulting requirement for the resolution of the ADC is 8 bits (1LSB = 0.4% of FSR).

Converter architecture

Given the resolution of the system, an 8 bit successive approximation register converter with R-2R DAC will meet the requirements. The acquisition and conversion time is limited

by the double sampling algorithm to a total of 450ns (see Fig. 7.3). Thus, the acquisition time is set to 50ns, resulting in 400ns for the 8 bit trials of the conversion process.

As the acquisition time is limited, the signal has to be buffered in order to allow full settling within 50ns into the sample and hold (S&H) block. The signal buffer must show a unity gain bandwidth greater than 20MHz to allow 6 time constants settling within 50ns. The buffer is based on a folded cascode with Miller output stage architecture, with DC gain over 80dB. The time constant of the switch ON resistance and sampling capacitor is 6ns (R_{ON_SW}=2kΩ and C_{SAMPLE}=3pF). An additional half-size dummy switch (actuated in anti-phase) has been added to cancel the charge injection and clock feedthrough of the sampling switch.

The offset of the converter caused by the signal path buffer, comparator and DAC reference buffer is digitally trimmed with the aid of the fourth input of the multiplexer connected to $V_{REF}/2$. Additionally, the offset and the gain error can be evaluated through the V_{IN} or V_{OUT} inputs of the multiplexer. The trimming of the offset is done digitally with the aid of an offset register that is added to the result of each ADC conversion, while the gain error is trimmed through the reference voltage of the ADC.

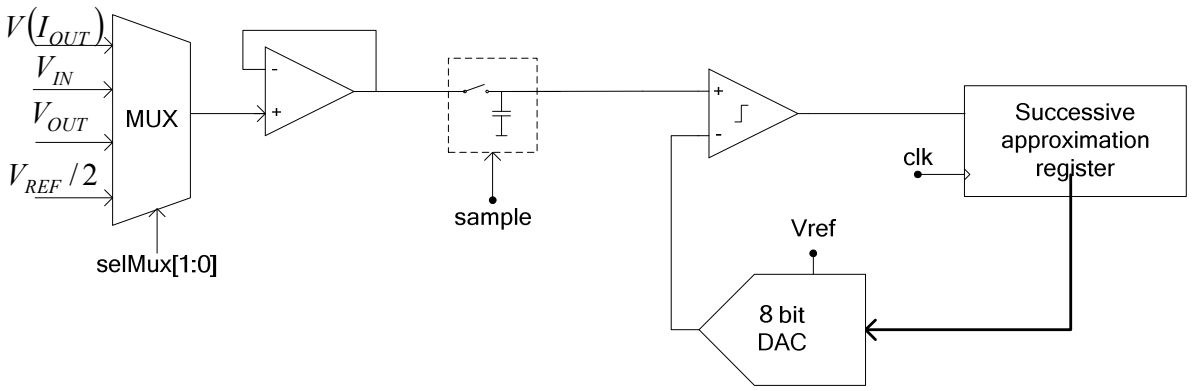


Figure 7. 10 Successive approximation analogue to digital converter architecture

The comparator is built as a high gain two-stage preamplifier followed by a current comparator, as previously described in section 5.3.6. A latched comparator could be used as an alternative, but the overall performance of the converter would be still dominated by the DAC and comparator pre-buffer.

An R-2R topology has been selected for the DAC topology as is provides good performance and low die area. Figure 7.11 presents the diagram of the R-2R DAC. The unit resistor value has been set to 12.5kΩ for settling requirements. The reference buffer bandwidth is set to over 20MHz to allow full settling after 50ns, similar to the sampling buffer.

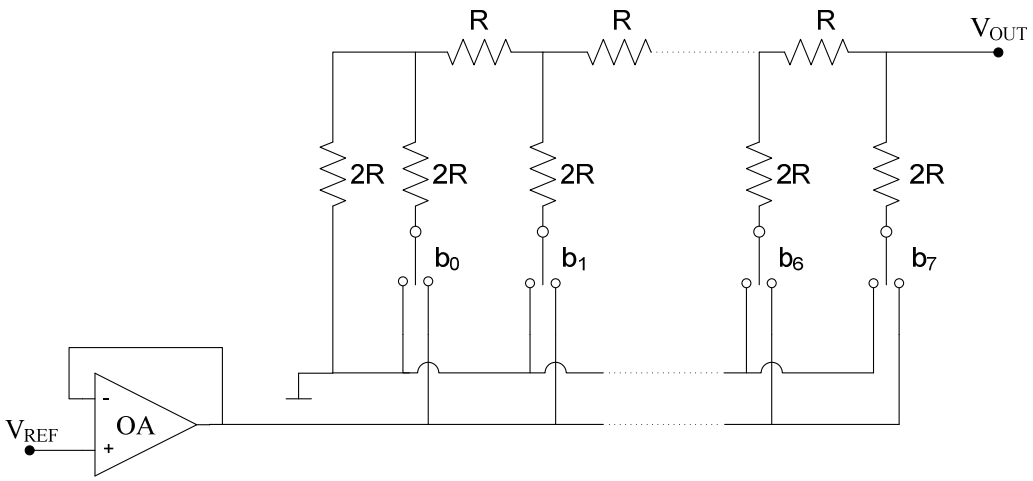


Figure 7. 11. R-2R DAC architecture

The main accuracy of the ADC is limited by the following factors: matching of the resistors, matching of the switch ON resistances, settling of signals within 50ns (settling to 6τ) and noise of the comparator/amplifiers. In the following discussion the noise of the comparator and amplifiers will be ignored due to the large size of the LSB (1LSB = 4.88mV). Figure 7.12 presents the error of the DAC after 50ns from a code transition. This includes the systematic error due to the switches and the settling error of the resistive ladder and DAC reference buffer.

The expected INL of the DAC has been evaluated by statistical simulation (device mismatch over the process corners) showing a maximum value of 0.75LSB. The maximum nonlinearity and DNL point is observed at the transition of the MSB (as is commonplace in many DAC architectures) due to the mismatch between the equivalent resistance of the resistor elements for first 7 bits and the single one of the MSB. Figure 7.13 shows the statistical results of the INL for a set of 100 runs.

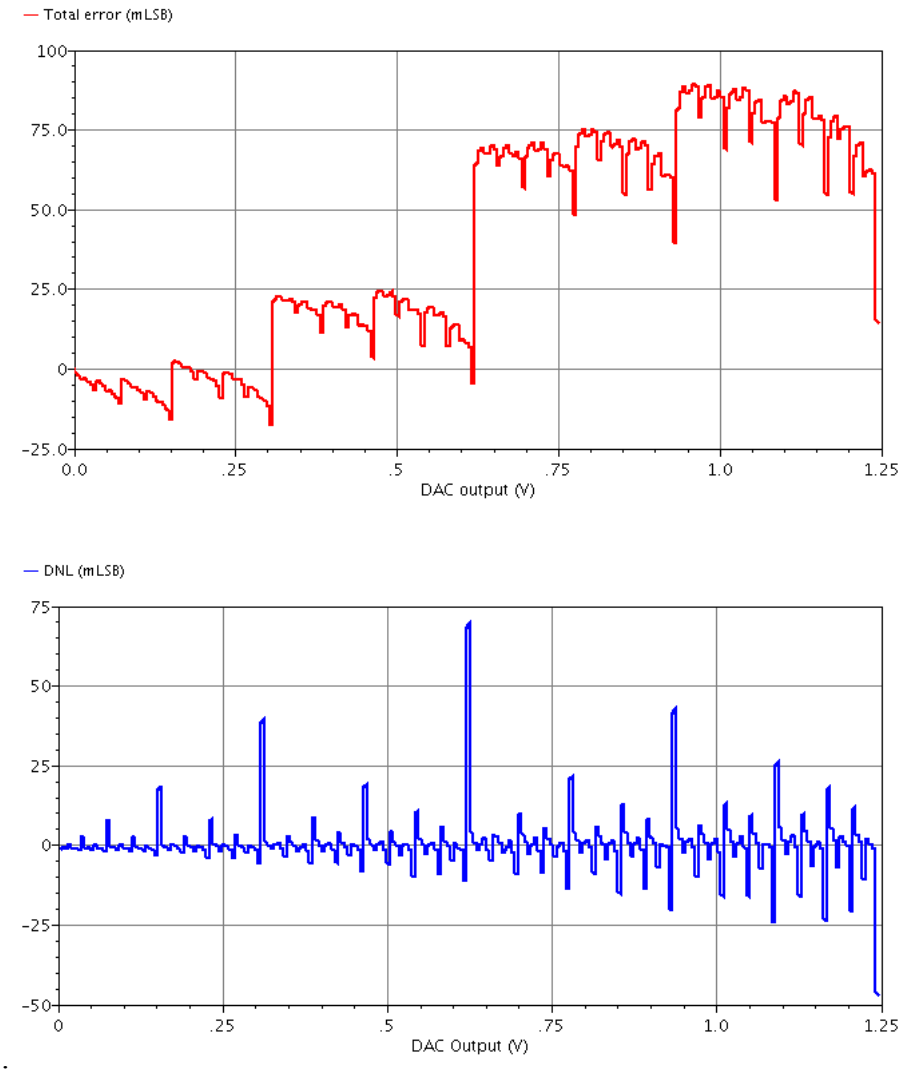


Figure 7. 12. R-2R DAC nominal error simulation results after 50ns from code transition: top - total conversion error (nonlinearity and settling error); bottom - differential nonlinearity error

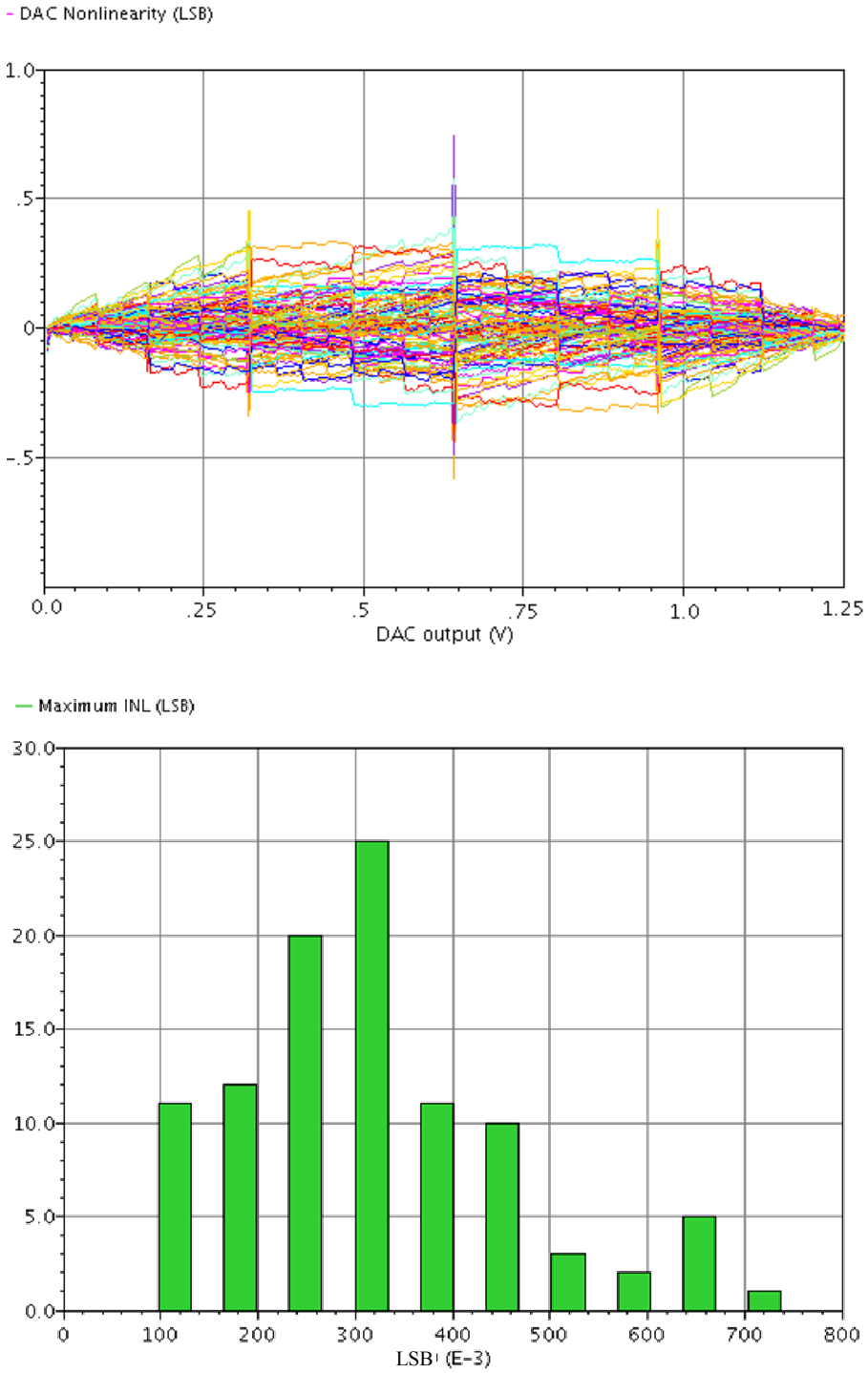


Figure 7. 13. Statistical simulation results for the DAC nonlinearity;
top – variation of the nonlinearity over the full scale range
bottom – histogram of the nonlinearity magnitude

The layout of the ADC is presented in figure 7.14, with the main block highlighted. The dimensions of the converter including the sampling block are 260µm×230µm. Standard AMS library digital cells have been used, hence the large size of the digital block.

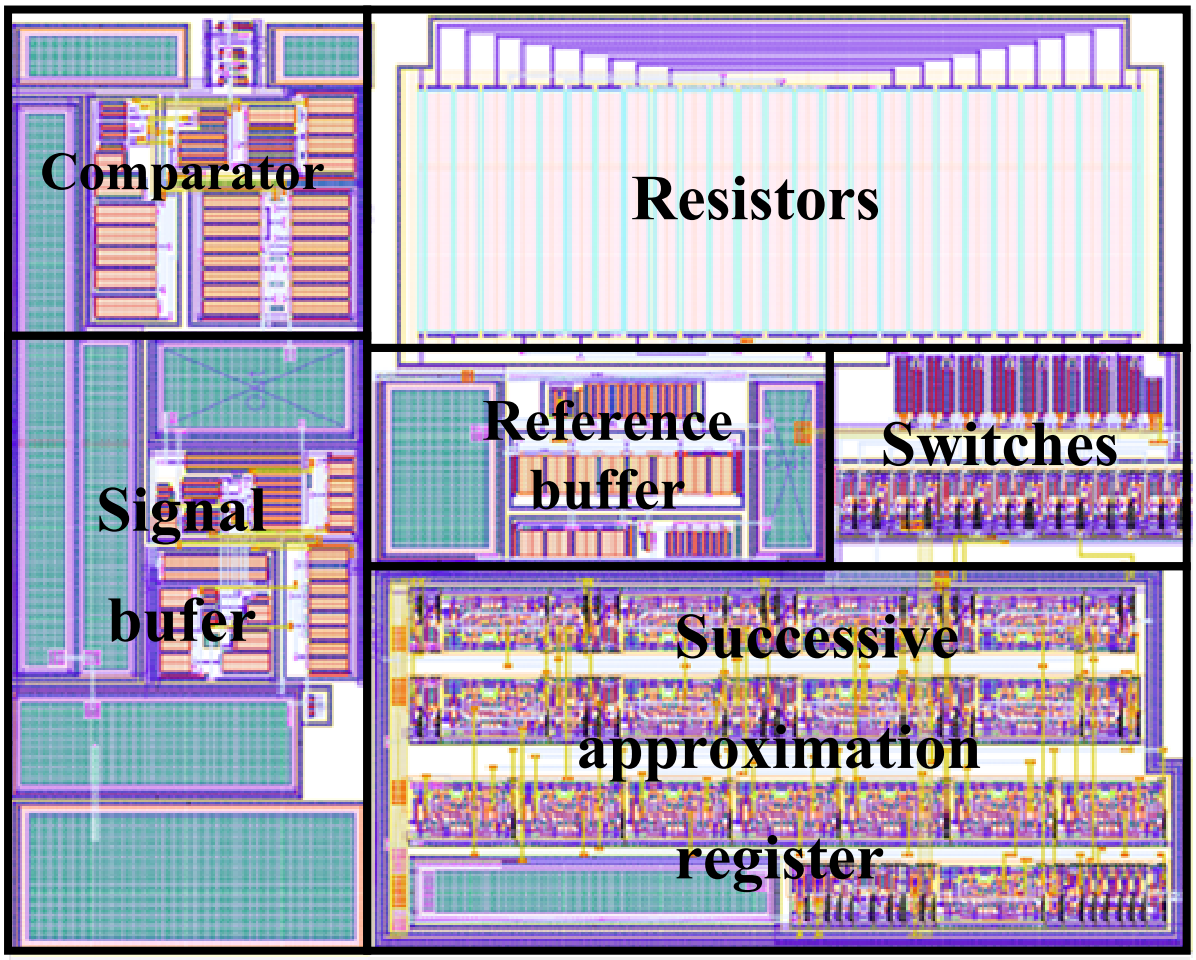


Figure 7. 14 Analogue to digital converter layout

7.4 ADC and divider control logic

To increase the flexibility of the system, the digital block is intended to be implemented off-chip. This allows the user easily switch between the two different OFF-time estimation algorithms, and also to optimise the system to suit specific requirements. From a digital perspective only, the system is presented in figure 7.15.

The divider uses a Serial Input Parallel Output (SIPO) data register to hold the denominator value, which is updated during each OFF cycle using the serial input. The clock signal is shared between the divider and the ADC itself, as the same number of bits is required for the A-to-D conversion as for the update of the DAC register. The ADC and the divider are activated by the rising edge of the clock, but the divider serial input data is updated on the falling edge to avoid register metastability.

In the digital block, the ADC and divider interface module is responsible for generating the clock and control signals, as well as reading from the ADC output and writing to the divider register. The operation of the interface module is described in the following section

with the aid of the algorithmic state machine (ASM) diagram, and the plot of the main waveforms presented in figures 7.16 and 7.17, respectively. The Verilog code for the ADC interface is attached in appendix 12.

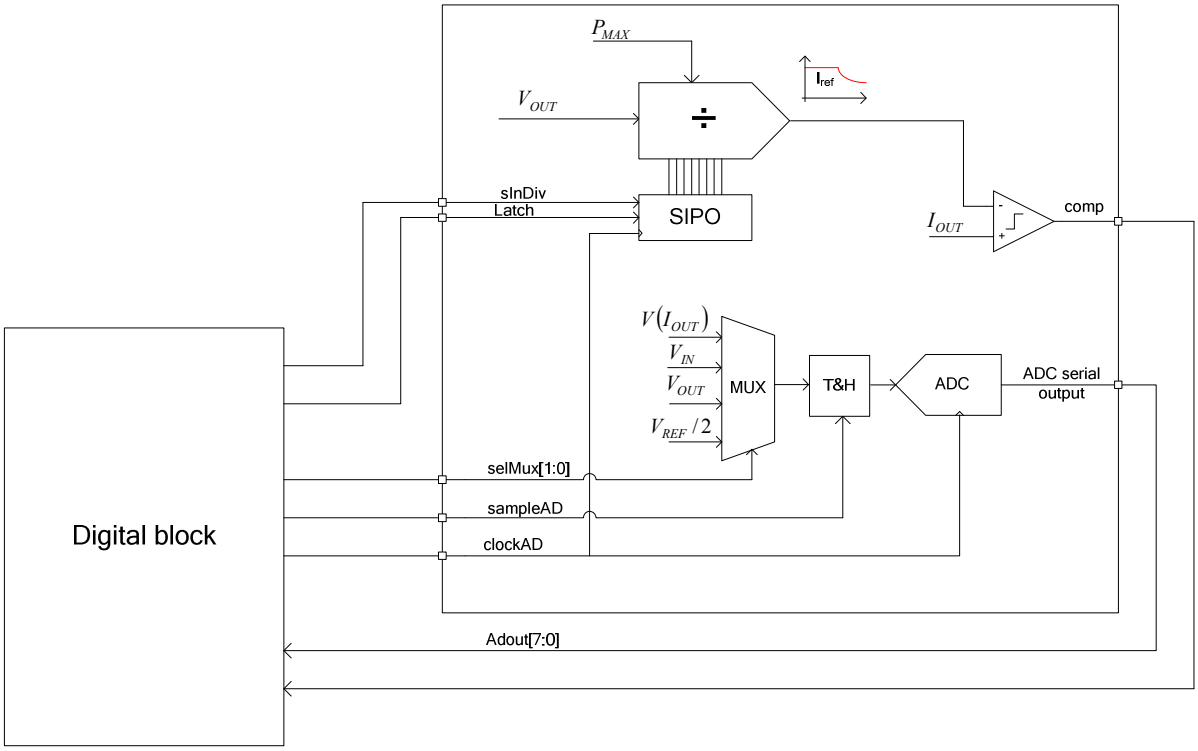


Figure 7. 15. Block diagram of the digital signal path

The ADC and divider control logic have two main states corresponding to the operation of the ADC, i.e. sampling and conversion. Once in sampling state, the converter starts to count until the minimum sampling time is reached and sets the *ready* flag afterwards. The *ready* flag then triggers the start of the analogue to digital conversion. When the start of the A-to-D conversion signal is triggered, the clock divider is initiated and the logic switches to conversion state.

In the conversion state, a counter (the clock divider) measures the number of system clock cycles (N) within half a period of the ADC clock. During the OFF cycle, on the falling edge of the ADC clock, the controller updates the divider input and latches the result during the 8^{th} clock cycle. On the rising edge of the ADC clock the result of the bit trial is saved into a shift register. After eight ADC clock cycles the controller switches automatically into sampling mode, waiting for the next A-to-D conversion trigger.

Figure 7.17 presents the waveforms of the logic module for two ADC conversions. The first conversion takes place at the end of the ON phase (state 1 → 0). The system has previously sampled the sense current (SelMux = 0). The result of the A-to-D conversion (83

in this example) is stored in the *ADout* register after the 8th clock of the ADC. The controller toggles the multiplexer input to the *Vout* signal, switches to tracking mode and then waits for the start of the next ADC conversion. The second conversion is triggered by the start of a new ON phase (state 0 → 1) and the process repeats, with the exception that the divider register is not updated during the ON cycle.

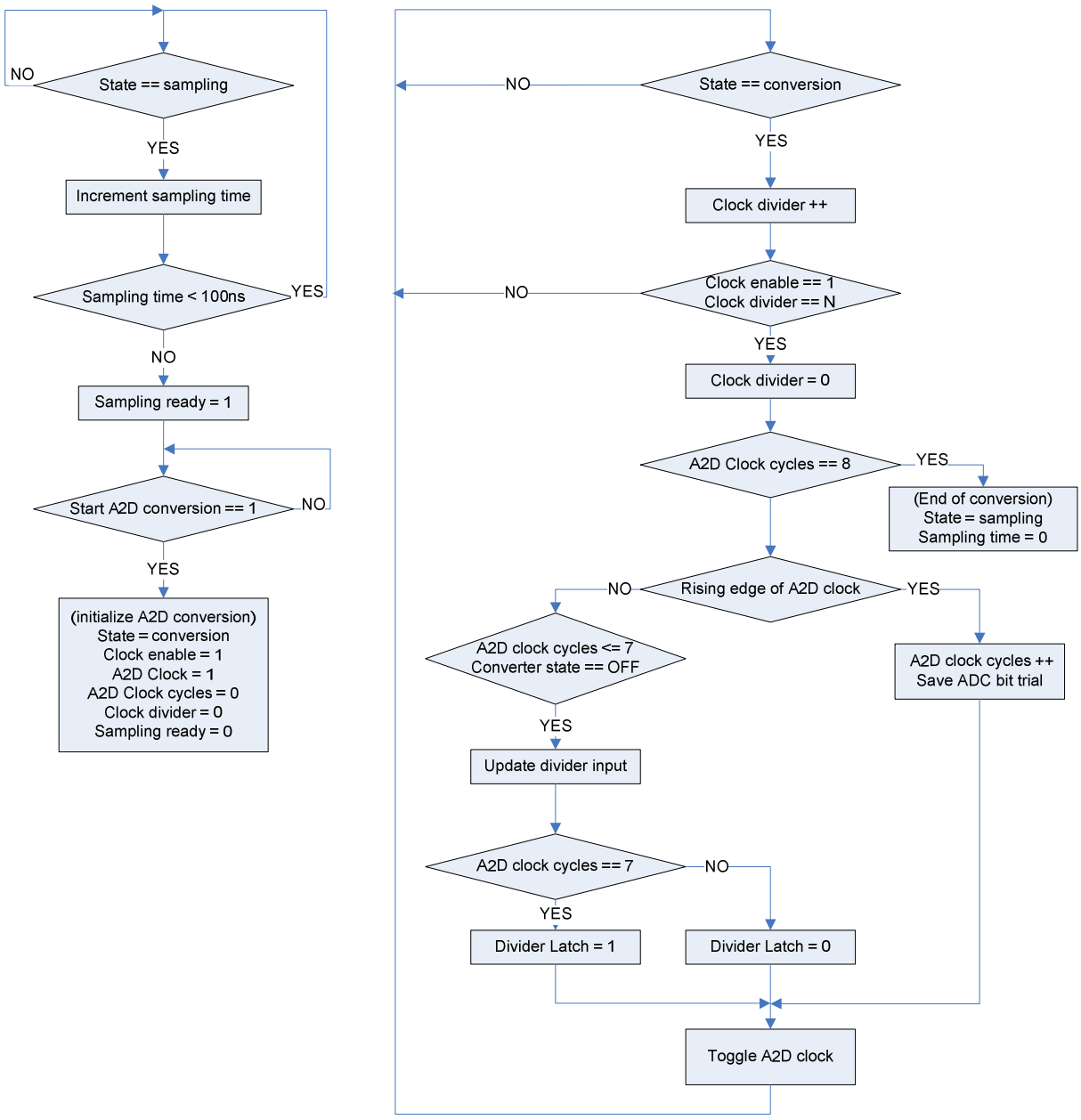


Figure 7. 16 ASM chart for the ADC and divider controller

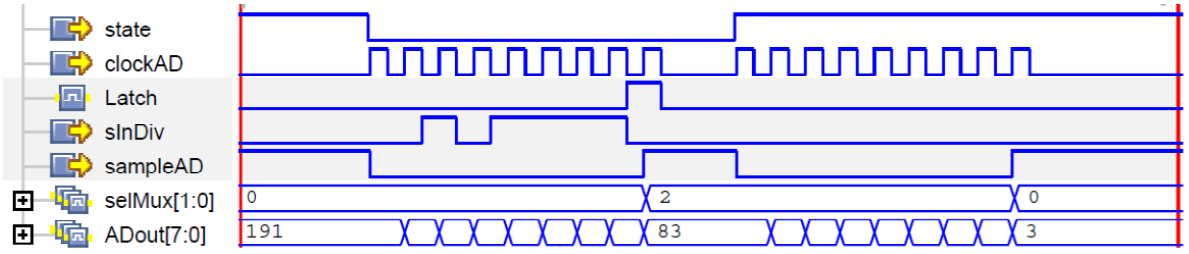


Figure 7. 17 Simulation waveforms for the ADC and divider interface

7.5 OFF time estimation loop control logic

The operation of the digital controller is based on the system operation described in chapter 7.1 and waveforms from figure 7.2 are repeated here for convenience in figure 7.18. During each ON cycle the ADC has two tasks. In the first part, it will convert the previously sampled signal, V_{IN} or V_{OUT} (alternated every cycle). In the second half of the ON cycle it will track the voltage on the sense resistor and sample it at the end of the ON cycle. During the OFF cycle the converter will complete the conversion of the signal corresponding to the output current and sample the signal corresponding to V_{IN} or V_{OUT}, alternatively.

In order to determine the duration of the OFF cycle the controller will integrate the value of $V_{in}\frac{N_S}{N_P} - (V_o + V_D)$, compute the error, and recalculate the duration of the next OFF cycle, as described in the previous chapters.

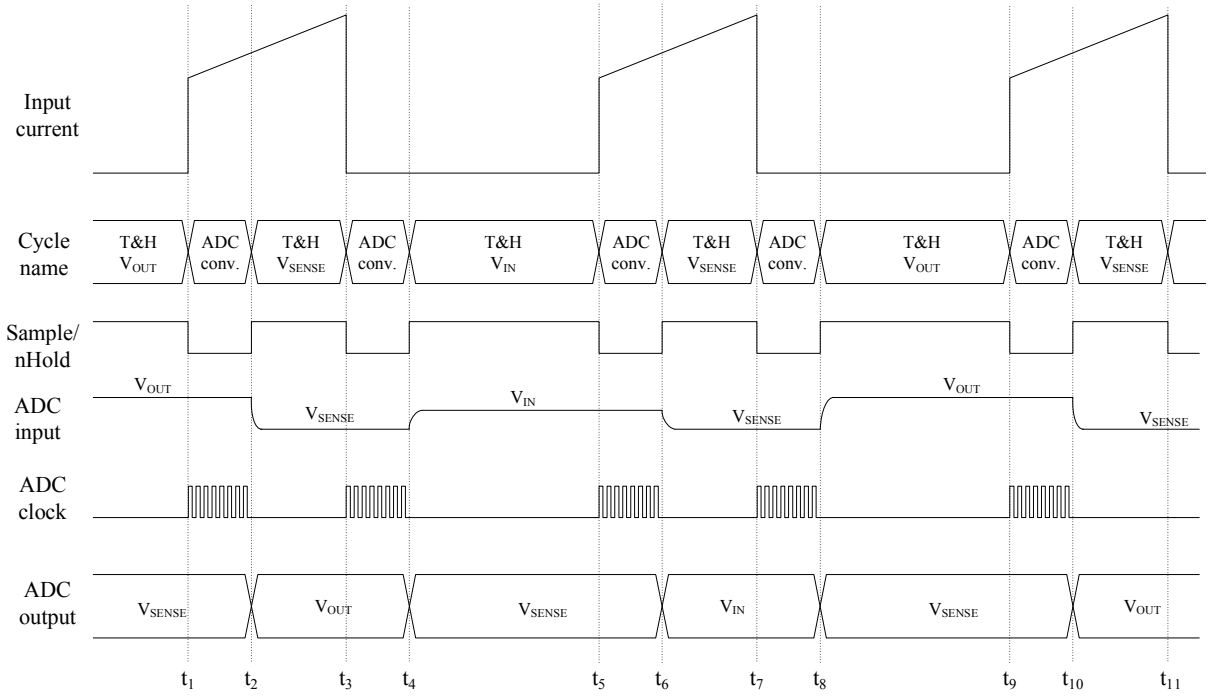


Figure 7. 18 *OFF time* algorithm main waveforms

In the following discussion, the operation of the OFF time estimation digital block is described with the aid of the ASM charts from figure 7.19. Two main states define the operation of the system, ON and OFF. The operation of the converter is conditioned by the *enable* signal, activated at the beginning of the charging cycle and cleared when the output voltage reaches the preset threshold. Before the controller starts cycling through the ON and OFF states, the registers are loaded with the default values during the initialise phase, triggered by the rising edge of the *enable* signal. During this cycle, the digital module also loads the trimming registers for capacitors and resistors. Afterwards, the controller goes into the OFF state, measures the input voltage and then switches to the ON state.

During the ON state the controller integrates the value of $V_{in}\frac{N_S}{N_P} - (V_o + V_D)$ according to the algorithm previously described, by means of successive summations. Once the ADC completes the conversion triggered by the previous OFF cycle, the result is stored and the converter starts sampling the signal corresponding to the output current. The system waits in this state for the rising edge of the comparator signal, indicating that the output current has reached the threshold and the ON cycle is complete.

During the OFF cycle, similarly to the ON state, in the first stage the controller checks for the completion of the ADC conversion. Once the ADC result is available, if the previous signal converted was *Vsense*, the algorithm compares the value of the output current to the over-current threshold. If the value exceeds the threshold, the duration of the OFF cycle is increased by 5us, to allow a quick recovery of the system. If output current is within the defined limits, the duration of the OFF cycle is updated with the error signal, according to the '*ON time integration algorithm'*. At the end of the cycle, when the OFF time counter value equals the previously calculated OFF time duration (greater than the minimum off time), the controller switches to ON state and start a new A-to-D conversion of the signal Vin or Vout. The Verilog code for the digital controller is attached in appendix 13.

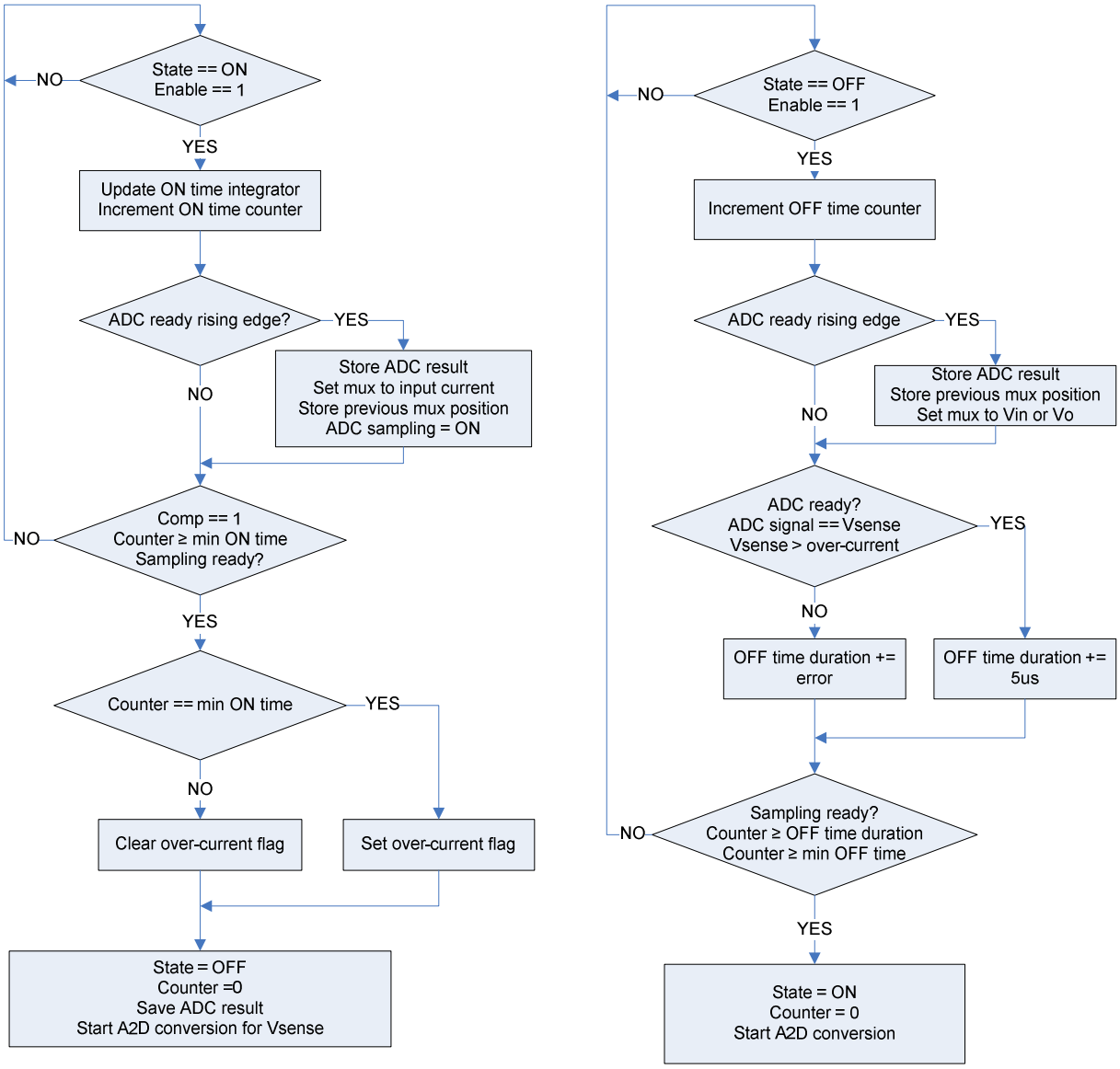


Figure 7. 19 Simplified ASM chart for the digital controller

7.6 Simulation results

Figure 7.20 presents the start-up sequence of the mixed signal implementation of the converter. The start-up represents the most demanding part of the cycle for the control logic as the OFF time duration has to be adjusted quickly from a minimum value (approx 500ns, during the current ramp from 0 to 30A) to a steady state value, after the output current reaches the threshold value. In particular, when the load voltage starts from zero volts, the OFF time duration is at a maximum value (over 20μs). As the loop time constant is larger than a few microseconds, which is required for the converter to make the transition from 500ns to 20μs, the output current can significantly exceed the reference current (30A) and destroy the switches and transformer.

This problem has been overcome by monitoring the output current with the aid of the ADC. When the output current exceeds 31A the increment of the OFF time duration is significantly larger, allowing the output current to decay at a faster pace. This region can be observed during the start-up process (figure 7.20) between 40µs and 200µs. After the settling of the output current, the OFF time duration drops slowly until the current ripple reaches 1A, this can be observed in Figure 7.21.

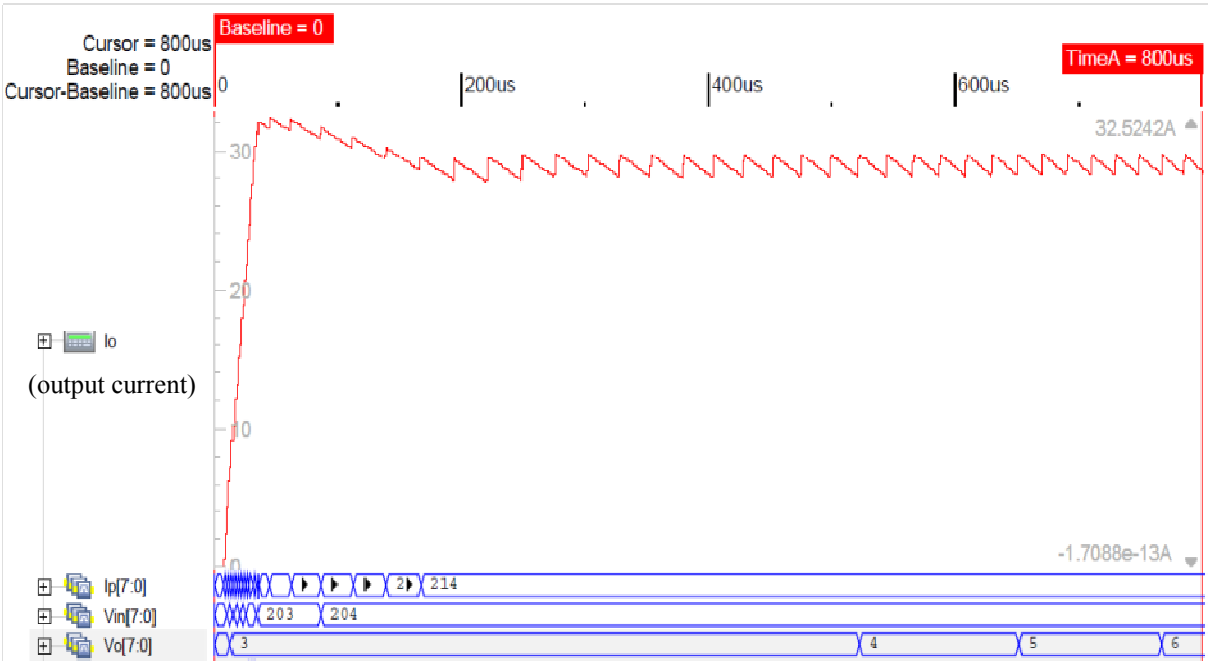


Figure 7. 20 Converter start-up simulation from VOUT=0V;
I_O – output current; I_P[7:0] – output current measured from the primary register
Vin[7:0] – input current register; V_O[7:0] – output voltage register

Figure 7.22 shows a zoomed-in portion of the waveform from figure 7.21, highlighting the regulation of the OFF time register and the *error* signal. As the ripple of the output current drops, the value of the error decreases towards zero.

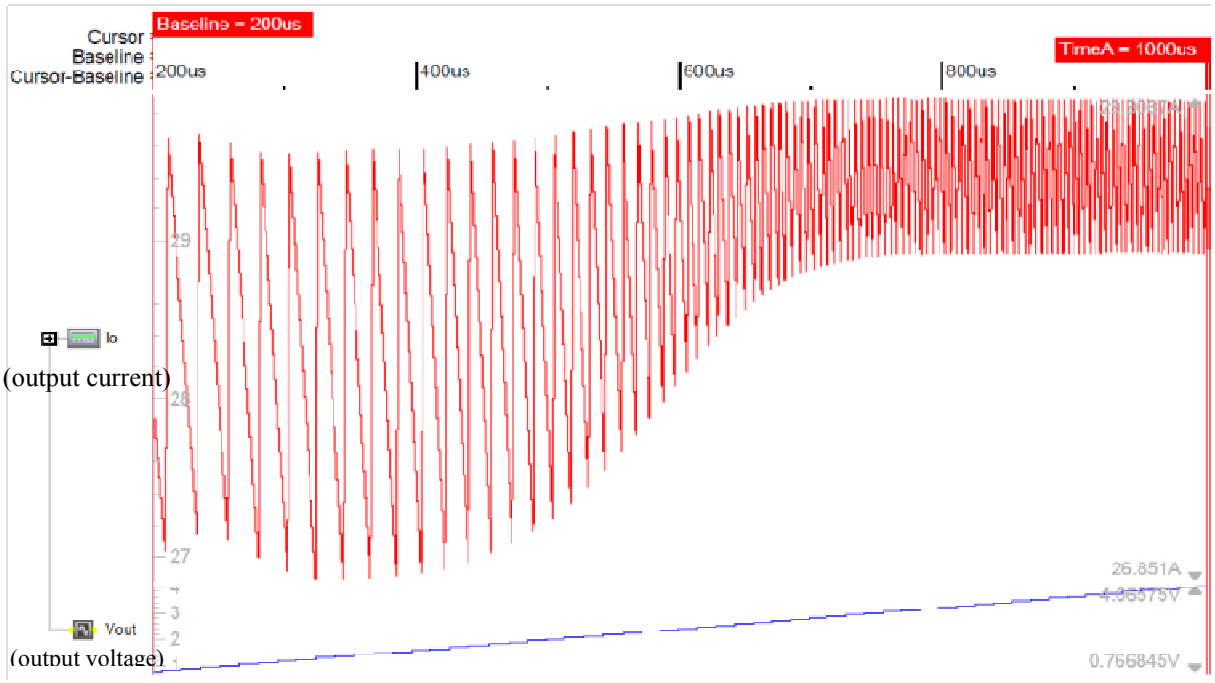


Figure 7. 21 Simulation of output current settling after start-up
Io – output current (red trace); Vout – output voltage (blue trace)

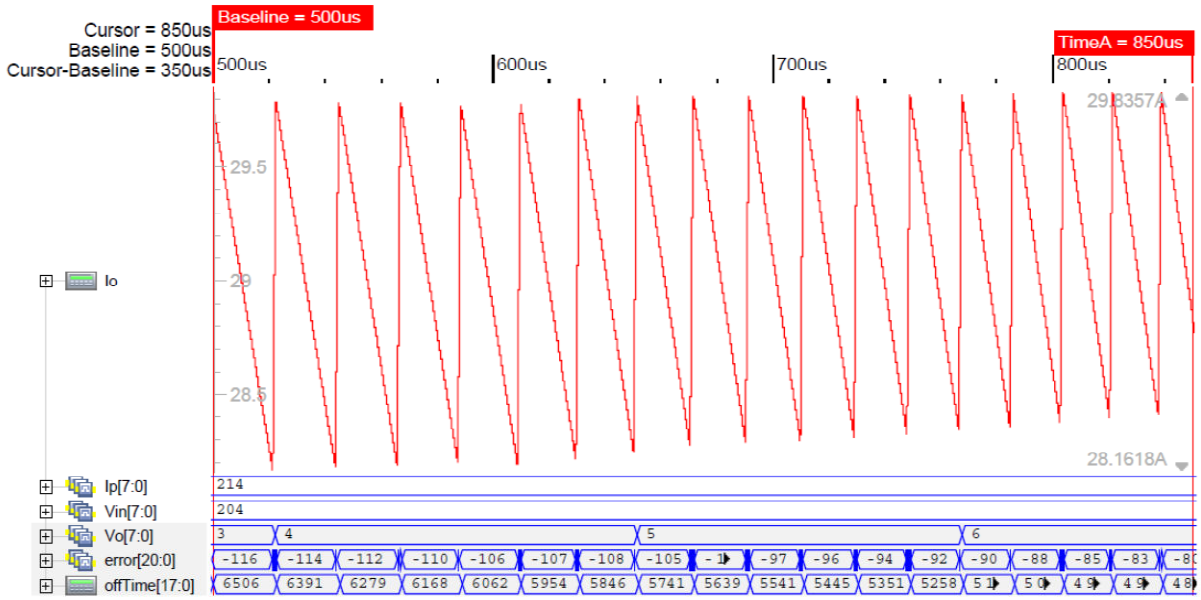


Figure 7. 22. Zoomed-in region of figure 7.21, highlighting the error and OFF time register values; Io – output current (red trace) ; I_P[7:0] – output current measured from the primary register; Vin[7:0] – input voltage register; Vo[7:0] – output voltage register; error[20:0] – error register; offTime[20:0] – OFF time duration register

In order to simulate the behaviour of the converter with an EDLC load, the duration of the transient simulation would be between hundreds of milliseconds to tens of seconds (depending on the load size. This is unfeasible from the simulator point of view and a smaller capacitive load has been used instead (10mF), in a similar way as used for the analogue system. The smaller load brings the benefit of a faster load voltage change and therefore poses higher stress on the OFF time regulation loop. Even with the smaller load, the full charging

cycle from 0 to 16.2V could not be captured into a single transient simulation and has been split into two overlapping fragments: 0 to 9V and 8V to 16.2V depicted in figure 7.23 and 7.24, respectively.

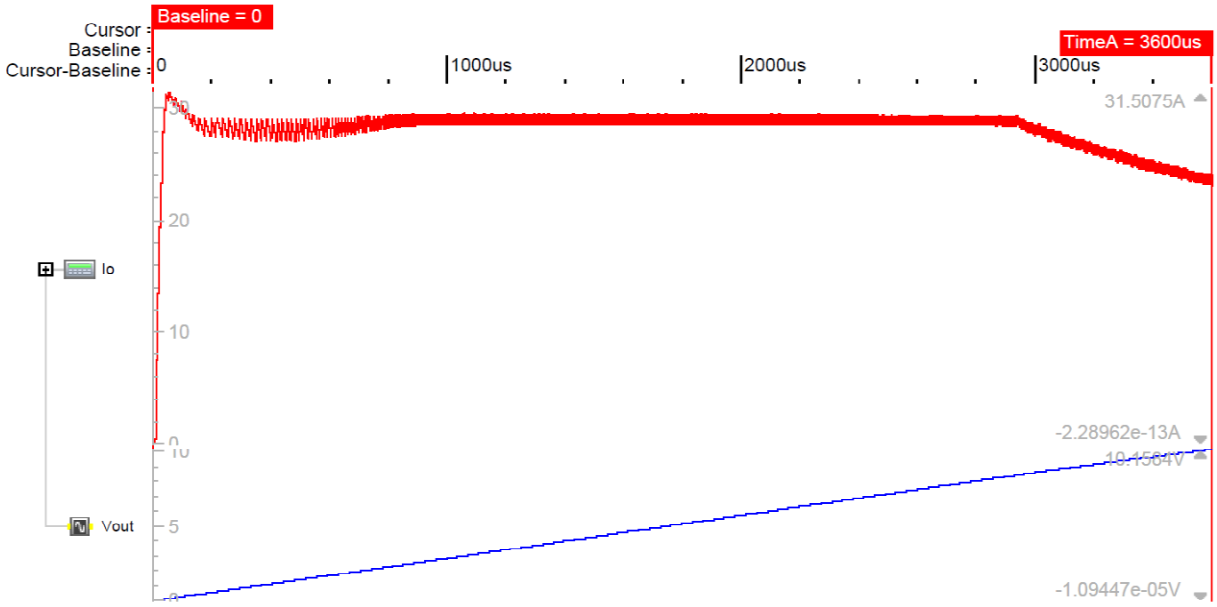


Figure 7. 23 Simulation of load charging from 0 to 9V;
Io – output current (red trace); Vout – output voltage (blue trace)

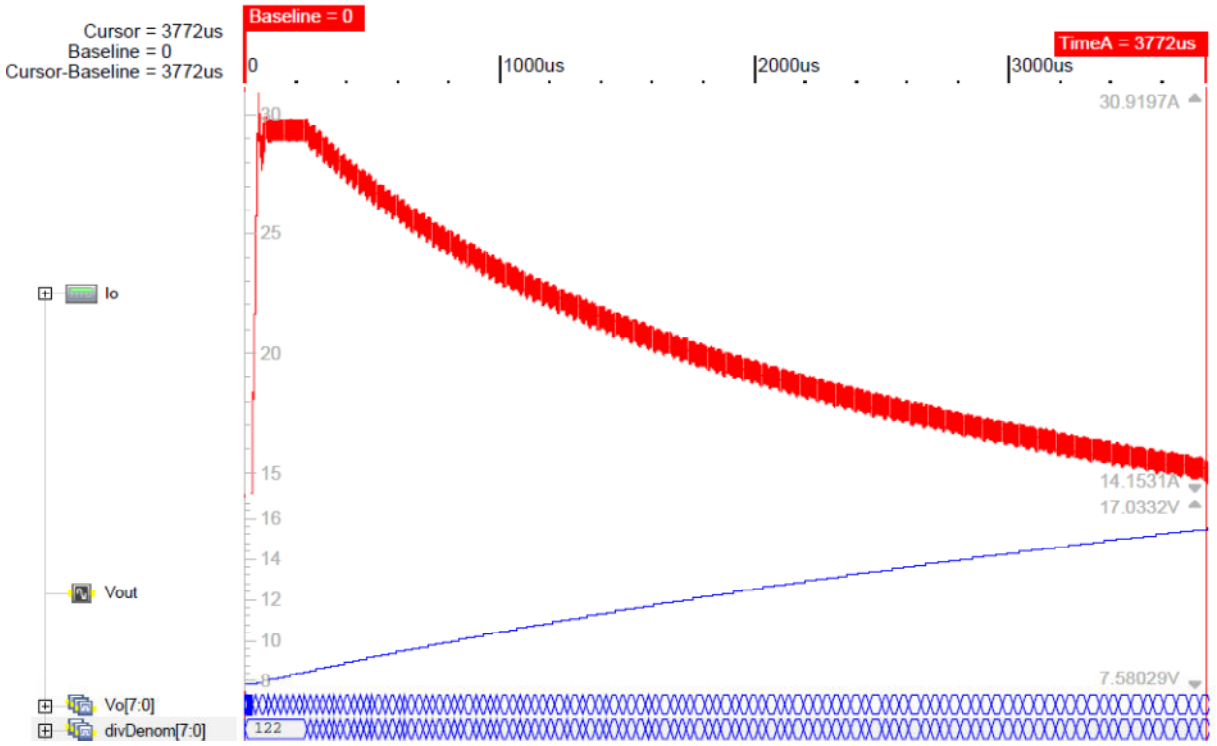


Figure 7. 24 Simulation of load charging from 8V to 16.2V;
Io – output current (red trace); Vout – output voltage (blue trace);
Vo[7:0] output voltage register; divDenom[7:0] – R-2R divider denominator register

Compared with the fully analogue system, the profile of the output current from 8.4V to 16.2 is marked by the steps of the DAC divider. The divider output cannot be filtered as the time constant would have to be in the order of hundreds of microseconds (to cover several on/off cycles). Thus, the transition from one divider code to another is a stability test for the converter, especially when loaded with 10mF. Figure 7.25 presents in detail the first steps (the largest steps) of the output current when the system enters the power limitation regime (8.4V), with the divider denominator code shown at the bottom of the plot. Figure 7.26 shows the simulated start-up current profile when V_{OUT}=8V.

Even though the Verilog code has been developed at RTL level, the synthesis of the logic and evaluation of the system with an FPGA were not possible within the timescales of the project. As the regulation algorithm has been verified within the system in the analogue IC implementation and the breadboard evaluation, it is expected with a high level of confidence for the mixed signal platform to be functional.

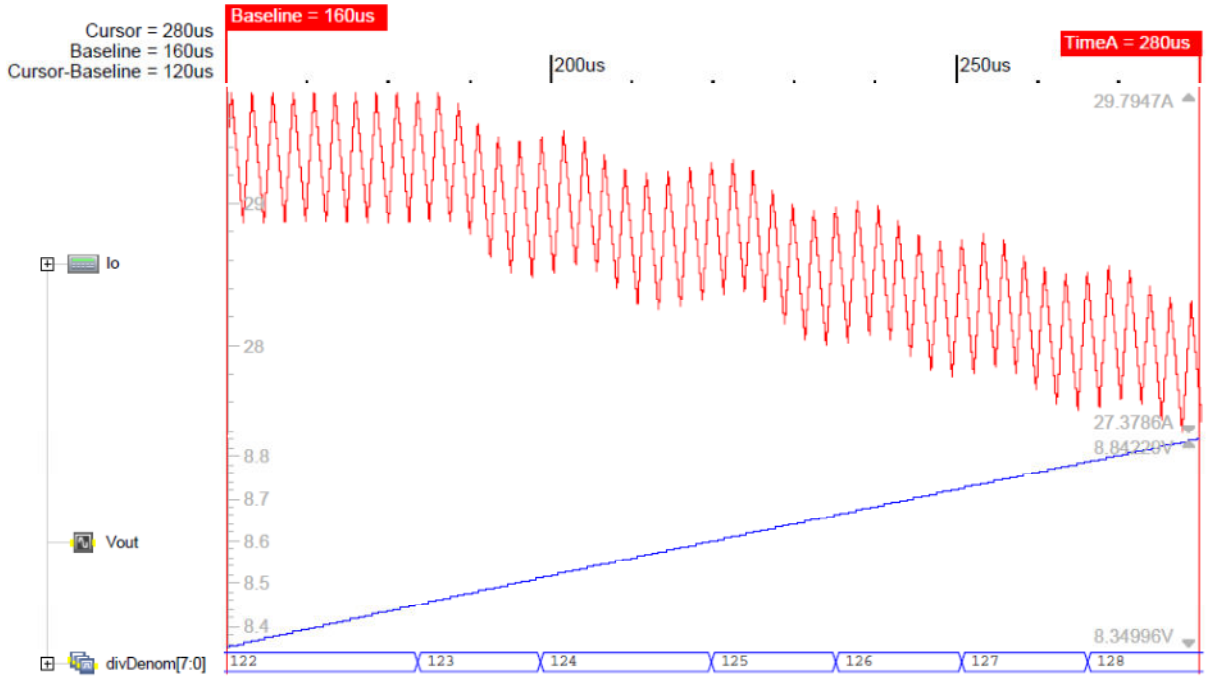


Figure 7. 25 Detail representation of the simulated output current steps when entering power limitation regime; Io – output current (red trace); Vout – output voltage (blue trace); divDenom[7:0] – R-2R divider denominator register

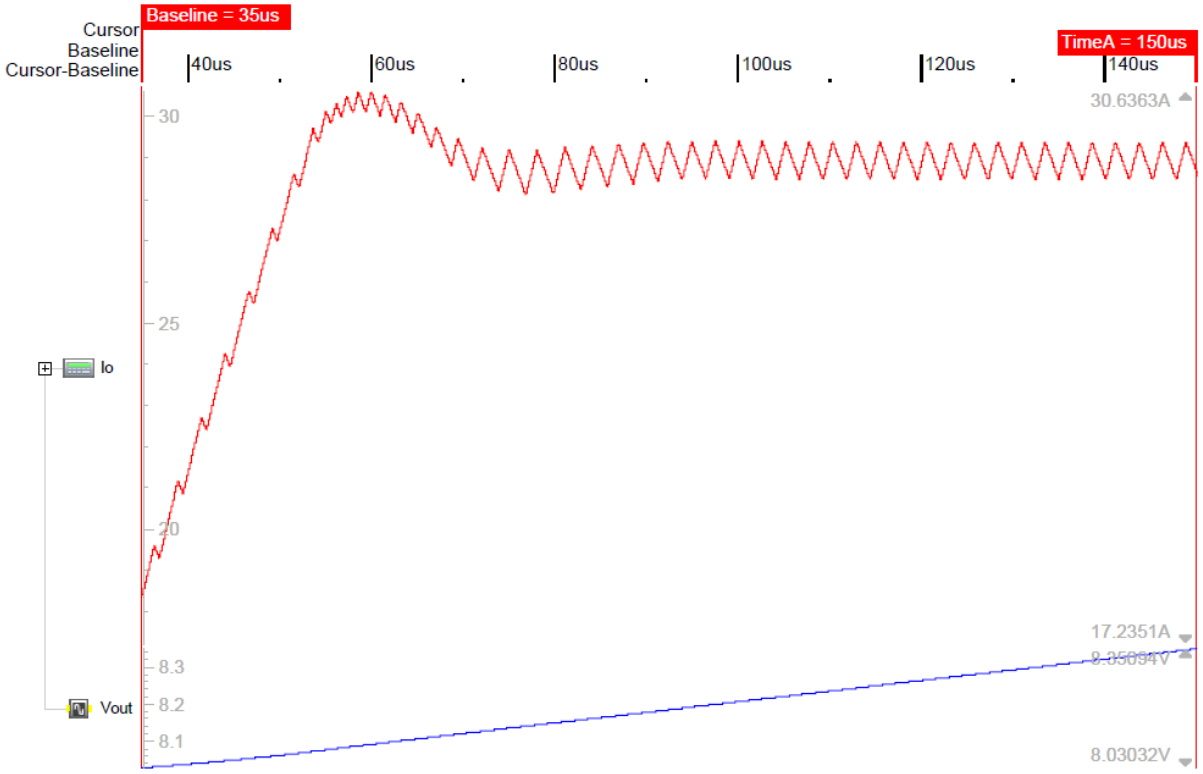


Figure 7. 26 Detail of the simulated circuit start-up for V_{OUT}=8V;
Io – output current (red trace); Vout – output voltage (blue trace);

Chapter 8 CONCLUSIONS AND FUTURE WORK

This thesis has presented the design and implementation of novel charger architectures for ultracapacitors starting from the application requirements, algorithm development, breadboard testing, analogue IC architecture design, circuit design, layout, verification and IC evaluation.

The combination of constant current and constant power output characteristics allows a very fast charging of the EDLCs while the size of the complete charger system remains compact. The push-pull converter has been identified as most suitable conventional architecture for the following reasons: low side switches in the input circuit, continuous output current, medium output power, galvanic insulation and flexible current sensing scheme. The control algorithm features a choice between two new OFF time estimation circuits based on fast feed-forward and a slow feed-back loop that together compensate for the fluctuations in the mains network and the tolerances of the components. These algorithms allow an accurate monitoring and regulation of the output current without the need of a sensing resistor in the secondary side. The variable frequency algorithm enhances the converter by always operating at the minimum frequency required, thus minimizing the losses and boosting the efficiency. The control algorithms, designed specifically for EDLC charging, exploit a fundamental property of this load, the slow variation of the load voltage. The low frequency load voltage variation makes it possible for the feedback loop to regulate the current by calculating the error figure over successive cycles.

The sensing of the output current from the primary side of the transformer removes the need of introducing current sense circuitry on the secondary side as is more conventional. Hence the losses associated with a low voltage, high current sensing arrangement are reduced. This approach also facilitates full galvanic isolation of the high-frequency signal and provides inherent over-current protection in the transformer.

The simulations and measurements of the breadboard circuit allowed us to adapt the circuit design so that it can cope with the non-ideal behaviour of the transformer and the main switches. The reliability of the device will strongly depend on the minimisation of the noise coupling, track impedance and the accuracy of the individual blocks.

The monolithic IC version brings the challenge of having large transient currents and voltages on chip, along with very accurate circuits, and fast switching logic, to be

implemented with a single metal layer and large parasitic capacitances. Special attention must be given to the power dissipation on chip and the optimisation of the switching losses.

The medium voltage analogue IC driver demonstrates the feasibility of the monolithic IC architecture and circuits. The matching simulations and practical measurement results prove the validity of the theoretical considerations and optimisation. The evaluation of silicon results with the real transformer has also tested the algorithm for the possible non-symmetry in the primary and secondary windings. Also, from a thermal point of view, it was possible to observe the heating of the magnetic components combined with the thermal inertia of the magnetic core.

Several basic cells were developed for this project with improved performance compared with previously published designs. The high accuracy current memory developed specifically for coarse geometry HV CMOS processes compensates for second order errors more evident in such devices, making possible the implementation of the system's signal processing in a compact current mode scheme suitable for a fully monolithic IC without compromising the performance of the regulation loop.

An enhanced current comparator design was developed that shows reduced quiescent current consumption and improved response time compared with the existing architectures. This has been used to advantage in both monolithic designs.

While the first and main part of the work has focussed on developing an analogue control system suitable for integration in a HV technology, it has also been recognised that there where the target technology is suitable, there are advantages in the use of a more digital implementation. Besides the higher level of integration, a major advantage is the potential flexibility of a digital control loop. The flexibility of a digital regulation loop lead to multiple advantages: scalability of the system and magnetic components, implementation of both OFF time regulation algorithms (input current sampling and ON time integration), trimming of the system parameters (output current ripple, transformer maximum flux density, supply voltage, etc.) and customization of the algorithm for specific types of magnetic cores, input switches, output inductor, etc. In this work, the digital part has been targeted towards off-chip programmable logic, but clearly full integration is desirable with some embedded control, possibly comprising a microcontroller and either flash or one-time-programmable memory.

The growth of portable electronic devices and electric / hybrid vehicles in the last decade has driven the development of the ultracapacitors and other novel energy storage devices. The recent research publications have presented EDLC devices energy density of up to half of the Li-Ion batteries can be achieved through different methods. Further

enhancement of the energy storage density is expected as the nanofabrication evolves, making the ultracapacitors a possible replacement for the Lithium – polymer batteries. In this context, the fast charging using low cost and compact systems becomes a key element.

The project has so far offered the foregoing conclusions, but there are many areas of continuing work that can be seen to arise and would benefit from further research. The paragraphs below describe the potential aspects that should be considered.

Smaller magnetic components could be used as the power dissipation measured is below the expected level. Further optimisation can be achieved by monitoring the temperature of the critical devices to prevent overheating, by allowing the transformer and inductor to operate at a higher temperature, closer to the maximum allowed temperature. Additionally a PWM controlled fan could be fitted to control the temperature of the system. This could be needed in cases where the charger is used quasi-continuously rather than in the more likely intermittent mode.

The reliability and heating of the ultracapacitors also needs to be looked at into finer detail, in order to determine the maximum ripple of the output current that can be tolerated. Operating the charger at maximum output ripple allows further optimization of the magnetic components size and losses.

The evaluation of the mixed-signal IC and digital synthesis of the Verilog code are necessary in order to prove the operation of the system. This architecture can be used to evaluate the operation of the charger with smaller magnetic components, as the parameters corresponding to transformer and the choke are contained in the digital block.

A commercial implementation would also require a step-down converter (from rectified mains) to power the control circuitry and the drivers. The trimming of the resistors could be implemented by using the sense resistor as a reference (usually 1-2% tolerance) and the RC time constant of the integrators could be tuned automatically by using an accurate external clock as reference, based on a dual slope integrator. Automatic trimming reduces the test costs and could potentially remove the temperature coefficient of the polysilicon resistors, thus ensuring a temperature independent RC time constant of the integrators.

A method that monitors individually the state of charge and health of each ultracapacitor would be required to detect damaged or shorted cells and prevent overcharging the rest of the stack. Also depending on the charge distribution a cell balancing system could prove to be useful to provide an even charging of each cell.

The OFF time regulation loop could also be effectively implemented using switched capacitors. This approach could improve the circuit noise especially for signal sampling and simplify the auto-zeroing of the amplifiers.

The error of the OFF time block could be digitized using a sigma-delta like architecture, given the slow variation of the output voltage and error. This implementation would save area and improve the low noise figure by means of digital filtering. This would give greater stability for the feedback loop by improving the signal to noise ratio.

Another aspect that could be considered is the galvanic insulation of the output voltage (V_O), which is currently achieved using a large resistor (>1MΩ). This could also be achieved by using a micro-transformer on chip. The benefit of such an implementation would be the reduced cost of on-chip transformer and large bandwidth of the output voltage signal.

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Appendix 1 Transformer design

Based on the equations presented in chapter 2.5 we can write the primary winding current as:

$$I_p(t) = \frac{V_{IN}}{L_{Pm}} t + I_{Lo} \frac{N_S}{N_P} + \frac{V_{IN}}{L_o} \left(\frac{N_S}{N_P}\right)^2 t - (V_o + V_D) \frac{t}{L_o} \frac{N_S}{N_P}$$

It can be observed that all the terms except the magnetisation current will decrease with the rise of N_P/N_S. Thus in order to minimise the conduction losses on-chip we have to aim for the maximum turns ration.

On the other hand, the output power of the converter can be written as:

$$P_O = 2D_{max} \times V_{INw} \frac{N_S}{N_P} I_O \eta$$

Where D_{max} is the maximum duty cycle, V_{INw} is the worst case input voltage and η is the efficiency of the converter measured at the output of the transformer.

For our converter we have defined D_{max}=0.45, I_O=30A, η=0.9 and V_{INw}=280V. Thus in order to provide an output power greater than 250W we must have:

$$\frac{N_P}{N_S} \leq \frac{2D_{max} \times V_{INw} I_O \eta}{P_o}$$

$$\frac{N_P}{N_S} \leq 27.12$$

The transformer secondary winding output voltage during the ON phase must be:

$$V_{sec} \geq V_{Omax} + V_D + V_{Lon}$$

Where V_{Omax} is the maximum output voltage (16.2V), V_D is the forward voltage drop on the output diodes (0.6V) and V_{Lon} is the voltage drop on the output inductor during the ON phase. The minimum voltage drop on the inductor during the ON phase is approximated to 2V. Thus the secondary voltage must be greater than 18.8V.

This condition must be fulfilled regardless of the input voltage, therefore:

$$V_{INw} \frac{N_S}{N_P} \geq 18.8V$$

$$\xrightarrow{yields} \frac{N_P}{N_S} \leq 14.89$$

The maximum turns ratio (N_P/N_S) for the specifications of this design is: N_P/N_S=14.

Core selection and maximum flux swing

The core selection is usually based on the value of the maximum output power and the operating frequency. We have selected the ETD39 core and N97 material.

As the core losses for ferrite increase at about 2.7^{th} power of the peak flux density and 1.6^{th} power of the frequency we have to establish first the maximum flux density for a certain temperature rise.

For the first design we have selected a maximum temperature rise of 50°C and the corresponding power loss for the core is:

$$P_{loss\_max} = \frac{\Delta T}{R_{th}}$$

$$P_{loss\_max} = 3.125W$$

Where ΔT is the temperature rise and R_{th} is the core thermal resistance.

The losses are usually assigned equally between the core losses and winding losses, thus:

$$P_{loss\_core} = 1.5W$$

$$P_{loss\_winding} = 1.625W$$

The maximum core loss per cm^3 is:

$$P_{loss\_core}/cm^3 = \frac{1.5W}{11.5cm^3} = 130mW/cm^3$$

The peak flux density for a core loss of 130mW/cm^3 is 95mT, as per figure A1.1 below. Thus the peak-to-peak flux density swing is:

$$\Delta B_{p-p} = 190mT$$

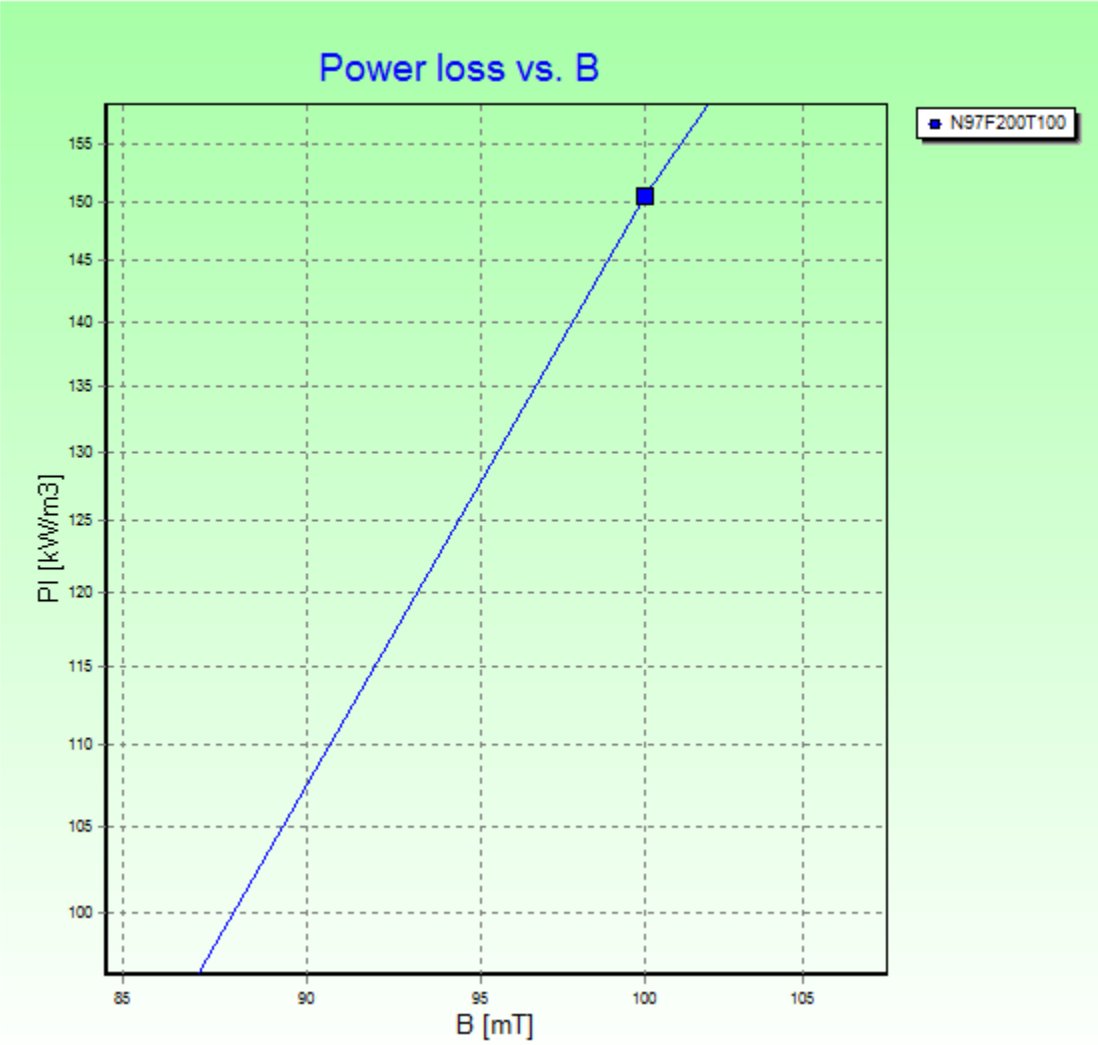


Figure A1. 1 Core power loss versus peak flux density

Number of winding turns

The maximum magnetic flux density swing is:

$$\Delta B_{max} = \frac{E}{A_e N_P} \Delta t_{on\_max}$$

where E is the voltage applied on the primary winding and A_e is the area of the core.

Thus the minimum number of primary turns is:

$$N_{P\_min} = \frac{V_{IN\_min}}{A_e \Delta B_{max}} \Delta t_{on\_max}$$

$$N_{P\_min} = \frac{280}{125e-6 \times 190e-3} \times 2.25e-6$$

$$N_{P\_min} = 26.5$$

We have selected $\mathbf{N_P = 28}$, as it is the first value multiple of the turns ratio (N_P/N_S=14). The resulting value for the secondary winding turns is $\mathbf{N_S = 2}$.

Checking the maximum flux swing for V_{IN_max} and Δt_{on_max}:

$$\Delta B_{max} = \frac{V_{IN\_max}}{A_e N_P} \Delta t_{on\_max} = 212mT$$

This is acceptable as it is much lower than the saturating flux density, $B_{SAT} \cong 400mT$.

The inductance of the primary winding (magnetising inductance) is given by:

$$L_P = N_P^2 \mu_e A_e / l_e$$

$$L_P = 2.16mH$$

The inductance of the secondary winding is:

$$L_S = N_S^2 \mu_e A_e / l_e$$

$$L_S = 11.02\mu H$$

Figure A1.2 and A1.3 present the measured inductance of the primary and secondary windings, respectively.

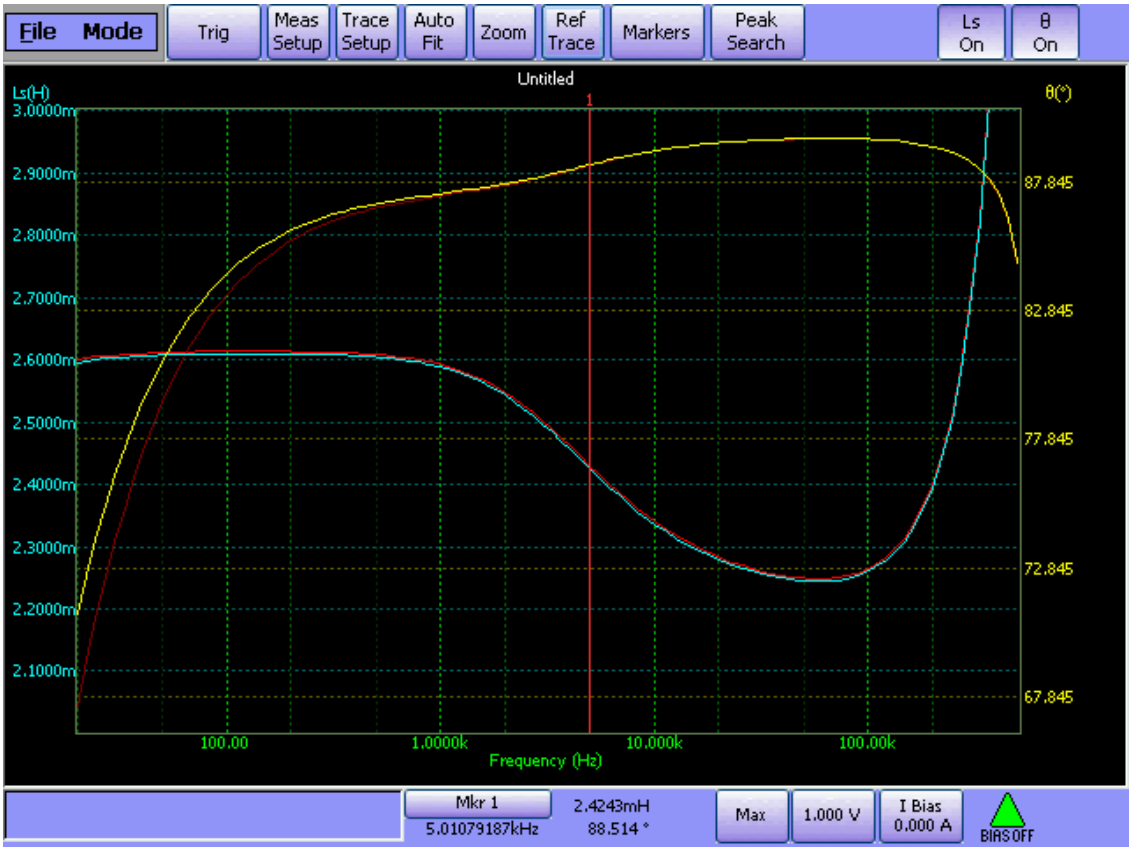


Figure A1. 2. Measured primary winding inductance;
blue and red – inductance of both primary windings;
yellow and brown – phase shift of the voltage across the primary windings

Figure A1. 3 Measured secondary winding inductance

Figure A1.4 presents the leakage inductance of the two primary windings. A larger value can be observed for one of them as this is placed on the outer layer of the transformer core and hence the coupling of the magnetic field into the core is lower.

Figure A1. 4. Measured leakage inductance of the transformer primary windings; blue – primary winding 1; red – primary winding 2; yellow – phase shift

Appendix 2 Matlab code – transient simulation

This code represents the first level behavioural modelling of the converter and it has been used to evaluate and verify the transient evolution of the main parameters during the charging process (i.e. input/output current, frequency, duty cycle, etc.).

```
clear all;
clc;
Lp = 2.16e-3;
Ls = 30e-6;
Np = 28;
Ns = 2;
Lo = 15e-6;
Co = 3e-2;
Po = 250;            %output power
Vin = 280;
Vd = 0.7;            %voltage drop on the diode
Vo(1) = 0;
Il(1) = 0;           %initial value of the inductor current
i = 1;               %main time counter *10ns
k = 0;               %counter for Il
l = 1;               %counter for Ip
% The values of Io, and Ip are saved only at the beginning and end of the
% on and off cyles, to reduce the array size.
% Array A, B hold the values of the counters k, l when data was saved
% in array Il and Ip
% Thus at the end the plot function is: plot(A,Io)
delta_Io = 1;        %ripple of the oputput current
sim = 20;            %simulation time in ms
sim = sim*1e5;

Io(1) = Il(1);
Io_c = Io(1);
Ip(1) = 0;
Vo_c = Vo(1);

Imax = Po/Vo + delta_Io/2;
if Imax > 30 + delta_Io/2
    Imax = 30 + delta_Io/2;
end
Imin = Imax - delta_Io;

ton_max = 330*225/Vin;

while i<sim
%state 1
    j = 0;
    l = l+1;
    Ip(l) = Vin/Lp*(j+1)*1e-8 + Io_c*Ns/Np;   %primary current
    B(l) = (i+1)/100;
    VLo = Vin*Ns/Np - Vo_c - (Vd + 0.2);
    while (j < ton_max) && (Io_c < Imax)
        Vo_c = Vo_c + Io_c*1e-8/Co;
        Io_c = Io_c + VLo/Lo*1e-8;      %inductor current
        i = i+1;
        j = j+1;
    end                 % at the end of the loop j represents the on time
    k = k+1;
    Io(k) = Io_c;
    Vo(k) = Vo_c;
    A(k) = i/100;
```

```
    l = l+1;
    Ip(l) = Vin/Lp*(j+1)*1e-8 + Io_c*Ns/Np;   %primary current
    B(l) = i/100;
    ton = j/100;
%state 2
    j = 0;
    l = l+1;
    Ip(l) = 0;          %primary current
    B(l) = (i+1)/100;
    VLo = -(Vo_c + 0.85);
    while (j < 25) || (Io_c > Imin)    %minimum off time is 0.25us (5%)
        Vo_c = Vo_c + Io_c*1e-8/Co;
        Io_c = Io_c + VLo/Lo*1e-8;
        j = j+1;
        i = i+1;
    end                 % at the end of the loop j represents the off time
    k = k+1;
    Io(k) = Io_c;
    Vo(k) = Vo_c;
    A(k) = i/100;
    l = l+1;
    Ip(l) = 0;          %primary current
    B(l) = (i+1)/100;
    toff = j/100;
    freq(i) = 1/(ton+toff);
    duty(i) = ton/(2*(ton+toff));
%update Imax
    Imax = Po/Vo_c;
    Imax = Imax .* [Imax<=30] + 30 .* [Imax>30]  + delta_Io/2;
    Imin = Imax - delta_Io;
%state 3
    j = 0;
    l = l+1;
    Ip(l) = Vin/Lp*(j+1)*1e-8 + Io_c*Ns/Np;   %primary current
    B(l) = (i+1)/100;
    VLo = Vin*Ns/Np - Vo_c - (Vd + 0.2);
    while (j < ton_max) && (Io_c < Imax)
        Vo_c = Vo_c + Io_c*1e-8/Co;
        Io_c = Io_c + VLo/Lo*1e-8;     %inductor current
        i = i+1;
        j = j+1;
    end
    ton = j/100;
    k = k+1;
    Io(k) = Io_c;
    Vo(k) = Vo_c;
    A(k) = i/100;
    l = l+1;
    Ip(l) = Vin/Lp*(j+1)*1e-8 + Io_c*Ns/Np;   %primary current
    B(l) = i/100;
%state 4
    j = 0;
    l = l+1;
    Ip(l) = 0;          %primary current
    B(l) = (i+1)/100;
    VLo = -(Vo_c + 0.85);
    while (j < 25) || (Io_c > Imin)    %minimum off time is 0.5us (5%)
        Vo_c = Vo_c + Io_c*1e-8/Co;
        Io_c = Io_c + VLo/Lo*1e-8;
        j = j+1;
        i = i+1;
    end
    k = k+1;
    Io(k) = Io_c;
```

```
    Vo(k) = Vo_c;
    A(k) = i/100;
    l = l+1;
    Ip(l) = 0;          %primary current
    B(l) = (i+1)/100;
    toff = j/100;
    freq(i) = 1/(ton+toff);
    duty(i) = ton/(2*(ton+toff));
Imax = Po/Vo_c;
Imax = Imax .* [Imax<=30] + 30 .* [Imax>30]  + delta_Io/2;
Imin = Imax - delta_Io;
end
x = 1:1:i;
figure(1);
plot (A,Io);        %plot of the inductur current vs. time in us
xlabel ('time [us]');
ylabel ('Output inductor current [A]');
figure(2);
plot (A,Vo);
xlabel ('time [us]');
ylabel ('Output voltage [V]');
figure(3);
plot (B,Ip);
xlabel ('time [us]');
ylabel ('Sum of the primary windings current [A]');
figure(4);
plot(x/100,freq*1e3/2);
xlabel ('time [us]');
ylabel ('Frequency [KHz]');
figure(5);
plot(x/100,duty*100);
xlabel ('time [us]');
ylabel ('Duty cycle [%]');
Ton = duty./freq*2;
figure(6);
plot(x/100,Ton);
xlabel ('time [us]');
ylabel ('On time [us]');
Toff = (1-duty)./freq;
figure(7);
plot(x/100,Toff);
xlabel ('time [us]');
ylabel ('Off time [us]');
hold on;
t_off = delta_Io*Lo./(Vo+0.8)+Vo*6e-8;
%plot (A,t_off,'red');
hold off;
figure(8);
plot (A,Io);
hold on;
plot (A,Vo.*Io/10);
xlabel ('time [us]');
ylabel ('Output inductor current [A] and output power [W]');
hold off;
```

Appendix 3 Matlab code – switching simulation

This second Matlab modelling of the converter evaluates the main parameters as function of the output voltage (DC sweep). Similarly to the transient behavioural simulation, it looks at the evolution of the frequency and duty cycle, but it also looks at other parameters like the AC current, flux density and flux density penetration depth.

```
clear all;
Vo = 0.001:0.2:16.201;
Lo = 15e-6;
Vin = 330;
Ns = 2;
Np = 28;
Ae = 1.25e-4;
delta_Io = 1;
Po_max = 250;
Io = Po_max./Vo;
Io = Io .* [Io<=30] + 30 .* [Io>30];
Po = Io.*Vo;
ton_max = 330*2.25/Vin*1e-6;
Vd = 0.8;
Rsw = 5;   %switch on resistance

ton = delta_Io*Lo./(Vin*Ns/Np - Vo -Vd);

%introduce ton limit
ton = ton .* [ton<=ton_max] + ton_max .* [ton>ton_max];
%reevaluate delta Io
delta_Io = (Vin*Ns/Np - Vo -Vd).*ton/Lo;
%calculate toff
toff = delta_Io*Lo./(Vo + Vd);
%calculate ratio between ton and toff
r = ton./toff;
%calculate duty cycle for a switch
D = r./(2*(1+r));
%calculate frequency
f = 1./(2*toff.*(1+r));
%Penetration depth
Dpen = 76./sqrt(f);
%Flux density swing
delta_B = Vin.*D./(f*Ae*Np);

Is_avg = Io.*0.5;     %average current for a secondary winding
Is_rms = Is_avg./sqrt(0.5);
Is_ac = sqrt((Is_rms).^2 - (Is_avg).^2);
Ip_avg = (Io.*D)*Ns/Np;     %primary average current
Ip_rms = Ip_avg./sqrt(D);
Ip_ac = sqrt((Ip_rms).^2 - (Ip_avg).^2);

figure(1);
plot (Vo,D);
xlabel ('Output voltage [V]');
ylabel ('Duty cycle for a switch [%]');
figure(2);
plot (Vo,f/1e3);
xlabel ('Output voltage [V]');
ylabel ('Transformer frequency [kHz]');
figure(3);
plot (Vo,Io,Vo,Po/10);
xlabel ('Output voltage [V]');
```

```
ylabel ('Maximum output current [A]');
figure (4);
plot (Vo,Ip_avg);
xlabel ('Output voltage [V]');
ylabel ('Average current for a switch');
figure (5);
plot (Vo,Ip_ac);
xlabel ('Output voltage [V]');
ylabel ('AC current for a primary winding (switch)');
figure (6);
plot (Vo,Is_avg);
xlabel ('Output voltage [V]');
ylabel ('Average current for a secondary winding');
figure (7);
plot (Vo,Is_ac);
xlabel ('Output voltage [V]');
ylabel ('AC current for a secondary winding');
figure (8);
plot (Vo,delta_B*1e3);
xlabel ('Output voltage [V]');
ylabel ('Flux density swing [mTesla]');
figure (9);
plot (Vo,Dpen);
xlabel ('Output voltage [V]');
ylabel ('Penetration depth [mm]');
figure (10);
plot (Vo,toff);
xlabel ('Output voltage [V]');
ylabel ('Off time');
figure (11);
plot (Vo,ton);
xlabel ('Output voltage [V]');
ylabel ('On time');
figure (12);
[AX,H1,H2] = plotyy (Vo,ton,Vo,f/1e3);
set(get(AX(1),'Ylabel'),'String','On time (\musec)')
set(get(AX(2),'Ylabel'),'String','Transformer frequency [kHz]')
xlabel ('Output voltage [V]');
figure (13);
[AX,H1,H2] = plotyy (Vo,toff,Vo,f/1e3);
set(get(AX(1),'Ylabel'),'String','Off time (\musec)')
set(get(AX(2),'Ylabel'),'String','Transformer frequency [kHz]')
xlabel ('Output voltage [V]');

% power dissipation in a switch
Psw = Rsw * (Io * Ns/Np).^2 .* D;   %DC power dissipation in a switch
figure (14);
[AX,H1,H2] = plotyy (Vo,Psw,Vo,Io * Ns/Np);
set(get(AX(1),'Ylabel'),'String','DC Power dissipation in a switch [W]')
set(get(AX(2),'Ylabel'),'String','Input current [A]')
xlabel ('Output voltage [V]');
```

Appendix 4 Matlab switching simulation results

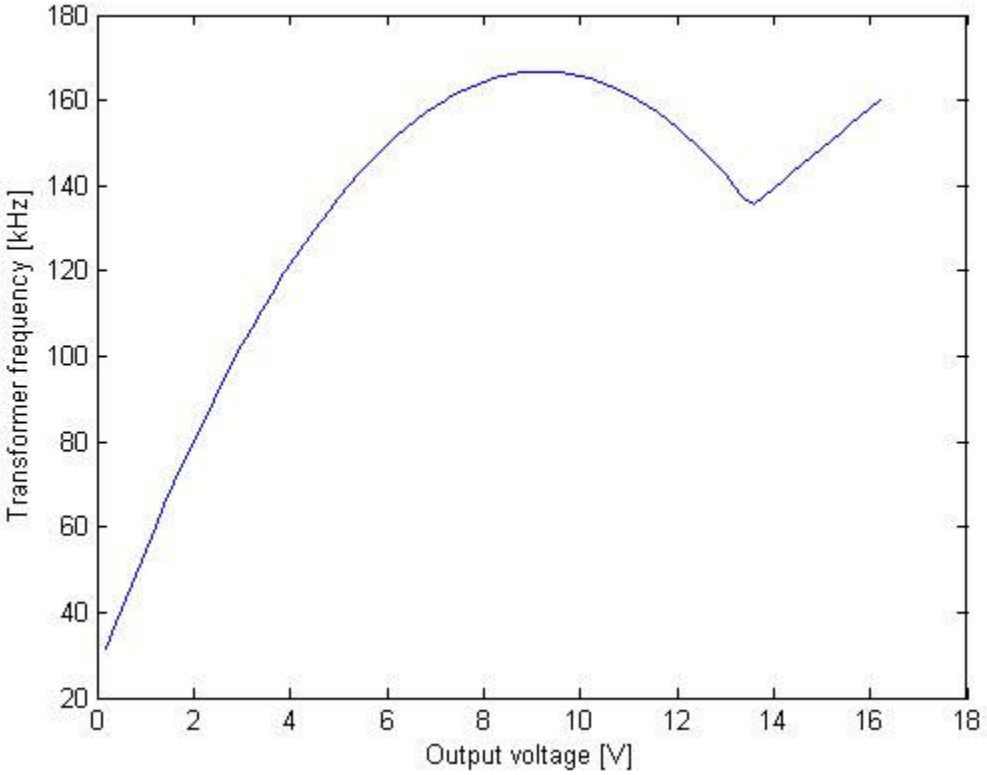


Figure A4. 1 Transformer and main switches operating frequency, V_{IN}=280V

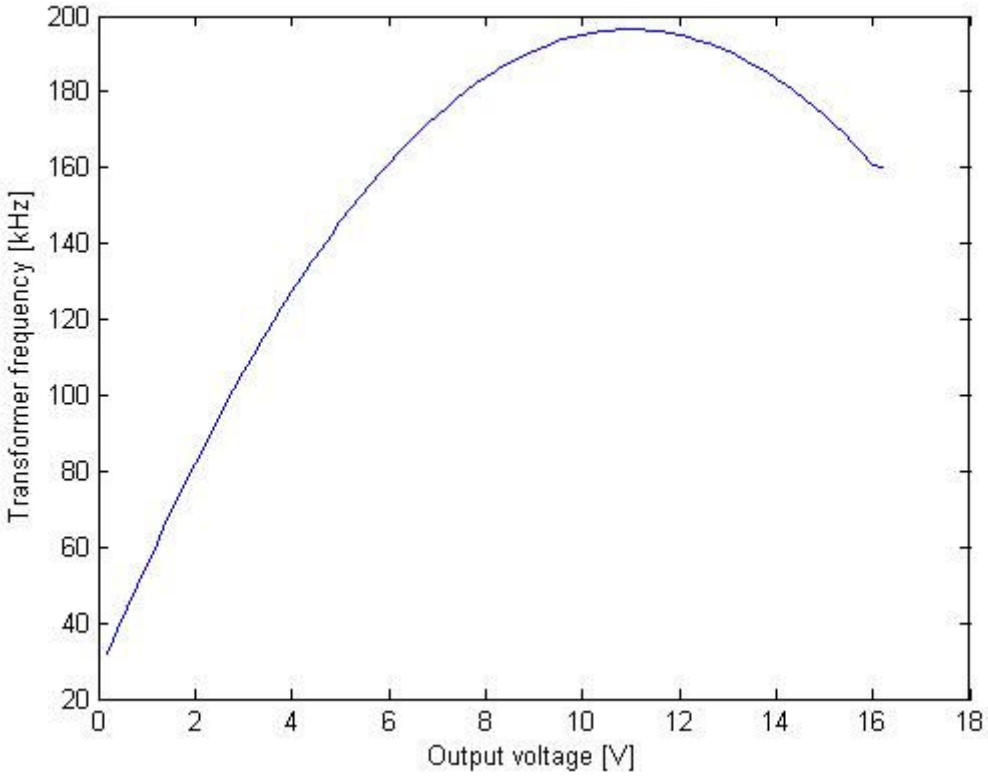


Figure A4. 2 Transformer and main switches operating frequency, V_{IN}=330V

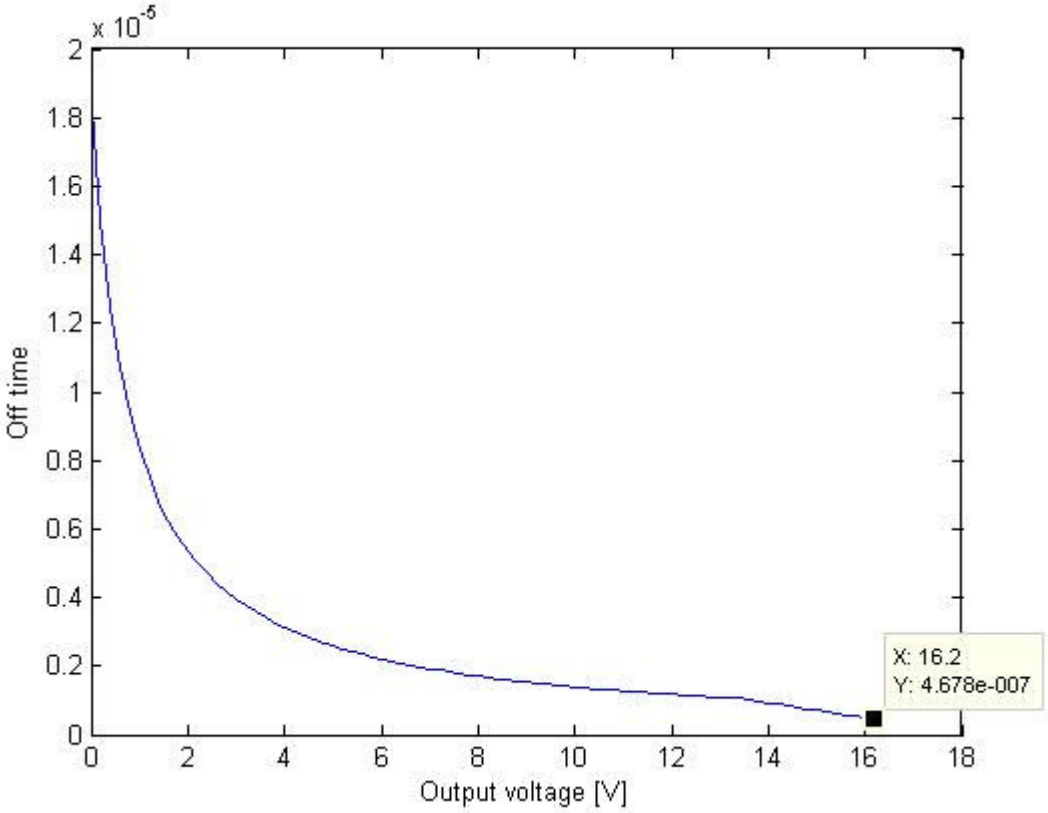


Figure A4. 3 OFF time duration, V_{IN}=280V

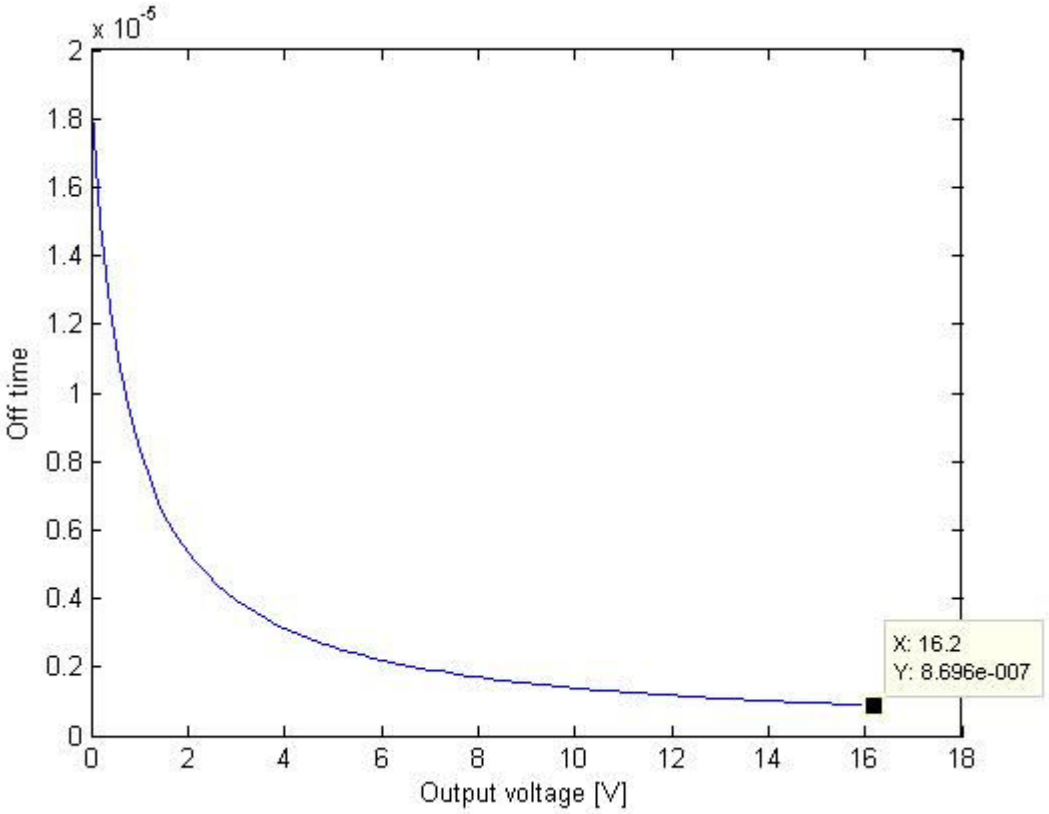


Figure A4. 4 OFF time duration, VIN=330V

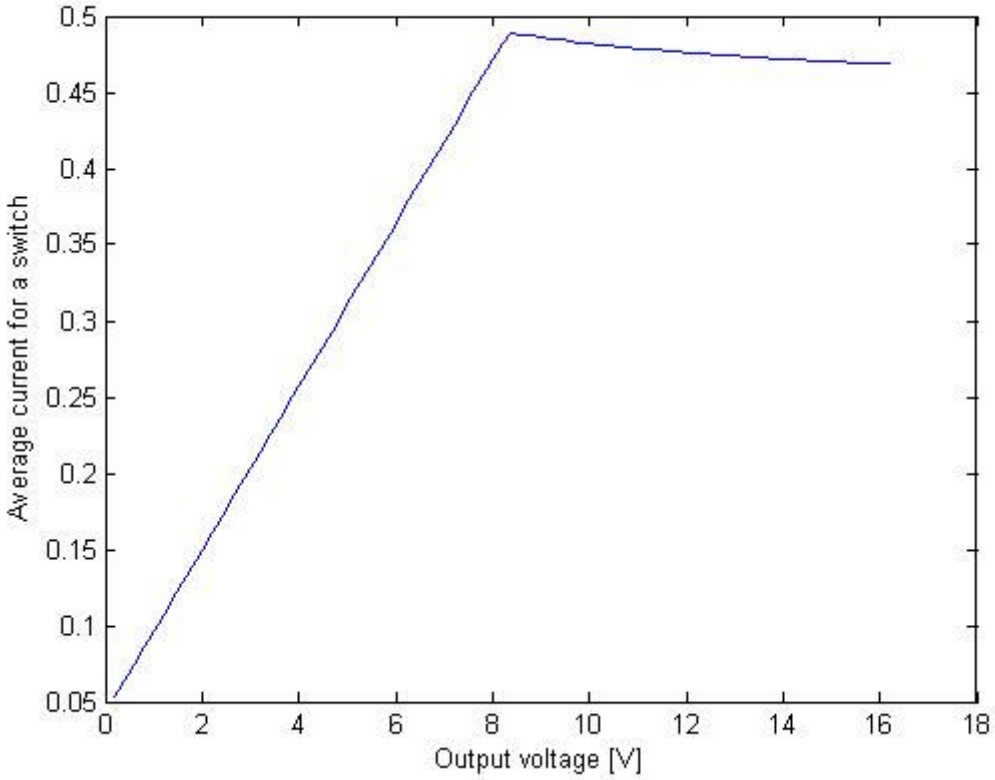


Figure A4. 5 DC current for a switch and primary windings,V_{IN}=280V

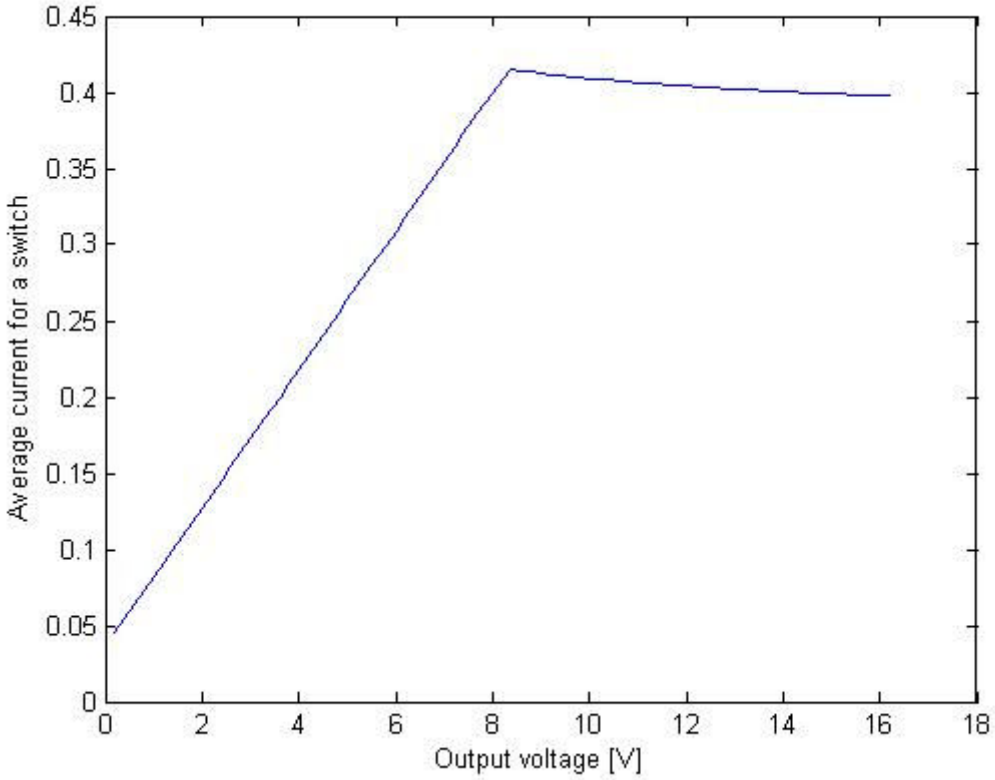


Figure A4. 6 DC current for a switch and primary windings V_{IN}=330V

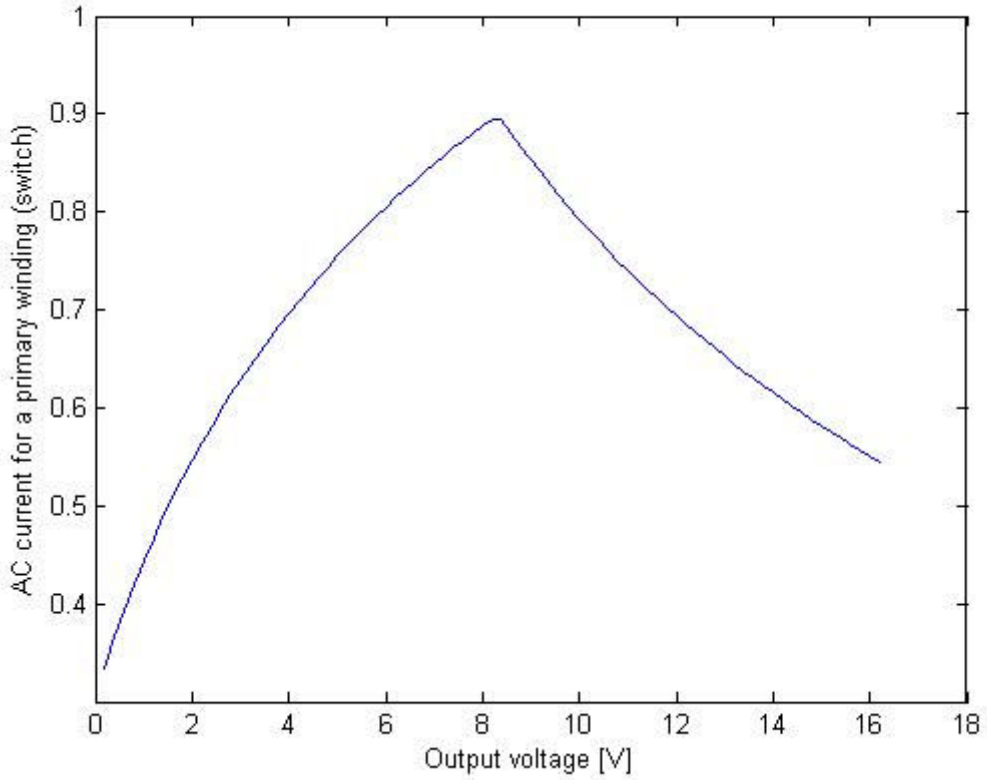


Figure A4. 7 AC current for a switch and primary winding, V_{IN}=280V

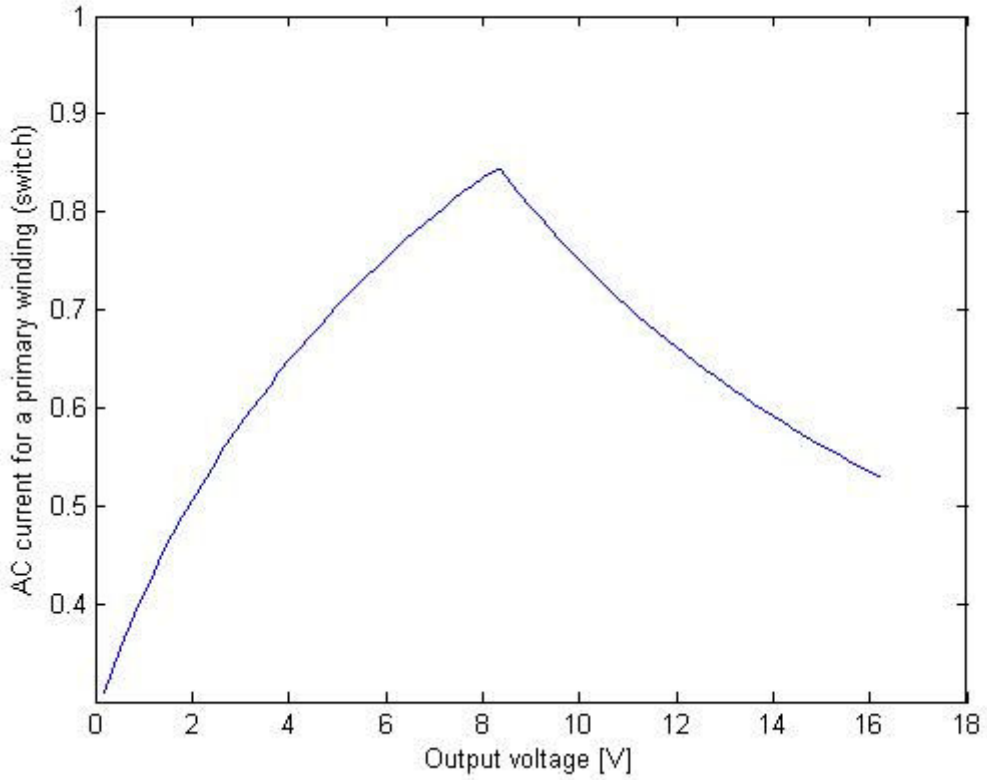


Figure A4. 8 AC current for a switch and primary winding, V_{IN}=330V

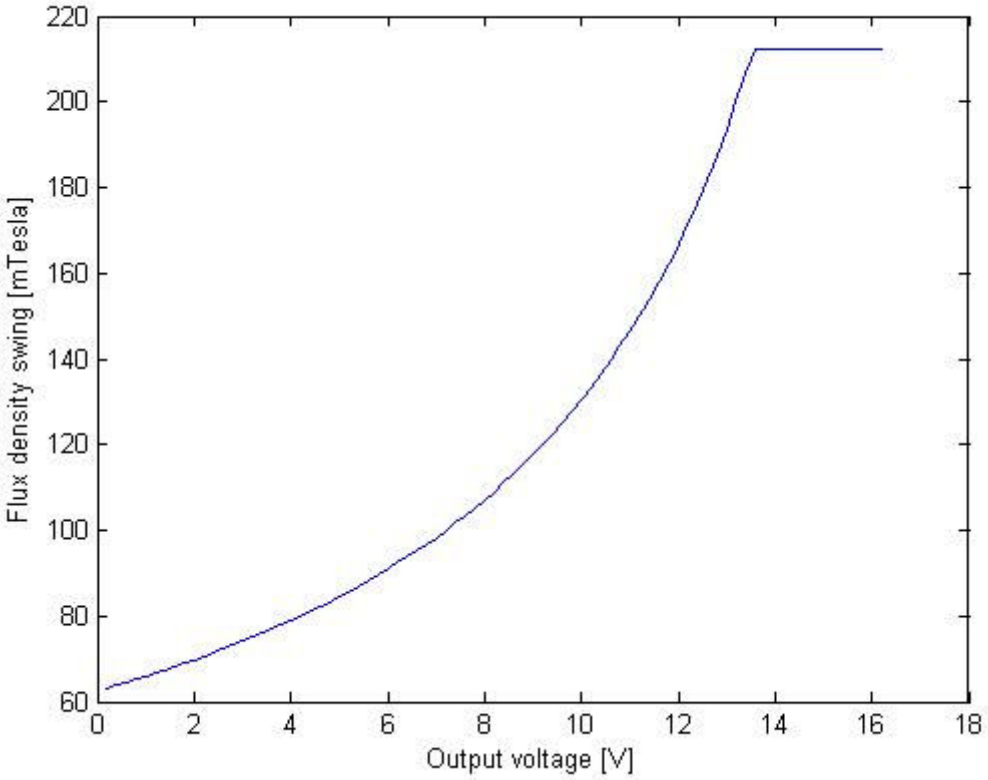


Figure A4. 9 Transformer flux density swing, V_{IN}=280V

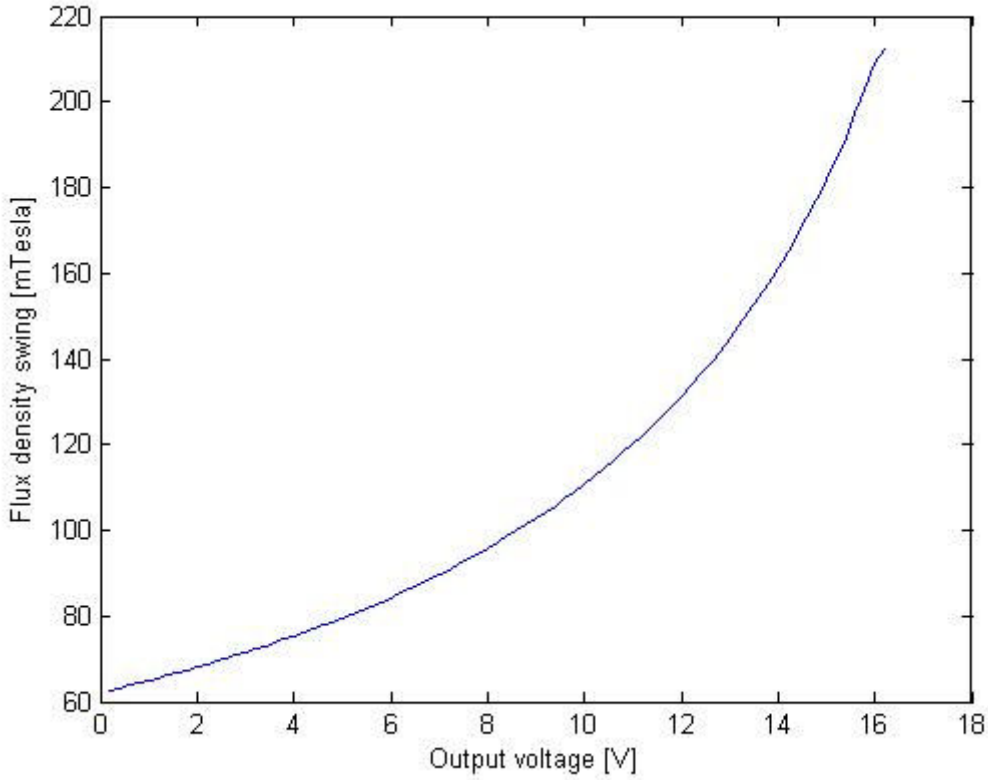


Figure A4. 10 Transformer flux density swing, VIN=330V

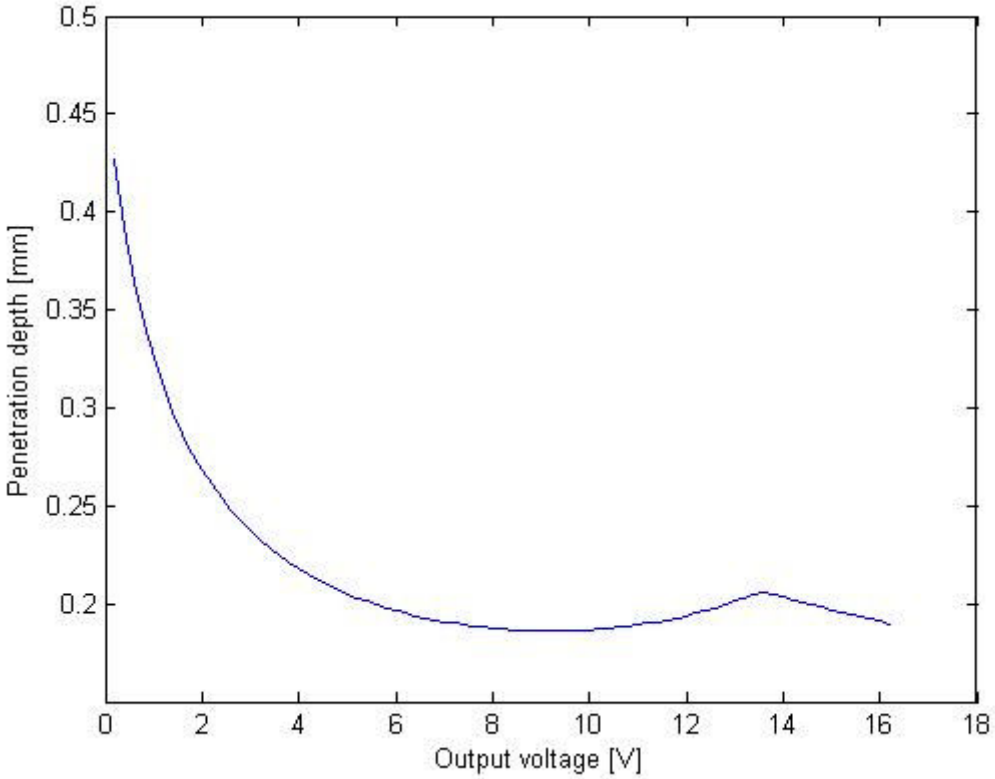


Figure A4. 11 Skin effect penetration depth, VIN=280V

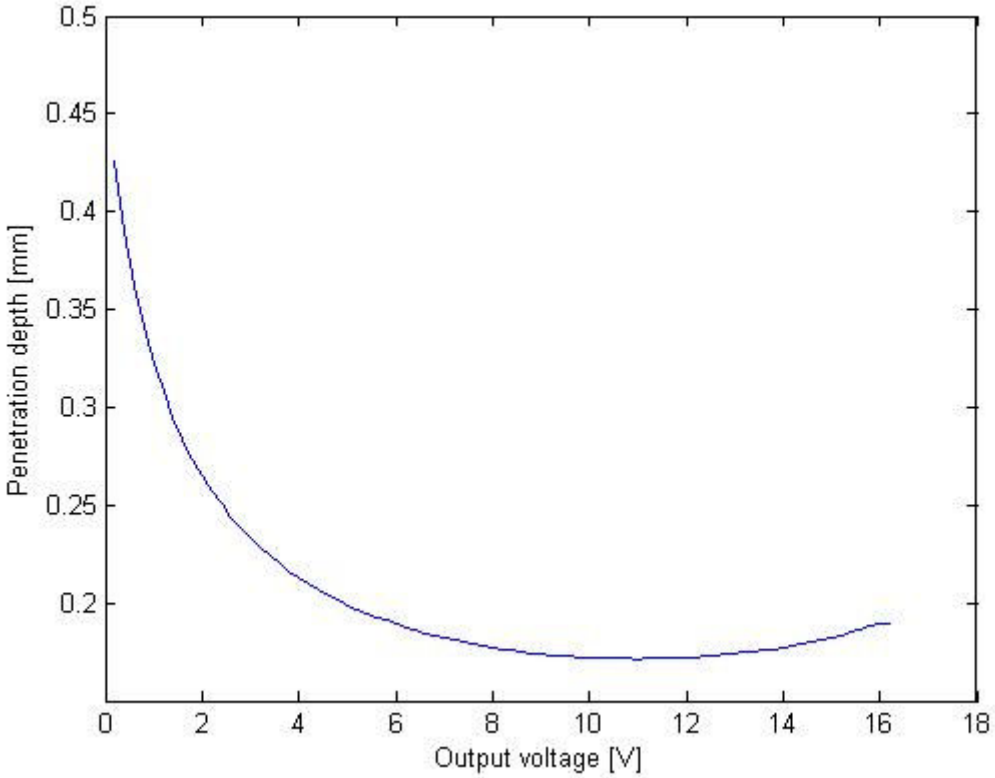


Figure A4. 12 Skin effect penetration depth, VIN=280V

Appendix 5 Current reference block

Circuit diagram of the current reference block, corresponding to chapter 4.1, figure 4.1. The block generates the *output current reference* as a function of the output voltage when the converter operates in power limitation mode. The output clamping buffer limits the value of the *output current reference* to the equivalent of 30A, when the converter operates in constant current mode.

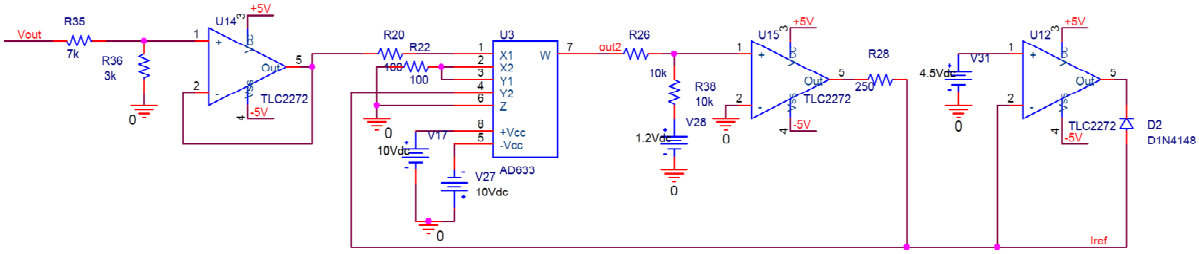


Figure A5. 1 Diagram of the current reference block (corresponding to figure 4.1)

Appendix 6 Output current block

Circuit diagram of the output current estimation block, described in chapter 4.1 and corresponding to the fuctional diagram presented in figure 4.3. The circuit senses the over-current condition (amplifier U104), logic output *"ov_crt_in"*. Amplifier U64A monitors the maximum duration of the ON time, logic output *"max_on_time"*. Under normal operating conditions (when the over-current or the maximum ON time is not exceeded), comparator U102 turns OFF the power switches when the value corresponding to the estimated output current exceeds the value of the *output current reference.*

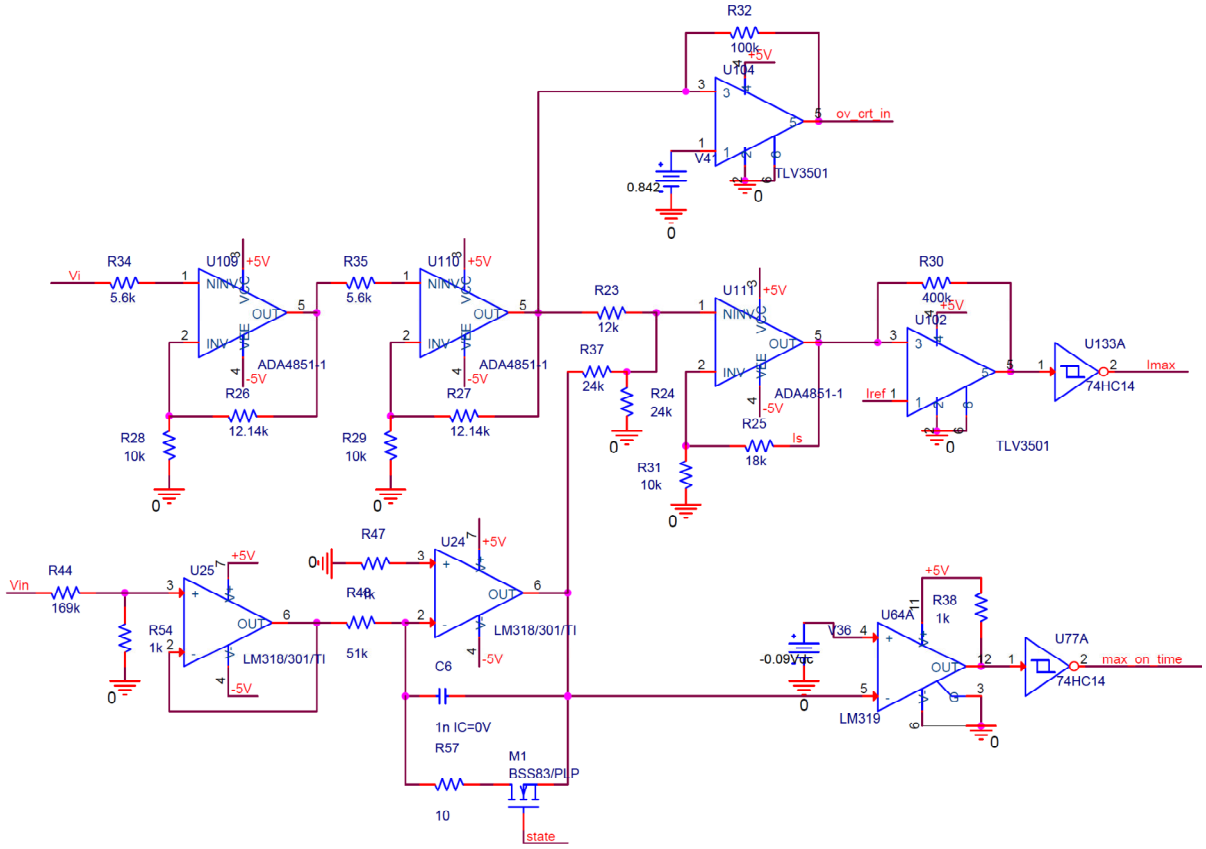


Figure A6. 1 Circuit diagram of the output current block (corresponding to figure 4.3)

Appendix 7 OFF time estimation block – input current sampling algorithm

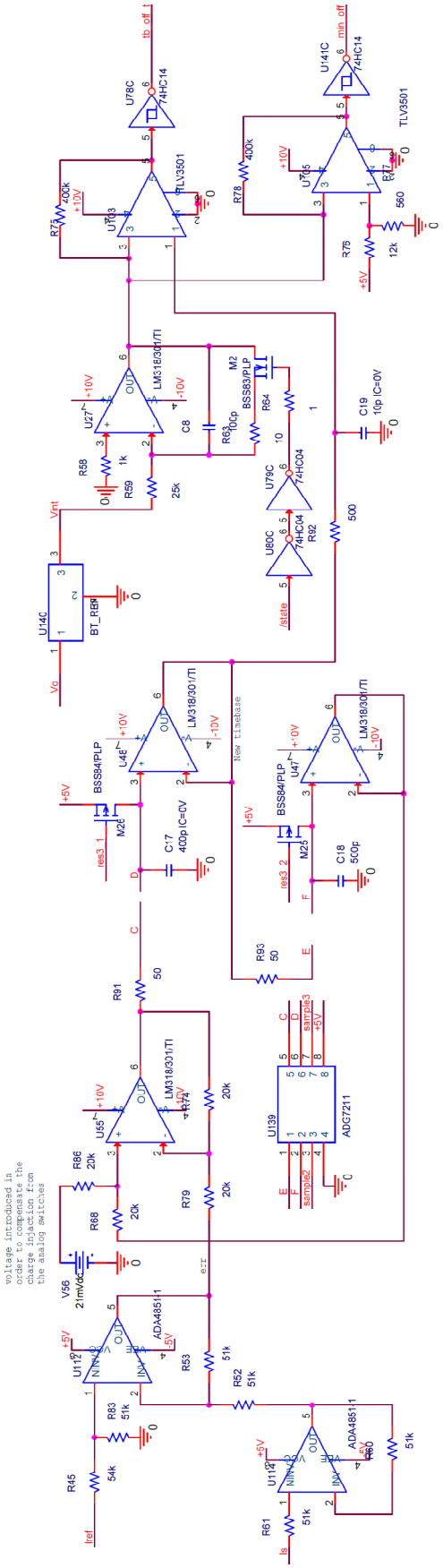
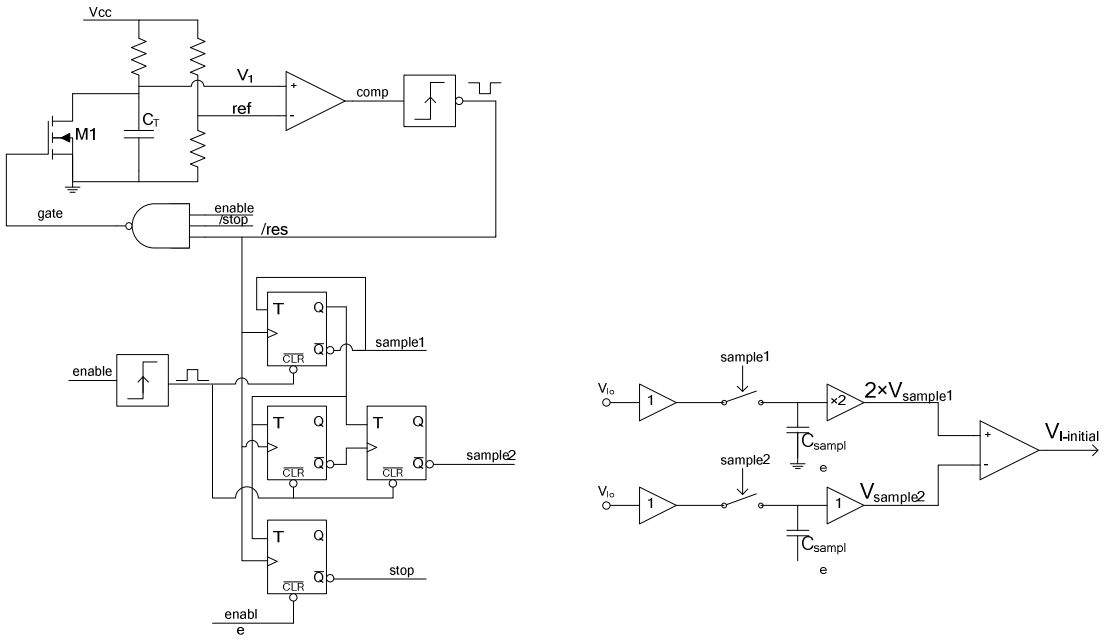


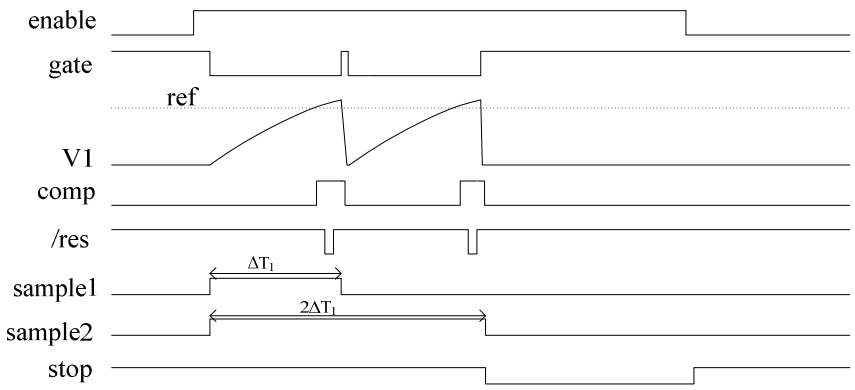
Figure A7. 1 Circuit diagram of the OFF time estimation block corresponding to figure 4.4)

Appendix 8 Double sampling circuit

Below we present the diagram of the double sampling circuit and the waveforms of the logic circuit, respectively. When the "ON phase" starts, the double sampling circuit is activated through the "enable" signal. At this moment the MOSFET M1 is turned off, allowing capacitor C_T to charge. Also the rising edge of the enable signal resets the flip-flops for sample1 and sample2 signals, thus turning on the sampling switches. When voltage V_1 reaches the reference voltage set by the resistive divider, the comparator changes state and a negated pulse is generated by the edge detector. This pulse has the purpose of resetting the capacitor voltage (through the NAND gate) and also acts as a clock signal for the flip-flops. Capacitor C_T is charged up to the reference voltage two consecutive times. The reset signal (/res) activated at the end of the first cycle toggles only the "sample1" flip-flop. Due to the connections at the input, this flip-flop will be locked in this state until the asynchronous reset is activated. The second pulse toggles the other three flip-flops. Two cascaded flip-flops had to be used for the sample2 signal in order to maintain the ratio between the sampling times. The "stop" flip-flop is used to inhibit the recharging of the capacitor until the start of the next "on phase".



a)



b)

Figure A8. 1 Double sampling: a) circuit diagram; b) waveforms

The duration of the sample1 and sample2 pulses is composed of:

$$T_{sample1} = t_{pd\text{-}NAND} + t_{charge} + t_{d\text{-}comp} + t_{d\text{-}re} + t_{pulse} + t_{pd\text{-}ff} \quad \text{(A8.1)}$$

$$T_{sample2} = t_{pd\text{-}NAND} + t_{charge} + t_{d\text{-}comp} + t_{d\text{-}re} + t_{pulse} + t_{pd\text{-}NAND} + t_{charge} + t_{d\text{-}comp} + t_{d\text{-}re} + t_{pulse} + 2\times t_{pd\text{-}ff} \quad \text{(A8.2)}$$

where: $t_{pd\text{-}NAND}$ is the propagation delay of the NAND gate, t_{charge} is the charging time of the capacitor, $t_{d\text{-}comp}$ is the delay of the comparator, t_{pulse} is the duration of the pulse including the propagation delay and $t_{pd\text{-}ff}$ is the propagation delay of the flip-flop.

It can be observed from equations (A8.1) and (A8.2) that the duration of the sample2 pulse is precisely double the duration of the sample1 pulse.

The simulation waveforms of the sampled signals and the estimated value are presented in figure A.8.2.

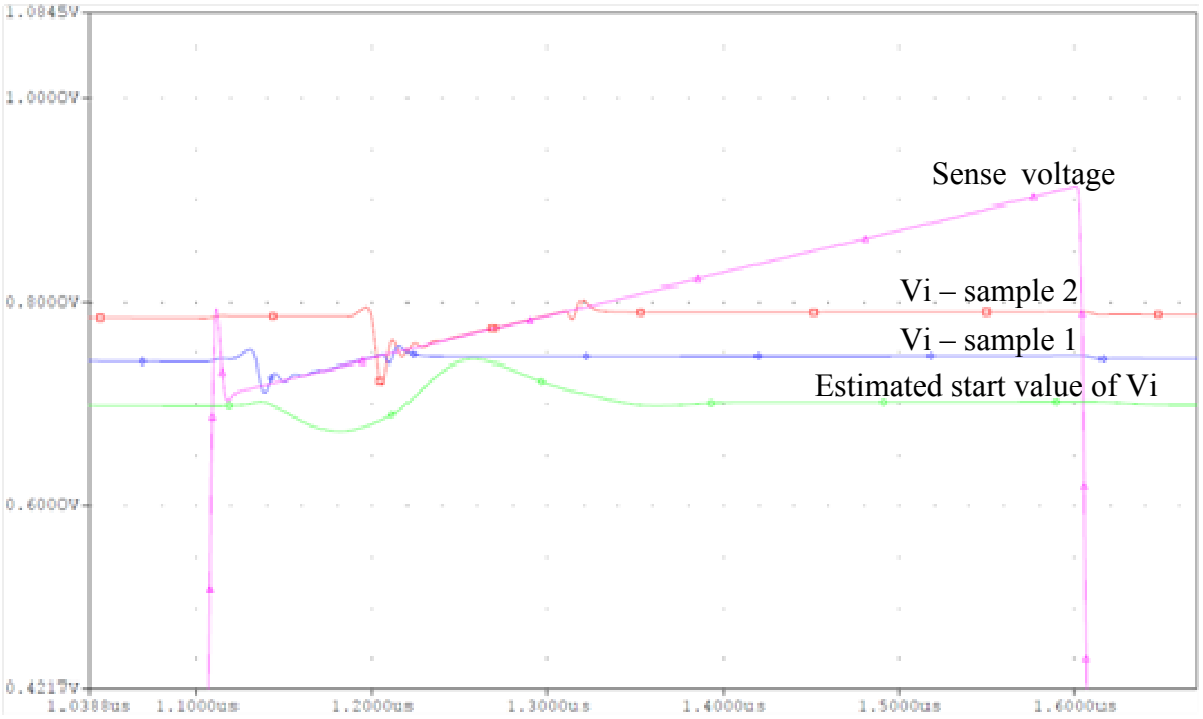


Figure A8. 2 Double sampling circuit waveforms for the sampled signals and the estimated initial value

Appendix 9 V-I conversion circuit

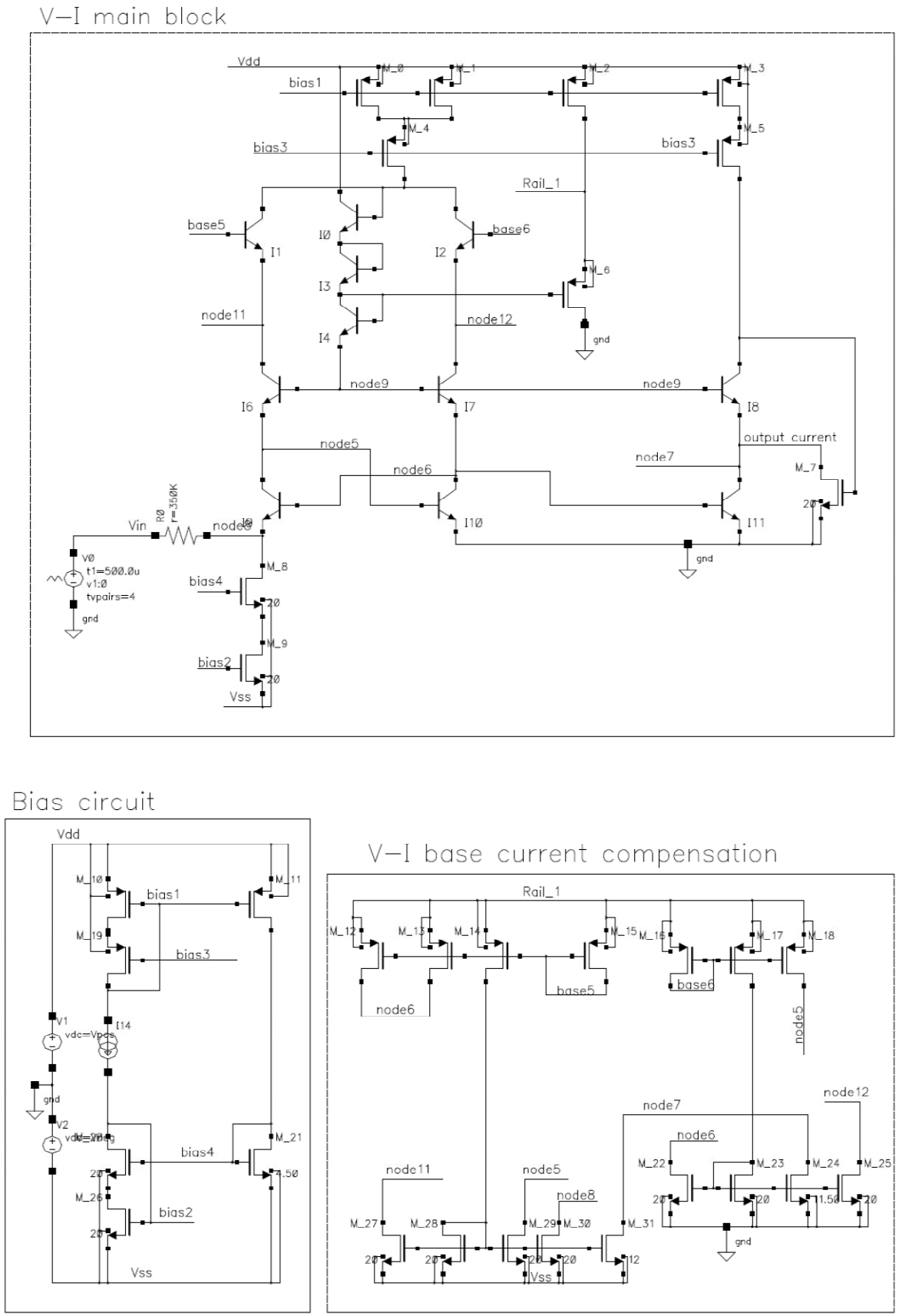


Figure A9. 1 Circuit diagram of the V-I conversion block (corresponding to figure 5.5) implemented in NXP EZ-HV process [ref]

Appendix 10 Current divider and limiting circuit

The operation of the current limiting circuit at the output of the current divider is fairly simple. The description of the circuit is based on the simplified schematic from figure A10.1.

If the current divider output current, I_o, is less than the limiting current, I_{MAX}, then the value of $I_{diff} = I_o - I_{max}$ is zero and the output current I_o' is equal to I_o.

When I_o exceeds I_{max}, the value of I_{diff} starts to increase and the limiter's output current is: $I_o' = I_o - (I_o - I_{max}) = I_{max}$

The full schematics of the circuit designed for the NXP EZ-HV process are shown in figure A10.2

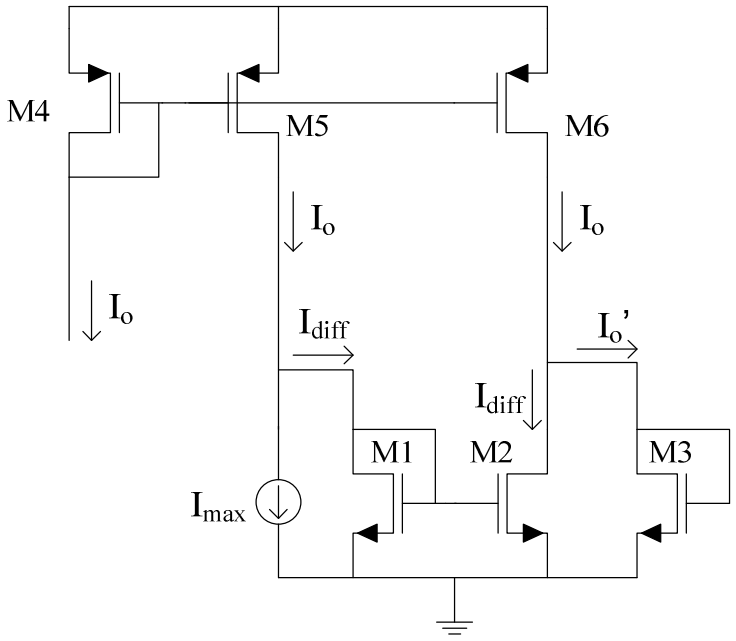


Figure A10. 1 Diagram of the current limiting circuit

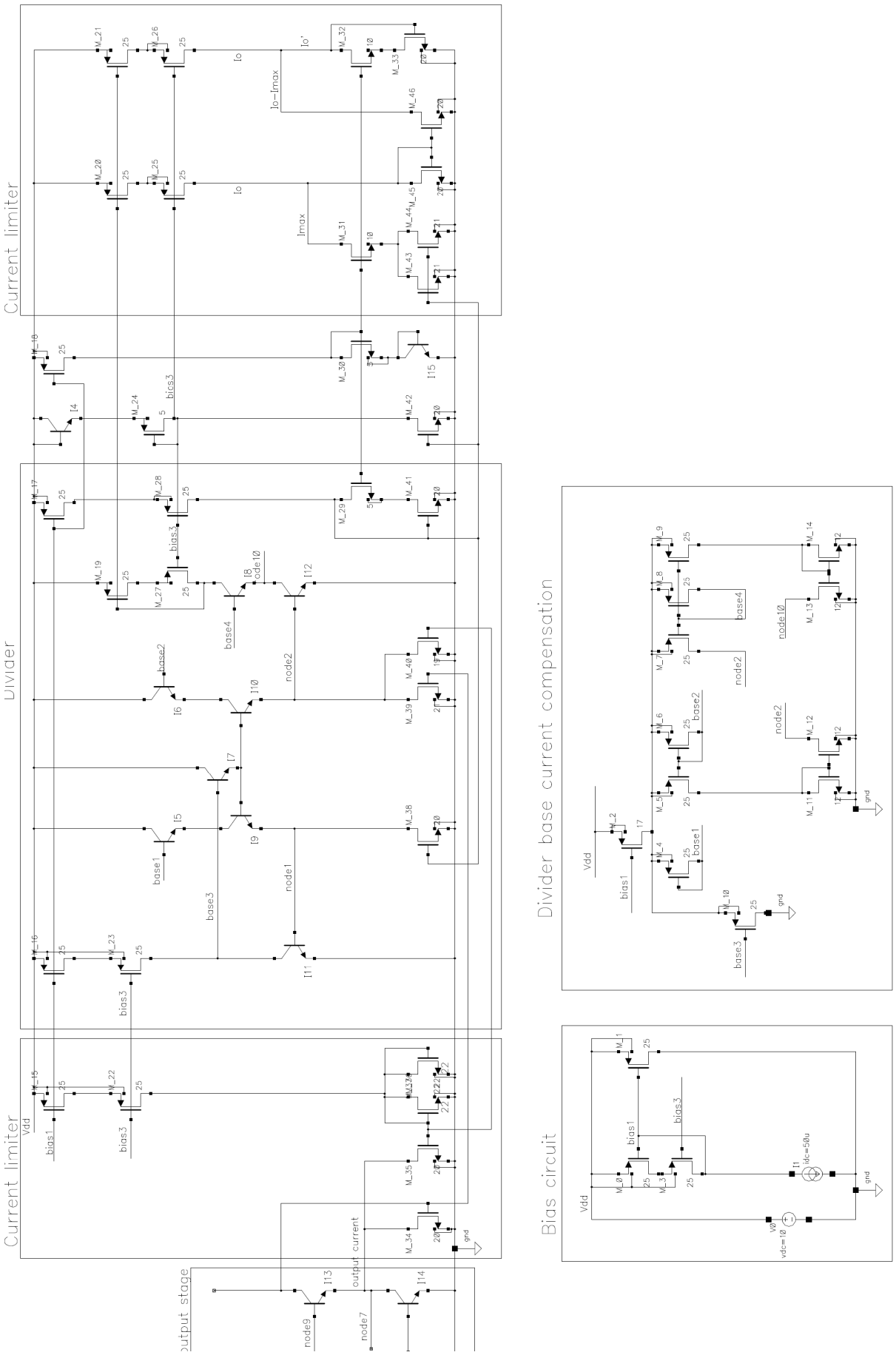


Figure A10. 2 Circuit diagram of the divider block (corresponding to figure 5.7)

Appendix 11 Current sampling circuit

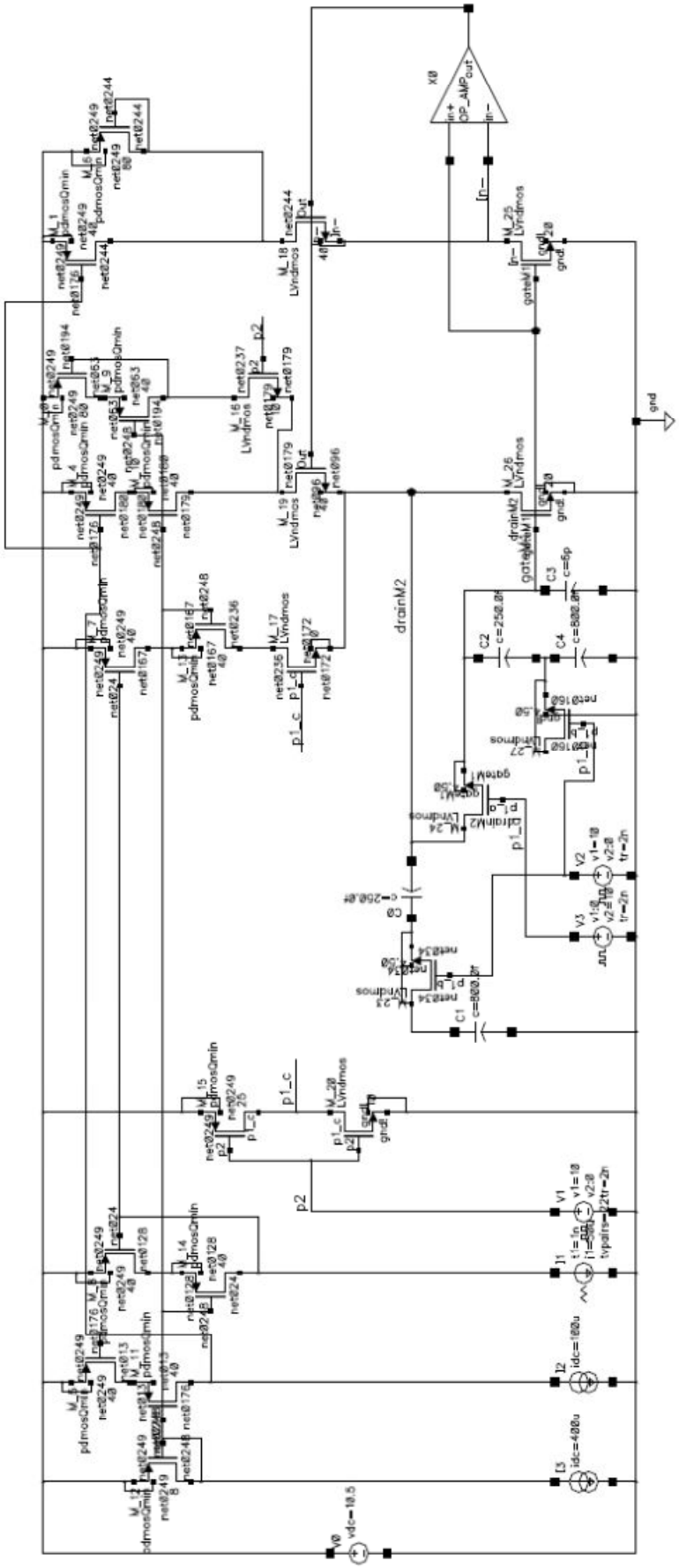


Figure 11. 1. Detailed circuit diagram of the current sampling block in the NXP EZ-HV process (corresponding to figure 5.9)

Appendix 12 ADC and divider controller Verilog code

Verilog code for the mixed signal implementation (AMS 0.35µm process), describing the ADC and divider controller. The code corresponds to the ASM chart from figure 7.16.

```
`timescale 1ns/10ps

module ADcontrol (sampleAD, clkAD, ready, dataOut, sInDiv, Latch, startAD,
sIn, divDenom, state, clock, nReset );

output reg sampleAD, clkAD, ready, sInDiv, Latch;
output reg [7:0] dataOut;
input [7:0] divDenom;
input startAD, sIn, state, clock, nReset;

reg [4:0] sampleTime;
reg [3:0] clockCycles;
reg [3:0] clockCount;
reg clockEN, start1;
reg [8:0] denom;

parameter refSampleTime = 30;       //50ns = 15 clock cycles
parameter refClockCount = 7;

always @ (negedge nReset)
  begin
    sampleAD <= #1 1;
    clkAD <= #1 0;
    sampleTime <= #1 0;
    clockCycles <= #1 0;
    clockCount <= #1 0;
    clockEN <= #1 0;
    ready <= #1 0;
    start1 <= #1 0;
    dataOut <= #1 0;
    sInDiv <= #1 0;
    denom <= #1 0;
    Latch <= #1 0;
  end

always @ (posedge clock)
begin
  start1 <= #1 startAD;      //start1 is startAD delayed by one clock cycle
  if (sampleAD && ~ready)
      sampleTime <= #1 sampleTime + 1;    //Increment sample time

  if (sampleTime == refSampleTime)  //At the end of the sampling interval
      ready <= #1 1;                //Set the ready sample flag

  if (startAD && ready && ~start1)  //At the rising edge of startAD
      begin
        sampleAD <= #1 0;           //Switch from sample to hold mode
        clkAD <= #1 1;              //Toggle the ADC clock
        clockCycles <= #1 0;        //Reset the bit trials counter
        clockEN <= #1 1;            //Set the enable flag for the ADC clock
        ready <= #1 0;              //Reset the ready sample flag
        denom <= #1 divDenom;       //Save local copy of the denominator at
                                 //the start of the AD conversion
      end
```

```
//Clock divider
  if (clockEN)                              //If the ADC clock flag is set
    clockCount <= #1 clockCount + 1;        //Increment the clock divider

if ((clockEN) && (clockCount == refClockCount)) //On the + edge of ADC clock
     begin
       clockCount <= #1 0;                  //Reset the clock divider counter
       if ((~clkAD) && (clockCycles == 7))      //End of the conversion
              begin
                  sampleAD <= #1 1;             //Go into sample mode
                  sampleTime <= #1 0;           //Reset sample time counter
                end
        if (~clkAD)           //At the end of the ADC period (rising edge)
            begin
              clockCycles <= #1 clockCycles + 1;   //Inc ADC clock cycles
              if (clockCycles < 8)
                dataOut <= #1 {dataOut[6:0], sIn}; // Save ADC bit trial
             end
       else             // On the falling edge update the divider register
            begin
            if       ((clockCycles       <       8)       &&       ~state)
//Update divider serial in during the OFF phase
                 sInDiv <= #1 denom[clockCycles];
//Update the sOutDiv at the falling edge of the clkAD
            if ((clockCycles == 7) && ~state)
//After 7 clock cycles latch the SIPO reg
                 Latch <= #1 1;              //Set latch signal
                   else
                 Latch <= #1 0;              //Clear latch signal
            end
        if ((~clkAD) && (clockCycles == 8))  //After 8 clock cycles
           clockEN <= #1 0;   //Deactivate the ADC/divider clock enable
        else
             clkAD <= #1 ~clkAD;    // If # clock cycles < 8 toggle clock
     end
end
endmodule
```

Appendix 13 Digital controller for OFF time estimation algorithm

Verilog code for the mixed signal implementation (AMS 0.35µm process), describing the top level digital controller. The code corresponds to the ASM chart from figure 7.19.

```
//Verilog HDL for "digitalLib", "digitalBlock" "verilog"

`timescale 1ns/10ps

module digitalBlock (state, sInDiv, LatchDiv, LatchTune, sampleAD, nResAn,
clockAD, selMux[1:0], comp, sIn, enable, clock, nResDig);

output sInDiv, LatchDiv, LatchTune, sampleAD, clockAD, nResAn;
output reg selMux[1:0];
output reg state;
input comp, sIn, enable, clock, nResDig;

parameter on = 1'b1, off = 1'b0;
parameter selIp = 2'b00, selVin = 2'b01, selVout = 2'b10;
parameter [20:0] refOnTime = 658285;
parameter minOnTime = 162, maxOnTime = 600;
parameter minOffTime = 170;
parameter K1 = 17;
parameter K2 = 95;
parameter n = 11;
parameter minADtime = 160;
parameter multipleConversion = 0;
parameter [2:0] capTune = 1;

reg  enable1,  enable2,  comp1,  comp2,  toggleVinVo,  startAD,  readyMux1,
readySample1, ovrCrt, init;
reg [14:0] counterOffTime ;
reg [17:0] offTimeRef;
reg signed [20:0] error1, error2;
reg [9:0] counterOnTime;
reg [7:0] Vin, Vo, Ip, divDenom;
reg [20:0] integVin;
reg [1:0] selMux, selMuxOld;

wire readySample, readyMux, Latch;
wire [7:0] ADout, divTuneOut;
wire [9:0] dOffMax;
wire signed [20:0] error, errorT, error0, errorT20n;

always @ (negedge nResDig)
 begin
   state <= #1 off;
   selMux <= #1 2'b00;
   selMuxOld <= #1 2'b00;
   counterOffTime <= #1 0;
   offTimeRef <= #1 0;
   counterOnTime <= #1 0;
   integVin <= #1 0;
   Vin <= #1 0;
   Vo <= #1 0;
   Ip <= #1 0;
   toggleVinVo <= #1 0;
   startAD <= #1 0;
   enable1 <= #1 0;
   enable2 <= #1 0;
```

```
   comp1 <= #1 0;
   comp2 <= #1 0;
   divDenom <= #1 0;
   readyMux1 <= #1 0;
   readySample1 <= #1 0;
   ovrCrt <= #1 0;
   error1 <= #1 0;
   error2 <= #1 0;
   init <= #1 0;
 end

always @ (posedge clock)
begin
  enable1 <= #1 enable;
  enable2 <= #1 enable1;            //synchronized version of enable signal
  comp1 <= #1 comp;
  comp2 <= #1 comp1;                //synchronized    version    of    the
comparator signal
  readyMux1 <= #1 readyMux;         //readyMux  corresponds  to  ADC  sample
signal
  readySample1 <= #1 readySample;   //active  after  100ns  from  readyMux  -
settling time for sampled signal

if (~enable2 & enable1) // Start procedure
  begin
    state <= #1 off;    // Start in OFF state
    init <= #1 1;       // Set the init flag to load the tune registers
    counterOnTime <= #1 0;    //Clear ON time counter
    startAD <= #1 1;          //Start ADC
    toggleVinVo <= #1 1;            //Set the Vin/Vo selMux flag
    divDenom <= #1 122;
    offTimeRef <= #1 150;
  end

if ((state == on) && (enable2 == 1))
     begin
           //integrate the on time duration
      integVin <= (integVin[20:n]   < refOnTime[20:n] + 400) ? integVin +
(K1*Vin - (10*Vo + K2)) : integVin;
      counterOnTime <= #1 counterOnTime + 1;          //increment  on  time
copunter
        if (readyMux & ~readyMux1)        //when  the  ADC  is  ready  for
sampling
          begin
            selMux <= #1 selIp;           //set  the  multiplexer  to  sample
the input current
            selMuxOld <= #1 selMux;       // store the previous position of
the mux (Vin or Vo)
          end
      if  (((readySample  ==  1)  &&  (comp2  ==  1)  &&  (counterOnTime  >=
minOnTime)) || (counterOnTime >= maxOnTime))
            begin                         //Transition fron ON to OFF state
               if ((counterOnTime == minOnTime) && (comp2 == 1))  //If comp
is set before minOntime
                    ovrCrt <= #1 1;       //Set the overcurrent flag
                  else
                    ovrCrt <= #1 0;       //Clear the overcurrent flag
               state <= #1 off;                 // Switch to OFF state
               counterOffTime <= #1 0;          // Reset OFF counter
               Vin <= #1 (selMuxOld == selVin) ? ADout : Vin;     //Save
the result of the ADC conversion
               Vo <= #1 (selMuxOld == selVout) ? ADout : Vo;      //Save
the result of the ADC conversion
```

```
              startAD <= #1 1;                          // Generate pulse to
switch the AD from sample to hold and start conversion
            end
             else
            begin
               startAD <= 0;              //   Keep   sampling   Ip   until
readySample ==1 and comp == 1
            end
     end


if ((state == off) && (enable2 == 1))
   begin
       counterOffTime   <=   #1   counterOffTime   +   1;          //increment
counterOffTime while state == off
       if (readyMux & ~readyMux1)
         begin
           selMuxOld <= #1 selMux;              //Store     the     previous
position of selMux
           selMux <= #1 (~toggleVinVo) ? selVout : selVin;  //
           toggleVinVo <= #1 ~toggleVinVo;      //Toggle      the      VinVo
conversion flag
        end
       if (readySample && ~readySample1)        //  If  the  ADC  sampling  is
ready
          begin
            Ip <= #1 (selMuxOld == selIp) ? ADout : Ip;      //Save     the
aquired sample
            Vin <= #1 (selMuxOld == selVin) ? ADout : Vin;
            Vo <= #1 (selMuxOld == selVout) ? ADout : Vo;
          if (selMuxOld == selIp)                     //Compute   the   new
value of offTimeRef
            if (ADout > 223)
              offTimeRef <= #1 offTimeRef + dOffMax;
                else
              if ($signed(offTimeRef) + error < minOffTime)
                 offTimeRef <= #1 minOffTime;
               else
                 offTimeRef <= #1 $unsigned($signed(offTimeRef) + error);
          end
      if (readySample && ((counterOffTime >= minOffTime) && (counterOffTime
>= offTimeRef)))    //If end of the OFF cycle
          begin
            state <= #1 on;               //switch to on state
            init <= #1 0;                 //Clear init flag
            counterOnTime <= #1 0;        //Reset ON time counter
            startAD <= #1 1;        //Start ADC
            integVin <= #1 0;               //Reset the integrator
          end
         else
          startAD <= #1 0;
   end

end
assign  error  =  errorT20n  <  -($signed(dOffMax))  ?  -($signed(dOffMax))  :
errorT20n < $signed(dOffMax) ? errorT20n : dOffMax;
assign error0 = ($signed(refOnTime) -$signed(integVin)) >>> 1;
assign errorT = (error0 >>> 1) + (error0 >>> 2) + (error1 >>> 3) + (error2
>>> 3);
assign errorT20n = errorT >>> n;
assign dOffMax =  50 + (Vo<<1) < 400 ? 400 - (Vo<<1) : 50;        // If 400
- 2*Vo is greater than 50, set the dOffMax to 400 - 2*Vo, else 50
assign #1 nResAn = (enable2 & ~enable1);
```

```
assign divTuneOut = (init) ? {capTune[0], capTune[1], capTune[2], 5'b00000}
: divDenom;
assign LatchDiv = (init) ? 0 : Latch;
assign LatchTune = init;
ADcontrol ADcontrol1 (sampleAD, clockAD, readySample, ADout, sInDiv, Latch,
startAD, sIn, divTuneOut, state, clock, nResDig);
assign readyMux = sampleAD;
endmodule
```