Locally Erasable Couplers for Optical Device Testing in Silicon on Insulator

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***Abstract*—Wafer scale testing is critical to reducing production costs and increasing production yield. Here we report a method that allows testing of individual optical components within a complex optical integrated circuit. The method is based on diffractive grating couplers, fabricated using lattice damage induced by ion implantation of germanium. These gratings can be erased via localised laser annealing, which is shown to reduce the outcoupling efficiency by over 20 dB after the device testing is completed. Laser annealing was achieved by employing a CW laser, operating at visible wavelengths thus reducing equipment costs and allowing annealing through thick oxide claddings. The process used also retains CMOS compatibility.**

***Index Terms*—Gratings, optical components, optical couplers, optical coupling, optical diffraction, optical planar waveguide couplers, periodic structures.**

I. Introduction

SILICON photonics has grown significantly in the past decade, adapting to suit a diverse range of applications.

A wide range of integrated components can now be realised, including high speed modulators [1]–[4], low cost photodetectors [5], [6], and monolithically integrated lasers [7]. Autonomous wafer scale testing is one of the few remaining challenges for a successful silicon photonics platform to be realised.

Processed silicon has a relatively high cost associated with it. If a fabrication error occurs, the early identification of the problem could lead to significant cost savings.

Maximising wafer yield is essential for cost reduction and introducing silicon photonics to the mainstream [8], yet currently very few options are available to ensure the integrity of an optical device until the device is fully processed and functional. Test points are essential in allowing optical circuits or individual components on a wafer to be autonomously tested after selected manufacturing steps, hence allowing poor performance or device failures to be detected early so that either production can be ceased or the damaged device repaired using direct write methods [9]. Optical assessment could be performed under a microscope by an operator or a computer vision system, though this would be expensive and time consuming in a manufacturing environment and would only provide basic information.

Grating couplers were first demonstrated by Dakss *et al.* [10]. They offer the ability to couple light into or out from a waveguide at intermediate points along the optical circuit, allowing for autonomous testing at a component level. However, grating couplers in the silicon on insulator platform are traditionally fabricated using a surface relief approach [11]–[13]. It is impractical to remove gratings fabricated using this approach after testing, resulting in significant residual losses in the optical circuit due to the fabricated test point. In 2008 a method was suggested of incorporating a metal grating coupler directly onto the end of a fibre facet rather than etching the grating into the waveguide surface, effectively creating an optical test probe [14]. The probe has limited durability due to the fragile nature of the unprotected metal thin film, and the probe must be placed within 200 nm of the waveguide surface to achieve efficient coupling. Such close proximity thus prevents testing if the waveguide is coated with any cladding and could result in the samples being contaminated with gold, preventing this technique from being used in CMOS fabrication facilities, though other materials may be used to overcome this issue. Later in 2011 a CMOS compatible wafer scale testing methodology was presented utilising erasable Bragg reflectors [15], [16]. Bragg grating reflectors reflect light back along a waveguide and data can be collected by connecting the input fibre to a detector via a circulator, opposed to grating couplers which allow light to be directly coupled out of the waveguide. Erasable Bragg reflectors have the potential to offer a useful wafer scale testing methodology for devices spanning a small wavelength range, with typical erasable Bragg reflectors offering up to a few nanometers wavelength reflectivity, though wider channels could be interrogated using longer Bragg reflectors, lengths of ~400–600 μm per nanometre of required bandwidth would be required [16]. The other disadvantage to monitoring a reflection is it may not depict the operation of devices which have asymmetrical transmission characteristics accurately, such as optical modulators. However, by moving to a scheme using an erasable grating coupler, the single pass transmission characteristics can be easily obtained. Unlike Bragg reflectors, grating couplers direct light towards

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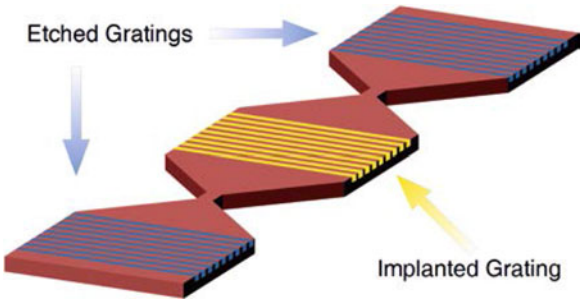

Fig. 1. Bow tie silicon waveguide structure for characterising erasable gratings. The end coupling regions represent surface relief gratings, the middle grating region represents an erasable implanted coupler.

the superstrate as opposed to relying on transmitting a reflection back through the circuit to the input surface relief grating coupler to obtain the test data. Grating couplers are relatively easy to fabricate and they allow light to be coupled out from any location on the device without the need for polishing, thus making them a good candidate for an optical test point. Implanted grating couplers have previously been demonstrated with coupling loss of 5.5 dB per coupler [17].

In this paper we demonstrate the components of a wafer scale testing platform using ion implanted diffractive grating couplers. The couplers are formed by modulating the effective index of the waveguide by using alternating regions of amorphous and crystalline silicon. The amorphous silicon regions have been measured by ellipsometry, the results show a Δn of 0.48 between crystalline and amorphous silicon [17]. The implanted grating enables testing of the optical circuit, and the grating is subsequently removed using localised laser annealing techniques to restore the low loss characteristics of the waveguide.

II. Testing Methodology

Simply characterising the output of an erasable grating coupler to show the performance of the device before and after annealing is a very crude measure of the erasability and does not tell the whole story. Using only direct measurements would require measuring an absence of light if the grating coupler was erased successfully. Absence of light could be caused by operator errors such as reduced alignment accuracy, a shift of the operational wavelength of the grating coupler or coupling the power to other leaky modes due to a refractive index change.

For this reason the concept of a bow tie structure is introduced as shown in Fig. 1. This structure allows the erasable grating to be considered as a three port device empirically and characterised in a controlled manner. Specifically optical characterisation can be performed for the case of: (i) coupling into a conventional etched grating coupler and outcoupling through the implanted grating coupler and (ii) coupling from one conventional etched grating (input) to the other (output). A successfully erased device will show both a substantial decrease in the optical power in the etched grating to implanted grating transmission (case i), and an increase in optical power in the etched grating to etched grating transmission (case ii), when compared with pre-annealed measurements.

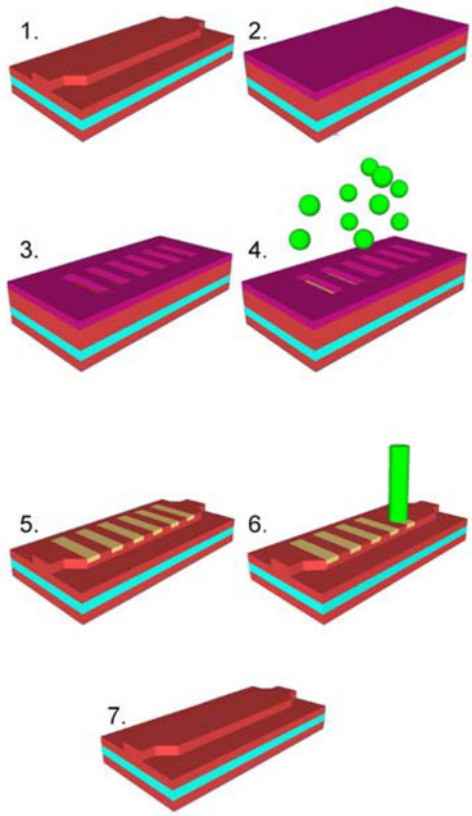

Fig. 2. Device fabrication process: 1. Waveguide etch, 2. resist spin, 3. Pattern & develop resist, 4. Introduction of lattice disorder via Ge ion implantation, 5. Resist removal and optical circuit testing, 6. Laser annealing, 7. Grating removed, waveguide operational regime.

III. Grating Fabrication and Removal Process

A critical element of wafer scale testing is simple, reliable processing. The processing steps used are shown in Fig. 2.

Initially the waveguide is fabricated and then ZEP 520 A e-beam resist is spun onto the wafer surface at 2000 rpm to achieve a resist thickness of 500 nm. The waveguide sections are comprised of a 220 nm thick silicon wire waveguide with a 400 nm width to ensure single mode operation; the buried silicon dioxide layer has a thickness of 2 μm. The waveguide grating width is increased to 10 μm via a dual step taper to maximise the overlap integral between the fibre and grating modes, and to facilitate straightforward alignment between fibre and waveguide. The taper flare angle from 10 to 3 μm is set at 0.6° and the angle from 3 to 400 nm at 0.2°.

Electron beam lithography is used to pattern the resist, which is subsequently developed before the entire structure is implanted with germanium ions using a dose of 1×10^{15} ions cm^{-2} to ensure amorphisation [17]. The implantation energy is varied depending on the required depth of amorphisation. Following implantation the resist is removed using a 3 stage solvent clean of acetone, isopropanol and deionised water for 2 min. per bath in the listed order, followed by a 10 min. O_2 plasma ash process. The oxygen plasma ash was performed at 200 °C with an oxygen flow rate of 800 mL/min using an RF

power of 800 W. The amorphous grating can be tested an unlimited number of times during other manufacturing stages of the optical circuit. However, exposure to extreme heat (above 500 °C) for extended periods of time may reduce coupling efficiency [18]. After testing, the grating can then be erased from the optical circuit via an annealing process, with an aim of returning the circuit to its peak performance, with no residual deficiency caused by the testing process. Annealing can either be carried out in an oven at a minimum temperature of 500 °C or by a laser. Using oven annealing is not desirable as the heat applied may cause damage to other fabricated devices and therefore to the whole circuit. Laser annealing offers an advantageous localised annealing method which does not affect other fabricated devices.

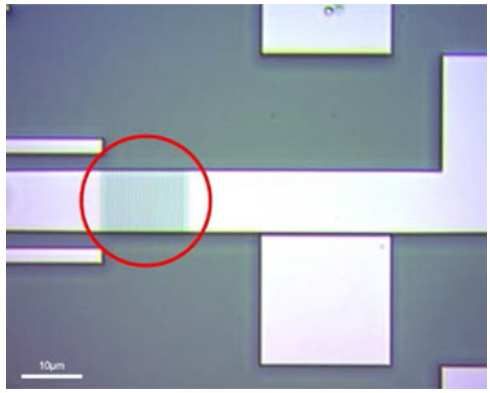

Fig. 3. Microscope image of an implanted grating before annealing.

IV. Laser Annealing

Implanted Bragg reflectors have been demonstrated previously by our group, the characteristics of the Bragg reflectors were successfully removed by laser annealing over an area of 3 mm^2 using a nanosecond pulsed deep ultra violet (DUV) laser source with a central wavelength of 248 nm [16], [19]. In this work, the implant profile required is more than 6 times deeper than that of the low implantation energy Bragg grating work [16]. The deeper implant will require more thermal energy for successful annealing and hence more care must be taken to avoid ablation of the surrounding silicon when annealing the larger volume of amorphous silicon.

Analysis of the absorption coefficients for amorphous and crystalline silicon, showed that at the 248 nm laser wavelength used by Loiacono *et al.*, both allotropes of silicon have similar absorption coefficients of 1.65×10^8 and 1.83×10^8 cm^{-1}, respectively. This means the laser must be very stable and operate within a very small power tolerance to ensure the amorphous silicon is fully annealed, whilst not causing deformation to the crystalline silicon by softening or ablation. The continuous-wave (CW) laser used in this work allows annealing with much lower peak powers than pulsed sources which reduces the risk of ablation considerably and also delivers greater power stability. It is worth noting that using lateral crystallization techniques, amorphous silicon films regrown using CW lasers have demonstrated larger silicon crystal grain sizes with fewer defects than those obtained by pulsed sources, resulting in higher quality poly-silicon, which is attributed to the lower cooling rate after laser irradiation from CW sources [20]. A further change in this work is a shifting of the annealing laser wavelength from 248 to 488 nm so that the absorption coefficient of amorphous silicon is now 40 times larger than that of silicon, at 4.10×10^7 and 1.02×10^6 cm^{-1}, respectively. Thus we expect the longer wavelength CW source to allow for a substantially greater power tolerance, rendering the annealing process more robust.

Another factor to consider when developing an annealing process for silicon is its relatively high thermal conductivity of 149 W m^{-1} K^{-1}. A high thermal conductivity means that the choice of process parameters depends critically on the dimensions of the silicon device being annealed. Conditions suitable for annealing a 10 μm wide grating structure may burn a 400 nm wide waveguide due to different rates of heat dissipation. For this reason, annealing conditions are strongly device specific. Shifting to a continuous wave laser at 488 nm gives a host of additional benefits other than less stringent power requirements, such as higher availability and lower costs of laser sources, cheaper focusing optics and the potential at this wavelength to anneal through a $\mathbf{SiO_2}$ cladding.

To erase the implanted grating coupler a laser exposure was performed over the grating region in a raster scan pattern to ensure a regular crystal growth direction [21]. To achieve the raster scan pattern the sample was moved with respect to the laser. A 488 nm CW laser set to a power of 180 mW was used for annealing the grating. The laser passed over the sample with an effective scan rate of 10 μm/s. The laser spot size was measured to be $\sim$1.5 μm with the separation between adjacent scans set to 0.5 μm, such that there was an overlap width of $\sim$1 μm between successive scans. The large overlap ensures uniform melting of the surface by the Gaussian shaped beam. The laser scan was perpendicular to the waveguide and the path used for annealing extended 20 μm beyond either side of the waveguide. The purpose of the extra distance effectively travelled by the laser was twofold; the excess distance removed any effects of acceleration in the sample movement, ensuring a constant velocity (and therefore constant exposure) over the grating region undergoing the annealing process and also prevented excessive heating of the waveguide due to the increased dwell time encountered during the changes of direction in the raster pattern. In an optimized annealing process, the 20 μm exposure extending beyond the grating coupler to be annealed could be reduced or potentially even removed by using a beam stop to block the laser beam during a change of direction or speed. Optical microscopy images of the implanted grating region were taken before and after laser annealing as shown in Figs. 3 and 4, respectively.

In Fig. 3 the implanted grating is clearly visible on the waveguide section before annealing. After annealing the optical contrast of the grating is significantly reduced, a grating is barely visible in Fig. 4. However, a faint grating does remain after annealing which may suggest residual cross-linked resist remains on the wafer surface or that some of the more complex defects at the waveguide surface have not been removed.

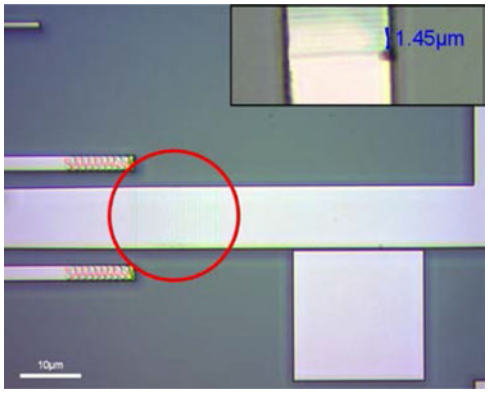

Fig. 4. Microscope image of an implanted grating after annealing. The inset image is a demonstration of the locality of the anneal with a single laser pass showing an annealing linewidth of 1.45 μm.

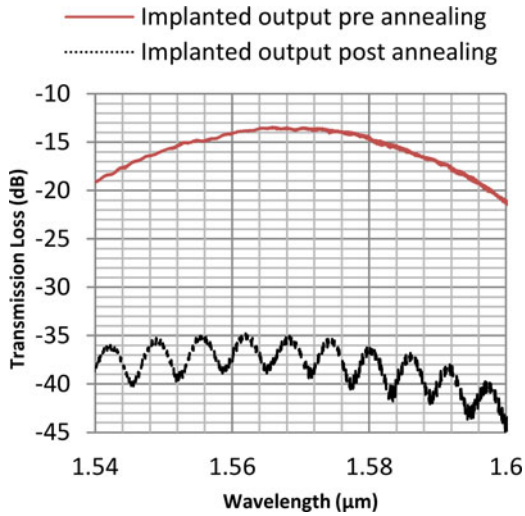

Fig. 5. 100 KeV implanted grating coupling before and after annealing a 100 KeV, 1×10^{15} ions cm^{-2} grating.

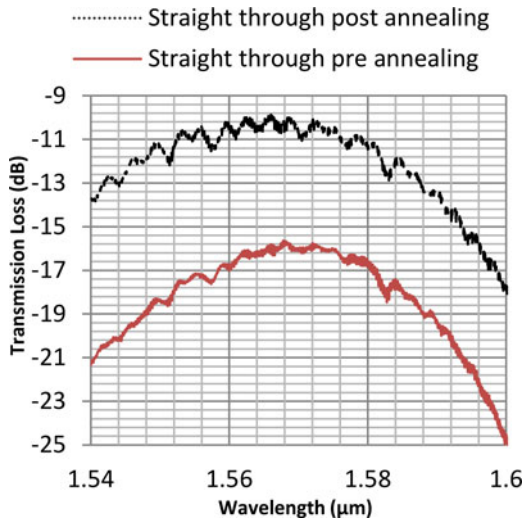

Fig. 6. Fixed couplers end to end performance before and after annealing a 100 KeV, 1×10^{15} ions cm^{-2} grating.

For a wafer scale testing mechanism to be practical, the locality of the annealing process is critical. The high temperatures required for the recrystallization of silicon would be catastrophic to many fabricated devices such as modulators, germanium detectors or some metalisation layers. Hence rendering the wafer scale testing methodology useless if the anneal was applied to the whole circuit.

To demonstrate localised annealing, a single laser pass over an implanted grating was performed and stopped before reaching the end of the waveguide as shown in the inset image of Fig. 4; this shows an annealed linewidth of $\sim$1.45 μm, which indicates that the heating is indeed localized to within the laser spot of $\sim$1.5 μm. A 1.5 μm annealing linewidth allows a gradual performance reduction of the implanted grating. Assuming a 600 nm period, a single grating period could be removed by starting at one end of the grating and overlapping only $\sim$30% of the laser spot with the device.

V. Grating Characterisation

Using the bow structure described earlier, there are two important data sets required to demonstrate successful laser annealing. Firstly the implanted grating performance before laser annealing was measured, followed by measuring the performance after the grating anneal has taken place. The results of these measurements are shown in Fig. 5. Then it is important to demonstrate that transmission through the annealed region has increased by measuring the throughput of the device before and after annealing, these results are shown in Fig. 6. All results have been collected from an implanted grating coupler with a period of 600 nm. The results have been normalised to a standard transmission measurement of the optical setup, which excludes the device under test (see Fig. 1). The etched grating couplers used in this work have a coupling loss of 4.5 dB per coupler. The implanted couplers used in this work have a coupling loss of $\sim$6.8 dB per coupler, though implanted couplers have been demonstrated elsewhere operating at 5.5 dB per coupler [17].

It is clear that annealing has dramatically affected the implanted grating outcoupling performance, with a 21 dB attenuation observed in the collected output laser power. After annealing the implanted coupler offers a peak performance of -35 dB per coupler and a clear periodic response occurs in the spectrum as shown in Fig. 5. The free spectral range ($\Delta\lambda$) of the spectral peaks is 7 nm. The cause of this is likely to be a Fabry-Pérot cavity forming within the setup, or the device. The length of a Fabry-Pérot etalon can be expressed in terms of the free spectral range of the periodic response using the equation

$$l = \frac{\lambda_0^2 - \lambda_0 \Delta\lambda}{2\Delta\lambda n_{\text{eff}} \cos\theta} \tag{1}$$

where θ is the angle of propagating light through the cavity, which for a waveguide is 0. Also, as the correctional term in the numerator of $-\lambda_0 \Delta\lambda$ gives an adjustment of less than one percent of the final value, it can be ignored for practical purposes,

resulting in the simplified equation

$$l = \frac{\lambda_0^2}{2\Delta\lambda n_{\text{eff}}}. \quad (2)$$

Assuming that the refractive index of the annealed silicon region is 3.48, the effective index of the 10 μm waveguide is 2.84. At the transmission central wavelength (λ_0) of 1.57 μm, the cavity length is calculated to be 62 μm. This length is of the same order as the 50 μm length of the middle section of the bow tie, which indicates the cavity is formed from reflections originating from the tapers either side of the central region. We note that other circuit components can be discounted as they are considerably longer than the cavity length calculated from the resonance observed. To verify this hypothesis, test structures with the central region replaced by single mode waveguide were measured, and these structures did not show the resonance observed in the annealed bow-tie structures. Furthermore it is reasonable to assume that the cavity length may be effectively extended beyond the 50 μm central section by 6 μm in both directions by an initial low reflection region in the 0.6° flare angle taper. This highlights the importance of considering the effects of Fabry-Pérot resonant cavities, which may remain after grating erasure without careful device design. In future iterations such resonance features will be removed by using improved tapers.

The inability to couple light out of the implanted coupler does not, however, give the full picture. To ensure the grating has been efficiently removed, it is essential to check that the throughput of light power increases after grating removal. This measurement also allows any additional loss introduced by the implantation and annealing process to be characterised. Fig. 6 shows the fixed end-to-end coupler response increasing by 5.7 dB following annealing, clearly showing the grating was annealed.

After annealing the implanted grating, it is possible a residual loss will exist in the in the transmission spectrum of the annealed region. To estimate any residual loss contributions, measurements were also conducted on a control bow tie structure that has not been implanted and subtracting this from the loss measured through a bow tie structure with an implanted grating which has been annealed. However, we found that the residual loss contributions were within the accuracy of the measurement system, which is approximately 0.7 dB. A more accurate measurement would test a cascade of erased test points, which we will consider in future work. We note that residual losses could potentially arise within the process such as an increase in surface roughness from sputtering during implantation or laser ablation during annealing or alternatively a decrease in material quality.

To investigate material quality, Raman spectroscopy has been performed on the annealed material as shown in Fig. 7.

Comparing the measured Raman spectra with characterisation data obtained for amorphous semiconductors from [22], shows the successful formation of amorphous silicon prior to annealing, highlighted by rounded peaks at 140 and 480 cm^{-1}. Using the same characterisation data it is also important to highlight an absence of peaks at 75 cm^{-1} or in the vicinity of 270 cm^{-1}, which show the material is not significantly impacted by the choice to use germanium for amorphisation. This

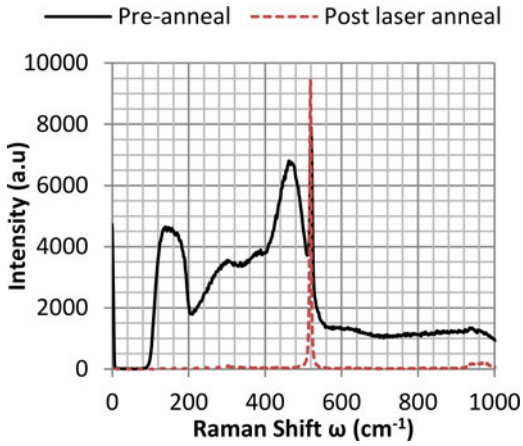

Fig. 7. Raman spectra of Ge implanted silicon before and after annealing.

is not surprising as the refractive index change is caused dominantly by lattice disorder, with simulations indicating that 2215 vacancies are created on average in crystalline silicon per germanium ion implanted at 100 KeV. Based on the implantation conditions the atomic percentage of germanium present in the implanted grating crenel can be calculated. For a 10 μm wide, 600 nm period grating with a 0.5 duty cycle, the atomic percentage of germanium is only 0.045%, and diffusion effects during annealing may make this value up to four times lower in the post annealed case. A germanium peak is observed in the post-annealing Raman spectra at 302 cm^{-1}, however the low concentration present makes it difficult to observe on the graph presented in Fig. 7. The germanium and silicon intensity peaks are measured to be 112 and 9431, respectively.

A sharp peak is observed in Fig. 7 at 520 cm^{-1} both before and after annealing, showing a contribution from crystalline silicon before annealing. A crystalline peak is observed in the amorphous data due to the Raman spot size being slightly larger than the width of an amorphous grating period region (300 nm), as well as the Raman laser penetrating to the crystalline silicon waveguide beneath the implanted region.

Interrogating the same grating region with Raman spectroscopy post laser annealing shows clearly that only a single peak at 520 cm^{-1} exists. This demonstrates the amorphous regions have been successfully annealed. A Voigt fit applied to the spectrum taken on the annealed material reveals a Lorentzian linewidth of 4.3 cm^{-1} compared to 2.7 cm^{-1} for single crystal silicon. This suggests the annealed silicon is in fact polycrystalline, which has a higher loss than single crystal material. It is likely that the annealing process can be further optimised to improve the quality of the regrown material.

VI. Summary and Conclusion

In this paper a novel method of grating coupler fabrication and local erasure to facilitate wafer scale testing has been presented. The method uses implanted grating couplers to couple light at intermediate points along the waveguide. Subsequently localised laser annealing is used to permanently remove the amorphous silicon grating after the device testing was completed.

This wafer scale testing method results in a waveguide with an unperturbed surface, and an optical circuit that is not impeded by the erased test point. After laser annealing the performance of the implanted grating decreases by 21 dB, while the transmission through the annealed regions increases by 5.7 dB when compared with the grating transmission performance before annealing. These results suggest that this is a very powerful wafer scale testing method that will directly enable an increased yield of optical integrated circuits when fabricating complex photonic designs.

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