Silicon photonic integration platform – Have we found the sweet spot?

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***Abstract*— The current trend in silicon photonics towards higher levels of integration as well as the model of using CMOS foundries for fabrication are leading to a need for standardization of substrate parameters and fabrication processes. In particular, for several established research and development foundries that grant general access, silicon-on-insulator wafers with a silicon thickness of 220 nm have become the standard substrate for which devices and circuits have to be designed. In this study we investigate the role of silicon device layer thickness in design optimization of various components that need to be integrated in a typical optical transceiver, including both passive ones for routing, wavelength selection, and light coupling as well as active ones such as monolithic modulators and on-chip lasers produced by hybrid integration. We find that in all devices considered there is an advantage in using a silicon thickness larger than 220 nm, either for improved performance or for simplified fabrication processes and relaxed tolerances.**

***Index Terms*—Integrated optics, silicon photonics, photonic integration, optical interconnect, optoelectronics.**

I. INTRODUCTION

From long distance telecommunication to intra-chip computer interconnects, the demand for data transport bandwidth continues to grow. To overcome the limitations of traditional copper-based technologies, optical solutions have penetrated ever deeper into the communications fabric [1, 2]. Further deployment of optical solutions requires that the new technologies satisfy similar demands facing the microelectronics industry: increased power efficiency, increased performance and reduced cost. To that end, silicon photonics has gained increasing acceptance as the platform of choice for photonic integration to meet the requirements in optical communications, with all components built on silicon-on-insulator (SOI) substrates through monolithic or hybrid integration [2-8]. Through the research of the last two decades, the performance of many discrete silicon photonic components has been improved to match or even out-perform that of their traditional counterparts [9-12]. In recent years, more effort has been directed towards the integration of multiple functions into photonic integrated circuits (PICs) on chip to realize the true advantage of silicon photonics [7, 13-16]. During the phase of optimizing individual components, the silicon waveguide structures have been chosen to meet the respective needs in each situation. For passive devices, modulators and photodetectors, the thickness of the silicon device layer typically ranges from 200 nm to 400 nm [9, 17-26]. The hybrid integration of III-V lasers using bonding techniques has been demonstrated by several groups [12, 27-29], but most are on SOI structures with a silicon thickness of at least 400nm in order to achieve efficient evanescent coupling between the laser and the silicon waveguide [30]. Since large scale integration is the ultimate goal of silicon photonics, a common platform that optimizes all considerations is the necessary starting point. Although waveguide widths can be easily modified across a photonic circuit, modifying the silicon thickness locally requires additional fabrication steps and often high precision alignments. The silicon thickness of the SOI substrates should therefore be carefully chosen by weighing the trade-offs between various factors.

Another important trend in silicon photonics is the emergence of fabrication foundries [31-34]. Due to the high cost associated with the fabrication of sophisticated state-of-the-art devices, many research labs and companies have adopted the fabless model and use speciality CMOS foundries that are publicly accessible to prototype their own designs. Cost saving is particularly significant for MPW (multi-project wafer) runs, allowing new players to enter the silicon photonics field at a modest expense, and accelerated the pace of research and development (R&D). Initial attempts of offering flexible choices for the silicon thickness in the starting SOI wafers have proven too costly. Now established silicon photonics foundries around the world, namely EpixFab (IMEC and LETI) and A*Star/IME, have converged to using SOI wafers with 220 nm thick silicon for their MPW runs [34]. Passive components, plasma dispersion modulators and Ge photodetectors are all offered on this platform. Consequently, this particular choice has become the de facto platform of photonic integration for much of the research community and small companies. Commercially available optical transceiver cables from Luxtera/Molex are based on

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SOI with 300-310 nm thick silicon, which was chosen to accommodate low loss compact passive devices and for a bulk-like transistor process [35, 36]. Silicon photonics development at Oracle is also based on this platform [37]. Even though the foundry service on this platform has been made available since 2011, it has not been widely adopted by the research community. Other strategies to deal with some of the conflicting requirements in integration are being explored, while the trend of 'standardization' is moving ahead. Economic analysis suggests that the incentive for using silicon photonics, i.e. the existing capital-intensive infrastructure in Si-CMOS, can also become its own demon. In CMOS manufacturing, competitiveness relies on high product volumes and manufacturing yield. At this juncture, we ask these questions: How can the requirements from key building blocks best be met with satisfactory trade-offs? Is there a 'sweet spot' in the silicon layer thickness that enables optimizing the performance of devices, minimizing fabrication complexities, and maximizing tolerances to the inevitable variations in fabrication? Are there important remaining issues? Have we, the silicon photonics community, found the 'sweet spot' for silicon photonic integration?

In this contribution, we examine the optimization considerations for passive and active components required in an optical transceiver for fiber links as a case study, since it is currently the main driver for silicon photonic integrated circuits (PICs). Requirements for chip-level computer interconnects share many commonalities, although it is sufficient to use one polarization since silicon waveguides are polarization maintaining. Our analysis is focused on the integration scenario of using monolithic silicon carrier-depletion modulators and hybrid lasers, a strategy seen as the path for near to medium term commercialization. State-of-the-art development of key building blocks is reviewed. We highlight their common as well as sometimes conflicting requirements on the silicon waveguide structures and the operating polarizations. In our discussions, we not only consider the device performance, but also pay particular attention to the fabrication tolerance. Research that emerged recently to address some of these concerns is reviewed. Potential alternative strategies to meet the diverging requirements in photonic integration are explored, with the intention of inviting debate and further exploration from the research community. We believe continued research in photonic devices over a range of dimension and material options is still vital to achieve far-reaching commercialization of silicon photonics and to provide guidance for evolving standardization.

II. OVERVIEW OF KEY COMPONENTS IN AN OPTICAL TRANSCEIVER AND KEY CHALLENGES

For data transport at all distances, the key components include filters/routers, lasers, modulators and photodetectors. Figure 1 illustrate the block diagram of a coherent optical transceiver with dual-polarization and quadrature phase-shift keying (DP-QPSK), as defined by the Optical Internetworking Forum (OIF), mainly considered for long-haul communications at present. A simple method for increasing data capacity is to split the input light into multiple channels and then encode each stream separately [38]. Multiple fibers are then used to capture the output signals. The wavelength-division-multiplexing (WDM) technique is often used to further increase the data capacity by combining signals carried on different wavelengths in a single transmission fiber, using multiplexers and demultiplexers. In the transmitter section, only one polarization is used for traditional on-off-keying signals, while for dual-polarization keying, the addition of polarization rotators (PR) and a polarization beam splitters (PBS, which also can serve as polarization combiners) right before coupling to the output fiber suffice to complete the function. For applications with a high data rate and a transmission distance of more than 1 kilometer, single mode edge emitting lasers are generally used. Since edge-emitting lasers launch light with transverse electric (TE) field, this polarization is the natural choice for the subsequent components such as the demultiplexers and modulators. In the receiver section, signals in all polarizations need to be recovered since the currently installed optical fibers do not maintain the orientation of the light polarization. Due to the high polarization dependence in sub-micrometer SOI waveguides associated with the high index contrast, the polarization diversity approach is generally considered to be the practical solution [7, 13]. For short transmission distance as needed e.g. in data centers, the use of polarization maintaining fibers may also be a viable alternative. In both transmitter and receiver sections, it is preferable to process the signals in only one polarization, typically TE.

Despite encouraging research outcomes in monolithic light sources using Ge or doped silicon [39, 40], a commercially viable laser based on group IV materials is still a distant prospect. Current development efforts are focused on using lasers made of III-V semiconductors. The lasers can be coupled to the silicon PICs by flip-chip bonding techniques at the die level [16]. A wafer level approach by bonding the III-V wafer at selective areas on the SOI substrate and then proceeding with laser fabrication has also been demonstrated by a number of groups [12, 28-30]. In this contribution we limit our discussion to the latter case which facilitates wafer level fabrication.

Photonic integrated circuits are pursued for optical communications to overcome the disadvantages of a discrete architecture, namely size, cost, power consumption and reliability. With the compact device size and potentially high level of integration enabled by the high index contrast in silicon waveguides, the cost of the PICs is largely determined by the fabrication facilities required, the complexity of the processes and the yield of all fabrication steps [41]. Due to insufficient control in the waveguide dimensions using current fabrication technologies that result in variability in the optical phase within devices, wavelength dispersive components are generally biased to the desired operating point by thermal tuning or using a p-i-n junction [35, 42, 43]. Device power consumption is therefore not only determined by the efficiencies of signal modulation and detection, it is also strongly affected, and at times even dominated, by the power necessary for biasing. Optical losses in waveguide transmission and laser-chip-fiber couplings increase the required laser output, further contributing to the overall power budget. In the following, design considerations to meet these

demands and the current status for key transceiver components are reviewed. Since a large fraction of the R&D work in silicon photonic has been centered in the 1550 nm wavelength range, we limit our discussions to this case only. Recently there is an emergence of interest for the 1310 nm wavelength range for applications in data centers. Even though the spirit of our investigation still holds, the preferred silicon thickness will obviously differ.

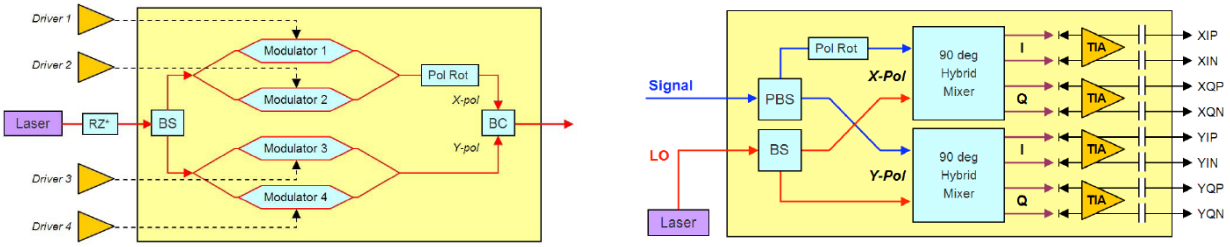

Fig. 1: Coherent transceiver modules. Left: Block diagram of a DP-QPSK transmitter module; Right: Block diagram of a DP-QPSK receiver module, shown with balanced detection and outputs. Source: www.oiforum.com (Optical internetworking forum).

III. PASSIVE COMPONENTS

Various filtering and routing functions can be realized using basic building blocks such as directional couplers, multi-mode interferometers (MMIs), micro-ring resonators (MRR), Mach-Zehnder interferometers, arrayed waveguide gratings (AWGs) and echelle gratings. In these devices important figures-of-merit include low insertion loss, precise channel wavelength and channel spacing, high extinction ratio, and high polarization discrimination. Tight waveguide bends with low radiation losses are needed for achieving compact device size and providing the desired free spectral range in some components such as ring resonators. All these properties are largely controlled by the waveguide cross-sectional geometry. In particular, the propagation loss is dominated by the modal overlap with interface roughness, and the accuracy of the operating wavelength is dominated by the waveguide size control.

There have been prior attempts to provide guidelines for global parameter optimization of silicon waveguide resonators based on similar design criteria: sufficiently large feature size, low sensitivity to dimensional variations, low loss and efficient thermo-optic tuning [44, 45]. The conclusion for TE polarization differs considerably from the conventional 2:1 aspect ratio typically used at present, identifying waveguides of 600×110 nm and 455×265 nm as the optimal choice for TE and TM respectively. Evidently, that recommendation for TE has not been adopted and is not appropriate for all class of devices. For example, a silicon thickness of 110 nm is not suitable for devices such as modulators which use rib structures for electric contacts. It is interesting to note that the identified structure for TM polarization coincides with a number of other works on biosensing and polarization rotators and splitters [18, 46].

In designing an integrated photonic circuit consisting of different components, there are a multitude of possibilities to handle the different trade-offs. It is not possible to single out a particular waveguide design that will optimize all components. On the other hand, there are only a few waveguide cross-sections that are widely used by the silicon photonics community. In the following, we compare the properties of these waveguides with three silicon thickness values which are the most common, i.e. 220 nm, 250-260 nm, and 300 nm.

A. Modal and polarization properties of waveguides

Silicon *wire* waveguides, where the sidewalls are etched to the buried oxide layer, have been the most commonly used for signal routing. The requirement for single mode operation limits the width of wire waveguides to below a few hundred nanometers. In this range, the effective indices are very sensitive to dimensional variations. In order to obtain acceptable control of the effective index and reduce the propagation loss while maintaining a small bend radius, rectangular wire waveguides with an aspect ratio of 2:1 are generally used for constructing the device portion of the circuits.

Electric field distributions of a wire waveguide are shown in Fig. 2 (a, b) for the TE and TM (transverse-magnetic) polarizations, respectively. Clearly, the TE mode has a large overlap with the sidewalls, while the TM mode has a large overlap with the top and bottom interfaces. Effective indices n_{eff} of the TE and TM modes as a function of waveguide width W are shown in Fig. 2(c, d) for waveguide height H of 220 nm and 260 nm, respectively. For an aspect ratio of ~ 2:1 as typically used, the fundamental TE mode is better confined than TM, having a larger effective index. For waveguides with H = 220 nm in a symmetric environment (SiO_2 as the upper cladding), the TM mode is supported theoretically for a waveguide as narrow as W ~ 200 nm. However n_{eff} is close to the index of the buried oxide layer and the guiding is weak. When the upper cladding has a different index than that of the buried oxide layer, or if the waveguide is in a small bend, guiding can be easily lost. For example for a waveguide with air cladding, TM is cut-off for W < 350 nm [47]. For devices with SiO_2 cladding, only a radius of large than 30 μm can ensure a low bend loss [65]. It was shown in early studies that TE is really the only useful polarization for this wire height, and it has been used extensively since [48]. Most foundries use this silicon thickness and supply input grating couplers for TE polarization. For larger silicon thickness, such as those shown in Fig. 2(d) with H = 260 nm, both TE and TM polarizations are well guided and can support a waveguide

bend radius of 5 μm with low loss. A range of components including modulators, polarization rotators/splitters and biosensors, with high performance employing either TE or TM mode, have been demonstrated using this slightly larger silicon thickness [18, 22, 25, 49, 50]. For wire waveguides with H = 300 nm, higher order modes are supported for W > 320 nm. Typically, rib waveguides with partially etched sidewalls are used.

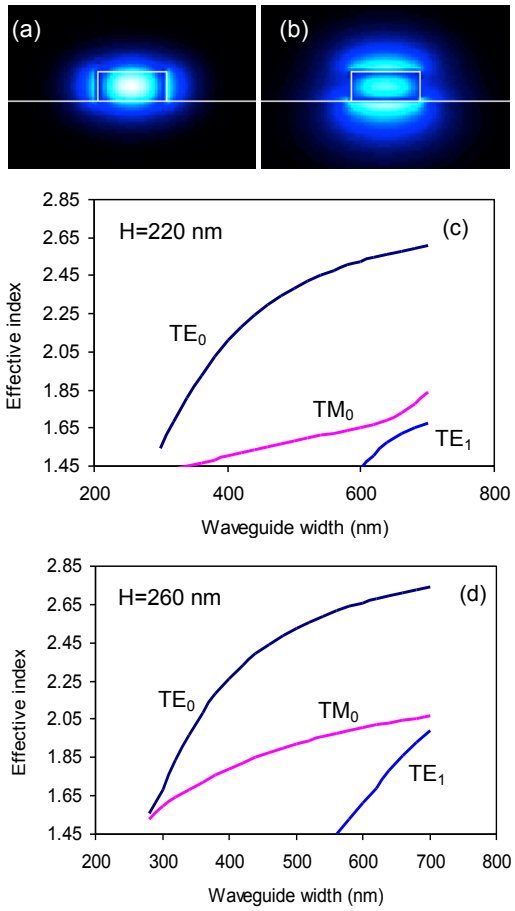

Fig. 2: Electric field distribution of silicon waveguides with a height H = 220 nm and a width W = 450 nm: (a) TE and (b) TM. The effective indices as a function of the waveguide width for (c) H = 220 nm, and (d) H = 260 nm. The wavelength is 1550 nm.

B. Phase accuracy and device reproducibility

For all interferometric optical components, accurate control of the waveguide propagation constant (i.e. phase) is the key for achieving high extinction ratio and reproducible device spectral performance. In silicon waveguides, the core material, being single crystalline silicon, has highly uniform material index. Therefore phase control in silicon devices essentially translates to controlling the waveguide cross-sectional and horizontal dimensions.

For SOI wafers commonly used in silicon photonics such as Unibond wafers by SOITEC, the silicon thickness of 150 mm and 200 mm wafers is only guaranteed to 3σ = ±10 nm as stated in the product specifications [52]. Recent wafer mapping found the uniformity to be somewhat better, with a 3σ non-uniformity of ± 6 nm [51] across the wafer. The wafer fabrication technology continues to improve. For 300 mm wafers which have recently been used for silicon photonics, the uniformity has reached a 3σ of ±1 nm [36, 55]. These data are summarized in Table I. This uniformity has come close to that for SOI wafers used for microelectronics (3σ = ± 0.9 nm), even though for much thicker silicon layers [52].

The in-plane dimensions of waveguides are determined by the mask technology, the lithography tool and etching processes. In current foundry services, DUV dry lithography using 248 nm or 193 nm light sources are available for 200 mm wafers. The size of CD (critical dimension) features is typically controlled to a 3σ accuracy of ±8 nm in 193 nm lithography [53, 54]. Linewidth uniformity for 248 nm lithography is considerably worse [53]. For other features of different widths and gaps, especially between areas with different pattern densities, dimensional controls are more challenging due to proximity effects. For either e-beam or DUV lithography, size deviations of up to ±10 nm from design are not uncommon. A few research and pre-commercial facilities have started processing silicon photonics circuits using 300 mm wafer fabs where 193 nm immersion lithography becomes available. Although the minimum CD is reduced 80 nm [36], the results reported so far only showed marginal improvement in absolute linewidth uniformity as summarized in Table I [54, 63]. This comes far short of the more than ×5 times improvement seen in the silicon thickness uniformity. Furthermore, these facilities are not yet publicly available. Coming hand-in-hand with higher precisions, such infrastructures are also much more costly. Wide spread use of such facilities requires even higher product volume to justify.

Table I: Statistical variations (3σ) for the best-in-class SOI wafers and silicon photonics fabrication technologies.

Wafer diameter	200 mm	300 mm
Lithography	193 nm dry litho	193 nm immersion litho
Linewidth uniformity	±7.8 nm [53, 54]	±7.6 nm [55]
Within-wafer thickness uniformity	±6 nm [53, 63]	±1 nm [36, 55]

The resonance wavelength of a ring resonator can be used to characterize the phase sensitivity of the constituent cavity waveguide. Figure 3 shows the spectral wavelength shift with respect to dimensional changes, defined as $\delta\lambda/\delta W = (\lambda/n_g)\delta n_{eff}/\delta W$ and $\delta\lambda/\delta H = (\lambda/n_g)\delta n_{eff}/\delta H$, where λ is the wavelength and n_g is the waveguide group index. For waveguides with typically used aspect ratio of 2:1, the TE mode is more sensitive to width variations, while the TM mode is more sensitive to height variations as one naturally expects. The expected 3σ variability in the resonance wavelength for resonators made by state-of-the-art 193 nm immersion lithography on 300 mm wafers is summarized in Table II for waveguide structures typically used. The linewidth and thickness uniformity data in Table I are used for these estimations. Clearly, such variations are still unsatisfactory for meeting the spectral requirements of most dispersive devices, not to mention integrating a large number of components. Currently, spectral tuning using thermo-optic

effect or current injection in p-n junctions is used to mitigate the problem. The associated power consumption and design complexity, however, pose severe limits on the transceiver performance and cost.

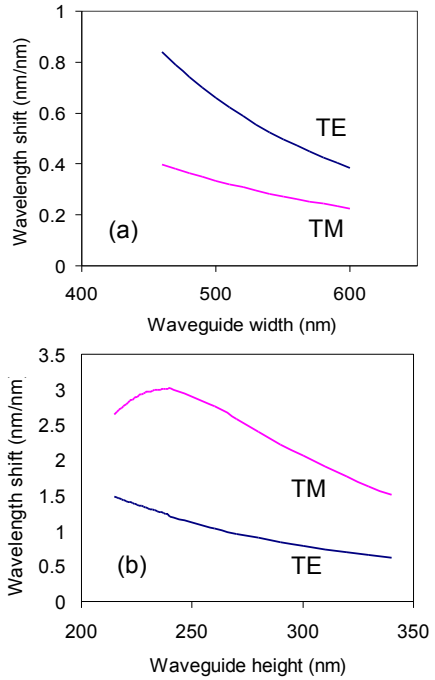

Fig. 3: (a) Wavelength shift $\delta\lambda/\delta W$ as a function of waveguide width for H= 260 nm; (b) Wavelength shift $\delta\lambda/\delta H$ as a function of waveguide height for W= 450 nm. Here the upper cladding is air and the wavelength is 1550 nm.

Different strategies can be pursued to reduce the tuning power. Comparing between the TE and TM polarizations with their respective limitations as shown in Fig. 3, we observe that $(\delta\lambda/\delta H)_{TM} \sim 3(\delta\lambda/\delta W)_{TE}$. This relation suggests that when the achievable dimension control is $\delta H < 3\ \delta W$, the use of TM polarization gives a higher degree of phase control. This requirement is already achieved for uniformity in 300 mm wafer technology. Furthermore, the thickness of the wafers can be mapped and corrected over the wafer by using location specific processing [58]. Although such thickness correction of SOI wafers requires additional processing, it is still beneficial for achieving systems with low thermal tuning power. To improve the phase precision of the TE polarization, however, requires even more stringent dimensional control than currently achieved in 193 nm immersion lithography, which appears to be unrealistic within the medium term. The control of in-plane dimensions is ultimately limited by the accuracy of the processing and metrology tools, which is presently at 2 nm. Given the recent development, we believe an even higher precision of silicon thickness control at the wafer manufacture source is at least a plausible improvement that may be achieved in the near or medium term.

Another strategy of improving phase accuracy is by introducing rib waveguides in the photonic circuits. Due to coupling to the slab TE mode, the TM polarization is not well supported in such geometries unless the etch is deep [59]. Both the rib width and the etch depth can be adjusted to alter the degree of modal confinement of the TE mode and the corresponding phase sensitivity. For signal transport, multi-mode straight waveguides can be adopted, but only single-mode waveguides are used in phase sensitive sections [57]. This imposes a trade-off between bend radius and phase sensitivity. Detailed characterization of two particular single-mode rib geometries has been reported, namely for waveguides with a height/width/etch depth of 220/450/70 nm [57] and 300/360/150 nm [37]. The corresponding calculated phase sensitivities are indicated in Table II. An etch depth precision of ±5 nm, now routinely obtained for 300 mm technology, is used. This represents a higher level of control compared to the ±10 nm variations observed in an 200 mm technology [8]. One can observe that the tolerance to width variations is improved in both structures compared to that for wires, but the calculated tolerance to the ±5 nm etch depth variation demonstrates that etch depth uniformity is an important issue for rib waveguides. In particular, for the case of 300/360/150 waveguides, the etch depth sensitivity is comparable to the width sensitivity of wires. It is the aspect ratio, not merely the rib height that determines the phase sensitivity [45].

Table II. Expected wavelength 3σ scatter $\Delta\lambda_{3\sigma}$ (in nm) due to dimensional variations for different waveguide structures made using state-of-the-art 193 nm immersion lithography. These values are obtained using simulated $\Delta\lambda/\Delta H$, $\Delta\lambda/\Delta W$ and $\Delta\lambda/\Delta D$, together with the dimensional uniformity data from Table I (i.e. $\Delta W_{3\sigma}$=±7.6 nm and $\Delta H_{3\sigma}$=±1 nm). An etch depth control of $\Delta D_{3\sigma}$= ±5 nm is assumed. Note that TM is only weakly guided for waveguides with a height of 220 nm.

Wire structure	**$\Delta\lambda_{3\sigma}$** (Wire-TE)		**$\Delta\lambda_{3\sigma}$** (Wire-TM)	
H / W (nm)	$\Delta\lambda_{3\sigma}(W)=7.6\times\Delta\lambda/\Delta W$	$\Delta\lambda_{3\sigma}(H)=1.0\times\Delta\lambda/\Delta H$	$\Delta\lambda_{3\sigma}(W)=7.6\times\Delta\lambda/\Delta W$	$\Delta\lambda_{3\sigma}(W)=1.0\times\Delta\lambda/\Delta H$
220 / 450	±6.6	±1.4	±2.8	±2.7
260 / 450	±6.4	±1.1	±3.0	±2.7

Rib structure - TE					
H / W / D	Minimum radius (μm)	Min. loss (dB/cm)	$\Delta\lambda_{3\sigma}(W)=7.6\times\Delta\lambda/\Delta W$	$\Delta\lambda_{3\sigma}(H)=1.0\times\Delta\lambda/\Delta H$	$\Delta\lambda_{3\sigma}(D)=5\times\Delta\lambda/\Delta D$
220 / 700 / 70	25	0.12 [62]	±0.8	±1.9	-/+1.8
300 / 360 / 150	10 [56]	2 [56]	±3.0	±1.5	-/+6.2

C. Waveguide propagation loss, back reflection and bend loss

In silicon waveguides, propagation loss is mainly due to scattering from the roughness at the core-cladding interfaces. In commonly used SOI wafers, the silicon surface is atomically smooth with an RMS of less than 0.1 nm. Waveguide sidewall roughness is determined by the lithography and etching processes and is typically on the order of a few nanometers, much larger than the surface roughness [60]. Even though post-processing steps such as re-oxidation of the waveguides have been used to reduce sidewall roughness, and fabrication technologies continue to improve (e.g. the use of immersion lithography), scattering remains the dominant cause of loss in silicon waveguides. For fully etched wire waveguides, the TE mode suffers a higher loss than TM because of its larger overlap with sidewall roughness [61]. For example, propagation losses of 2.4 dB/cm and 0.59 dB/cm are obtained for TE and TM mode respectively for waveguides made using 0.13μm CMOS technology (H=220 nm) [62]. This trend has been observed experimentally for H of 200 nm to 260 nm, showing the loss for TE is approximately 2 to 4 times of that for TM. Using 300 mm wafer technology (see Table I), the loss for TE has recently been reduced to a record low value of 0.7 dB/cm [63]. It should be expected that this improvement in sidewall roughness would also lower the loss of the TM mode proportionally.

Based on the argument of modal overlap with sidewall roughness, the loss in single mode wire waveguides with larger H is expected to be larger, but there has not been a direct experimental comparison reported. A number of studies have used rib waveguides with shallow etch to reduce the loss significantly. The modal confinement, controlled by both the etch depth and rib width, determines the overall loss. For single mode waveguides with H/W/D of 220/700/70 nm, a low loss of 0.12 dB/cm has been achieved using the 300 mm technology [63]. In waveguides with H= 300 nm made using the 200 mm technology, single mode waveguides of 360 nm width exhibited a loss of 2 dB/cm (after full CMOS processing), while 3 μm wide multi-mode waveguides showed a loss as low as 0.026 dB/cm (both with an etch depth of 150 nm) [37]. The price one has to pay for achieving these low losses is a much larger bend radius for using this type of geometry, or more complex layouts with rib-to-wire transitions, giving these structures each its own appropriate utility [57].

Back reflection can generate a variety of impairments in optical systems such as crosstalk and return loss degradation. This can severely hinder the application of silicon photonic components in many practical applications, although the reflection is only a small contribution to the forward transmission loss. Similar to forward propagation loss in waveguides, back reflection originates from sidewall roughness. Therefore they share similar characteristics and can be mitigated using similar strategies. For waveguides with a typical aspect ratio of 2:1, TE polarization experiences higher backscattering than TM by as much as 20 dB [61]. Backscattering can be resonantly enhanced in devices such as ring resonators and becomes the limiting factor for device performance [64]. This limits the quality factor to below 10^4 and resonance splitting is common. When the TE polarization is used in the circuit, one mitigation strategy is to locally use a resonant cavity in TM mode as demonstrated in [65]. However the design is complex and the waveguide dimension control is stringent. Alternatively, rib waveguides can be used with a larger bend radius. A simpler option is to adopt the TM mode as the general polarization in wire waveguides using a silicon thickness where the mode is well supported (e.g. H $\sim\geq$ 250 nm).

There has been extensive simulation work which shows that the bend loss for the TE mode is lower than that for TM polarization in wire waveguides [66-68]. Nonetheless for radii of larger than 5 μm, both polarizations give minimum bending loss [69-72], and high performance resonators have been demonstrated in TM polarization with a radius as small as 2 μm [72]. This range of radii can satisfy most circuit layout requirements.

Silicon is transparent not only in the near-infrared (NIR) but also up to a wavelength of $\lambda \sim 8$ μm and is potentially a viable material for mid-infrared (MIR) applications. Therefore, in addition to the intensive NIR research activity, MIR silicon photonics has become an increasingly interesting research area [73]. The MIR is a spectral region of tremendous scientific and technological interest. Spanning a large wavelength range (2-20μm), it contains strong vibrational signatures for a number of gases and molecules, and hence photonic devices that operate in this region can be potentially applied for a host of applications in gas, environmental, and bio-chemical sensing, industrial process control, defence and security sectors, or point of care diagnostics.

Silicon dioxide, which usually serves as a bottom cladding for NIR silicon photonic devices, has a high material loss for λ between 2.6 and 2.9μm, and beyond $\lambda \sim 4$ μm [74]. SOI is a desirable photonic material platform in the MIR regions with low SiO_2 absorption due to mature fabrication processes and the high material quality achieved over the last 20 years. To date, for the 2-4μm wavelength range, different SOI thicknesses have been used: from 220nm in [75] for wavelengths around 2.3μm, to 340nm in suspended structures [76], to 400 and 500nm in [77, 78]. To identify how waveguides of different thicknesses perform, we have simulated SOI wire waveguides across the 1.5-4μm wavelength range

Figure 4 shows the maximum width for single mode propagation for wire SOI waveguides with different silicon thicknesses for TE polarization. Points are plotted only where there is single mode propagation and propagation loss is below 2dB/cm, thus representing the transparency ranges of the platform. In the simulations, which do not take into account scattering losses, the cut-offs at longer wavelengths are mostly due to radiative losses stemming from waveguide geometry. For TM polarization, the dependence on silicon thickness is more severe, resulting in lower transparency ranges than for TE polarization. It can be seen from Fig. 4 that thicker Si layers can exploit the full SiO_2 transparency range up to 4μm, and therefore they would be preferred platforms for the MIR. If foundry fabrication for such SOI wafers becomes more readily available, it can accelerate the penetration of silicon

photonics into other product areas beyond optical communications.

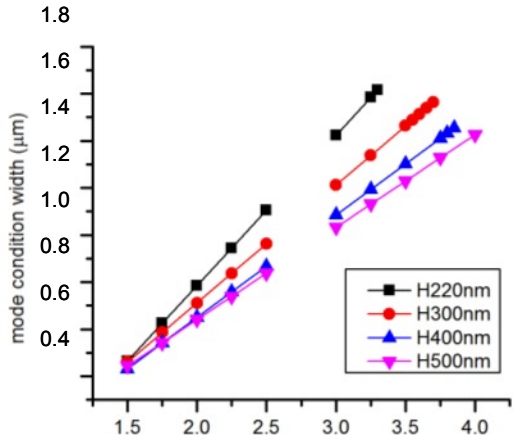

Fig. 4: Single mode width versus wavelength for SOI strip waveguides with different heights.

D. Evanescent coupling strength and losses

Directional couplers are commonly used as beam splitters in a variety of devices such as Mach-Zehnder interferometers and ring resonators. This device relies on the evanescent coupling of optical modes between two closely spaced waveguides. The coupling strength can be characterized by a coupling length L_x which is the length for full power transfer from one waveguide to the other [79]. For a coupler of physical length L_C, the power cross-coupling coefficient is $\kappa^2=\sin(\pi L_C/2L_x)$. An example of the coupling length as a function of the waveguide center-center separation is shown in Fig. 5(a). The coupling between TM modes is much stronger than that for TE at the same waveguide separation, with $L_x^{TE} \sim 10\ L_x^{TM}$.

To achieve a power cross-coupling coefficient of $\kappa^2 \sim 5\%$ using a coupler of 4 μm length with H=260 nm, the gap size required is 110 nm and 400 nm for TE and TM respectively. To obtain a similar coupling in TE for H =220 nm, the gap size is 140 nm. Obviously, a much narrower gap is required for TE polarization than for TM to achieve a given coupling strength. The fabrication of a TE directional coupler is therefore more challenging, suffering from proximity effects in the lithography process. Additionally, a significant mode-conversion loss occurs in resonators with small bend radius. A gap size of below 120 nm [80] or 200 nm [81] has been observed to cause significant coupling losses, depending on the bend radius used. By using the TM mode, this problem can be alleviated since a much larger gap can be used.

The coupling coefficient is also strongly affected by small dimensional variations or incomplete etching in the gap. If the etching is complete, the coupling variation generally comes from the waveguide width fluctuations. The center-center separation between the waveguides can be considered accurate. In this case, the coupling coefficient as a function of the waveguide width is shown in Fig. 5(b). The TM polarization is also observed to be slightly more tolerant.

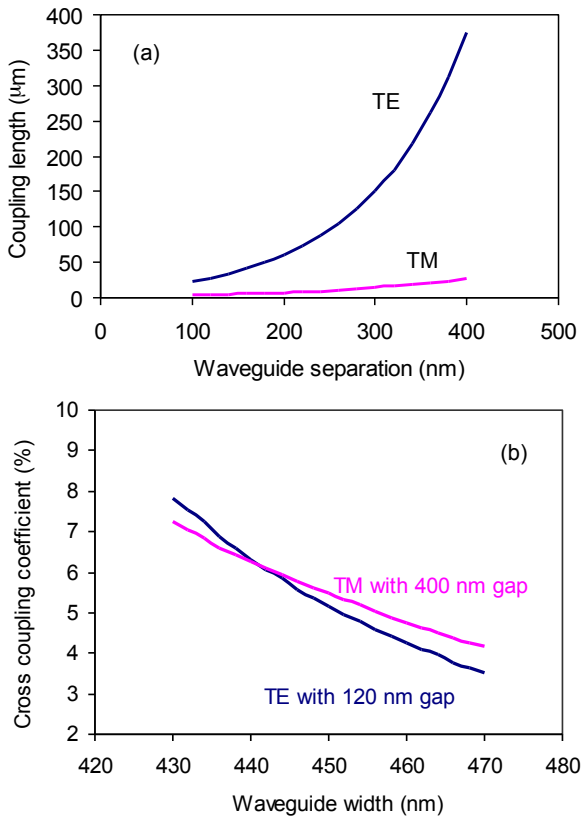

Fig. 5: (a) Coupling length L_x for full power transfer as a function of waveguide separation. Here H = 260 nm, W = 450 nm, the wavelength is 1550 nm and air is the upper cladding. (b) Cross-coupling coefficient as a function of the waveguide width, with the center-center separation kept at a constant.

E. Grating couplers

Grating coupling has been developed rapidly in the last few years for coupling light between optical fibers and silicon sub-micron-sized waveguides. Compared to the butt-coupling approach, grating couplers can be located anywhere on the chip with an out-of-plane coupling scheme. This increases significantly the flexibility in the circuit design, and also enables wafer-scale automated testing. Grating couplers also generally have larger tolerances in fabrication and alignment process than butt-coupling approaches. Here we focus on an analysis of the coupling efficiency, which is the key criterion for most applications. We found that the best coupling efficiency achievable for grating couplers is largely affected by the waveguide thickness.

For ease of analysis, we consider only light traveling from grating to fiber. The efficiency of light that is coupled in the opposite direction should be the same due to reciprocity. In order to maximize the coupling efficiency of a grating coupler, three issues have to be addressed. The first is eliminating the back reflection from the grating. The second is increasing the mode matching efficiency between the grating mode and the mode in the optical fiber. These two can be addressed by proper design of the grating structures, such as apodization [82-84], without complicating the fabrication process. The last one is enhancing the directionality, which is defined as the optical power coupling upwards towards the fibre, as a

fraction of the total coupled power. Typically, a significant portion of the light would be coupled into the substrate and lost. The back reflection and mode matching efficiency can generally be optimized to values approaching zero and unity, respectively, for most common SOI waveguide geometries by careful grating design. The overall coupling efficiency would then be limited only by the directionality. Theoretically, one way to improve directionality is by adding a metal or dielectric mirror underneath the grating coupler [85]. However, this is difficult to realize in practice. The optical resonance between the mirror and grating can also compromise the achievable optimum coupling efficiency.

A simple and effective way to enhance the directionality of the grating coupler is to optimize the etch depth of the grating, as has been proposed and demonstrated for micrometric SOI rib waveguides [86]. The directionality would be improved when there is constructive interference for coupling upwards and destructive interference for coupling downwards to the substrate. Here we perform two-dimensional FDTD simulations to calculate the directionality of gratings for SOI platforms with various waveguide thicknesses in the submicron range, and the results are plotted in Fig. 6. The directionality is found to change approximately sinusoidally with respect to the etch depth. More importantly, the best directionality achievable varies significantly for different waveguide thicknesses. We assume coupling to a 10 degree titled single-mode fiber (with 10.4 μm mode field diameter). The waveguide grating is embedded in a top oxide cladding, and the silicon substrate is not considered in the simulations. Therefore, no light interference from the buried oxide (BOX) layer is included. The fill factor of the grating is about 0.4, which is defined as the ratio of the shallow-etched groove width to the grating period. We find that the fill factor has negligible effect on the directionality. The grating periods are calculated for every combination of the top silicon thickness and grating etching depth according to the phase matching equation, to ensure a peak coupling wavelength of 1550nm. Only the TE mode is considered in Fig. 6.

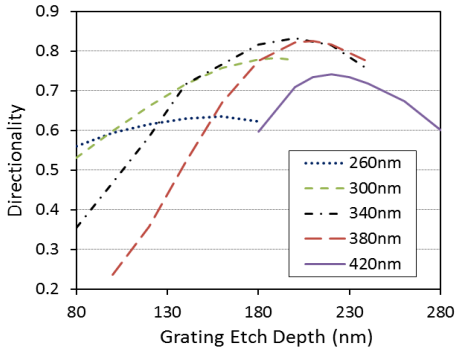

Fig. 6: Calculated directionality of gratings against grating etch depths for SOI platforms with various waveguide thicknesses.

More simulations are carried out to search for the best achievable directionality for SOI platform with various waveguide thicknesses and both TE and TM polarizations. The results are plotted in Fig. 7. We can see that for TE polarization gratings would have a peak directionality of 0.84 for ~350nm waveguide thickness. TM polarization gratings would have a peak directionality of 0.71 for ~330nm waveguide thickness. Although the directionality can also be improved by adopting a BOX layer with a proper thickness, or by adding dielectric layers on top, the optimization of waveguide thickness and grating etch depth gives a more significant improvement in directionality. Besides, all those parameters and techniques can be utilized at the same time to maximize performance improvement. Therefore, it should be recommended to choose a SOI platform with waveguide thickness around the peak value of the directionality as shown in Fig. 7 to optimize the coupling efficiency of grating couplers. One good example was presented in [87] where the coupling efficiency of a uniform grating was improved from 37% to 78% (or 1.5 dB), by adding a 150nm poly-silicon overlay to the silicon waveguide with 220nm thickness. This enhancement is due to the directionality change as shown in Fig. 7. Grating coupling efficiencies of 1.5 dB (at 1490 nm wavelength) and 1.9 dB (at 1550 nm) reported for SOI platform with 310 nm silicon thickness and optimized BOX thickness are supporting examples of this finding [36].

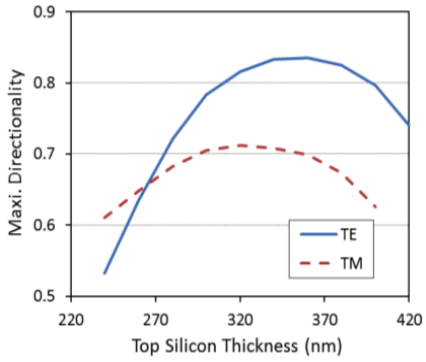

Fig. 7: The best achievable directionality for SOI platforms with various waveguide thicknesses for both TE and TM polarizations.

IV. CARRIER DEPLETION SILICON MODULATORS

Silicon optical modulators based upon carrier depletion have received significant research interest due to the potential for high speed operation, fabrication simplicity, and CMOS compatibility [22, 24, 88, 89]. The geometry of the waveguide in which the modulator is based has a significant impact on the device performance [90-92]. In this section we theoretically analyze with varying geometries the performance of the modulator in terms of its speed, loss and power consumption and polarization dependence.

The most popular configuration of carrier depletion modulator is shown in Fig. 8. It is based within a rib waveguide with the p-n junction positioned in the centre of the waveguide. Highly doped p and n type regions which are used to form ohmic contacts to the device electrodes are positioned in the slab regions to either side of the waveguide.

Even within this relatively simple design there are several variants aside from the waveguide geometry which affect the performance of the device. In this analysis we fix these variants using typical parameters as demonstrated in the

literature in order to perform a more general analysis of the device performance with different waveguide geometries. The slab height is fixed at 100 nm, the p and n type doping densities at 5×10^{17} ions.cm^{-3}, the p+ and n+ doping densities at 1×10^{20} ions.cm^{-3} and rib edge to highly doped region separation at 1000 nm.

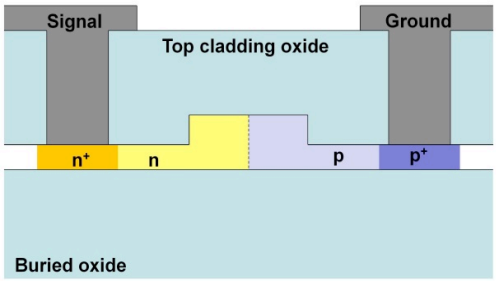

Fig. 8: Cross sectional diagram of a typical carrier depletion modulator.

A. Power consumption

The parameters which dictate the device power consumption depend on how the phase modulator element is driven. If traveling wave electrodes are used as typically is the case in Mach-Zehnder devices, a termination is required after the modulator which will dissipate all of the power not consumed by the modulator. Therefore the power consumption will depend only on the drive voltage. For devices driven as a lumped element which do not use a termination resistor, both the capacitance of the device and the drive voltage are important.

In both cases therefore, a low power consumption results when a low drive voltage is used. In order to minimize the drive voltage required the modulation efficiency of the device should be optimized. A large modulation efficiency results when a large overlap between the optical mode and the region of depleting free carrier occurs. The depletion width for a device with p and n type densities of 5×10^{17} ions.cm^{-3} and a reverse bias of 2V (CMOS compatible) is approximately 125 nm. Optical modeling has been used to calculate the fraction of the total optical power propagating in waveguides which overlaps with this 125 nm region in the centre of the waveguide for different waveguide geometries. The results are shown in Fig. 9 for the TE and TM polarizations. For the TE polarization the modal overlap with the varying depletion tends to increase with waveguide height in the range considered with an optimal waveguide width of approximately 350 nm. For the TM polarization the same trend in waveguide height is observed, however the optimal width is smaller (~300 nm).

The capacitance of the device is dependent on the doping density of the p and n type regions and the height of the waveguide since the area of the capacitor is effectively increased. The capacitance of the device for different waveguide heights can be theoretically calculated for the doping densities stated above. Figure 10 shows the theoretical junction capacitance per mm length at 0V for different waveguide heights (and widths). Although the capacitance is not dependent on the waveguide width a 2D plot is used to retain consistency with the other figures.

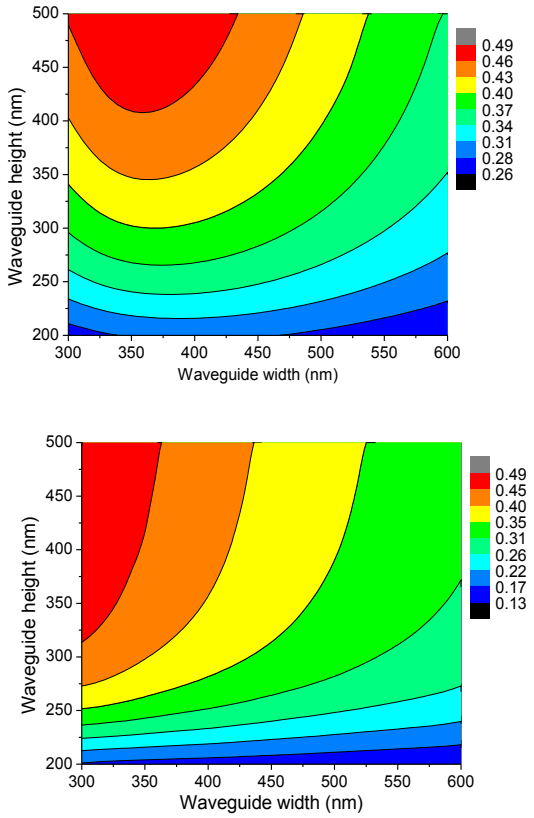

Fig. 9: Fraction of optical power propagating within a 125 nm slit in the middle of the waveguide for TE polarization (top) and TM polarization (bottom).

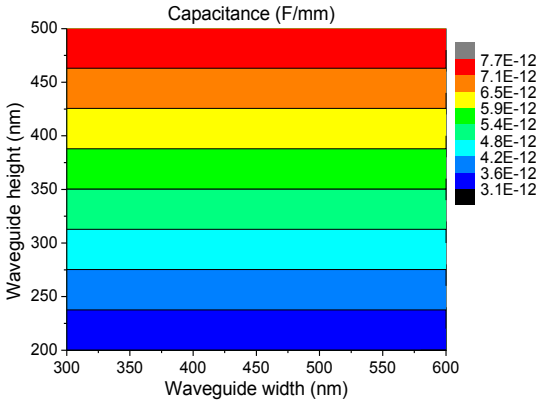

Fig. 10: Device capacitance per mm length against different waveguide geometries.

In both traveling wave and lumped element devices the power consumption has a second order dependence on the drive voltage but a linear dependence on the capacitance. The modulation efficiency is therefore the dominant factor in achieving low power consumption and therefore our results

suggest that the best results occur for thicker silicon device layers as shown in Fig. 9.

B. Optical loss

The optical loss of the device due to the doped regions of the waveguide has been calculated by running optical simulations on the structure at 0V (with depletion width of approximately 70nm). The results of this analysis in dB/mm can be seen in Fig. 11 for both TE and TM polarizations. In both cases the optical loss tends to increase with increasing waveguide width. For TM polarized light there is also large waveguide height dependence for values below 300nm.

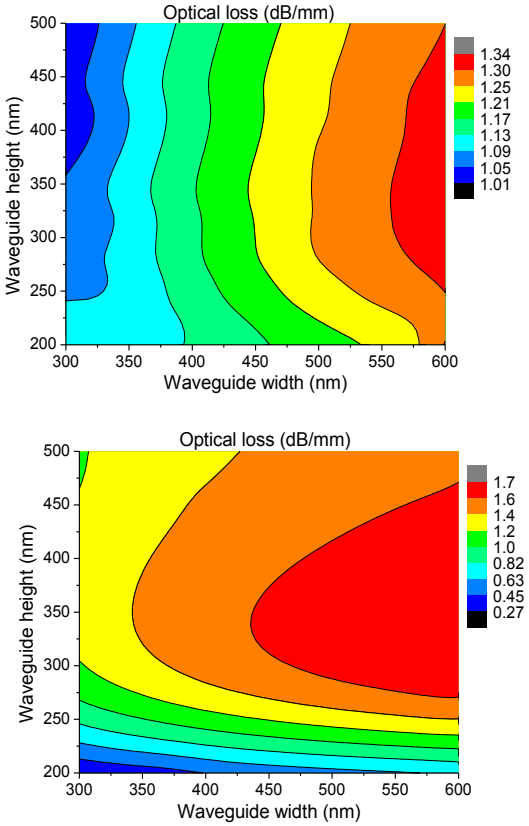

Fig. 11: Optical doping loss (dB/mm) against different waveguide dimensions for TE polarization (top) and TM polarization (bottom).

C. Device speed

The speed of the phase modulator element is usually dictated by its RC time constant. In devices driven in traveling wave configuration a large capacitance will also restrict the length over which high speed electrical signals can be propagated along the electrodes.

The resistance element comprises contact resistance between the highly doped regions and the electrodes, and resistance through the slab and rib regions which will be dependent on the respective thicknesses and the doping configurations. The highest resistance by about an order or magnitude is usually the resistance of the p and the n type slab regions since they are both thin, having high resistivity and a relatively long electrical length. With the slab height and doping densities fixed in this analysis the total access resistance will not vary significantly with waveguide geometry. The dependence of the device capacitance on the waveguide geometry, shown in Fig. 10, suggests that the fastest devices should be based on thinner SOI.

D. Overall Figure of Merit

If we consider an overall figure of merit (FOM) which takes into account the speed, optical loss and power consumption we can estimate the optimal waveguide dimensions on which a carrier depletion modulator should be based. Ideally, we want high speed, low optical loss and low power consumption for a modulator. As previously discussed the FOM should have a second order dependence on the modulation efficiency since the power consumption is proportional to the square of the voltage which itself is inversely proportional to the modulation efficiency. The FOM should then have a linear dependence on the optical loss and capacitance (speed). An overall figure of merit can therefore be calculated using the expression below.

$$FOM = \frac{(Fraction\ of\ modal\ overlap\ with\ depleted\ region)^2}{Capacitance \times Optical\ loss}$$

Figure 12 shows the figure of merit calculated for different dimensions for both TE and TM polarizations. For TE polarization the optical waveguide width and height are approximately 350nm and 360nm respectively. For TM polarization the optimal dimensions for low loss needs to be out of the range considered with a required width less than 300nm.

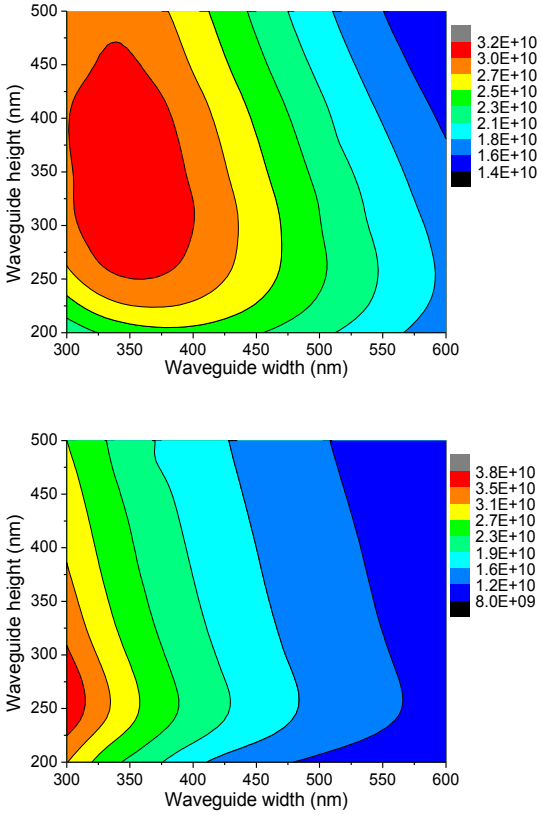

Fig. 12: Figure of merit against different waveguide dimensions for

TE polarization (top) and TM polarization (bottom).

E. Further considerations

1) Passive waveguide loss

As discussed in section IIIC the optical loss of the passive waveguides (in which the phase modulators are also fabricated) is dominated by scattering loss due to sidewall roughness. If the width of the waveguide is reduced to achieve increased modulation efficiency, the scattering loss will dramatically rise. This loss will place a minimum on the waveguide width which should be used for the modulator.

2) Polarization independence

An optical circuit that has a performance which is not sensitive to the input polarization is advantageous in terms of ease of packaging, ultimately meaning that the cost of assembly can be reduced. For the modulator, the modulation efficiency and the optical loss should ideally be the same for both polarizations. Figure 13 is a plot of the difference between the fraction of modal overlap and the difference in the loss for both polarizations. If a waveguide width of 350nm and height of 300nm are considered both the difference in optical loss and difference in the fraction of modal overlap are very low.

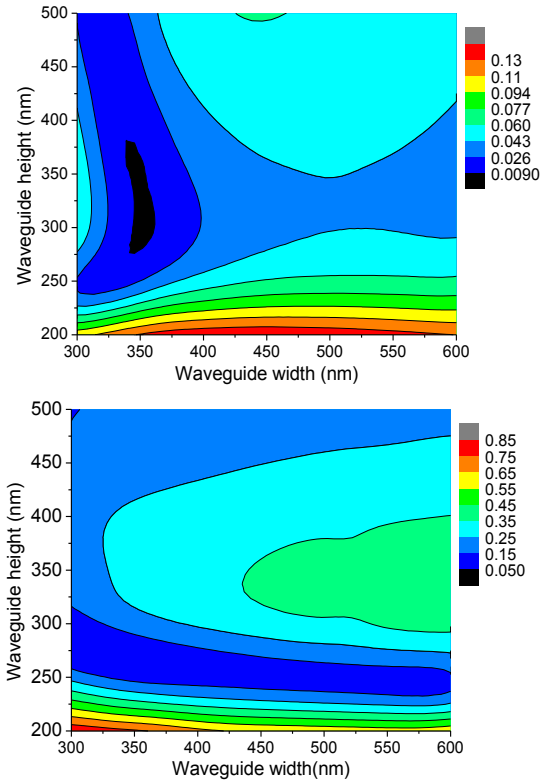

Fig. 13: Difference between the fraction of modal overlap with the varying depletion region for TE and TM polarizations (top) and difference in the optical loss in dB/mm for TE and TM polarizations (bottom).

V. WAFER SCALE INTEGRATION OF LASERS

Although direct monolithic growth on silicon of III-V direct bandgap semiconductors [93] or strained germanium [94] are currently heavily being investigated, these approaches are still in their infancy and considerable improvement is needed before efficient lasers can be demonstrated using these techniques. The most viable wafer scale type approach for realizing lasers on a silicon waveguide platform today is the hybrid integration platform whereby III-V epitaxial layers are integrated on silicon using wafer-to-wafer and die-to-wafer bonding techniques [12]. Following this bonding step the substrate of the III-V wafers is removed and the lasers or amplifiers are further processed using standard processing techniques, including mesa etching and metallization. Such hybrid III-V on silicon lasers have mostly been demonstrated starting from InP active layers and output powers above 20mW, threshold currents below 20mA, operation till 80°C and a wavelength tuning range of more than 45 nm were demonstrated [30, 95-97]. Recently also GaAs and GaSb-based devices were demonstrated [98, 99]. In some cases the mode in the active section is a true hybrid mode, spread out over both the III-V and the silicon layers [100]. In other cases, the mode in the active section is largely located in the III-V layers [96, 101]. In all cases the aim is to couple the mode fully to the silicon guide at the end of the active section, e.g. using adiabatic tapers [27, 101, 102], where they can be integrated with e.g. DBR-mirrors, ring resonators or arrayed waveguide grating routers [102-104] to create more complex laser structures. Also integration with active devices such as modulators has been demonstrated [97, 105].

In practice most of this work was carried out on thicker silicon waveguides (400 nm and above). The reason can be understood by having a look at Fig. 14. The horizontal lines in this figure depict the effective index of a slab layer of silicon with thicknesses of respectively 220 nm, 300 nm, 400 nm and 500 nm. In principle this is the highest index a waveguide fabricated in this layer can reach. The solid curves on the other hand give the effective index of 3 representative III-V epitaxial stacks, as a function of their width. We first focus on the blue line, which represents the effective index of a waveguide fabricated in a 2 μm thick epitaxial stack, containing a 300 nm thick active layer. Details of this layer structure can be found in [30]. All simulations were carried out for a wavelength of 1550 nm. It is immediately obvious that coupling from this layer to the 220 nm thick silicon layer will be very difficult: to allow for adiabatic coupling the index of both waveguides has to cross. For the 220 nm silicon layer and the thick III-V waveguide this only happens when we decrease the width of the latter below 0.3 μm, which is far from trivial in practice. Even if we decrease the thickness of the III-V layer stack to e.g. 500 nm (red in Fig. 14), as was used for realizing microdisk lasers (see [106] for details of this stack), the waveguide still has to be tapered down to below 0.5 μm. Only when using thin membranes (green in Fig. 14, 200 nm thick InP membrane), coupling to the 220 nm layer stack becomes trivial. If the thickness of the silicon layer is increased to 400 nm the width of the III-V waveguide can be increased to 1.0 μm to ensure mode crossing. Such a width seems rather straightforward to define, even using standard contact mask lithography. Figure 14 does not tell the full story however. Contrary to lateral adiabatic tapers, where the

distance between both guides can be gradually increased following the mode crossing point, in this vertical structure the distance between the center of both guides remains constant and relatively low. As a consequence, even when the mode has been pushed down to the silicon layer still a large fraction of the light remains in the III-V guide, which is problematic because it will result in losses and unwanted reflections at the end of the III-V guide. This is illustrated in Fig. 15, which shows the light confinement factor in the III-V layers as a function of the III-V taper width (assuming a 2 μm wide and 400 nm thick silicon waveguide, and the 2 μm thick III-V layer stack discussed above). For thin bonding layers the confinement factor changes very gradually as a function of the taper width and even for very narrow tapers, a considerable fraction of the light remains in the III-V layers (note that we assumed the 200 nm InP bottom cladding remained unetched). If the bonding layer increases however, the mode switches much more abruptly between each layers around the mode matching point, and the amount of light remaining in the III-V layer becomes negligible. Using thicker bonding layers however will require a longer taper to keep mode transformation losses low. Returning to Fig. 14, we see that the effective index of the 500 nm thick silicon layer is quasi similar to that of the wider III-V waveguides. In this case a truly hybrid mode can form.

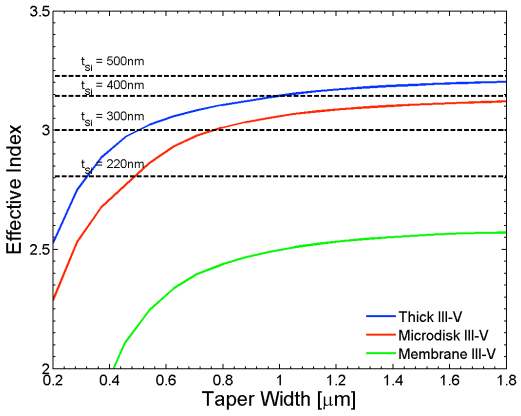

Fig. 14: Effective mode index of silicon slab waveguides with varying thickness (horizontal dashed black lines) and of three representative III-V waveguides, as a function of their width.

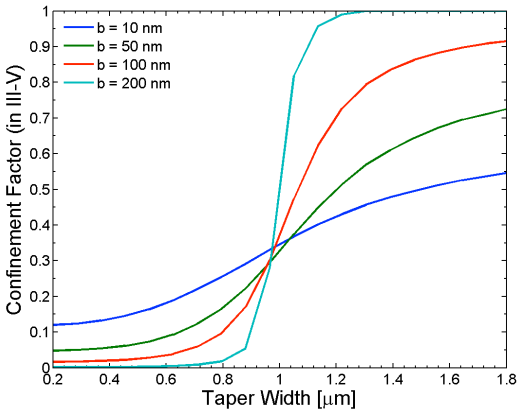

Fig. 15: Light confinement in the III-V layer as a function of the taper width for a III-V hybrid structure on top of a 2 μm wide and 400 nm thick silicon waveguide, for different bonding layer thicknesses *b*.

Another aspect which is worth considering is the influence of the silicon layer thickness on the strength of a grating defined in this silicon layer, below a III-V active layer, e.g. when realizing a distributed feedback laser (DFB). Figure 16 shows the coupling factor as a function of the etch depth for a hybrid III-V / silicon grating, using the thick III-V layer stack discussed above (2 μm), a 20nm bonding layer and for three different silicon layer thicknesses (*t*). It is obvious that for the 220nm silicon layer the coupling factor remains relatively low, while for the thicker layers the coupling factor can become relatively strong.

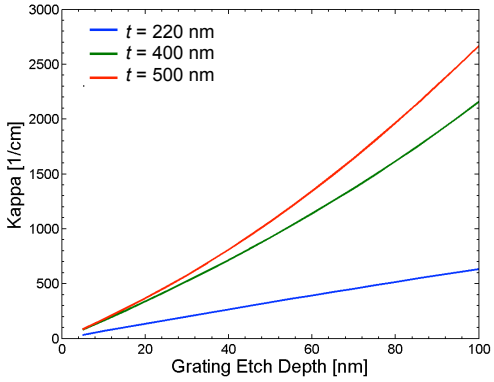

Fig. 16: Coupling factor for hybrid III-V silicon grating.

To overcome the challenges involved with coupling directly to standard 220 nm thick silicon waveguides using adiabatic tapers, several groups have investigated alternative schemes. In one approach a small fraction of the light is coupled out evanescently while the main part of the light remains in the cavity formed by the III-V structure. The best known example is the microdisk laser shown in Fig. 17(a) [107], whereby the III-V disk forms the laser cavity and a few percent of the total circulating power is coupled out every roundtrip to an evanescently coupled silicon waveguide below the cavity. This structure has the additional advantage that the total III-V layer structure thickness can be reduced: since the whispering gallery mode is situated at the edge of the device it will not feel the metal top contact as long as the latter has a diameter somewhat smaller than the III-V disk diameter. Recently also an inline laser exploiting intracavity evanescent outcoupling was demonstrated (Fig. 17(b)). In this case the cavity is formed by two III-V / silicon hybrid DBR mirrors and light is coupled out evanescently through a directional coupler located in the center of the cavity [108]. Of course one can also decrease the thickness of the III-V layer to such an extent that direct coupling to the silicon layer becomes trivial, as for example has been done to demonstrate optically pumped amplifiers [109] and switches [110] or photonic crystal based microlasers [111]. The main challenge then is to make this stack compatible with electrical injection without introducing excessive losses through the top metal contact. In [112] an approach involving microstructuring of the upper InP-cladding

was proposed to resolve this. However, this has yet to be demonstrated. An alternative approach to cope with the large mismatch between the III-V and silicon propagation constant is to include a grating in the design. In [113] contradirectional coupling through a corrugated silicon waveguide was used to couple light between these layer stacks (Fig. 17(c)). In [114], at each end side of the device light is coupled from the III-V stack to a cavity defined in the silicon layer stack (Fig. 17(d)). This approach has the advantage that the thickness of the layer stack can be increased compared to evanescently coupled devices.

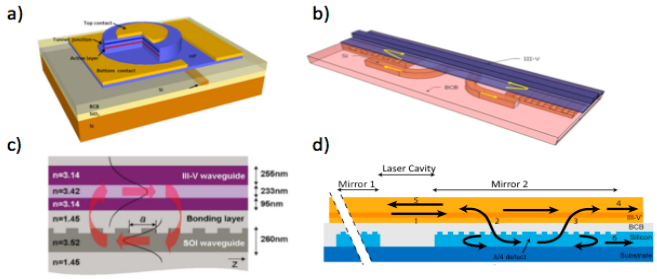

Fig. 17: (a) Evanescent coupling in microdisk laser (from [107]), (b) Evanescent intracavity coupling in DBR-laser (from [108] (c) Contradirectional coupling through grating in silicon layer (from [113]), (d) Mirror formed by coupling to resonant cavity (from [114]).

From the above discussion it is obvious that realizing hybrid III-V on silicon lasers is more straightforward when using thicker silicon waveguide layers (400 nm and above) than when coupling to 220 nm or even 300nm thick silicon. Unfortunately these thicker layer stacks are not available through the standard multi project wafer runs. Therefore it remains important to investigate novel approaches for realizing equally efficient lasers also on the standard silicon layer thicknesses.

VI. Conclusions

Silicon photonics has reached an important crossroads. As the first commercial products are being deployed and many more are in development, we observe two important trends that are pushing the field towards greater standardization. The first is the need for the integration of a greater number of individual optical components on a chip, which means that whilst historically many components have been designed and optimized in isolation, they now have to be made compatible with a common integration platform. The second important trend is the move to a fabless design company model making use of existing CMOS foundries for fabrication - driven more by economical rather than technical concerns. For silicon photonics to be competitive within this model requires the production of large volumes of devices with a high fabrication yield, requirements which also demand a high degree of standardization for the integration platform and the fabrication processes used. The most basic standardization parameters are the layer thicknesses of the substrate, in particular that of the active silicon device layer. For the leading foundries that offer multi-project wafers, a thickness of 220 nm has for now become the norm.

We have reviewed the silicon layer thickness considerations in the design of several individual components that are part of an integrated optical transceiver, namely passive components for waveguiding, wavelength selection, and light coupling as well as active components such as modulators and on-chip lasers produced by hybrid integration. A fairly complex picture arises from this review. For simple waveguides, standard 220 nm thick waveguides work well for TE but preclude the use of TM polarization, which is only well guided by waveguides with a thickness in excess of 250 nm when covered by a variety of cladding materials. This leads to sub-optimal performance of devices in particular with respect to propagation loss and back reflection. We have also discussed the implications for fabrication tolerances in wavelength selective devices and directional couplers which tend to be better for devices operating in TM polarization, considering in particular the improvements in silicon thickness uniformity achieved in 300 mm SOI wafers. Directionality of grating couplers is found to be optimized in silicon waveguides of approximately 350 nm thickness. For 220 nm silicon substrates, this problem is sometimes circumvented by the use of polycrystalline silicon overlayers in the grating region. For optical modulators we have defined a figure of merit for the design optimization. The results indicate an optimal silicon thickness of 360 nm and approximately 250 nm for TE and TM polarizations, respectively. Finally, we discussed the considerations for the hybrid integration of laser sources. Here we found that the strong coupling of laser and SOI waveguides necessary for good power transfer is achieved in a straightforward way only for thicker silicon waveguides of 400 nm and above, although more complex solutions for 220 nm thick waveguides are under investigation.

The review of the components then appears to indicate that a choice of 220 nm silicon is not ideal for any of the components we have discussed for the integration strategy of using monolithic silicon carrier-depletion modulators and hybrid lasers operating in the 1550 nm wavelength range. This conclusion may of course be expected for an integration platform that needs to make trade-offs for various components. More important to consider is the fact that in all cases we found that better performance or more robust fabrication could be achieved by using a thicker silicon waveguide layer, indicating that the sweet spot for integration may in fact be found for thicknesses greater than the now standard 220 nm. Other more exploratory integration strategies, such as the use of graphene-based modulators overgrown on silicon, are beginning to be investigated. These strategies will certainly lead to different conclusions of the optimum silicon thickness. We believe that further research into the optimized silicon integration platform considering different options for the substrates will be of great importance in ultimately answering the question we have asked in the title and hope that this discussion paper has made a constructive contribution to this process.

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