A High-Efficiency, Low-Cost IBC Cell Using Doped Laser Cut Back-Side Contacts.

W.J. Mughal[1*], H.A. Mughal[2], A.G. Laffoley[2], D.M. Bagnall[3], N.E.B. Cowern[4], S. Simdyankin[4] and S.A. Boden[1]

[1] Nano Group, Electronics and Computer Science, University of Southampton, SO17 1BJ

[2] Silicon CPV plc, Akhter House, Perry Road, Harlow, Essex, CM18 7PN

[3] School of Photovoltaic and Renewable Energy Engineering, The University of New South Wales, Sydney, NSW 2052, Australia

[4] School of Electrical Engineering and Electronics, Newcastle University, NE1 7RU

[*] Corresponding Author: wjm1c12@soton.ac.uk

Abstract

We present a new cell geometry for IBC solar cells. The cells have a shorter current path between the carrier generation and collection regions allowing materials with shorter diffusion lengths to be used. Modelling of this geometry shows that efficiencies of 19.8% are possible.

Introduction

Since the introduction of the concept in 1970s by Schwartz and Lammert [1], work into the interdigitated back contact (IBC) cell has shown that the geometry can produce amongst the highest efficiency silicon solar cells (e.g. Sun Power's Maxeon Gen 3 cell giving performances of up to 24% [2]). However these current designs have proven to have relatively high costs for two main reasons. Firstly, wafers with high recombination lengths have to be used because the traditional IBC geometry with contacts at the rear leads to longer current paths. Secondly, the processing costs to create these designs are more costly than more conventional silicon cells. The consequence of this is that current IBC designs, despite their high efficiency, are still inhibited by the cost per watt when competing with traditional architectures.

We are developing an IBC cell with laser cut doped rear contacts and a geometry that reduces the length of the current path. This allows the use of conventional solar grade silicon wafers. The objective of this approach is to significantly reduce the cost of fabrication whilst also increasing performance, ultimately leading to a competitive final cost per watt price when compared with traditional solar cells. In this paper, the development of laser grooving process and its incorporation into a full cell fabrication process is presented. Several areas for improvements are then discussed including the antireflection coating, front side emitter and ohmic contacts to the p-type grooves. A process for fabrication of an enhanced cell, incorporating these improvements, is then presented.

Cell Geometry

With IBC cells, the carriers are generated at the front surface and collected at the rear. To overcome the problem of efficiently collecting the carriers at the rear, conventionally either super thin wafers or high life time silicon substrates are used, both of which are costly.

In this work, the cell is to be fabricated on solar grade silicon using a p-type wafer. To overcome the problem of generating carriers at the front surface and collecting them at the back, grooves are cut into the rear surface using a laser so as to bring the point of collection closer to the point of generation. The top surface is textured with random micron-sized pyramids to provide antireflection and to aid light trapping. An oxide/nitride stack provides additional antireflection and surface passivation. In order to prove that the proposed geometry can produce working devices, a simplified cell design, shown in Figure 1, was fabricated.

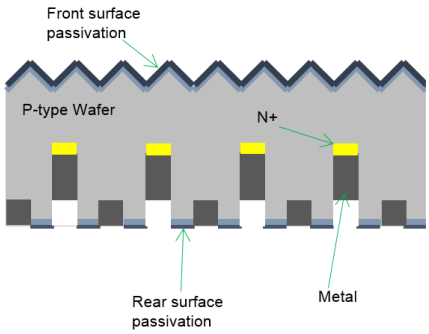

Figure 1. Illustrated cross section of simplified cell design.

Cell Fabrication

The chosen substrates are *p*-type <100> 5" wafers with a resistivity of 10-30 Ω-cm.

Following a degrease and clean, the wafers undergo a saw damage removal step and are then textured with pyramids using a 2% KOH, 2% IPA solution for 20 mins to enhance light trapping. Figure 2 shows the textured surface. The front and rear surfaces are then passivated with thermally grown wet oxide. Initially, 100 nm of SiO_2 is grown at 900°C for 25 mins to reduce surface recombination. Then 100 nm of LPCVD silicon nitride is deposited, at 770°C for 25 mins, on both front and rear surfaces for masking purposes and as an antireflective coating. Using a 1064 nm wavelength YAG laser, the deep *n*-type contact fingers and busbar are cut to a depth of 80 µm into the rear surface, with a spacing of 0.6 mm between the fingers.

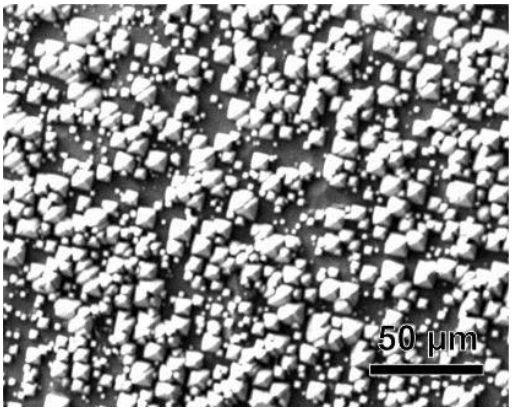

Figure 2. SEM micrograph of textured surface.

These grooves are shown in the optical micrograph in figure 3. The groove damage caused by the laser along with debris left in the groove are then removed using a sodium hydroxide solution.

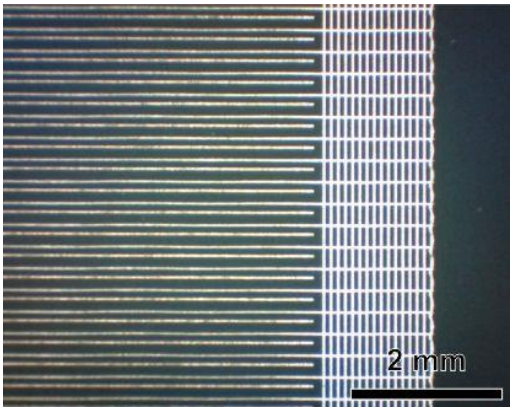

Figure 3. Optical micrograph of metallized rear contact fingers and busbars.

The grooves are cut through the rear surface oxide nitride stack allowing them to be doped to a sheet resistivity of 10 Ω/square by $POCl_3$ diffusion at 880°C for 15 mins with a 10 min drive in. The phosphorus glass is then etched from the grooves using hydrofluoric acid. This leaves areas of the wafer now doped *n*-type whilst the bulk substrate remains *p*-type giving a *pn* junction. The shallow *p*-type collector fingers and busbar are then cut into the rear surface using the same laser, with the spacing between the *p*-type fingers being 0.6 mm, therefore interdigitating the *n*-type fingers with a spacing of 0.3 mm. The busbar is cut on the opposite side of the device to the *n*-type busbar. The grooves are then cleaned and cleared of debris from the laser cutting process using a sodium hydroxide solution. To enable current collection from the device, the grooves are then metallised using electroless plating. With the LPCVD nitride on the rear surface acting as a mask, only the silicon substrate at the base of the grooves is exposed for plating. Nickel is deposited initially to act as a diffusion barrier prior to copper being deposited in the grooves on top of the nickel. Finally, to allow for better contact to be made to the busbars, they are then plated electrolessly with silver.

Solar Cell Results

The IV curve from one of the successfully fabricated devices is presented in Figure 4. With only the laser grooving optimized at this point, devices were produced with efficiencies ranging from 4-8%, with a fill factor of 83.4%, a V_{oc} of 0.5V and an I_{sc} 27 mA, for a device of 50 mm × 45 mm.

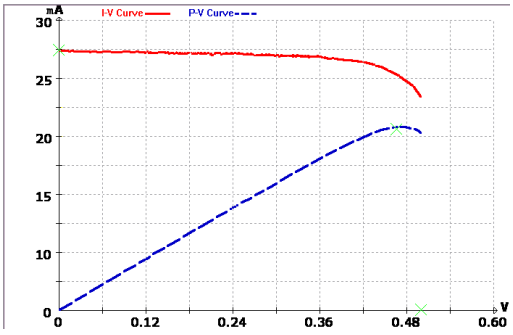

Figure 4. IV curve obtained with simplified cell geometry.

Antireflection Coating Optimization

Using a transfer matrix approach [3], the transmittance of light through the oxide/nitride stack on a flat silicon substrate was calculated for thicknesses of SiO_2 and Si_3N_4 from 0-350 nm (Figure 5). The refractive index data for SiO_2 and LPCVD Si_3N_4 were obtained from [3] and

[4], respectively. The transmittance can be weighted to the spectral irradiance ($I(\lambda)$) of the AM1.5 solar spectrum (ASTM173G, global tilt) and then the average weighted transmittance (T_w) can be calculated using equation 1.

$$T_w = \frac{\int_{\lambda\,\max}^{\lambda_{\min}} T(\lambda)\, I(\lambda)\, d\lambda}{\int_{\lambda\,\max}^{\lambda_{\min}} I(\lambda)\, d\lambda} \qquad (1)$$

T_w can then be used as a figure of merit in an optimization of the thicknesses of the two layers in the stack. This was implemented in Matlab using a simplex-based search method.

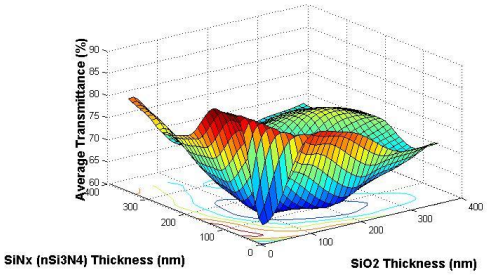

Figure 5. Surface plot of SiO_2 and Si_3N_4 thicknesses vs. average transmittance.

A contour map of the thicknesses of oxide and nitride vs. T_w is shown in Figure 6. The optimum values are presented in Table 1.

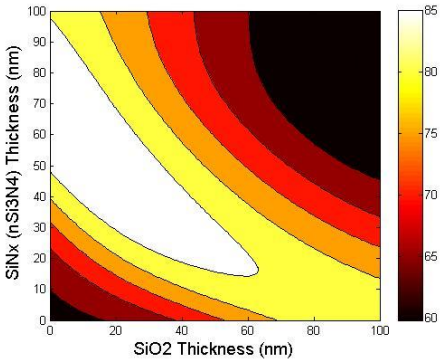

Figure 6. Contour map of SiO_2 and Si_3N_4 thicknesses vs. T_w.

Oxide thickness (nm)	2.3
Nitride thickness (nm)	65.5
T_w (%)	89.6

Table 1. Optimized values of oxide and nitride thickness for antireflective coating.

This optimization does not consider passivation requirements which would have to be included before these thicknesses can be implemented in the next batch of solar cells to further reduce the front surface reflectance. Further improvements are possible by using experimental refractive index data from the cell fabrication process in the optimization calculations. Also, the current optimization only considers a planar surface and so could be advanced by accounting for the pyramidal texturing.

Further Improvements

A 2D TCAD package (Sentaurus TCAD software from Synopsys) was employed to simulate the cell and investigate potential efficiency improvements as a result of adding a front side emitter and improving the ohmic contact on the *p*-type contact fingers. Plots of simulated cell efficiency against doping concentration of front side emitter and rear side collector are shown in figures 7 and 8. The predicted incremental improvements in efficiency over the simple device are presented in Table 2. These results show that the performance of early working devices is close to what is predicted by the TCAD model. This indicates that with the addition of a few extra steps the efficiency can be greatly improved, to approximately 20%.

	Modelled Efficiency	**Measured Efficiency**
Simple Device	*8.3%*	*4-8%*
+Front side emitter	*+7% (15.3%)*	-
+Improved back contact for *p*-type grooves	*+4.5% (19.8%)*	-

Table 2. Device steps with modelled and measured efficiency.

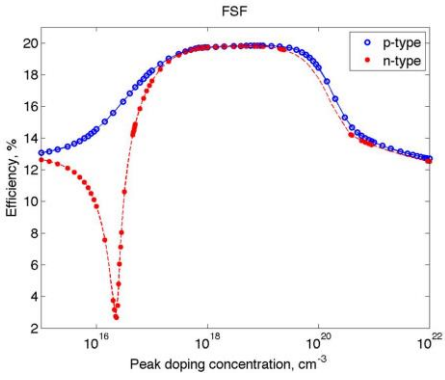

Figure 7. Cell efficiency vs. doping concentration of front side emitter.

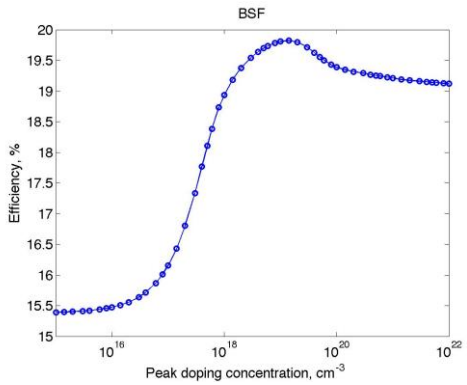

Figure 8. Cell efficiency vs. doping concentration of rear side collector.

Enhanced Cell Design

According to the modelling, the addition of a front side emitter can greatly increase the cell efficiency. This simple step can be achieved by lightly diffusing phosphorous into the front surface of the wafer prior to the front surface passivation steps. To improve the ohmic contact within the *p*-type grooves, a *p*+ doping step can be incorporated into the fabrication process. In order to avoid extra thermal processing, a layer of epitaxial silicon will be grown using hot wire chemical vapour deposition (HWCVD). Figure 9 shows the cross section of the full cell design. The HWCVD step will provide a blanket coverage of epitaxial growth, which will cause problems during the metallisation process. To overcome this, a layer of PECVD oxide will be deposited before cutting the *p*-type grid which will allow lift off of any excess epitaxial growth. A summary of the process steps for the enhanced cell design is presented in Figure 10.

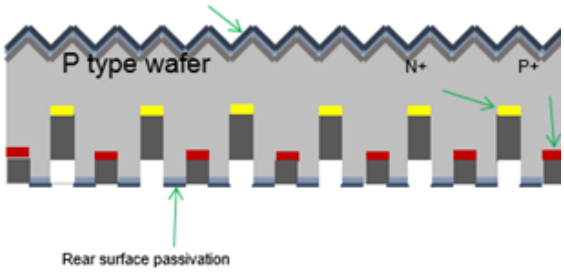

Figure 9. Cross sectional view of enhanced cell design.

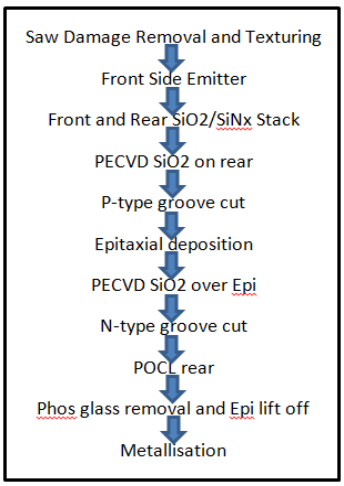

Figure 10. Process steps for enhanced cell design.

Conclusions

This report presents a new approach to IBC solar cell design and fabrication which uses low cost manufacturing techniques and enables silicon with relatively short diffusion lengths to be used. Working devices have been demonstrated with performances in line with predictions from simulations. Modelling suggests that by implementing several relatively simple improvements to the design, this cell geometry is capable of achieving efficiencies of 19.8%.

Acknowledgements

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