High Performance Hetero-Junction Solar Cells with Plasmonic Light Trapping.

L. J. Crudgington*, M.A. Rind, S. A. Boden and Prof. D. M. Bagnall.
• University of Southampton, University Road, Southampton, SO17 1BJ
* Corresponding Author ljc1g09@ecs.soton.ac.uk

This paper attempts to describe the process flows and the optimum deposition parameters for high-performance heterojunction solar cells, and the proposed introduction of plasmonic nanoparticles. In the investigation, the optimum deposition conditions for the crystalline / amorphous heterojunction will be experimentally determined, and charge-carrier lifetime measurements will be presented. Investigations will then be performed on self-aligned Ag nanoparticles deposited on amorphous silicon, and the optimal particle configuration based on annealing temperature and duration will be identified.

Introduction

Hetero-junction solar cells are currently one of the best performance designs for achieving high energy conversion efficiency in solar cells. This is due to their innovative use of a single-crystal silicon as a light absorption layer, and amorphous silicon intrinsic and doped regions which provide the charge carrier separation and passivation of the silicon material. [1,2] This design prevents much of the charge carrier recombination at the device surfaces and therefore demonstrates energy conversion efficiencies of up to 25%. The purpose of this work is to investigate further enhancement of the performance of the devices achieved by applying plasmonic light-trapping treatments, which enhance the optical path length of the incoming light photons and ensure optimum light absorption. [3] This additionally allows for devices which use less silicon material as thinner absorption layers are necessary to absorb incoming photons, leading to a reduction in device cost.

Device Architecture

The combined use of doped and intrinsic amorphous silicon layers deposited at a low temperature on crystalline absorber layers provides significantly superior surface passivation compared to conventional devices. This design eliminates the high-temperature dopant diffusion and oxide passivation steps of conventional solar cells. Because the amorphous layers are not used for absorption and carrier generation, the device does not suffer from light-induced degradation as purely amorphous devices do, while the use of n-type crystalline wafers ensures that no boron-oxygen reactions occur and create recombination centres in this region after exposure. Additionally, the improved surface passivation reduces the temperature dependence of the device and ensures the maximum possible charge carrier lifetimes. [4-5]

Due to the significant performance losses which can result from reflection from the top surface, detailed attention must be paid to the optical topology. The use of anti-refection coatings, light-trapping and path-length enhancement technologies can significantly improve the performance of a device, while the use of these technologies can also reduce the required device thickness by several times. [6-7] Light-scattering concepts in particular are very important in achieving high-efficiency photovoltaic device designs, which cause optical path-length enhancement by preferential scattering of the incident light into the semiconductor absorber layer material. This scattering can be achieved via the method of localised surface plasmons by the positioning of sub-wavelength plasmonic metal nanoparticles within the photovoltaic device. [8].

Experimental Detail

The modern device topology is based upon a low-doped crystalline silicon n-type wafer. The amorphous silicon layers are then deposited on either side, which initially consist of a very thin layer of intrinsic material, followed by the doped emitter and back-surface field regions. The deposition of the intrinsic layers in this investigation is performed using an Oxford Instruments PlasmaLab System 100. The excitation frequency of this system is 13.56MHz, which supplies ample

excitation energy at low power whilst minimising ion bombardment damage to the growing films. The deposition chamber is supplied with source gases via a series of programmable mass-flow controllers (MFCs) which combine and provide the atomic species for CVD via a uniform shower-head arrangement.

Deposited layers are then coated with a thin TCO layer, which is necessary due to the low charge carrier mobility of the doped layers, and then finally the metallisation grid is deposited. Texturing of the wafer to improve light absorption and enhances internal reflection and light trapping, the inclusion of the back-surface field and rear passivation layers have been included in recent devices to maximise performance, and the current state-of-the-art devices approach efficiencies of 25%.

The highest quality of amorphous silicon material is that which has a low density of stressed Si bonds, fewer defects, a smaller quantity of micro-void regions and a slightly decreased band-gap. This material has a lower density of bonded hydrogen within the matrix and is therefore said to be less susceptible to light-induced degradation. [9-10]

The first step of the fabrication process is to determine the optimum deposition conditions for the amorphous silicon. The quality of the amorphous silicon thin films are variable depending on the deposition conditions, so these purposes it is essential to fabricate individual thin film single layers using varying deposition conditions and thoroughly examine their optical and electrical performance before committing these conditions to a complete heterojunction device. The first step is to examine the dark and photo conductivities (σ), optical band gap (E_g), optical absorption and reflectivity at various wavelengths and thin film thickness. From these experiments it is possible to determine specific deposition problems such as inefficient doping of layers or contamination of intrinsic material.

Once optimum layer quality has been obtained, deposition of heterojunction structures using the optimised single-layer conditions is performed, and the device can be examined by means of charge carrier lifetime measurements, which are fundamental in determining the energy conversion efficiency (η), fill factor, V_{OC}, I_{SC}, and maximum power output of the final device.

Fabrication

A. Intrinsic Layers

The intrinsic region of the heterojunction structure is fundamental in defining the performance of the solar device. The intrinsic region performs surface passivation of the crystalline substrate absorber layer, and therefore must be free from all contamination which could provide Shockley-Reid-Hall recombination centres.

It is vitally important that the temperature is maintained below 180°C to prevent the amorphous material crystallising on contact with the substrate material. The hydrogen passivation mechanism is additionally very important in this region, so while the atomic hydrogen species in the SiH_4 source gas is often sufficient in PECVD, dilution in additional hydrogen (H_2) has been investigated. Care must be taken with this dilution ratio, as the restructuring effect of hydrogen can result in microcrystalline films being formed at sufficient dilutions.

The complete set of experimental results are published elsewhere, [11] while the results of this investigation are presented in table 1. The resultant silicon thin films are investigated electronically via their photo- and dark-conductivity measurements and the optimum layer conditions are identified.

Table 1 - Intrinsic Layer Deposition Parameters

Variable	Unit	Value
RF Power	*(W)*	10
Temp	*(°C)*	180
Chamber Pressure	*(mTorr)*	350
SiH_4 Flow Rate	*(sccm)*	50
H_2 Flow Rate	*(sccm)*	50
Thickness	*I (nm)*	375
Deposition Rate (p-type)	(nm/sec)	0.60
Deposition Rate (n and i-type)	(nm/sec)	0.26

B. Heterojunction Devices

Based on the optimum results from the single layer investigations in section A, the deposition of the silicon heterojunction structures have been fabricated. The substrate material is a 625µm double-side polished n-type crystalline <100> silicon wafer, with resistivity between 1-30 Ω-sq. In order to prepare both sides of the device, an oxide cap is required to protect one side of the silicon surface. This is deposited using PECVD to a thickness

depth of 300nm, after thorough RCA cleaning using the sequence. After these steps, it is necessary to perform a further cleaning step immediately before deposition of the first amorphous silicon layers.

The first side of the device to be fabricated is the intrinsic and n-type regions, which are performed in sequence using PECVD based on the optimum conditions determined in section A. 15nm of intrinsic material is first deposited followed by 15nm of n-type doped material. This is then immediately transferred to a Leybold Optics LAB700 e-beam assisted evaporation system for the deposition of 200nm of indium-doped tin oxide to enhance the charge carrier collection from the silicon surface. The ITO layers are deposited to a resistivity of 20 Ω-sq using a rate of 2.5Å/s. After this step it is advisable to perform a chamber 'recondition' on the plasma deposition tool, in order to mask any dopants which may be on the chamber surfaces and affect subsequent films.

The next stage in the deposition is to protect the silicon and ITO layers whilst the sample is once again cleaned and the other side is deposited. This is achieved by the spinning of 6µm AZ9260 photo-resist, chosen for its resistance to high temperatures and cleaning solution, followed by a subsequent hard-bake. After this step it is necessary to perform the cleaning routine once more and additionally perform an extended oxide etch for around 60 seconds in hydrofluoric acid (HF) to remove the protective oxide on the second side deposited in the first step. This step can be continued until the surface becomes hydrophobic and the pure silicon surface is exposed.

The second side of the device can now be fabricated, which is performed under the same conditions as the first apart from the doped layer, which is p-type in this instance. Once again the newly deposited silicon material is transferred to the e-beam evaporator which deposits a further 200nm to the p-type side. This side is now able to be metallised with the aluminium contact grid. Once the p-type side is completed, the photoresist layer must be removed using a plasma ashing step, at 800W 2.45GHz RF in an environment of oxygen / nitrogen. Following this, the aluminium metallisation grid can be deposited on the n-type side using e-beam evaporation finalising the completed cell.

Results

The performance of the heterojunction is in part proportional to the minority charge carrier lifetime. A high charge carrier lifetime increases the likelihood that collection of a charged particle will occur and will and is therefore proportional to the efficiency of the solar cell.

Initial results are concerned with devices which have a silicon nitride cap as opposed to the indium-doped tin oxide layer. Figure 1 depicts the charge carrier lifetime measurements, performed using a calibrated Sinton WCT-120 Photo-conductance Lifetime Tester.

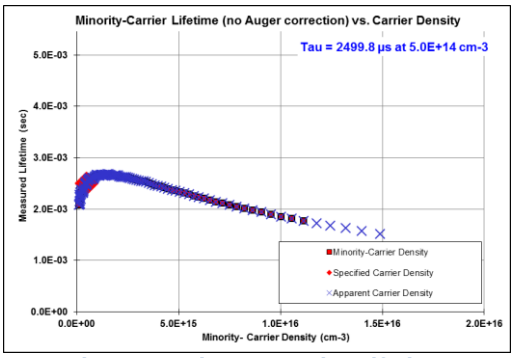

Figure 1 - Charge Carrier Lifetime

C. Self-Aligned Nano-particles

In order to enhance the optical absorption within the heterojunction device, a series of self-aligned silver nanoparticles will be deposited within the surface transparent-conductive oxide layer. Particle arrays are fabricated by the e-beam assisted evaporation of silver granules on to the substrate material, which are subsequently annealed for a specific time period and temperature. The shape, dimensions and periodicity of such particles is dependent on these conditions of fabrication, such as the material, layer thickness, and anneal time and duration. These attributes define the extent to which light is scattered within the absorber layer, and at which wavelengths. It is therefore essential to accurately tailor the response of the particle array to a particular type of photovoltaic device, to ensure that the optimum performance enhancement is achieved.

Fabrication

The deposition of the particle arrays is performed on 375nm of intrinsic amorphous silicon, deposited on a plain glass substrate using PECVD with the

optimum electrical and optical quality for photon absorption as described in section A. A layer of silver is subsequently deposited directly on to the silicon using a Leybold Optics BAK600 e-beam assisted evaporation system. The depth of these layers is varied between 5, 10 and 15nm thicknesses although 15nm only is presented here. The layers are subsequently transferred to a Jipelec JetFirst 200C rapid thermal annealer and optically heated to temperatures ranging from 225°C to 300°C for between 30 and 90 minutes.

Measurement is performed using a Bentham PVE300 quantum efficiency and integrating sphere system, first by measuring the optical transmission over the wavelength range 400 – 1100nm followed by the optical reflection over the same range. The optical absorption of the device can therefore be calculated which will illustrate the performance of the device.

Results

The data presented in figure 2 shows the optimum light absorption values for the best performing durations for annealing at temperatures ranging from 225°C – 300°C.

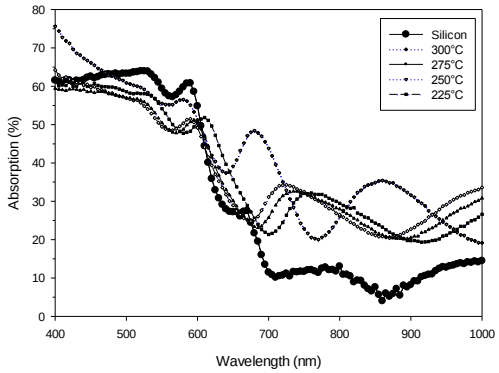

Figure 2 - Optical Absorption of Silver Arrays

The results from the investigation illustrate the extent to which the self-aligned nanoparticle arrays can affect the absorption of light within a silicon thin film. For this data set of 15nm films, it can be determined that an annealing step at a temperature of 300°C for a total duration of 70 minutes provides the optimum absorption of photons. Figure 3 below illustrates an SEM image of the nanoparticles, which confirms their size, shape and diameter.

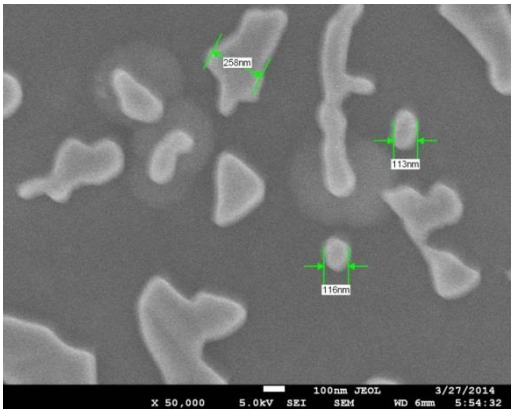

Figure 3 - SEM Image of Silver Nano-Particles

Summary

It was experimentally determined that excellent silicon wafer passivation can be achieved using amorphous silicon within a hetero-junction structure, based on charge carrier lifetime measurements. Subsequently, the optimum light absorption conditions were found by the use of self-aligned silver nanoparticle arrays on amorphous silicon. The continuation of this work is the fabrication of a functional heterojunction solar cell as per the process flow defined in this paper, and to deposit the silver arrays on to the device while observing the optical and electrical performance compared to a cell with no such nanoparticle coating and / or conventional silicon wafer texturing steps.

References

[1] Mishima, Takahiro, *et al*. Solar Energy Materials and Solar Cells 95.1 (2011): 18-21

[2] Tanaka, Makoto, *et al.* Photovoltaic Energy Conversion, 2003. Proceedings of 3rd World Conference on. Vol. 1. IEEE, (2003).

[3] Tristan L. Temple and Darren M. Bagnall Progress in Photovoltaics: Research and Applications (2012).

[4] Sark, Wilfried G. J. H. M.; Korte, Lars; Roca, Francesco, Springer, (2011).

[5] Mishima, T., Taguchi, M., Sakata, H., Maruyama, E.: Sol. Energ. Mat. Sol. 95, 18 (2010).

[6] R.S.A. Sesuraj, T.L. Temple, D.M. Bagnall, Solar Energy Materials and Solar Cells, Volume 111, (2013), Pages 23-30,

[7] Catchpole, K. R., and Albert Polman, Optics express 16.26 (2008): 21793-21800.

[8] Hairen Tan, Rudi Santbergen, Arno H. M. Smets, and Miro Zeman, Nano Letters (2012) 12 (8), 4070-4076

[9] Fehr, M., Schnegg, A., Rech, B., Astakhov, O., Finger, F., Bittl, R., Teutloff, C., Lips, K.. Rev. Lett., (2014)

[10] A. H. Mahan, J. Carapella, B. P. Nelson, R. S. Crandall, and I. Balberg, J. Appl. Phys. 69, 6728 (1991).

[11] L. J. Crudgington *et al*. Molecular Crystals and Liquid Crystals, 589 (2014)