HELICS Cell: Laser-cut Grooves to Create a High-efficiency, Low-cost IBC Solar Cell.

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***Abstract* — A novel approach to the production of interdigitated back contact (IBC) solar cells is presented. IBC cells have all the contacts on the rear of the cell, thus preventing the 'dead areas' that appear on conventional solar cells with front-side contacts. Current IBC cell designs are relatively expensive, but by using laser grooved contacts it is possible to create cheaper IBC solar cells using solar grade silicon wafers. The concept is verified by experiments and detailed TCAD simulations.**

***Index Terms* — IBC, lasers, photovoltaic cells, silicon.**

I. Introduction

Interdigitated back contact (IBC) solar cells were first developed in the 1970's by Schwartz and Lammert [1] and the concept has since been shown to be capable of producing cells with power conversion efficiencies over 23% (e.g. Sun Power's Maxeon 3 [2]). Indeed, Panasonic have recently announced a new world record efficiency for c-Si based solar cells of 25.6% with a design that incorporates the IBC concept into their HIT (Heterojunction with Intrinsic Thin-layer) technology [3]. However these current designs have proven to have relatively high costs for two main reasons. Firstly, wafers with high recombination lengths have to be used because the traditional IBC geometry with contacts at the rear leads to longer current paths. Secondly the processing costs to realize these designs are higher than those for current conventional silicon cells. The consequence of this is that current IBC designs, despite their high efficiencies, are still inhibited by the cost per watt when competing with traditional architectures.

We are developing the HELICS cell (High Efficiency Laser Interdigitated Contact), a novel interdigitated back contact cell design, using laser-cut, doped rear contacts to provide a cell geometry that reduces the length of the current path, thereby allowing the use of conventional solar grade silicon wafers. The objective of this approach is to significantly reduce the cost of fabrication whilst also increasing the performance relative to traditional front contact solar cell architectures, ultimately leading to a high performance device with a competitive final cost per watt.

II. Cell Design

The cell is designed to be fabricated on solar grade silicon using a p-type doped wafer. After cleaning and saw damage removal the wafer is textured with pyramids for light trapping. This is done in a 2% KOH, 2% IPA solution for 20 minutes at 70˚C. Fig. 1 is an SEM micrograph showing the textured surface.

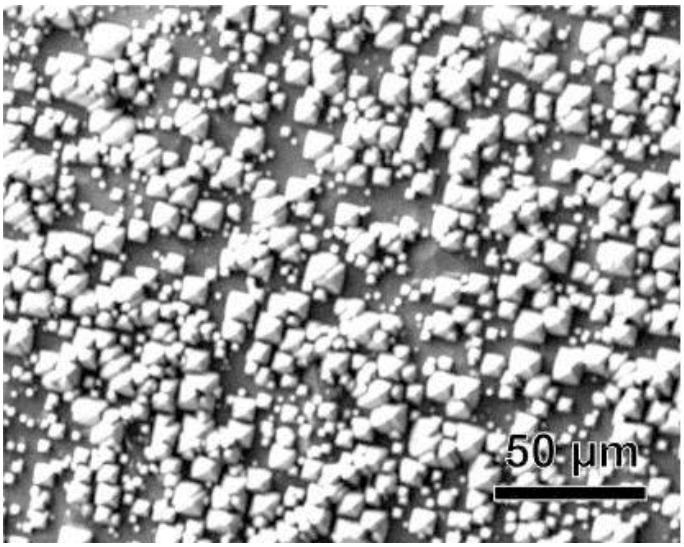

Fig. 1. SEM micrograph of textured surface.

The front surface of the wafer is then lightly doped with phosphorous to give a front side floating emitter. Both the front and rear surfaces are then passivated through deposition

of a silicon nitride/silicon oxide stack. Shallow grooves are then cut into the rear side of the wafer with a 1064 nm YAG laser to produce the p-type rear side contacts. The grooving pattern consists of horizontal fingers connected to a vertical busbar at the edge as shown in Fig. 2.

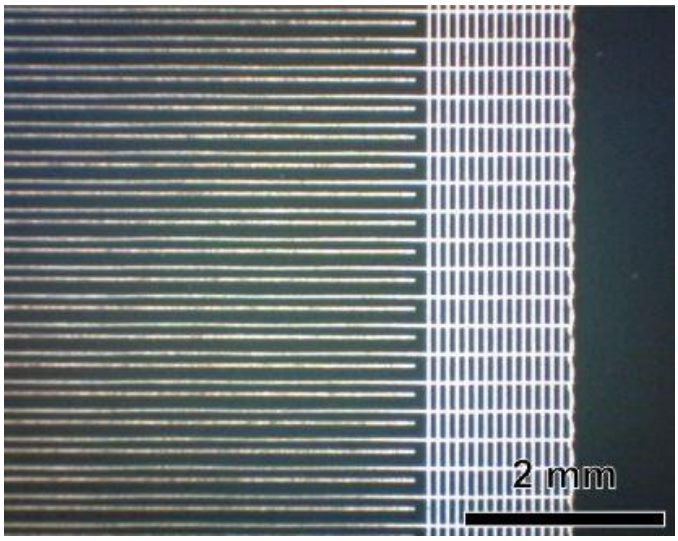

Fig. 2. Optical micrograph showing metalized p-type grooves attached to a busbar and n-type grooves.

An epitaxial deposition is then performed to dope these grooves p+ using hot wire chemical vapor deposition (HWCVD). This is then masked off with oxide before the n-type grooves and busbar are laser cut into the back of the wafer. The fingers of the p-type grooves and n-type grooves interdigitate as shown in Fig. 2. Phosphorus is then diffused into the n-type grooves to give an n+ region, then the grooves are contacted by electroless plating. The cross sectional view of the completed device is illustrated in fig.3.

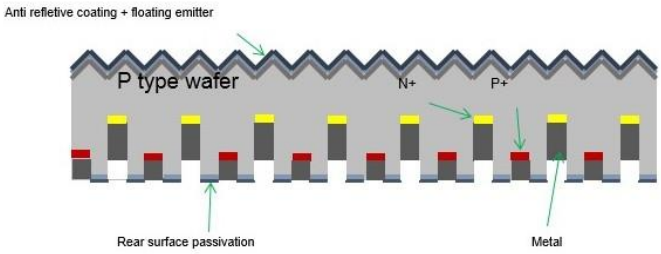

Fig. 3. Illustrated cross section of full cell design.

III. Experimental Proof Of Concept

In order to demonstrate fabrication of a working solar device using the proposed geometry, a simplified version of our architecture was devised. Whilst maintaining the geometry, the process was modified by omitting the epitaxial p-type deposition and floating emitter. As the wafer is already p-type doped, a PN junction could be created without the epitaxial p-type deposition. The resultant device would demonstrate fabrication of the laser cut groove geometry, however the efficiency would be low due to the absence of epitaxial deposition and a floating emitter. This is shown in fig. 4.

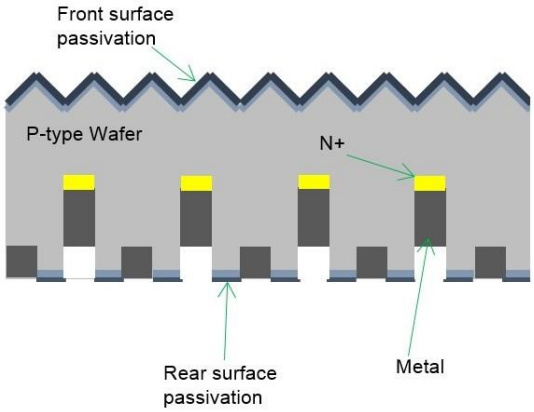

Fig. 4. Illustrated cross section of simplified cell design.

The simplified cell design was successfully fabricated as described. Fig. 5 shows the IV characteristics of this initial device. Even with no optimization of steps, no front side floating emitter or epitaxial p-type deposition, the fabricated device exhibited an efficiency of approximately 8%, with a fill factor of 83.4%, a V_{OC} of 0.5 V and an I_{SC} of 27 mA, for a device of 50 mm × 45 mm. In the following section a modelling assessment of the potential of the HELICS architecture, once the full process is put in place, is reported showing that it has the potential to approach efficiencies in the range of 22-24%.

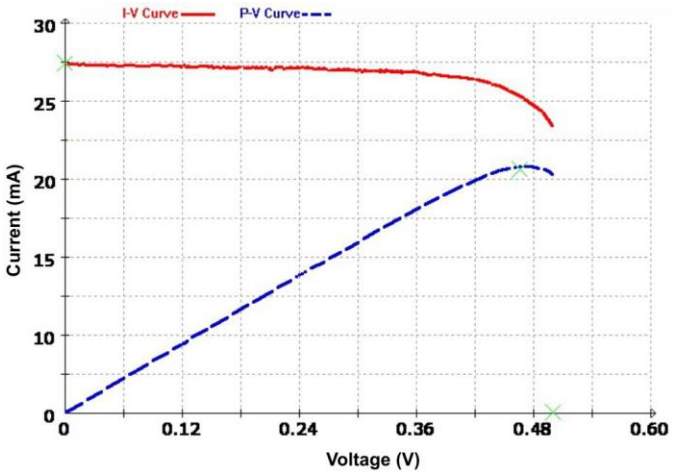

Fig. 5. IV curve obtained with the simplified cell geometry

IV. TCAD Modelling

In this section 2D TCAD simulations of the optical and electrical behavior of the HELICS cell are presented, along with the expected efficiency as a function of device parameters. Simulations are performed using the Sentaurus

TCAD software from Synopsys. Parameters of particular interest for this work are the n-type groove depth and the selected level of silicon wafer quality (specified in terms of a recombination time), as these relate to some of the key advantages claimed in terms of efficiency and cost of the HELICS technology.

Fig. 6 shows calculated efficiency as a function of the distance from the groove tip to the front surface of the wafer, for the case of 200 µm thick (semiconductor grade) silicon wafers. We expect a somewhat higher efficiency in reality, as the simulations reported here do not include wafer texture. Process 1 is for grooves filled partially with metal and process 2 shows the modelled results for the grooves filled entirely with metal.

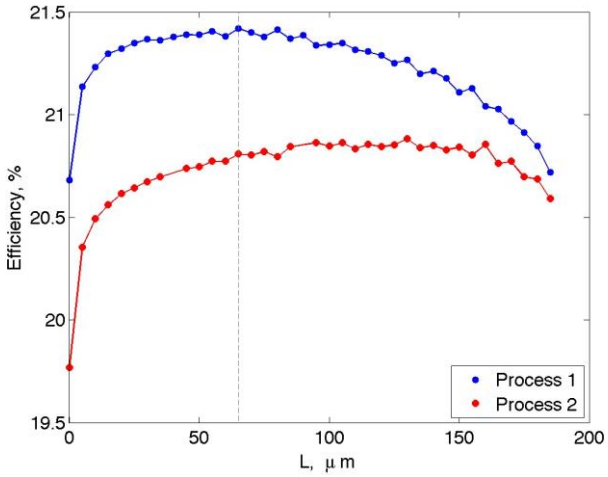

Fig. 6. Simulated efficiency versus groove-tip to front-surface separation, *L*, in the HELICS technology, using two alternative processing options. Efficiency is for an un-textured cell. When texture is included in simulations, and in practice, one may expect efficiency in the range 22-24%.

The efficiency increases as the groove depth is increased (i.e. as the groove tip approaches the front surface), until the groove starts to affect the optical absorption significantly. At this point despite improved collection of the generated carriers, overall efficiency falls as a dead zone begins to form. For 'process 1' the optimal tip-to-surface distance in a 200-µm thick wafer is about 65 µm (vertical line in Fig. 6).

Fig. 7 shows the dependence of efficiency on wafer quality for the two processes shown in Fig. 6. In both cases the efficiency is significantly better than in a standard IBC cell using wafer thicknesses that can currently be handled on an industrial scale.

Table 1 shows the expected modelled efficiency of the device compared to the actual measured efficiency from fabricated devices. It shows that for the simple device, the model would give us a device of 8.3% efficiency, and the actual measured efficiency was 8%. Adding some simple process steps to include a front side emitter and doping the p-type grooves should show considerable efficiency improvements.

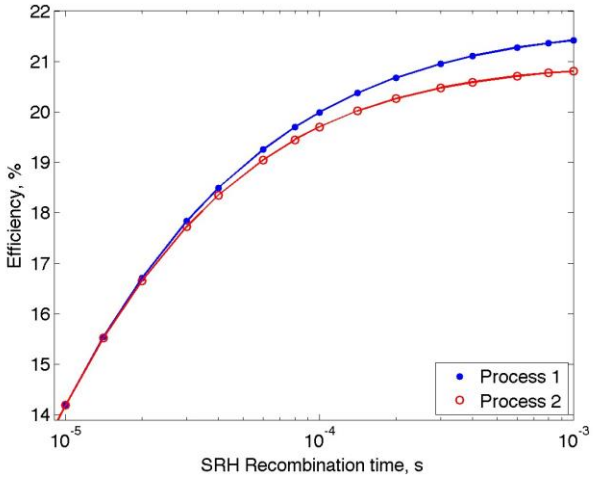

Fig. 7. Simulated efficiency versus wafer quality

	Modelled Efficiency	**Measured Efficiency**
Simple Device	*8.3%*	*4-8%*
+Front side emitter	*+7%* *(15.3%)*	-
+Improved back contact for *p*-type grooves	*+4.5%* *(19.8%)*	-

Table 1. Device steps with modelled and measured efficiency.

V. Antireflection Coating Optimization

Using a transfer matrix approach [4], the transmittance of light through the oxide/nitride stack on a flat silicon substrate was calculated for thicknesses of SiO_2 and Si_3N_4 from 0-350 nm (Fig.8). The refractive index data for SiO_2 and LPCVD Si_3N_4 were obtained from [4] and [5], respectively.

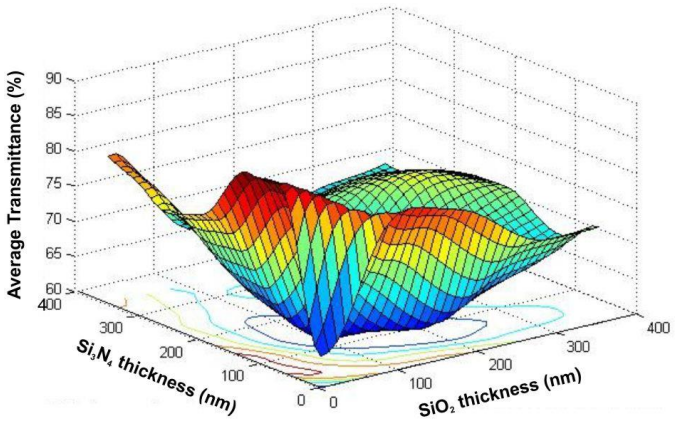

Fig. 8. Surface plot of SiO_2 and Si_3N_4 thicknesses vs. average transmittance.

The transmittance can be weighted to the spectral irradiance ($I(\lambda)$) of the AM1.5 solar spectrum (ASTM173G, global tilt) and then the average weighted transmittance (T_w) can be calculated using (1).

$$T_w = \frac{\int_{\lambda\min}^{\lambda\max} T(\lambda) I(\lambda)\, d\lambda}{\int_{\lambda\min}^{\lambda\max} I(\lambda)\, d\lambda} \quad (1)$$

T_w can then be used as a figure of merit in an optimization of the thicknesses of the two layers in the stack. This was implemented in Matlab using a simplex-based search method. A contour map of the calculated T_w versus thicknesses of oxide and nitride layers is shown in Fig. 9. The optimum values are presented in Table 2.

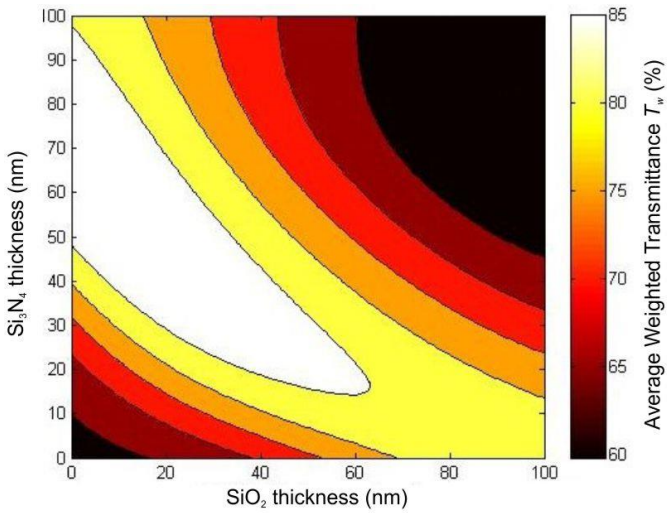

Fig. 9. Contour map of T_w vs. SiO_2 and Si_3N_4 thicknesses.

Oxide thickness (nm)	2.3
Nitride thickness (nm)	65.5
T_w (%)	89.6

Table 2. Optimized values of oxide and nitride thickness for antireflective coating.

This optimization does not consider passivation requirements which would have to be included before these thicknesses can be implemented in the next batch of solar cells to further reduce the front surface reflectance. Further improvements are possible by using experimental refractive index data from the cell fabrication process in the optimization calculations. Also, the current optimization only considers a planar surface and so could be advanced by accounting for the pyramidal texturing.

VI. Future Work

Back contact cells have already been proven to be able to give higher efficiencies than conventional solar cells. The ability to overcome the problems associated with them (cost and ease of fabrication) will allow production of high efficiency cells at prices competitive with conventional low-cost solar cells.

The next stages of this project are to fabricate the full design incorporating the simplified design as well as the floating emitter and epitaxial deposition. Once a working device has been made in this architecture, each step will be optimized which should allow us to achieve our goal efficiency of 22-24%. Fig. 10 shows the proposed process steps for the enhanced cell design.

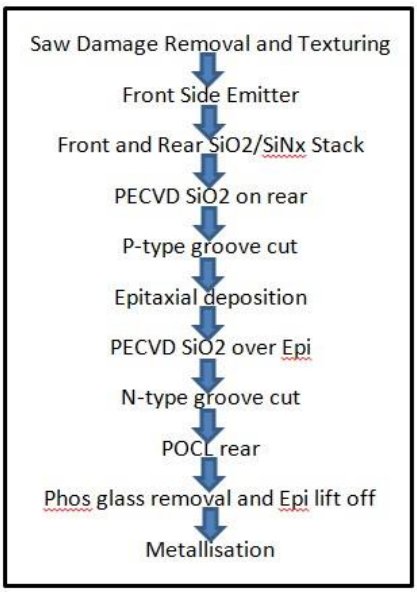

Fig. 10. Process steps for enhanced cell design

VII. Conclusions

This report presents a new approach to IBC solar cell design and fabrication which uses low cost manufacturing techniques and enables silicon with relatively short diffusion lengths to be used. Working devices have been demonstrated with performances in line with predictions from simulations. Modelling suggests that by implementing several relatively simple improvements to the design, this cell geometry is capable of achieving efficiencies of 22-24%.

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