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FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Electronics and Computer Science

Efficiency Improvement in MEMS Thermoelectric Generators Employing Solar Concentration

by

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ABSTRACT

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Thermoelectric generators (TEGs) are devices that convert heat into electricity. The efficiency of thermoelectric generators depends on the temperature difference across the device, the average temperature of operation, and on the thermoelectric properties of the material. Most work on improving the TEG efficiency deals with improving the thermoelectric properties of the material. In this work, a method of improving the efficiency of the TEG by increasing the temperature difference is proposed. To accomplish this, a lens is used to concentrate solar radiation on the membrane of the TEG. By focusing solar radiation, the input heat flux increases; the temperature difference also increases; and the efficiency of the TEG improves as well.

Two implementations of the TEG are explored. The first one involves a simple TEG implementation using a glass substrate with p-type polysilicon and aluminum as the thermoelectric materials. Although a significant amount of heat is lost through the substrate, test results still demonstrate that a significant improvement in the device efficiency as the input heat flux is increased. The second implementation involves fabricating the TEG on a SOI substrate where the buried oxide layer is not etched and a thin portion of the handle layer is retained to provide additional structural stability. The thermoelectric materials for this TEG implementation are p-type silicon and aluminum. Although this implementation performs poorly than when both handle and buried oxide layers of the SOI under the membrane and thermoelements are etched, a SOI wafer with a thinner device layer is used to compensate for the losses.

The fabricated TEGs are characterized using a laser test set-up where the input power is varied up to 1 W and the spot size diameter is fixed at 1 mm. Measurement results on fabricated TEGs with 1 W input power exhibited a temperature difference of up to 226 $^\circ$C, open-circuit voltage of 3 V, output power of 25 μW, and about 10 times improvement in conversion efficiency. The fabricated TEGs are also tested using a solar simulator and three lenses of different diameters to emulate conditions where the device would be deployed as a solar TEG. Using a 50.8 mm diameter lens, the largest temperature difference measured is 18 $^\circ$C, which gives an open-circuit voltage and output power of 803 mV and 431 nW, respectively.

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DECLARATION OF AUTHORSHIP

I, Maria Theresa G. de Leon, declare that this thesis entitled

"Efficiency Improvement in MEMS Thermoelectric Generators Employing Solar Concentration "

and the work presented in it are my own and has been generated by me as the result of my own original research.

I confirm that:

1. This work was done wholly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
4. Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
5. I have acknowledged all main sources of help;
6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
7. Parts of this work have been published as:
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Signed: .....

Date: .....

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Definitions and Abbreviations

T_H	Hot side temperature
T_C	Cold side temperature
ΔT	Temperature difference
V_O	Open-circuit voltage
α_{AB}	Seebeck coefficient of thermocouple with materials A and B
I	Current through conductor
q	Heating rate
π_{AB}	Peltier coefficient of thermocouple with materials A and B
β	Thomson coefficient
N	Number of thermocouples
α_A	Seebeck coefficient of material A
α_B	Seebeck coefficient of material B
R_L	Load resistance
$P_{O,max}$	Maximum power delivered to the load
R_{TEG}	Electrical resistance of TEG
η_{TEG}	TEG efficiency
η_C	Carnot efficiency
$\bar{T}$	Average absolute temperature
Z	Thermoelectric figure-of-merit
α	Seebeck coefficient
λ	Thermal conductivity
ρ	Electrical resistivity
ϕ	TEG efficiency factor
A_G	TEG chip area
η_{tot}	Total efficiency
η_s	Solar concentrator efficiency
η_{th}	Thermal collector efficiency
q_h	Heat power density of incoming heat flux
γ	Solar concentration factor
τ_{lens}	Lens transmittance
α_{mem}	Membrane absorptance
q_s	Solar irradiation density

$d_{lens,eff}$	Effective lens diameter
d_{spot}	Spot size diameter
Q_{MEM}	Heat flow rate from heat absorber to TEG
Q_{RIM}	Heat flow rate from TEG to rim
T_1	Membrane temperature
T_2	Rim temperature
α_{Al}	Seebeck coefficient of aluminum
$\alpha_{p\text{-}Si}$	Seebeck coefficient of p-type silicon
ρ_{Al}	Electrical resistivity of aluminum
$\rho_{p\text{-}Si}$	Electrical resistivity of p-type silicon
λ_{Al}	Thermal conductivity of aluminum
$\lambda_{p\text{-}Si}$	Thermal conductivity of p-type silicon
l	Thermoelement length
w	Thermoelement width
t	Thermoelement thickness
S_{TEG}	Total Seebeck coefficient of TEG
K_{TEG}	Total thermal conductance of TEG
V_{TEG}	Open-circuit TEG voltage
P_{OUT}	TEG output power under matched load conditions
A_h	Surface area of heated part of TEG membrane
Q_{IN}	TEG input power
K_{MEM}	Thermal conductance between thermocouples and heat absorber
K_{RIM}	Thermal conductance between thermocouples and rim
$Q_{CONV,M}$	Heat loss due to convection at membrane
$Q_{CONV,R}$	Heat loss due to convection at rim
$Q_{RAD,M}$	Heat loss due to radiation at membrane
$Q_{RAD,R}$	Heat loss due to radiation at rim
A_{MEM}	Surface area of membrane
A_{RIM}	Surface area of rim
A_{TEG}	Surface area of thermoelements
ε	Surface emissivity
σ	Stefan-Boltzmann constant
h_{conv}	Convective heat transfer coefficient

d_{mem}	Membrane diameter
w_{tr}	Isolation trench width
$R_A,\ R_B$	Van der Pauw structure's characteristic resistances
R_S	Sheet resistance
U	Thermovoltage between two ends of a planar structure
R_C	Contact resistance
S_{side}	Sidewall step coverage
S_{bot}	Bottom step coverage
C	Cusping
T_{SUB}	Temperature at bottom of glass substrate
K_{SUB}	Thermal conductance of substrate directly below heated area of membrane
$Q_{CONV,SUB}$	Heat loss due to convection through substrate
A_{SUB}	Surface area of substrate
TCR_{Al}	Temperature coefficient of resistance of aluminum
R_{series}	Series resistance
R_{t0}	Initial resistance of temperature monitor
R_t	Resistance of temperature monitor
V_{planar}	Voltage across planar structure
V_{canti}	Voltage across cantilever structure
α_{poly}	Seebeck coefficient of HWCVD polysilicon
ρ_{poly}	Electrical resistivity of HWCVD polysilicon
λ_{poly}	Thermal conductivity of HWCVD polysilicon
P_{in}	Actual laser input power to the TEG
T_{amb}	Ambient temperature
λ_{glass}	Thermal conductivity of glass substrate
$d_{spot,min}$	Minimum spot size
D	Lens diameter
f	Lens focal length
n	Lens refractive index
k	Lens shape factor
t_c	Lens center thickness
t_e	Lens edge thickness
R	Lens radius of curvature

f_b	Lens back focal length
$d_{lens\text{-}to\text{-}spot}$	Distance between the flat side of the plano-convex lens to the actual spot size
K_{BOX}	Thermal conductance of buried oxide layer directly below heated area of membrane
K_{HAN}	Thermal conductance of thinned handle layer directly below heated area of membrane
T_{HAN}	Temperature at the bottom of the thinned handle layer
$Q_{CONV,HAN}$	Heat loss due to convection through thinned handle layer
α_{Si}	Seebeck coefficient of SOI device layer
ρ_{Si}	Electrical resistivity of SOI device layer
λ_{Si}	Thermal conductivity of SOI device layer
λ_{SiO2}	Thermal conductivity of buried oxide layer

CA	Clear Aperture
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical Mechanical Polishing
CPC	Compound Parabolic Collector
DI	Deionized
DRIE	Deep Reactive Ion Etching
DSSC	Dye-Sensitized Solar Cell
EEG	Electroencephalogram
ETC	Evacuated Tube Collector
FNA	Fuming Nitric Acid
FPC	Flat Plate Collector
FTIR	Fourier Transform Infrared Spectroscopy
HF	Hydrofluoric Acid
HFVPE	HF Vapor Phase Etching
HWCVD	Hot Wire Chemical Vapor Deposition
ICP	Inductively Coupled Plasma
IPA	Isopropyl Alcohol
IR	Infrared
KOH	Potassium Hydroxide
LF	Low Frequency

LPCVD	Low Pressure Chemical Vapor Deposition
MEMS	Microelectromechanical Systems
MIF	Metal Ion Free
MOCVD	Metal Organic Chemical Vapor Deposition
NDF	Neutral Density Filter
NIR	Near Infrared
NMP	N-Methyl-2-Pyrrolidone
OIPT	Oxford Instruments Plasma Technology
ORC	Optoelectronics Research Center
PCB	Printed Circuit Board
PECVD	Plasma Enhanced Chemical Vapor Deposition
PV	Photovoltaic
RF	Radio Frequency
RIE	Reactive Ion Etching
SEM	Scanning Electron Micrograph
SOI	Silicon-on-Insulator
SSA	Solar Selective Absorber
STC	Silicon Thin-Film Cell
STEG	Solar Thermoelectric Generator
TC	Thermocouple
TE	Thermoelectric
TEC	Thermoelectric Cooler
TEG	Thermoelectric Generator
TEOS	Tetraethyl Orthosilicate
TIC	Thermoionic Converter
TSG	Tantalum-Antimony-Germanium
USG	Undoped Silicate Glass
UV	Ultraviolet

Chapter 1: Introduction

The global energy crisis has paved the way for researchers to explore alternative means of generating power. One approach to providing electrical energy is by direct conversion of heat to electricity with the use of thermoelectric generators (TEGs). It is attractive to use TEGs because they have no mechanical parts; hence resulting in an alternative power system that is silent, stable, reliable, environment-friendly, and possess virtually unlimited lifetime (Deng & Liu 2009)(Strasser et al. 2004).

A major challenge in the design of TEGs is its limited efficiency. A typical thermoelectric device exhibits only 5-10% conversion efficiency depending on the materials used and the temperature difference involved (Matsubara and Matsuura 2006). Meanwhile, the best solar cell at present is 3-5 times more efficient than thermoelectric devices (Savage 2011). One way to increase the conversion efficiency of a TEG is by increasing the temperature difference across the thermoelements (Rowe 2006a)(Chen & Ren 2010). An increase in temperature difference can be realized by using a high input heat flux such as that coming from the sun (Chen et al. 2011). In this regard, the use of a solar concentrator to improve the efficiency of TEGs by focusing solar radiation onto the hot junction of the TEG is proposed. By doing so, the temperature difference across the device can be increased; subsequently improving the TEG's efficiency.

1.1 Motivation

Several implementations of TEGs focus on improving its efficiency by exploring advanced thermoelectric materials such as skutterudites (Wang et al. 2001)(Chen et al. 2011), clathrates (Kleinke 2010), Zn-Sb alloys (Caillat & Fleurial 1996), Pb-Te alloys (Gelbstein, Dashevsky, and Dariel 2008)(Heremans et al. 2008)(Mu 2010)(Pei et al. 2011), InGaN alloys (Pantha et al. 2009), and ZnO alloys (Schaeuble et al. 2008)(Ong, Singh, and Wu 2011). Higher efficiency TEGs have also been designed by using segmented thermoelectric legs to exploit the operating temperatures of several materials;

thereby optimizing heat flow across the thermoelements (Fleurial et al. 1996)(Caillat et al. 2001)(Maciá 2004)(Snyder 2004). Meanwhile, other researchers emphasized nanostructuring of bulk materials to improve the material's thermoelectric figure merit (Majumdar 2004)(Qiu 2008)(Singh & Terasaki 2008)(Lan et al. 2010). In nanostructuring, the material's figure of merit is increased by creating materials composed of nanosized grains. By doing so, the thermal conductivity of the material is decreased while maintaining its electrical conductivity. The technique of nanostructuring has been applied to silicon (Bunimovich 2007) (Hochbaum et al. 2008)(Lee et al. 2008)(Bux et al. 2009)(Ramayya and Knezevic 2009)(Boukai 2010)(Cerofolini et al. 2010)(Hao et al. 2010), silicon germanium (Ghamaty 2006)(Wang et al. 2008), bismuth telluride alloys (Venkatasubramanian et al. 2001)(Wang et al. 2005)(Koukharenko et al. 2008)(Lan et al. 2009)(Minnich et al. 2009), and complex cobalt oxides (Robert et al. 2005).

The above-mentioned techniques focus on improving the thermoelectric properties of the materials to improve the efficiency of the TEG. While results obtained by these techniques are promising, synthesizing novel compounds, fabricating segmented thermoelements, and creating nanostructured materials are quite complex.

Another aspect that can be explored to improve the efficiency of a TEG is by increasing the temperature difference across the thermoelements. This can be accomplished by increasing the amount of input heat flux at the hot junction of the generator. In this regard, a solar concentrator can be used to concentrate solar radiation onto the hot side of the TEG. Several researches have demonstrated the functionality of such systems on a large scale by using commercially-available solar concentrators and TEG modules.

At chip scale, the use of a lens to concentrate light onto a TEG that serves as power supply to a microactuator have already been proposed (Baglio et al. 2002a). Recently, an improvement in TEG efficiency has been achieved by employing both solar and thermal concentration on a flat-panel solar thermoelectric generator composed of a pair of n- and p-type thermoelectric materials based on nanostructured Bi_2Te_3 alloys (Kraemer et al. 2011). Despite having the best thermoelectric figure of merit, the use of Bi_2Te_3 alloys in

MEMS systems is hindered by challenges in technological compatibility (Roncaglia & Ferri 2011). It is therefore more practical to use materials like silicon or polysilicon as thermoelectric materials as they have better compatibility with standard CMOS and MEMS processes. Thus, it is worthwhile to investigate the feasibility of implementing solar thermoelectric generator (STEG) systems utilizing conventional materials in MEMS and CMOS processing and characterize its improvement in efficiency as this gives way to future advancements in solar energy harvesting.

Preliminary heat transfer simulations on a proposed STEG design have shown promising results in terms of increasing the temperature difference across the device. Hence, a prototype of this system is to be developed using simple fabrication processes that are compatible with existing CMOS and MEMS technologies. It is important to choose materials and processes that will enable easy integration of the solar-driven TEG with on-chip electronics as this microscale system is envisioned to have promising applications in on-board power sources, sensor networks, and autonomous microsystems.

1.2 Objectives

The main objective of this study is to demonstrate the effectiveness of using solar concentrators in improving the efficiency of thermoelectric generators. To do this, several TEGs with different geometries must be designed and fabricated so the effects of the physical parameters of the device on its performance can be investigated. The fabricated TEGs must then be tested and properly characterized to establish the improvement in efficiency. Note that it is envisioned to have TEGs with a temperature difference of more than 300 $^\circ$C. This would govern decisions made during the study concerning the dimensions of the devices to be fabricated, as well as the materials to be used in fabrication.

The secondary objective of this work is to develop an analytical model that predicts the performance of the TEG depending on its geometry, material properties, and input conditions. By having an analytical model that can closely estimate the actual performance of the device; it can be demonstrated how much improvement in efficiency is

can be achieved by using solar concentrators along with TEGs that have better thermoelectric materials.

1.3 Contributions

This thesis brings a number of contributions to the field of solar thermoelectric generator research. First, the design and fabrication of a thermoelectric generator with the thermoelements oriented radially around a circular membrane was explored. Most lateral TEG implementations in literature use square or rectangular membranes. By using a circular membrane, optimum transfer of heat from the membrane to the hot side of the thermoelements is established. Second, this thesis explored the use of a lateral TEG in a STEG system as this type of TEG is simpler to fabricate and has better potential for integration with on-chip electronics. Micro-level implementations of solar thermoelectric generators found in literature utilize vertical TEGs. Third, analytical thermal models of the TEGs considered in this work were developed. These models, which are based on the use of lumped thermal conductances, are computationally simpler than finite element modelling and agreed reasonably well with the actual measurement results. Lastly, this thesis also investigated the use of hot-wire chemical vapor deposited polysilicon as a thermoelectric material. To the researchers' knowledge, this is the first time that the use of hot-wire polysilicon in thermoelectric generators is reported.

1.4 Thesis Organization

This report examines the current state of thermoelectric generators and solar TEGs in Chapters 2 and 3, respectively. Chapter 4 describes the heat transfer simulations performed in COMSOL and the thermal equivalent model developed based on energy balance equations. Chapter 5 gives information on the TEG design, layout, and proposed fabrication process. Chapters 6 and 7 provide details on the two TEG implementations realized in this work. Lastly, Chapter 8 presents the conclusions of this research, including its limitations, as well as suggesting directions for further studies. The structure and content of each chapter are discussed in detail below.

Chapter 2: Thermoelectric generators. This chapter presents a review of published works on thermoelectric generators. Basic principles governing thermoelectric conversion are first discussed, followed by different metrics used to evaluate TEG performance. Then, the three types of TEGs are enumerated and focus is given on published lateral/lateral implementations as it is the type selected for this work.

Chapter 3: Solar thermoelectric generators. This chapter presents a review of published works on solar thermoelectric generators (STEGs). An overview of the concept of solar-powered thermoelectric generators is first presented. Then, three types of STEGs are described and several implementations of each STEG type are examined. Lastly, thermal-photovoltaic hybrid systems are also discussed to demonstrate the possibility of further enhancement in efficiency by utilizing both photovoltaic and thermoelectric technologies.

Chapter 4: STEG simulation and modelling. The design of the proposed STEG with a lens acting as a solar concentrator is presented in this chapter. Heat transfer simulation results are also given to verify that the use of a solar concentrator significantly increases the temperature difference across the TEG, consequently resulting in an improvement in device efficiency. Then, an analytical thermal model of the device is developed. Finally, results obtained from heat transfer simulations are compared to those calculated using the thermal model to validate the model's ability to predict the STEG's thermoelectric performance.

Chapter 5: TEG design and proposed fabrication. In this chapter, details on the design of the TEG are reported. Several design considerations are presented and the dimensions of the TEGs to be fabricated are given. The proposed TEG fabrication procedure is also presented, where two methods explored in refilling isolation trenches are discussed. Lastly, the problems encountered in the fabrication process are described, which led to the investigation of alternative means of fabricating TEGs.

Chapter 6: TEG implementation on a glass substrate. This chapter focuses on the TEG implementation on a glass substrate. The design and modifications to the thermal model are presented first, followed by a description of the fabrication process. Lastly, measurement results with a laser set-up and with a solar simulator are presented and analyzed.

Chapter 7: TEG implementation on a SOI substrate. In this chapter, the discussion is focused on the TEG implementation on a SOI substrate. The design and modifications to the thermal model are presented first, followed by a description of the fabrication process. Measurement results with a laser set-up and with a solar simulator are also presented and analyzed. Finally, the performance of TEGs implemented on a SOI substrate is compared with that of TEGs implemented on a glass substrate.

Chapter 8: Conclusions and recommendations. This chapter draws some conclusions from the work and ideas in this thesis. Recommendations for future research to extend the usefulness of the proposed system are also set out.

Chapter 2: Thermoelectric Generators

This chapter presents a review of published works on thermoelectric generators. First, basic principles governing thermoelectric conversion are discussed, followed by different metrics used to evaluate TEG performance. Then, the three types of TEGs are enumerated and focus is given on published lateral/lateral implementations as it is the type selected for this work.

2.1 Thermoelectricity

There are three basic principles governing thermoelectric energy conversion: (1) Seebeck effect, (2) Peltier effect, and (3) Thomson effect.

2.1.1 Seebeck Effect

The principle of thermoelectric energy conversion can be easily discussed by referring to the schematic of a thermocouple shown in Figure 2-1. The thermocouple, made of two dissimilar electrically conducting materials (metal or semiconductor) A and B, are connected electrically in series and thermally in parallel. The Seebeck effect occurs when the junction between A and B, and the materials' edges, are maintained at different temperatures T_H and T_C where T_H is greater than T_C. The difference between these two temperatures is also denoted as ΔT. An open circuit voltage V_O is generated across nodes a and b and is given by:

$$V_O = \alpha_{AB}(T_H - T_C) = \alpha_{AB}\Delta T \tag{2-1}$$

where α_{AB} is the Seebeck coefficient of the thermocouple; and

T_h and T_C are the temperatures at the hot and cold sides, respectively.

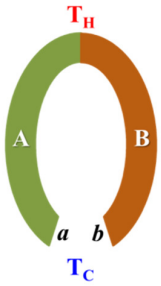


Figure 2-1: Diagram of a basic thermocouple.

The major contributor to the Seebeck voltage is the higher average velocity in charge carriers with increasing temperature (VanHerwaarden & Sarro 1986). Hence, the diffusion of electrons from the hot side into the cold side dominates the transport of carriers as electrons from the hot side have a higher average velocity. This leads to a build-up of charges on the cold side and since there can be no net current in the circuit, a potential is set up such that the charges on the cold side are attracted to the hot side in order to counteract the natural flow of the charge carriers. Another contributor to the Seebeck voltage is that the Fermi energy of the material moves further away from the band edge with increasing temperature (O'Mara et al. 1990). This phenomenon is shown in the energy band diagram of an n-type semiconductor in Figure 2-2 where the change in temperature causes the Fermi level to shift such that there is flow of electrons from a higher Fermi energy (cold side) to a lower Fermi energy (hot side). This phenomenon is often ignored as it usually has negligible effect to the total Seebeck voltage. The third contributor to the Seebeck voltage is due to thermally-excited lattice vibrations or phonons (MacDonald 2006). A temperature difference across a thermoelectric material causes the phonon system to be placed out of thermodynamic equilibrium. This is evident in the heat current generated where phonon energy is propagated down the temperature difference. If there is strong interaction between phonons and charge carriers, the phonons may impart some of their energy to the diffusing carriers via momentum transfer. At open circuit, the phonons effectively 'drag' the carriers along the temperature difference which causes an increase in the build-up of charges on the cold side, on top of that contributed by diffusion alone. This phenomenon contributes significantly to the Seebeck voltage at temperatures lower than room temperature. In

general, diffusion dominates the Seebeck voltage in metals while phonon drag dominates the Seebeck voltage in semiconductors (Boukai 2008).

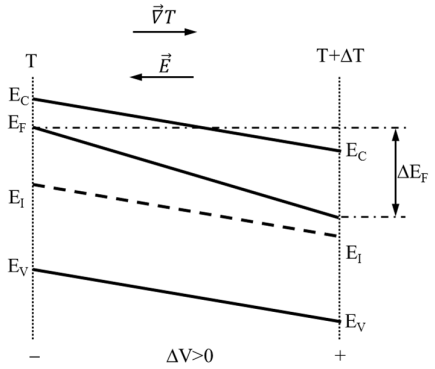


Figure 2-2: Energy band diagram showing the change in Fermi energy of an n-type semiconductor when a temperature difference is applied across it.

2.1.2 Peltier Effect

Referring back to Figure 2-1, the Peltier effect happens when an external voltage source is applied across nodes a and b. When a clockwise current I flows through the conductors, a rate of heating q occurs at one junction while a rate of cooling -q occurs at the other junction. The ratio of the electric current I to the heating rate q defines the Peltier coefficient π_{AB} of the thermocouple and is given by:

$$\pi_{AB} = {}^{I}/_{q} \tag{2-2}$$

2.1.3 Thomson Effect

In the Thomson effect, heat is absorbed or produced at a rate q as a result of current I flowing through a portion of a single conductor where there is a temperature difference ΔT. The heating rate q is related to I and ΔT by:

$$q = \beta I \Delta T \tag{2-3}$$

where β is the Thomson coefficient.

2.1.4 Kelvin Relationships

The three thermoelectric coefficients previously mentioned are related by the Kelvin relationships:

$$\pi_{AB} = \alpha_{AB} T \tag{2-4}$$

$$\frac{d\alpha_{AB}}{dT} = \frac{\beta_A - \beta_B}{T} \tag{2-5}$$

where T is the absolute temperature.

Equation 2-4 describes the relationship between the Seebeck and Peltier effects, and indicates that materials suitable for thermoelectric power generation are also suitable for thermoelectric refrigeration. Equation 2-5, on the other hand, describes the relationship between the Seebeck and Thomson effects, and defines the Seebeck coefficient of a single material to be $d\alpha = (\beta/T)dT$. Note that in contrast to *temperature difference* ΔT, which denotes the difference between temperatures at two specific points of a material, the *temperature gradient* dT, describes at what rate the temperature changes along the length of a material.

Moreover, it can also be derived from equation 2-5 that the Seebeck coefficient of a thermocouple is equal to the difference between the Seebeck coefficients of the two materials or simply put,

$$\alpha_{AB} = \alpha_A - \alpha_B. \tag{2-6}$$

2.1.5 TEG Performance Metrics

As shown in Figure 2-3, a thermoelectric generator is basically composed of a number of thermocouples connected electrically in series and thermally in parallel. By the Seebeck effect, the difference between the temperature at the hot junction T_H and the temperature at the cold junction T_C results in an open-circuit output voltage given by:

$$V_O = N(\alpha_A - \alpha_B)(T_H - T_C) \tag{2-7}$$

where N is the number of thermocouples and

α_A and α_B are the Seebeck coefficients of the two thermoelectric materials used.

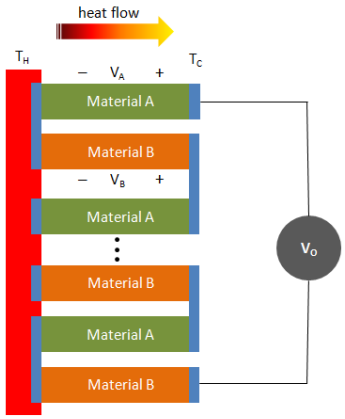


Figure 2-3: A basic thermoelectric generator.

If a load resistance R_L is attached to the output of the TEG, the maximum power delivered to the load is:

$$P_{O,max} = \frac{V_O^2}{4R_{TEG}} \tag{2-8}$$

where R_{TEG} is the electrical resistance of the TEG and $R_{TEG} = R_L$.

The efficiency of the TEG is the ratio between the energy supplied to the load and the heat energy absorbed at the hot junction. At maximum power output, the TEG efficiency is derived to be equal to (Rowe & Bhandari 1983):

$$\eta_{TEG} = \eta_C \gamma \tag{2-9}$$

where η_C is the Carnot efficiency described as

$$\eta_C = \frac{T_H - T_C}{T_H} \tag{2-10}$$

and γ embodies the parameters of the thermoelectric materials and is given by:

$$\gamma = \frac{\sqrt{1+Z\bar{T}}-1}{\sqrt{1+Z\bar{T}}+{}^{T_C}/_{T_H}}. \tag{2-11}$$

$\bar{T}$ is the average absolute temperature of the hot and cold junctions, i.e. $\bar{T} = \frac{T_H+T_C}{2}$, and Z is the figure of merit of the thermocouple defined as:

$$Z = \frac{\alpha^2}{\lambda\rho} \tag{2-12}$$

where α, λ, and ρ are the Seebeck coefficient, thermal conductivity and electrical resistivity of the thermocouple, respectively.

Based on equation 1-12, an efficient thermocouple should then have high Seebeck coefficient, low thermal conductivity, and low electrical resistivity. Metals typically have Seebeck coefficients of 10μV/K or less, high thermal conductivity, and low electrical resistivity, giving efficiencies of only a fraction of 1% (Rowe 1995). Although the ratio of the thermal to electrical conductivity of semiconductors is greater than in metals, semiconductors possess Seebeck coefficients in excess of 100μV/K leading to efficiencies of about 5% (Rowe & Bhandari 1983).

Going back to equation 2-10, it is evident that an increase in the temperature difference across the thermoelements provides a corresponding increase in the Carnot efficiency; subsequently increasing the efficiency of the TEG in equation 2-9. The relationship between the conversion efficiency and the operating temperature difference for different values of Z is shown in Figure 2-4. It can be seen on this plot that large temperature differences are desirable to achieve higher conversion efficiency. As an example, a thermocouple fabricated from thermoelement materials with an average Z of $3\text{x}10^{-3}$ K^{-1} would have an efficiency of around 20% when operated over a temperature difference of 500K.

To optimize the efficiency of thermoelectric generators, it is also important to consider thermal matching of the thermoelectric generator to the other heat fluxes present in its environment (Leonov et al. 2009). For optimum thermal matching, the thermal

resistance of the TEG must be equal to the combined thermal resistance of all the other heat fluxes present in its environment.

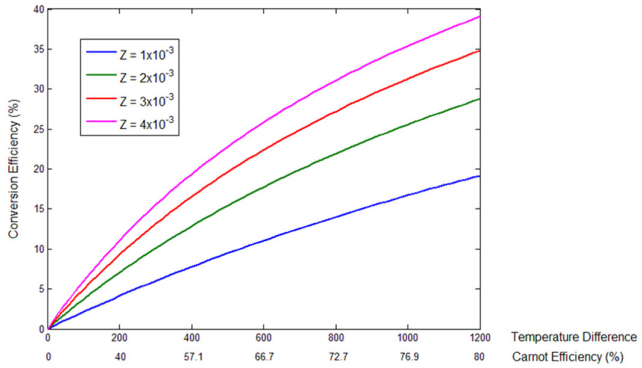


Figure 2-4: Conversion efficiency as a function of temperature and thermocouple material figure of merit Z. Cold junction temperature is 300K.

To compare the output power of different TEGs, (Strasser et al. 2004) introduced another figure of merit defined as the thermoelectric efficiency factor ϕ and is defined as:

$$\phi = \frac{P_O}{A_G \cdot \Delta T^2} \tag{2-13}$$

where A_G is the TEG chip area and ΔT is the temperature difference across the thermoelements.

2.2 Types of Micro-TEGs

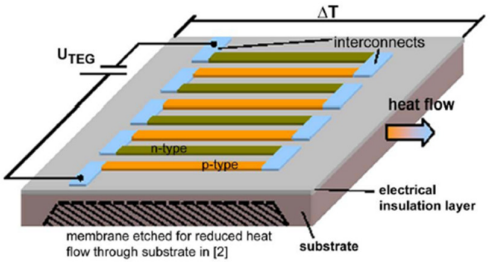
Thermoelectric generators (TEGs) are devices that convert heat into electricity. It is advantageous to use TEGs as alternative power sources because they are extremely reliable, silent in operation, small in size, capable of operating at high temperatures, suitable for small-scale and remote applications, and environment-friendly (Ismail and Ahmed 2009).

Microscale TEGs, shown in Figure 2-5, can be classified into three types based on the direction of heat flow through the device and on the layout orientation of the thermocouples during fabrication (Glatz et al. 2009). These are:

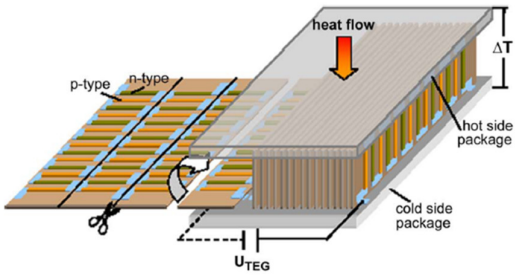
1. Lateral/Lateral TEG – lateral heat flow and laterally-fabricated thermocouples

2. Vertical/Lateral TEG – vertical heat flow realized by assembly of laterally-fabricated thermocouples
3. Vertical/Vertical TEG – vertical heat flow and vertically-fabricated thermocouples

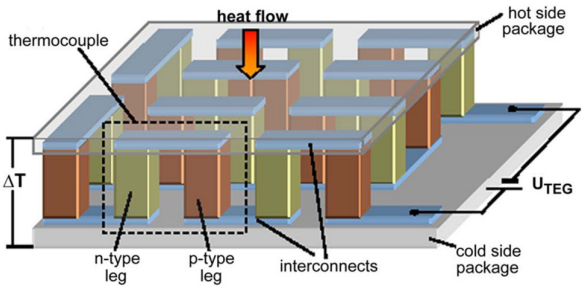
Initial implementations of microscale TEGs (μTEGs) are of the lateral/lateral type. This was mainly due to limitations in deposition thickness of available thin-film deposition methods to achieve a sufficient thermocouple length. First implementations of this type used n-type and p-type silicon (Rowe et al. 1989), n-type and p-type polysilicon (Kiely et al. 1994), polysilicon and Al (Sarro et al. 1994), or silicon and Al (Nieveld 1982)(Glosch et al. 1999) as the thermoelectric materials. Eventually, since deposition of polysilicon is an established fabrication process and polysilicon has fairly good thermoelectric



(a)



(b)



(c)

Figure 2-5: Three types of micro-TEGs. (a) Lateral/Lateral TEG, (b) Vertical/Lateral TEG, and (c) Vertical/Vertical TEG. (Glatz et al. 2009)

properties, majority of succeeding implementations of lateral/lateral μTEGs used n-type and p-type polysilicon thin films as thermoelectric materials (Jacquot et al. 2002)(Tseng et al. 2008)(Yang et al. 2009)(Kao et al. 2010)(Xie et al. 2010). To simplify the fabrication of the thermoelements, other implementations use n-type polysilicon and a metal (Al or Ni) as the thermoelectric materials (Huesgen et al. 2008)(Randjelović et al. 2008)(Hong et al. 2009). Lastly, some implementations explore the use of other thermoelectric materials such as Sb-Bi thermocouple pairs (Qu et al. 2001)(Savelli et al. 2006), Au-Ni thermocouples (Boniche 2010), NiCr and CuNi pairs (Chen et al. 2004), n-type and p-type poly-SiGe (Schaevitz et al. 2001), n-type Bi_2Te_3 and p-type Sb_2Te_3 thin films (Ghafouri et al. 2008)(Goncalves et al. 2008)(Carmo et al. 2010), n-type Bi_2Te_3 and p-type $Bi_{0.4}Sb_{1.6}Te_3$ (Kwon et al. 2009), n-type $Bi_2Te_{2.7}Se_{0.3}$ and p-type $Bi_{0.4}Te_3Sb_{1.6}$ (Takashiri et al. 2007)(Kurosaki et al. 2009), n-type GaN and Au (Sztein et al. 2009), and PdAg and a Ta-Sb-Ge alloy (Markowski et al. 2005).

To demonstrate the advantage of vertical heat flow, which occurs in commercially-available TEGs, lateral/vertical μTEGs are eventually designed. One way to accomplish this is by integrating microcavities in the substrate to direct heat to flow vertically on n-type and p-type polysilicon thermocouples (Strasser et al. 2002)(Strasser et al. 2004) or n-type and p-type poly-SiGe (Su et al. 2010). Another way to implement vertical heat flow is by folding a polyimide sheet patterned with planar Cu-Ni thermocouples into a wavelike shape (Hasebe et al. 2004)(Itoigawa et al. 2005). Lastly, as shown in Figure

2-5b, vertical heat flow can also be achieved by vertical assembly of a stack of thin foil segments, with each segment consisting of several planar thin-film BiTe-based thermocouples (Stark and Stordeur 1999).

Advancements in fabrication technology eventually enabled vertical fabrication of thermocouples, leading to the vertical/vertical μTEG type. Initial implementations of this type used two substrates; one substrate is used to form the n-type Bi_2Te_3 thermoelements while another substrate is used to form the p-type $(Bi,Sb)_2Te_3$ thermoelements. These two substrates, as shown in Figure 2-6, are then assembled and joined together to form a TEG (Kishi et al. 1999)(Bottner et al. 2004). More recent implementations of vertical/vertical μTEGs use subsequent electrochemical deposition of thermoelectric materials in a silicon mold (Li et al. 2003), polymer mold (Lim et al. 2002)(Snyder et al. 2003)(Glatz et al. 2006)(Glatz et al. 2009), or alumina nanotemplate (Lim et al. 2005). Other implementations utilize standard micromachining steps to fabricate vertically-oriented thermoelements (Sato et al. 2005)(Wang et al. 2009) while others explore methods such as PCB-like processing (Lindeberg et al. 2008) and dispenser printing (Chen et al. 2009). The thermoelectric materials used for these implemented vertical/vertical μTEGs are Cu and Ni (Glatz et al. 2006), Sb and Ni (Lindeberg et al. 2008), Si and Au (Sato et al. 2005), and n-type and p-type compounds based on Bi, Sb, and Te (Kishi et al. 1999)(Lim et al. 2002)(Li et al. 2003)(Snyder et al. 2003)(Lim et al. 2005)(Chen et al. 2009)(Glatz et al. 2009)(Wang et al. 2009)(Kraemer et al. 2011).

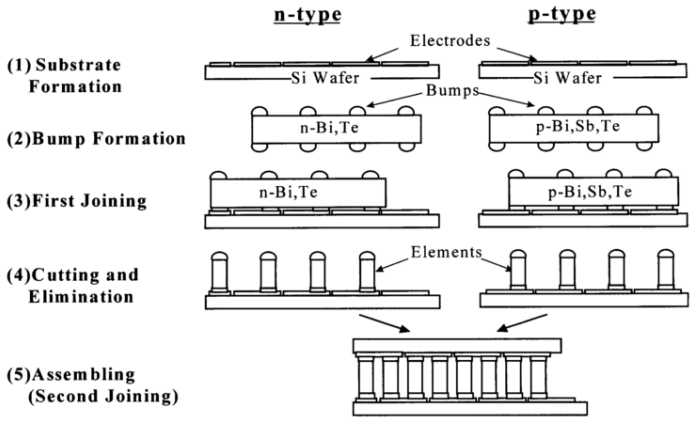


Figure 2-6: Fabrication process of vertical/vertical μTEG formed using two substrates. (Kishi et al. 1999)

The lateral/lateral type is chosen for implementation in this work as it is the simplest to fabricate and has the most potential for integration with on-chip electronics due to its planar structure (Carmo, Goncalves, and Correia 2010). A review of published implementations of the lateral/lateral type is further presented in the next section.

2.3 Lateral/lateral TEG Implementations

In this section, previous implementations of lateral/lateral μTEGs are presented based on the type of thermoelectric materials used. A brief description of the fabrication process for each TEG implementation is given, as well as its dimensions and performance characteristics when available. Towards the end of the section, all discussed TEGs are compared and analyzed to provide a good perspective on the scope and limitations of each implementation.

2.3.1 Metal-based TEGs

Metal-based TEGs are defined in this work as devices where both thermoelectric materials used are metals or metal alloys. Although the Seebeck coefficient of metals is low and the thermal conductivity is high compared to semiconductors, researchers still implement metal-based TEGs due to the availability of materials, as well as ease of fabrication.

To achieve device flexibility, (Qu, Plotner, and Fischer 2001) designed and fabricated a flexible thermoelectric generator consisting of Sb-Bi thermocouples embedded on a 50 μm thick epoxy film. A 50 μm thick copper sheet was used as the substrate in which antimony and bismuth were electrodeposited to form the thermocouples. Bismuth was also deposited onto the Sb strip ends to form the required electrical contacts between the two materials. Then, an epoxy film was spin-coated onto the substrate and hardened under UV radiation to serve as mechanical support for the thermocouples. Lastly, the copper sheet was etched away using 20% ammoniumperoxodisulfate. Each thermoleg has a length of 20 mm, width of 40 μm, and thickness of 10 μm. The fabricated μTEG, with 100 thermocouples, has a Seebeck coefficient of 8.4 mV/K.

Another μTEG implementation using Bi and Sb thermocouples was realized by (Savelli et al. 2006). The thermocouples were deposited on a glass substrate by sputtering and were electrically connected by Ti and Au metallic junctions, also deposited by sputtering. This work explores varying the width of the thermolegs from 20 μm to 40 μm with a constant chip area of 1cm×1cm. The device with 20 μm wide thermolegs generated the highest Seebeck voltage of 535 mV while the device with 40 μm wide thermolegs delivered the highest output power of 1.2 μW, both for ΔT=100K.

Using commercially available alloys exhibiting the highest thermoelectric power at the time, (Chen et al. 2004) made a μTEG using chromel ($Ni_{90}Cr_{10}$) and constantan ($Cu_{55}Ni_{45}$) as the thermoelectric materials. Blanket coatings of these two alloys were deposited on an alumina substrate by thermal spraying. The spray coatings were then patterned by ultrafast laser micromachining. Isolation between the two materials was provided by a 100 μm thick alumina layer sandwiched between the NiCr and CuNi layers. The length of each thermoelement was 34 mm and the widths were varied from 230 μm to 1085 μm. The Seebeck coefficient of each junction was measured to be 54 μV/K and the fabricated devices delivered 140 μW – 250 μW of power for a temperature difference of 280 K.

Similarly, (Markowski, Dziedzic, and Prociow 2005) also used metal alloys as thermoelectric materials. The thermoelement materials used in this work were PdAg and a special Ta-Sb-Ge (TSG) alloy. A circular alumina substrate was used, giving rise to a design with thermoelements arranged in a radial manner. The 250 μm wide PdAg tracks were screen-printed through a 325-mesh stainless screen mask while the TSG tracks were deposited by magnetron sputtering. The fabricated device generated an output voltage of about 600 mV for a temperature difference of 100 K.

To establish a large and uniform temperature difference across the thermolegs, (Boniche et al. 2009) also designed a μTEG with radially-oriented thermocouples. The proposed design was intended to generate power for sensors and other electronic devices using hot gases flowing at the central channel of the device as the heat source. The design was optimized for several semiconductor thin films but for ease of fabrication, the actual

device was fabricated using sputter-deposited Au and Ni thermoelements (Boniche 2010). Several prototypes with different thermoelement widths for a chip area of 132.7 mm^2 were fabricated, leading to variations in the number of thermocouples for each prototype. The best-performing device consisted of 65 thermocouples and has a Seebeck coefficient of 14.3 μV/K, maximum temperature difference of 74 ˚C, and a maximum output power of 0.47 μW.

2.3.2 Silicon-based TEGs

Silicon-based TEGs are devices where at least one thermoelectric material is bulk silicon. Silicon has the advantage of a higher Seebeck coefficient than metals but for a simpler fabrication process, some researchers use aluminum as the second thermoelement.

The earliest implementation of a lateral/lateral μTEG found in literature was designed by (Nieveld 1982) and consisted of 152 pairs of p-type silicon and Al thermocouples fabricated on an n-type silicon substrate. Each thermoelement has a length of 1.5 mm, width of 10 μm, and thickness of 6.5 μm. The fabricated device, which has a total internal resistance of 250 kΩ, produced an output voltage of 76 mV per degree increase in temperature. To increase the generated output voltage of the device, the researchers recommend the use of both n-type and p-type silicon as thermoelement materials.

The next lateral/lateral μTEG implementation, designed by (Rowe et al. 1989), has both n-type and p-type silicon thermocouples. Aside from this, a silicon-on-sapphire wafer was also used to effectively isolate the thermocouples from the substrate. The silicon device layer was alternately doped with boron and phosphorus via ion implantation at a concentration greater than $1x10^{18}$ cm^{-3} to produce n-type and p-type silicon strips. Undoped silicon areas were then removed with reactive ion etching (RIE). Lastly, 0.1 μm thick aluminum was deposited to provide electrical connectivity between thermolegs. Each thermoleg has a length of 4.5 mm, width of 100 μm, and thickness of 0.4 μm. The fabricated μTEG has a Seebeck coefficient of 530 μV/K and delivered approximately 2 nW to a matched load at a temperature difference of 10 K.

Half a decade later, another lateral/lateral μTEG was implemented by (Glosch et al. 1999), utilizing n-type silicon and aluminum as the thermoelectric materials. The areas of the silicon wafer where the thermoelements were situated were thinned to a thickness of 10 μm to optimize heat flow. The n-type silicon thermolegs were doped to achieve a resistivity of 1.4×10^{-5} Ωm. The aluminum thermolegs were deposited by evaporation. Each thermoleg has a length of 500 μm, width of 7 μm, and thickness of 1.2 μm. The chip was then mounted on docking elements made of aluminum, which serve as the hot and cold junctions of the device. The fabricated μTEG has a Seebeck coefficient of 240 μV/K with 20 thermocouples and delivered approximately 1.5 μW to a 750 kΩ load at a temperature difference of 10 K.

A general purpose thermal sensor was developed by (Randjelović et al. 2008) based on thermopiles composed of p-type diffusion-doped silicon and sputtered Al on an n-type silicon substrate. The thermocouples were electrically isolated by sputtered SiO_2 layer placed between the two thermoelectric materials. It was also observed in this work that complete removal of the residual n-type silicon under the thermocouples has the highest influence on sensor performance. Evaluating the device with the thinnest (3μm) membrane as a thermal converter, an output voltage of 38 mV was measured for an input power of 40 mW.

2.3.3 Polysilicon-based TEGs

Polysilicon-based TEGs are defined in this work as devices where at least one thermoelectric material is polycrystalline silicon. Most implementations of lateral/lateral TEGs found in literature are polysilicon-based, which can be attributed to the well-established process of depositing polysilicon in the semiconductor industry. Aside from this, polysilicon has fairly good thermoelectric properties. For ease of fabrication, some implementations also use a metal (Al or Ni) as the second thermoelement, similar to silicon-based TEGs.

Improving on the work by (Rowe et al. 1989), (Kiely, Morgan, and Rowe 1994) explored the use of a polysilicon-on-quartz substrate to improve the thermal conversion efficiency

of a μTEG fabricated on a silicon-on-sapphire substrate. The change to quartz wafers from sapphire ones was mainly motivated by the ten-fold increase in thermal resistivity and lesser cost. Although doped single crystal silicon can have higher Seebeck coefficients than polysilicon, the latter was used for ease of fabrication. The polysilicon layer was alternately doped with boron and phosphorus via ion implantation to define the thermoelement materials. Undoped silicon areas were removed by RIE and Al is deposited for electrical contacts between thermolegs. Each thermoleg has a length of 0.45 mm, width of 100 μm, and thickness of 0.4 μm. The fabricated μTEG has a Seebeck coefficient of 490 μV/K and delivered approximately 2 nW at a temperature difference of 10 K. Note that the length of the thermoelements was ten times shorter for the polysilicon-on-quartz μTEG compared to the silicon-on-sapphire μTEG. For μTEGs with the same thermoelement dimensions, the conversion efficiency of the μTEG fabricated on a polysilicon-on-quartz substrate was 50 times higher.

With compatible standard semiconductor fabrication technologies in mind, (Jacquot et al. 2002) designed an in-plane thermoelectric μTEG. A <100>-oriented silicon wafer was deposited with silicon nitride and silicon dioxide by low pressure chemical vapor deposition (LPCVD). Then, a polysilicon layer was deposited and patterned for alternate n- and p-doping to form the thermocouples. The electrical interconnections were subsequently made by depositing a layer of Cr/Au/Cr and patterning by lift-off. KOH etching was then used to release the membrane. Unfortunately, results presented in the paper were all from numerical simulations and do not include actual results of the fabricated TEG. The authors, however, claim that their device can produce as much as 60 μW with an output voltage of 1.5 V.

In (Huesgen, Woias, and Kockmann 2008), a TEG composed of 3 modules to optimize the heat flow path was designed and fabricated. An illustration of the TEG is shown in Figure 2-7. *Module A* consisted of the n-type polysilicon and Al thermopiles. Fabrication of *Module A* starts with deposition of a 300 nm thick thermal SiO_2 and 300 nm thick LPCVD Si_3N_4 on a 300 μm thick, 4 inch silicon wafer. Next, n-doped polysilicon was deposited and structured by dry etching. A 250 nm thick aluminum layer was then

sputtered and wet etched. The n-type poly-Si thermoleg has a length of 120 µm, width of 40 µm, and thickness of 0.7 µm while the Al thermoleg has a length of 120 µm, width of 5 µm, and thickness of 0.25 µm. A barrier layer of 1.2 µm thick SiO_2 was then deposited to insulate the thermopiles from the thermal contact structure fabricated in *Module B*. The thermal connectors on top of the thermoelectric structure that conduct heat from the top surface to the hot thermocouple junctions are described by *Module B*. In *Module C*, a backside deep reactive ion etching (DRIE) process through the substrate was performed such that the hot junction becomes thermally insulated from the bottom, cold side of the generator. A second wafer was then bonded to the backside for good thermal contact and to avoid cavity contamination. The fabricated µTEG, with 125 thermocouples, has a Seebeck coefficient of 9.5 mV/K and an internal resistance of 84 kΩ.

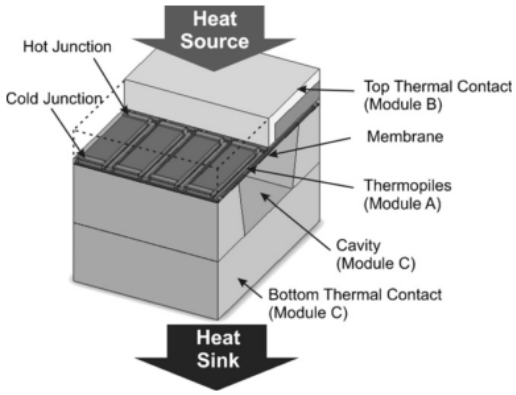


Figure 2-7: Illustration of TEG consisting of three modules to optimize the heat flow path. (Huesgen, Woias, and Kockmann 2008)

Taking advantage of an available CMOS foundry, (Tseng et al. 2008) designed a CMOS-integrated thermal sensor with 30 pairs of n^+/p^+ polysilicon thermopiles using a standard 0.18 µm CMOS process. To fabricate suspended thermopiles, a post-CMOS process of anisotropic oxide etch was performed to remove oxide between meandering thermopile structures, followed by an isotropic Si dry etch to remove silicon under the polysilicon thermopiles and reduce thermal conduction through the substrate. The output voltage of the device controls the bias current of a high-frequency oscillator circuit, causing a shift in the output frequency. The researchers were able to successfully demonstrate that the

thermopiles generate enough voltage to cause a shift on the output frequency of the oscillator.

(Hong, Chou, and Tsai 2009) designed a thermoelectric generator using the MetalMUMPS process as their platform. Nickel and n-type polysilicon were utilized for the thermolegs. For the electrical connections, 10 nm Cr and 25 nm Pt were used. The n-type poly-Si thermoleg has a length of 600 μm, width of 100 μm, and thickness of 0.7 μm while the Ni thermoleg has a length of 600 μm, width of 100 μm, and thickness of 2 μm. The fabricated μTEG, consisting of 40 thermocouples, produced 3.6 mV for a heating power of 1 W.

In (Yang et al. 2009), a TEG was designed and fabricated in a commercial 2-poly 4-metal 0.35 μm CMOS process. The TEG consisted of n-type and p-type polysilicon strips for the thermocouples and Al for the electrical connections. Vertical SiO_2 etching was then performed post-CMOS with the top aluminum layer as the etching mask forming slits surrounding the thermolegs. Similarly, isotropic Si etching was also done post-CMOS to create a 10 μm deep thermal isolation cavity beneath the thermolegs. Several TEGs with different dimensions were fabricated with the best-performing TEG having a length of 60μm and width of 4 μm. The said μTEG has a power factor of 0.0417 $\mu W/cm^2K^2$ and voltage factor of 2.417 V/cm^2K.

A commercial 0.35 μm CMOS process was also used in (Kao et al. 2010) to fabricate their TEG design. The TEG also consisted of n-type and p-type polysilicon thermocouples and Al interconnects. The hot side of the device is connected to an Al plate to improve its heat-receiving capability. Anisotropic dry etching was performed post-CMOS to remove the oxide sacrificial layer. Isotropic dry etching was also done post-CMOS to etch the silicon substrate under the thermocouples. Each thermoleg has a length of 640 μm, width of 5 μm, and thickness of 0.3 μm. The fabricated μTEG, with 24 thermocouples, has a Seebeck coefficient of 67 μV/K and delivered approximately 0.46 pW to a 2.45 kΩ load at a temperature difference of 1 K.

Lastly, (Xie et al. 2010) proposed a method of improving the heat flux path by embedding the thermolegs between top and bottom vacuum cavities as shown in Figure 2-8. An analytical model using finite element method for this device is presented in (Xie & Lee 2008). Fabrication of the TEG starts with deposition of 0.7 μm thick polysilicon on a silicon wafer. The poly-Si layer was then partially implanted with phosphorus to form the n-type thermolegs, followed by boron implantation to generate the p-type thermolegs. Aluminum was then deposited and etched to form the electrical connections. Next, bottom cavities were formed using a micromachining step consisting of SiO_2 hard mask patterning, Si DRIE, and isotropic Si etching. The bottom cavities were then sealed by a low-stress undoped silicate glass (USG) layer deposited by PECVD. Finally, top vacuum cavities were created by patterning a deposited USG sacrificial layer, opening of etch holes, removal of USG layer, and sealing the cavities. Each thermoleg has a length of 16 μm, width of 5 μm, and thickness of 0.7 μm. The fabricated μTEG has an open-circuit voltage of 480 mV at a temperature difference of 30 K for a 1 × 1 cm^2 device.

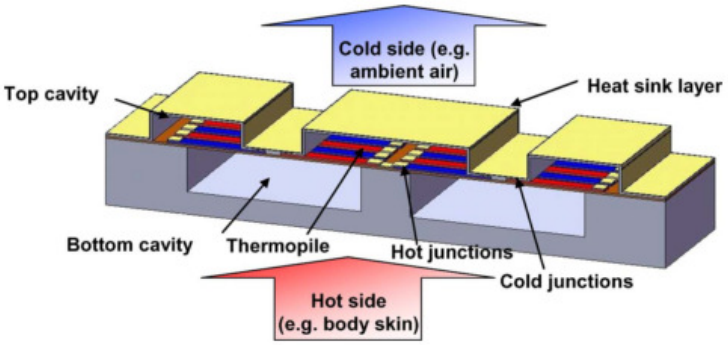


Figure 2-8: Diagram of TEG with top and bottom vacuum cavities to optimize heat flux path. (Xie et al., 2010)

2.3.4 Bismuth Telluride-based TEGs

Some researchers explored the use of compounds based on bismuth telluride (BiTe), as well as some related ternary alloys, due to its good thermoelectric figure of merit at room temperature. Commonly applied ternary alloys consist of bismuth telluride with either bismuth selenide (BiSe) or antimony telluride (SbTe). This group of TEG implementations as is referred in this work as BiTe-based TEGs.

(Takashiri et al. 2007) fabricated a lateral/lateral μTEG with thermocouples made out of p-type $Bi_{0.4}Te_3Sb_{1.6}$ and n-type $Bi_2Te_{2.7}Se_{0.3}$ deposited by a flash evaporation method. A glass substrate was used and 1 μm thick Bi_2Te_3-based films were deposited and patterned using shadow masks. The thermolegs were connected electrically by 2 μm thick Al deposited by sputtering. Each thermoleg has a length of 15 mm, width of 1 mm, and thickness of 1 μm. Each thermocouple has a Seebeck coefficient of 433.7 μV/K and the device delivered 0.21 μW of power at a temperature difference of 30 K.

In (Goncalves et al. 2008), co-evaporation was applied in the fabrication of p-type Sb_2Te_3 and n-type Bi_2Te_3 thin films, which were used as the thermoelectric materials in their TEG. First, 1 μm thick p-type Sb_2Te_3 was deposited on a kapton substrate by thermal co-evaporation followed by a 100 nm layer of Ni to avoid diffusion of the thermoelectric material into the succeeding deposited layers. This layer was then patterned and wet etched to form the first set of thermoelements. Similarly, 1 μm thick n-type Bi_2Te_3 followed by a 100 nm Ni layer were also deposited, patterned, and wet etched to complete the thermocouples. Lastly, contacts made up of 100 nm Ni and 100 μm Al were deposited and patterned. Several μTEGs were fabricated with Seebeck coefficients ranging from 150-250 μV/K for each thermoelectric junction. The target application for this work was as a power supply in EEG modules (Carmo, Goncalves, and Correia 2010).

(Ghafouri et al. 2008) also used Sb_2Te_3 and Bi_2Te_3 thermocouples fabricated on a SU-8 polymer substrate, which gives the device added flexibility as this μTEG scavenges power from the change in body temperature of a beetle during flight. To fabricate, a 20 nm Ti sacrificial layer was first deposited on a Si support wafer. Then, a 5 μm thick layer of SU-8 photoresist was spun and patterned to define areas for metal contact pads, lines, heat pipes, and resistor temperature sensors, which were formed from a Cr/Au layer deposited on top of the polymer. Subsequently, a 50 μm thick SU-8 mold was spun and patterned to define cavities under the thermoelements and through-holes that were aligned to the underlying pads. Next, the holes were filled with conductive epoxy to provide electrical connections between the thermocouples and the contact pads. A 200 μm thick layer of the thermoelectric material was then attached to the polymer substrate

and dicing was performed to remove excess thermoelectric material. Once the thermoelectric material was patterned, the polymer substrate is released from the supporting Si wafer by dissolving the sacrificial Ti layer. The fabricated device, consisting of 10 thermocouples, delivered 10 μW/cm^2 at a temperature difference of 11 K.

Bismuth telluride films were also used as thermoelectric materials in (Kurosaki et al. 2009). Silicon nitride was first deposited onto a silicon wafer by plasma-enhanced chemical vapor deposition (PECVD). Then, patterning of the configurations of the shadow masks appropriate for the thermolegs followed. Both p- and n-type BiTe-based films were subsequently deposited by flash evaporation method using shadow masks to evaporate the materials with their patterns. Copper was used for the electrical connections between the thermoelements. Each thermoleg has a length of 1200 μm, width of 200 μm, and thickness of 1 μm. The fabricated μTEG, with 16 thermocouples, has a Seebeck coefficient of 3.7 mV/K and delivered approximately 16 nW to a 72 kΩ load at a temperature difference of 13 K.

Metal organic chemical vapor deposition (MOCVD) was utilized by (Kwon et al. 2009) in depositing 4 μm thick p-type $Bi_{0.4}Sb_{1.6}Te_3$ and n-type Bi_2Te_3 on a GaAs substrate. The thermoelements were connected electrically by 0.5 μm thick thermally-evaporated Al. The fabricated μTEG consisted of 20 thermocouples and each thermoelement has a length of 12 mm and width of 200 μm. Each thermocouple has a Seebeck coefficient of 315 μV/K and the device delivered 1.3 μW at a temperature difference of 45 K.

2.3.5 Other semiconductor-based TEGs

This section discusses other TEG implementations using semiconductors that are not covered by the previous four classifications as thermoelectric materials. These include silicon germanium (SiGe) and gallium nitride (GaN).

Targeting the use of burning hydrocarbons or other hydrogen-containing fuels as heat source, (Schaevitz et al. 2001) designed and fabricated a combustion-based thermoelectric generator consisting of n- and p-type poly-SiGe thermoelements on a thermally-insulating

silicon nitride membrane. To begin, a silicon wafer was coated with low-stress silicon nitride and a potassium hydroxide (KOH) etch mask is patterned at the backside. Then, two layers of silicon germanium were deposited and patterned sequentially to form the thermoelements. Metallization was realized with a TiN barrier layer and an e-beam deposited Ti/Pt layer. Then, the channels were etched from the back using KOH. Lastly, the combustion catalyst was e-beam deposited with the use of a specially microfabricated, self-aligned shadowmask. In this work, the device generated an output voltage up to 7 V, with thermal efficiencies up to 0.02 %.

MOCVD was used to grow 3.5 μm thick GaN on a sapphire substrate in (Sztein et al. 2009). Silicon was then doped into the material to make it n-type. The GaN mesas were formed via conventional lithography methods and then dry-etched using an inductively coupled plasma etcher. Due to the extremely high resistivity of p-type GaN, Au was used as the second thermoelement. Each thermoleg has a length of 1 mm, width of 100 μm, and thickness of 3.5 μm. The fabricated TEG, consisting of 25 thermocouples, has an output voltage of 300 mV and matched load power of 2.1 μW at a temperature difference of 30 K. Although GaN has high thermal conductivity, InGaN thin films prepared via MOCVD have shown significantly lower thermal conductivity without degrading the Seebeck coefficient and electrical conductivity significantly (Pantha et al. 2009).

2.3.6 Summary and Analysis of Published Lateral/lateral TEGs

Table 2-1 chronologically summarizes the geometry, fabrication process, and performance parameters of published TEG implementations previously discussed. In cases where data are not explicitly provided, calculations are made to determine the values of certain parameters based on given data. For the computation of the efficiency factor, when the actual chip area is not explicitly stated in the text, an optimistic estimate is made based only on the dimensions of the thermoelements and the gap between thermoelements when available. This is true in the case of (Glosch et al. 1999), (Savelli et al. 2006), (Sztein et al. 2009), and (Kwon et al. 2009). As such, the efficiency factors listed in Table 2-1 for these implementations is higher than the actual efficiency factor of the

device as the chip area is definitely larger than the optimistic estimate that was used in the computation.

Majority of the implementations use silicon wafers as this makes it easier to integrate the TEG as on-chip power supply. The geometry of the thermocouples greatly varies with each implementation; the length ranging from 16 μm to 34 mm, the width ranging from 4 μm to 1085 μm, and the thickness ranging from 0.18 μm to 200 μm. For a larger temperature difference across the thermocouples, it is desirable to have longer lengths, narrower widths, and smaller thicknesses. However, the achievable geometry of the thermocouples is also dependent on the fabrication process and on the topology of the TEG. For example, topologies with a suspended membrane as in (Glosch et al. 1999), (Schaevitz et al. 2001), (Jacquot et al. 2002), (Ghafouri et al. 2008), (Huesgen, Woias, and Kockmann 2008), (Randjelović et al. 2008), (Tseng et al. 2008), (Boniche et al. 2009), (Hong, Chou, and Tsai 2009), (Kurosaki et al. 2009), (Yang et al. 2009), (Kao et al. 2010), and (Xie, Lee, and Feng 2010), have lengths less than 2 mm since a longer length would make the membrane structurally unstable. As previously mentioned, most of the TEGs in Table 2-1 use polysilicon in at least one of the thermoelectric materials because of the straightforward process of depositing polysilicon, which is available in standard CMOS technology processes. It is, however, important to note that those that use other thermoelectric materials generally have higher Seebeck coefficients. The TEG by (Rowe et al. 1989) using n-type and p-type silicon as its thermoelectric materials have a Seebeck coefficient of 530 μV/K – almost twice as much as the Seebeck coefficient of the TEG in (Xie, Lee, and Feng 2010), which has the highest Seebeck coefficient in all of the polysilicon-based TEGs. For the electrical connections between thermoelements, most of the implementations use aluminum as this is the most commonly used metal for this purpose. To simplify the fabrication process, (Nieveld 1982), (Glosch et al. 1999), (Randjelović et al. 2008), and (Huesgen, Woias, and Kockmann 2008) even used aluminum as the second thermoelement in their TEG. With regards to the fabrication process, the ones that use either silicon or polysilicon as thermoelements have relatively simpler processes.

Table 2-1: Comparison of published lateral/lateral μTEGs.

Authors Year	Substrate/ Process	TE length (μm)	TE cross sec. area (μm²)	Integration (TCs/cm²)	TC material	Seebeck coeff. (μV/K)	Interconnect material and thickness	Deposition method	TC patterning	Efficiency factor (μW/K²cm²)
Nieveld 1982	bulk n-Si	1500	10 x 6.5	2666.7	p-Si / Al	500	Al	Doping and evaporation	---	0.0023
Rowe et.al. 1989	Silicon on sapphire	4500	100 x 0.4	55.6	p-Si / n-Si	530	Al, 0.1μm	Ion implanting	RIE	0.0011
Kiely et.al. 1994	Polysilicon on quartz	450	100 x 0.4	555.6	p-polySi / n-polySi	490	Al, 0.1μm	Ion implanting	RIE	0.011
Glosch et.al. 1999	bulk Si	500	7 x 1.2	6060.6	Al / n-Si	240	Al, 1.2μm	Evaporation and doping	---	0.091
Qu et.al. 2001	Copper	20000	40 x 10	31.25	Sb / Bi	90	Sb/Bi	Electro-deposition	Lithography	5.167×10^{-4}
Schaevitz et.al. 2001	Si wafer with nitride membrane	---	---	---	p-polySiGe / n-polySiGe	---	Ti/Pt	UHV-CVD	Wet etching	---
Jacquot et.al. 2002	bulk Si	---	---	---	p-polySi / n-polySi	---	Cr/Au/Cr	LPCVD	Wet etching	---
Chen et.al. 2004	Alumina	34000	1085 x 25	1.17	Chromel / Constantan	54	Chromel / Constantan	Thermal spraying	Laser micro-machining	4.49×10^{-7}

Table 2-1: Comparison of published lateral/lateral μTEGs. (*continued*)

Author Year	Substrate Process	TE length (μm)	TE cross sec. area (μm²)	Integration (TCs/cm²)	TC material	Seebeck coeff. (μV/K)	Interconnect material and thickness	Deposition method	TC patterning	Efficiency factor (μW/K²cm²)
Markowski et.al. 2005	Alumina	---	---	---	PdAg / Ta-Sb-Ge alloy	250	---	Magnetron sputtering	lithography	2.37×10^{-5}
Savelli et.al. 2006	Glass	---	---	---	Sb / Bi	42.8	Ti/Au	Sputtering	Etching	1.2×10^{-4}
Takashiri et.al. 2007	Glass	15000	1000 x 1	2.08	p-$Bi_{0.4}Te_3Sb_{1.6}$ / n- $Bi_2Te_{2.7}Se_{0.3}$	433.7	Al, 2μm	Flash evaporation	Etching	4.42×10^{-5}
Randjelovic et.al. 2008	bulk Si	---	---	---	p-Si / Al	---	Al	Doping and sputtering	---	---
Huesgen et.al. 2008	bulk Si	120	5 x 0.25 / 40 x 0.7	9259.3	Al / n-polySi	76.08	Al, 0.25μm	LPCVD / sputtering	Wet and dry etching	0.01612
Tseng et.al. 2008	0.18μm CMOS	---	---	---	p-polySi / n-polySi	---	Al	LPCVD	Dry etching	---
Goncalves et.al. 2008	Kapton	---	---	---	p-Sb_2Te_3 / n-Bi_2Te_3	150-250	Ni/Al, 100nm/1μm	Thermal co-evaporation	Wet etching	---
Ghafouri et.al. 2008	Polymer (SU-8)	2000	350 x 200	15.625	p-Sb_2Te_3 / n-Bi_2Te_3	---	Cr/Au	Physical attachment	Dicing	0.0207

Table 2-1: Comparison of published lateral/lateral μTEGs. (*continued*)

Author Year	Substrate/ Process	TE length (μm)	TE cross sec. area (μm²)	Integration (TCs/cm²)	TC material	Seebeck coeff. (μV/K)	Interconnect material and thickness	Deposition method	TC patterning	Efficiency factor (μW/K²cm²)
Kurosaki et.al. 2009	bulk Si	1200	200 x 1	104.2	p-$Bi_{0.4}Te_3Sb_{1.6}$ / n-$Bi_2Te_{2.7}Se_{0.3}$	433.7	Cu	Flash evap.	RIE	5.92 x 10^{-4}
Sztein et.al. 2009	sapphire	1000	100 x 3.5	250	Au / n-GaN	350	Ti/Al/Ni/Au, 20/120/30/50nm	MOCVD / e-beam dep.	Dry etching	0.0233
Kwon et.al. 2009	GaAs	12000	200 x 4	16.67	p-$Bi_{0.4}Te_3Sb_{1.6}$ / n-Bi_2Te_3	315	Al, 0.5μm	MOCVD	Wet etching	0.00107
Boniche et.al. 2009	Si with polyimide/oxide membrane	2000	50 x 0.5 / 40 x 0.4	48.98	Au / Ni	14.3	Au/Ni, 0.4μm	Sputtering	Lift-off	8.03 x 10^{-5}
Hong et.al. 2009	MetalMUMPS	600	100 x 2 / 100 x 0.7	416.7	Ni / n-polySi	100.5	Cr/Pt, 10nm/25nm	Electroplating / deposition	RIE	---
Yang et.al. 2009	0.35μm CMOS	60	4 x 0.275 / 4 x 0.18	104166.7	p-polySi / n-polySi	160	Al	LPCVD	Dry etching	0.0417
Kao et.al. 2010	0.35μm CMOS	640	5 x 0.3	7812.5	p-polySi / n-polySi	67	Al, 0.6μm	LPCVD	Dry etching	0.0064
Xie et.al. 2010	bulk Si	16	5 x 0.7	312500	p-polySi / n-polySi	279	Al	LPCVD	Dry etching	0.052

It can also be observed from Table 2-1 that bismuth telluride and antimony telluride-based compounds are commonly used as thermoelectric materials as well. This is primarily because these compounds have the highest thermoelectric figure-of-merit in the room temperature range (Rowe 1995)(Venkatasubramanian et al. 2001). However, looking at Figure 2-9 where a comparison of the efficiency factor of the published lateral/lateral μTEGs discussed is shown, bismuth telluride-based μTEGs relatively have low level of integration compared to silicon- and polysilicon-based devices. In addition, only (Ghafouri et al. 2008) has a comparable efficiency factor to those implemented with polysilicon thermocouples. In fact, most implementations of bismuth telluride-based μTEGs that have high efficiency factor at a high level of integration are of the vertical/vertical type (Glatz et al. 2009). Another observation that can be made from Figure 2-9 is that metal-based thermoelectric generators, due to their low Seebeck coefficient and high thermal conductivity, have poor performance compared to other implementations. It is also worthwhile to note that the μTEG in (Glosch et al. 1999) has the highest efficiency factor among all the lateral/lateral μTEG implementations.

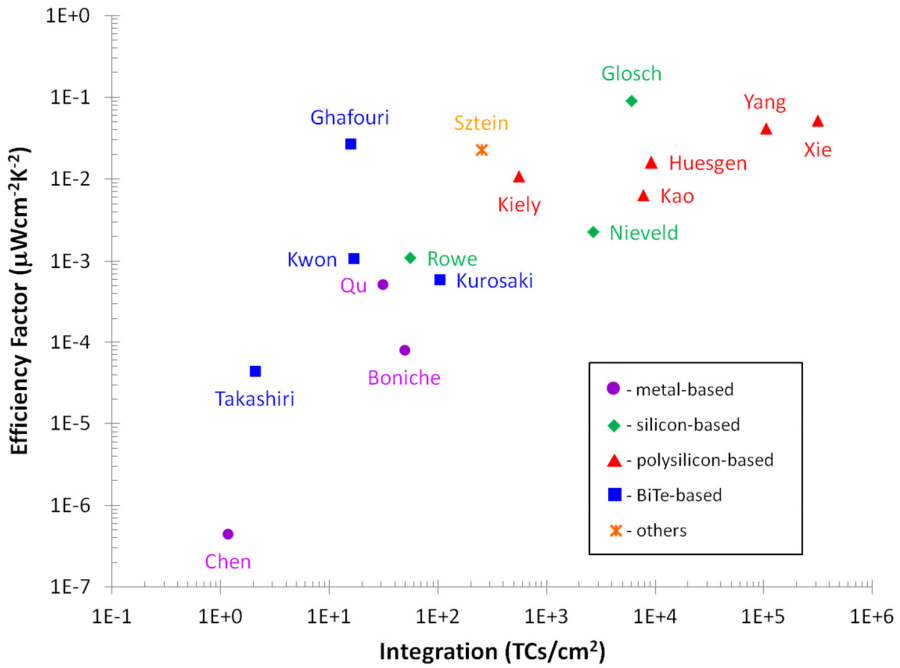


Figure 2-9: Comparison of efficiency factor vs. level of integration of published lateral/lateral μTEGs grouped according to thermoelectric material used.

Although not fabricated, it is also relevant to look into the lateral/lateral TEG design in (Egbert, Harvey, and Otis 2007) where a silicon-on-insulator (SOI) wafer was used. As shown in Figure 2-10, the SOI wafer's device layer was utilized for the suspended membrane and thermoelements. The membrane acts as the heat absorber of the TEG while the substrate acts as the heat sink. This design is the basis of the TEG design in this work, which is discussed in more detail in Chapters 4 and 5.

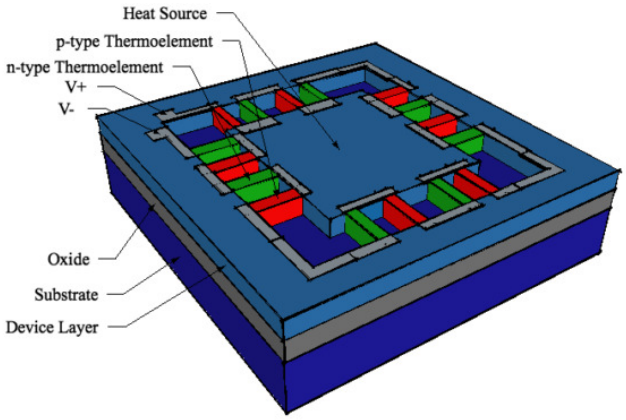


Figure 2-10: A lateral/lateral TEG using a SOI wafer. (Egbert, Harvey, and Otis 2007)

2.4 Summary

A review of published works on thermoelectric generators, specifically lateral/lateral TEGs, has been presented in this chapter. After reviewing all published implementations of lateral/lateral thermoelectric generators, it is shown that silicon-based and polysilicon-based TEGs give the best efficiency factors at high levels of integration for this type of TEGs. Although bismuth telluride-based TEGs have higher Seebeck coefficients, they have relatively low levels of integration when implemented as lateral/lateral TEGs. In fact, bismuth telluride-based TEGs are more appropriate for vertical/vertical TEG implementation where they have high efficiency factors at high levels of integration (Glatz et al. 2009).

For the TEGs to be implemented in this work, a design using a SOI wafer similar to the one described in (Egbert, Harvey, and Otis 2007) is considered. The device layer of the

SOI wafer is to be used as one of the thermoelements and for simplicity in fabrication, aluminum is to be used as the second thermoelement.

Chapter 3: Solar Thermoelectric Generators

This chapter presents a review of published works on solar thermoelectric generators (STEGs). It starts with an overview of the concept of solar-powered thermoelectric generators. Then, several implemented STEGs are discussed. To facilitate discussion on the various implementations of published STEGs, they are classified into three types: (1) STEGs with thermal collectors, (2) STEGs with solar concentrators, and (3) STEGs employing both solar and thermal concentration. Lastly, thermal-photovoltaic hybrid systems are also discussed to demonstrate the possibility of further enhancement in efficiency by utilizing both photovoltaic and thermoelectric technologies.

3.1 STEG Concept

The concept of using solar concentrators to focus light onto a thermoelectric device is not new. Solar radiation covers vast areas and when concentrated, can have especially high heat flux. As such, direct solar thermal power generation is an attractive electricity generation technology since it can achieve a flexible power generation scheme that is environment-friendly, has high efficiency, and has high reliability characteristics (Deng & Liu 2009). STEGs are also scalable, making it suitable for both small- and large-scale applications (Baranowski, Snyder, and Toberer 2012). Moreover, photovoltaics are limited to the fraction of incident solar radiation above the bandgap while STEGs utilize a larger portion of the solar spectrum. This characteristic also makes it attractive to utilize STEGs along with photovoltaics (PVs) as a more efficient way of harvesting solar energy.

One way of implementing solar-powered TEGs is by using a thermoelectric generator and a thermal collector (Riffat and Ma 2003). As shown in Figure 3-1a, heat from the sun is absorbed by the thermal collector and conducted over to the thermoelectric generator. This generates a temperature difference across the thermoelements, which results in an output voltage. Another way to realize STEGs is by using a thermoelectric generator and

a solar concentrator as shown in Figure 3-1b. In this case, the solar concentrator focuses solar heat onto the TEG, which increases the amount of input heat flux to the TEG. To further enhance the efficiency of STEGs, a solar concentrator can be placed before the thermal collector in Figure 3-1a to focus solar heat onto the thermal collector. This is shown in in Figure 3-1c. In this case, the total efficiency of the system, η_{tot}, becomes dependent on the solar concentrator efficiency, η_s; thermal collector efficiency, η_{th}; and TEG efficiency, η_{TEG}.

$$\eta_{tot} = \eta_s \cdot \eta_{th} \cdot \eta_{TEG} \tag{3-1}$$

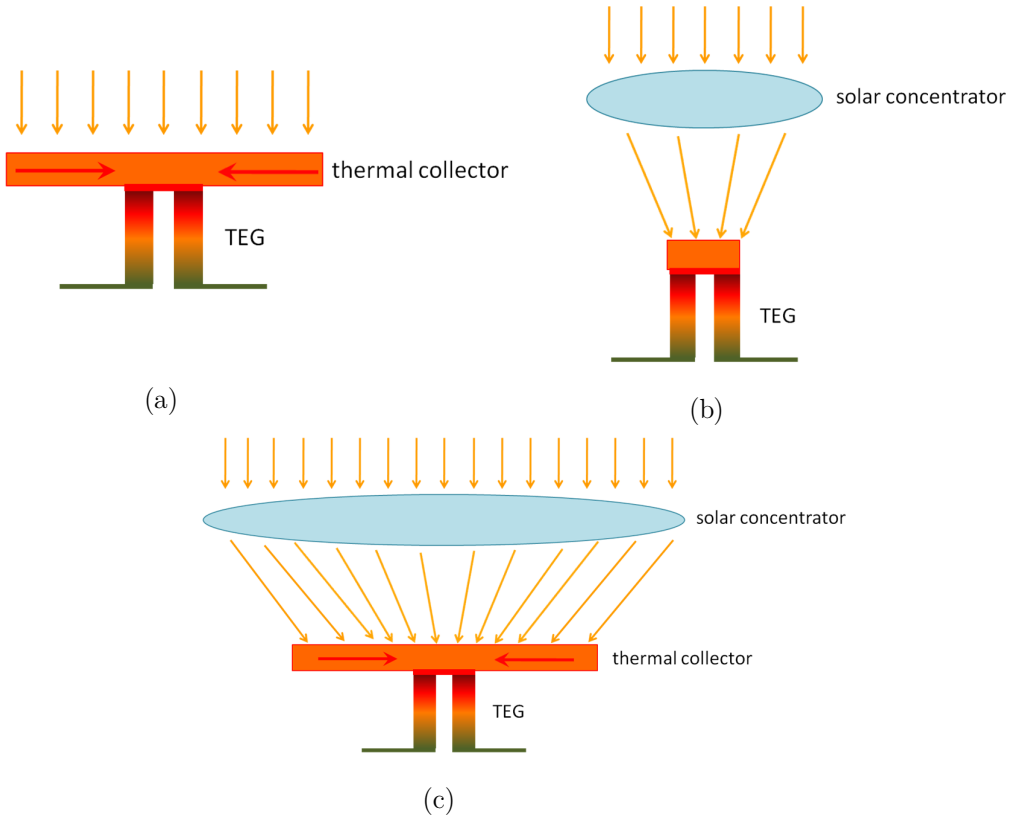


Figure 3-1: (a) STEG implemented with a TEG and thermal collector. (b) STEG implemented with a TEG and a solar concentrator. (c) STEG implemented with a TEG and both solar concentrator and thermal collector.

3.2 STEG Implementations

As previously discussed, published STEGs can be classified into three types depending on the implementation. The first type of STEGS uses thermal collectors or sometimes

referred to as non-concentrating solar collectors such as flat plate collectors (FPCs) and evacuated tube collectors (ETCs). The second type of STEGs uses solar concentrators, which are also referred to as concentrating solar collectors. Examples of solar concentrators are compound parabolic collectors (CPCs), and refractive lenses. Lastly, the third type uses a combination of both solar and thermal concentration to further improve the STEG's efficiency.

3.2.1 STEGs with Thermal Collectors

Flat plate collectors are the simplest and cheapest type of thermal collectors. When solar radiation passes through the cover of a FPC, the plate absorbs a large fraction of this energy and transfers heat onto the thermocouples. (Telkes 1954) developed a STEG that used a flat-plate collector along with a thermocouple made out of a p-type ZnSb alloy and an n-type Bi-based alloy. The reported efficiency of this STEG system was 0.63% under a temperature difference of 70 $^\circ$C. (Poinas et al. 2002) investigated the performance of a flat plate STEG with skutterudite thermocouples, which is to be mounted on a spacecraft flying to/from Mercury. Although performance was inferior to STEGs with solar concentrators, the added design complexity in such systems prompted the researchers to conclude that the simpler flat plate STEGs were more favorable for their application. An alumina plate coated by a graphite layer served as a FPC in the STEG developed by (Tomeš et al. 2010). The plate was coated with graphite to improve emissivity, leading to an increased absorption of solar radiation. This flat plate STEG consisted of a 4-leg TEC module with two pairs of p-type $La_{1.98}Sr_{0.02}CuO_4$ and n-type $CaMn_{0.98}Nb_{0.02}O_3$ legs. The TEC module was then placed at the focal plane of a High Flux Solar Simulator (HFSS) developed by (Hirsch, Zedtwitz, and Osinga 2003) to simulate the heat transfer characteristics of highly concentrating solar systems. A heat flux between 4-8 W/cm^2 gave the maximum efficiency of 0.082% for a TEC with a leg length of 10 mm. Another implementation of a flat-plate STEG by (Hwang, Vorobyev, and Guo 2011) attached a 1 mm thick Al foil to a TEG module. To increase the absorption capacity of the foil, it was treated by femtosecond laser pulses. Their experiments showed that laser-treating the Al foil enhances its absorptance in the UV and visible wavelengths

leading to a greater temperature difference across the TEG module. This resulted in 4-9 times higher efficiency when compared to a STEG with an untreated Al foil.

Thermodynamic analysis of a solar-driven TEG based on a well-insulated flat plate collector was presented in (Chen 1996). The schematic diagram of the modelled solar-driven TEG is shown in Figure 3-2. In this model, the total insolation q_s equals I_sA, where I_s is solar insolation and A is the aperture area of the FPC. The net rate of heat input from the FPC at temperature T_h to the thermoelectric device is denoted as q_h while the net rate of heat rejection from the thermoelectric device to the heat sink at temperature T_c is denoted as q_c. The heat leak via the thermoelectric device is q_k and the heat loss of the FPC is q_L. The corresponding thermal conductances present in the system are represented as k_i's. The useful electrical power P produced by the thermoelectric generator is received by the load resistance R_L. I represents the electrical current. T_1 and T_2 are the temperatures of the two junctions in the thermoelectric device. There are four irreversibilities governing the energy balance and heat transfer equations used in developing the thermodynamic model of the solar-driven TEG. These four irreversibilities are: (1) finite-rate heat transfer between the thermoelectric device and the external heat reservoirs, (2) heat leak via the thermoelectric device, (3) ohmic heat production inside the thermoelectric device, and (4) heat loss in the thermal collector. After evaluating pertinent equations, the total efficiency η_{tot} of the solar-driven TEG is derived to be equal to the product of the thermal collector efficiency η_{th} and the TEG efficiency η_{TEG}.

$$\eta_{tot} = \eta_{th} \cdot \eta_{TEG} \tag{3-2}$$

Characteristic equations show that an increase in the operating temperature of the thermal collector results in a decrease in η_{th} and an increase in η_{TEG}. Hence, the maximum efficiency of the solar-driven TEG exists at a certain optimum operating temperature. The model was then employed using parameters of a typical flat plate collector and a TEG made of n-type semiconductor (75% Bi_2Te_3 and 25% Bi_2Se_3) and p-type semiconductor (25% Bi_2Te_3 and 75% Sb_2Te_3) materials. Results show that a maximum total efficiency of about 5% can be achieved. Characteristic curves generated

in this work relate the total efficiency of the system to the operating temperature of the thermal collector, the reduced current, and the load resistance.

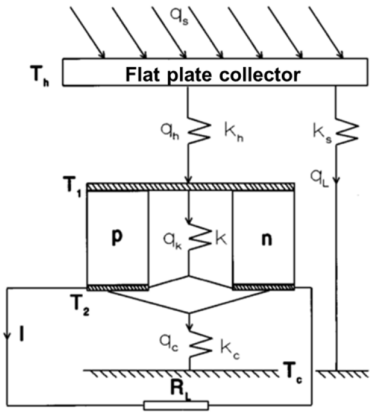


Figure 3-2: Schematic diagram used to develop a thermodynamic model of a solar thermoelectric generator implemented with a TEG and a flat plate thermal collector. (Chen 1996)

STEGs with thermal collectors can also be implemented with evacuated tube collectors (ETCs), which consist of a heat pipe inside a vacuum-sealed tube. They are more preferred than FPCs when weather conditions become unfavorable as condensation and moisture causes early deterioration and system failure in FPCs. (Hasebe et al. 2006) used an ETC to harvest energy from a road pavement and converted this energy into electricity with commercially-available TE modules consisting of n-type $Bi_{0.5}Sb_{1.5}Te_3$ and p-type $Bi_{1.8}Sb_{0.2}Te_{2.85}Se_{0.15}$ thermocouples. The implemented STEG has 19 TE modules, with each module having 64 thermocouples. The peak output power was about 5 W for an electronic load of 30 **Ω**.

3.2.2 STEGs with Solar Concentrators

The use of solar concentrators that concentrate solar radiation results in an enhancement in STEG efficiency (Yazawa and Shakouri 2010). The main reason for this is that solar concentration enables the TEG to achieve temperatures above those attainable by using FPCs or ETCs (Kalogirou 2004). The most commonly-used solar collectors of this type are refractive lenses and compound parabolic collectors (CPCs).

Aside from implementing a flat plate STEG, (Telkes 1954) also investigated the improvement in efficiency of a STEG when using a concentrating solar collector such as a lens. A Fresnel lens with 50× optical concentration was used to achieve a temperature difference of 247 ° C and an efficiency of 3.35% was observed, much higher than the 0.63% efficiency achieved by a flat plate STEG.

A two-dimensional steady-state heat transfer model of a thermoelectric converter (TEC) subjected to concentrated solar radiation was presented in (Suter et al. 2010). The model couples radiation, conduction, and convection heat transfer with electrical potential distribution. A cross section of the model domain, divided into $m \times n$ cells, is depicted in Figure 3-3. It contains three major components: the absorber plate, one p-type and one n-type thermoelectric leg, and the space in-between legs. The domain is assumed to be infinitely long and as such, periodic boundaries are set at the right and left sides. It is also assumed that conductive heat transfer occurs at the entire domain, radiative heat transfer occurs on all surfaces, and convective heat transfer only occurs from the top of the hot plate. With these assumptions, governing equations for heat transfer and electrical potential are formulated, discretized, and solved numerically by applying the finite volume (FV) technique. In this work, the solar-to-power efficiency of the TEC module is defined as:

$$\eta = \frac{P_{max}}{A_{abs} \cdot q''_{solar}} \tag{3-3}$$

Higher temperature difference across the thermoelectric legs is observed for higher values of q''_{solar}, which should result in higher efficiency. However, re-radiation losses that are proportional to T^4 cause the efficiency to decrease with higher temperature difference. Thus, an optimum q''_{solar} for maximum efficiency is obtained. For example, a 4-leg TEC module with leg lengths of 10 mm was measured to have a maximum efficiency of 0.083% at $q''_{solar} = 4$ W/cm^2.

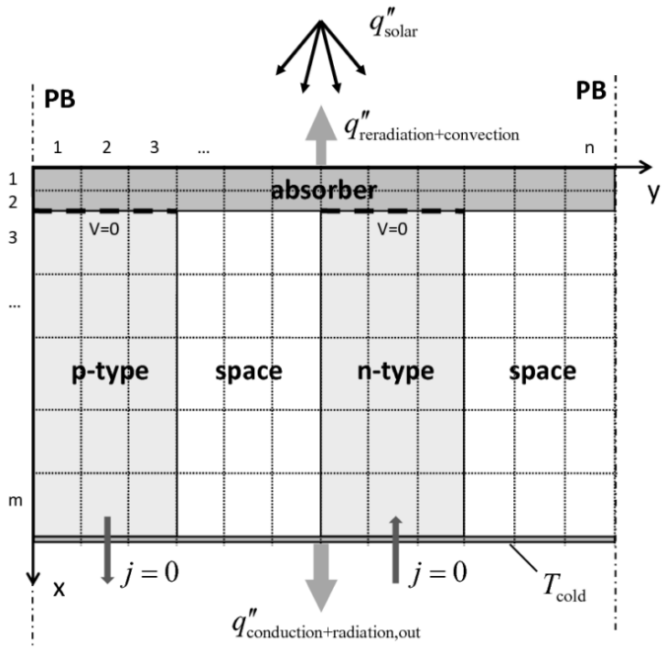


Figure 3-3: Cross section of heat transfer model divided into m × n cells, with indicated boundary conditions. (Suter et al. 2010)

A thermodynamic analysis of a STEG using cheap parabolic concentrators with high-ZT thermoelectric modules by (Amatya and Ram 2010) predicts the thermal-to-electrical conversion efficiency of the device. The thermodynamic analysis is based on the principles of energy balance and heat transfer. The model considers losses in the concentrator and losses in the thermoelectric module. The efficiency of the concentrator is limited by convective and radiative losses, which defines how effectively solar flux can be guided into the thermoelectric module. Meanwhile, the TE module efficiency mainly depends on the material and its design. Applying their model to a system with 70× solar concentration on Bi_2Te_3 TE modules (ZT = 0.64) under natural air convection yielded a system efficiency of 4%. This model takes into account the temperature dependence of material properties such as thermal conductivity, electrical resistivity, and Seebeck coefficient. Simulations of the system efficiency at various input solar fluxes showed that a peak in the system efficiency exists because the thermoelectric properties of the material degrade as the hot side temperature increases. This trend in system efficiency was also confirmed in the model for STEGs with thermal collector developed by (Cai et al. 2011). The latter model concluded that if the thermal conductivity of the heat collector is greater than 50 W/mK, it would have little influence on the system efficiency.

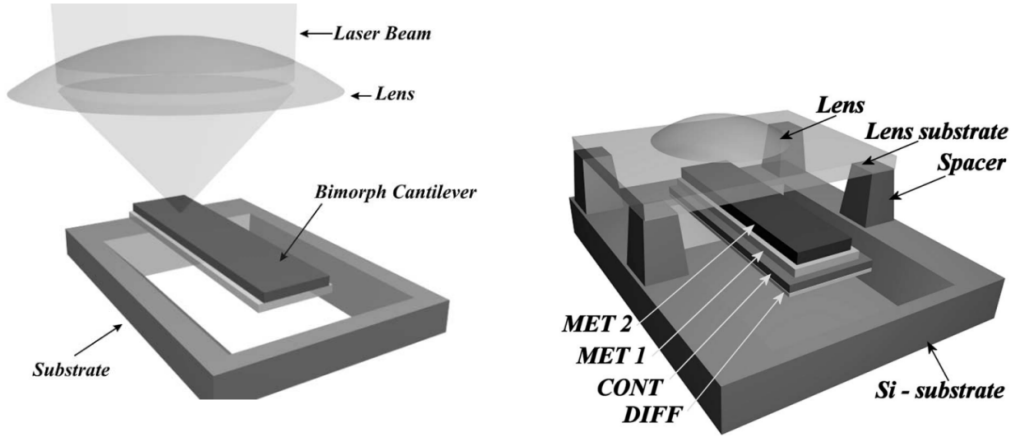
Two-stage solar concentrators can more efficiently concentrate solar radiation as demonstrated in (Amatya and Ram 2010) where a parabolic reflector was used to direct sunlight onto a fixed focal spot. The hot side of a commercial Bi_2Te_3 TEG module was then placed at this spot and heats up as it absorbs concentrated sunlight. A second concentrator, a Fresnel lens, was also used to further increase flux concentration. The total system efficiency as described in equation 2-14 was measured as 3% for a solar concentration of 66× suns. The authors also predicted that a total system efficiency 5.6% can be achieved with novel thermoelectric materials such as n-type $(InGaAs)_{1-x}(InAlAs)_x$ and p-type $(AgSbTe)_x(PbSnTe)_{1-x}$.

A prototype of a solar TEG using a CPC was developed in (Vatcharasathien et al. 2005). The solar TEG uses a CPC with locally-made Al foil reflector to concentrate heat onto sixteen TEG modules that were connected to form a 4×4 TEG array. Although poor performance was observed owing to the relatively small surface area and low reflectivity of the CPC reflector used, the authors still concluded that the system of using solar collectors in conjunction with TEG modules was practically feasible.

A CPC was also designed and fabricated by (Mgbemene et al. 2010) as the solar collector in their STEG system comprising of a commercially-available TEG module with 127 pairs of thermoelements. The surface of the CPC was covered with aluminum foil and attached to a thin copper heat spreader. The experimental set-up has a concentration ratio of 7.6 and gave a power density of approximately 6 kW/m^2 – more than 6 times better than the 0.945 kW/m^2 power density of the TEG without a CPC.

At the micro scale, a monolithic model of a novel photo-thermo-mechanical microactuator was presented in (Baglio et al. 2002b) where a lens is used to focus a laser beam onto one end of a bimorph cantilever as shown in Figure 3-4a. The lens was proposed to be mounted on top of the cantilever using spacers as shown in Figure 3-4b. A standard CMOS technology was proposed for fabricating the device, along with bulk anisotropic etching of the silicon to realize the suspended cantilever. An additional oxide layer would then be required for the realization of the microlenses (Baglio et al. 2002c). The aim of the lens was to improve the efficiency of the actuation system since the

amount of energy that the actuator gets becomes proportional to the ratio of the surface area of the lens to the irradiated surface area of the cantilever. The authors further explored adding a TEG, i.e. thermopiles, on the heated end of the cantilever to serve as an on-chip power supply (Baglio et al. 2003). A 2×3 array of these photo-thermo-mechanical actuators was also proposed to realize a six-legged autonomous micro-robot (Baglio et al. 2002a). Regrettably, no work on the fabricated system, if any, has been published. However, in relation to applying photo-thermo-mechanical conversion at the micro scale, optical actuation of surface micromachines has already been successfully reported (Oliver, Vigil, and Gianchandani 2003)(Liu et al. 2008)(Elbuken et al. 2008).



(a) (b)

Figure 3-4: (a) Proposed structure of the photo-thermo-mechanical microactuator. (b) Illustration showing the use of spacers to mount lens above the microactuator. (Baglio et al. 2002b)

A patent of a solar thermoelectric generator using a lens as concentrator has also been published (Chen & Ren 2010). Several designs using a lens to concentrate solar radiation onto either a vertical/vertical TEG or a lateral/lateral TEG were proposed. The patent also claims that increasing the temperature difference between the hot and cold side of the TEG to 700K can improve the efficiency of the device up to 17-25%.

Lastly, (McEnaney et al. 2011) developed a model that calculates the efficiency of STEGs with either cascaded or segmented vertical/vertical TEGs. The cascaded architecture has slightly higher efficiency over its segmented counterpart. This is attributed to the

additional degree of freedom brought about by the fact that there are two currents flowing through the cascaded STEG. Cascaded STEGs can have a theoretical efficiency exceeding 10% with the hot-side temperature running at 600 ° C and a solar concentration ratio of 45. Results from experiments with no or little solar concentration match those of the model. For cases where there is high optical concentration, effectivity of the model was only implied and not yet tested.

3.2.3 STEGs with both Solar and Thermal Concentration

Another approach to further improve the efficiency of STEGs is to use thermal collection in addition to solar concentration. In this type, a solar concentrator is used to focus solar radiation onto a thermal collector. Heat is absorbed by the thermal collector and conducted through the TEG legs.

The theoretical efficiency of a single couple solar powered thermoelectric generators based on Si-Ge alloys with both solar and thermal concentration was first presented in (Rowe 1981). It was shown that the efficiency improved with increasing solar concentration and that under optimal operating conditions, the overall efficiency of the device was computed to be in excess of 12% when operating between room temperature and 1000 K.

Researchers from Tohoku University in Japan also demonstrated this approach when they combined a thermionic system with a thermoelectric system (Naito et al. 1996). A schematic diagram of their system is shown in Figure 3-5. A paraboloidal mirror was used to concentrate solar radiation onto the inner wall of a cavity-type graphite solar receiver. The molybdenum (Mo) cup acted as a thermal collector, which eliminated thermal radiation heat loss through the outside of the receiver. Heat was then directed to a thermoionic converter (TIC) through a small hole in the Mo cup. Thermal energy released from the TIC was transferred to the hot side of the thermoelectric converter (TEC) using a heat pipe. The researchers claim that this type of conversion system has potential for high-efficiency conversion because the TIC emitter is heated more effectively by concentrated solar radiation.

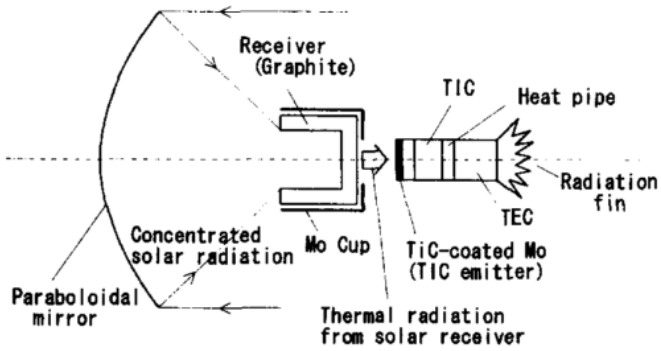


Figure 3-5: Schematic diagram of solar-powered conversion system developed in Tohuku University, Japan. (Naito et al. 1996)

In (Li et al. 2010), two Fresnel lenses were proposed to be used to concentrate solar radiation from both sides of a collector by means of a reflective mirror. The heat collector is to be coated with a selective absorber in order to absorb sunlight more efficiently. The heat collector is to be attached to thermoelectric modules, which are then attached to a heat sink. Numerical simulations based on performance parameters of Bi_2Te_3 obtained from literature yielded the highest possible efficiency of 9.8% at 60× concentration ratio. As of writing of this report, no working STEG prototype from these researchers has been found.

A parabolic dish collector and four BiTe-based thermoelectric cells were used in (Fan et al. 2011) to implement a concentrating STEG. A copper receiver plate, acting as the thermal collector, was positioned below the focal point of the dish to capture radiation reflected from the collector. The receiver plate then evenly spreads heat onto the thermoelectric cells. Tests were conducted under different heat fluxes and the system was able to produce electric power of up to 5.9W with a temperature difference of 35 ° C.

A theoretical analysis of the potential performance of STEGs with both solar and thermal concentration under terrestrial conditions has been presented in (Chen 2011). Solar radiation irradiates a solar concentrator and gets transmitted through a wavelength-selective surface, which acts as a thermal collector. The wavelength-selective surface then absorbs the radiation and heat is conducted through the thermoelements and is dissipated to the environment at the cool side. Thermal concentration is achieved by taking the ratio of the selective surface area to the total cross-sectional area of the

thermoelements. The mathematical model of the system assumes that the selective surface is maintained at a uniform temperature, thermoelectric properties of the material are temperature-independent and electrical and thermal contact resistances are negligible. The maximum STEG efficiency, which is the product of the solar-thermal efficiency and the device efficiency, exists because the device efficiency increases but the solar-thermal efficiency decreases with increasing hot side temperature. Hence, there is an optimal hot-side temperature that maximizes the STEG efficiency. For a given optical concentration ratio, this optimal hot-side temperature depends on the thermoelectric materials' non-dimensional figure-or-merit, the optical properties of wavelength-selective surface and the efficiency of the solar concentrator system. Calculations using this model indicate that with minimal or no solar concentration, STEG system efficiency larger than 5% can be achieved with a hot-side operational temperature between 150–250 $^\circ$C.

(Kraemer et al. 2011) reported a functional prototype of a STEG employing both solar and thermal concentration. The device is shown without the solar concentrator in Figure 3-6. It consisted of a pair of nanostructured n- and p-type Bi_2Te_3 alloys, the thermoelectric properties of which have been fully characterized in (Poudel et al. 2008). In addition to using materials with a high thermoelectric figure-of-merit, high-performance wavelength selective absorbers were also used to increase the absorption capacity of the thermal concentrator. Lastly, the thermoelements were also enclosed in vacuum to minimize air convection and conduction losses. Without any solar concentration, the researchers reported an efficiency of 5% (Kraemer et al. 2012). The researchers further predicted that the STEG efficiency can reach up to 14% provided that thermoelements have ZT=2, 10$\times$ solar concentration is employed, and the absorber has an optimum temperature of 300 $^\circ$C.

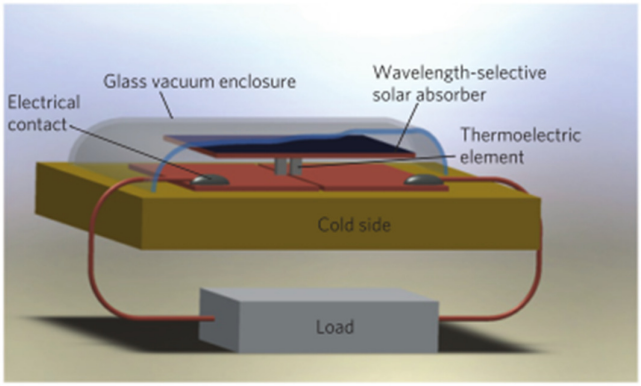


Figure 3-6: An evacuated STEG device illustrating thermal concentration with the use of a selective solar absorber. (Kraemer et al. 2011)

3.3 PV-TE Hybrid Devices

Thermoelectric (TE) generators can also be used along with photovoltaic (PV) cells to enhance the performance of a solar-to-electric conversion system (Tobias and Luque 2002) (Dai et al. 2003)(Yu et al. 2008)(Kraemer et al. 2008)(Bermel et al. 2010)(Chang et al. 2010). Only a small portion of the sun's total spectrum is available for photovoltaic conversion; a large amount of remaining solar radiation mainly produces heat energy. A patent by (Hunt 2004) presented a simple structure shown in Figure 3-7, which had at least one thermoelectric module thermally attached to a PV module and could generate electricity from both the PV cell and the thermoelectric module. Note that a lens is positioned over the PV module for focusing solar radiation.

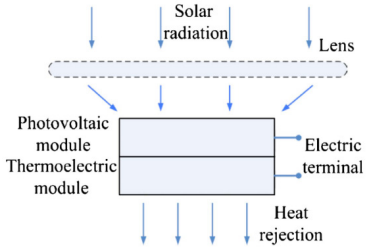


Figure 3-7: A simple structure combining photovoltaic (PV) and thermoelectric (TE) conversion. (Hunt 2004)

As shown in Figure 3-8, (Wang et al. 2011) implemented a novel PV-TE hybrid device composed of a series-connected dye-sensitized solar cell (DSSC), a commercially-available solar selective absorber (SSA), and a commercially-available TEG. The DSSC was

constructed from a dye-coated TiO_2 film photoanode, a transparent platinum counter electrode, a polyethylene spacer, and an iodide-based liquid electrolyte. The SSA and TEG utilize residual sunlight transmitted through the DSSC to improve the overall efficiency. The conversion efficiency of the DSSC was 9.26%; the conversion efficiency of the DSSC with a TEG was 12.8%; and the conversion of the DSSC with both the SSA and TEG was 13.8%.

A PV-TE hybrid solar generator using a commercially available PV module of amorphous silicon from Sanyo Electric and a bismuth telluride-based TE module has been implemented by (Mizoshiri, Mikami, and Ozaki 2012). This system is shown in Figure 3-9. Ultraviolet (UV) to visible light was used for PV conversion whereas near infrared (NIR) light, which does not contribute to PV conversion, was separated from solar light using a hot mirror. A cylindrical NIR lens focused as much NIR light as possible to the TE module so as to maximize the temperature difference across the TEG. The PV-TE system generated an open circuit voltage of 78 mV and output power of 190 nW at a temperature difference of 20 ° C. The voltage generated by the PV-TE system

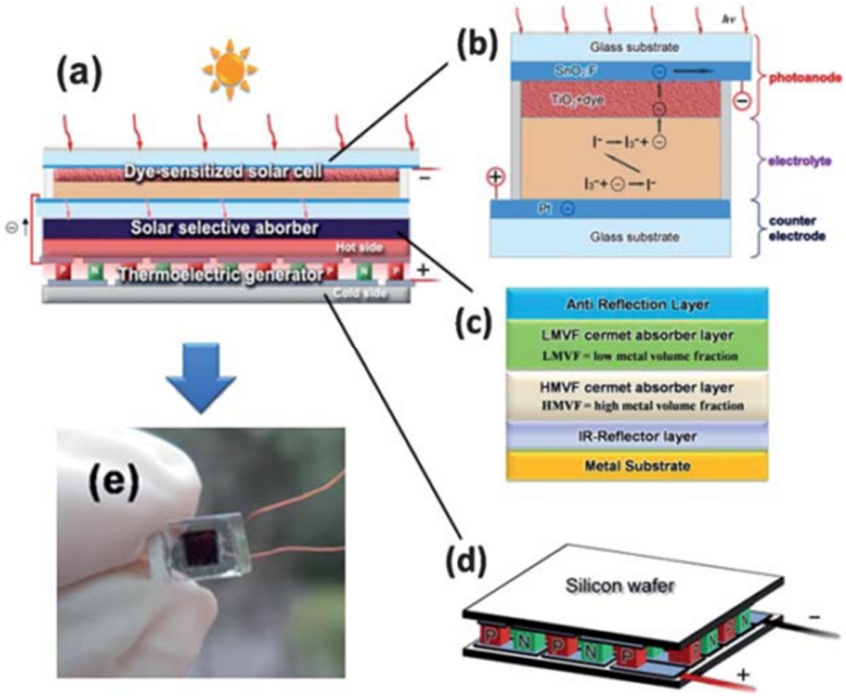


Figure 3-8: Schematic illustrations of: (a) PV-TE hybrid device, (b) DSSC, (c) SSA, and (d) TEG; photograph of (e) PV-TE hybrid device (Wang et al. 2011).

increased by 1.3% compared to that generated by the PV module alone. Although this increase in output voltage is rather small, the authors recommended that depositing thicker films to decrease the resistance should result in higher output power from the PV-TE system. The authors also recommended using an optimized NIR focusing lens with high numerical aperture to increase the temperature difference across the TEG, which would result in a more significant improvement on the PV-TE system's efficiency.

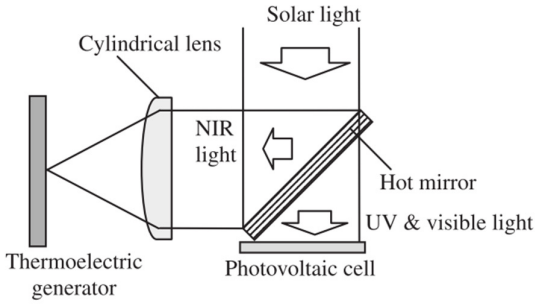


Figure 3-9: A schematic illustration of a PV-TE hybrid system composed of a PV module, TEG module, hot mirror, and a cylindrical focusing NIR lens (Mizoshiri, Mikami, and Ozaki 2012).

In (Deng et al. 2013), a PV-TE hybrid system was implemented consisting of an amorphous silicon thin-film cell (STC), four commercially available TEGs electrically connected in series, and a bowl-shaped heat collector. A schematic illustration of this system is shown in Figure 3-10. The heat collector was made up of a copper foil covered with a black polymer to effectively absorb solar heat. A foam polymer was taped at the back of the copper foil to provide insulation. Not only the residual heat from the STC was utilized by the TEGs, but also parts of the solar energy were collected by the heat collector and conducted to the TEGs. The total power generated by this PV-TE hybrid system was 393 mW, which was twice that generated from a single STC.

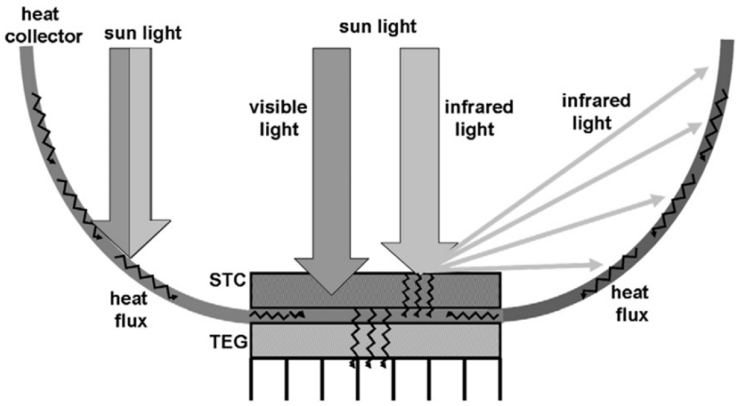


Figure 3-10: A schematic illustration of a PV-TE hybrid system composed of a silicon thin-film cell (STC), a TEG, and a heat collector (Deng et al. 2013).

3.4 Summary

In this chapter, three ways of implementing solar thermoelectric generators are presented. The first type of STEGs is implemented with a TEG and a thermal collector, where heat from the sun is absorbed by the thermal collector and conducted over to the thermoelectric generator. The second type of STEGs is implemented with a TEG and a solar concentrator, where the solar concentrator focuses solar heat onto the TEG and results in an increase in the amount of input heat flux to the TEG. The third type of STEGs is implemented with both a thermal collector and a solar concentrator to further enhance the TEG's efficiency.

Several analytical models and implementations of the 3 types of STEGs have also been discussed. The concept of using a lens with a vertical/vertical μTEG has been successfully demonstrated in (Kraemer et al. 2011). Although no implementation of a STEG employing lateral/lateral μTEGs have been found, the concept of using a lens in conjunction with a lateral/lateral thermoelectric generator to serve as on-chip supply to a microactuator is presented in (Baglio et al. 2003). This motivates further work on implementing a solar-driven micro-scale lateral/lateral TEG.

Lastly, thermal-photovoltaic hybrid systems are also discussed to demonstrate a very promising way of solar energy utilization with the possibility of further enhancement in efficiency by utilizing both photovoltaic and thermoelectric technologies.

Chapter 4: STEG Simulation and Modelling

In this chapter, the design of the proposed STEG with a lens acting as a solar concentrator is presented. First, results of experiments done using commercially available devices are reported to illustrate the proposed system's feasibility. Next, the conceptual design of the solar-driven TEG is described. Heat transfer simulation results are also given to verify that the use of a solar concentrator significantly increases the temperature difference across the TEG, consequently resulting in an improvement in device efficiency. Then, an analytical thermal model of the device is developed. Finally, results obtained from heat transfer simulations are compared to those calculated using the thermal model to validate the model's ability to predict the STEG's thermoelectric performance.

4.1 Proof-of-Concept Experiments

The functionality of using a magnifying lens as the solar heat concentrator of a commercially-available TEG unit is verified in (de Leon, Taatizadeh, and Kraft 2010). The set-up of the experiment is shown in Figure 4-1. To perform the experiment, a Farnell MCPE1-12707AC-S Peltier TEG unit is placed over the center of a Farnell 395-1AB heat sink. A 5x magnifying lens is then positioned over the TEG keeping a distance equivalent to its focal length to give the best solar heat concentration ratio. To monitor the temperature changes, one thermocouple wire is glued to the middle of the TEG unit and another wire is glued 1cm away. The output terminals of the TEG are connected to a digital multimeter that displays the value of the generated voltage.

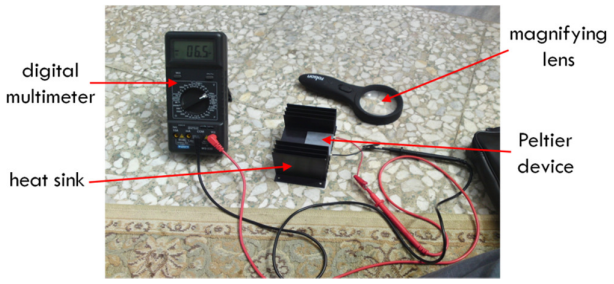


Figure 4-1: Experiment set-up using discrete components. (de Leon, Taatizadeh, and Kraft 2010)

Figure 4-2 shows a plot of the system's output voltage with and without the use of a magnifying lens. Two magnifying lenses having diameters of 6 cm and 10 cm are used. As expected, higher voltage is generated when a lens is used which can only be attributed to a greater temperature difference across the thermocouple junctions of the TEG. Moreover, using the lens with a larger surface area resulted in a higher output voltage. Unfortunately, the thermocouple wires placed on the surface of the TEG unit only gives information on how heat is distributed across the device but not the actual temperature difference across the thermocouple junctions. Nevertheless, the increase in the amount of voltage generated is sufficient to show that the efficiency can be increased by using a solar concentrator.

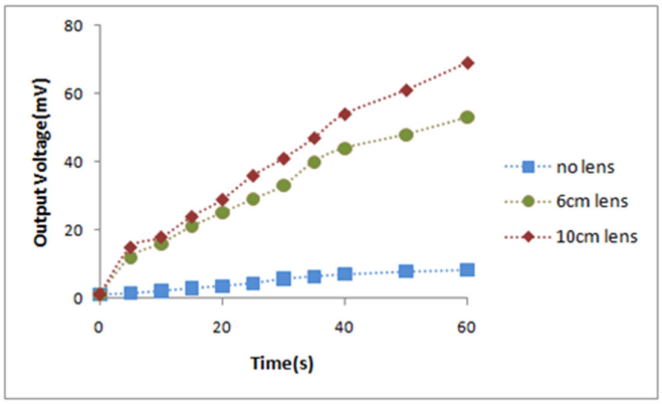


Figure 4-2: Open circuit output voltage measured with the experiment set-up with and without a magnifying lens. (de Leon, Taatizadeh, and Kraft 2010)

4.2 Conceptual Design of Solar TEG

After verifying that using a solar concentrator can effectively improve the efficiency of thermoelectric generators using discrete components, its application at the micro level is investigated. The proposed solar TEG is shown in Figure 4-3. As mentioned in section 2.3.6, the TEG design is adapted from that of (Egbert, Harvey, and Otis 2007) where a SOI wafer is used and the thermoelements are fully suspended through a membrane so as to increase the heat flux path across the device. Their proposed fabrication process involved using a SOI wafer with a high-resistivity device layer and alternately doping by diffusion to form n- and p-type thermoelements. To simplify the TEG fabrication process,

it is planned to utilize a SOI wafer with a pre-doped device layer and utilize this layer as one of the thermoelements, and with aluminum as the second thermoelement. Another difference of the TEG design from that of (Egbert, Harvey, and Otis 2007) is that the thermoelements are oriented radially around the circular membrane. The suspended membrane is circular in geometry to insure optimum transfer of heat from the center of the membrane to the tip of the thermoelements.

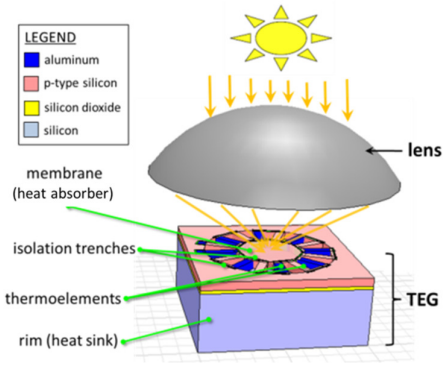


Figure 4-3: Proposed design of solar-driven TEG using an SOI wafer.

Suppose the sun uniformly irradiates an energy density q_s onto the lens, then the heat power density q_h of the incoming heat flux to the TEG membrane is given by:

$$q_h = \gamma \tau_{lens} \alpha_{mem} q_s \tag{4-1}$$

where γ is the concentration factor, τ_{lens} is the lens transmittance, and α_{mem} is the membrane absorptance. The concentration factor is proportional to the ratio of the effective lens diameter to the spot size diameter on the membrane as given by equation 4-2. The effective lens diameter is smaller than the actual lens diameter and is dependent on the lens mount used and the clear aperture of the lens.

$$\gamma = \left({d_{lens,eff}}/{d_{spot}} \right)^2 \tag{4-2}$$

With this approach, an input heat flux in the order of hundreds of kW/m^2 can be generated. Based on the general heat transfer equation (Bejan and Kraus 2003), an increase in the input heat flux would translate to a corresponding increase in the

temperature difference across the thermoelements; also resulting in an effective increase in its output voltage as described in equation 2-7.

4.3 Heat Transfer Simulations

To further investigate the functionality of the proposed system, a case study involving 3-dimensional heat transfer simulations of several TEG device configurations are performed using COMSOL. All simulations are performed with the TEG device in an open circuit. This means that Peltier effect, Thomson effect, and Joule heating are not considered in the simulations. Four of these configurations are shown in Figure 4-4. In all four cases, there are 8 Si-Al thermocouples with each thermoelectric leg having a length of 200 μm and a width of 50 μm. For the first three configurations in Figure 4-4, the SOI wafer used in the simulations has the following thicknesses: 500 μm for the substrate layer, 2 μm for the oxide layer, and 5 μm for the device layer. Heat transfer by convection is modelled by setting the top surface of the membrane, top surface of the rim, and bottom surface and sidewalls of the substrate to have heat transfer coefficients corresponding to natural external convection with air. The ambient temperature is set to 20 ° C. The device has an area of 1×1 mm^2 and the membrane has a diameter of 400 μm and the area being heated located in the middle of the membrane has a diameter of 300 μm. The input heat flux is 200 kW/m^2 in all four cases.

As can be observed from the heat distribution of TEG devices in Figure 4-4, the highest temperature difference is achieved when the membrane and thermoelements are fully suspended. The cavity effectively minimizes heat loss through the substrate and maximizes the temperature difference between the hot and cold junctions of the device. However, this entails a more challenging fabrication procedure than the other configurations as the structural stability of a fully suspended membrane has to be taken into account. A compromise between thermal efficiency and structural stability is by keeping the buried oxide layer under the membrane and thermoelements as is shown in Figure 4-4b. Although the buried oxide layer is just in the order of a few microns, it will still provide a certain level of structural stability to the device. It can also be noted that

since the oxide layer has a low thermal conductivity, the absolute temperatures across the device is higher than the TEG in Figure 4-4a. The TEG configuration in Figure 4-4c further reinforces the need to remove the handle layer of a SOI wafer as significant heat losses occur through the substrate, bringing down the temperature difference to just about a tenth of a degree. In contrast, a substrate with a low thermal conductivity, such as glass, is shown in Figure 4-4d. This configuration is highly structurally stable as there are no suspended elements and is still able to generate a substantial temperature

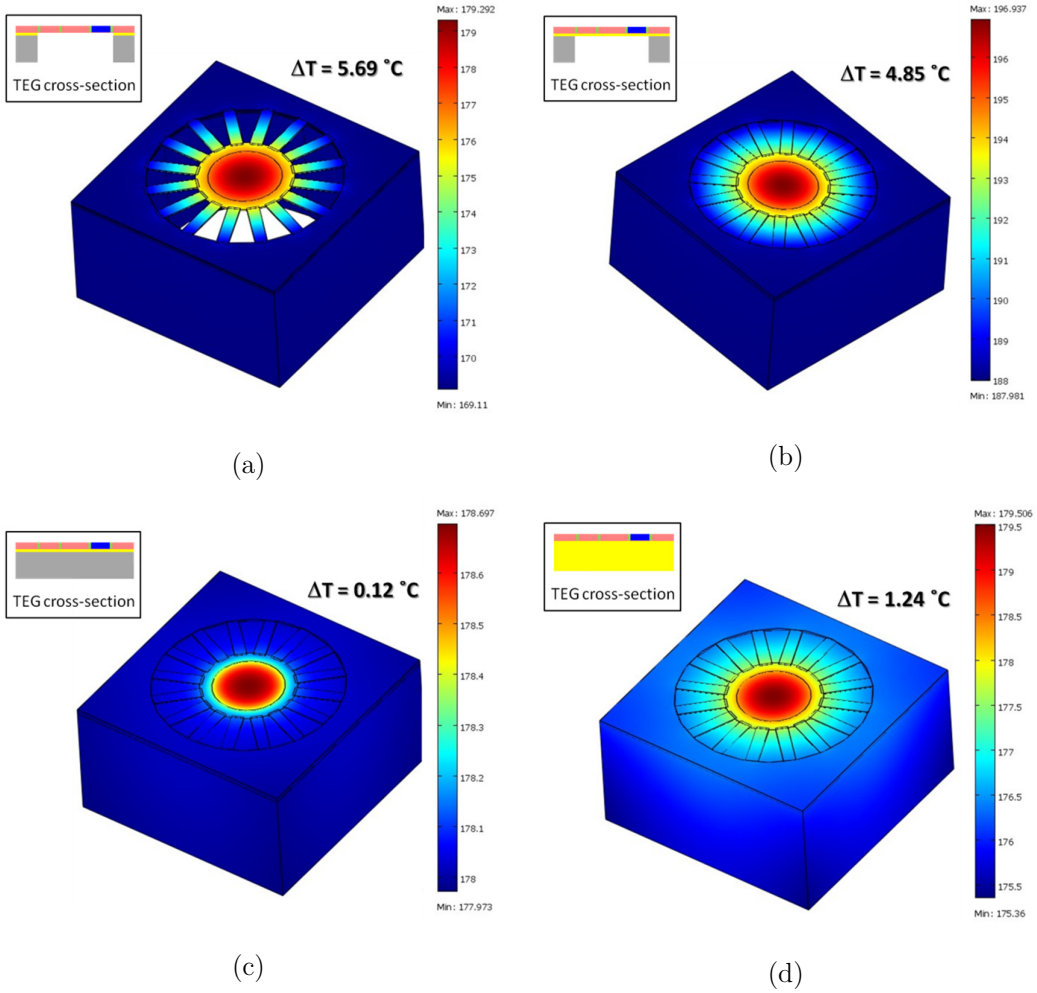


Figure 4-4: Temperature distribution after 10min for 1×1 mm^2 TEG devices (a) with both handle and oxide layers of a SOI wafer under the membrane and thermoelements fully etched, (b) with the handle layer of a SOI wafer etched until the buried oxide layer, (c) with no etching performed on the handle and oxide layers of a SOI wafer, and (d) with a glass substrate. All devices have 8 thermocouples (length = 200 µm, width = 50 µm, and membrane diameter = 400 µm) and an input heat flux of 200 kW/m^2.

difference across the thermoelements. Although the thermal efficiency is not as good as that with a fully suspended membrane, the fabrication process using a glass substrate is simpler and cheaper.

Focusing on the TEG configuration in Figure 4-4a and with the device layer of the SOI wafer set to have a thickness of 5 µm, COMSOL's two-dimensional out-of-plane heat transfer module is employed to simulate 10 x 10 mm^2 devices as it was verified from three-dimensional heat transfer simulations that for a suspended 5 µm thick device layer, there is no significant temperature variation across the thickness of the thermoelements. Figure 4-5 shows a sample finite element heat transfer simulation of the proposed thermoelectric generator design. The amount of input power on the TEG membrane is the product of the input heat flux and the heated membrane surface area.

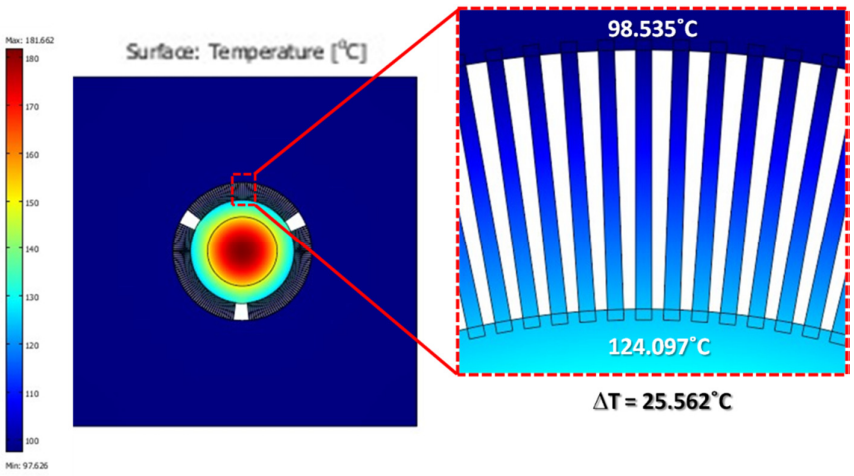


Figure 4-5: Heat distribution on a SOI TEG with length = 500 µm, width = 30 µm, thickness = 5 µm, membrane diameter = 3 mm, and 81 thermocouples for a concentration factor of 225, lens transmittance of 90%, and membrane absorptance of 50%, with a 2 mm diameter solar radiation spot size

To demonstrate the effect of using a solar concentrator, a constant heat flux occupying 1 mm^2 is applied at the center of the membrane. The value of the input heat flux is varied from 50 kW/m^2 to 500 kW/m^2. With the solar heat flux equivalent to 1kW/m^2 (Amatya and Ram 2010), the concentration factor is then varied to emulate the use of different-sized lenses to focus solar heat onto the center of the device. Table 4-1 lists the results of heat transfer simulations performed on the TEG in Figure 4-5 as the concentration factor

is varied. Results clearly show that the efficiency of the TEG improves with increasing input heat flux. This means that by using a convex lens, the temperature difference across a thermocouple can be increased; resulting in an increase on the TEG's efficiency.

In contrast to a TEG with fully-suspended membrane and thermoelements, simulating a TEG fabricated on a glass substrate cannot employ two-dimensional out-of-plane heat transfer as there is significant heat lost through the substrate. Because of this lossy substrate, thinner thermoelements has to be considered so as to maximize the temperature difference across the thermoelements. In this particular case, three-dimensional heat transfer simulations are performed for a device with the same dimensions as in Figure 4-5 except that the thickness is set to 1μm. Despite this 5-fold decrease in thermoelement thickness, the temperature difference is only about 5 ˚ C.

Table 4-1: Temperature difference, Carnot efficiency, and conversion efficiency of 10×10 mm^2 TEG with fully suspended membrane and thermoelements. TEG dimensions: length = 500 μm, width = 30 μm, membrane diameter = 3 mm, and 81 thermocouples, lens transmittance of 90%, membrane absorptance of 50%, and varying concentration factors, with a 1 mm diameter solar radiation spot size.

Concentration Factor, γ	T_H (˚ C)	T_C (˚ C)	ΔT (˚ C)	η_C (%)	η_{TEG} (%)
100	32.51	29.71	2.80	0.92	0.0026
200	44.56	38.94	5.62	1.77	0.0051
300	56.34	47.90	8.44	2.56	0.0077
400	67.92	56.65	11.27	3.30	0.010
500	79.31	65.21	14.10	4.00	0.013
600	90.53	73.62	16.91	4.65	0.015
700	101.61	81.88	19.73	5.26	0.018
800	112.53	89.99	22.54	5.84	0.021
900	123.31	97.96	25.35	6.39	0.023
1000	133.96	105.80	28.16	6.92	0.026
1500	185.20	143.12	42.08	9.18	0.038
2000	233.30	177.50	55.80	11.02	0.051
2500	278.41	209.16	69.25	12.56	0.063
3000	320.69	238.29	82.40	13.88	0.075

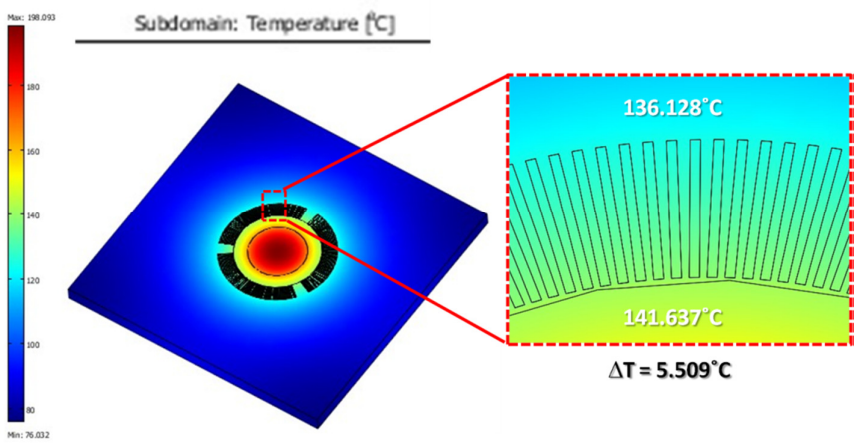


Figure 4-6: Heat distribution on a TEG on a glass substrate with length = 500 µm, width = 30 µm, thickness = 1 µm, membrane diameter = 3 mm, and 81 thermocouples for a concentration factor of 225, lens transmittance of 90%, and membrane absorptance of 50%, with a 2 mm diameter solar radiation spot size

4.4 STEG Thermal Model

Prior to going into the details of the STEG thermal model, consider that the thermocouple materials are to be p-type silicon and aluminum. This is under the assumption that the SOI wafer to be used has a boron-doped silicon device layer. An initial survey of available SOI wafers at Ultrasil Corporation showed that there are more available heavily doped p-type SOI wafers with thin device layers than n-type ones. Aluminum is assumed as the second thermoelement for ease of fabrication. The electrical and thermal properties of both p-type silicon and Al are listed in Table 4-2. These parameters are used to calculate the predicted performance of the proposed STEG, which are presented later in this chapter.

Table 4-2: Electrical and thermal properties of p-type Si and Al.

	p-type Silicon	Aluminum
Seebeck coefficient (µV/K)	375 [b]	-1.8 [a]
Electrical resistivity (Ω-cm)	$5x10^{-3}$ [b]	$2.65x10^{-6}$ [c]
Thermal conductivity (W/mK)	125 [b]	237 [d]

[a] (Kasap 2001)
[b] (Egbert, Harvey, and Otis 2007)
[c] (The Physics Hypertextbook)
[d] (Shackelford and Alexander 2001)

Figure 4-7 shows the top and cross-sectional views of the proposed thermoelectric generator. Q_{MEM} refers to the rate of heat flow from the heat absorber to the TEG while Q_{RIM} refers to the rate of heat flow from the generator to the TEG's rim. The temperatures at specific points are also labelled in Figure 4-7b.

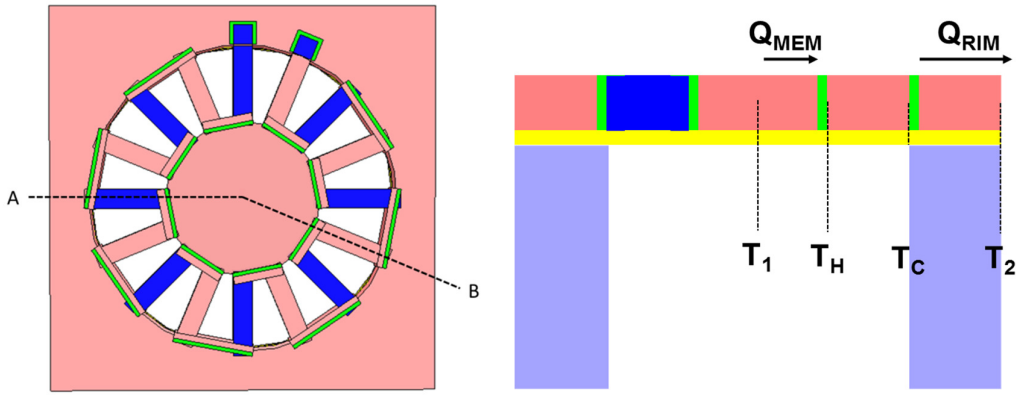


Figure 4-7: (a) Top view and (b) cross section along AB of thermoelectric generator.

The effective electrical and thermal properties of a thermocouple (TC) based on the materials' properties and assuming that both legs of the TC have the same dimensions are as follows:

$$\text{Seebeck coefficient of TC: } \alpha = \alpha_{Al} - \alpha_{p-Si} \tag{4-3}$$

$$\text{Electrical resistivity of TC: } \rho = \rho_{Al} + \rho_{p-Si} \tag{4-4}$$

$$\text{Thermal conductivity of TC: } \lambda = \lambda_{Al} + \lambda_{p-Si} \tag{4-5}$$

It is also assumed that α, ρ, and λ of the TCs are independent of temperature. Hence, the TEG's total electrical resistance R_{TEG} is approximated to be:

$$R_{TEG} = N\frac{\rho l}{wt} \tag{4-6}$$

where N is the number of thermocouples, l is the length of each thermoelectric leg, w is the width of each thermoelectric leg, and t is the thickness of each thermoelectric leg.

Similarly, the total Seebeck coefficient S_{TEG} and total thermal conductance K_{TEG} of the TEG are given by:

$$S_{TEG} = N\alpha \tag{4-7}$$

$$K_{TEG} = N\frac{\lambda wt}{l} \tag{4-8}$$

The open-circuit output voltage of the TEG is then given by:

$$V_{TEG} = S_{TEG} \cdot \Delta T \tag{4-9}$$

where $\Delta T = T_H - T_C$.

Assuming that a load resistance equal to R_{TEG} is attached to the output, then the current I and the output power P_{OUT} can be expressed as:

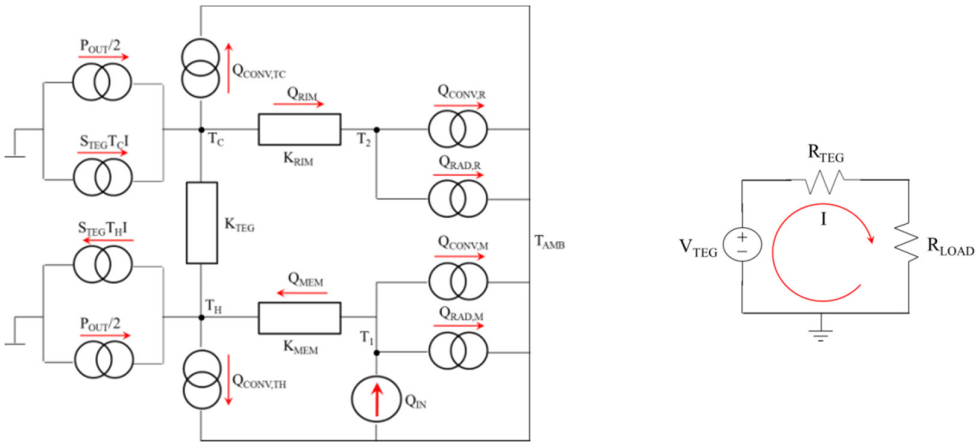
$$I = \frac{V_{TEG}}{2R_{TEG}} = \frac{S_{TEG} \cdot \Delta T}{2R_{TEG}} \tag{4-10}$$

$$P_{OUT} = \frac{{V_{TEG}}^2}{4R_{TEG}} = \frac{(S_{TEG} \cdot \Delta T)^2}{4R_{TEG}} \tag{4-11}$$

Multiplying q_h in equation 4-1 by the surface area of the heated part of the membrane A_h then gives an approximation for the input power Q_{IN} as:

$$Q_{IN} = q_h A_h \tag{4-12}$$

To obtain the heat balance equations, refer to the thermal equivalent circuit of the TEG shown in Figure 4-8a. The corresponding Thevenin equivalent circuit is also shown in Figure 4-8b. In the thermal equivalent circuit, heat contributions due to Peltier effect ($S_{TEG}T_CI$ and $S_{TEG}T_HI$) and Joule heating ($P_{OUT}/2$) in the generator are included. K_{MEM} is the thermal conductance between the thermocouples and the heat absorber, K_{RIM} is the thermal conductance between the thermocouples and the rim, and I is the electric current flowing through the thermocouples. Q_{CONV}'s and Q_{RAD}'s in the thermal model represent heat losses due to convection and radiation, respectively, at different areas of the device.



(a) (b)

Figure 4-8: (a) Thermal equivalent circuit and (b) Thevenin equivalent circuit of solar TEG. (de Leon, Chong, and Kraft 2012)

Referring to each temperature node in Figure 4-8a, the heat balance equations are:

at T_1: $$Q_{IN} = Q_{MEM} + Q_{RAD,M} + Q_{CONV,M} \tag{4-13}$$

at T_H: $$Q_{MEM} = K_{TEG}(T_H - T_C) + S_{TEG}T_H I - \frac{1}{2}P_{OUT} + Q_{CONV,TH} \tag{4-14}$$

at T_C: $$Q_{RIM} = K_{TEG}(T_H - T_C) + S_{TEG}T_C I + \frac{1}{2}P_{OUT} - Q_{CONV,TC} \tag{4-15}$$

at T_2: $$Q_{RIM} = Q_{RAD,R} + Q_{CONV,R} \tag{4-16}$$

Expressing heat losses due to convection and radiation as functions of geometry and temperature gives:

$$Q_{CONV,M} = h_{conv}A_{MEM}(T_1 - T_{AMB}) \tag{4-17}$$

$$Q_{CONV,R} = h_{conv}A_{RIM}(T_2 - T_{AMB}) \tag{4-18}$$

$$Q_{CONV,TH} = h_{conv}A_{TEG}(T_H - T_{AMB}) \tag{4-19}$$

$$Q_{CONV,TC} = h_{conv}A_{TEG}(T_C - T_{AMB}) \tag{4-20}$$

$$Q_{RAD,M} = \varepsilon\sigma A_{MEM}\left({T_1}^4 - {T_{AMB}}^4\right) \tag{4-21}$$

$$Q_{RAD,R} = \varepsilon\sigma A_{RIM}\left(T_2{}^4 - T_{AMB}{}^4\right) \tag{4-22}$$

where A_{MEM}, A_{RIM}, and A_{TEG} refer to the surface areas of the membrane, rim, and thermoelements, respectively; ε is the surface emissivity; σ is the Stefan-Boltzmann constant; h_{conv} is the convective heat transfer coefficient. Free convection in air would have h_{conv} values between 5-50 W/m^{2}K while forced convection in air would have h_{conv} values between 25-250 W/m^{2}K (Welty et al. 2008).

Considering heat flow through K_{MEM} and K_{RIM}, equations for T_H and T_C in terms of T_1 and T_2, respectively, can be derived.

$$T_H = T_1 - {}^{Q_{MEM}}/_{K_{MEM}} \tag{4-23}$$

$$T_C = T_2 + {}^{Q_{RIM}}/_{K_{RIM}} \tag{4-24}$$

The temperature difference between the hot and cold sides of the thermocouples is also defined as:

$$\Delta T = T_H - T_C \tag{4-25}$$

Incorporating equations 4-17 to 4-25 into the heat balance equations in equations 4-13 to 4-16, the following expressions are derived:

$$Q_{IN} = Q_{MEM} + \varepsilon\sigma A_{MEM}\left(T_1{}^4 - T_{AMB}{}^4\right) + h_{conv}A_{MEM}(T_1 - T_{AMB}) \tag{4-26}$$

$$Q_{MEM} = K_{TEG}\Delta T + S_{TEG}\left(T_1 - \frac{Q_{MEM}}{K_{MEM}}\right)I - \frac{1}{2}P_{OUT} + h_{conv}A_{TEG}\left(T_1 - \frac{Q_{MEM}}{K_{MEM}} - T_{AMB}\right) \tag{4-27}$$

$$Q_{RIM} = K_{TEG}\Delta T + S_{TEG}\left(T_2 + \frac{Q_{RIM}}{K_{RIM}}\right)I + \frac{1}{2}P_{OUT} - h_{conv}A_{TEG}\left(T_2 + \frac{Q_{RIM}}{K_{RIM}} - T_{AMB}\right) \tag{4-28}$$

$$Q_{RIM} = \varepsilon\sigma A_{RIM}\left(T_2{}^4 - T_{AMB}{}^4\right) + h_{conv}A_{RIM}(T_2 - T_{AMB}) \tag{4-29}$$

Referring back to the thermal equivalent circuit in Figure 4-8a, the temperature difference T_1 and T_2 between can be expressed as:

$$T_1 - T_2 = \frac{Q_{MEM}}{K_{MEM}} + \Delta T + \frac{Q_{RIM}}{K_{RIM}} \tag{4-30}$$

In equations 4-27 and 4-28, the current I and output power P_{OUT} can be expressed in terms of ΔT using equations 4-10 and 4-11, respectively. Hence, combining equations 4-26 and 4-27 gives a fourth-order polynomial in T_1 with only T_1 and ΔT as unknown variables.

$$\varepsilon\sigma A_{MEM}{T_1}^4 + \left(S_{TEG}I + h_{conv}(A_{TEG} + A_{MEM})\right)T_1 + C_1 = 0 \tag{4-31}$$

where

$$\begin{aligned} C_1 = {} & K_{TEG}\Delta T - S_{TEG}\frac{Q_{MEM}}{K_{MEM}}I - \frac{1}{2}P_{OUT} - \varepsilon\sigma A_{MEM}{T_{AMB}}^4 \\ & - h_{conv}\left(\frac{Q_{MEM}}{K_{MEM}}A_{TEG} + (A_{TEG} + A_{MEM})T_{AMB}\right) - Q_{IN} \end{aligned} \tag{4-32}$$

By using Ferrari's solution to a quartic function[1] in solving the roots of equation 4-31, four expressions for T_1 as functions of ΔT can be derived. By plugging in a positive value for ΔT and calculating the roots, the expression that gives a real and positive value for T_1 is selected. Similarly, equations 4-28 and 4-29 can be combined to form the following fourth-order polynomial equation:

$$\varepsilon\sigma A_{RIM}{T_2}^4 + (h_{conv}(A_{TEG} + A_{RIM}) - S_{TEG}I)T_2 + C_2 = 0 \tag{4-33}$$

where

$$\begin{aligned} C_2 = {} & -K_{TEG}\Delta T - S_{TEG}\frac{Q_{RIM}}{K_{RIM}}I - \frac{1}{2}P_{OUT} - \varepsilon\sigma A_{RIM}{T_{AMB}}^4 \\ & + h_{conv}\left(\frac{Q_{RIM}}{K_{RIM}}A_{TEG} - (A_{RIM} + A_{TEG})T_{AMB}\right) \end{aligned} \tag{4-34}$$

The roots of equation 4-33 can then be solved and T_2 can be expressed in terms of ΔT. The derived equations for T_1 and T_2 can then be substituted into equation 4-30, which gives an equation with only ΔT as the unknown variable. The temperature difference across the thermoelements, ΔT, can then be solved numerically using Matlab. The Matlab program used to solve for ΔT can be found in Appendix A.

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[1] Weisstein, Eric W. "Quartic Equation." From MathWorld--A Wolfram Web Resource. http://mathworld.wolfram.com/QuarticEquation.html

Once ΔT is determined, the open-circuit output voltage and matched output power can be calculated using equations 4-9 and 4-11, respectively. Moreover, recalling from section 2.1.5, the Carnot efficiency η_C, TEG efficiency η_{TEG}, and TEG efficiency factor Φ can then be calculated as follows:

$$\eta_C = \frac{T_H - T_C}{T_H} \tag{4-35}$$

$$\eta_{TEG} = \eta_C \cdot \frac{\sqrt{1 + Z\bar{T}} - 1}{\sqrt{1 + Z\bar{T}} + (T_C/T_H)} \tag{4-36}$$

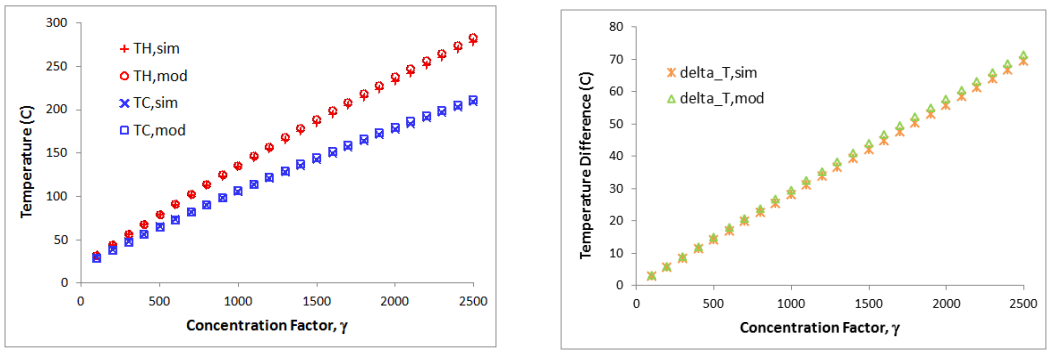
$$\Phi = \frac{P_{OUT}}{A_G \cdot {\Delta T_{TEG}}^2} \tag{4-37}$$

Using the electrical and thermal properties of p-type silicon and aluminum listed in Table 4-2 for a TEG with the following thermoleg dimensions: $l = 200$ µm, $w = 15$ µm, and $t = 5$ µm; assuming that there are 488 thermocouples, the membrane diameter d_{mem} is 7 mm, $\gamma = 100$, and $h_{conv} = 50$ W/m^{2}K, the following performance parameters of the TEG are obtained: $\Delta T_{TEG} = 117$ K, $V_O = 21.5$ V, $P_{OUT} = 1.78$ mW, $\eta_C = 8.163\%$, $\eta_{TEG} = 0.023\%$, and $\phi = 0.1298$ µW/cm^{2}K^2. The computed TEG efficiency factor is higher than in all the published lateral/lateral TEGs listed in Table 2-1.

4.5 Simulations vs. Thermal Model

Figure 4-9a shows a comparison of the hot and cold side temperatures obtained from simulations and from the thermal model discussed in the previous section. Looking at these graphs, it can be seen that there is good agreement between temperatures obtained from COMSOL finite element analysis heat transfer simulations and temperatures derived from analytical thermal modelling based on energy balance and heat transfer equations using lumped thermal conductances. Looking at Figure 4-9b, it can be observed that the temperature difference from the thermal model is slightly higher than that of the simulations. The gap in the temperature difference between simulations and model slightly increases as the concentration factor increases. At a concentration factor of 2500,

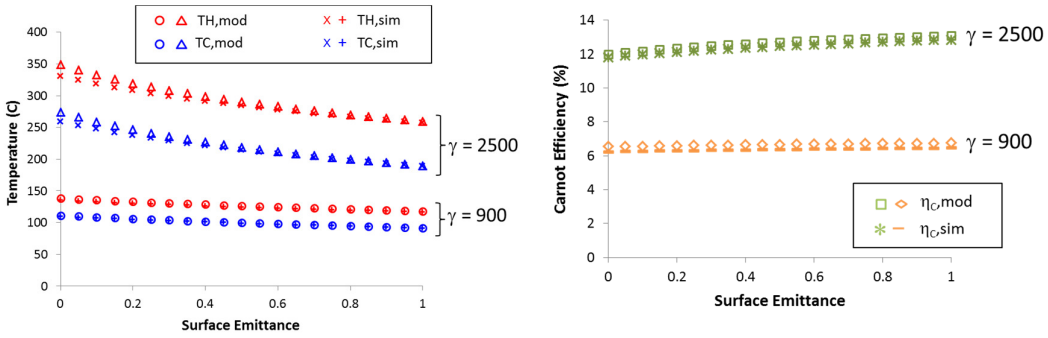
the temperature difference of the thermal model is 2.7 ° C higher than that of the simulation. This can be attributed to the assumption in the model that the thermoelectric properties of the material are constant with temperature.



(a) (b)

Figure 4-9: Comparison between simulations (*sim*) and thermal model (*mod*) with varying solar concentration ratio for (a) hot (T_H) and cold (T_C) side temperatures and (b) temperature difference ΔT. TEG has the following parameters: $l = 500$ µm, $w = 30$ µm, $d_{mem} = 3$ mm, $N = 81$, $\varepsilon = 0.6$, $h_{conv} = 25$ W/m^{2}K, $\tau_{lens} = 0.9$, $\alpha_{mem} = 0.5$, and $d_{spot} = 1$ mm.

Next, the effect of the surface emittance on the hot and cold side temperatures of the TEG is investigated. This is shown in Figure 4-10a. The emissivity of a material is the relative ability of its surface to emit energy by radiation. As the surface emittance is increased, the hot side temperature decreases; leading to a slight increase in the TEG Carnot efficiency as shown in Figure 4-10b.



(a) (b)

Figure 4-10: Effect of surface emittance on (a) hot and cold side temperatures, and (b) Carnot efficiency at different concentration ratios. TEG parameters: $l = 500$ µm, $w = 30$ µm, $d_{mem} = 3$ mm, $N = 81$, $h_{conv} = 25$ W/m^{2}K, $\tau_{lens} = 0.9$, $\alpha_{mem} = 0.5$, and $d_{spot} = 1$ mm.

Figure 4-11a shows the effect of convective heat flux on the hot and cold side temperatures of the TEG. It can be seen that for convective heat flux greater than 20 W/m^{2}K, simulation results agree well with that of the thermal model; whereas for convective heat flux less than 20 W/m^{2}K, temperatures obtained from simulations are lower than those derived from the thermal model. This signifies that the thermal model developed is effective for convective heat flux greater than 20 W/m^{2}K. It can also be observed that as the convective heat transfer coefficient is increased, the hot side temperature decreases. From Figure 4-11b, it can be observed that the temperature difference across the device also decreases with increasing convective heat flux. Given that the Carnot efficiency is the ratio of the temperature difference to the hot side temperature, it can be inferred that the rate of decrease of the hot side temperature is faster than the rate of decrease of the temperature difference, leading to an increase in the TEG Carnot efficiency as the convective heat flux is increased. This trend in Carnot efficiency is shown in Figure 4-11c.

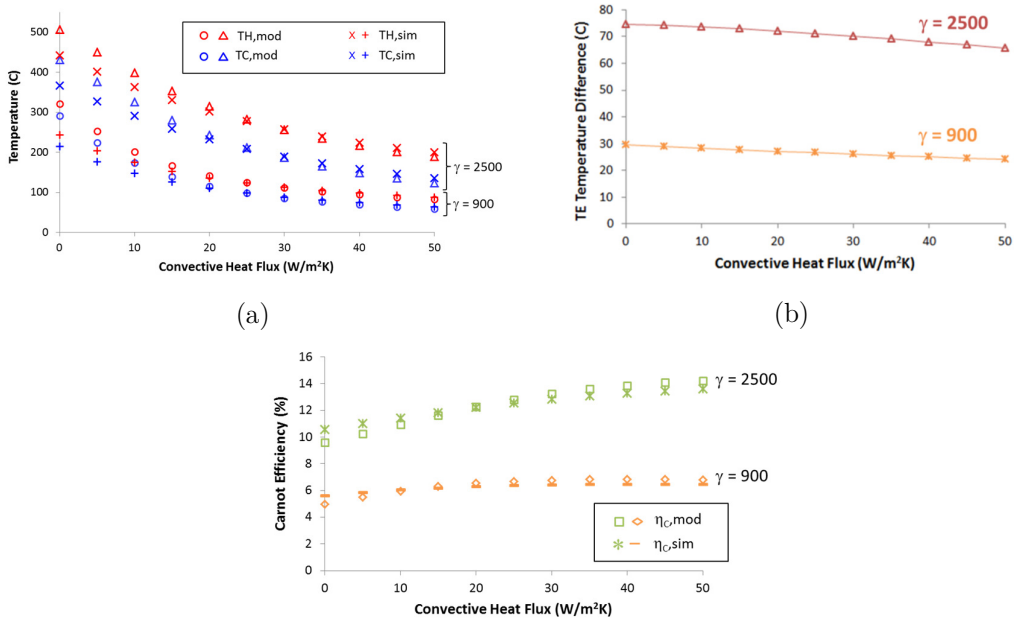
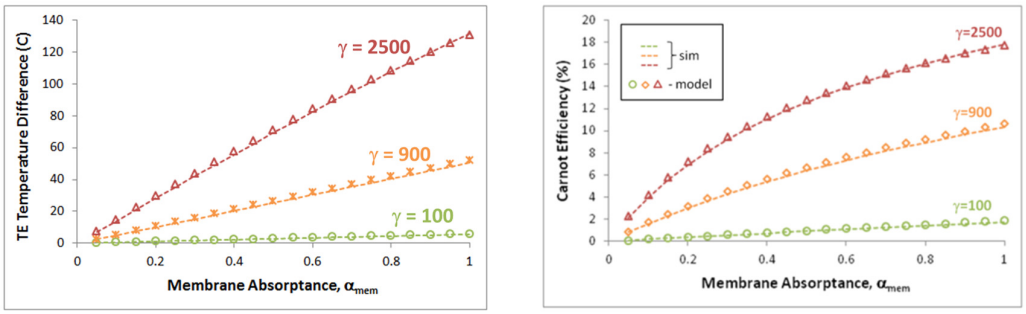


Figure 4-11: Effect of convective heat flux on (a) hot and cold side temperatures, (b) temperature difference and (c) Carnot efficiency at different concentration ratios. TEG parameters: $l = 500$ µm, $w = 30$ µm, $d_{mem} = 3$ mm, $N = 81$, $\varepsilon = 0.6$, $\tau_{lens} = 0.9$, $\alpha_{mem} = 0.5$, and $d_{spot} = 1$ mm.

Lastly, the effect of the membrane absorptance on the temperature difference of the TEG is investigated. This is shown in Figure 4-12a. As the absorptance of the membrane is increased, the temperature difference increases leading to an increase in the TEG Carnot efficiency as shown in Figure 4-12b. This indicates that aside from increasing the concentration ratio, the efficiency of the system can also be improved by improving membrane absorptance. This can be done by coating the surface with a high absorptance material such as graphite (Tomeš et al. 2010) and laser-treated aluminum (Hwang, Vorobyev, and Guo 2011).



(a) (b)

Figure 4-12: Effect of membrane absorptance on (a) TEG temperature difference and (b) Carnot efficiency and for different concentration ratios. TEG parameters: $l = 500$ μm, $w = 30$ μm, $d_{mem} = 3$ mm, $N = 81$, $h_{conv} = 25$ W/m^{2}K, $\varepsilon = 0.6$, $\tau_{lens} = 0.9$, and $d_{spot} = 1$ mm.

Table 4-3 lists performance parameters of TEGs with different geometries derived using the thermal model developed in this study. By focusing solar radiation onto the membrane of a TEG with a 1 mm diameter spot size, Carnot efficiencies of up to 29% can be achieved with a concentration factor of 900. The best efficiency factor of 0.249 is also higher than those listed in Table 2-1.

Table 4-3: Performance parameters derived using the thermal model for various geometries. In all cases, γ= 900, τ_{ens}=90%, α_{mem}=50%, , h_{conv} = 25 W/m^{2}K, ε = 0.6, and solar radiation is concentrated on the TEG membrane with d_{spot} = 1mm.

l (μm)	w (μm)	d_{mem} (mm)	N	ΔT	V_{TEG} (V)	η_C (%)	η_{TEG} (%)	Φ (μW/cm²K²)
200	15	1	31	70.14	0.82	15.4	0.064	0.041
500	15	1	34	156.24	2.00	29.0	0.14	0.018
200	15	3	108	16.50	0.67	4.2	0.015	0.143
500	15	3	111	38.35	1.60	9.4	0.035	0.059
500	20	3	91	35.22	1.21	8.7	0.032	0.064
500	30	3	81	26.61	0.81	6.7	0.025	0.086
1000	15	3	114	68.84	2.96	15.7	0.063	0.030
200	15	5	188	6.49	0.46	1.8	0.0059	0.249
500	15	5	188	15.31	1.08	4.1	0.014	0.099
1000	15	5	191	27.18	1.95	7.1	0.025	0.051

4.6 Conclusions

In this chapter, the design of the proposed solar-driven TEG was presented. Experiments involving commercially-available components verified that using a lens to concentrate solar radiation onto a Peltier device results in an increase in the output voltage, which can only be attributed to a larger temperature difference across the device. Heat transfer simulations that were performed also confirmed that increasing the proportion of the lens surface area to the heated area of the TEG membrane leads to an improvement in the device's Carnot efficiency. The analytical model of the solar-driven TEG based on energy balance and heat transfer equations showed good agreement with simulation results, making the thermal model suitable for characterizing solar TEG performance. With the proposed design, TEG efficiency factors greater than that of published lateral/lateral μTEGs can be achieved.

Chapter 5: TEG Design and Proposed Fabrication

In this chapter, details on the design of the TEG are reported. Several design considerations are presented and the dimensions of the TEGs to be fabricated are given. Then, the TEG layouts are shown and structures included in the wafer to aid in characterizing the thermocouple materials are also discussed. Lastly, the proposed TEG fabrication procedure is presented, where two methods explored in refilling isolation trenches are discussed. Lastly, the problems encountered in the fabrication process are described, which led the researchers to explore alternative means of fabricating TEGs that are presented in Chapters 6 and 7.

5.1 TEG Design

Based on the heat transfer simulations presented in section 4.3, a SOI-based TEG design has optimum heat transfer when the membrane and thermoelements are fully suspended, i.e. the buried oxide and handle layers under the membrane and thermoelements are completely etched. As such, the configuration of the proposed TEG is as shown in Figure 5-1. This design is similar to the one in (Egbert, Harvey, and Otis 2007) where the SOI wafer's device layer is utilized for the suspended membrane and thermoelements. The membrane acts as the heat absorber of the TEG while the substrate acts as the heat sink. The suspended membrane is circular in geometry to insure optimum transfer of heat from the center of the membrane to the tip of the thermoelements. The oxide and substrate layers below the membrane and the thermoelements are to be etched away to provide better thermal isolation and to optimize the heat flux path so as to obtain the largest temperature difference across the device.

The thermocouple materials are heavily-doped p-type silicon and aluminum. Heavily-doped silicon is seen to be a viable choice for thermoelement material since it has high Seebeck coefficients at doping levels between $3.5\text{x}10^{19}$ cm^{-3} to $1.6\text{x}10^{20}$ cm^{-3} (Salleh et al.

2009)(Ikeda and Salleh 2010). A high doping level is also preferred because the electrical resistivity of silicon decreases with increasing dopant concentration; thus providing a smaller series electrical resistance to the TEG device. It is preferred that both thermoelements use doped silicon but to minimize the number of masks needed during fabrication, aluminum is selected for the second thermoelement instead. Furthermore, it was decided to utilize the device layer of the SOI wafer for the p-type silicon thermoelements. In this regard, isolation trenches have to be added into the design in order to electrically isolate the thermoelements from the membrane and rim of the TEG.

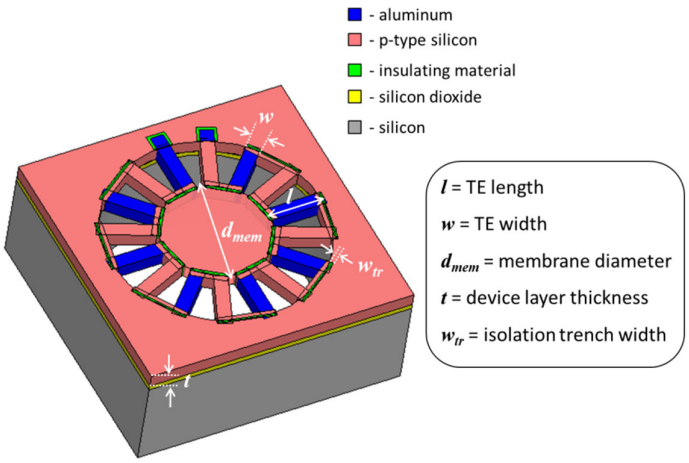


Figure 5-1: TEG design with the SOI device layer as one of the thermoelements. Design parameters based on the geometry of the device are also indicated.

After settling on the TEG design with fully suspended membrane and thermoelements, design parameters that can be investigated in this work were identified. These design parameters are annotated in Figure 5-1. The design space essentially includes the dimensions (length, width, and height) of the thermoelements, the diameter of the membrane, and the width of the isolation trenches.

Using the thermal model developed in section 4.4, the temperature, voltage, and power trends of the TEG with respect to its dimensions are examined. Higher efficiencies can be achieved by using TEGs with longer lengths and narrower widths. However, the mechanical stability of the TEG after etching out the oxide and substrate layers must also be considered. It is targeted to fabricate different geometries of the device to explore this tradeoff. Characterizations of these variations are exhibited in Figure 5-2 to Figure

5-4. In these plots, the thickness of the device layer is assumed to be 5 µm to be consistent with the device layer thickness of the SOI wafer to be used during fabrication. The electrical and thermal properties of the thermoelectric materials used for these plots are the ones listed in Table 4-2.

Figure 5-2 shows the effects of varying thermoelement length. As can be seen from Figure 5-2a, the hot side temperature increases with thermoelement length whereas the cold side temperature do not vary significantly. This translates to the temperature difference across the device also increasing with the thermoelement length as shown in Figure 5-2b. This is expected since TEGs with longer thermolegs have a lower thermal conductance. Correspondingly, the open-circuit output voltage and matched output power shown in Figure 5-2c and Figure 5-2d, respectively, also shows an increasing trend with increasing thermoelement length.

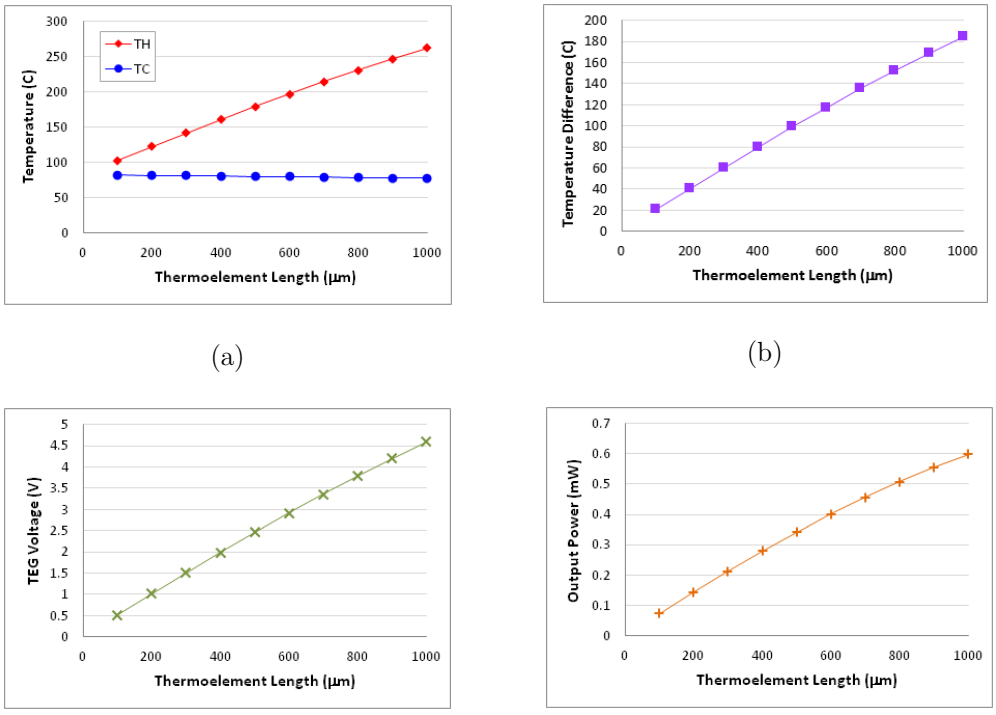


Figure 5-2: (a) Hot and cold side temperatures, (b) Temperature difference, (c) open circuit TEG voltage, and (d) output power to a matched load for different thermoelement lengths ($w = 15$ µm, $d_{mem} = 1$ mm, and $N = 66$). Parameters derived from the thermal model with $\gamma = 1000$, $h_{conv} = 50$ W/m^{2}K, $\alpha_{mem} = 0.5$, and $\tau_{lens} = 1$.

Figure 5-3 shows the effects of varying thermoelement width. A wider thermoelement would have lesser number of thermocouples for the same membrane diameter. Since the thermal conductance of the TEG varies linearly with both the thermoelement width and the number of thermocouples, then the TEG thermal conductance is not expected to vary significantly. This is verified by the hot and cold side temperatures, and the temperature difference shown in Figure 5-3a and Figure 5-3b, respectively, where the values do not change significantly with increasing thermoelement width. Figure 5-3c shows that the open-circuit TEG voltage decreases with increasing thermoelement width. This is a result of the decreasing number of thermocouples. However, the matched output power as shown in Figure 5-3d also do not show significant changes with thermoelement width. The supposed reduction in output power due to the drop in the output voltage is offset by the lower series resistance of wider thermoelements, showing minimal variations of the output power to a matched load.

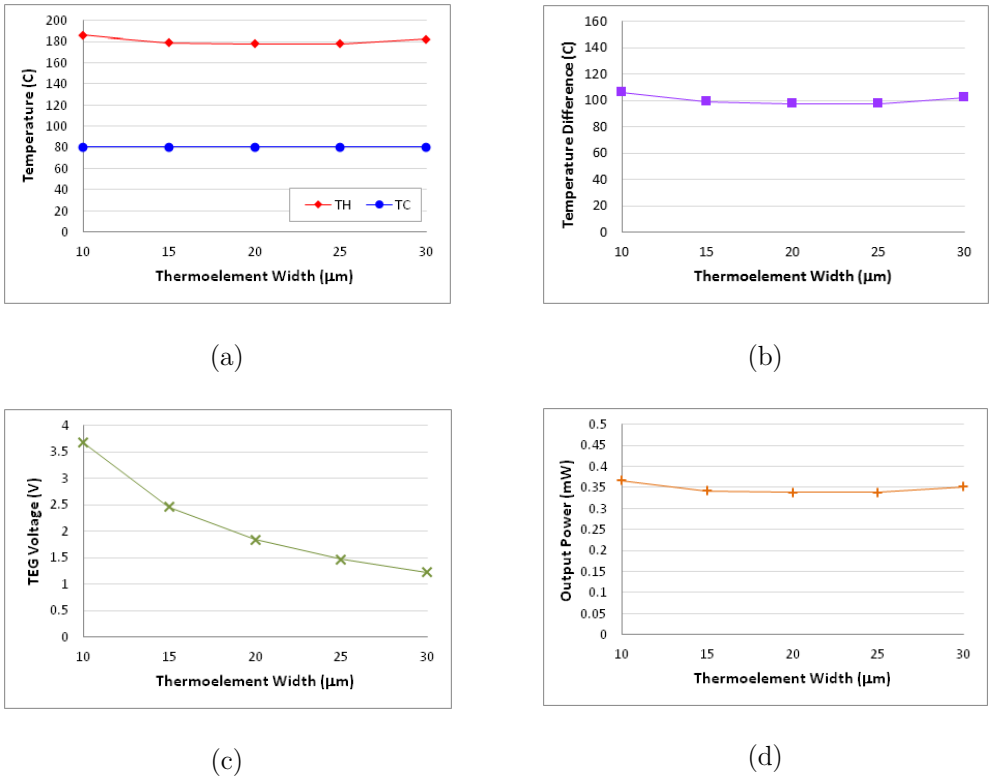


Figure 5-3: (a) Hot and cold side temperatures, (b) Temperature difference, (c) open circuit TEG voltage, and (d) output power to a matched load for different thermoelement lengths (l = 500 µm and d_{mem} = 1 mm). Parameters derived from the thermal model with γ= 1000, h_{conv} = 50 W/m^{2}K, α_{mem} = 0.5, and τ_{lens} = 1.

Figure 5-4 shows the effects of varying the membrane diameter. Changing the membrane diameter also means a change in the number of thermocouples of the device. A smaller membrane diameter implies lesser number of thermocouples. Figure 5-4a shows that both the hot and cold side temperatures of the device decreases with increasing membrane diameter. Because of the increase in the number of thermocouples, the thermal conductance of the TEG increases with increasing membrane diameter. As the thermal conductance increases, it is expected that the temperatures would also decrease. This is also evident in the temperature difference plot in Figure 5-4b. The open-circuit voltage of the TEG as shown in Figure 5-4c shows a decreasing trend as the membrane diameter is increased. This implies that the decrease in temperature difference affects the output voltage more than the increase in the number of thermocouples. The matched output power shown in Figure 5-4d shows a decreasing trend as the membrane diameter is increased. This is attributed to both the decrease in voltage and increase in electrical resistance of the TEG as the membrane diameter is increased.

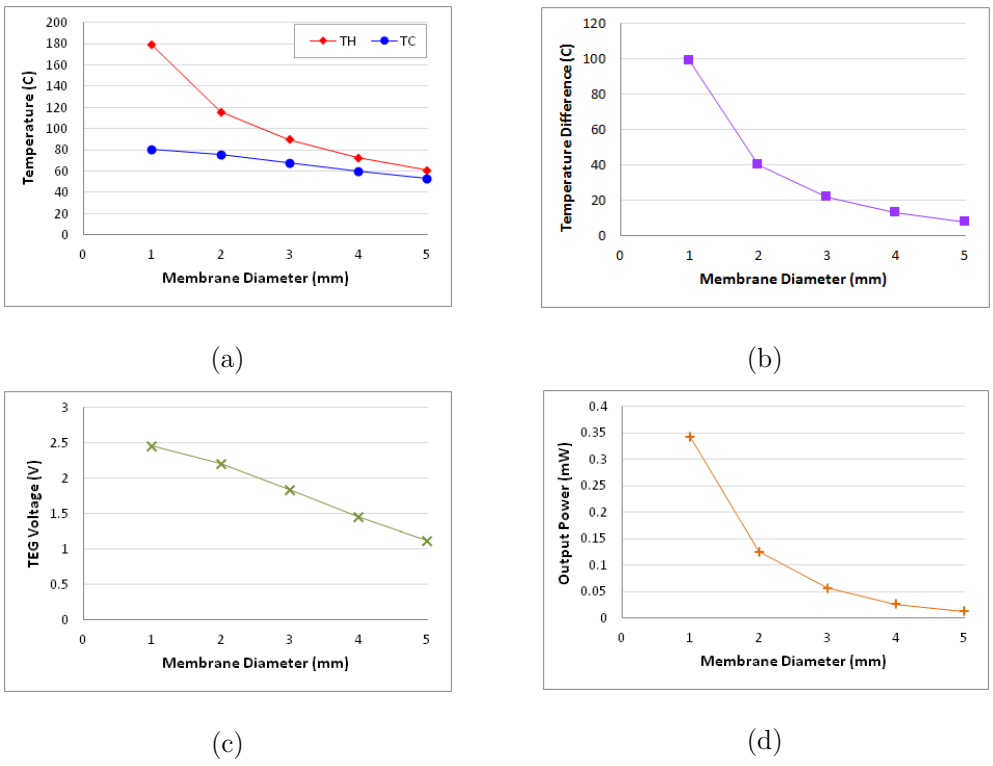


Figure 5-4: (a) Hot and cold side temperatures, (b) Temperature difference, (c) open circuit TEG voltage, and (d) output power to a matched load for different thermoelement lengths ($l = 500$ µm and $w = 15$ µm). Parameters derived from the thermal model with $\gamma = 1000$, $h_{conv} = 50$ W/m^{2}K, $\alpha_{mem} = 0.5$, and $\tau_{lens} = 1$.

Based on the characterization curves previously discussed, the dimensions of the TEGs to be fabricated are decided. It is desirable for the lengths of the thermoelements to be long so as to achieve a larger temperature difference across the device. However, longer thermoelements can be mechanically unstable once suspended. As such, the lengths are varied from 100 μm to 500 μm at increments of 100 μm, with two additional lengths set at 750 μm and 1 mm.

With regards to the thermoelement width, narrower thermoelements are ideal for a larger open-circuit voltage across the device. However, a tradeoff in mechanical stability also exists with narrow thermoelements. In this regard, the thermoelement widths are varied from 10 μm to 30 μm at 5 μm increments to properly characterize effects of width variations on the electrical, thermal, and mechanical properties of the TEG.

The membrane diameter also plays a crucial part in the overall performance of the TEG. Based on the characterization curves, it is desirable to have a smaller membrane diameter so as to have a higher temperature difference across the device. The area of the suspended membrane must also be kept small to achieve good mechanical stability (Korvink and Paul 2006). However, it will be more difficult to focus solar light onto a device with a smaller membrane. Hence, the membrane diameter is varied from 1 mm to 5 mm at 1 mm increments, with an additional implementation at 7 mm. The 7 mm diameter is set to be the largest implementation since each TEG chip is to have a dimension of 10×10 mm^2.

Lastly, the width of the isolation trenches is mainly constrained by the minimum feature size achievable by optical lithography. In this regard, it is decided to implement TEGs with 1 μm, 2 μm, and 3 μm wide trenches. The number of thermocouples (N) for each TEG is determined from the leg width, membrane diameter, and setting a gap between thermoelements of at least 5 μm.

Table 5-1 lists the dimensions of the TEGs proposed for fabrication. Most of the TEGs have membranes with 1 mm diameter as this dimension has already been proven to be mechanically stable in literature (Schenk et al. 2001).

Table 5-1: Dimensions of TEGs proposed for fabrication grouped according to width of isolation trenches.

TEGs with $w_{tr} = 1$ µm			
l (µm)	w (µm)	d_{mem} (mm)	N
100	15	1	66
200	15	1	66
300	15	1	66
400	15	1	66
500	15	1	66
750	15	1	66
1000	15	1	66
200	10	1	88
200	20	1	51
200	25	1	44
200	30	1	34
200	15	2	138
200	15	3	213
200	15	4	288
200	15	5	348
200	15	7	488
500	15	3	213
500	15	5	348
500	15	7	488
1000	15	3	213
1000	15	5	348
1000	15	7	488

TEGs with $w_{tr} = 2$ µm			
l (µm)	w (µm)	d_{mem} (mm)	N
200	15	1	41
500	15	1	41
200	15	3	141
500	15	3	141
500	20	3	116
500	30	3	94
1000	15	3	141
200	15	5	241
500	15	5	241
1000	15	5	241

TEGs with $w_{tr} = 3$ µm			
l (µm)	w (µm)	d_{mem}	N
200	15	1	31
500	15	1	34
200	15	3	108
500	15	3	111
500	20	3	91
500	30	3	81
1000	15	3	114
200	15	5	188
500	15	5	188
1000	15	5	191

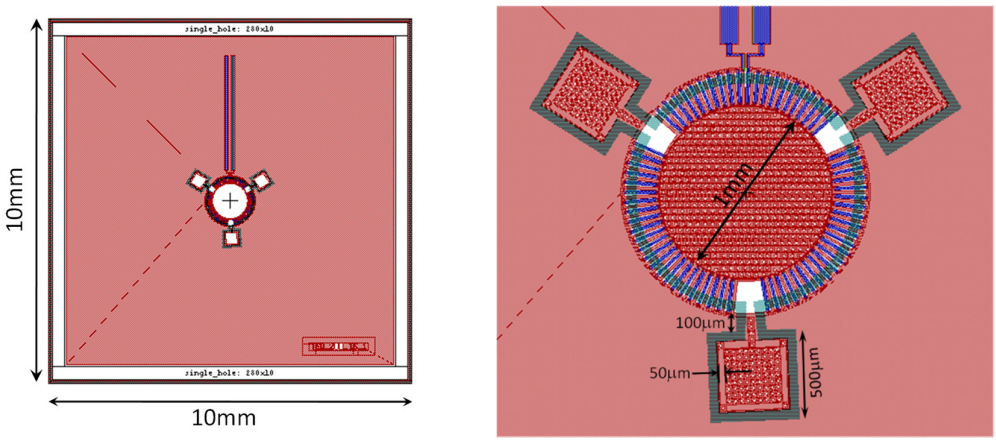
The expected TEG performance parameters for the above TEG dimensions are calculated using the analytical model discussed in section 4.4 and can be found in Appendix B for reference.

5.2 TEG Layout Implementation

After establishing the dimensions of the TEGs to be fabricated, layout of the TEGs can commence. This section discusses details on the TEG layout, as well as layouts of other structures necessary to determine the electrical and thermal properties of the thermoelectric materials used.

5.2.1 TEG Layout

Figure 5-5 shows the whole layout of a 10mm x 10mm TEG device. In this particular layout, the membrane has a diameter of 1mm and the dimensions of each thermoelement leg are as follows: length = 200µm and width = 15µm. Note that release holes are also patterned on the membrane and on part of the rim to aid in etching the buried oxide layer.

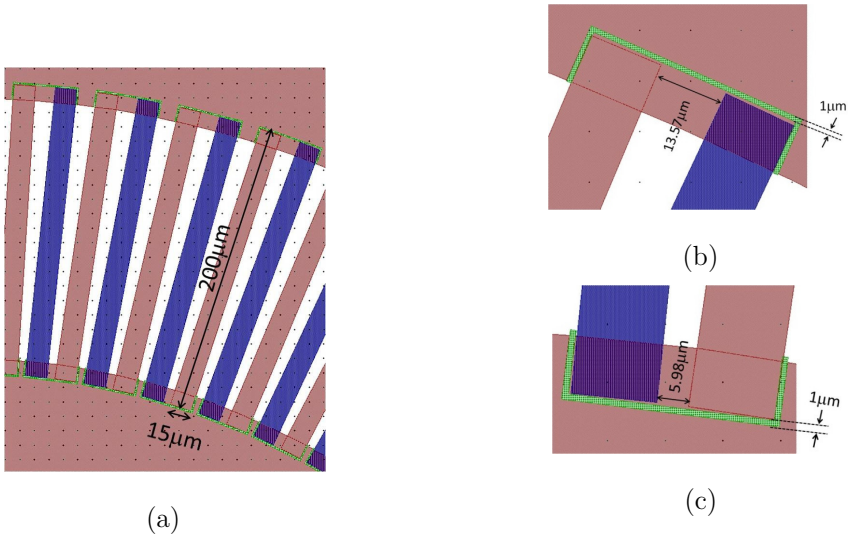


(a) (b)

Figure 5-5: (a) whole TEG layout and (b) zoomed-in layout of TEG with l = 200 µm, w = 15 µm, and d_{mem} = 1 mm.

Figure 5-6 shows more details on the dimensions of the TEG. To determine the number of thermocouples that can fit around the circumference of the membrane, a minimum gap of 5 µm is set between thermoelements. Then, calculations are made to arrive at the maximum number of thermocouples that gives reasonable and exact decimals for the inter-thermoelement angles. In the case of a 1 mm diameter membrane with 200×15 µm^2 thermoelement legs, the maximum number of thermocouples is computed to be 75, giving

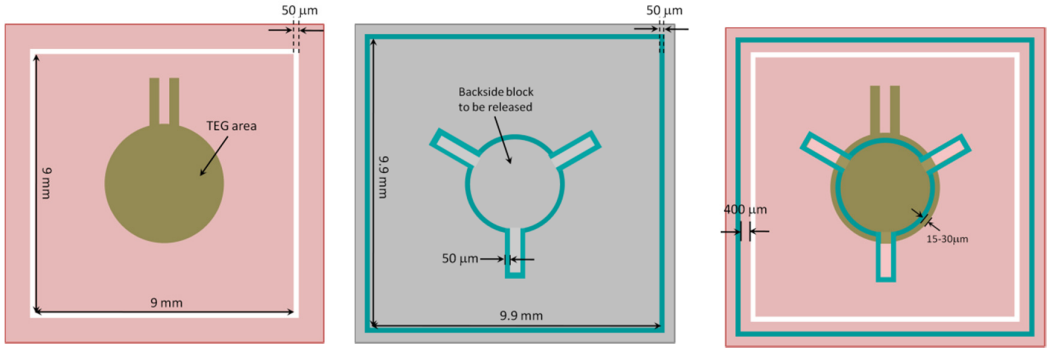
an angle of 2.4˚ between thermoelements. Note that for this example, the isolation trenches are 1 µm wide.



(a) (b) (c)

Figure 5-6: (a) TEG legs, (b) outer trench, and (c) inner trench.

As previously mentioned, it is important to release the membrane and thermoelements from the buried oxide and handle layers so as to maximize the temperature difference across the thermocouples. To realize this, 50 µm wide backside trenches are patterned in such a way that dicing-free release of both membrane and chip from the wafer can be done simultaneously as described in (Sari, Zeimpekis, and Kraft 2010). An illustration of this technique is shown in Figure 5-7. The outline of the TEG device area and frontside trenches are shown in Figure 5-7a. Meanwhile, Figure 5-7b shows the inner backside trench which defines the block of the handle layer underneath the membrane and thermoelements that is to be released. The outer backside trench, along with the frontside trench, defines the chip border and is used for separating each chip from the wafer. As shown in Figure 5-7c, the frontside and backside trenches defining the chip border have an offset of 400 µm from each other as recommended in (Sari, Zeimpekis, and Kraft 2010). It can also be seen from Figure 5-7c that the backside block to be released has an offset of 15-30 µm from the edge of the TEG area. This distance is set to be 15 µm for TEGs with 1 µm wide isolation trenches; 20 µm for TEGs with 2 µm wide isolation trenches; and 30 µm for TEGs with 3 µm wide isolation trenches. Assuming



(a) (b) (c)

Figure 5-7: (a) Frontside showing TEG device area and 50 µm wide front trenches, (b) Backside showing block to be released and 50 µm wide back trenches, and (c) Front and back trenches 400 µm apart.

that the backside silicon etching recipe would yield a negatively-tapered sidewall having an angle between 1-2 ° and that the handle layer is 550 µm thick, the inner backside trench should be 10-20 µm away from the TEG edge. To account for possible mismatches in lithography, this distance is set to 15-30 µm instead.

The dimensions of the pads and the routing wires are given in Figure 5-8. Note that the pads are 100 µm wide and extends up to the edge of the chip as shown in Figure 5-5a. This offers flexibility in bonding the TEGs to a chip carrier or to other devices during testing.

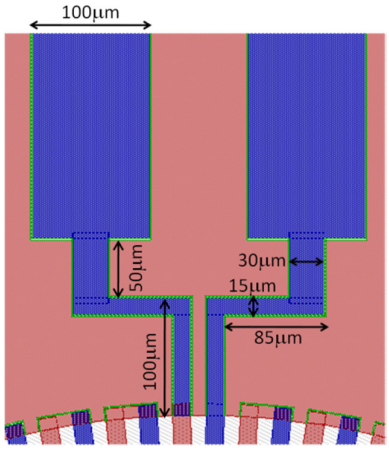


Figure 5-8: Close-up view of pads and wires. Trenches surrounding pads and wires are 1 µm wide.

Figure 5-9 shows the four layers of a TEG layout, corresponding to four masks required for fabrication. Mask 1 is for frontside patterning, which includes the rim, membrane, p-type silicon thermoelements, and frontside border trench. Mask 2 defines the isolation trenches and mask 3 defines the aluminum thermoelements, wires and pads. Lastly, mask 4 is for backside trench patterning.

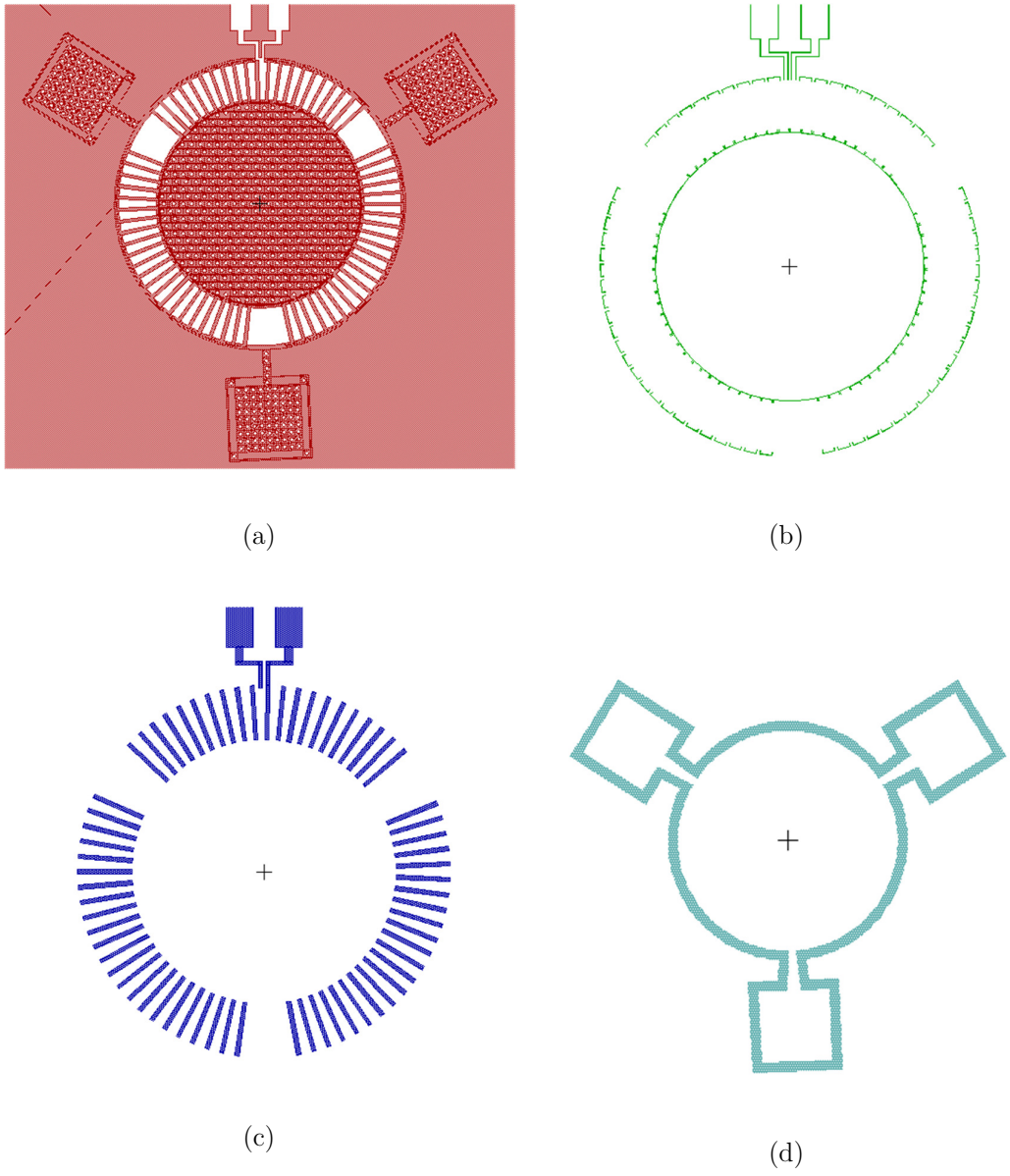


Figure 5-9: (a) Mask 1 for frontside patterning of membrane and silicon thermoelements, (b) Mask 2 for isolation trenches, (c) Mask 3 for aluminum thermoelements, and (d) Mask 4 for backside trenches.

The layout of the 6 inch wafer consisting of the thermoelectric generators to be fabricated is presented in Appendix C.

5.2.2 Auxiliary Layouts

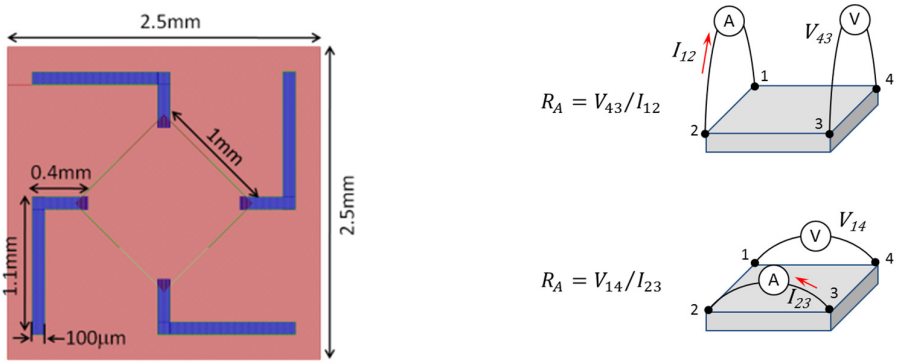
To properly characterize the TEG, the electrical and thermal properties of the thermoelectric materials used must be determined. To do this experimentally, several structures are also implemented. The Van der Pauw structures are to be used to determine the electrical resistivity of the thermocouple materials; the planar structures are to be used to determine the Seebeck coefficients; the cantilever structures are to be used to determine the thermal conductivity of the thermocouple materials; and the Kelvin structure are to be used to determine the contact resistance. The design of these structures is based on the test structures in (Xie et al. 2009) for polysilicon films used as thermoelectric material in a CMOS-MEMS thermoelectric power generator.

The Van der Pauw structure to be used for determining the electrical resistivity of silicon is shown in Figure 5-10a, annotated with dimensions. The Van der Pauw technique is widely used in research and industry to determine the resistivity of uniform samples. In this technique, one uses an arbitrarily-shaped sample containing four small contacts placed on the corners of the plate. The schematic of the structure is shown in Figure 5-10b. To calculate the resistivity of the material, the sheet resistance R_S must be determined. Van der Pauw demonstrated that there are actually two characteristic resistances R_A and R_B associated with the corresponding terminals shown in Figure 5-10b. These resistances are related to the sheet resistance through the van der Pauw equation:

$$\exp(-\pi R_A/R_S) + \exp(-\pi R_B/R_S) = 1 \tag{5-1}$$

Once R_S is solved numerically, the bulk electrical resistivity can be calculated using $\rho = R_S t$, where t is the thickness of the film.

The planar structure to be used for determining the Seebeck coefficient of silicon is shown in Figure 5-11. A silicon strip with a length of 500 μm and a width of 30 μm is



(a) (b)

Figure 5-10: (a) Van der Pauw structure to measure electrical resistivity and (b) Van der Pauw schematic.

connected to aluminum at its two ends (pads 5 and 6). A 110 µm × 20 µm silicon heater (pads 11 and 12) is positioned 20 µm away from the hot contact of the silicon strip. The aluminum contacts at the ends of the silicon strip also act as temperature monitors and are in four-point measurement configurations (pads 1, 2, 3, 4 and pads 7, 8, 9, 10) to enable tracking of small temperature variations by measuring small resistance changes.

When current is applied to the heating resistor, the temperature of the hot and cold contacts increases from T_0 to T_h and T_c, respectively. These changes in temperature are determined using the temperature-dependent resistance of the temperature monitors. The Seebeck coefficient is then calculated from the expression:

$$\alpha|_{\frac{T_h+T_c}{2}} = \frac{U}{T_h - T_c} = \frac{U}{\Delta T} \tag{5-2}$$

where U is the thermovoltage between the two ends of the silicon strip.

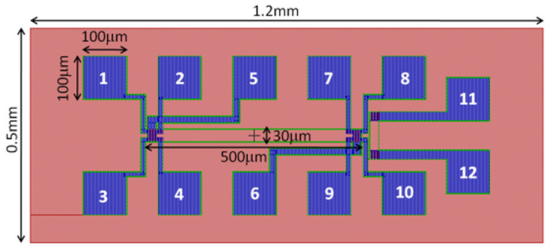


Figure 5-11: Planar structure to measure Seebeck coefficient.

The cantilever structure to be used for determining the thermal conductivity of silicon is shown in Figure 5-12a. The 300 µm x 100 µm cantilever is suspended over a cavity with two aluminum contacts (pads 5 and 6) to measure the thermally generated voltage. Two silicon resistors are integrated into the hot tip of the cantilever. The 92 µm × 20 µm resistor (pads 1 and 2) close to the end of the beam is used as a heater. The other resistor (pads 3 and 4) is used as a temperature monitor, with a total length of 250 µm and a width of 20 µm. When a power P is dissipated in the heater, the temperature of the hot tip of the cantilever is increased by ΔT. The overall thermal conductance of the structure can then be calculated as equal to $^{P}/_{\Delta T}$. The etch holes are present in the structure to allow etching of the buried oxide layer, thereby suspending the cantilever.

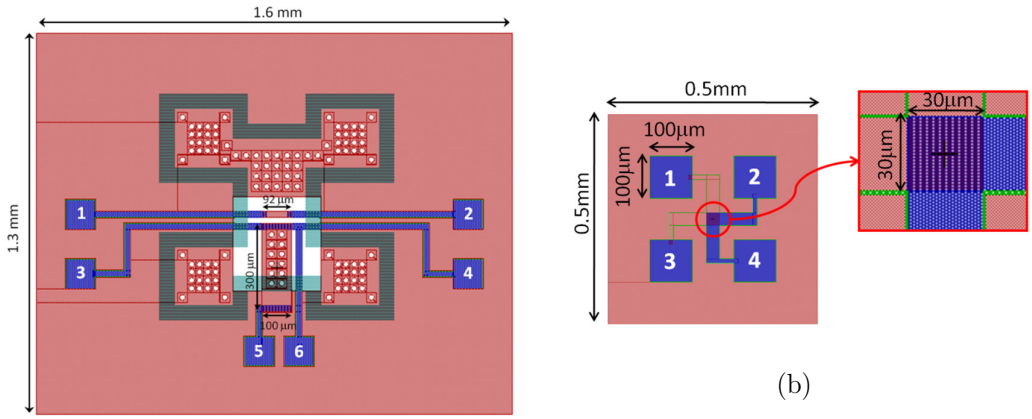


Figure 5-12: (a) Cantilever structure to measure thermal conductivity and (b) Kelvin structure to measure contact resistance..

The Kelvin structure to be used for measuring contact resistance is shown in Figure 5-12b. By forcing a current between pads 1 and 4 and measuring the voltage across pads 2 and 3, the contact resistance can be determined from the following equation:

$$R_C = (V_2 - V_3)/I_{14} \tag{5-3}$$

5.3 Proposed TEG Fabrication Process

The proposed TEG fabrication process involves the use of a SOI wafer with a device layer that has been pre-doped to have the desired resistivity of the silicon

thermoelements. To electrically isolate the membrane and the rim from the thermocouples, isolation trenches have to be added into the TEG design. Typically, trenches are used to electrically isolate MEMS structures with each other and from other CMOS circuits when everything is implemented on a single chip (Zhu et al. 2005). The usual process to fabricate an isolation trench is by employing DRIE to etch out silicon trenches on a SOI wafer and successively refilling these trenches with a dielectric material. These isolation trenches can be refilled by SiO_2 (Lo, Huang, and Zhang 1995)(Lin et al. 1999), Si_3N_4 (Sarajlic et al. 2003)(Gokirmak and Silva 2007) or polysilicon (Qingping et al. 1998) (Li et al. 2004). They can also be refilled by a combination of dielectric materials such as SiO_2 and undoped polysilicon (Ayazi et al. 2000)(Bashir et al. 2001)(Schenk et al. 2001)(Zhang et al. 2001)(Brosnihan et al. 2003)(Clavelier et al. 2003) (DePestel et al. 2003)(Yan et al. 2004)(Zhu et al. 2005)(Wu & Fang 2006)(Juang et al. 2008) or Si_3N_4 and undoped polysilicon (Brosnihan et al. 1997)(Bellew, Hollar, and Pister 2003)(O'Brien and Monk 2007). A more novel way of refilling these isolation trenches is by using polymers such as parylene C (Lei et al. 2009) or BenzoCycloButene (Mahfoz-Kotb et al. 2009). Isolation trenches have also been used to enable independent excitation of two different potentials on a movable frame of a 2D-scanner chip (Schenk et al. 2001). It is worthwhile to note that in the 2D-scanner chips developed in (Schenk et al. 2001), the suspended mirror has dimensions up to 1.5 mm×1.5 mm and mechanical tests performed on the chip show high mechanical stability of the filled isolation trench, considering that one anchor of the mirror is completely formed by filled trenches.

With the potential of incorporating isolation trenches into the TEG design, the fabrication process is then developed. An illustration of the proposed TEG fabrication process is shown in Figure 5-13. Fabrication starts by RCA cleaning of the SOI wafer. The next step is patterning of silicon thermoelements by RIE. In this step, sections of the device layer to be occupied by the isolation trenches and aluminum thermoelements are also etched out. The next step is deposition and etching of dielectric material to fill the isolation trenches. Similarly, deposition through e-beam evaporation and liftoff of aluminum follow to form the aluminum thermoelements and the electrical connections of

the thermocouples. The next step is back etching of the substrate under the membrane and thermoelements by DRIE. Finally, the membrane and thermoelements are released by HF vapor etching.

To optimize the heat flow path, the oxide layer under the membrane and thermoelements are to be etched out as well. Oxide etching may also be performed by HF vapor phase. In this case, etch holes on the membrane should be included in the first DRIE process and the isolation trenches must be filled with an insulator other than oxide or if oxide is to be used, it must be capped with another dielectric material that is more resistant to HF vapor etching.

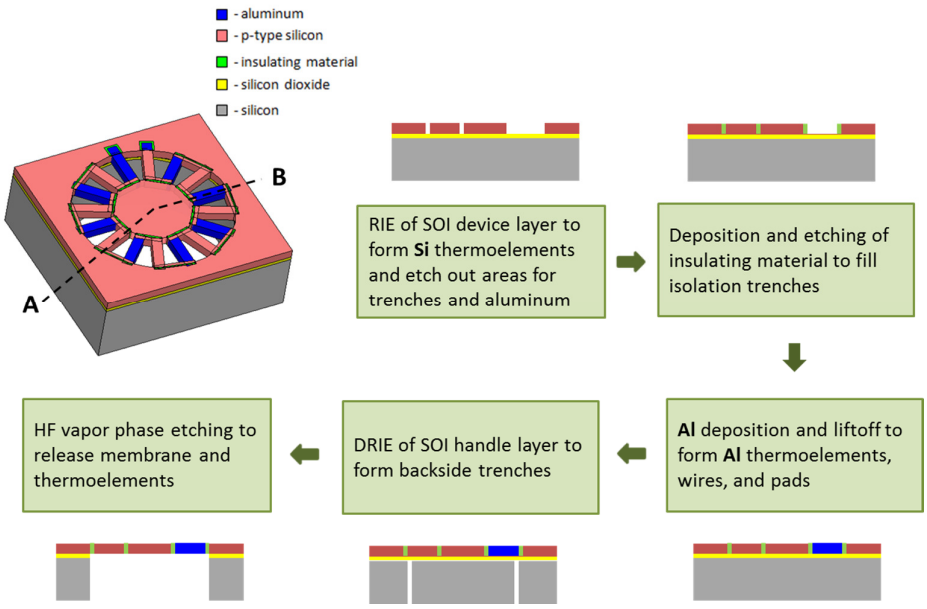


Figure 5-13: Proposed TEG fabrication process using a SOI wafer with a doped device layer. Cross-sectional view is along AB.

To facilitate discussion, this section is divided into the six major steps of the fabrication process which are:

1) Hardmask patterning of both front and back sides.
2) Frontside RIE.
3) Refilling of isolation trenches.
4) Aluminum deposition and lift-off.
5) Backside DRIE.

6) HF vapor phase etching.

The process starts with acquiring a 6 inch SOI wafer from Ultrasil Corporation with the following thicknesses: 530 ± 25 μm handle layer, 2 μm ± 5% buried oxide layer, and 5 ± 0.5 μm device layer. The handle layer is boron-doped with a resistivity greater than 1000 Ω-cm while the device layer is also boron-doped and has a resistivity less than 0.001 Ω-cm.

For a more detailed illustration of the proposed device fabrication on a SOI wafer, the reader is referred to Appendix D.

5.3.1 Hardmask Patterning of Front and Back Sides

To protect the device layer during backside patterning, an oxide hardmask was patterned at the frontside. For this hardmask, a 1 μm thick SiO_2 based on silane (SiH_4) was deposited by using an OIPT SYS100 capacitive-based PECVD reactor. The gas flow rates of silane-based oxide were 4.2 sccm SiH_4, 350 sccm N_2O, and 80 sccm N_2. The deposition was performed at a table temperature of 350 ° C, chamber pressure of 1000 mTorr, and RF power of 20 W. The deposition rate was about 1 nm/s.

Initially, the frontside SiO_2 hardmask was patterned first; then the backside was patterned with photoresist and etched by DRIE. However, a vacuum error with the spinner occurred in subsequent steps that require photoresist spinning. At this point, it was decided to use a hardmask at the backside as well and perform backside DRIE at the latter part of the fabrication process. Hence, after deposition of 1 μm SiO_2 at the frontside, the wafer was immediately rinsed in isopropyl alcohol (IPA) and blow-dried using a N_2 gun. Then, a 3.6 μm thick silane-based SiO2 was deposited at the backside.

After coating both front and back sides with PECVD oxide, the wafer was cleaned in fuming nitric acid (FNA) for 10 minutes, followed by 3 quick dump rinse (QDR) cycles. Then, the wafer was spin-dried using an automated spin rinse dryer. After drying, the wafer was dehydrated in a 120 ° C oven for 30 minutes in preparation for frontside lithography.

Lithography at the frontside starts with spinning TI Prime[2], which is an adhesion promoter that improves photoresist adhesion on the silicon substrate. TI Prime was spun using a Brewer Science Spin Coater at 3000 rpm for 20 seconds. Then, the wafer was baked on a hotplate at 120 ˚C for 2 minutes. The wafer was then immediately spin-coated with a 6 µm thick AZ9260 positive photoresist with spin settings as depicted in Figure 5-14. After spinning, the photoresist was soft-baked at 110 ˚C for 2 minutes and 30 seconds. Then, the wafer was allowed to rehydrate for 30 minutes before exposing in vacuum contact for 10 seconds at a UV broadband intensity of 20 mW/cm^2 using an EVG620TB mask aligner. After which, the photoresist was developed in 1:3 AZ400K:H_2O solution for 2 minutes and 30 seconds, rinsed in deionised (DI) water, and blow-dried using a N_2 gun . At this point, the photoresist is patterned with the first mask, which defines the areas for the p-type silicon thermoelements, the rim, and the perforated membrane.

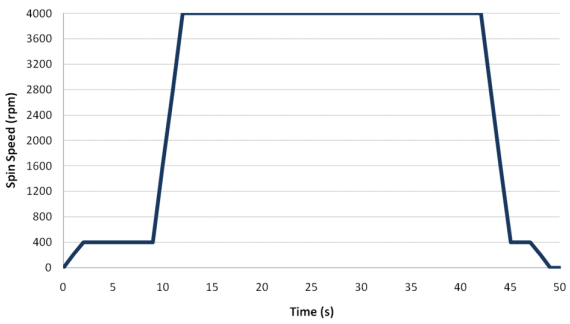


Figure 5-14: Spin settings for a target 6 µm thick AZ9260 photoresist.

After lithography, the wafer was placed inside the chamber of an OIPT SYS380 inductively-coupled plasma (ICP) etcher for SiO_2 etching. The gases used for this purpose were 37.4 sccm CHF_3, 34 sccm C_4F_8, and 8.5 sccm O_2. Etching was done at a table temperature of 15 ˚C, chamber pressure of 7 mTorr, RF power of 100 W, and ICP power of 1500W. To avoid the photoresist from burning, helium was introduced into the chamber at a pressure of 10 T to cool down the wafer. The SiO_2 etch rate was approximately 150 nm/min and its selectivity to AZ9260 was about 1:1. Note that the

[2] http://microchemicals.com/micro/ti_prime.pdf

buried oxide layer of the SOI wafer can act as a thermal insulator so it is important to do etching in short intervals (about 4-5 minutes at a time) and allow a few minutes for the wafer to cool down before proceeding with another etching run.

Once the exposed PECVD oxide was completely etched, the photoresist was stripped in O_2 plasma using a Tepla 300 asher and once again, FNA-cleaned in preparation for the second lithography step. Similar to the first lithography step, the wafer was first dehydrated in a 120 $^\circ$C oven for 30 minutes. Then, the same procedure of photoresist spinning, exposure, and development was performed on the SOI backside. The PECVD SiO_2 at the backside was also etched in an ICP etcher to form the backside trenches and once completely etched, the photoresist was stripped in O_2 plasma. Figure 5-15 summarizes the process of patterning the front and back hardmasks previously discussed. Additionally, Figure 5-16 shows optical micrographs of both frontside and backside hardmasks.

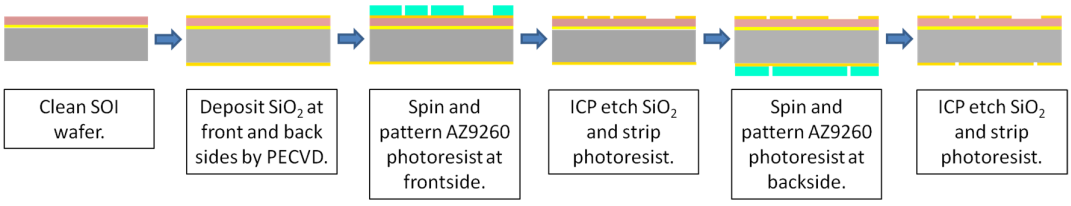
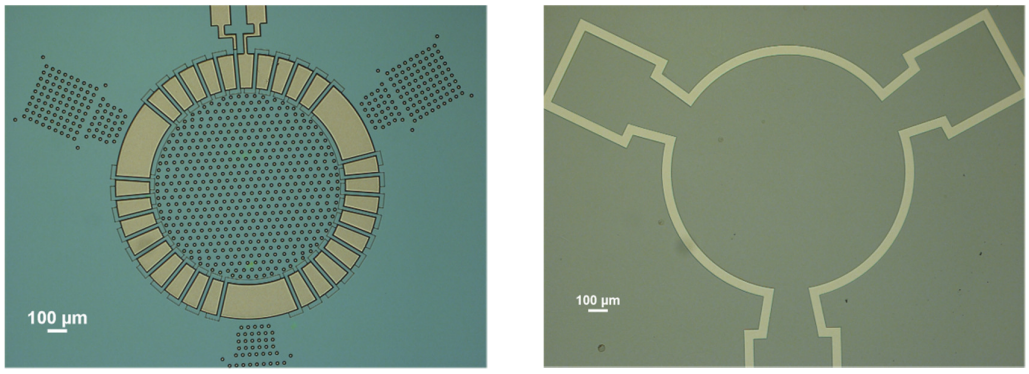


Figure 5-15: Process of patterning hardmasks for both front and back sides of the SOI wafer.



(a) (b)

Figure 5-16: Optical micrographs of (a) frontside and (b) backside hardmasks.

5.3.2 Frontside RIE

Once the front and back hardmasks were patterned, the exposed silicon device layer was etched up to the buried oxide layer using the OIPT reactive ion etch (RIE) tool. The RIE conditions for this process were: 18 sccm SF_6, 22 sccm O_2, table temperature of 20 ° C, chamber pressure of 30 mTorr, and RF power of 100 W. Under these settings, the silicon etch rate was 280 nm/min whereas the SiO_2 etch rate was 33 nm/min, making it an appropriate masking material with a selectivity of about 8.5. The sidewalls were also slightly positiviely-tapered as shown in Figure 5-17 to aid in the refilling of the isolation trenches, which is crucial in the next fabrication step.

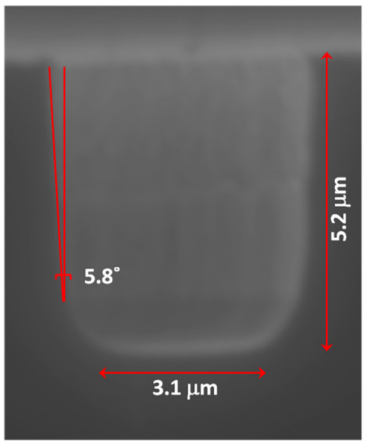


Figure 5-17: SEM image of a 3 µm wide isolation trench after 1100 seconds of frontside RIE.

5.3.3 Refilling of Isolation Trenches

After frontside RIE, the wafer was FNA-cleaned to make certain that there are no unwanted particles on the surface of the wafer prior to the succeeding deposition process. As previously discussed, the isolation trenches have to be refilled with a dielectric material. Since the TEG is envisioned to have temperature differences of more than 300 ° C, the dielectric material should be able to withstand temperatures of up to at least 350 ° C. Hence, two ways of refilling the isolation trenches are explored: (1) using PECVD SiO_2 capped with PECVD Si_xN_y and (2) lining the trench with polysilicon and filling with a spin-on dielectric.

5.3.3.1 Refilling with PECVD SiO2 capped with PECVD Si_xN_y

Both silicon dioxide and silicon nitride have good adhesion to silicon and have excellent insulating properties. Silicon dioxide can be deposited by PECVD using either silane gas precursor or tetra-ethyl-ortho-silicate (TEOS) liquid precursor. In gas-phase SiO_2 deposition, SiH_4 is diluted in N_2 and reacted with nitrous oxide. In TEOS-based SiO_2 deposition, the liquid precursor is transported to the reaction chamber with inert argon gas and is reacted with oxygen. Between the two PECVD methods, TEOS-based SiO_2 tends to have better step coverage and results in a more conformal film deposition (Yu et al. 1990)(Foggiato 2002)(Chang et al. 2004)(Kim et al. 2004)(Archard et al. 2010). The step coverage and conformality of deposited films, as illustrated in Figure 5-18, are characterized by the sidewall step coverage, bottom step coverage, and cusping. For excellent trench filling, the film should ideally have 100% sidewall and bottom step coverage and cusping should be zero.

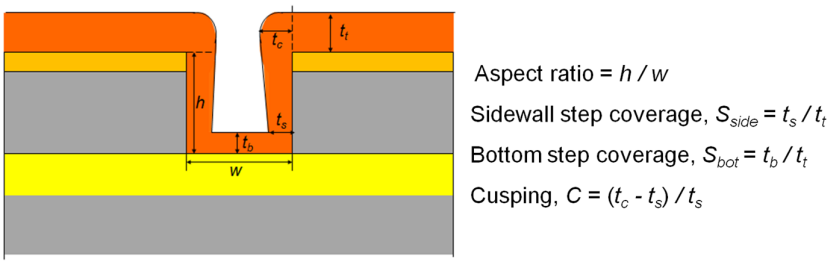


Figure 5-18: Parameters that characterize step coverage and conformality of deposited film.

Scanning electron microscope (SEM) images of trenches filled using the two methods of SiO_2 deposition by PECVD are shown in Figure 5-19. Two types of trenches are shown in the figure – a wide trench having an aspect ratio less than 1 and a narrow trench having an aspect ratio greater than 1. The thicknesses of the deposited films are measured by ellipsometry and verified by SEM imaging. Looking at Figure 5-19, it can be seen that depositing SiH_4-based SiO_2 further would result in voids in the trenches. In this regard, it was confirmed that TEOS-based SiO_2 has better gap filling characteristics between the two methods.

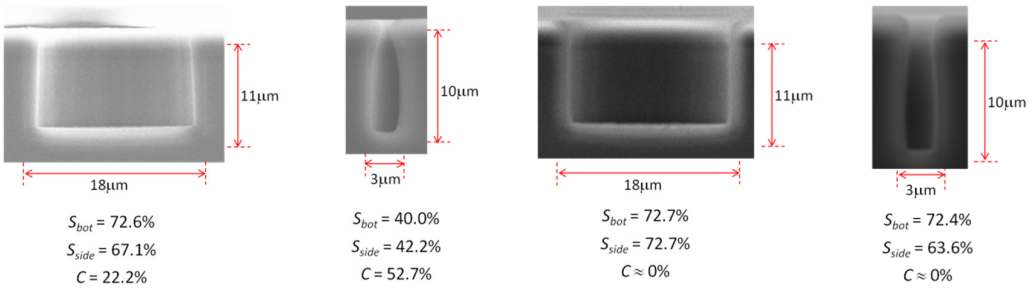


Figure 5-19: Step coverage of SiH_4-based SiO_2 for (a) wide and (b) narrow trenches; and TEOS-based SiO_2 for (c) wide and (d) narrow trenches.

After verifying that using TEOS is preferable for refilling trenches, the deposition of thicker films to fully cover the trenches with SiO_2 is investigated. A 2 µm thick TEOS-based SiO_2 film was successfully deposited with no problems. However, when depositing a 3 µm thick film, cracks occurred on the film as shown in Figure 5-20, which can only be attributed to the increasing internal stress of the film as thickness is increased (Bulla and Morimoto 1998)(Zhang et al. 2001). This problem can be alleviated by decreasing chamber pressure and/or using dual-frequency deposition (VanDeVen, Connick, and Harrus 1990).

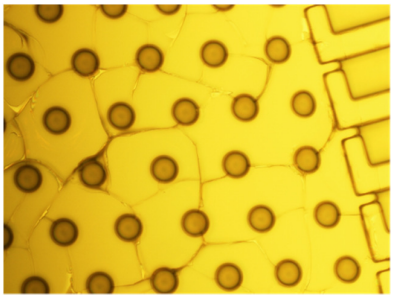


Figure 5-20: Cracks in 3 µm thick TEOS-based deposited SiO_2 film using standard PECVD recipe.

The standard and modified recipes for depositing TEOS-based silicon dioxide are listed in Table 5-2. To improve film stress, the chamber pressure was reduced and dual frequency deposition was utilized. In the modified recipe, a cycle of RF power applied for 12 s, followed by LF power for 8 s, was employed. These settings are consistent with those recommended by OIPT for improving film stress of TEOS oxide. With the modified recipe, it was possible to deposit good quality oxide films with thicknesses of up to 3 µm.

As the deposition time was increased to deposit thicker films, fractures at the edge of the wafers were observed as shown in Figure 5-21. Since no cracks were observed in the trench areas and the parts of the film where fractures are evident will eventually be etched out, it was decided to continue with the fabrication process using the modified TEOS-based SiO_2 recipe.

Table 5-2: Standard and modified recipes for TEOS-based SiO_2 deposition.

	O_2 (sccm)	**Ar (sccm)**	**Temp ($^\circ$C)**	**Pressure (mT)**	**P_{RF} (W)**	**P_{LF} (W)**	**Dep. Rate (nm/min)**
Standard recipe	500	50	350	1500	40	0	58
Modified recipe	500	50	350	500	40	40	30

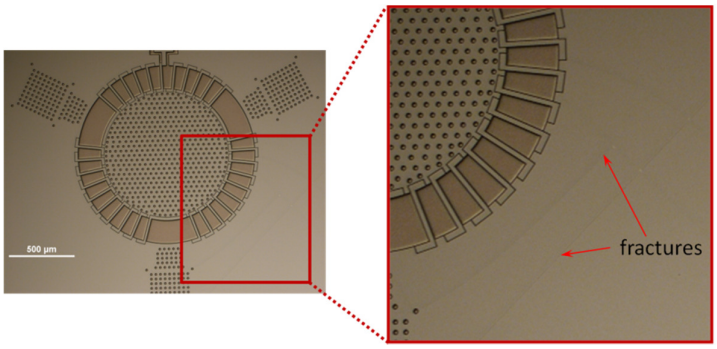


Figure 5-21: Fractures in 4 µm thick TEOS-based SiO_2 deposited using modified recipe.

Using the modified recipe for TEOS-based SiO_2 deposition, a 3.6 µm thick SiO_2 film on a wafer processed up to the frontside DRIE step was deposited. Once the thick oxide film was deposited, the wafer was FNA-cleaned and lithography of a 6 µm thick AZ9260 photoresist was carried out to pattern the isolation trenches. The TEOS-based oxide was then anisotropically etched with the ICP etcher using the same recipe discussed in section 5.3.1. Then, the photoresist was stripped in O_2 plasma using the Tepla 300 asher. A cross-section image of a refilled 3 µm wide trench is shown in Figure 5-22. The presence of a void in the refilled trench is still evident. This can be explained by the degradation in sidewall step coverage as the trench width decreases during deposition, which eventually results in the sealing of the trench. Although a void is still present,

dual-frequency TEOS deposition is chosen for refilling trenches because it not only has better step coverage than SiH_4-based SiO_2, internal film stress is also more controllable.

To protect the oxide from HF vapor etching to be performed later on in the fabrication process, the deposited oxide was capped with 360 nm thick silicon-rich silicon nitride deposited by PECVD. Stoichiometric silicon nitride can be easily etched by HF vapor etching (Bakke et al. 2005). However, changing the deposition parameters so as to obtain a silicon-rich nitride film can result in a suitable etch stop material for HF vapor etching (Chiaroni et al. 2004)(Tsau and Nunan 2010). In depositing a silicon-rich nitride film, the SiH_4 to NH_3 gas flow rates ratio was increased from 0.625 to 2. The deposition was performed at a table temperature of 350 ˚C and chamber pressure of 750 mTorr. Dual-frequency deposition was also utilized so as to lower down the absolute value of stress (Williams, Gupta, and Wasilik 2003). Hence, RF power of 20 W pulsed for 12 s and LF power of 40 W pulsed for 8 s were employed. Table 5-3 shows a comparison between stoichiometric Si_3N_4 and silicon-rich SiN films in terms of their deposition and etch parameters. ICP etching utilized 35 sccm SF_6 and 65 sccm C_4F_8 gas flow rates, table temperature of 20 ˚C, chamber pressure of 14m Torr, RF power of 80 W, and ICP power of 1500 W. Meanwhile, blanket etching in HF vapor phase was done at 40 ˚C for 20 minutes.

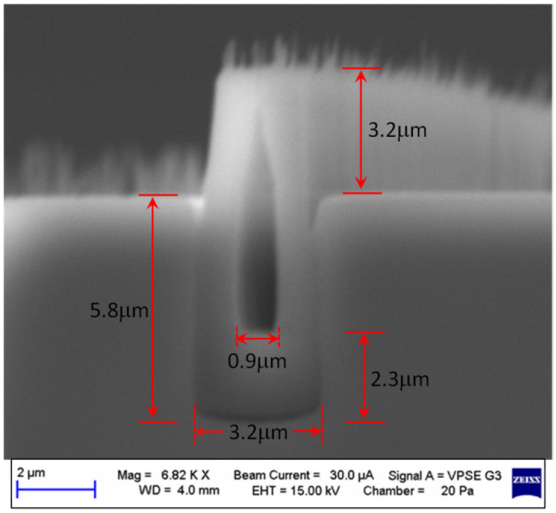


Figure 5-22: Trench filled with TEOS-based SiO_2 using dual-frequency deposition and then anisotropically etched using an ICP etcher.

Table 5-3: Comparison between deposition and etch parameters for stoichiometric Si_3N_4 and silicon-rich SiN films. N_2 gas flow rate is 500 sccm, table temperature is 350 ˚C, and chamber pressure is 750 mTorr.

	SiH_4 (sccm)	NH_3 (sccm)	P_{RF} (W)	P_{LF} (W)	Deposition rate (nm/min)	Refractive index	ICP etch rate (nm/min)	HF VPE etch rate (nm/min)
Stoichiometric Si_3N_4	12.5	20	20	0	12	2.03	280	26
Silicon-rich SiN	30	15	20	40	12.3	2.35	440	5.8

Once both oxide and nitride layers were deposited, the wafer was FNA-cleaned and lithography of a 6µm AZ9260 photoresist as discussed in section 5.3.1 was carried out. The photoresist was patterned such that the isolation trenches are protected from the following etching step. The SiN_x film was first ICP-etched using the SF_6 and C_4F_8 gases as discussed earlier in this section and then, SiO_2 was also anisotropically etched with the ICP etcher, utilizing the same recipe in etching PECVD SiO_2 hardmasks discussed in section 5.3.1. Once etching was completed, the photoresist was stripped in O_2 plasma in preparation for the next fabrication step. Figure 5-23 shows an optical image of one TEG device after SOI wafer processing up to this fabrication step.

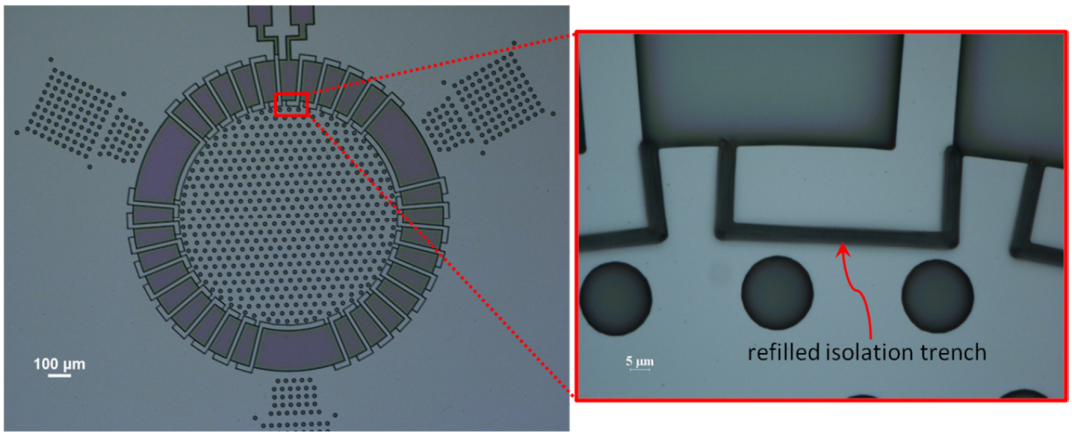


Figure 5-23: Optical micrograph of TEG on SOI wafer after refilling isolation trenches with TEOS-based SiO_2 capped with silicon-rich silicon nitride.

5.3.3.2 Refilling with hot-wire SiN, polysilicon, and spin-on dielectric

Another method in refilling isolation trenches also explored in this study is by lining the trenches with a thin layer of silicon nitride and intrinsic polysilicon. After which, the trenches are filled with SINR-3570[3], a spin-on dielectric based on novel siloxane chemistry from ShinEtsu MicroSi, Inc. The thin silicon nitride layer provides electrical insulation while the polysilicon layer acts as a protective layer for the SINR-3570. The step-by-step process of refilling isolation trenches in this manner is outlined in Figure 5-24.

As shown in Figure 5-24a, the isolation trenches were first lined with silicon nitride and intrinsic polysilicon deposited using hot-wire chemical vapor deposition (HWCVD). The HWCVD technique involves the decomposition of precursor gases by means of heating one or more metallic filaments (usually tungsten or tantalum) at 1600-2100 °C. The dissociated gas molecules are then deposited onto a heated substrate. The Nitor 301 tool from Echerkon Technologies, Ltd was used for HWCVD processing. Twenty-nine tungsten filaments with a diameter of 200 μm were heated at 2100 °C. For silicon nitride, the following deposition parameters were used: 9 sccm SiH_4, 90 sccm NH_3, 540 sccm H_2, with a chamber pressure of 0.065 mbar, and with the bottom heater set at 550 °C. The silicon nitride recipe was executed for 20 minutes, which resulted in a 180 nm thick highly conformal film; thus giving a deposition rate is 0.15 nm/s. For the intrinsic polysilicon, the following deposition parameters were used: 6 sccm SiH_4, 294 sccm H_2, with a chamber pressure of 0.024 mbar, and with both top and bottom heaters set at 550 °C. These conditions heat up the substrate to a temperature of 462 °C. The polysilicon recipe has a deposition rate of 0.1 nm/s and was performed for 3 hours, resulting in a film with thickness of about 1 μm.

[3] http://www.microsi.com/user/document/Photodefinable%20Materials%20for%20Advanced%20Packaging.pdf

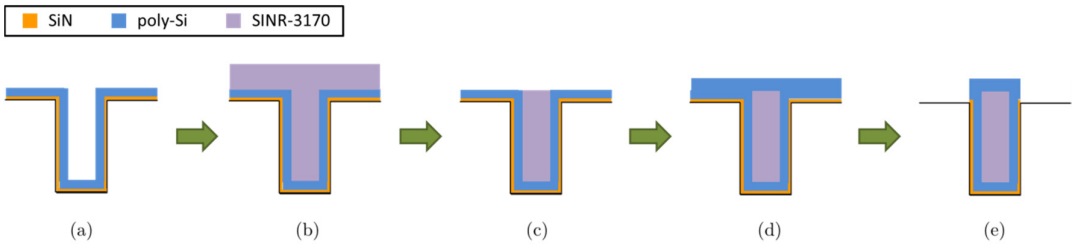


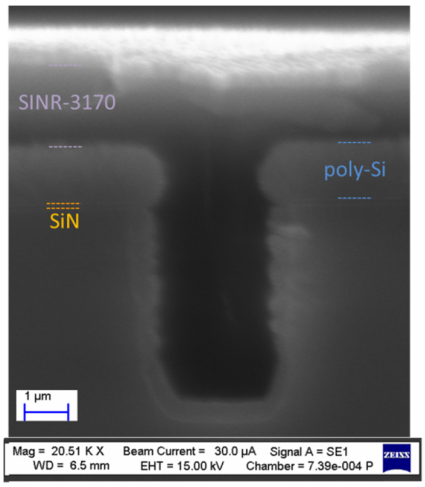
Figure 5-24: Second method of refilling isolation trenches: (a) Line trench with HWCVD silicon nitride and intrinsic polysilicon. (b) Spin coat with SINR-3570. (c) Dry etch SINR-3570. (d) Cap trench with HWCVD intrinsic polysilicon. (e) Dry etch intrinsic polysilicon and silicon nitride that are not part of isolation trenches.

After lining the trench with silicon nitride and polysilicon, two coatings of SINR-3570 was applied onto the wafer. In both cases, the Brewer Science Spin Coater was used with the lid open so as to reduce the pressure in the chamber and yield thicker films. The first coating spun SINR-3570 at 1100 rpm for 30 s, and then the wafer was baked at 90 ˚C for 2 mins. Then, the second coating was done by spinning SINR-3570 at 1000 rpm for 45 s and again baked at 90 ˚C for 2 mins. Then, the SINR-3570 film was exposed in flood exposure mode for 5 minutes using an EVG620TB mask aligner. A post-exposure bake at 120 ˚C for 2 mins was then performed and the wafer was soaked in IPA for 30 s, rinsed with DI water, and dried using a N_2 gun. Lastly, the film underwent curing at a temperature of 180 ˚C in N_2 ambient for 1 hour using an EVG520 bonder. The thickness of the SINR-3570 film after curing was 5.6 µm, measured from the top surface of the HWCVD polysilicon.

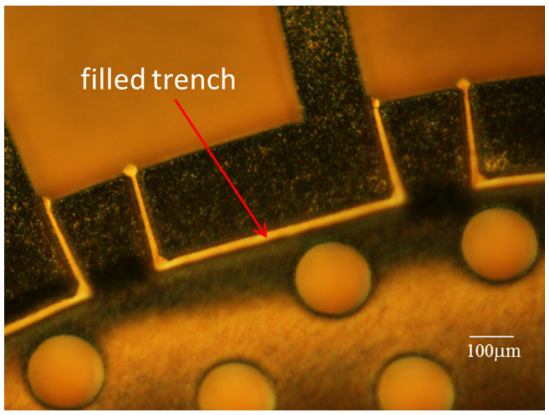
Once the SINR-3570 was cured, planarization was done by blanket etching SINR-3570 in an ICP etcher until the polysilicon layer was reached. This is shown in Figure 5-24c. The etching recipe involves 16 sccm CHF_3, 34 sccm Ar, table temperature of 15 ˚C, chamber pressure of 30 mTorr, RF power of 100 W, and ICP power of 1600W. The etch rate was about 200 nm/min and to make sure that the SINR-3570 does not burn during the etching process, etching steps were done 5 minutes at a time, after which the wafer was allowed to cool for a few minutes before doing another etching step. Figure 5-25a shows a SEM image of a 3 µm wide trench after 4 µm of planarization on the SINR-3570 film. A thin film of polysilicon was deposited on top for easier imaging since the SINR-3570 film is a non-conductive film and is subject to a build-up of electrons that causes scattering of

the electron beam. Figure 5-25b shown a photomicrograph of a filled trench after planarization. The roughness of HWCVD polysilicon is also evident on this figure.

After the SINR-3570 film was planarized, it was capped with another layer of HWCVD intrinsic polysilicon as shown in Figure 5-24d. Since the film was cured only at 180 ˚C, it is important to deposit the capping polysilicon at a temperature not exceeding 250 ˚C so as not to have significant mass loss of the dielectric film (J. Kim, Kim, and Paik 2011). To do this in the HWCVD tool, 75 µm diameter tungsten filaments were heated at 1850 ˚C and the heaters were not switched on. The resulting substrate temperature was 216 ˚C and the following deposition parameters were used for the capping polysilicon: 13 sccm SiH_4, 487 sccm H_2, and with a chamber pressure of 0.024 mbar, yielding a deposition rate of 0.15 nm/s. Deposition was done for 3 hours, giving a thickness of about 1.6 µm.



(a)



(b)

Figure 5-25: (a) SEM image of 3 µm wide trench after etching 4 µm of the SINR-3570 film. (b) Optical micrograph of trench filled with SINR-3570 after planarization.

At this point, the isolation trenches were refilled and the next task was to remove the polysilicon and silicon nitride layers on the surface of the wafer. This is illustrated in Figure 5-24e. To do this, photolithography of a 6 µm thick AZ9260 photoresist was done as discussed in section 5.3.1. Mask 2 was used for this purpose. Then, ICP etching of polysilicon was performed at a rate of 150 nm/min using the following etching parameters: 25 sccm SF_6, 45 sccm C_4F_8, table temperature of 15 ˚C, chamber pressure of

15 mTorr, RF power of 50 W, and ICP power of 700 W. Lastly, the remaining silicon nitride was also etched using the same ICP recipe with an etch rate of 60 nm/min.

5.3.4 Aluminum Deposition and Lift-off

After the trenches were refilled, the wafer was FNA-cleaned and dehydrated in a 120 ˚C oven for 30 minutes. To start off, TI Prime was spun at 3000 rpm for 20 seconds. Then, the wafer was baked at 120 ˚C for 2 minutes. The wafer was then immediately spin-coated with a 14 µm thick AZnlof2070 negative photoresist with the spin settings as depicted in Figure 5-26. After spinning, the photoresist was softbaked at 110 ˚C for 2 minutes. Then, the wafer was allowed to rehydrate for 30 minutes before exposing in vacuum contact for 30 seconds at an intensity of 12mW/cm^2 using the EVG620TB mask aligner with the I-line filter. After which, post-exposure bake at 110 ˚C for 2 minutes was performed. Then, the photoresist was developed in AZ726 MIF solution for 2 minutes and 30 seconds, rinsed in deionised (DI) water, and blow-dried using a N_2 gun. At this point, the photoresist was patterned with the mask defining the areas to be occupied by the aluminum thermoelements, wires, and pads.

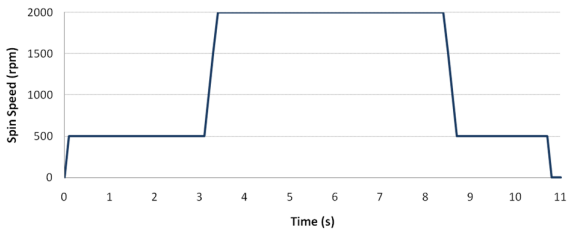


Figure 5-26: Spin settings for a target 14 µm thick AZnlof2070 photoresist.

After patterning, the wafer was dipped in 20:1 HF for 30 seconds to remove any native oxide prior to aluminum deposition. Then, 6 µm thick aluminum was e-beam deposited at a rate of 0.5 nm/s using the Leybold LAB700EB evaporator. Next, the wafer was submerged in N-Methyl-2-pyrrolidone (NMP) solvent, which acts as the lift-off medium in this process. The wafer was left in a beaker with NMP overnight to completely lift-off unwanted aluminum. After which, the wafer was cleaned with IPA and blow-dried with a N_2 gun. Figure 5-27 shows an image of the device after aluminum deposition and lift-off.

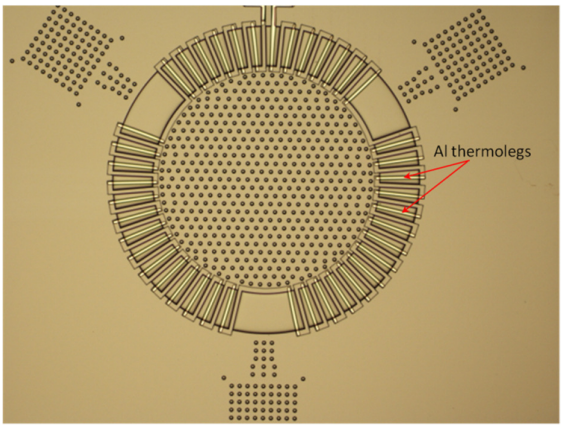


Figure 5-27: Optical micrograph of TEG after aluminum deposition and lift-off.

5.3.5 Backside DRIE

After depositing aluminum, the backside trenches were etched by deep reactive ion etching (DRIE) up to the buried oxide layer using the Plasmatherm Versaline Deep Silicon Etcher. The DRIE conditions for this process are listed in Table 5-4. Under these settings, the silicon etch rate was about 7.8 μm/min and the sidewall angle is 0.16 ˚, as calculated from the measurements shown in Figure 5-28.

Table 5-4: Backside DRIE settings

	Deposition	**Etch A**	**Etch B**
SF_6 (sccm)	0	150	350
C_4F_8 (sccm)	150	0	0
Ar (sccm)	30	30	30
Pressure (mT)	25	40	80
ICP Power (W)	2000	2000	2500
LF Bias (V)	10	350 to 450	10
Morphing Factor	1	0.5	1
Cycle Time (s)	2	1.5	2
Spool Temp (˚C)	180		
Lid Temp (˚C)	150		
Liner Temp (˚C)	70		
Electrode Temp (˚C)	15		
Helium Pressure (mT)	4000		

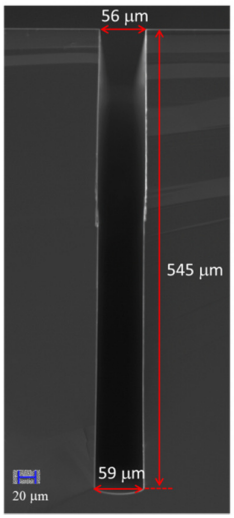


Figure 5-28: SEM image of trench after 70 minutes of backside DRIE.

5.3.6 HF Vapor Phase Etching

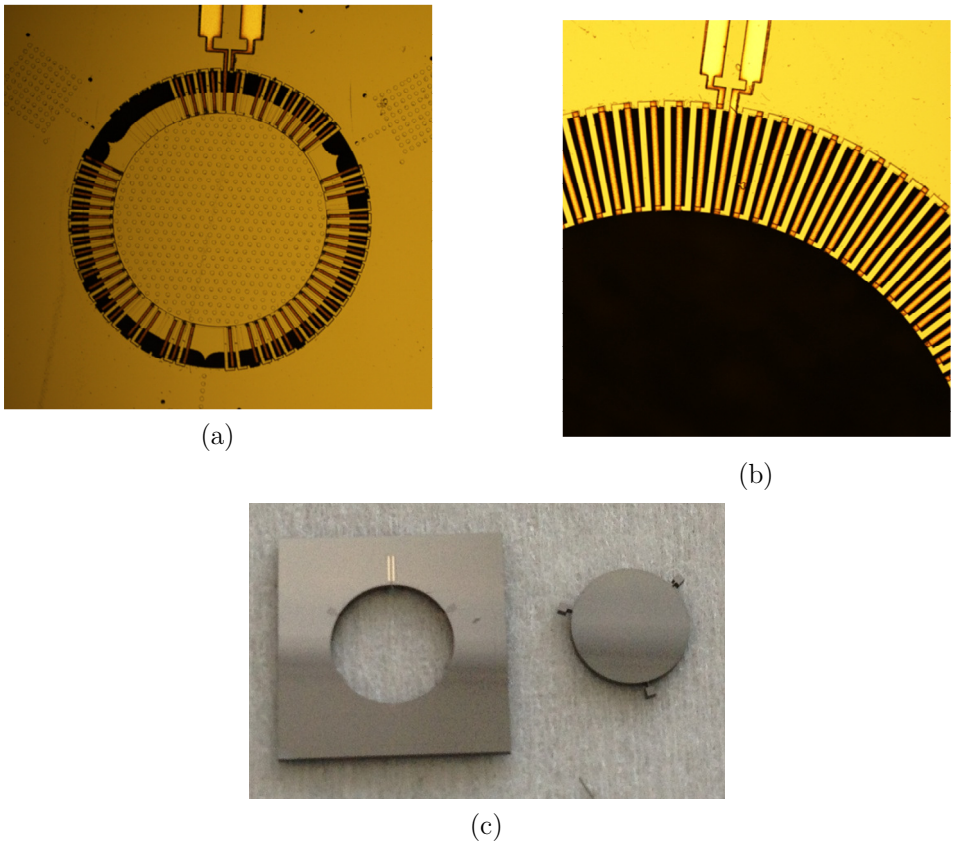
Once the backside trenches were etched, the wafer was first subjected to HF vapor etching (HFVPE) for 20 minutes at a temperature of 40 ° C using the Idonus HF Vapor Phase Etcher. The HF solution used for this purpose was highly concentrated at 48% HF:H_2O dilution. The wafer was then left on the heated chuck for a further 20 minutes to allow enough time for condensed water on the surface of the wafer to evaporate. The process of 20 minute etching and 20 minute evaporation was then repeated until the membrane is released. This iterative process was performed to minimize stiction on the devices. This step allows for dicing-free release of each TEG chip from the substrate (Overstolz et al. 2004)(Sari, Zeimpekis, and Kraft 2010).

5.3.7 Problems Encountered

Figure 5-29 shows images illustrating fabrication problems encountered after HFVPE, which is the last step in the proposed TEG fabrication process. One of the problems encountered was that some of the thermoelements broke midway through the HFVPE step. This is shown in Figure 5-29a. Since the thermoelements have to be electrically connected in series, having even only one thermoelement broken makes the device an open circuit. Another problem encountered, as shown in Figure 5-29b, is that the TEG

membrane separated from the thermoelements during HFVPE. This happens for devices with large membrane diameters (5 mm and 7 mm), as well as for some devices with 3 mm diameter membranes. Figure 5-29c shows another problem encountered wherein the membrane and thermoelements separates from the device rim. All these problems were evident for both methods used in filling the isolation trenches.

The fabrication issues encountered in the last step of the proposed fabrication process can be attributed to several factors. One possibility is that the TEOS and SINR-3570 films, although roughly protected from HF vapor with silicon-rich silicon nitride and polysilicon, respectively; could still be etched as there is the possibility of the HF vapor getting through especially if there are certain regions in the film that are porous. Another reason for these fabrication failures is that the materials used to fill the isolation trenches



(a) (b) (c)

Figure 5-29: Images illustrating problems encountered after HFVPE: (a) broken thermoelements, (b) membrane separating from thermoelements, and (c) membrane and thermoelements separates from device rim.

are not mechanically strong enough to hold the membrane and thermoelements in place. Moreover, the relatively thin device layer of the SOI makes the membrane more fragile so careful handling of the devices is critical. In some cases, membranes separating from the thermoelements during the process of transferring a device from the Idonus HFVPE chuck to a chip tray were experienced.

5.4 Conclusions

In this chapter, details on the design, layout, and fabrication of thermoelectric generators were presented. The most challenging step in the fabrication process is the filling of the isolation trenches which requires a material that is a good electrical insulator, has low stress for mechanical stability, and operational at temperatures of up to at least 350 $^{\circ}$C. The two methods of refilling isolation trenches explored did not result in any good devices. There were problems encountered during HFVPE, which is the last step of the proposed fabrication process. In this regard, alternative means of fabricating TEGs were investigated and presented in succeeding chapters.

Chapter 6: TEG Implementation on a Glass Substrate

As discussed in the previous chapter, several problems were encountered during the HFVPE step of the proposed fabrication process. To resolve this issue, two implementations of TEGs are investigated – one using a glass substrate and another one using a SOI substrate. In both cases, the HFVPE step is eliminated in the fabrication process. For this chapter, focus is given on the TEG implementation on a glass substrate. The design and modifications to the thermal model are presented first, followed by a description of the fabrication process. Lastly, measurement results with a laser set-up and with a solar simulator set-up are presented and analyzed.

6.1 Design and Modelling of TEGs Implemented on a Glass Substrate

The use of a substrate with low thermal conductivity such as glass has been briefly described in section 4.3. This configuration, shown in Figure 6-1, is highly stable mechanically as there are no suspended elements. Although the thermal efficiency is not as good as that with a fully suspended membrane, the fabrication process using a glass substrate is simpler and cheaper.

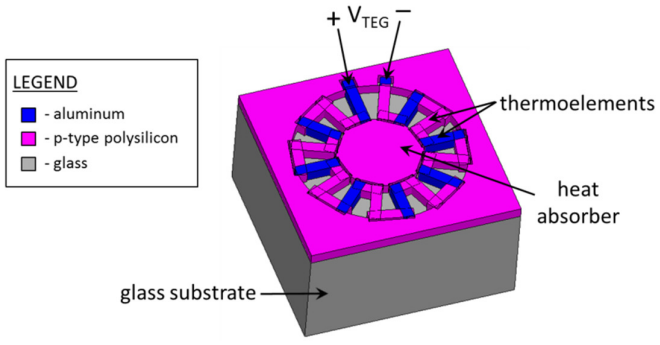


Figure 6-1: TEG implementation on a glass substrate with p-type polysilicon and aluminum as thermoelement materials.

Figure 6-2 shows a modified thermal equivalent model of the TEG in Figure 6-1. Aside from adapting the calculation of thermal conductances to the geometry of the device, heat losses through the substrate are also taken into account and highlighted in Figure 6-2 as component K_{SUB}, which is the thermal conductance of the portion of the substrate directly below the heated area of the device. The temperature node T_{SUB} is the temperature at the bottom of the glass substrate. Heat lost due to convection at the bottom of the substrate is also represented in this modified thermal model as $Q_{CONV,SUB}$.

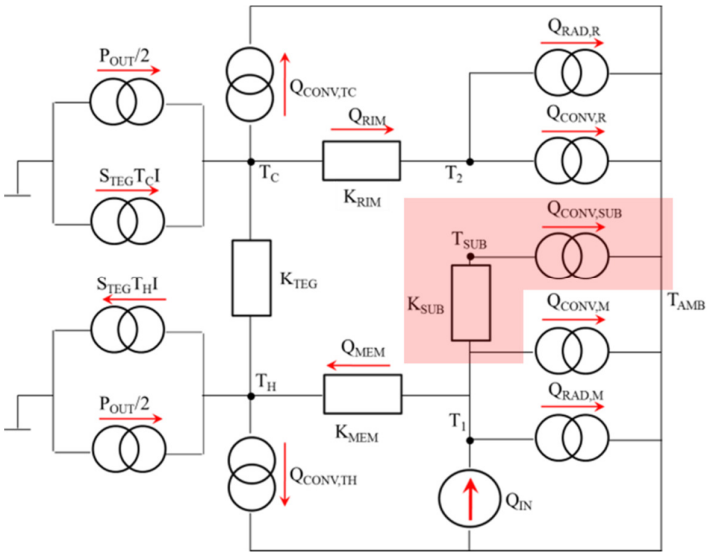


Figure 6-2: Thermal equivalent model of TEG implemented on a glass substrate. T_{SUB} is the temperature at the bottom of the substrate, K_{SUB} is the thermal conductance of the portion of the substrate directly below the heated area of the device, and $Q_{CONV,SUB}$ represents heat lost due to convection at the bottom of the substrate.

Referring to each temperature node in Figure 6-2, the heat balance equations then become:

at T_1:
$$Q_{IN} = Q_{MEM} + Q_{RAD,M} + Q_{CONV,M} + K_{SUB}(T_1 - T_{SUB}) \tag{6-1}$$

at T_H:
$$Q_{MEM} = K_{TEG}(T_H - T_C) + S_{TEG}T_H I - \frac{1}{2}P_{OUT} + Q_{CONV,TH} \tag{6-2}$$

at T_C:
$$Q_{RIM} = K_{TEG}(T_H - T_C) + S_{TEG}T_C I + \frac{1}{2}P_{OUT} - Q_{CONV,TC} \tag{6-3}$$

at T_2:
$$Q_{RIM} = Q_{RAD,R} + Q_{CONV,R} \tag{6-4}$$

at T_{SUB}: $$Q_{CONV,SUB} = K_{SUB}(T_1 - T_{SUB}) \tag{6-5}$$

The heat lost through the bottom of the substrate due to convection is given by:

$$Q_{CONV,SUB} = h_{conv}A_{SUB}(T_{SUB} - T_{AMB}) \tag{6-6}$$

where A_{SUB} refers to the surface area of the substrate.

Considering heat flow through K_{MEM} and K_{RIM}, the same equations as in section 4.3 for T_H and T_C in terms of T_1 and T_2, respectively, are derived.

$$T_H = T_1 - {Q_{MEM}}/{K_{MEM}} \tag{6-7}$$

$$T_C = T_2 + {Q_{RIM}}/{K_{RIM}} \tag{6-8}$$

Incorporating equations 4-17 to 4-22 and equations 6-6 to 6-8 into the heat balance equations in equations 6-1 to 6-5, and also noting that $\Delta T = T_H - T_C$, the following expressions are derived:

$$Q_{IN} = Q_{MEM} + \varepsilon\sigma A_{MEM}\left({T_1}^4 - {T_{AMB}}^4\right) + h_{conv}A_{MEM}(T_1 - T_{AMB}) + K_{SUB}(T_1 - T_{SUB}) \tag{6-9}$$

$$Q_{MEM} = K_{TEG}\Delta T + S_{TEG}\left(T_1 - \frac{Q_{MEM}}{K_{MEM}}\right)I - \frac{1}{2}P_{OUT} + h_{conv}A_{TEG}\left(T_1 - \frac{Q_{MEM}}{K_{MEM}} - T_{AMB}\right) \tag{6-10}$$

$$Q_{RIM} = K_{TEG}\Delta T + S_{TEG}\left(T_2 + \frac{Q_{RIM}}{K_{RIM}}\right)I + \frac{1}{2}P_{OUT} - h_{conv}A_{TEG}\left(T_2 + \frac{Q_{RIM}}{K_{RIM}} - T_{AMB}\right) \tag{6-11}$$

$$Q_{RIM} = \varepsilon\sigma A_{RIM}\left({T_2}^4 - {T_{AMB}}^4\right) + h_{conv}A_{RIM}(T_2 - T_{AMB}) \tag{6-12}$$

$$h_{conv}A_{SUB}(T_{SUB} - T_{AMB}) = K_{SUB}(T_1 - T_{SUB}) \tag{6-13}$$

From equation 6-13, an expression for T_{SUB} in terms of T_1 can be derived:

$$T_{SUB} = \frac{K_{SUB}T_1 + h_{conv}A_{SUB}T_{AMB}}{h_{conv}A_{SUB} + K_{SUB}} \tag{6-14}$$

Substituting T_{SUB} in equation 6-9 with equation 6-14 gives:

$$Q_{IN} = Q_{MEM} + \varepsilon\sigma A_{MEM}\left({T_1}^4 - {T_{AMB}}^4\right) + h_{conv}A_{MEM}(T_1 - T_{AMB}) + K_{SUB}\left(T_1 - \frac{K_{SUB}T_1 + h_{conv}A_{SUB}T_{AMB}}{h_{conv}A_{SUB} + K_{SUB}}\right) \quad (6\text{-}15)$$

Referring back to the thermal equivalent circuit in Figure 6-2, the temperature difference between T_1 and T_2 can be expressed as:

$$T_1 - T_2 = \frac{Q_{MEM}}{K_{MEM}} + \Delta T + \frac{Q_{RIM}}{K_{RIM}} \quad (6\text{-}16)$$

In equations 6-10 and 6-11, the current I and output power P_{OUT} can be expressed in terms of ΔT using equations 4-10 and 4-11, respectively. Hence, combining equations 6-10 and 6-15 gives a fourth-order polynomial in T_1 with only T_1 and ΔT as unknown variables.

$$\varepsilon\sigma A_{MEM}{T_1}^4 + C_3T_1 + C_4 = 0 \quad (6\text{-}17)$$

where $$C_3 = S_{TEG}I + h_{conv}(A_{TEG} + A_{MEM}) + K_{SUB}\left(1 - \frac{K_{SUB}}{h_{conv}A_{SUB} + K_{SUB}}\right) \quad (6\text{-}18)$$

and $$C_4 = K_{TEG}\Delta T - S_{TEG}\frac{Q_{MEM}}{K_{MEM}}I - \frac{1}{2}P_{OUT} - \varepsilon\sigma A_{MEM}{T_{AMB}}^4 - \frac{K_{SUB}h_{conv}A_{SUB}T_{AMB}}{h_{conv}A_{SUB} + K_{SUB}} - h_{conv}\left(\frac{Q_{MEM}}{K_{MEM}}A_{TEG} + (A_{TEG} + A_{MEM})T_{AMB}\right) - Q_{IN} \quad (6\text{-}19)$$

Similar to the procedure discussed in section 4.3, four expressions for T_1 as functions of ΔT can be derived by solving the roots of equation 6-17 using Ferrari's solution to a quartic function. By plugging in a positive value for ΔT and calculating the roots, the expression that gives a real and positive value for T_1 is selected. Similarly, equations 6-11 and 6-12 can be combined to form the following fourth-order polynomial equation:

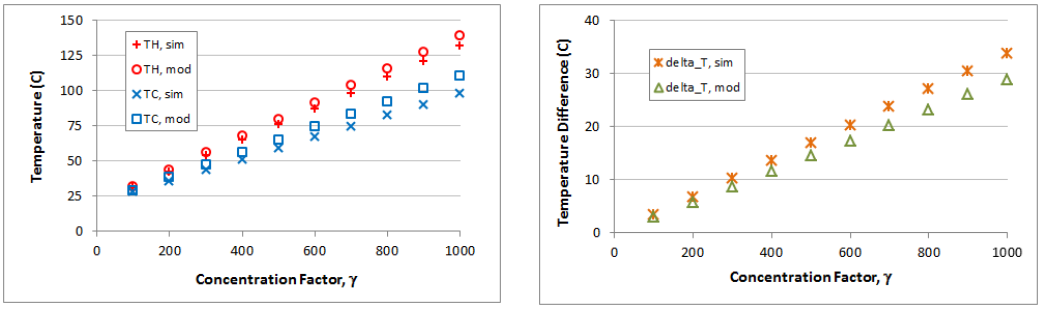
$$\varepsilon\sigma A_{RIM}{T_2}^4 + (h_{conv}(A_{TEG} + A_{RIM}) - S_{TEG}I)T_2 + C_2 = 0 \quad (6\text{-}20)$$

where

$$C_2 = -K_{TEG}\Delta T - S_{TEG}\frac{Q_{RIM}}{K_{RIM}}I - \frac{1}{2}P_{OUT} - \varepsilon\sigma A_{RIM}{T_{AMB}}^4 + h_{conv}\left(\frac{Q_{RIM}}{K_{RIM}}A_{TEG} - (A_{RIM} + A_{TEG})T_{AMB}\right) \quad (6\text{-}21)$$

The roots of equation 6-20 can then be solved and T_2 can be expressed in terms of ΔT. The derived equations for T_1 and T_2 can then be substituted into equation 6-16, which gives an equation with only ΔT as the unknown variable. The temperature difference across the thermoelements, ΔT, can then be solved numerically using Matlab. The Matlab program used to solve for ΔT can be found in Appendix A.

Figure 6-3 illustrates how this modified thermal model compares with 3-dimensional heat transfer simulations. The trends in hot and cold side temperatures, as well as in the temperature difference, are plotted with respect to the concentration factor. It can be observed that the temperatures obtained from the model are higher than those taken from simulations. The deviation between temperatures obtained from simulations and thermal model also increases with increasing concentration factor. This can be attributed to the assumption in the thermal model that the thermal conductivities of the thermoelectric materials are constant with temperature. For polysilicon, the thermal conductivity decreases with increasing temperature (Hopkins and Phinney 2009). A lower thermal conductivity would lead to a larger temperature difference across the device.

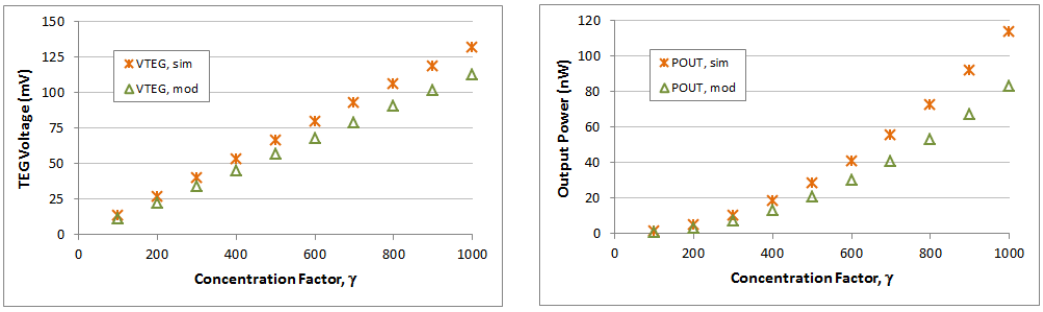


(a) (b)

Figure 6-3: (a) Hot (T_H) and cold (T_C) side temperatures and (b) temperature difference ΔT between simulations (*sim*) and thermal model (*mod*) of TEG on a glass substrate with varying solar concentration ratio. TEG has the following parameters: $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, $N = 34$, $\varepsilon = 0.6$, $h_{conv} = 50$ W/m^{2}K, $\alpha_{mem} = 0.5$, $\tau_{lens} = 1$, and $d_{spot} = 1$ mm.

Hence, it is expected that the temperature difference calculated from the thermal model is lower than that obtained from simulations as the concentration factor increases.

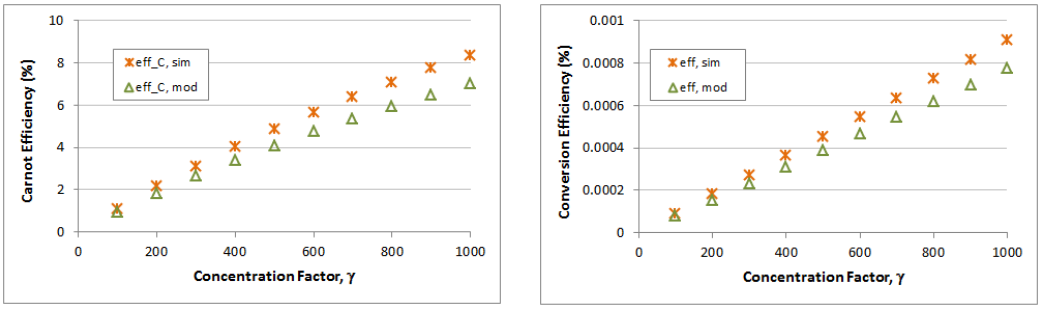
As a consequence of the difference between the temperatures obtained from the simulations and derived from the thermal model, the generated open-circuit voltage and matched output power obtained from simulations are higher than those computed from the thermal model. These relationships are shown in Figure 6-4. Moreover, both output voltage and output power increases with increasing solar concentration ratio as expected.



(a) (b)

Figure 6-4: (a) Open-circuit TEG voltage and (b) matched output power between simulations (*sim*) and thermal model (*mod*) of TEG on a glass substrate with varying solar concentration ratio. TEG has the following parameters: $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, $N = 34$, $\varepsilon = 0.6$, $h_{conv} = 50$ W/m^{2}K, $\alpha_{mem} = 0.5$, $\tau_{lens} = 1$, and $d_{spot} = 1$ mm.

The trends with both Carnot and conversion efficiencies are illustrated in Figure 6-5. The efficiencies obtained from simulations are higher than those derived from the thermal model. Both Carnot and conversion efficiencies increase with increasing solar concentration ratio, which reinforces that there is significant improvement in the efficiency of the device as solar energy is concentrated into the hot side of the TEG. The low values for the conversion efficiency is due to the poor thermoelectric figure-of-merit of the materials used, which is in the order of $1\text{x}10^{-6}$ K^{-1}. This value is three orders of magnitude lower than those plotted in Figure 2-4, where close to 5% conversion efficiency is calculated for a material with thermoelectric figure-of-merit of $1\text{x}10^{-3}$ K^{-1} and with a temperature difference of 200 K. Nonetheless, it was shown that the conversion efficiency improves by about 8 times when the solar concentration ratio is increased from 100 to 1000 for both simulations and thermal model.



(a) (b)

Figure 6-5: (a) Carnot efficiency and (b) conversion efficiency between simulations (*sim*) and thermal model (*mod*) of TEG on a glass substrate with varying solar concentration ratio. TEG has the following parameters: $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, $N = 34$, $\varepsilon = 0.6$, $h_{conv} = 50$ W/m^{2}K, $\alpha_{mem} = 0.5$, $\tau_{lens} = 1$, and $d_{spot} = 1$ mm.

6.2 TEG Fabrication Process on a Glass Substrate

The fabrication process for a TEG implemented on a glass substrate is illustrated in Figure 6-6. The process starts with a 500 µm thick, 4 inch Pyrex wafer. A 4 inch wafer was used instead of a 6 inch wafer due to availability. As shown in Figure 6-6, the process starts with deposition of boron-doped polysilicon by hot-wire chemical vapor deposition (HWCVD). Then, the deposited HWCVD polysilicon was patterned to form frontside trenches that define the polysilicon thermoelements, membrane, and rim of the device. Isolation trenches were also etched in this step so as to provide electrical isolation. After which, 1 µm thick Al was deposited and lifted-off to define the second thermoelement and bonding pads. The wafer was then diced into TEG devices and several chips were wire bonded on 24-pin chip carriers, which were then soldered onto corresponding headers. Each step involved in this fabrication process is further discussed in succeeding sections. For a detailed outline of actual device fabrication on a glass wafer, the reader is referred to Appendix E.

To facilitate discussion, this section is divided into the three major steps of the fabrication process which are:

1) HWCVD polysilicon deposition and etching.
2) Aluminum deposition and lift-off.
3) Wafer dicing and chip wirebonding.

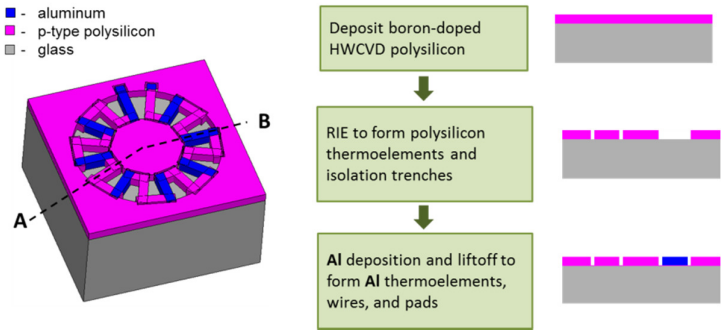


Figure 6-6: TEG fabrication process using a Pyrex wafer with HWCVD p-type polysilicon and aluminum as thermoelement materials. Cross-sectional view is along AB.

6.2.1 HWCVD Polysilicon Deposition and Etching

HWCVD is predominantly used for the deposition of amorphous, polycrystalline, and epitaxial silicon films for photovoltaic applications (Rath 2003). This technique involves the decomposition of precursor gases by means of heating one or more metallic filaments (usually tungsten or tantalum) at 1600-2100 ˚C. The dissociated gas molecules are then deposited onto a heated substrate. The filament and substrate temperatures, chamber conditions, and proportion of gases used determine the properties of the deposited film (Iiduka, Heya, and Matsumura 1997)(Pant et al. 2001). The main advantages of the HWCVD technique over PECVD are that the deposition mechanism is inherently free of dust because of the absence of plasma, no damage due to energetic ions occurs, and the technique is considered low-cost since there are no expensive RF supplies and matching boxes (Schropp 2004).

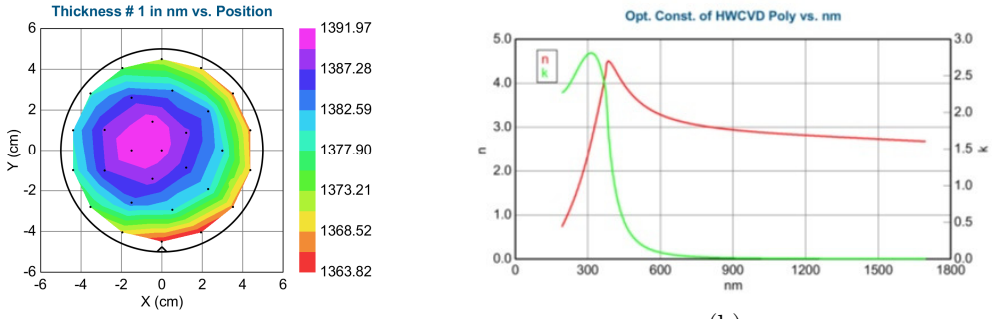
Several experiments were performed to characterize the quality of the deposited HWCVD polysilicon. The HWCVD tool has two doping gases: 0.1% PH_3 in H_2 for n-type Si and 10% B_2H_6 in H_2 for p-type Si. The target polysilicon film should be heavily-doped with a resistivity in the order of 10^{-3} Ω-cm. Initial experiments show that this resistivity is not achievable with the maximum PH_3 flow, unless annealing at temperatures greater than 800 ˚C is performed after deposition. Although annealing was found to significantly decrease the resistivity of films deposited on a Si wafer, using a glass wafer limits processing temperature making an 800 ˚C annealing step after deposition not possible.

Hence, it was decided that a p-type polysilicon film be used for the devices. Table 6-1 summarizes the experiments performed for boron-doped HWCVD polysilicon.

Table 6-1: Boron-doped HWCVD polysilicon experiments. In all cases, filament temperature is 2100 ° C, substrate temperature is 440 ° C, and chamber pressure is at 0.024 mB. Resistivity is calculated as the product of the film thickness and the sheet resistance measured with a four-point probe system.

Sample No.	SiH_4 (sccm)	B_2H_6 (sccm)	H_2 (sccm)	Deposition rate (nm/s)	resistivity (Ω-cm)
1	12	0.1	150	0.239	0.04816
2	12	0.25	300	0.194	0.029225
3	12	0.25	150	0.243	0.025754
4	12	0.5	150	0.237	0.016226
5	12	1	150	0.234	0.009683
6	6	1	75	0.132	0.00903
7	6	10	75	0.123	0.00444
8	6	20	75	0.114	0.005474

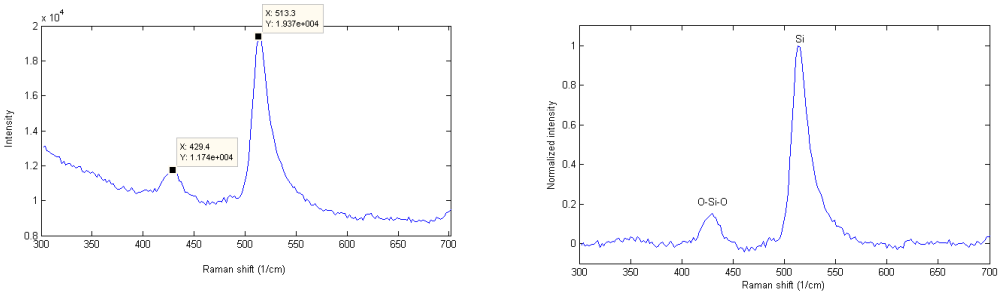
As expected, the resistivity decreases with increasing B_2H_6 flow except in the case of sample 8. This implies that the amount of Si atoms in the chamber reacting with the boron atoms have saturated and more SiH_4 have to be introduced in the chamber to lower the resistivity. However, adding more SiH_4 can lead to a more amorphous film, which would require an annealing step to improve the film's crystallinity. In this regard, sample 7 was selected as the material to be used for the TEG. The dopant concentration of the deposited film was measured to be in the order of $1x10^{21}$ cm^{-3} using a Hall Effect system. To be able to uniformly heat up the Pyrex substrate at the substrate temperature, a silicon wafer was placed at the back of the Pyrex wafer to act as a thermal spreader. The deposition was done for 2.5 hours with a 10 minute seeding layer step to enhance the film's crystallinity. An ellipsometry scan of the deposited film was performed afterwards and the film was represented using a Cody-Lorentz dispersion model. Figure 6-7a shows the calculated thickness based on this model, which is 1379 ± 8.7nm, giving a uniformity of 98%. The film's optical constants are also shown in Figure 6-7b. The refractive index is 3.22 at 633nm and approaches 2.69 at the infrared wavelengths.



(a) (b)

Figure 6-7: (a) Thickness representation and (b) optical constants based on ellipsometry results of p -type HWCVD polysilicon deposited on a Pyrex substrate for 2.5 hours.

To check the crystallinity of the film, Raman spectroscopy was performed. Figure 6-8 shows the raw and baseline-corrected Raman spectra of the polysilicon film deposited on a Pyrex substrate. The sharp peak at 513 cm^{-1} indicates excellent crystallinity of the polysilicon film.



(a) (b)

Figure 6-8: (a) Raw and (b) baseline-corrected Raman spectra of boron-doped HWCVD polysilicon deposited on a Pyrex substrate.

Fourier transform infrared (FTIR) spectroscopy was also done to verify the heat absorption ability of the deposited polysilicon film. Figure 6-9 shows the FTIR spectra of the 5 µm thick SOI device layer and the p-type HWCVD polysilicon. As can be seen from the graph, the SOI has lower transmittance (higher absorptance) at shorter wavelengths whereas the polysilicon has zero transmittance (very high absorptance) at longer wavelengths. These properties confirm that the deposited HWCVD polysilicon is able to absorb and retain heat and can be a viable material for the thermoelectric device.

Lastly, the distance between interference fringes mainly corresponds to the thickness of the material. The nearer the fringes are to each other, the thicker the material.

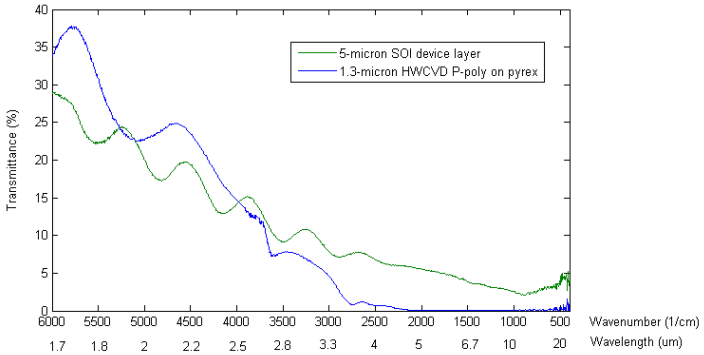


Figure 6-9: FTIR spectra of SOI device layer and HWCVD p-type polysilicon.

The deposited polysilicon on the glass substrate was then patterned to define the thermoelements and isolation trenches using the 6 µm thick AZ9260 lithography discussed in section 5.3.1. Once the photoresist mask was patterned, the polysilicon was etched using a reactive ion etcher with the following conditions: 18 sccm SF_6 and 22 sccm O_2 at a table temperature of 20 ° C, chamber pressure of 30 mTorr, and RF power of 100 W. The HWCVD polysilicon etch rate was about 2.3 nm/s. After which, the photoresist was stripped off in O_2 plasma and the wafer was FNA-cleaned in preparation for the next fabrication step.

6.2.2 Aluminum Deposition and Lift-off

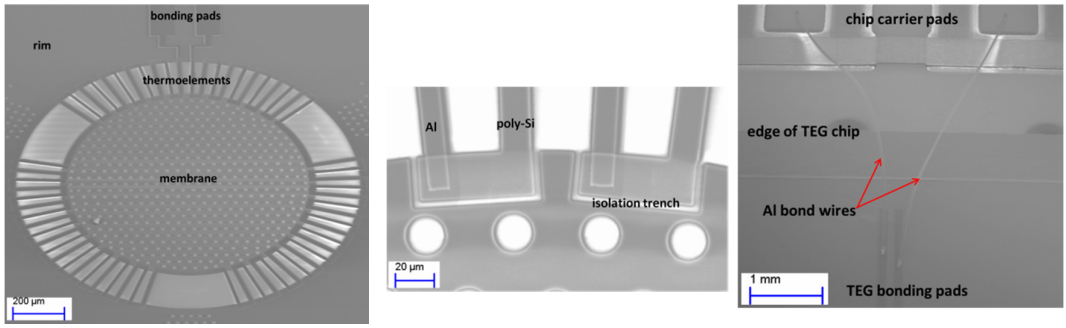
The steps performed in the deposition and lift-off of aluminum on the Pyrex substrate is the same as the one discussed in section 5.3.4. The only difference is that instead of depositing 6 µm thick aluminum, only 1 µm thick was deposited, which is of the same order in thickness as that of the deposited polysilicon.

6.2.3 Wafer Dicing and Chip Wirebonding

The last step in the TEG fabrication process on a glass substrate involves dicing the wafer to obtain separate TEG chips from the wafer using a dicing saw. To protect the

patterned thermoelements prior to dicing, S1813 photoresist was spun onto the wafer at 5000 rpm for 30 seconds. Then, the wafer was baked at 115 ˚C for 60 seconds. The wafer was then diced to separate the TEG chips from each other. After separation, the S1813 photoresist was stripped in acetone and each chip was rinsed in IPA and DI water then dried using a N_2 gun.

SEM micrographs of a sample TEG device are shown in Figure 6-10. Once the wafer was diced and cleaned accordingly, each chip was bonded to a chip carrier using thermal paste and the voltage pads were wire-bonded onto the chip carrier using a Delvotek wirebonder. Figure 6-10c illustrates how the TEG voltage pads are connected to the chip carrier pads with aluminum wires. Figure 6-11 shows a photograph of the assembled TEG on a prototyping board, ready for testing.



(a) (b) (c)

Figure 6-10: (a) TEG with thermolength of 200 µm, thermowidth of 15 µm and membrane diameter of 1 mm with 31 thermocouples. (b) Closer view of connection between thermoelements. (c) Bonding wires connecting the TEG to the chip carrier.

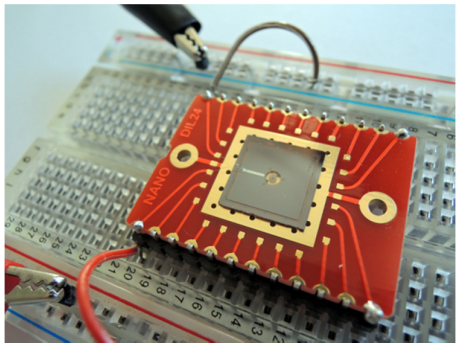


Figure 6-11: TEG with thermolength of 500 µm, thermowidth of 15 µm, membrane diameter of 1 mm, and 34 thermocouples on a prototyping board.

6.3 HWCVD Polysilicon Characterization

As discussed in section 5.2.2, several test structures have been designed and fabricated to measure the electrical and thermal properties of the materials used as thermoelements. Focus is now given to the characterization of the HWCVD polysilicon thermoelements as the electrical and thermal properties of aluminum have little effect on the performance of the device. The electrical and thermal properties of aluminum is assumed to be those listed in Table 4-2 where it has higher thermal conductivity, lower electrical resistivity and lower Seebeck coefficient than polysilicon.

The discussion starts with the Van der Pauw structure, which enable the measurement of electrical resistivity. Then, results of measurements performed on planar and cantilever structures, which allows the derivation of the Seebeck coefficient and thermal conductivity, respectively, are discussed. Lastly, the contact resistance is obtained from measurements made on the Kelvin structures.

6.3.1 Electrical Resistivity

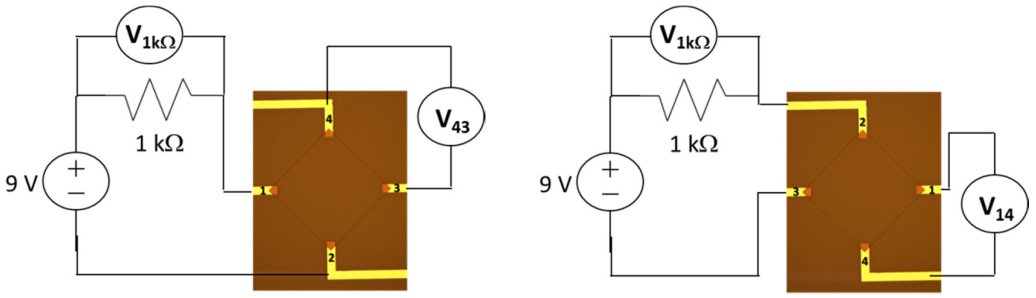
The circuits used to derive the two characteristic resistances R_A and R_B of the fabricated HWCVD polysilicon Van der Pauw structure is shown in Figure 6-12. Electrical current was applied on two ends of these structures by using a 9 V battery in series with a 1 kΩ resistor. Then, voltage was measured on the other two ends of the structure using a voltmeter. The current through the structure is derived using Ohm's law from the measurement of the voltage across the 1 kΩ resistor. The characteristic resistances are calculated using these two equations:

$$R_A = V_{43}/I_{12} \tag{6-22}$$

$$R_B = V_{14}/I_{23} \tag{6-23}$$

These resistances are related to the sheet resistance through the van der Pauw equation:

$$\exp(-\pi R_A/R_S) + \exp(-\pi R_B/R_S) = 1 \tag{6-24}$$



(a) (b)

Figure 6-12: Two circuits used to derive the two characteristic resistances R_A and R_B of a Van der Pauw structure.

Once R_S is solved numerically, the bulk electrical resistivity can be calculated using $\rho = R_S t$, where t is the thickness of the material. Table 6-2 lists the results of measurements performed on the two circuits in Figure 6-12.

Table 6-2: Results of measurements made on HWCVD polysilicon Van der Pauw structure fabricated on a Pyrex substrate.

I_{12} (mA)	V_{43} (mV)	R_A (Ω)	I_{23} (mA)	V_{14} (mV)	R_B (Ω)	R_S (Ω/□)	t (μm)	resistivity (Ω -m)
6.606	38.9	5.89	6.778	37.7	5.56	25.97	1.38	**3.58×10^{-5}**

6.3.2 Seebeck Coefficient

The circuit used for determining the Seebeck coefficient of HWCVD polysilicon using the planar structure discussed in section 5.2.2 is shown in Figure 6-13. A polysilicon planar strip is connected to aluminum at pads 5 and 6. A polysilicon heater connected at pads 11 and 12 is positioned 20 μm away from the hot contact of the polysilicon strip. The aluminum contacts at the ends of the polysilicon strip also act as temperature monitors and are in four-point measurement configurations (pads 1, 2, 3, 4 and pads 7, 8, 9, 10) to enable tracking of small temperature variations by measuring small resistance changes. When current is applied to the heating resistor, the temperature of the hot and cold contacts increases from T_0 to T_h and T_c, respectively. These changes in temperature are determined using the temperature-dependent resistance of the temperature monitors. To determine the temperature variation in the aluminum temperature monitors, the

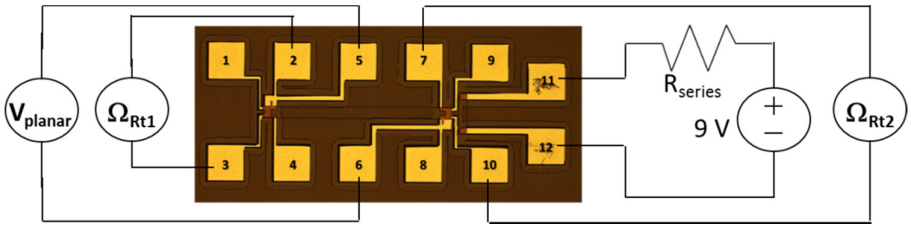


Figure 6-13: Circuit for determining Seebeck coefficient of HWCVD polysilicon utilizing planar structure.

temperature coefficient of resistance of aluminum, TCR_{Al}, is assumed to be 0.00429/ ° C[4]. The initial resistance of the two temperature monitors, R_{t1O} and R_{t2O}, are measured as 22 and 53.1 ohms, respectively. The heater was connected to a 9 V battery in series with varying series resistors, R_{series}. Then, the voltage across the planar structure, V_{planar}, and the resistance of the temperature monitors, R_{t1} and R_{t2}, were measured. The temperature change on the temperature monitors are calculated using the following equation:

$$\Delta T = \frac{R_{t1}-R_{t1O}}{TCR_{Al}R_{t1O}} - \frac{R_{t2}-R_{t2O}}{TCR_{Al}R_{t2O}} \tag{6-25}$$

The Seebeck coefficient is then calculated from the expression:

$$\alpha|_{\frac{T_h+T_c}{2}} = \frac{V_{planar}}{T_h-T_c} = \frac{V_{planar}}{\Delta T} \tag{6-26}$$

Table 6-3 lists down the measurement results obtained on a polysilicon planar structure using three different series resistors. The average Seebeck coefficient of HWCVD p-type polysilicon is calculated to be 113 μV/K.

Table 6-3: Results of measurements made on polysilicon planar structure fabricated on a Pyrex substrate.

R_{series} (Ω)	V_{planar} (mV)	R_{t1} (Ω)	R_{t2} (Ω)	ΔT (K)	α (μV/K)
296	9.30	28	47	90.35	102.93
987	1.22	22.7	52.4	10.49	116.30
1980	0.338	22.1	52.7	2.82	119.86

[4] http://hyperphysics.phy-astr.gsu.edu/hbase/tables/rstiv.html

6.3.3 Thermal Conductivity

The circuit used for determining the thermal conductivity of HWCVD polysilicon using the cantilever structure discussed in section 5.2.2 is shown in Figure 6-14. The polysilicon cantilever is connected with two aluminum contacts at pads 5 and 6 to measure the thermally generated voltage. Two resistors are integrated into the hot tip of the cantilever. The polysilicon resistor across pads 1 and 2 close to the end of the beam is used as a heater. The aluminum resistor across pads 3 and 4 acts as a temperature monitor. When a power P is dissipated in the heater, the temperature of the hot tip of the cantilever is increased by ΔT. The overall thermal conductance of the structure can then be calculated as equal to $^{P}/_{\Delta T}$ and the thermal conductivity is derived by using the following equation:

$$\lambda = \frac{P}{\Delta T}\frac{l}{wt} \tag{6-27}$$

where l, w, and t are the length, width, and thickness of the cantilever, respectively.

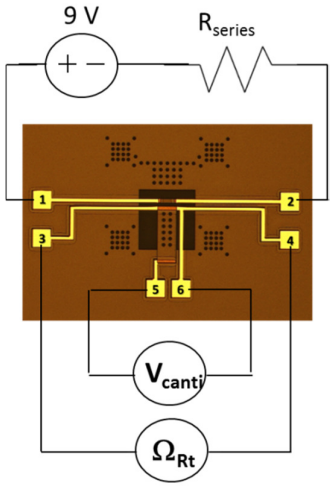


Figure 6-14: Circuit for determining thermal conductivity of HWCVD polysilicon utilizing cantilever structure.

Similar to the planar structure, the temperature coefficient of resistance of aluminum, TCR_{Al}, is also assumed to be 0.00429/ ° C. The initial resistance of the temperature monitor, R_{tO}, is measured as 88.7 Ω. The heater was also connected to a 9V battery in series with varying series resistors, R_{series}. Then, the voltage across the 300 µm x 100 µm

cantilever structure, V_{canti}, and the resistance of the temperature monitor, R_t, was measured. The temperature change on the temperature monitor is calculated using:

$$\Delta T = \frac{R_t - R_{tO}}{TCR_{Al} R_{tO}} \tag{6-28}$$

Power is calculated as the square of V_{canti} divided by 4 times the resistance of the cantilever, which is measured to be 260 Ω.

Table 6-4 lists down the measurement results obtained on a polysilicon cantilever structure using three different series resistors. The average thermal conductivity of HWCVD p-type polysilicon is calculated to be 126 W/mK.

Table 6-4: Results of measurements made on polysilicon cantilever structure fabricated on a Pyrex substrate.

R_{series} (Ω)	V_{canti} (V)	R_t (Ω)	P (mW)	ΔT (K)	λW/mK)
296	1.95	112	3.656	61.23	124.02
987	0.736	91.8	0.521	8.15	132.77
1980	0.402	89.7	0.155	2.63	122.40

6.3.4 Contact Resistance

The circuit with the Kelvin structure used for measuring contact resistance is shown in Figure 6-15. By forcing a current between pads 1 and 4 and measuring the voltage across pads 2 and 3, the contact resistance can be determined from the following equation:

$$R_C = V_{23}/I_{14} \tag{6-29}$$

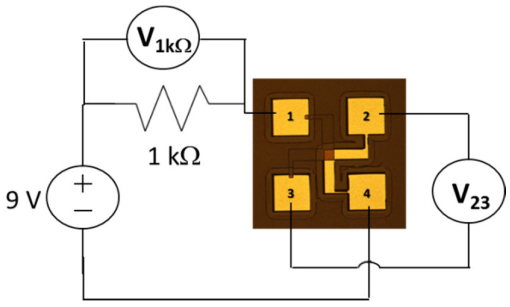


Figure 6-15: Circuit for determining contact resistance utilizing Kelvin structure.

The measured voltage V_{23} is 1.45 mV and the current I_{14} is 6.159 mA. Using equation 6-29, the measured contact resistance of the Kelvin structure fabricated on a Pyrex substrate is 0.235 **Ω,** translating to a specific contact resistance of 211.5 **Ω–**μm^2.

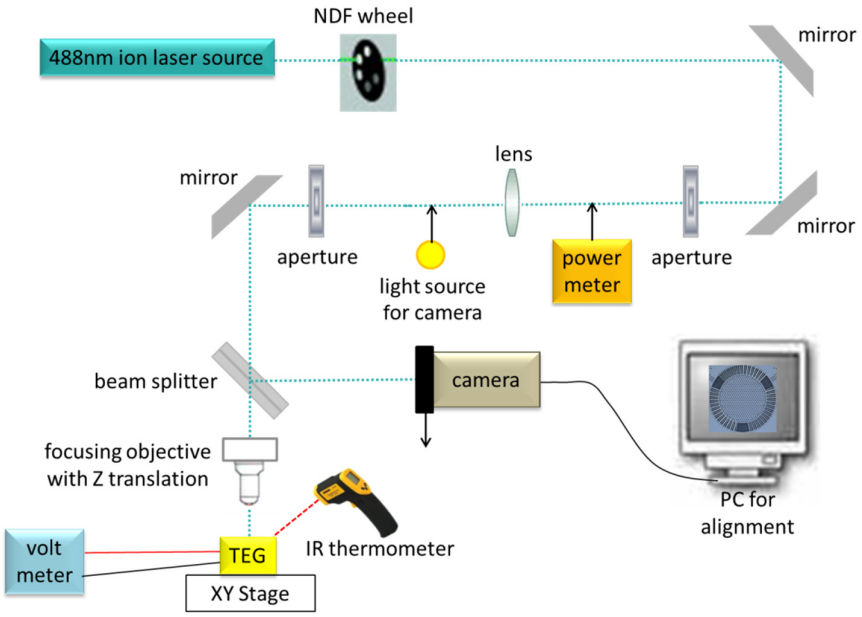
6.4 Measurement Results

Due to the limited amount of chip carriers available, only ten TEGs implemented on a glass substrate were tested. These representative TEGs all have 3 μm wide isolation trenches with the dimensions listed in Table 5-1. To properly characterize the fabricated TEGs on a glass substrate, two measurement set-ups were performed. First, the TEGs were tested using a laser set-up where the input power is varied at a constant spot size. This allows depiction of a scenario where there is precise control of the solar spot size and the variation in input power represents varying the concentration ratio. The second set-up involved testing the TEGs using a solar simulator and three lenses with different diameters to emulate the environment with which the devices are to be used as solar TEGs employing solar concentration.

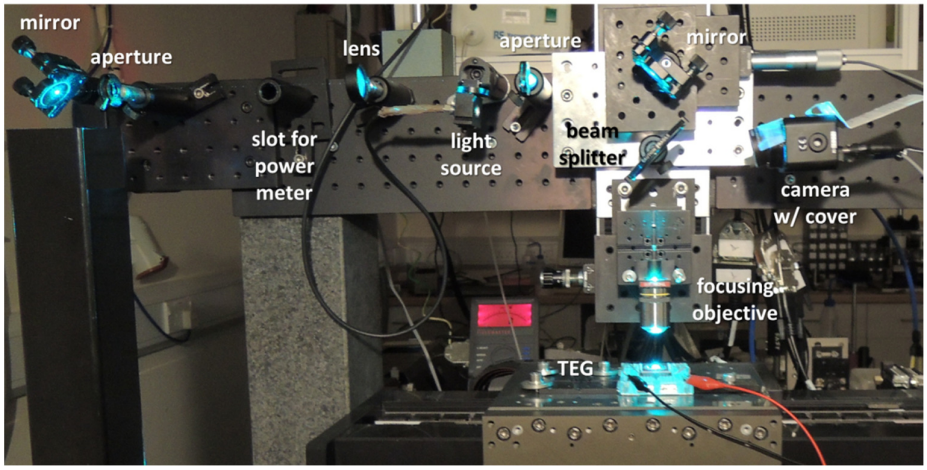
6.4.1 Laser Testing

The laser testing set-up is shown in Figure 6-16. This set-up is located at the Optoelectronics Research Center (ORC) of the University of Southampton. The laser source was a 488 nm Innova™ 300C FreD™ ion laser source from Coherent, Inc[5]. This laser utilizes inter-cavity frequency doubling to produce continuous-wave laser emission. A neutral density filter (NDF) wheel was placed after the laser source to modulate the power of the laser beam. Mirrors were placed in the set-up to redirect the laser beam. A lens was used to focus the laser on to the device under test while the apertures assist in limiting the spot size of the laser beam. A beam splitter with 8% reflection and 92% transmission characteristics was utilized to split the source into two – the reflected signal

[5] http://www.coherent.com



(a)



(b)

Figure 6-16: (a) Illustration and (b) partial photograph of laser testing set-up with a 488 nm ion laser. Input power is varied using the NDF wheel. Alignment is done by inserting the power meter and light source as indicated, and removing the camera cover. The power meter is inserted to the set-up each time that the NDF wheel is adjusted to record the change in input power.

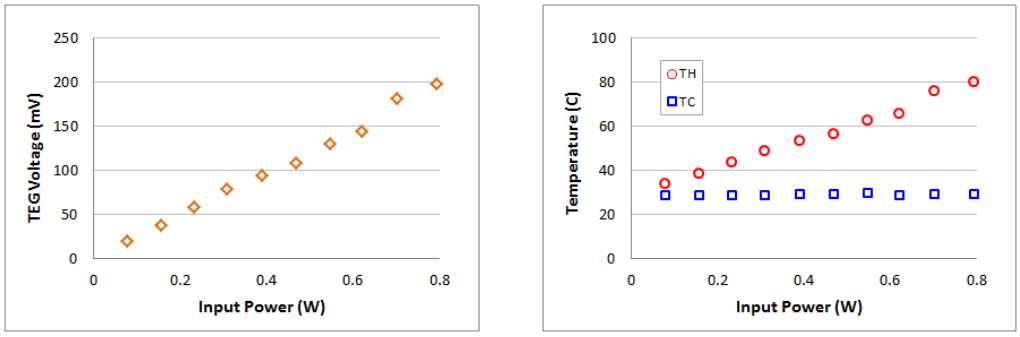
was used for aligning the beam into the center of the TEG using a camera connected to a PC for control of the TEG's XY stage while the transmitted signal was directed to a focusing objective which controls the spot size of the laser that reaches the center of the TEG. Before any measurements can take place, the objective efficiency was first determined by measuring the ratio of the power reading at the location of the power

meter indicated in Figure 6-16 to the power reading after the focusing objective. For the multiple days that the measurements were taken, the average objective efficiency was found to be around 80%. This means that if the power reading is 100 mW, the actual input power to the TEG is 80 mW. All the measured power by the power meter is then multiplied by the objective efficiency to obtain the actual input power of the TEG. Once the objective efficiency was known, the Z translation of the focusing objective was adjusted to have a spot size of about 1 mm. This was done by rotating the NDF wheel for an input power of about 10 mW. Then, the focusing objective was gradually moved in the Z-direction while a ruler was used to measure the spot size at each adjustment. Once the spot size was about 1 mm, the Z translation of the focusing objective was fixed at this configuration for all measurements and laser testing can commence. For each TEG, alignment was first performed to make sure that the TEG is centrally placed on the XY stage. To do this, the power meter was placed to block the laser, a light source was inserted, and the camera cover was removed as indicated in Figure 6-16a. This configuration allows viewing of the TEG on the PC screen. The XY stage was then adjusted such that the crosshair on the screen is aligned to the center of the TEG. After alignment, the light source was removed and the camera cover was replaced. Then, the NDF wheel was adjusted to have varying input power levels up to 1 W. At each change in input power, the corresponding output voltage as measured by the volt meter was recorded. An infrared thermometer was also used to measure the temperature at the cold side of the TEG for each iteration of the input power. Ten measurements were taken for each TEG.

Figure 6-17a shows a plot of the measured open-circuit TEG voltage with varying laser input power for a TEG with $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 34$. Taking the slope of this graph, it can be derived that the generated voltage is 247 mV/W. Since the Seebeck coefficient of the materials are known ($\alpha_{poly} = 113$ µV/K and $\alpha_{Al} = -1.8$ µV/K), then the temperature difference can be computed as:

$$\Delta T = \frac{V_{TEG}}{N(\alpha_{poly} - \alpha_{Al})} \tag{6-29}$$

As previously discussed, the cold side temperature, T_C, was measured using an infrared thermometer. The hot side temperature, T_H, is then calculated as the sum of T_C and ΔT. Figure 6-17b shows a plot of the hot and cold side temperatures of the same TEG. It can be observed that the cold side temperature is almost constant at about 29 ° C. Applying the thermal model developed in section 6.1, it is determined that to keep the cold side temperature close to this value, the heat transfer coefficient due to convection must be around 250 W/m^{2}K, which correspond to forced convection in air. This is possible as the set-up at ORC includes nitrogen cooling for the laser and the room has an exhaust system as well.



(a) (b)

Figure 6-17: Measured (a) open-circuit TEG voltage and (b) hot and cold side temperatures versus laser input power of a TEG implemented on a glass substrate with these dimensions: $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 34$.

The dependence of the membrane absorptance on the wavelength of the laser is also considered. The absorption of photons entering a semiconductor material is a statistical process. The sites of photon-absorption are statistically distributed with an exponential dependence of distance from the semiconductor surface and wavelength of the incoming light. The distance where 37% of the total photon flux is absorbed is called the penetration depth (Lange 2000). Looking at the graph of the penetration depth versus wavelength in Figure 6-18a, it can be observed that short wavelengths are absorbed in a short distance from the surface while longer wavelengths are absorbed deeper into the

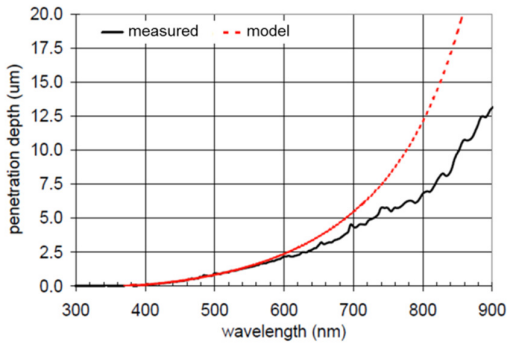
silicon film. In fact, the penetration depth for silicon is 569 nm[6] for a wavelength of 488 nm. Figure 6-18b shows the absorptance of light with a wavelength of 488 nm on silicon. This plot is generated using the exponential equation below:

$$absorptance\ at\ 488nm = e^{-x/569nm} \tag{6-30}$$

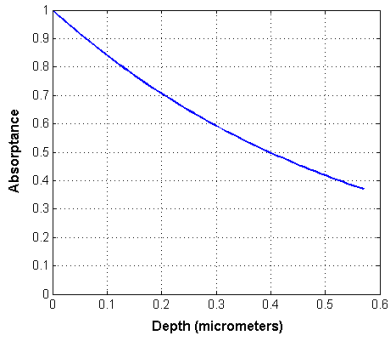
The area under the curve, which represents the amount of photons absorbed and divide that by the penetration depth, is then calculated. This gives the membrane absorptance, α_{mem}, which is computed to be 63%. Note that it is assumed that beyond the penetration depth, negligible amount of 488 nm photons is absorbed.

The input power Q_{IN} of the thermal model in Figure 6-2 is then represented as a function of the laser input power P_{in} and the membrane absorptance as:

$$Q_{IN} = \alpha_{mem} P_{in} \tag{6-31}$$



(a)



(b)

Figure 6-18: (a) Optical penetration depth of silicon (Lange 2000). (b) Absorptance of light with a wavelength of 488 nm on silicon.

Table 6-5 lists down the parameters used in the thermal model to represent the conditions of the laser set-up. Figure 6-19 shows a comparison between the simulated, thermal model, and measured parameters. It can be seen from Figure 6-19a that the hot and cold side temperatures derived from the thermal model agrees well with the measurements. The temperature values derived from the thermal model are within 2.8%

[6] http://www.horiba.com/fileadmin/uploads/Scientific/Documents/Raman/Semiconductors01.pdf

of the measured temperature values. The simulated temperatures, however, are less than 10 ˚C higher than the measurements. This can be attributed to the extremely coarse meshing employed in the simulations. The relatively large variation in the dimensions of the 10×10 mm^2 TEG, e.g. 500 µm thick substrate and 1 µm thick polysilicon, influenced the decision to employ extremely coarse meshing so as to resolve memory runtime errors. In spite of this, the temperature difference ΔT derived from the three sets of data are

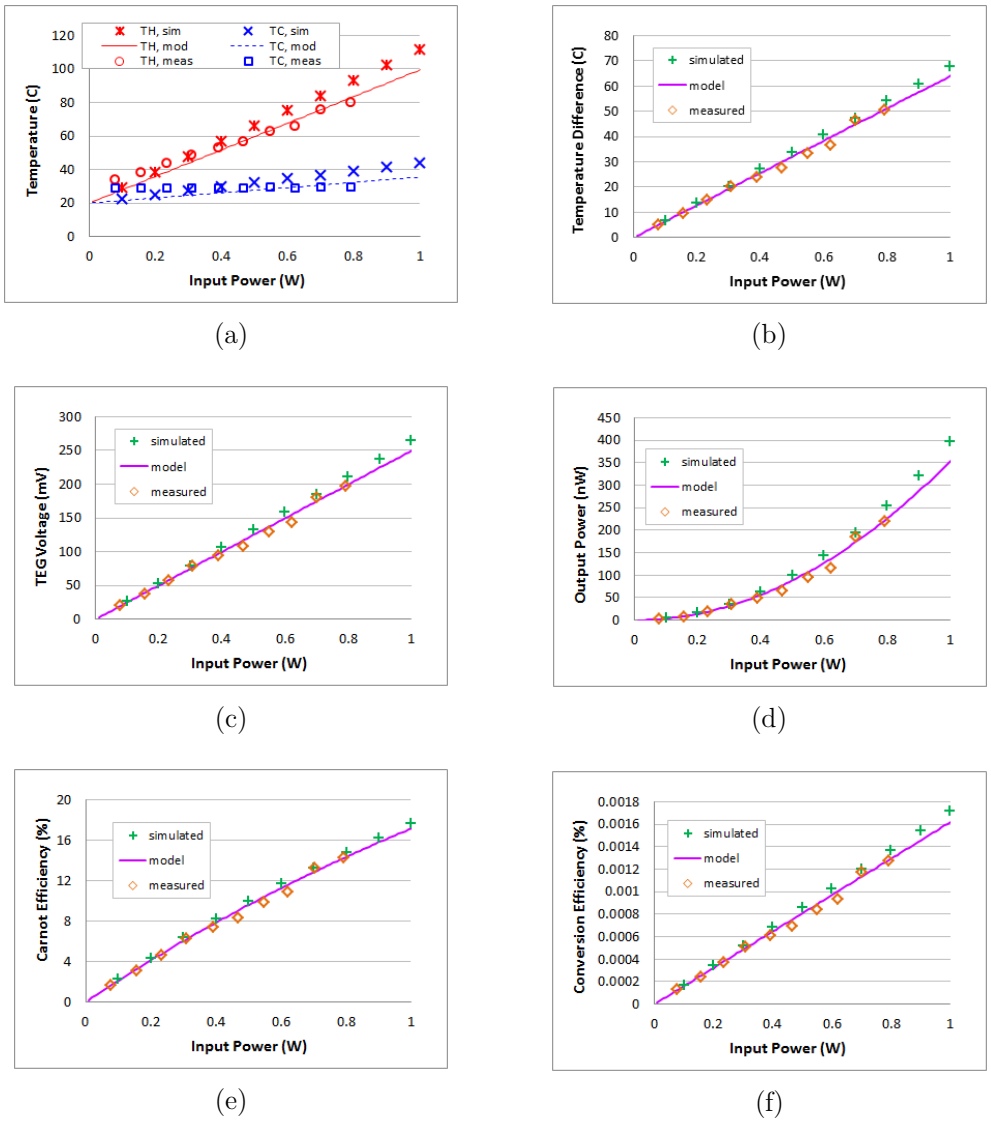


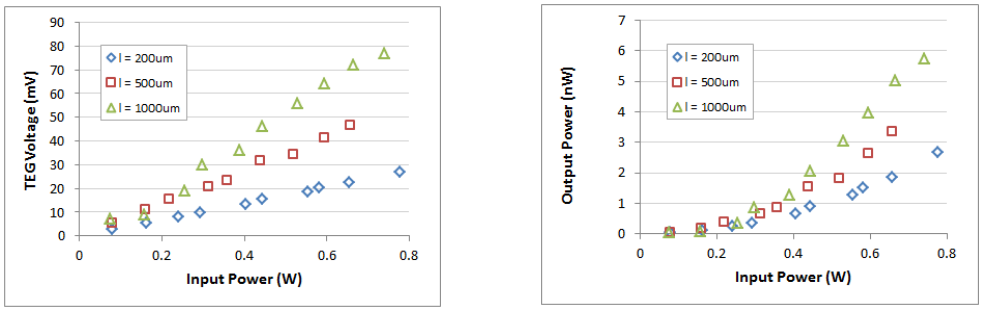
Figure 6-19: Comparison between simulations, thermal model, and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) matched output power, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 34$.

Table 6-5: Parameters used in thermal model of TEG on glass substrate to emulate conditions in laser test set-up.

Parameter	Value	Parameter	Value
α_{poly}	113 μV/K	λ_{glass}	1.4 W/mK
λ_{poly}	126 W/mK	α_{mem}	0.63
ρ_{poly}	3.58 x 10^{-5} Ωm	h_{conv}	250 W/m^{2}K
α_{Al}	-1.8 μV/K	ε	0.6
λ_{Al}	237 W/mK	d_{spot}	1 mm
ρ_{Al}	2.65 x 10^{-8} Ωm	T_{amb}	20 ° C

within less than 10 ° C of each other, indicating good agreement with the simulated, thermal model, and measured values as is evident from Figure 6-19b. The open-circuit TEG voltage shown in Figure 6-19c and the output power under matched load conditions shown in Figure 6-19d also show good agreement between the simulated, thermal model, and measured values. The same is true for the Carnot efficiency in Figure 6-19e and the conversion efficiency in Figure 6-19f. Based on these graphs, it can be inferred that the thermal model developed in section 6.1 can closely predict the performance of the actual device.

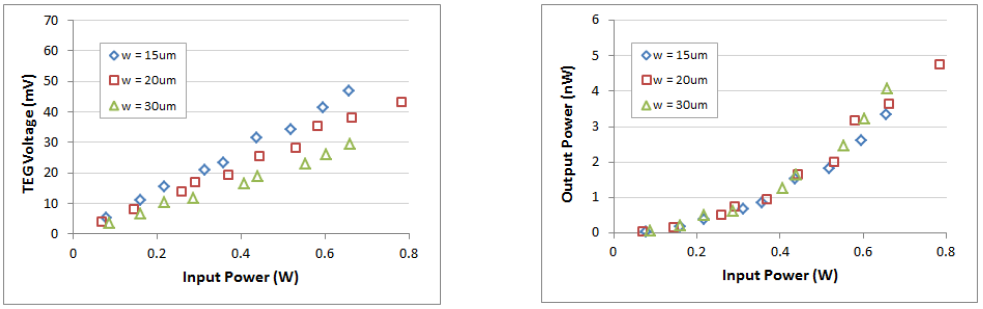
The effect of geometry on the performance of the fabricated TEG devices was also explored. Figure 6-20 shows the open-circuit TEG voltage and matched output power of the TEGs with different thermoelement lengths while keeping the width at 15 μm and the membrane diameter at 3 mm. As can be observed from the voltage graph, the output voltage increases as the thermoelement length is increased. This is attributed to the lower thermal conductance of the TEG, which contributes to a higher temperature difference across the thermoelements. The increase in thermoelement length also has a corresponding increase in the TEG's series electrical resistance. However, since the matched output power is squarely proportional to the TEG voltage and inversely proportional to the series electrical resistance, it can be inferred that the increase in output voltage dominates the trend in output power; thereby resulting in the output power increasing with increasing thermoelement length.



(a) (b)

Figure 6-20: Measured (a) open-circuit TEG voltage and (b) matched output power of TEGs implemented on a glass substrate with varying thermoelement lengths ($w = 15$ µm and $d_{mem} = 3$ mm)

Figure 6-21 shows the open-circuit TEG voltage and matched output power of the TEGs with different thermoelement widths while keeping the length at 500 µm and the membrane diameter at 3 mm. The TEGs with wider thermoelements would have a higher thermal conductance, resulting in a lower temperature difference across the device. As such, it can be observed from the voltage graph that the output voltage decreases as the thermoelement width is increased. The increase in thermoelement width also has a corresponding decrease in the TEG's series resistance. However, the combined effect of the decrease in both the output voltage and the series resistance of the TEG as the thermoelement width is increased have minimal effect on the resulting output power of the devices.

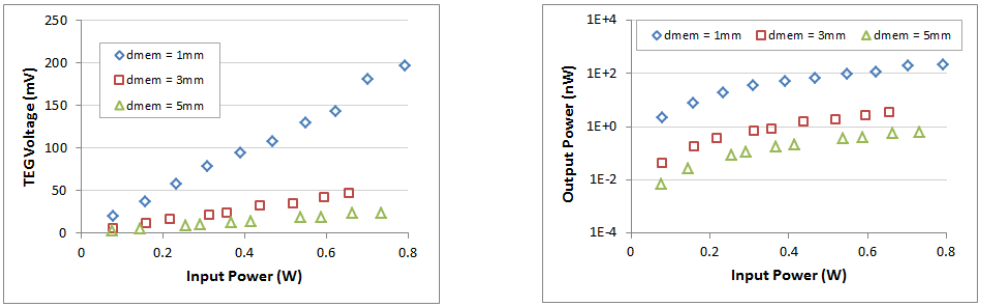


(a) (b)

Figure 6-21: Measured (a) open-circuit TEG voltage and (b) matched output power of TEGs implemented on a glass substrate with varying thermoelement widths ($l = 500$ µm and $d_{mem} = 3$ mm)

Figure 6-22 shows the open-circuit TEG voltage and matched output power of the TEGs with different membrane diameters while keeping the length at 500 µm and the width at

15 µm. The TEG with a larger membrane diameter has more thermocouples, which results in a higher thermal conductance of the TEG. This translates to a lower temperature difference across the device. This is evident from the voltage graph where the output voltage decreases as the membrane diameter is increased. The increase in the number of thermocouples as the membrane diameter is increased also results in an increase in the TEG's series electrical resistance. The combined effect of the decrease in output voltage and increase in the series resistance of the TEG as the membrane diameter is increased results in a dramatic decrease in the output power of the devices. This is shown in Figure 6-22b where the output power of the TEG with a 5 mm diameter membrane is 2 orders of magnitude less than the output power of the TEG with a 1 mm diameter membrane.



(a) (b)

Figure 6-22: Measured (a) open-circuit TEG voltage and (b) matched output power of TEGs implemented on a glass substrate with varying membrane diameters (l = 500 µm and w = 15 µm)

The efficiency factors of the ten fabricated TEGs on glass are listed in Table 6-6. The TEG with the best efficiency factor has a length of 200 µm, width of 15 µm, and membrane diameter of 5 mm. For the same membrane diameter and thermoelement width, the efficiency factor decreases as the thermoelement length increases. For the same membrane diameter and thermoelement length, the efficiency factor increases as the thermoelement width increases.

For more graphs showing the measurements performed on all ten TEGs fabricated on a glass substrate with the laser test set-up, the reader is referred to Appendix G.

Table 6-6: Efficiency factor of TEGs fabricated on a glass substrate. The TEG with the best efficiency factor is highlighted in **bold**.

l (μm)	w (μm)	d_{mem} (mm)	N	ϕ (μW/cm²K²)
200	15	1	31	1.58×10^{-4}
500	15	1	34	8.66×10^{-5}
200	15	3	108	5.74×10^{-4}
500	15	3	111	2.49×10^{-4}
500	20	3	91	2.78×10^{-4}
500	30	3	81	4.08×10^{-4}
1000	15	3	114	1.66×10^{-4}
200	**15**	**5**	**188**	$\mathbf{1.24 \times 10^{-3}}$
500	15	5	188	5.27×10^{-4}
1000	15	5	191	2.69×10^{-4}

6.4.2 Solar Simulator Testing

For the test set-up using a solar simulator, three different-sized uncoated N-BK7 plano-convex spherical lenses from Thorlabs, Inc. were used to focus the solar input onto the membrane of the TEG. Figure 6-23 shows a diagram of a plano-convex lens indicating its physical properties. The values of the variables labelled in Figure 6-23 for the three different lenses used are listed in Table 6-7. In a perfectly ideal spherical convex lens, all incoming rays parallel to the optic axis converge at the focal point. However, lenses inherently have spherical aberration, which is an optical effect that occurs due to the increased refraction of light rays when they strike a lens. This imperfection prohibits the lens from focusing all incident light onto the focal point, resulting in a minimum spot size. The minimum spot size can be calculated using the equation below[7]:

$$d_{spot,min} = \frac{D^3}{f^2}\left[\frac{n^2-(2n+1)k+(n+2)k^2/n}{32(n-1)^2}\right] \quad (6\text{-}31)$$

[7] http://www.crystech.com/technologysupport/OpticsDesign.htm#Spherical_Aberration

where n is the refractive index of the lens and k is the shape factor of the lens. For a properly oriented plano-convex lens with $n = 1.5$, the bracketed factor is 0.073. Using this equation, it can be calculated that the minimum spot sizes are 374 μm, 788 μm, and 957 μm for the lenses with diameters of 12.7 mm, 30 mm, and 50.8 mm, respectively. Note that these minimum spot sizes are only applicable in the case when all light rays strike the lens parallel to the optical axis. In the case of the solar simulator, however, light rays strike the lens from several angles, which makes it difficult to calculate the exact spot size. Ray tracing can be done to determine the spot size but this task would be too tedious and is not in the scope of this work.

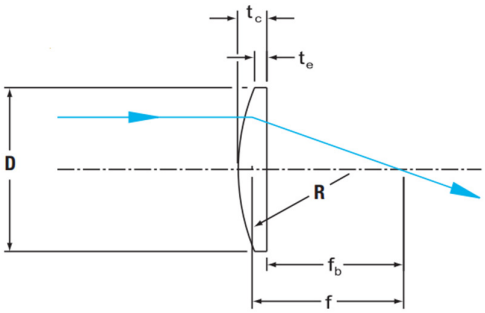


Figure 6-23: Diagram of plano-convex lens indicating the lens diameter (D), center thickness (t_c), edge thickness (t_e), radius of curvature (R), back focal length (f_b), and focal length (f).

It is then decided to estimate the minimum spot size for each lens experimentally. To do this, a blank piece of paper was taped on a prototyping board and the distance between the lens and the paper was adjusted incrementally until it is visually verified that the smallest possible spot size is achieved. A standard ruler was used to measure the actual spot size. Table 6-8 lists down the minimum spot size computed from equation 6-31, the actual spot size determined experimentally, and the distance of the actual spot to the flat

Table 6-7: Parameters of plano-convex lenses used in the test set-up. *CA* refers to the clear aperture as dictated by the lens mount used.

Lens Part No.	D (mm)	t_c (mm)	t_e (mm)	R (mm)	f_b (mm)	f (mm)	CA (mm)
LA1074	12.7	4	1.8	10.3	17.4	20	10.9
LA1102	30	7.3	2.5	25.8	45.2	50	28
LA1050	50.8	9.7	3	51.5	93.6	100	48.5

side of the lens. Note that the intensity of the spot size increases dramatically towards its center. This means that although the actual spot size might be larger than the membrane diameter of the TEG, a temperature difference can still occur across the thermoelements as an effect of this variation in the intensity of the spot size. An exception to this case is the use of the 50.8 mm diameter lens to focus solar light onto TEGs with membrane diameters of 1 mm. Since the minimum spot size of this lens due to spherical aberrations is 957 μm (very close to 1 mm), it is possible that non-idealities in the system can actually result in a spot size with maximum intensity at an area greater than the 1 mm spot size. If this is the case, then the thermoelements are also exposed at the same amount of intensity as the membrane, which would not result in any temperature difference across the device. This has been verified experimentally where no open-circuit voltage was measured for this lens and membrane diameter combination.

Table 6-8: Minimum and actual spot sizes for each of the three lenses used. The distance $d_{lens\text{-}to\text{-}spot}$ refers to the distance of the actual spot to the flat side of the lens.

Lens Part No.	D (mm)	$d_{spot,min}$ (μm)	$d_{spot,\ act}$ (mm)	$d_{lens\text{-}to\text{-}spot}$ (mm)
LA1074	12.7	374	3	10
LA1102	30	788	4	40
LA1050	50.8	957	7	85

The test set-up with the solar simulator is shown in Figure 6-24. An Abet Technologies Sun 3000 Solar Simulator Model 11016A was used to provide the solar input. As previously mentioned, a lens was used to focus the solar input onto the center of the device. Since there was no translation stage for the TEG in this set-up, alignment of the lens to the center of the TEG was done manually. This was first done through visual inspection and then verified by making sure that the output voltage is maximum at the current location by slowly moving the device systematically while monitoring the output voltage. Once the lens is satisfactorily aligned with the TEG, five measurements were performed on each device at 1 minute intervals. The voltage and current measurements awere monitored using a Keithley Model 2400 source meter and data was captured through LabView. Regrettably, there was not enough clearance in this set-up to allow the

measurement of the cold side temperature using an IR thermometer as was done in the laser test set-up.

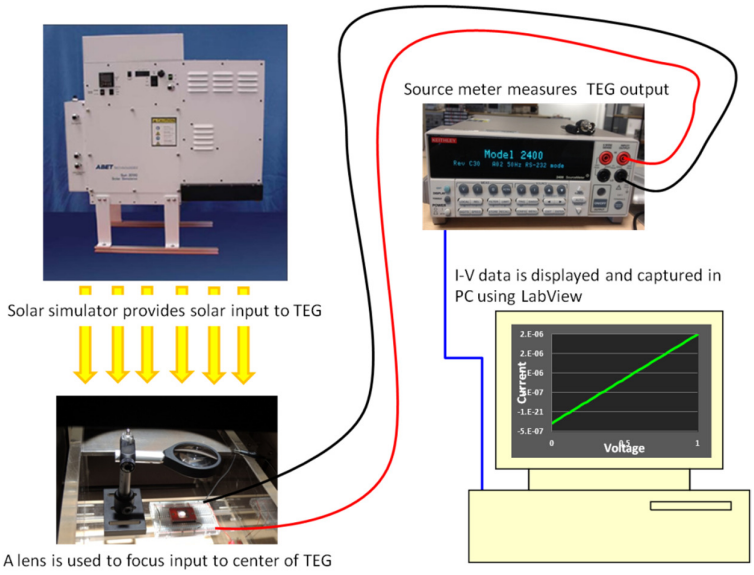


Figure 6-24: Measurement set-up with a solar simulator providing solar input and a Keithley Model 2400 source meter sensing the TEG's output.

The V-I characteristics of a solar TEG with varying lens diameters used in focusing solar light onto the center of the device are displayed in Figure 6-25. The x-intercept of the line defines the open-circuit voltage. It can be observed that the open circuit voltage increases as the lens diameter increases. This implies an increase in the input heat flux as the lens diameter is increased. The slope of the line slightly increases as the amount of solar input is increased, translating to a decrease in the TEG's electrical resistance. The reduction in TEG resistance can be attributed to an increase in the electrical conductivity of the heavily-doped HWCVD polysilicon brought about by an increase in temperature difference across the thermoelements as the amount of solar input increases.

Table 6-9 lists the open-circuit voltage, series resistance, temperature difference, and output power under matched load conditions for TEGs with varying thermoelement lengths. There are three sets of values for each parameter corresponding to the three plano-convex lenses used in the solar simulator measurements. Each parameter value is the result of the average of five measurements. As expected, the open-circuit voltage and output power increases as the thermoelement length increases. This is attributed to the increase in temperature difference across the device brought about by the decrease in

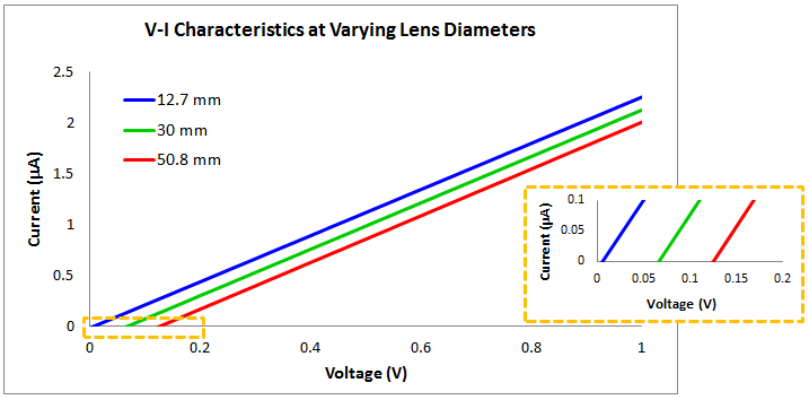


Figure 6-25: V-I characteristics of TEG implemented on a glass substrate with $l = 1000$ μm, $w = 15$ μm, $d_{mem} = 5$ mm, and $N = 191$ using three different lens diameters. Inset shows a zoomed-in plot of the intersection of the V-I characteristics with the x-axis which denotes the open-circuit voltages.

thermal conductance. For each TEG, the open-circuit voltage is expected to increase as the diameter of the lens used is increased. However, this is not the case for the TEG with a thermoelement length of 200 μm where the open-circuit voltage decreased from 19 mV to 16 mV when changing the lens from LA1102 ($D = 30$ mm) to LA1050 ($D = 50.8$ mm). This decrease in the open-circuit voltage can be explained by the variation in the intensity of the spot size. It can be argued that for the LA1050 lens, which has a measured spot size of 7 mm, the region where the intensity is maximum is greater than 3 mm in diameter. This translates to the effective thermoelement length being less than 200 μm, which could explain the decrease in voltage measurement. This assumption is further confirmed by the relatively small increase in output voltage for the other two TEG devices when changing lens from LA1102 to LA1050.

Table 6-9: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a glass substrate with varying thermoelement lengths ($w = 15$ μm and $d_{mem} = 3$ mm). For each of the three types of plano-convex lenses used, data is taken from the average of five measurements.

l (μm)	V_{TEG} (mV)			R_{TEG} (kΩ)			ΔT (°C)			P_{OUT} (nW)		
	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050
200	0.14	19.17	16.12	67.04	66.39	64.41	0.011	1.55	1.30	$7.4\text{x}10^{-5}$	1.38	1.01
500	0.58	43.98	47.31	161.25	159.11	155.35	0.046	3.45	3.71	$5.3\text{x}10^{-4}$	3.04	3.60
1000	2.04	86.25	92.11	260.35	259.11	255.04	0.156	6.59	7.04	$4.0\text{x}10^{-3}$	7.18	8.31

Table 6-10 lists the open-circuit voltage, series resistance, temperature difference, and output power under matched load conditions for TEGs with varying thermoelement widths. As the thermoelement width is increased, the voltage decreases while the output power increases. The decrease in voltage is consistent with the increase in thermal conductance brought about by increasing the thermoelement width. The increase in output power is mainly due to the decrease in the TEG's series resistance as the thermoelement width is increased. For each TEG, the output voltage and output power increases as the lens diameter is increased. This is expected as increasing the lens diameter means an increase in the input heat flux. It is also worthwhile to note that the increase in voltage when changing the lens from LA1074 ($D = 12.7$ mm) to LA1102 ($D = 30$ mm) is relatively larger than the increase in voltage when changing the lens from LA1102 ($D = 30$ mm) to LA1050 ($D = 50.8$ mm). This further reinforces the assumption from the results in Table 6-9 that for the LA1050 lens, the diameter of the region where the intensity of the spot size is maximum is greater than 3 mm, which is the diameter of the membrane of all devices listed in Table 6-10. For a specific lens, there is very little change observed with the temperature difference across the device as the width is varied.

Table 6-10: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a glass substrate with varying thermoelement widths ($l = 500$ µm and $d_{mem} = 3$ mm). For each of the three types of plano-convex lenses used, data is taken from the average of five measurements.

w (µm)	V_{TEG} (mV)			R_{TEG} (kΩ)			ΔT ($^\circ$C)			P_{OUT} (nW)		
	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050
15	0.58	43.98	47.31	161.25	159.11	155.35	0.046	3.45	3.71	$5.3\text{x}10^{-4}$	3.04	3.60
20	0.47	36.32	43.96	97.82	96.47	92.50	0.045	3.48	4.21	$5.6\text{x}10^{-4}$	3.42	5.22
30	0.21	32.00	33.55	54.49	54.17	52.47	0.023	3.44	3.61	$2.1\text{x}10^{-4}$	4.73	5.36

Table 6-11 lists the open-circuit voltage, series resistance, temperature difference, and output power under matched load conditions for TEGs with varying membrane diameters. The open-circuit voltage increases as the membrane diameter is increased for both LA1074 and LA1050 lenses. This is not the case for the LA1102 lens where the voltage decreases from 44 mV to 32 mV as the membrane diameter is increased from 3

mm to 5 mm. This can be explained by the actual spot size of the LA1102 lens which was measured to be around 4 mm. Since the actual spot size is greater than 3 mm, the thermoelements of the TEG with a membrane diameter of 3 mm experiences additional heating coming from the excess in the spot size of focused light. This translates to an additional contributor to the temperature difference across the device, which results in a higher output voltage. This effect is also evident in the output power where it is higher for a membrane diameter of 3mm when using the LA1102 lens.

For a complete list of the results from the solar simulator measurements performed on all ten TEGs fabricated on a glass substrate, the reader is referred to Appendix I.

Table 6-11: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a glass substrate with varying membrane diameters ($l = 500$ μm and $w = 15$ μm). For each of the three types of plano-convex lenses used, data is taken from the average of five measurements.

d_{mem} (mm)	V_{TEG} (mV)			R_{TEG} (kΩ)			ΔT (°C)			P_{OUT} (nW)		
	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050
1	0.32	17.40	---	43.61	43.32	---	0.081	4.46	---	$5.7\text{x}10^{-4}$	1.75	---
3	0.58	43.98	47.31	161.25	159.11	155.35	0.046	3.45	3.71	$5.3\text{x}10^{-4}$	3.04	3.60
5	3.12	32.02	65.40	220.26	219.90	218.51	0.144	1.48	3.03	0.011	1.16	4.89

6.5 Conclusions

This chapter covered the design, modelling, fabrication, and testing of the implementation of TEGs on a glass substrate. Although a significant amount of heat is lost through the substrate, this implementation has the advantage of a much simpler fabrication process. This thesis demonstrated that hot-wire polysilicon can be used as a thermoelectric material. To the researchers' best knowledge, this is the first study that explores the use of HWCVD films for thermoelectric applications. The modified thermal model for the TEG implementation on glass also showed good agreement with heat transfer simulations. Furthermore, the thermal model was able to closely predict the actual performance of the device based on the laser measurements performed.

Based on the laser measurements, a maximum TEG voltage per watt of input power for a TEG with a length of 500 μm, width of 15 μm, membrane diameter of 1 mm, and 34 thermocouples was generated. For a 1 W laser input with a spot size of 1 mm, the open circuit voltage is 247 mV, which translates to a temperature difference of 63 ˚ C across the thermoelements. The output power under matched load conditions is 347 nW with Carnot and conversion efficiencies at 17.3% and 0.0016%, respectively. The resulting efficiency factor for this TEG is 8.7×10^{-5} $\mu W/cm^2K^2$.

Of all the tested TEGs implemented on a glass substrate, the best efficiency factor is computed for a TEG that has a length of 200 μm, width of 15 μm, and membrane diameter of 5 mm. The best efficiency factor is found to be 1.24×10^{-3} $\mu W/cm^2K^2$.

Based on the solar simulator measurements, a maximum TEG voltage of 124 mV was generated, which translates to a temperature difference of 5.7 ˚ C across the thermoelements. This was achieved by using a 50.8 mm diameter plano-convex lens to focus solar input to a TEG with a length of 1000 μm, width of 15 μm, membrane diameter of 5 mm, and 191 thermocouples. The corresponding output power under matched load conditions is 8.8 nW.

Chapter 7: TEG Implementation on a SOI Substrate

As discussed in Chapter 5: there were problems encountered during the HFVPE step of the proposed fabrication process. To resolve this issue, two implementations of TEGs are investigated – one using a glass substrate and another one using a SOI substrate. The first implementation has been discussed in detail in the previous chapter. For this chapter, focus is given on the TEG implementation on a SOI substrate. The design and modifications to the thermal model are presented first, followed by a description of the fabrication process. Measurement results with a laser set-up and with a solar simulator are also presented and analyzed. Finally, the performance of TEGs implemented on a SOI substrate is compared with that of TEGs implemented on a glass substrate.

7.1 Design and Modelling of TEGs Implemented on a SOI Substrate

The problems encountered in the proposed TEG fabrication process involves HFVPE, which is performed to remove the buried oxide layer of the SOI wafer so as to optimize the heat flux path by suspending the device membrane and thermoelements. To do away with the HFVPE step, it was decided to retain the buried oxide layer and a thin part of the handle layer under the membrane and thermoelements in the structure of the TEG. This modified TEG design in shown in Figure 7-1. Although heat would be lost through the buried oxide and handle layers, the added structural stability that retaining these layers provides influenced the decision to modify the TEG design accordingly.

The effect of keeping the buried oxide under the membrane and thermoelements has been briefly described in section 4.3. To compensate for the heat lost through the buried oxide and handle layers, it is planned to use a SOI wafer with a thinner device layer for this implementation. A thinner device layer translates to thinner thermoelements and lower

thermal conductance; leading to a higher temperature difference across the thermoelements. Aside from adding structural stability, another reason for keeping a thin part of the handle layer under the membrane and thermoelements is to manage the etching non-uniformity during the chip-level backside DRIE step. Since a large area of the silicon handle layer is exposed, the tendency is for etching to be non-uniform; thus increasing the possibility of damaging devices when certain areas are over-etched. In this regard, it was decided to thin out the SOI handle layer under the membrane and thermoelements to about 5 µm.

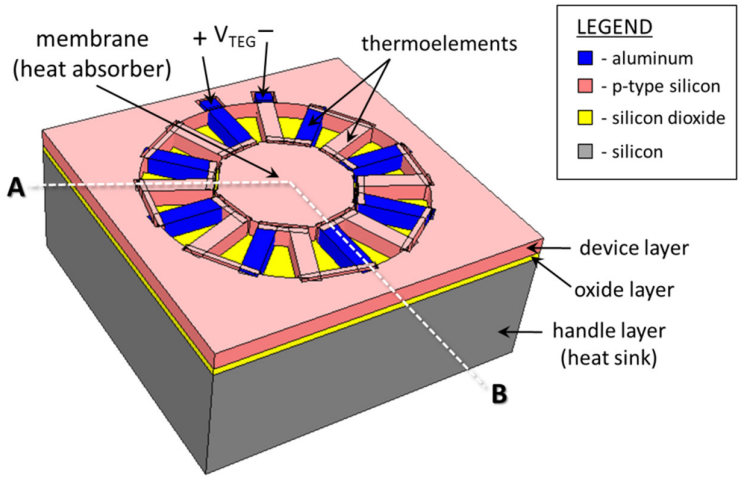


Figure 7-1: Modified TEG design on a SOI substrate with buried oxide layer and a thin part of the handle layer retained for added structural stability.

Figure 7-2 shows a thermal equivalent circuit of the TEG in Figure 7-1. Aside from adapting the calculation of thermal conductances to the geometry of the device, heat losses through the buried oxide layer and the thin handle layer under the membrane and thermoelements are also taken into account and highlighted in Figure 7-2. K_{BOX} is the thermal conductance of the portion of the buried oxide layer directly below the heated area of the device. K_{HAN} is the thermal conductance of the portion of the handle layer that is also directly below the heated area of the device. The temperature node, T_{HAN}, is the temperature at the bottom of the thinned area of the handle layer. Heat lost through the bottom of the thinned handle layer due to convection is also represented in this modified thermal model as $Q_{CONV,HAN}$.

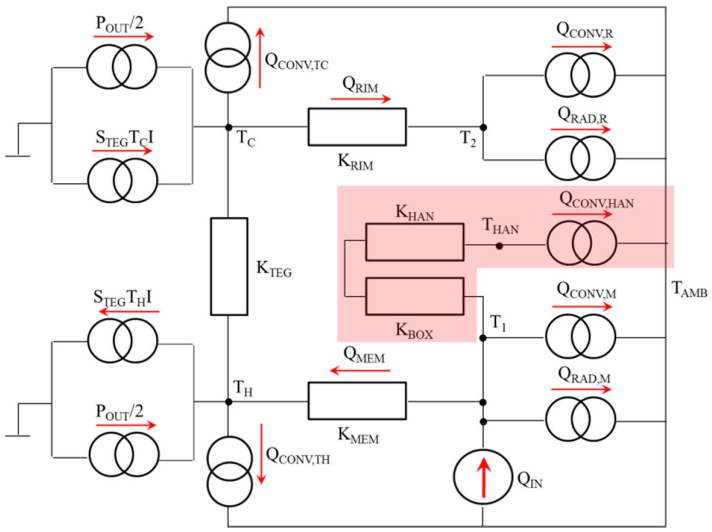


Figure 7-2: Thermal equivalent model of TEG implemented on a SOI substrate with buried oxide layer retained. T_{HAN} is the temperature at the bottom of the thinned area of the handle layer, K_{BOX} and K_{HAN} are the thermal conductances directly below the heated area of the device of the buried oxide and handle layers, respectively, and $Q_{CONV,HAN}$ represents heat lost due to convection at the bottom of the thinned handle layer.

Referring to each temperature node in Figure 7-2, the heat balance equations then become:

at T_1: $$Q_{IN} = Q_{MEM} + Q_{RAD,M} + Q_{CONV,M} + (K_{BOX} + K_{HAN})(T_1 - T_{HAN}) \tag{7-1}$$

at T_H: $$Q_{MEM} = K_{TEG}(T_H - T_C) + S_{TEG}T_H I - \frac{1}{2}P_{OUT} + Q_{CONV,TH} \tag{7-2}$$

at T_C: $$Q_{RIM} = K_{TEG}(T_H - T_C) + S_{TEG}T_C I + \frac{1}{2}P_{OUT} - Q_{CONV,TC} \tag{7-3}$$

at T_2: $$Q_{RIM} = Q_{RAD,R} + Q_{CONV,R} \tag{7-4}$$

at T_{HAN}: $$Q_{CONV,HAN} = (K_{BOX} + K_{HAN})(T_1 - T_{HAN}) \tag{7-5}$$

The heat lost through the bottom of the substrate due to convection is given by:

$$Q_{CONV,HAN} = h_{conv}A_{HAN}(T_{HAN} - T_{AMB}) \tag{7-6}$$

where A_{HAN} refers to the surface area of the bottom of the thinned handle layer.

Considering heat flow through K_{MEM} and K_{RIM}, the same equations as in section 4.3 for T_H and T_C in terms of T_1 and T_2, respectively, can be derived.

$$T_H = T_1 - {}^{Q_{MEM}}/_{K_{MEM}} \tag{7-7}$$

$$T_C = T_2 + {}^{Q_{RIM}}/_{K_{RIM}} \tag{7-8}$$

Incorporating equations 4-17 to 4-22 and equations 7-6 to 7-8 into the heat balance equations in equations 7-1 to 7-5, and also noting that $\Delta T = T_H - T_C$, the following expressions can be derived:

$$\begin{aligned} Q_{IN} = Q_{MEM} + \varepsilon\sigma A_{MEM}\left({T_1}^4 - {T_{AMB}}^4\right) + h_{conv}A_{MEM}(T_1 - T_{AMB}) \\ + (K_{BOX} + K_{HAN})(T_1 - T_{HAN}) \end{aligned} \tag{7-9}$$

$$Q_{MEM} = K_{TEG}\Delta T + S_{TEG}\left(T_1 - \frac{Q_{MEM}}{K_{MEM}}\right)I - \frac{1}{2}P_{OUT} + h_{conv}A_{TEG}\left(T_1 - \frac{Q_{MEM}}{K_{MEM}} - T_{AMB}\right) \tag{7-10}$$

$$Q_{RIM} = K_{TEG}\Delta T + S_{TEG}\left(T_2 + \frac{Q_{RIM}}{K_{RIM}}\right)I + \frac{1}{2}P_{OUT} - h_{conv}A_{TEG}\left(T_2 + \frac{Q_{RIM}}{K_{RIM}} - T_{AMB}\right) \tag{7-11}$$

$$Q_{RIM} = \varepsilon\sigma A_{RIM}\left({T_2}^4 - {T_{AMB}}^4\right) + h_{conv}A_{RIM}(T_2 - T_{AMB}) \tag{7-12}$$

$$h_{conv}A_{HAN}(T_{HAN} - T_{AMB}) = (K_{BOX} + K_{HAN})(T_1 - T_{HAN}) \tag{7-13}$$

From equation 7-13, an expression for T_{HAN} in terms of T_1 can be derived:

$$T_{HAN} = \frac{(K_{BOX} + K_{HAN})T_1 + h_{conv}A_{HAN}T_{AMB}}{h_{conv}A_{HAN} + K_{BOX} + K_{HAN}} \tag{7-14}$$

Substituting T_{HAN} in equation 7-9 with equation 7-14 gives:

$$\begin{aligned} Q_{IN} = Q_{MEM} + \varepsilon\sigma A_{MEM}\left({T_1}^4 - {T_{AMB}}^4\right) + h_{conv}A_{MEM}(T_1 - T_{AMB}) \\ + (K_{BOX} + K_{HAN})\left(T_1 - \frac{(K_{BOX} + K_{HAN})T_1 + h_{conv}A_{HAN}T_{AMB}}{h_{conv}A_{HAN} + K_{BOX} + K_{HAN}}\right) \end{aligned} \tag{7-15}$$

Referring back to the thermal equivalent circuit in Figure 7-2, the temperature difference between T_1 and T_2 as can be expressed as:

$$T_1 - T_2 = \frac{Q_{MEM}}{K_{MEM}} + \Delta T + \frac{Q_{RIM}}{K_{RIM}} \tag{7-16}$$

In equations 7-10 and 7-11, the current I and output power P_{OUT} can be expressed in terms of ΔT using equations 4-10 and 4-11, respectively. Hence, combining equations 7-10 and 7-15 gives a fourth-order polynomial in T_1 with only T_1 and ΔT as unknown variables.

$$\varepsilon\sigma A_{MEM}{T_1}^4 + C_3T_1 + C_4 = 0 \tag{7-17}$$

where
$$C_3 = S_{TEG}I + h_{conv}(A_{TEG} + A_{MEM}) + (K_{BOX} + K_{HAN})\left(1 - \frac{(K_{BOX} + K_{HAN})}{h_{conv}A_{HAN} + K_{BOX} + K_{HAN}}\right) \tag{7-18}$$

and
$$C_4 = K_{TEG}\Delta T - S_{TEG}\frac{Q_{MEM}}{K_{MEM}}I - \frac{1}{2}P_{OUT} - \varepsilon\sigma A_{MEM}{T_{AMB}}^4 - \frac{(K_{BOX} + K_{HAN})h_{conv}A_{HAN}T_{AMB}}{h_{conv}A_{HAN} + K_{BOX} + K_{HAN}} - h_{conv}\left(\frac{Q_{MEM}}{K_{MEM}}A_{TEG} + (A_{TEG} + A_{MEM})T_{AMB}\right) - Q_{IN} \tag{7-19}$$

Similar to the procedure discussed in section 4.3, four expressions for T_1 as functions of ΔT can be derived by solving the roots of equation 7-17 using Ferrari's solution to a quartic function. By plugging in a positive value for ΔT and calculating the roots, the expression that gives a real and positive value for T_1 is selected. Similarly, equations 7-11 and 7-12 can be combined to form the following fourth-order polynomial equation:

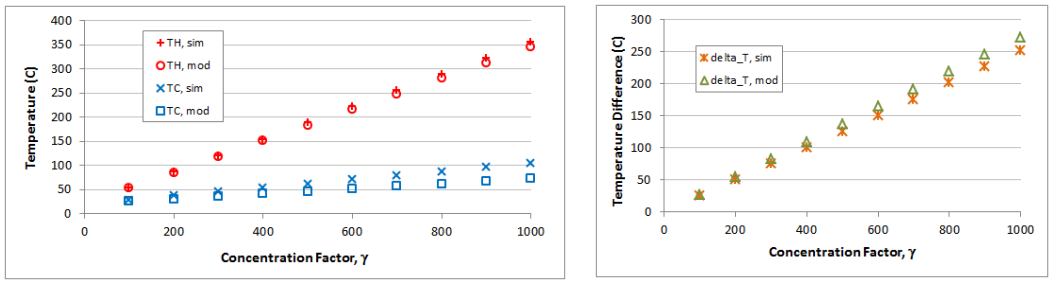
$$\varepsilon\sigma A_{RIM}{T_2}^4 + (h_{conv}(A_{TEG} + A_{RIM}) - S_{TEG}I)T_2 + C_2 = 0 \tag{7-20}$$

where
$$C_2 = -K_{TEG}\Delta T - S_{TEG}\frac{Q_{RIM}}{K_{RIM}}I - \frac{1}{2}P_{OUT} - \varepsilon\sigma A_{RIM}{T_{AMB}}^4 + h_{conv}\left(\frac{Q_{RIM}}{K_{RIM}}A_{TEG} - (A_{RIM} + A_{TEG})T_{AMB}\right) \tag{7-21}$$

The roots of equation 7-20 can then be solved and T_2 can be expressed in terms of ΔT. The derived equations for T_1 and T_2 can then be substituted into equation 7-16, which gives an equation with only ΔT as the unknown variable. The temperature difference

across the thermoelements, ΔT, can then be solved numerically using Matlab. The Matlab program used to solve for ΔT can also be found in Appendix A.

Figure 7-3 illustrates how the modified thermal model for TEGs implemented on a SOI substrate compares with 3-dimensional heat transfer simulations. The plot shows trends in hot and cold side temperatures, as well as in the temperature difference, with respect to the solar concentration factor. The temperatures T_H and T_C obtained from the model are lower than those taken from simulations by up to 10 ˚C and 32 ˚C, respectively. As for the temperature difference, the thermal model computes up to 21 ˚C larger temperature difference compared to that obtained from simulations. In the simulations, the SOI device layer is represented as bulk silicon where the thermal conductivity is constant with temperature. This is based on the study by (Asheghi et al. 1998) which showed that thermal simulations of SOI transistors with device layers thicker than about 1.5 µm should use the thermal conductivity of bulk silicon. Hence, the slight decrease in the temperature difference obtained from the simulations can be attributed to the effect of the increase in thermal conductivity of aluminum as temperature is increased.

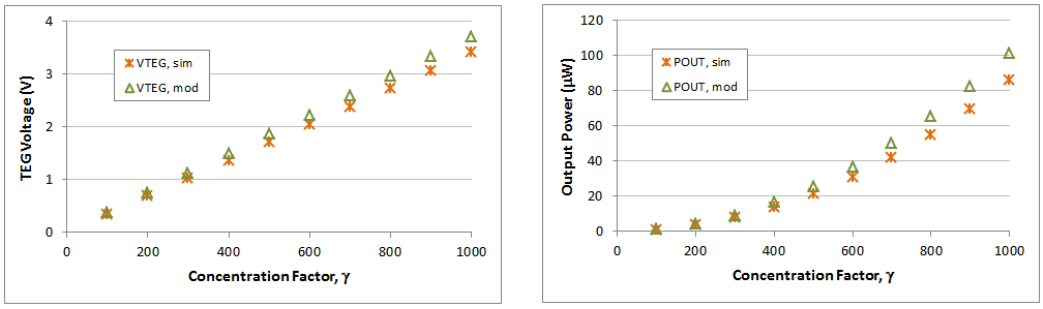


(a) (b)

Figure 7-3: (a) Hot (T_H) and cold (T_C) side temperatures and (b) temperature difference ΔT between simulations (*sim*) and thermal model (*mod*) of TEG on a SOI substrate with varying solar concentration ratio. TEG has the following parameters: $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, $N = 34$, $\varepsilon = 0.6$, $h_{conv} = 50$ W/m^{2}K, $\alpha_{mem} = 0.5$, $\tau_{lens} = 1$, and $d_{spot} = 1$ mm.

As a consequence of the slightly larger temperature difference derived from the thermal model, the generated open-circuit voltage and matched output power from the thermal model are also slightly higher than those obtained from simulations. These relationships

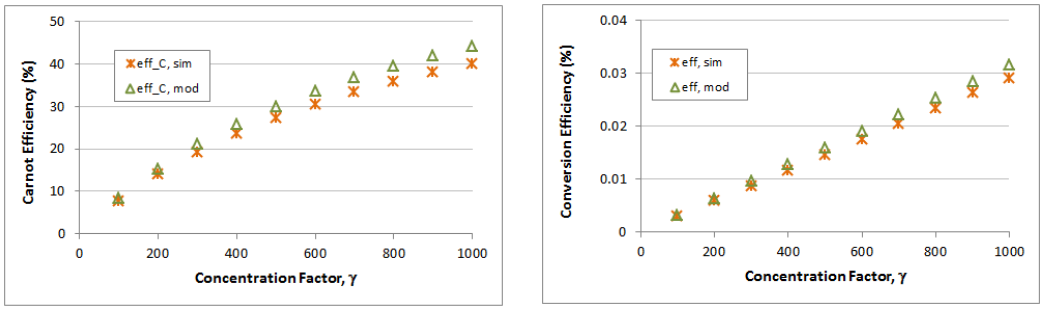
are shown in Figure 7-4. In addition, both output voltage and output power increases with increasing solar concentration ratio as expected.



(a) (b)

Figure 7-4: (a) Open-circuit TEG voltage and (b) matched output power between simulations (*sim*) and thermal model (*mod*) of TEG on a SOI substrate with varying solar concentration ratio. TEG has the following parameters: $l = 500$ μm, $w = 15$ μm, $d_{mem} = 1$ mm, $N = 34$, $\varepsilon = 0.6$, $h_{conv} = 50$ W/m^{2}K, $\alpha_{mem} = 0.5$, $\tau_{lens} = 1$, and $d_{spot} = 1$ mm.

The trends in both Carnot and conversion efficiencies are shown in Figure 7-5. The efficiencies derived from the thermal model are higher than those obtained from simulations. As expected, both Carnot and conversion efficiencies increase with increasing solar concentration ratio. This verifies that there is significant improvement in the efficiency of the device as solar energy is concentrated into the hot side of the TEG. The thermoelectric figure-of-merit of the materials used is about 5x10^{-6} K^{-1}, which is 5 times



(a) (b)

Figure 7-5: (a) Carnot efficiency and (b) conversion efficiency between simulations (*sim*) and thermal model (*mod*) of TEG on a SOI substrate with varying solar concentration ratio. TEG has the following parameters: $l = 500$ μm, $w = 15$ μm, $d_{mem} = 1$ mm, $N = 34$, $\varepsilon = 0.6$, $h_{conv} = 50$ W/m^{2}K, $\alpha_{mem} = 0.5$, $\tau_{lens} = 1$, and $d_{spot} = 1$ mm.

that of the thermoelectric figure-of-merit of the materials used in the TEG implemented on a glass substrate. As a result, the conversion efficiency improved by about 40 times when the TEG is implemented on a SOI substrate. The conversion efficiency is also improved by about 10 times when the solar concentration ratio is increased from 100 to 1000 for both simulations and thermal model.

7.2 TEG Fabrication Process on a SOI Substrate

The fabrication process for a TEG implemented on a SOI substrate is illustrated in Figure 7-6. Note that to carry out this modified fabrication process, a new mask was created for the lithography of the SOI backside where areas under the membrane and thermoelements are to be exposed for etching. Since the dimensions of the exposed areas are relatively large, a high-resolution acetate mask is sufficient to translate the patterns into the wafer. An advantage of using an acetate mask is that it is cheaper and faster to manufacture. The acetate mask was ordered through Micro Lithography Services Limited[8].

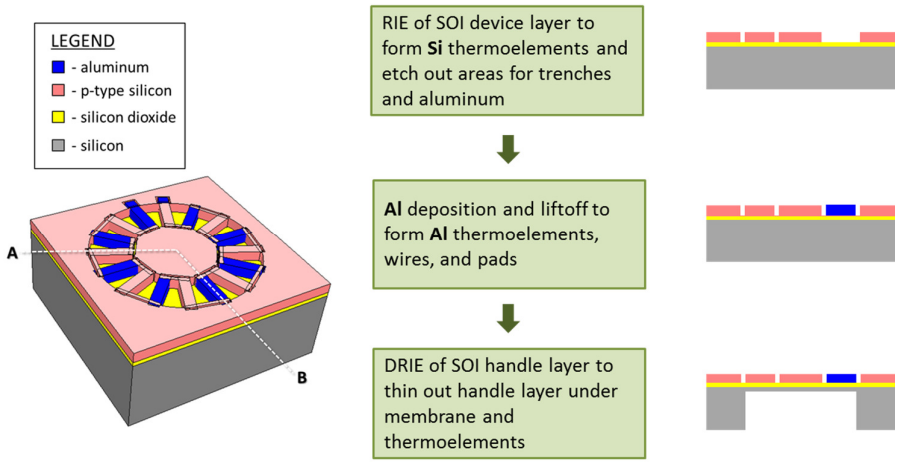


Figure 7-6: Overview of TEG fabrication process using a SOI wafer with p-type silicon and aluminum as thermoelement materials. Cross-sectional view is along AB.

[8] http://www.microlitho.co.uk

The fabrication process starts with a 6 inch SOI wafer from Ultrasil Corporation with the following thicknesses: 500 ± 15 μm handle layer, 400 nm buried oxide layer, and 3 ± 0.5 μm device layer. The handle layer is boron-doped with a resistivity of 1-30 Ω-cm while the device layer is also boron-doped and has a resistivity of 0.005-0.02 Ω-cm. To facilitate discussion, this section is divided into the six major steps of the fabrication process which are:

1) Hardmask patterning of both front and back sides.
2) Frontside RIE.
3) Aluminum deposition and lift-off.
4) Wafer-level backside DRIE.
5) Wafer dicing.
6) Chip-level backside DRIE and wirebonding.

For a more detailed outline of the device fabrication on a SOI wafer, the reader is referred to Appendix F.

7.2.1 Hardmask Patterning of Front and Back Sides

To protect the device layer during backside patterning, a silicon dioxide hardmask was used at the frontside. Since the device layer for this SOI wafer is thinner than the one used in section 5.3.1, a thinner mask was also used for the frontside. For this hardmask, a 500 nm thick SiO_2 based on silane (SiH_4) was deposited by using an OIPT SYS100 capacitive-based PECVD reactor. The gas flow rates of silane-based oxide were 4.2 sccm SiH_4, 350 sccm N_2O, and 80 sccm N_2. The deposition was performed at a table temperature of 350 ° C, chamber pressure of 1000 mTorr, and RF power of 20 W. The deposition rate was about 1 nm/s. After deposition of 500 nm SiO_2 at the frontside, the wafer was immediately rinsed in isopropyl alcohol (IPA) and blow-dried using a N_2 gun. Then, a 3.6 μm thick silane-based SiO_2 was deposited at the backside.

After coating both front and back sides with PECVD oxide, the wafer was cleaned in fuming nitric acid (FNA) for 10 minutes, followed by 3 quick dump rinse (QDR) cycles. Then, the wafer was spin-dried using an automated spin rinse dryer. After drying, the

wafer was dehydrated in a 120 ˚C oven for 30 minutes in preparation for frontside lithography.

Lithography of 6 µm thick AZ9260 positive photoresist was then performed using the same steps described in section 5.3.1. At this point, the photoresist was patterned with the first mask, which defines the areas for the p-type silicon thermoelements, the rim, and the perforated membrane.

After lithography, the wafer was placed inside the chamber of an OIPT SYS380 inductively-coupled plasma (ICP) etcher for SiO_2 etching. The gases used for this purpose were 37.4 sccm CHF_3, 34 sccm C_4F_8, and 8.5 sccm O_2. Etching was done at a table temperature of 15 ˚C, chamber pressure of 7 mTorr, RF power of 100 W, and ICP power of 1500 W. To avoid the photoresist from burning, helium was introduced into the chamber at a pressure of 10 T. The SiO_2 etch rate was approximately 150 nm/min and its selectivity to AZ9260 was about 1:1.

Once the exposed PECVD oxide was completely etched, the photoresist was stripped in O_2 plasma using a Tepla 300 asher and once again, FNA-cleaned in preparation for the second lithography step. Similar to the first lithography step, the wafer was first dehydrated in a 120 ˚C oven for 30 minutes. Then, the same procedure of photoresist spinning, exposure, and development was performed on the SOI backside. The PECVD SiO_2 at the backside was etched using the Plasmatherm Versaline Deep Silicon Etcher as it was observed that it etches oxide more uniformly than the ICP etcher in cases where larger areas of oxide are exposed. The etching parameters used for this purpose were as follows: 50 sccm CF_4, chamber pressure of 5 mT, high-frequency bias of 100 W, and ICP power of 400 W. The SiO_2 etch rate was about 180 nm/min with a selectivity to AZ9260 photoresist of 3:4.

7.2.2 Frontside RIE

Once the front and back hardmasks were patterned, the exposed silicon device layer was etched up to the buried oxide layer using the OIPT RIE tool. The RIE conditions for this

process were: 18 sccm SF_6, 22 sccm O_2, table temperature of 20 ˚C, chamber pressure of 30 mTorr, and RF power of 100 W. Under these settings, the silicon etch rate was 280 nm/min whereas the SiO_2 etch rate was 33 nm/min, making it an appropriate masking material with a selectivity of about 8.5. Then, the remaining oxide mask at the frontside was stripped in 7:1 HF solution for 2 minutes.

7.2.3 Aluminum Deposition and Lift-off

The steps performed in the deposition and lift-off of aluminum on the SOI substrate is the same as the one discussed in section 5.3.4. The only difference is that instead of depositing 6 μm thick aluminum, only 3 μm thick was deposited, which is of the same order in thickness as that of the SOI device layer.

7.2.4 Wafer-level Backside DRIE

After depositing aluminum, wafer-level backside DRIE was performed where about 450 μm of the handle layer was etched using the DRIE conditions listed in Table 5-4. The remaining 50 μm of the handle layer ensures that the devices are mechanically able to withstand the stress of the next step, which is wafer dicing.

7.2.5 Wafer Dicing

The next step in the TEG fabrication process on a SOI substrate involved dicing the wafer to obtain separate TEG chips from the wafer using a dicing saw. To protect the patterned thermoelements prior to dicing, S1813 photoresist was spun onto the wafer at 5000 rpm for 30 seconds. Since the handle layer at this point has been significantly etched, a vacuum error occurs with the spinner when the SOI wafer was placed on the spinner chuck. To resolve this, the back of the SOI wafer was attached to a blue adhesive tape prior to spinning the S1813 photoresist. After spinning, the tape was carefully removed and the wafer was baked at 115 ˚C for 60 seconds. The wafer was then diced to separate the TEG chips from each other. After separation, the photoresist was stripped in acetone and each chip was rinsed in IPA and DI water then dried using a N_2 gun.

7.2.6 Chip-level Backside DRIE and Wirebonding

Once the TEG chips were separated from each other, the handle layer under the membrane and thermoelements were thinned out further to a thickness of about 5 μm. The DRIE settings used in this step is listed in Table 7-1. The silicon etch rate was about 5 μm/min and each TEG chip was placed on top of a silicon wafer coated with PECVD SiO_2. Each chip first underwent a 5-minute etching step. After which, etching was done at 1 minute intervals and the TEG chip was visually inspected under an optical microscope in between etching steps to keep track of damages that may occur due to the stress that the bombardment of etching ions may impose on the fragile membrane and thermoelements. It was found that devices with large membranes (above 5mm in diameter) tend to get damaged more easily.

Table 7-1: Settings for chip-level backside DRIE.

	Deposition	**Etch A**	**Etch B**
SF_6 (sccm)	0	150	150
C_4F_8 (sccm)	150	0	0
Ar (sccm)	30	30	30
Pressure (mT)	25	40	40
ICP Power (W)	2000	2000	2500
LF Bias (V)	10	250	10
Morphing Factor	1	1	1
Cycle Time (s)	2	1.5	2
Spool Temp (° C)	180		
Lid Temp (° C)	150		
Liner Temp (° C)	70		
Electrode Temp (° C)	15		
Helium Pressure (mT)	4000		

Once the handle layer of the TEG chip was suitably thinned to about 5 μm, it was bonded to a chip carrier and the voltage pads were wire bonded onto a chip carrier using a Delvotek wirebonder.

7.3 SOI Device Layer Characterization

The same procedures discussed in section 6.3 in extracting the electrical and thermal properties of HWCVD polysilicon were used for determining the properties of the SOI device layer. The silicon material of the SOI device layer is the thermoelement that significantly affects the performance of the device. Once again, the electrical and thermal properties of aluminum are assumed to be those listed in Table 4-2 where it has higher thermal conductivity, lower electrical resistivity and lower Seebeck coefficient than silicon.

The electrical resistivity extracted from the fabricated Van der Pauw structure is first presented. This is then followed by results of measurements performed on planar and cantilever structures, which allows the derivation of the Seebeck coefficient and thermal conductivity, respectively. Lastly, the contact resistance is obtained from measurements made on the Kelvin structures.

7.3.1 Electrical Resistivity

The same two circuits shown in Figure 6-12 were used to derive the two characteristic resistances R_A and R_B of the fabricated silicon Van der Pauw structure. Table 7-2 lists the results of measurements performed on the silicon Van der Pauw structure fabricated on a SOI substrate.

Table 7-2: Results of measurements made on silicon Van der Pauw structure fabricated on a SOI substrate.

Material	I_{12} (mA)	V_{43} (mV)	R_A (Ω)	I_{23} (mA)	V_{14} (mV)	R_B (Ω)	R_S (Ω/□)	t (μm)	resistivity (Ω-m)
HWCVD poly-Si	9.057	61	6.735	9.06	58	6.472	29.81	3	**8.94×10^{-5}**

7.3.2 Seebeck Coefficient

The circuit shown in Figure 6-13 was also used for determining the Seebeck coefficient of the fabricated silicon planar structure. The initial resistance of the two temperature monitors, R_{t1O} and R_{t2O}, were measured as 10 and 24 ohms, respectively. Table 7-3 lists

down the measurement results obtained on a fabricated silicon planar structure using three different series resistors. The average Seebeck coefficient of the p-type silicon device layer is calculated to be 397 μV/K.

Table 7-3: Results of measurements made on a silicon planar structure fabricated on a SOI substrate.

R_{series} (Ω)	V_{planar} (mV)	R_{t1} (Ω)	R_{t2} (Ω)	ΔT (K)	α (μV/K)
296	56.7	14.3	19.5	143.94	393.91
987	7.9	10.6	23.4	19.82	398.59
1980	1.7	10.1	23.8	4.27	398.12

7.3.3 Thermal Conductivity

The circuit shown in Figure 6-14 was also used for determining the thermal conductivity of p-type silicon device layer using the cantilever structure. The initial resistance of the temperature monitor, R_{tO}, was measured as 40.8 Ω whereas the resistance of the cantilever structure was measured to be 300 Ω.

Table 7-4 lists down the measurement results obtained on a silicon cantilever structure using three different series resistors. The average thermal conductivity of the p-type silicon is calculated to be 146 W/mK.

Table 7-4: Results of measurements made on a silicon cantilever structure fabricated on a SOI substrate.

R_{series} (Ω)	V_{canti} (V)	R_t (Ω)	P (mW)	ΔT (K)	λ (W/mK)
296	4.12	57.8	14.145	97.12	145.64
987	1.47	43.1	1.801	13.14	137.06
1980	0.846	41.6	0.705	4.57	154.27

7.3.4 Contact Resistance

The same circuit shown in Figure 6-15 with the Kelvin structure was used for measuring contact resistance. The measured voltage V_{23} was 2.32 mV and the current I_{14} was 21.48 mA. Using equation 6-29, the measured contact resistance of the Kelvin structure fabricated on a SOI substrate is 0.108 Ω, translating to a specific contact resistance of 97.2 Ω–μm^2.

7.4 Measurement Results

For the fabrication of TEGs on a SOI substrate, attention is directed to the TEGs with 3 μm wide isolation trenches as these would have the same geometry as the ones tested for TEGs on glass. There are two sets of the ten distinct TEGs with 3 μm wide isolation trenches across a 6 inch wafer. Of the 20 TEGs, only six TEGs are fabricated successfully. The other 14 were damaged during the chip-level backside DRIE step where the non-uniformity in etching caused specific areas to be over-etched. Table 7-5 lists the dimensions of the successfully fabricated TEGs on SOI.

Table 7-5: List of TEGs successfully fabricated on a SOI substrate.

l (μm)	w (μm)	d_{mem} (mm)	N
200	15	1	31
500	15	1	34
500	15	3	111
500	30	3	81
1000	15	3	114
200	15	5	188

Similar to the TEGs implemented on a glass substrate, two measurements set-ups were also performed on the TEGs implemented on a SOI substrate. First, the TEGs were tested using a laser set-up where the input power is varied at a constant spot size. This allows depiction of a scenario where there is precise control of the solar spot size and the variation in input power represents varying the concentration ratio. The second set-up involved testing the TEGs using a solar simulator and three lenses with different diameters to emulate the environment with which the devices are to be used as solar TEGs with solar concentration.

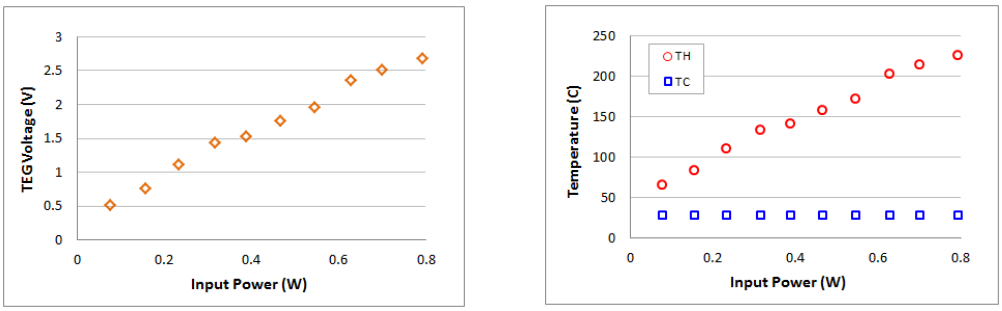
7.4.1 Laser Testing

The same laser testing set-up discussed in section 6.4.1 was used for testing the fabricated TEGs on a SOI substrate. In this set-up, the laser power was modulated by using a NDF wheel. At each change in input power, the corresponding output voltage was measured with a volt meter. An infrared thermometer was also used to measure the

temperature at the cold side of the TEG for each iteration of the input power. Ten measurements were taken for each TEG.

Figure 7-7a shows a plot of the measured open-circuit TEG voltage with varying laser input power for a TEG with $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 34$. Taking the slope of this graph, it can be derived that the generated voltage is about 3.06 V/W. This is 12 times better than the TEG on glass with the same dimensions. Since the Seebeck coefficient of the materials are known ($\alpha_{Si} = 397$ µV/K and $\alpha_{Al} = -1.8$ µV/K), then the temperature difference can be computed as:

$$\Delta T = \frac{V_{TEG}}{N(\alpha_{Si} - \alpha_{Al})} \tag{7-22}$$



(a) (b)

Figure 7-7: Measured (a) open-circuit TEG voltage and (b) hot and cold side temperatures versus laser input power of a TEG implemented on a SOI substrate with these dimensions: $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 34$.

As previously discussed, the cold side temperature, T_C, was measured using an infrared thermometer. The hot side temperature, T_H, is then calculated as the sum of T_C and ΔT. Figure 7-7b shows a plot of the hot and cold side temperatures of the same TEG. As in the case of the TEGs on glass, it can be observed that the cold side temperature is almost constant at about 28 ° C. Applying the thermal model developed in section 7.1, it was determined that to keep the cold side temperature close to this value, the heat transfer coefficient due to convection must be around 250 W/m^{2}K, which correspond to forced convection in air.

To compare the laser measurements with simulations and the thermal model developed earlier in this chapter, Table 7-6 lists down the parameters to represent the conditions of the laser set-up. Figure 7-8 shows a comparison between the simulated, thermal model, and measured parameters. From Figure 7-8a, the hot and cold side temperatures derived from the thermal model is within 5.9% and 1.2%, respectively, of those obtained from measurements. The simulated cold side temperature, however, deviates from the measurements and the thermal model as the input power increases. This results in the simulated temperature difference ΔT being up to 30 ˚C lower than the thermal model and the measured values as is evident from the temperature difference graphs in Figure 7-8b. The open-circuit TEG voltage shown in Figure 7-8c and the output power under matched load conditions shown in Figure 7-8d also show good agreement between the simulated, thermal model, and measured values. Note that due to the deviation of the simulated temperature difference at higher input power, the simulated values of the open-circuit voltage and output power are also lower than the thermal model and measured data at higher input power levels. The same is true for the Carnot efficiency in Figure 7-8e and the conversion efficiency in Figure 7-8f. Based on these graphs, it can be inferred that the thermal model developed in section 7.1 can reasonably predict the performance of the actual device, with the temperature difference derived from the thermal model being within 3.5% of the measured value when the input power is 800 mW.

Table 7-6: Parameters used in thermal model of TEG on a SOI substrate to emulate conditions in laser test set-up.

Parameter	Value	Parameter	Value
α_{Si}	397 µV/K	λ_{SiO2}	1.4 W/mK
λ_{Si}	146 W/mK	α_{mem}	0.63
ρ_{Si}	8.94 x 10^{-5} Ωm	h_{conv}	250 W/m^{2}K
α_{Al}	-1.8 µV/K	ε	0.6
λ_{Al}	237 W/mK	d_{spot}	1 mm
ρ_{Al}	2.65 x 10^{-8} Ωm	T_{amb}	20 ˚C

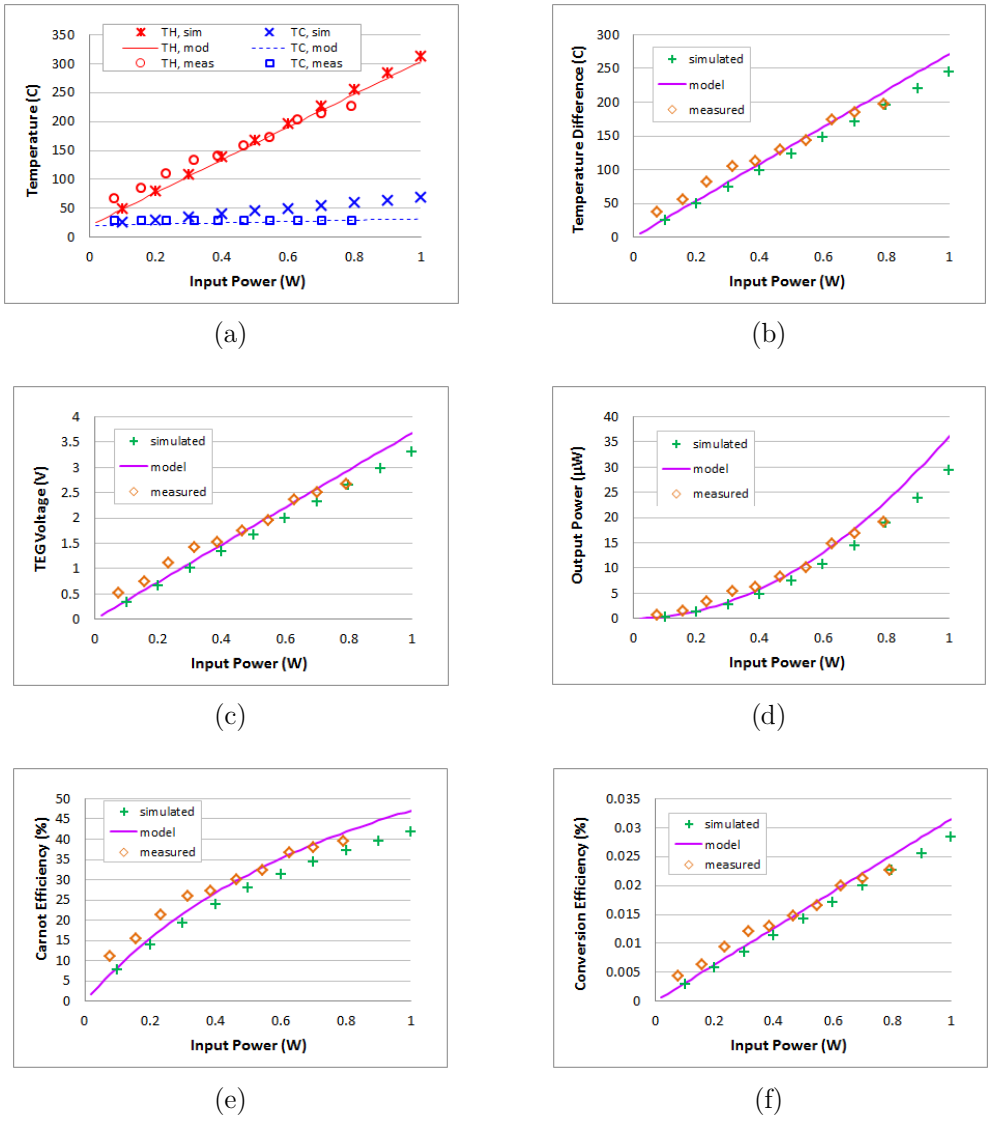
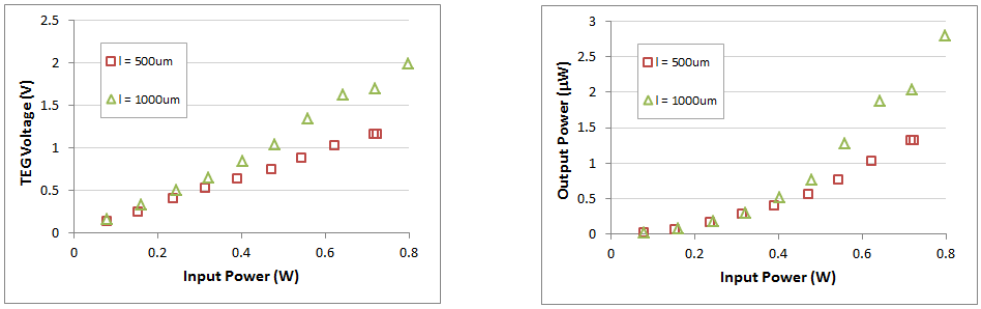


Figure 7-8: Comparison between simulations, thermal model, and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) matched output power, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a SOI substrate with $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 34$.

The effect of geometry on the performance of the fabricated TEG on SOI devices was also examined. Figure 7-9 shows the open-circuit TEG voltage and matched output power of the TEGs with two different thermoelement lengths while keeping the width at 15 µm and the membrane diameter at 3 mm. The same trends as the TEGs implemented on a glass substrate are observed. Both the TEG voltage and the output power increases as the thermoelement length is increased. This is attributed to the lower thermal

conductance of the TEG, which contributes to a higher temperature difference across the thermoelements. The increase in TEG voltage also led to an increase in the matched output power as the thermoelement length is increased.

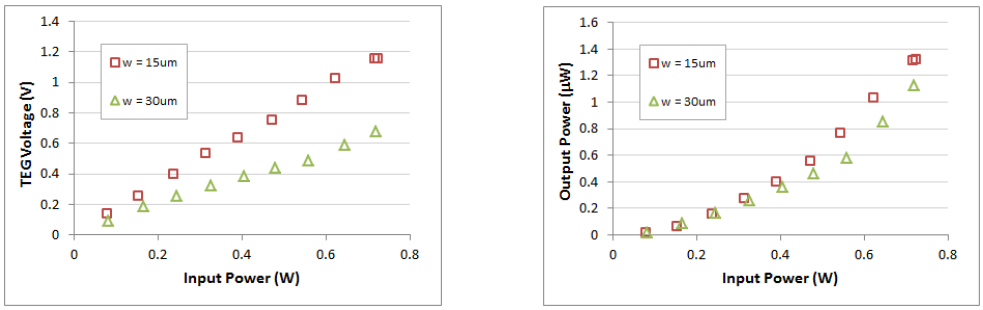


(a) (b)

Figure 7-9: Measured (a) open-circuit TEG voltage and (b) matched output power of TEGs implemented on a SOI substrate with varying thermoelement lengths ($w = 15$ µm and $d_{mem} = 3$ mm)

Figure 7-10 shows the open-circuit TEG voltage and matched output power of the TEGs with different thermoelement widths while keeping the length at 500 µm and the membrane diameter at 3 mm. The TEGs with wider thermoelements would have a higher thermal conductance, resulting in a lower temperature difference across the device. As such, it can be observed from Figure 7-10a that the output voltage decreases as the thermoelement width is increased. The increase in thermoelement width has a corresponding decrease in the TEG's series electrical resistance. Since the matched output power is squarely proportional to the TEG voltage and inversely proportional to the series resistance, the decrease in the open-circuit voltage dominates the trend in output power; thereby resulting in the output power decreasing with increasing thermoelement width.

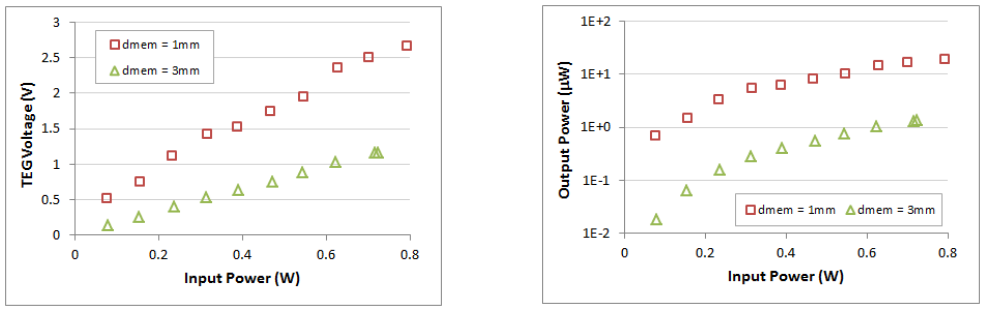
Figure 7-11 shows the open-circuit TEG voltage and matched output power of the TEGs with different membrane diameters while keeping the length at 500 µm and the width at 15 µm. The TEG with a larger membrane diameter has more thermocouples, which result in a higher thermal conductance of the TEG. This translates to a lower temperature difference across the device. This is evident from the voltage graph where the output voltage decreases as the membrane diameter is increased. The increase in the number of



(a) (b)

Figure 7-10: Measured (a) open-circuit TEG voltage and (b) matched output power of TEGs implemented on a SOI substrate with varying thermoelement widths ($l = 500$ µm and $d_{mem} = 3$ mm)

thermocouples as the membrane diameter is increased also results in an increase in the TEG's series resistance. The combined effect of the decrease in output voltage and increase in the series resistance of the TEG as the membrane diameter is increased results in a decrease in the output power of the devices. This is shown in Figure 6-22b where the output power of the TEG with a 3 mm diameter membrane is an order of magnitude less than the output power of the TEG with a 1 mm diameter membrane.



(a) (b)

Figure 7-11: Measured (a) open-circuit TEG voltage and (b) matched output power of TEGs implemented on a SOI substrate with varying membrane diameters ($l = 500$ µm and $w = 15$ µm)

The efficiency factors of the six fabricated TEGs on SOI are listed in Table 7-7. The TEG with the best efficiency factor has a length of 200 µm, width of 15 µm, and membrane diameter of 5 mm. For the same membrane diameter and thermoelement width, the efficiency factor decreases as the thermoelement length increases. For the same membrane diameter and thermoelement length, the efficiency factor increases as the thermoelement width increases.

Table 7-7: Efficiency factor of TEGs fabricated on a SOI substrate. The TEG with the best efficiency factor is highlighted in **bold**.

l (µm)	w (µm)	d_{mem} (mm)	N	ϕ (µW/cm²K²)
200	15	1	31	7.26×10^{-4}
500	15	1	34	4.91×10^{-4}
500	15	3	111	1.93×10^{-3}
500	30	3	81	2.56×10^{-3}
1000	15	3	114	1.47×10^{-3}
200	**15**	**5**	**188**	**4.9×10^{-3}**

For more graphs showing the measurements performed on all ten TEGs fabricated on a SOI substrate with the laser test set-up, the reader is referred to Appendix H.

7.4.2 Solar Simulator Testing

The same solar simulator testing set-up discussed in section 6.4.2 was used for testing the fabricated TEGs on a SOI substrate. In this set-up, three different-sized uncoated N-BK7 plano-convex spherical lenses from Thorlabs, Inc. were used to focus the solar input onto the membrane of the TEG. The physical properties of the lenses used are listed in Table 6-7. The test set-up was composed of an Abet Technologies Sun 3000 Solar Simulator Model 11016A that was used to provide the solar input. A lens was then used to focus the solar input onto the center of the device. The voltage and current measurements were monitored using a Keithley Model 2400 source meter and data was captured through LabView.

The V-I characteristics of a solar TEG with varying lens diameters used in focusing solar light onto the center of the device are displayed in Figure 7-12. The x-intercept of the line defines the open-circuit voltage. It can be observed that the open circuit voltage increases as the lens diameter increases. This implies an increase in the input heat flux as the lens diameter is increased. Unlike the TEGs implemented on a glass substrate, the slope of the line slightly decreases as the amount of solar input is increased, translating to a slight increase in TEG resistance. This increase in TEG resistance can be attributed

to an increase in the silicon's electrical resistivity brought about by the increase in temperature as the amount of solar input increases.

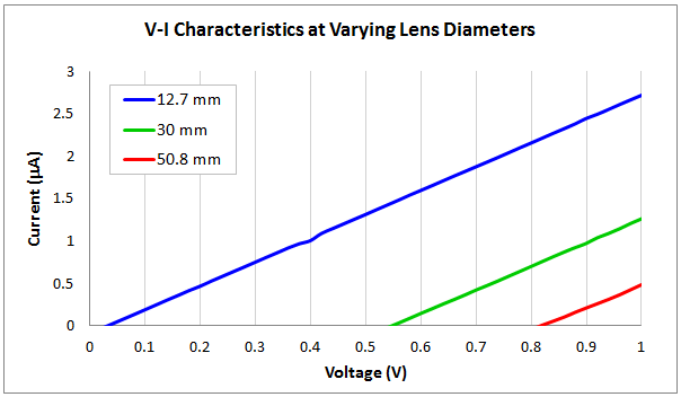


Figure 7-12: V-I characteristics of TEG implemented on a SOI substrate with $l = 1000$ μm, $w = 15$ μm, $d_{mem} = 3$ mm, and $N = 114$ using three different lens diameters.

Table 7-8 lists the open-circuit voltage, series resistance, temperature difference, and output power under matched load conditions for TEGs with varying thermoelement lengths. There are three sets of values for each parameter corresponding to the three plano-convex lenses used in the solar simulator measurements. Each parameter value is the result of the average of five measurements. As expected, the open-circuit voltage and output power increases as the thermoelement length increases. This is attributed to the increase in temperature difference across the device brought about by the decrease in thermal conductance. For each TEG, the open-circuit voltage increases as the diameter of the lens used is increased. This is due to the increase in temperature difference as the input heat flux increases with the increasing lens diameter. As a result of the increase in

Table 7-8: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a SOI substrate with varying thermoelement lengths ($w = 15$ μm and $d_{mem} = 3$ mm). For each of the three types of plano-convex lenses used, data is taken from the average of five measurements.

l (μm)	V_{TEG} (mV)			R_{TEG} (kΩ)			ΔT (°C)			P_{OUT} (nW)		
	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050
500	20.9	437.1	581.2	255.1	255.4	257.1	0.47	9.9	13.1	0.43	187	328.4
1000	30.5	546.1	803.2	355.2	360.1	374.3	0.67	12	17.7	0.65	207	430.9

open-circuit TEG voltage, the output power under matched load conditions also increases with increasing lens diameter.

Table 7-9 lists the open-circuit voltage, series resistance, temperature difference, and output power under matched load conditions for TEGs with varying thermoelement widths. As the thermoelement width is increased, the voltage decreases while the output power increases. The decrease in voltage is consistent with the increase in thermal conductance brought about by increasing the thermoelement width. The increase in output power is mainly due to the decrease in the TEG's series resistance as the thermoelement width is increased. For each TEG, the output voltage and output power increases as the lens diameter is increased. This is expected as increasing the lens diameter means an increase in the input heat flux. For a specific lens, there is very little change observed with the temperature difference across the device as the width is varied.

Table 7-9: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a SOI substrate with varying thermoelement widths ($l = 500$ µm and $d_{mem} = 3$ mm). For each of the three types of plano-convex lenses used, data is taken from the average of five measurements.

w (µm)	V_{TEG} (mV)			R_{TEG} (kΩ)			ΔT (°C)			P_{OUT} (nW)		
	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050
15	20.9	437.1	581.2	255.1	255.4	257.1	0.47	9.9	13.1	0.43	187	328.4
30	19.3	372.4	451.6	102.7	104.5	109.6	0.6	11.5	14	0.9	331.8	465.1

Table 7-10 lists the open-circuit voltage, series resistance, temperature difference, and output power under matched load conditions for TEGs with varying membrane diameters. Due to the higher number of thermocouples, the temperature difference decreases as the membrane diameter is increased. Since the output voltage is proportional to both the number of thermocouples and the temperature difference, it can be inferred that the increase in the number of thermocouples dominates as is evident in the increase in the open-circuit TEG voltage as the membrane diameter is increased. This increase in the open-circuit TEG voltage results in a corresponding increase in the output power as the membrane diameter is increased.

Table 7-10: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a SOI substrate with varying membrane diameters ($l = 500$ μm and $w = 15$ μm). For each of the three types of plano-convex lenses used, data is taken from the average of five measurements.

d_{mem} (mm)	V_{TEG} (mV)			R_{TEG} (kΩ)			ΔT (°C)			P_{OUT} (nW)		
	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050	LA1074	LA1102	LA1050
1	13.8	232.7	---	94.6	96.1	---	1.01	17.2	---	0.5	140.9	---
3	20.9	437.1	581.2	255.1	255.4	257.1	0.47	9.9	13.1	0.43	187	328.4

For a complete list of the results from the solar simulator measurements performed on all six TEGs fabricated on a SOI substrate, the reader is referred to Appendix I.

7.5 TEG on Glass vs. TEG on SOI

This section compares the performance of the two TEG implementations investigated in this study. Before going into the difference in performance of the two implementations, it is worthwhile to first look at Table 7-11 where the properties of the materials used in both implementations are listed. The Seebeck coefficient of the silicon material is 3.5 times more than that of the polysilicon material. This is due to the difference in the doping concentration between the two. From measurements performed using an Accent HL5500 Hall Effect system, the dopant concentration of the hot-wire polysilicon was found to be in the order of 10^{21} cm^{-3} whereas that of the silicon device layer of the SOI is in the order of 10^{19} cm^{-3}. The derived thermal conductivities of both thermoelectric materials are comparable and the electrical resistivities of both materials are of the same order. For the measured dopant concentration of the hot-wire polysilicon, it is expected that its thermal conductivity and electrical resistivity would be lower. Annealing of the deposited hot-wire polysilicon film, which was not done in this thesis due to the temperature limits of the glass substrate used, could potentially alter the properties of the material to lower both its thermal conductivity and electrical resistivity. Having a lower thermal conductivity can further increase the temperature difference across the device and having a lower electrical resistivity can result in a larger output power.

Table 7-11: Comparison between the electrical and thermoelectric properties of polysilicon and silicon materials used in the TEG on glass and TEG on SOI implementations, respectively.

Thermoelectric material	Seebeck coefficient (mV/K)	Thermal conductivity (W/mK)	Electrical resistivity (Ω-m)
p-type polysilicon (TEG on glass)	113	126	3.58×10^{-5}
p-type silicon (TEG on SOI)	396	146	8.94×10^{-5}

Figure 7-13 shows the measured parameters from laser measurements of two TEGs with the same dimensions but of two different implementations. As can be seen from the temperature difference plot in Figure 7-13a, the temperature difference of the TEG on SOI is significantly larger than the temperature difference of the TEG on glass. This is primarily due to the design of the two TEGs. The TEG on glass has a substantial amount of heat lost through the substrate. The TEG on SOI, on the other hand, having a cavity under the thinned handle layer directly beneath the membrane and thermoelements enhances the heat flux path across the device and leads to a higher temperature difference across the device. As a result of the higher temperature difference and Seebeck coefficient of the TEG on SOI, the generated open-circuit voltage is also higher than the TEG on glass implementation, as is shown in Figure 7-13b. With regards to the output power, it can be seen that the output power of the TEG on SOI is 2 orders of magnitude greater than the TEG on glass. This is also a result of the higher output voltage generated from the TEG on SOI. Lastly, the conversion efficiency of the TEG on SOI is at least an order of magnitude higher than that of the TEG on glass, which is due to the larger temperature difference and better thermoelectric figure-of-merit.

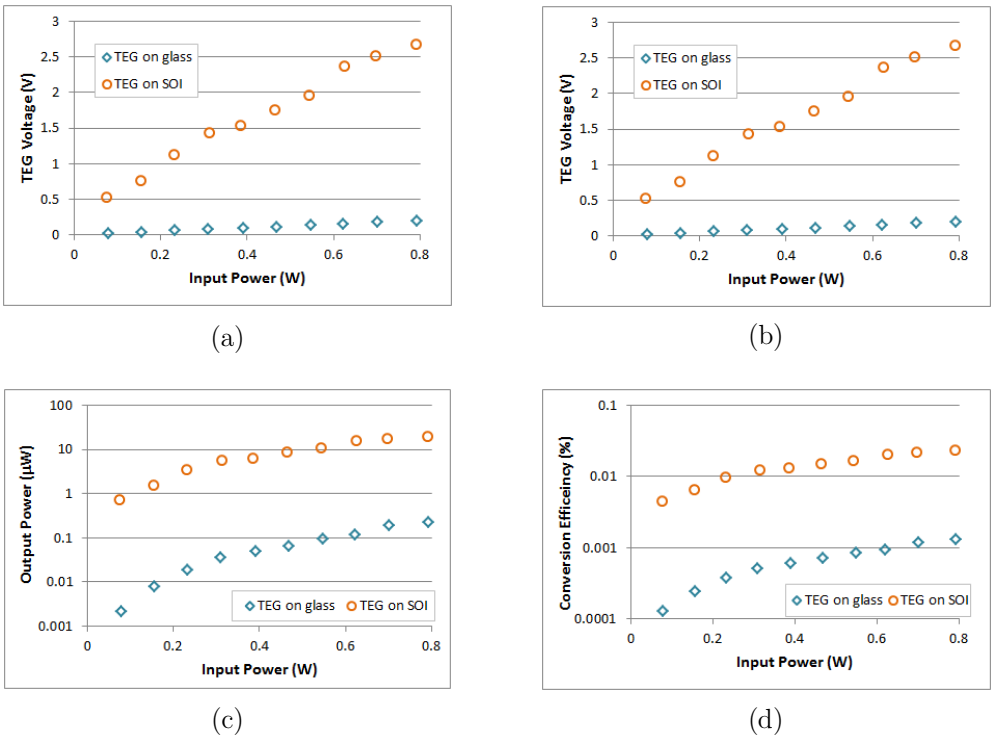


Figure 7-13: Comparison between measured (a) temperature difference, (b) open-circuit TEG voltage, (c) matched output power, and (d) conversion efficiency of both TEG on glass and TEG on SOI with $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 34$.

Table 7-12 lists efficiency factors of six sets of TEG dimensions that were both implemented on glass and on SOI. In both implementations, the TEG with the best efficiency factor has a length of 200 µm, width of 15 µm, and membrane diameter of 5 mm. The efficiency factors of the TEGs implemented on SOI are also higher than those implemented on glass.

Table 7-12: Comparison between efficiency factors of TEGs fabricated on glass and TEGs fabricated on SOI. The TEG with the best efficiency factor is highlighted in **bold**.

l (µm)	w (µm)	d_{mem} (mm)	N	ϕ (µW/cm²K²)	
				TEG on glass	TEG on SOI
200	15	1	31	1.58×10^{-4}	7.26×10^{-4}
500	15	1	34	8.66×10^{-5}	4.91×10^{-4}
500	15	3	111	2.49×10^{-4}	1.93×10^{-3}
500	30	3	81	4.08×10^{-4}	2.56×10^{-3}
1000	15	3	114	1.66×10^{-4}	1.47×10^{-3}
200	**15**	**5**	**188**	$\mathbf{1.24 \times 10^{-3}}$	$\mathbf{4.9 \times 10^{-3}}$

Table 7-13 compares the performance of two TEGs having the same geometry but different implementations when a LA1050 plano-convex lens is used to focus the light coming from the solar simulator onto the center of the TEG. The TEG on SOI clearly outperforms the TEG on glass, having 10 ˚C more temperature difference, more than 8 times the output voltage, and more than 50 times the output power.

Table 7-13: Comparison between solar simulator measurements of both TEG on glass and TEG on SOI with $l = 1000$ µm, $w = 15$ µm, $d_{mem} = 3$ mm, and $N = 114$ using a LA1050 ($D = 50.8$ mm) plano-convex lens.

	V_{TEG} (mV)	R_{TEG} (kΩ)	ΔT (˚C)	P_{OUT} (nW)
TEG on glass	92.11	255.04	7.04	8.31
TEG on SOI	803.2	374.3	17.7	430.9

7.6 Conclusions

This chapter covered the design, modelling, fabrication, and testing of the implementation of TEGs on a SOI substrate. To do away with the problematic HFVPE step in the proposed TEG fabrication process, it is decided to retain the buried oxide layer of the SOI and a thin layer of the handle layer to add structural stability to the device. To compensate for the heat lost through the buried oxide layer and the thin handle layer, a SOI wafer with a thinner device layer for this implementation was used. The modified thermal model for the TEG implementation on SOI also showed good agreement with heat transfer simulations. Furthermore, the thermal model was able to closely predict the actual performance of the device based on the laser measurements performed.

Based on the laser measurements, a maximum TEG voltage per watt of input power for a TEG with a length of 500 µm, width of 15 µm, membrane diameter of 1 mm, and 34 thermocouples was generated. For a 1 W laser input with a spot size of 1mm, the open circuit voltage is 3.06 V, which translates to a temperature difference of 226 ˚C across the thermoelements. The output power under matched load conditions is 25 µW with

Carnot and conversion efficiencies at 42.8% and 0.026%, respectively. The resulting efficiency factor for this TEG is 4.91×10^{-4} $\mu W/cm^2K^2$.

Of all the tested TEGs implemented on a SOI substrate, the best efficiency factor is computed for a TEG that has a length of 200 μm, width of 15 μm, and membrane diameter of 5 mm. The best efficiency factor is found to be 4.9×10^{-3} $\mu W/cm^2K^2$.

Based on the solar simulator measurements, a maximum TEG voltage of 803 mV was generated, which translates to a temperature difference of 18 ° C across the thermoelements. This was achieved by using a 50.8 mm diameter plano-convex lens to focus solar input to a TEG with a length of 1000 μm, width of 15 μm, membrane diameter of 3 mm, and 114 thermocouples. The corresponding output power under matched load conditions is 431 nW.

The temperature difference of the TEG on SOI is larger than the temperature difference of the TEG on glass because the TEG on glass has a substantial amount of heat lost through the substrate. As a result of the higher temperature difference and Seebeck coefficient of the TEG on SOI, the generated open-circuit voltage is also higher. The output power of the TEG on SOI is 2 orders of magnitude greater than the TEG on glass. Lastly, the conversion efficiency of the TEG on SOI is at least an order of magnitude higher than that of the TEG on glass.

Chapter 8: Conclusions and Recommendations

The feasibility of applying solar concentration on thermoelectric generators is evaluated in this study. To accomplish this, a system is proposed wherein a lens is used to focus solar radiation onto the membrane of a TEG. Several large scale implementations of such a system already exist. At the micro scale, a recent implementation using a vertically-oriented thermocouple employing both solar and thermal concentration showed 7-8 times improvement in efficiency (Kraemer et al. 2011). However, this implementation uses nanostructured Bi_2Te3 alloys which have limited compatibility to standard MEMS and CMOS processes. As such, the use of p-type silicon and aluminum as thermoelement materials for the proposed solar thermoelectric generator system was explored.

With the TEG and lens system in mind, several chip-scale TEG implementations are reviewed. Three different types of TEGs are reported and the lateral/lateral TEG type is chosen for implementation as it is the simplest to fabricate and has the most potential for integration with on-chip electronics. N-type and p-type silicon are initially preferred as thermoelectric materials for the TEG because of their high Seebeck coefficients. Moreover, aluminum is chosen as the contact material to electrically connect the thermoelements in series as it is commonly the metal used for this purpose in previous implementations. However, to further simplify the fabrication process by minimizing the required number of masks, aluminum is selected for the second thermoelement instead. Evidently, this incurs a trade-off between TEG performance and fabrication complexity. Since the main objective of this work is to demonstrate the advantages of using solar concentration on a TEG and not on optimizing the TEG performance, it was opted to employ a simpler fabrication process for the TEG.

Heat transfer simulations in COMSOL show that the temperature difference across thermoelements increases with increasing input heat flux, which is the result of increasing the ratio of the lens surface area to the heated membrane surface of the TEG.

Consequently, the increase in the temperature difference results in an improvement in TEG efficiency.

An analytical model of the TEG is also developed based on energy balance and heat transfer equations derived from a thermal equivalent circuit of the designed TEG. Using this model, a 10×10 mm^2 TEG with a fully suspended membrane and thermoelements having dimensions $l = 200$ μm, $w = 15$ μm, $t = 5$ μm, $N = 188$ thermocouples, and d_{mem} = 5 mm has a temperature difference of 40 ° C. This translates to an open-circuit output voltage of 1.2 V, generating 73μW of matched output power. This leads to a computed TEG efficiency factor of 0.2496 $\mu W/cm^2K^2$, which is higher than in all the published lateral/lateral TEGs reviewed in this report.

The proposed TEG fabrication process involves the use of a SOI wafer with a pre-doped device layer to simplify the fabrication process. To electrically isolate the thermoelements from the rim and membrane of the TEG, isolation trenches are added into the TEG design. These trenches are formed by etching the silicon device layer and backfilling with a non-conducting material. The proposed TEG fabrication process involved six major fabrication steps: (1) hardmask patterning of front and back sides, (2) frontside RIE, (3) refilling of isolation trenches, (4) aluminum deposition and lift-off, (5) backside DRIE, and (6) HF vapor phase etching. Two methods of refilling isolation trenches are explored. The first method uses TEOS-based PECVD silicon dioxide capped with silicon-rich silicon nitride whereas the second method uses HWCVD silicon nitride, HWCVD polysilicon, and SINR-3570, a siloxane-based spin-on dielectric. Unfortunately, there were problems encountered during HFVPE, which is the last step of the proposed fabrication process. It was found that the materials used for filling the isolation trenches are not able to provide enough mechanical stability once the membrane and thermoelements are suspended. In this regard, two alternative methods of fabricating TEGs are investigated.

The first fabrication method involves the implementation of TEGs on a glass substrate. Although a significant amount of heat is lost through the substrate, this implementation has the advantage of a much simpler fabrication process. The TEG design involves the use of HWCVD p-type polysilicon and aluminum as thermoelectric materials. The

HWCVD technique is predominantly used in depositing silicon for solar cell applications. This is the first study that explores the use of HWCVD films for thermoelectric applications. The simpler fabrication process of TEGs on glass only involves three major fabrication steps. These are: (1) HWCVD polysilicon deposition and etching, (2) aluminum deposition and lift-off, and (3) wafer dicing and chip wirebonding.

The second fabrication method involves the implementation of TEGs on a SOI substrate. In this TEG design, it was decided to retain the buried oxide layer of the SOI and a thin layer of the handle layer to add structural stability to the device. To compensate for the heat lost through the buried oxide layer and the thin handle layer, a SOI wafer with a thinner device layer was used for this implementation. The fabrication process of TEGs on SOI involves 6 major fabrication steps. These are: (1) hardmask patterning of front and back sides, (2) frontside RIE, (3) aluminum deposition and lift-off, (4) wafer-level backside DRIE, (5) wafer dicing, and (6) chip-level backside DRIE and wirebonding.

Because of the slight changes in TEG structure due to the amendments in the fabrication process, the thermal model initially developed had to be modified to consider the additional heat losses of the two fabrication methods investigated. In both cases, the modified thermal model is shown to agree well with heat transfer simulations.

To properly characterize the fabricated TEGs, a laser test set-up is performed where the input power is varied at a constant spot size. This allows depiction of a scenario where there is precise control of the solar spot size and the variation in input power represents varying the concentration ratio. Results from the laser test set-up are in good agreement with the thermal model. A second set-up involves testing the TEGs using a solar simulator and three lenses with different diameters to emulate the environment with which the devices are to be used as solar TEGs with solar concentration.

Based on the laser measurements, Table 8-1 lists the parameters of both TEG on glass and TEG on SOI having the same geometry for an input power of 1 W. The TEG on SOI implementation clearly outperforms the TEG on glass implementation. This is primarily due to the design of the two TEGs. The TEG on glass has a substantial

amount of heat lost through the substrate. The TEG on SOI, on the other hand, having a cavity under the thinned handle layer directly beneath the membrane and thermoelements enhances the heat flux path across the device and leads to a 163 ˚C higher temperature difference across the device. As a result of the higher temperature difference, the other parameters of the TEG on SOI implementation are also higher than those of the TEG on glass. The generated open-circuit voltage of the TEG on SOI is about 12 times higher than the TEG on glass. The output power of the TEG on SOI is about 70 times greater than the TEG on glass. The conversion efficiency of the TEG on SOI is 16 times better than that of the TEG on glass. Lastly, the efficiency factor of the TEG on SOI is about 5.5 times higher than that of the TEG on glass.

Table 8-1: Comparison between parameters of both TEG on glass and TEG on SOI with $l = 500$ μm, $w = 15$ μm, $d_{mem} = 1$ mm, and $N = 31$ for an input power of 1 W.

	ΔT (˚C)	V_{TEG} (V)	P_{OUT} (μW)	η_C (%)	η (%)	ϕ (μW/cm²K²)
TEG on glass	63	0.247	0.347	17.3	0.0016	8.7×10^{-5}
TEG on SOI	226	3.06	25	42.8	0.026	4.91×10^{-4}

Of all the tested TEGs for both implementations, the best efficiency factor is computed for a TEG that has a length of 200 μm, width of 15 μm, and membrane diameter of 5 mm. The best efficiency factor is found to be 1.24×10^{-3} μW/cm²K² and 4.9×10^{-3} μW/cm²K² for the TEG on glass and TEG on SOI implementations, respectively.

Based on the solar simulator measurements, Table 8-2 lists the TEGs with the highest generated voltage using a 50.8 mm diameter plano-convex lens to focus solar light onto the center of the TEG. In both cases, the highest voltages are achieved for the successfully fabricated TEGs that have the largest membrane diameter and longest thermoelement length.

Solar simulator measurements also verified that applying solar concentration by varying the lens diameter results in a higher TEG voltage and output power as the lens diameter is increased. This implies that increasing the lens diameter increases the input heat flux to the device; thereby increasing the temperature difference and improving its efficiency.

Table 8-2: TEGs with the highest output voltage based on solar simulator measurements for both TEG on glass and TEG on SOI implementations using a LA1050 ($D = 50.8$ mm) plano-convex lens.

	l (μm)	w (μm)	d_{mem} (mm)	N	V_{TEG} (mV)	R_{TEG} (kΩ)	ΔT (°C)	P_{OUT} (nW)
TEG on glass	1000	15	5	191	124	446.2	5.7	8.8
TEG on SOI	1000	15	3	114	803.2	374.3	17.7	430.9

Table 8-3 lists some of the published lateral/lateral TEGs discussed in Chapter 2 along with the proposed TEG with a fully suspended membrane and the two TEG implementations investigated in this study. The two TEG implementations have a lower efficiency factor than the other published TEGs. Note that in the six published lateral/lateral TEGs listed in Table 8-3, only the one by (Kiely et al. 1994) do not have a fully suspended membrane. Hence, it is inevitable that the two TEG implementations would perform poorly than the other TEGs. As for the TEG by (Kiely et al. 1994), they used both p-type and n-type polysilicon as thermoelements, which translates to a higher Seebeck coefficient. This is the reason why their implementation, although implemented on quartz, still outperforms the TEG on SOI implementation. However, it is worthwhile to note that if the proposed TEG with a fully suspended membrane and thermoelements as described in Chapters 4 and 5 is implemented, then an efficiency factor more than 2.5 times better than the TEG implemented by (Glosch et al. 1999), which has the highest efficiency factor among all the published lateral/lateral μTEG implementations reviewed in this study, can be achieved.

To give a better perspective of how the TEGs investigated in this study compares with published TEG implementations, Figure 8-1 shows a plot of the efficiency factor versus the level of integration of the published lateral/lateral μTEGs discussed in Chapter 2 and the TEGs investigated in this study. Based on this figure, it can be concluded that the fully suspended TEG implementation has the capability of outperforming the other TEGs.

Table 8-3: Comparison of TEGs examined in this work with selected published lateral/lateral μTEGs.

Authors Year	Substrate/ Process	TE length (μm)	TE cross sec. area (μm²)	Integration (TCs/cm²)	TC material	Seebeck coeff. (μV/K)	Interconnect material and thickness	Deposition method	TC patterning	Efficiency factor (μW/K²cm²)
This work (model only)	*fully suspended TEG*	*200*	*15 x 5*	*188*	*p-Si / Al*	*376.8*	*Al, 3μm*	*evaporation*	*RIE and lift-off*	***0.2496***
This work (fabricated)	*TEG on SOI*	*200*	*15 x 3*	*188*	*p-Si / Al*	*399.8*	*Al, 3μm*	*evaporation*	*RIE and lift-off*	*0.0049*
This work (fabricated)	*TEG on glass*	*200*	*15 x 1*	*188*	*p-poly / Al*	*114.8*	*Al, 1μm*	*HWCVD and evaporation*	*RIE and lift-off*	*0.00124*
Glosch et.al. 1999	bulk Si	500	7 x 1.2	6060.6	Al / n-Si	240	Al, 1.2μm	Evaporation and doping	---	0.091
Xie et.al. 2010	bulk Si	16	5 x 0.7	312500	p-polySi / n-polySi	279	Al	LPCVD	Dry etching	0.052
Yang et.al. 2009	0.35μm CMOS	60	4 x 0.275 / 4 x 0.18	104166.7	p-polySi / n-polySi	160	Al	LPCVD	Dry etching	0.0417
Huesgen et.al. 2008	bulk Si	120	5 x 0.25 / 40 x 0.7	9259.3	Al / n-polySi	76.08	Al, 0.25μm	LPCVD / sputtering	Wet and dry etching	0.01612
Kiely et.al. 1994	Polysilicon on quartz	450	100 x 0.4	555.6	p-polySi / n-polySi	490	Al, 0.1μm	Ion implanting	RIE	0.011
Kao et.al. 2010	0.35μm CMOS	640	5 x 0.3	7812.5	p-polySi / n-polySi	67	Al, 0.6μm	LPCVD	Dry etching	0.0064

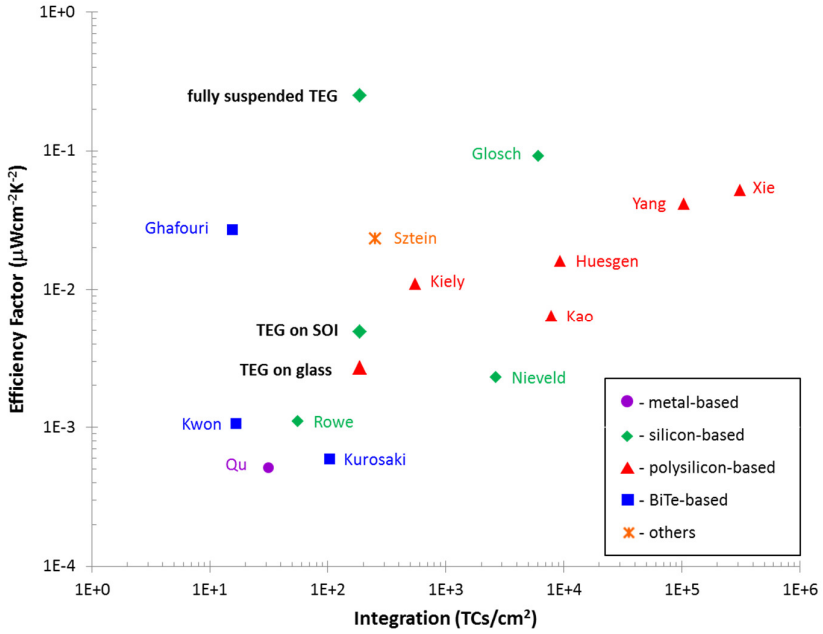


Figure 8-1: Comparison of efficiency factor vs. level of integration of TEGs investigated in this study and published lateral/lateral µTEGs grouped according to thermoelectric material used.

The main issue that has to be addressed to successfully fabricate the initially proposed TEG design with a fully suspended membrane and thermoelements is to find a material to fill the isolation trenches that will keep the structure mechanically stable after the HFVPE step. Lining the trench with HWCVD silicon nitride and filling with HWCVD intrinsic polysilicon could work but would require a chemical mechanical polishing (CMP) step for proper planarization of the trench.

Based on the test measurements performed on the fabricated TEGs, it has been shown that precise control of the spot size is necessary to be able to accurately model the performance of the TEG. This manifested in the good agreement between the laser measurement results and the thermal model, which was demonstrated in both Chapters 6 and 7. Proper modelling of the solar simulator measurements was not possible because of the variation in the intensity of the solar spot size brought about by the fact that not all the light rays from the solar simulator strike the lens at the optic axis. In spite of this, efficiency improvement is still implied by the increasing TEG voltage measured as the diameter of the lens used is increased. One way to resolve this issue is to use lenses with

shorter focal lengths. Although this would solve the problem with the spot size, it should be noted that this would mean positioning the lens more closely to the TEG. In this case, it would be practical to use translation stages for both the lens and the TEG to allow for better alignment and precise distance control.

This study also introduces the use of the HWCVD technique for thermoelectric applications. Although the TEG on glass implemented in this study do not perform very well, several factors can be developed to improve the TEG efficiency. One factor that can be examined for future work is the quality of the film. Preliminary investigations have shown that annealing the deposited polysilicon film at temperatures greater than 800 $^\circ$C improves the film's crystallinity and activates more dopants, which results in a lower electrical resistivity. Annealing can be done when using glass substrates that have high melting temperatures or when using a SiO_2-coated silicon substrate where the TEG on SOI design in this study can be applied. Another factor that can be explored is using both n- and p-type HWCVD polysilicon as thermoelectric materials. This would result in a higher thermocouple Seebeck coefficient at the expense of an additional lithography mask and a slightly more complicated fabrication process.

For future studies, the use of nanostructured silicon as thermoelectric material can also be explored as this should have a better thermoelectric figure-of-merit, leading to a more efficient device. The possibility of coating the membrane with a higher absorptance material can also be explored. A thermal collector can also be incorporated into the TEG design to further enhance its conversion efficiency. It would also be worthwhile to explore the possible improvement in efficiency when the TEG is integrated into a PV-TE hybrid system.

To further optimize the device, a study on the application of thermal matching to the design of the STEG can also be explored. With knowledge of the thermoelectric properties of the material as well as the values of the other thermal fluxes present in the system, the efficiency of the device can be maximized by applying the thermal matching technique.

It is also worthwhile to emphasize the relatively high temperature differences generated on chip as can be seen in Table 8-1 where the temperature difference was 63 ˚C and 226 ˚C for the TEG on glass and TEG on SOI implementations, respectively. This demonstration of having a large temperature difference on chip can be explored further for other applications such as in microfluidics or even in creating on-chip Stirling engines.

Appendix A: TEG Thermal Models in MATLAB

This is the MATLAB program used to calculate the performance parameters of the TEG using the analytical model developed in section 4.3. This involves the proposed TEG with a fully suspended membrane and thermoelements.

```
tic;
clear;
format short e;
pi = 3.1416;
sbc = 5.676e-8; %Stefan Boltzmann constant
init_delta_T = 0; %setting delta_T initially at zero for iterative
solving of delta_T using the 'bisect' function
hconv = 25; %convective flux in W/m^2K
erad = 0.6; %radiative emittance
Ta = 293.15; %ambient temperature set to 20 degC
d_lens = 28e-3; %clear diameter of lens after placing in lens mount
lens_ap = 0.9; %clear aperture of lens
d_lens_eff = d_lens * lens_ap; %effective lens diameter
abs = 0.5; %membrane absorptance
trans = 0.9; %lens transmittance
qs = 1000; %solar heat flux in W/m^2

teg = xlsread('d:\matlab files\data\teg_dimensions.xls'); %read XLS
file containing TEG geometry
header = {'L(um)' 'W(um)' 'D(mm)' 'N' 'Dh(mm)' 'T1(degC)' 'T2(degC)'
'TH(degC)' 'TC(degC)' 'delta_T' 'VOUT(V)' 'POUT(mW)' 'effC(%)'
'eff(%)' 'phi(uW/cm2K2)'};
xlswrite('d:\matlab
files\data\steg_model_v3_abstrans_hconv_25_erad_06_lens_30mm.xls',
header, 'sheet', 'A1');
label =
{'A1','A2','A3','A4','A5','A6','A7','A8','A9','A10','A11','A12','A13',
'A14','A15','A16','A17','A18','A19','A20','A21','A22','A23','A24','A25
','A26','A27','A28','A29','A30','A31','A32','A33','A34','A35','A36','A
37','A38','A39','A40','A41','A42','A43'};
row = 1;

while row < 43

% TEG dimensions
lg = teg(row,1) * 1e-6; % thermoelement length
wg = teg(row,2) * 1e-6; %thermoelement width
dm = teg(row,3) * 1e-3; %membrane diameter
N = teg(row,4); %number of thermocouples
tg = 5e-6; %thermoelement thickness
d_spot = 1e-3; %diameter of heated area

% silicon properties
s1 = 375e-6; %seebeck coefficient
r1 = 1e-5; %electrical resistivity
k1 = 125; %thermal conductivity

% aluminum properties
s2 = -1.8e-6; %seebeck coefficient
```

```
r2 = 2.65e-8; %electrical resistivity
k2 = 237; %thermal conductivity

kc = k1; %thermal conductivity of cold side material
kh = k1; %thermal conductivity of hot side material

% thermocouple properties
s_tc = s1 - s2; %seebeck coefficient
r_tc = r1 + r2; %electrical resistivity
k_tc = k1 + k2; %thermal conductivity
Z = s_tc^2/(r_tc*k_tc); %thermoelectric figure of merit

% thermoelectric generator properties
S_TEG = N* s_tc; %seebeck coefficient of TEG
R_TEG = N * r_tc * lg / (wg * tg); %electrical resistance of TEG
K_TEG = N * k_tc * wg * tg / lg; %thermal conductance of TEG
if dm == d_spot
    K_MEM = kh*pi*(dm/2)^2 / tg ;
else
    K_MEM = 2*pi*kh*tg / log((dm/2)/(d_spot/2));
end
K_RIM = 2*pi*kc*537e-6 / log((5e-3)/((dm/2)+lg));

% convection parameters
Aconv_R = (((10e-3)^2 - (pi*((dm/2)+lg)^2))) + (4*10e-3*537e-6);
Aconv_M = 2*pi*((dm/2)^2);
Aconv_T = 2*N*lg*wg;
Kconv_R = hconv * Aconv_R;
Kconv_M = hconv * Aconv_M;
Kconv_T = hconv * Aconv_T;

% radiation parameters
Arad_R = (((10e-3)^2 - (pi*((dm/2)+lg)^2)));
Arad_M = pi*((dm/2)^2);

% computation of input heat flux
Ah = (pi*(d_spot/2)^2) + (2*pi*(d_spot/2)*tg); % membrane heated
surface area
qh = abs * trans * qs * (d_lens_eff/d_spot)^2;
Qin =  qh * Ah;

syms delta_T T1 T2;

% output voltage and power
VOUT = S_TEG * delta_T;
POUT = VOUT^2 / (4 * R_TEG);
CUR = VOUT / (2 * R_TEG);

VOUT = eval(VOUT);
POUT = eval(POUT);
CUR = eval(CUR);

if erad == 0
    Q_RIM = Kconv_R*(T2-Ta);
    C1 = Q_RIM + (Kconv_T*(T2+(Q_RIM/K_RIM)-Ta)) -
(S_TEG*(T2+(Q_RIM/K_RIM))*CUR) - (K_TEG*delta_T) - (0.5*POUT);
    C2 = eval(C1);
    T2a = solve(C2,'T2');
    T2 = T2a;
```

```
    QCa = eval(Q_RIM);
    Q_RIM = QCa;

    Q_MEM = Qin - (Kconv_M*(T1-Ta));
    D1 = Q_MEM - (Kconv_T*(T1-(Q_MEM/K_MEM)-Ta)) - (S_TEG*(T1-
(Q_MEM/K_MEM))*CUR) - (K_TEG*delta_T) + (0.5*POUT);
    D2 = eval(D1);
    T1a = solve(D2,'T1');
    T1 = T1a;
    QHa = eval(Q_MEM);
    Q_MEM = QHa;

    F1 = T2 - T1 + (Q_MEM / K_MEM) + delta_T + (Q_RIM / K_RIM);
    F2 = eval(F1);
    Ttemp = solve(F2,'delta_T');
    Ttemp = subs(Ttemp);
    delta_T = Ttemp(2);
else
    Q_RIM = (Kconv_R*(T2-Ta)) + (erad*sbc*Arad_R*(T2^4-Ta^4));
    C1 = Q_RIM + (Kconv_T*(T2+(Q_RIM/K_RIM)-Ta)) -
(S_TEG*(T2+(Q_RIM/K_RIM))*CUR) - (K_TEG*delta_T) - (0.5*POUT);
    C2 = eval(C1);
    C3 = collect(C2,T2);
    L = coeffs(C3,T2);
    T2a = quartic(L(3),0,0,L(2),L(1));
    if hconv == 0
        T2 = T2a(2);
    else
        T2 = T2a(4);
    end
    QCa = eval(Q_RIM);
    Q_RIM = QCa;

    Q_MEM = Qin - (Kconv_M*(T1-Ta)) - (erad*sbc*Arad_M*(T1^4-Ta^4));
    D1 = Q_MEM - (Kconv_T*(T1-(Q_MEM/K_MEM)-Ta)) - (S_TEG*(T1-
(Q_MEM/K_MEM))*CUR) - (K_TEG*delta_T) + (0.5*POUT);
    D2 = eval(D1);
    D3 = collect(D2,T1);
    M = coeffs(D3,T1);
    T1a = quartic(M(3),0,0,M(2),M(1));
    T1 = T1a(4);
    QHa = eval(Q_MEM);
    Q_MEM = QHa;

    F1 = T2 - T1 + (Q_MEM / K_MEM) + (Q_RIM / K_RIM) + delta_T;
    F2 = eval(F1);

    delta_T = bisect(F2,'delta_T',init_delta_T);

end

T1 = eval(T1);
T2 = eval(T2);

QHb = eval(QHa);
QCb = eval(QCa);
TH = T1 - (QHb/K_MEM);
TC = T2 + (QCb/K_RIM);
Tave = 0.5 * (TH + TC);
```

```
effC = delta_T / TH;
effg = (sqrt(1 + (Z * Tave)) - 1) / (sqrt(1 + (Z * Tave)) + (TC /
TH));
eff = effC * effg;
VOUT = eval(VOUT);
POUT = eval(POUT);
phi = POUT / (10e-3^2 * delta_T^2);

disp(sprintf('\rTEG Dimensions: L=%d um, W=%d um, D=%d mm,
N=%d',lg/1e-6, wg/1e-6, dm/1e-3, N));
disp(sprintf('T1 (membrane temperature): %f degC',T1-273.15));
disp(sprintf('T2 (rim temperature): %f degC',T2-273.15));
disp(sprintf('TH (hot side temperature): %f degC',TH-273.15));
disp(sprintf('TC (cold side temperature): %f degC',TC-273.15));
disp(sprintf('Temperature Difference across TCs: %f degC',delta_T));
disp(sprintf('Open Circuit Output Voltage: %f V',VOUT));
disp(sprintf('Output Power at Matched Load Conditions: %f
mW',POUT*1000));
disp(sprintf('Carnot Efficiency: %f percent',effC*100));
disp(sprintf('TEG Efficiency: %f percent',eff*100));
disp(sprintf('TEG Efficiency Factor: %f uW/cm2K2',phi*100));
toc;

data(row,:) = [lg/1e-6 wg/1e-6 dm/1e-3 N d_spot/1e-3 T1-273.15 T2-
273.15 TH-273.15 TC-273.15 delta_T VOUT POUT*1000 effC*100 eff*100
phi*100];

row = row + 1;
xlswrite('d:\matlab
files\data\steg_model_v3_abstrans_hconv_25_erad_06_lens_30mm.xls',
data(row-1,:), 'sheet', char(label(row)));
end


% Computes for the roots of a 4th order polynomial function

function [x] = quartic(A, B, C, D, E)
alpha = -((3*B^2)/(8*A^2))+(C/A);
beta = ((B^3)/(8*A^3))-((B*C)/(2*A^2))+(D/A);
gamma = -((3*B^4)/(256*A^4))+((C*B^2)/(16*A^3))-((B*D)/(4*A^2))+(E/A);
if beta==0
    x1 = -(B/(4*A))+sqrt((-alpha+sqrt(alpha^2-(4*gamma)))/2);
    x2 = -(B/(4*A))+sqrt((-alpha-sqrt(alpha^2-(4*gamma)))/2);
    x3 = -(B/(4*A))-sqrt((-alpha+sqrt(alpha^2-(4*gamma)))/2);
    x4 = -(B/(4*A))-sqrt((-alpha-sqrt(alpha^2-(4*gamma)))/2);
else
    P = -((alpha^2)/12)-gamma;
    Q = -((alpha^3)/108)+((alpha*gamma)/3)-((beta^2)/8);
    R = -(Q/2)+sqrt((Q^2/4)+(P^3/27));
    U = R^(1/3);
    if U==0
        y = -((5/6)*alpha) + U - Q^(1/3);
    else
        y = -((5/6)*alpha) + U - (P/(3*U));
    end
    W = sqrt(alpha+(2*y));
    x1 = -(B/(4*A))+((W-sqrt(-((3*alpha)+(2*y)+((2*beta)/W))))/2);
    x2 = -(B/(4*A))+((W+sqrt(-((3*alpha)+(2*y)+((2*beta)/W))))/2);
    x3 = -(B/(4*A))+((-W-sqrt(-((3*alpha)+(2*y)-((2*beta)/W))))/2);
    x4 = -(B/(4*A))+((-W+sqrt(-((3*alpha)+(2*y)-((2*beta)/W))))/2);
end
```

```
x = [x1 x2 x3 x4];

% Iteratively solves the value of x by starting with an initial guess
value

function [x] = bisect(F, var, guess)
    e = 1;
    count = 1;
    a = guess;
    b = guess+1;

    while e > 1e-4,
        z1 = subs(F, var, a);
        z2 = subs(F, var, b);
        if z1*z2 < 0
            c = 0.5*(a+b);
            z3 = subs(F, var, c);
            if z1*z3 < 0
                b = c;
                e = abs(z1-z3)/(2^count);
            else
                a = c;
                e = abs(z2-z3)/(2^count);
            end
            count = count+1;
        else
            a = a+1;
            b = b+1;
        end
    end
x = [c];
```

This is the MATLAB program used to calculate the performance parameters of the TEG using the analytical model developed in section 6.1. This involves the TEG implemented on a glass substrate with p-type polysilicon and aluminum as thermocouple materials.

```
tic;
clear;
format short e;
pi = 3.1416;
sbc = 5.676e-8; %Stefan-Boltzmann constant
init_delta_T = 0; %setting delta_T initially at zero for iterative
solving of delta_T using the 'bisect' function
hconv = 25; %convective flux in W/m^2K
erad = 0.6; %radiative emittance
Ta = 293.15; %ambient temperature set to 20 degC
d_lens = 28e-3; %clear diameter of lens after placing in lens mount
lens_ap = 0.9; %clear aperture of lens
d_lens_eff = d_lens * lens_ap; %effective lens diameter
abs = 0.5; %membrane absorptance
trans = 0.9;%lens transmittance
qs = 1000; %solar heat flux in W/m^2
t_sub = 500e-6; %substrate thickness


teg = xlsread('d:\matlab files\data\teg_dimensions_3um.xlsx'); %read
XLS file containing TEG geometry
header = {'L(um)' 'W(um)' 'D(mm)' 'N' 'Dh(mm)' 'T1(degC)' 'T2(degC)'
'Tsub(degC)' 'TH(degC)' 'TC(degC)' 'delta_T' 'VOUT(V)' 'POUT(mW)'
'effC(%)' 'eff(%)' 'phi(uW/cm2K2)'};
xlswrite('d:\matlab files\data\steg_model_pyrex_v3_75mm_3um.xls',
header, 'sheet', 'A1');
label =
{'A1','A2','A3','A4','A5','A6','A7','A8','A9','A10','A11','A12','A13',
'A14','A15','A16','A17','A18','A19','A20','A21','A22','A23','A24','A25
','A26','A27','A28','A29','A30','A31','A32','A33','A34','A35','A36','A
37','A38','A39','A40','A41','A42','A43'};
row = 1;

while row < 11

% TEG dimensions
lg = teg(row,1) * 1e-6; % thermoelement length
wg = teg(row,2) * 1e-6; %thermoelement width
dm = teg(row,3) * 1e-3; %membrane diameter
N = teg(row,4); %number of thermocouples
tg = 1e-6; %thermoelement thickness
d_spot = 1e-3; %diameter of heated area

% HWCVD polysilicon properties
s1 = 113e-6; %seebeck coefficient
r1 = 3.58e-5; %electrical resistivity
k1 = 126; %thermal conductivity


% aluminum properties
s2 = -1.8e-6; %seebeck coefficient
r2 = 2.65e-8; %electrical resistivity
k2 = 237; %thermal conductivity
```

```
% glass substrate properties
k3 = 1.4; %thermal conductivity

kc = k1; %thermal conductivity of cold side material
kh = k1; %thermal conductivity of hot side material

% thermocouple properties
s_tc = s1 - s2; %seebeck coefficient
r_tc = r1 + r2; %electrical resistivity
k_tc = k1 + k2; %thermal conductivity
Z = s_tc^2/(r_tc*k_tc); %thermoelectric figure of merit

% thermoelectric generator properties
S_TEG = N * s_tc; %seebeck coefficient of TEG
R_TEG = N * r_tc * lg / (wg * tg); %electrical resistance of TEG
K_TEG = (N * k_tc * wg * tg / lg) + (2*pi*k3*t_sub /
log(((dm/2)+lg)/((dm/2)))); %thermal conductance of TEG

if dm > d_spot
    K_MEM = (2*pi*kh*tg / log((dm/2)/(d_spot/2))) + (2*pi*k3*t_sub /
log((dm/2)/(d_spot/2)));
else
    K_MEM = kh*pi*(dm/2)^2 / tg;
end
K_SUB = k3*pi*(d_spot/2)^2 / t_sub;

K_RIM = (2*pi*kc*tg / log((5e-3)/((dm/2)+lg))) + (2*pi*k3*t_sub /
log((5e-3)/((dm/2)+lg)));

% convection parameters
Aconv_R = (((10e-3)^2 - (pi*((dm/2)+lg)^2))) + (4*10e-3*(tg+t_sub));
Aconv_M = pi*((dm/2)^2);
Aconv_T = 2*N*lg*wg;
Aconv_S = (10e-3)^2 + (4*10e-3*t_sub);
Kconv_R = hconv * Aconv_R;
Kconv_M = hconv * Aconv_M;
Kconv_T = hconv * Aconv_T;
Kconv_S = hconv * Aconv_S;

% radiation parameters
Arad_R = (((10e-3)^2 - (pi*((dm/2)+lg)^2)));
Arad_M = pi*((dm/2)^2);

% computation of input heat flux
Ah = (pi*(d_spot/2)^2) + (2*pi*(d_spot/2)*tg); % membrane heated
surface area
qh = abs * trans * qs * (d_lens_eff/d_spot)^2;
Qin =  qh * Ah;

syms delta_T T1 T2;

% output voltage and power
VOUT = S_TEG * delta_T;
POUT = VOUT^2 / (4 * R_TEG);
CUR = VOUT / (2 * R_TEG);

VOUT = eval(VOUT);
POUT = eval(POUT);
```

```
CUR = eval(CUR);

if erad == 0
    Q_RIM = Kconv_R*(T2-Ta);
    C1 = Q_RIM + (Kconv_T*(T2+(Q_RIM/K_RIM)-Ta)) -
(S_TEG*(T2+(Q_RIM/K_RIM))*CUR) - (K_TEG*delta_T) - (0.5*POUT);
    C2 = eval(C1);
    T2a = solve(C2,'T2');
    T2 = T2a;
    QCa = eval(Q_RIM);
    Q_RIM = QCa;

    Tsub = ((K_SUB*T1)+(Kconv_S*Ta))/(Kconv_S+K_SUB);
    Q_MEM = Qin - (Kconv_M*(T1-Ta)) - (K_SUB*(T1-Tsub));
    D1 = Q_MEM - (Kconv_T*(T1-(Q_MEM/K_MEM)-Ta)) - (S_TEG*(T1-
(Q_MEM/K_MEM))*CUR) - (K_TEG*delta_T) + (0.5*POUT) ;
    D2 = eval(D1);
    T1a = solve(D2,'T1');
    T1 = T1a;
    QHa = eval(Q_MEM);
    Q_MEM = QHa;

    F1 = T2 - T1 + (Q_MEM / K_MEM) + delta_T + (Q_RIM / K_RIM);
    F2 = eval(F1);
    Ttemp = solve(F2,'delta_T');
    Ttemp = subs(Ttemp);
    delta_T = Ttemp(2);
else
    Q_RIM = (Kconv_R*(T2-Ta)) + (erad*sbc*Arad_R*(T2^4-Ta^4));
    C1 = Q_RIM + (Kconv_T*(T2+(Q_RIM/K_RIM)-Ta)) -
(S_TEG*(T2+(Q_RIM/K_RIM))*CUR) - (K_TEG*delta_T) - (0.5*POUT);
    C2 = eval(C1);
    C3 = collect(C2,T2);
    L = coeffs(C3,T2);
    T2a = quartic(L(3),0,0,L(2),L(1));
    if hconv == 0
        T2 = T2a(2);
    else
        T2 = T2a(4);
    end
    QCa = eval(Q_RIM);
    Q_RIM = QCa;

    Tsub = ((K_SUB*T1)+(Kconv_S*Ta))/(Kconv_S+K_SUB);
    Q_MEM = Qin - (Kconv_M*(T1-Ta)) - (erad*sbc*Arad_M*(T1^4-Ta^4)) -
(K_SUB*(T1-Tsub));
    D1 = Q_MEM - (Kconv_T*(T1-(Q_MEM/K_MEM)-Ta)) - (S_TEG*(T1-
(Q_MEM/K_MEM))*CUR) - (K_TEG*delta_T) + (0.5*POUT);
    D2 = eval(D1);
    D3 = collect(D2,T1);
    M = coeffs(D3,T1);
    T1a = quartic(M(3),0,0,M(2),M(1));
    T1 = T1a(4);
    QHa = eval(Q_MEM);
    Q_MEM = QHa;

    F1 = T2 - T1 + (Q_MEM / K_MEM) + (Q_RIM / K_RIM) + delta_T;
    F2 = eval(F1);

    delta_T = bisect(F2,'delta_T',init_delta_T);
```

```
end

T1 = eval(T1);
T2 = eval(T2);
Tsub = eval(Tsub);

QHb = eval(QHa);
QCb = eval(QCa);
TH = T1 - (QHb/K_MEM);
TC = T2 + (QCb/K_RIM);
Tave = 0.5 * (TH + TC);

effC = delta_T / TH;
effg = (sqrt(1 + (Z * Tave)) - 1) / (sqrt(1 + (Z * Tave)) + (TC /
TH));
eff = effC * effg;
VOUT = eval(VOUT);
POUT = eval(POUT);
phi = POUT / (10e-3^2 * delta_T^2);

disp(sprintf('\rTEG Dimensions: L=%d um, W=%d um, D=%d mm,
N=%d',lg/1e-6, wg/1e-6, dm/1e-3, N));
disp(sprintf('T1 (membrane temperature): %f degC',T1-273.15));
disp(sprintf('T2 (rim temperature): %f degC',T2-273.15));
disp(sprintf('Tsub (substrate temperature): %f degC',Tsub-273.15));
disp(sprintf('TH (hot side temperature): %f degC',TH-273.15));
disp(sprintf('TC (cold side temperature): %f degC',TC-273.15));
disp(sprintf('Temperature Difference across TCs: %f degC',delta_T));
disp(sprintf('Open Circuit Output Voltage: %f V',VOUT));
disp(sprintf('Output Power at Matched Load Conditions: %f
mW',POUT*1000));
disp(sprintf('Carnot Efficiency: %f percent',effC*100));
disp(sprintf('TEG Efficiency: %f percent',eff*100));
disp(sprintf('TEG Efficiency Factor: %f uW/cm2K2',phi*100));
toc;

data(row,:) = [lg/1e-6 wg/1e-6 dm/1e-3 N d_spot/1e-3 T1-273.15 T2-
273.15 Tsub-273.15 TH-273.15 TC-273.15 delta_T VOUT POUT*1000 effC*100
eff*100 phi*100];

row = row + 1;
xlswrite('d:\matlab files\data\steg_model_pyrex_v3_30mm_3um.xls',
data(row-1,:), 'sheet', char(label(row)));
end
```

This is the MATLAB program used to calculate the performance parameters of the TEG using the analytical model developed in section 7.1. This involves the TEG implemented on a SOI substrate with p-type silicon and aluminum as thermocouple materials.

```
tic;
clear;
format short e;
pi = 3.1416;
sbc = 5.676e-8; %Stefan-Boltzmann constant
init_delta_T = 0; %setting delta_T initially at zero for iterative
solving of delta_T using the 'bisect' function
hconv = 25; %convective flux in W/m^2K
erad = 0.6; %radiative emittance
Ta = 293.15; %ambient temperature set to 20 degC
d_lens = 28e-3; %clear diameter of lens after placing in lens mount
lens_ap = 0.9; %clear aperture of lens
d_lens_eff = d_lens * lens_ap; %effective lens diameter
abs = 0.5; %membrane absorptance
trans = 0.9;%lens transmittance
qs = 1000; %solar heat flux in W/m^2
t_sub = 500e-6; %substrate thickness
t_sio2 = 400e-9; %buried oxide layer thickness
t_handle = 5e-6; %thickness of handle layer under membrane and
thermoelements

teg = xlsread('d:\matlab files\data\teg_dimensions_3um.xlsx'); %read
XLS file containing TEG geometry
header = {'L(um)' 'W(um)' 'D(mm)' 'N' 'Dh(mm)' 'T1(degC)' 'T2(degC)'
'Tsub(degC)' 'TH(degC)' 'TC(degC)' 'delta_T' 'VOUT(V)' 'POUT(mW)'
'effC(%)' 'eff(%)' 'phi(uW/cm2K2)'};
xlswrite('d:\matlab files\data\steg_model_pyrex_v3_75mm_3um.xls',
header, 'sheet', 'A1');
label =
{'A1','A2','A3','A4','A5','A6','A7','A8','A9','A10','A11','A12','A13',
'A14','A15','A16','A17','A18','A19','A20','A21','A22','A23','A24','A25
','A26','A27','A28','A29','A30','A31','A32','A33','A34','A35','A36','A
37','A38','A39','A40','A41','A42','A43'};
row = 1;

while row < 11

% TEG dimensions
lg = teg(row,1) * 1e-6; % thermoelement length
wg = teg(row,2) * 1e-6; %thermoelement width
dm = teg(row,3) * 1e-3; %membrane diameter
N = teg(row,4); %number of thermocouples
tg = 3e-6; %thermoelement thickness
d_spot = 1e-3; %diameter of heated area

% silicon properties
s1 = 397e-6; %seebeck coefficient
r1 = 8.94e-5; %electrical resistivity
k1 = 146; %thermal conductivity

% aluminum properties
s2 = -1.8e-6; %seebeck coefficient
r2 = 2.65e-8; %electrical resistivity
```

```
k2 = 237; %thermal conductivity

% sio2 properties
k3 = 1.4; %thermal conductivity

kc = k1; %thermal conductance of cold side material
kh = k1; %thermal conductance of hot side material

% thermocouple properties
s_tc = s1 - s2; %seebeck coefficient
r_tc = r1 + r2; %electrical resistivity
k_tc = k1 + k2; %thermal conductivity
Z = s_tc^2/(r_tc*k_tc); %thermoelectric figure of merit

% thermoelectric generator properties
S_TEG = N * s_tc; %seebeck coefficient of TEG
R_TEG = N * r_tc * lg / (wg * tg); %electrical resistance of TEG
K_TEG = (N * k_tc * wg * tg / lg) + ((2*pi*k3*t_sio2) /
log(((dm/2)+lg)/((dm/2)))); %thermal conductance of TEG

if dm > d_spot
    K_MEM = (2*pi*kh*tg / log((dm/2)/(d_spot/2))) + (2*pi*k3*t_sio2 /
log((dm/2)/(d_spot/2))) + (2*pi*k1*t_handle / log((dm/2)/(d_spot/2)));
else
    K_MEM = (kh*pi*(dm/2)^2 / tg) + (k3*pi*(dm/2)^2 / t_sio2) +
(k1*pi*(dm/2)^2 / t_handle);
end
K_BOX = (k3*pi*(d_spot/2)^2 / t_sio2);
K_HAN = (k1*pi*(d_spot/2)^2 / t_handle);

K_RIM = (2*pi*(kc*tg + k3*t_sio2 + k1*t_handle + k1*t_sub) / log((5e-
3)/((dm/2)+lg)));

% convection parameters
Aconv_R = (((10e-3)^2 - (pi*((dm/2)+lg)^2))) + (4*10e-
3*(tg+t_sio2+t_sub));
Aconv_M = pi*((dm/2)^2);
Aconv_T = 2*N*lg*wg;
Aconv_Han = (pi*((dm/2)+lg)^2);
Kconv_R = hconv * Aconv_R;
Kconv_M = hconv * Aconv_M;
Kconv_T = hconv * Aconv_T;
Kconv_Han = hconv * Aconv_Han;

% radiation parameters
Arad_R = (((10e-3)^2 - (pi*((dm/2)+lg)^2)));
Arad_M = pi*((dm/2)^2);

% computation of input heat flux
Ah = (pi*(d_spot/2)^2) + (2*pi*(d_spot/2)*tg); % membrane heated
surface area
qh = abs * trans * qs * (d_lens_eff/d_spot)^2;
Qin =  qh * Ah;

syms delta_T T1 T2;

% output voltage and power
VOUT = S_TEG * delta_T;
POUT = VOUT^2 / (4 * R_TEG);
```

```
CUR = VOUT / (2 * R_TEG);

VOUT = eval(VOUT);
POUT = eval(POUT);
CUR = eval(CUR);

if erad == 0
    Q_RIM = Kconv_R*(T2-Ta);
    C1 = Q_RIM + (Kconv_T*(T2+(Q_RIM/K_RIM)-Ta)) -
(S_TEG*(T2+(Q_RIM/K_RIM))*CUR) - (K_TEG*delta_T) - (0.5*POUT);
    C2 = eval(C1);
    T2a = solve(C2,'T2');
    T2 = T2a;
    QCa = eval(Q_RIM);
    Q_RIM = QCa;

    Than =
(((K_BOX+K_HAN)*T1)+(Kconv_Han*Ta))/(Kconv_Han+K_BOX+K_HAN);
    Q_MEM = Qin - (Kconv_M*(T1-Ta)) - ((K_BOX+K_HAN)*(T1-Than));
    D1 = Q_MEM - (Kconv_T*(T1-(Q_MEM/K_MEM)-Ta)) - (S_TEG*(T1-
(Q_MEM/K_MEM))*CUR) - (K_TEG*delta_T) + (0.5*POUT) ;
    D2 = eval(D1);
    T1a = solve(D2,'T1');
    T1 = T1a;
    QHa = eval(Q_MEM);
    Q_MEM = QHa;

    F1 = T2 - T1 + (Q_MEM / K_MEM) + delta_T + (Q_RIM / K_RIM);
    F2 = eval(F1);
    Ttemp = solve(F2,'delta_T');
    Ttemp = subs(Ttemp);
    delta_T = Ttemp(2);

else
    Q_RIM = (Kconv_R*(T2-Ta)) + (erad*sbc*Arad_R*(T2^4-Ta^4));
    C1 = Q_RIM + (Kconv_T*(T2+(Q_RIM/K_RIM)-Ta)) -
(S_TEG*(T2+(Q_RIM/K_RIM))*CUR) - (K_TEG*delta_T) - (0.5*POUT);
    C2 = eval(C1);
    C3 = collect(C2,T2);
    L = coeffs(C3,T2);
    T2a = quartic(L(3),0,0,L(2),L(1));
    if hconv == 0
        T2 = T2a(2);
    else
        T2 = T2a(4);
    end
    QCa = eval(Q_RIM);
    Q_RIM = QCa;

    Than =
(((K_BOX+K_HAN)*T1)+(Kconv_Han*Ta))/(Kconv_Han+K_BOX+K_HAN);
    Q_MEM = Qin - (Kconv_M*(T1-Ta)) - (erad*sbc*Arad_M*(T1^4-Ta^4)) -
((K_BOX+K_HAN)*(T1-Than));
    D1 = Q_MEM - (Kconv_T*(T1-(Q_MEM/K_MEM)-Ta)) - (S_TEG*(T1-
(Q_MEM/K_MEM))*CUR) - (K_TEG*delta_T) + (0.5*POUT);
    D2 = eval(D1);
    D3 = collect(D2,T1);
    M = coeffs(D3,T1);
    T1a = quartic(M(3),0,0,M(2),M(1));
    T1 = T1a(4);
```

```
    QHa = eval(Q_MEM);
    Q_MEM = QHa;

    F1 = T2 - T1 + (Q_MEM / K_MEM) + (Q_RIM / K_RIM) + delta_T;
    F2 = eval(F1);

    delta_T = bisect(F2,'delta_T',init_delta_T);

end

T1 = eval(T1);
T2 = eval(T2);
Than = eval(Than);

QHb = eval(QHa);
QCb = eval(QCa);
TH = T1 - (QHb/K_MEM);
TC = T2 + (QCb/K_RIM);
Tave = 0.5 * (TH + TC);

effC = delta_T / TH;
effg = (sqrt(1 + (Z * Tave)) - 1) / (sqrt(1 + (Z * Tave)) + (TC /
TH));
eff = effC * effg;
VOUT = eval(VOUT);
POUT = eval(POUT);
phi = POUT / (10e-3^2 * delta_T^2);

disp(sprintf('\rTEG Dimensions: L=%d um, W=%d um, D=%d mm,
N=%d',lg/1e-6, wg/1e-6, dm/1e-3, N));
disp(sprintf('T1 (membrane temperature): %f degC',T1-273.15));
disp(sprintf('T2 (rim temperature): %f degC',T2-273.15));
disp(sprintf('Than (handle layer temperature): %f degC',Than-273.15));
disp(sprintf('TH (hot side temperature): %f degC',TH-273.15));
disp(sprintf('TC (cold side temperature): %f degC',TC-273.15));
disp(sprintf('Temperature Difference across TCs: %f degC',delta_T));
disp(sprintf('Open Circuit Output Voltage: %f V',VOUT));
disp(sprintf('Output Power at Matched Load Conditions: %f
mW',POUT*1000));
disp(sprintf('Carnot Efficiency: %f percent',effC*100));
disp(sprintf('TEG Efficiency: %f percent',eff*100));
disp(sprintf('TEG Efficiency Factor: %f uW/cm2K2',phi*100));
toc;

data(row,:) = [lg/1e-6 wg/1e-6 dm/1e-3 N d_spot/1e-3 T1-273.15 T2-
273.15 Than-273.15 TH-273.15 TC-273.15 delta_T VOUT POUT*1000 effC*100
eff*100 phi*100];

row = row + 1;
xlswrite('d:\matlab files\data\steg_model_soi_v3_30mm_3um.xls',
data(row-1,:), 'sheet', char(label(row)));
end
```

Appendix B: TEG Performance Parameters

The calculated performance parameters of the different TEGs to be fabricated are listed here. The Matlab program in Appendix A for a TEG with fully suspended membrane and thermoelements is used for the computations. In all the tables below, the thickness of the device layer is set to 5 μm, $\alpha_{mem} = 0.5$, $\tau_{lens} = 0.9$, $\varepsilon = 0.6$, and $h_{conv} = 25$ W/m^{2}K, and $d_{spot} = 1$ mm.

Table B-1: Performance parameters of TEGs with 1-μm wide trenches for an input heat flux of 100 kW/m^2.

l (μm)	w (μm)	d_{mem} (mm)	N	T_H (°C)	T_C (°C)	ΔT (°C)	V_{TEG} (V)	P_{OUT} (mW)	η_C (%)	Φ (μW/cm^{2}K^2)
100	15	1	66	32.60	30.67	1.85	0.046	0.00060	0.61	0.1752
200	15	1	66	34.35	30.63	3.68	0.092	0.00119	1.20	0.0876
300	15	1	66	36.06	30.60	5.50	0.137	0.00177	1.78	0.0584
400	15	1	66	37.90	30.56	7.29	0.181	0.00233	2.34	0.0438
500	15	1	66	39.62	30.53	9.06	0.225	0.00288	2.90	0.0350
750	15	1	66	43.80	30.46	13.37	0.332	0.00417	4.22	0.0234
1000	15	1	66	47.88	30.39	17.47	0.434	0.00535	5.44	0.0175
200	10	1	88	34.75	30.63	4.14	0.137	0.00134	1.35	0.0779
200	20	1	51	34.28	30.63	3.58	0.069	0.00115	1.16	0.0903
200	25	1	44	34.01	30.63	3.32	0.055	0.00107	1.08	0.0974
200	30	1	34	34.28	30.63	3.58	0.046	0.00115	1.16	0.0903
200	15	2	138	31.80	30.12	1.65	0.086	0.00050	0.54	0.1832
200	15	3	213	30.19	29.28	0.94	0.076	0.00025	0.31	0.2828
200	15	4	288	28.90	28.24	0.59	0.064	0.00013	0.19	0.3823
200	15	5	348	27.68	27.22	0.40	0.052	0.00007	0.13	0.4620
200	15	7	488	25.78	25.61	0.18	0.033	0.00002	0.06	0.6478
500	15	3	213	31.37	29.10	2.28	0.183	0.00059	0.75	0.1131
500	15	5	348	28.03	27.07	0.95	0.124	0.00017	0.31	0.1848
500	15	7	488	25.92	25.48	0.41	0.076	0.00004	0.14	0.2591
1000	15	3	213	33.14	28.85	4.27	0.343	0.00103	1.39	0.0566
1000	15	5	348	28.61	26.86	1.73	0.227	0.00028	0.57	0.0924
1000	15	7	488	26.08	25.35	0.73	0.135	0.00007	0.24	0.1296

Table B-2: Performance parameters of TEGs with with 2-μm wide trenches for an input heat flux of 100 kW/m^2.

l (μm)	w (μm)	d_{mem} (mm)	N	T_H (˚C)	T_C (˚C)	ΔT (˚C)	V_{TEG} (V)	P_{OUT} (mW)	η_C (%)	Φ (μW/cm^{2}K^2)
200	15	1	41	36.55	30.63	5.92	0.091	0.00191	1.91	0.0544
500	15	1	41	45.07	30.52	14.53	0.224	0.00460	4.57	0.0218
200	15	3	141	30.69	29.28	1.42	0.076	0.00038	0.47	0.1872
500	15	3	141	32.55	29.12	3.42	0.182	0.00088	1.12	0.0749
500	20	3	116	32.27	29.12	3.13	0.137	0.00080	1.02	0.0821
500	30	3	94	31.69	29.12	2.58	0.091	0.00067	0.85	0.0998
1000	15	3	141	35.28	28.92	6.38	0.339	0.00152	2.07	0.0374
200	15	5	241	27.86	27.25	0.57	0.052	0.00011	0.19	0.3199
500	15	5	241	28.53	27.14	1.36	0.124	0.00024	0.45	0.1280
1000	15	5	241	29.51	27.02	2.48	0.225	0.00039	0.82	0.0640

Table B-3: Performance parameters of TEGs with 3 μm wide trenches for an input heat flux of 100 kW/m^2.

l (μm)	w (μm)	d_{mem} (mm)	N	T_H (˚C)	T_C (˚C)	ΔT (˚C)	V_{TEG} (V)	P_{OUT} (mW)	η_C (%)	Φ (μW/cm^{2}K^2)
200	15	1	31	38.41	30.61	7.82	0.091	0.00251	2.51	0.0412
500	15	1	34	47.94	30.50	17.47	0.224	0.00551	5.44	0.0181
200	15	3	108	31.13	29.26	1.85	0.075	0.00049	0.61	0.1434
500	15	3	111	33.42	29.09	4.32	0.181	0.00110	1.41	0.0589
500	20	3	91	33.07	29.11	3.96	0.136	0.00101	1.29	0.0644
500	30	3	81	32.10	29.13	2.99	0.091	0.00077	0.98	0.0860
1000	15	3	114	36.69	28.87	7.80	0.335	0.00184	2.52	0.0303
200	15	5	188	27.98	27.26	0.73	0.052	0.00013	0.24	0.2496
500	15	5	188	28.89	27.14	1.73	0.123	0.00030	0.57	0.0998
1000	15	5	191	30.13	27.04	3.09	0.222	0.00048	1.02	0.0507

Table B-4: Performance parameters of TEGs with 1-μm wide trenches for an input heat flux of 900 kW/m^2.

l (μm)	w (μm)	d_{mem} (mm)	N	T_H (°C)	T_C (°C)	ΔT (°C)	V_{TEG} (V)	P_{OUT} (mW)	η_C (%)	Φ (μW/cm^{2}K^2)
100	15	1	66	128.09	111.40	16.63	0.413	0.04844	4.14	0.1752
200	15	1	66	144.18	111.08	33.10	0.823	0.09597	7.93	0.0876
300	15	1	66	160.21	110.76	49.38	1.228	0.14243	11.39	0.0584
400	15	1	66	175.91	110.47	65.46	1.628	0.18771	14.58	0.0438
500	15	1	66	191.48	110.18	81.30	2.022	0.23167	17.50	0.0350
750	15	1	66	229.25	109.51	119.76	2.978	0.33511	23.84	0.0234
1000	15	1	66	265.21	108.90	156.31	3.887	0.42817	29.04	0.0175
200	10	1	88	148.27	111.08	37.22	1.234	0.10789	8.83	0.0779
200	20	1	51	143.15	111.08	32.12	0.617	0.09316	7.72	0.0903
200	25	1	44	140.83	111.07	29.79	0.494	0.08641	7.20	0.0974
200	30	1	34	143.15	111.08	32.12	0.412	0.09316	7.72	0.0903
200	15	2	138	121.62	106.77	14.76	0.768	0.03992	3.74	0.1832
200	15	3	213	107.93	99.54	8.43	0.676	0.02009	2.21	0.2828
200	15	4	288	96.06	90.81	5.24	0.569	0.01050	1.42	0.3823
200	15	5	348	85.74	82.22	3.53	0.463	0.00575	0.98	0.4620
200	15	7	488	70.22	68.58	1.56	0.287	0.00158	0.46	0.6478
500	15	3	213	118.37	98.04	20.33	1.631	0.04673	5.19	0.1131
500	15	5	348	89.33	80.92	8.39	1.101	0.01302	2.32	0.1848
500	15	7	488	71.35	67.66	3.66	0.673	0.00347	1.06	0.2591
1000	15	3	213	133.91	95.93	37.96	3.047	0.08149	9.33	0.0566
1000	15	5	348	94.55	79.24	15.32	2.009	0.02169	4.17	0.0924
1000	15	7	488	73.07	66.60	6.47	1.191	0.00543	1.87	0.1296

Table B-5: Performance parameters of TEGs with with 2-μm wide trenches for an input heat flux of 900 kW/m^2.

l (μm)	w (μm)	d_{mem} (mm)	N	T_H ($^\circ$C)	T_C ($^\circ$C)	ΔT ($^\circ$C)	V_{TEG} (V)	P_{OUT} (mW)	η_C (%)	Φ (μW/cm^{2}K^2)
200	15	1	41	164.11	110.99	53.16	0.821	0.15381	12.16	0.0544
500	15	1	41	240.01	109.92	130.10	2.010	0.36851	25.35	0.0218
200	15	3	141	112.23	99.54	12.69	0.674	0.03015	3.29	0.1872
500	15	3	141	128.53	98.07	30.46	1.618	0.06946	7.58	0.0749
500	20	3	116	125.98	98.14	27.84	1.217	0.06365	6.97	0.0821
500	30	3	94	121.11	98.14	22.99	0.814	0.05278	5.83	0.0998
1000	15	3	141	152.57	96.11	56.47	3.000	0.11938	13.26	0.0374
200	15	5	241	87.49	82.39	5.08	0.461	0.00826	1.41	0.3199
500	15	5	241	93.43	81.41	12.04	1.094	0.01857	3.29	0.1280
1000	15	5	241	102.19	80.34	21.86	1.985	0.03057	5.82	0.0640

Table B-6: Performance parameters of TEGs with 3 μm wide trenches for an input heat flux of 900 kW/m^2.

l (μm)	w (μm)	d_{mem} (mm)	N	T_H ($^\circ$C)	T_C ($^\circ$C)	ΔT ($^\circ$C)	V_{TEG} (V)	P_{OUT} (mW)	η_C (%)	Φ (μW/cm^{2}K^2)
200	15	1	31	180.96	110.83	70.14	0.819	0.20246	15.45	0.0412
500	15	1	34	265.88	109.65	156.24	2.002	0.44072	28.99	0.0181
200	15	3	108	115.84	99.35	16.50	0.671	0.03904	4.24	0.1434
500	15	3	111	136.05	97.68	38.35	1.604	0.08670	9.37	0.0589
500	20	3	91	133.06	97.86	35.22	1.208	0.07991	8.67	0.0644
500	30	3	81	124.76	98.16	26.61	0.812	0.06090	6.69	0.0860
1000	15	3	114	164.39	95.55	68.84	2.957	0.14344	15.73	0.0303
200	15	5	188	88.86	82.34	6.49	0.460	0.01051	1.79	0.2496
500	15	5	188	96.62	81.32	15.31	1.084	0.02339	4.14	0.0998
1000	15	5	191	107.53	80.36	27.18	1.956	0.03746	7.14	0.0507

Table B-7: Performance parameters of TEGs with 1-μm wide trenches for an input heat flux of 2500 kW/m^2.

l (μm)	w (μm)	d_{mem} (mm)	N	T_H (°C)	T_C (°C)	ΔT (°C)	V_{TEG} (V)	P_{OUT} (mW)	η_C (%)	Φ (μW/cm^{2}K^2)
100	15	1	66	292.90	246.77	46.05	1.145	0.37167	8.14	0.1752
200	15	1	66	337.52	245.89	91.58	2.278	0.73489	15.00	0.0876
300	15	1	66	381.47	245.02	136.49	3.394	1.08822	20.85	0.0584
400	15	1	66	424.79	244.13	180.68	4.493	1.43021	25.89	0.0438
500	15	1	66	467.28	243.24	224.06	5.572	1.75950	30.26	0.0350
750	15	1	66	569.30	240.92	328.35	8.166	2.51901	38.98	0.0234
1000	15	1	66	664.18	238.50	425.67	10.586	3.17509	45.41	0.0175
200	10	1	88	348.82	245.82	102.96	3.414	0.82560	16.55	0.0779
200	20	1	51	334.80	245.90	88.90	1.708	0.71350	14.62	0.0903
200	25	1	44	328.36	245.92	82.47	1.367	0.66206	13.71	0.0974
200	30	1	34	334.80	245.90	88.90	1.139	0.71350	14.62	0.0903
200	15	2	138	275.58	235.04	40.54	2.108	0.30106	7.39	0.1832
200	15	3	213	239.28	216.45	22.78	1.828	0.14674	4.45	0.2828
200	15	4	288	208.82	194.83	13.96	1.515	0.07453	2.90	0.3823
200	15	5	348	183.66	174.38	9.33	1.223	0.04019	2.04	0.4620
200	15	7	488	147.30	143.22	4.15	0.762	0.01113	0.99	0.6478
500	15	3	213	267.01	212.42	54.61	4.383	0.33728	10.11	0.1131
500	15	5	348	193.44	171.29	22.12	2.900	0.09038	4.74	0.1848
500	15	7	488	150.87	141.18	9.69	1.781	0.02431	2.28	0.2591
1000	15	3	213	307.56	206.60	100.94	8.101	0.57620	17.38	0.0566
1000	15	5	348	207.50	167.37	40.16	5.266	0.14903	8.36	0.0924
1000	15	7	488	156.13	139.09	17.07	3.139	0.03776	3.98	0.1296

Table B-8: Performance parameters of TEGs with with 2-μm wide trenches for an input heat flux of 2500 kW/m^2.

l (μm)	w (μm)	d_{mem} (mm)	N	T_H (°C)	T_C (°C)	ΔT (°C)	V_{TEG} (V)	P_{OUT} (mW)	η_C (%)	Φ (μW/cm^{2}K^2)
200	15	1	41	392.25	245.38	146.85	2.269	1.17370	22.07	0.0544
500	15	1	41	597.08	241.29	355.81	5.497	2.75623	40.89	0.0218
200	15	3	141	250.16	215.97	34.21	1.817	0.21904	6.54	0.1872
500	15	3	141	292.42	211.19	81.24	4.316	0.49416	14.36	0.0749
500	20	3	116	286.04	211.67	74.39	3.251	0.45448	13.30	0.0821
500	30	3	94	273.91	212.29	61.65	2.184	0.37948	11.27	0.0998
1000	15	3	141	352.26	204.35	147.91	7.858	0.81899	23.65	0.0374
200	15	5	241	187.92	174.52	13.41	1.218	0.05754	2.91	0.3199
500	15	5	241	203.37	171.78	31.62	2.871	0.12791	6.63	0.1280
1000	15	5	241	225.65	168.76	56.89	5.166	0.20711	11.41	0.0640

Table B-9: Performance parameters of TEGs with 3 μm wide trenches for an input heat flux of 2500 kW/m^2.

l (μm)	w (μm)	d_{mem} (mm)	N	T_H (°C)	T_C (°C)	ΔT (°C)	V_{TEG} (V)	P_{OUT} (mW)	η_C (%)	Φ (μW/cm^{2}K^2)
200	15	1	31	438.20	244.73	193.42	2.259	1.53958	27.19	0.0412
500	15	1	34	664.72	239.73	424.98	5.444	3.26074	45.31	0.0181
200	15	3	108	259.49	215.13	44.37	1.806	0.28228	8.33	0.1434
500	15	3	111	311.10	209.38	101.72	4.254	0.60983	17.41	0.0589
500	20	3	91	303.75	210.16	93.61	3.210	0.56455	16.23	0.0644
500	30	3	81	283.01	211.86	71.16	2.172	0.43563	12.80	0.0860
1000	15	3	114	379.86	201.41	178.45	7.665	0.96385	27.33	0.0303
200	15	5	188	191.32	174.20	17.11	1.212	0.07303	3.68	0.2496
500	15	5	188	211.15	171.11	40.05	2.837	0.16015	8.27	0.0998
1000	15	5	191	238.34	167.98	70.37	5.064	0.25109	13.76	0.0507

Appendix C: TEG Wafer Layout

The layout of the wafer consisting of all the TEGs to be fabricated is shown below.

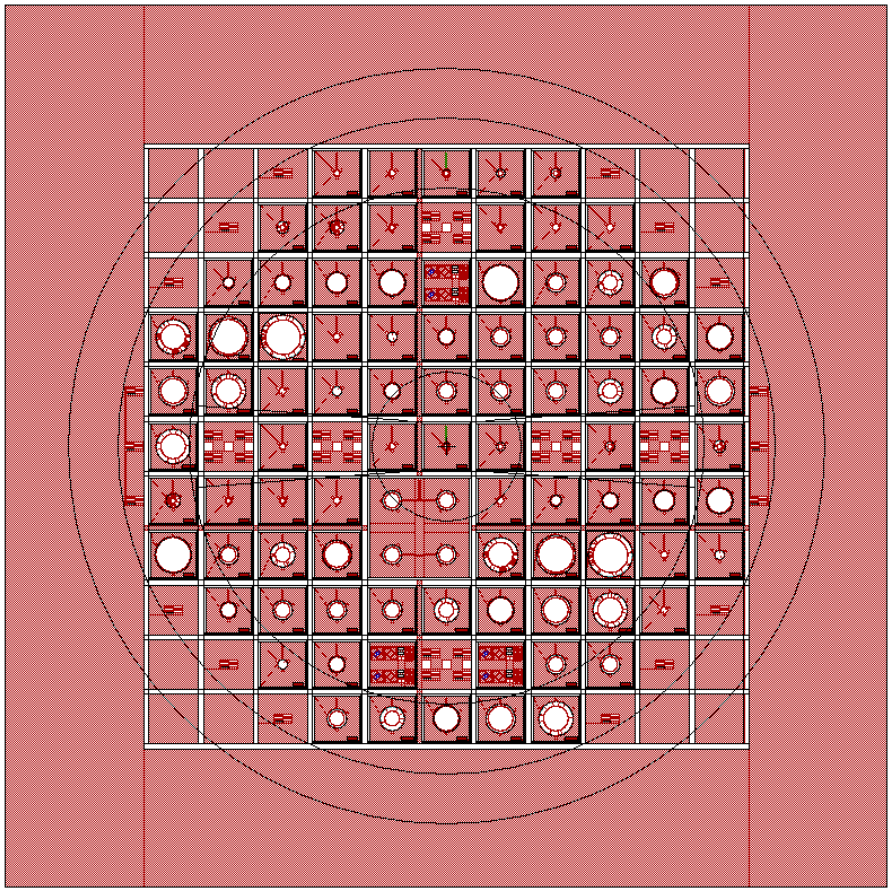


Figure C-1: 6 inch wafer layout consisting of all TEGs to be fabricated.

The floorplan of the wafer layout is shown in Figure C-2. All blue blocks are individual TEG devices while the orange block is a 2×2 TEG array. The three green blocks contain test structures discussed in section 5.2.2 and the pink blocks contain mask alignment and precision marks.

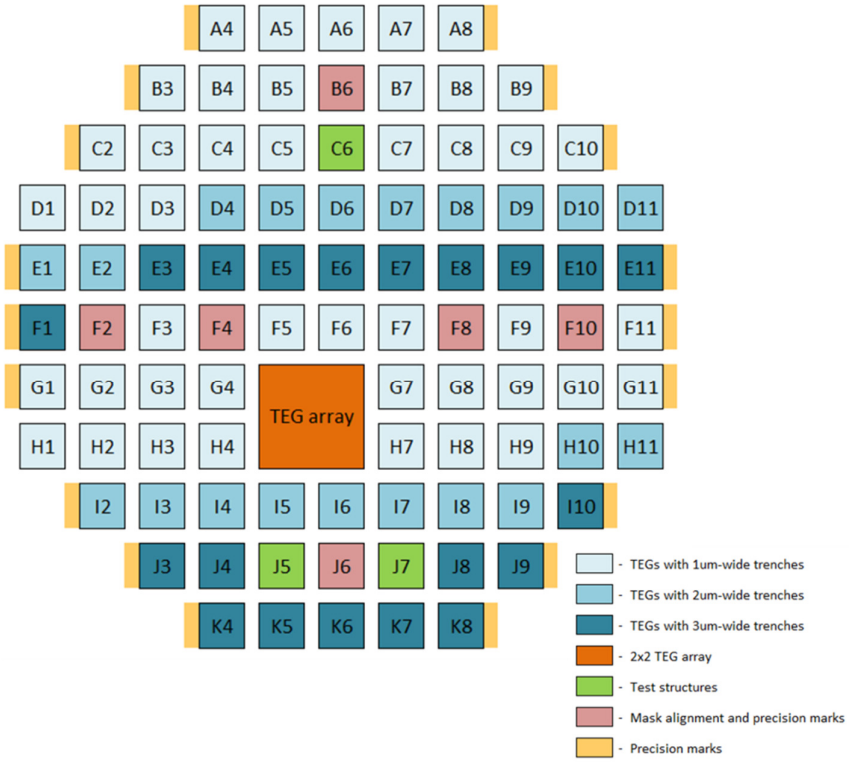


Figure C-2: Floorplan of 6 inch wafer.

Tables C-1 to C-3 list the dimensions of the TEG and other pertinent parameters of each of the blocks in Figure C-2.

Table C-1: Dimensions of TEGs with 1-μm wide trenches (L=length, W=width, D=membrane diameter, N=number of thermocouples).

Block Name	l (μm)	w (μm)	d_{mem} (mm)	N	Block Name	l (μm)	w (μm)	d_{mem} (mm)	N
A4, F3	100	15	1	66	C2, G8	200	15	2	138
A5, F5	200	15	1	66	C3, G9	200	15	3	213
A6, F6	300	15	1	66	C4, G10	200	15	4	288
A7, F7	400	15	1	66	C5, G11	200	15	5	348
A8, F9	500	15	1	66	C7, H1	200	15	7	488
B3, F11	750	15	1	66	C8, H2	500	15	3	213
B4, G1	1000	15	1	66	C9, H3	1000	15	3	213
B5, G2	200	10	1	88	C10, H4	500	15	5	348
B7, G3	200	20	1	51	D1, H7	1000	15	5	348
B8, G4	200	25	1	44	D2, H8	500	15	7	488
B9, G7	200	30	1	34	D3, H9	1000	15	7	488

Table C-2: Dimensions of TEGs with 2-μm wide trenches.

Block Name	l (μm)	w (μm)	d_{mem} (mm)	N
D4, H10	200	15	1	41
D5, H11	500	15	1	41
D6, I2	200	15	3	141
D7, I3	500	15	3	141
D8, I4	500	20	3	116
D9, I5	500	30	3	94
D10, I6	1000	15	3	141
D11, I7	200	15	5	241
E1, I8	500	15	5	241
E2, I9	1000	15	5	241

Table C-3: Dimensions of TEGs with 3 μm wide trenches.

Block Name	l (μm)	w (μm)	d_{mem} (mm)	N
E3, I10	200	15	1	31
E4, J3	500	15	1	34
E5, J4	200	15	3	108
E6, J8	500	15	3	111
E7, J9	500	20	3	91
E8, K4	500	30	3	81
E9, K5	1000	15	3	114
E10, K6	200	15	5	188
E11, K7	500	15	5	188
F1, K8	1000	15	5	191

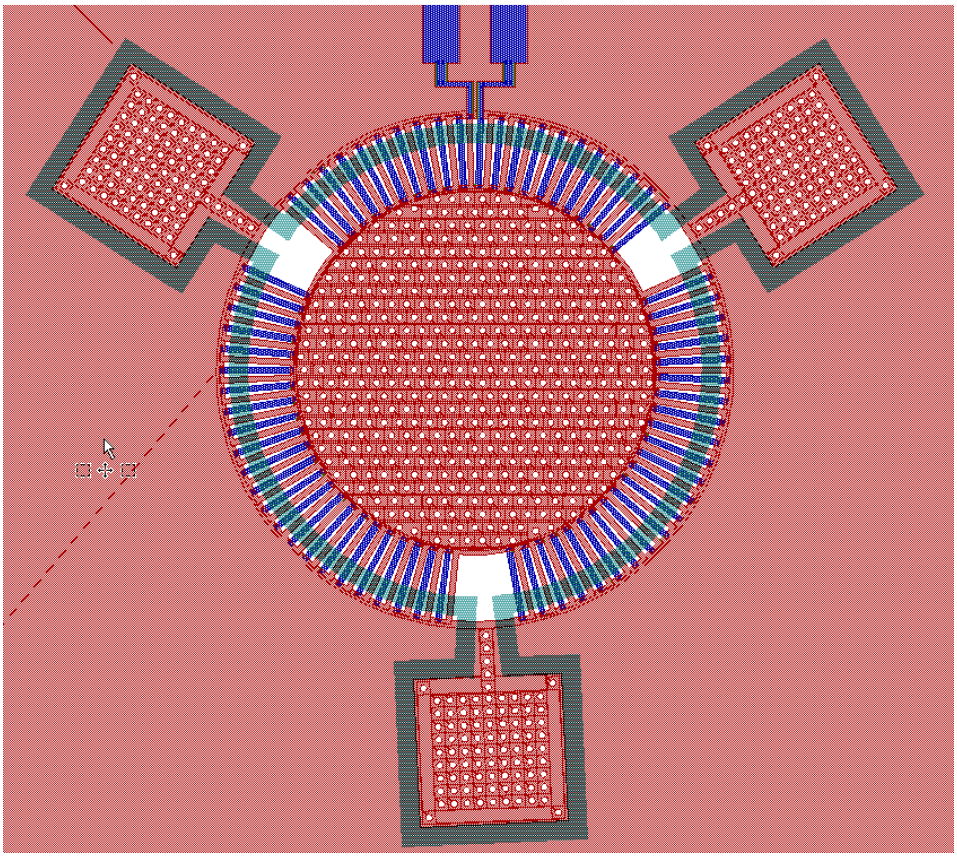


Figure C-3: Sample TEG layout ($l = 200$ µm, $w = 15$ µm, and $d_{mem} = 1$ mm with 1-µm wide trenches)

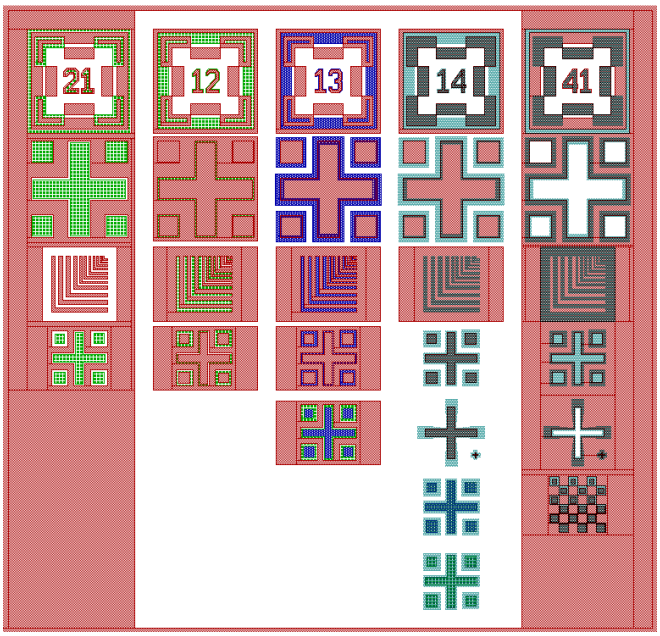


Figure C-4: Mask alignment marks

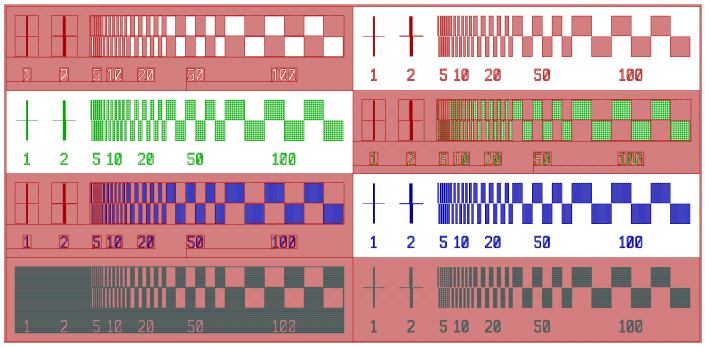


Figure C-5: Precision marks

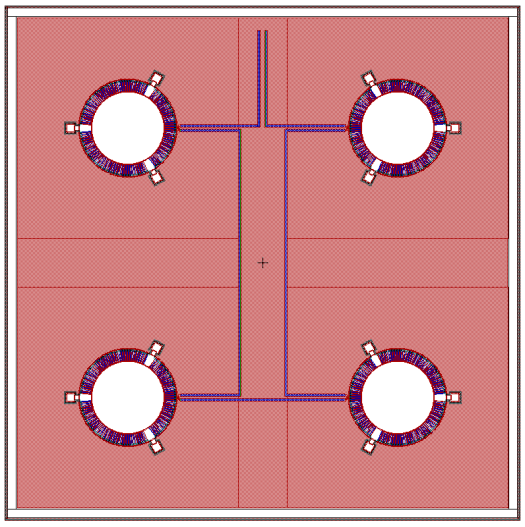


Figure C-6: 2x2 TEG array ($l = 500$ μm, $w = 15$ μm, and $d_{mem} = 3$ mm with 3 μm-wide trenches)

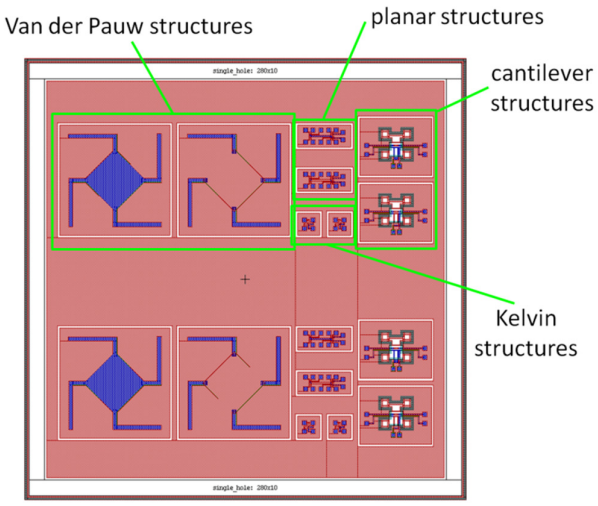


Figure C-7: Test structures

Appendix D: Proposed TEG Fabrication Process

The proposed TEG fabrication process using a SOI wafer with a pre-doped device layer is described in more detail here. The proposed fabrication sequence is outlined for a cross section AB as indicated in Figure D-1.

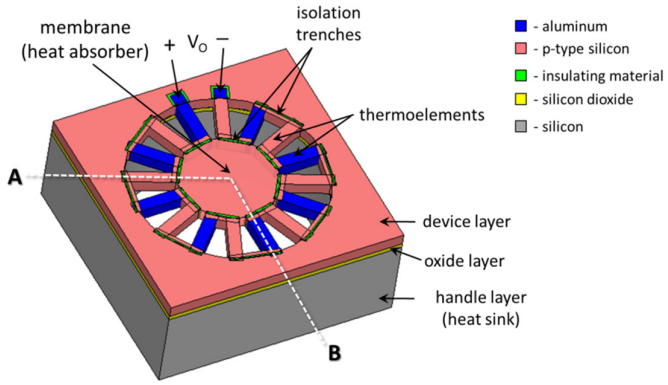
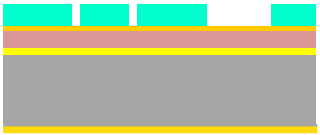
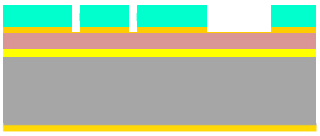
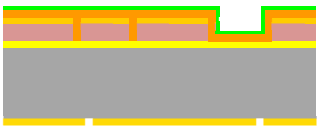
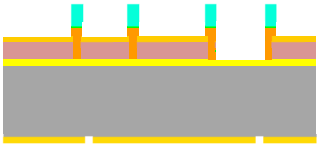
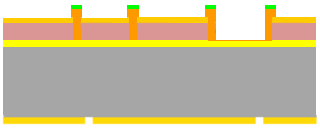
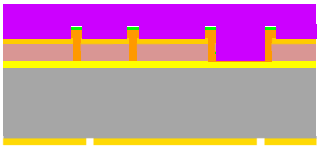
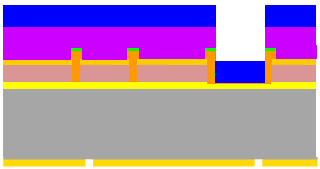
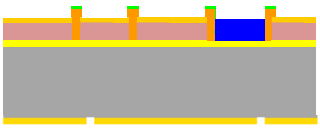
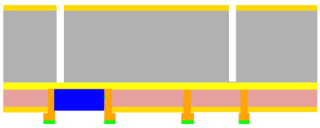
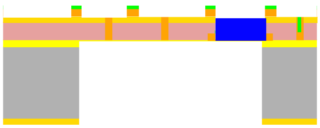


Figure D-1: TEG using a SOI wafer with a doped device layer

1. Start with clean SOI wafer	
2. Pattern hardmasks for front and back sides	
i. Deposit 1 µm SiH_4-based PECVD SiO_2 at SOI frontside.	
ii. Clean wafer with IPA and blow-dry with N_2 gun. Deposit 3.6 µm SiH_4-based PECVD SiO_2 at SOI backside.	
iii. Clean wafer with FNA then spin 6 µm thick AZ9260 photoresist at SOI frontside.	

iv. Pattern photoresist (*mask #1*).	
v. Anisotropically etch SiO_2 using ICP etcher.	
vi. Strip photoresist using O_2 plasma.	
vii. Clean wafer with FNA then spin 6 µm thick AZ9260 photoresist at SOI backside.	
viii. Pattern photoresist (*mask #4*).	
ix. Anisotropically etch SiO_2 using ICP etcher.	
x. Strip photoresist using O_2 plasma.	
3. Frontside RIE to form Si thermoelements and etch out areas for trenches and Al	
i. Clean wafer with FNA then etch SOI device layer using RIE.	
4. Deposition and etching of dielectric material to refill isolation trenches	

i. Clean wafer with FNA then deposit 3.6 µm TEOS SiO_2 and 360 nm Si_3N_4 by PECVD	
ii. Clean wafer with FNA then spin 6 µm thick AZ9260 photoresist.	
iii. Pattern photoresist (*mask #2*)	
iv. Anisotropically etch SiO_2 and Si_3N_4 using ICP etcher.	
v. Strip photoresist using O_2 plasma.	
5. Al deposition and lift-off to form Al thermoelements, wires, and pads	
i. Clean wafer with FNA then spin 14 µm thick AZnlof2070 photoresist	
ii. Pattern photoresist (*mask #3*)	

iii. Dip wafer in 20:1 HF for 30 sec then deposit 6 μm thick Al by e-beam evaporation	
iv. Al lift-off using NMP solvent	
6. Backside DRIE to form backside trenches	
i. Clean wafer with IPA then etch SOI handle layer using DRIE.	
7. HF vapor etching	
i. HF vapor etching to release membrane and thermoelements (membrane is perforated in *mask#1* for this purpose).	

Appendix E: TEG Fabrication on a Glass Substrate

The TEG fabrication process using a Pyrex substrate with HWCVD boron-doped polysilicon and aluminum as thermoelements is described in more detail here. The fabrication sequence is outlined for a cross section AB as indicated in Figure E-1.

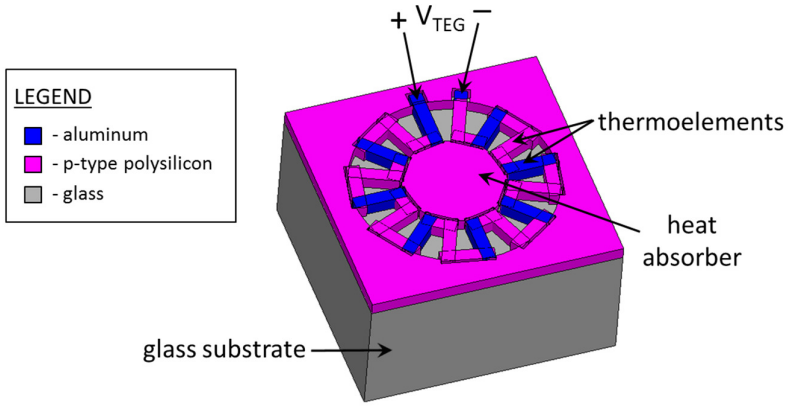


Figure E-1: TEG fabricated on a Pyrex wafer.

1. Start with clean Pyrex wafer.	
2. Deposit 1 µm HWCVD p-type polysilicon.	
3. Etch HWCVD polysilicon to form the first thermoelements.	
i. Clean wafer with FNA then spin 6 µm thick AZ9260 photoresist.	
ii. Pattern photoresist (*mask #1*).	
iii. Anisotropically etch HWCVD polysilicon SiO_2 using RIE.	

iv. Strip photoresist using O_2 plasma.	
4. Al deposition and lift-off to form Al thermoelements, wires, and pads	
i. Clean wafer with FNA then spin 14 µm thick AZnlof2070 photoresist	
ii. Pattern photoresist (*mask #3*)	
iii. Dip wafer in 20:1 HF for 30 sec then deposit 1 µm thick Al by e-beam evaporation	
iv. Al lift-off using NMP solvent	
5. Spin coat wafer with 1 µm thick S1813 photoresist.	
6. Separate TEG chips from each other using a dicing saw.	
7. Strip photoresist from each chip using acetone, IPA, and DI water.	

Appendix F: TEG Fabrication on a SOI Substrate

The TEG fabrication process using a SOI wafer with the buried oxide layer under the membrane and thermoelements retained is described in more detail here. The proposed fabrication sequence is outlined for a cross section AB as indicated in Figure F-1.

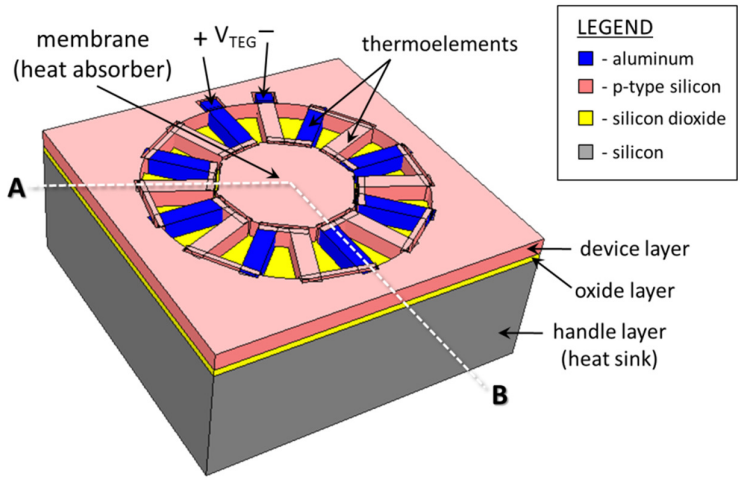


Figure F-1: TEG fabricated on a SOI wafer with the buried oxide layer under the membrane and thermoelements retained.

1. Start with clean SOI wafer	
2. Pattern hardmasks for front and back sides	
i. Deposit 500 nm SiH_4-based PECVD SiO_2 at SOI frontside.	
ii. Clean wafer with IPA and blow-dry with N_2 gun. Deposit 3.6 µm SiH_4-based PECVD SiO_2 at SOI backside.	
iii. Clean wafer with FNA then spin 6 µm thick AZ9260 photoresist at SOI frontside.	

iv. Pattern photoresist (*mask #1*).	
v. Anisotropically etch SiO_2 using ICP etcher.	
vi. Strip photoresist using O_2 plasma.	
vii. Clean wafer with FNA then spin 6 μm thick AZ9260 photoresist at SOI backside.	
viii. Pattern photoresist (*mask #5*).	
ix. Anisotropically etch SiO_2 using ICP etcher.	
x. Strip photoresist using O_2 plasma.	
3. Frontside RIE to form Si thermoelements and etch out areas for trenches and Al	
i. Clean wafer with FNA then etch SOI device layer using DRIE.	
ii. Strip frontside mask in 7:1 HF solution for 2 minutes.	

4. Al deposition and lift-off to form Al thermoelements, wires, and pads	
i. Clean wafer with FNA then spin 14 µm thick AZnlof2070 photoresist	
ii. Pattern photoresist (*mask #3*)	
iii. Dip wafer in 20:1 HF for 30 sec then deposit 3 µm thick Al by e-beam evaporation	
iv. Al lift-off using NMP solvent	
5. Backside DRIE to partially etch handle layer under membrane and thermoelements.	
i. Clean wafer with IPA then etch SOI handle layer using DRIE.	
6. Spin coat wafer frontside with 1 µm thick S1813 photoresist.	
7. Separate TEG chips from each other using a dicing saw.	
8. Strip photoresist from each chip using acetone, IPA, and DI water.	
9. Backside DRIE at chip level to thin out handle layer under membrane and thermoelements.	
i. Thin out SOI handle layer using DRIE at chip level.	

Appendix G: Laser Measurements (TEG on Glass)

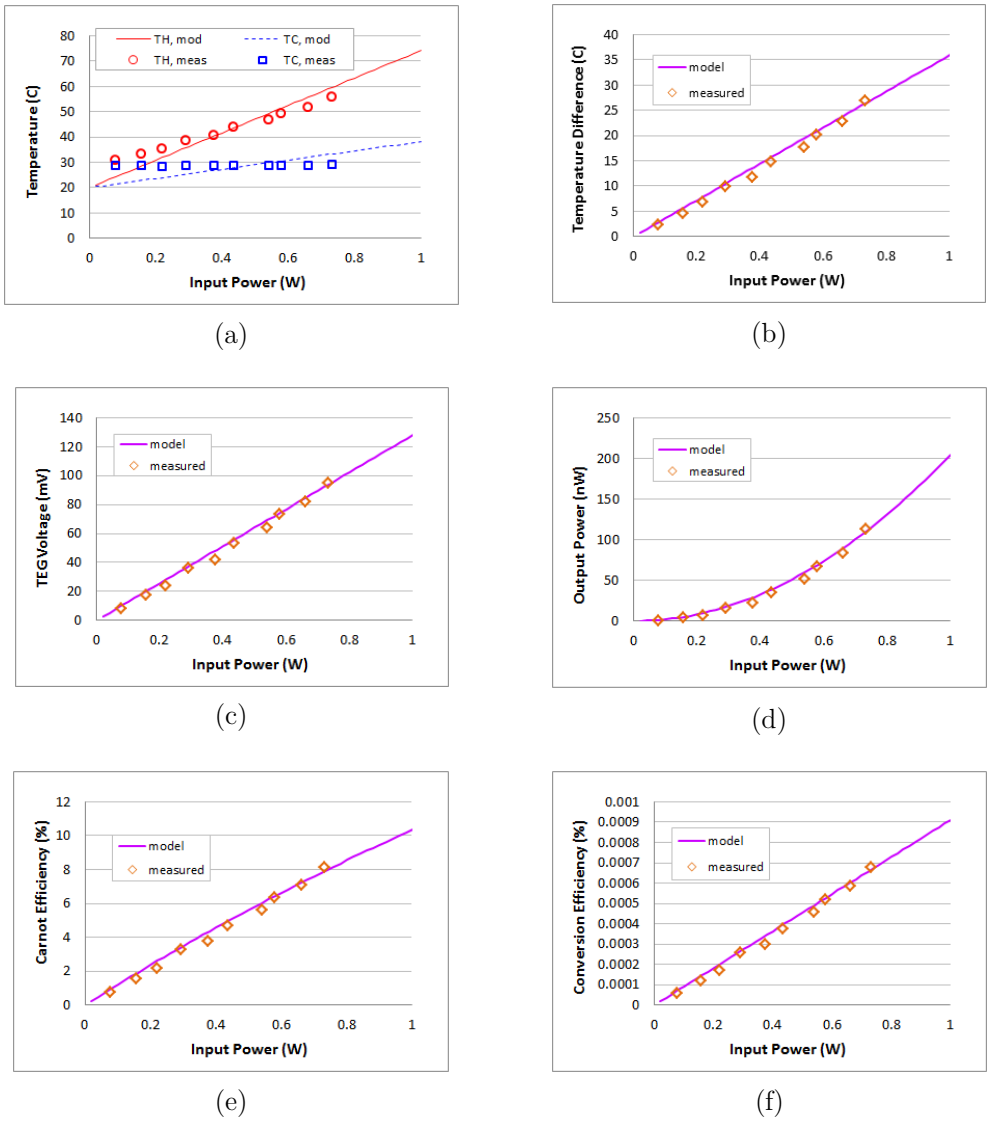


Figure G-1: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 200$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 31$.

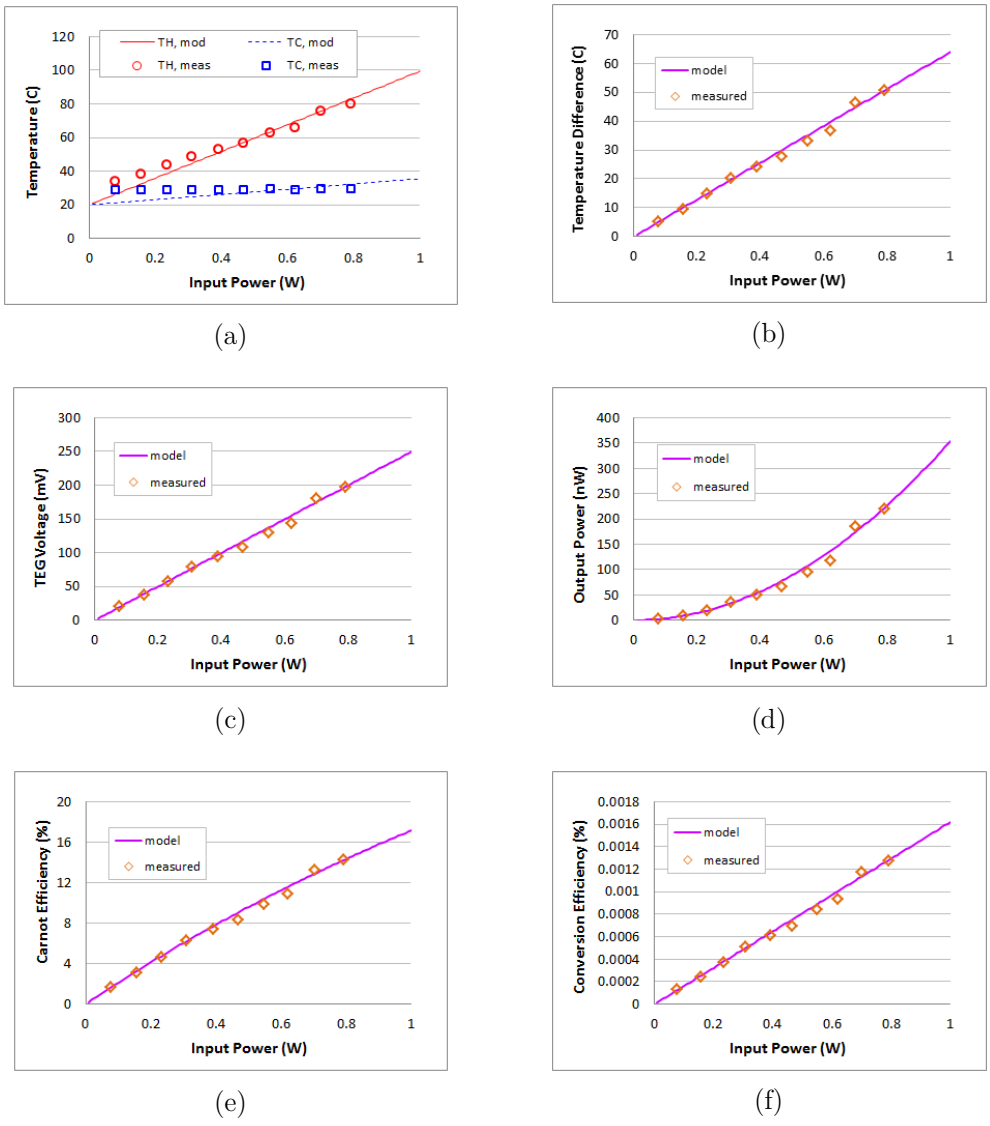


Figure G-2: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 34$.

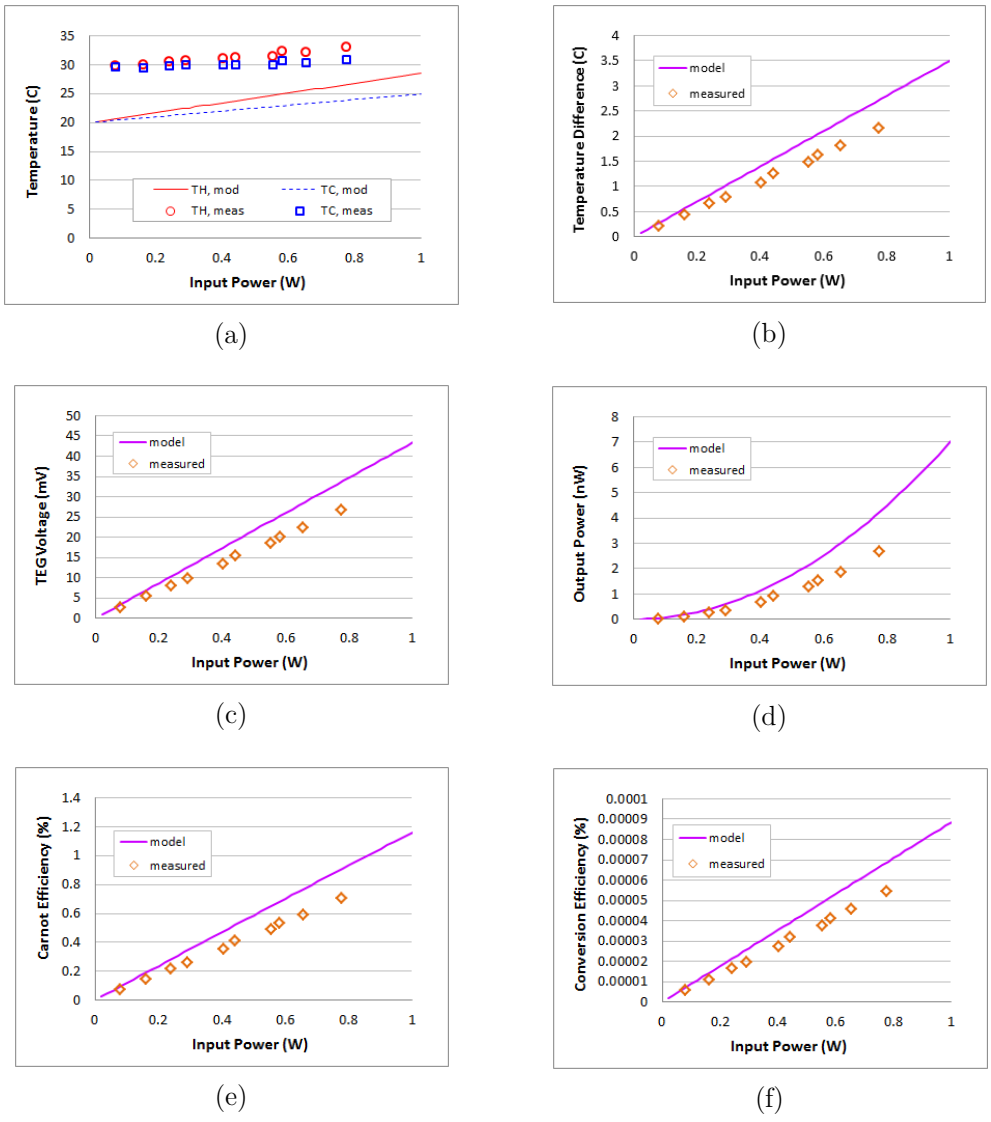


Figure G-3: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 200$ µm, $w = 15$ µm, $d_{mem} = 3$ mm, and $N = 108$.

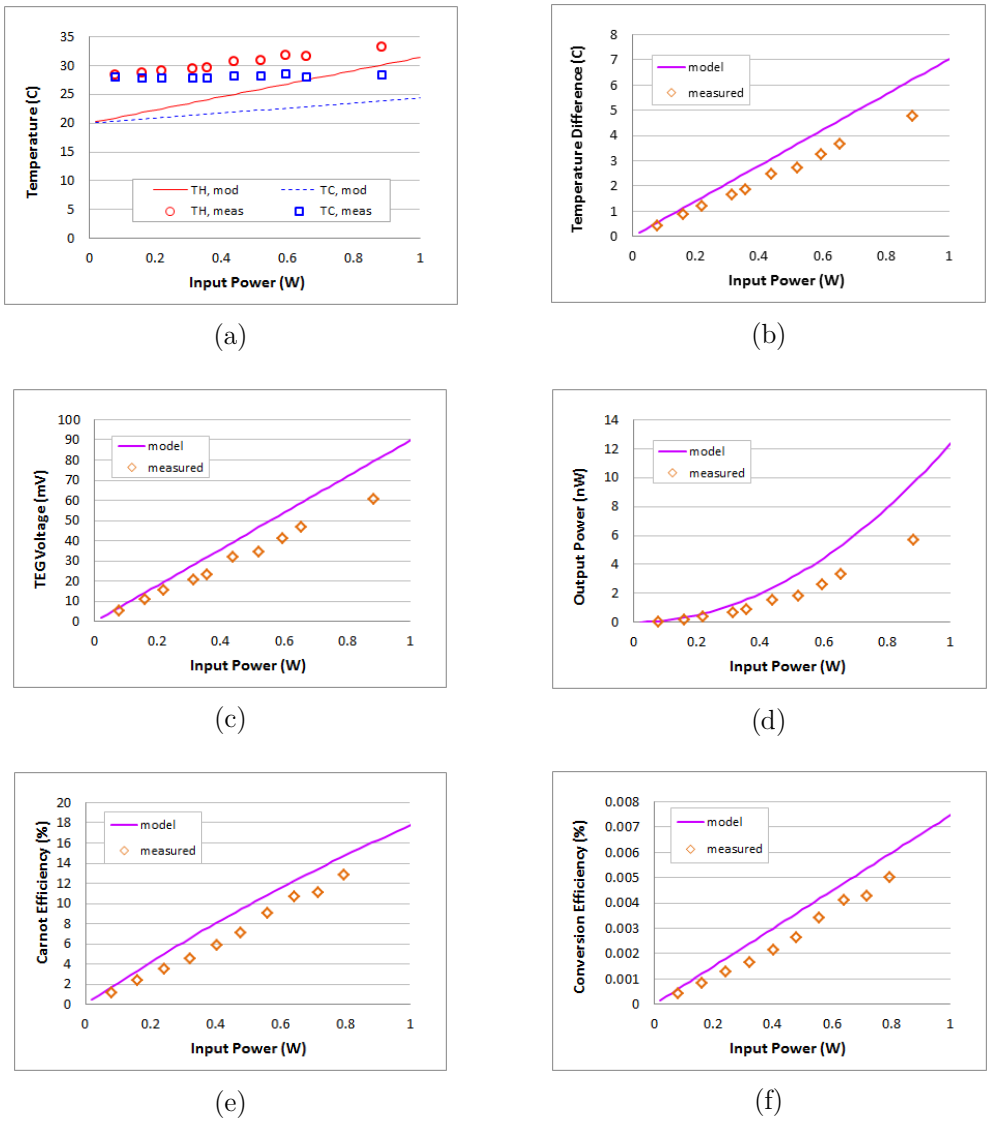


Figure G-4: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 500$ µm, $w = 15$ µm, $d_{mem} = 3$ mm, and $N = 111$.

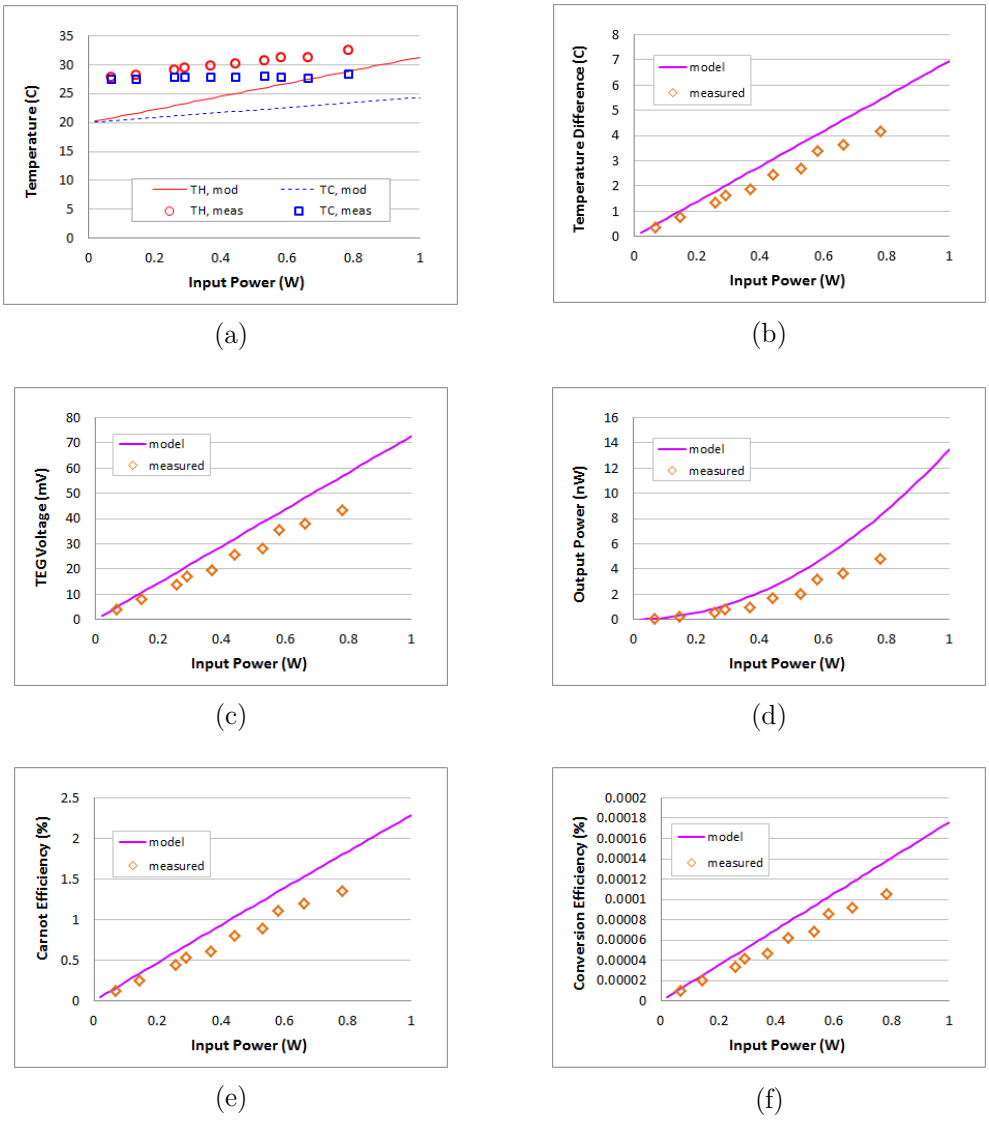


Figure G-5: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 500$ µm, $w = 20$ µm, $d_{mem} = 3$ mm, and $N = 91$.

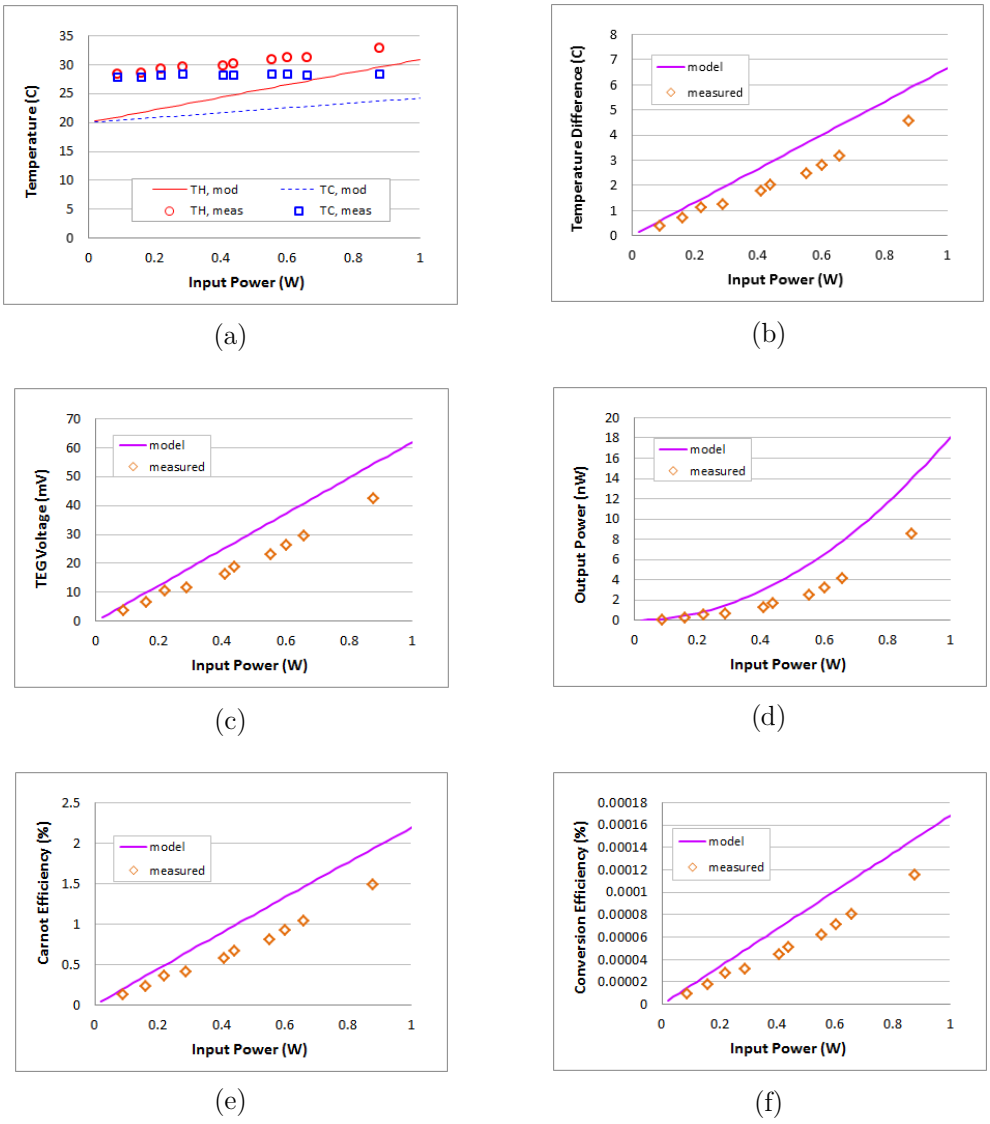


Figure G-6: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 500$ µm, $w = 30$ µm, $d_{mem} = 3$ mm, and $N = 81$.

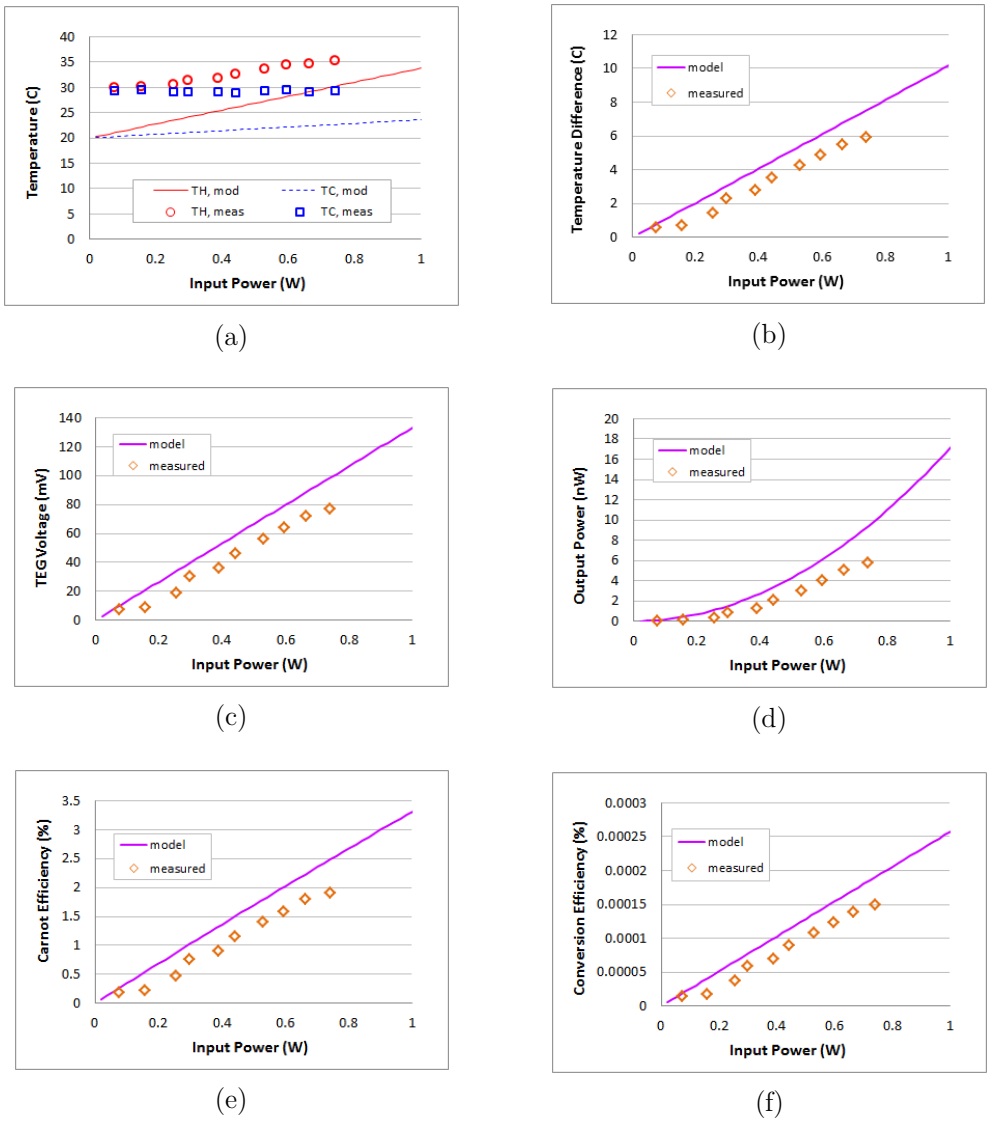
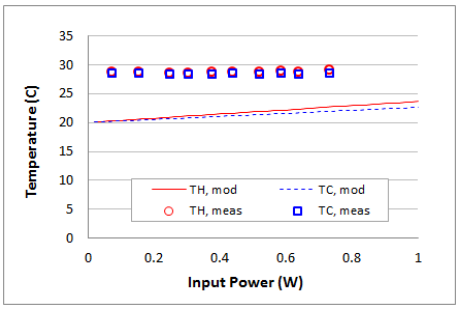
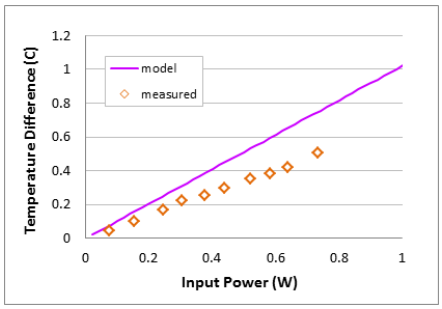


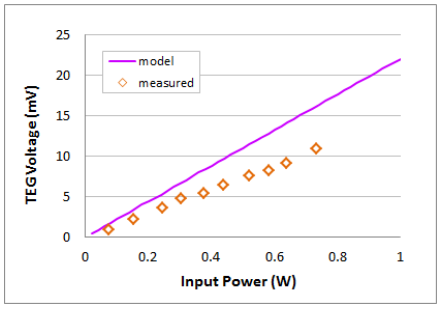
Figure G-7: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 1000$ µm, $w = 15$ µm, $d_{mem} = 3$ mm, and $N = 114$.



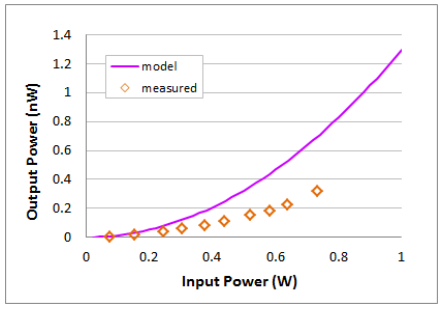
(a)



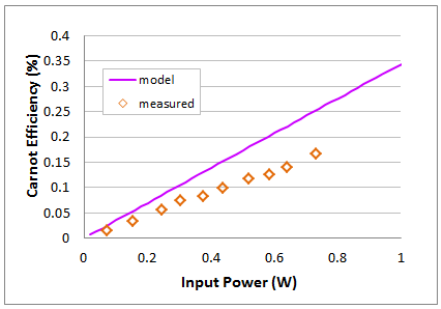
(b)



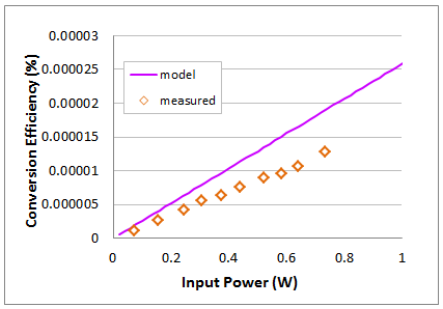
(c)



(d)



(e)



(f)

Figure G-8: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 200$ µm, $w = 15$ µm, $d_{mem} = 5$ mm, and $N = 188$.

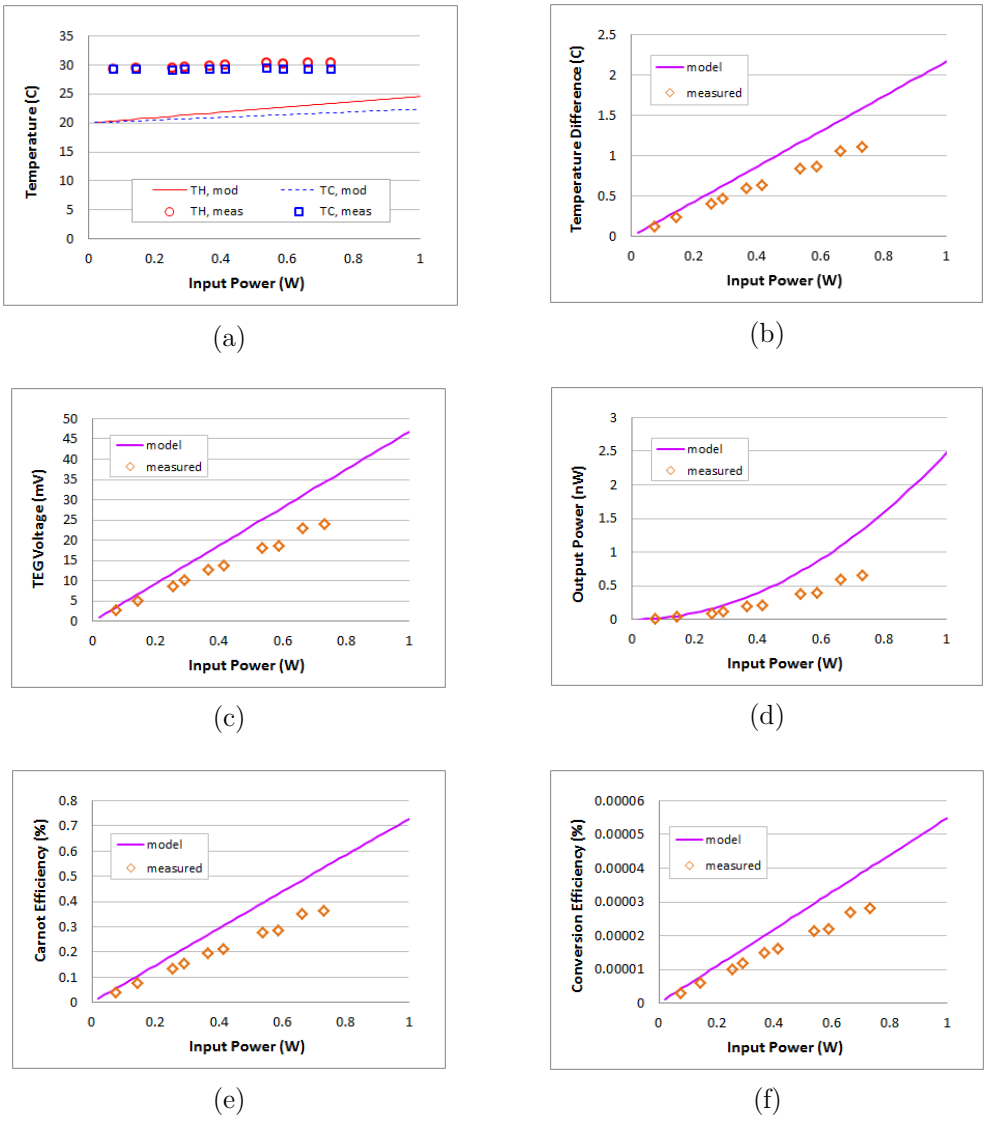


Figure G-9: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 500$ µm, $w = 15$ µm, $d_{mem} = 5$ mm, and $N = 188$.

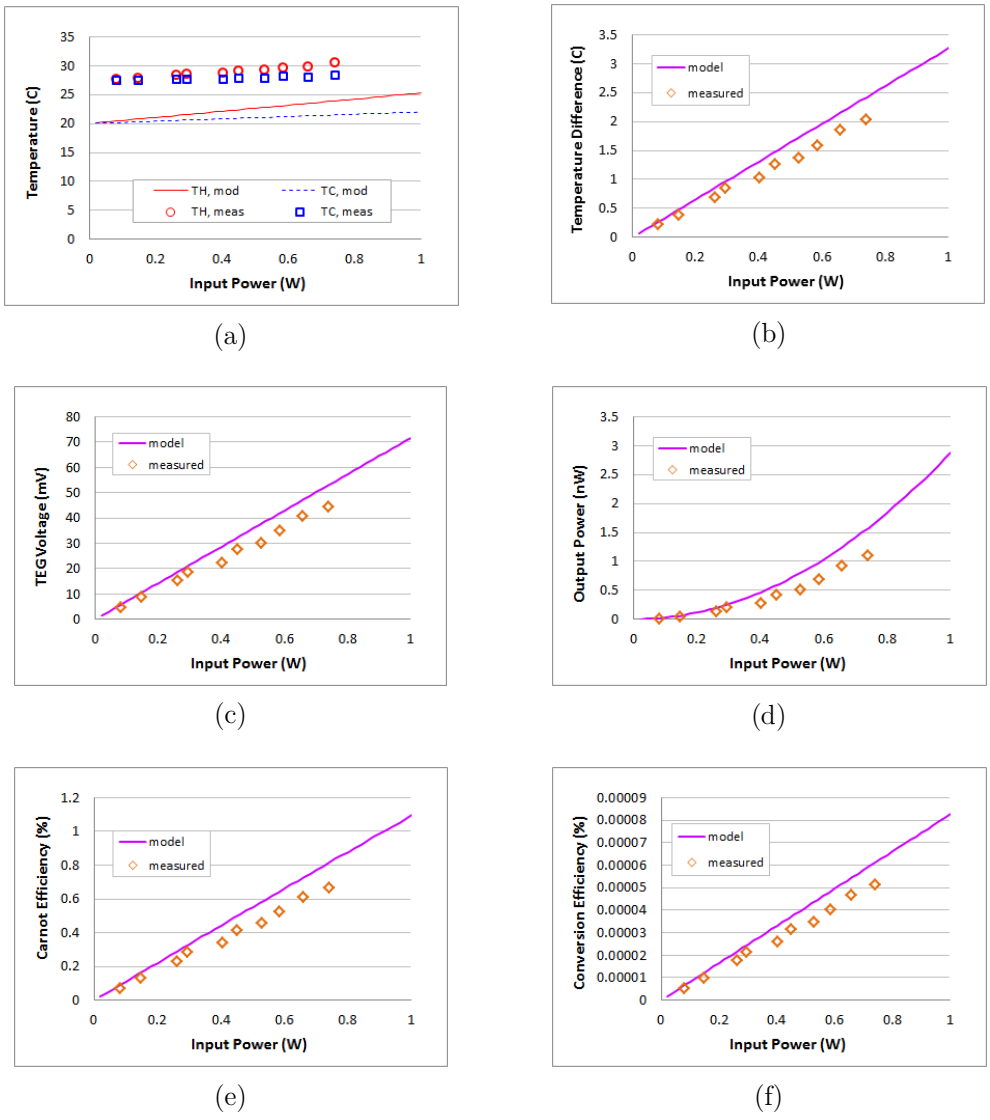


Figure G-2: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a glass substrate with $l = 1000$ µm, $w = 15$ µm, $d_{mem} = 5$ mm, and $N = 191$.

Appendix H: Laser Measurements (TEG on SOI)

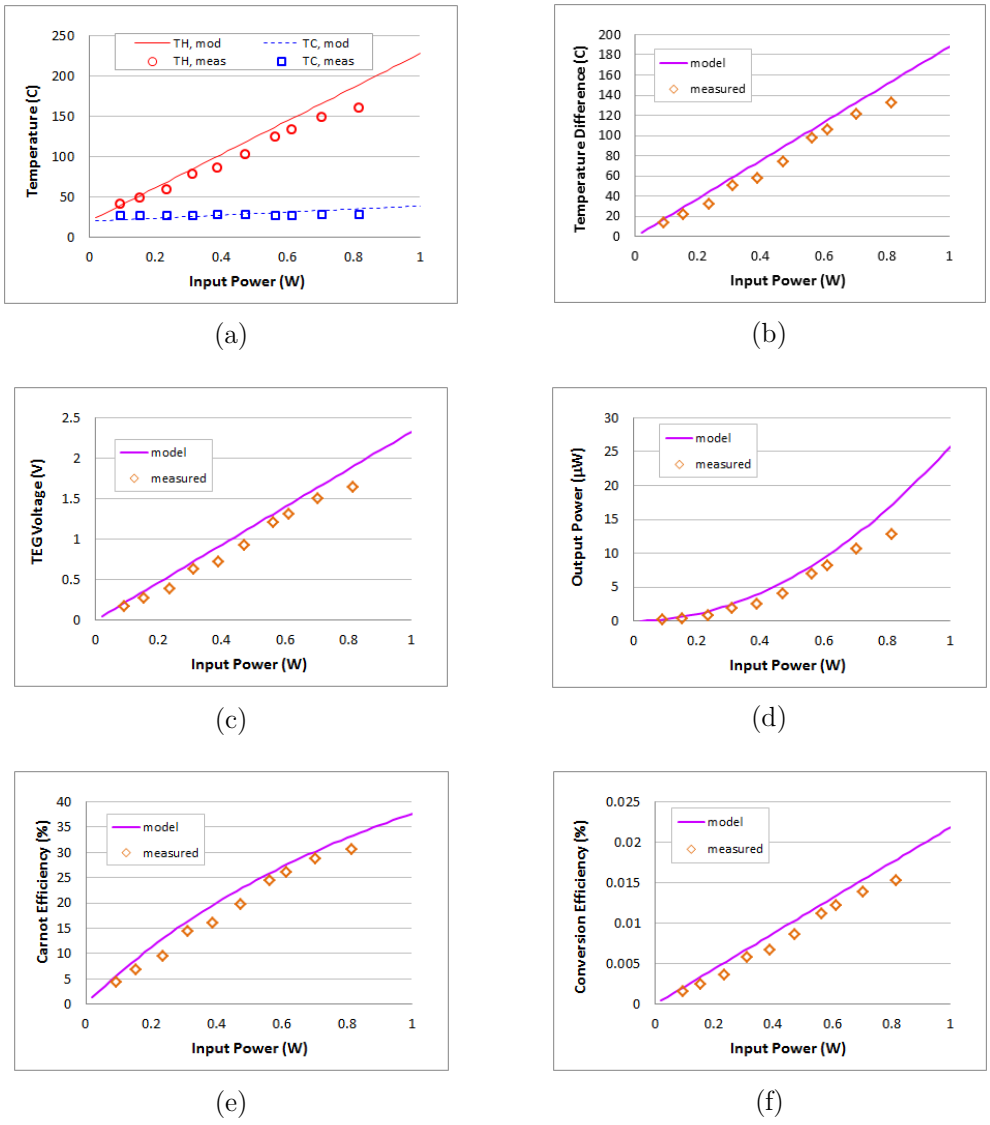


Figure H-1: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a SOI substrate with $l = 200$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 31$.

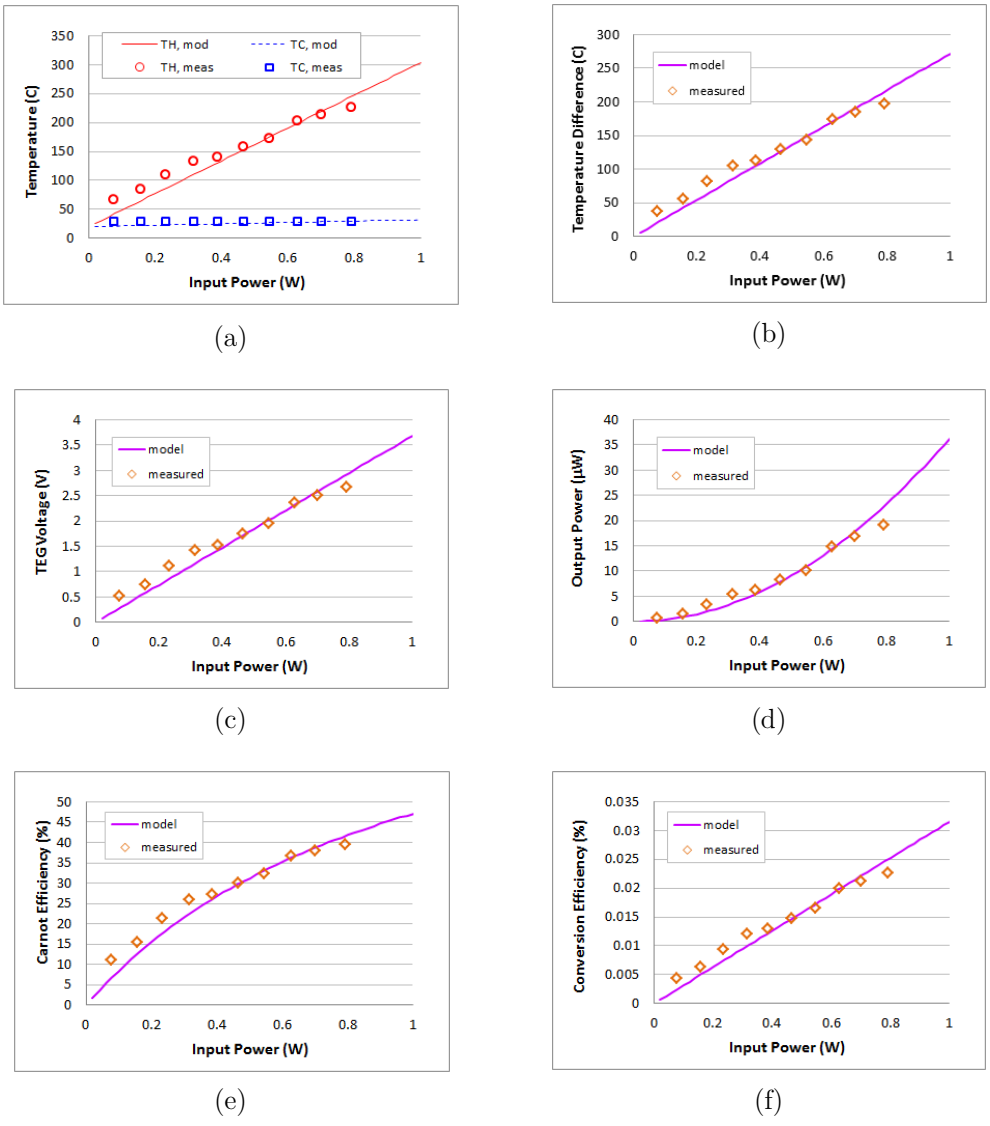


Figure H-2: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a SOI substrate with $l = 500$ µm, $w = 15$ µm, $d_{mem} = 1$ mm, and $N = 34$.

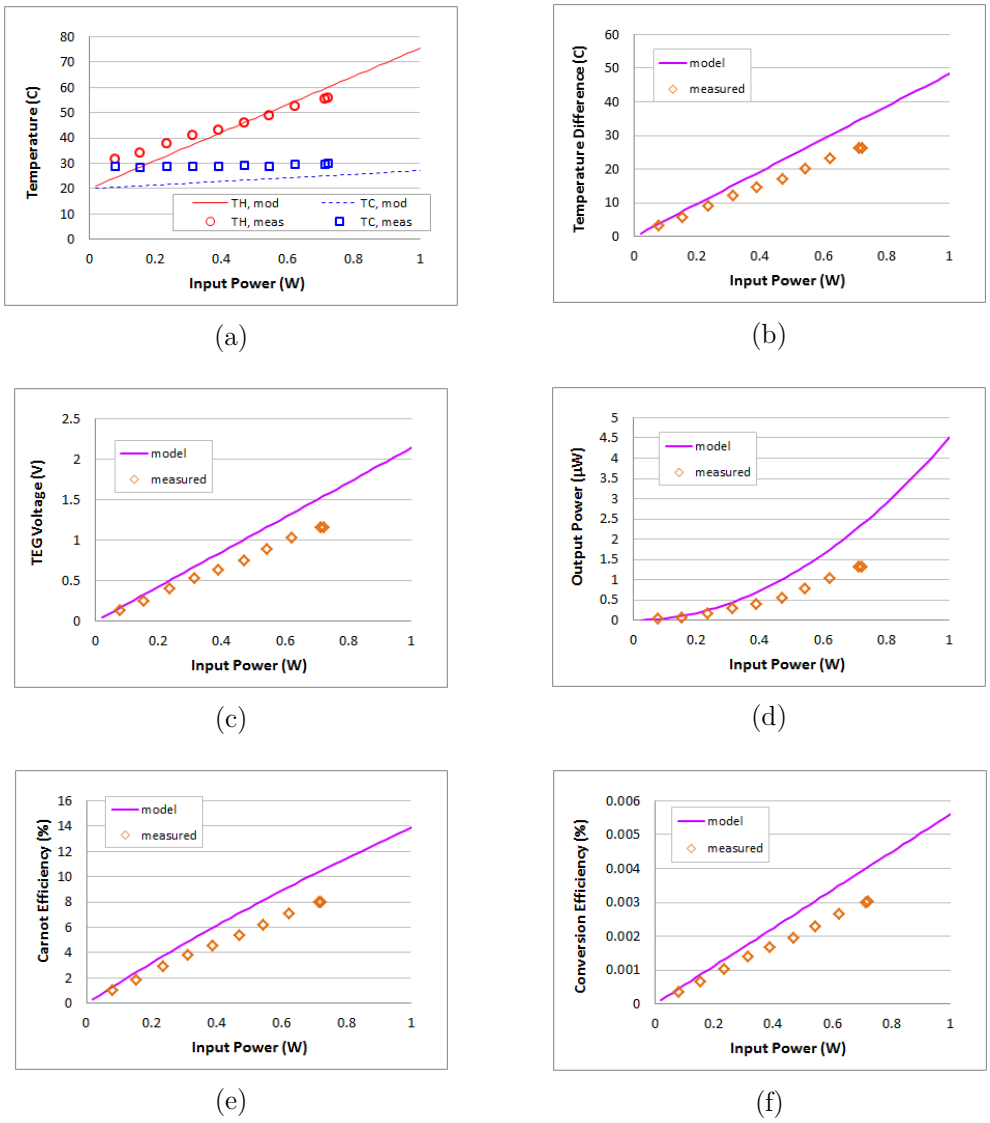


Figure H-3: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a SOI substrate with $l = 500$ μm, $w = 15$ μm, $d_{mem} = 3$ mm, and $N = 111$.

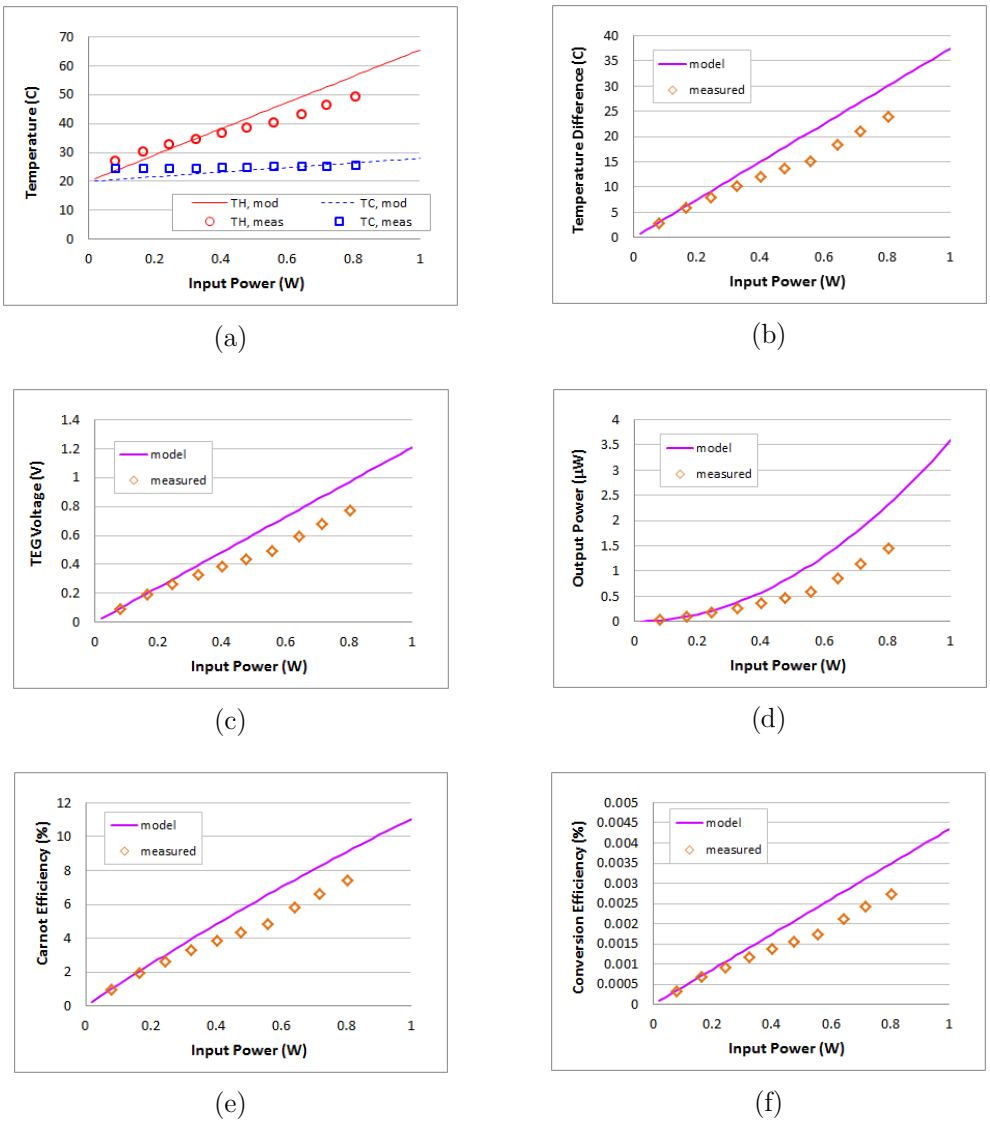


Figure H-4: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a SOI substrate with $l = 500$ µm, $w = 30$ µm, $d_{mem} = 3$ mm, and $N = 81$.

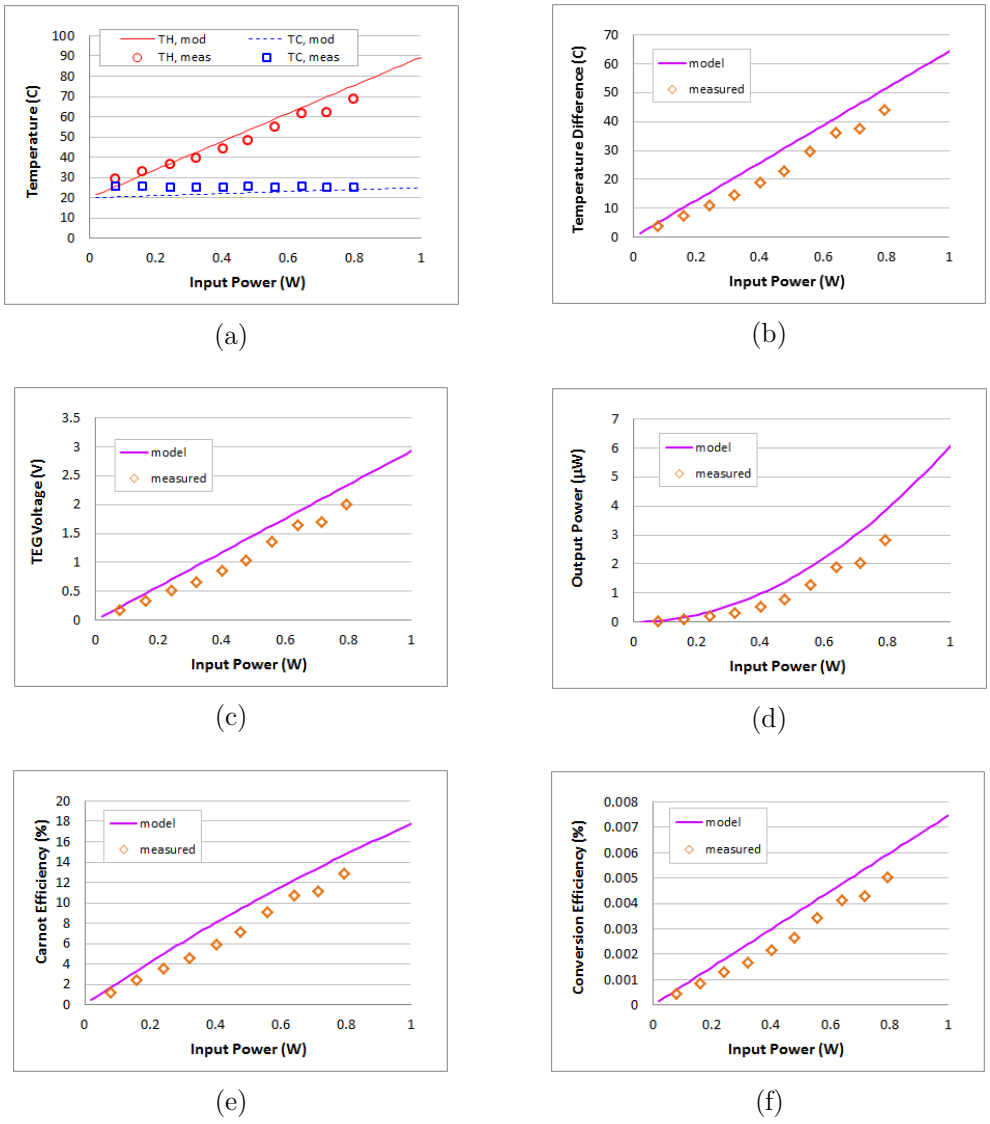


Figure H-5: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a SOI substrate with $l = 1000$ µm, $w = 15$ µm, $d_{mem} = 3$ mm, and $N = 114$.

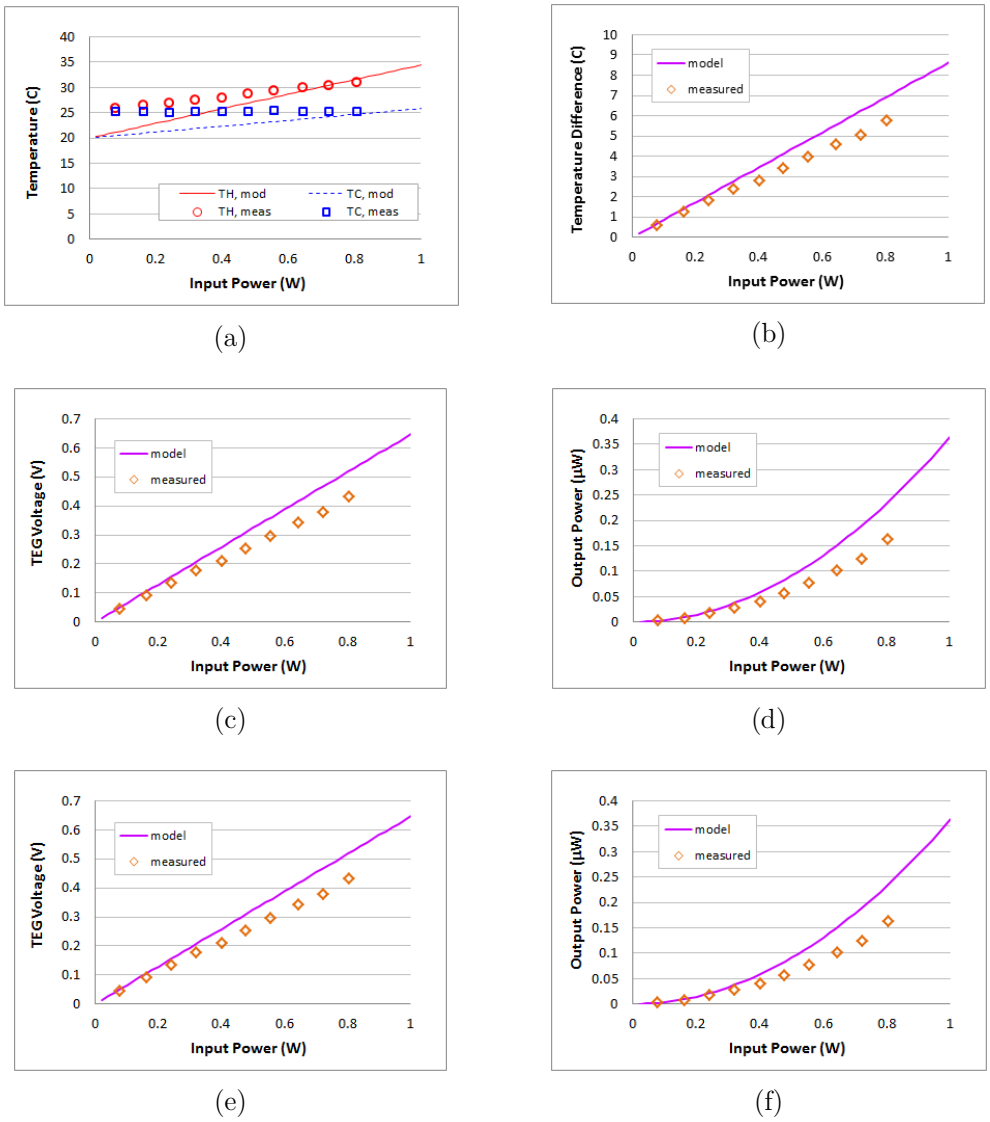


Figure H-6: Comparison between thermal model and measured parameters: (a) hot and cold side temperature, (b) temperature difference, (c) open-circuit TEG voltage, (d) output power under matched load conditions, (e) Carnot efficiency, and (f) conversion efficiency for a TEG implemented on a SOI substrate with $l = 200$ µm, $w = 15$ µm, $d_{mem} = 5$ mm, and $N = 188$.

Appendix I: Solar Simulator Measurements (TEG on Glass)

Table I-4: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a glass substrate using the LA1074 lens. Data is taken from the average of five measurements.

l (µm)	w (µm)	d_{mem} (mm)	N	V_{TEG} (mV)	R_{TEG} (kΩ)	ΔT (°C)	P_{OUT} (nW)
200	15	1	31	0.16	19.68	0.045	$3.3\text{x}10^{-4}$
500	15	1	34	0.32	43.61	0.081	$5.7\text{x}10^{-4}$
200	15	3	108	0.14	67.04	0.011	$7.4\text{x}10^{-5}$
500	15	3	111	0.58	161.25	0.046	$5.3\text{x}10^{-4}$
500	20	3	91	0.47	97.82	0.045	$5.6\text{x}10^{-4}$
500	30	3	81	0.21	54.49	0.023	$2.1\text{x}10^{-4}$
1000	15	3	114	2.04	260.35	0.156	$4.0\text{x}10^{-3}$
200	15	5	188	0.91	124.71	0.042	$1.7\text{x}10^{-3}$
500	15	5	188	3.12	220.26	0.144	0.011
1000	15	5	191	6.26	442.43	0.28	0.022

Table I-5: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a glass substrate using the LA1102 lens. Data is taken from the average of five measurements.

l (µm)	w (µm)	d_{mem} (mm)	N	V_{TEG} (mV)	R_{TEG} (kΩ)	ΔT (°C)	P_{OUT} (nW)
200	15	1	31	4.67	19.68	1.31	0.28
500	15	1	34	17.40	43.61	4.46	1.75
200	15	3	108	19.17	66.39	1.55	1.38
500	15	3	111	43.98	159.11	3.45	3.04
500	20	3	91	36.32	96.47	3.48	3.42
500	30	3	81	32.00	54.17	3.44	4.73
1000	15	3	114	86.25	259.11	6.59	7.18
200	15	5	188	13.45	123.60	0.62	0.37
500	15	5	188	32.02	219.90	1.48	1.16
1000	15	5	191	64.94	440.33	2.96	2.40

Table I-6: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a glass substrate using the LA1050 lens. Data is taken from the average of five measurements.

l (µm)	w (µm)	d_{mem} (mm)	N	V_{TEG} (mV)	R_{TEG} (kΩ)	ΔT ($^\circ$C)	P_{OUT} (nW)
200	15	1	31	---	---	---	---
500	15	1	34	---	---	---	---
200	15	3	108	16.12	64.41	1.30	1.01
500	15	3	111	47.31	155.35	3.71	3.60
500	20	3	91	43.96	92.50	4.21	5.22
500	30	3	81	33.35	52.47	3.61	5.36
1000	15	3	114	92.11	255.04	7.04	8.31
200	15	5	188	23.61	118.81	1.09	1.17
500	15	5	188	65.40	218.51	3.03	4.89
1000	15	5	191	124.27	437.03	5.67	8.83

Appendix J: Solar Simulator Measurements (TEG on SOI)

Table J-7: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a SOI substrate using the LA1074 lens. Data is taken from the average of five measurements.

l (µm)	w (µm)	d_{mem} (mm)	N	V_{TEG} (mV)	R_{TEG} (kΩ)	ΔT (°C)	P_{OUT} (nW)
200	15	1	31	0.95	53	0.077	$4.3x10^{-3}$
500	15	1	34	13.8	94.6	1.01	0.5
500	15	3	111	20.9	255.1	0.47	0.43
500	30	3	81	19.3	102.7	0.6	0.9
1000	15	3	114	30.5	355.2	0.67	0.65
200	15	5	188	8.3	287.3	0.11	0.06

Table J-8: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a SOI substrate using the LA1102 lens. Data is taken from the average of five measurements.

l (µm)	w (µm)	d_{mem} (mm)	N	V_{TEG} (mV)	R_{TEG} (kΩ)	ΔT (°C)	P_{OUT} (nW)
200	15	1	31	26.7	53.7	2.16	3.32
500	15	1	34	232.7	96.1	17.2	140.9
500	15	3	111	437.1	255.4	9.9	187
500	30	3	81	372.4	104.5	11.5	331.8
1000	15	3	114	546.1	360.1	12	207
200	15	5	188	99.1	288.7	1.32	8.5

Table J-9: Open-circuit voltage, series resistance, temperature difference, and matched output power of TEGs implemented on a SOI substrate using the LA1050 lens. Data is taken from the average of five measurements.

l (µm)	w (µm)	d_{mem} (mm)	N	V_{TEG} (mV)	R_{TEG} (kΩ)	ΔT (°C)	P_{OUT} (nW)
200	15	1	31	---	---	---	---
500	15	1	34	---	---	---	---
500	15	3	111	581.2	257.1	13.1	328.4
500	30	3	81	451.6	109.6	14	465.1
1000	15	3	114	803.2	374.3	17.7	430.9
200	15	5	188	217	295.2	2.9	39.9

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