Can Clock Faults Be Detected Through Functional Test ?*

C. Metra D. Rossi M. Omaña J.M. Cazeaux TM Mak

DEIS, University of Bologna
Viale Risorgimento 2, 40136 Bologna, Italy
{cmetra, drossi, momana, jmcazeaux}@deis.unibo.it

Intel Corporation
Santa Clara (CA)
t.m.mak@intel.com

***Abstract*-We analyze the probability to detect clock faults indirectly through conventional functional testing by considering realistic datapaths derived from ISCAS'85 benchmarks. We show that, even optimistically assuming that we are able to test all short and long paths for min and max delay violations, the detection of clock faults can not be guaranteed, thus mandating new, specific testing approaches for clock faults, otherwise possibly compromising the system correct operation in the field, with dramatic consequences on product quality and defect level.**

I. INTRODUCTION

Clock is one of the most critical signal in any synchronous system. It has to be buffered and distributed throughout the whole chip. This leads to the need of sophisticated routing, balancing, buffering, deskewing and calibration strategies [1-12].

In [13] we have shown that clock faults are likely. They can cause duty-cycle variations that may be neither detected through conventional structural testing, nor compensated by the existing calibration and correction schemes [13, 14].

We can expect that their effect on the operation of a system may be catastrophic (i.e., the system will crash), thus easily detectable. In [15] we have recently shown (considering very simple data paths) that this may be not the case. In fact, the system may not crash, but no longer satisfy its timing constraints. For instance, clock faults can make a perfectly designed (and compensated) data-path violate its min delay or max delay timing constraints.

This opens new needs and problems from the testing point of view. While max delay problems can be detected through functional testing, this is not necessarily the case for min delay problems. Traditionally, testing has been focused on max delay faults only, assuming that min delay problems are designed out with appropriate design and validation methodologies, and there is little consideration of min time problems due to manufacturing faults. As discussed in [15] and proven here with reference to more realistic datapaths, min delay problems can indeed also take place because of faults, as a result of bridging defects with clock signals.

While max delay can be tolerated by binning the device to a lower frequency rating, min time cannot be tolerated as it will come in at any frequency. Speed binning is no longer a solution. Moreover, because of the setup/hold time characteristic of latches and flops, min time is usually a problem for cold temperature and high V_{dd}, which is the opposite of the test condition for max delay testing.

Based on these considerations and on the preliminary results found in [15] by analyzing very simple datapaths, in this paper we analyze more realistic datapaths, derived from the ISCAS'85 benchmark circuits, and we derive the probability that clock duty-cycle variations can give rise to min and max delay violations. We will show that clock faults, which we have in turn proven likely [13], can indeed give rise to min delay problems. We will then evaluate the probability that clock faults can be detected indirectly through functional testing. We will show that even for functional testing, the detection of clock faults can not be guaranteed.

Consequently, new testing approaches for clock faults are needed.

The remainder of this paper is organized as follows. In Section 2, we give some preliminaries on clock faults causing duty-cycle variations. In Section 3, we present the results of the timing analyses that we have performed in order to evaluate the probability to have min or max delay problems due to clock faults. In Section 4, we discuss the probability that clock faults can be detected indirectly by standard functional testing. In Section 5, we provide some comments about the need to test for clock faults, and finally, in Section 6, we give some conclusive remarks.

II. CLOCK FAULTS PRELIMINARIES

As proven in [13], due to the vast routing (up and down the metal layers between buffering) and shielding of clocks (with V_{dd}/V_{ss}), faults involving a clock signal (CK) are very likely. Particularly, this is the case of bridging faults (BFs) involving a clock net and V_{dd} or V_{ss}. We performed inductive fault analyses with the Intel® Eiffel tool on the Itanium® microprocessor and we found that the BFs between a clock net and V_{dd}/V_{ss} are 2 orders of magnitude more likely than any other bridging in the microprocessor (primarily due to the design practice of routing V_{dd}/V_{ss} next to the clock as partial

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shielding of the clock), other than the BFs between V_{dd} and V_{ss} ! While different BFs will likely result in stuck ats, we have verified that BFs involving clock nets and V_{dd}/V_{ss} will result in a skewed clock waveform (faster on one edge and slower on the other), giving rise to clock incorrect duty cycle [13]. As an example, considering the case of a bridging fault between the CK net and V_{dd}, this will speed up the CK rising phase, while slowing down the falling one, thus widening the CK high phase, compared to the fault free case. This case is illustrated in Fig. 1 [13] where, as an example, we considered a BF between a clock node outside a regional grid and V_{dd}. The figure shows the voltage at the output of a leaf of a regional clock grid [3]. Analogously, if a BF between the clock and V_{ss} were considered, we would have a shorting of the clock high phase. Furthermore, in [14] we have shown that similar consequences can also arise because of BFs involving internal nodes of a deskew buffer. In particular, we have verified that duty-cycle variations can overcome the 50% of the correct clock duty-cycle [16].

Recently, by considering the simple case of datapaths consisting of a few cascaded inverters, we have shown that one of the most dangerous consequences of a clock duty-cycle variation can be the violation of the path min delay constraints [15].

In the next section, by considering more realistic datapaths, we prove that this can likely occur and we evaluate in details its probability, along with the probability of max delay violations due to a CK fault.

III. Min and Max Delay Violations due to Clock Faults

We consider data paths with the generic structure shown in Fig. 2. L_1 and L_2 denote two (level-sensitive) latches that are transparent during the clock high phase. CK (CK_1 and CK_2) denote a clock signal, with 50% duty-cycle, while D_1 and D_2 (Q_1 and Q_2) are the latch inputs (outputs). Finally, C denotes the combinational block of the considered path.

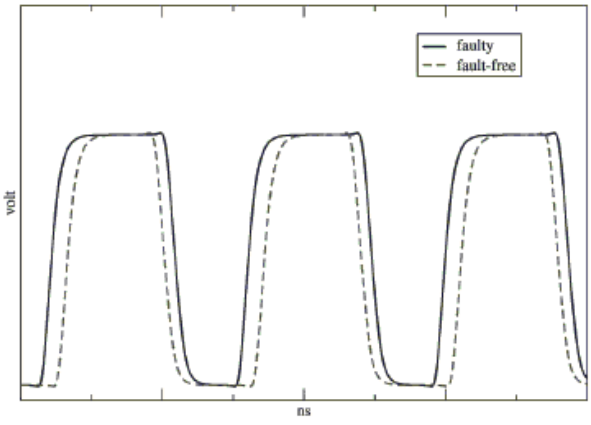

Fig. 1 Clock voltage in the fault-free case and in the case of a 50Ω bridging fault toward V_{dd}.

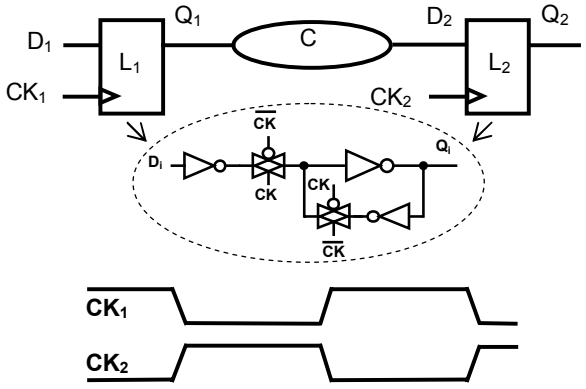

Fig. 2 Paths considered for the performed analyses.

As for such combinational blocks, we have considered circuits belonging to the benchmark set ISCAS'85. They have been synthesized by means of the *Synopsis Design Compiler*, adopting a standard 0.25μm CMOS technology, with V_{dd} = 1.8V. All benchmarks have been optimized for performance, and their timing behavior has been analyzed by employing the *Synopsis Design Compiler Timing Analyzer*.

Table I resumes the timing characteristics of such benchmarks. The second column reports the total number of paths of each benchmark that can be activated by the input vectors; the third and fourth columns show the propagation delay of the shortest and longest path, respectively; finally, the last column shows the simulation frequency (f_{max}) for each benchmark. This has been tailored to the propagation delay of the longest path, with no time slack.

As for the considered CK faults, they can be located at different levels of the clock distribution hierarchy. In particular, we can distinguish between faults involving clock nets at the local level, that is faults affecting only one clock between CK_1 and CK_2, and faults involving clock nets at the global level, that is faults making all local clocks have the same duty-cycle error. We can notice that, in this latter case, the local clocks derived by the same global clock net are not overlapped.

TABLE I

ISCAS'85 Benchmarks' Characteristics

ISCAS Bench.	N_{tot} of Paths	Shortest Path Delay	Longest Path Delay	f_{max} (MHz)
C17	18	0.44ns	2ns	250
C880	14818	0.14ns	2.5ns	200
C2670	23224	0.001ns	3ns	167
C432	39536	0.34ns	3ns	167
C499	332738	0.11ns	2ns	250
C1355	545396	0.16ns	3.1ns	161
C1908	637868	0.11ns	3.7ns	135
C3540	605602	0.14ns	4.5ns	111
C5315	133028	0.001ns	3.4ns	147
C7552	169178	0.001ns	2.6ns	192

In this paper we consider CK faults at the local level (i.e., we consider either CK_1 or CK_2 as faulty), with the clock faults either widening or shortening the high phase of the correct duty cycle (DC_{Cor} in Fig. 3 (a) and (b), respectively). We denote by Δ_{DC} (Fig. 3) the relative variation of the clock duty-cycle with respect to the correct one. It can be expressed by:

$$\Delta_{DC}\% = [(DC_{Faulty}/DC_{Cor}) - 1] * 100.$$

Table II reports the number of paths presenting a min delay violation for duty-cycle variations up to the 50%, possibly due to CK faults [16]. Of course, this value depends critically on the particular benchmark but, as expected, the number of paths violating the min delay constraint increases with the increase of the clock duty-cycle variation. This trend is shown in Fig. 4, where the percentage of paths presenting a min delay violation is plotted as a function of the duty-cycle variation.

In Table III and Fig. 5 we show the analogous results that we have obtained for max delay violations. They are qualitatively similar to those obtained for min delay. However, there is a quantitative difference in the number of paths violating the max delay constraint for each value of duty-cycle variation, due to the higher number of critical timing paths of the optimized for performance benchmarks.

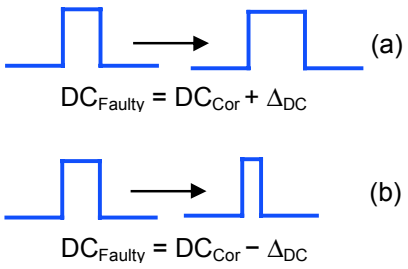

Fig. 3 Possible CK fault effect on duty cycle: clock high phase widened (a), and clock high phase shortened (b).

TABLE II

NUMBER OF PATHS OF ISCAS'85 BENCHMARKS WHICH PRESENT A MIN DELAY VIOLATION AS A FUNCTION OF THE DUTY CYCLE VARIATION

ISCAS Bench.	Duty-cycle variation				
	10%	20%	30%	40%	50%
C17	0	0	4	6	8
C880	44	119	296	563	889
C2670	209	372	673	1254	2322
C432	0	16	119	277	790
C499	133	133	133	133	6654
C1355	54	109	109	109	545
C1908	64	128	256	1914	4465
C3540	0	182	424	1211	5450
C5315	93	266	931	2660	6651
C7552	101	169	507	1692	5075

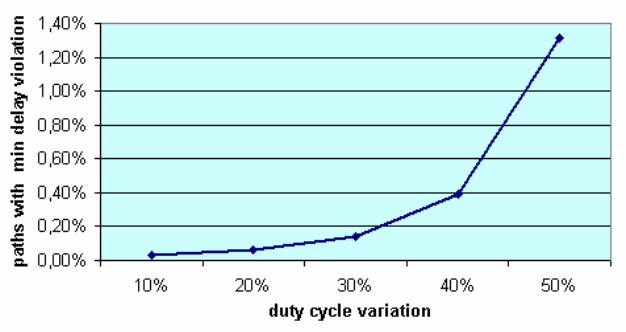

Fig. 4 Percentage of paths presenting a min delay violation as a function of the duty-cycle variation.

It is worth noticing that, if we had considered edge sensitive flip-flops, instead of level sensitive latches, there would have been no min delay problem, as proven in [15]. As for max delay problems, instead, their occurrence depends on the employed clocking scheme. If the datapaths are clocked by a single clock, no max delay problem can occur [15], while we have verified that this can be the case if the same clocking scheme as that shown in Fig. 2 is adopted.

TABLE III

NUMBER OF PATHS OF ISCAS'85 BENCHMARKS WHICH PRESENT A MAX DELAY VIOLATION AS A FUNCTION OF THE DUTY CYCLE VARIATION

ISCAS Bench.	Duty-cycle variation				
	10%	20%	30%	40%	50%
C17	2	4	8	8	10
C880	3704	8891	12003	13336	13929
C2670	1626	8825	15328	19508	20902
C432	13047	27280	33606	37164	38745
C499	89839	219607	272845	316101	326083
C1355	141803	409047	512672	544305	544850
C1908	229632	484780	554945	612353	633403
C3540	242240	381529	496594	575322	600151
C5315	25275	77156	107753	119725	126377
C7552	28760	91356	135342	157335	164103

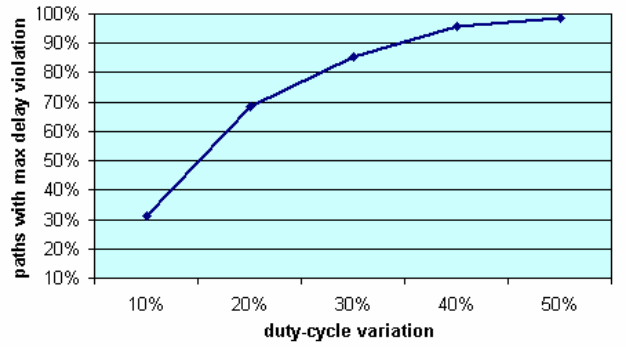

Fig. 5 Percentage of paths presenting a max delay violation as a function of the duty-cycle variation.

IV. Probability of Clock Fault Detection by Functional Testing

Let us evaluate the probability to detect clock faults indirectly by functional testing, considering the same realistic data paths as in the previous section.

It can be easily verified [15] that short paths can give rise to min delay violations when the clock high phase is widened (due to faults), while long paths may present max delay violations when the clock high phase is shortened (due to faults).

Let us evaluate the probability that clock faults (possibly causing min or max delay violations, as analyzed in the previous section) can be detected through conventional functional test.

In order to ease our evaluation, and to obtain results not critically dependent on the particular performed functional test, we have made the following hypotheses: i) a fault involving a clock net either at a local or global level is present; ii) we can conveniently test short paths for min delay; iii) we (optimistically) test all short paths (for min delay) and all long paths (for max delay).

The probability to detect a CK fault by testing all short paths is given by:

$$P_{det\text{-}sp} = P_{wid} \times P_{fck\text{-}sp} \times P_{tst\text{-}sp}. \quad (1)$$

The first factor (P_{wid}) is the probability that the CK fault results in a widening of the clock high phase; the second factor ($P_{fck\text{-}sp}$) represents the probability that a CK fault affecting a short path gives rise to a min delay problem; the latter factor accounts for the probability that the affected short path is tested.

Analogously, the probability to detect a CK fault by testing all long paths can be written as:

$$P_{det\text{-}lp} = P_{sht} \times P_{fck\text{-}lp} \times P_{tst\text{-}lp}, \quad (2)$$

where P_{sht} is the probability to have a shortening of the clock high phase, as a consequence of a CK fault; $P_{fck\text{-}lp}$ represents the probability that a CK fault affecting a long path gives rise to a max delay problem; $P_{tst\text{-}lp}$ is the probability that the affected long path is tested. It is worth reminding that the widening of the clock high phase can impact only short paths (possibly causing a min delay violation), while dual comments hold true for the case of the shortening of the clock high phase [15].

As for the first factors in the previous equations, since we can reasonably assume that BFs between the affected clock net and V_{dd} or V_{ss} are equally likely, we can consider $P_{sht} = P_{wid} = 0.5$.

The second factors ($P_{fck\text{-}lp}$ and $P_{fck\text{-}sp}$) depend on whether the fault affects a local or a global clock. If the CK fault is at the global level, it is: $P_{fck\text{-}lp} = 1$, if Δ_{DC} is high enough to give rise to max delay violations for at least one circuit path; $P_{fck\text{-}lp} = 0$, if Δ_{DC} is tolerable. Analogously, since the local clocks do not overlap, and consequently no min delay violation can occur, it is $P_{fck\text{-}sp} = 0$. If the CK fault is at local level, it is $P_{fck\text{-}lp}$ ($P_{fck\text{-}sp}$) = $\#CK_{dr} / \#CK_t$, where $\#CK_{dr}$ is the number of local clocks driving a latch at the end of a short (long) path that give rise to a min (max) delay violation, while $\#CK_t$ is total number of local clocks driving output latches.

According to hypotheses ii) and iii) introduced above, $P_{tst\text{-}sp}$ and $P_{tst\text{-}lp}$ are assumed equal to 1. Therefore, depending on the value of $P_{fck\text{-}sp}$ ($P_{fck\text{-}lp}$), $P_{det\text{-}sp}$ ($P_{det\text{-}lp}$) can reach a maximum value of 0.5.

Table IV reports the values of $P_{det\text{-}sp}$, that is the probability to detect a CK fault by testing all short paths, as a function of the duty-cycle variation. As expected, $P_{det\text{-}sp}$ increases for high values of Δ_{DC}% and, for several benchmarks, it reaches, or approximates, the 50%.

Analogously, in Table V we report the value of $P_{det\text{-}lp}$, that is the probability to detect a CK fault while testing all long paths. Comments similar to those for the previous case hold true.

In Fig. 6 we resume the achieved results. In particular, we draw the probability to detect CK faults indirectly, while (optimistically) testing all short and long paths for min and max delay violations, respectively, by functional test.

TABLE IV

PROBABILITY OF CK FAULT DETECTION WHEN TESTING SHORT PATHS, AS A FUNCTION OF CLOCK DUTY-CYCLE VARIATION

ISCAS Bench.	Duty-cycle variation				
	10%	20%	30%	40%	50%
C17	0%	0%	25%	25%	25%
C880	21%	42%	50%	50%	50%
C2670	34%	47%	49%	49%	49%
C432	0%	14%	50%	50%	50%
C499	50%	50%	50%	50%	50%
C1355	50%	50%	50%	50%	50%
C1908	32%	48%	48%	48%	48%
C3540	2%	14%	22%	22%	22%
C5315	16%	39%	50%	50%	50%
C7552	24%	30%	40%	43%	43%

TABLE V

PROBABILITY OF CK FAULT DETECTION WHEN TESTING LONG PATHS, AS A FUNCTION OF CLOCK DUTY-CYCLE VARIATION

ISCAS Bench.	Duty-cycle variation				
	10%	20%	30%	40%	50%
C17	25%	25%	50%	50%	50%
C880	17%	17%	17%	17%	17%
C2670	3.6%	3.6%	3.6%	5%	5%
C432	29%	29%	36%	50%	50%
C499	50%	50%	50%	50%	50%
C1355	50%	50%	50%	50%	50%
C1908	18%	20%	48%	50%	50%
C3540	10%	24%	26%	32%	32%
C5315	21%	26%	28%	30%	30%
C7552	20%	22%	23%	23%	23%

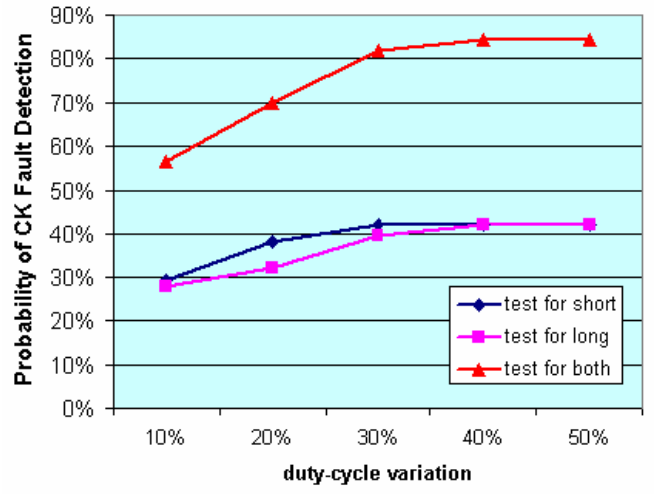

Fig. 6 CK faults detection probability by testing for min and max delay violations through functional test.

The probabilities have been averaged on all paths, and are given by:

$$P^{av}_{\det-sp}(\Delta DC) = \sum_{i=1}^{10} \frac{N_{i-sp}(\Delta DC)}{N_{tot}},$$

$$P^{av}_{\det-lp}(\Delta DC) = \sum_{i=1}^{10} \frac{N_{i-lp}(\Delta DC)}{N_{tot}}, \qquad (3)$$

$$P^{av}_{\det-tot} = P^{av}_{\det-sp} + P^{av}_{\det-lp}.$$

From the graphs in Fig. 6 we can derive that, even (optimistically) assuming that all short and long paths are tested while performing functional testing, we can not guarantee the indirect detection of CK faults by conventional functional testing.

To face this problem, new testing paradigms for clock faults should be devised.

V. Discussion

Even though we have presented the argument here that we cannot guarantee the detection of clock faults with structural and functional tests, we know that there is always the question that some of you have: "Does clock fault matters?". Anyway, if a device is functional, does it matter that there is a fault with the clock network. The problem is that we usually do not fully test a device with all the functional patterns at all the conditions. These clock defects, while they do not manifest as a functional failure during manufacturing test phase (with limited functional tests), may eventually fail at the end use environment and become a field failure.

As for possible approaches to test for clock faults, new testing (or DFT) solutions could be developed (applied). Clock faults can be targeted either directly (e.g., by proper current testing of the BFs involving clock lines), or indirectly, by testing for min delay that we have proven being an indirect effect of clock faults. For instance, self-checking detectors for clock faults (e.g., of the kind in [13, 17]) could be employed. They allow clock faults' testing both at the end of fabrication and in the field, by checking the correctness of the clock waveforms at the outputs of clock buffers. It should be noted that, especially if employed at local level, they may imply a non negligible cost.

Alternatively, lower cost self-correcting clock buffers (e. g., of the kind in [18, 19]) could be employed, both at the global and local level. They are able to keep on self-correcting their generated output clock waveforms, thus compensating possible faults affecting clock nets, as well as the buffers themselves.

VI. Conclusions

By considering realistic data-paths derived from the ISCAS'85 benchmarks, we have shown that min delay (as well as max delay) problems can occur after manufacturing because of faults affecting clock signals. We have evaluated the probability to detect such clock faults indirectly by functional testing. We have shown that, even optimistically assuming that all short and long paths are tested, we can not guarantee the detection of such clock faults, thus mandating the development of new testing approaches.

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