# A Novel Dual-Walled CNT Bus Architecture with Reduced Cross-Coupling Features

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***Abstract*— Carbon Nano Tubes (CNTs) have been widely proposed as interconnect fabric for nano and very deep sub-micron (silicon-based) technologies due to their robustness to electromigration. In this paper, a novel bus architecture with low crosstalk features is proposed. It is made of dual-walled nanotubes (DWNTs) arranged in parallel. It achieves reductions up to 72% of the crosstalk-induced delay, and up to 76% for the crosstalk-induced peak voltage, at a modest area increase. Therefore, the proposed bus arrangement significantly improves performance and provides reliable operation in an interconnect.**

## I. Introduction

Global interconnects (such as the so-called bus) are widely employed to distribute data, clock, power supply and ground throughout the entire area of an integrated circuit (IC). At high current density, most materials used in today's interconnects (such as Al and Cu) [22] are affected by electromigration, thus substantially impacting reliability (as measured by the correct operation of the IC). Additionally, crosstalk coupling may cause signal delays, speed-ups and glitches (usually referred to as crosstalk noise) [18]. The delay due to crosstalk negatively impacts performance, while crosstalk noise constitutes a serious problem for reliable operation of an interconnect [12]. Crosstalk can result in a glitch that depending on duration and amplitude, may be propagated to the output of a bus receiver, thus causing a logic error at the output of the sampling (receiving) device. Correct operation may be affected. As for crosstalk coupling, line delay depends on the switching activity of adjacent lines, resulting in a crosstalk-induced delay uncertainty, that also may negatively impact reliability [12].

Carbon Nano Tubes (CNTs) offer unique capabilities due to their conductive, mechanical and thermal properties [22]. For example, CNTs have been proposed for providing signals for clocking Quantum-dot Cellular Automata (QCA) circuits [10]. These devices can be classified as single-walled (SWNTs) and multi-walled nanotubes (MWNTs). A SWNT consists of a single sheet of graphene rolled up into a cylindrical tube, that can have a diameter in the nanometer range and a length in the micrometer range [2]. A MWNT consists of two or more SWNTs, that are concentrically wrapped one over the other [2]. Depending on the direction in which they are rolled (referred to as chirality), CNTs can behave either as a semiconductor, or a conductor [19]. Conductive (or metallic) nanotubes are envisioned as ideal interconnect devices for emerging technologies at nano scale as well as for today's very deep sub-micron (silicon-based) electronics [17], [13], [11], [16], [8], [14].

Despite their potential, only recently research has been reported on nanotube based interconnects [17], [13], [15], [20], [21], [16], [6], [14], [5], [4]. The problem of possible crosstalk coupling between bus lines has been analyzed only in [7], in which existing models (based on equivalent RLC circuits) of CNT interconnects have been changed to account for the geometry of different bus architectures.

In this paper, initially the crosstalk effects of a "standard" SWNTs based bus architecture [20], [7] are evaluated. Then, a bus architecture made of parallel dual-walled nanotubes (DWNTs) is proposed; a DWNT consists of a MWNT made of two shells. Two arrangements in the CNTs are analyzed. We have compared the proposed architecture with the considered parallel SWNTs bus and verified that crosstalk-induced delay, delay uncertainty and crosstalk-induced peak voltage are significantly reduced (72% for crosstalk-induced delay, and 76% for crosstalk-induced peak voltage compared to the SWNT based bus).

This paper is organized as follows. In Sect. II, the crosstalk effects of a SWNTs based bus architecture are evaluated. In Sect. III, the proposed bus architecture is proposed. In Sect. IV, this bus architecture is compared with the SWNTs bus. Final remarks are given in Sect. V.

## II. Parallel SWNT Bus Architecture

The evaluation of crosstalk effects in terms of both crosstalk-induced delay and peak voltage is reported for a bus architecture made of three parallel SWNTs. Simulation has been performed using HSPICE by considering a bus frequency of $800MHz$, a spacing between bus lines of $2nm$, a line length of $10\mu m$, and a diameter of $1nm$. The latter value represents the smallest SWNT diameter allowed by current nanotechnology [1].

Fig. 1 shows the eye diagram obtained by simulation. As for the crosstalk-induced delay in the worst and best cases ($\tau_{dw}$ and $\tau_{db}$) and the delay uncertainty ($\Delta\tau_d$), the following values have been obtained: $\tau_{dw} = 131.3ps$, $\tau_{db} = 9.5ps$ and $\Delta\tau_d = 121.8ps$. $\Delta\tau_d$ is approximately 92% of $\tau_{dw}$, that indicates a large uncertainty in the signal propagation delay through the

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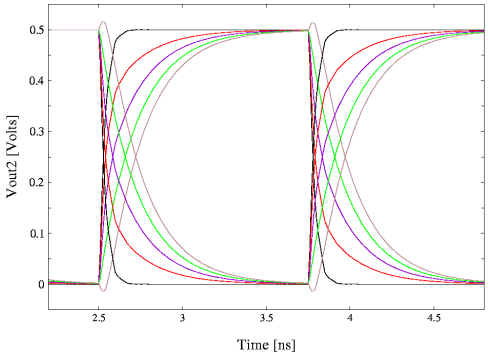


Fig. 1. Eye diagram for a 3-line bus architecture made of parallel SWNTs.

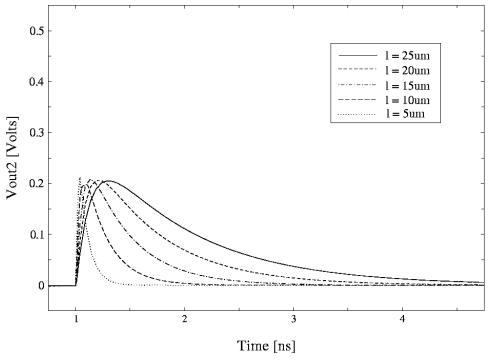


Fig. 2. Crosstalk-induced peak voltage for a 3-line bus architecture made of parallel SWNTs.

simulated bus architecture (with negative impact on reliable operation [12]).

Fig. 2 shows the peak voltage induced on the victim line (that is supposed to be steady at 0) by the simultaneous switching of the aggressors in the same direction ($0 \rightarrow 1$ in this case), for several values of line length. By increasing the line length, initially the peak amplitude and duration increase too. For higher values of length, the glitch amplitude saturates at a level slightly above 0.2V, while the duration continues to increase. Therefore, for the case of symmetric receivers, and sampling elements with a threshold voltage $\simeq V_{dd}/2 = 0.25V$, the induced peak voltage will never reach the threshold voltage of the receivers. By considering also the receiver filtering ability, the glitch at the output will never reach the logic threshold of the input gates of the sampling elements. Consequently, the induced peak voltages will not produce a logic error at the output of the receiver sampling elements.

## III. Proposed Parallel DWNT Bus Architecture

A new bus architecture that reduces crosstalk effects is proposed (Fig. 3). The proposed architecture consists of $N$ parallel dual-walled nanotubes (DWNTs), each nanotube carries one bus signal. As DWNTs are MWNTs with two shells, it is assumed that the inner nanotube carries the bus signal ($Vin_i$), while the outer nanotube is connected to a shielding signal ($Vis_i$) for crosstalk reduction. Two possible arrangements are

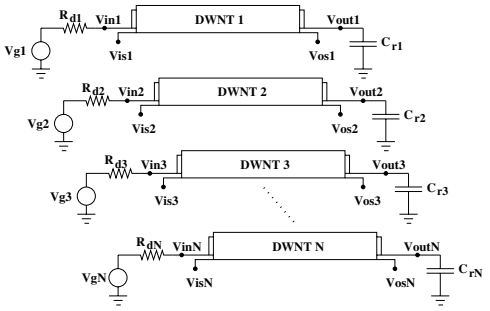


Fig. 3. Proposed DWNT bus architecture.

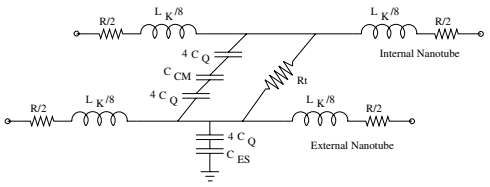


Fig. 4. Equivalent RLC circuit of the MWNT geometry of Fig. 3.

proposed; they differ in the shielding signal (allowing different levels of crosstalk reduction), but at the expense of bus power consumption and implementation difficulty.

The RLC equivalent circuit of each DWNT is shown in Fig. 4. Individual shells are modeled as concentric coupled nanotransmission lines, each with a distributed resistance and kinetic inductance ($L_k/4$). The outermost nanotube presents a distributed coupling electrostatic ($C_{ES}$) and quantum capacitance ($4C_Q$) versus the ground plane, as well as a distributed coupling electrostatic ($C_{CM}$) and quantum capacitance ($4C_Q$) versus the internal shell. Furthermore, the internal shell presents only a distributed coupling electrostatic ($C_{CM}$) and quantum capacitance ($4C_Q$) versus the external shell. Finally, the intershell resistance ($R_t$) accounts for intershell tunnel transport phenomena [3].

Electrical level simulation has been performed for the proposed bus implementations by using HSPICE. As an example, the case of a 3-line bus has been considered. The crosstalk effects (in terms of both crosstalk-induced delay and peak voltage) have been evaluated. Simulations have been performed at a bus frequency of $800MHz$, a spacing between adjacent DWNTs of $4nm$, and a DWNT length and diameter of $10\mu m$ and $2nm$, respectively (as permitted by current nanotechnology [16]). The total coupling capacitance between the outermost shells of adjacent DWNTs has been derived from a conventional metallic coaxial configuration. The two cases in the arrangements of the DWNTs are given as follows.

### A. Case 1

Assume that the shielding signal of each DWNT of the 3-line bus is connected to a copy of the considered signal, i.e, each bus driver is duplicated and the output is connected to the corresponding shielding signal. Fig. 5 shows the eye diagram obtained by simulation. As for the crosstalk-induced delay in the worst and best cases ($\tau_{dw}$ and $\tau_{db}$), and the crosstalk-

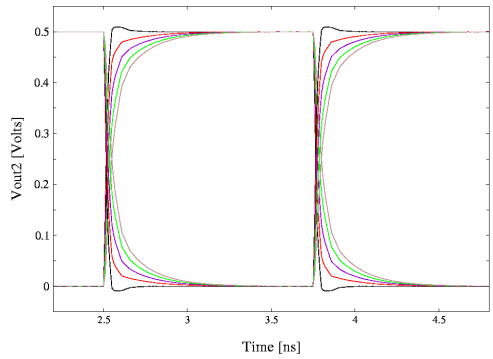


Fig. 5. Eye diagram for the 3-line DWNT bus, Case 1.

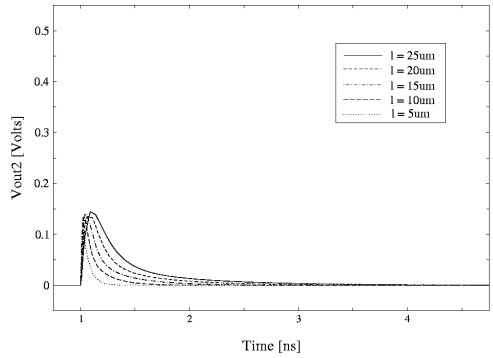


Fig. 6. Crosstalk-induced peak voltage for the proposed bus architecture (Case 1).

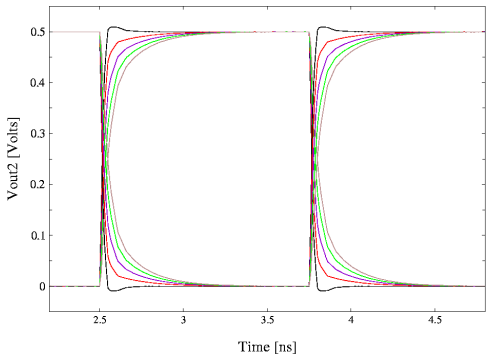


Fig. 7. Eye diagram for the 3-line DWNT bus, Case 2.

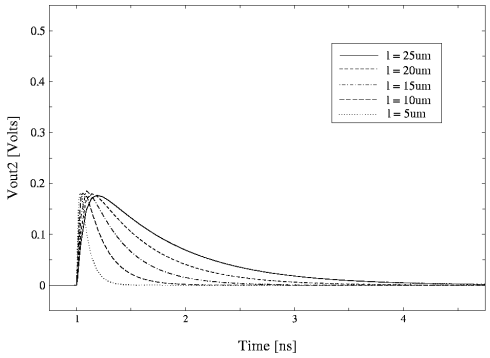


Fig. 8. Crosstalk-induced peak voltage for the proposed 3-line bus architecture (Case 2).

induced delay uncertainty ($\Delta\tau_d$), the following values have been found by simulation: $\tau_{dw} = 36.7ps$, $\tau_{db} = 6.9ps$ and $\Delta\tau_d = 29.8ps$. Therefore, $\Delta\tau_d$ is approximately $81\%$ of $\tau_{dw}$, that indicates a high uncertainty in signal propagation delay to negatively impact reliability. As shown in Fig. 5 the signal voltage swing is not reduced from the expected $0.5V$.

Fig. 6 shows the peak voltage induced on the victim line (that is supposed to be steady at 0) by the simultaneous switching of the aggressors in the same direction ($0 \rightarrow 1$ in this example), for several values of nanotube length. As the line length increases, at first the peak amplitude and duration increase too. For longer length, the glitch amplitude saturates at a level slightly below 0.15V, while the duration continues to increase. This induced peak voltage is therefore always below the threshold voltage of the symmetric receivers ($\simeq V_{dd}/2 = 0.25V$). By considering also filtering at the receiver, the glitch at the output of the receiver will never reach the logic threshold of the input gates of the sampling elements connected to the receiver.

### B. Case 2

While reduced voltage noise margins and increased power consumption with a substantial reduction in crosstalk can be resolved by utilizing the bus implementation of Case 1, the difficulty encountered in connecting each shell of the DWNT to different signals still remains [13], [9], [17].

Therefore, assume that it is possible to connect the shielding signal of each DWNT of the 3-line bus with the corresponding input signal, i.e. both shells of each DWNT are connected to the same signal by means of a single contact (i.e., $Vin_i = Vis_i$). As proved in [13], [17], [9], this is possible also in today's technology.

Fig. 7 shows the eye diagram obtained by simulation. The following values have been found by simulation: $\tau_{dw} = 64ps$, $\tau_{db} = 7.9ps$ and $\Delta\tau_d = 56.1ps$. Therefore, $\Delta\tau_d$ is approximately $88\%$ of $\tau_{dw}$, i.e. a high uncertainty is encountered in signal propagation delay. This may negatively impact reliability.

Fig. 8 shows the peak voltage induced on the victim line under the same switching conditions considered for Case 1. The same type of behavior as for Case 1 (Fig. 6) is found, but the glitch amplitude saturates at a level slightly below 0.2V.

## IV. Comparison of CNT Bus Architectures

A comparison has been performed between the proposed DWNT architecture (for both cases) and the "standard" bus architecture composed by parallel SWNTs described in Sect. II. This comparison accounts for area, power consumption, crosstalk-induced delay, delay uncertainty and crosstalk-induced peak voltage. In the simulations, the parameters are the same as those reported in the previous section. Table I summarizes the results (entries in bold identify the best performance).

For comparison, the area on the horizontal plane has been

TABLE I

COMPARISON AMONG BUS ARCHITECTURES.

| Bus Architecture | SWNTs | DWNT (Case 1) | DWNT (Case 2) |
|---|---|---|---|
| Area $[\mu m^2/\mu m]$ | **0.005** | 0.01 | 0.01 |
| Power Consumption $[nWatts]$ | **775** | 800 | 780 |
| $\tau_{dw}$ $[ps]$ (for $l = 10\mu m$) | 131.3 | **36.7** | 64 |
| $\Delta\tau_d$ $[ps]$ (for $l = 10\mu m$) | 121.8 | **29.81** | 56.1 |
| Crosstalk-induced peak voltage $[V]$ | 0.21 | **0.15** | 0.2 |

considered. From Table I, the proposed bus architectures require an area that is twice as large as for a bus architecture implemented by parallel SWNTs. The significant difference in area between the proposed parallel DWNT and the SWNT bus architectures occurs due to geometry, i.e. the smallest diameter has been considered for SWNT bus architecture (the smallest diameter for a current SWNT fabrication process is equal to 1nm [1]).

For the crosstalk-induced delay, Table I reports the remarkable advantage of the proposed bus architecture over the previous one. The proposed bus architecture features a worst case delay up to $72\%$ (Case 1) shorter than a SWNT bus, allowing to noticeably increase bus speed. As previously introduced, a possible strategy to reduce the crosstalk effects in the SWNT bus is to increase the spacing between adjacent lines. Note that by considering the same bus area ($sp$ = $4.5nm$ for the SWNT bus), the proposed architecture allows a significant reduction (up to 62%) of the worst case delay with respect to the SWNT bus (albeit at a 34% power increase).

For delay uncertainty, the value for the proposed architecture is $81\%$ for Case 1, and $87\%$ for Case 2, of their worst delay, respectively, while for the SWNT bus it is $93\%$ of its worst delay.

Furthermore from Table I the proposed bus architecture presents a crosstalk-induced peak voltage lower (29%) or comparable than for the SWNT bus. Therefore, the probability of crosstalk noise (that may result in logic errors) is much lower in the proposed architecture.

Therefore, the proposed bus architecture considerably improves performance and reliable operation of the IC.

## V. CONCLUSIONS

A novel bus architecture (with two different implementations) has been proposed; it consists of dual-walled nanotubes (DWNTs) in parallel. In the proposed architecture, the crosstalk-induced delay and delay uncertainty, as well as the crosstalk-induced peak voltage are significantly reduced (up to $72\%$ for crosstalk-induced delay, and up to $76\%$ for crosstalk-induced peak voltage) compared with previously presented CNT bus architectures. This has been achieved at the cost of a modest increase in area.

## REFERENCES


[1] P. Avouris, J. Appenzeller, R. Martel, and S. Wind, "Carbon Nanotube Electronics", *Proc. of the IEEE*, pages 1772 – 1784, November 2003.

[2] R. H. Baughman, A. Zakhidov, and W. A. de Heer, "Carbon Nanotubes–the Route Toward Applications", *Science*, pages 787–792, August 2002.

[3] B. Bourlon, C. Miko, L. Forró, D. C. Glattli, and A. Bachtold "Determination of the Intershell Conductance in Multiwalled Carbon Nanotubes", *Physical Review Letters*, pages 176806–1 – 176806–4, October 2004.

[4] P. J. Burke, "Luttinger Liquid Theory as a Model of the Gigahertz Electrical Properties of Carbon Nanotubes", *IEEE Trans. on Nanotechnology*, pages 129 – 143, September 2002.

[5] P. J. Burke, "An RF Circuit Model for Carbon Nanotubes", *IEEE Trans. on Nanotechnology*, pages 55 – 58, March 2003.

[6] P. J. Burke, "Quantitative Theory of Nanowire and Nanotube Antenna Performance", *ArXiv Condensed Matter e-prints*, pages 1 – 15, August 2004.

[7] J. M. Cazeaux. D. Rossi, C. Metra, and F. Lombardi, "Modeling Crosstalk Effects in CNT Bus Architectures", unpublished.

[8] W. B. Choi, E. Bae, D. Kang, S. Chae, B. Cheong, J. Ko, E. Lee, and W. Park, "Aligned carbon nanotubes for nanoelectronics", *IoP J. of Nanotechnology*, pages S512 – S516, October 2004.

[9] P. J. de Pablo, E. Graugnard, B. Walsh, R. P. Andres, S. Datta, and R. Reifenberger, "A simple, reliable technique for making electrical contact to multiwalled carbon nanotubes", *Applied Physics Letters*, pages 323–325, October 1999.

[10] S. Frost, T. Dysart, P. Kogge, and C. Lent, "Carbon Nanotubes for Quantum-Dot Cellular Automata Clocking", In *Proc. of IEEE Conf. on Nanotechnology*, pages 171 – 173, August 2004.

[11] W. Hoenlein, F. Kreupl, G. S. Duesberg, A. P. Graham, M. Liebau, R. V. Seidel, and E. Unger, "Carbon Nanotube Applications in Microelectronics, *IEEE Trans. on Components and Packaging Technologies*, pages 629 – 634, December 2004.

[12] L. D. Huang, H. M. Cheng, and D. F. Wong, "Global Wire Bus Configuration with Minimum Delay Uncertainty", In *Proc. of Design, Automation and Test in Europe Conf.*, pages 50 – 55, 2003.

[13] H. J. Li, W. G. Lu, J. J. Li, X. D. Bai, and C. Z. Gu, "Multichannel Ballistic Transport in Multiwall Carbon Nanotubes", *Physical Review Letters*, pages 086601–1 – 086601–4, August 2005.

[14] J. Li, Q. Ye, A. Cassell, J. Koehne, H. T. Ng, J. Han, and M. Meyyappan, "Carbon Nanotube Interconnects: a Process Solution", In *Proc. of IEEE Int. Interconnect Technology Conf.*, pages 271 – 272, 2003.

[15] A. Naeemi, R. Sarvari, and J. Meindl, "Performance Comparison Between Carbon Nanotube and Copper Interconnects for Gigascale Integration (GSI)", *IEEE Electron Device Letters*, pages 84 – 86, February 2005.

[16] Q. Ngo, D. Petranovic, S. Krishnan, C. A. M, Q. Ye, J. Li, M. Meyyappan, and C. Y. Yang, "Electron Transport Through Metal-Multiwall Carbon Nanotube Interfaces", *IEEE Trans. on Nanotechnology*, pages 311 – 317, June 2004.

[17] M. Nihei, D. Kondo, A. Kawabata, S. Sato, H. Shioya, M. Sakaue, T. Iwai, M. Ohfuti, and Y. Awano, Low-resistance Multi-walled Carbon Nanotube Vias with Parallel Channel Conduction of Inner Shells, In *Proc. of IEEE Int. Interconnect Technology Conf.*, pages 251 – 253, 2005.

[18] A. K. Palit, V. Meyer, W. Anheier, and J. Schloeffel, "Modeling and Analysis of Crosstalk Coupling Effect on the Victim Interconnect Using the ABCD Network Model", In *Proc. of IEEE Int. Work. on Defect and Fault Tolerance in VLSI Systems*, pages 174 – 182, 2004.

[19] A. Raychowdhury, S. Mukhopadhyay, and K. Roy, "A Circuit-Compatible Model of Ballistic Carbon Nanotube Field-Effect Transistors", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, pages 1411 – 1420, October 2004.

[20] A. Raychowdhury and K. Roy, "Modeling of Metallic Carbon Nanotube Interconnects for Circuit Simulations and a Comparison with Cu Interconnects for Scaled Technologies", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, pages 1213 – 1224, January 2006.

[21] S. Salahuddin, M. Lundstrom, and S. Datta, "Transport Effects on Signal Propagation in Quantum Wires", *IEEE Trans. on Electron Devices*, pages 1734 – 1742, August 2005.

[22] B. Q. Wei, R. Vajtai, and P. Ajayan, "Reliability and current carrying capacity of carbon nanotubes", *Applied Physics Letters*, pages 1172 – 1174, July 2001.