Novel Approach to Reduce Power Droop During Scan-Based Logic BIST[*]

M. Omaña   D. Rossi   F. Fuzzi   C. Metra

ARCES – DEI, University of Bologna
Bologna, Italy
{martin.omana, d.rossi, filippo.fuzzi, cecilia.metra}@unibo.it

C. Tirumurti   R. Galivache

Intel Corporation
Santa Clara, CA
{chandra.tirumurti, rajesh.galivanche}@intel.com

Abstract— **Significant peak power (PP), thus power droop (PD), during test is a serious concern for modern, complex ICs. In fact, the PD originated during the application of test vectors may produce a delay effect on the circuit under test signal transitions. This event may be erroneously recognized as presence of a delay fault, with consequent generation of an erroneous test fail, thus increasing yield loss. Several solutions have been proposed in the literature to reduce the PD during test of combinational ICs, while fewer approaches exist for sequential ICs. In this paper, we propose a novel approach to reduce peak power/power droop during test of sequential circuits with scan-based Logic BIST. In particular, our approach reduces the switching activity of the scan chains between following capture cycles. This is achieved by an original generation and arrangement of test vectors. The proposed approach presents a very low impact on fault coverage and test time, while requiring a very low cost in terms of area overhead.**

Keywords— Logic BIST, Power Droop, Test, Microprocessor

I. INTRODUCTION

The aggressive scaling of microelectronic technology is allowing the fabrication of increasingly complex ICs. Together with several benefits (improved functionality, decreased cost per function, etc.), this comes through with several challenges, especially from the points of view of system test and reliability.

The increase in peak power (PP), and consequently in power droop (PD), are serious concerns for ICs' test and operation in the field. Particularly, the PP and PD during test may exceed those experienced during the IC in field operation, due to the higher switching activity (SA) induced by the applied test patterns [1, 2, 3, 4, 5, 6, 7]. As a consequence, a delay effect may be generated on circuit under test (CUT) signal transitions, which may be erroneously recognized as presence of delay faults, with the consequent erroneous generation of a test fail (hereinafter referred to as false test fail), with consequent increase of yield loss [2, 3].

Many ATPG approaches have been proposed to avoid this problem. Most of them utilize *don't care* (X) bits to reduce the SA induced by the applied test patterns (e.g., those in [9, 10]). However, such approaches cannot be used for system debug or field test, where Logic Built-In Self-Test (LBIST) is becoming increasingly vital [8].

As known, LBIST can take the form of "combinational LBIST" or "scan-based LBIST", depending on whether the CUT is a combinational or a sequential circuit with scan [6, 11]. A linear feedback shift register (LFSR) generates test patterns to be directly given to the CUT primary inputs, in case of combinational CUT, or to the scan chain inputs, in case of sequential CUT [1, 2, 6, 12, 13]. In scan-based LBIST, testing consists of two phases [6, 12]: a shift phase, during which the scan chains are filled with test patterns, and a capture phase, in which the test patterns are applied to the CUT and the produced outputs are sampled. Despite being a widely adopted design, LBIST, both combinational and scan-based, suffers from the PD-induced problems described above.

As a significant case, in this paper we consider sequential CUT with scan-based LBIST. During the capture phase, this kind of circuits suffer from the PD problems discussed above, due to the high SA of the CUT, which is induced by the applied test patterns. The produced delay effect can be erroneously recognized as presence of a delay fault, with the consequent generation of a false test fail. Solutions to reduce PD during the capture phase in scan-based LBIST are therefore needed, in order to avoid yield loss increase.

Several solutions have been proposed in the literature to reduce PP, thus also PD, for combinational LBIST (e.g., [1, 3, 6]), while fewer approaches exist for scan-based LBIST [2, 8, 14]. The solutions for combinational LBIST in [1, 3, 6] modify the internal structure of traditional LBIST LFSRs to generate intermediate test vectors. Such vectors, inserted between each couple of original test vectors, allow to reduce the SA of the CUT inputs, thus reducing the whole CUT SA [1]. Therefore, the PP and PD are reduced as well. These techniques require low area overhead and feature negligible impact on fault coverage (FC) and test time, but are not effective in reducing PD during the capture cycles in scan-based LBIST.

To address the issue of PD reduction during the capture cycles in scan-based LBIST, the solutions in [2, 8, 14] have been proposed. Particularly, in [2] PD is reduced by alternately disabling groups of scan chains during test. This is a successful approach to reduce PD, but requires a significant increase in the number of test vectors, and consequently test time, to achieve the same FC as with conventional scan-based LBIST. In [8] PD is reduced by a multi-cycle BIST scheme with partial observation. This solution does not significantly impact FC, but it allows to reduce PD by only 10% compared to conventional

IEEE
computer
society

scan-based-LBIST.

Instead, compared to conventional scan-based LBIST, the solution in [14] inserts an additional phase, namely a "burst" phase, between the scan shift and capture cycles. Such an additional burst phase aims at increasing the current drawn from the power supply up to a value similar to that absorbed by the CUT during the capture cycle. This way, the inductive component of the PD occurs during the burst phase, and vanishes before the capture cycle. Therefore, the PD occurring during the capture cycle, consisting of the resistive component only, is considerably reduced. This solution does not impact test coverage and can be used together with other power reduction techniques. However, it requires an accurate modeling of the power supply network and increases the total power consumed during testing, as well as test time.

Based on these considerations, in this paper we propose a novel approach to reduce PD during the capture cycles in scan-based LBIST, thus reducing the probability to have false test fails during test. Similarly to the solution in [1, 6], our proposed approach reduces the SA of the CUT by proper modification of test vectors, compared to conventional scan-based LBIST. This is accomplished by exploiting the phase shifter, which is usually adopted in scan-based LBIST to reduce the correlation among the test vectors applied to adjacent scan-chains [15].

In our proposed approach, the test vector to be applied at the generic capture cycle i in conventional scan-based LBIST is replaced by a new vector, hereinafter denoted by *substitute test vector*, which is generated starting from the test vectors to be applied at capture cycles $(i$-1$)$ and $(i+1)$, in order reduce the CUT SA. Such two test vectors are provided by the phase shifter at proper outputs, as clearly described in Section IV. The substitute test vector is generated in order to reduce the maximum number of transitions at the outputs of the scan chains between capture cycles $(i$-1$)$ and i, and i and $(i+1)$, compared to the original test sequence. This way, the CUT SA, thus also PD, is decreased during capture cycles. Our approach allows a 50% reduction of the maximum SA during capture cycles, with no impact on test length and fault coverage compared to conventional scan-based LBIST. Moreover, it requires a very limited area overhead.

The remainder of the paper is organized as follows. In Section II, we describe the considered scan-based LBIST. In Section III, we introduce our approach for PD reduction during capture cycles. In Section IV, we describe a possible implementation of our proposed approach. In Section V, we evaluate the effectiveness and costs of our approach, and compare them to those of conventional scan-based LBIST and of the solution in [2] providing a PD reduction similar to our approach. Finally, some conclusions are drawn in Section VI.

II.   CONSIDERED SCENARIO

We consider the widely adopted scan-based LBIST architecture represented in Fig. 1 [1, 4, 6, 12, 15].

The state flip-flops of the CUT are converted into scan flip-flops, and arranged into many short scan chains (s scan chains in Fig. 1). Additional scan flip-flops are included in such scan chains to drive and sample the primary inputs (PI) and primary
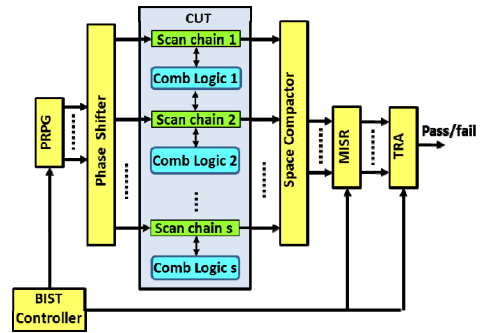

Fig. 1. Considered scan-based LBIST architecture.

outputs (PO), respectively.

The Pseudo-Random Pattern Generator (PRPG) is implemented by an LFSR [4, 12, 15]. The Phase Shifter (PS), allowing to reduce the correlation among the test vectors applied to adjacent scan-chains [15], is composed by an XOR network expanding the number of outputs of the LFSR in order to match the number of scan chains s. In fact, the number of LFSR outputs is usually considerably smaller than the number of scan chains [15]. At the same clock cycle, the PS provides as outputs, the current LFSR sequence together with many future/past sequences. As described later on, this feature will be exploited by our proposed solution in order to derive the new test vectors allowing to reduce PD during capture cycles.

The Space Compactor compacts the outputs of the s scan chains to match the number of inputs of the MISR. The MISR, as well as the Test Response Analyzer (TRA) and the BIST Controller are the same as in conventional scan-based LBIST [6, 12].

As known, two phases can be identified in scan-based LBIST [12]: a shift phase, during which the scan chains are filled with test vectors, and a capture phase, in which the test vectors are applied to the CUT and the produced outputs are sampled. In particular, during the shift phase, at each clock cycle, the phase shifter provides a new bit to each one of the s scan chains (in parallel). Thus, in this phase, the test vector T_i^m to be applied to the CUT at the i-th capture cycle is loaded into the m-th scan chain ($m = 1..s$) after n shift cycles (where n is the number of scan flip-flops of the longest scan chain). After such shift cycles, a single capture cycle is performed, and the CUT response is sampled on the scan chains. Then, other n scan shift cycles are required to shift-out the CUT response and to shift-in the new test vector T_{i+1}^m ($m = 1..s$).

As for scan-flip-flops, we have considered the widely adopted scheme in [16], which updates its output only at the beginning of capture cycles, while keeping it constant to its previous value loaded during the shift phase.

III.   PROPOSED APPROACH FOR POWER DROOP REDUCTION DURING SCAN-BASED LBIST

In this section, we introduce our approach for PD reduction during the capture phase in scan-based LBIST. As previously introduced, our approach exploits the phase shifter (PS) to determine the substitute test vector ST_i^m (Fig. 2(a)) replacing the original test vector T_i^m to be applied to the scan chain m

(*m*=1..*s*) at the *i-th* capture cycle. As will be shown later, the PS allows to easily construct ST_i^m, based on the structure of test vectors T_{i-1}^m and T_{i+1}^m to be applied to scan chain *m* at the *(i-1)-th* and *(i+1)-th* capture cycles. Starting from the *(i-1)-th* capture cycle (as represented in Fig. 2), the new test vector sequence in each scan chain *m* will be as follows:

$$T_{i-1}^m - ST_i^m - T_{i+1}^m - ST_{i+2}^m - T_{i+3}^m \ \cdots$$

As schematically represented in Fig. 2(b), the substitute test vector is constructed using random injection [6]. As can be observed from Fig. 2(b), denoting by $ST_i^m(j)$, $T_{i-1}^m(j)$ and $T_{i+1}^m(j)$ the values in position *j* in the test vectors ST_i^m, T_{i-1}^m and T_{i+1}^m, respectively, the value of $ST_i^m(j)$ is determined as follows:

$$ST_i^m(j) = \begin{cases} T_{i-1}^m(j) & if \ T_{i-1}^m(j) = T_{i+1}^m(j) \\ \\ R & if \ T_{i-1}^m(j) \neq T_{i+1}^m(j) \end{cases},$$

where R is a random bit. Therefore, in all positions *j* in which vectors T_{i-1}^m and T_{i+1}^m coincide, ST_i^m maintains the same logic value as the previous vector T_{i-1}^m, while in the positions *j* in which vectors T_{i-1}^m and T_{i+1}^m differ, ST_i^m assumes a random logic value *R*. The bit *R* can simply come from one of the outputs of the LFSR itself, as suggested in [6].

This way, ST_i^m will present more bits equal to T_{i-1}^m and T_{i+1}^m than the original T_i^m, and thus, the number of switching bits in the new sequence T_{i-1}^m - ST_i^m - T_{i+1}^m will be smaller than that in the original test vector sequence of conventional LBIST T_{i-1}^m - T_i^m - T_{i+1}^m. Moreover, ST_i^m presents a random bit R in the positions where T_{i-1}^m and T_{i+1}^m are different. This way, the new sequence T_{i-1}^m - ST_i^m - T_{i+1}^m preserves the randomness of the original sequence in these bits [6].

As will be shown in Section V, our approach allows a reduction of approximately 50% in the SA of the CUT with respect to conventional LBIST, while featuring the same fault coverage and test length. In turn, this leads to a significant reduction of the PD and, consequently, of the probability to generate false test fails.

Since our approach reduces the number of switching bits in the new test sequence compared to conventional LBIST, the power consumption associated to glitches due to unbalanced

paths within the CUT is expected to be reduced as well.

It is worth noticing that, if a higher SA reduction is required, our solution can be properly scaled by introducing two or more proper substitute test vectors (depending on the target SA reduction) between two original test vectors.

IV. POSSIBLE IMPLEMENTATION

Our solution exploits the fact that, for each scan chain *m* and capture cycle *i*, at every scan CK cycle *j* (*j=1..n*), the PS provides at its outputs the values $T_i^m(j)$ (*m = 1..s*), together with many of its past/future values. In fact, if the number of outputs *m* of the PS is considerably larger than the depth *n* of the longest scan chain (i.e., if *m >> n*), as it is usually the case in actual designs [15], then it is very likely that the value of $T_i^m(j)$ at *n* past and future CK cycles are provided by other outputs of the PS. Nevertheless, the PS can be designed in order to provide all necessary values for the application of the proposed approach. Therefore, given the PS design, at each scan CK cycle *j*, we can determine the past/future logic value ($T_{i-1}^m(j)/T_{i+1}^m(j)$) of each $T_i^m(j)$ (*m=1..s*) by observing proper outputs of the PS itself.

Denoting by O^m (*m = 1..s*) the PS output feeding the scan chain *m*, the logic value in the *j-th* position of the *i-th* test vector of the scan chain *m*, that is $T_i^m(j)$, is given by:

$$T_i^m(j) = O^m(\xi),$$

where $\xi = n(i-1) + j$ is the current shift clock cycle, represented as the number of the total shift clock cycles applied by the LBIST architecture from the beginning of the test. Therefore, considering that each capture cycle *i* requires *n* shift cycles, the logic values in the position *j* of the vector applied at the previous and to be applied at the next capture cycles to the scan chain *m* ($T_{i-1}^m(j)$ and $T_{i+1}^m(j)$, respectively) are the values assumed by O^m at *n* cycles before and after, respectively, the current shift clock cycle *ξ*. Namely, it is:

$$T_{i-1}^m(j) = O^m(\xi - n); \quad T_{i+1}^m(j) = O^m(\xi + n).$$

As per the characteristic of the PS to provide at its outputs many past/future values of each output O^m, we can determine the values of $O^m(\xi - n)$ and $O^m(\xi + n)$ from the current value present at proper two PS outputs. Therefore, there exist two values *k* and *p*, with *k, p = 1..s, k ≠ p* and both different from *m*, so that:

$$O^m(\xi - n) = O^k(\xi); \quad O^m(\xi + n) = O^p(\xi).$$

As an example, Fig. 3 shows a possible implementation of our proposed scheme, for the case in which the depth of the longest chain(s) is *n*.

As shown in Fig. 3, our approach requires 2 multiplexers (M1 and M2) and an XOR gate for each scan chain *m*. The multiplexer M2 allows to load in the scan chain *m* : 1) at the *(i-1)-th* and *(i+1)-th* capture cycles, the test vectors T_{i-1}^m and T_{i+1}^m generated by PS, by setting the selection signal *int*=0; 2) at the *i-th* capture cycle, the substitute vector ST_i^m, provided by the multiplexer M1, by setting *int*=1. The signal *int* is generated in such a way that it switches from 0 to 1 (and vice versa), at following capture cycles.
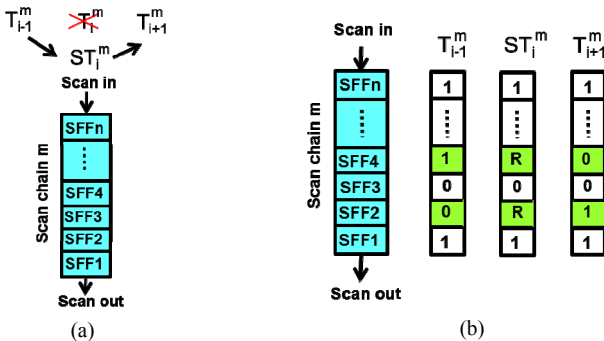

Fig. 2. Schematic representation of our approach: (a) sequence of test vectors filling each scan chain, (b) substitute test vector ST_i^m using the random injection approach scan-based LBIST architecture.
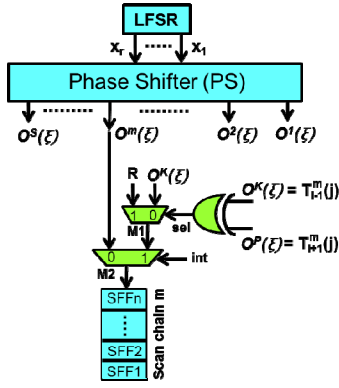
Fig. 3. Schematic representation of a possible implementation of our proposed approach.

As for the XOR gate, at each scan CK cycle j, it compares the logic value at PS output $O^k(\xi)$ (equal to $T_{i-1}^m(j)$) with the logic value at PS output $O^p(\xi)$ (equal to $T_{i+1}^m(j)$). Thus, the XOR makes $sel=0$, if $O^k(\xi) = O^p(\xi)$ (or, equivalently, if $T_{i-1}^m(j) = T_{i+1}^m(j)$), indicating that the logic value of bit $ST_i^m(j)$ should be equal to $O^k(\xi) = T_{i-1}^m(j)$. Instead, the XOR gate makes $sel=1$, if $O^k(\xi) \neq O^p(\xi)$ (or, equivalently, if $T_{i-1}^m(j) \neq T_{i+1}^m(j)$), indicating that the logic value of $ST_i^m(j)$ should be a random value R. Therefore, when it is $int=1$, depending on the sel value, M1 selects whether to drive in the scan chain m the value on $O^k(\xi)$, or the random value R.

In order to better illustrate our proposed approach, let us consider the simple scan-based LBIST structure schematically represented in Fig. 4 as an example. It consists of: i) a 4 bit LFSR ($x_1(\xi)$, $x_2(\xi)$, $x_3(\xi)$, $x_4(\xi)$), with the characteristic polynomial $p(x)=x^4+x+1$; ii) a phase shifter (PS), expanding the 4 bits of the LFSR to $s=12$ outputs: $O^1(\xi)..O^{12}(\xi)$ (providing signals $T_i^1(j) .. T_i^{12}(j)$), where 12 is the number of scan chains in the considered scan-based LBIST structure. Additionally, for simplicity, but without loss of generality, we suppose that the longest scan chain is composed by $n=3$ scan flip-flops. Therefore, in the considered example, each shift phase requires 3 scan CK cycles.

As shown in Fig. 4, the PS has been designed in order to provide, at every shift cycle ξ,: i) the current state of the LFSR (i.e., $x_1(\xi)..x_4(\xi)$), on $O^2(\xi)$, $O^5(\xi)$, $O^8(\xi)$, $O^{11}(\xi)$; ii) the state of the LFSR at 3 scan CK cycles before the current state (i.e., $x_1(\xi-3)..x_4(\xi-3)$), on $O^1(\xi)$, $O^4(\xi)$, $O^7(\xi)$, $O^{10}(\xi)$;
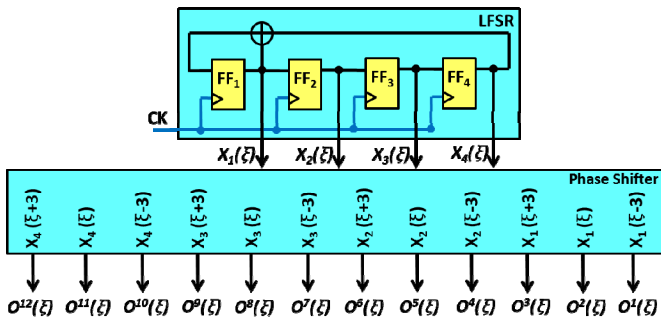
iii) the state of the LFSR at 3 scan CK cycles after the current state of the LFSR (i.e., $x_1(\xi+3)..x_4(\xi+3)$), on the remaining signals $O^3(\xi)$, $O^6(\xi)$, $O^9(\xi)$, $O^{12}(\xi)$.

The logic operations performed by PS to compute $O^1(\xi)..O^{12}(\xi)$ as a function of the current state of the LFSR $x_1(\xi)..x_4(\xi)$ are reported in the second column of Table I. As can be seen, all $O^m(\xi)$ signals ($m=1..12$) are expressed as linear combinations of the present state of the LFSR, and can be computed by simple XOR trees.

As previously discussed, since the depth of the longest scan chain is $n=3$, for each scan chain m ($m=1..12$) and at each scan CK cycle ξ, our approach needs to determine the value present on the considered scan chain at 3 scan CK cycles before (i.e., $O^m(\xi-3)$) and at 3 scan CK cycles after (i.e., $O^m(\xi+3)$), to determine $T_{i-1}^m(j)$ and $T_{i+1}^m(j)$, respectively. The third and fourth columns of Table I report the PS outputs, or output combinations, giving $O^m(\xi-3)$ and $O^m(\xi+3)$ for each $O^m(\xi)$ ($m=1..12$).

From Table I, we can observe that the logic values $O^m(\xi-3)$ and $O^m(\xi+3)$, for $m = 1, 2, 5, 8, 11$ and 12, are equal to the values assumed by other outputs of the PS at the current CK cycle ξ.

Instead, for $m = 3, 4, 6, 7, 9$ and 10, the past/future values of $O^m(\xi)$ are not directly present on other outputs of the PS. Nevertheless, they can be simply obtained as a linear combination of the current outputs of the PS. This will require a small extra area overhead, due to the additional XOR gates. However, this extra area is negligible in practical designs with a large number of PS outputs.

V. VERIFICATION AND COMPARISON

In this section, we first report the results of the simulations that we have performed with the Synopsys Design Compiler tool to verify the effectiveness of our approach in reducing PD during scan-based LBIST. In particular, we have evaluated the SA at the outputs of the scan chains between two following capture cycles. We also report the results of the Synopsys TetraMAX simulations that we have performed to evaluate the

Fig. 4. Schematic representation of the simple LFSR and phase shifter considered here to illustrate the operation of our approach.

TABLE I. PS PERFORMED FUNCTIONS AND GENERATED OUTPUTS.

$O^m(\xi)$ $= T_i^m(j)$	PS Function	$O^m(\xi-3) =$ $T_{i-1}^m(j)$	$O^m(\xi+3) =$ $T_{i+1}^m(j)$
$O^1(\xi)$	$X_4(\xi)$	$O^{10}(\xi)$	$O^2(\xi)$
$O^2(\xi)$	$X_1(\xi)$	$O^1(\xi)$	$O^3(\xi)$
$O^3(\xi)$	$X_1(\xi)\oplus X_2(\xi)\oplus X_3(\xi)\oplus X_4(\xi)$	$O^2(\xi)$	$O^3(\xi)\oplus O^6(\xi)$
$O^4(\xi)$	$X_1(\xi)\oplus X_2(\xi)$	$O^4(\xi)\oplus O^{11}(\xi)$	$O^5(\xi)$
$O^5(\xi)$	$X_2(\xi)$	$O^4(\xi)$	$O^6(\xi)$
$O^6(\xi)$	$X_1(\xi)\oplus X_3(\xi)\oplus X_4(\xi)$	$O^5(\xi)$	$O^3(\xi)\oplus O^9(\xi)$
$O^7(\xi)$	$X_2(\xi)\oplus X_3(\xi)$	$O^4(\xi)\oplus O^7(\xi)$	$O^8(\xi)$
$O^8(\xi)$	$X_3(\xi)$	$O^7(\xi)$	$O^9(\xi)$
$O^9(\xi)$	$X_1(\xi)\oplus X_4(\xi)$	$O^8(\xi)$	$O^3(\xi)\oplus O^2(\xi)$
$O^{10}(\xi)$	$X_3(\xi)\oplus X_4(\xi)$	$O^7(\xi)\oplus O^{10}(\xi)$	$O^{11}(\xi)$
$O^{11}(\xi)$	$X_4(\xi)$	$O^{10}(\xi)$	$O^{12}(\xi)$
$O^{12}(\xi)$	$X_1(\xi)$	$O^{11}(\xi)$	$O^3(\xi)$

fault coverage (FC) achieved with our solution.

Finally, we also compare effectiveness and costs of our approach with those of conventional scan-based LBIST [12] (hereinafter referred to as Conv-LBIST) and the solution in [2], which provides a PD reduction similar to our proposed scheme.

A. Verification and Comparison with Conv-Scan-Based LBIST

We have considered the five ISCAS'89 benchmarks reported in Table II and, for all circuits, we have used a 20 bits LFSR, with the maximal length characteristic polynomial $p(x) = x^{20} + x^3 + 1$ [17]. The number of scan chains employed for each benchmark circuit is reported in Table II. As for PS, it has been implemented in order to minimize area overhead, according to the rules described in [15].

For our solution and the Conv-LBIST, Fig. 5 shows the distribution of SA in all scan-chains between any two following test vectors, after the application of 10000 test vectors. As can be seen, for all considered cases our solution allows to reduce considerably (by approximately 50%, as expected) the maximum SA (SA_{MAX} in Tab. II) with respect to the Conv-LBIST. Therefore, our solution allows a considerable
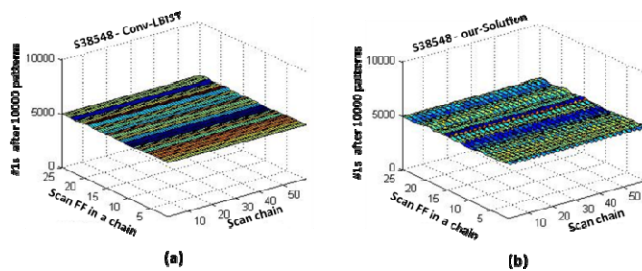
Fig. 6. Total number of 1s on each scan FF after the application of all 10000 test vectors to the s38584 benchmark implemented using: (a) conventional scan-based LBIST, (b) our proposed scan-based LBIST solution.

PD reduction compared to conventional scan-based LBIST. Moreover, from Fig. 5 we can observe that, for all considered cases, our solution allows to reduce also the mean SA by approximately 50% compared to Conv-LBIST. As a result, also the total power associated with the capture cycles is considerably reduced. As shown later, these results are achieved without increasing the test length.

Fig. 6 shows the total number of 1s loaded on each scan FF after the application of all 10000 test vectors for both Conv-LBIST and our solution. The large benchmark s38548 has been considered. We can observe that the number of 1s in each SFF of our solution (Fig. 6(b)) is approximately equal to 5000 (half the number of applied test vectors, and approximately equal to the number of 0s), which is equal to the number of 1s in each SFF in the Conv-LBIST (Fig. 6(a)). Thus, we can expect that our solution does not impact the randomness of test vectors with respect to a conventional scan-based LBIST, as shown in [6]. The preservation of the randomness of the test vectors, as described in [6], and as proven later in this section, allows us to reasonably expect that the FC achieved with our approach will be approximately the same as that of Conv-LBIST.

Table II reports the values of the FC and the SA_{MAX} for our solution and Conv-scan-based LBIST, as well as their relative variations, for five different ISCAS'89 benchmarks, after the application of 10000 test vectors. The relative variations of FC and SA_{MAX} are calculated as: $\Delta FC = 100*(FC_{OUR} - FC_{Conv-LBIST}) / FC_{Conv-LBIST}$, and $\Delta SA_{MAX} = 100*(SA_{MAX\ OUR} - SA_{MAX\ Conv-LBIST}) / SA_{MAX\ Conv-LBIST}$.

As anticipated before, we can observe that, in all cases, our solution allows to reduce considerably (approximately 50%) the SA_{MAX} with respect to Conv-LBIST for the same number of applied test vectors #TV, while featuring a similar FC.
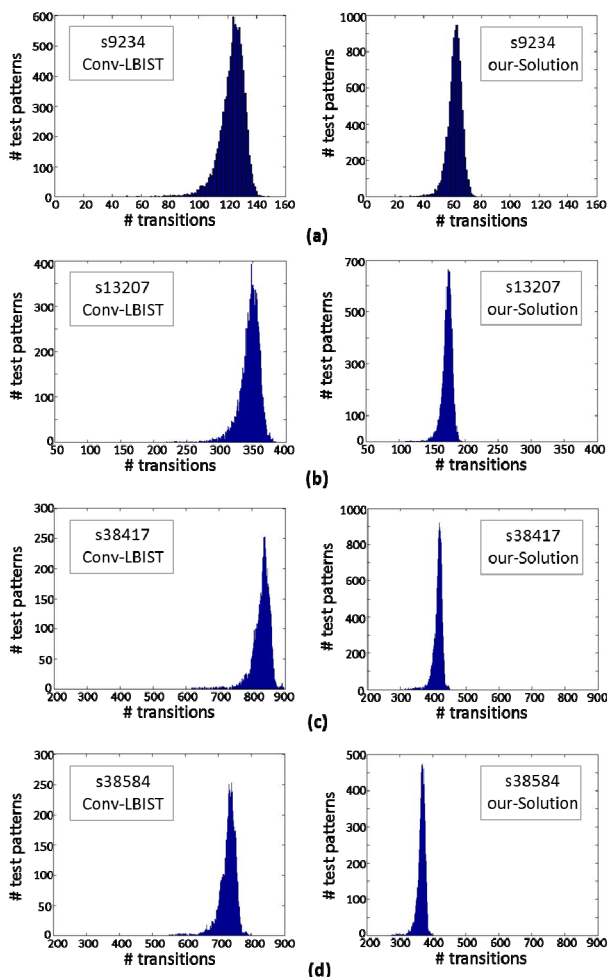

Fig. 5. Distribution of the total switching activity in all scan-chains between two following test patterns, for both the conventional scan-based LBIST and our approach, for the benchmarks: (a) s9234, (b) s13207, (c) s38417 and (d) s38584.

TABLE II. COMPARISON OF THE FC AND THE SA$_{MAX}$ OF OUR SOLUTION AND CONV-LBIST.

		s9234	s13207	s15850	s38417	s38584
#gates		2027	2573	3448	8709	11448
#FFs		211	638	534	1636	1426
# of scan chains		10	28	25	67	59
Conv-LBIST	FC (%)	85.57	94.01	93.01	92.95	93.92
	SA$_{MAX}$	148	385	344	895	799
LBIST with our solution	FC (%)	85.01	96.47	95.67	94.52	95.15
	ΔFC (%)	-0.7	2.6	2.9	1.7	1.3
	SA$_{MAX}$	76	195	174	449	402
	ΔSA$_{MAX}$ (%)	-48.6	-49.4	-49.4	-49.8	-49.7

Therefore, with respect to conventional scan-based LBIST, our solution allows to reduce considerably the PD, without impacting neither the FC, nor the test length.

As for area overhead, we evaluated it for the two largest benchmarks (i.e., the s38417 and the s38584 ones) as the relative area increase in the PS, due to the extra XOR gates that are needed to generate the missing past/future states in the PS. For the s38417 benchmark circuit, such an area overhead is +0.3%, while for the s3854 circuit, it is +1.8%. Therefore, the area increase required by our solution over the area of the whole LBIST architecture is negligible.

It is worth noticing that the increase in the layout complexity over conventional scan-based LBIST is negligible. In fact, since the additional circuitry required by our solution can be placed close to the PS, the layout of the signals from the PS to the scan chains is not significantly modified.

B Comparison with Alternative Solution

We have compared our solution with the alternative technique proposed in [2] in terms of: 1) SA_{MAX} in the scan chains between following capture cycles; 2) number of test vectors (#TV) required to achieve a target FC. For comparison purposes, we have considered the same benchmarks and implementation of our solution as in the previous subsection. As for the solution in [2], it has been implemented considering two scan-chain groups (i.e., the case of N=2 described in [2]), thus allowing to obtain a value of SA_{MAX} similar to that obtained with our approach.

The results of the performed comparison are summarized in Table III, where the relative variations of SA_{MAX} and #TV are calculated as: $\Delta SA_{MAX} = 100*(SA_{MAX\ OUR} - SA_{MAX\ [2]}) / SA_{MAX\ [2]})$, and $\Delta \#TV = 100 * (\#TV_{OUR} - \#TV_{[2]}) / \#TV_{[2]}$.

As can be seen, to achieve the same FC, the compared solutions present a similar SA_{MAX}, thus both allowing to reduce significantly the PD with respect to Conv-LBIST. However, the solution in [2] requires more than twice (in the best case) the number of test vectors required by both our approach and by Conv-LBIST. Therefore, our solution allows to reduce significantly the total test time with respect to [2], while achieving the same FC and a similar PD reduction.

VI. CONCLUSIONS

We have presented a novel approach to reduce peak power and power droop during the capture cycles in scan-based Logic BIST, thus reducing the probability that the induced delay effect is erroneously recognized as presence of a delay fault, with consequent erroneous generation of a test fail. We showed that our approach allows to reduce by approximately 50% the switching activity (SA) in the scan chains between following capture cycles, with respect to standard scan-based LBIST. This is achieved by exploiting the operation of the phase shifter, usually inserted in LBIST structures in order to reduce the correlation among the test patterns applied to adjacent scan-chains. We also showed that our approach requires a significantly lower test time compared to the alternative, recent technique in [2]. The proposed approach exhibits no impact on test coverage and test time, while requiring a very low cost in

TABLE III. COMPARISON OF THE FAULT COVERAGE (FC), NUMBER OF TEST VECTORS (#TV) TO ACHIEVE A TARGET FC, AND MAXIMUM SWITCHING ACTIVITY (SAMAX) OF OUR APPROACH AND THE SOLUTION IN [2].

		s9234	s13207	s15850	s38417	s38584
Target FC % [2]		85.64	96.8	91.71	95.37	95.24
Solution in [2]	#TV	37000	54500	29500	80500	49000
	SA_{MAX}	81	215	195	465	423
LBIST with our solution	#TV	15505	14006	2514	21534	18496
	Δ#TV (%)	-58	-74	-91	-73	-62
	SA_{MAX}	76	195	174	449	402
ΔSA_{MAX} (%)		-6.2	-9.3	-10.8	-3.4	-5

terms of area overhead. Moreover, it is fully compatible with standard scan-based LBIST architectures.

REFERENCES

[1] P. Girard, et al., "A Modified Clock Scheme for a Low Power BIST Test Pattern Ggenerator" in *Proc. of IEEE VLSI Test Symp.*, 2001, pp. 306 – 311.

[2] S. M. Reddy, et al., "A Low Power Pseudo-Random BIST Technique", in *Proc. of IEEE Int.l On-Line Testing Workshop*, 2002, pp. 140 – 144.

[3] M.Tehranipoor, M. Nourani, N. Ahmed, "Low Transition LFSR for BIST-Based Applications", in Proc. of 14th Asian Test Symp., 2005, pp. 138 – 143.

[4] Y. Huang, X. Lin, "Programmable Logic BIST for At-Speed Test", in Prco. of 16th Asian Test Symp., 2007, pp. 295 – 300.

[5] I. Polian, A. Czutro, S. Kundu, B. Becker, "Power Droop Testing", IEEE Design & Test of Computers 24(3), 2007, pp. 276 – 284.

[6] M. Nourani, et al., "Low-Transition Test Pattern Generation for BIST-Based Applications", *IEEE Trans. on Comp.*, Vol. 57, No. 3, March 2008, pp. 303 – 315.

[7] X. Lin, E. Moghaddam, N. Mukherjee, J. Tyszer, "Power Aware Embedded Test", in Proc. of IEEE Asian Test Symp., 2011, pp. 511 – 516.

[8] Y. Sato, S. Wang, T. Kato, Kohei Miyase, S. Kajihara, "Low Power BIST for Scan-Shift and Capture Power", in Proc. of IEEE Asian Test Symp., 2012, pp. 173 – 178.

[9] X. Wen, Y. Yamashita, S. Kajihara, L-T. Wang, K. Saluja, K. Kinoshita, "On Low-Capture-Power Test Generation for Scan Testing", in Proc. of IEEE VLSI Test Symp., 2005, pp. 265 – 270.

[10] E. Moghaddan, J. Rajski, S. Reddy, "At-Speed Scan Test with Low Switching Activity", in Proc. of IEEE VLSI Test Symp., 2010, pp. 177 – 182.

[11] L-T Wang, C. Stroud, N. Touba, "System-on-Chip Test Architectures: Nanometer Design for Testability", Morgan kaufmann, San Francisco, Nov. 2007.

[12] G. Hetherington, T. Fryars, N. Tamarapalli, M. Kassab, A. Hassan, J. Rajski, "Logic BIST for Large Industrial Designs: Real Issues and Case Studies", in Proc. of Int. Test Conference, 1999, pp. 358 – 367.

[13] P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, J. Figueras, S. Manich, P. Texeira, M. Santos, "Low-Energy BIST Design: Impact of the LFSR TGP Parameters on the Weighted Switching Activity", in *Proc. of IEEE Int'l Symp. on Circuits and Syst.*, 1999, pp. 110 – 113.

[14] B. Nadeau-Dostie, K. Takeshita, J.-F. Cote, "Power-Aware At-Speed Scan Test Methodology for Circuits with Synchronous Clocks", in Proc. of *IEEE Int'l Test Conference*, 2008, paper 9.3.

[15] J. Rajski, N. Tamarapalli, J. Tyszer, "Automated Synthesis of Large Phase Shifters for Built-In Self-Test", in Proc. of Int. Test Conference, 1998, pp. 1047 – 1056.

[16] A. Mishra, N. Sinha, Satdev, V. Singh, S. Chakravarty, A. D. Singh, "Modified Scan Flip-Flop for Low Power Testing", in Proc. of Asian Test Symposium, 2010, pp. 367 – 370.

[17] www.xilinx.com/support/documentation/application_notes/xapp052.pdf