

# Ten Times Faster: Error correction at the speeds required for 5G mobile telephony

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## Introduction

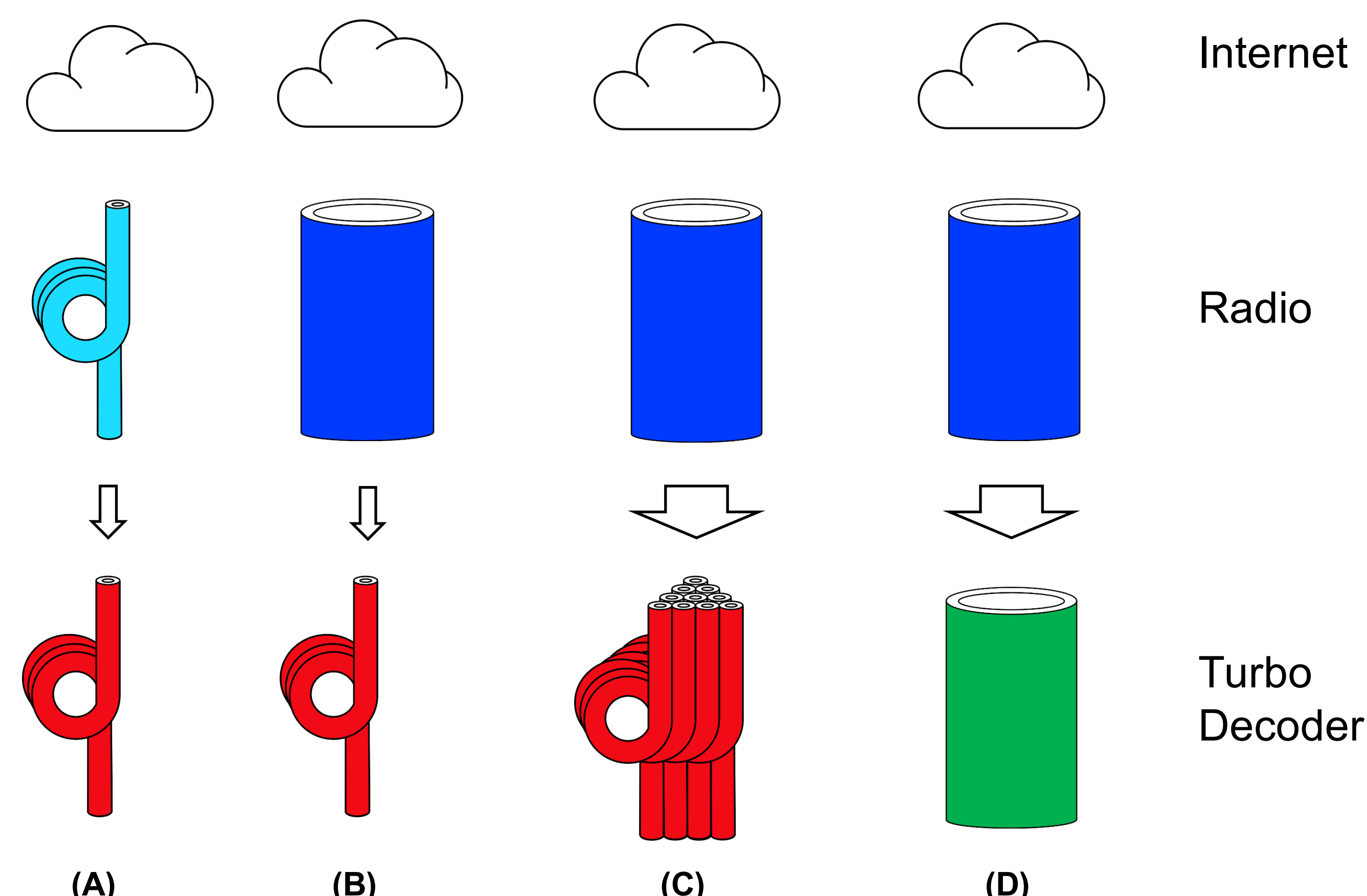
- Turbo decoders are used in 3G and 4G mobile telephony for correcting communication errors caused by poor signal quality.
- Compared to 4G, the target for 5G is to achieve ten times reductions in download times and in the lag experienced in video chat and online games.
- However, **conventional turbo decoders** are not fast enough to meet both of these requirements, even when many of them work together.

- This is because the data-dependencies within the **conventional turbo decoder** require each of its steps to be performed one-at-a-time and in the correct order.
- This invention is the world's first general-purpose **fully-parallel turbo decoder**, which breaks the data dependencies and allows the steps to be performed at the same time.
- For the first time, our **fully-parallel turbo decoder** is fast enough to meet the requirements of 5G.

## Analogy

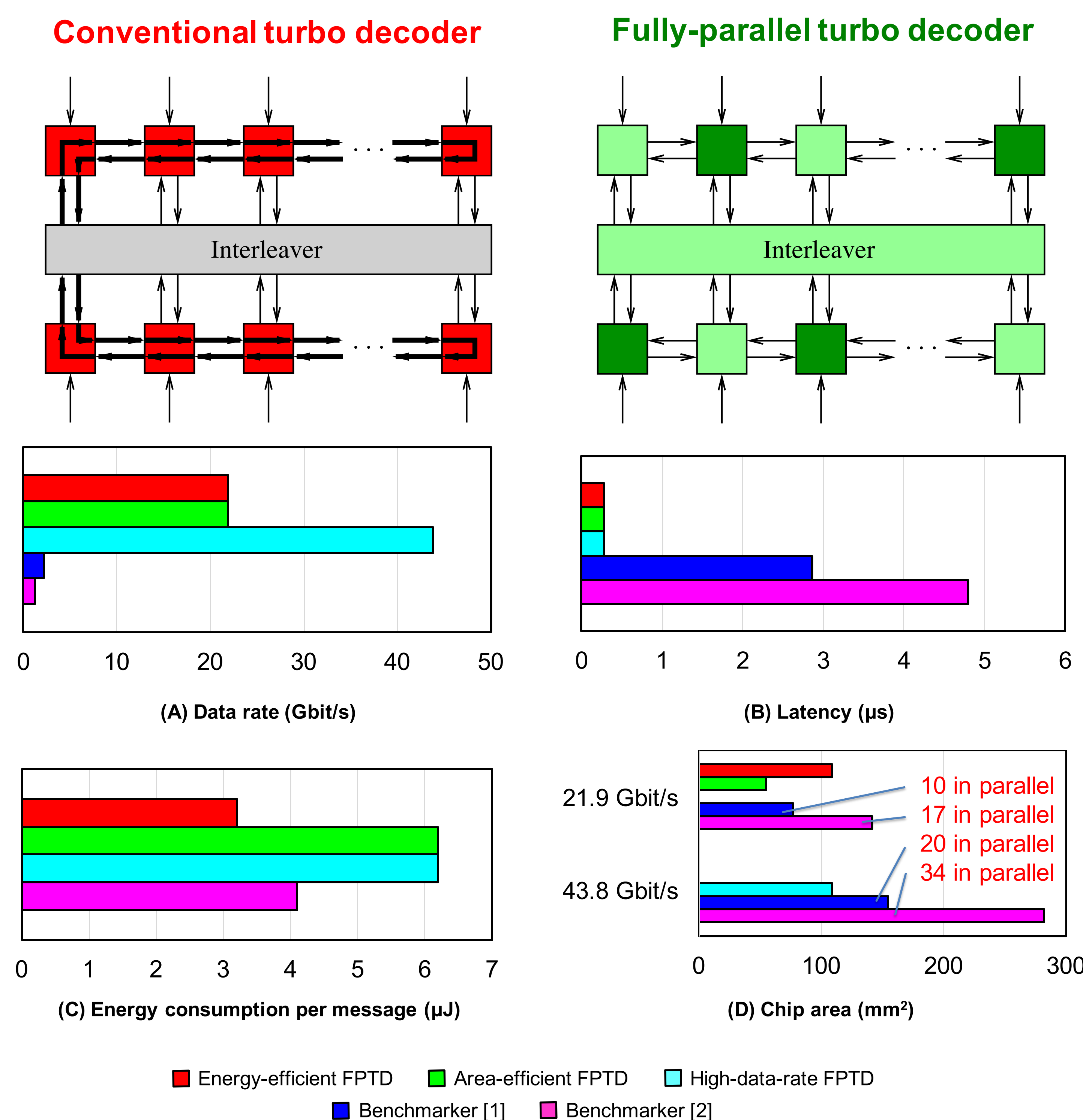
- The radio and turbo decoder parts of 4G and 5G systems each have associated data rates and latencies, which can be represented by pipes:
  - Data rate - Wider pipes allow more information to flow per second, reducing download times;
  - Latency - Shorter pipes deliver the information to the other end with less delay, reducing lag in video chat and on-line games.

- 4G radio** and **conventional turbo decoder**. This has a peak data rate of **1 Gbit/s** and a latency of **10 ms**.
- 5G radio** and **conventional turbo decoder**. The latter bottlenecks peak data rate to **1 Gbit/s** and latency to **10 ms**.
- 5G radio** and multiple **conventional turbo decoders**. This removes the data rate bottleneck, giving **10 Gbit/s**, but does not remove the latency bottleneck of **10 ms**.
- 5G radio** and **fully-parallel turbo decoder**. Only this gives the desired peak data rate of **10 Gbit/s** and latency of **1 ms**.



## Technical Perspective

- Conventional turbo decoder**
  - Data dependencies require blocks to be operated one-at-a-time, in the order indicated by the bold arrows in the schematic to the right.
  - 100s or 1000s of clock cycles are required to decode each message.
- Fully-parallel turbo decoder**
  - Blocks having the same shading in the schematic to the right are operated at the same time.
  - Only 10s of clock cycles are required to decode each message.
  - Energy-efficient version** decodes one message at a time:
    - Light blocks operate in odd clock cycles;
    - Dark blocks operate in even clock cycles.
  - Area-efficient version** decodes one message at a time:
    - Reuses hardware for light and dark blocks in alternate clock cycles.
  - High-data-rate version** decodes two messages at the same time:
    - Light blocks decode 1st message in odd clock cycles, while dark blocks decode 2nd message;
    - Light and dark blocks swap messages in even clock cycles.
- ASIC Performance** in comparison with Benchmarkers [1] and [2]:
  - Data rate** – better than 10 times higher;
  - Latency** – better than 10 times lower;
  - Energy efficiency** – up to 20% lower;
  - Area efficiency** – up to 30% lower.



- FPGA performance** – up to 7 times faster.
- GPGPU performance** – up to 3 times faster.

## Commercialisation

- We have patented this technology [3], published a paper [4] and produced a marketing video [5].
- We are participating in the SETSquared Innovation to Commercialisation of University Research Programme (ICURE)

- We are seeking industrial partners to help us commercialise:
  - Manufacturers of basestations;
  - Manufacturers of specialist wireless system;
  - Vendors of soft-IP.
- Contact: David Woolley, Technology Transfer Manager, University of Southampton, [dw1@soton.ac.uk](mailto:dw1@soton.ac.uk), 023 8059 8341

## References

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