Modelling Approaches for DC-DC Converters With Switched Capacitors

J.C. Mayo-Maldonado, *Student Member*, *IEEE*, J.C. Rosas-Caro, *Member*, *IEEE* and P. Rapisarda

***Abstract*—In this paper we review relevant problems in the modelling of DC-DC converters with switched capacitors. We study several approaches that overcome the exposed modelling difficulties, addressing ideal and non-ideal cases and using dynamic equations that are valid in a large signal domain.**

***Index Terms*—Averaging, DC-DC converters, modelling, switched capacitors; switched systems.**

I. Introduction

Switched capacitor (SC) converters offer several advantages such as light weight, small size, high power density and large voltage conversion ratios [1], which results important for a large number of applications (see e.g. recent developments in [2], [3], [4], [5], [6]). For these reasons, increased interest has been given to their design, modelling and control. Many control techniques for power converters are based on nonlinear models, see for instance the extensive compendium of control techniques presented in [7]. Such models and consequently their associated nonlinear controllers are able to perform well in wide ranges of operation compared with linearised models. However, the conventional approach for the regulation of SC based converters is a linear feedback control that is based on approximate small-signal linearised models of the circuit topologies. In some applications, this approach does not make the converters able to respond well to requirements of regulation in the presence of a wide range of input voltages and load variations [8].

Different approaches have been proposed for the modelling of SC converters, such as incremental graph approaches [9], useful for determining steady state voltage gains. In [10], [11], [12], approaches for modelling SC are given by considering the inherent losses produced when capacitors are connected in parallel. A steady state modelling approach is provided [13] in which SC converters are analysed by considering equivalent output impedances. The approach in [14] provides state-space models by solving numerically the loss equations depending on the position of the switches. The results are used to calculate the steady state gain and a steady state equivalent resistance. Approaches considering ideal switches and consequently, discontinuities on the voltages across capacitors have been discussed in [15], [16]. Parasitic resistances have played also an important role in the study the dynamic performance of SC converters [17], since energy losses during charge/discharge processes permit the elaboration of accurate dynamic models (see [11],[18],[19],[20]).

In this paper we gather and discuss theory and principles regarding the operation of SC converters. Moreover, we present a systematic exposition of three modelling approaches for DC-DC converters with SCs. The procedures are illustrated using a *Fibonacci SC converter* obtained from [21] and the *three switch high-voltage converter* proposed in [22]. The methods are similar to the classical averaging techniques that consider equivalent circuits depending on the position of the switches. However, instead of using the real ESR lumped in the circuit (see for instance [8],[23]), we consider: 1) the case with ideal switches where discontinuous signals are allowed, 2) an average loss modelling based on the results provided in [18], and 3) a reduced order model based on a voltage balancing property.

II. Preliminaries

Power electronics devices with two linear dynamic modes and ideal switches can be modelled using the following switched linear system structure (see [24], [25])

$$\frac{d}{dt}x = A_u x + B_u \ ; \ u = 0, 1 \ ; \tag{1}$$

where $x(t) \in \mathbb{R}^{n\times 1}$ is called the state function; $A_u \in \mathbb{R}^{n\times n}$, $B_u \in \mathbb{R}^{n\times 1}$ are the matrices that define the physical laws of the dynamic modes, and $u = 0, 1$, a binary index term that denotes which of the two modes is active according to a specified switching signal. If we assume that the switching signal is periodic and that the trajectories of the system variables are everywhere continuous, we can approximate the dynamics of

J.C. Mayo-Maldonado and P. Rapisarda are with the CSPC group, School of Electronics and Computer Science, University of Southampton, Great Britain, e-mail: jcmm1g11,pr3@ecs.soton.ac.uk, Tel: +(44)2380593367, Fax: +(44)2380594498. J.C. Rosas-Caro is with Universidad Panamericana Campus Guadalajara, Mexico.

the switched linear system into averaged quantities by considering a *duty cycle* denoted by D. This action is equivalent to approximate a switched linear system into a nonlinear system where the so-called current and voltage ripples of the converter are neglected. The *averaging technique* allow us to obtain the following structure

$$\frac{d}{dt}x_{av} = [DA_0 + (1-D)A_1]\, x_{av} + DB_0 + (1-D)B_1 \; ; \tag{2}$$

where $x_{av}(t) \in \mathbb{R}^{n\times 1}$ is the averaged state function. When we consider the duty cycle D as an input, the averaged system can be conveniently written in *state affine nonlinear form* $\frac{d}{dt}x_{av} = f(x_{av}) + g(x_{av})D$; with $f(x_{av}) := A_1 x_{av} + B_1$ and $g(x_{av}) := (A_0 - A_1)x_{av} + B_0 - B_1$. The latter structure is usually the starting point for the dynamic analysis and control of DC-DC converters, since it can be derived almost directly from the switched linear system structure (1) and it allows to apply a wide number of nonlinear control techniques (see for instance the compendium of controllers in [7]). Unfortunately, as we will expose in the following section, the traditional averaging technique cannot be applied to systems with discontinuous trajectories, as it is the case of switched-capacitor converters. In other words, the parallel connection between capacitors, which is the main feature of such converters, produces discontinuities on the voltages across their terminals at switching instants. In mathematical terms, such situation is derived from the introduction of algebraic constraints to the dynamic modes of the converter. Consequently, an averaged state affine nonlinear model cannot be directly obtained. In order to overcome this issue, we study several modelling alternatives for this type of converters.

III. Modelling approaches

In order to discuss the modelling procedures, we consider the *Two-phase Fibonacci SC converter* depicted in Fig. 1, corresponding to a simplified version[1] of the SC converter in Fig. 1(b) of [21]. We aim at showing a detailed exposition that provides sufficient insight to extend the discussed approaches to other topologies with SCs.

The converter in Fig. 1(a) has two possible modes depending on the position of the group of switches "1" and "2" illustrated by blocks and whose operation is complementary. Fig. 1(b) and Fig. 1(c) show the two possible equivalent circuits of the converter.

[1]For ease of exposition, the third "Fibonacci cell" of the SC converter in Fig. 1(b) of [21] has been omitted, and a parallel RC load is considered.

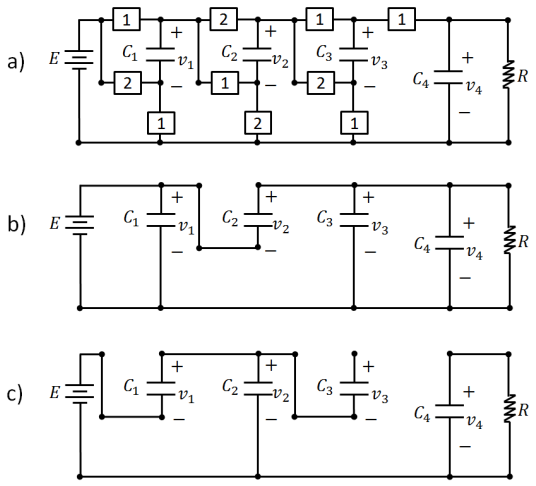

Fig. 1. Fibonacci switched-capacitor converter: (a) Full schematic; Equivalent circuits when (b) the switches "1" are closed and when (c) the switches "2" are closed.

A. Dynamic modelling with ideal switches

In order to describe the dynamics of the converter considering ideal switches, we proceed as usual; we model the dynamic modes for each equivalent circuit using current and voltage laws. Let us consider the case in Fig. 1(b). We obtain the following set of equations

$$\Sigma_1 : \begin{cases} v_1 - E = 0 \; , \\ v_1 + v_2 - v_3 = 0 \; , \\ v_3 - v_4 = 0 \; , \\ C_2\dfrac{d}{dt}v_2 + (C_3 + C_4)\dfrac{d}{dt}v_4 + \dfrac{v_4}{R} = 0 \; . \end{cases} \tag{3}$$

Moreover, the set of equations corresponding to the circuit in Fig. 1(c), are the following

$$\Sigma_2 : \begin{cases} v_1 - v_2 + E = 0 \; , \\ C_1\dfrac{d}{dt}v_1 + C_2\dfrac{d}{dt}v_2 = 0 \; , \\ C_3\dfrac{d}{dt}v_3 = 0 \; , \\ C_4\dfrac{d}{dt}v_4 + \dfrac{v_4}{R} = 0 \; . \end{cases} \tag{4}$$

Note that since the switching produces parallel connections among the capacitors and the source, there exist algebraic equations expressing the corresponding equalities for their voltages. As studied in the previous section, when we model standard power converters, the following step usually consists in obtaining one single set of equations by considering the duty cycle and the average value of the state variables as in equation (2). However, if we try to follow such a method, we find that the structure (2), which is based in a set of first order

differential equations, cannot be satisfied since zero-th order equations (i.e. algebraic constraints) are involved in the dynamics of the converter. Moreover, we eventually find two additional issues:

1. The voltages across capacitors are discontinuous at switching instants, i.e. there exist instantaneous "jumps" in the trajectories of the system variables.
2. The value of the voltages at the switching instants is not uniquely determined, i.e. there exist more than one possible consistent choice of initial conditions that satisfy the equations at switching instants.

Since the value of the capacitors need to be uniquely specified at switching instants, we consider a model addressing instantaneous values, instead of using the traditional averaging technique. We proceed to complete the dynamic model of the converter by introducing a *reset rule* for the system variables acting at the switching instants. In order to do so, we use the notation $f(t^-) := \lim_{\tau \nearrow t} f(\tau)$ and $f(t^+) := \lim_{\tau \searrow t} f(\tau)$, to define the limit of a time function taken from the left and from the right respectively.

In order to provide a realistic set of initial conditions at the switching instants, the reset must respect the "principle of conservation of charge" (cf. the redistribution of charge in [15], [19]). We proceed by considering the capacitors whose voltage is subject to algebraic constraints, for instance when we switch from Σ_2 to Σ_1, the total charge in the capacitors that exhibits a redistribution due to parallel connections must be the same before and after every switching instant t_s, i.e.

$$\begin{aligned} &C_2 v_2(t_s^-) + C_3 v_3(t_s^-) + C_4 v_4(t_s^-) \\ &= C_2 v_2(t_s^+) + C_3 v_3(t_s^+) + C_4 v_4(t_s^+) \, . \end{aligned}$$

Additionally, the algebraic constraints of Σ_1 dictate that $v_1(t_s^+) = E(t_s^+)$, $v_2(t_s^+) = v_3(t_s^+) - v_1(t_s^+)$, $v_3(t_s^+) = v_4(t_s^+)$.

After straightforward algebraic manipulations and assuming without loss of generality that the voltage E is constant (and consequently $E(t_s^-) = E(t_s^+)$), we obtain the following reset rule

$$\begin{bmatrix} E(t_s^+) \\ v_1(t_s^+) \\ v_2(t_s^+) \\ v_3(t_s^+) \\ v_4(t_s^+) \end{bmatrix} = \frac{1}{C_{e_1}} \begin{bmatrix} C_{e_1} & 0 & 0 & 0 & 0 \\ C_{e_1} & 0 & 0 & 0 & 0 \\ -C_3 - C_4 & 0 & C_2 & C_3 & C_4 \\ C_2 & 0 & C_2 & C_3 & C_4 \\ C_2 & 0 & C_2 & C_3 & C_4 \end{bmatrix} \begin{bmatrix} E(t_s^-) \\ v_1(t_s^-) \\ v_2(t_s^-) \\ v_3(t_s^-) \\ v_4(t_s^-) \end{bmatrix} , \quad (5)$$

where $C_{e_1} = C_2 + C_3 + C_4$. Similarly, when we switch from Σ_1 to Σ_2, the physical redistribution of charge establishes that for every switching instant t_s we have that

$$C_1 v_1(t_s^-) + C_2 v_2(t_s^-) = C_1 v_1(t_s^+) + C_2 v_2(t_s^+) \, .$$

which together with the algebraic constraint $v_2(t_s^+) - v_1(t_s^+) = E(t_s^+) = E(t_s^-)$, we can determine the reset rule

$$\begin{bmatrix} E(t_s^+) \\ v_1(t_s^+) \\ v_2(t_s^+) \\ v_3(t_s^+) \\ v_4(t_s^+) \end{bmatrix} = \frac{1}{C_{e_2}} \begin{bmatrix} C_{e_2} & 0 & 0 & 0 & 0 \\ -C_2 & C_1 & C_2 & 0 & 0 \\ C_1 & C_1 & C_2 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} E(t_s^-) \\ v_1(t_s^-) \\ v_2(t_s^-) \\ v_3(t_s^-) \\ v_4(t_s^-) \end{bmatrix} , \quad (6)$$

where $C_{e_2} = C_1 + C_2$.

The voltage ripples of the converter using equations[2] (4)-(6) and a periodic switching signal are shown in Fig. 2. Note that the discontinuous voltages are concatenated via the reset rules after the switch.

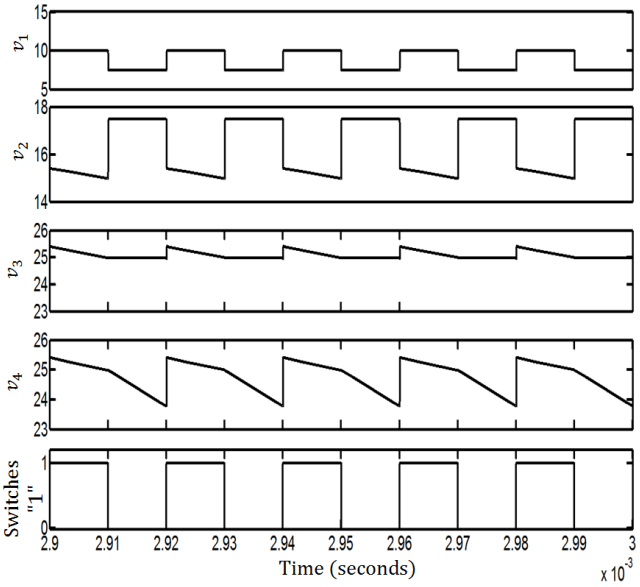

Fig. 2. Voltage ripples of the Fibonacci SC converter.

Equations (4)-(6) represent an alternative dynamic model based on instantaneous values for the discussed SC converter. Note also that the model describes dynamics in a large signal domain.

Remark 1. The presented approach allows to study the dynamics of the SC converters in the sense of switched linear systems (see e.g. [24], [25], [26]). Consequently, their overall dynamic properties such as stability, stabilisability and control can be studied in this setting.

Remark 2. Note that the need to specify reset rules corresponds to a more general dynamic modelling approach than that of traditional converters whose trajectories are continuous at switching instants. For instance, in the case of the switched linear system in equation (1), it is assumed that $x(t_s^-) = x(t_s^+)$ and consequently, the matrices associated to the reset rules are trivially equal to the identity.

[2]For this simulation, we used the parameters specified in Sec. III-3.

B. Average losses-based modelling

The study of the large signal dynamics of SC converters considering averaged quantities can be performed in the nonlinear systems setting by considering non-ideal switches. In this case, the issue regarding voltage discontinuities vanishes.

We now discuss the concept of average dynamic modelling with non-ideal switches. The approach has been studied in detail in [18] for the modelling of purely capacitor-based converters and in [20] for a hybrid multiplier converter. Such approach applies the method of average current between capacitors in parallel, rather than the use of instantaneous values. The method is first discussed in relation to Fig. 3(a) in which a capacitor C_1 is connected via a switch S to a second capacitor C_2, while the initial voltages across capacitors C_1 and C_2 are different, i.e. $V_2(0) \neq V_1(0)$.

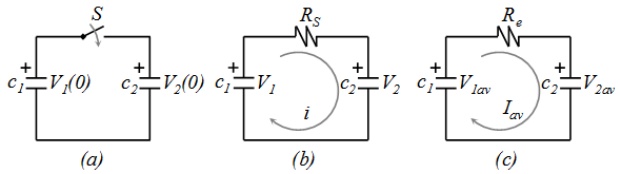

Fig. 3. Electric diagram of a simple SC circuit and its equivalent circuits.

When the switch is closed, assuming $V_1(0) > V_2(0)$, an electrical current flow from C_1 to C_2. The shape of the charging/discharging current will depend on the total loop resistance R_s, see Fig. 3(b), which consists of the sum of the switch resistance and capacitors' ESR. Hence, the actual circuit can be described by Fig. 3(b). The instantaneous circuit of Fig. 3(b) can be converted into an average equivalent form by calculating the power loss of the circuit in Fig. 3(b). The intuition behind this method is to obtain an *off-line* expression derived from the computation of the average amount of dissipated energy according to the duty cycle of the converter, then such expression is associated to the value of a *variant equivalent series resistor*. The time domain solution of the energy loss P dissipated by the loop resistor R_s in Fig. 3, can be expressed in terms of decaying exponentials as (see [18], p. 3343)

$$P = \frac{I_{av}^2}{2 f_s C_e}\left(\frac{1+e^{-\beta}}{1-e^{-\beta}}\right) , \tag{7}$$

where $\beta := (DT_s)/(R_s C_e)$, f_s is the switching frequency, I_{av} is the average current of the circuit (over the switching period $T_s = 1/f_s$), D the duty cycle that sets the charge/discharge time period DT_s (when switch S in Fig. 3(a) is closed), for the circuit in Fig. 3(b), and $C_e = (C_1 C_2)/(C_1 + C_2)$ is the equivalent capacitance. From the above equation, considering average values, an the equivalent resistance R_e of the circuit can be defined as a function of the duty cycle, i.e. $R_e : [0,1] \to \mathbb{R}$, where

$$R_e(D) := \frac{1}{2 f_s C_e}\left(\frac{1+e^{-\beta}}{1-e^{-\beta}}\right) , \tag{8}$$

with $\beta = (DT_s)/(R_s C_e)$.

Remark 3. In [27], it has been determined that the value of the dissipated power (7) in steady state is bounded by the *Slow/Fast Switching Limits*, corresponding respectively to the dissipated power considering ideal switches and the absence of parasitic resistances; and to the case when non ideal elements appear and the switching frequency is fast enough to consider constant voltages across capacitors during the switching period.

We can conclude that the average behaviour of the circuit can be described by the average model of Fig. 3(c) in which voltages and currents are assumed to be constant within the switching period T_s, which is consistent with the concept of average models. In this basic circuit, the average current I_{av} can be expressed as,

$$I_{av} = \frac{V_{1av} - V_{2av}}{R_e(D)} .$$

Following the losses-based averaging technique discussed above, we obtain the following set of equations for the Fibonacci SC converter in Fig. 1 by applying current laws with respect to each capacitor

$$\Sigma_{\text{loss}} : \begin{cases} C_1 \dfrac{d}{dt} V_{1av} = \dfrac{E - V_{1av}}{R_{e_1}(D)} - \dfrac{E + V_{1av} - V_{2av}}{R_{e_3}(D)} \\ \qquad\qquad - \dfrac{V_{1av} + V_{2av} - V_{3av}}{R_{e_2}(D)} , \\ C_2 \dfrac{d}{dt} V_{2av} = \dfrac{E + V_{1av} - V_{2av}}{R_{e_3}(D)} \\ \qquad\qquad - \dfrac{V_{1av} + V_{2av} - V_{3av}}{R_{e_2}(D)} , \\ C_3 \dfrac{d}{dt} V_{3av} = \dfrac{V_{1av} + V_{2av} - V_{3av}}{R_{e_2}(D)} \\ \qquad\qquad - \dfrac{V_{3av} - V_{4av}}{R_{e_4}(D)} , \\ C_4 \dfrac{d}{dt} V_{4av} = \dfrac{V_{3av} - V_{4av}}{R_{e_4}(D)} - \dfrac{V_{4av}}{R} . \end{cases} \tag{9}$$

with

$$R_i(D) := \frac{1}{2 f_s C_{e_i}}\left(\frac{1+e^{-\beta_i}}{1-e^{-\beta_i}}\right) \; ; \; \beta_i = \frac{DT_s}{R_{s_i} C_{e_i}} \; ;$$

where R_{s_i}, C_{e_i}, $i = 1, ..., 4$, are the total resistance and capacitance respectively of the loops where the average currents are analysed.

Remark 4. The dynamic model (9) presents several advantages: 1) The model describes the dynamics of the converter in a large-signal domain. 2) The averaged equations permit the computation of the converter gain in a standard way, i.e. we can consider the derivative of the state variables to be equal to zero, and after straightforward computations it follows that $V_{3av} \approx 3E$ where the approximation accounts the power losses of the circuit. 3) The model is able to capture additional situations including: complete charging, partial charging and no effective charging; depending on the ratio $(DT_s)/(R_sC_e)$ (cf. [18]).

Remark 5. The main disadvantage of the presented model is its very high nonlinear structure. Due to this issue, standard nonlinear control techniques that have been set up for state affine nonlinear systems as in equation (2) cannot be applied in a straightforward way using this type of models and a more sophisticated mathematical treatment is required. Moreover, the accurate estimation of the equivalent loop resistances R_s may not be an easy task, however a detailed exposition of the modelling of non-ideal elements in SC loops including non-ideal switches has been provided in [18].

C. Simulation results

In Fig. 4, we show the comparison between the circuit-based simulation of the output voltage v_4 the SC converter in Fig. 1 using the software `Synopsys Saber`, and that of the simulations of the model with ideal switches in (4)-(6) and the average power loss-based model in (9) using `Matlab`. We consider the parameters $E = 10V$, $f_s = 50kHz$, $C_1 = C_2 = C_3 = C_4 = 10\mu F$ and $R = 100\Omega$. The total loop resistances are $R_{s_1} = 0.21\Omega$, $R_{s_2} = 0.043\Omega$, $R_{s_3} = 0.032\Omega$, $R_{s_4} = 0.022\Omega$, which are for this case the sum of the *switch on* resistances $R_{sw} = 0.01\Omega$ of the transistors and the capacitors ESR $R_c = 0.001\Omega$, i.e. $R_{s_1} = 2R_{sw} + R_c$, $R_{s_2} = 4R_{sw} + 3R_c$, $R_{s_3} = 3R_{sw} + 2R_c$, and $R_{s_4} = 2R_{sw} + 2R_c$.

Remark 6. The simulation shows that both, the discontinuous and the average power loss-based models provide reliable information regarding the dynamics of the circuit. Since both the switched linear- and the nonlinear- systems frameworks offer powerful tools for dynamic analysis and control, the selection of the more appropriate approach relies on the application, i.e. where either instantaneous or averaged values can be of special interest.

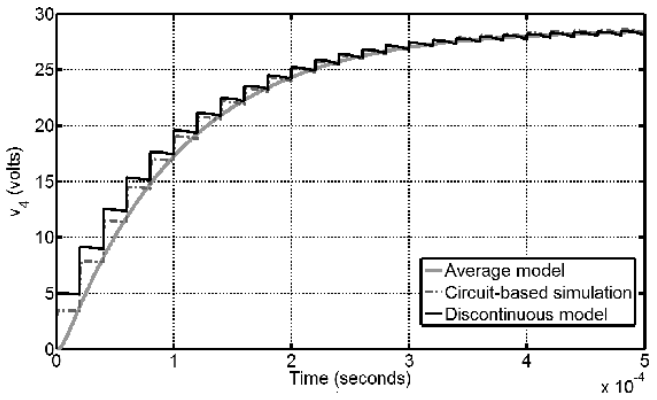

Fig. 4. Comparison of the output voltage "v_4" simulation and the proposed dynamic models.

IV. Dynamic modelling of hybrid converters

SCs can be also combined with inductor/capacitor stages that are not necessarily of discontinuous nature, we call these type of topologies *hybrid SC converters*. An example of a hybrid topology is the *three switch high-voltage converter* depicted in Fig. 5, that was firstly proposed in [22] and recently used for current-ripple cancellation topologies [28]. Although the topology presents a basic principle of operation and a reduced number of components, only its small-signal dynamic model is available in the literature (see [22]). According to the material discussed in the previous sections, we show two large-signal dynamic models for the three switch high-voltage converter. The model with ideal switches derived from the material in Sec. III-A encompasses the following modes according to the equivalent circuits in

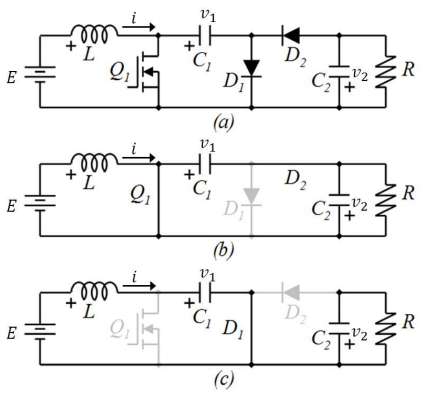

Fig. 5. Three Switch High Voltage Converter: (a) Full schematic; Equivalent circuits when (b) the switch is closed and (c) the switch is open.

Fig. 5(b) and Fig. 5(c) respectively.

$$\Sigma_1 := \begin{cases} L\dfrac{d}{dt}i = E - v_1 \ , \\ C_1\dfrac{d}{dt}v_1 = i \ , \\ C_2\dfrac{d}{dt}v_2 = -\dfrac{v_2}{R} \ . \end{cases}$$

$$\Sigma_2 : \begin{cases} L\dfrac{d}{dt}i = E \ , \\ (C_1+C_2)\dfrac{d}{dt}v_1 = -\dfrac{v_1}{R} \ , \\ v_2 = v_1 \ . \end{cases}$$

The reset rule when we switch from Σ_2 to Σ_1 at t_s is given by

$$\begin{bmatrix} E(t_s^+) \\ i(t_s^+) \\ v_1(t_s^+) \\ v_2(t_s^+) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} E(t_s^-) \\ i(t_s^+) \\ v_1(t_s^-) \\ v_2(t_s^-) \end{bmatrix} \ ,$$

Similarly, when we switch from Σ_1 to Σ_2 at t_s we have

$$\begin{bmatrix} E(t_s^+) \\ i(t_s^+) \\ v_1(t_s^+) \\ v_2(t_s^+) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & \frac{C_1}{C_1+C_2} & \frac{C_2}{C_1+C_2} \\ 0 & 0 & \frac{C_1}{C_1+C_2} & \frac{C_2}{C_1+C_2} \end{bmatrix} \begin{bmatrix} E(t_s^-) \\ i(t_s^+) \\ v_1(t_s^-) \\ v_2(t_s^-) \end{bmatrix} \ .$$

Applying the the power-loss based modelling in Sec. III-B we obtain the following set of average nonlinear dynamic equations for the converter in Fig. 5.

$$\Sigma_{\text{Av}} : \begin{cases} L\dfrac{d}{dt}I_{Lav} = V_{in} - (1-D)V_{1av} \ , \\ C_1\dfrac{d}{dt}V_{1av} = (1-D)I_{av} \\ \qquad\qquad - 2f_sC_e\left(\dfrac{1-e^{-\beta}}{1+e^{-\beta}}\right)(V_{1av}-V_{2av}) \ , \\ C_2\dfrac{d}{dt}V_{2av} = -\dfrac{V_{2av}}{R} \\ \qquad\qquad + 2f_sC_e\left(\dfrac{1-e^{-\beta}}{1+e^{-\beta}}\right)(V_{1av}-V_{2av}) \ . \end{cases} \tag{10}$$

with $\beta = (DT_s)/(R_sC_e)$, where R_s is the total loop resistance between the SCs and $C_e = (C_1C_2)/(C_1+C_2)$.

Moreover, a particular property in hybrid SC converters allow us to propose a third modelling method based on a reduced order approximation. This method offers additional structural advantages with respect to the previously discussed approaches, such as basic mathematical representations, i.e. allowing standard state affine nonlinear forms, and a reduced number of equations. In order to obtain such model, we recall the *voltage balancing property* (cf. [23],[29]). The intuition behind this method is to exploit the fact that the dynamics of the SCs are much faster than those of the overall converter, consequently a zero-th order approximation on the voltages across the SCs is used. Consider the SC sub-circuit in Fig. 3(c) which shows an equivalent circuit that considers the average current between capacitors. In such circuit, the magnitude of the equivalent resistor R_e may vary arbitrarily by modifying the duty cycle or the switching period. Moreover, from equation (8) we can conclude that at higher frequencies, the average losses inherent in the SCs decrease and the voltage across capacitors tends to be constant during the switching period T_s (see [30]). Consequently, the voltage across C_1 and C_2 tend to be the same with the average difference being the voltage across the resistor R_e, i.e. $V_{1av} - V_{2av} = R_eI_{av}$ for the circuit in Fig. 3(c). In the case of the converter in Fig. 5, if we assume that the average voltage across capacitors C_1 and C_2 is the same, i.e. $V_{1av} = V_{2av}$, we automatically neglect the nonlinear terms associated to the power losses by considering the sum of the dynamic equations for C_1 and C_2 in (10). Thus we obtain the following reduced order average dynamic model

$$\Sigma_{\text{RO}} : \begin{cases} L\dfrac{d}{dt}I = E - (1-D)V_o \ , \\ (C_1+C_2)\dfrac{d}{dt}V_o = (1-D)I - \dfrac{V_o}{R} \ . \end{cases} \tag{11}$$

where I is the input current and V_o the output voltage (the voltage across C_2). The model provides an approximation with a reduced number of equations considering an ideal case (without losses), which can easily adopt the standard state affine nonlinear form (2). The "open loop" comparison of the output voltage considering the circuit simulation and equations (11) is depicted in Fig. 6. The parameters used for the simulations are $C_1 = C_2 = 50\mu F$, $R = 50\Omega$ and $L = 300\mu H$.

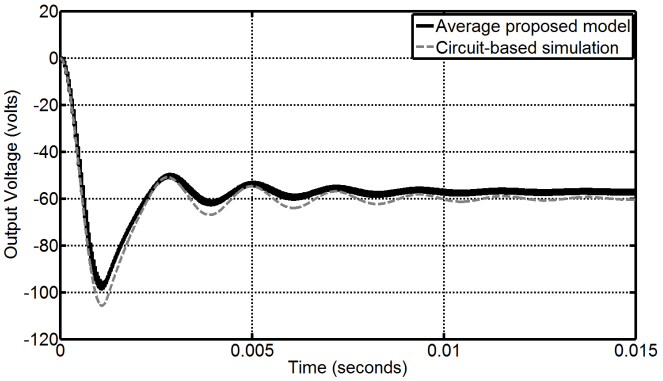

Fig. 6. Comparison of the output voltage "v_2" circuit simulation and the reduced order model.

Remark 7. Note that the reduced order model is based on the voltage-balancing assumption. Consequently, cases such as soft-switching (see e.g. [31]) can be considered as long as the assumption holds. However the introduction of new dynamic elements such as small series inductors will increase the differences in the dynamics on the voltages across switched capacitors, reducing the level of accuracy of the model.

Remark 8. Fig. 4 and Fig. 6 correspond to open-loop simulations of the circuit topologies and the proposed models. The simulations corroborate the "energy transfer" principles that have been studied in this paper and illustrates the discussed features of the proposed approaches. Closed-loop implementations can be used to test the discussed models under more challenging scenarios e.g. in the presence of arbitrary load and input voltage variations. However, since the theory and the technical issues that arise from those implementations are part of an important research area in control systems that needs to be studied in detail, we have reserved such theoretical developments for future work extensions.

We close this section by summarising the key features of the presented modelling approaches in Table I.

TABLE I
DYNAMIC MODELLING OF DC-DC CONVERTERS WITH SCS

Approach	Advantages	Disadvantages
Ideal Switches	Allows to study the current and voltage ripples in converters with switched capacitors.	Averaged signals are not considered, but discontinuous ones. Classic controllers for state affine nonlinear systems cannot be applied.
Power-losses	Averaged signals are obtained. Non-ideal switches are considered, thus a more accurate model is obtained.	Equivalent loop resistances need to be specified. Highly nonlinear structures are obtained, and standard nonlinear controllers cannot be applied.
Reduced-order (hybrid case)	Averaged signals are obtained. A reduced number of equations and a state affine nonlinear form is obtained.	The approximation neglects the converter losses and the switched capacitor dynamics.

V. CONCLUSIONS

We studied three modelling approaches for standard SC based DC-DC converters with two modes. The methods were illustrated using a Fibonacci SC converter and a three switch high voltage converter. The method discussed in Sec. III-A allows the study of the converter in a large signal domain allowing discontinuous signals, taking into account instantaneous values; the latter results convenient for the analysis of current and voltage ripples. The approach in Sec. III-B provides an average nonlinear model that captures non-ideal features such as power losses. Finally, the method in Sec. IV allows the use of basic nonlinear models with a reduced number of equations that results convenient for control purposes. Future research directions include the development of control techniques using the approaches discussed in this paper. Associated with the approach in Sec. III-A, new theoretical developments are under study, where issues such as *modularity*, i.e. the incremental development and combination of mode dynamics, are of special interest, see e.g. [26] and [32].

REFERENCES

[1] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits Syst. Mag.*, vol. 1, no. 3, pp. 37–42, 2001.

[2] E. Babaei and S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Trans. Ind. Electron.*, vol. 61, pp. 4614–4621, Sept 2014.

[3] M.-Y. Kim, C.-H. Kim, J.-H. Kim, and G.-W. Moon, "A chain structure of switched capacitor for improved cell balancing speed of lithium-ion batteries," *IEEE Trans. Ind. Electron.*, vol. 61, pp. 3989–3999, Aug 2014.

[4] Y.-S. Hwang, H.-H. Chou, Y.-B. Chang, and J.-J. Chen, "A high-efficiency DC-DC converter with wide output range using switched-capacitor front-end techniques," *IEEE Trans. Ind. Electron.*, vol. 61, pp. 2244–2251, May 2014.

[5] Y. Hinago and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, pp. 878–887, Feb 2012.

[6] S. Kiratipongvoot, S.-C. Tan, and A. Ioinovici, "Phase-shift interleaving control of variable-phase switched-capacitor converters," *IEEE Trans. Ind. Electron.*, vol. 60, pp. 5575–5584, Dec 2013.

[7] H. Sira-Ramirez and R. Silva-Ortigoza, *Control Design Techniques in Power Electronics Devices*. Springer-Verlag London, 2006.

[8] S.-C. Tan, S. Bronstein, M. Nur, Y. Lai, A. Ioinovici, and C. Tse, "Variable structure modeling and design of switched-capacitor converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 9, pp. 2132–2142, 2009.

[9] M. Makowski, "On systematic modeling of switched capacitor dc-dc converters: Incremental graph approach," in *IEEE 12th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–6, June 2010.

[10] S. Ben-Yaakov, "Behavioral average modeling and equivalent circuit simulation of switched capacitors converters," *IEEE Trans. Power Electron.*, vol. 27, pp. 632–636, Feb 2012.

[11] S. Ben-Yaakov, "On the influence of switch resistances on switched-capacitor converter losses," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 638–640, 2012.

[12] H.-P. Le, S. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor dc-dc converters," *IEEE J. Solid-State Circuits*, vol. 46, pp. 2120–2131, Sept 2011.

[13] J. Henry and J. Kimball, "Switched-capacitor converter state model generator," *IEEE Trans. Power Electron.*, vol. 27, pp. 2415–2425, May 2012.

[14] J. Henry and J. Kimball, "Practical performance analysis of complex switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 26, pp. 127–136, Jan 2011.

[15] A. Sommariva, "Solving the two capacitor paradox through a new asymptotic approach," *Proc. IEE Proceedings Circuits, Devices and Systems*, vol. 150, pp. 227–231, June 2003.

[16] C. Tse, S. Wong, and M. H. L. Chow, "On lossless switched-capacitor power converters," *IEEE Trans. Power Electron.*, vol. 10, pp. 286–291, May 1995.

[17] F. Zhang, L. Du, F. Z. Peng, and Z. Qian, "A new design method for high-power high-efficiency switched-capacitor dc-dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 832–840, 2008.

[18] M. Evzelman and S. Ben-Yaakov, "Average-current-based conduction losses model of switched capacitor converters," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3341–3352, 2013.

[19] C.-K. Cheung, S.-C. Tan, C. Tse, and A. Ioinovici, "On energy efficiency of switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 28, pp. 862–876, Feb 2013.

[20] M. Evzelman and S. Ben-Yaakov, "Simulation of hybrid converters by average models," *IEEE Trans. Ind. Appl.*, vol. PP, no. 99, pp. 1–1, 2013.

[21] T. Tanzawa, "On two-phase switched-capacitor multipliers with minimum circuit area," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, pp. 2602–2608, Oct 2010.

[22] D. Zhou, A. Pietkiewicz, and S. Cuk, "A three-switch high-voltage converter," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 177–183, 1999.

[23] J. Mayo-Maldonado, R. Salas-Cabrera, J. Rosas-Caro, J. De Leon-Morales, and E. Salas-Cabrera, "Modelling and control of a dc-dc multilevel boost converter," *IET Power Electron.*, vol. 4, no. 6, pp. 693–700, 2011.

[24] D. Liberzon, *Switching in Systems and Control*. Birkhauser. Boston, Basel, Berlin, 2003.

[25] J. P. Hespanha and A. S. Morse, "Switching between stabilizing controllers," *Automatica*, vol. 38, no. 11, pp. 1905–1917, 2002.

[26] J. Mayo-Maldonado, P. Rapisarda, and P. Rocha, "Stability of switched linear differential systems," *IEEE Trans. Autom. Control*, vol. 59, pp. 2038–2051, Aug 2014.

[27] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, pp. 841–851, March 2008.

[28] J. Rosas-Caro, F. Mancilla-David, J. Mayo-Maldonado, J. Gonzalez-Lopez, H. Torres-Espinosa, and J. Valdez-Resendiz, "A transformer-less high-gain boost converter with input current ripple cancelation at a selectable duty cycle," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4492–4499, 2013.

[29] J. Rosas-Caro, J. Ramirez, and A. Valderrabano, "Voltage balancing in DC/DC multilevel boost converters," in *Proc 40th North American Power Symposium (NAPS)*, pp. 1–7, 2008.

[30] J. Kimball, P. Krein, and K. Cahill, "Modeling of capacitor impedance in switching converters," *IEEE Power Electron Lett.*, vol. 3, pp. 136–140, Dec 2005.

[31] R. Pilawa-Podgurski and D. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, pp. 1557–1567, July 2012.

[32] J. Mayo-Maldonado and P. Rapisarda, "Modelling of switching dynamics in electrical systems," in *Proc. Mathematical Theory of Networks and Systems Symposium (MTNS),* Groningen, NL, 2014.