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Graphene FET Circuit-level Device Modelling

by

Ime J. Umoh

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ABSTRACT

FACULTY OF ENGINEERING AND APPLIED SCIENCE
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Doctor of Philosophy

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This thesis presents models for a graphene based field effect transistor (GFET). The graphene material has been widely studied since its synthesis in 2004 and the material holds promise for the next generation electronic applications. Therefore, there is a need to model its device characteristics.

In this respect the contributions presented here are, firstly, a SPICE-compatible model for both dual gate and single gate graphene transistors. The derivation of the carrier transport of both hole and electron conduction results in a set of analytical equations. These derivations cover the three identified regions of operation as well as the boundary voltage conditions that define the regions. The Jacobian entries are shown to be continuous across the region boundaries.

Secondly, circuit levels model of a single-layer GFET and multi layer GFET suitable for a direct implementation in SPICE. In this contribution, a more accurate threshold voltage compared to other models is derived. This contribution also shows how models can be extended to as many layers the graphene channelled transistor has.

Finally, the introduction of a thermionic resistance, which is modelled in parallel with the resistance due to gate induced charges, provides a model for the temperature dependent channel resistance. The contribution goes further to derive equations between the off current and the vertical electric fields. Thus, giving a good estimation of the tunable bandgap opening in graphene.

The models in this contributions are validated against experimentally measured transistor characteristics which have been carried out by other research groups and the models show a good agreement in all cases validated. The thesis equally presents the use of a floating gate to optimize the transistors characteristics. To illustrate these contributions, algorithms of the models have been implemented on the following CAD tools, HSPICE, VHDL-AMS and Berkeley SPICE. During the course of this work one journal and five conference papers have been published.

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Listings

Nomenclature

x,y	Axis direction
a_1, a_2	Primitive vectors
b_1, b_2	Reciprocal vectors
k_1, k_2	wave function
v	plane velocity
A_1, A_2, B_1, B_2	lattice sites
$\hbar$	Reduced Plank's constant
Δ, E_g	Band gap energy
γ	Nearest neighbour hopping energy
M, K, K', Γ	Points in the first brillouin zone
$E(k)$	Dispersion energy
p	momentum
v_F	Fermi velocity
μ	mobility
ϵ	Permittivity of free space
ϵ_1, ϵ_2	Relative permittivity
q	Electronic charge
K_B	Boltzmann's constant
T	Absolute temperature
V_g, V_b, V_d, V_s	Potential of top-gate, back-gate, drain, source
φ, V_{ch}	Surface potential
V_{bs}^0	Back-gate voltage offset
V_{gs}^0	Top-gate voltage offset
$V_{ds-sat1}$, $V_{ds-sat2}$	Saturation voltage for unipolar, ambipolar
C_{ox}, C_e, C_{TG}	Top-gate capacitance
C_b, C_{BG}	Back-gate capacitance
C_q	Quantum capacitance
α, β, η, n	Characteristic constant
E_c	Critical electric field
E_{ox} , E	Electric field
V_{ox}	Potential drop across oxide
v_{sat}	Velocity saturation

V_E	Drift velocity
C_{top}	effective top-gate capacitance
C_{back}	effective back-gate capacitance
V_o	Threshold velocity
W	Width
L	Length
t_{ox}, t	Top-gate dielectric thickness
H_{sub}	Back-gate dielectric thickness
R_s	Series resistance
I_{ds}	Drain current
I_{ds-sat}	Unipolar saturation current
I_{disp}	Saturation displacement current
I_{off}	Drain off-current
g_m	Transconductance
g_{ds}	Output conductance
U	Potential energy per unit area
ϕ_b, ϕ_g	Potential barrier
V_T	Voltage constant
T_α	Temperature constant
T_{ref}	Reference temperature
T_o	Temperature parameter
n_0	Minimum charge density
R_s^0	Intrinsic resistance
R_q	off-current resistance
C_o	Interlayer capacitance

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To My Parents

Chapter 1

Introduction

Bare graphene is a two dimensional structure of tightly bound carbon atoms with a honey combed lattice. This structure can be wrapped up into a zero-dimension buckminsterfullerene, a one-dimension carbon nanotube and a three-dimensional stacked graphene commonly called graphite. In the last two decades there has been a lot of research into the behaviour and possible application of both carbon nanotubes and graphene.

1.1 Carbon nanotubes

The carbon nanotube (CNT) was first synthesised in the early 1990s [1, 2, 3] with many potential applications in the fields of nanoelectronics, optics and material science. The nanotube is categorized into two groups, single-walled and multi-walled. A single-walled nanotube is formed by rolling just one atomically thin graphene sheet while a multi-walled nanotube refers to the rolling of two or more stacks of graphene sheets. Experiments and theory have shown that both of the nanotube categories can be either metallic [4, 5] or semiconducting [6]. Either of the forms of CNTs has potential application in future generation integrated circuits (ICs). As such there have been a number of compact models developed [7, 8, 9, 10, 11]. With one of the models [11] using cubic spline approximations to ensure shorter circuit simulation time. Since CNT is analysed as a rolled up two-dimensional graphene, therefore its remarkable electrical properties originates from the electronic structure of graphene [12, 13]

1.2 Graphene

The isolation of graphene from graphite came much later than the CNT in 2004 [14], by mechanical exfoliation. Like the CNT, two dimensional graphene holds a lot of prospects as a possible candidate to complement silicon in the next generation ICs

because of its high carrier mobility and high current density. Graphene being flat makes it easy to be integrated into the current CMOS lithographic process [15]. Similar to the categorization in CNTs, graphene has single-layers, bilayers, trilayer and so forth. For eleven and greater stacked layers of graphene sheets, the structure is considered to be three-dimensional graphite [16, 17] and between three to ten layers, the structure is referred to as few layer graphene [16].

Particular interest will be given to devices with single-layer to a few layers. Other than mechanical exfoliation, few layered graphene has been grown epitaxially by chemical vapour deposition on metal substrates [18, 19, 20, 21] as well as by thermal deposition on silicon carbide (SiC) [22]. Chemical vapour deposition in making transistors is more commercially viable than mechanical exfoliation and also a more viable route to electronic applications. One of the most remarkable features of graphene is its high carrier mobility at room temperature [23]. To put this in perspective, suspended graphene has a recorded mobility in excess of $200,000 cm^2/Vs$ [24] at room temperature compared to $1,400 cm^2/Vs$ for silicon and $8,500 cm^2/Vs$ for gallium arsenide [25]. In terms of cut-off frequency and high speed electronics, graphene currently out-performs other semiconductors with a cut-off frequency of up to 300GHz [26, 27, 28]. Both graphene and CNT transistor were used to implement a ring oscillator. The graphene based ring oscillator had a frequency as high as 1.28GHz while the CNT based ring oscillator was limited to 52MHz [29].

1.2.1 Graphene Transistor Modelling

Despite its remarkable carrier mobility among other physical properties, graphene does not have a bandgap. It is referred to as a semi-metal because both its conduction and valence bands touch at the Fermi level. The gapless nature of graphene is the reason it is modelled as an ambipolar device [14, 30, 31] whereby carriers can be tuned from being hole-like to electron-like. The main aim of modelling graphene transistors is to be able to predict its performance in circuit designs. As the fabrication of graphene becomes more controlled, the current models will be greatly improved to predict the behaviour of a transistor prior to fabrication.

1.3 Research Challenges

The need to design circuits has prompted a lot of research into developing model targeted for circuit simulations. The modelling still has a number of challenges.

- A number of simulation program with integrated circuit emphasis (SPICE) compatible models have been reported which use either a numerical [32, 33] or an

analytical [34] approach to model the transport behaviour, yet the models do not show the boundary voltage conditions for all the three regions of operation.

- Determining the threshold voltage is very important in circuit design as the threshold voltage accounts for the off-state of a field effect transistor. Models adopt a simple linear relationship to determine the behaviour of the threshold voltage in graphene which has shown a good agreement for some experiments and large deviations for others. Therefore there is a need to develop graphene layer specific models which will give a good agreement against all measured threshold voltages.

- A tunable bandgap has been successfully opened in two or more layered graphene. Therefore, there is a need to model the off-current resulting from the opening of a bandgap.

- Published experimental analysis of graphene devices are carried out at varying temperatures. Some at room temperature and some at temperatures as low as 4.7 Kelvin, therefore it is important to know how the device is dependent on temperature to accurately model its characteristics.

1.4 Research Aims and Contributions

In light of the challenges faced by the currently available modelling, the aim of this research is to develop a graphene model that is both SPICE compatible so as to facilitate circuit design and closely predicts the behaviour of the graphene field effect transistor (FET) at various bias and temperature conditions. This research develops both a compact model which is analytical for a single-layer and a numerically intensive model. The compact model guarantees a fast simulation time which is necessary for very large scale designs such as in digital circuits. Furthermore, to facilitate development of circuit designs, the research focuses on the implementation of the model in popularly used computer aided design (CAD) tools. These contributions include:

- Ambipolar saturation transport modelling:

  This contribution presents an analytical equation for modelling the transport characteristics in the ambipolar saturation region that is observed in the graphene bilayer field effect transistor. Being able to determine and model this region is very important because this region can make the transistor draw a destructive amount of current leading to its breakdown. This work presents derived equations that capture the device physics over the phenomenological expressions used in previous literature [34, 35, 36, 37]. This contribution has been published in the IEEE Transaction in Nanotechnology [38]. Three conference papers [35, 36, 37] describing this model have been published in the 55^{th} ETRAN (electronics, telecommunication,

computers, automatic control and nuclear engineering) conference [35], the FDL (Forum on specification & Design Languages) 2011 conference [36] and the Virtual Worldwide Forum for PhD Researchers in Electronic Design Automation 2011 conference [37] respectively.

- Transistor current region boundaries:

  Another contribution of this work is the derivation of the analytical equations of the boundary voltages for the respective regions of operation of the transistor. This is the first presentation of an analytical equation that distinguishes the unipolar saturation region from the ambipolar saturation region. The Jacobian entries have been shown to be continuous across these boundaries, which indicates that the proposed model is suitable for SPICE implementation. This contribution has been published in IEEE [38].

- Behavioural model implementation:

  This contribution presents the development of behavioural models for computer simulation of graphene bilayer field effect transistors. This models are based on close analytical equations which allows them to be very fast and take up low computation power. The models are also very efficient since they do not use numerical analysis to approximate the drain current characteristics. Behavioural models of two commercial CAD tools have so far been published; one in HSPICE [35] and the other in VHDL-AMS [36].

- Circuit level implementation:

  This contribution presents the development of a circuit level implementation of the transistor in Berkeley SPICE. Berkeley SPICE is an open source SPICE simulator and in this work the graphene transistor library has been integrated into the simulator.

- Floating gate and digital logic implementation:

  This contribution presents the use of a floating gate to control charge density in the transistor. The control of the charge density has been exploited to develop a inverter with symmetrical transfer characteristics. This is the first presentation of the use of a floating gate on a graphene bilayer transistor. This technique shows promise for optimising the graphene transistor. A conference paper [39] has been published based on this contribution.

- Accurate threshold voltage modelling:

  In this research one of the main contributions is accurate calculation of the threshold voltage. The threshold voltage is calculated from the proposed equivalent circuit model. This confirms that the equivalent model presented here better fits the transistor device. This contribution has been published in IEEE [40]

- Temperature dependence and bandgap estimation:

  Furthermore, another contribution of this work is the development of a phenomenological equation that models the channel conductance dependence on temperature. This allows for the estimation of the amount of bandgap opening and how the band gap is tuned by varying model parameters. This contribution has been published in IEEE [40] and has been presented in a conference [41, 42].

1.5 Thesis Organisation

This thesis is organised into seven chapters. Of the seven chapters the last five focus solely on my work.

Chapter 2 is a literature review of the state-of-the-art in graphene electronics. The chapter presents techniques researchers are exploring to engineer a band gap in graphene. It also presents the energy dispersion and the quantum capacitance of graphene and the role it plays in the carrier transport characteristics. This chapter explores the transport mechanism of carriers as well as the tunneling using a floating gate.

Chapter 3 proposes an analytical derivation of the drain current characteristics of a graphene transistor. The general model used here can apply to any graphene FET. Layer specific models for single-layer and few layer graphene transistor can be mapped to the general model to calculate the respective transport characteristics. Two sections show the derivation for both hole and electron conduction. For each of the carrier conduction modes, the analytical derivation covers the three regions of operation namely, unipolar, unipolar saturation and ambipolar saturation and their respective voltage boundaries. Work carried out in this chapter has been published in the IEEE Transaction in Nanotechnology [38] as well as presented in conferences and workshops [35, 36, 37].

Chapter 4 presents a single-layer specific model. The equivalent circuit model with derivation the effective capacitance and the threshold voltages for both a single and a dual gated transistor are presented. The chapter explains how the single-layer specific model of either the single or dual gate can be mapped to the general model to calculate the transport characteristics. Operational temperature analysis of the single-layer is also discussed. The model is validated against published experimental data and a comparison is presented. Work carried out in this chapter is to be presented in a conference [42].

Chapter 5 describes a multi-layer graphene FET model. It focuses mostly on the bilayer graphene and a four layer graphene transistor. The salient feature of the multi-layer model is that it can be extended to a graphene channel with an arbitrary number of layers. The chapter also shows how such a model can be mapped to the general model to calculate its drain current and the channel resistance transfer characteristics. Also a temperature analysis is performed and equations of the channel resistance dependence

on temperature are presented. The off-current and its dependence on the electric field is also derived. Using the model of the off-current, an estimation of the bandgap opening is obtained. The model presented is validated against published experimental data and a comparison made. Work carried out in this chapter has been submitted for a journal publication in the IEEE Nanotechnology Transaction [40] where it is currently under review and has been presented in a conference [41].

Chapter 6 describes CAD tools used in the project and the optimization of the transistor using a floating gate. Supporting this work, the model has been implemented in three CAD tools which are HSPICE, VHDL-AMS and Berkeley SPICE. Work in this chapter shows how the model is implemented in the various CAD tools and how the model interacts with the CAD tool simulator. Also the concept of a floating-gate has been exploited to implement a logic inverter. Work carried out in this chapter had been presented in various conferences [35, 36, 39, 43].

The final chapter provides a general conclusion of the work carried out so far and presents areas further work is to be carried out.

Chapter 2

Literature Review

Carbon has six electrons making it a Group IV element in the periodic table. The four valence electrons in its outer shell allows carbon to undergo one of three forms of hybridization; sp^3, sp^2 or sp which is the mixing of atomic orbitals. In sp^2 hybridization, each of the carbon atoms shares a double bond with an adjacent carbon atom. Fig. 2.1 shows three stable forms of carbon with sp^2 hybridization that has been successfully synthesised; fullerenes [44], carbon nanotubes [1] and graphene [14].

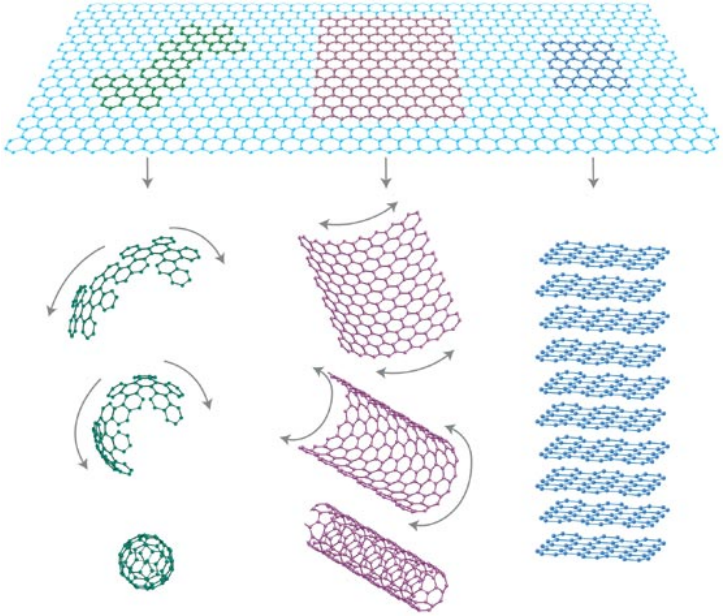


FIGURE 2.1: A two-dimension graphene rolled into a zero-dimension fullerene (left), one-dimension carbon nanotube (middle) and stacked into three-dimension graphite (right). Reprinted with permission from [16]. Copyright 2007, Rights Managed by Nature Publishing Group.

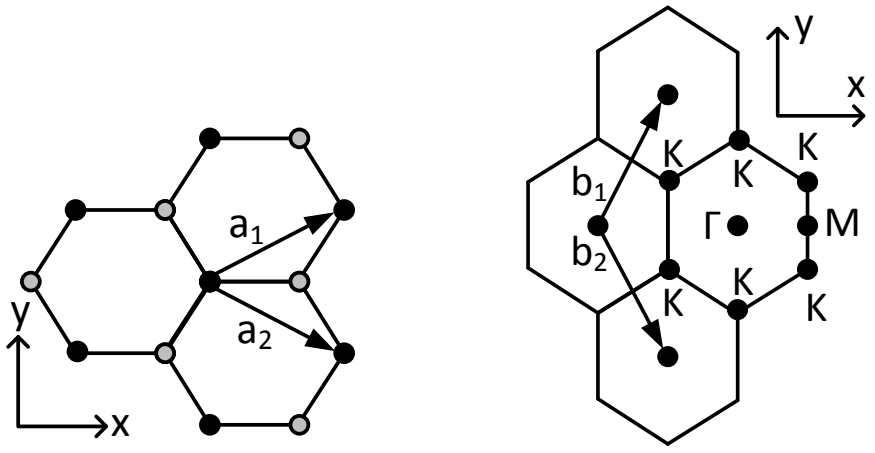
TABLE 2.1: Allotropes of graphene [45]

Dimension	0-D	1-D	2-D	3-D
Allotrope	Fullerenes	Carbon nanotubes	Graphene	Graphite
Structure	Spherical	Cylindrical	Planar	Stacked planar
Hybridization	sp^2	sp^2	sp^2	sp^2
Electronic properties	Semiconductor	Metal or semiconductor	Semi-metal	Metal

2.0.1 Single-Layer Tight Binding

Table (2.1) shows that despite carbon having an sp^2 hybridization, it can have a varying structure, allotrope and electrical properties. Owing to the six electrons, carbon has electrons in the following orbitals; 1s, 2s, $2p_x$ and $2p_y$. The 2s and 2p orbital interact to form three hybrid orbitals, $2p_x$, $2p_y$ and $2p_z$. In bonding, three σ bonds are formed with a π bond. The σ bonds are strong covalent bonds with electrons localized along the plane of the bond between the carbon atoms, while the π bond is weakly bound to the nuclei and originates from the $2p_z$ electrons [45]. With loosely bound electrons, the π bond determines the electrical properties of graphene. For both carbon nanotubes and graphene the crystal lattice is cyclohexane in structure (see Fig. 2.2(a)).

The hexagonal lattice structure has a carbon to carbon distance of approximately 0.142nm. From Fig. 2.2(a), each of the carbon atoms in the lattice has two set of carbon atoms with analogous bonds. One set of analogous bonding atoms are coloured black and the other gray.



(a) Graphene honeycomb lattice (b) The reciprocal lattice of graphene

FIGURE 2.2: The lattice structure of an atomic layer of graphene

2.0.1.1 Brillouin Zone

Crystal lattices are often described by their Bravais lattice. In an array of atoms, there exist an atom or a collection of atoms whereby the orientation is always the same when looking at other atoms from that atom or collection of atoms. This representation at any point in the structure is referred to as Bravais lattice while the number of atoms in the collection is called its basis. Graphene's honeycomb lattice has a basis of two.

From Fig. 2.2(a), an atom is projected to its two analogous atoms with primitive vectors a_1 and a_2. These primitive vectors in Eqn. (2.1) are associated with the Bravais lattice vector $R = n_1a_1 + n_2a_2$ where n_1 and n_2 are integers and $a = |a_1| = |a_2|$ also $a = \sqrt{3}a_{c-c}$.

$$a_1 = \left(\frac{\sqrt{3}a}{2}, \frac{a}{2}\right), a_2 = \left(\frac{\sqrt{3}a}{2}, -\frac{a}{2}\right) \tag{2.1}$$

The primitive vectors and the Bravais lattice describe the direct lattice or real lattice. The central feature of electrons in crystalline solid is periodicity and regularity [45]. The primitive vectors allow us to view the lattice in say the time domain. In order to view the lattice in the frequency domain, a discrete Fourier transform of the direct lattice is required which gives a reciprocal lattice.

When considering a 3-D lattice, the primitive vectors $|a_1|$, $|a_2|$ and $|a_3|$ have corresponding reciprocal vectors $|b_1|$, $|b_2|$ and $|b_3|$, which is represented by Eqn. (2.2).

$$b_1 = 2\pi\frac{a_2 \times a_3}{a_1.(a_2 \times a_3)}, b_2 = 2\pi\frac{a_3 \times a_1}{a_1.(a_2 \times a_3)}, b_3 = 2\pi\frac{a_1 \times a_2}{a_1.(a_2 \times a_3)} \tag{2.2}$$

But the graphene direct lattice is a 2-D lattice, therefore Eqn. (2.2) will be reduced to Eqn. (2.3) [45].

$$b_1 = 2\pi\frac{R_{90}(a_2)}{\det(a_1, a_2)}, b_2 = 2\pi\frac{R_{90}(-a_1)}{\det(a_1, a_2)} \tag{2.3}$$

In Eqn. (2.3), R_{90} is an operator that rotates the vector clockwise by 90 degrees. For example rotation on a vector $v = v_1\hat{x} + v_2\hat{y}$ gives $R_{90}(\pm v) = \pm(v_1\hat{x} - v_2\hat{y})$.

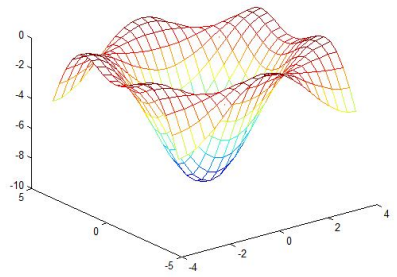
Applying Eqn. (2.3) to the primitive vectors, Eqn. (2.1) yields:

$$b_1 = \left(\frac{2\pi}{\sqrt{3}a}, \frac{2\pi}{a}\right), b_2 = \left(\frac{2\pi}{\sqrt{3}a}, -\frac{2\pi}{a}\right) \tag{2.4}$$

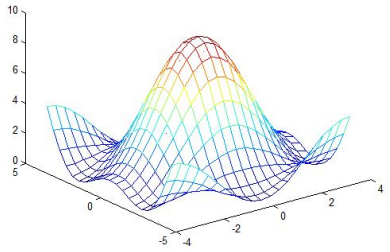
It can be seen that the corresponding reciprocal lattice vectors in Eqn. (2.4) are either parallel or normal to the associate primitive vectors. The reciprocal vectors are shown in Fig. 2.2(b).

In the reciprocal lattice there are some points of interest; the Γ-point, the K -point and the M -point. These points describe the first Brillouin zone. The Brillouin zone is used to investigate the electronic band structure in crystals. The Γ-point is in the center of the Brillouin zone and the M-point is midway the K - K′. Therefore, there are six K-points and six M-points.

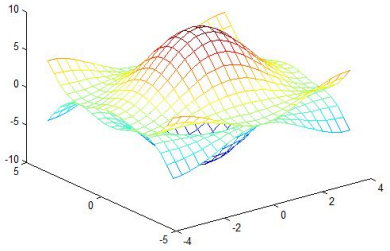
2.0.1.2 Energy Dispersion



(a) Valence band energy



(b) Conduction band energy



(c) The graphene energy band

FIGURE 2.3: The energy band spectrum for graphene in the Brillouin zone

In the graphene lattice, each carbon atom with its four valence electrons forms 2s and 2p orbitals. The resulting atomic orbitals electronic wave functions overlap. The overlap between the $2p_z$ and the 2s, $2p_x$ or $2p_y$ have zero symmetry as such the $2p_z$ is treated independently [46]. The $2p_z$ are responsible for the π electrons which determine the electronic properties of graphene. The energy spectrum of the first Brillouin zone is therefore calculated from the Schrodinger wave equation along with Bloch's theorem which states that a wave function is periodic with the length of its lattice [45].

Hence, the energy dispersion in the first Brillouin zone is given by Eqn. (2.5) [46].

$$E(k)^{\pm} = \pm\gamma\sqrt{1 + 4\cos\frac{\sqrt{3}a}{2}k_x\cos\frac{a}{2}k_y + 4\cos^2\frac{a}{2}k_y} \tag{2.5}$$

Eqn. (2.5) is plotted for $E(k)^-$, $E(k)^+$ and $E(k)^\pm$ and can be seen in Fig. 2.3(a), Fig. 2.3(b) and Fig. 2.3(c) respectively.

2.0.2 Bilayer Tight Binding

The device bandgap greatly influences the channel conductivity. In the bilayer graphene the electric field opens the bandgap by creating an asymmetry between the layers [47].

2.0.2.1 Bernal Stacking

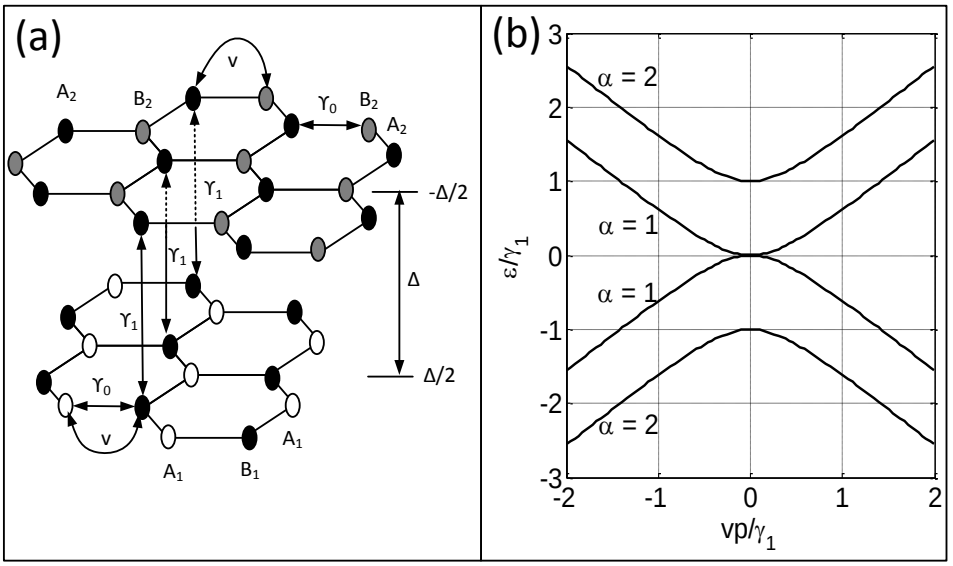


FIGURE 2.4: (a) bilayer lattice in Bernal stacking. (b) low energy bands near the K-points

Fig. 2.4-a considers Bernal stacking of the two layers in bilayer graphene such that one corner of the hexagon on the top sheet is directly above the center of the hexagon in the bottom sheet. Every A_2 (black circles) site on the top layer lies directly above every B_1 (black circle) site on the bottom layer, but other sites B_2 (gray circle) and A_1 (white circle) are not directly opposing each other.

By applying the tight-binding model of graphite to describe the electronic band structure of bilayer graphene [48, 49, 50, 51], it is taken that the in-plane couplings between sites A_1 and B_1 ($\gamma_{A_1B_1}$) as well as between A_2 and B_2 ($\gamma_{A_2B_2}$) are equal and equivalent to γ_0. Also, the inter-layer couplings between sites A_2 and B_1 ($\gamma_{A_2B_1}$) are equivalent to γ_1. Although, there are other inter-layer couplings such as between sites A_1 and B_2 but these are weaker than γ_1 and they have been ignored.

2.0.2.2 Energy Dispersion

The in-plane velocity, v, in Fig. 2.4 is $v = (\sqrt{3}/2)a\gamma_0/\hbar$, where a is the lattice constant and $\hbar$ is the reduced Plank's constant. Given the wave vector k, the momentum, p, with respect to the wave vector is $p = \hbar k$. Δ accounts for the asymmetry between inter-layer site energies. Taking Δ into account, the energy dispersion is given by Eqn. (2.6) [47, 49].

$$\varepsilon^2 = \frac{\gamma_1^2}{2} + \frac{\Delta^2}{4} + v^2p^2 + (-1)^\alpha\sqrt{\frac{\gamma_1^4}{4} + v^2p^2(\gamma_1^2 + \Delta^2)} \tag{2.6}$$

Fig. 2.4-b shows the normalized energy dispersion for a coupled bilayer graphene with $\Delta = 0$, $a = 0.246nm$, γ_0 and γ_1 are 3.0eV and 0.35eV respectively. At the K-points where both the conduction and valence bands touch, the momentum $p = 0$.

2.0.3 Energy Dispersion Close to the K-points

In the graphene lattice, there are six K-points (see Fig. 2.3), these points are referred to as Dirac points and they are shown in Fig. 2.2(b). In Eqn. (2.7), the energy dispersion close to the Dirac points can be simplified to a linear dispersion, $E(k)$, whose gradient is given by the product of the reduced Plank's constant $\hbar$, the Fermi velocity v_F and the spherical coordinate k [52].

$$E(k) = \pm\hbar v_F\sqrt{k_x^2 + k_y^2} \tag{2.7}$$

Thus, for both single-layer and bilayer graphene, Fig. 2.5 displays the energy dispersion around the Dirac point. The single-layer shows a clearly linear dispersion in Fig. 2.5-i and since both bands touch it is a semi-metal with a zero bandgap. But by slicing the single-layer into a few nanometer wide ribbon, a measure of bandgap opens as shown in Fig. 2.5-ii. Equally, in the case of bilayer as shown in Fig. 2.5-iii, at the Dirac point both bands touch but in the case of the bilayer the dispersion is parabolic. On applying an electric field a tunable bandgap opens as shown in Fig. 2.5-iv.

2.0.4 Electron Confinement Using a Potential Barrier

In metallic single walled carbon nanotube (SWCNT), there is an absence of backscattering even in the presence of scatters, this makes the metallic SWCNT a good conductor [54]. Any potential drop in the metallic SWCNT is across its contact resistance, while conduction through the channel is ballistic [55]. On the other hand, the semiconductor SWCNT shows a large voltage dependent resistance along the nanotube channel. This

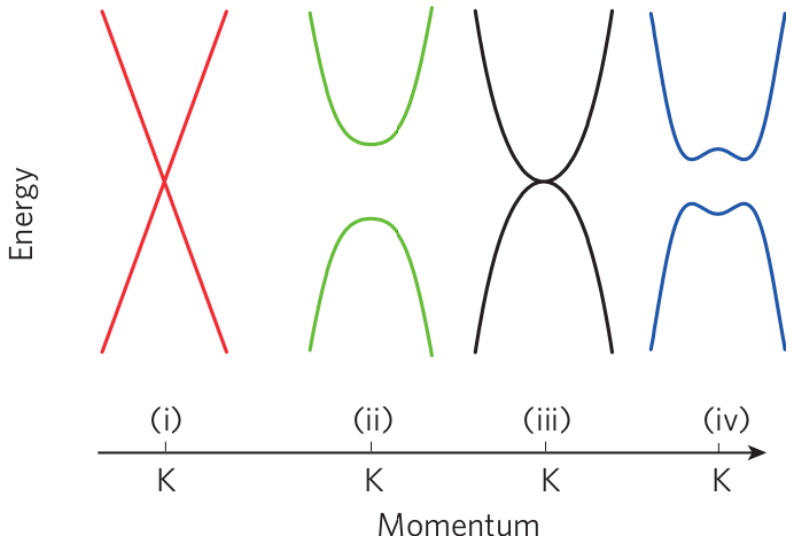


FIGURE 2.5: The energy dispersion close to the K-points for i) single-layer ii) nanoribbons iii) bilayer with zero electric field and iv) bilayer in the presence of an electric field. Reprinted with permission from [53]. Copyright 2010, Rights Managed by Nature Publishing Group.

resistance confirms the presence of backscattering in semiconducting SWCNT. Thus, by having backscattering for semiconducting SWCNT and not for metallic SWCNT implies that the chirality plays a dominant role in the backscattering.

In taking the case of a finite rectangular potential barrier of height V_o and width D, when an electron of energy E is incident on the barrier as shown in Fig. 2.6-b, ideally, the transmission energy through the barrier decays exponentially with the height and width of the barrier. As such no transmission is expected through the forbidden region in classical mechanics [57]. By solving the transmission probability for a p-n-p junction, transmission in graphene is perfect at an angle normal to the barrier [56] as shown in Eqn. (2.8):

$$T = \frac{cos^2\varphi}{1 - cos(q_x D)sin\varphi} \tag{2.8}$$

where φ is the angle on incidence and q_x is a wave factor.

Carriers from the green (red) branch, which are electron-like (hole-like) in Fig. 2.6-a for a single-layer and Fig. 2.6-c for a bilayer at zero energy, can only be scattered into states of the same branch. A flip in pseudospin will be required to scatter into an alternate branch. Hence, a hole-like carrier can enter the barrier via the red branch, transmute into an electron-like carrier and exit via the green branch. This is possible because Dirac particles cannot be confined by an electrostatic potential [58]; Dirac particles have both positive and negative energy states and their transmission probability is weakly dependent on the barrier height [57].

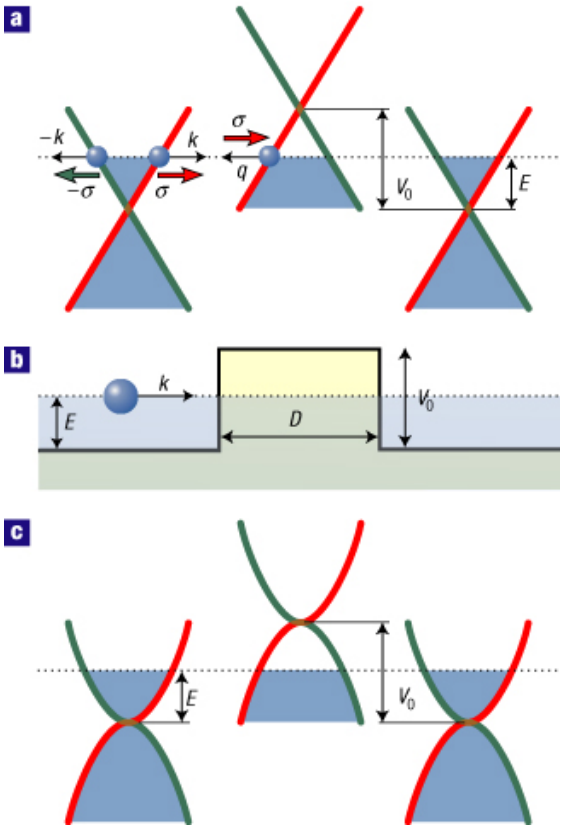


FIGURE 2.6: (a) Single-layer energy dispersion. (b) Rectangular potential barrier and (c) Bilayer energy dispersion. Reprinted with permission from [56]. Copyright 2006, Rights Managed by Nature Publishing Group.

2.1 Graphene Transistor Modelling

Graphene can have carriers travel ballistically between submicron distances, giving it an excellent electronic property. High carrier mobility [23] plays a vital role in its electronic property as the dimension of the channel is reduced due to scaling. Carrier mobility in graphene is in the vicinity of $2 \times 10^3 cm^2 V^{-1} s^{-1}$ to $15 \times 10^3 cm^2 V^{-1} s^{-1}$ for a substrate supported sample [30, 59] and $2 \times 10^5 cm^2 V^{-1} s^{-1}$ for a suspended sample[59, 60].

2.1.1 Carrier Scattering

Currently, suspended graphene has the highest mobility but compared to graphene on substrates their conductivity at the Dirac point is strongly dependent on temperature. Above 100K the transport carriers suffer from thermal scattering and approach ballistic transport at temperatures of liquid helium [60].

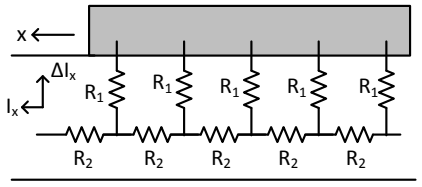
Thermal scattering is independent of the channel length. As the device geometric dimensions are scaled further into the nano-level other secondary effects become more prominent, while phonon and acoustic scattering become negligible. The mean free length for phonon scattering is estimated at $l_{ph} = 0.77 \mu m$ [61].

In ballistic transport, for lengths lower than l_{ph}, other secondary effects such as; Coulomb scattering by charged impurities near the interface between graphene and the substrate (μ_c), surface roughness (μ_{sr}), line-edge roughness (μ_{ler}) and short range scattering (μ_r) due to lattice defects will limit the conductivity [62, 63, 64, 65]. Thus, the effective mobility can be formulated with Mathiessens rule [66] which is represented by Eqn. (2.9).

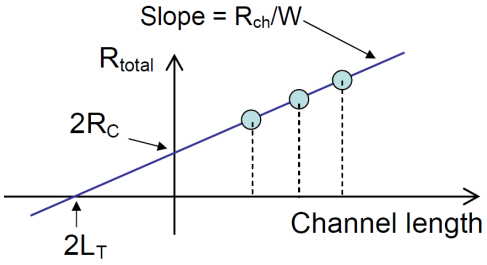
$$\mu_{eff}^{-1} \propto \mu_c^{-1} + \mu_{sr}^{-1} + \mu_{ler}^{-1} + \mu_r^{-1} \tag{2.9}$$

2.1.2 Metal Contact

A very important function performed on the transistor is that of getting carriers into and out of the transistor. In the absence of backscattering, especially in the single-layer graphene, ballistic transport is expected. Therefore, any limiting current is due to the presence of a contact resistance. Fig. 2.7 shows the schematic (see Fig. 2.7(a)) and the characteristics of the contact resistance against changes in the contact spacing (see Fig. 2.7(b)) for a metal contact on a thin semiconductor.



(a) Distributed resistor network schematic of the contact resistance



(b) The total contact resistance against the channel length. Reprinted with permission from [67]. Copyright 2011, Rights Managed by Nature Publishing Group.

FIGURE 2.7: Characteristic of a metal on a thin semiconductor

This technique of modelling the total contact resistance has been applied in investigating the behaviour of a metal contact on the graphene channel [67, 68, 69]. Solving Fig. 2.7(a) results in a differential equation for both current and voltage with respect to the distance, x. The contact resistance $R_1 = \rho_G/W\Delta x$ and the semiconductor resistance $R_2 = R_{ch}\Delta x/W$. Where R_c, W, ρ_G and R_{ch} are the total resistance of the contact, width, the contact resistivity and the channel sheet resistance respectively.

Specifically, in the case of metal on graphene, there is a presence of charge carriers at the infinitesimally small spacing between the metal and the graphene layer as shown in Fig, 2.8-b [67]. Both the work functions of the metal and graphene separated by a dielectric constitutes a band profile. As such, Fig. 2.8-c confirms that the contact resistance

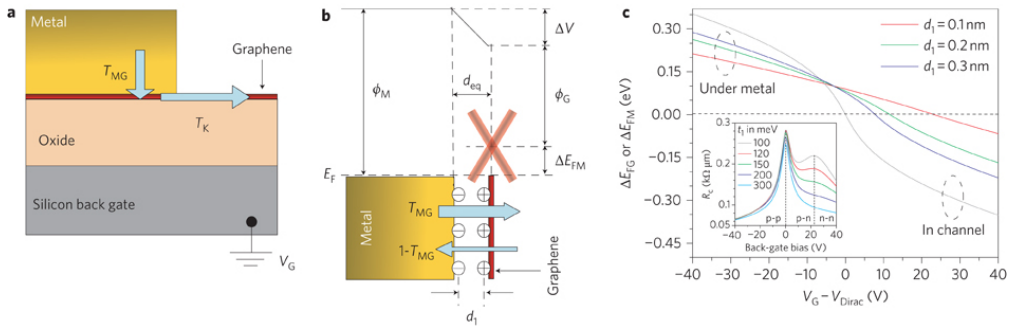
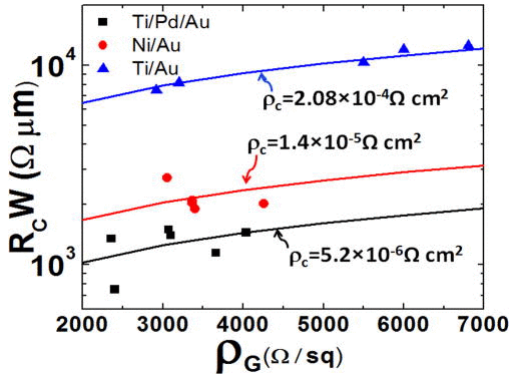
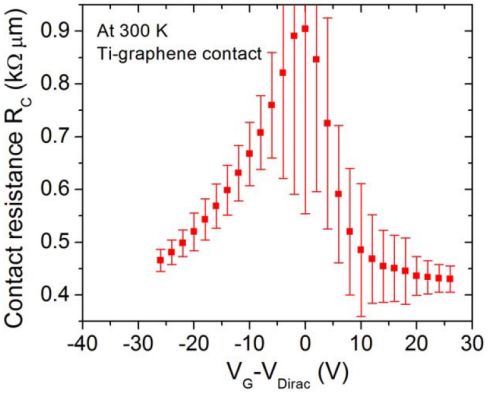


FIGURE 2.8: (a) Layout of the transistor under the metal contact (b) Charge distribution between the graphene and metal contact. (c) Energy level for a sweep in the gate voltage. Reprinted with permission from [67]. Copyright 2011, Rights Managed by Nature Publishing Group.

is modulated by the gate voltage and the contact resistance shows a dependence on temperature; decreasing against a decrease in temperature.



(a) Contact resistance R_cW versus the sheet resistance of graphene channel ρ_G for different source/drain contacts. Reprinted with permission from [68]. Copyright 2011, Rights managed by AIP Publishing LLC.



(b) Characteristics of Titanium metal contact on graphene. Reprinted with permission from [67]. Copyright 2011, Rights Managed by Nature Publishing Group.

FIGURE 2.9: Comparison of various contact resistance and the gate modulation of Ti contact resistance on graphene

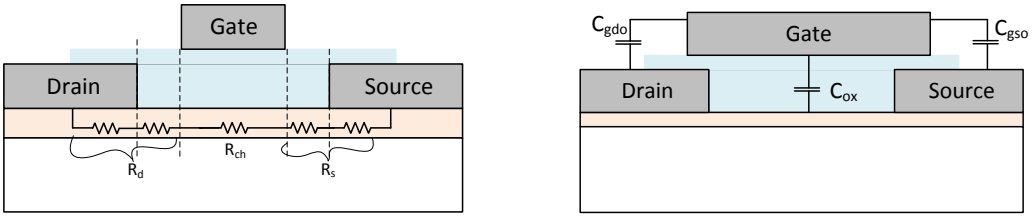
Palladium (Pd) and Titanium (Ti) are one of the most commonly used metal contacts on graphene, owing to their ability to adhere to graphene.

Ti has a contact resistance which is about twice that of Pd [67]. This is illustrated with a Gold (Au) on Ti, Ti/Au, contact which gave the largest resistance of about 7500$\Omega\mu m$, an Au on Nickel (Ni), Ni/Au, contact shows a smaller resistance compared to Ti/Au, of around 2100$\Omega\mu m$ and the lowest contact resistance was given by Ti/Pd/Au, which is around 750$\Omega\mu m$ [68]. In the last case, Ti is used primarily to provide better adhesion between Pd and the substrate while contact resistance is dominated by Pd. Fig. 2.9 shows the contact resistances of these two metals with respect to changes in the gate voltage.

Two things are to be taken into consideration when determining a suitable contact for graphene: 1) the work function difference between the metal and graphene. Metals with higher work function difference such as Pd gave better results. 2) The interaction between the metal and graphene. Ti gives a stronger interaction and has been used to improve adhesion, but gives higher resistance because charges doped under Ti are not easily modulated by the gate [67].

2.1.3 Parasitic Capacitance and Series Resistance

Along side the contact resistance is the access resistance. This is the resistance of the ungated region between the source/drain and the gate. Both the contact and the access resistance are referred to as series resistance. In field effect transistor design, there is a trade-off between series resistance and the parasitic overlap capacitance.



(a) Series resistance transistor schematic

(b) Overlapping capacitance transistor schematic

FIGURE 2.10: Field effect transistor layout

Fig. 2.10 shows two transistor layouts, one of which results in large series resistance (see Fig. 2.10(a)) and the other, results in an overlapping capacitance (see Fig. 2.10(b)). The series resistance limits the drain current. In RF applications, a half-fold reduction in the series resistance can yield a four-fold increase in the transconductance [26]; greatly increasing the transistor's cut-off frequency.

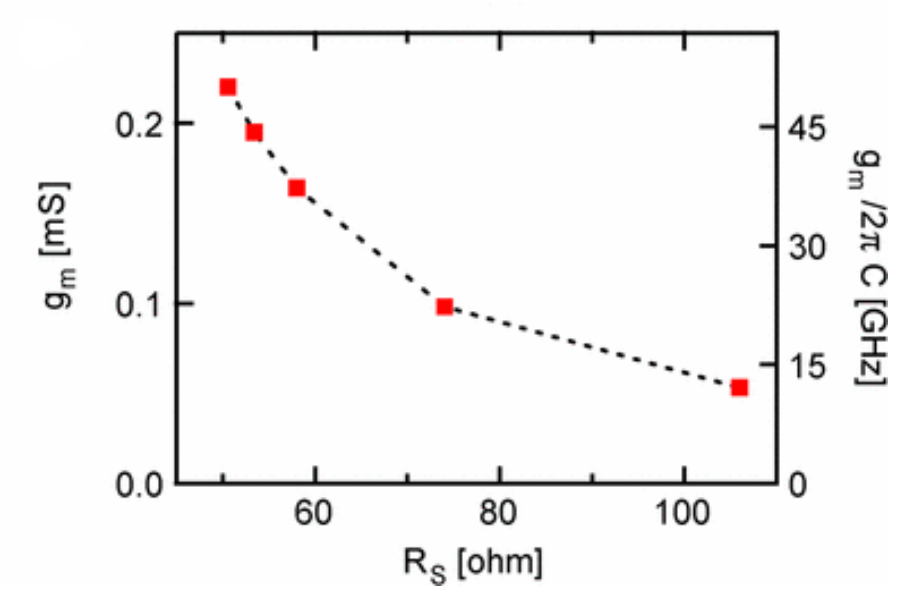


FIGURE 2.11: The transconductance and cut-off frequency versus the series resistance. Reprinted with permission from [26]. Copyright 2010, Rights Managed by IEEE.

The behaviour of the the transconductance, g_m, against the series resistance, is illustrated in Fig. 2.11. The measured g_m increases with a decrease in the series resistance. This illustrates the need to reduce the series resistance for high speed circuit applications.

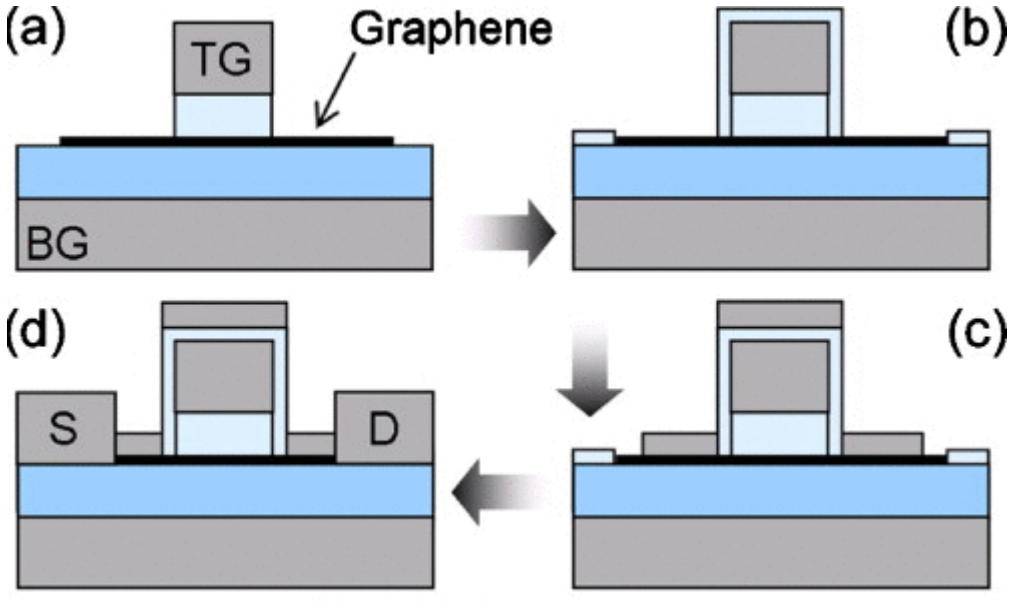
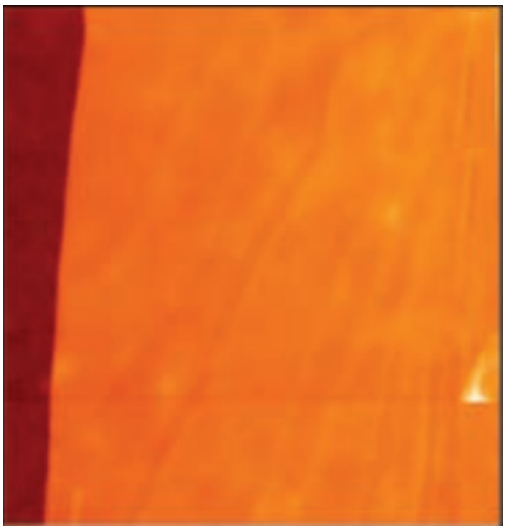


FIGURE 2.12: The fabrication process for a self-align graphene FET. Reprinted with permission from [70]. Copyright 2010, Rights managed by AIP Publishing LLC.

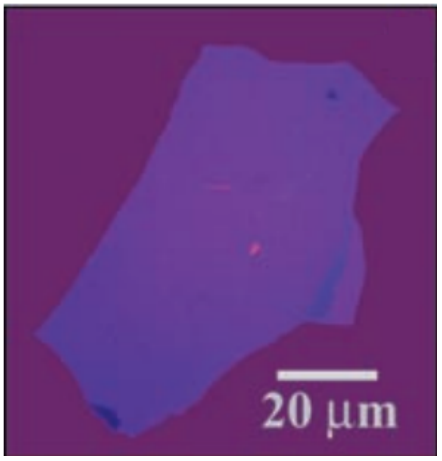
Research is on-going into using self-aligned techniques in the fabrication of graphene FET. Fig. 2.12 demonstrates one of the steps used in the fabrication process. Using the technique shown, an access length as low as 20nm has been achieved [70]. From Fig. 2.12(a), on the wafer, which is the back-gate (BG) and the BG oxide, graphene is deposited. On the deposited graphene, a top-gate (TG) oxide and a TG is deposited.

The idea of this is to used the formed active area to align the source (S) and drain (D) terminals. Next, a thin oxide layer is deposited as shown in Fig. 2.12(b). This thin oxide acts as a spacer between the TG to S/D terminals. The thin oxide is etched off where contact need to be make. That is, on the graphene channel and on the TG. From Fig. 2.12(c), metal is deposited and in Fig. 2.12(d) the S/D contacts are formed.

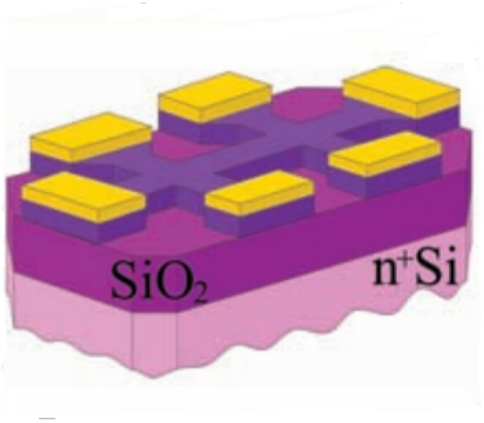
2.1.4 Channel Conductance



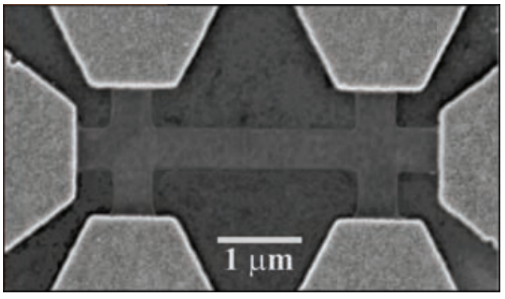
(a) Single-layer graphene with colour yellow-brown on a dark brown SiO_2 surface



(b) Multilayer graphene flake on an oxidized Si wafer



(c) Schematic of a graphene transistor



(d) Scanning electron microscope image of the graphene transistor

FIGURE 2.13: Device feature of the graphene transistor. Reprinted with permission from [14]. Copyright 2004, Rights Managed by American Association for the Advancement of Science.

On SiO_2, the a single-layer graphene flake has a distinguishing yellow-brown (see Fig. 2.13(a)) in contrast to the purple of a multilayer graphene flake with many layers as shown in Fig. 2.13(b). The colour is one of the indicators used to confirm the number of layers especially when fabricating a single-layer graphene transistor. The device

schematic is shown in Fig. 2.13(c) and its scanned electron microscope image in Fig. 2.13(d).

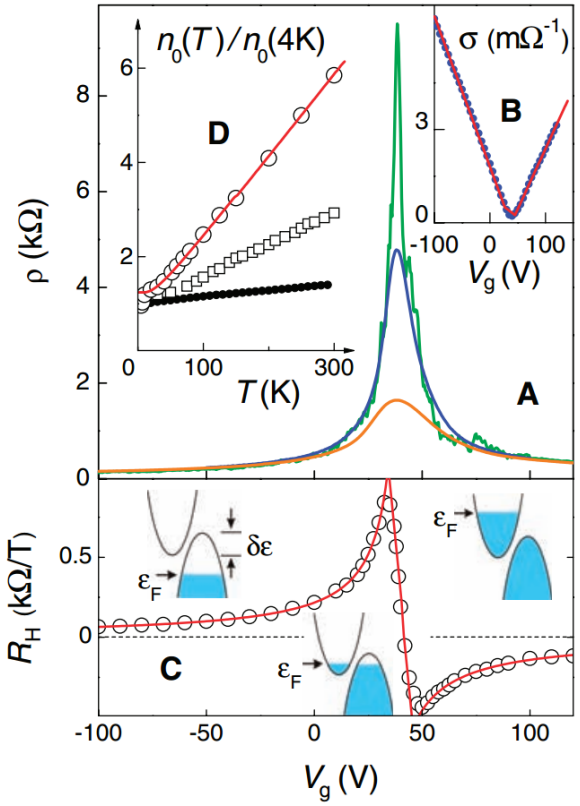


FIGURE 2.14: Transport characteristic of the field effect graphene (A) dependence of the resistivity on the gate voltage (B) A plot of the conductivity against the gate voltage (C) The Hall coefficient R_H versus the top-gate (D)The dependence of the carrier concentration on the temperature. ε_F is the Fermi energy and $\partial\varepsilon$ is the overlap between the conduction and valence bands. Reprinted with permission from [14]. Copyright 2004, Rights Managed by American Association for the Advancement of Science.

2.1.4.1 Conductance Against Changes in Gate Voltage

Using samples of the prepared films in Fig. 2.13, a study of the transport characteristics was carried out as shown in Fig. 2.14. The dependence of the resistivity ρ ($\sigma = 1/\rho$) on the gate bias V_g shows a peak resistance at a particular value of V_g regardless of the channel temperature. The respective temperatures are 5, 7 and 300 Kelvin from top to bottom. For a DC sweep of the gate voltage, an analysis of the Hall coefficient R_H gives an insight into the resistivity of the channel.

A sharp reversal of value of R_H is seen where the transistor shows a peak resistivity. This phenomenon indicates an ambipolar conduction. The carrier density of holes and electrons in graphene are in the order of $10^{13} cm^{-2}$ [14]. These carriers are electrostatically doped in the channel as a result of the capacitive coupling between the gate and

the substrate [71, 72, 73]. The electrostatic doping shows a linear relationship between the carrier density and the gate bias given by:

$$n = \epsilon_0 \epsilon V_g t_{ox} q \tag{2.10}$$

where n is the carrier density, ϵ_0 and ϵ are the permittivity of free space and SiO_2, t_{ox} is the thickness of SiO_2 and q is the electron charge. The charge density takes into consideration a minimum charge density due to impurities [74]. Doping the channel shifts the position of the Fermi energy which determines the transistor conductance.

Single-layer Conductance

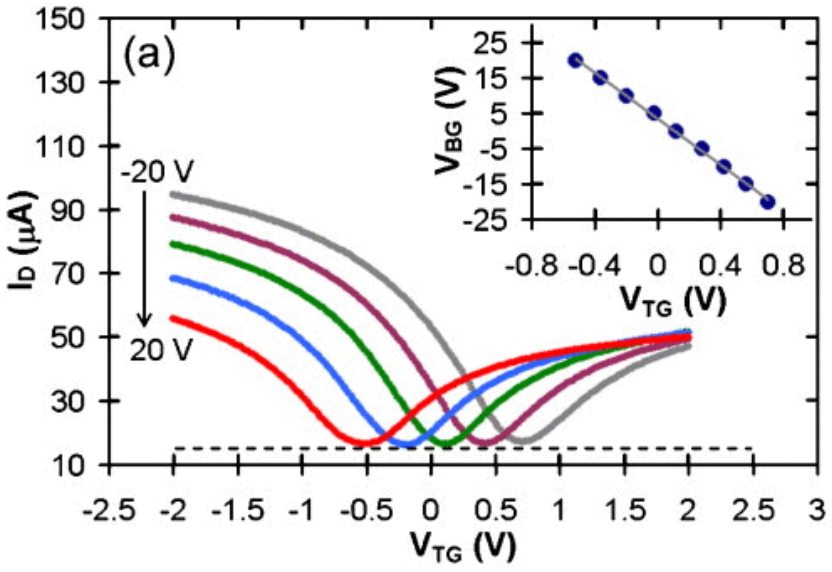


FIGURE 2.15: Electronic transport in single-layer graphene FET. Reprinted with permission from [70]. The transport characteristics of the top-gate voltage V_{TG} against the drain current I_D. Inset is the is relationship between V_{TG} and the back-gate voltage, V_{BG}. Copyright 2010, Rights managed by AIP Publishing LLC.

The single-layer shows the same level of the minimum current irrespective of the value of V_{bs}. Fig. 2.15 displays the current characteristics against variations in the gate voltage for steps in the back-gate voltage. Thus, V_{BG} only acts in the capacity of determining the threshold voltage. The threshold voltage, that is the value of V_{TG} at which the current is minimum, shows a linear relationship with V_{BG} (see inset in Fig. 2.15) [70].

A three port transistor with no back-gate is also being researched [75, 76]. In the three port transistor, only one threshold voltage is achievable.

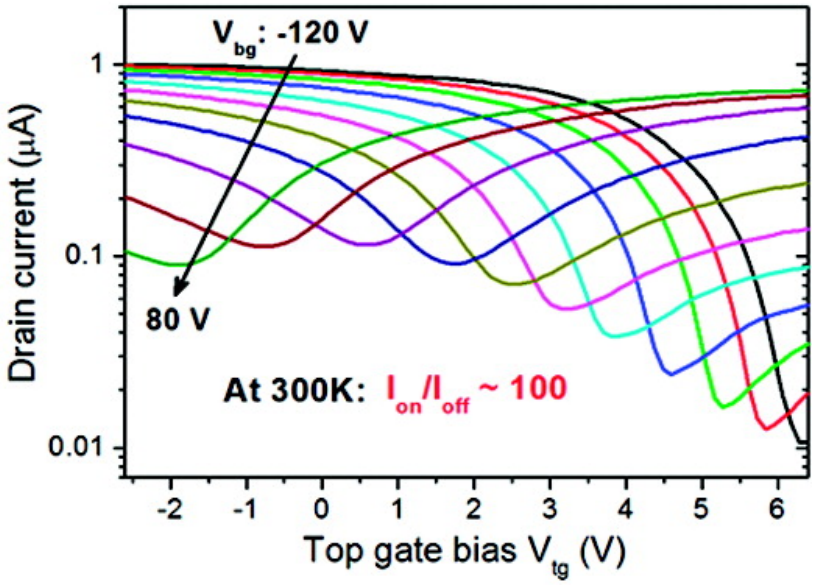


FIGURE 2.16: Electronic transport in bilayer graphene FET. Reprinted with permission from [77]. The transport characteristics of the top-gate voltage V_{tg} against the drain current for a sweep of the back-gate voltage V_{bg}. Copyright 2010, Rights Managed by American Chemical Society.

Bilayer Conductance

Unlike in the case of a single-layer, in the bilayer channel, the minimum current is dependent on V_{bs}. Fig. 2.16 shows an ambipolar current characteristics similar to that of the single-layer but the minimum current slopes downwards with an increase in the gate voltage from 0V. An increase in the on-off current ratio is observed with the lower values of the minimum current. The same threshold model used in the single-layer transistor has shown a good agreement for some bilayer transistors [33].

2.1.4.2 Drain Current Against Changes in Drain Voltage

Ambipolar conduction equally manifests in the drain current characteristics against changes in the drain voltage. For larger gate voltages, the characteristics appear similar to those of silicon MOSFETs. However, for lower gate voltages, it is evident that the graphene transistor has three regions of operation [53, 33, 78]. Fig. 2.17 displays the three regions indicated as regions I, II and III respectively. In the third region it is assumed that carriers are injected from the drain [33].

This phenomenon is not only peculiar to 2-D graphene transistors; ambipolar conduction has also been reported in carbon nanotubes, silicon nanowires and organic semiconductors [79, 80, 81, 82, 83].

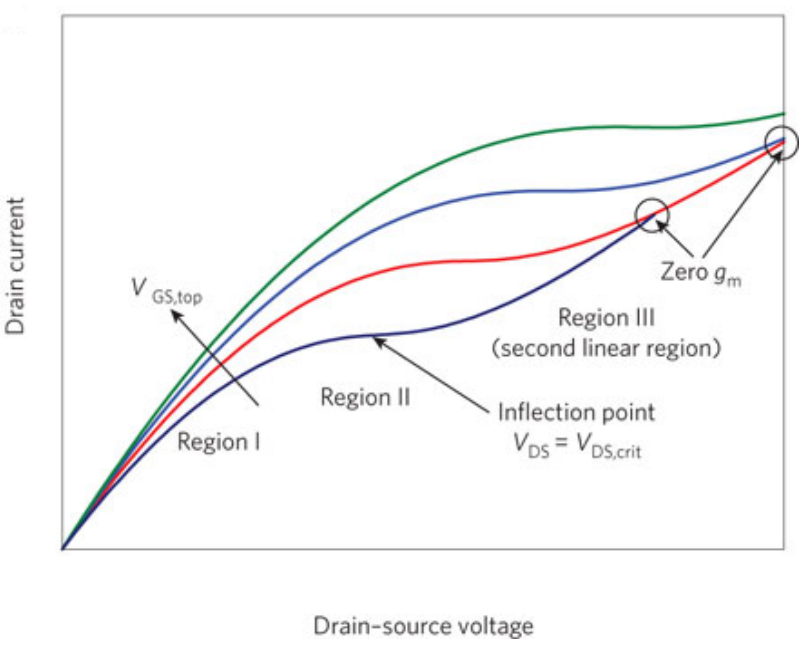


FIGURE 2.17: The regions of operation of a graphene transistor for variations in the drain voltage. Reprinted with permission from [53]. Copyright 2010, Rights Managed by Nature Publishing Group.

2.1.5 Quantum Capacitance

A large gate capacitance is undoubtedly good for the transistor as the gate voltage has more control over the electrostatically doped carriers. As the transistor is scaled into the nano regime, scaling the gate oxide naturally results in a higher gate capacitance and high-k dielectrics are equally used to prevent tunneling [84]. This large gate capacitance now becomes comparable with the quantum capacitance in the semiconductor. The quantum capacitance is essentially a measure of the energy required to pump in carriers from the source into the channel [45].

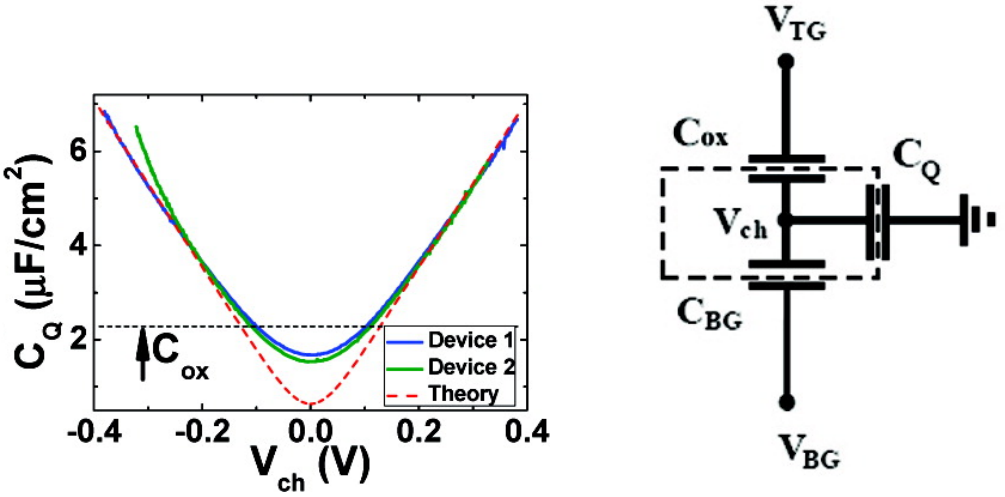
The quantum capacitance is derived from the two-dimensional gas model [86] shown in Eqn. (2.11):

$$C_Q = q^2 \frac{2k_B T}{\pi(\hbar v_f)^2} \log\left[2\left(1+\cosh\frac{qV_{ch}}{k_B T}\right)\right] \tag{2.11}$$

where V_{ch} is the surface potential of graphene, q is the electronic charge, $\hbar$ is the reduced Plank's constant and v_f is the Fermi velocity. Eqn 2.11 can be approximated to Eqn. (2.12) [87].

$$C_Q = q^2 \frac{2}{\pi} \frac{q|V_{ch}|}{(\hbar v_f)^2} \tag{2.12}$$

This equation applies irrespective of whether the gate is metallic [85] or an ionic electrolytic liquid which gives an electrochemical gate voltage [88]. Fig. 2.18(a) shows the



(a) Characteristics of the quantum capacitance against the gate voltage

(b) Schematic of the capacitance model

FIGURE 2.18: Interaction of the quantum capacitance in the graphene channel. Reprinted with permission from [85]. Copyright 2011, Rights Managed by American Chemical Society.

quantum capacitance dependence on the surface potential. Although the gate capacitance is constant, the effective capacitance that is responsible for modulation of the channel conductance varies with the quantum capacitance and is modelled in series with the quantum capacitance as shown in Fig. 2.18(b).

2.1.6 Thermal Transport

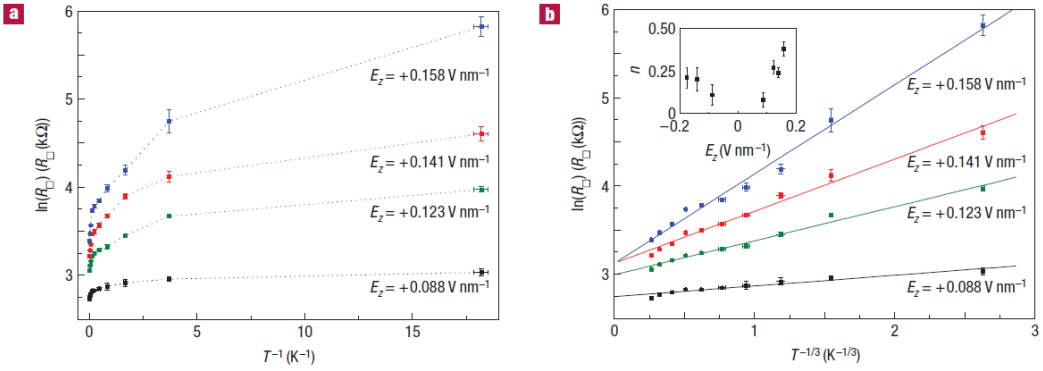


FIGURE 2.19: Thermal transport in bilayer graphene. Reprinted with permission from [89]. Copyright 2008, Rights Managed by Nature Publishing Group.

Currently graphene can operate at a range of temperatures from close to 0K to room temperature. In semiconductor devices the thermal transport of carrier gives insight to the band structure. Fig. 2.19 shows the relationship between the channel resistance and temperature. The relationship deviates from that seen in silicon devices given by the

equation $R = R_{intrinsic} \exp(\frac{E_g}{k_B T})$ but aligns better with models used in thermistors [90, 91].

2.2 Improving the Transistor

Despite the impressive electronic properties of graphene, research is on-going to develop a lithographic process whereby the charged impurities which makes graphene fall short in terms of the current ratio and reduces the off-current can be controlled. The impurities have been widely assumed not to emanate from the graphene itself, but assumed to be from other sources such as the presence of surface dangling bonds which form a coupling with graphene, resulting in either a hole or electron doping [92] and the substrate on which the graphene sits [65, 93].

A report reveals that the explanation of hole and electron puddles emerging from the extrinsic substrate only applies in the case of perfect graphene. That is, a suspended graphene which has no substrate will have no hole and electron puddles. As the chemical potential variation observed in graphene is probably due to charge impurities above and below the layer [94]. But both theory and experiment agree that the anomalous behaviour of a non zero minimal conductivity at a zero density of state can be explained by the presence of puddles. Both the substrate and the gate dielectric that sandwiches the graphene layer play a prominent role in improving the transistor behaviour. A number of gate dielectrics and dielectric substrates have been investigated [95, 96, 97, 98, 99].

2.3 Graphene Bandgap Engineering

Bare graphene is a semi-metal with a zero bandgap. The graphene sheet has a zero bandgap because the conduction and valence band touch at the K point in the Brillouin zone as can be seen in Fig. 2.3.

Having a bandgap is an essential feature in a semiconductor, and as such a number of techniques have been employed to open up a band gab in graphene. These techniques can be classified into two groups [100]: The methods that destroy the honeycomb structure and the methods that preserve the honeycomb structure.

2.3.1 Methods That Destroy the Honeycomb

This class includes graphene nanoribbons, graphene nanomeshes and chemical functionalization. The disadvantage of this method is that the FET suffers a reduction in both the carrier mobility and the on-state current as a result of destroying the honeycomb

structure. The destruction also introduces scattering centers, enhances the carrier effective mass and produces a non-tunable bandgap [100].

2.3.1.1 Graphene Nanoribbons

Slicing of the graphene sheet into one dimension nanoribbons as shown in Fig. 2.20 is being looked at as a technique of creating a bandgap. Consider that a single graphene hexacyclone structure has six K-points (refer to Figs. 2.2(b), 2.3(a), 2.3(b) and 2.3(c)). It is at this K- point that the conduction and valence bands touch. Outside the K-point an energy bandgap exists.

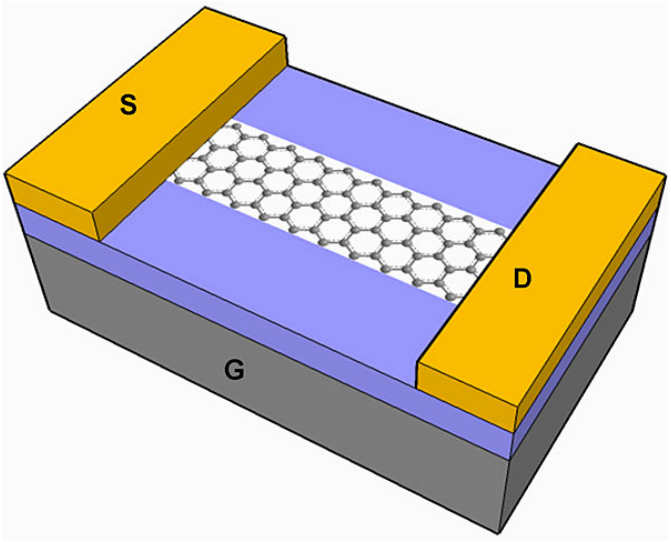


FIGURE 2.20: Schematic of graphene nanoribbon FET.

Slicing pristine graphene into nanoribbons confines the 2-D graphene into a 1-D graphene structure which gives rise to a finite bandgap [101, 52]. It is expected that the 2-D graphene energy dispersion will split into a number of 1-D modes [102]. Some set of 1-D modes will bypass the intersections where the valence and conduction bands touch giving rise to a finite bandgap. To achieve a high bandgap a narrow diameter of the ribbon is required. It has been reported that with a diameter of 5nm a corresponding bandgap of 0.5eV is expected [103].

A published report of sub-10 nm wide graphene nanoribbon field-effect transistors showed semiconducting properties with an Ion/Ioff ratio of up to 10^6, an on-state current density as high as $2000\mu A/\mu m$, a carrier mobility of approximately $200cm^2/Vs$ and a scattering mean free path of $10nm$ [104].

There are problems that hinder the use of nanoribbons for digital circuits;

- Nanoribbons are not compatible with the current complementary metal-oxide-semiconductor (CMOS) lithographic process [15].

- The lithographic process cannot guarantee accuracy for the diameter of the nanoribbons required to produce an acceptable bandgap [103]. To give graphene nanoribbons a high mobility compared to silicon it is expected that the bandgap is less than 0.5eV [105].
- An increase in the bandgap will degrade the carrier mobility [105, 102].
- The bandgap depends on how many 1-D modes pass through the intersection between the valence and conduction bands. Therefore, it is challenging to develop an analytical association between the bandgap energy and the diameter of the nanoribbon.

  Graphene nanoribbons have an electronic bandgap which depends on the orientation of the ribbon edges and the ribbon width which is similar to chirality in CNTs [105, 106]. However, the advantage of the graphene nanoribbon over the CNT is that for sub-10nm with an ultra-thin diameter ($d \leq \approx 2nm$) semiconducting properties are guaranteed [104].

2.3.1.2 Graphene Nanomeshes

While in the case of graphene nanoribbons a bandgap is opened by cutting the graphene material, in the case of graphene nanomesh (GNM) an array of nanoscale holes are punched into a single or few layers of graphene using a self-assembled block copolymer thin film as the mask template [107], as shown in Fig. 2.21.

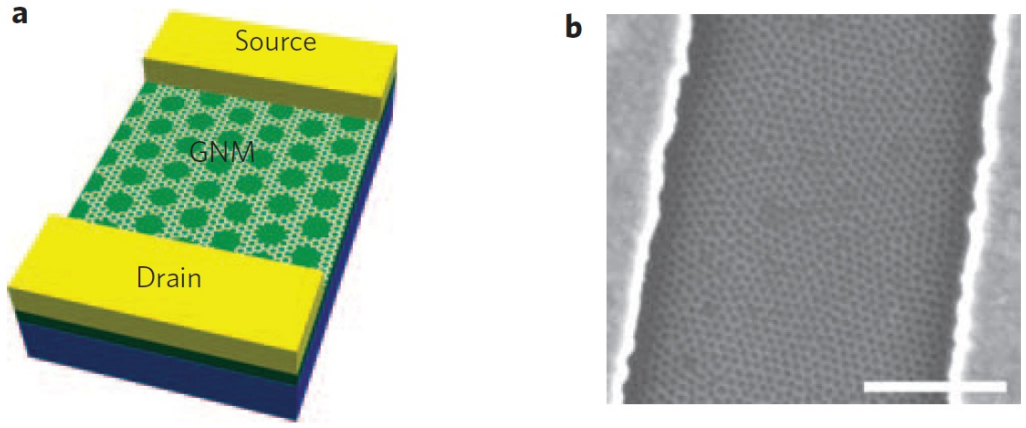


FIGURE 2.21: a) Transistor layout with graphene nanomesh b) SEM image of a GNM device. Reprinted with permission from [107]. Copyright 2010, Rights Managed by Nature Publishing Group.

Compared with graphene nanoribbons, nanomeshes have a comparable current on/off ratio but nanomeshes support higher currents than nanoribbon in the order of 100 times for a variable periodicity and a neck width as low as 5nm [107]. Periodicity is the distance between the centre of one nanohole to the center of an adjacent nanohole. Neck width is

the distance between the edges of the closest nanoholes. Controlling the periodicity and the neck width is important in controlling the electronic properties of the transistor.

This can be easily understood by looking at the nanomesh as various interconnections of nanoribbons. The width of the nanoribbon has been reported to influence the bandgap. Therefore, the transport characteristics are dependent on the current's critical pathway. Nanomeshes also have an added advantage that they are compatible with the current fabrication process.

2.3.1.3 Chemical Functionalization

In this method of bandgap engineering, chemical elements such as hydrogen [108] or fluorine [109] have been induced into the single-layered graphene flakes. In graphene, carbon is a two dimensional structure with sp_2 hybridization. As such, pristine graphene is a gapless material. The absence of a bandgap implies that there is a small resistance difference between the Dirac point voltage and the voltage of large carrier concentration areas. This translates to a low off/on current ratio. Therefore, by functionalization of graphene with suitable elements such as hydrogen and fluorine, the two dimensional sp_2 bonds will transform into three dimensional sp_3 bonds, resulting in an expected bandgap of 3.8eV and 4.2eV respectively[109]

The absorption of hydrogen into the graphene flakes alters its electronic properties, thereby presenting a means of altering the electronic behaviour of graphene. Although hydrogen barriers present a promising way to control the electronic property of graphene [110, 111], a report indicates that graphene conductivity due to hydrogenation is itself uncontrolled [110]. However, selective hydrogen absorption on graphene is being investigated [108].

In both cases of inducing graphene with fluorine and hydrogen, the electronic behaviour shows an increase in the on/off ratio, presenting a tunable electronic transport of graphene [112]. On the other hand, to be used in large scale electronics the degree of functionalization has to be controlled.

2.3.2 Methods That Preserve the Honeycomb

In these methods, the honeycomb structure of graphene is maintained, and as a result both the high carrier density and mobility is maintained. Techniques which open a bandgap and yet maintain the structure include; graphene substrate interaction, the application of strain and the application of an electric field.

2.3.2.1 Graphene Substrate Interaction

To open up a bandgap in graphene, perturbation has to be induced. In the case of graphene nanoribbon, cutting the graphene sheet breaks the translational symmetry thus introducing these perturbations. Another means of inducing perturbations is by breaking the A and B sublattice symmetry, which opens up a bandgap. Breaking the A and B sublattice symmetry in graphene was first reported by epitaxially growing graphene on a Silicon Carbide (SiC) substrate[113] resulting in energy bandgap as high as 0.26eV. This has been validated by various reports of substrate interactions when graphene is grown on Ni(111) [114], graphene is grown on boron nitrite substrate[115] with a bandgap of 53meV and suspended graphene on graphite substrate [116] with a bandgap of 10meV. The various bandgap energies of graphene on different substrates shows an interaction between the graphene π bonds and substrate bonds.

2.3.2.2 Strain Application

Strain is a process whereby the graphene structure is stretched. Strains can either be uniaxial or isotropic [117]. Uniaxial strain can be induced by bending of the substrate on which graphene lies thereby elongating the graphene structure. It has been reported that no significant bandgap opens for isotropic strain on graphene with the energy bands strongly dependent on the direction of the strain [117]. A set of reports of theoretical calculation from first principles using tight-binding description of graphene shows that strain graphene does not open up a bandgap [117, 118]. However, there is other work which reports the opening of a bandgap in asymmetrically strained graphene and a zero bandgap for symmetrically strained graphene [119, 120].

Fig. 2.22 shows an asymmetrically strained graphene perpendicular to the C-C bonds. The dispersion indicates a band opening in the strained graphene. This is due to the creating of an asymmetry in the layers. For about 1% strain a bandgap of up to 300meV is expected [120]. Fig 2.23 shows the relationship between the bandgap and an applied strain.

Recent work [121] into the effect of strain on the electronic properties of graphene reports that both single-layer and bilayer graphene show a change in their electronic properties. For single-layer graphene both the energy dispersion and the gapless characteristics were retained while there was a change in the Fermi velocity. However, for bilayer graphene the energy dispersion characteristic was retained while the direction of the strain could either enlarge or reduce its band overlap. Therefore, the strained graphene is equivalent to a vertical electric field by the strained layers [100].

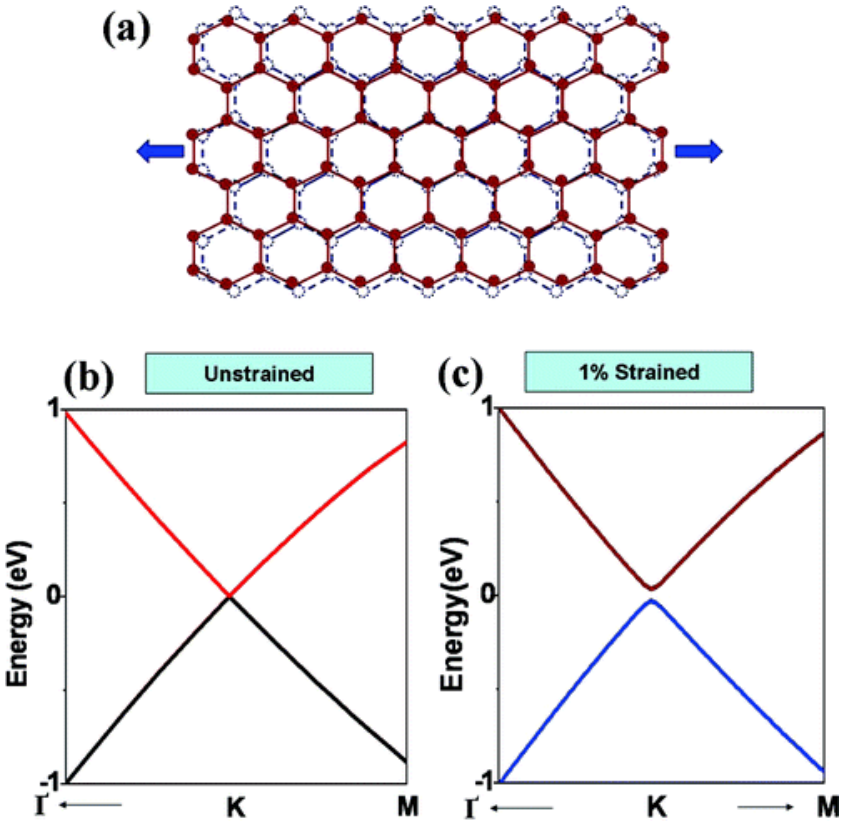


FIGURE 2.22: a) Uniaxial strain on multi layer graphene. Energy dispersion for b) unstrained and c) strained graphene. Reprinted with permission from [120]. Copyright 2008, Rights Managed by American Chemical Society.

2.3.2.3 Electric Field Application

Application of a vertical electric field can be used to break the sublattice symmetry. This method does not however apply to single-layer graphene (SLG) because the two sublattices remain equivalent under the vertical electric field as shown in Fig. 2.24. However, SLG on boron nitride layers as the substrate will open a tunable bandgap using an electric field [100] as is done for bilayer graphene (BLG). An electric field applied to a single-layer graphene SLG channel has been reported to open up a tunable bandgap, ranging from 0.16eV to 0.32eV for strong electric fields[100] when sandwiched between boron nitride.

In this method of bandgap opening, a transverse electric field is applied to a Bernal stacked bilayer graphene which renders the A and B sublattices non-equivalent [77, 89]. Fig. 2.25(a) shows the structure of a suspended bilayer graphene transistor and Fig. 2.25(b) shows the lattice structure. The bandgap opening works on the principle that a transverse electric field to the channel creates a strong coupling in the bilayer graphene. This strong coupling distorts the lattice symmetry (A_1 and B_2 in Fig. 2.25(b)) that exists thereby creating a bandgap [103]. Using this method, a bandgap opening as high as 300meV has been reported [77, 95].

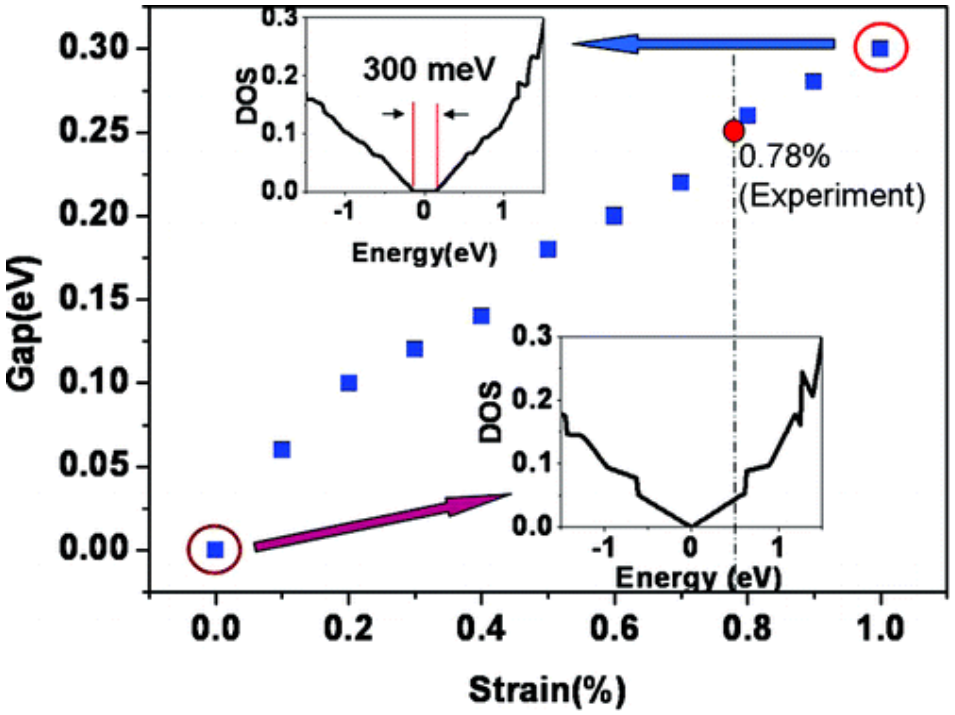


FIGURE 2.23: The predicted bandgap against the amount of uniaxial strain. Reprinted with permission from [120]. Copyright 2008, Rights Managed by American Chemical Society.

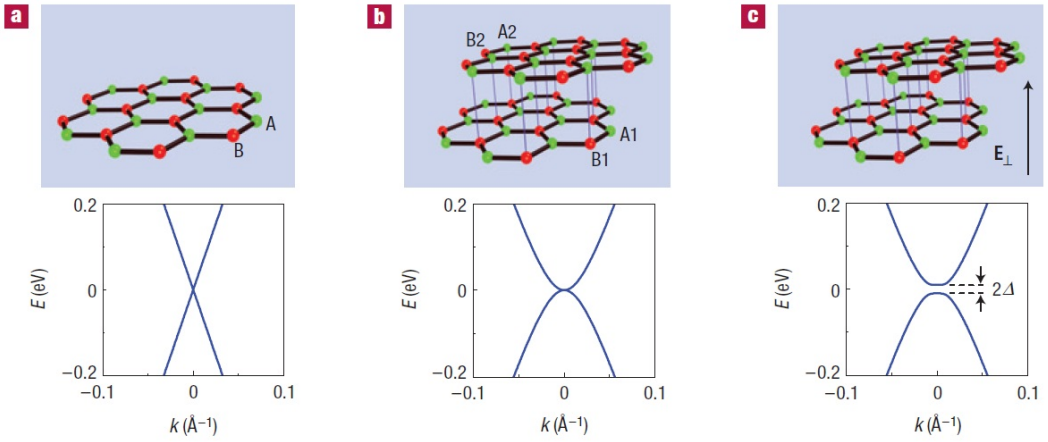
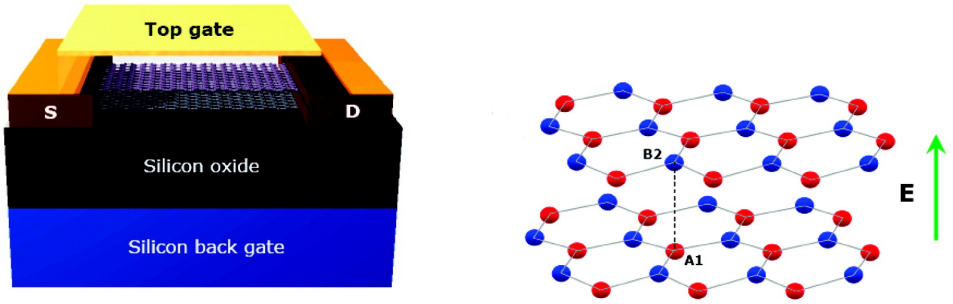


FIGURE 2.24: Energy dispersion and the sublattice structure for a) single-layer, b) bilayer graphene without electric field and c) bilayer graphene with vertical electric field applied. Reprinted with permission from [89]. Copyright 2008, Rights Managed by Nature Publishing Group.

This technique preserves the intrinsic properties of bilayer graphene and the bandgap created in this method is tunable. This method is compatible with the current CMOS lithographic process, making bilayer graphene a likely method for fabricating transistors targeted for digital circuits [15].



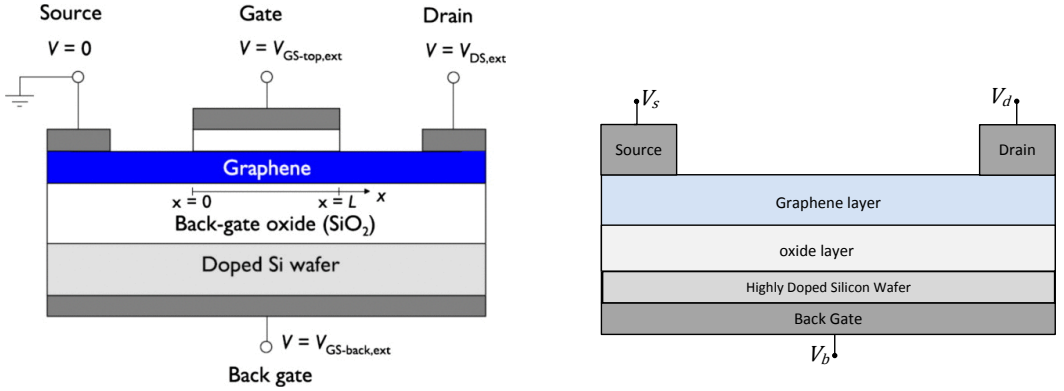
(a) Bilayer graphene field effect transistor (b) bilayer graphene lattice structure

FIGURE 2.25: Fabricated bilayer transistor and corresponding sublattice interaction. Reprinted with permission from [77]. Copyright 2010, Rights Managed by American Chemical Society.

2.4 Existing Graphene Device Circuit Models

Due to the absence of sufficient bandgap opening [95] only a small on-off current ratio is achievable thus limiting digital logic applications. However, this does not exclude analog and radio frequency (RF) applications, as there has been extensive research into graphene FET radio frequency performance [26, 27, 122]. Equally, RF models have been published with good f_{MAX} and f_T performance for some devices [123, 32, 124, 125, 126].

In addition to the growing research into RF performance, there have been a number of experimental results on the characterization of graphene transistors with respect to the drain DC current transport characteristics [77, 33, 127, 89]. The availability of experimental data as well as the need to design circuits has led to extensive research into compact models which supplement the RF models [33, 34, 128, 129, 130, 131, 132].



(a) The dual-gate graphene transistor layout. Reprinted with permission from [32]. Copyright 2010, Rights managed by AIP Publishing LLC.

(b) The single-gate graphene transistor layout

FIGURE 2.26: Schematic of the graphene transistor

The dual-gate transistor design (see Fig. 2.26(a)) has attracted a lot of attention in terms of modellings and experiments compared to the single-gate transistor (see Fig.

2.26(b)) because the former can have its threshold optimized by V_{bs} while the channel is modulated by V_{gs}.

2.4.1 Modelling Assumptions

Models of the graphene transistor use the drift equation to model the transport characteristic for both small signal and large signal. Some models assume a constant quantum capacitance in their calculation [33, 34] while others used the simplified quantum capacitance (see Eqn. (2.12)). No model has so far used Eqn. (2.11) in its calculations. By simplifying calculations of the channel charge, an analytical model has been reported for graphene [34].

Another assumption is the linear relationship between the threshold voltage, that is the voltage at charge neutrality, against the back-gate voltage for a dual-gate bilayer graphene transistor. This assumption has been supported by a number of experimental validations [33]. However, there is a report [131] and experimental measurement [77] that shows the linear relationship does not apply in all cases. This report models the threshold using a second order polynomial of V_{bs}.

A field dependent drift velocity derived from silicon has been used in graphene modelling as shown in Eqn. (2.13) [133, 134, 135]:

$$v_E = \frac{\mu E}{(1 + (\mu E / v_{sat})^c)^{1/c}} \tag{2.13}$$

where E is the electric field between the source and drain, μ is the carrier mobility, $v_{sat} = \mu E_c$ is the saturation velocity, E_c is the critical electric field and c is a characteristic constant. $1 \leq c \leq 2$ has been found to match experimental data [136, 137, 138] with $c = 1$ for holes and $c = 2$ for electrons. Models use equal values of c for both holes and electrons, while some use $c = 1$ which gives a simplified drift velocity, $c = 1.8$ has equally been used [130].

The series resistance shows a dependence of the charge doping between the contact and the graphene as well as the charge density of the un-gated area. Thus, it is expected that the source and drain side should have different series resistances [139]. However, all models assume equal series resistance at both ends.

2.4.2 Equivalent Circuit

The field effect graphene transistor derives most of its modelling technique from the way silicon is modelled. A similar derivation is the small signal model shown in Fig. 2.27

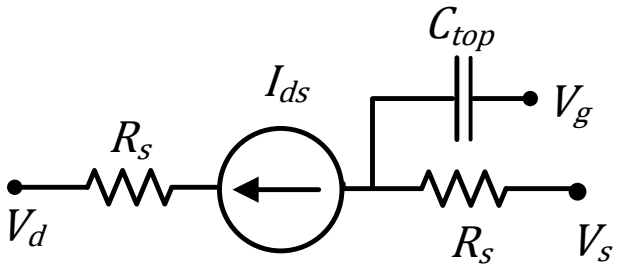


FIGURE 2.27: Graphene FET small signal model

C_{top} is the effective gate capacitance which takes into consideration the geometric gate capacitances and the quantum capacitance. C_{top} is dependent on the capacitance model used to model the graphene charge distribution. There are two widely used capacitance models, one is shown in Fig. 2.18(b) and the other is shown in Fig. 2.28

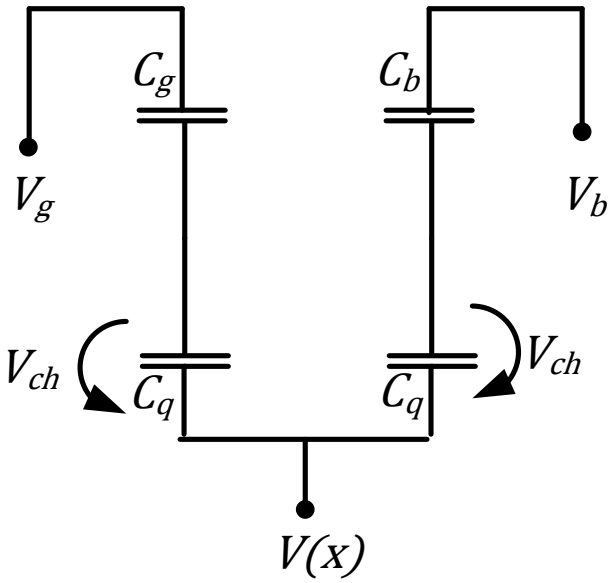


FIGURE 2.28: The capacitance model for a graphene FET. Reproduced with permission from [32]. Copyright 2010, Rights managed by AIP Publishing LLC.

2.4.3 Popular CAD Tools Used for Graphene Modelling

Computer-aided design plays a vital role in designing VLSI systems. Companies such as Accellera, Synopsys, Cadence and Mentor develop some of the most popular electronic design automation tools used nowadays. As the production volume of integrated circuits continues to increase and the need for production cost to reduce, CAD tools will always play a role in the development of electronic systems. The objectives for the use of CAD

tools include; shortening the design time, providing an accurately generated representation of the final system and performing complex design analysis in a very short amount of time [140]. They also provide an enabling environment for developers to optimize designs as well as a knowledge domain where concepts of the circuit components can be learned.

There are a number of CAD tools developed for circuit designs; some of which are commercial tools such as HSPICE [141] by Synopsys, VHDL-AMS by Mentor Graphics [142] implemented in the SystemVision simulator [143] and Verilog-AMS [144] by Accellera. The Berkeley SPICE CAD tool by University of California, Berkeley using the ngspice simulator [145] is open source.

Although, Mathematical Laboratory (MATLAB) is not used for circuit simulation, the MATLAB tool is used in the development of CAD libraries. MATLAB provides a convenience of drawing up the mathematical expressions that govern the physics of the transistor before implementing such expressions in electronic design tools.

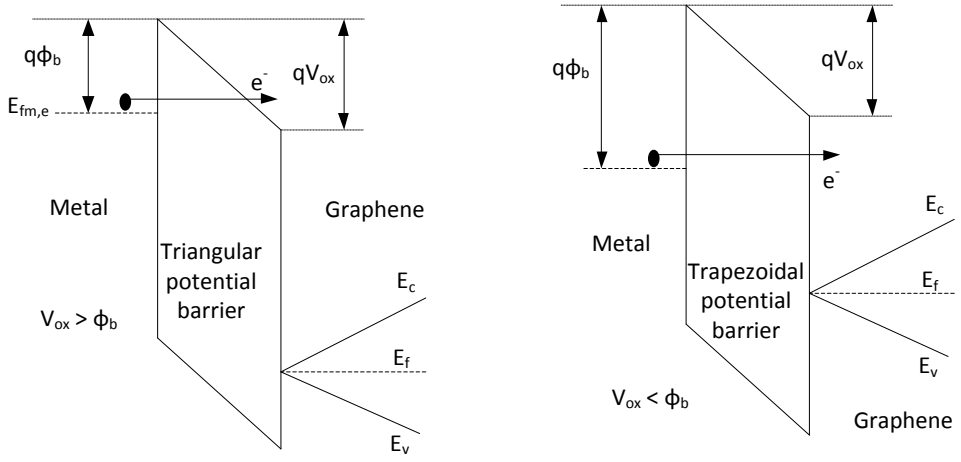
2.4.4 Tunneling Through Gate Oxides

Floating-gates were first reported in 1967 [146] and have since been widely used as a mechanism for nonvolatile data storage. They are charged by transferring electrons between the floating-gate and a terminal, such that a positive or negative charge can be induced in the floating-gate. Charge in the floating-gate interacts with the conductance of the transistor resulting in a threshold shift [147, 148].

With a high quality insulator, charges stored in floating-gates can stay permanently, hence providing long term memory. Estimates of 15 years have been reported for charges in a floating-gate [149]. Aside digital memory, floating-gates have been applied; to solve mismatches in temperature compensating transistors [150] and to optimize high precision amplifiers [151].

2.4.4.1 Mechanisms of Tunnelling

As semiconductor channel lengths are scaled into the nano-level, the required gate dielectric thickness has been further reduced such that 1.2nm - 1.5nm gate thickness were required for sub−100nm CMOS [152]. For ultra-thin gate oxides, having a potential drop of 1.8V can lead to large tunnelling current flow between the channel and the gate terminal. For a gate oxide as thin as 1.5nm [153, 154, 155], long channels have been reported to exhibit unusual electrical characteristics due to tunnelling, but not for shorter channels, indicating that an increase in area will result in a higher tunnelling current as shown in eqn. (2.14). There are two mechanism of electron tunneling through the gate oxide, namely Fowler−Nordheim (FN) tunneling and Direct tunneling.



(a) Fowler-Nordheim tunneling band diagram (b) Direct tunneling band diagram

FIGURE 2.29: Mechanisms for tunneling through the gate oxide

2.4.4.2 Electric Field Responsible For Tunneling

In FN tunneling the electrons tunnel through a triangular potential barrier into the conduction band of the oxide as shown in Fig. 2.29(a). This takes place when $V_{ox} > \phi_b$. Where V_{ox} is the oxide potential and ϕ_b is the conduction band potential barrier of the metal with respect to the oxide. Considering the case of direct tunneling shown in Fig. 2.29(b), the electrons tunnel when $V_{ox} < \phi_b$ through the forbidden bandgap of the oxide. Unlike FN tunneling, direct tunneling barrier is through the trapezoidal potential barrier. This mechanism of tunneling is predominant in short channels because the normally operate at $V_{ox} < \phi_b$. FN tunneling current is given by [156]:

$$J_{FN} = AE_{ox}^2 \exp\left(-\frac{B}{E_{ox}}\right) \tag{2.14}$$

where $A = \frac{q^3}{16\pi^2\hbar\phi_b}$, $B = \frac{4(\sqrt{2m_{eff}})\phi_b^{1.5}}{3q\hbar}$, electric field, $E_{ox} = \frac{V_{ox}}{t_{ox}}$, electronic chanrge, q, reduced Plank's constant, $\hbar$, oxide potential barrier, ϕ_b, electron effective mass, m_{eff} and oxide thickness, t_{ox}.

Direct tunneling is however limited to oxides thinner that 5nm because the tunnel probability for thicker oxides is small [157]. The direct tunneling current is presented in Eqn 2.15 [157].

$$J_{DT} = AE_{ox}^2 \exp\left[\frac{-B\left(1-\left(1-\frac{V_{ox}}{\phi_b}\right)^{1.5}\right)}{E_{ox}}\right] \tag{2.15}$$

A major challenge in the semiconductor industry was to find a suitable gate oxide to replace silicon dioxide (SiO_2). As transistors are scaled into the nano-level, gate oxides are made thinner therefore high permittivity oxides are required to reduce the electric field for a given charge. Thinner oxides are more susceptible to tunneling, as such, gate oxides with high barrier potentials are required to reduce the tunneling probability. Typical values of the a critical electric field beyond which tunneling should be expected range from 0.75/nm to 1.0V/nm [149, 158]. However, it has been reported for silicon dielectric compounds that an increase in the dielectric constant tends to lead to a reduction in the potential barrier [159].

2.4.4.3 Band Offset of Various Dielectrics

A variety of dielectrics and oxides are being considered such as hafnium oxide (HfO_2) [160, 161], aluminium oxide (Al_2O_3) and boron nitride (BN) to replace SiO_2 [162, 163] in a graphene based transistor. Al_2O_3 has been reported to have a conduction band offset of 2.73eV [164] for an 8nm thickness of the oxide with silicon and 3.5eV [165] for a 16.1nm thickness based on experimental analysis and an offset of 2.8eV [165] based on theoretical predictions. Similarly, HfO_2 with a thickness of 16.1nm has an experimentally calculated conduction band offset of 2.7eV [165] with respect to silicon while the theoretical calculation of 1.5eV [165] is predicted.

2.4.4.4 Work Function of Graphene

Graphene can be electrostatically doped by applying an electric field perpendicular to the channel. The electric field causes a Fermi level shift thereby changing the work-function of the channel giving graphene a tunable work- function. Work-function is the energy difference between the Fermi level and the vacuum level [133].

Therefore the barrier height of doped graphene is expressed as:

$$q\phi_b = q\phi_g \pm E_D \tag{2.16}$$

where $q\phi_g$ is the barrier height with no doping and the positive(negative) E_D is for holes(electrons). Carriers have an effective mass of $0.041m_e$ for electrons and $0.036m_e$ for holes [166].

On bare SiO_2 graphene has a work-function of 4.5eV [167]. Single-layer graphene and bilayer graphene show different work-functions of 4.57eV and 4.69eV respectively [168] with the work-function of bilayer graphene close to that of graphite [169].

Barrier height is defined as the difference between the electron affinity of the gate insulator and the work-function of the metal. Electron affinity is a measure of the energy

between the bottom of the conduction band and the vacuum level. Note that the work-function of a semiconductor is given by [133]:

$$\phi_S = X + \frac{E_g}{2q} \tag{2.17}$$

where qX is the electron affinity, E_g is the semiconductor bandgap. Barrier height can also determined by interface states. Eqn. (2.17) assumes two conditions, one that the interface states are a property of the semiconductor alone and independent of the metal and two, that there is an intimate contact between the metal and semiconductor, and the interfacial layer will be transparent to electrons but withstand the potential across it [133].

2.5 Graphene and World Economics

The reason graphene is so extensively researched is because of its prospective applications. Its electronic and physical properties are remarkable despite the absence of a bandgap and challenges in producing transistors with a small or zero mismatch in their transfer characteristics. Though graphene was first synthesised in 2004 [14] Fig. 2.30 shows patents in graphene related research date to as far back as year 2000.

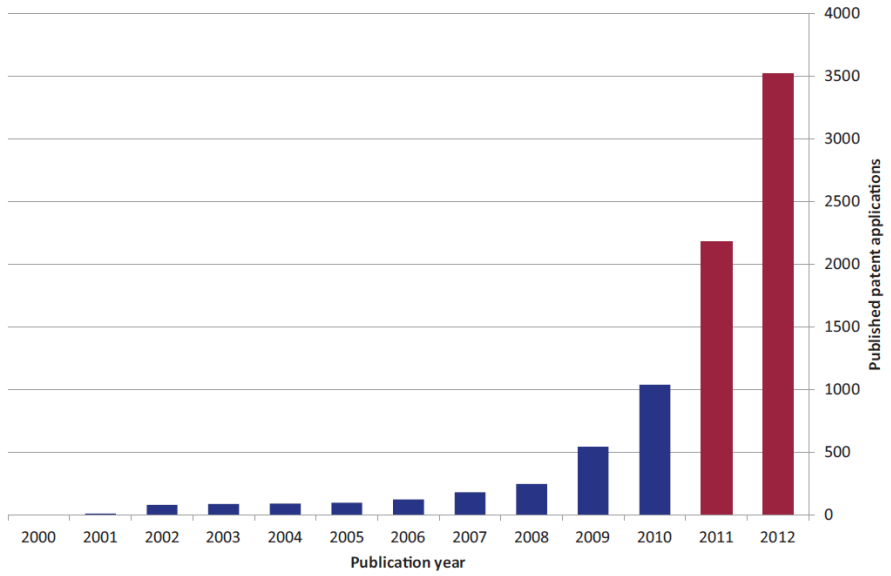


FIGURE 2.30: Worldwide published patents and year of application. Reprinted with permission from [170]. Copyright 2013, Rights managed by Intellectual Property Office.

However, from 2004 the application for patents have seen a steady rise to date with China leading the number of published patents. It is no surprise that the countries perceived to dominate the world markets are those reflected in promoting graphene research. This is supported by taking the 2012 gross domestic product report by the World Bank (see

Table 2.2) [171] and comparing it with number of published patents per country [170] shown in Fig. 2.31. China, United States and Germany which are the top most ranked countries in their continent are at the forefront in published patents.

TABLE 2.2: World Bank Gross Domestic Product 2012 [171]

Ranking	Country	millions of US dollars
1	United States	16,244,600
2	China	8,227,103
3	Japan	5,959,718
4	Germany	3,428,131
5	France	2,612,878
6	United Kingdom	2,471,784

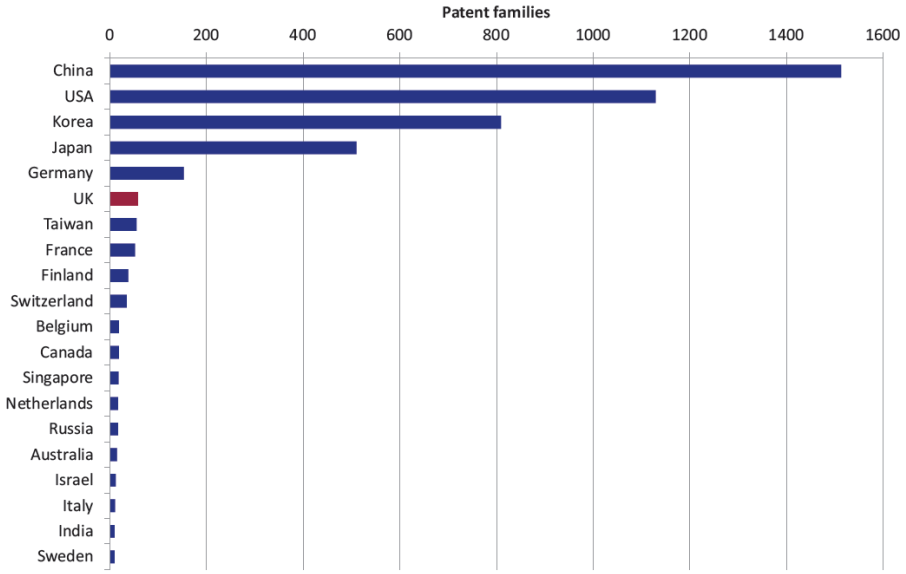


FIGURE 2.31: Worldwide published patents and year of application. Reprinted with permission from [170]. Copyright 2013, Rights managed by Intellectual Property Office.

This goes to prove that electronics is at the center of the world economies and the importance of prospective applications of graphene makes it tipped to be at the center of the electronics industry.

2.6 Graphene Based Applications

It will still be a while before graphene based electronics will be on the shelves of supermarket stores. Currently, researchers have successfully built graphene based applications. The absence of a bandgap favours analog and mixed signal applications.

2.6.1 Ring Oscillator

The ring oscillator is an important component in the semiconductor industry. It is composed of a circle loop of an odd number of inverters. An inverter is the fundamental building block of digital logic. Fig. 2.32 shows the design used to achieve a graphene based ring oscillator.

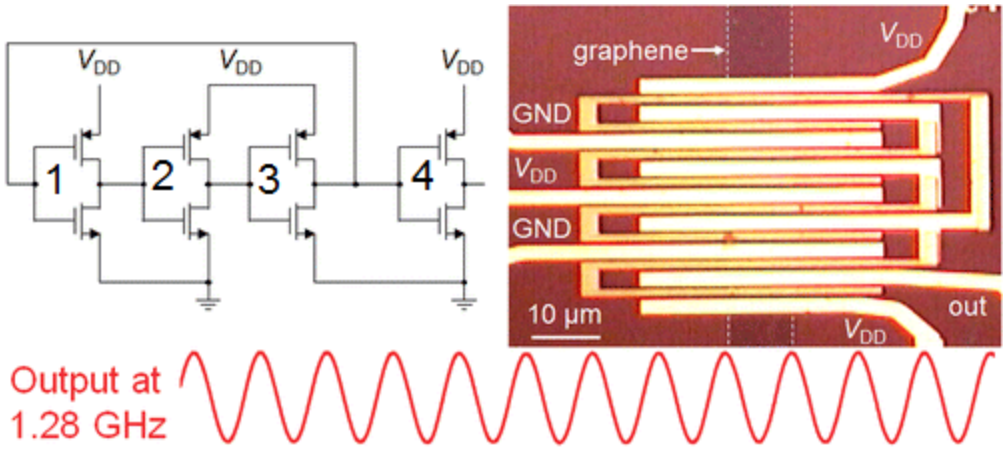


FIGURE 2.32: Schematic of a graphene ring oscillator. Reprinted with permission from [29]. Copyright 2013, Rights Managed by American Chemical Society.

So far only one graphene ring oscillator has been reported [29]. A fourth inverter is used in the design solely for decoupling the measurement device from the ring oscillator. A major problem in ring oscillator is parasitic capacitance which limits the switching frequency. Using various channel lengths the oscillator shows an increase in frequency with a decrease in length and voltage swing.

Fig. 2.33 shows the frequency against $L = 1\mu m$, $2\mu m$ and $3\mu m$. The frequency (voltage swing) of 350MHz (0.284V), 618MHz (0.208V) and 1.22GHz (0.136V) were obtained respectively. The highest frequency so far measured is 1.28GHz and the highest swing is 0.57V.

2.6.2 Frequency Mixer and Multipliers

Two radio frequency applications have been reported [172, 173, 174]. Both the frequency mixer and multiplier utilize the ambipolar nature of graphene to achieve its function. This is particularly interesting because the success achieved is hinged on the absence of a bandgap. Fig. 2.34 shows the circuit design for the frequency mixer. Fig. 2.35 shows both the layout and the working behaviour of the graphene frequency multiplier. In both cases the voltage at the minimum conduction is reference voltage.

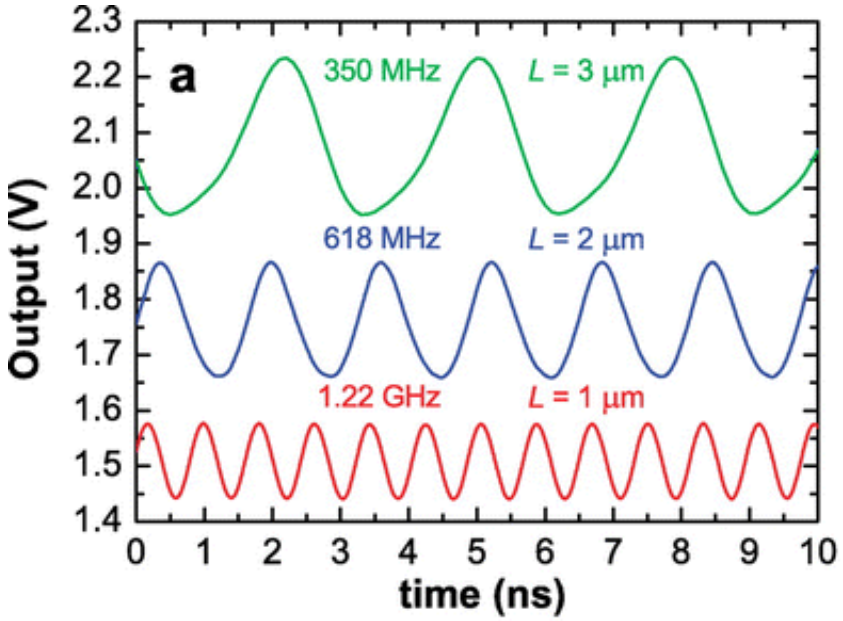


FIGURE 2.33: Operating frequency and output voltage for varying length. Reprinted with permission from [29]. Copyright 2013, Rights Managed by American Chemical Society.

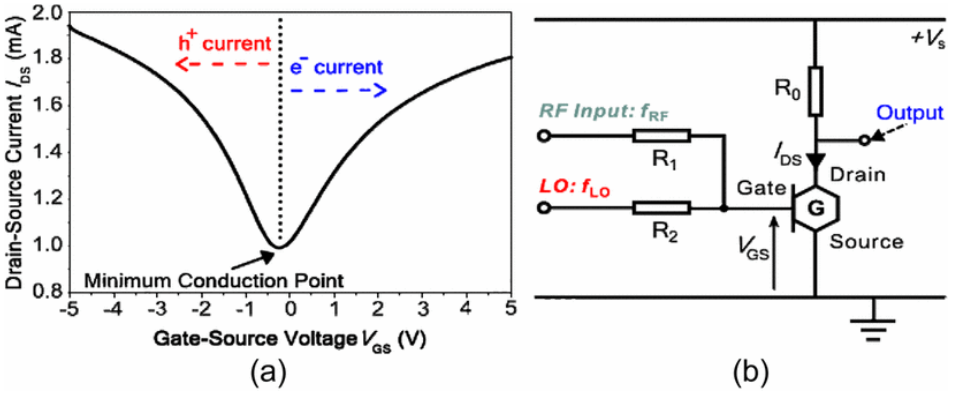


FIGURE 2.34: Operating frequency and output voltage for varying length. Reprinted with permission from [173]. Copyright 2010, Rights Managed by IEEE.

2.6.3 Digital Applications

Success has been achieved with cut-off frequencies of up to 300GHz [122]. For semiconductors to be used in digital circuits it is essential that they meet the following requirements[175]. Firstly, they should be able to be switched off otherwise it will not be possible to pull-up or pull-down to the respective power rails. Secondly, they should not suffer from excessive short channel effects and degraded electrostatics. Finally, the charge carriers should have a high mobility to allow for fast switching.

Graphene falls short of these requirements compared to silicon when deployed in digital circuits. Graphene, unlike silicon, does not have a bandgap, therefore the graphene transistor cannot turn off, resulting in a V-shaped output conductance [176].

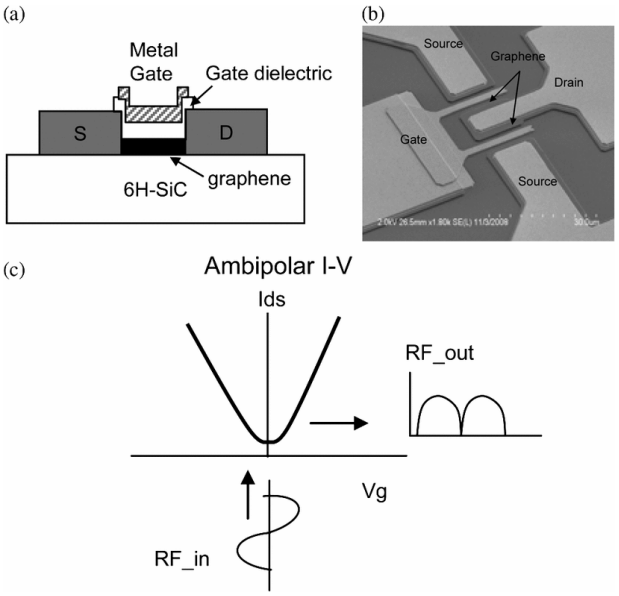
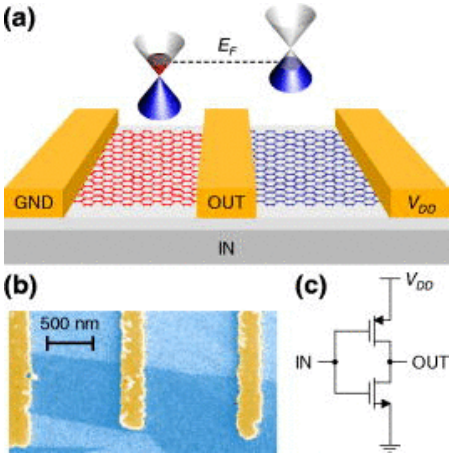


FIGURE 2.35: Mode of operation of graphene frequency multiplier. Reprinted with permission from [174]. Copyright 2011, Rights Managed by IEEE.

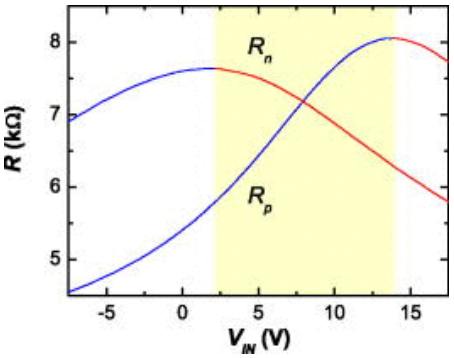
However, there are a number of reports of digital logic circuits based on the bilayer and single-layer graphene transistors [15, 177, 178, 179]. However, the inverter transfer characteristics are not symmetrical.

Fig. 2.36 shows the characteristics of a complementary monolayer graphene inverter. One transistor is made P-type and the other is made N-type (see Fig. 2.36(a)) splitting the charge neutrality of the inverter into two as show in Fig. 2.36(b). The region between both charge neutrality points is utilized to achieve the inversion characteristics. From Fig. 2.36(c) it can be observed that this region also has the highest output gain as such has also been utilised in designing voltage amplifiers [180, 181, 182, 183].

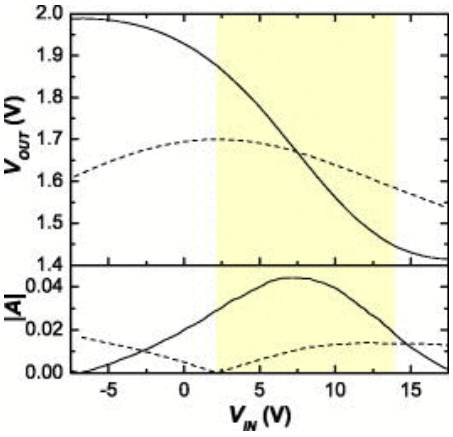
Analysing each transistor as a variable resistor, the output characteristics of the inverter is given by the potential that divides both resistors. Fig. 2.36(d) shows the inversion characteristic of the input signal. By setting the input signal at different frequencies, the output signal shows visible distortion for higher frequencies. This is due to charging and discharging parasitic capacitances.



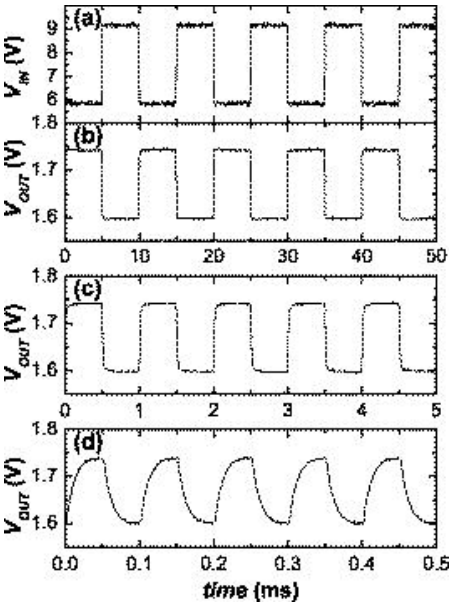
(a) Layout for a graphene complementary inverter



(b) Output conductances for both transistors



(c) Gain over the inversion characteristics



(d) Input and inverted output signal for the following frequencies: 100Hz, 1kHz and 100kHz (top to bottom) respectively

FIGURE 2.36: Properties of a graphene complementary inverter. Reprinted with permission from [178]. Copyright 2009, Rights managed by AIP Publishing LLC.

Chapter 3

Graphene FET drift-current perspective

This chapter presents a SPICE compatible general field effect transistor model with an analytical derivation of the carrier transport characteristics for both hole and electron conduction.

3.1 The Graphene Transistor

Fig. 3.1 shows a schematic of the transistor layout of a dual-gate graphene FET. Graphene is commonly placed on an already prepared silicon wafer, composed of an oxide, usually silicon-dioxide on a highly doped silicon substrate. The doped substrate forms the back-gate contact. An oxide can also be sandwiched between the graphene channel and a top-gate to form a dual-gate transistor. Each end of the channel is terminated by source/drain contacts.

Metal contacts are used with a graphene channel. Unlike graphene, in silicon FET the source/drain contacts are formed by ion implantation. Ion implantation makes the access area highly electrically conductive. The access area of a transistor is the region between the gate and the source/drain contact. The presence of an access area reduces parasitic overlapping capacitance but leads to a current limiting series resistance. However, in graphene, ion implantation introduces defects into the lattice structure.

Fig. 3.2 displays a circuit model for a dual-gate graphene transistor. C_{top} is the effective top-gate capacitance while C_{back} is the effective back-gate capacitance. They both account for the top-gate and back-gate oxide geometric capacitance along with the capacitance due to the carriers induced in the channel. Contact and access resistance on both the source and drain account for the series resistance and a current source accounts for the gate voltage controlled drain current.

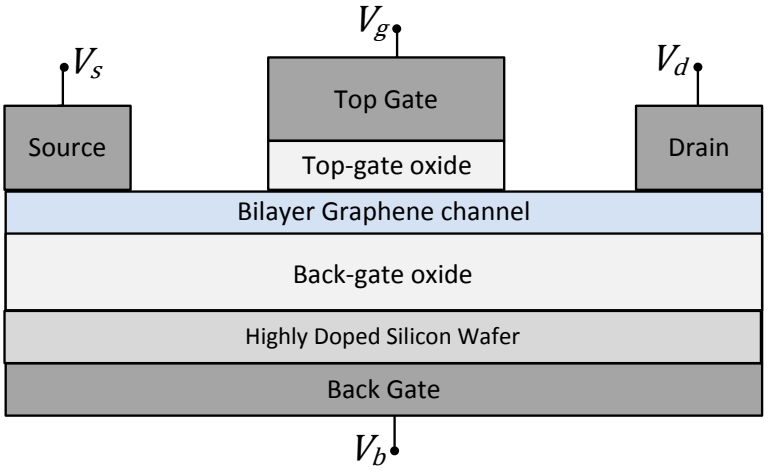


FIGURE 3.1: Schematic layout of the graphene field effect transistor

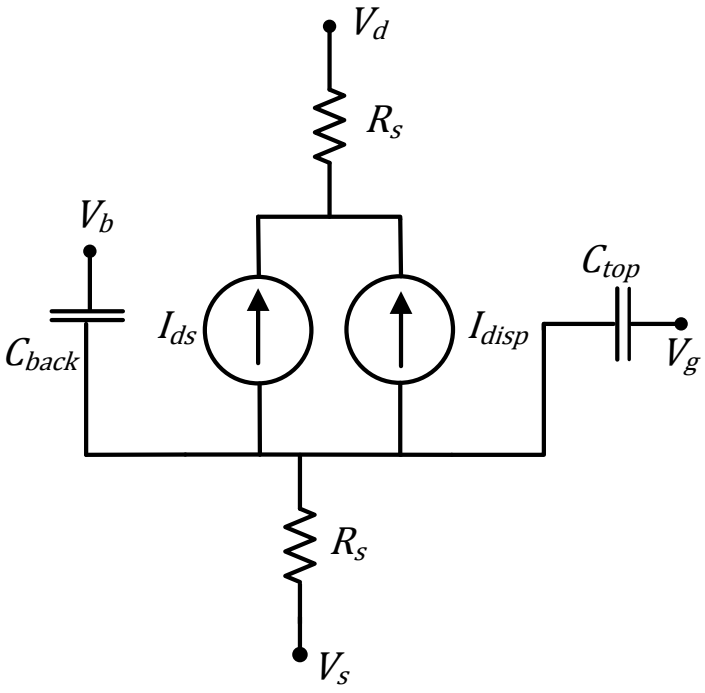


FIGURE 3.2: Proposed general circuit model schematic for the dual-gate graphene field effect transistor

All potentials are evaluated in reference to the source. V_d, V_g, V_s and V_b are the drain, top-gate, source and back-gate voltage respectively.

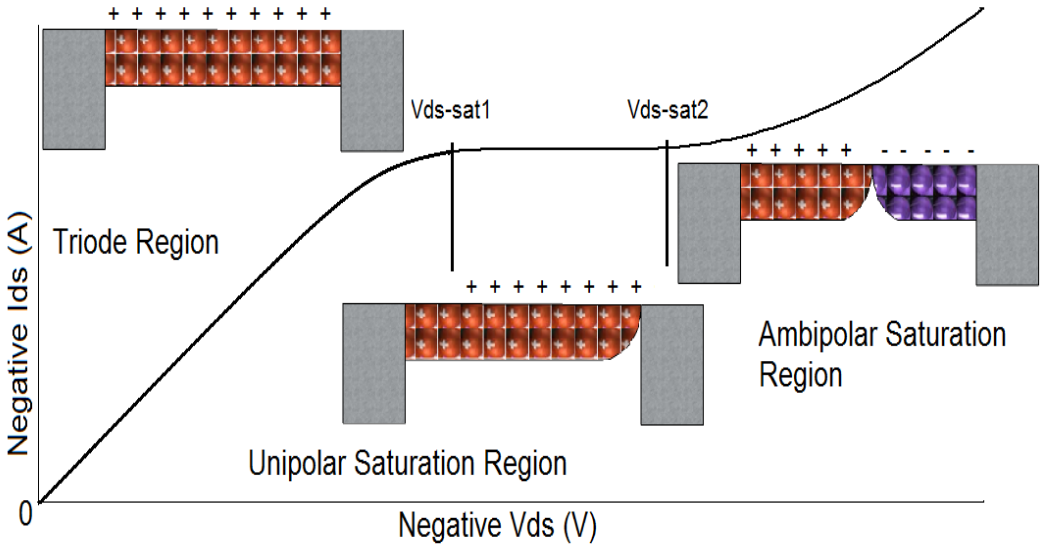


FIGURE 3.3: I-V characteristics showing the three regions identified as the triode region, the unipolar saturation region and the ambipolar saturation region along with the charge interaction in the channel.

In Fig. 3.3 the I-V characteristic of a graphene channel is divided into three regions: the triode region, the unipolar saturation region and the ambipolar saturation region. Carrier transport in the first two regions is unipolar, through either holes or electrons. In the unipolar saturation region the channel is pinched off at the drain end. Further, increase in the drain voltage bias enables transport in the channel to be performed by both electron and hole carriers. This region is referred to as ambipolar saturation region.

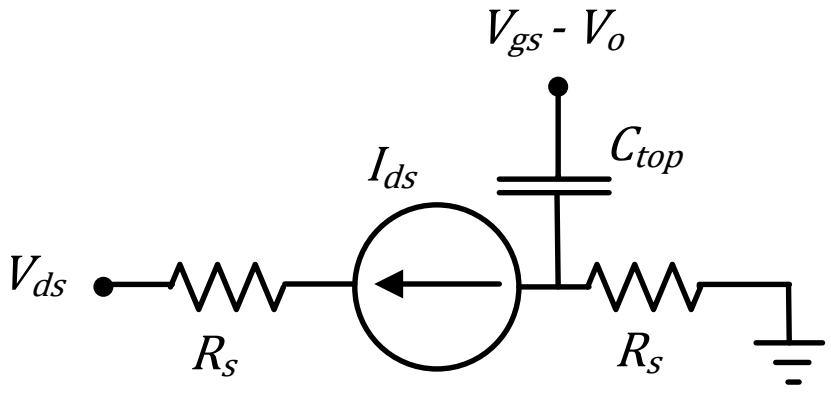


FIGURE 3.4: A proposed general graphene model for both single-gate and dual-gate field effect transistor. V_{bs} and C_{back} are represented by an offset voltage, V_o.

In graphene, ambipolar conduction means that the conduction medium can be electrostatically doped by hole-like or electron-like carriers. The convention adopted here is that the back-gate is responsible for doping the channel while the top-gate modulates the carrier conduction. Hence, V_b along with C_{back}, C_{top} and other in-built voltage offsets determines the threshold voltage, V_o of the transistor. The threshold voltage is the

top-gate voltage at which the channel will experience charge neutrality. Fig. 3.2 can be simplified to a single-gate model in Fig. 3.4. In the case of a single-gate model, V_o will be extracted from the transistor Dirac point voltage.

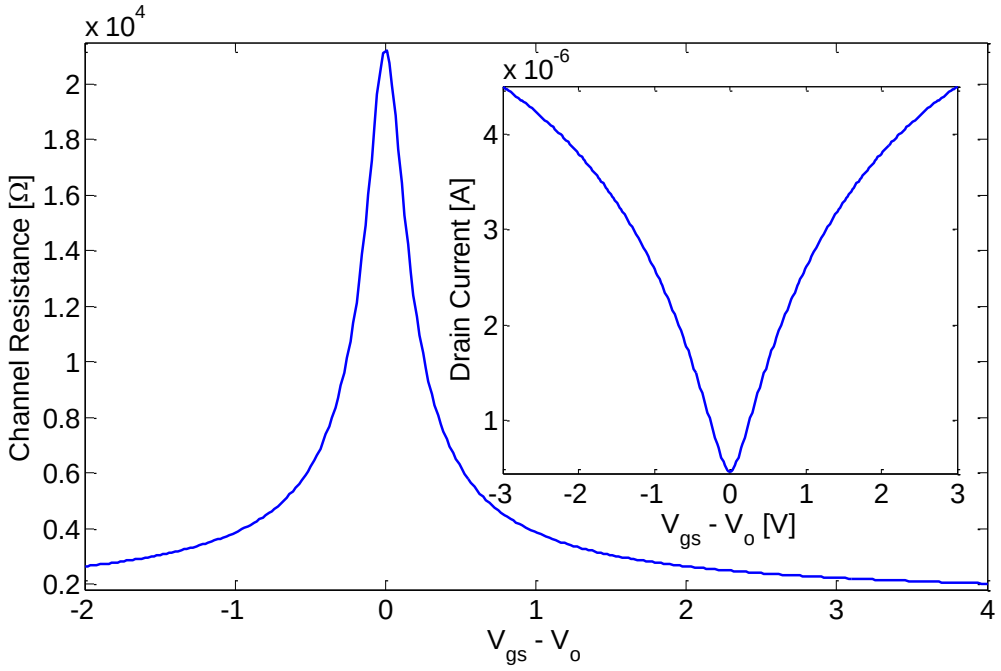


FIGURE 3.5: Transfer characteristic of a graphene channel field effect transistor

Due to the gapless nature of graphene in an intrinsic state, the graphene channel supports ambipolar transport. As such majority carrier conduction can be undertaken by both holes or electrons. A plot of the channel resistance against the top-gate voltage is shown in Fig. 3.5. Inserted in this figure is the plot of the drain current against the top-gate voltage. The negative half of the normalised top-gate voltage for both plots indicates that the majority carrier is hole-like while the positive half indicates electron-like carriers. Thus, the ambipolar conduction is observed to have a V-shape characteristic of conductance in respect to changes in V_{gs}.

Holes or electrons can be majority carriers depending on the top-gate bias, hence, in deriving the carrier transport using the drift-diffusion model, the hole conduction is derived separately from the electron conduction.

3.2 Hole Conduction

The voltage overdrive $(V_{gs} - V_o)$, indicates how the channel is doped. For hole conduction $V_{gs} - V_o < 0$. In this region with holes as majority carriers, the drain current characteristics with respect to changes in the drain voltage can be divided into three

sub regions namely; the triode, the unipolar saturation and tne ambipolar saturation regions.

3.2.1 The Triode Region

In field effect transistors the top-gate capacitance modulates the source potential barrier. As such the net charge density is:

$$Q(x) = -C_{top}(V_{gs} - V(x) - V_0) \tag{3.1}$$

where $V(x)$ is the channel potential at x. x is taken from the source to the drain. For clarity in presentation the C_{top} will not be shown as a function of the surface potential. The presence of an electric field between the source and the drain drifts carriers from the source to the drain results in I_{ds} which is represented by Eqn. (3.2) [134, 135]:

$$I_{ds} = -WQ(x)v_E(x) \tag{3.2}$$

where W is the channel width and $v_E(x)$ is the carrier drift velocity. As the drain voltage is increases, the lateral electric fields between the drain and the source equally increases resulting in the carriers saturating at a saturation velocity. Hence, the field dependent drift velocity is defined as [133]:

$$v_E = \frac{\mu E}{(1 + (\mu E/v_{sat})^c)^{1/c}} \tag{3.3}$$

where E is the electric field between the source and drain, μ is the carrier mobility, v_{sat} is the saturation velocity ($v_{sat} = \mu E_c$), E_c is the critical electric field and c is a characteristic constant. $1 \leq c \leq 2$ has been found to match experimental data [136, 137, 138].

Therefore in this model the parameter β has been introduced to Eqn. (3.3) to provide a realistic approximation when $c > 1$ and still produce a closed form analytical equation.

$$v_E = \frac{\beta\mu E}{1 + \mu E/v_{sat}} \tag{3.4}$$

$1 \leq \beta \leq 1.4$ is the boundary for $1 \leq c \leq 2$.

In this region the graphene FET shows a linear dependence on the drain-source voltage. Considering a series resistance (R_s), at both the source and drain terminals, the electric potential in the channel is $V(0) = I_{ds}R_s$ and $V(L) = V_{ds} - I_{ds}R_s$ for the source end

and the drain end respectively. This assumes that in Fig. 3.2 both series resistances are equal [139].

By applying the above equations and using an electric field of $E = -\delta V/\delta x$, the general current equation of this region is given by:

$$I_{ds} = \frac{-\beta W \mu \int_{V(0)}^{V(L)} C_{top}(V_{gs} - V_o - V(x))\delta V/\delta x}{\int_0^L \left[1 + \frac{\mu(-\delta V/\delta x)}{v_{sat}}\right]} \tag{3.5}$$

where L is the length of the active area of the channel, and

$$I_{ds} = \frac{1}{4R_s}\left[V_c - V_{ds} + 2Y\left(\frac{V_{ds}}{2} - V_{ov}\right) - \sqrt{\left(V_c + V_{ds} + 2Y\left(\frac{V_{ds}}{2} - V_{ov}\right)\right)^2 - 4V_c V_{ds}}\right] \tag{3.6}$$

where $V_c = Lv_{sat}/\mu$, $Y = \beta W v_{sat} C_{top} R_s$ and $V_{ov} = V_{gs} - V_o$ [34]

3.2.2 The Unipolar Saturation Region

The drain current as shown in Eqn. (3.6) has a quadratic relationship to the drain voltage. The turning point of the drain current with respect to the drain voltage defines the beginning of the saturation region. At the turning point $\delta I_{ds}/\delta V_{ds} = 0$.

Therefore, the drain voltage at the onset of saturation is represented by Eqn. (3.7).

$$V_{ds-sat1} = \frac{1}{(Y+1)^2}\left[2V_{ov}Y(1+Y) + (1-Y)\left(V_c - \sqrt{V_c^2 - 2V_c V_{ov}(Y+1)}\right)\right] \tag{3.7}$$

The resulting saturation current is shown in Eqn. (3.8).

$$I_{ds-sat} = \frac{Y}{R_s(1+Y)^2}\left[-V_c + (1+Y)V_{ov} + \sqrt{V_c^2 - 2(1+Y)V_c V_{ov}}\right] \tag{3.8}$$

As shown in Fig. 3.3 the saturation drain current (I_{ds-sat}) is constant throughout this region. Although the hole carriers saturate at $V_{ds-sat1}$, the drain end of the channel may not experience charge neutrality at this potential.

From Eqn. (3.1) the drain end will have a zero charge at $V_{ds} = V_{gs} - V_o$. Assuming that there is a linear charge progression between $V_{ds-sat1}$ and V_{ov}, where $V_{ov} = V_{gs} - V_o$. The charge between these two voltages is shown in Eqn. (3.9).

$$Q_{dep} = -\frac{C_{top}}{2}(|V_{ov} - V_{ds-sat1}|) \tag{3.9}$$

At the end of this region Q_{dep} has to be overcome. The voltage $V_{ds-sat2}$ marks the end of the unipolar saturation region and the charge between $V_{ds-sat1}$ and $V_{ds-sat2}$, $-C_{top}(V_{ds-sat1} - V_{ds-sat2})$ should thus be equal to Q_{dep}. Hence, the second boundary point of the unipolar saturation region can be calculated using Eqn. (3.10).

$$V_{ds-sat2} = V_{ds-sat1} - \frac{1}{2}(|V_{ov} - V_{ds-sat1}|) \tag{3.10}$$

At this point the channel is pinched-off as illustrated in Fig. 3.3.

3.2.3 Ambipolar Saturation Region

In the first and second regions the channel is unipolar and the carrier transport is by holes. An additional increase in the drain voltage pushes the charge neutrality at the drain end deeper into the channel, towards the source. As a result electrons are injected into the channel from the drain end. Rather than having a depleted region between the point of pinch-off and the drain terminal with fixed negative charges, these electrons are mobile. This is as a result of a zero bandgap in 2D graphene and the phenomenon is known as ambipolar transport [33].

L' to denote the position of the pinch-off region in the channel with respect to the source terminal. From Eqn. (3.1), with $V(L') = V_{ds-sat2}$, the charge at the point of pinch off is represented by Eqn. (3.11).

$$Q(L') = -C_{top}(V_{gs} - V(L') - V_o) \tag{3.11}$$

The potential in the channel at the drain end is $V(L) = V_{ds}$. Thus, Eqn. (3.12) is the corresponding charge at the drain end.

$$Q(L) = -C_{top}(V_{gs} - V(L) - V_o) \tag{3.12}$$

As the charge in the channel is conserved, the injected charge is $Q_d = Q(L) - Q(L')$, as expressed in Eqn. (3.13) and Eqn. (3.14) respectively.

$$Q_d = -C_{top}(V_{ds} - V_{ds-sat2}) \tag{3.13}$$

$$\frac{\partial Q_d}{\partial V_{ds}} = -C_{top} \tag{3.14}$$

For a drift velocity of $\mu_n \frac{dV}{dx}$. μ_n is the mobility of the alternative carriers. This may not be equal to the mobility used in the triode region. Integrating Eqn. (3.2) using Eqn. (3.14) gives rise to Eqn. (3.15).

$$I_{disp} = -\frac{W\mu_n Q_d^2}{2L(C_{top})} \tag{3.15}$$

Hence, from Eqns. (3.13) and (3.15) the saturation displacement current present when the transistor enters this region is shown in Eqn. (3.16).

$$I_{disp} = -\frac{W}{2L}\mu_n(C_{top})V_{ds-sat2}^2\left(\frac{V_{ds}}{V_{ds-sat2}} - 1\right)^2 \tag{3.16}$$

The charge in the channel between the source and the charge neutrality point is equivalent to the charge at the onset of saturation. This charge yields the saturation current in Eqn. (3.8). In addition, the charge between the pinched off point and the drain, namely the depletion charge, Q_d, gives rise to the saturation displacement current in Eqn. (3.16).

Therefore, the total current flowing in the channel (I_{ds}) is the algebraic sum of the saturation current, Eqn. (3.8), and the saturation displacement current, Eqn. (3.16).

$$I_{ds} = I_{ds-sat} + I_{disp} \tag{3.17}$$

3.3 Electron Conduction

In this section, the transport behaviour when V_{ds} is positive is considered. From Fig. 3.5 electron conduction occurs when $V_{gs} > V_o$. As previously shown for hole conduction, electron conduction is composed of three regions namely; the triode region, the unipolar saturation region and the ambipolar saturation region. The characteristics of each of these regions are as shown in Fig. 3.3, with I_{ds} and V_{ds} positive, in this case of electron conduction.

3.3.1 The Triode Region

Field effect transistors have both horizontal and vertical electric fields. The vertical electric field is used to modulate the channel carrier drifted from the source to the drain by the horizontal electric field. So, the vertical electric field will induce a net charge density in the channel represented by Eqn. (3.18).

$$Q(x) = -C_{top}(V_{gs} - V_o - V(x)) \tag{3.18}$$

This net charge is responsible for the drain current in Eqn. (3.19) that will flows from the drain terminal to the source terminal.

$$I_{ds} = -WQ(x)v(x) \tag{3.19}$$

From Eqn. (3.19), W is the channel width and $v(x)$ is the drift velocity for a length x from the source to the drain. The drift velocity is expressed in Eqn (3.20):

$$v(x) = \frac{-\beta\mu E}{1 + |E|/E_c} \tag{3.20}$$

where $E = -\delta V/\delta x$ is the horizontal electric field. As previously demonstrated for hole conduction, an equal series resistance is assumed for both the source and drain. Therefore, the electric potential at the source is $V(0) = I_{ds}R_s$ and the potential at the drain end is $V(L) = V_{ds} - I_{ds}R_s$. Hence, the drain current in this region is shown in Eqn. (3.21):

$$I_{ds} = \frac{\beta W\mu \int_{V(0)}^{V(L)} C_{top}(V_{gs} - V_o - V(x))\delta V/\delta x}{\int_0^L \left[1 + \frac{\mu(\delta V/\delta x)}{v_{sat}}\right]} \tag{3.21}$$

or;

$$I_{ds} = \frac{1}{4R_s}\left[V_c + V_{ds} - 2Y\left(\frac{V_{ds}}{2} - V_{ov}\right) - \sqrt{\left(-V_c + V_{ds} + 2Y\left(\frac{V_{ds}}{2} - V_{ov}\right)\right)^2 + 4V_cV_{ds}}\right] \tag{3.22}$$

where $V_c = Lv_{sat}/\mu$, $Y = \beta W v_{sat} C_{top} R_s$ and $V_{ov} = V_{gs} - V_o$

3.3.2 The Unipolar Saturation Region

Eqn. (3.22) holds for $V_{ds} < V_{ds-sat1}$ where $V_{ds-sat1}$ is the drain voltage at the onset of saturation. At this voltage the current is said to be saturated. Therefore, the saturation voltage is calculated by differentiating I_{ds} with respect to V_{ds} at the turning point.

$$V_{ds-sat1} = \frac{1}{(Y+1)^2}\left[2V_{ov}Y(1+Y)+ (Y-1)\left(V_c - \sqrt{V_c^2 + 2V_cV_{ov}(Y+1)}\right)\right] \tag{3.23}$$

Thus the resulting saturation current is shown in Eqn. (3.24).

$$I_{ds-sat} = \frac{Y}{R_s(1+Y)^2}\left[V_c + (1+Y)V_{ov} - \sqrt{V_c^2 + 2(1+Y)V_cV_{ov}}\right] \tag{3.24}$$

To calculate the discontinuity in the drain current characteristics between the ambipolar and unipolar saturation regions, Eqn. (3.9) gives the charge to be overcome at the onset of ambipolar activity. Also, $-C_{top}(V_{ds-sat2} - V_{ds-sat1})$ is the charge at the drain end at which this charge is overcome. Here, $V_{ds-sat2}$ indicates the voltage beyond which the Eqn. (3.24) no longer holds.

$$V_{ds-sat2} = V_{ds-sat1} + \frac{1}{2}(|V_{ov} - V_{ds-sat1}|) \tag{3.25}$$

3.3.3 The Ambipolar Saturation Region

In this region the channel conduction is due to both electrons and holes and a second linear drain current is experienced with an increase in the drain voltage. Similar to the analysis carried out for hole conduction, by considering Eqn. (3.11 - 3.14) for a drift velocity given by $-\mu\frac{\delta V}{\delta x}$, the saturation displacement current is shown below.

$$I_{disp} = \frac{W}{2L}\mu_n(C_{top})V_{ds-sat2}^2\left(\frac{V_{ds}}{V_{ds-sat2}} - 1\right)^2 \tag{3.26}$$

The total current flowing in the channel when the transistor enters this region is the superposition of the saturation current and the saturation displacement current. Consequently, the total current flowing in the channel is the algebraic sum of the saturation

current, Eqn. (3.24), and the saturation displacement current, Eqn. (3.26) as stated in Eqn. (3.17).

3.4 SPICE Jacobian Entries

The Jacobian entries in SPICE is a matrix of first order partial derivatives. The derivatives with from the matrix are the conductance, the transconductance and the bulk transconductance.

The output conductance is defined as the variation in the drain current with a small variation in the drain-source voltage while keeping the gate-source voltage constant.

$$g_{ds} = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs},V_{bs}} \tag{3.27}$$

The transconductance is defined as the drain current variation with a gate-source variation while keeping the drain-source voltage constant. This is given by

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds},V_{bs}} \tag{3.28}$$

The bulk transconductance measures the amount of drain current increase caused by the increment in the back-gate bias while the gate-source and drain-source voltages are constant

$$g_{mb} = \left.\frac{\partial I_{ds}}{\partial V_{bs}}\right|_{V_{gs},V_{ds}} \tag{3.29}$$

Using these derivatives SPICE calculates the voltage across each node of the transistor and the current flowing through the each node.

3.5 Summary

This chapter presents a SPICE-compatible dc model for both dual-gate and single-gate graphene transistors. Analytical equations have been derived for the drain transport of both hole and electron conduction. In both modes of conduction the current characteristics are divided into three regions with derived voltage boundary conditions. The Jacobian entries are continuous across the region boundaries.

A saturation displacement current that models the drain current behaviour in the ambipolar saturation region has been derived. By superimposing the saturation displacement current and the unipolar saturation current the model comprises the total drain current, thus confirming the theory of ambipolar transport in graphene.

Chapter 4

Single-Layer graphene FET model for circuit simulation

This chapter presents a model for both a dual-gate single-layer graphene field effect transistor (GFET) and a single-gate single-layer graphene FET. Here, the model investigates the temperature dependence of the single-layer transistor, its drain transport characteristics and the conductance transfer characteristics, and then compares the model with the carrier behaviour of multi-layered channels.

4.1 Dual-gate Single-Layer

A dual-gate transistor has a distinguishing feature of shifting the threshold voltage of the transistor using the electric field between the gates. Two models are presented, one is a compact model based on closed form analytical equations and the other is a numerical model. A SPICE implementable general model has been developed for both hole and electron conduction, presented earlier in Chapter 3. This chapter only maps the single-layer specific models for both cases to the general model to calculate the drain current. The corresponding drain transport characteristics are used for validate against experimental data.

4.1.1 Electrostatics

Currently, graphene transistors use metallic terminal contacts for the drain, top-gate, source and back-gate as shown in Fig. 4.1. Graphene is used as a semiconductor that creates a channel between the source and drain terminals. The channel is sandwiched by dielectrics between the top-gate and back-gate terminal. C_e and C_b are the resulting capacitance between the top-gate and the channel as well as the back-gate and the

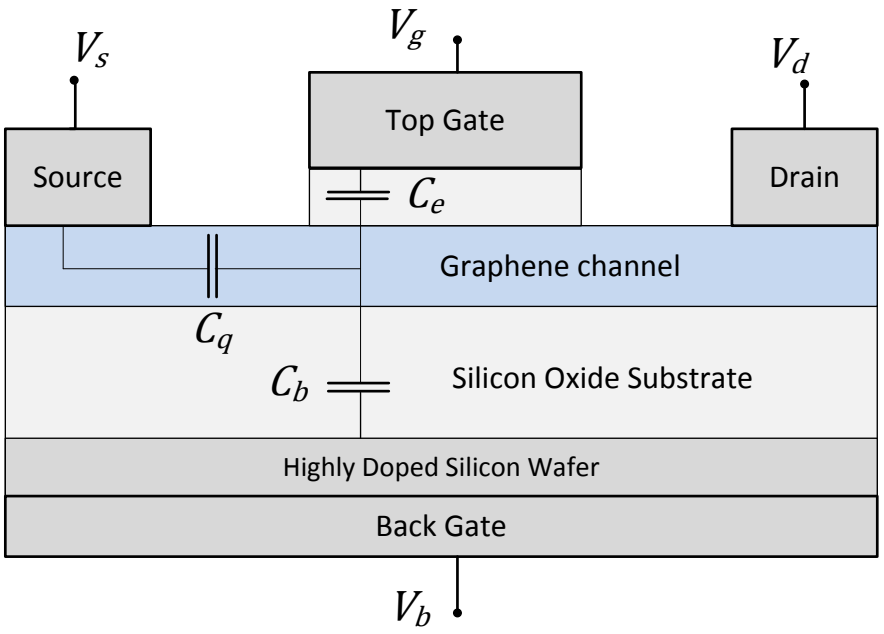


FIGURE 4.1: Structure of a dual-gate single-layer graphene transistor with geometric capacitances.

channel. Both C_e and C_b are fixed capacitances as a result of the dielectric geometry and have a theoretical value represented by Eqn. (4.1) and Eqn. (4.2) respectively.

$$C_e = \epsilon_0 \epsilon_1 / t_{ox} \tag{4.1}$$

$$C_b = \epsilon_0 \epsilon_2 / H_{sub} \tag{4.2}$$

In both equations, ϵ_0 is permittivity of free space, ϵ_1, is top-gate dielectric constant, ϵ_2, is back-gate dielectric constant, t_{ox} is top-gate dielectric thickness and H_{sub} is back-gate dielectric thickness. A number of top-gate dielectric materials have been used on the graphene channel such as hafnium oxide, HfO_2 with a theoretical dielectric constant value of 25 [160] and SiO_2 with a dielectric constant value of 3.9.

Fig. 4.2 shows the equivalent circuit model for the single-layer transistor. The vertical electric field induces mobile charges in the graphene channel. An energy is required to pump carriers from the source into the channel [45]. The quantum capacitance is a measure of this energy. It is a derivative of the net charge in the channel to the potential of the channel. Therefore, the quantum capacitance, C_q, is a variable capacitance which varies with the channel charge density.

In the equivalent circuit in Fig. 4.2, the quantum capacitance is apportioned to the source even though it is distributed along the channel.

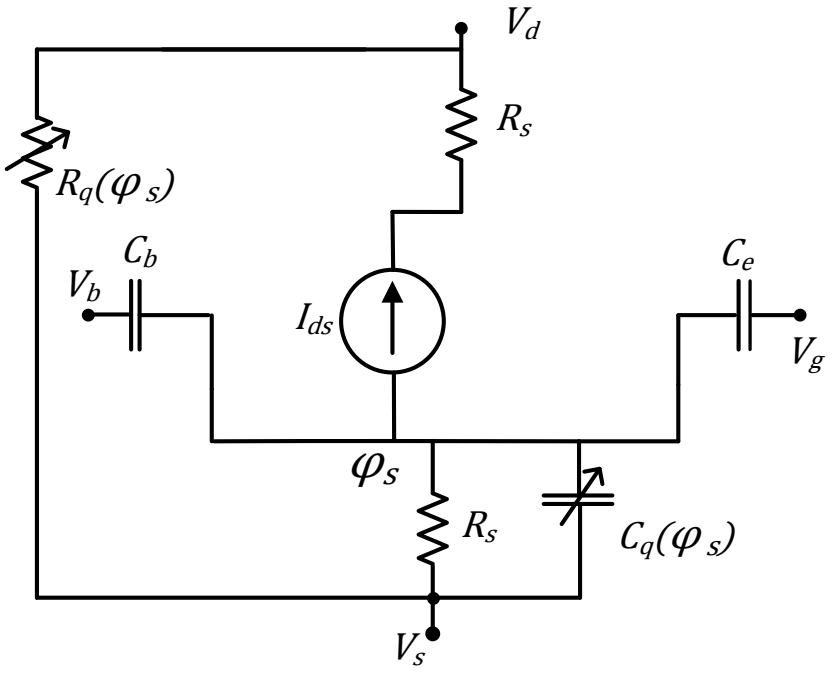


FIGURE 4.2: Equivalent circuit model for a single layer graphene transistor

Based on the expression derived from the two dimensional free electron gas model, the quantum capacitance is shown in Eqn. (4.3) [86]:

$$C_{qvar}(\varphi_s) = \frac{2q^2 k_B T}{\pi(\hbar v_f)^2} \ln\left[2\left(1+\cosh\frac{q\varphi_s}{k_B T}\right)\right] \tag{4.3}$$

where φ_s is the potential difference between the channel and the source terminal, V_s, v_f is the Fermi velocity, electronic charge is q and the reduced Plank's constant is $\hbar$, k_B is the Boltzmann's constant and T is the temperature in degrees Kelvins. Eqn. (4.3) can be reduced to Eqn. (4.4) [87, 88].

$$C_{qvar} = q^2 \frac{2}{\pi} \frac{q|\varphi_s|}{(\hbar v_f)^2} \tag{4.4}$$

From Eqn. (4.4), a zero quantum capacitance is expected at a zero surface potential. However, this is not the case. A non zero quantum capacitance at zero surface potential is observed as a result of induced charge impurities around the Dirac point [85].

Charged impurities around the Dirac point account for the minimum charge density of the channel, and in turn the off-current. Graphene semiconductors do not have a low off-current relative to its on-current as silicon does, even though the density of states vanishes at the Dirac point. Published works report a minimum carrier sheet density in the vicinity of $0.5 \times 10^{12} cm^{-2}$ at the Dirac point[33, 26].

Accounting for the presence of a minimum charge in the channel when the surface potential is zero, the quantum capacitance at zero surface potential is given by Eqn. (4.5):

$$C_{qmin} = \frac{q^2\sqrt{n_0}}{\sqrt{\pi}\hbar v_f} \tag{4.5}$$

where the minimum carrier density is n_0. From the Drude model, the charge density in the channel is $n = \sqrt{n_0^2 + n_*^2}$ where n_* is the charge density caused by the gate potential. Hence, the quantum capacitance of the layer is given by Eqn: 4.6.

$$C_q(\varphi_s) = \frac{C_{qmin}^2 + 2(C_{qvar}(\varphi_s)/2)^2}{\sqrt{C_{qmin}^2 + (C_{qvar}(\varphi_s)/2)^2}} \tag{4.6}$$

A simpler model can be equally assumed, of which both the minimum charge density and the induced charge density are superimposed such that $n = n_0 + n_*$.

$$C_q(\varphi_s) = C_{qmin} + C_{qvar}(\varphi_s) \tag{4.7}$$

The quantum capacitance of the later yields a model that is analytical, while that of the former results in a numerical model.

4.1.2 Surface Potential

An analytical model is usually preferred in cases where the model is to be used to simulate large digital circuits, to reduce the simulation time. However, in the case of analogue and RF applications which use a few transistors, a more accurate numerical model is preferred.

4.1.2.1 Analytical model

From Eqn. (4.4), the quantum capacitance is a function of the surface potential. By solving the equivalent circuit in Fig. 4.2 φ_s is given by Eqn 4.8:

$$\varphi_s = \frac{C_e(V_{gs} - V_{gs}^0) + C_b(V_{bs} - V_{bs}^0)}{C_e + C_b + C_{qmin} + \frac{1}{2}C_{qvar}(\varphi_s)} \tag{4.8}$$

where V_{gs}^0 is the top-gate to source Dirac voltage and V_{bs}^0 is the back-gate to source Dirac voltage. Both V_{gs}^0 and V_{bs}^0 are voltage offsets to V_{gs} and V_{bs}, similar to a flat band voltage in silicon transistor.

Both Eqns. (4.4) and (4.8) have to be solved self-consistently in computing φ_s. An analytical solution of φ_s is possible. The analytical solution of φ_s gives rise to two separate equations, one half solves for a positive value of φ_s and the other half solves for a negative value of φ_s.

When the surface potential is positive, φ_s is represented by Eqn. (4.9):

$$\varphi_s = -\frac{\delta C_{qvar}}{\delta \varphi_s}\left[C_b + C_e + C_{qmin} - \sqrt{2\frac{\delta C_{qvar}}{\delta \varphi_s} C_e (V_{gs} - V_o) + (C_b + C_e + C_{qmin})^2}\right] \tag{4.9}$$

and when the surface potential is negative, φ_s is represented by Eqn. (4.10):

$$\varphi_s = \frac{\delta C_{qvar}}{\delta \varphi_s}\left[C_b + C_e + C_{qmin} - \sqrt{-2\frac{\delta C_{qvar}}{\delta \varphi_s} C_e (V_{gs} - V_o) + (C_b + C_e + C_{qmin})^2}\right] \tag{4.10}$$

where V_o is the threshold voltage and $\frac{\delta C_{qvar}}{\delta \varphi_s} = q^2 \frac{2}{\pi} \frac{q}{(\hbar v_f)^2}$. Between Eqns. (4.9) and (4.10) the two conditions have to be satisfied by the surface potential. One, the surface potential must be a real value and two, the result must have the assumed sign used in calculating (Eqns. (4.9) and (4.10) must produce a positive or negative φ_s respectively).

An algorithm for solving the self-consistency is shown in Algorithm 1.

Data: The geometric capacitances C_q, C_b, C_{qmin}, the inbuilt voltages, V_{bs}^0, V_{gs}^0, the gate voltages, V_{gs}, V_{bs} and q, $\hbar$, v_f
Result: The surface potential φ_s
φ_{s+} = Eqn. (4.9)
φ_{s-} = Eqn. (4.10)
if $\varphi_{s+} > 0$ *and* φ_{s+} *is real* **then**
  $\varphi_s = \varphi_{s+}$;
else
  $\varphi_s = \varphi_{s-}$
end

Algorithm 1: Solving self consistency in single-layer GFET

4.1.2.2 Numerical model

In this model, the Drude model is taken into consideration in calculating the charge density of in the channel. Therefore, the surface potential of the layer is expressed by Eqn. (4.11).

$$0 = -C_e(V_{gs} - V_{gs}^0 - \varphi_{s1}) - C_b(V_{bs} - V_{bs}^0 - \varphi_{s1}) + \varphi_{s1}\sqrt{(C_{qvar}(\varphi_{s1})/2)^2 + C_{qmin}^2} \quad (4.11)$$

To calculate the correct surface potential, φ_s has to be self consistent with both Eqns. (4.4) and (4.11)

4.1.2.3 Comparison of both models

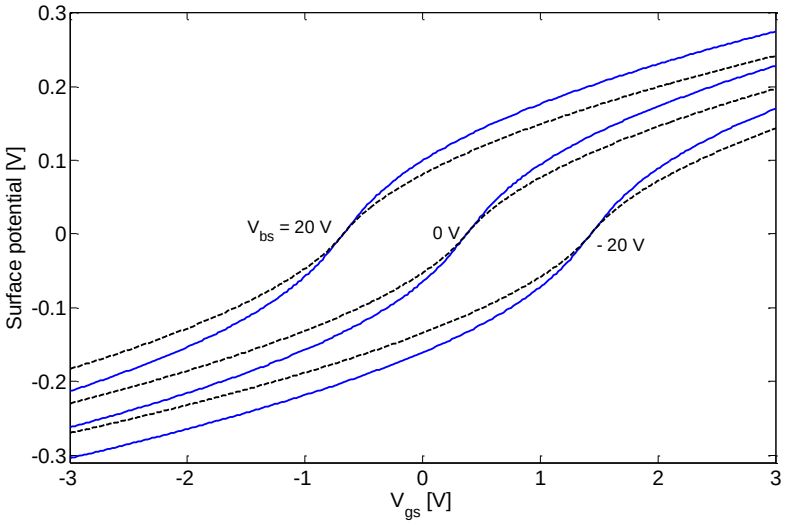
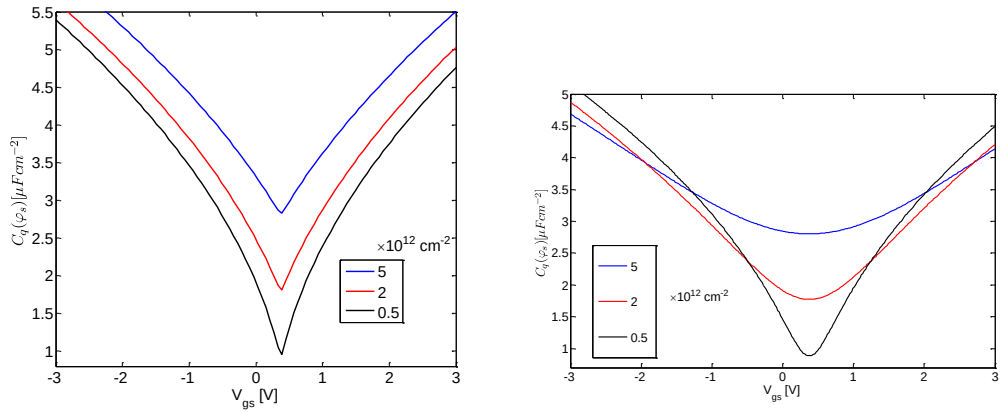


FIGURE 4.3: The surface potential, φ_s, as a function of V_{gs} for V_{bs} of $20V$, $0V$ and $-20V$ for both the analytical (dash) and numerical model (solid)

Fig. 4.3 (see parameter values in Table 4.2) shows the behavior of φ_s as a function of V_{gs} for $V_{bs} = 20V$, $0V$ and $-20V$ respectively for both the analytical (dash lines) and numerical model (solid lines). Positive values of φ_s indicates the Fermi level is in the conduction band, in the valence band for negative values and charge neutrality point at a zero value [14].

Both models converge at threshold voltage, where the surface potential is zero and diverge a further away from the threshold voltage. From Fig. 4.4, both models will have an equal quantum capacitance at the threshold voltage.

Fig. 4.4 (see parameter values in Table 4.2) shows the behaviour of the quantum capacitance as a function of the top-gate voltage for both models. In the case of the



(a) The quantum capacitance against variation in V_{gs} for an analytical model

(b) The quantum capacitance against variation in V_{gs} for a numerically intensive model

FIGURE 4.4: The quantum capacitance against variation in V_{gs} for a minimum charge density of 0.5, 2 and 5 $\times 10^{12} cm^{-2}$ respectively

analytical model in Fig. 4.4(a) the quantum capacitance characteristic translates vertically with variations in the minimum charge density, such that the lines are parallel to each other. On the other hand, the numerical model in Fig. 4.4(b) translates as the analytical model but the lines are not parallel to each other. The more pronounced parabolic characteristics with increased impurity density is consistent with reports on the quantum capacitance [88]. Thus, the numerical model tends to the analytical model at lower minimum charge densities.

4.1.3 Threshold Voltage

The threshold, V_o, for a given V_{bs} represents the value of V_{gs} at which the channel will experience charge neutrality. V_o has been reported to have a linear relationship with V_{bs} [33], of which the slope is the ratio of the back-gate and top-gate capacitances. At the charge neutrality point (CNP), the surface potential is zero. Thus, solving for $\varphi_s = 0$ in Eqns. (4.8) and (4.11) $V_{gs} = V_o$.

$$V_o = V_{gs}^0 + (C_b/C_e)(V_{bs}^0 - V_{bs}) \tag{4.12}$$

4.1.4 Effective Gate Capacitance

In matching the equivalent circuit in Fig. 4.2 with the general GFET circuit model in Fig. 3.2, the gate capacitance of both gates is modelled in series with the quantum capacitance.

$$C_{top} = \frac{C_e C_q(\varphi_s)}{C_e + C_b + C_q(\varphi_s)} \tag{4.13}$$

$$C_{back} = \frac{C_b C_q(\varphi_s)}{C_b + C_e + C_q(\varphi_s)} \tag{4.14}$$

4.2 Off-current Hole/Electron Activation Energy

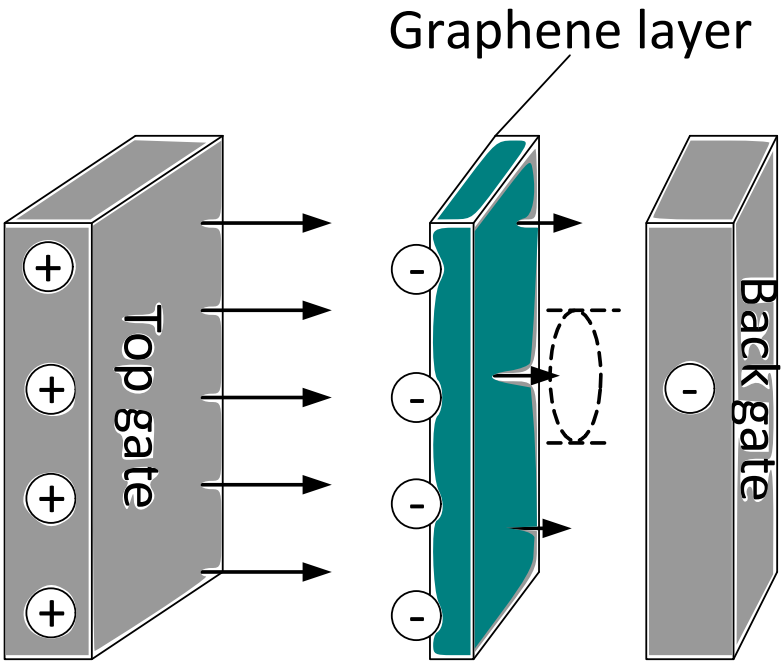


FIGURE 4.5: Schematic of a single-layer graphene with metallic gate terminal showing the electric field. The dash lines show the Gaussian surface which is induced by the electric field between the layers

Insulators and semiconductors exhibit a resistive dependence on the operating temperature. In the graphene semiconductor, thermal excitations of the carriers from the valence band to the conduction band creates mobile carriers in both bands. These mobile carriers limit the maximum resistance at the charge neutrality point where the transistor is in an intrinsic state.

The maximum channel resistance is determined by charged impurities between the graphene layer and the substrate. Therefore, the potential energy between the graphene channel and the back-gate is responsible for modulating the charged impurities.

4.2.1 Electric Field Dependent Energy

In the presence of an electric field due perpendicular to the channel, the single-layer graphene FET shows a shift in its threshold voltage as shown in Eqn. (4.12). A bandgap is not created by the presence of an electric field. The electric field will create an induced charge on the channel quantum capacitance.

$$Q_s = \frac{\varphi_{s1}}{2} C_{qvar}(\varphi_{s1}) \tag{4.15}$$

Thus, the corresponding potential energy is shown below.

$$U_{s1} = \frac{\varphi_{s1}^2}{6} C_{qvar}(\varphi_{s1})) \tag{4.16}$$

An index number 1 is used for consistency even though the channel in Fig. 4.5 has only one layer. At the condition of charge neutrality, $\varphi_s = 0$, the potential energy in Eqn. (4.16) diminishes. Thus, there can be no bandgap creation with respect to the presence of an electric field. However, outside the charge neutrality condition there is a potential energy in the layer.

A Gaussian cylinder is inserted between the channel and the back-gate as shown in Fig. 4.5. Assuming a uniform electric field through the cylinder. A parallel plate capacitor of capacitance C_b between the graphene layer and the back-gate can be considered. The resulting potential energy between the graphene layer and the back-gate is $1/2C_bV_E^2$. Where V_E is the potential difference as a result of a uniformly distributed charge.

$$V_E = \sqrt{\frac{2U_{s1}}{C_b}} \tag{4.17}$$

For a given temperature, V_E being a reflection of the energy band should satisfy the relationship $R_q \propto \exp(V_E/V_T)$ where in silicon FET $V_T = k_BT/q$.

$$R_q = R_s^0 \exp(V_E/V_T) \tag{4.18}$$

From Eqn. (4.18), R_s^0 is the resistance at intrinsic state, that is at charge neutrality condition, and V_T is a constant voltage.

Based on the Drude model used in characterising graphene devices R_s^0 is given by Eqn. (4.19):

$$R_s^0 = \frac{L}{Wqn_o\mu} \tag{4.19}$$

where L is the channel length, W is the channel width, q is the electronic charge, n_o is the minimum charge density and μ is the carrier mobility.

4.2.2 Temperature Dependence of the off-current

Assuming that there are no defects in the insulators, for a sharply defined bandgap which is sufficiently large enough, electrons in the valence band are thermally excited to the conduction band using the relation $\exp(q\phi_{barrier}/k_BT)$. A large single-layer graphene channel displays a weak dependence of the output conductance against variations in the temperature [89]. A weak dependence of the channel resistance against changes in temperature suggests that the bandgap opened is too small.

The relationship $I_{off} \propto \exp((T_o/T)^n)$ [89] fits the graphene FET in which $n = 1/3$. The exponent parameter $n = 1/3$ suggests the presence of localized impurities in the bandgap.

Aside from graphene, in other semiconducting materials the temperature dependence has equally been modeled using the exponent $n = 1/3$ in the Steinhart and Hart equation [90] and using the exponent $n = 1/4$ in the Hoge-3 equation [91].

However, in this model a reference temperature is introduced, T_{ref} such that $I_{off} \propto \exp((T_o(1/T - 1/T_{ref}))^n)$ where $n = 1/3$.

A factor R_T in Eqn. (4.20) is thereby multiplied to Eqn. (4.18) to capture the channel resistance dependence on temperature.

$$R_T = \exp\left(\left(\frac{T_o(T_{ref} - T)}{TT_{ref}}\right)^{1/3}\right) \tag{4.20}$$

Eqn. (4.20) holds as long as the condition $T \leq T_{ref}$ is satisfied. For validations against experimental measurements, T_{ref} set to room temperature gives a good agreement. Also, the intrinsic resistance, R_s^0 is the resistance at room temperature. For the single-layer graphene FET ,T_o is a constant temperature.

Thus, the resulting off-current due to R_q is shown in Eqn. (4.21).

$$I_{off} = V_{ds}/R_q, \tag{4.21}$$

$$R_q = R_s^0 \exp\left(\left(\frac{T_o(T_{ref} - T)}{TT_{ref}}\right)^{1/3}\right) \exp(V_E/V_T) \tag{4.22}$$

R_q is integrated into the calculation of the drain current in chapter 3, in taking into consideration the assumptions on the charge density in the channel. In the case of the analytical model, the drain current is shown below:

$$I_{ds} = I_{off} + I_{ds*} \tag{4.23}$$

where I_{ds*} is the drift current as calculated in chapter 3 (see Eqn. (3.17)). For the numerical model, the Drude model is used to calculate charge density, thus, the drain current is shown below.

$$I_{ds} = \sqrt{I_{off}^2 + I_{ds*}^2} \tag{4.24}$$

4.3 Single-gate Single-Layer

A three port graphene FET which uses only a single-gate, is much easier to fabricate than the dual gate and interest in its behaviour is attracting attention [75]. Chemical doping can be used to control the channel making it possible to obtain high ON-OFF ratio with just a single-gate graphene transistor. Models have been centred on the dual-gated structure of the graphene field effect transistor, and none so far on the single-gate structure.

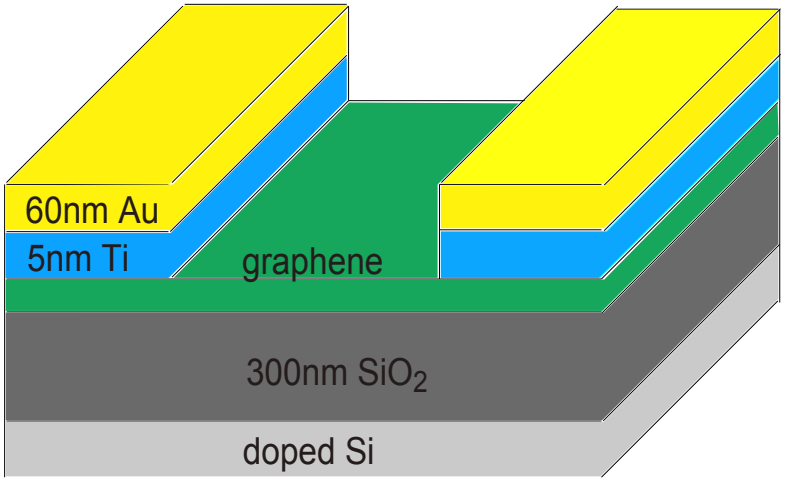


FIGURE 4.6: Schematic diagram of a single-layer graphene FET

4.3.1 Graphene Device Fabrication

The single-gated, single-layer graphene transistor shown in Fig. 4.6 is fabricated by micromechanical cleaving of natural graphite [14]. The graphene used in the transistor is identified to be single-layer graphene. Electrical contacts to the flake source and drain was made by deposition of a Ti/Au bilayer (5/60 nm thick) giving the graphene channel the following dimensions; $W = 1\mu m$, $L = 6\mu m$. The flakes are deposited onto SiO_2 (300 nm thick) sitting on a highly doped silicon. The doped silicon substrate is used as the device gate [76].

4.3.2 Capacitance Model

The circuit level schematic of the single-layer graphene transistor is shown in Fig. 4.7. Fig. 4.7 is a modification of the earlier equivalent circuit in Fig. 4.2. C_e is the gate capacitance, $C_{q(\varphi_s)}$ is the quantum capacitance, R_s is the series resistance and R_q is the off-current resistance.

Here, the quantum capacitance is a function of the surface potential, and Eqns. (4.4) and (4.5) apply. For an accurate modeling of the gate capacitance, a quantum capacitance is modeled in series with the gate capacitance.

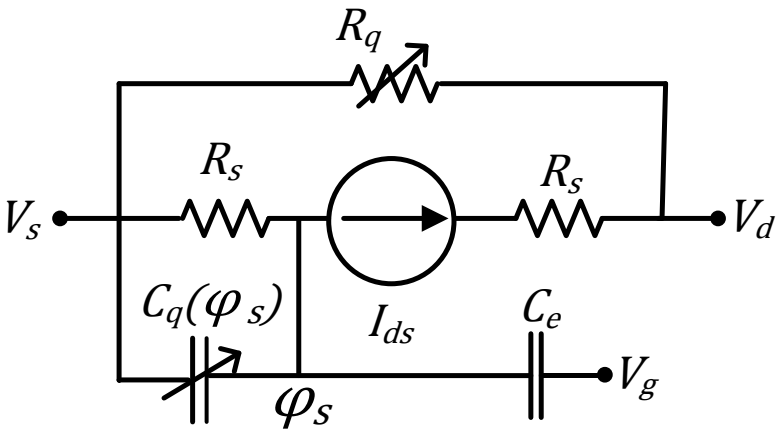


FIGURE 4.7: Equivalent circuit-level diagram for a single-gate graphene field effect transistor

4.3.2.1 Using a simplified analytical method

Solving the equivalent circuit, the surface potential is given by Eqn. (4.25):

$$\varphi_s = \frac{C_e(V_{gs} - V_o)}{C_e + C_{qmin} + \frac{1}{2}C_{qvar}(\varphi_s)} \tag{4.25}$$

where V_o is the gate to source Dirac voltage. With a single-gate, the gate both electrostatically dopes the channel and modulates the doping intensity. Eqn. (4.25) has to be solved self-consistently with the quantum capacitance in computing φ_s. Two analytical solutions of φ_s are obtained depending whether φ_s is positive or negative.

When the surface potential is positive φ_s is expressed by:

$$\varphi_s = -\frac{\pi}{2}\frac{(\hbar v_f)^2}{q^3}[C_e + C_{qmin} - \sqrt{q^2\frac{4}{\pi}\frac{q}{(\hbar v_f)^2}C_e(V_{gs} - V_o) + (C_e + C_{qmin})^2}] \tag{4.26}$$

and when the surface potential is negative φ_s is represented by Eqn. (4.27)

$$\varphi_s = \frac{\pi}{2}\frac{(\hbar v_f)^2}{q^3}[C_e + C_{qmin} - \sqrt{-q^2\frac{4}{\pi}\frac{q}{(\hbar v_f)^2}C_e(V_{gs} - V_o) + (C_e + C_{qmin})^2}] \tag{4.27}$$

Equally, the self consistency here can be solved as shown in Algorithm 1 where Eqns. (4.9) and (4.10) are replaced by Eqns. (4.26) and (4.27) respectively. From Eqn. (4.26) and (4.27) the gate offset voltage is the threshold voltage of the device in contrast to the dual-gate where back-gate optimizes the threshold value (see Eqn. (4.12)). With a single-gate, there is only one possible threshold voltage, which is the gate offset, V_o. Only through chemical doping can the threshold voltage be shifted.

4.3.2.2 Using the Drude model

Using the Drude model to approximate the charge in the channel of the equivalent circuit, the respective potential gives rise to Eqn. (4.28).

$$0 = -C_e(V_{gs} - V_o - \varphi_{s1}) + \varphi_{s1}\sqrt{(C_{qvar}(\varphi_{s1})/2)^2 + C_{qmin}^2} \tag{4.28}$$

Eqn. (4.28) has to be solved for φ_{s1}.

4.3.2.3 Comparison between both methods

For an SiO_2 on Si wafer with an oxide thickness of 300nm (see parameters in Table 4.1) the models are compared for a sweep of the gate overdrive, that is $V_{gs} - V_o$, from -50V to 50V. Fig. 4.8 shows the surface potential of both models for $n_0 = 0.5 \times 10^{16} m^{-2}$.

In Fig. 4.8, for a negative surface potential, the Fermi level is in the valence band and the conduction is by holes, while for a positive surface potential, the Fermi level is in the conduction band and the conduction is by electrons. A charge neutrality point is at a surface potential of zero.

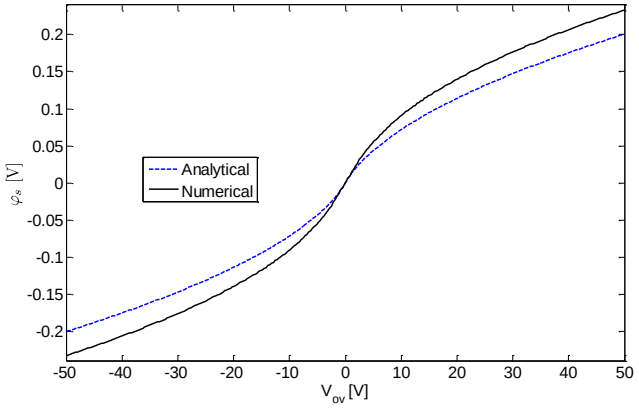
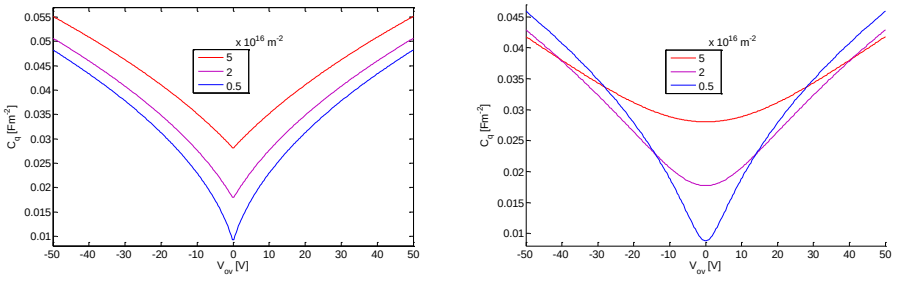


FIGURE 4.8: Surface potential for both an analytical model and the Drude based numerical model.

The deviations between the surface potential of both models becomes pronounced at high overdrive voltages. Compared to the case of a dual-gate, where an overdrive of about 3V produced large deviations in the surface potential between both models, here, about twenty times the overdrive is needed to produce similar deviations in the surface potentials.



(a) Quantum capacitance using the simplified analytical model

(b) Quantum capacitance using the Drude based numerical model

FIGURE 4.9: Quantum capacitance for a single-gate single-layer transistor

Also, the behaviour of the quantum capacitance is compared using three sets of minimum sheet charge densities. Fig. 4.9(a) shows the characteristics of the quantum capacitance using the analytical model, while Fig. 4.9(b) shows the same characteristics using the Drude based model. It can be observed that the analytical model shows sharp V-shaped quantum capacitance at the Dirac point irrespective of the minimum charge density, while the numerical model shows a parabolic characteristics.

Fig. 4.10 illustrates that despite the prominent differences in the quantum capacitances between both plots in Fig. 4.9, the effective capacitance which is responsible for modulating the doped carriers in the channel closely approximate to each other. This is as a result of the gate capacitance, C_e, being so small compared to the quantum capacitance. Therefore, the quantum capacitance has negligible effect on the overall capacitance.

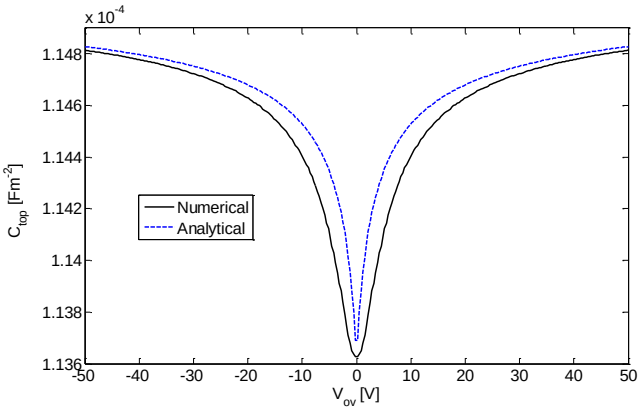


FIGURE 4.10: Effective gate capacitance against variations in the gate voltage

4.3.3 Singe-gate Activation Energy of the off-current

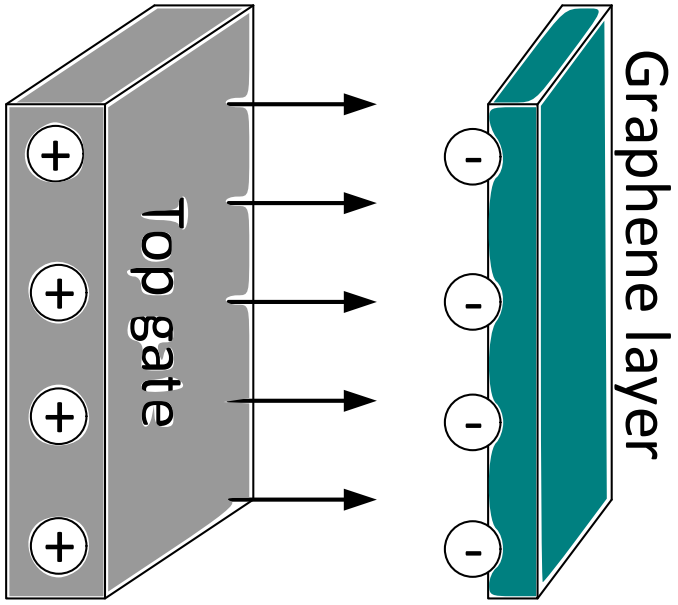


FIGURE 4.11: Schematic of a single-layer graphene with a single metallic gate terminal showing the electric field and the excess charge.

Taking a close look at the perpendicular electric field and the resulting channel conductance, Fig. 4.11 is a parallel plate capacitor between the graphene channel and the gate. Assuming the gate is positively charged as shown in the figure, the electric field emanating from the gate will charge one side of the graphene semiconductor with a negative charge. Thus, irrespective of the potential at the gate, R_q has a constant resistance given by R_s^0 in Eqn. (4.29).

Since the channel has a non zero charge density at the charge neutrality point, n_o, with a carrier mobility, μ, the channel has a limiting channel resistance R_s^0.

$$R_s^0 = \frac{L}{W q n_o \mu} \tag{4.29}$$

This resistance is represented by R_q in the equivalent circuit diagram (see Fig. 4.7). R_q is a constant irrespective of the number of layer of the graphene channel. A published experimental result for a bilayer graphene transistor using a single-gate shows a transfer characteristic similar to a single-layer [75]. That is, the transistor has a zero bandgap opening. Comparing the single-gate transistor with the dual-gate one, from Eqn. (4.18) it is observed that the exponential increase in R_q is due to the presence of two gates.

At the charge neutrality point, the total resistance of the channel is given by R_q. As the gate voltage moves away from the charge neutrality point and the channel begins to be doped. Doping the channel makes the total channel resistance less than R_q.

Well away from the charge neutrality point, the carriers reduce the channel resistance much less than R_q, thereby closely approximating the channel carrier transport. There are published models that use only the electrostatic doping of the charge to estimate the carrier transport behaviour, and give a good agreement with experimental data away from the charge neutrality point [34, 38].

Here, the carrier transport is obtained by matching this model with the general model shown in Fig. 3.4.

4.4 Experimental Validation

Both models described in this chapter are validated against experimental measurements. Experimental measurements published elsewhere [89] are used in validating the dual-gate graphene model, while the experimental measurements used in validating the single-gate graphene model are presented in this work.

4.4.1 Single-gate Case

Table 4.1 shows the model parameters. Here, only the analytical model is used because the gate capacitance is very small compared to the quantum capacitance.

Fig. 4.12 shows the channel resistance plotted against the gate voltage at room temperature for both the experimental data and the model. The model uses a constant $V_{ds} = 0.01V$ with series resistances of 10Ω. The transistor has a maximum resistance of $18k\Omega$ at the Dirac point voltage of $V_{gs} = 80V$, and a minimum resistance of approximately $4k\Omega$ at $V_{gs} = -20V$. Thus, having an ON/OFF current ratio of about 4.5.

TABLE 4.1: Model parameters for single-gate monolayer graphene FET

Model parameter	Parameter value
$L(\mu m)$	6
$W(\mu m)$	1
$t_{ox}(nm)$	300
ϵ_1	3.9
$V_{gs}^0(V)$	80
$R_q(k\Omega)$	18
$n_0(m^{-2})$	0.5×10^{16}
$\mu_h[cm^2/V.s]$	1000
$\mu_e[cm^2/V.s]$	800

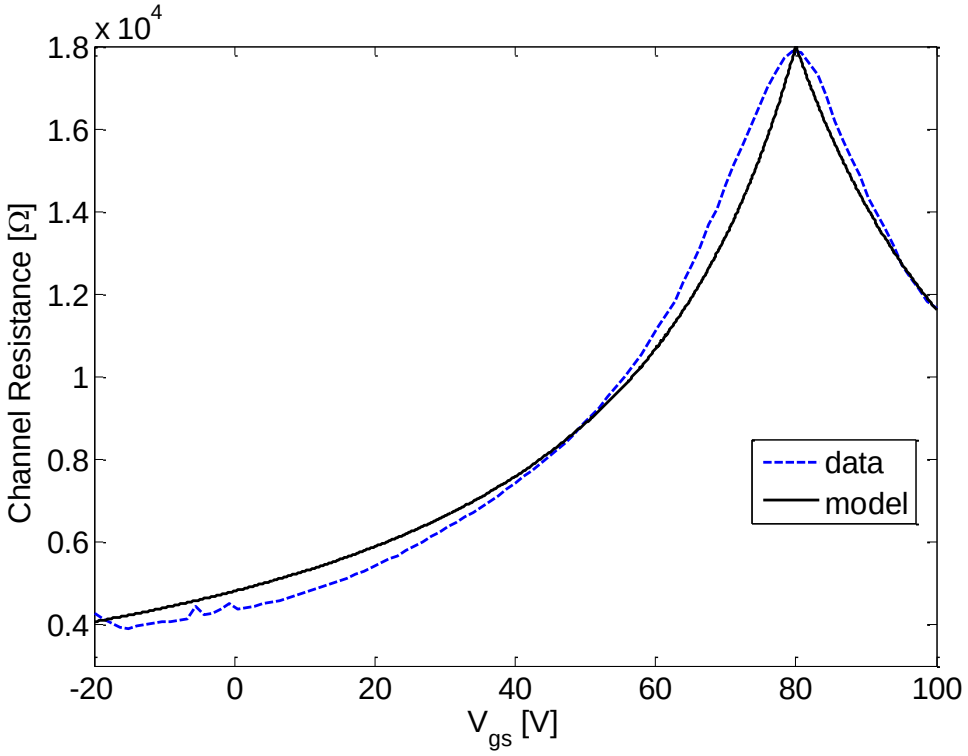


FIGURE 4.12: Transfer characteristics of a single-gate monolayer transistor at room temperature [76].

To fit with experimental data, the model uses a mobility of $\mu_h = 1000cm^2/V.s$ for hole conduction and $\mu_e = 800cm^2/V.s$ for electron conduction. Both carrier fitting values, compared to silicon based channels where the hole mobility is lower than that of the electron, show an approximately equal hole and electron mobility. This is as a result of the symmetry between the valence and conduction bands [53].

4.4.2 Dual-gate FET

Model parameters of the transistor are shown in Table 4.2. For this test case the graphene channel is sandwiched between two SiO_2 dielectrics.

TABLE 4.2: Model parameters for monolayer graphene FET

Model parameter	Parameter value
$L(\mu m)$	1
$W(\mu m)$	1.1
$t_{ox}(nm)$	15
ϵ_1	3.9
ϵ_2	3.9
$V_{gs}^0(V)$	2.22
$V_{bs}^0(V)$	-35
$H_{sub}(nm)$	285
$V_T(V)$	2
$R_s^0(k\Omega)$	4.65
$n_0(m^{-2})$	0.5×10^{16}

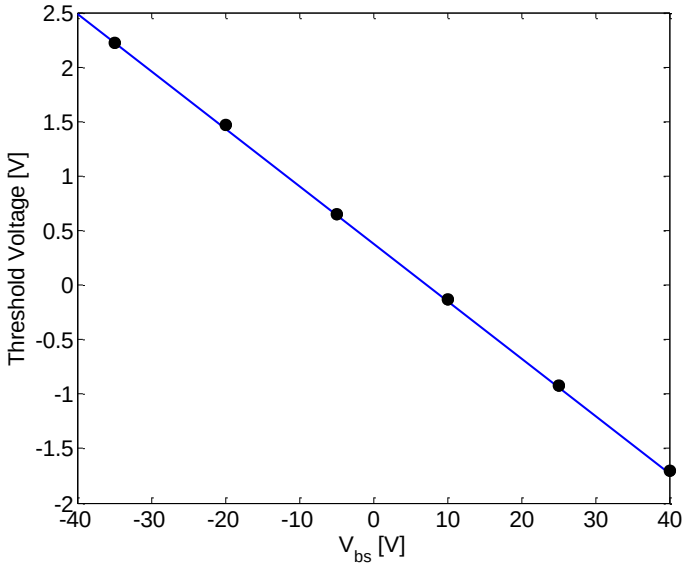


FIGURE 4.13: Experimental data (circles) [89] and the proposed model (solid line) of the threshold voltages of a single-layer graphene FET

The equation of the threshold voltage in Eqn. (4.12) shows that a positive back-gate voltage will shift V_o toward a negative value, and a negative back-gate voltage will result in a more positive V_o. The shift leads to a linear relationship between V_o and V_{bs} as shown In Fig. 4.13.

In the case of a single-layer graphene FET the potential energy, U_{s1}, of the layer tends to zero as the device approaches charge neutrality (see Eqn. (4.16)). A zero potential energy indicates that the device is in the intrinsic state with a zero band-gap opening. For any back-gate voltage the device is always at intrinsic state at the charge neutrality point. Therefore, any known back-gate voltage with its corresponding threshold voltage can be used as the reference voltages in calculating other back-gate voltages and threshold voltages. Here, the reference voltages used are a device threshold voltage of 2.22V and $V_{bs} = -35V$ [89].

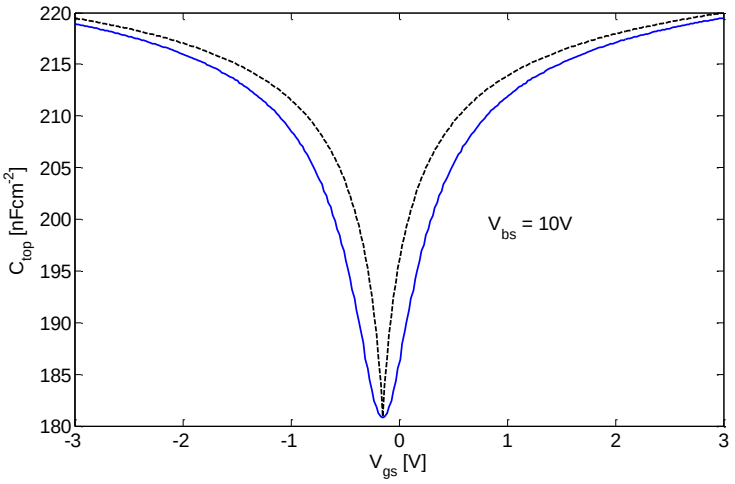


FIGURE 4.14: The effective top-gate capacitance, C_{top} against a sweep of V_{gs} for both the analytical (dash) and Drude numerical (solid) models from -3V to 3V for $V_{bs} = 10V$.

The top-gate to source capacitance varies with the quantum capacitance as can be seen in Fig. 4.14. From Fig. 4.14, the capacitance is bound by $C_e \geq C_{top} \geq C_e C_{qmin}/(C_e + C_{qmin} + C_b)$ for $C_e = 230nF/cm^{-2}$ and $C_{qmin} = 887nF/cm^{-2}$. It is observed that the device has a minimum capacitance at the charge neutrality point.

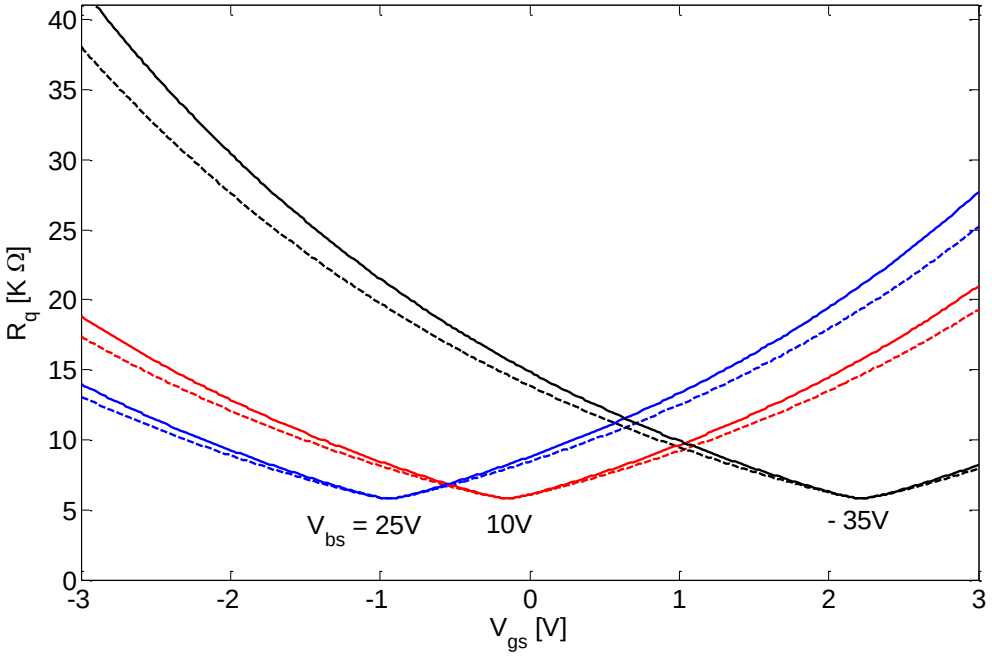


FIGURE 4.15: Characteristics of R_q against V_{gs} for V_{bs} of $25V$, $10V$, $0V$ and $-35V$ respectively. Plots of the characteristics for an analytical (dash) and a Drude numerical (solid) model.

Alongside C_{top}, R_q varies with the gate voltage, showing an exponential relationship

against the surface potential, indicated in Eqn. (4.18). R_q limits the channel conductance about the charge neutrality point as the density of states vanishes. Here, the resistance due to the induced charge density is far greater than R_q. Fig. 4.15 shows the transfer characteristics of the current due to R_q at a constant operating temperature of 52K.

It can be observed that R_q has a minimum value at the charge neutrality point equal to R_s^0. Away from the charge neutrality point the parallel conductance due to the induced charge quickly becomes comparable to R_q, or even much less than R_q. Therefore, to achieve very high ON/OFF current ratios, techniques of increasing R_s^0 is a prerequisite.

From Fig. 4.15, R_s^0 is $4.65k\Omega$, which is low for digital circuit applications; leading to a high off current. It is assumed that a complementary transistor configuration is used to develop digital logic.

Irrespective of the back-gate voltage, R_q always has a minimum value given by R_s^0 at the charge neutrality point. This implies that for a single-layer GFET, no tunable transport bandgap is formed.

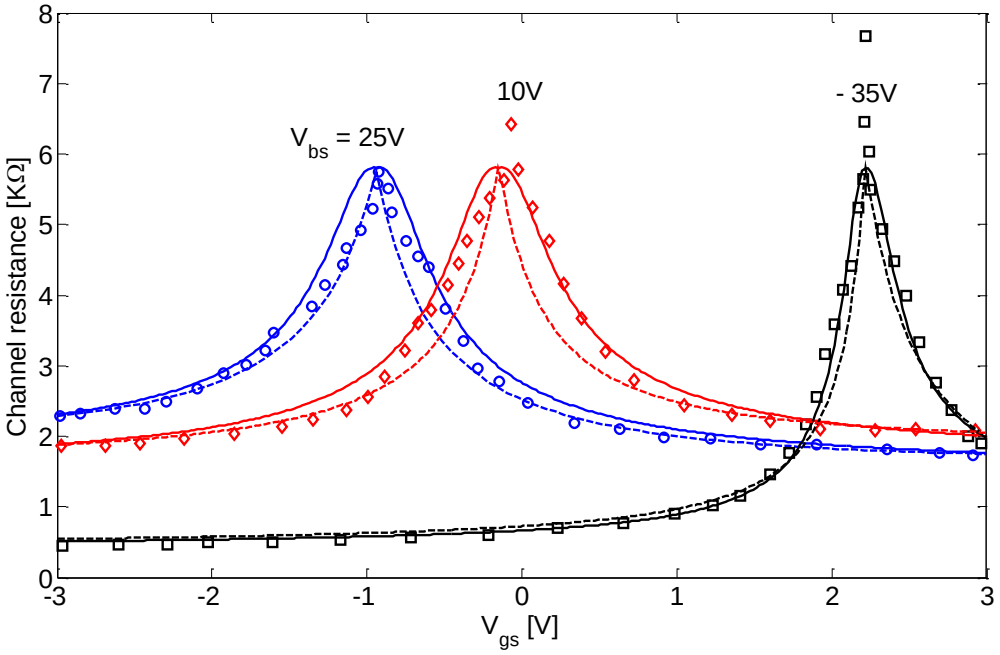


FIGURE 4.16: Experimental data (○ ◊ □) [89], the analytical model (dash) and the Drude numerical model (solid) for the channel resistance against V_{gs} at a temperature of 4.7K, V_{bs} of 25V, 10V and -35V respectively and $V_{ds} = 0.01V$

Fig. 4.16 shows the variation of the channel resistance with changes in the top-gate for $V_{ds} = 0.01V$ and an operational temperature of 4.7K. The model gives the best fit against experimental data [89] with fitting parameters shown in Table 4.3 and Table 4.4 for the analytical and Drude model respectively.

TABLE 4.3: Experimental data fitting parameters using analytical model

	hole		electron	
$V_{bs}[V]$	$R_s[\Omega]$	$\mu_h[cm^2/V.s]$	$R_s[\Omega]$	$\mu_e[cm^2/V.s]$
25	720	1600	720	2200
10	720	2200	850	2200
-35	200	5200	200	2500

TABLE 4.4: Experimental data fitting parameters using Drude model

	hole		electron	
$V_{bs}[V]$	$R_s[\Omega]$	$\mu_h[cm^2/V.s]$	$R_s[\Omega]$	$\mu_e[cm^2/V.s]$
25	850	3200	720	3200
10	720	3200	850	3200
-35	200	7200	500	5500

For both models, Table 4.3 and Table 4.4 shows a mobility and a series resistance that is dependent on V_{bs}, this is due to V_{bs} modulating the un-gated regions of the transistor. The Drude model estimates a higher mobility and gives a better fit to the experimental data than the analytical model.

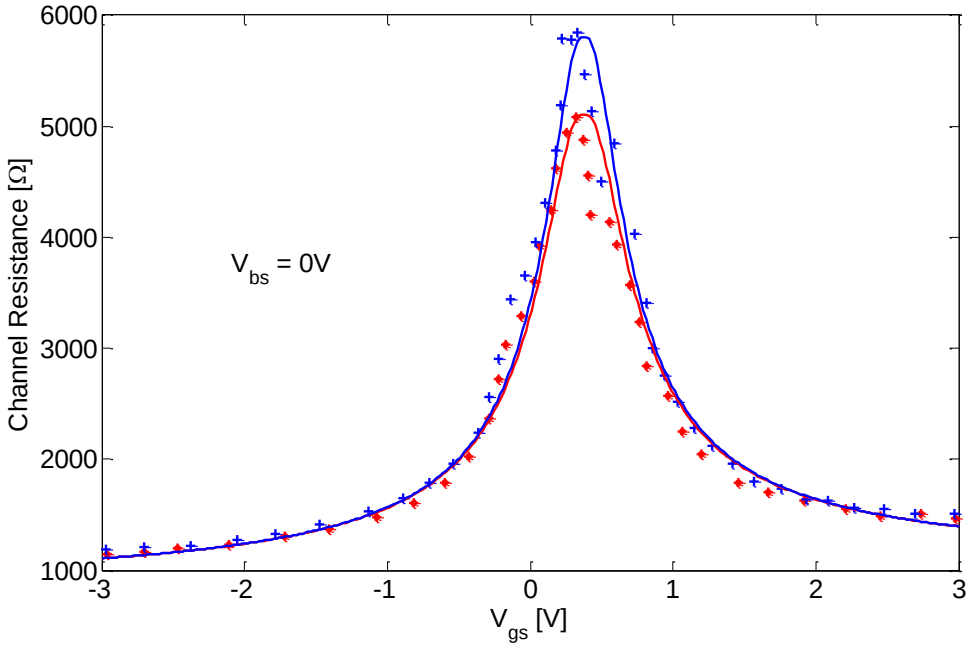


FIGURE 4.17: Experimental data (cross and star) [89] and the Drude based model (solid and dash lines) of the channel resistance against V_{gs} for temperatures of 4.7K and 52K respectively, at V_{bs} of 0V

In Fig. 4.17, the model is applied to data for temperatures 4.7K and 52K respectively. Table 4.5 which shows the fitting parameters for the experimental data at temperatures 4.7K, 14.4K and 52K respectively; shows no carrier mobility and series resistance dependence on the temperature.

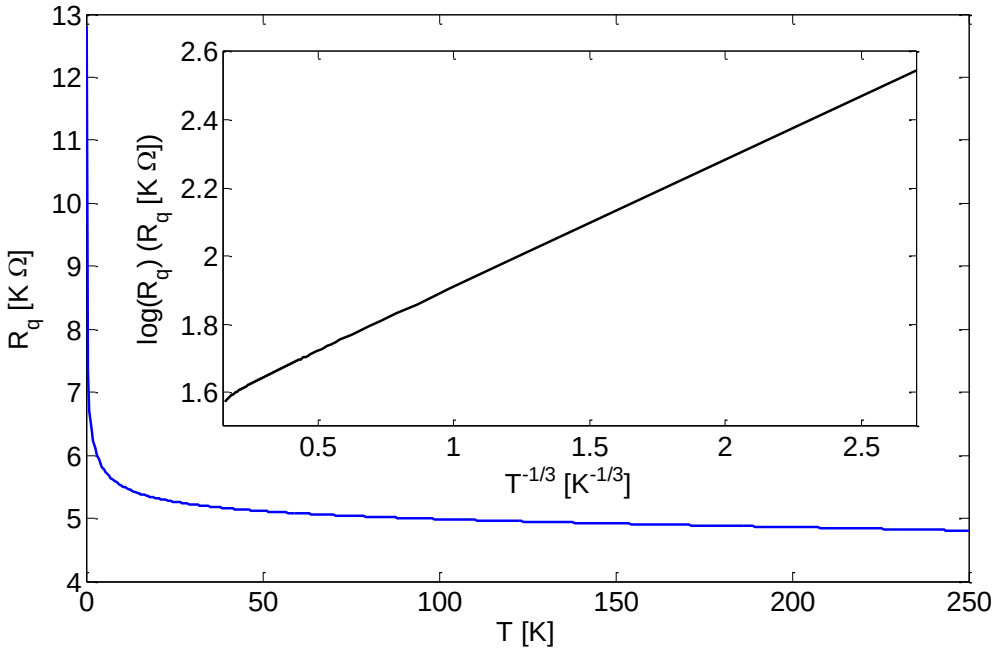


FIGURE 4.18: Interpolation of the dependence of the maximum channel resistance with respect to changes in temperature for a temperature sweep from $0.05K$ to $250K$

TABLE 4.5: Experimental data fitting parameters using the Drude based model

	hole		electron	
$Temp.[K]$	$R_s[\Omega]$	$\mu_h[cm^2/V.s]$	$R_s[\Omega]$	$\mu_e[cm^2/V.s]$
4.7	400	4000	500	4000
14.4	400	4000	500	4000
52	400	4000	500	4000

However, the thermionic resistance shows a slight dependence on temperature with values ranging between $5.1k\Omega$ and $5.8k\Omega$ for temperatures of 52K to 4.7K respectively. For an operating temperature of $14.4K$, the model estimates $R_q = 5.4k\Omega$ as the maximum channel resistance which agrees with experimental data [89]. R_q shows a dependence on temperature given by Eqn. (4.20), where the fitting temperature parameter $T_o = 0.052K$.

By plotting the maximum channel resistance against a sweep of the operating temperature from 0.05K to 250K as shown in Fig. 4.18, the device shows a very small change in resistance to large changes in temperature, for temperatures above 50K. The temperature dependent resistance shows a current ratio of 1 between room temperature and 0.05K (from inset diagram in Fig. 4.18 the current ratio is calculated as $Log(R_{q(T=0.05)}) - Log(R_{q(T=300)})$).

In comparing both transistor layouts, the single-gate transistors shows more promise to attaining very high ON/OFF current ratio. With reference to Fig. 4.12 and Fig.

4.15, at room temperature, a single-gate has an off state resistance of $18k\Omega$ compared to $4.65k\Omega$ of the dual-gate. Also, a single-gate has a series resistance as low as 10Ω compared to a dual-gate with series resistance in hundreds of ohms. This improvement in series resistance is attributed to the absence of un-gated regions in the single-gate transistor. Also, the electron and hole carrier mobility are approximately equal in the single-gate transistor.

An investigation is carried out into validating the single-layer model for a multilayer channel with two or more layers. This will give an insight into whether the single-layer model can be used as a general graphene FET model.

4.4.3 Single-layer Model Applied To Bilayer Graphene

Here, the single-layer model is validated against a bilayer transistor. The transistor is in intrinsic state with $V_{bs} = 2.7V$. At this voltage the transistor behaves like a single-layer. Experimental analysis are however published for $V_{bs} = 40V$ and $-40V$ [33] which suggests band-gap opening. To validate the model against the published experiment measurements, two test cases are used. One test case uses a V_{bs} of -40V and the other test case uses a V_{bs} of +40V. Table 4.6 shows the model parameters that fit the experimental data in both test cases.

TABLE 4.6: Model parameters for bilayer graphene FET

Model name	Model parameter
$L(\mu m)$	1
$W(\mu m)$	2.1
$t_{ox}(nm)$	15
$H_{sub}(nm)$	285
ϵ_1	8.8
ϵ_2	3.9
$V_{gs}^0(V)$	1.45
$V_{bs}^0(V)$	2.7
$R_s^0(K\Omega)$	12.88
V_T (V)	2

From Table 4.6, the top-gate dielectric, HfO_2, is estimated to have a dielectric constant of 8.8. However, the theoretical dielectric constant for HfO_2 is 25 [160], which indicates that the top-gate oxide has been unintentionally doped or the top-gate has more than one layer of oxide. Also, from the published experimental data, the top-gate oxide is estimated to have a dielectric constant of 16 [33]. The discrepancy between both reports is as a result of the equation used to estimate the dielectric constant. Here, the slope of the threshold voltage is given by the ratio between C_b and C_e, while in the published report the slope used is the ratio between $C_bC_q/(C_b + C_q)$ and $C_eC_q/(C_e + C_q)$. Where C_q is assumed to be a constant value of $2\mu Fcm^{-2}$.

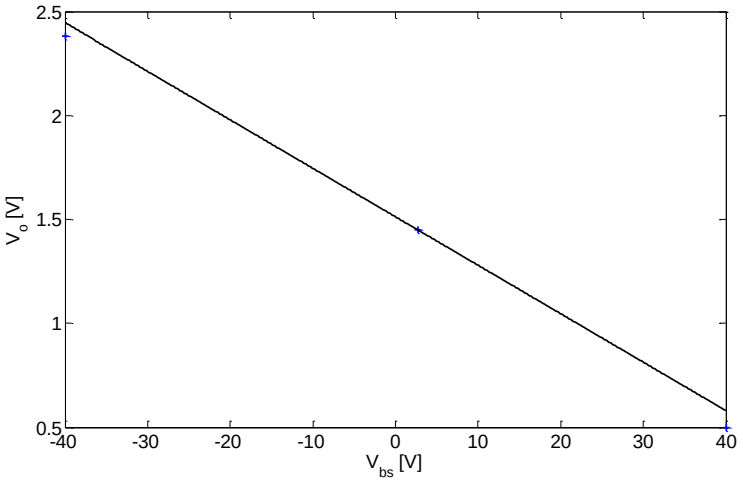


FIGURE 4.19: Threshold voltage against V_{bs} (Experimental data(+) [33], proposed model(–))

Fig. 4.19 shows the threshold voltage against V_{bs}. The best fit for the threshold voltage points estimates the top-gate dielectric to be 8.8.

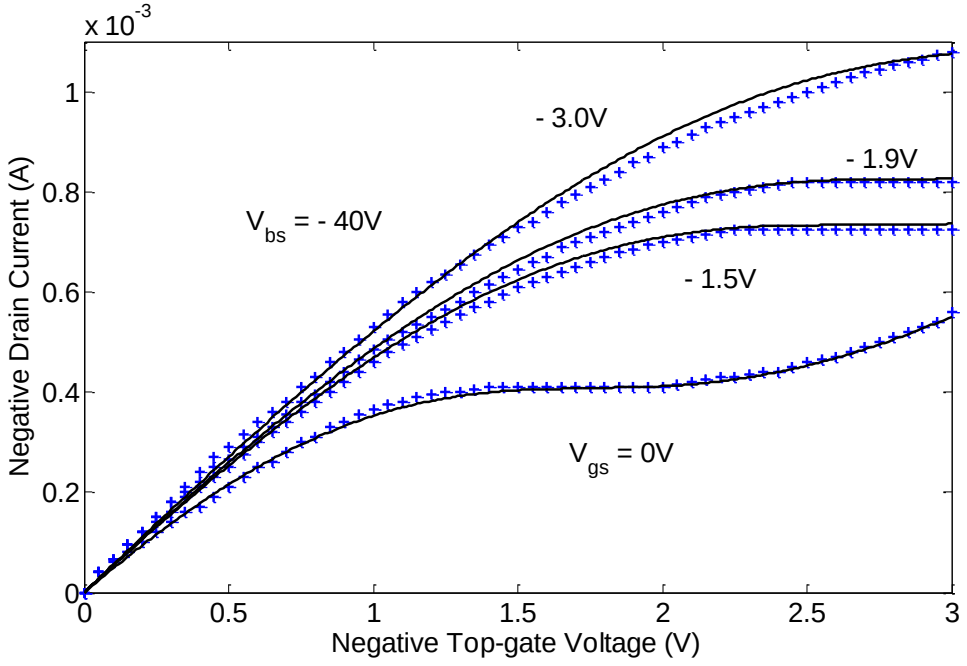


FIGURE 4.20: Experimental data (+) [33] and the proposed model (–) at an operating temperature of 1.7K for negative I_{ds} vs negative V_{ds} characteristics at V_{bs}=-40V. V_{ds} is varied from 0 to -3V for top-gate voltages of 0V, -1.5V, -1.9V and -3.0V (from bottom to top)

For the first test case, Fig. 4.20 shows the I-V characteristics for the transistor with a V_{bs} of -40V and V_{gs} of 0V, -1.5V, -1.9V and -3V. A good agreement with experimental

data is achieved with $V_T = 2$, $R_s = 800\Omega$, $E_c = 4.5kV/cm$, $\mu_h = 800cm^2/V.s$ and $\mu_n = 320cm^2/V.s$.

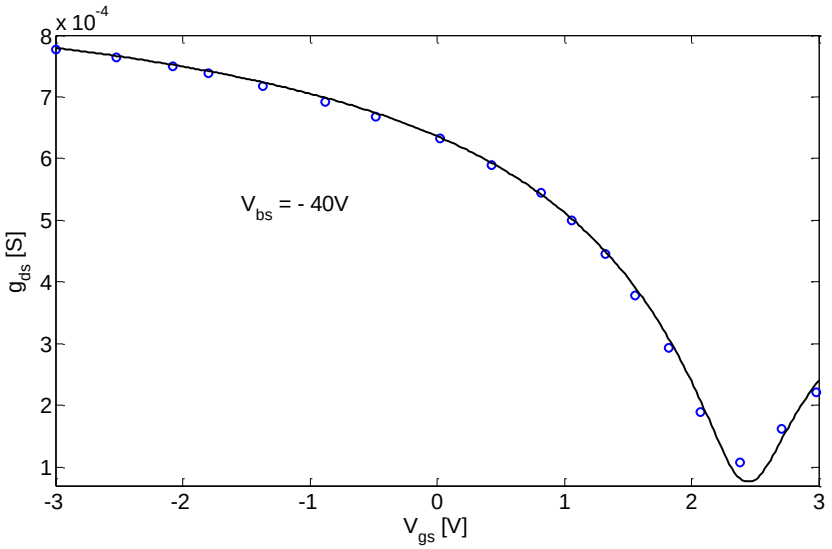


FIGURE 4.21: Characteristics of the channel output conductance against the top-gate voltage for $V_{bs} = -40V$ (Experimental data(o) [33], proposed model(–))

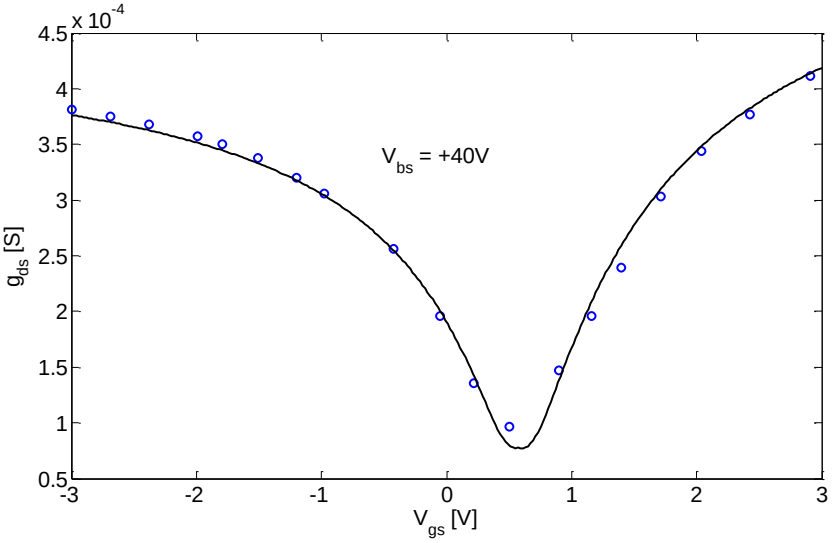


FIGURE 4.22: Characteristics of the channel output conductance against the top-gate voltage for $V_{bs} = 40V$(Experimental data(o) [33], proposed model(–))

The output conductance, g_{ds}, is defined as the variation in the drain current with a small variation in the drain-source voltage while keeping the gate-source voltage constant.

In Fig. 4.21, g_{ds} is plotted for a range of V_{gs} with V_{bs} of $-40V$. Carrier transport fitting parameters for both hole and electron conduction are shown in Table 4.7.

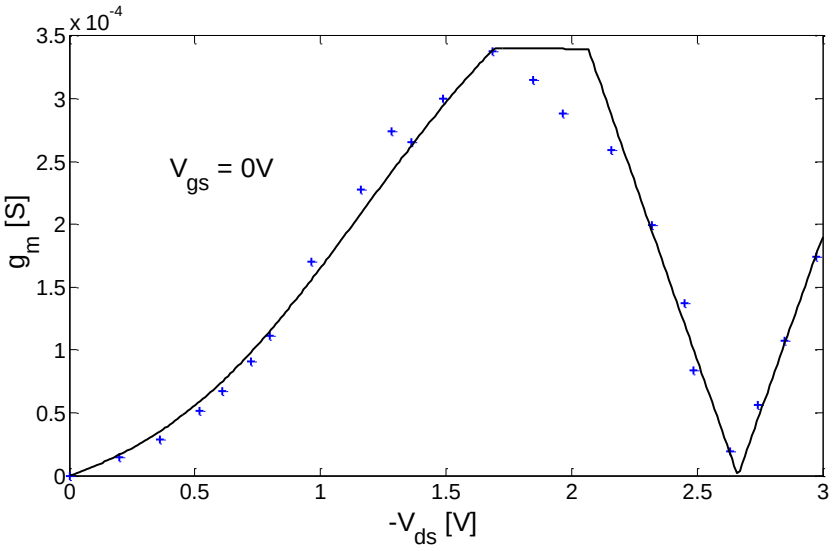


FIGURE 4.23: Characteristics of the channel transconductance against the top-gate voltage for $V_{bs} = -40V$ (Experimental data(+) [33], proposed model(–))

TABLE 4.7: Experimental data fitting parameters for output conductance

	hole		electron	
$V_{bs}[V]$	$R_s[\Omega]$	$\mu_h[cm^2/V.s]$	$R_s[\Omega]$	$\mu_e[cm^2/V.s]$
-40	530	800	850	800
40	1100	600	850	600

In Fig. 4.22, g_{ds} is plotted for a range of V_{gs} with V_{bs} of $40V$. Carrier transport fitting parameters for both hole and electron conduction are shown in Table 4.7.

Both figures of the output conductance show a good agreement against the experiment data. Using the intrinsic resistance extracted from the experimental data [33] in the model, the model accurately estimates the conductance at the charge neutrality point.

Back-gate voltages used are approximately $40V$ away from the intrinsic back-gate voltage of $2.7V$, as such a pronounced difference between R_q in the model and the maximum measured resistance from the original work is expected, due to the opening of a tunable band-gap [14, 47]. Therefore, this phenomenon implies that one layer of the transistor is torn. This is why the minimum conductance approximately $40V$ away from intrinsic state is the same as the intrinsic conductance.

The transconductance, g_m, is defined as the variation in the drain current with a small variation in the V_{gs} while keeping the V_{ds} and V_{bs} constant.

In Fig. 4.23, absolute g_m is plotted against V_{ds} for a $V_{gs} = 0V$ and a $V_{bs} = -40V$. The best fit with experimental data is for $R_s = 540\Omega$, $\mu_h = 1300cm^2/V.s$ and $E_c = 4.5e5V/m$ and $\mu_n = 702cm^2/V.s$. Fig. 4.22, 4.21 and 4.23 confirm that the Jacobian entries are continuous across the boundary points for all regions of operation.

The series resistance accounts for the contact resistance and the un-gated resistance (access resistance) between the contacts and the active area of the channel. For optimal RF application, the series resistance should be at a minimum. Between V_{bs} of $40V$ and V_{bs} of $-40V$ for hole conduction, in Table. 4.7, the series resistance is halved resulting in an enhancement of the transconductance [26].

4.4.4 Single-layer Model Applied To a Four Layer Graphene Channel

The model is validated against a four-layer GFET. With respect to a bilayer GFET, increasing the number of graphene layers results in a reduction in the tunable bandgap opened. Table 4.8 shows the model parameters.

TABLE 4.8: Model parameters for a four-layer GFET

Model parameter	Parameter value
$L(\mu m)$	10
$W(\mu m)$	5
$t_{ox}(nm)$	40
$E_c(KV/cm)$	8
ϵ_1	25.0
ϵ_2	3.9
$V_{gs}^0(V)$	0.75
$V_{bs}^0(V)$	0
$H_{sub}(nm)$	500
$V_{bs}(V)$	0
$n_0(m^{-2})$	0.5×10^{16}

The top-gate dielectric used is HfO_2 with a dielectric constant of 25 [160, 161] giving a capacitance, $C_e = 553nF/cm^{-2}$ and a temperature of 300K. Fig. 4.24 shows the effective gate-to-source capacitance, C_{top}, for a sweep of the top-gate voltage from $-2V$ to $3V$ for $V_{bs} = 0V$.

Fig. 4.25 plots the variation of the drain current with changes in V_{gs} for a V_{ds} of $0.1V$. Table 4.8 shows the model parameters of the transistor. The single-layer model gives the best fit against experimental data [127] using the following parameter fitting values; $R_s = 300\Omega$ and $\mu_h = 5000cm^2/V.s$ for hole conduction, and $R_s = 320\Omega$ and $\mu_e = 2800cm^2/V.s$ for electron conduction, $V_T = 8V$ and $R_s^0 = 3.7k\Omega$.

Fig. 4.26 shows the variation of the drain current against changes in the drain voltage. The model is validated against experimental data [127] for a V_{bs} of $0V$ and V_{gs} of -1.25V, -0.75V, -0.25V , 0.25V and 0.75V. The following model parameters show a good fit against experimental measurements; $V_T = 8$, $R_s = 400\Omega$, $\mu_h = 10000cm^2/V.s$ and $\mu_n = 2700cm^2/V.s$.

For low horizontal electric field, the channel transport is determined by R_s^0 at a V_{gs} of $0.75V$, the displacement saturation current becomes pronounced at high electric fields.

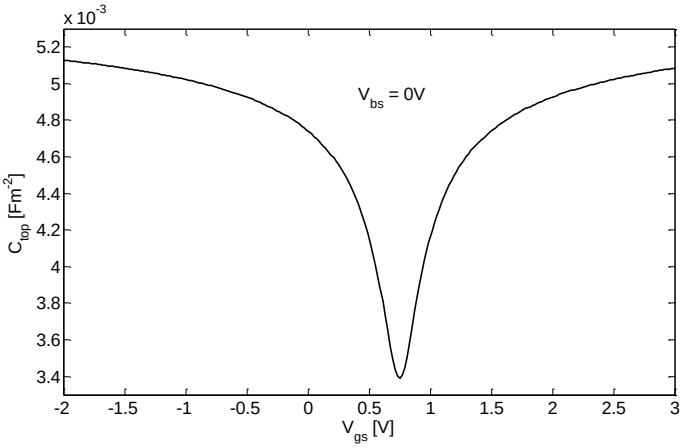


FIGURE 4.24: The effective top-gate capacitance, C_{top} against a sweep of V_{gs} from -3V to 3V for test case two

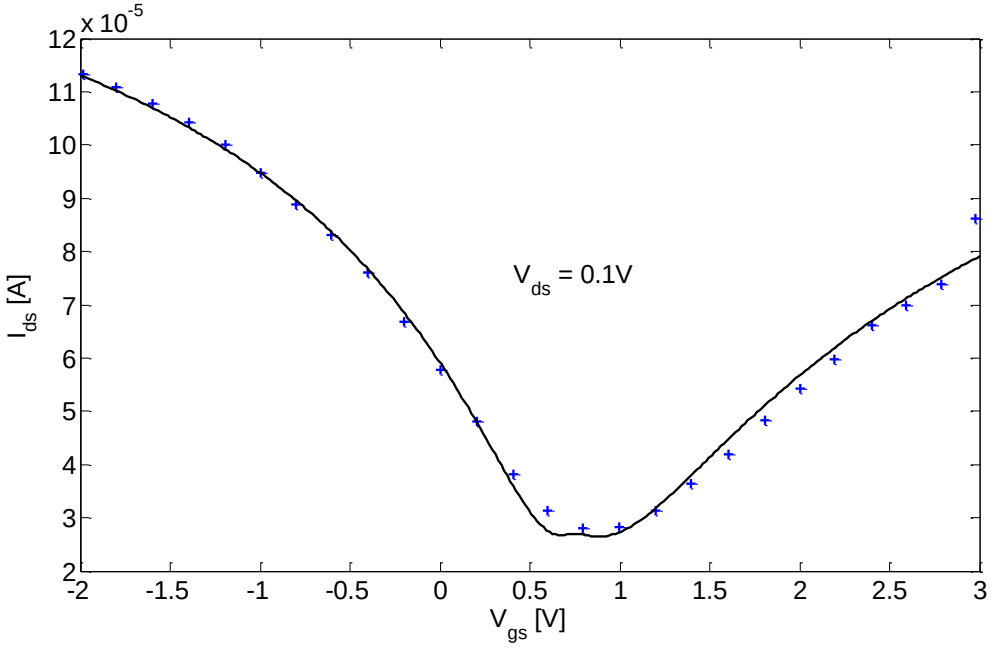


FIGURE 4.25: Characteristics of the channel Drain current against the top-gate voltage for $V_{ds} = 0.1V$ at room temperature(Experimental data(+) [127], proposed model(−))

The single-layer model gives a good agreement for a multi-layer transistor, especially at the region of the transistor where transport is dominated by the induced charges. When the transistor is in intrinsic state as shown in Fig. 4.25, the single-layer model also accurately estimates the current at the charge neutrality point. The shortfall of this model is that it does not estimate the minimum conductance when $V_{bs} \neq V_{bs}^{0}$.

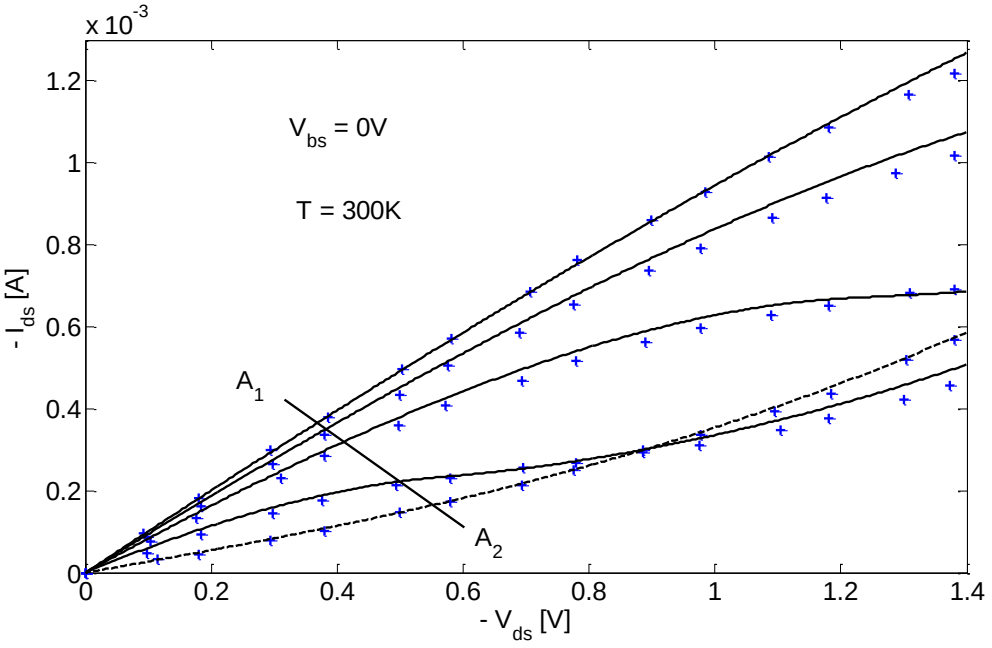


FIGURE 4.26: Experimental data (+) [127] and the proposed model (–) for negative I_{ds} vs negative V_{ds} characteristics at room temperature for V_{bs}= 0V. V_{ds} is varied from 0 to -1.4V for top-gate voltages of -1.25V, -0.75V, -0.25V, 0.25V and 0.75V (from top to bottom between cross-section A_1 and A_2)

4.5 Summary

This chapter presents a circuit level model of a single-gate single-layer graphene field effect transistor (GFET) and a dual-gate single-layer GFET suitable for a direct implementation in SPICE. Both models have been validated against experimental data published by another research group [89] and experimental data as part of this work. All validations show a good agreement.

Equations that calculate the drain current characteristics for both electron and hole conduction has been presented in a previous chapter. In this chapter, the model is mapped to the general model used to calculate the current transport.

To map this model to the general models, the surface potential is calculated self-consistently with the channel quantum capacitance and the gate-to-source capacitance. The effective gate capacitance is modelled as a series combination of the gate capacitance and the channel's quantum capacitance. The thermionic resistance is modelled in parallel with the resistance that results due to the induced charges in the channel.

From the current transport, this chapter provides an accurate estimation of the channel conductance. The model has been validated against published experimental data and shows a good agreement. Unlike silicon based channels with lower hole mobilities, an approximately equal hole and electron mobility is used in the model. The model also

accurately estimates the conductance at the charge neutrality point. This chapter derives a linear relationship between the threshold voltage and the back-gate voltage in the case of a dual-gate transistor, the slope of the relationship being the ratio of both gate capacitances. The threshold voltage gives the voltage of the top-gate at which the channel will experience charge neutrality, that is minimum conduction. In the case of a single-gate transistor, only one threshold voltage exists, with no bandgap opened irrespective of the number of graphene layers.

Computing the potential energy in the layers, the model establishes that at the charge neutrality point there is a zero potential energy. Thus, a single-layer GFET is a zero bandgap device. Also, the single-layer currently developed shows a high minimum conductance at room temperature, in the order of millisiemens. This is not suitable for digital circuitry applications. Equally, the conductance does not change remarkably between room temperature and 50K. To get any off state resistance meaningful for digital circuits the device has to be operated close to 0K.

In validating the model against experimental results from a multi-layer graphene, the model shows a good agreement for both the drain current against the drain voltage and against the gate voltage. In cases where a band-gap opening occurs, the model cannot determine the resulting maximum channel resistance. Thus, a modification to the equivalent model is necessary depending on the number of layers.

Chapter 5

Dual-gate multi-layer graphene FET model

This chapter presents models specific to a two and four channel graphene transistor. For the multi-layer specific models, the chapter shows how the models are extended from the single-layer model described in chapter 4.

The model provides an accurate estimation of the conductance at the charge neutrality point (CNP). Features of the model presented here include; equations for the channel resistance at the CNP, off-currents for a range of electric fields perpendicular to the channel, channel resistance dependence on temperature and an estimation of the amount of bandgap opening created by the application of an electric field.

A number of models of the transfer characteristics for a bilayer graphene FET have been published [33, 38, 34, 129, 130, 131, 132]. These models show a good agreement with experimental data. However, these models cannot estimate the amount of bandgap opening and how this bandgap influences the off-current. This work is first to present a model that can calculate the off-current as a result of the opening of a tunable bandgap in graphene as well as the dependence of the off-current on temperature.

As done in the case of the single-layer model in chapter 4, the multilayer specific circuit-level model is mapped to the equivalent general model. Thus, the equation derived in Chapter 3 will be used to calculate the drain current.

Some models [33, 38, 34] use a linear relationship of the back-gate voltage to calculate the threshold voltage (that is the top-gate voltage at the CNP). Although this method proves a simple way to estimate the threshold voltage and it is accurate for the single-layer graphene FET (see Fig. 4.13), an experiment [77] shows that the linear relationship can deviate substantially for back-gate voltages further away from the back-gate voltage at the Dirac point. In this work, the equivalent circuit presented is used to calculate the threshold voltage.

5.1 Bilayer Capacitance Model

Compared to existing models, this work introduces an interlayer capacitance which is used in calculating the channel surface potential and the channel resistance at the charge neutrality point (CNP). Fig. 5.1 shows the schematic of a bilayer transistor. The bilayer graphene composes of two layers of graphene held together by Van der Waals forces. It is assumed in this work that the a free space exists between the layers. The interlayer capacitance has been used in determining the layer asymmetry and consequently estimating the bandgap opening [49, 47].

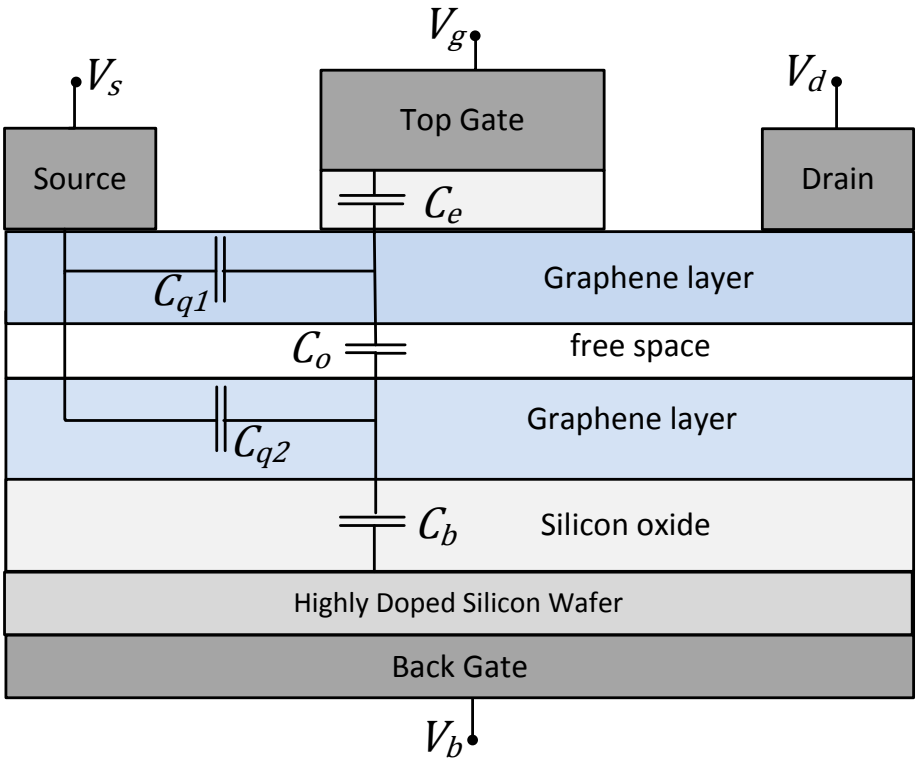


FIGURE 5.1: Bilayer graphene transistor layout

Fig. 5.2 shows an equivalent circuit for a bilayer graphene FET. single-layer samples of graphene have been reported to have a measured quantum capacitance [88] which is a function of the surface potential [86]. The proposed model uses a quantum capacitance for each layer namely $C_q(\varphi_{s1})$ and $C_q(\varphi_{s2})$ as shown in Fig. 5.2. Both quantum capacitances are separated by an interlayer capacitance, C_o. In naming the layers the convention used here numbers the layers relative to the top-gate, with the closest layer as 1, 2 for the next layer and so forth.

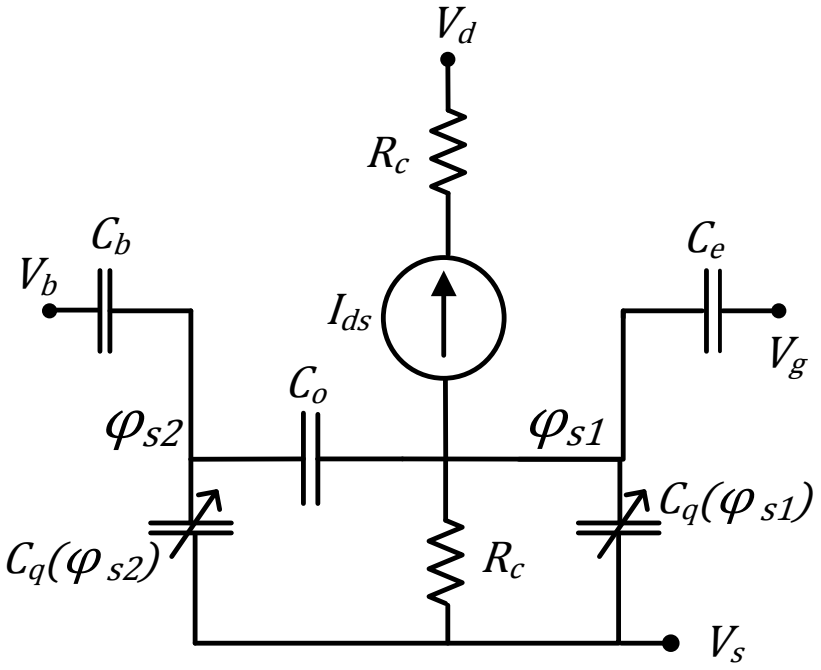


FIGURE 5.2: Proposed equivalent circuit for a bilayer graphene transistor

5.1.1 Surface Potential

For the top-layer, the quantum capacitance varies by its surface potential, φ_{s1}, represented by Eqn. (5.1):

$$C_{qvar}(\varphi_{s1}) = q^2 \frac{2}{\pi} \frac{q|\varphi_{s1}|}{(\hbar v_f)^2} \tag{5.1}$$

where v_f is the Fermi velocity [87], electronic charge q and the reduced Plank's constant $\hbar$. At $\varphi_{s1} = 0$ the channel has been reported to have a charge density, n_0 [70, 74]. Taking n_0 into consideration, at $\varphi_{s1} = 0$ the resulting capacitance is shown below.

$$C_{qmin} = \frac{q^2\sqrt{n_0}}{\sqrt{\pi}\hbar v_f} \tag{5.2}$$

From the Drude model the charge density in the channel is $n = \sqrt{n_0^2 + n_*^2}$ where n_* is the charge density caused by the gate potential. Hence, the quantum capacitance of the layer is $C_q(\varphi_s)$.

$$C_q(\varphi_s) = \frac{C_{qmin}^2 + 2(C_{qvar}(\varphi_s)/2)^2}{\sqrt{C_{qmin}^2 + (C_{qvar}(\varphi_s)/2)^2}} \tag{5.3}$$

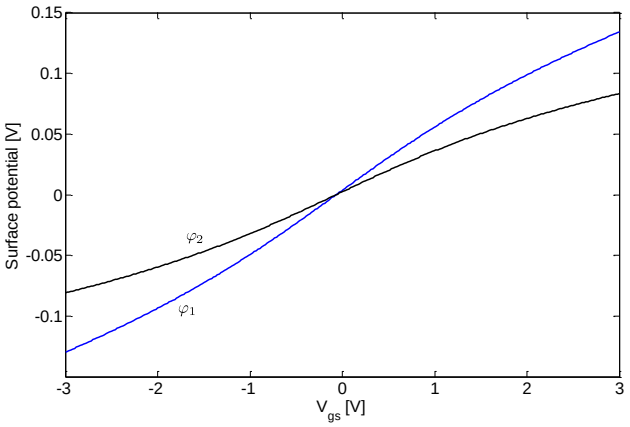


FIGURE 5.3: The surface potential φ_{s1} and φ_{s2} of the layers as a function of V_{gs} at $V_{bs} = 50V$.

From the capacitance model in Fig. 5.2 the surface potentials can be solved, given that C_e is the capacitance due to the dielectric between the top-gate and the channel, C_b is the capacitance between the channel and the back-gate, V_d, V_g, V_s and V_b are the drain, top-gate, source and back-gate voltages respectively. Therefore, the surface potential of the second layer is shown in Eqn. (5.4):

$$\varphi_{s2} = \frac{1}{C_o}\left[-C_e(V_{gs} - V_{gs}^0) + \varphi_{s1}(C_e + C_o) + \varphi_{s1}\sqrt{(C_{qvar}(\varphi_{s1})/2)^2 + C_{qmin}^2}\right] \tag{5.4}$$

where V_{gs}^0 is the top-gate-to-source Dirac point voltage and V_{bs}^0 is the back-gate-to-source Dirac point voltage. Equally, the first layer surface potential is shown below.

$$\varphi_{s1} = \frac{1}{C_o}\left[-C_b(V_{bs} - V_{bs}^0) + \varphi_{s2}(C_e + C_o) + \varphi_{s2}\sqrt{(C_{qvar}(\varphi_{s2})/2)^2 + C_{qmin}^2}\right] \tag{5.5}$$

φ_{s1} determines the conduction state of the channel. For example, Fig. 5.3 (see parameter values in test case B of Table 5.2) shows the behavior of the surface potential of both layers as a function of V_{gs} for $V_{bs} = 50V$. Algorithm 2 shows how φ_{s1} and φ_{s2} are calculated. Positive values of φ_{s1} indicates the Fermi level is in the conduction band,

Data: The capacitances C_q, C_b, C_o, C_{qmin},C_{qvar}, the inbuilt voltages, V_{bs}^0, V_{gs}^0, the gate voltages, V_{gs}, V_{bs}
Result: The surface potentials φ_{s1} and φ_{s2}
Initialize φ_{s1} to a value
for i = *start value to stop value* **do**
  φ_{s2} = Eqn. (5.4)
  φ_{s1new} = Eqn. (5.5)
  Compare = Compare φ_{s1new} and φ_{s1}
  if *Compare is less than error tolerance range* **then**
    Retain the values of φ_{s1} and φ_{s2}
    End iterations
  else
    if $\varphi_{s1} > \varphi_{s1new}$ **then**
      Increment φ_{s1}
    else
      Decrement φ_{s1}
    end
  end
end

Algorithm 2: Solving self-consistency in bilayer GFET

negative values indicates the Fermi level is in the valence band and a zero value indicates a charge neutrality point [14].

5.1.2 Effective Gate Capacitance

Since the top-gate capacitance is comparable to the quantum capacitance, to accurately model the capacitance between V_g and V_s the quantum capacitance has to be taken into consideration. This gives an effective capacitance, C_{top}, shown below.

$$C_{top} = \frac{C_e(C_oC_q(\varphi_{s2}) + (C_o + C_q(\varphi_{s2}) + C_b)C_q(\varphi_{s1}))}{C_oC_q(\varphi_{s2}) + (C_o + C_q(\varphi_{s2}) + C_b)(C_q(\varphi_{s1}) + C_e)} \tag{5.6}$$

5.1.3 Threshold Voltage

Eqns. (5.4) and (5.5) are the surface potential of both layers as a function of V_{gs}. At charge neutrality, $\varphi_{s1} = 0$ and the value of V_{gs} which satisfies this condition is referred to as the threshold voltage, V_o.

$$V_o = V_{gs}^0 - \varphi_{s2}\frac{C_o}{C_e} \tag{5.7}$$

5.2 Four-layer Capacitance Model

A major feature of the models presented here is that the quantum capacitance is computed layer by layer as shown in Fig. 5.4. The model avoids representing the entire channel by a single quantum capacitance irrespective the number of channel layers.

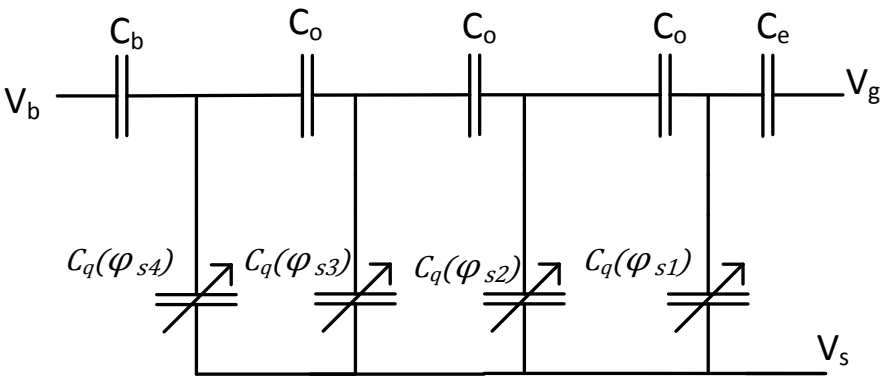


FIGURE 5.4: schematic four-layer graphene transistor capacitance model

The quantum capacitance of each layer is calculated the same way that each layer is done for the bilayer transistor in section 5.1. In each layer, C_q is composed of two parallel capacitances; a variable capacitance, C_{qvar}, given by Eqn. (5.1) and a fixed capacitance, C_{qmin}, given by Eqn. (5.2). Equally here, the naming convention is maintained with the layer closest to the top-gate assigned an index number 1.

5.2.1 Surface Potential

Between each layer is an interlayer capacitance, C_o. By solving the capacitance model shown in Fig. 5.4 the surface potential of each layer can be calculated. For multilayer cases, it is mathematically challenging to deduce an analytical expression for the surface potential. Hence, numerical analysis is used.

The equation of the surface potential for each of the layers is given by the following equations.

$$\varphi_{s2} = \frac{1}{C_o}\left[-C_e(V_{gs} - V_{gs}^0 - \varphi_{s1}) + \varphi_{s1}C_o \right. \\ \left. \varphi_{s1}\sqrt{(C_{qvar}(\varphi_{s1})/2)^2 + C_{qmin}^2}\right] \tag{5.8}$$

$$\varphi_{s3} = \frac{1}{C_o}\left[\varphi_{s2}\sqrt{(C_{qvar}(\varphi_{s2})/2)^2 + C_{qmin}^2} + 2\varphi_{s2}C_o\right] - \varphi_{s1} \tag{5.9}$$

$$\varphi_{s4} = \frac{1}{C_o}\left[\varphi_{s3}\sqrt{(C_{qvar}(\varphi_{s3})/2)^2 + C_{qmin}^2} + 2\varphi_{s3}C_o\right] - \varphi_{s2} \tag{5.10}$$

To establish self consistency of the surface potential in the various layers, Eqn. (5.10) has to be within a tolerance range to Eqn. (5.11).

$$\varphi_{s4} = \frac{1}{C_o}\left[-C_b(V_{bs} - V_{bs}^0 - \varphi_{s3}) + \varphi_{s3}C_o \right. \\ \left. \varphi_{s3}\sqrt{(C_{qvar}(\varphi_{s3})/2)^2 + C_{qmin}^2}\right] \tag{5.11}$$

In a similar fashion, the initially guessed value of φ_{s1} has to be in tolerance range with Eqn. (5.12):

$$\varphi_{s1} = \frac{1}{C_o}\left[\varphi_{s2}\sqrt{(C_{qvar}(\varphi_{s2})/2)^2 + C_{qmin}^2} + 2\varphi_{s2}C_o\right] - \varphi_{s3} \tag{5.12}$$

where both φ_{s3} and φ_{s2} are re-calculated from φ_{s4} in Eqn. (5.11).

Data: The capacitances C_q, C_b, C_o, C_{qmin}, C_{qvar}, the inbuilt voltages, V_{bs}^0, V_{gs}^0, the gate voltages, V_{gs}, V_{bs}
Result: The surface potentials φ_{s1}, φ_{s2}, φ_{s3} and φ_{s4}
Initialize φ_{s1} to a value
for *i = start value to stop value* **do**
  φ_{s2} = Eqn. (5.8)
  φ_{s3} = Eqn. (5.9)
  φ_{s4} = Eqn. (5.10)
  φ_{s1new} = Eqn. (5.12)
  Compare = Compare φ_{s1new} and φ_{s1}
  if *Compare is less than error tolerance range* **then**
    Retain the values of φ_{s1}, φ_{s2}, φ_{s3} and φ_{s4}
    End iterations
  else
    if $\varphi_{s1} > \varphi_{s1new}$ **then**
      Increment φ_{s1}
    else
      Decrement φ_{s1}
    end
  end
end

Algorithm 3: Solving self-consistency in four layer GFET

Using Algorithm 3, Fig. 5.5 shows the surface potential of each of the four layers for variation in the top-gate voltage. The surface potential of layer 1 determines the carrier doping of the channel as done for the bilayer model. Its positive sign indicates electron-like conduction and its negative sign indicated hole-like conduction.

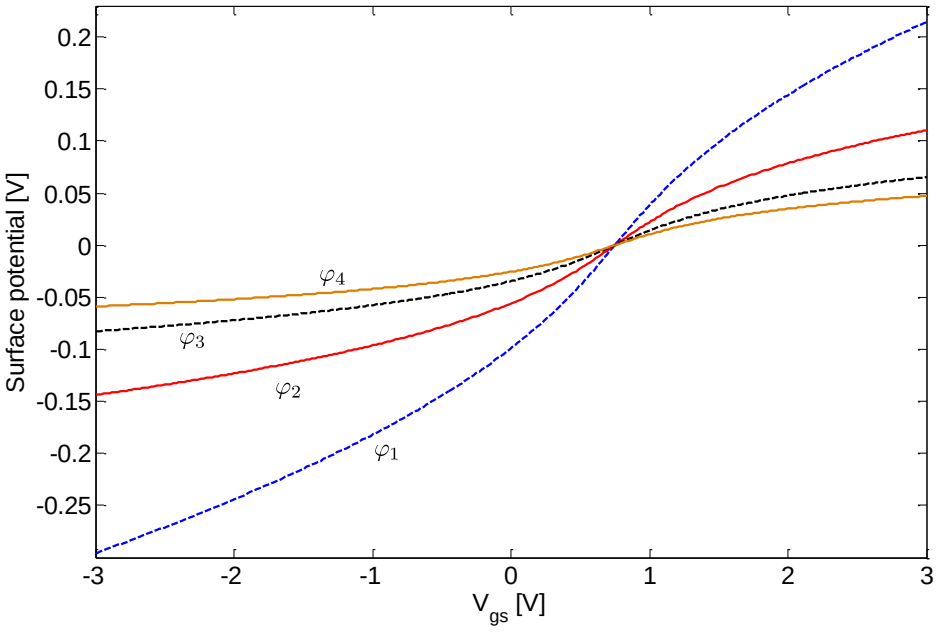


FIGURE 5.5: The surface potential for each of the four layers as a function of V_{gs} at $V_{bs} = 0V$.

5.2.2 Effective Gate Capacitance

To successfully map this model to the general model in order to compute its drain current, the capacitance model has to be represented by an effective capacitance C_{top}.

$$\begin{aligned} C_3 &= \frac{C_o C_q(\varphi_{s4})}{C_o + C_q(\varphi_{s4}) + C_b} \\ C_2 &= \frac{C_o(C_3 + C_q(\varphi_{s3}))}{C_o + C_3 + C_q(\varphi_{s3})} \\ C_1 &= \frac{C_o(C_2 + C_q(\varphi_{s2})}{C_o + C_2 + C_q(\varphi_{s2})} \\ C_{top} &= \frac{C_e(C_1 + C_q(\varphi_{s1})}{C_e + C_1 + C_q(\varphi_{s1})} \end{aligned} \tag{5.13}$$

5.2.3 Threshold Voltage

By following the convention of charge neutrality when $\varphi_{s1} = 0$, the threshold is calculated by solving Eqn. (5.8).

$$V_o = V_{gs}^0 - \varphi_{s2}\frac{C_o}{C_e} \tag{5.14}$$

Thus, both the bilayer transistor (see Eqn. (5.7)) and the four layer transistor (see Eqn. (5.14)) show a dependence of the threshold on φ_{s2}. φ_{s2} at charge neutrality can be calculated using Algorithm 4.

Data: The capacitances C_q, C_b, C_o, C_{qmin},C_{qvar}, the inbuilt voltages, V_{bs}^0, V_{gs}^0, the gate voltages, V_{gs}, V_{bs}
Result: The surface potentials φ_{s2}, φ_{s3} and φ_{s4}
Initialize φ_{s2} to a value
for *i = start value to stop value* **do**
  φ_{s3} = Eqn. (5.9)
  φ_{s4} = Eqn. (5.10)
  solve φ_{s2new} from Eqn. (5.12)
  Compare = Compare φ_{s2new} and φ_{s2}
  if *Compare is less than error tolerance range* **then**
    Retain the values of φ_{s2}, φ_{s3} and φ_{s4}
    End iterations
  else
    if $\varphi_{s1} > \varphi_{s1new}$ **then**
      Increment φ_{s1}
    else
      Decrement φ_{s1}
    end
  end
end

Algorithm 4: Surface potential at threshold voltage in four layer GFET

The threshold voltage of any dual-gate multilayer graphene channel irrespective of the number of layers is a linear relationship against the φ_{s2}. The slope of which is determined by the ratio of the interlayer capacitance and the top-gate capacitance. Equally, for a single-layer channel a similar linear relationship of the threshold is deduced.

5.2.4 Bilayer Electric Field Gap

In the presence of an electric field perpendicular to the channel, the A_2 and B_1 site (see section 2.0.2) inter-layer coupling breaks giving rise to a bandgap which is tunable. The value of this tunable bandgap is calculated at the threshold voltage. In the case of multi-layered channels, each layer will have a surface potential which will result in a band energy. The potential energy at the threshold voltage determines this minimum band energy referred to as the bandgap.

Considering the bilayer graphene shown in Fig. 5.6 with interlayer capacitance, C_o, the charge density on the first layer is Q_{s1} and the charge density of the second layer is Q_{s2}.

$$Q_{s1} = \frac{\varphi_{s1}}{2} C_{qvar}(\varphi_{s1}) \tag{5.15}$$

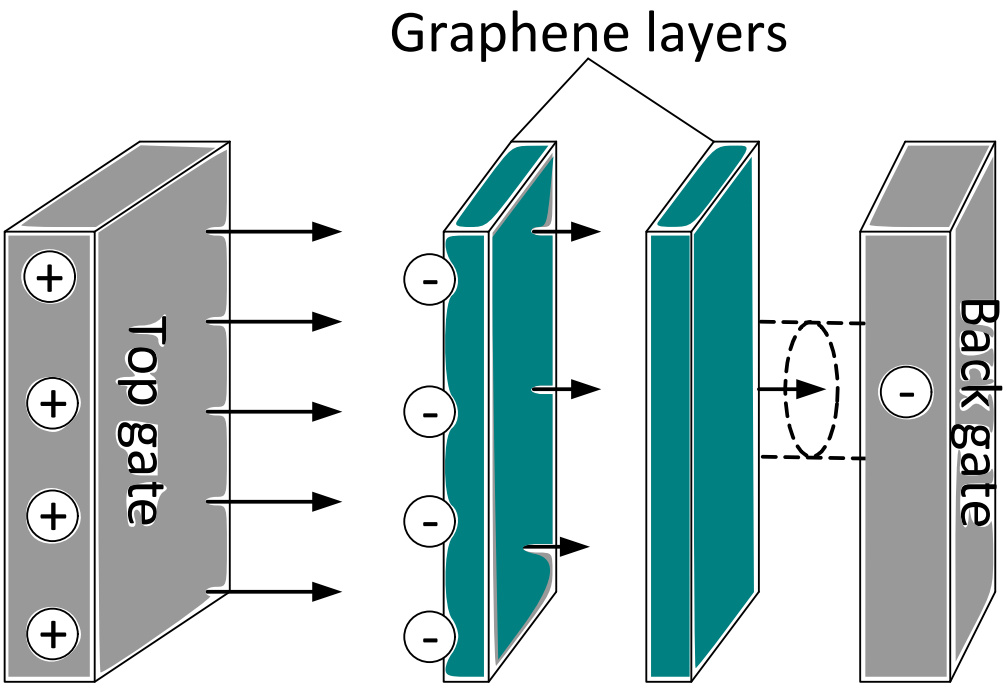


FIGURE 5.6: Schematic of a bilayer graphene with metallic gate terminal showing the electric field. The dash lines show the Gaussian surface which is induced by the electric field between the layers

$$Q_{s2} = \frac{\varphi_{s2}}{2} C_{qvar}(\varphi_{s2}) \tag{5.16}$$

At charge neutrality the charge density of layer 2 corresponds to the excess charge density. The corresponds change in potential energy is represented by Eqn. (5.17).

$$\Delta U_s = \frac{\varphi_{s2}^2}{6} C_{qvar}(\varphi_{s2})) \tag{5.17}$$

Note that φ_{s2} used in Eqn. (5.17) satisfies the condition of charge neutrality, $\varphi_{s1} = 0$. The change in the potential energy ΔU_s determines the layer asymmetry [47]. The charge distributed throughout the layer gives rise to the electric field between the layers and the resulting change in potential energy determines the asymmetry between the layers [47].

Introducing the bare asymmetry [47, 49] for a non zero density the total potential energy is given by Eqn. (5.18).

$$U_s = \frac{\varphi_{s1}^2}{6} C_{qvar}(\varphi_{s1})) + \Delta U_s \tag{5.18}$$

While ΔU_s is constant for a given back-gate voltage, the potential energy of layer 1 (the first part of Eqn. (5.18)) varies by the top-gate voltage.

The interaction of the electric field from graphene to the back-gate results in a potential energy $1/2C_bV_E^2$. Where V_E is the potential difference as a result of a uniformly distributed charge.

$$V_E = \sqrt{\frac{2U_s}{C_b}} \tag{5.19}$$

For a given temperature, V_E being a reflection of the bandgap opening should satisfy the relationship $R_q \propto \exp(V_E/V_T)$.

$$R_q = R_s^0 \exp(V_E/V_T) \tag{5.20}$$

Where R_s^0 is the resistance at intrinsic state, that is at charge neutrality condition with zero bandgap opening and V_T is a constant voltage.

Based on the Drude model used in characterising graphene devices, R_s^0 can be obtained from Eqn. (5.21):

$$R_s^0 = \frac{L}{Wqn_o\mu} \tag{5.21}$$

where L is the channel length, W is the channel width, q is the electronic charge, n_o is the minimum charge density and μ is the mobility.

The bandgap opening is determined for a zero charge density, when the channel experiences charge neutrality, for a given back-gate voltage. Eqn. (5.20) gives a channel resistance R_q.

$$R_q = R_s^0 \exp\left(\sqrt{\frac{\varphi_{s2}^2 C_{qvar}(\varphi_{s2})}{3V_T^2 C_b}}\right) \tag{5.22}$$

5.2.5 Four-layer Electric Field Gap

Fig. 5.7 shows the general schematic of a multi-layer graphene with m channels. In the case of more than two layers the potential energy is given by the summation of both the bare asymmetry and the potential difference between adjacent layers. Given that for a four-layer channel U_1, U_2, U_3 and U_4 are the respective potential energies. The potential difference between layer 1 and 2 ($U_{12} = U_1 - U_2$) is as shown in Eqn. (5.17). Hence, ΔU_s is given by $U_{12} + U_{23} + U_{34}$.

$$\Delta U_s = \frac{\varphi_{s4}^2}{6} C_{qvar}(\varphi_{s4})) \tag{5.23}$$

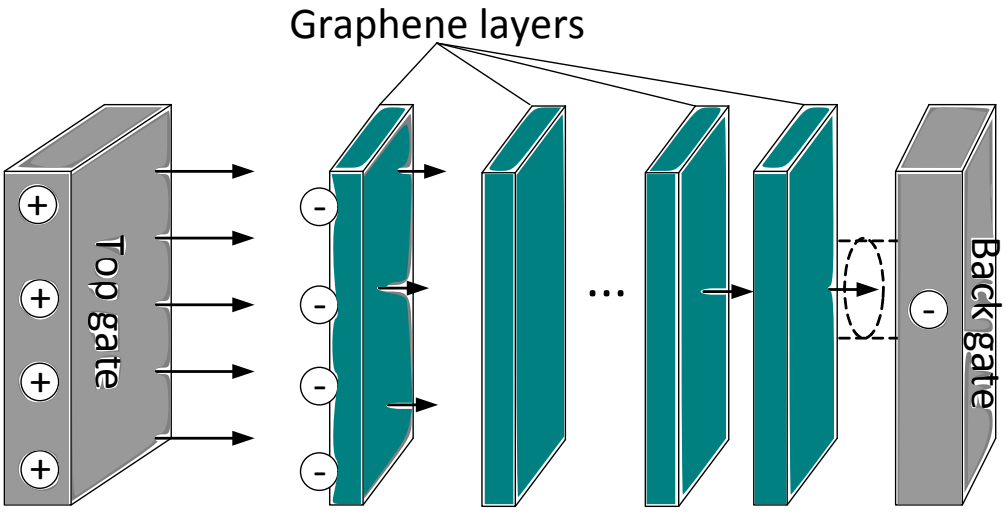


FIGURE 5.7: Schematic of a multi-layer graphene with metallic gate terminal showing the electric field. Where m is the number of graphene layers. The dash lines show the Gaussian surface which is induced by the electric field between the layers

Note that Eqn. (5.23) is a constant for a given V_{bs}. The excess charge used to calculate the change in potential energy must satisfy the condition of charge neutrality, $\varphi_{s1} = 0$.

Hence, it can be observed that the change in potential energy is given the excess charge in the m^{th} layer. In the case here of a four-layer channel $m = 4$. Eqn. (5.23) is then used in Eqns. (5.18), (5.19) and (5.20) to calculate the off-current resistance with respect to variations in the electric field.

5.2.6 Temperature Dependence

Analytical equation that model the dependence of the channel conductance against temperature has been presented in section 4.2.2. These equations equally apply to a multi-layer graphene transistor.

The factor R_T is thereby multiplied to Eqn. (5.20) to capture the resistance's dependence on temperature.

$$R_T = \exp\left(\left(\frac{T_o(T_{ref} - T)}{TT_{ref}}\right)^{1/3}\right) \tag{5.24}$$

By decreasing the electric field, the fitting parameter T_o equally decreases. T_o relates with surface potential at the threshold voltage by a phenomenological equation.

$$T_o = T_\alpha \exp\left(\frac{\eta\varphi_{s2}}{\varphi_\alpha}\right) \tag{5.25}$$

where η, T_α and φ_α are characteristic, temperature and voltage fitting constants respectively. φ_{s2} is the surface potential at the CNP when $\varphi_{s1} = 0$.

Therefore, the off-current is shown below.

$$I_{off} = V_{ds}/R_q \tag{5.26}$$

The drain current is a root of the sum of squares of both the off-current, I_{off} and the drift current, I_{ds*} (see Chapter. (3), Eqn. (3.17)).

$$I_{ds} = \sqrt{I_{off}^2 + I_{ds*}^2} \tag{5.27}$$

For a semiconductor with appreciable bandgap and sharply defined energy bands, the off-current has a exponential relationship against T^{-1}. The bandgap opening is estimated relative to the general Schottky barrier equation, $exp(\Delta E/2k_BT)$, where ΔE is the bandgap and k_B is the Boltzmann's constant.

$$\Delta E = 2k_BT\left(\left(\frac{T_o(T - T_{ref})}{TT_{ref}}\right)^{1/3} + \frac{V_E}{V_T}\right) \tag{5.28}$$

5.3 Experimental Validation

The presented model is validated against published experimental data for both a bilayer and a four-layer graphene FET. Five test cases are used in the validation process. An interlayer separation, t_{il}, of $0.335nm$ between the top and bottom layer in the graphene channel is assumed. This is consistent with experiment and theory [49, 50, 51] for Bernal stacking structure of two layer graphene. Thus, C_o, has a capacitance of $2.64\mu Fcm^{-2}$ using a dielectric constant of 1.

5.3.1 Test Case A

Test cases A transistor use HfO_2 as the top-gate dielectric with SiO_2 for back-gate dielectric. The model parameters are shown in Table 5.1

For test case A, Fig. 5.8 shows a plot of the threshold voltage against V_{bs}. A good fit against experimental data is attained with $C_e \approx 319nFcm^{-2}$, thus the top-gate dielectric constant, ϵ_1, is estimated to be 5.4.

Fig. 5.9 shows a plot of the off-current of the transistor for three sets of V_{bs} values. In this test case, the model shows a good agreement with the transistor measurements

TABLE 5.1: Model parameters for bilayer graphene FET in test case A

Model parameter	Parameter value
Ref	[33]
$L(\mu m)$	1
$W(\mu m)$	2.1
$t_{ox}(nm)$	15
$t_{il}(nm)$	0.335
ϵ_2	3.9
$V_{gs}^0(V)$	1.45
$V_{bs}^0(V)$	2.7
$V_T(V)$	2.0
$H_{sub}(nm)$	285
$R_s^0(k\Omega)$	12.88

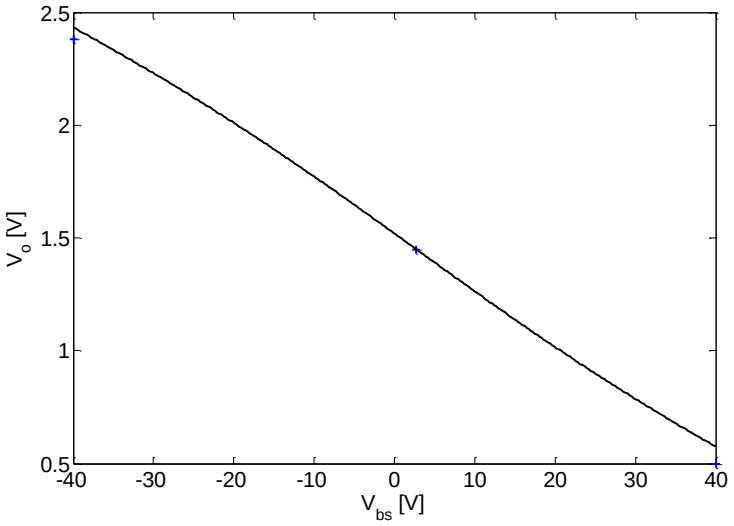


FIGURE 5.8: The threshold voltage, V_o, against V_{bs} for the Experimental data (+) [33], the proposed model (solid line)

at $V_{bs} = 2.7$ using the following fitting parameters; $V_T = 2.0V$, $C_e \approx 319nFcm^{-2}$, $T = 300K$, $n_0 = 1.0 \times 10^{16}m^{-2}$ and an intrinsic resistance, $R_s^0 = 12.88k\Omega$. For the other two measured points, $V_{bs} = 40V$ and $V_{bs} = -40V$, shown in Fig. 5.9 there is a deviation between the model and the measured data. The measured data shows an equal resistance for all three points, a behaviour consistent with a single-layer graphene FETs where there is no bandgap opening due to electric field.

Hence, the bilayer model estimates a lower conductance than is measured by the experiment. This can be attributed to a tear in one of the layers resulting in the minimum conductance that is well captured by a single-layer model.

The output conductance, g_{ds}, is defined as the variation in the drain current for a small variation in the drain-source voltage while keeping the gate-source voltage constant.

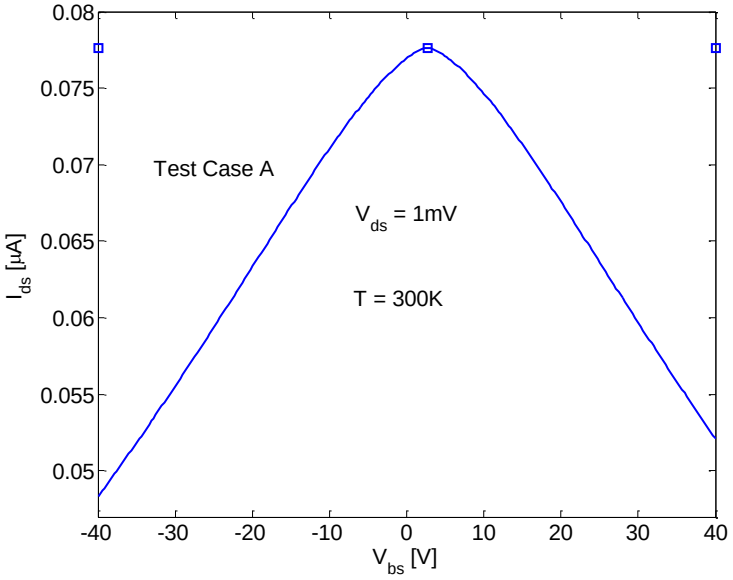


FIGURE 5.9: A plot of the device off-current against V_{bs} for $V_{ds} = 1mV$ shows the proposed model against experimental data for case A (experimental data (□) [33]) at room temperature

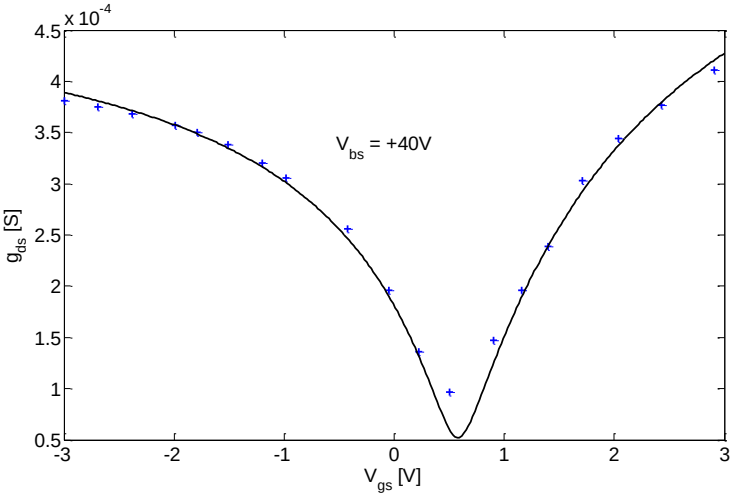


FIGURE 5.10: Transfer Characteristics of the channel output conductance at room temperature against the top-gate voltage for $V_{bs} = 40V$ for published experimental data(+) [33] and the proposed model(–)

In Fig. 5.10 g_{ds} is plotted against V_{gs} from -3V to 3V with $V_{bs} = 40V$ and $V_{ds} = 0.01V$. For the best fit against the experimental data, $R_c = 1000\Omega$ and $\mu = 3000cm^2/Vs$ for hole conduction and $R_c = 700\Omega$ and $\mu = 2700cm^2/Vs$ for electron conduction.

In Fig. 5.11 g_{ds} is plotted against a sweep of V_{gs} from -3V to 3V with V_{bs} = -40V and $V_{ds} = 0.01V$. For the best fit against the experimental data, $R_c = 515\Omega$ and $\mu = 4400cm^2/Vs$ for hole conduction, and $R_c = 300\Omega$ and $\mu = 2700cm^2/Vs$ for electron conduction.

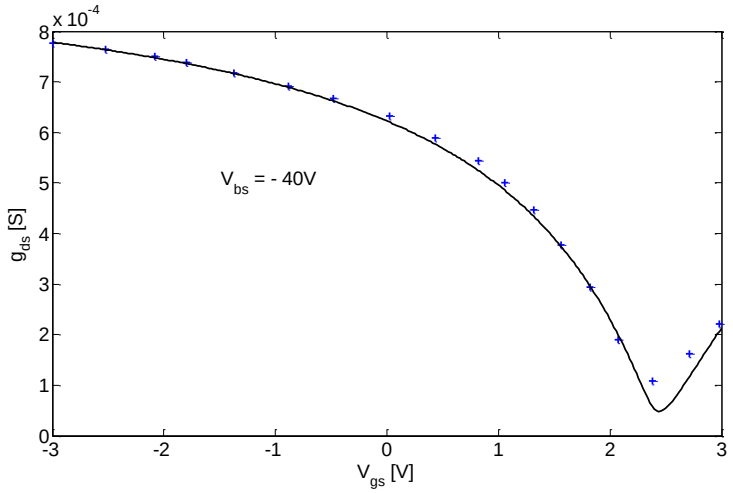


FIGURE 5.11: Transfer characteristics of the channel output conductance at room temperature against the top-gate voltage for $V_{bs} = -40V$ for published experimental data(+) [33] and the proposed model(–)

When this experiment is validated using a single-layer model, C_e was estimated to have a dielectric constant of 10 compared to a dielectric constant of 5.4 in this test case. This shows that the measuring of the device parameters is strongly dependent on the model used in characterizing the transistor.

5.3.2 Test Case B

In Test case B the top-gate dielectric is a stack of HfO_2 on a derivative of polyhydroxystyrene (the polymer NFC 14003CP manufactured by JSR Micro, Inc) with SiO_2 as back-gate dielectric. Table 5.2 shows the model parameters that fit the experimental data in all cases.

TABLE 5.2: Model parameters for bilayer graphene FET

Model Name	Model value
Ref	[77]
$L(\mu m)$	3
$W(\mu m)$	1.6
$t_{ox}(nm)$	10
$t_{il}(nm)$	0.335
ϵ_2	3.9
$V_{gs}^0(V)$	-0.066
$V_{bs}^0(V)$	50
$V_T(V)$	1.75
$H_{sub}(nm)$	300
$R_s^0(k\Omega)$	8.08

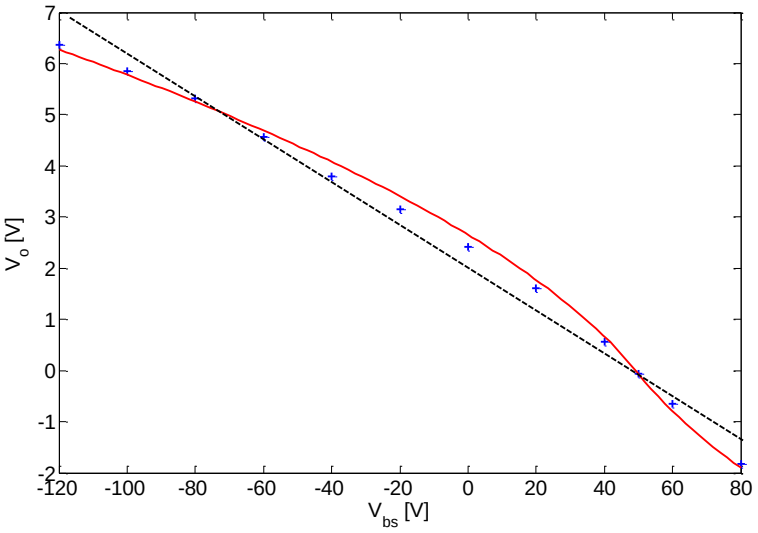


FIGURE 5.12: Threshold voltage, V_o, against V_{bs} for published experimental data (+) [77], the proposed model (solid line) and the best fit of a straight line (dash lines)

To accurately determine the top-gate capacitance, the model is validated against the extracted threshold voltage for a range of V_{bs}. Fig. 5.12 gives a good fit against the experiment results with $C_e \approx 133nFcm^{-2}$ which estimates the top-gate dielectric ϵ_1 to be 1.5.

By using a line of best fit in the plot of V_o against V_{bs}, it is observed that a straight line greatly diverges from the experiment for large values of V_{bs}. This shows that although a single-layer model presents a simple technique of characterizing the transistor, it may not be sufficient in some cases.

Since the threshold voltage is the point of charge neutrality for a given V_{bs}, it is also the top-gate voltage at which the off-current for a given V_{bs} flows. Fig. 5.13 shows the drain current of V_o against V_{bs} with $V_{ds} = 1mV$ at room temperature. The model shows a good agreement against experiment [77] for $V_T = 1.75V$.

The model shows a good agreement against the experiment data [77] in this test case using the following parameters: $V_T = 1.75V$, $C_e \approx 133nFcm^{-2}$, $T = 300K$, $n_0 = 1.2 \times 10^{16}m^{-2}$ and $R_s^0 = 8.08k\Omega$. The current characteristics depicts that the device is in intrinsic state when $V_{bs} = 50V$. At this value of V_{bs} the device has a zero bandgap. From the surface potential characteristics shown in Fig. 5.3, both φ_{s1} and φ_{s2} equal to zero at the threshold voltage.

Fig. 5.14 shows the transfer characteristics of the drain current plotted against variations in V_{gs} for a set of V_{bs} values from 80V to -120V in steps of 40V. Also, Fig. 5.15 shows the transfer characteristics of the drain current plotted against variations in V_{gs} for a set of V_{bs} values from 60V to -100V in steps of 40V. All experimental measurements of the

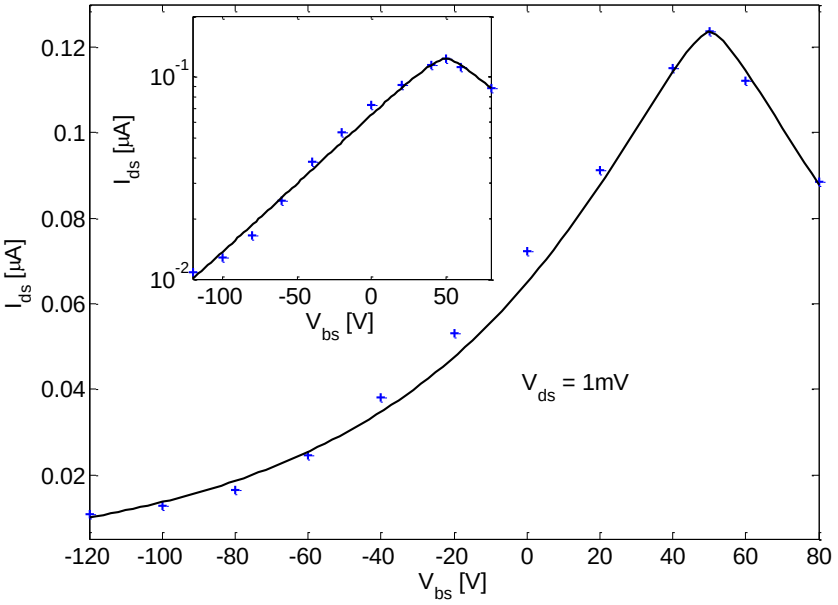


FIGURE 5.13: Validation of the transistor off-current against various back-gate voltages for published experimental data (+) [77] and the proposed model (–) at room temperature. Analysis is carried out at a constant drain voltage, $V_{ds} = 1mV$. Inset: A logarithm plot of the off-current against V_{bs}

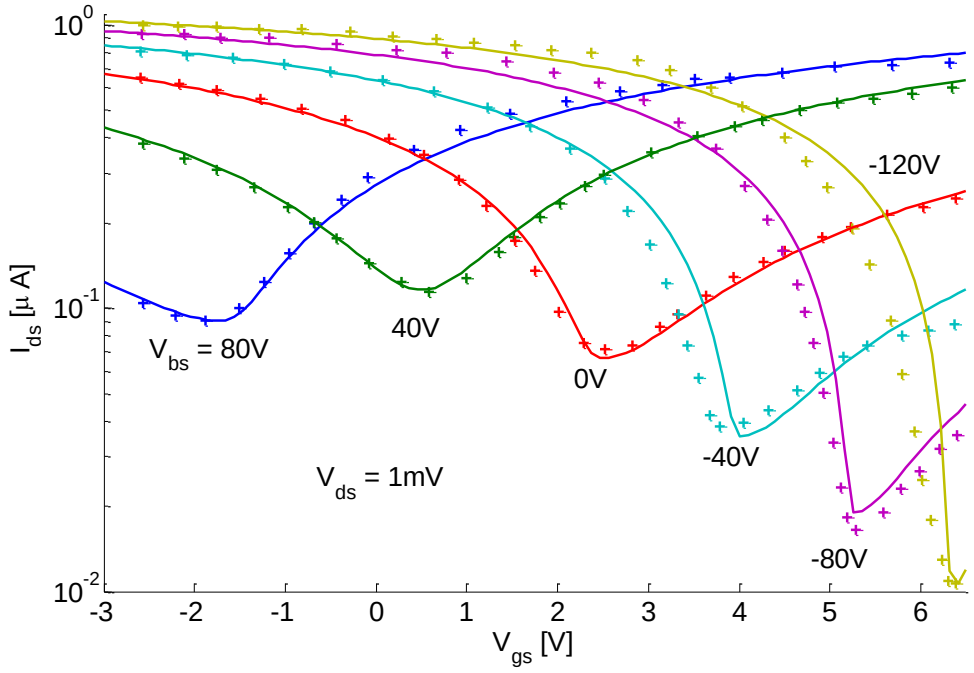


FIGURE 5.14: Transfer characteristics of the transistor drain current against variations in V_{gs} at room temperature. Validation between published experimental data (+) [77] and the proposed model (–). V_{bs} is varied from 80V to -120V in steps of 40V at a constant drain voltage, $V_{ds} = 1mV$

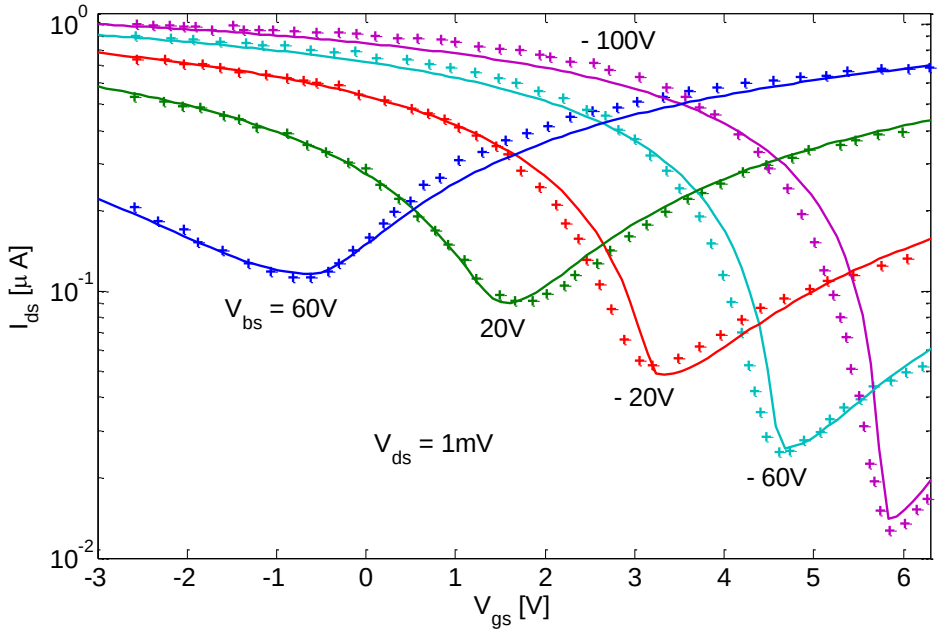


FIGURE 5.15: Transfer characteristics of the transistor drain current against variations in V_{gs} at room temperature. Validation between published experimental data (+) [77] and the proposed model (–). V_{bs} is varied from 60V to -100V in steps of 40V at a constant drain voltage, $V_{ds} = 1mV$

original work [77] were taken at room temperature. Hence, $R_T = 1$ from Eqn. (5.24) because T_{ref} of 300K is assumed for all the analysis carried out in this work.

The model shows a good agreement against experiment. The model accurately captures the minimum conductance. Different carriers mobilities for holes and electrons are used to fit the model to experimental data. Tables 5.3 and 5.4 shows the fitting model parameters.

TABLE 5.3: Experimental data fitting parameters for Fig. 5.14

	hole		electron	
$V_{bs}[V]$	$R_s[\Omega]$	$\mu_h[cm^2/V.s]$	$R_s[\Omega]$	$\mu_e[cm^2/V.s]$
-120	330	5000		
-80	330	4500	300	500
-40	330	4000	300	700
0	330	3200	300	1100
40	330	2500	300	2500
80	330	1100	300	2700

TABLE 5.4: Experimental data fitting parameters for Fig. 5.15

	hole		electron	
$V_{bs}[V]$	$R_s[\Omega]$	$\mu_h[cm^2/V.s]$	$R_s[\Omega]$	$\mu_e[cm^2/V.s]$
-100	330	4800	300	400
-60	330	4300	300	500
-20	330	3700	300	800
20	330	3000	300	1800
60	330	1500	300	2500

Unlike for a dual-gate single-layer graphene transistor where for various V_{bs} values an averagely equal mobility is expected for both the holes and electrons, here the difference in the electron and hole mobilities is attributed to the symmetry of the conduction and valence bands away from the Dirac point. From both Table 5.3 and Table 5.4 a see-saw behaviour is observed for the carrier mobilities. For a V_{bs} of about -80V, the conductance shows a hole mobility far greater than the electron mobility. Also, for a V_{bs} of about 80V the conductance shows a greater electron mobility than a hole mobility. And both electron and hole mobilities more closely equate each other as V_{bs} tends to 50V. With respect to an equal mobility expected in the single-layer, the bilayer transistor at $V_{bs} = 50V$ is in an intrinsic state. In other words, it behaves as though it was a single-layer transistor.

Therefore, it can be assumed that there is a suppression of either the holes or the electrons as the transistor moves away from its intrinsic state. This is presented in Fig. 5.16 showing the suppression of the respective bands. When the transistor is in intrinsic state, the Fermi energy and the intrinsic energy both coincide. Here, both bands are symmetrical as such equal hole and electron mobilities are observed.

Away from the intrinsic state towards $V_{bs} = -120V$, the negative back-gate voltage dopes the transistor with positive charges. As the top-gate modulate the channel carriers from being hole-like to being electron-like, the back-gate induced positive charges favour hole conduction and restrict electron conduction (a p-n-p junction is formed).

The reverse holds away from the intrinsic towards $V_{bs} = 80V$. The action of the back-gate induces negative charges in the transistor making it N-type. Therefore, modulation of the channel by the top-gate results in an n-p-n junction for hole-like carriers and an n-n-n junction for electron-like carriers.

To avoid any confusion, in this work two conventions are used. The first assumes that the action of the top-gate induces and modulates carriers that behave as either holes or electrons. The other, assumes that the back-gate determines if the transistor P-type, N-type or intrinsic.

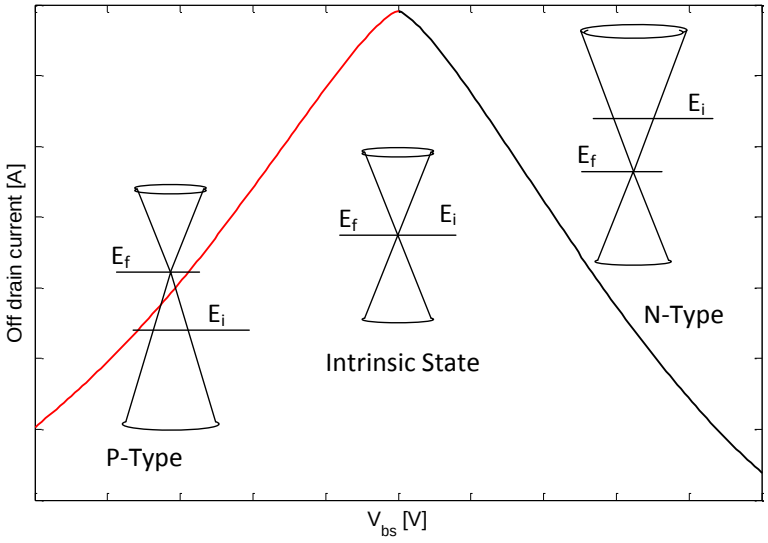


FIGURE 5.16: Representation of the energy levels and the conduction and valence bands symmetry for the characteristics of the off-current against variations in V_{bs}. E_i and E_f are the intrinsic and Fermi energy levels.

5.3.3 Test Case C

In this test case the model is validated against result of a transistor with 15nm thick SiO_2 top-gate dielectric. Table 5.5 shows the model parameters that fit the experimental data.

TABLE 5.5: Model parameters for bilayer graphene FET

Model parameter	Parameter value
Ref	[89]
$L(\mu m)$	8
$W(\mu m)$	1
$t_{ox}(nm)$	15
$t_{il}(nm)$	0.335
ϵ_2	3.9
$V_{gs}^0(V)$	-0.195
$V_{bs}^0(V)$	0
$V_T(V)$	1.1
$H_{sub}(nm)$	285
$R_s^0(k\Omega)$	1.23

As done earlier, by fitting the model to the threshold voltages for a variation of V_{bs}, the top-gate capacitance is obtained. Due to the uncontrolled doping in the fabrication process, there is the possibility of unintentional doping which alters the dielectric constant from the theoretically expected value. For example, C_e of approximately $130nFcm^{-2}$ provides a good agreement for the threshold points. This estimates a dielectric constant of approximately 2.2 compared to the theoretically expected value of 3.9 for SiO_2.

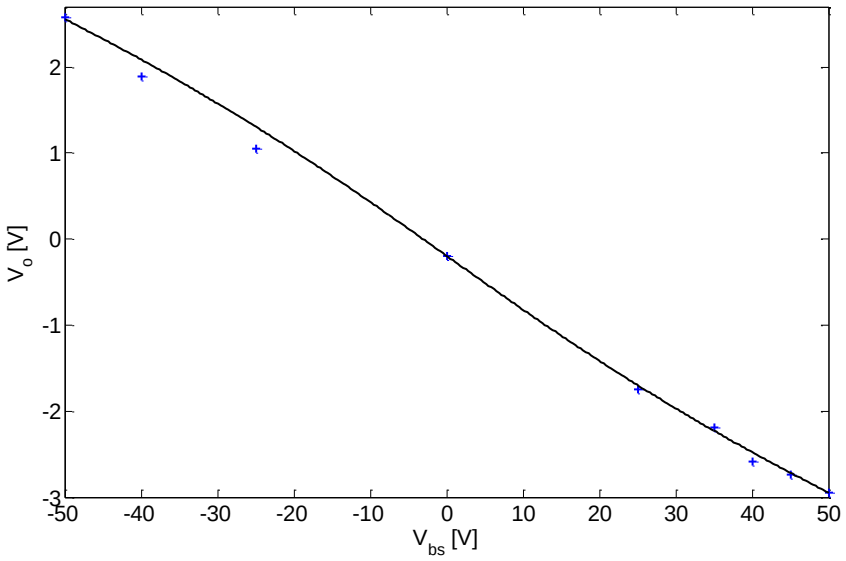


FIGURE 5.17: The threshold voltage, V_o, against V_{bs} for published experimental data (+) [89] and the proposed model (solid line)

In this case, it can seen that a line of best fit will shows a good agreement against extracted threshold voltage points.

In this test case the transistor is measured at various operating temperatures. Fig. 5.18 shows a temperature analysis of the device channel resistance for various electric fields. The proposed model shows a good agreement against experimental data using a reference temperature, $T_{ref} = 300K$, $V_T = 1.05$ and $R_s^0 = 1.23k\Omega$. Eqn. (5.24) is used in modeling the channel's dependence on temperature.

By decreasing the electric field the fitting parameter T_o equally decreases. For the following electric fields, $0.158Vnm^{-2}$, $0.141Vnm^{-2}$, $0.123Vnm^{-2}$ and $0.088Vnm^{-2}$, the following values of T_o, $1.0K$, $0.275K$, $0.066K$ and $0.003K$ gave a good fit. The electric field is calculated using $(V_{bs} - V_o)/(t_{ox} + H_{sub})$ where t_{ox} and H_{sub} are the thickness of the top-gate and back-gate dielectric. Fitting parameters used in Eqn. (5.25) are, $T_\alpha = 6 \times 10^{-7}K$, $\varphi_\alpha = 0.0086V$ and $\eta = 1$.

As the device tends towards its intrinsic state, T_o tends towards zero. Equally, the channel resistance dependence on temperature increases against an increase in the electric field.

Fig. 5.19 shows a validation of the model against experimental results of the channel conductance at threshold voltage against V_{bs}. The validation is done for three operating temperatures, 53K, 4.2K and 0.055K respectively. The model shows a good agreement against measured data for all operating temperatures. Fitting parameters used for the electric field relation to temperature in Eqn. (5.25) are, $T_\alpha = 6 \times 10^{-7}K$ and $\varphi_\alpha = 0.0086V$.

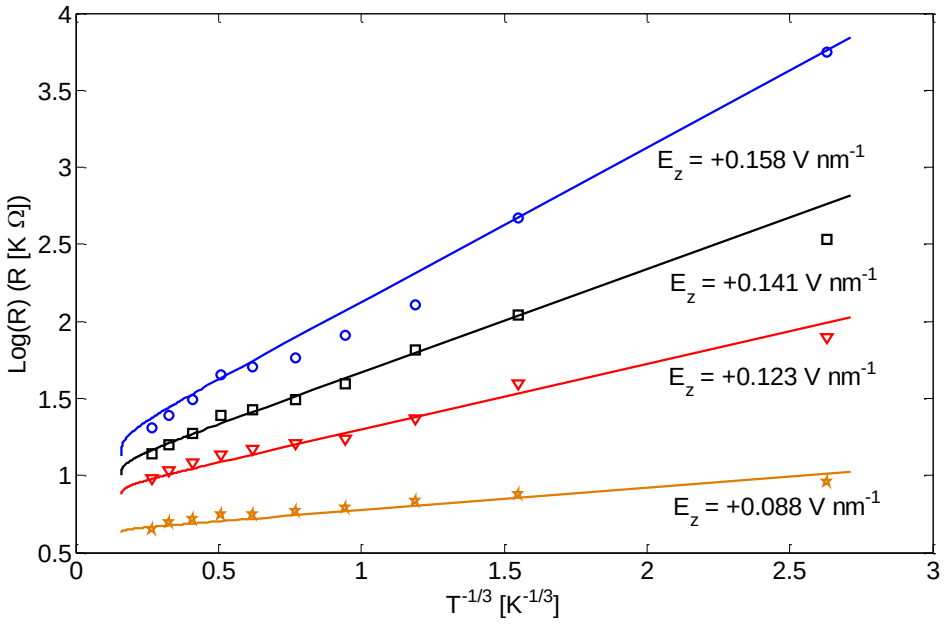


FIGURE 5.18: A logarithm of the peak channel resistance against inverse cube root of the temperature for a range of perpendicular electric fields $((V_{bs}-V_o)/(t_{ox}+H_{sub})$ where t_{ox} and H_{sub} are the thickness of the top-gate and back-gate dielectric). Published experimental data [89] is shown in crosses and the model is shown in a solid line

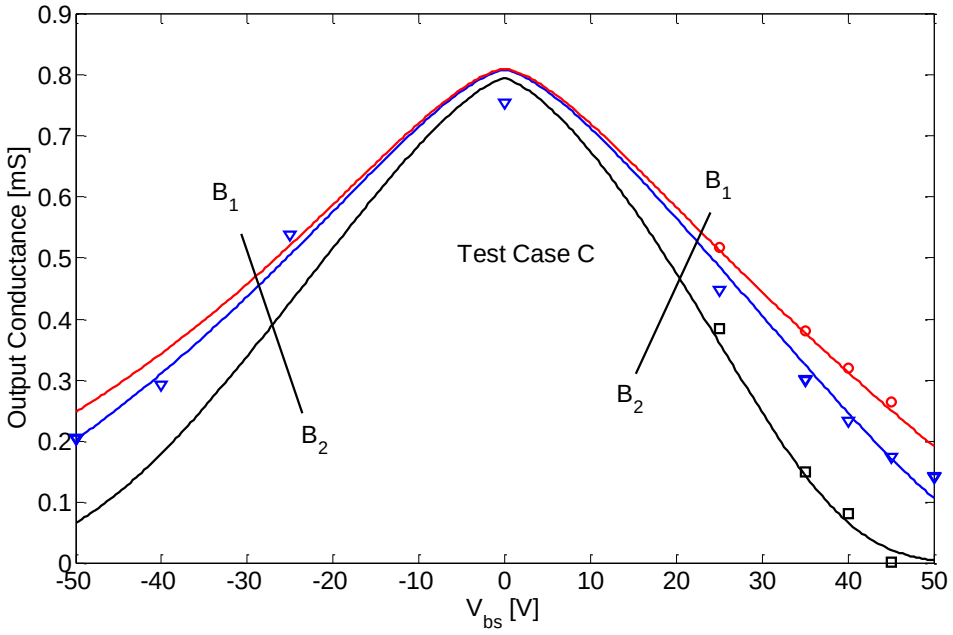


FIGURE 5.19: A plot of the device charge neutrality conductance against V_{bs} for test case C. cross-section B_1 to B_2 (top to bottom) shows the proposed model against experimental data [89] at a temperature of 53K (○), 4.2K (▽) and 0.055K (□)

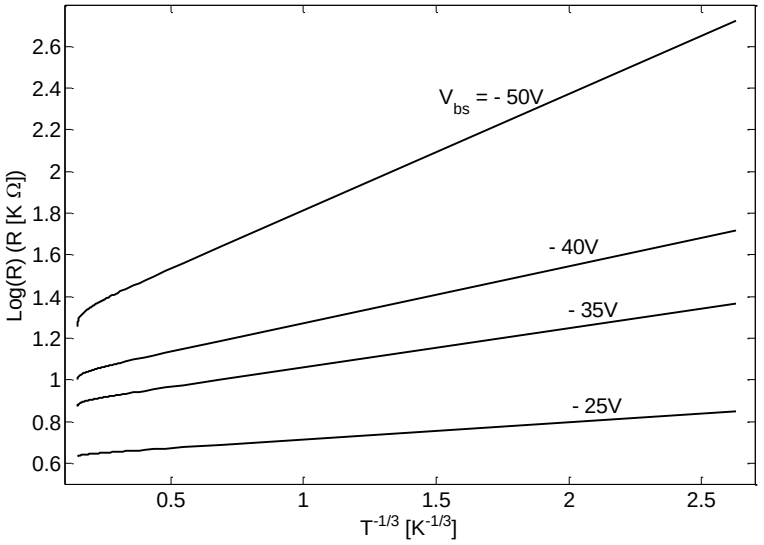


FIGURE 5.20: A logarithm of the maximum channel resistance against inverse cube root of the temperature for various back-gate voltages. Back gate voltages are -50V, -40V, -35V and -25V respectively

For positive values of φ_{s2} at the threshold voltage, $\eta = 1$ gives a good fit, while for negative values of φ_{s2} at the threshold voltage, $\eta = 0.8$ gives a good fit. It is assumed that a negative value of φ_{s2} at the threshold voltage indicates a P-type transistor and a positive value of φ_{s2} at the threshold voltage indicates an N-type transistor.

For the P-type with $\eta = 1$ Fig. 5.20 shows the maximum channel resistance against temperature. At $V_{bs} = -50V$, the transistor is P-type and has an electric field of $-0.175Vnm^{-2}$ which is higher than both $0.141Vnm^{-2}$ and $158nm^{-2}$ of an N-type transistor yet has a lower current ratio $(Log(R_{(T=0.005K)}) - Log(R_{(T=250K)}))$ than either of them. This is due to the difference in η between a P-type and N-type transistor.

In mapping the modeling equation against that of the Schottky barrier general equation, an estimate of the bandgap created is deduced. Fig. 5.21 shows an increasing bandgap by increasing temperature, as well as a bandgap of less than $50meV$ at room temperature, which confirms the dependence of the resistance on the $\exp(T^{-1/3})$ factor.

The rising bandgap against increase in temperature explains why the transistor shows a small current ratio between operating at room temperature and low temperatures. Between $300K$ and $53K$ only a very slight increase in the maximum resistance is observed, especially under low electric field. It is expected that towards $0K$ the device bandgap approaches zero.

It should be understood that graphene is a semi-metal filled with mobile carriers, unlike silicon where carriers are bound in the lattice and are made available by breaking the lattice either through thermal excitations or doping. Thus, by viewing the channel resistance in graphene relative to exponential relationship of the activation energy

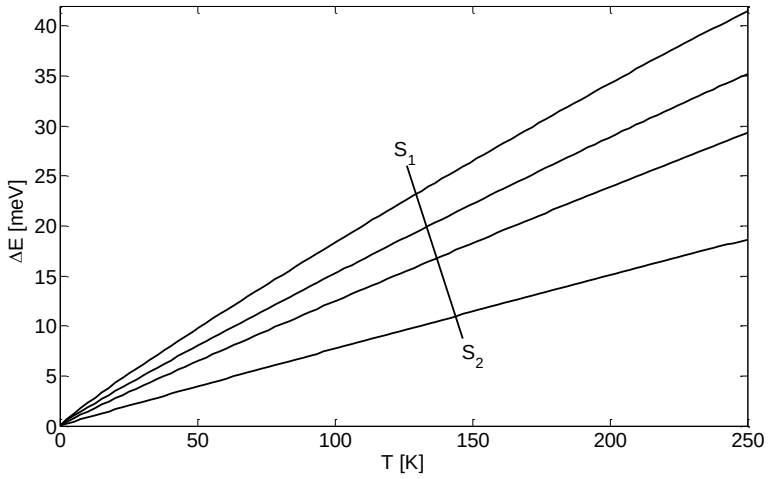


FIGURE 5.21: Estimated energy bandgap created by varying the operating temperature from 0K to 250K at various vertical electric fields. The electric fields are $0.158Vnm^{-2}$, $0.141Vnm^{-2}$, $0.123Vnm^{-2}$ and $0.088Vnm^{-2}$ respectively from top to bottom of cross section S_1 to S_2.

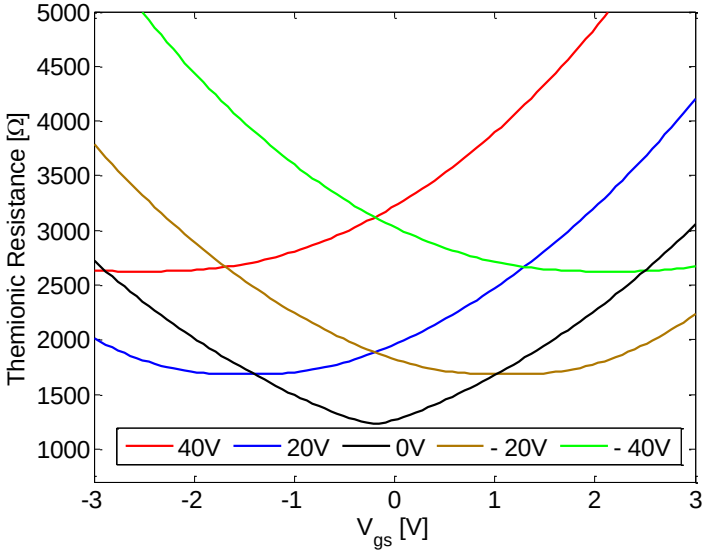


FIGURE 5.22: Transfer characteristic of R_q against V_{gs} at room temperature for V_{bs} from 40V to -40V in steps of 20V

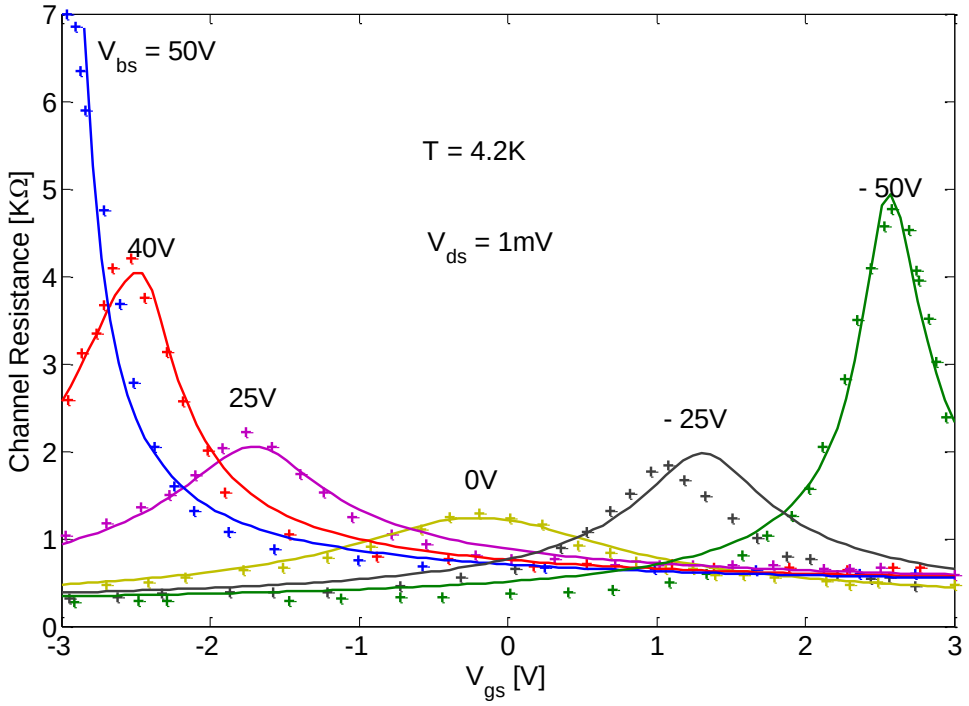


FIGURE 5.23: Transfer characteristics of the transistor output resistance at a temperature of 4.2K against V_{gs}. Validation between published experimental data (+) [89] and the proposed model (–) for V_{bs} of 50V, 40V, 25V, 0V, -25V and -50V respectively and a constant $V_{ds} = 1mV$

given by the Arrhenius equation, the activation energy is shown to be tunable against temperature. This is rightly so, because the carriers can be excited at low temperatures.

The off-current resistance in graphene limits the channel conductance at charge neutrality. In Fig. 5.22, R_q reflects the resistance due to thermal excitations and electric field induced bandgap. R_q shows a dependence on the electric field, with the field yielding a higher resistance and equally a higher ON/OFF current ratio. However, the absence of a bandgap in the intrinsic state of graphene, in a bias of $V_{bs} = 0$, results in a very low minimum resistance of about $1.23k\Omega$. To achieve a high minimum resistance a very large electric field is required. The gate oxide layer may suffer degradation or breakdown before such a resistance is attained. For example, between $0V$ and $40V$ only a difference of $1.5k\Omega$ is attained.

As R_q limits the off-current, the electrostatically doped carrier resistance limits the ON current. Fig. 5.23 shows the output resistance of the channel for a set of V_{bs} values between -50V to 50V. Table 5.6 presents the experimental fitting parameters.

TABLE 5.6: Experimental data fitting parameters for Fig. 5.23

	hole		electron		
$V_{bs}[V]$	$R_s[\Omega]$	$\mu_h[cm^2/V.s]$	$R_s[\Omega]$	$\mu_e[cm^2/V.s]$	η
-50	100	80000	100	60000	.8
-25	100	80000	100	60000	.8
0	100	80000	100	70000	.8
25	100	60000	200	70000	1
40	100	40000	200	70000	1
50			200	70000	1

5.3.4 Test Case D

The original transistor is measured at an operating temperature of 20K. HfO_2 is used as the top-gate dielectric. Table 5.7 shows the model parameters that fit the experimental data.

TABLE 5.7: Model parameters for bilayer graphene FET

Model parameter	Parameter value
Ref	[77]
$L(\mu m)$	1.5
$W(\mu m)$	1.2
$t_{ox}(nm)$	29
$t_{il}(nm)$	0.335
ϵ_1	6.0
ϵ_2	3.9
$V_{gs}^0(V)$	0.3
$V_{bs}^0(V)$	10
$T_\alpha(\mu K)$	.6
$V_T(V)$	0.57
$H_{sub}(nm)$	285
$R_s^0(k\Omega)$	9.5
$n_0(\times 10^{16} m^{-2})$	1

In the fabrication process of the transistor, an atomic layer deposition of HfO_2 is preceded by spin coating of organic seed. Thus, by fitting the threshold voltage point to the model, the actual capacitance of the transistor can be determined. A good agreement against extracted threshold voltage points in Fig. 5.24 is achieved with a dielectric constant of 6.

By inspection, this is another case where the threshold voltage deviates from a best fit line for back-gate voltages away from the intrinsic voltage. At a constant temperature of 20K Fig. 5.25 shows the transfer characteristics of the drain current against V_{bs} for V_{gs} at the respective threshold voltages. In the plot V_{bs} is varied from 0V to 120V. The off-current decreases away from the intrinsic state due to the opening of a tunable bandgap. The transistor fits experiment with $T_\alpha = .6\mu K$, $\varphi_\alpha = 0.017V$ and $\eta = 1$.

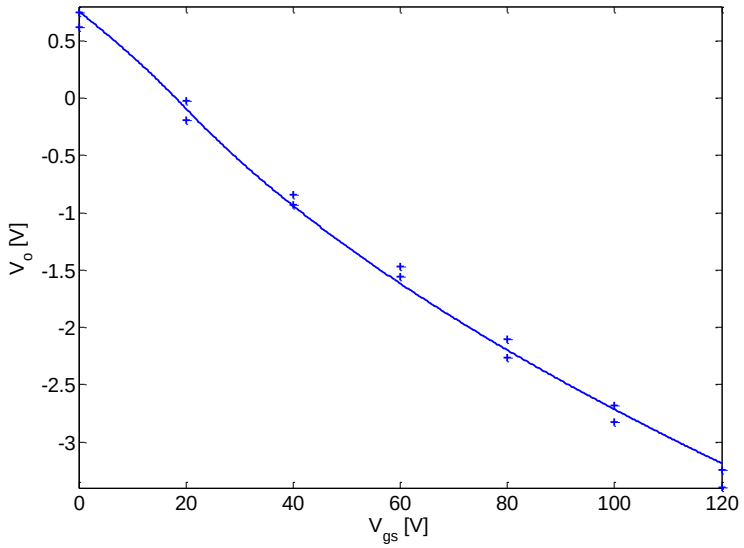


FIGURE 5.24: The threshold voltage, V_o, against V_{bs} for published experimental data (+) [77] and the proposed model (solid line)

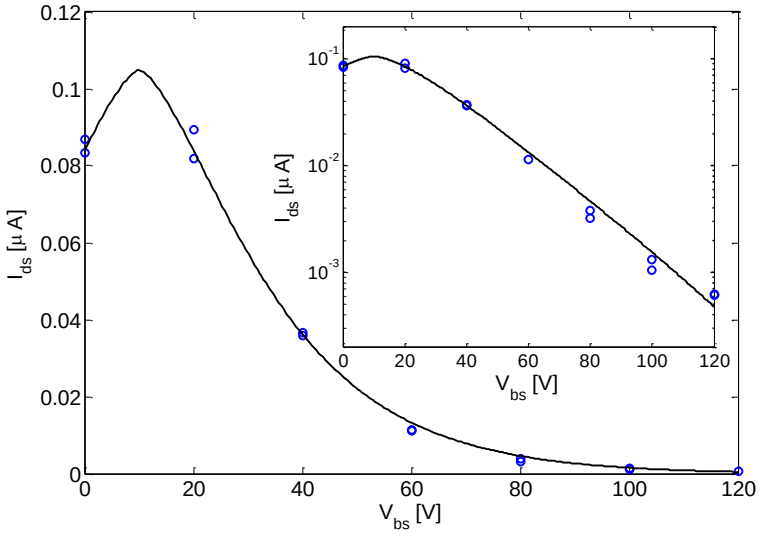


FIGURE 5.25: Transfer characteristics of the minimum drain current at the charge neutrality point against the respective V_{bs} at an operating temperature of 20K. Published experimental data [77] is shown in crosses and the model is shown in solid line. Inset: A logarithmic plot of the minimum drain current with V_{bs}

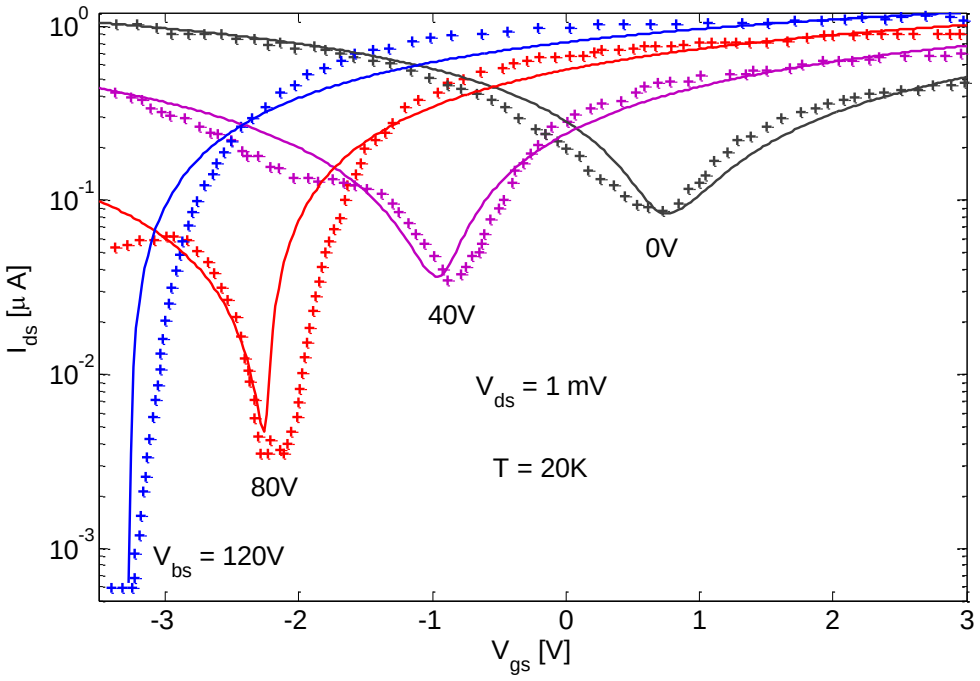


FIGURE 5.26: Transfer characteristics of the transistor drain current against variations in V_{gs} at 20K. Validation between published experimental data (+) [77] and the proposed model (–). V_{bs} is varied by 120V, 80V, 40V and 0V respectively at a constant drain voltage, $V_{ds} = 1mV$

By comparing η here and the transistor in test case C (see section 5.3.3), for the η/φ_α expression, 1/0.0086 and 0.8/0.0086 are required for the P-type and N-type transistor in test case C while in this test case, 1/0.017 fits both the both the P-type state and N-type transistor. It is currently unclear what determines the η/φ_α expression.

TABLE 5.8: Experimental data fitting parameters for Fig. 5.26

	hole		electron		
$V_{bs}[V]$	$R_s[\Omega]$	$\mu_h[cm^2/V.s]$	$R_s[\Omega]$	$\mu_e[cm^2/V.s]$	η
0	200	3000	200	2000	1
40	200	1500	200	2000	1
80	200	600	200	2300	1
120			200	2600	1

TABLE 5.9: Experimental data fitting parameters for Fig. 5.27

	hole		electron		
$V_{bs}[V]$	$R_s[\Omega]$	$\mu_h[cm^2/V.s]$	$R_s[\Omega]$	$\mu_e[cm^2/V.s]$	η
20	200	2500	200	2000	1
60	200	600	200	2000	1
100	200	300	200	2600	1

In modulating V_{gs} for a given V_{bs}, the is channel electrostatically dopes the channel on the opened gap. By the action of V_{gs} for φ_{s1} away from zero, the change in potential energy in Eqn. (5.18) increases. Using carrier fitting parameters in Table 5.8 and Table

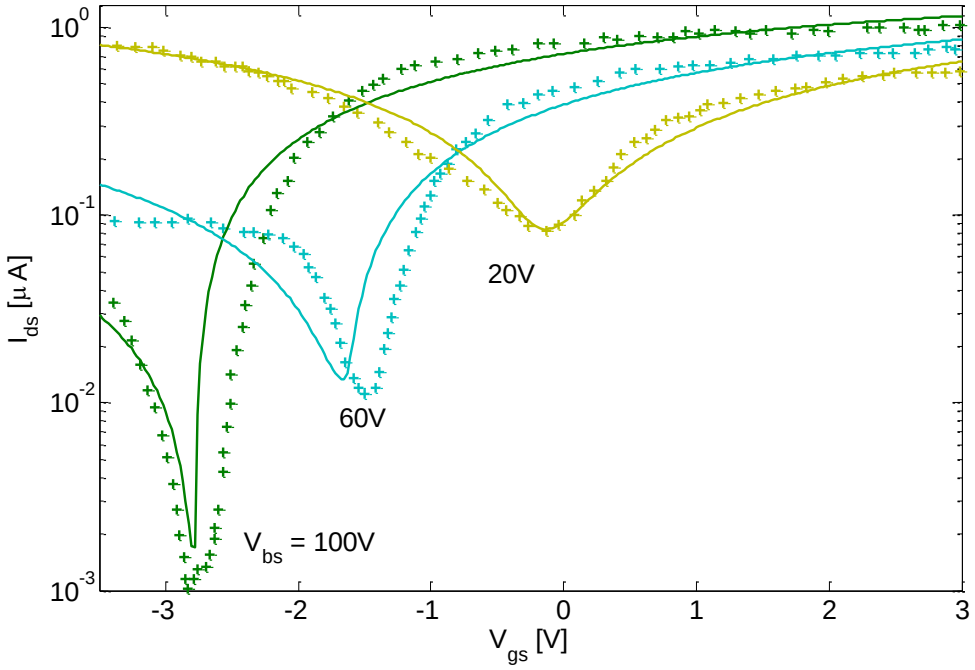


FIGURE 5.27: Transfer characteristics of the transistor drain current against variations in V_{gs} at 20K. Validation between published experimental data (+) [77] and the proposed model (–). V_{bs} is varied by 100V, 60V and 20V respectively at a constant drain voltage, $V_{ds} = 1mV$

5.9, Figs. 5.26 and 5.27 show the drain current transfer characteristics for variations in V_{gs}.

As it is observed in all the earlier test cases, here the mobilities of both carriers show the pattern of having a see-saw behaviour between the hole and electron carriers. The hole mobility increasing from $V_{bs} = 120V$ towards $V_{bs} = 10V$ while the electron mobility decreases. This confirms the assumption of carrier suppression of hole-like conduction in an N-type transistor and electron-like conduction in a P-type transistor.

5.3.5 Test Case E

The multi-layer graphene is composed of stacks of graphene sheets held together by Van der Waal forces. C_o, is the interlayer capacitance. It is assumed that all layers are equally spaced with an interlayer spacing, t_{il}, of $0.355nm$. The capacitance model for a four-layer graphene channel is shown in Fig. 5.4.

TABLE 5.10: Model parameters for four-layer graphene FET for Fig. 5.30

Model parameter	Parameter value
Ref	[127]
$L(\mu m)$	10
$W(\mu m)$	5
$t_{ox}(nm)$	40
$t_{il}(nm)$	0.355
k_1	17.0
k_2	3.9
$V_{gs}^0(V)$	0.75
$V_{bs}^0(V)$	0
$H_{sub}(nm)$	500
$R_s^0(k\Omega)$	3.7

In a similar way the bilayer transistors were analysed in the earlier sections, the threshold model is derived from the equivalent circuit. In this work the dielectric constants are confirmed through the threshold modelling. Because in the original work [127], the various threshold voltage points were not available, and the theoretical estimation of the HfO_2 [160] has not been currently measured in a graphene transistor, a dielectric constant of 17 is assumed [161]. This dielectric constant is in the range of a published dielectric of HfO_2 on graphene [33]. Using the model parameters in Table. 5.10, the threshold voltage point is shown in Fig. 5.28.

From Table 5.10 the back-gate Dirac point voltage is assumed to be $0V$. For a DC sweep of the top-gate voltage Fig. 5.5 shows the surface potential of each of the four-layers. At the Dirac point the electric field is taken to be zero and there is no bandgap opening. This is why the characteristics of the surface potential of each layer meet at 0V.

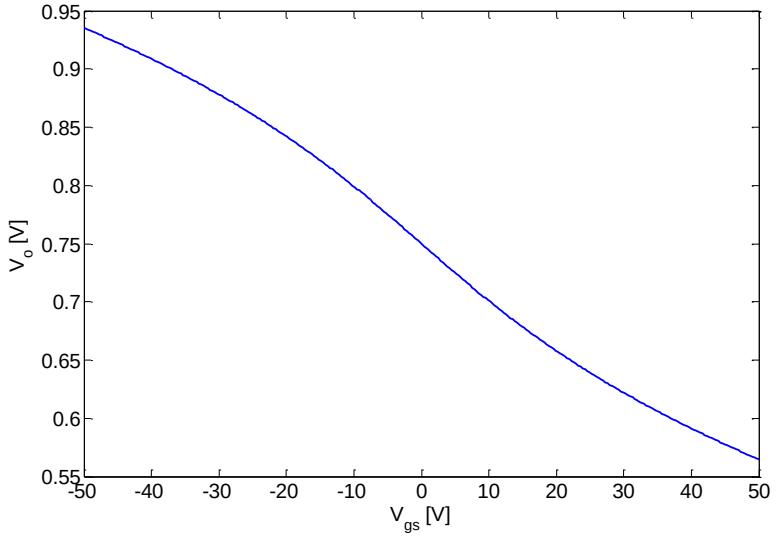


FIGURE 5.28: The threshold voltage, V_o, against V_{bs}

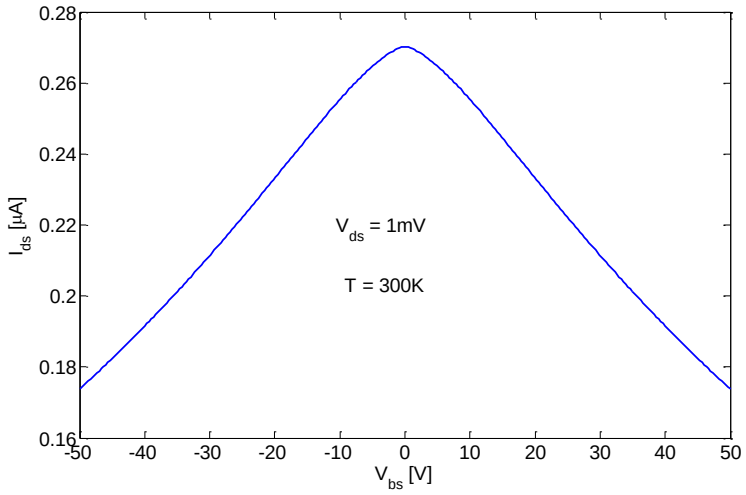


FIGURE 5.29: Transfer characteristics of the minimum drain current at the charge neutrality point against the respective V_{bs} at an room temperature.

By plotting the drain current against V_{bs} for V_{gs} at the various threshold voltages, it is can be observed that the current peaks at the Dirac point. Fig. 5.29 shows the plot of the drain current against V_{gs} at room temperature for $V_{ds} = 1mV$.

Fig. 5.30 shows the variation of the drain current against changes in the drain voltage. The model is validated against experimental data [127] for $V_{bs} = 0V$ and V_{gs} of -1.25V, -0.75V, -0.25V , 0.25V and 0.75V respectively. The model parameters are shown in Table 5.10. A good fit against the experimental results is achieved using the following fitting parameters, $n_0 = 0.5 \times 10^{16} m^{-2}$, $V_T = 3.0V$, $C_e \approx 376nFcm^{-2}$, $R_c = 390\Omega$, $E_c = 15kV/cm$, hole carrier mobility $\mu = 13,000cm^2/V.s$ and alternate carrier mobility $\mu_n = 2900cm^2/V.s$.

Comparing the gate bias of $V_{gs} = 0.25V$ and $V_{gs} = -0.75V$, $V_{gs} = 0.75V$ the transistor shows only one region which is the ambipolar saturation region. This is because the transistor is biased at its CNP resulting in a both unipolar saturation boundary voltages being 0V.

Fig. 5.31 shows the variation of the drain current against changes in the top-gate for $V_{ds} = 0.1V$. The model gives the best fit against experimental data [127] using the following fitting parameters; $R_c = 290\Omega$ and $\mu = 7000cm^2/V.s$ for hole conduction and $R_c = 200\Omega$ and $\mu = 3200cm^2/V.s$ for electron conduction.

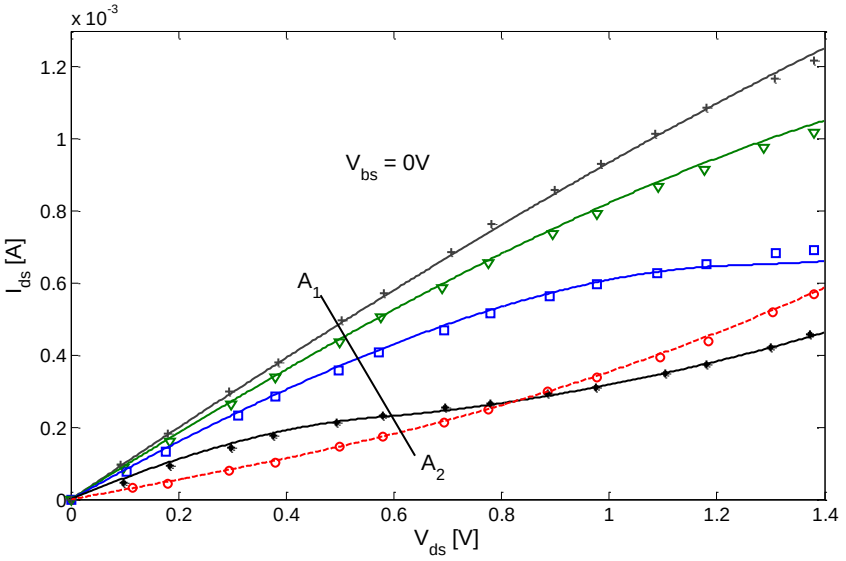


FIGURE 5.30: Experimental data (+) [127] and the proposed model (–) for negative I_{ds} vs negative V_{ds} characteristics at V_{bs}= 0V. V_{ds} is varied from 0 to -1.4V for top-gate voltages of -1.25V, -0.75V, -0.25V , 0.25V and 0.75V (from top to bottom between cross-section A_1 and A_2)

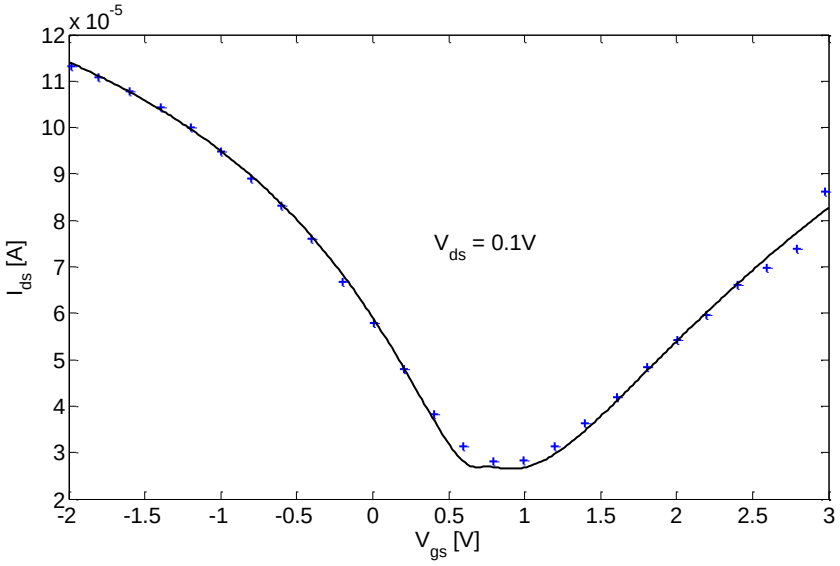


FIGURE 5.31: Characteristics of the channel Drain current against the top-gate voltage for $V_{ds} = 0.1V$(Experimental data(+) [127], proposed model(–))

5.4 Summary

In this chapter a circuit-level model that describes a dual-gate multi-layered graphene transistor is presented. The model has been validated against published experimental data [77, 33, 127, 89] for both a bilayer and a four-layered graphene transistor and shows a good agreement. The validation against experimental data was done for the channel output conductance, the drain current characteristics for changes in the drain voltage, the device off-current for a range of back-gate voltages and the dependence of the channel conductance on temperature.

In the presented model, surface potentials of all the layers are calculated for both the bilayer and four-layer transistor. Each layer is represented by a quantum capacitance that is a function of its surface potential.

Equally, the model uses the presented equivalent circuit in calculating the threshold voltage. The model shows a good agreement for extracted experimental data of the threshold voltage for a range of V_{bs}. It is observed that although linear function of V_{bs} against the threshold voltages provides a quick method of evaluating the threshold voltage, it may be insufficient in some cases. The method presented here proves to be accurate for all the cases validated. Using the threshold model, the top-gate capacitance is also calculated as it is the only parameter used to fit the model against experiment. The use of organic seeds prior to deposition of oxide layer in current fabrication techniques can lead to a top-gate capacitance being smaller than the expected theoretical value. Therefore, this technique proves a suitable way of validating the top-gate capacitance.

Also, the presented model implements the transistor as having a channel resistance which is determined by the both the electrostatically induced carries and an off-current resistance. The off-current resistance limits the channel resistance and determines the device off-current. The model estimated off-current shows a very good agreement against experimental data [77, 89].

At a constant temperature, the channel resistance shows a exponential relationship against the surface potential by varying the perpendicular electric field. This has been demonstrated to consistent for both the bilayer and the four layer channel.

For a constant electric field and a varying the operating temperature, the surface potential equally determines how sensitive the channel resistance is to changes in temperature.

Using the Schottky barrier general equation, the presented model estimates the amount of bandgap opening for a given back-gate voltage. The results agree with known theory of a bandgap opening by the presence of a perpendicular electric field. Also the model reveals an increase in the bandgap by increasing the operating temperature, resulting in a zero bandgap 0K.

Chapter 6

CAD Tool Design and Transistor Optimization

Computer based circuit simulations are widely used by designers and students as a valuable tool to validate a design and learn the behaviour of a component or system without fabricating a physical circuit. As such with simulation, parameters of circuit elements can be quickly changed which is often difficult or challenging to do in a physical circuit.

Historically, circuit simulators have been tailored to support either analog or digital simulation algorithms. An analog simulator models circuit response by iteratively calculating Kirchhoff's law over steps of an independent parameter which may be time in the case of a transient analysis. Here, the behaviour of a circuit design is calculated by the convergence of the numerical approximations to a stable value. On the other hand, in a digital simulator, solutions to Kirchhoff's law is not required as the simulator must predict if a logic state is high or low.

In developing graphene FET libraries for use in CAD tools, this work focuses on an analog simulator type model because fabricated graphene transistors are not currently well suited for digital applications and the analog simulator can be extended to a digital simulator by applying voltage levels to a logic high and a logic low. The only downside to using an analog simulator as a substitute to digital one is the longer simulation time.

6.1 CAD Tool Development

Computer aided design tools play a major role in the creation, analysis and optimization of designs. This has become a necessary tool to explore how an intended design will behave when fabricated. There are currently a number of CAD tools targeted toward electronic development automations. The commercial tools used in this project include

HSPICE by Synopsis [141] and VHDL-AMS by Mentor [142]. Berkeley SPICE [145] is the only open source simulator used in this project. The choice of these CAD tools is only a matter of personal preference. This project has a resource website [43] where all CAD tools developed are posted. In this project, library files for three simulators have been developed.

Both the HSPICE and the VHDL-AMS are commercial tools in which only a behavioural model can be implemented. The behaviour model implementation is itself restrictive. As such, iterations required to calculate the surface potential are very challenging or impossible, because these tools do not support loop statements. Therefore, the behavioural models presented are limited to the use of fixed quantum capacitances and implementation of a general model which is better suited to a single-layer graphene FET.

6.2 HSPICE Project Library Development

HSPICE simulator has two main limitations. One is that it does not allow the logical "if" command in sub-circuit descriptions which makes developing a behavioural model difficult to troubleshoot and difficult to read. The other is that it does not support "for" loops which makes numerical analysis challenging or even impossible.

6.2.1 Structure of the graphene FET library

Two files have been developed in the behavioural model which are param.lib and gfet.lib. Listing. B.1 and Listing. B.2 shows the code of the files created for both the param.lib and gfet.lib. The param.lib contains the fixed device parameters definition. The gfet.lib contain the mathematical expression that govern the device physics of the graphene transistor. Their interaction with a testbench file can be seen in Fig. 6.1.

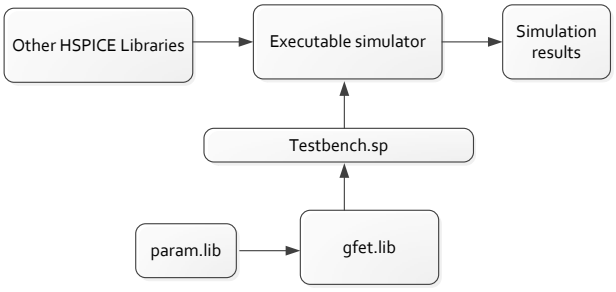


FIGURE 6.1: Interaction between the behavioural model and the simulator

In making the behavioural model, gfet.lib library has the transistor instances declared as a sub-circuit. A sub-circuit is a SPICE circuit element that has a user specified number of nodes which can be connected in the main circuit.

In the testbench file, the gfet.lib file has to be included. This allows the testbench to call the transistors instance. Using the device instance declaration beginning with the letter "X", the HSPICE simulator knows that a sub-circuit is being referred to [141]. The working bilayer transistor model with a testbench can be downloaded from the project transistor resource [43].

6.2.2 Simulating with the HSPICE graphene library

TABLE 6.1: HSPICE Model parameters for bilayer graphene FET

HSPICE symbol	Parameter Name	Parameter Value [33]
Hsub	Back-gate dielectric thickness	285×10^{-9}
tox	Top-gate dielectric thickness	15×10^{-9}
L	Channel length	1×10^{-6}
W	Channel width	2.1×10^{-6}
Cgio	Top-gate capacitance factor	0.8072
Ec	Critical electric field	
Rs	Series resistance	
mu	Carrier mobility	
ntop	Charge density	2.1209×10^{16}
Vgs0	Gate voltage at Dirac point	1.45
Vbs0	Back-gate voltage at Dirac point	2.7
k_sub	Back-gate dielectric constant	3.9
k	Top-gate dielectric constant	16

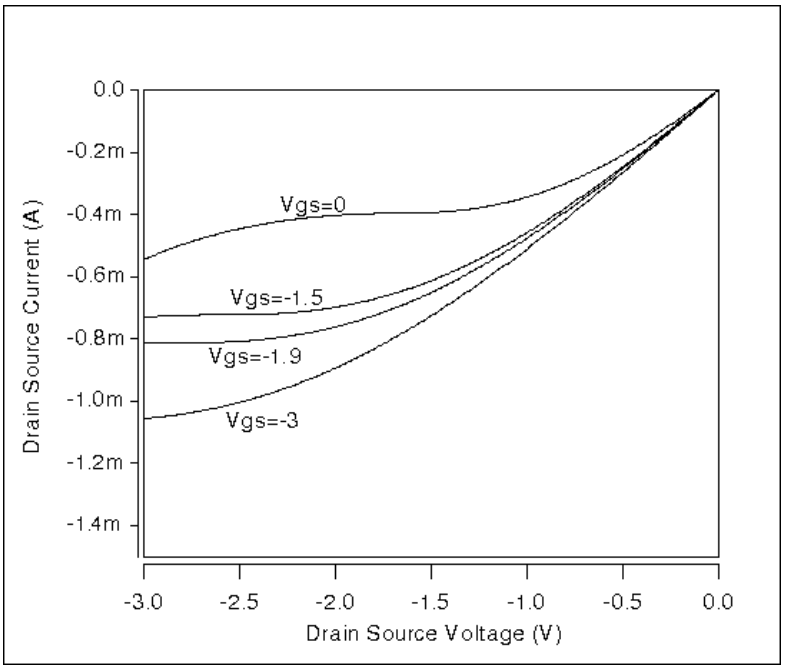


FIGURE 6.2: An HSPICE plot of the drain current I_{ds} as a function of the drain voltage V_{ds} for a back-gate voltge $V_{bs} = -40V$ for the top-gate voltages 0V, -1.5V, -1.9V and -3V respectively

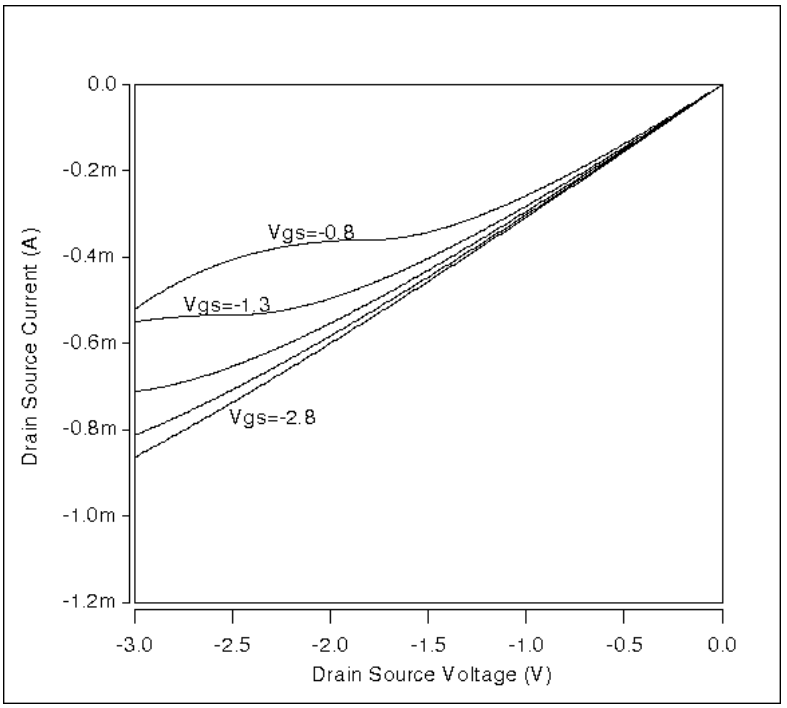


FIGURE 6.3: An HSPICE plot of the drain current I_{ds} as a function of the drain voltage V_{ds} for a back-gate voltge $V_{bs} = +40V$ for the top-gate voltages -0.8V, -1.3V, -1.8V, -2.3V and -2.8V respectively

Table 6.1 shows the HSPICE symbols and the description of the symbols. The I-V characteristics of the behavioural model is plotted for two test cases using parameters of a fabricated transistor [33], where $V_{bs} = -40V$ and $V_{bs} = 40V$.

For the case $V_{bs} = -40V$, HSPICE model parameters of $mu = 700$, $Rs = 800$ and and $Ec = 4.5 \times 10^5$) are taken. Fig. 6.2 shows the HSPICE modelling of the I-V characteristics for a sweep of V_{ds} is from 0V to -3V at the following V_{gs}: 0, -1.5, -1.9 and -3V.

Also, for test case $V_{bs} = +40V$, HSPICE model parameters of $mu = 1200$, $Rs = 1500$ and and $Ec = 15 \times 10^5$) are taken. Fig. 6.3 shows the result of the HSPICE model. The I-V characteristics are plotted for a drain voltage from 0 to -3V and a top-gate voltage of -0.8V, -1.3V, -1.8V, -2.3V and -2.8V respectively. The testbench listing is shown in Listing. 6.1.

```
.TITLE 'IV Characteristics for GFET Transistor'

.options POST
.options AUTOSTOP
.options INGOLD=2     DCON=1
*.options GSHUNT=1e-20 RMIN=1e-20
.options ABSTOL=1e-5  ABSVDC=1e-4
.options RELTOL=1e-2  RELVDC=1e-2
.options NUMDGT=4     PIVOT=13
.param   TEMP=27
.lib 'gfet.lib' gfet
```

```
*Beginning of circuit and device definitions
*Supplies and voltage params:
.param Supply=-3
.param Vg=-3
.param Vd='Supply'
.param Vb=40

*Overide GFET parameters
.param W_bg =285e-9 $Width from back-gate to Channel
.param W_tg =15e-9  $Width from top-gate to Channel
.param L_g =1e-6 $Length of top-gate
.param CH_Wdt =2.1e-6 $Channel layer width
.param impurity_coef = 0.8072

* Define power supply
Vdd     Drain   Gnd     Vd
Vss     Source  Gnd     0
Vgg     Gate    Gnd     Vg
Vsub    Sub     Gnd     Vb

* Main Circuits
* pFET
XFET1 Drain Gate Source Sub pGFET  Hsub=W_bg  tox=W_tg  L=L_g
W=CH_Wdt Cgio=impurity_coef Ec=15e5 Rs=1500 mu=1200e-4

* Measurements
* test gFETs, Ids vs. Vgs
.DC      Vdd   START='0'  STOP='-3'   STEP='-.01'
Vgg POI 5 -0.8 -1.3 -1.8 -2.3 -2.8
.print I(Vdd)
.end
```

LISTING 6.1: Testbench of the HSPICE graphene library in file gfetmodel.sp

6.3 VHDL-AMS Project Library Development

Like HSPICE, VHDL-AMS is commercial software. Unlike HSPICE, VHDL-AMS allows the use of the logical-if statment. This project is carried out using the SystemVision simulator [143]. The VHDL-AMS simulator builds on the VHDL one by providing a mechanism for analogue and mixed signal behaviour specification.

6.3.1 Structure of the VHDL-AMS Project Library

For DC analysis of the behavioural model, four files have been created. Fig. 6.4 shows how the library files communicated in the whole design. Two of the files, gfetmodel.vhd (see Listing. B.5) and gTransistor.vhd (see Listing. B.6), contain expressions that govern the behaviour of the bilayer transistor. A function in gfetmodel.vhd calculates the drain current characteristics of the transistor. The gTransistor.vhd library file is a top-level model that connects the gfetmodel.vhd to external voltage or current sources.

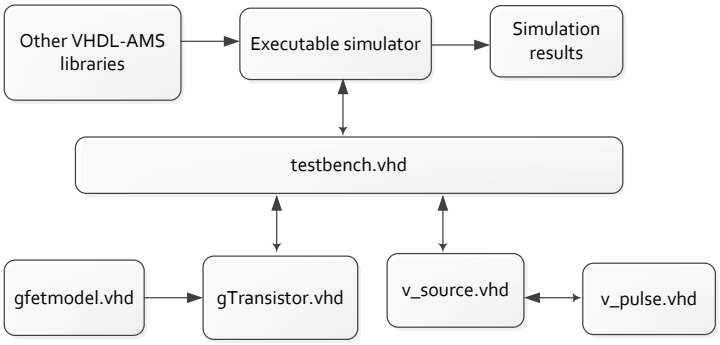


FIGURE 6.4: Layout of the interactions of the VHDL-AMS files used in the behavioural model

Mentor Systemvision simulator has a fundamental limitation that it cannot carry out a DC sweep of a voltage source connect to a node. Therefore, as a work-around this limitation, two library files have been created, v_pulse.vhd (see Listing. B.3) and v_source.vhd (see Listing. B.4) respectively. Both library files implement a time dependent voltage ramp which is used to run dc analysis of the transistor's behavioural model.

The complete model of the implementation of the behavioural model in VHDL-AMS is available in the project transistor resource [43]. The resource contains all the library files as well as the top-level testbench script.

6.3.2 Simulating with the VHDL-AMS graphene library

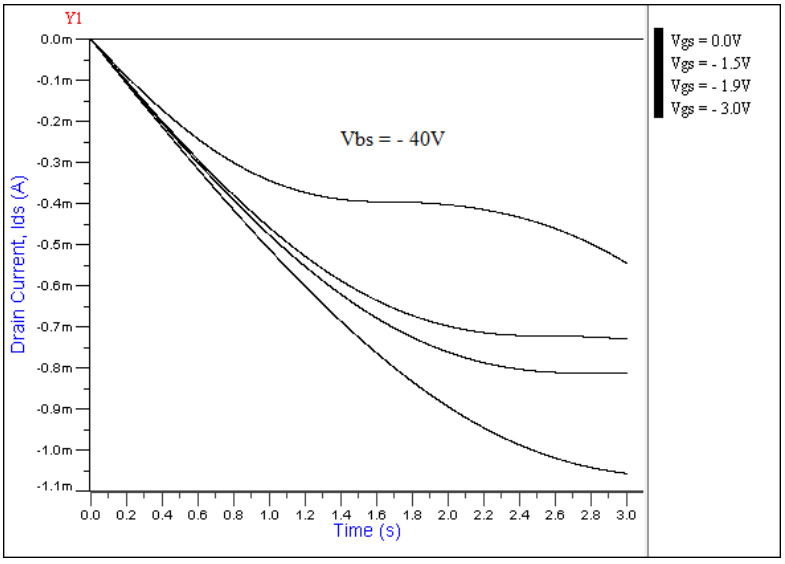


FIGURE 6.5: A VHDL-AMS plot of the drain current I_{ds} as a function of the time for a back-gate voltge $V_{bs} = -40V$ for the top-gate voltages 0V, -1.5V, -1.9V and -3V respectively (from top to bottom).

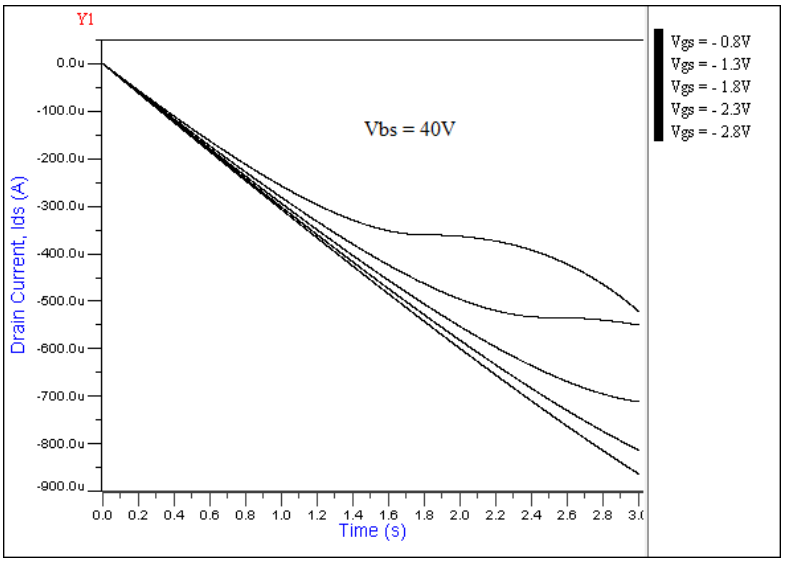


FIGURE 6.6: A VHDL-AMS plot of the drain current I_{ds} as a function of the drain voltage V_{ds} for a back-gate voltge $V_{bs} = +40V$ for the top-gate voltages -0.8V, -1.3V, -1.8V, -2.3V and -2.8V respectively (from top to bottom).

Table 6.1 shows the VHDL-AMS symbols and the description of the symbols. The I-V characteristics of the behavioural model is plotted for two test cases of an originally fabricated transistor [33], where $V_{bs} = -40V$ and $V_{bs} = 40V$.

For the case $V_{bs} = -40V$, VHDL-AMS model parameters of $mu = 700$, $Rs = 800$ and and $Ec = 4.5 \times 10^5$) are taken. Fig. 6.5 shows the I-V characteristics for a sweep of V_{ds} is from 0V to -3V at the following V_{gs}: 0, -1.5, -1.9 and -3V.

Also, for test case $V_{bs} = +40V$, VHDL-AMS model parameters of $mu = 1200$, $Rs = 1500$ and and $Ec = 15 \times 10^5$) are taken. Fig. 6.6 shows the I-V characteristics are plotted for a drain voltage from 0 to -3V and a top-gate voltage of -0.8V, -1.3V, -1.8V, -2.3V and -2.8V respectively. The testbench listing is shown in Listing. 6.1.

When implemented in VHDL-AMS the current characteristics shows a transient analysis of the drain current. To create a dc sweep of the drain voltage a negative ramp voltage source is applied to the drain. For convenience a slope of -1V/s is used. This is the slope that will be used throughout the simulation with VHDL-AMS. This allows the use of the transcient analysis in VHDL-AMS to carry out a dc sweep analysis over the voltage range (V_{ds} varied from 0V to -3V in this case). Separate transistor instances are used for each value of the top-gate voltage being considered. The testbench architecture of the test circuit is shown in Listing. 6.2.

```
--Testbench
library IEEE;
use IEEE.math_real.all;
use IEEE.electrical_systems.all;

entity test_gTransistor is
end entity test_gTransistor;
```

```
architecture test of test_gTransistor is
  terminal Vd, Vg0_0,Vg1_5,Vg1_9,Vg3_0, Vb: electrical;
  alias ground is ELECTRICAL_REF;
begin
  vb_dc: entity v_source generic map (VDC=>-40.0)
         port map (V_term=>Vb, V_ref=>ground);
  vi: entity v_pulse generic map (pulse=>-3.0,
      tchange=>3sec) port map(po=>Vd,ne=>ground);
-- for Vgs = 0.0
vg_dc0_8: entity v_source generic map (VDC=>0.0)
          port map (V_term=>Vg0_0, V_ref=>ground);
transistor1: entity gTransistor generic map (Cgio=> 0.8072)
port map (drain=>Vd, gate=>Vg0_0, back_gate=>Vb,
source=>ground);
-- for Vgs = -1.5
vg_dc1_5: entity v_source generic map (VDC=>-1.5)
          port map (V_term=>Vg1_5, V_ref=>ground);
transistor2: entity gTransistor generic map (Cgio=> 0.8072)
port map (drain=>Vd, gate=>Vg1_5, back_gate=>Vb,
source=>ground);
-- for Vgs = -1.9
vg_dc1_9: entity v_source generic map (VDC=>-1.9)
          port map (V_term=>Vg1_9, V_ref=>ground);
transistor3: entity gTransistor generic map (Cgio=> 0.8072)
port map (drain=>Vd, gate=>Vg1_9, back_gate=>Vb,
source=>ground);
-- for Vgs = -3.0
vg_dc3_0: entity v_source generic map (VDC=>-3.0)
          port map (V_term=>Vg3_0, V_ref=>ground);
transistor4: entity gTransistor generic map (Cgio=> 0.8072)
port map (drain=>Vd, gate=>Vg3_0, back_gate=>Vb,
source=>ground);
end architecture test;
```

Listing 6.2: Testbench of the VHDL-AMS test circuit

6.4 Berkeley SPICE Project Library Development

Berkeley SPICE offers the advantage over HSPICE and VHDL-AMS by being an open source simulator. Therefore, a circuit-level model can be developed as compared to a behavioural model. Berkeley SPICE is written in C/C++ programming language, so the numerical analysis required in the transistor modelling can be implemented. In Fig. 6.7, the model libraries are integrated into the simulator, with the testbench telling the simulator to invoke the respective models.

6.4.1 Important Files to be updated

The developed library GNT is derived from the existing MOSFET template. This allows the developed library to be invoked in the same way MOSFETs are invoked in SPICE.

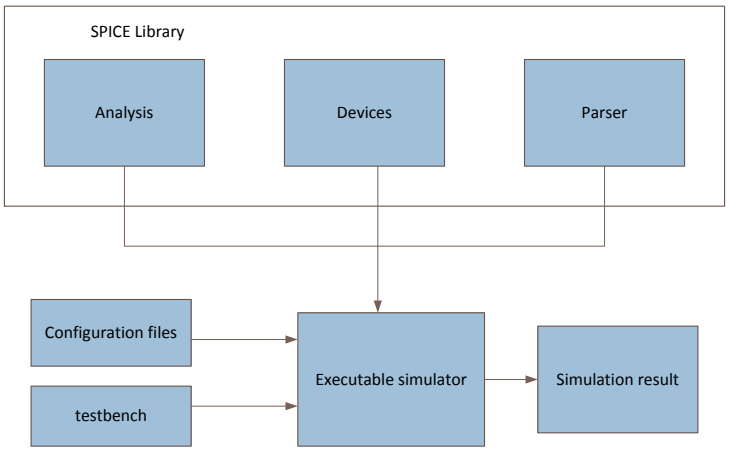


FIGURE 6.7: Layout of the interactions of the Berkeley SPICE files used in the model

Fig. 6.8 shows the important files that form the structure of the fully working model and the locations for these files.

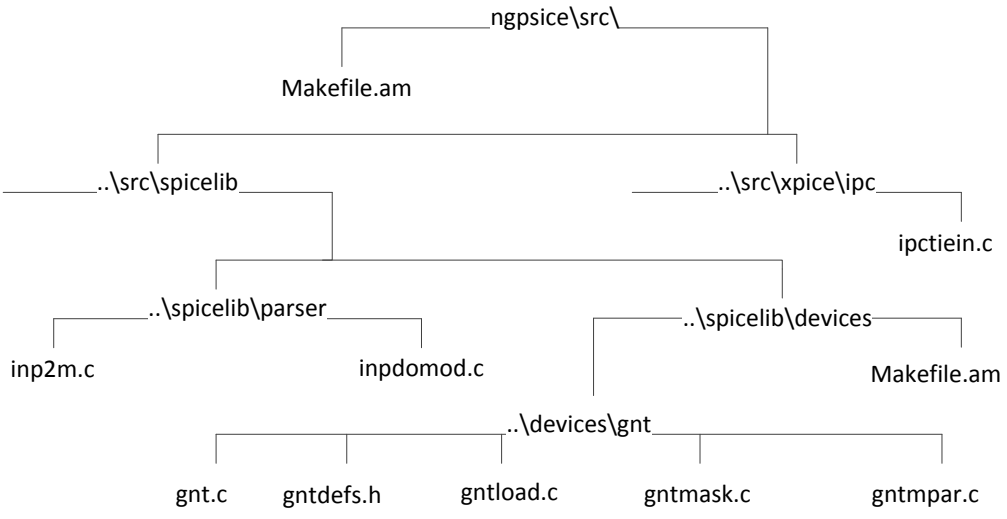


FIGURE 6.8: A tree of the Berkeley SPICE files updated in the project

File named Makefile.am tells the compiler of all the library files to compile. Update to this file is done to enable the compiler develop the respective object files.

Three files; ipctiein.c, inp2m.c and inpdomod.c tells the simulator that a command invoked in the testbench is directed towards the gnt model. The simulator will in turn make the required function call to the gnt model and transfer any model parameters to the model.

The following are files that describe the graphene FET, gnt.c gntload.c, gntdefs.h, gntmpar.c and gntmask.c. The gnt.c is a table that assigns all the model parameters of the

transistor. The model parameters are defined in the file gntdefs.h. The file gntmpar.c, sets the required flag for user defined parameters and updates the respective parameter with the user defined values. The gntmask.c file assigns the model parameter with the default value in the event that a user defined value is not available. The gntload.c file contains the mathematical expression that determine the device physics of the model.

6.4.2 Installing the simulator

The version of Berkeley SPICE simulator used is the ngspice. Ngspice is a direct derivative of spice3f5 from UC Berkeley. An executable Berkeley SPICE simulator can be generated on both the Linux and Windows platform. In the Linux system, the following commands are run to generate an executable file:

./autogen.sh

./configure

make

make install

Administrative privileges are required in generating the executable file. The command 'sudo' is used before every to assume administrator rights. The simulator executable file is named ngspice.

Installing in the Windows platform, in the visualc folder MS Visual C++ files vngspice.sln (project starter) and vngspice.vcproj (project contents) allow to compile and link ngspice with MS Visual Studio 2008 or later. An executable file is created by running the build solution command. The created executable file is named vngspice.exe. Also, applications that allow the running of native Linux commands on Windows, such as Cygwin, can be used to generate a Windows compatible executable file. Here, the installation commands used on the Linux platform apply. The resulting generated executable file will be name ngspice.exe.

6.4.3 Running the SPICE simulator

This work uses the .sp extension for SPICE scripts files, although any naming of the input script file and the output log file is acceptable by the simulator. In the Linux and Linux related platforms (i.e Cygwin) executing a SPICE script takes the form

ngspice [-b] [-o logfile] [SPICE script]

In the Windows case, the command ngspice is replace with vngspice. The $-b$ argument allows the simulator to run in batch mode and the $-o$ argument tells the simulator where to save the output prints or plots.

Table 6.2 shows the various command line options that can be used with the ngspice simulator.

TABLE 6.2: Command Line option for ngspice [145]

Option	Long option	Meaning
-		Don't try to load the default data file "rawspice.raw") if no other files are given (ngnutmeg only).
-n	no-spiceinit	Dont try to source the file ".spiceinit" upon start-up
-t TERM	terminal=TERM	The program is being run on a terminal with mfb name term (obsolete)
-b	batch	Run in batch mode. Ngspice reads the default input source (e.g. keyboard) or reads the given input file and performs the analyses specified
-s	server	Run in server mode.
-i	interactive	Run in interactive mode.
-r FILE	rawfile=FILE	Use rawfile as the default file into which the results of the simulation are saved.
-o	output=FILE	All logs generated during a batch run (-b) will be saved in outfile.
-h	help	A short help statement of the command line syntax
-v	version	Prints a version information.
-a	autorun	Start simulation immediately, as if a control section *.control* *run* *.endc* had been added to the input file.
	soa-log=FILE	output from Safe Operating Area (SOA) check

6.4.4 Simulating with the graphene FET library

Since the developed graphene FET library is a derivative of the MOSFET template, the device instance in SPICE scripts have to start with the letter 'M'. Table 6.3 shows the modelling parameters of the graphene FET library.

TABLE 6.3: Ngspice Model parameters for the graphene FET library

Parameter symbol	Parameter description
l	Channel length
w	Channel width
gnt	Model name
T	Operating temperature
u0	Hole-like surface mobility
k1	Top-gate dielectric constant
k2	Back-gate dielectric constant
vgs0	V_{gs} at the Dirac point
vbs0	V_{bs} at the Dirac point
ef	Critical electric field
hsub	Thickness of bulk substrate
rsp	hole-like conduction series resistance
rsn	electron-like conduction series resistance
n0	Minimum carrier density
u1	electron-like surface mobility
uf1	Alternative carrier mobility factor in electrons-like conduction
uf0	Alternative carrier mobility factor in holes-like conduction
nl	Number of layers
vef	Constant voltage due to electric field
rvbs0	Maximum resistance at the Dirac point
t_alpha	Temperature constant parameter
eta_p	Constant for resistance slope in the p-type region
eta_n	Constant for resistance slope in the n-type region
vtemp	Voltage constant parameter for the temperature
tref	Reference temperature

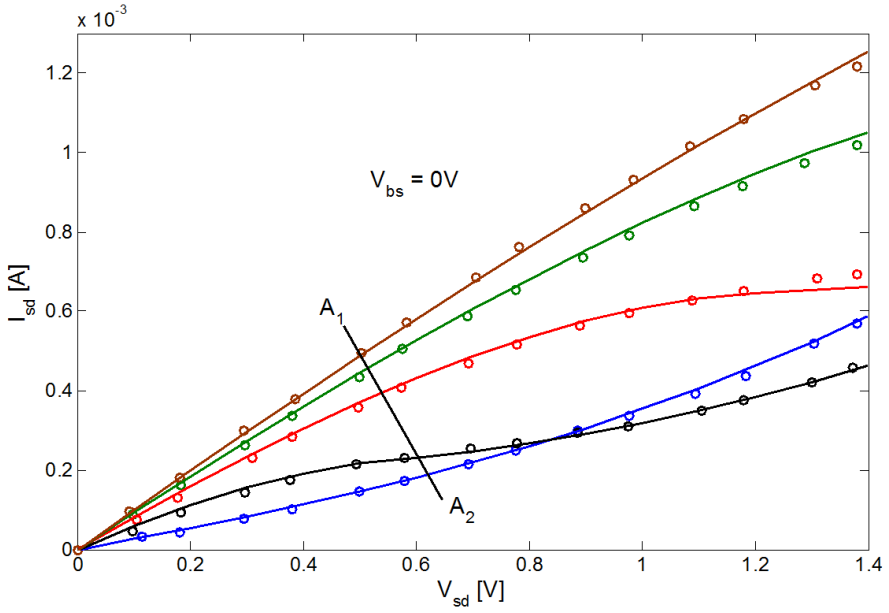


FIGURE 6.9: Experimental data (o) [127] and the Berkeley SPICE simulator model (–) for I_{sd} vs V_{sd} characteristics at V_{bs}= 0V. V_{ds} is varied from 0 to -1.4V for top-gate voltages of -1.25V, -0.75V, -0.25V , 0.25V and 0.75V (from top to bottom between cross-section A_1 and A_2)

This model allows the user to simulate an arbitrarily number of graphene channels. The model is limited to about 100 layers in the transistor. Taking the case of a four layer graphene channel, Fig. 6.9 shows a validation of the SPICE model with experimental measurement [127] for a sweep of V_{ds} at different V_{gs}. The netlist used to achieve the I-V characteristics is shown in Listing. 6.3.

```
.TITLE 'IV Characteristics for four layer GFET Transistor'

Vd    Vdd   Gnd   0
Vs    Vss   Gnd   0
Vg    Var   Gnd   0.75
Vb    Vbs   Gnd   0

M2 Vdd Var Vss Vbs gnt l=10e-6 w=5e-6 temp=26
.model gnt gnt nl=4 u0=13000e-4 tox=40e-9 ef=15e5
+k1=17 k2=3.9 vgs0=0.75 vbs0=0 hsub=500.0e-9 rsp=390
+u1=2900e-4 rvbs0=.37e4 eta_p=.8 eta_n=.8 vtemp=0.0086
+vef=3 tref=300 t_alpha=6e-7 n0=.5e16 uf0=0.223 uf1=0.223
+rsn=290

.op

.dc Vd -1.4 0 0.1 Vg 0.75 0.75 -.5
.dc Vd -1.4 0 0.1 Vg 0.25 0.25 -.5
.dc Vd -1.4 0 0.1 Vg -0.25 -0.25 -.5
.dc Vd -1.4 0 0.1 Vg -0.75 -0.75 -.5
.dc Vd -1.4 0 0.1 Vg -1.25 -1.25 -.5

.print dc I(Vs)
.end
```

LISTING 6.3: Netlist for a four-layer graphene FET I_{ds} Vs V_{ds} characteristics shown in Fig. 6.9

The model shows good agreement with the experimental data. Also, for the four layer channel the model shows good agreement when validated against experiment for a sweep of V_{gs} as a constant V_{ds} in Fig. 6.10. The netlist is shown in Listing. 6.4.

```
.TITLE 'Ids Vs Vgs Characteristics for four layer GFET Transistor'

Vd    Vdd   Gnd   0.1
Vs    Vss   Gnd   0
Vg    Var   Gnd   0
Vb    Vbs   Gnd   0

M2 Vdd Var Vss Vbs gnt l=10e-6 w=5e-6 temp=26
.model gnt gnt nl=4 u0=7000e-4 tox=40e-9 ef=15e5
+k1=17 k2=3.9 vgs0=0.75 vbs0=0 hsub=500.0e-9 rsp=290
+u1=3200e-4 rvbs0=.37e4 eta_p=.8 eta_n=.8 vtemp=0.0086
+vef=3 tref=300 t_alpha=6e-7 n0=.5e16 uf0=0.223 uf1=0.223
+rsn=200

.dc Vg -2 3 0.1

.print dc I(Vs)
.end
```

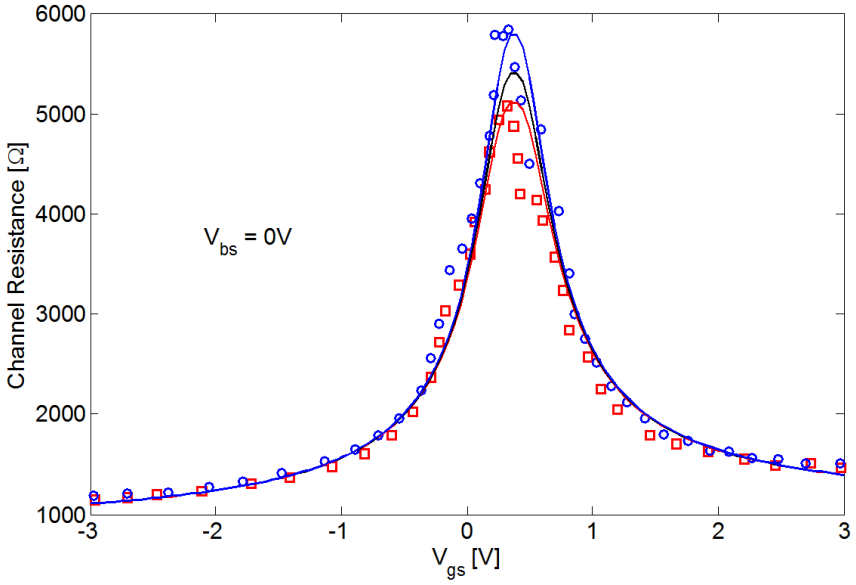


FIGURE 6.10: Characteristics of the channel Drain current against the top-gate voltage for $V_{ds} = 0.1V$(Experimental data(o) [127], Berkeley SPICE simulator model(–))

LISTING 6.4: Netlist for a four-layer graphene FET I_{ds} Vs V_{gs} characteristics shown in Fig. 6.10

Both Fig. 6.9 and Fig. 6.10 show good agreement with experimental data. This confirms that the SPICE model accurately simulates all the regions of operation of the transistor and the Jacobian entries are also accurate.

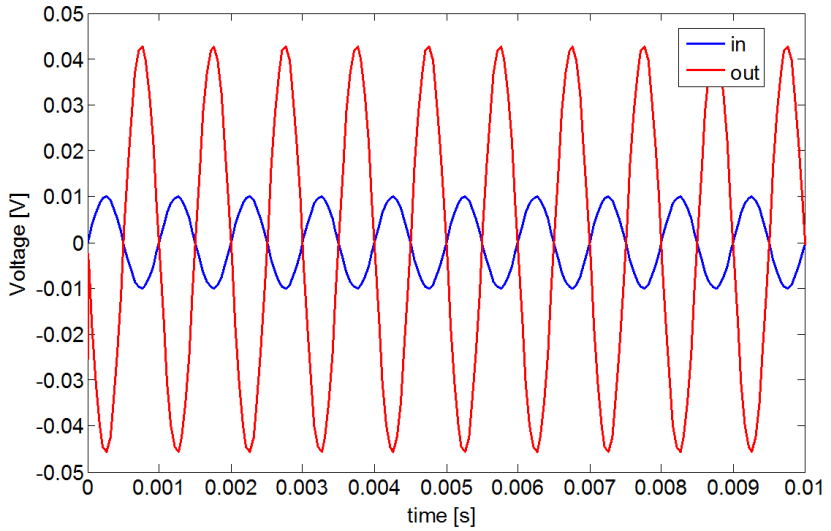


FIGURE 6.11: Characteristics of the channel resistance against V_{gs} at $V_{bs} = 0V$ for various operating temperatures. Result from the SPICE simulator is shown in solid line for temperatures 4.7K (blue), 14.4K (black) and 53K (red) (top to bottom). The experimental measurement [89] is shown in □ (53K) and *o* (4.7K)

In changing the *nl* (see Table. 6.3) model parameter from 4 to 1, the model can be used to simulate a single-layer graphene transistor. In Fig. 6.11, the model is validated against experimental data [89] for a plot of the channel resistance against V_{gs}. This test case is simulated at the following operating temperatures: 4.7K, 14.4K and 53K. The netlist is shown in Listing. 6.5.

```
.TITLE 'IV Characteristics for GFET Transistor'

Vd    Vdd   Gnd   0.01
Vs    Vss   Gnd   0
Vg    Var   Gnd   0.5
Vb    Vbs   Gnd   0

M2 Vdd Var Vss Vbs gnt l=1e-6 w=1.1e-6
.model gnt gnt nl=1 u0=4000e-4 tox=15e-9 ef=4.5e5
+k1=3.9 k2=3.9 vgs0=2.22 vbs0=-35 hsub=285.0e-9 rsp=400
+u1=4000e-4 rvbs0=4.65e3 eta_p=1 eta_n=1 vtemp=0.0086
+vef=2 tref=300 t_alpha=0.052 n0=.5e16 uf0=0.223 uf1=0.223
+rsn=500

.op

.dc Vg -3 3 0.05  temp -268.3 -268.3 1
.dc Vg -3 3 0.05  temp -258.6 -258.8 1
.dc Vg -3 3 0.05  temp -221 -221 1

.param par(Vdd,Vs)='V(Vdd)/I(Vs)'
.print dc par(Vdd,Vs) V(Vdd) I(Vs)

.end
```

LISTING 6.5: Netlist for a Single layer graphene FET channel resistance Vs V_{gs} characteristics shown in Fig. 6.10

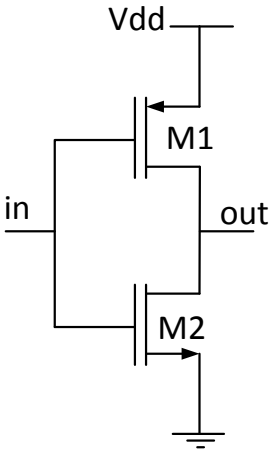
6.4.5 Example circuits

In this section the graphene FET library will be validated using two test circuits; a small signal voltage amplifier and a frequency multiplier. For analog and RF applications, graphene FET based voltage amplifiers [180, 181, 182] and frequency mixers and multipliers [172, 173, 174] have been reported. Although, graphene FET transistor are not currently suitable for making digital circuits, the ability to achieve a complementary transistor [15, 183] by shifting the threshold voltage is exploited in analog designs.

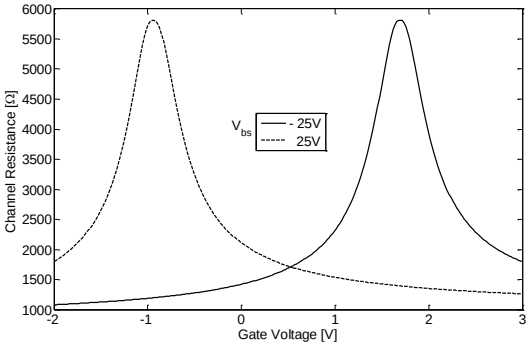
6.4.5.1 Voltage Amplifier

The circuit shown in Fig. 6.12(a) is simple two transistor voltage amplifier. This circuit design utilises two complementary transistors where transistor 'M1' can be viewed as P-type in the MOSFET sense and transistor 'M2' as N-type. The circuit design is the same as that used to achieve inversion by a complementary inverter [15]. In this circuit,

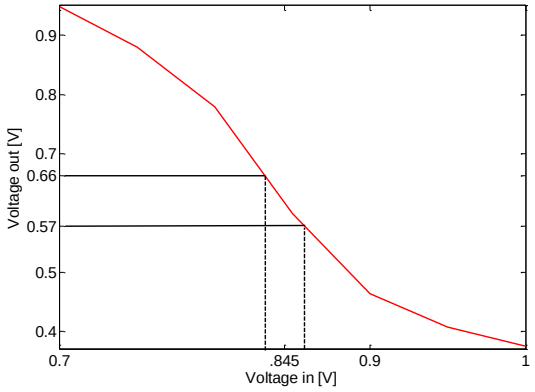
both transistors use a single-layer graphene channel. The SPICE netlist is shown in Listing. 6.6.



(a) Complementary graphene FET



(b) The conductance of each of the transistors



(c) A voltage sweep of the gate voltage around the voltage amplifier bias point

FIGURE 6.12: Circuit design and characteristics of the voltage amplifier

```
.TITLE 'GFET Transistor Voltage Amplifier'

Vd     Vdd    Gnd    1.5
Vs     Vss    Gnd    0
Vb     Vbs1   Gnd    25
Vb2     Vbs2  Gnd     -25
Vg   Var   Gnd   SINE(0.85 .01 1k)

M2 one Var Vss Vbs1 gnt l=1e-6 w=1.1e-6 temp=-268.3
.model gnt gnt nl=1 u0=4000e-4 tox=15e-9 ef=4.5e5
+k1=3.9 k2=3.9 vgs0=2.22 vbs0=-35 hsub=285.0e-9 rsp=400
+u1=4000e-4 rvbs0=4.65e3 eta_p=1 eta_n=1 vtemp=0.0086
+vef=2 tref=300 t_alpha=0.052 n0=.5e16 uf0=0.223 uf1=0.223
+rsn=500

M1 Vdd Var one Vbs2 gnt l=1e-6 w=1.1e-6 temp=-268.3
.model gnt gnt nl=1 u0=4000e-4 tox=15e-9 ef=4.5e5
+k1=3.9 k2=3.9 vgs0=2.22 vbs0=-35 hsub=285.0e-9 rsp=400
+u1=4000e-4 rvbs0=4.65e3 eta_p=1 eta_n=1 vtemp=0.0086
```

```
+vef=2 tref=300 t_alpha=0.052 n0=.5e16 uf0=0.223 uf1=0.223
+rsn=500

.op

.tran 50u .01
.print tran V(var) V(one)

.end
```

LISTING 6.6: Netlist for a single-layer graphene FET Voltage Amplifier shown in Fig. 6.13

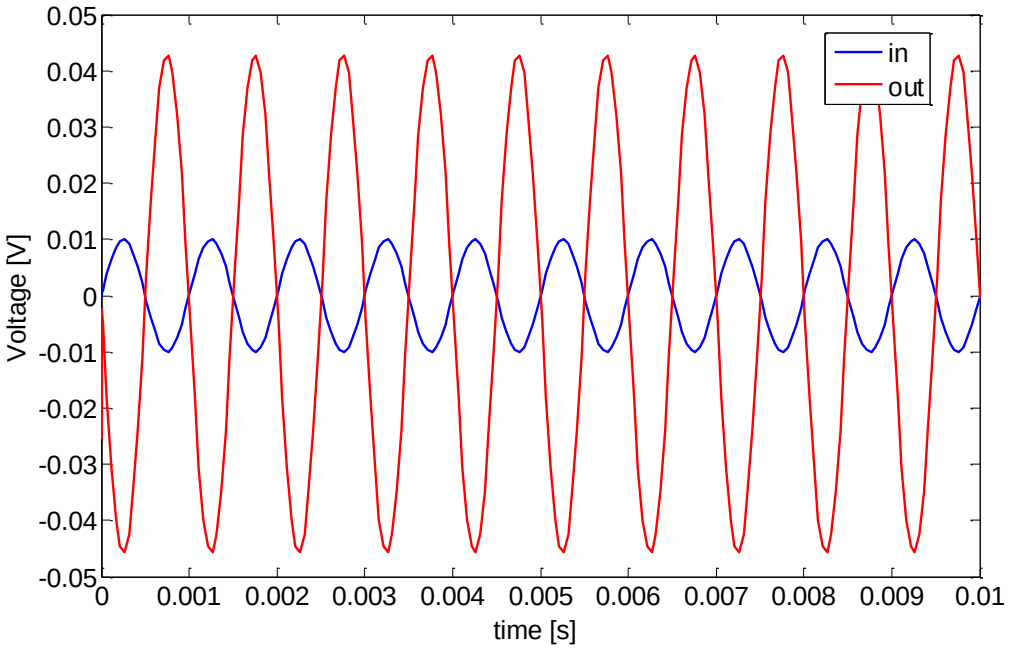


FIGURE 6.13: Normalized single-layer graphene FET characteristics of a small signal voltage amplifier

Fig. 6.12(b) shows the conductance of each of the transistors in the circuit. Biasing transistor 'M1' with 'V_{bs1}' ($V_{bs} = 25V$) a positive gate threshold voltage relative to the source voltage, ground, is achieved. This 'M1' serves as an N-type transistor in the complementary transistor circuit. Biasing transistor 'M2' with 'V_{bs2}' ($V_{bs} = -25V$) a negative gate threshold voltage relative to the source voltage, 'V_{dd}' is achieved. Thus, 'M2' is acts like a P-type transistor in the complementary transistor circuit. A sweep of the gate voltage will result in an inverter-like output characteristic as shown in Fig. 6.12(c).

Of particular interest is the linear voltage output where the both transistors experience charge neutrality point splitting. A DC voltage is used to bias the transistor at this region. Thus, for a small AC signal with a frequency of 1kHz, an amplitude of 20mV

and a DC offset of 0.85V, the AC gate voltage is amplified at the output. Fig. 6.13 shows about a four times amplification of the input voltage.

6.4.5.2 Frequency multiplier

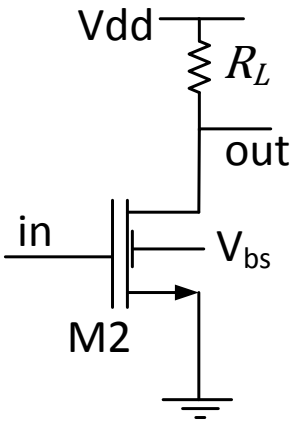


FIGURE 6.14: Circuit design for a graphene FET frequency doubler

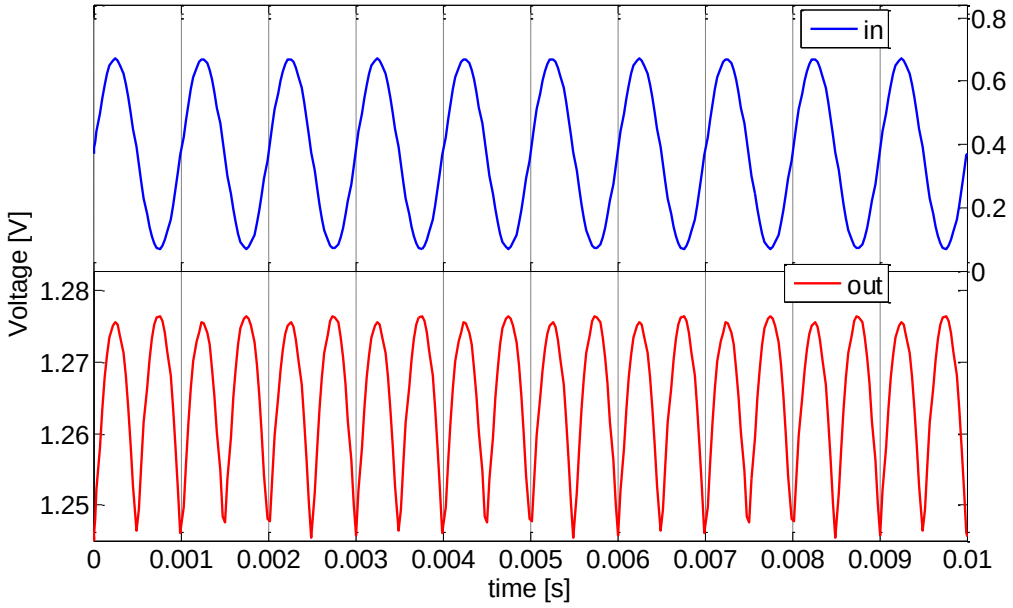


FIGURE 6.15: Single-layer graphene FET characteristics of a frequency doubler

This circuit generates an output signal whose frequency is twice that of the input frequency. The circuit diagram is shown in Fig. 6.14 and the SPICE netlist is shown in Listing. 6.7.

```
.TITLE 'IV Characteristics for GFET Transistor'
```

```
Vd     Vdd    Gnd    1.5
Vs     Vss    Gnd    0
Vb     Vbs   Gnd    0
Vg   Var   Gnd   SINE(0.37 .3 1k)


M2 one Var Vss Vbs gnt l=1e-6 w=1.1e-6 temp=-268.3
.model gnt gnt nl=1 u0=4000e-4 tox=15e-9 ef=4.5e5
+k1=3.9 k2=3.9 vgs0=2.22 vbs0=-35 hsub=285.0e-9 rsp=400
+u1=4000e-4 rvbs0=4.65e3 eta_p=1 eta_n=1 vtemp=0.0086
+vef=2 tref=300 t_alpha=0.052 n0=.5e16 uf0=0.223 uf1=0.223
+rsn=500

R1 one Vdd 1K

.op

.tran 30u .01
.print tran V(var) V(one)
.end
```

LISTING 6.7: Netlist for a Single layer graphene FET frequency doubler circuit

A single-layer graphene transistor is used in this analysis. The circuitry utilised the ambipolar ability of the graphene transistor to achieve a doubling of the frequency similar to the action of a full wave rectifier. A DC voltage offset is used at the gate to bias the transistor at its threshold voltage. In this case an offset of 0.37V is required. The gate signal has a frequency of 1kHz and an amplitude of 300mV.

Fig. 6.15 shows both the input and output voltage characteristics. Assuming a normalised input voltage centred at 0V. The operation of the frequency doubler is such that during a positive cycle of the AC input signal, the transistor 'M2' become electron-like (similar to an N-type MOSFET) and thus allows conduction of electron-like carrier in the channel from the ground terminal to 'V_{dd}' and the resulting current flows in the opposite direction. In the second half of the cycle when the input signal is negative, the transistor then becomes hole-like (similar to a P-type MOSFET) and allows conduction of hole-like carrier from 'V_{dd}' to the ground. The resulting current conduction is in the same direction as the carriers.

In both test circuits the simulator performed as reported graphene voltage amplifiers [182] and frequency multiplier [173]. This means that the graphene library is correctly integrated into the SPICE simulator and can be used to simulate its behaviour in both graphene and non-graphene based circuit designs. Also, the results show that the SPICE simulator does not have DC convergence problems and it can accurately calculate the operating points of the various nodes in circuits.

6.5 Transistor Optimization using a floating-gate

Here a floating-gate is added to a transistor whose result has been published[33]. A floating-gate has not currently been fabricated on a graphene transistor, therefore a simplified model will be adopted here to show the feasibility of the concept.

6.6 Carrier Tunnelling

The general device structure of a graphene field effect transistor with a floating-gate is depicted in Fig.6.16. In Fig. 6.16 the floating-gate is between the channel and the back-gate. By means of Fowler-Nordheim tunnelling[156] carriers can tunnel into and out of the floating-gate resulting in a threshold shift in the channel. Injection of electrons can be controlled by a separate circuit [158].

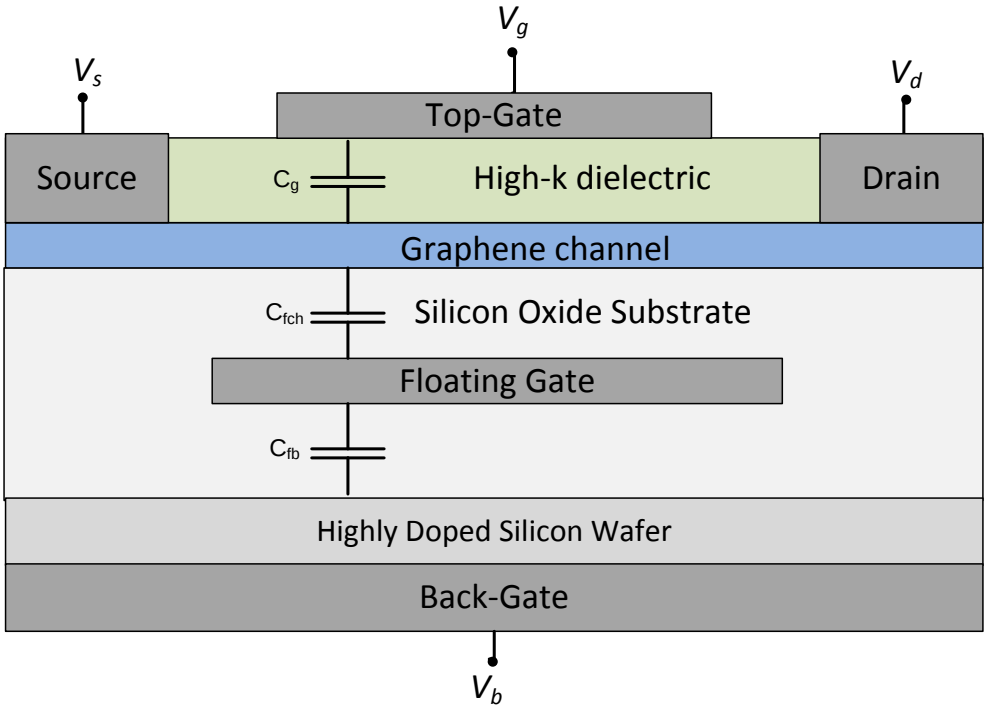


FIGURE 6.16: Transistor layout.

The following capacitances are created in the transistor, C_g between the top-gate and the channel, C_{fch} between the floating-gate and the channel and C_{fb} between the floating-gate and the back-gate terminal.

From Fig. 6.17, V_f is the potential of the floating-gate, V_s is the source potential, V_d is the drain potential and V_b is the back-gate potential.

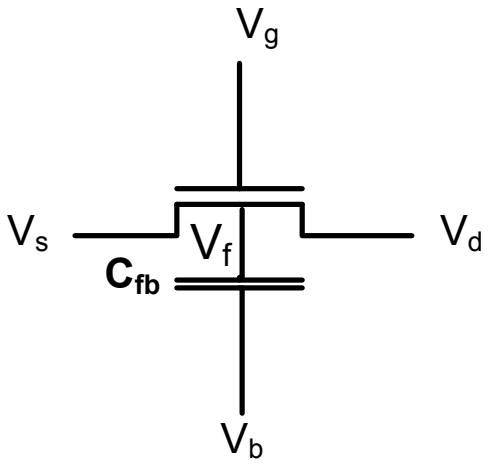


FIGURE 6.17: The capacitor and transistor equivalent of the floating-gate transistor

As C_g increases due to scaling of the transistor, it becomes comparable to the quantum capacitance [86], C_q, in the graphene channel. Therefore, for accurate modelling, C_g and C_q are in series, yielding $C_{top} = C_g C_q/(C_g + C_q)$.

C_{back} is the capacitance between the floating gate and the channel taking into account the quantum capacitance, $C_{back} = C_{fch} C_q/(C_{fch} + C_q)$.

As the transistor is further scaled into the nanoscale, direct tunneling will become an issue when the gate oxide is as thin as 1.5nm [154, 155]. assuming that there is no direct tunneling between the floating-gate and the terminals, then electrons will tunnel through the dielectric by Fowler-Nordheim tunneling [156] resulting in a current density given by

$$J_{tun} = \alpha E_{ox}^2 \exp\left(\frac{-\beta}{E_{ox}}\right) \tag{6.1}$$

where α and β are constants and E_{ox} is the electric field in the oxide between the floating-gate and the channel. Typical values of the critical electric field beyond which tunneling should be expected, range from 0.75/nm to 1.0V/nm [149, 158]. The tunnelling current density in Eqn. (6.1) shows a strong dependence on the electric field.

$$E_{ox} = \frac{Q_{ch} - Q_{fg}}{\epsilon_k} \tag{6.2}$$

From Eqn. (6.2), Q_{fg} is the charge density in the floating-gate, Q_{ch} is the charge density of the channel and ϵ_k is permittivity of the dielectric oxide. A proportionality of E_{ox}

with $1/\epsilon_k$ implies that for ultra thin gate oxides very high-k dielectric constant will be required to prevent tunneling.

6.7 Electronic Transport and Channel Resistance

The channel has a built-in potential at the Dirac point with the floating-gate-to-source at the Dirac point denoted by V_{fs}^0 and the top-gate-to-source at the Dirac point, V_{gs}^0. The threshold voltage V_o is given by Eqn. (6.3):

$$V_o = V_{gs}^0 + C_{back}/C_{top}(V_{fs}^0 - V_{fs}) \tag{6.3}$$

where V_{fs} is the floating-gate-to-source voltage. V_{fs} creates carriers in the graphene channel while the top-gate modulates the potential barrier in the channel to adjust the conductivity of the channel [71].

As the charge has to be conserved, the charge in the transistor is given by Q_{fb}.

$$Q_{fb} = C_{top}(V_{gs} - V_{gs}^0) + C_{back}(V_f - V_s - V_{fs}^0) + C_{fb}(V_f - V_b) \tag{6.4}$$

Thus, the channel carrier density in Eqn. (6.2) is shown below.

$$Q_{ch} = C_{top}(V_{gs} - V_o) \tag{6.5}$$

Based on the transistor terminal voltages, the potential of the floating-gate considering any possible tunnelling of carrier is given by Eqn. (6.6)

$$V_f(t_{i+1}) = \frac{Q_{fb}(t_{i+1}) - C_{top}(V_{gs} - V_{gs}^0)}{C_{back} + C_{fb}} + \frac{C_{back}(V_s + V_{fs}^0) + C_{fb}V_b}{C_{back} + C_{fb}} \tag{6.6}$$

where $t_i, i = 0, 1, ...$ is the time index, $\triangle t = t_{i+1} - t_i$ is the step size. For each step of the iteration the resulting charge $Q_{fg}(t_{i+1})$ will force a change in the floating-gate voltage in Eqn. (6.6). The electric field, E_{ox}, causes current to tunnel into or out of the floating-gate from Eqn. (6.1). Current tunneling between the floating-gate and the channel alters the charge in the floating-gate because $\frac{\partial Q_{fg}}{\partial t} = J_{tun}$. Due to tunnelling the charge in the floating-gate is shown below.

$$Q_{fg}(t_{i+1}) = Q_{fg}(t_i) + \triangle t(J_{tun}(t_i)) \tag{6.7}$$

V_g modulates the source potential barrier thereby controlling the resistance of the channel [74]. The total resistance of the channel is represented by Eqn. (6.8):

$$R_{total} = 2R_s + \frac{L}{W\mu q\sqrt{n_0^2 + n^2}} \tag{6.8}$$

where R_s is the series resistance which accounts for the contact resistance and the access resistance (the resistance between the contact and the active area of the channel), L is the length of the active area, W is the width, μ is the carrier mobility, n_0 is the residual carrier concentration and $n = Q_{ch}/q$ with q being the carrier charge. n_0 is usually extracted by fitting experimental data, its value usually lie in the vicinity of $10^{11}cm^{-2}$ [33, 74, 26] and it accounts for the drain current when $V_{gs} = V_o$.

6.8 Simulations of Transistor characteristics

In the simulation of a bilayer graphene transistor with a floating-gate, physical parameters [33] of an experimentally tested standard bilayer graphene transistor are used. Table. 6.4 shows the model parameters.

TABLE 6.4: Simulation Model Parameters

Model parameter	Value	Description
L(μm)	1	Channel length
W(μm)	2.1	Channel width
t_{ox}(nm)	15	Hafnium oxide thickness
$C_q(\mu\text{Fcm}^{-2})$	2	Quantum capacitance
k_1	16.0	Hafnium Oxide relative dielectric
k_2	3.9	Silicon oxide relative dielectric
V_{gs}^0(V)	1.45	Top-Gate to Source Dirac voltage
V_{bs}^0(V)	2.7	Back-gate to source Dirac voltage
H_{sub}(nm)	285	Floating-gate to channel thickness
$R_s(\Omega)$	1000	Series resistance
$\mu(\text{cm}^2/\text{V.s})$	300	mobility
X_{fg}(nm)	285	floating-gate to back-gate thickness

In the transistor using the transistor equations for the original transistor without a floating-gate, a mobility of 300cm^2/Vs closely matches the experimental data.

The channel resistance against changes in the top-gate voltage is shown in Fig. 6.18 for $V_{ds} = 0V$, V_{bs} of 10V, 0V and -10V respectively and a DC sweep of V_{gs} from -3V to 3V. The characteristics has a peak resistance at $V_{gs} = V_o$ which is 1.29V for $V_{bs} = 10V$ and 1.73V for $V_{bs} = -10V$. A back-gate bias of 68.73V is required to achieve a Dirac point voltage of 0V.

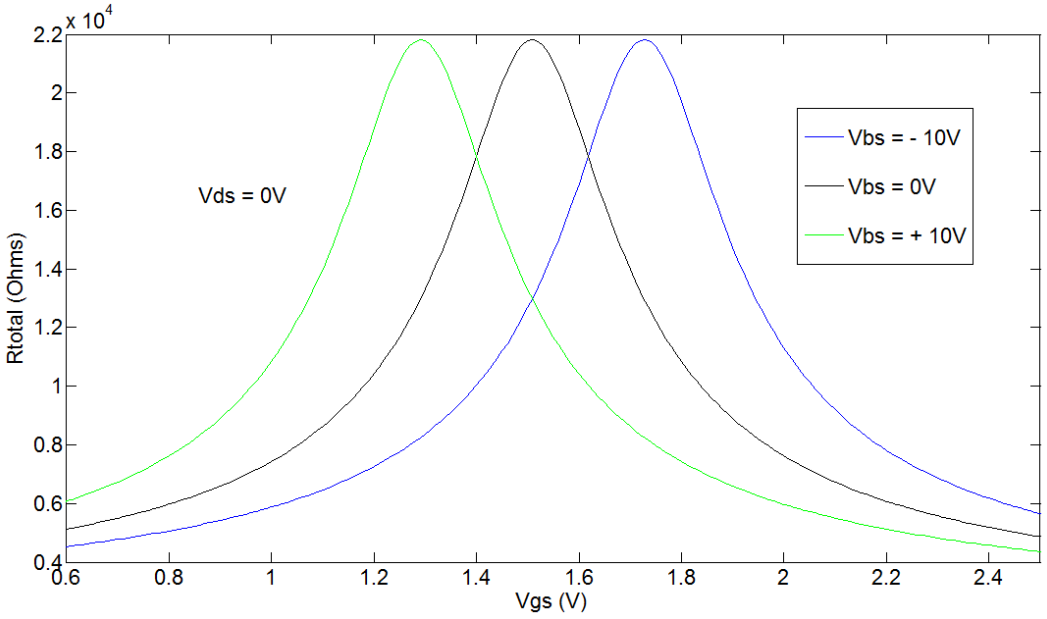


FIGURE 6.18: Channel resistance characteristics for graphene bilayer FET without a floating-gate

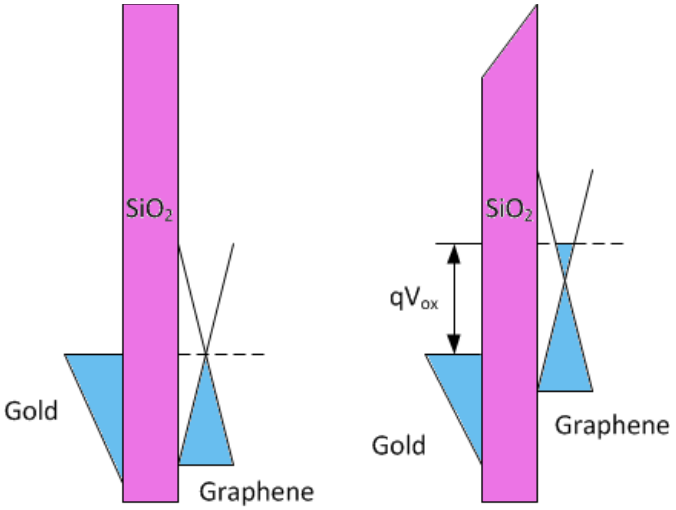


FIGURE 6.19: Electrons injected into the floating-gate

For a floating-gate attached, the device parameters α and β in Eqn. (6.1)are to be extracted from the transistor. These parameters have theoretical values of $\alpha = \frac{q^3}{16\pi^2\hbar(q\phi_b)}$, $\beta = \frac{4(\sqrt{2m_{eff}})(q\phi_b)^{1.5}}{3q\hbar}$ [156], where electronic charge, q, reduced Plank's constant, $\hbar$, oxide potential barrier, ϕ_b, electron effective mass, m_{eff} are the parameter definitions.

Fig. 6.19 illustrates the band diagram for electrons to be injected into the floating-gate. V_{ox} is the potential across the oxide. Using gold, Au, as the floating-gate with dimensions given in Table. 6.4. Au has a work-function of 5.1eV with SiO_2 corresponding to a conduction potential barrier, ϕ_b, of 4.0eV also bilayer graphene on SiO_2 has a work-function of 4.69eV [168] and a conduction potential barrier of band 3.59eV. The

conduction potential barrier is considered as the difference between the electron affinity of SiO_2 [162] and the work-function of the metal. This assumes that no layer of other dielectric is introduced into the SiO_2 between the floating-gate and the channel. This will considerable change the band offset due to a change in the band-gap [163].

$\alpha = 3.8704 \times 10^{-7} A/V^2$ and $\beta = 5.4885 \times 10^{10} V/m$ are the predicted device parameters for electrons to tunnel from the floating-gate. Here, the effective mass, $m_{eff} = 1.0 m_e$, where m_e is the free electron mass.

The graphene channel can be electrostatically doped by the electric field perpendicular to the channel. This doping causes a shift in the Dirac voltage giving rise to a tunable work-function [167] as the carriers can be by holes or electron, depending on the gate bias. Accordingly, for a positive (negative) V_{ov}, ($V_{ov} = V_{gs} - V_o$), implies the carrier is by electrons (holes). The excess carriers density induced by electrostatic doping is shown below [72].

$$n = \eta |V_{ov}| \tag{6.9}$$

The coefficient $\eta \approx 7.2 \times 10^{10} cm^{-2} V^{-1}$. The excess carrier density is a reflection of a shift from the graphene Dirac point [73].

$$E_D = \hbar v_F \sqrt{\pi n} \tag{6.10}$$

From Eqn. (6.10), v_F is the Fermi velocity. Therefore the barrier height of doped graphene on SiO_2 is expressed by Eqn. (6.11):

$$q\phi_b = q\phi_g \pm E_D \tag{6.11}$$

where $q\phi_g$ is the barrier height with no doping, in this case 3.59eV, and the positive (negative) E_D is for holes (electrons). Device parameters α and β for electron tunneling from the graphene channel can now be calculated using an effective mass of $0.041 m_e$ for electrons and $0.036 m_e$ for holes [166].

6.9 Complementary Inverter with Symmetrical Transfer Characteristics

The ability of the floating-gate to modulate the channel resistance has been exploited to develop an inverter. Two test cases are taken whereby one of the transistors, GFET1, is taken to have an initial charge in the floating-gate of 8.4fC and the second transistor,

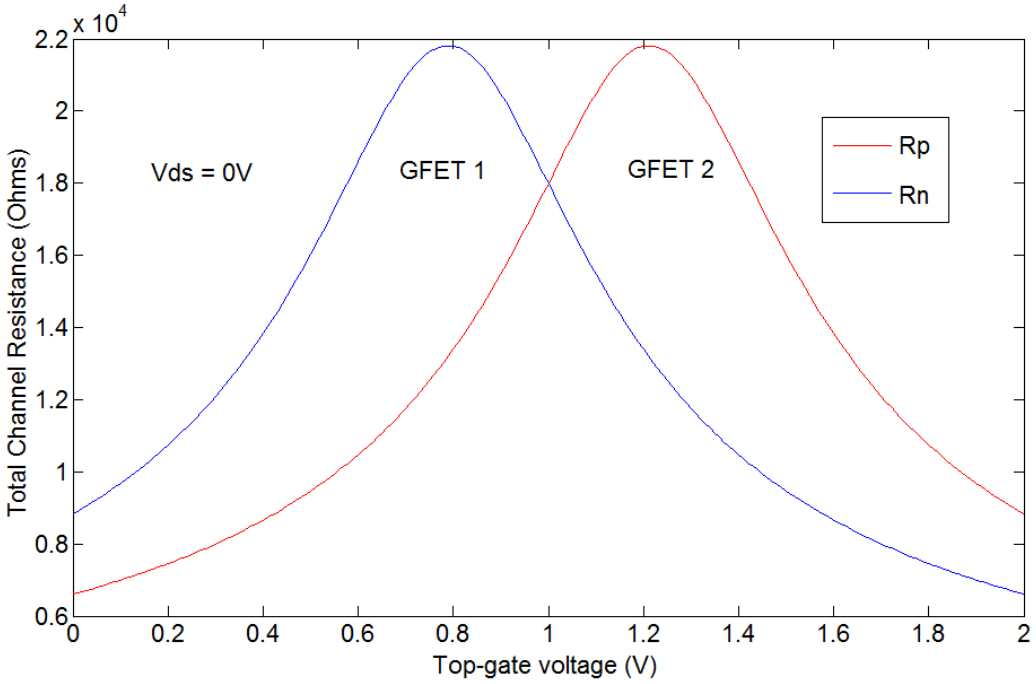


FIGURE 6.20: Channel resistance vs the top-gate voltage for a graphene transistor with and without a floating-gate

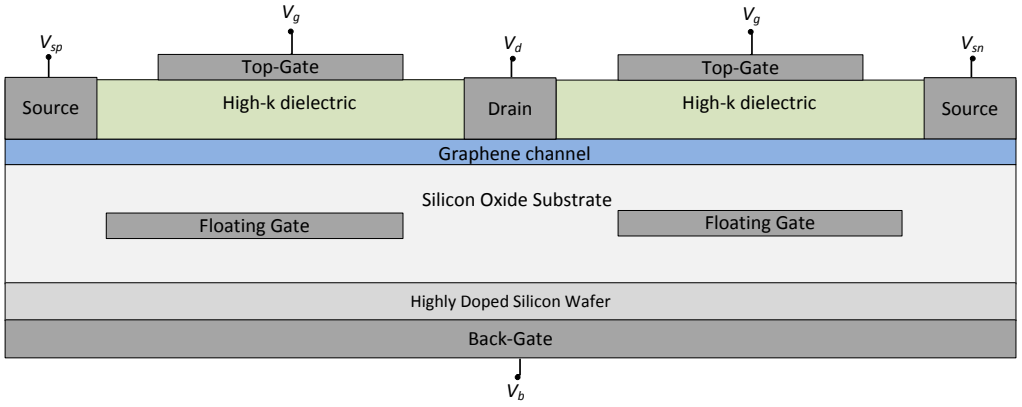


FIGURE 6.21: Complementary inverter layout using a floating-gate

GFET2, has a initial floating-gate charge of 27.3fC. For both transistors with $V_{ds} = 0V$ and the back-gate is grounded. Their respective channel resistance for a DC sweep of the top-gate from 0V to 2V is shown in Fig. 6.20. For GFET1 both the source and drain terminals are tied to ground while for GFET2, the source and drain are at 2V. A complementary inverter is simulated. The layout of the inverter is shown in Fig. 6.21. V_{sp} indicates the source terminal that is connected to the 2V supply while V_{sn} is grounded.

GFET1 shows an n-channel like behaviour while GFET2 shows a p-channel like behaviour presenting a complementary behaviour. Fig. 6.20 shows that both transistors

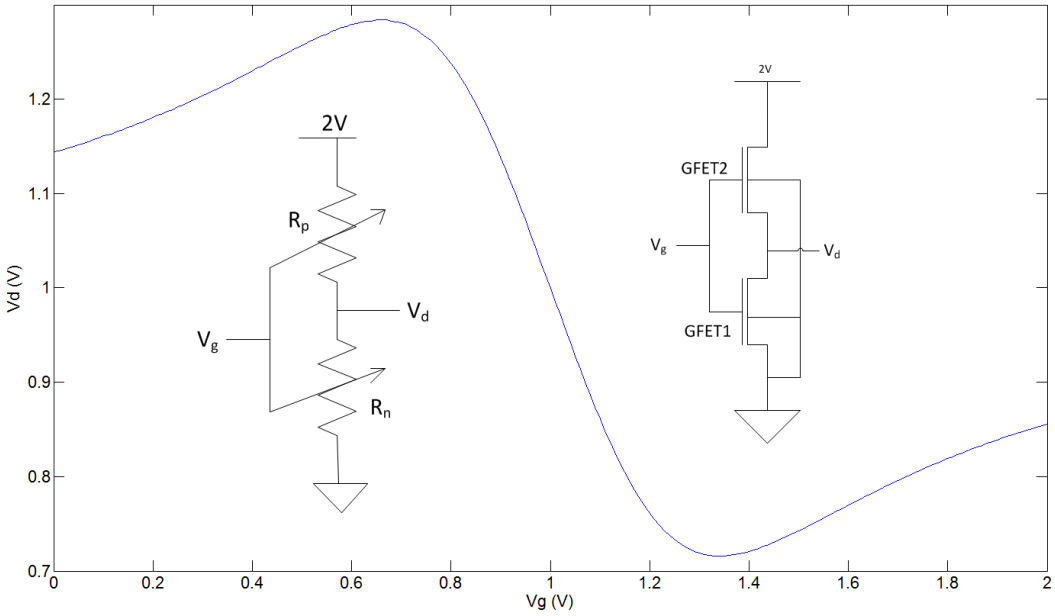


FIGURE 6.22: floating-gate complementary inverter characteristics for transistors induced with 27.3fC and 8.4fC respectively.

have a peak resistance at 0.8V and 1.2V respectively. Between the peaks the inverter will experience a charge neutrality point splitting which results in the inversion characteristics shown in Fig. 6.22.

The output voltage of the inverter is shown in Fig. 6.22 for a DC sweep of the input voltage, V_g, from 0 to 2V. In the simulation $V_b = 0V$, $V_{sp} = 2V$ and $V_{sn} = 0V$. A behavioural model was developed and simulated in HSPICE [141]. Bilayer graphene has no intrinsic bandgap as such the transistor does not cut-off. From Eqn. (6.8) the channel resistance of GFET1, R_n, and GFET2, R_p, are voltage controlled variable resistances as shown in Fig 6.22. Therefore, the inverter output voltage, V_d, is given by Eqn. (6.12):

$$V_d = V_{dd}\frac{R_n}{R_p + R_n} \tag{6.12}$$

where $V_{dd} = V_{sp} - V_{sn}$.

6.10 Summary

In this chapter, the implementation of the the proposed model for graphene FET in SPICE and the concept for a floating-gate graphene transistor is presented. The proposed model is implemented in three CAD tools; HSPICE, VHDL-AMS and Berkeley SPICE respectively. Using the circuit-level model developed in Berkeley SPICE, the proposed model shows a good agreement when validated against experimental data. Also, the experimentally validated transistor was used in simulating a voltage amplifier

and a frequency doubler. Both circuits simulations showed characteristics which agree with experimental observation of a similar circuits. Thus, the SPICE implementation correctly calculates the respective node voltages and currents.

In the analysis of a floating-gate, it was shown how the charge in the floating-gate creates an offset in the channel threshold thus making thee channel carrier density configurable. The channel carrier density is controlled by a floating-gate between the channel and the back-gate which results in a dependency of the Dirac point voltage on the charge in the floating-gate. This capability has been exploited to achieve p-type like and n-type behaviour.

The device parameter ensures that the inverter will be stable and there will be no tunnelling of electrons in and out of the floating-gate during the operation of the transistor. Using a floating-gate, a symmetric transfer characteristic in the inverter is achieved, with the voltage inversion centred at an input voltage of $V_{dd}/2$. To achieve this inverter characteristics without a floating-gate, each of the transistor would require a separate back-gate voltage to set the Dirac point voltage. This results in a large routing space and voltage sources in small designs because the Dirac point voltage is not controllable. Therefore, a different back-gate voltage source would be required for every transistor, while using a floating-gate allows both transistor have a common back-gate bias.

Chapter 7

Conclusion

In this thesis a novel SPICE-compatible models for the graphene transistor has been presented and successfully demonstrated. The models have been validated against a number of experimental measurements [77, 33, 127, 89] and shows a good agreement. To accurately model the drain current characteristics over the three regions of operation, both the hole-like and the electron-like conduction characteristics for each of the regions were derived using the drift equation. The derivation here is two fold. One aspect derives the transport characteristics within the region and the second aspect derives the boundary voltages within which these characteristics hold. To be compatible with SPICE, the Jacobian entries are shown to be continuous across the region boundaries.

By developing a layer specific capacitance model, an accurate relationship between the threshold voltage and the back-gate is demonstrated. The derivations of the threshold voltage carried out for both the single-layer and the bilayer transistor reveals that, in the single-layer the threshold voltage has a linear relationship with the back-gate voltage while in the bilayer, the linear relationship is against the surface potential of the second layer. This demonstrates the need for a layer specific equivalent circuit to accurately model the graphene transistor.

With a layer specific model, the change in potential energy between the layers accurately calculates the channel conductance with respect to its conductance at the intrinsic state. The models shows an equal conductance at the threshold voltages for a single-layer transistor, while the conductance of the bilayer slopes from the Dirac point voltage. At a constant temperature, the layer specific model can calculate the electric field induced off-current for a channel with an arbitrary number layers. Also, it is presented here that, in the bilayer transistor the surface potential of the second layer influences the degree to which the channel conductance is sensitive to changes in temperature. Therefore, an estimate of the bandgap of the graphene transistor is possible. A bandgap is essential if the transistor is to be used in future digital circuits.

In line with the growing need to design circuits with graphene transistors, a Berkeley SPICE library was developed for the layer specific model. Example circuits show that the model can be used for both digital and analog circuit designs. For easy use, the library is a derivative of the MOSFET template which allows circuit designers to invoke the library as it is currently done for MOSFETs. Also, to solve the problem of using individual back-gate voltages to optimize each transistor, a floating gate approach is also presented.

7.1 Chapter: Further Research

So far models use a fixed series resistance to model the transfer characteristics. Literature on experimental measurement of the contact resistance shows that it is modulated by the gate voltage. Depending on the transistor layout design, the transistor either has a dominant parasitic capacitance or an un-gated access resistance. The series resistance is combination of both the access and contact resistance and needs to be modelled to accurately estimate the carrier mobility in the channel.

In deriving the dependence of the channel on the vertical electric field, a fitting parameter, V_T is used. V_T gives a measure of the slope of the thermionic resistance with respect to electric field. However, different values of V_T are used to fit all the validations carried out. It is necessary in future work to determine model parameters that estimate V_T. Similar to V_T is T_o used in the single-layer transistor (see eqn. (4.20)) and T_α in the bilayer transistor (see eqn. (5.25)).

Section 2.6 of the literature review presents the current application of the graphene transistor which includes ring oscillator, frequency doubler and multiplier. So far just a little work has been done in investigating applications that utilize the ambipolar conduction of graphene. This is therefore an aspect for further work.

In the future engineering a bandgap in graphene to make it suitable for digital logic may be possible, therefore current graphene models have to be improved to apply to the graphene transistor with an intrinsic bandgap.

Appendix A

Published papers

Below are the list of publications during the course of this work.

1. I. Umoh, T. Kazmierski, and B. Al-Hashimi, "A dual-gate graphene fet model for circuit simulation - spice implementation," Nanotechnology, IEEE Transactions on, vol. 12, no. 3, pp. 427435, 2013.

2. I. J. Umoh and T. J. Kazmierski, "HSPICE implementation of a device model for a dual gate graphene field effect transistor," in ETRAN 2011, June 6-9 2011, pp. 1-4.

3. I. J. Umoh and T. J. Kazmierski, "VHDL-AMS model of a dual-gate graphene fet," in Specification Design Languages, 2011. Forum on, September 13-15 2011, pp. 1-5.

4. I. J. Umoh and T. J. Kazmierski, "Ambipolar graphene fet: modelling in VHDL-AMS," in Virtual Worldwide Forum for PhD Researchers in Electronic Design Automation, Nov 28 - Dec 3 2011, pp. 1-4.

5. I. J. Umoh and T. J. Kazmierski, "Graphene devices with bandgap - modelling and identication" in Proceedings of 57th ETRAN Conference, Zlatibor, Serbia, June 3-6, 2013, pp. EL1.1.1-5.

6. I. J. Umoh and T. J. Kazmierski, "A floating gate Graphene FET complementary inverter with symmetrical transfer characteristics," in ISCAS 2013, May 19-23 2013, pp. 1-4

7. I. J. Umoh, T.J. Kazmierski, and B.M. Al-Hashimi. "Multi-layer graphene FET compact circuit-level model with temperature effects." In: Nanotechnology, IEEE Transactions on (2014).

8. 5. I. J. Umoh and T. J. Kazmierski, "Temperature dependent graphene channel SPICE implementation," in 14th IEEE International Conference on Nanotechnology, August 18-21 2014,[Accepted]

Appendix B

CAD Tools

B.1 Behavioural model code for HSPICE

```
.protect
.PARAM q = 1.60217646e-19      $ electron charge
.PARAM T = 'temp+273'           $ Temperature of operation.
.PARAM Kb = 1.3806503e-23       $ Boltzmann's constant
.PARAM pi='355/113'            $ Constant PI
.PARAM vf = 1e6                 $ Characteristic electron velocity
.PARAM epsr = 8.85418782e-12     $ Permittivity of vacuum
.PARAM h = 6.626068e-34         $ Plank's constant
.PARAM h_ba = 'h/2/pi'         $ Reduced Plank's constant
.unprotect
```

Listing B.1: The HSPICE param.lib file

```
*        Library name: "GFET.lib"
.LIB gfet
.protect
.option EPSMIN=1e-99
.INCLUDE 'param.lib'

.SUBCKT  pGFET  Drain  Gate  Source  Sub  Hsub=285e-9  tox=15e-9  L=1e-6  W=2.1e-6
Cgio=1 Ec=4.5e5 Rs=800 mu=700e-4 ntop=2.1209e16 Vgs0=1.45 Vbs0=2.7 k_sub=3.9 k=16

.param Cq = 'sqrt(ntop/pi)*q^2/vf/h_ba'
.param Ce = 'Cgio*epsr*k/tox'
.param Ctop = 'Cq*Ce/(Cq+Ce)'
.param Cback = 'epsr*k_sub/Hsub'

*V0 functions as a device threshold voltage controlled by the back gate
.param aVo(Vbs) = 'Vgs0 + (Cback/Ctop)*(Vbs0 - Vbs)'

.param aVc = 'Ec*L'
.param aVg0(Vgs,Vbs) = 'Vgs - aVo(Vbs)'
.param Rc = '1/((W/L)*mu*Ctop*aVc)'
.param Rnorm = 'Rs/Rc'
.param aVdsat(Vgs,Vbs) = '2*Rnorm*aVg0(Vgs,Vbs)/(1+Rnorm)+(1-Rnorm)/
(1+Rnorm)^2*(aVc-sqrt(aVc^2-2*(1+Rnorm)*aVc*aVg0(Vgs,Vbs)))'
.param aIo(Vds,Vgs,Vbs) = '2*(W/L)*mu*aVc*Ctop*(Vgs-aVo(Vbs)-Vds/2)'
```

```
.param ans(Vds,Vgs,Vbs) = '-(1/4/Rs*(Vds-aVc+aIo(Vds,Vgs,Vbs)*Rs +
sqrt((Vds-aVc+aIo(Vds,Vgs,Vbs)*Rs)^2 -4*aIo(Vds,Vgs,Vbs)*Rs*Vds))*(Vds>aVdsat(Vgs,Vbs))+
(Vds<=aVdsat(Vgs,Vbs))*(Rnorm/Rs/(1+Rnorm)^2*(-Vc+(1+Rnorm)*aVg0(Vgs,Vbs)+sqrt(aVc^2-2*
(1+Rnorm)*aVc*aVg0(Vgs,Vbs)))+mu*Cback*(abs(Vbs-Vgs)-
abs(Vbs0-Vgs0))*Vds*W/L/10*(Vds/aVdsat(Vgs,Vbs) -1)^2))'
*****************************************
* capacitances and resistances
*****************************************
Cgs_ch      Gate      Schannel   '0.5*Ctop*W*L'
Cgd_ch      Gate      Dchannel   '0.5*Ctop*W*L'
Cbs_ch      Sub       Schannel   '0.5*Cback*W*L'
Cbd_ch      Sub       Dchannel   '0.5*Cback*W*L'
rs_ch       Drain     Dchannel   'Rs'
rd_ch       Source    Schannel   'Rs'
rdummy       drain     source     12e12
*****************************************
* voltage controlled current source
*****************************************
GFET1       Schannel  Dchannel      CUR='(V(Drain)<=V(Source))*
ans(V(Drain)-V(Source),V(Gate)-V(Source),V(Sub)-V(Source))'
GFET2       Dchannel  Schannel      CUR='(V(Drain)>V(Source))*
ans(V(Source)-V(Drain),V(Gate)-V(Drain),V(Sub)-V(Drain))'
.ENDS pGFET
.unprotect
.ENDL gfet
```

Listing B.2: Graphene FET HSPICE library file gfet.lib

B.2 Behavioural model code for VHDL-AMS

```
library IEEE;
use IEEE.math_real.all;
use IEEE.electrical_systems.all;
entity v_pulse is
    generic(
            initial: real:= 0.0;
            pulse : real:= 5.0;
            tchange : time:= 10sec); -- initial to pulse
    port(terminal po,ne: electrical);
end entity v_pulse;
architecture behaviour of v_pulse is
    function time2real(tt : time) return real is
    begin
    return time'pos(tt) * 1.0e-15;
    end time2real;
    constant sign : real := pulse/abs(pulse);
    constant slope:real := abs(pulse)/time2real(tchange);
    quantity v across i through po to ne;
    -- signal used in CreateEvent process below
    signal pulse_signal : real := initial;
begin
    v==sign*pulse_signal'slew(slope);
    CreateEvent : process
    begin
    wait until domain = time_domain; -- run process in Time Domain only
```

```
    pulse_signal <=abs(pulse);
    end process CreateEvent;
end architecture behaviour;
```

LISTING B.3: Time dependent voltage sweep in v_pulse.vhd

```
library IEEE;
use IEEE.math_real.all;
use IEEE.electrical_systems.all;
entity v_source is
       generic(VDC: voltage);
       port(terminal V_term, V_ref: electrical);
end entity v_source;
architecture val of v_source is
       quantity v across i through V_term to V_ref;
begin
       v == VDC;
end architecture val;
```

LISTING B.4: Voltage sources in v_source.vhd

```
library IEEE;
use IEEE.math_real.all;
use IEEE.electrical_systems.all;
use IEEE.fundamental_constants.all;
library work;
package gfetmodel is
        function Fgfet(Vds, Vgs, Vbs, Rs, mu, Ec, Cgio, Hsub, tox, L, W,
        ntop, Cq, Vgs0, Vbs0, k, k_sub: real)
        return real;
end package gfetmodel;

package body gfetmodel is
    -- some physical constants:
        --PHYS_EPS0     --Permittivity of vacumm
        --MATH_PI        -- Constant PI
        --PHYS_Q        -- Electronic Charge
        --constant vf   : real := 1.0E6; -- Characteristic electronic velocity

        --PHYS_H_OVER_2_PI       -- Reduced Plank's constant
        --PHYS_K        -- Boltzmann constant
        function Fgfet(Vds, Vgs, Vbs, Rs, mu, Ec, Cgio, Hsub, tox, L, W, ntop, Cq,
        Vgs0, Vbs0, k, k_sub: real) return real is
                        variable Ce, Ctop, Cback, Vc, Ids, Rc, Gamma, Vo, Vg0, Vdsat, Io: real:=0.0;
                begin
                  --Cq := (ntop/MATH_PI)**0.5*PHYS_Q**2/vf/PHYS_H_OVER_2_PI;
                  Ce := Cgio*PHYS_EPS0*k/tox;
                  Ctop := Cq*Ce/(Cq+Ce);
                  Cback := PHYS_EPS0*k_sub/Hsub;
                  --Vo functions as a device threshold voltage controlled by the back gate
                  Vo := Vgs0 + (Cback/Ctop)*(Vbs0 - Vbs);
                  Vg0 := Vgs - Vo;
                  Vc := Ec*L;
                  Rc := 1.0/((W/L)*mu*Ctop*Vc);
                  Gamma := Rs/Rc;
                  Vdsat := 2.0*Gamma*Vg0/(1.0+Gamma)+(1.0-Gamma)/(1.0+Gamma)**2.0*
                  (Vc-sqrt(Vc**2.0-2.0*(1.0+Gamma)*Vc*Vg0));
                  Io := 2.0*(W/L)*mu*Vc*Ctop*(Vgs-Vo-Vds/2.0);
                  if Vds > Vdsat then
```

```
                  Ids := 1.0/4.0/Rs*(Vds-Vc+Io*Rs + sqrt((Vds-Vc+Io*Rs)**2.0 - 4.0*Io*Rs*Vds))
                elsif Vds <= Vdsat then
                  Ids := (Gamma/Rs/(1.0+Gamma)**2.0*(-Vc+(1.0+Gamma)*Vg0+sqrt(Vc**2.0-2.0*
                  (1.0+Gamma)*Vc*Vg0))+mu*Cback*abs(Vbs-Vbs0)*Vds*W/L/10.0*(Vds/Vdsat -1.0)**2
                else
                Ids := 0.0;
                end if;
                      return Ids;
        end function Fgfet;
end package body gfetmodel;
```

Listing B.5: The graphene FET model package in gfetmodel.vhd

```
library IEEE;
library EDULIB;
use IEEE.math_real.all;
use IEEE.electrical_systems.all;
use IEEE.fundamental_constants.all;

library work;
use work.gfetmodel.all;
entity gTransistor is
    generic( -- model parameters
                        Rs : real := 800.0;
                        mu : real := 700.0e-4;
                        Ec : real := 4.5e5;
                        Cgio  : real := 0.8072;
                        Hsub  : real  := 285.0e-9; -- Substate thickness
                        tox : real  := 15.0e-9; -- top gate dielectric thickness
                        L : real  := 1.0e-6; -- Gate lenght
                        W : real  := 2.1e-6; -- Channel Width
                        ntop : real := 2.1209e16; -- carrier concentration
                        Cq   : real := 2.0e-2;  -- quantum capacitance
                        Vgs0 : real := 1.45; -- Gate-to-Source voltage at the Dirac point
                        Vbs0 : real := 2.7; -- Bulk-to-Source voltage at the Dirac point
                        k               : real := 16.0; -- Top gate dielectric
                        k_sub : real := 3.9 -- Back gate substrate dielectric
        );
    port (terminal drain, gate, back_gate, source: electrical);
end entity gTransistor;

architecture Characteristic of gTransistor is
        --terminal values
        terminal drainint, sourceint : electrical;
        quantity Vds across drain to source;
        quantity Vgs across gate to source;
        quantity Vbs across back_gate to source;
        quantity Ids through drainint to sourceint;
begin
        Ids == Fgfet(Vds, Vgs, Vbs, Rs, mu, Ec, Cgio, Hsub,     tox, L, W, ntop, Cq,
        Vgs0, Vbs0, k, k_sub);
        -- Capacitances of the model

        C1: entity EDULIB.capacitor(ideal) generic map( cap=>(Cq*PHYS_EPS0 * k  * Cgio *
        W * L/ tox/(Cq+PHYS_EPS0 * k  * Cgio * W * L/ tox))* 0.5)
        port map (p1=>gate, p2=>sourceint);
        C2: entity EDULIB.capacitor(ideal) generic map( cap=>(Cq*PHYS_EPS0 * k  * Cgio * W *
        L/ tox/(Cq+PHYS_EPS0 * k  * Cgio * W * L/ tox))* 0.5)
        port map (p1=>gate, p2=>drainint);
```

```
        C3: entity EDULIB.capacitor(ideal) generic map( cap=>PHYS_EPS0 *
        k_sub * W * L * 0.5/Hsub)
        port map (p1=>back_gate, p2=>sourceint);
        C4: entity EDULIB.capacitor(ideal) generic map( cap=>PHYS_EPS0 *
        k_sub * W * L * 0.5/Hsub)
        port map (p1=>back_gate, p2=>drainint);
        R1: entity EDULIB.resistor(ideal) generic map( res=>Rs)
        port map (p1=>drain, p2=>drainint);
        R2: entity EDULIB.resistor(ideal) generic map( res=>Rs)
        port map (p1=>source, p2=>sourceint);
end architecture Characteristic;
```

Listing B.6: Top level of the graphene FET model in gTransistor.vhd

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