UNIVERSITY OF SOUTHAMPTON

Development of Low Temperature Fabrication Processes of n-ZnO/p-Si Optical Switch and Poly-Silicon Waveguides for CMOS-Compatible Multi-Layered Silicon Photonics

by

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A thesis submitted in partial fulfillment for the degree of Doctor of Philosophy

in the

Faculty of Physical Sciences and Engineering

School of Electronics and Computer Science

August 2014

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING
SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

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The potential advantages and applications of *Silicon Photonics* (SiP) has initiated substantial research efforts. Silicon photonics has been favourably nominated to replace the current copper interconnects due to their high bandwidth, small footprint, and potentially low power consumption. However, the majority of the research into silicon photonics has been based on the silicon-on-insulator (SOI) platform. The focus on the SOI platform has limited the design of silicon photonic devices to two-dimensional (2D) structures. Moreover, the fabrication of optical active devices based on silicon photonics has relied on high temperature processing that is not compatible with CMOS back-end integration. New materials that are depositable at low temperatures can offer new possibilities for multi-layered, CMOS back-end compatible, and low optical loss silicon photonic devices. In this project, zinc oxide (ZnO) was investigated as a potential low temperature material whose fabrication is compatible with CMOS technology. Specifically, the naturally n-type doped ZnO can potentially form a heterojunction with p-type silicon without the need for high temperature processing. Poly-silicon is also a depositable and CMOS compatible material that can potentially form future multi-layered silicon photonic structures. However, low optical loss in poly-silicon has been based on high-temperature processing to improve the crystallinity and roughness of the deposited material. The deposition of poly-silicon in the SiP technology have been mainly carried out using plasma-enhanced chemical vapour deposition (PECVD) and other deposition techniques remain under investigated.

In this project, ZnO was, for the first time, deposited at low-temperature (150 °C) using atomic layer deposition (ALD) on a silicon waveguide to form a heterojunction diode capable of producing optical switching in the silicon core. Optical switching in the n-ZnO/p-Si heterojunction was caused by the plasma dispersion effect. The design of the optical switch comprised a straight silicon waveguide ($width = 1000$ nm, $height = 220$ nm, $slabheight = 60$ nm) partially covered with a thin ZnO film ($thickness = 10$ nm). The commonly used highly doped p^+ region were not included in the devices because of the high thermal budget ($T \simeq 900\,^{\circ}\mathrm{C}$) needed to activate the dopant. Moreover, the aluminium (Al) metal contacts were not annealed because the annealing temperature ($T_s = 425\,^{\circ}\mathrm{C}$) exceeds the high-temperature threshold ($T_s = 400\,^{\circ}\mathrm{C}$). An extinction ratio of ~ 10 dB was achieved for a 1 mm long device at 20 V forward-bias. This result can be expressed as a figure of merit of 5 dB/cm.V. The insertion loss of the device was estimated to be ~ 1.2 dB. The maximum switching speed of the devices was found to be ~ 1 MHz. Although this performance is inferior to the state-of-the-art silicon optical switches, it offers the first silicon-based electro-optical switch fabricated at low-temperatures with low insertion loss. Detailed analysis of the I-V and switching characteristics of the device revealed large series resistance and capacitance. It was also found that the switching speed is primarily governed by the

RC time constant of the device rather than the minority carrier lifetime. This fact has led us to believe that the device functions as both injection and accumulation electro-absorption switch. A thin SiO_2 layer is suspected to form at the ZnO/Si interface that facilitates the accumulation operation of the device and increases the RC time constant.

The first low loss and low-temperature poly-silicon waveguides are demonstrated in this project. Hot-wire chemical vapour deposition (HWCVD) was used to deposit poly-silicon films at 240 °C. The propagation loss of the TE mode for a 600 by 220 nm waveguide was 13.5 dB/cm. Detailed simulation analysis revealed that at least 60% of the loss was caused by the roughness of the top surface of the waveguides. The RMS roughness was measured using atomic force microscopy (AFM) and was found to be 8.9 nm. Optimisation of the design, the deposition process, and the reduction of the top surface roughness, through surface planarisation, led to a reduction in the propagation loss of the TE mode to $\sim$ 8.5 dB/cm while still maintaining low deposition temperature of 360°C. The crystal volume fraction of the optimised poly-silicon film was found to be $\sim$ 96%. An electro-optical switch based on ZnO and poly-silicon heterojunction was fabricated on a multi-layered poly-silicon structure. However, there were problems with the metal contact pads as well as the thickness of the first poly-silicon layer. Future work will focus on improving the n-ZnO/p-Si heterojunction electro-optical performance by adapting an accumulation type structure as well as optimising the multi-layered poly-silicon platform.

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Declaration of Authorship

I, Taha Ben Masaud, declare that the thesis entitled Low Temperature Fabrication Process of n-ZnO/p-Si Optical Switch and Hot-Wire Chemical Vapour Deposition Poly-Silicon Waveguides and the work presented in it are my own. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at the University;
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- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as:
  - **Ben Masaud, Taha**, Tarazona, Antulio, Jaberansary, Ehsan, Chen, Xia, Reed, Graham T., Mashanovich, Goran Z. and Chong, Harold M. H. (2013) Hot-wire Polysilicon Waveguides with Low Deposition Temperature. Optics Letters, 38, (20), 4030-2.
  - Jaberansary, Ehsan, **Ben Masaud, Taha M.**, Nedeljkovic, Milos, Miloevi, Milan, Mashanovich, Goran Z. and Chong, Harold M.H. (2013) Scattering loss estimation using 2D Fourier analysis and modelling of sidewall roughness on optical waveguides. IEEE Photonics Journal, 5, (3), 6601010.
  - Miloevi, Milan M., Nedeljkovic, Milos, **Ben Masaud, Taha M.**, Jaberansary, Ehsan, Chong, Harold M. H., Emerson, Neil G., Reed, Graham T. and Mashanovich, Goran Z. (2012) Silicon waveguides and devices for the mid-infrared. Applied Physics Letters, 101, (12), 121105-[4pp].
  - Mohamed Sultan, Suhana, Sun, Kai, Clark, Owain, **Ben Masaud, Taha**, Fang, Q., Gunn, R., Partridge, J., Allen, M. W., Ashburn, Peter and Chong, Harold (2012) Electrical characteristics of top-down ZnO nanowire transistors using remote plasma ALD. IEEE Electron Device Letters, 33, (2), 203-205.

- parts of this work have been published in the following conferences:
  - **Ben Masaud, Taha M.**, Tarazona, A., Chen, Xia, Reed, Graham T. and Chong, Harold M. H. (2013) Low temperature hot-wire polysilicon waveguides. In, Conference on Lasers and Electro-Optics Pacific Rim, Kyoto, Japan.
  - **Taha M. Ben Masaud**, Antulio Tarazona, Xia Chen, Graham Reed, and H. M. H Chong. Low Temperature Hot-Wire Polysilicon Waveguides Devices. In, European Optical Society Annual Meeting (EOSAM),September 2012, Aberdeen, Scotland (2012).
  - **Ben Masaud, Taha**, Jaberansary, Ehsan, Mohamed Sultan, Suhana, Clark, Owain D., Sharp, Thomas, Gunn, Robert, Bagnall, Darren M and Chong, Harold M H (2012) Compact Fabry-Perot electro-optic switch based on n-ZnO/p-Si heterojunction structure. In, IEEE Nano 2012 12th International Conference on Nanotechnology, Birmingham, UK.
  - **T. M. Ben Masaud**, E. Jaberansary, D. M. Bagnall, H. M. H. Chong, "Silicon Electro-optic Switch based on n-ZnO/p-Si Heterojunction Structure," paper number: P1.27, 136-138, The 8th IEEE International Conference on Group IV Photonics, London, UK, 14-16 Sep 2011.
- parts of this work is planned to be submitted as follows:
  - Silicon Electro-optic Switch based on n-ZnO/p-Si Heterojunction, in IEEE Technology Letters.
  - Low temperature Low Loss Hot-Wire CVD polysilicon waveguides for Photonic Integrated Circuits, in Optics Letters.
  - Multi-layered Silicon Photonics Platform, in CLEO Europe 2015.

Acknowledgements

First and foremost I praise and acknowledge Allah, the most beneficent and the most merciful.

The assistance and guidance of several people made the completion of this thesis possible. It is my pleasure to express my gratitude to those who contributed to this project and supported me in completing this thesis. Firstly, I would like to express my appreciation to Dr. Harold M. Chong for his exceptional supervision and invaluable assistance throughout my PhD research from the partial tuition fees funding to the completion of this thesis. I would like to thank him for his patience, assistance, and encouragement through critical times during my PhD. I am also thankful to Dr. Chong's critical thinking and superior knowledge that has helped me shape my research attitudes and skills. Secondly, I would like to express my gratitude to the Libyan Ministry of Education for partially sponsoring my PhD.

I would like to thank all members of the Nano Research Group for their assistance and kindness over the past four years. I would like to thank Dr. Ehsan Jaberansari for his help and assistance in the design and simulation of the n-ZnO/p-Si optical switch. I would also like to thank Dr. Suhana M. Sultan for her assistance, in using Silvaco ATLAS, with photolithography recipes, and with ZnO deposition and etching. I would also like to thank her for her assistance in using characterisation tools such as the MEMS prober and the Hall measurement system. I would like to thank Dr. Marek E. Schmidt for training me on the Nanonics AFM system and on the rapid thermal annealers, and also for helping me using the focused ion beam (FIB) system. I would like to express my gratitude to Dr. Owain Clark for his help and assistance in training me on several tools in the cleanroom and his patience and unconditional support in answering my questions regarding etching, deposition and characterisation of thin film properties. I also thank him for introducing me to the design of experiment (DoE) principle. I would also like to express my appreciation to Dr. Kian S. Kiang for his help and assistance in training me on several tools in the cleanroom and his patience and unconditional support in answering my queries and helping me develop recipes for photolithography processing. I would also like to thanks him for developing the initial recipe used for planarising the HWCVD poly-Si films. I would also like to express my gratitude to Mr. Zondy Webber for his extraordinarily help with carrying out e-beam lithography. I would like to express my greatest gratitude to Dr. Antulio Tarazona and Dr. Maria Theresa G De Leon for their help with the deposition and characterisation of HWCVD films. I would like to also thank Dr. Stuart Pearce for his help with fabricating a 1550 nm beam splitter and for his technical support with the evaporation tools, in particular the BAK 600. I would like to thank Mr. Peter Ayliffe, Mr. Jim Farmer, and Mr. Michael G. Perry for their technical assistance inside the cleanroom. I would also like to thank Dr. Milan Miloevi, Dr. Milos Nedeljkovic, Dr. David Thomson, Dr. Frederic Gardes, Dr. Nathan Owens, Dr. Youfang

Hu, and Dr. Goran Mashanovich for their helpful input and assistance with polishing and optical characterisation of silicon waveguides. The author would also like to express his gratitude for the help of Oxford Instruments, especially Thomas Sharp, Saleem Shabbir, Robert Gunn and Owain Thomas, who allowed the use of their equipments at a critical time of this project. I would like to thank all those who assisted me through my PhD but were unintentionally not mentioned in this humble acknowledgement.

Finally, I would like to thank my wife, parents, siblings, and all family and friends for their unconditional support and belief. This work would have not been possible to accomplish without the sacrifice of those closest to me.

To Libya

Nomenclature

α	Absorption coefficient
β	Propagation constant
ϵ_0	Permittivity of free space
λ	Wavelength
$\mathcal{E}_z$	Electric field component in the z direction
$\mathcal{F}$	Finesse
$\mathcal{H}_x$	Magnetic field component in the x direction
$\mathcal{H}_z$	Electric field component in the y direction
$\mathcal{H}_z$	Magnetic field component in the z direction
μ_e	Mobility of electrons
μ_h	Mobility of holes
ω	Angular frequency
ψ	Phase of the electromagnetic wave
θ_c	The critical angel
$\vec{P}$	Polarisation of the dielectric
a_E	Asymmetry factor for the TE mode
a_M	Asymmetry factor for the TM mode
b	Normalised guide index
d_E	Effective waveguide thickness
g	Damping coefficient
h_1	Transverse component of the wavevector in the guiding medium
k	Wavenumber
k_B	Boltzmann constant

m^*	Effective mass
n	Refractive index
N_A	Acceptor concentration
N_D	Donor concentration
n_e	Concentration of free electrons
n_h	Concentration of free holes
q	Electron charge $= 1 \times 10^{-19}$ C
T	Temperature
V	Normalised frequency and waveguide thickness
V_{bi}	Built-in voltage
TE	Transverse electric field
TM	Transverse magnetic field

Chapter 1

Introduction

1.1 Electrical and Optical Interconnects

For decades, microprocessor performance increased in accordance with Moores law. However, a performance wall was hit in the mid-2000 primarily due to excess waste heat that could not be dissipated within a single microprocessor chip [1]. The solution was to manufacture multiple processor cores that offered increased performance speed while maintaining acceptable waste heat level. Although performance is ultimately constrained by the external memory system, large bandwidth data links are required to increase the number of bytes transferred between multiple cores and the external memory. Current microelectronic industry utilises copper as a primary interconnect medium. However, as the demand for high-density interconnect increases, fundamental physical limitations of copper start to emerge [2]. For instance, electrical interconnects suffer from dispersion, cross-talk, and signal reflections as the bandwidth increases [3]. Hence, alternatives which are more immune to these effects have been investigated. One candidate has been optical links due to their capabilities to carry large bandwidth data with minimum cross-talk and dispersion. One of the optical materials considered for waveguide interconnects and data communication is silicon. Silicon is transparent at the telecommunications wavelength and is compatible with the CMOS fabrication process. Moreover, high-density waveguides can be realised using silicon due to the high contrast in refractive index between silicon and its claddings.

1.1.1 Challenges and Desired Performance of Optical Links

Long distance optics uses discrete components that are impracticable for dense interconnects, [3]. Optical devices must be integrable in a single silicon chip to provide density requirements for inter/intra-chip interconnects. The integration of optical interconnects with integrated electronics combines the high-performance computations capabilities of integrated electronics with the high-performance communication capabilities of integrated photonic circuits [1]. This fact implies that optical links and associated components must be made of materials that are compatible with silicon electronics. Furthermore, optical interconnects must meet future technology targets in order to replace copper wires. Optical links are already capable of supporting high

communication bandwidths [1]. Unlike copper wires, they are also characterised by low loss at high frequencies. Yet, power consumption targets for future CMOS chips may present a formidable challenge for both technologies. According to *Miller*, the total allowed energy consumption should be 97 fJ for the entire off-chip interconnects by 2015; this figure should fall to approximately 34 fJ by 2022 [4]. The author assumed that off-chip interconnects consume 20 of the total system energy per bit and bases/ed his calculations on the International Technology Roadmap for Semiconductors (ITRS). The corresponding on-chip interconnects power targets are expected to be five times smaller than off-chip interconnects. Hence, energy requirement for on-chip interconnects is estimated to be approximately 40 fJ per bit by 2015; whereas for the ITRS 2022 chip, the figure drops to only 4 fJ per bit. These figures restrict the consumption of an active electro-optic device to only 10 fJ per bit by 2015.

High energy consumption rates can be counter-balanced by the advantages that optical interconnects bring [3]. Moreover, current electrical interconnects already consume energies that are ten times higher than the energy targets demanded from their optical counterparts [4]. However, it could be argued that potential gains of adapting optical interconnects for on-chip and off-chip application can be further enhanced if optical interconnect technology is allowed to mature to the level of electrical interconnects technology. This requires that optical interconnect technology to be introduced to commercial applications so as to drive the development of such a technology. The extreme introduction costs of optical interconnects hinder its commercialisation as compared to the inexpensive electrical interconnects.

1.1.2 Materials for Electro-Optical Devices

For long-haul communications, several semiconductor materials have been exploited to realise functionalities needed for active optical devices. For example, Lithium Niobate (LiNbO3) is frequently used to make optical modulators due to its large electro-optic coefficients. Similarly, GaAs, which is a III-V compound, and its related alloys constitute the majority of semiconductor lasers due to their direct band gap that can be easily engineered by controlling the composition of GaAs alloys [5]. Photodetectors are also dominated by III-V compounds for the same reasons.

Silicon has received a growing interest from the integrated optics community to replace short-reach interconnects and form an all-optical communication link comprising a laser source, optical modulator, optical propagation medium (waveguide), and detector in a single chip. Recently, active materials, such as ITO and graphene, have been incorporated into the silicon photonics technology to either realise new capabilities or improve the existing performance of silicon photonics devices. The focus of these hybrid devices have primarily targeted active silicon photonics devices such as lasers, modulators, and detectors. Zinc oxide (ZnO) is another semiconductor material that has yet to be explored as part of a silicon photonics platform. In this project, ZnO was used to form a hybrid n-ZnO/p-Si electro-optical switch.

1.2 Silicon Photonics

The interest of using silicon as an optical material stems from its good optical properties around the telecommunication wavelengths, and the advanced silicon fabrication technology. Besides,

the use of silicon offers direct integration route for optical and electrical integrated circuits; thus, reducing the cost of fabrication and development. This is arisen by the fact that the most successful microelectronic technology (CMOS) is based on silicon. Due to the relatively high refractive index of silicon ~ 3.5 at wavelengths above 1100 nm, light confinement can be realised in a submicron cross-sectional dimensions. Therefore, high density silicon optical interconnects can be fabricated on chip. Although some non-silicon optical materials are compatible with CMOS technology and can offer greater optical advantages than silicon, integrating them within silicon platforms induces higher costs that may not be justified [6].

1.2.1 Optical Switches

Lithium niobate (LiNbO3) has been the conventional material used to realise photonic modulators due to its large linear electro-optic coefficient. However, linear electro-optic (Pockels) effect is absent in silicon due to its centrosymmetric crystalline structure. Despite the fact that Pockels effect can be artificially induced by using strained silicon, the effect is weak compared to other materials [7, 8]. Moreover, the Kerr effect and the Franz-Keldysh effect can also be induced in silicon by application of a large electric field [2]; albeit these are relatively weak at the telecommunication wavelengths. It is widely established now that the plasma dispersion effect, where a change in the free carrier concentration alters the refractive index of a material, can offer high speed efficient silicon-based modulators.

According to Drude-Lorentzs equation, perturbation of the concentration of free carriers leads to differential changes in the real and imaginary refractive indices of a material. A change in the imaginary part of the refractive index can be used to make electro-absorption modulators, where the intensity of the propagating light mode is directly reduced [5]. On the other hand, a change in the real part of the refractive index affects the phase of the propagating mode. Phase change can be translated into intensity modulation by using optical interference devices such as Mach-Zehnder (MZI), ring resonators, and Fabry-Perot interferometers. Nonetheless, sufficient phase-shift in silicon MZI devices tend to require extended active lengths (i.e. $l \simeq 3$ mm) [9, 10]. Similarly, silicon microring and microcavity based switches are susceptible to thermal effect [2].

To overcome these issues and realise added functionality, transparent semiconductors and conductors have been considered as one of the solutions [11]. An obvious advantage of some transparent semiconductors, such ITO and ZnO, is their low thermal budget; a requirement that current all-silicon optical modulators are unable to address effectively.

1.3 Transparent Semiconductor: Zinc Oxide for Electro-Optical Waveguide Applications

As a semiconductor with a wide band gap (~ 3.3 eV at 300 K) and excellent transparency over a broad range of wavelengths ($\Delta\lambda \simeq 390 - 2500$ nm), zinc oxide (ZnO) can be integrated into silicon photonics platforms to realise new functionalities. Particularly, ZnO can be used to form the n-type part of a p-n junction [12]. With the application of atomic layer deposition (ALD), ZnO can be coated over silicon waveguides to form a n-ZnO/p-Si heterojunction. Due to its

refractive index ($n \simeq 1.92$), ZnO can act as a cladding material similar to that provided by SiO_2. Moreover, ZnO is naturally n-type doped and the concentration level depends on the deposition technique . Hence, no complex ion implantation is needed to form the n-type region of p-n silicon optical modulators.

Passive and active optical devices based on ZnO have demonstrated at the visible wavelengths [13, 14, 15, 16]. However, there have been limited investigations into optical devices employing ZnO at the telecommunications wavelengths, in particular at a wavelength of 1550 nm.

As a naturally n-type doped material, ZnO has been used to realise heterojunction devices with silicon [17, 18]. Because of high transparency (80%) of ZnO at the telecommunications wavelengths and its excellent electrical properties, it can be integrated with silicon to fabricate a n-ZnO/p-Si heterojunction optical modulators operating at a wavelength of 1550 nm.

An advantage of using ZnO is the possibility of depositing high quality ZnO films at low temperatures using Atomic Layer Deposition (ALD) [19]. Finally, ZnO is compatible with CMOS technology for future CMOS-SiP integration [20].

1.4 Multi-Layered Silicon Photonics

Silicon on insulator (SOI) has been the dominant development platform for silicon photonics technology due to its low optical propagation loss. However, SOI is limited to lateral integration of photonics and electronics components. Vertical integration of photonic devices is usually performed through direct deposition of amorphous or polycrystalline silicon layers [21, 22, 23, 24]. Multi-layered integration is desirable because of several advantages such as reduced chip size, improved thermal isolation, and the possibility of integrating SiP with CMOS technology as shown in Figure 1.1. Recently, there has been an increased interest in polysilicon waveguides due to their low cost and added design flexibility [21, 22, 23, 24, 25, 26, 27, 28]. Amorphous silicon (a-Si) has also received interest because of its absorption loss and non-linear properties [29].

However, most of the reported polysilicon films were deposited or post-treated at high temperatures ($\geq$ 900 °C), e.g. [21, 24, 25, 26, 27, 28]. This high temperature may not be suitable for multilayer integration and back-end fabrication processing [30] 1.1.

We propose to use polysilicon waveguides with low thermal fabrication budget achieved using hot-wire chemical vapour deposition (HWCVD) method. The HWCVD method has been widely studied and used to fabricate solar cells. However, no work in the SiP technology has utilised this deposition method to realise poly-Si and a-Si optical devices.

The challenge with poly-Si and a-Si films used in the SiP technology is to improve their electrical and optical properties. This requires optimising the deposition recipes as well as developing low-temperature post-processes that can improve the electro-optical properties of poly-Si and a-Si films. A future multi-layered SiP system will probably combine poly-Si and a-Si waveguides according to functionality. While poly-Si exhibits superior electrical properties to a-Si, it also induces greater absorption loss. On the other hand, a-Si induces a relatively low absorption loss but it has inferior electrical properties to poly-Si.

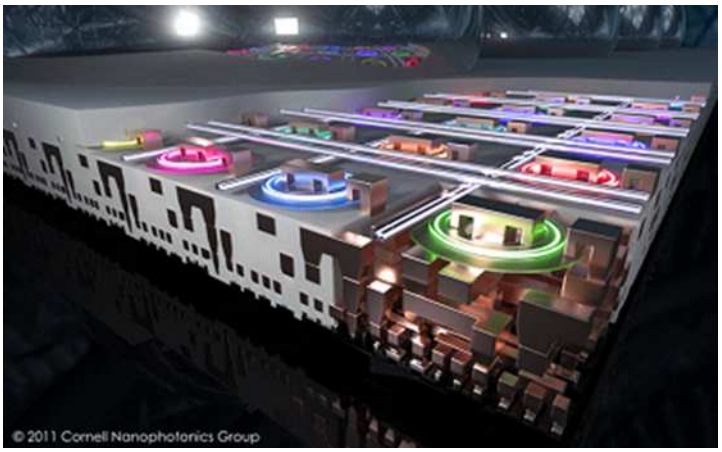


FIGURE 1.1: 3D schematic illustrating the proposed back-end integration of SiP with CMOS technology [31]

1.5 Research Objectives

This project aims to explore silicon photonics-compatible materials with low fabrication thermal budget. Ho et al. proposed a conservative thermal budget of 90 minutes at 450 °C [32]. In this project, the thermal budget limit was defined to be 90 minutes at 400 °C. Low temperature processing of silicon photonics devices is a requirement for CMOS back-end integration. The first primary aim of this project is to explore the advantages offered by integrating ZnO on silicon waveguide structures and demonstrate optical switching. To achieve the hybrid ZnO-Si waveguide devices, the following objectives have been investigated:

1. Develop a silicon-based optical modulators using low temperature processes.
2. Reduce fabrication complexity by eliminating silicon n-type doping.

The second primary aim of the project is to research the feasibility of realising low-temperature deposition and low optical loss poly-silicon waveguides. In order to realise this aim, the following objectives have been investigated:

1. Deposit poly-silicon film at low temperatures.
2. Fabricate low-temperature, single-mode poly-silicon waveguides.
3. Characterise the optical propagation loss of the poly-silicon waveguides.
4. Improve the propagation loss of the poly-silicon waveguides.

1.5.1 Achievements

The following objectives have been accomplished in this project:

1. Demonstrate the first heterojunction zinc oxide silicon-based optical switch.

2. Demonstrate the lowest optical propagation loss for poly-silicon waveguides deposited at $< 400\,^{\circ}\mathrm{C}$ by hot-wire chemical vapour deposition.

1.6 Report Structure

This thesis report is organised as follows. Chapter 2 offers a detailed literature review on silicon photonics modulators and the electrical/optical properties of ZnO. Chapter 3 provides an introduction and theoretical background to integrated optical waveguides and p-n junctions. Chapter 4 presents electrical and optical simulations on hybrid n-ZnO/p-Si Fabry-Perot and electro-absorption modulators. Chapter 5 presents a background on the ALD process and the optimisation procedure of ZnO thin films. Chapter 6 presents the fabrication process and electrical/optical characterisation of a hybrid n-ZnO/p-Si Fabry-Perot and electro-absorption modulators. Chapter 7 introduce the development process and characterisation of low loss, and low-temperature deposited poly-silicon waveguides using hot-wire chemical vapour deposition (HWCVD). Finally, Chapter 8 provides an insight into future related work on the use of both ZnO and poly-silicon in a multi-layered silicon photonics platform.

Chapter 2

Literature Review

2.1 Introduction

The *silicon photonics* technology has witnessed major milestones in the past few years. Most of the research in silicon photonics has focused on silicon-based optical switches. One focus of this project is also to develop a low-temperature silicon-based optical switch. In this chapter, significant and recent research in the development of fast and efficient silicon optical switches will be reviewed. Moreover, silicon photonics based on depositable materials, such as poly-silicon, has recently attracted the focus of some silicon photonics research groups. Deposited silicon photonics offers the possibility of developing multi-layered silicon platforms whereby many 3D design structures can be developed. Multi-layered silicon photonics also facilitates its integration with the contemporary CMOS technology. This chapter also focuses on recent development in deposited passive and active silicon photonics devices.

The state-of-the-art silicon optical switches have utilised sophisticated fabrication processes to enhance their performance. For example, lateral implantation, which has extremely low alignment tolerance, has been used to optimise the doping process of recent p-n junction based silicon optical switches [10]. Furthermore, high-temperature processing has been used almost universally to fabricate silicon optical switches. Materials such as zinc oxide (ZnO), deposited by atomic layer deposition (ALD), can offer the opportunity of developing silicon-based optical switches at low temperature. Similar high-temperature processing have been used by research focusing on depositable silicon photonics. In fact, most of the research achievements in passive poly-silicon waveguides have relied upon high temperature processing to lower the propagation loss of poly-silicon/amorphous-silicon waveguides. High-temperature processing is not currently compatible with CMOS back-end integration.

The first section of this chapter outlines the performance measures used to compare different silicon optical switches. Then, section 2.3 reviews the most significant and recent research achievements in silicon photonics switches. After that, section 2.4 reviews recent research into depositable silicon photonics passive and active devices. Finally, section 2.5 gives a brief review of zinc oxide's material properties and its applications.

2.2 Performance Parameters for Silicon Optical Switches

Electro-optical switches can be compared and assessed in terms of a number of performance metrics, namely [2]:

1. Speed or bandwidth (GHz or Gb/s).
2. Modulation depth of extinction ratio (dB/μm).
3. Power consumption (efficiency) (fJ).
4. Footprint or size (μm).

The speed of modulation is normally considered as the principal quality factor when comparing different modulators. Furthermore, modulation speed is bounded by conventional limits that define modulation bandwidth, which is characterised by the cut-off frequency or the -3dB point at which the amplitude of the propagating signal drops to 50% of its maximum value. Moreover, another important characteristic is the extinction ratio which is defined as the ratio of the output intensity of a modulator, when it is configured for maximum transmission , to the output intensity, when the modulator is configured for minimum transmission . The extinction ratio can be expressed as [33]:

$$\text{ExtenctionRatio}(\text{dB.s}^{-1}) = 10 \times \log_{10}\left(\frac{I_{out}}{I_{in}}\right) \tag{2.1}$$

It is clear that high extinction ratios are desirable to enhance the signal to noise ratio (SNR); the difference in optical power between a 1 and 0 signals must exceed the error margin at the receiving end. Moreover, power consumption is increasingly gaining significance in the silicon photonics community. As discussed in Chapter 1, optical interconnects systems must consume less energy than their electrical counterparts. According to Miller, the ITRS roadmap, device energy target should be approximately 10 fJ per bit by 2022 [34]. Furthermore, the optical power lost as a result of adding an electro-optical device to a system is termed the optical insertion loss (OL). This figure considers the overall loss including absorption, scattering, mode-coupling losses, and reflection. It is expressed in decibels as [35]:

$$\text{Opticalloss} = 10\log_{10}\left(\frac{I_{out}}{I_{in}}\right) \tag{2.2}$$

Footprint refers to the area occupied by a device on a chip. Smaller devices lead to higher integration density and less energy expended per bit. Nonetheless, decreasing the size of a device may compromise other characteristics, particularly the modulation depth or the extinction ratio [33]. The aforementioned metrics are generic and can be used to characterise any type of electro-optical modulators. However, the product $V_\pi L_\pi$ is normally quoted for the efficiency of Mach-Zhender devices; where V_π refers to the required bias voltage to achieve a π phase shift along a modulator length of L_π. For superior efficiency, the $V_\pi L_\pi$ product should be minimised [35].

2.3 Review of Silicon-Based Optical Switches

2.3.1 Electro-Absorption Modulators

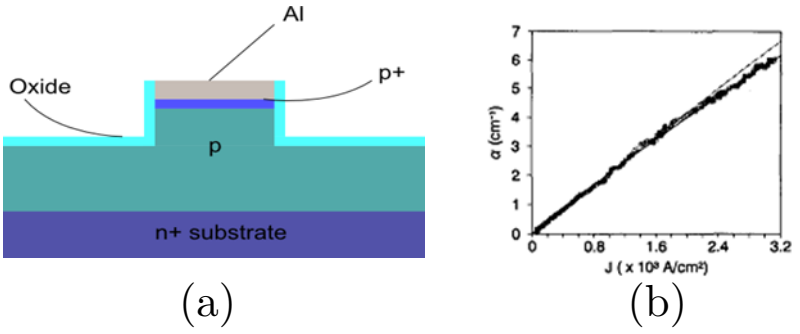


FIGURE 2.1: (a) cross-section view of the electro-absorption optical switch reported by Treyz, May, and Halbout [36]. (b) absorption-coefficient versus current density for an active length of 500 μm and width of 24 μm

The first silicon electro-absorption optical switch was reported by Treyz, May, and Halbout [36]. The design was based on a vertical *p-i-n* diode. Figure 2.1 (a) shows a cross-section layout of the optical switch. SiO_2 was deposited to act as a cladding layer. The authors reported a modulation depth of 6.2 dB at $\lambda = 1300$ nm and a response time of approximately 50 ns which corresponds to 20 MHz bandwidth. Carrier change resulted from injecting carriers from the heavily doped regions to the intrinsic p-type region under forward bias conditions. Figure 2.1 (b) shows the relationship between the applied current density and the change induced in the absorption coefficient. It is clear that the change in the absorption coefficient increases linearly with increased current density. However, the reported current density of 3×10^3 A/cm^2 causes significant power dissipation which makes this device impractical. It is thought that the high current density is due to the large cross-section dimensions of the modulator which also results in supporting multiple optical modes. In addition, the optical loss was expected to be high due to the reduced vertical confinement.

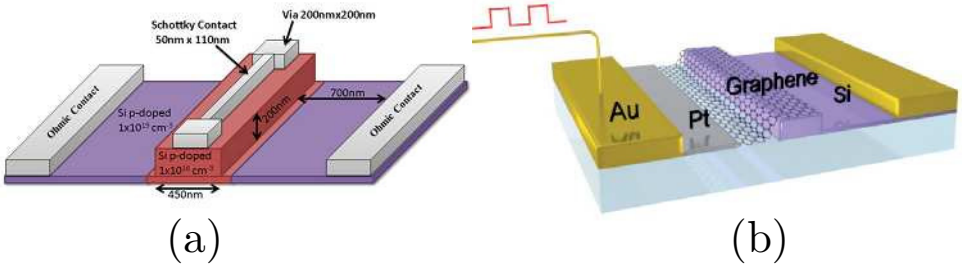


FIGURE 2.2: (a) a perspective view an electro-absorption optical switch based on Schottky diode as reported by Elshaari and Preble [37]. (b) a perspective view an electro-absorption optical switch employing a graphene overlayer as reported by Liu et al. [38].

Elshaari and Preble proposed an absorption modulator based on a Schottky diode [37]. Figure 2.2 (a) shows a 3D view of the proposed design. The device had an active length of 100 μm, a width of 450 nm, a height of 250 nm of which 50 nm was reserved for the rib. The active region of the waveguide was lightly doped ($n_h = 1 \times 10^{16}$ cm^{-3}); while the ribs were heavily doped

($n_h = 1 \times 10^{19}$ cm^{-3}). A Schottky contact ($\sim$ 50 nm wide) was connected to the top of the active region. Two via contacts were placed at the start and the end of the modulator to allow for electrical contact with the Schottky gate. Two ohmic contacts were placed on the heavily doped ribs. Interestingly, the device employs injection and depletion modes for its operation. The OFF state is characterised by negligible absorption achieved by reverse biasing the diode, i.e. depletion mode. On the other hand, the ON state is represented by change in the value of the absorption coefficient achieved by forward biasing the junction, i.e. injection mode: the voltage was swung between $\pm$1.25 V. The authors claim a modulation depth of 4.6 dB at 10 Gb/s. In addition, the reported insertion loss was 2.98 dB and the carrier concentration change was $N_h \simeq 1 \times 10^{19}$ cm^{-3}. Since the device is not interference-based, it has a large operating bandwidth $\sim$ 100 nm. Moreover, the device is based on single carrier change in the active region. Hence, free carrier recombination is eliminated and the speed of the device is expected to only be limited by the RC constant of the device. However, the reported results are only valid for TE polarisation. Furthermore, because of the sub-micron waveguide dimensions, scattering loss becomes more pronounced: the authors claim that scattering loss is negligible and hence it was not accounted for in the total insertion loss. In addition, the results merely rely on simulations and no real device was made to confirm the low loss claims reported by the authors. The change in the absorption coefficient was not stated. Furthermore, as a consequence of employing a Schottky diode, the device draws more current than normal p-i-n based modulators.

Recently, a hybrid-silicon electro-absorption modulator was demonstrated by Liu et al. [38]. The device structure is shown in Figure 2.2 (b). A monolayer of graphene was deposited using CVD and then mechanically placed on top of a silicon waveguide. The graphene and silicon are electrically isolated by a 7nm-thick layer of aluminium oxide (Al_2O_3). In order to reduce the sheet resistance of graphene, a platinum electrode was positioned only 600 nm away from the travelling mode. The modulator works by suppressing and allowing interband transitions in graphene by manipulating the Fermi level of graphene. The authors claim a modulation speed of 1 GHz, only limited by the RC constant of the device. The device also exhibited a broadband operation range between $1350 - 1600$ nm. In addition, the total footprint of the device was only 25 μm^2 with a modulation depth of 0.1 dB/μm for a voltage swing of 4 V. The insertion loss is negligible as the transparency of graphene at 1550 nm is around 97.5% [38]. However, the fabrication of this device is still not compatible with CMOS fabrication due to the mechanical transportation of the graphene layer. Moreover, the electrode connected to graphene must be close to the active area to reduce the sheet resistance: close metals may induce high absorption loss. The device is polarisation-sensitive and the mode has to travel mostly in the top and bottom of the waveguide to ensure optimal mode overlap with the graphene layer. This condition may not be easy to meet in real circuits and it may not ensure minimum propagation loss in the rest of the waveguide.

A similar device was proposed by [11]. Instead of using graphene, indium-tin-oxide (ITO) was used as the absorptive medium. The device adopted a MOS-capacitor structure as shown in Figure 2.3. The silicon strip waveguide (width = 800 nm, height = 340 nm) was coated with a 10 nm thick layer of ITO. Then, the ITO was coated with a 20 nm thick SiO_2. Finally, gold was deposited on top to form the gate electrode. For a voltage swing of 4 V, the device exhibited a modulation depth of 1 dB/μm with a broadband wavelength range ranging between $1200 - 2200$ nm. Since the modulation depth is high, the total device length was only 5 μm. However, the

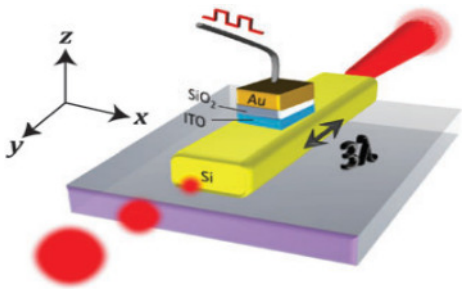


FIGURE 2.3: A 3D schematic of the hybrid silicon optical switch employing ITO as an absorptive medium [11].

insertion loss was extremely high 2×10^3 dB/cm. The authors did not report the modulation speed of the device but expect it to reach 1 THz if the RC time constant was not considered. Nevertheless, in order to optimise the light-matter interaction and reduce loss, the cross-sectional area had to be large. Moreover, the effect of the metal contact on the propagating mode was not analysed quantitatively.

The majority of electro-absorption switches require a metal region in a close proximity to the waveguide's core to improve efficiency. The proximity of metals to the optical mode does not only induce additional absorption loss, but can also prompt another modulation effect: namely the thermo-optic effect. The thermo-optic effect is produced by heating a silicon waveguide and is known to be $\mathrm{d}n/\mathrm{d}T = 1.86 \times 10^{-4}$ K^{-1} [33, 39]. If the current passing through a p-n junction based electro-absorption modulator was high, there is a strong possibility of heating the silicon core and thus producing the thermo-optic effect at low frequencies (< 1 MHz).

2.3.2 Electro-Refraction Modulators

Interferometric structures depend on constructive and destructive interference of light to achieve modulation. Interference effects occur when a phase difference $\Delta\phi$ exists between two waves, with the same frequency and comparable amplitudes. An interferometer splits the light, at its input, into two beams which experience different phase shifts. The two beams are then allowed to interact to produce intensity modulation. If I refers to the intensity of a light beam, the interference equation of two coherent beams I_1 and I_2 is given by [40]:

$$I = I_1 + I_2 + 2\sqrt{I_1 I_2}\cos(\phi) \tag{2.3}$$

where ϕ is the phase difference between the two beams. The phase difference is directly proportional to the refractive index difference:

$$\phi = \frac{2\pi L \Delta(n)}{\lambda_0} \tag{2.4}$$

$$I = 2I_0\left[1 + \cos\left(\frac{2\pi\Delta(n)}{\lambda_0}\right)\right] \tag{2.5}$$

Hence, for $\lambda = 1550$ nm and $L = 1000\,\mu$m, a refractive index change of $\Delta n = 1.55 \times 10^{-3}$ can result in a phase shift of 2π.

2.3.2.1 Mach-Zehnder Interferometer (MZI)

The majority of silicon optical modulators are based on travelling-wave Mach-Zehnder interferometers. An external stimulus, which results in a change in the optical properties of modulator material, is applied to one arm of the modulator. The stimulus can be an electric field, a magnetic field, an acoustic wave, or temperature. Indeed, Mach-Zehnder interferometers are normally used as benchmarks. An important characteristic, called the figure of merit, indicates the efficiency of optical modulators. The figure of merit is the product of the applied voltage (V) by the active length (L) of the modulator such that the induced phase difference between the two arms is π.

Soref and Bennett proposed the first silicon optical modulator based on the plasma dispersion effect [41]. An interaction length of less than 1mm was required to produce radian phase shift. The authors report an optical loss of less than 1 dB at a wavelength of 1300 nm. It is interesting to note that the waveguide had submicron dimensions. It is claimed that sub-micron waveguide dimensions ensure maximum carrier change within the active region with minimal applied voltage. Although the proposed device was not realised, it demonstrated the desire to have sub-micron waveguide dimensions. Indeed, there has recently been an observable trend towards smaller waveguide dimensions, especially after the significant advances in sub-micron fabrication processes. Sub-micron waveguide structures increase the switching speed of depletion-based modulators because they generally have smaller RC constant than those of large waveguide modulators [10].

An important milestone for silicon optical modulators was achieved in 2004 by Liu et al., where researches experimentally showed modulation speed in excess of 1 GHz [42]. A schematic diagram of the cross-section of the modulator is shown in Figure 2.4. The proposed modulator is based on metal-oxide-semiconductor (MOS) structure. Unlike injection and depletion, the free carriers are accumulated around the capacitor formed by the gate oxide. An asymmetric MZI (2 mm-long) was used to achieve optical modulation. Although modulation speeds in excess of 1 GHz were demonstrated, the modulator had a large insertion loss (6.7 dB). Moreover, due to the horizontal oxide layer, the modulator was polarisation-sensitive and only supported TE mode. As modulation speed surpassed the 1 GHz threshold, attention was shifted to the reduction of power consumption. Xia et al. presented a high-speed modulator (10 Gb/s) with power consumption of merely 5 pJ/bit [43]. The high speed and low energy can be attributed to the small waveguide dimensions. The authors reported a figure of merit of 3.6 V.cm for an active length of 200 μm.

Watts et al. attempted to optimise the waveguide's structure to maximise the plasma dispersion effect in sub-micron modulators [44]. They noted that change in the refractive index is more pronounced for small cross-section dimensions and that vertical p-n junction is easier to fabricate. Figure 2.5 illustrates the cross-section of the modulator. It is interesting to note the unique doping profile of the central region where the optical mode should be confined. Moreover, this device operated in the depletion mode and achieved a figure of merit of 1 V.cm: a significant improvement over the previous device. The modulation speed, obtained in a active length, was 10 Gb/s.

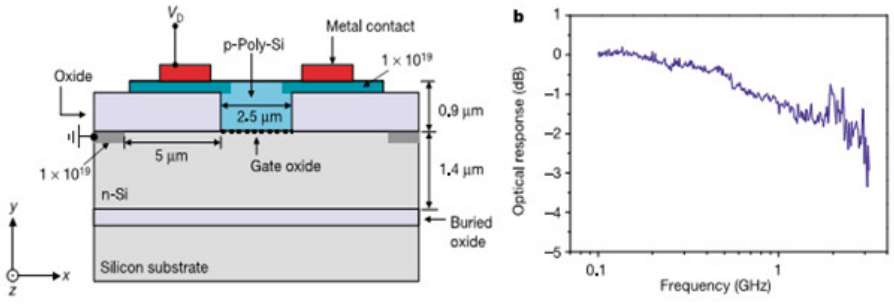


FIGURE 2.4: (a) A schematic view of the cross-section of the first > 1 GHz silicon optical modulator. The electrical structure implements a MOS structure. (b) Optical response of the device as a function of frequency [42].

MZI normally require a large interaction length to achieve acceptable modulation depth. Jiang et al. suggested that the use of Photonic Crystals (PC) can increase the value of the propagation constant by 100 times based on slow-light technique. Thus, interaction length of MZI is reduced by the same factor [45]. Indeed, the authors presented a MZI modulator with an interaction length of only 80 μm and a modulation depth of 92%.

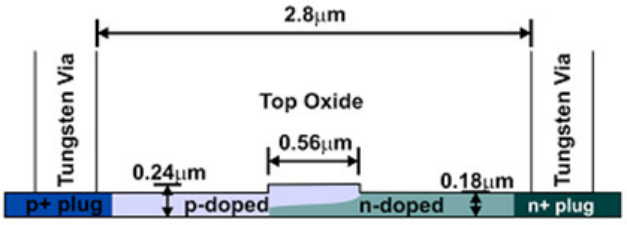


FIGURE 2.5: Schematic diagram of the proposed vertical p-n junction [44].

Nguyen et al. improved the use of PCs structures to attain modulation speed of 10 Gb/s in a 200 μm-long MZI modulator: the corresponding figure of merit was 0.028 V.cm [46]. To achieve a high speed operation, the drive signal was pre-emphasised. The reported figure of merit represented an improvement of at least an order of magnitude over previous MZI modulators. It is worth noting that the device operated in the depletion mode.

2.3.2.2 Bragg Gratings and Fabry-Perot Modulators

Cutolo et al. presented an all-silicon optical modulator based on Bragg grating design [47]. The modulator design comprises a p-i-n diode integrated with a Bragg grating with a period $\Lambda = 227$ nm. The modulator operated in the injection mode and was assessed in terms of MZI modulators' performance characteristics. The authors reported a 3 dB extinction ratio for a 3.2 mm long active length. The study concluded that Bragg grating structure can offer more power-efficient alternatives to the more common MZI modulators. Nonetheless, the modulator offered no improvement in the footprint over MZI modulators. Two Bragg gratings can be utilised to form the two partially reflective mirrors in Fabry-Prot resonators. Liu and Chou presented a

silicon optical modulator based on Fabry-Prot resonator structure [48]. Figure 2.6 (a) illustrates the modulator structure. The trenches' width was 145 nm, while the ridge width was 115 nm. The RC time constant, which determines the modulation speed, was 15 ps when the cavity was 10 μm wide and 18.3 μm long. Theoretical analysis showed that the cavity can have large sensitivity to carrier change. For example, a carrier change of $\Delta n = 1\times10^{18}\,\mathrm{cm}^{-3}$ results in 100% modulation depth for the same aforementioned dimensions. Furthermore, the authors suggested that sub-micron dimensions for the waveguide can lead to a better performance. Nonetheless, although reducing the active length lead to faster switching times, it also reduces the modulation depth substantially.

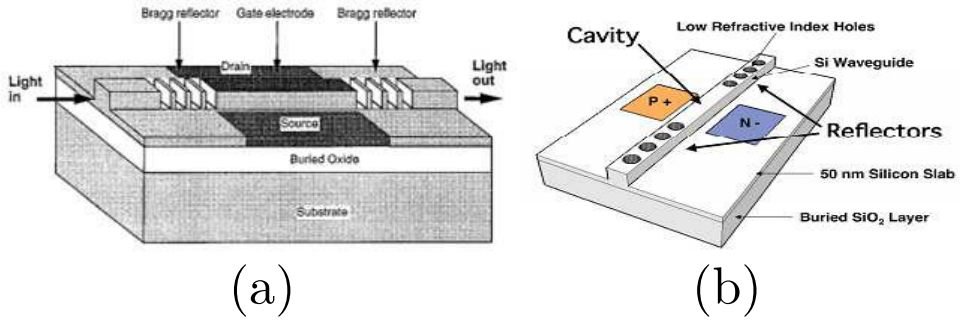


FIGURE 2.6: (a) Schematic view of the proposed Fabry-Perot modulator. The structure comprises two Bragg reflectors [48]. (b) Schematic of the Fabry-Prot modulator where holes were used instead of trenches [49].

proposed a compact Fabry- Prot modulator where conventional Bragg grating trenches were replaced with holes [49]. A schematic view of the modulator is shown in Figure 2.6 (b). The holes had a diameter of 220 nm and a periodic spacing of 420 nm. The total length of the modulator was only 6 μm of which 2.51 μm forms the cavity. The device achieved a speed of 300 MHz with a modulation depth of 6.6 dB. Although the device footprint was impressively small, the modulation speed was relatively slow.

The desire to minimise the footprint of silicon modulators encouraged researchers to consider different optical structures. Xu et al. proposed a p-i-n modulator integrated with a ring resonator, as shown in Figure 2.7 (a) [50]. The diameter of the ring was 12 μm , and the width of both the waveguide forming the ring and that coupling to the ring was 450 nm; whereas the height was 250 nm. The distance separating the ring from the coupling waveguide was . The device was operated in injection mode. The authors reported a 15 nm free-spectral range. The measured insertion loss was 9 dB. The transmission spectra of the modulator are illustrated in Figure 2.7 (b). The blue shift shown in the figure is due to the injection of carriers into the intrinsic region whereby the refractive index decreases. Using return-to-zero RZ signal with 6.9 V peak-to-peak voltage and 12 μm active length, the device was able to modulate information at 1.5 Gb/s. The modulation depth was 15 dB. Nevertheless, the bandwidth of the modulator was only $\Delta\lambda = 0.4$ nm, which is significantly smaller than bandwidths achieved by MZI structures. Furthermore, ring-resonator modulators are vulnerable to temperature variation and require temperature stabilisation units; hence compromising their operation high efficiency [33]. However, the design was later optimised to achieve modulation speed of 12.5 Gb/s for a ring diameter of 5 μm.

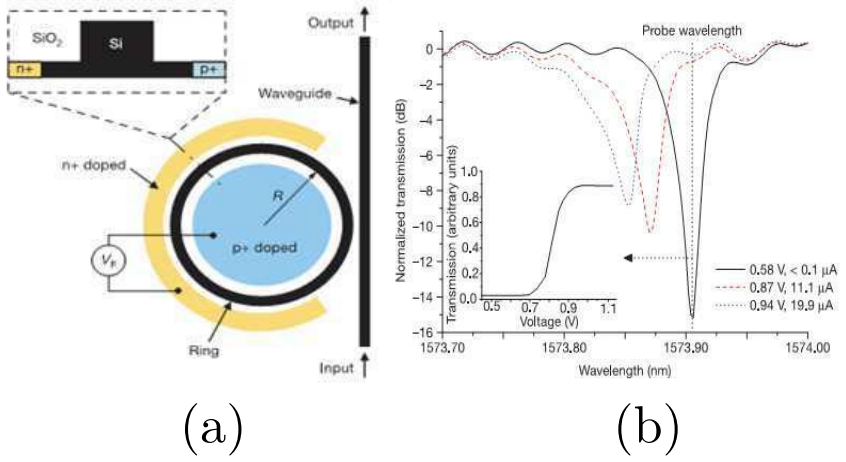


FIGURE 2.7: (a) Schematic diagram of the ring-resonator-based modulator. SEM top view of the ring-resonator [50]. (b) Transmission spectra of the ring resonator at different forward bias voltages. The inset shows the transmission as a function of applied voltage [50].

In order to increase the available bandwidth of ring-resonator modulators, Xu proposed a dual-ring resonator structure [51]. The device layout is shown in Figure 2.8. Because of the symmetry of the circuit, only one diode is forward biased at any moment; the other is reverse biased. When D1 is forward biased and D2 is reverse biased, the two rings have the same resonant frequency. However, as carriers are displaced from D1 to D2, the resonant frequencies of the coupled rings shift in opposite direction resulting in optical modulation. Since carriers are merely displaced from one diode to another, the switching speed can be considerably high. Indeed, with the use of pre-emphasis scheme, the authors reported a switching speed of 40 Gb/s. In order to compare ring resonator-based modulators, the authors noted that resonance tuning is proportional to the power consumption. They also define a unitless figure of merit (FOM) based on the ratio of the optical bandwidth to the resonance tuning. For the same bandwidth of 0.16 nm, single ring modulator has FOM = 0.17; while the dual-ring modulator has FOM = 0.53. Despite being efficient, small, and sensibly fast, the ring modulator was sensitive to temperature fluctuations. Although the authors did not report the sensitivity of the ring resonator to temperature fluctuations, it is normally in the range of $30 - 80\ \mathrm{pmK}^{-1}$. In addition, the operational bandwidth offered by ring modulators is considerably smaller than that offered by MZM, for instance [33].

2.4 Multi-Layered Integrated Silicon Photonics

2.4.1 Motivation for Multi-Layered Optical Designs

Silicon on insulator (SOI) has been the dominant development platform for silicon photonics technology due to its low optical propagation loss. However, SOI is limited to lateral integration of photonics and electronics components. Vertical integration of photonic devices is usually performed through direct deposition of amorphous or polycrystalline silicon layers [21, 22, 23, 24]. Multi-layered integration is desirable because of several advantages such as reduced chip size and improved thermal isolation.

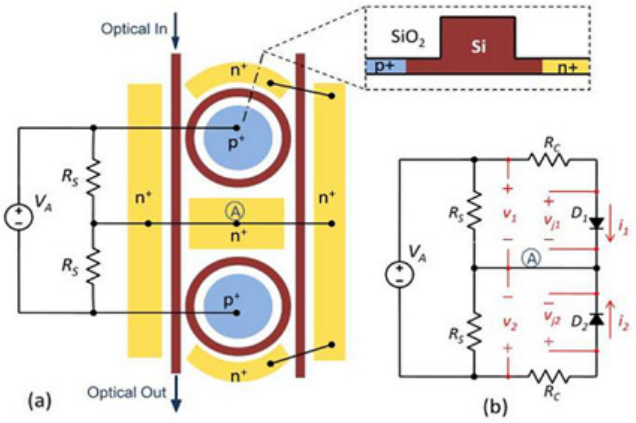


FIGURE 2.8: (a) top view of the dual-ring optical modulator. A cross-section of the modulator is shown in the inset. (b) electrical-circuit model of the dual-ring system.

Deposited SiP can offer a cheap and reliable implementation of SiP integration with the existing CMOS technology. SiP integrated circuits can be integrated either at the front-end or back-end of line of a CMOS chip [22, 52]. Figure 2.9 shows a schematic, envisioned by Ho et al., for future multi-layered SiP back-end integrated with existing CMOS chips. A number of challenges have been identified with the front-end integration of SiP with CMOS chips. For example, the thickness of the SiO_2 optical isolation layer is restricted by the buried oxide (BOX) thickness of SOI CMOS devices [32]. Moreover, the integration of SiP on the same layer as the CMOS transistors means that the two technologies will compete on valuable chop space [32]. The inclusion of SiP in front-end processing adds challenging restrictions on the design of most of SiP devices. Nonetheless, back-end integration offers less stringent requirements on the integration of SiP with CMOS technology. Back-end integration, however, has stringent thermal budget requirements. This thermal budget signifies the importance of developing low-temperature, low loss deposited silicon waveguides. Amorphous silicon and poly-silicon can both be deposited at a relatively low temperatures. However, the present plasma-enhanced chemical vapour deposition (PECVD) of poly-Si can only produce high optical loss waveguides: high temperature ($> 1000°C$) annealing is required to decrease the optical loss.

Another important motivation is the availability of low loss CMOS-compatible deposited materials such as silicon nitride and amorphous silicon. Silicon nitride is material that has low optical loss at the telecommunications wavelengths [31]. Indeed, silicon nitride has been used to realise a multi-layered photonic integrated circuit [31]. However, silicon nitride has two major disadvantages: small refractive index and the absence of any means to realise optical switching. The small refractive index inevitably leads to devices with large footprint. Therefore, another alternative material is needed for efficient and versatile integration of photonic integrated circuits (PIC) in short-reach interconnects technology. Ho et al. proposed a conservative thermal budget of 90 minutes at 450 °C for back-end integration of SiP [32].

Amorphous silicon (α-S) and hydrogenated micro-crystalline silicon (μc-S:H) have also be proposed for multi-layered PICs [53]. Although these two materials exhibit low transmission loss at 1550 nm, they show low charge mobility [53]. This disadvantage means that α-S and μc-S:H are only limited to passive devices and cannot be used to realise efficient and fast optical switches.

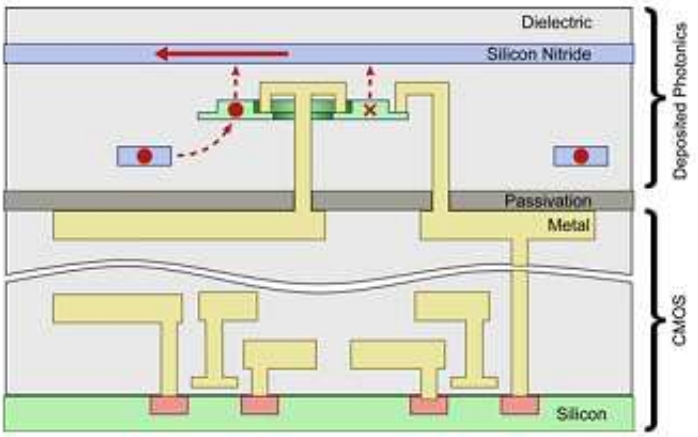


FIGURE 2.9: Schematic cross-sectional view of back-end integrated SiP using deposited silicon and silicon nitride waveguides.

2.4.2 Polysilicon in Multi-Layered Optical Structures

Recently, there has been an increased interest in polysilicon waveguides due to their low cost and added design flexibility [21, 22, 23, 24, 25, 27, 28, 26, 53]. An important characteristic of polysilicon waveguides is their low-cost compared to SOI. However, earlier reported optical propagation losses ($35 - 77$ dB/cm) abated the interest for using polysilicon in photonics applications [23]. Engineering the waveguide structure and deposition processes has recently resulted in reducing the optical propagation loss to ~ 6 dB/cm for TE mode [25]. However, annealing polysilicon at temperatures ≥ 900 °C has been widely used to improve the crystallinity of as-deposited polysilicon films.

Few active devices based on deposited silicon photonics have been reported in literature [54, 55]. Preston et al. demonstrated a ring-resonator, injection-based poly-silicon modulator operating at 2.5 Gb/s with an extinction ratio of 10 dB. The modulator employed a $p^+n^-n^+$ diode to realise optical modulation. The poly-Si waveguides were annealed at 1100 °C to reduce optical loss. The authors claim that injection-based poly-Si modulators are capable of achieving higher modulation speeds than crystalline-based modulators due to the short recombination time caused by the grain boundaries of poly-Si.

2.4.3 Introduction to Hot-Wire Chemical Vapour Deposition

Most of the reported polysilicon films were deposited or post-treated at high temperatures ($\geq$ 900 °C), e.g. [21, 24, 25, 27, 28]. This high temperature may not be suitable for multilayer integration and back-end fabrication processing [30]. Takei et al. reported low-loss, 6.5 dB/cm, silicon waveguides using hydrogenated microcrystalline silicon (μc-Si:H) deposited at 250 °C [30]. Nonetheless, μc-Si:H is not suitable for active optical devices. No poly-Si sub-micron waveguides with relatively low optical loss has been processed at temperatures below 900 °C.

The deposition of poly-Si films has been widely based on low-pressure chemical vapour deposition (LPCVD) processes [28, 24, 21, 26]. The majority of low-loss poly-Si waveguides have been

realised by depositing an a-Si film below 600 °C followed by a thermal anneal at > 1000 °C. Poly-Si can be directly deposited using LPCVD at temperatures higher than 600 °C [23]. While LPCVD is reliable, reproducible, and can achieve excellent film uniformity, it is limited by the high temperature required to deposit a good quality poly-Si films. Silane (SiH_4) relies on the temperature of the substrate for its decomposition and surface reaction to create a-Si or poly-Si films. Therefore, LPCVD is not suitable for back-end integration due to its high thermal budget.

Plasma-enhanced chemical vapour deposition (PECVD) offers low-temperature deposition of a-Si and poly-Si films. In a PECVD process, plasma radicals are used to break the Silane's bonds. The use of radicals allows the CVD process to take place at temperatures as low as 100 °C REF. However, the plasma introduces ion damage to the deposited films and this reduces the quality of poly-Si films obtained using PECVD. Moreover, the plasma normally produces dust inside the processing chamber becuase of the tendency of negatively charged particle to attach to the positively charged electrod. Hence, these particle may grow with the film and result in an inferior film quality [56]. Furthermore, PECVD is not as efficient in producing radical as other methods are such as the HWCVD process. The low efficiency of gas utilisation of PECVD stems from its reliance on the density of ions to break the SiH_4 bonds: a trade-off is needed between increasing the efficiency of gas utilisation, by increasing ion density, and the ion damage caused by this increase of ion density.

Another silicon deposition technique is the hot-wire chemical vapour deposition (HWCVD) [56, 57, 58]. Advantages of HWCVD include low deposition temperatures ($\leq$ 300 °C), low ion-induced damage, high deposition rate, controllable uniformity, large and scalable deposition area, and lower-cost polysilicon films [56]. Like LPCVD, HWCVD offers excellent uniformity step coverage while maintaining low temperature processing. HWCVD is also more efficient in utilising source gas under the same process pressure than PECVD becuase of the large surface area of the filament. Moreover, the wafer or sample on which a film is to be deposited does not function as part of the particle generation process, like PECVD where the wafer acts as an electrode [56]. This allows the scalling up of deposition systems easier to develop and maintain than PECVD [56].

In a hot-wire chemical vapour deposition (HWCVD) process, the precursor gas (silane) is efficiently broken into radicals using a remote filament while the substrate is only heated at low temperatures [56]. The chemical reaction that takes place in a HWCVD chamber is:

$$SiH_4 \rightarrow Si + 2H_2 \tag{2.6}$$

A schematic presentation of the deposition process is shown in Figure 2.10. An array of tungsten/tantalum wires is heated electrically to around 2000 °C. Then, precursor gases, silane SiH_4 and H_2 for poly-Si deposition, are injected into the chamber through a gas inlet. Thermal decomposition of the precursor gases occur on the heated wires to form radical species. Note that the efficiency of forming radical species in a HWCVD process is significantly superior to the conventional PECVD process [56]. Reaction by-products are pumped out of the chamber while useful radicals (mostly silicon hydrides) adsorbed on the substrate surface forming poly-Si crystals.

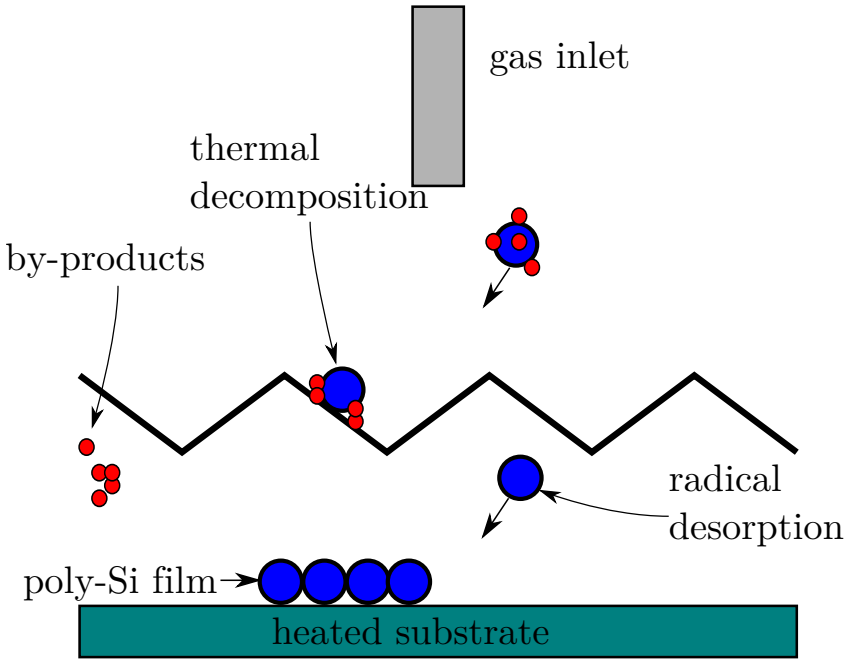


FIGURE 2.10: A schematic view of an example of a HWCVD process chamber. The schematic also shows a simple sequence of poly-Si formation using HWCVD.

To avoid high deposition temperatures, we used HWCVD instead of the more conventional low pressure CVD (LPCVD) and PECVD processing. We reported the first low-temperature, relatively low loss, sub-micron poly-silicon waveguides [59]. Losses as low as 13 dB/cm were obtained at deposition temperature of only 240 °C. This demonstration is important in the development of low-temperature, low loss deposited silicon waveguides for multi-layered CMOS-integrated SiP.

2.5 Zinc Oxide (ZnO) as an Electro-Optical Material

Being a transparent material at a wide range of wavelengths, ZnO has received substantial research focus for numerous potential electro-optical applications. Zinc oxide (ZnO) can be used across a wide range of wavelengths due to its wide band gap [60, 61]. Furthermore, the transparency of ZnO thin films can be as high as 80% [62] at a wavelength of 1550 nm. Zinc oxide has a large piezoelectric constant that can be used to introduce deformation within the crystal of the material; hence, enabling a wide range of applications such as actuators and transducers [63, 64]. Furthermore, ZnO is a good electrical material due to its high thermal conductivity that enables it to remove heat efficiently [65].

2.5.1 Electrical Properties of Zinc Oxide

Zinc oxide is naturally n-type doped material [65]. This unintentional doping has been widely attributed to oxygen vacancies and zinc interstitial sites [66, 67]. Nonetheless, it is difficult to control the conductivity of ZnO thin films because there is no clear evidence to what causes

its high n-type conductivity [65]. It is widely accepted that the preparation method of ZnO thin films is a predominant factor in determining the electrical and optical properties of ZnO. Because of the difficulty in materialising p-type ZnO, the material was incorporated into hybrid structures in order to realise electronic devices such as diodes and transistors. Indeed, several n-ZnO/p-Si heterojunction diodes have been reported [17, 18].

Zinc oxide can form ohmic contact with several metals including aluminium (Al) [68]. The annealing temperature for Al/ZnO contact is normally below 350 °C [68]. Moreover, aluminium has been used extensively to form ohmic contacts with silicon. Therefore, one metal can be used to form the ohmic contacts on both sides of the n-ZnO/p-Si heterojunction.

2.5.2 Optical Properties of Zinc Oxide

The interest in ZnO structures stems from its wide electrical band gap ($\sim$ 3.37 eV), which allows for electroluminance at the visible range where the semiconductor also shows good transparency (80%) [69]. However, there has been little work on the optical properties of ZnO at the telecommunication wavelengths. Srikant and Clarke reported that the transmission of bulk single-crystal ZnO at at a wavelength of 1550 nm is 80% [70].

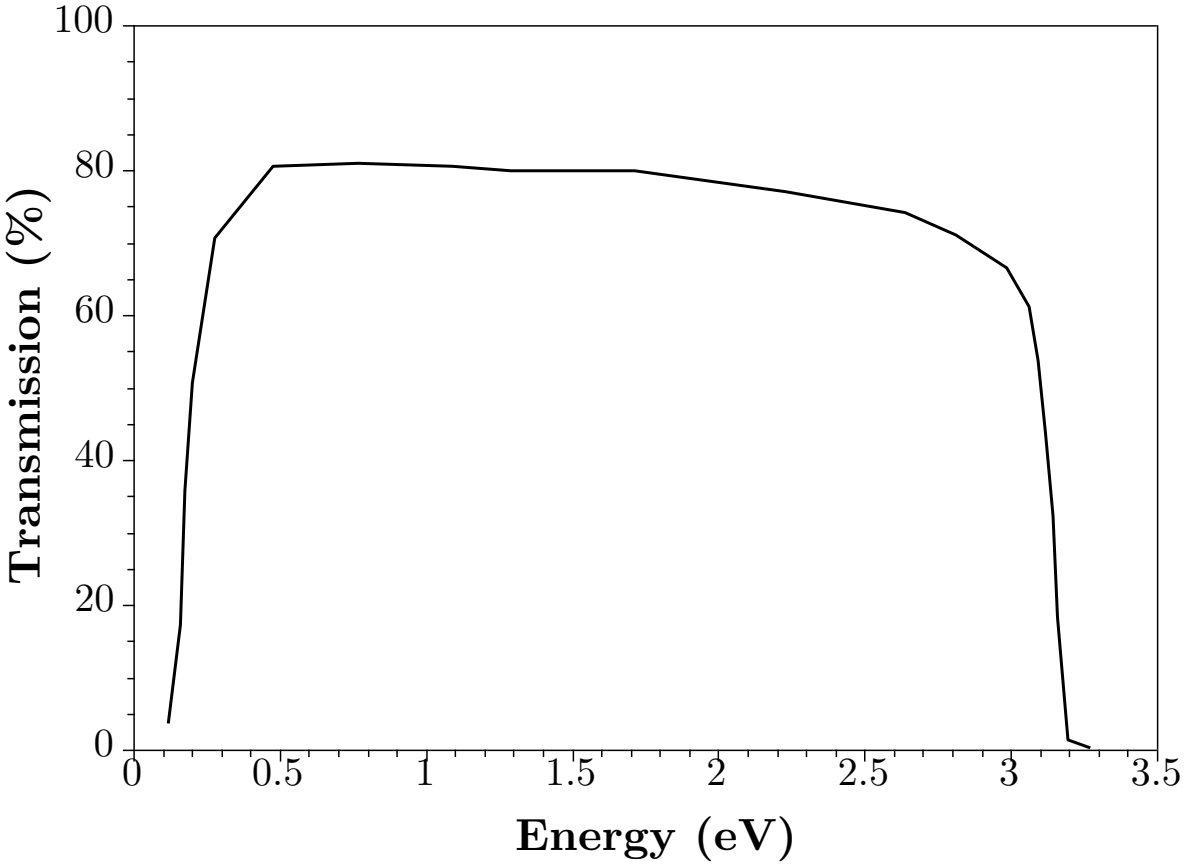


FIGURE 2.11: Transmission of bulk ZnO as a function of photon energy [70].

Figure 2.11 shows the transmission spectrum of bulk ZnO as a function of photon energy. The photon energy 0.8 eV corresponds to a wavelength of 1550 nm. It is clear from the figure that

the transmission at 1550 nm is approximately 80% . Despite the study considered bulk ZnO, the result should still be valid for high quality ZnO thin films; the transmission characteristics of bulk and thin film ZnO should be similar [70].

2.5.3 Optical Applications of Zinc Oxide

Zinc oxide has been widely investigated for photonics applications. Hammer et al. reported low loss epitaxial ZnO waveguides grown on aluminium oxide (Al_2O_3) [13]. The authors reported a propagation loss of 5 dB/cm for 10 μm thick ZnO waveguides at a wavelength of 650 nm and established that the loss depends on the level of free carrier concentration. ZnO ridge waveguides have also been deposited on silicon substrates [14]. Figure 2.12 shows a schematic view of the ZnO ridge waveguides. The authors investigated the optical gain at $\lambda = 385$ nm for a 100 nm thick and 2000 nm wide ridge waveguides. It was found that the optical gain was 120 cm^{-1} at a pump intensity of ~ 1.9 MW/cm^2.

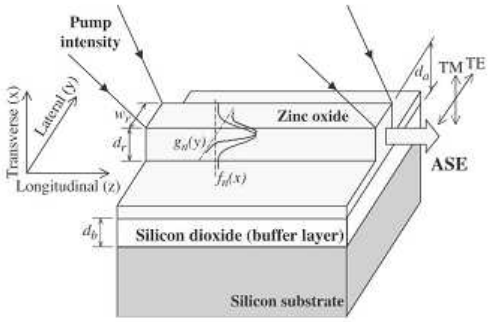


FIGURE 2.12: Schematic view of ridge ZnO waveguides deposited on a silicon substrate [14].

The non-linear optical properties of ZnO waveguides have also been investigated. Morales Teraoka et al. found that the non-linear parameter $\gamma_o = 22.5\ W^{-1}m^{-1}$ [15]. These finding promotes ZnO as an versatile optical material. ZnO has also been shown to function as a transducer in SiO_2 integrated Mach-Zehnder modulator [16]. The device relied on the high piezoelectric coefficient of ZnO films. Acoustic modulation at a wavelength of 633 nm was demonstrated.

The majority of ZnO optical devices have not been operated at the telecommunication wavelengths. ZnO has been mostly studied at wavelengths ranging from 300 to 900 nm. Although some studies showed that ZnO induces low absorption loss at the telecommunication wavelengths, no devices reported to operate at those wavelength [70].

2.5.4 Introduction to Atomic Layer Deposition (ALD)

Zinc oxide can be deposited by a number of deposition methods such as rf magnetron sputtering, molecular-beam epitaxy (MBE), pulsed-laser deposition (PLD), and chemical vapour deposition (CVD) [60]. The low temperature processing (< 400 °C), simplicity, and low cost of magnetron sputtering was the preferred deposition method in the early explorations of ZnO deposition [60]. Molecular-beam epitaxy(MBE) offers excellent control over the deposition parameters and allows the monitoring of film thickness in real-ttime [60]. The pulsed-laser deposition (PLD) method

produces high quality ZnO films at low temperatures (200 – 800 °C) [60]. All these methods operate by sputtering a high quality ZnO target and deposit on a substrate. On the other hand, CVD depositon of ZnO relies on the following chemical reaction between a Zn target and DI water:

$$Zn + H_2O \rightarrow ZnO + H_2 \tag{2.7}$$

The advantage of using CVD is its capability to deposit ZnO on a large areas and hence increasing the throughput [60]. All previously mentioned deposition technigues require either a high quality Zn or ZnO target. Moreover, most of the reported ZnO films, deposited using the already mentioned methods, have been deposited on substrates other than silicon. For ZnO deposition on silicon, atomic layer deposition (ALD) has received a significant investigation interest from the research community because of its atomic control over the thickness and high quality ZnO films that can be produced by ALD [71, 72, 73]. This method was chosen for the deposition of ZnO in this project because of the availability of ALD tools in the Southampton Nanofabrication Centre (SNC). Other methods were not feasible.

Atomic layer deposition (ALD) is a gaseous, self-limiting, deposition process in which a substrate is periodically exposed to a sequence of cycles to deposit a single mono-layer of the targeted material per a sequence of reactions. The sequential reaction phases distinguishes ALD from other deposition techniques such as CVD. Unlike CVD processes, reactants, in an ALD process, are introduced to the process chamber separately. As a consequence, chemisorptive bonds between a reactant and the substrates surface are not obstructed by the presence of another reactant which can lead to unwanted defects such as pin-holes [19]. The introduction of a precursor (or reactant) is always preceded by a purging step in which an inert gas such as N_2 is used. During purging, excess molecules, that were not chemisorbed to the surface, are driven out of the chamber. Hence, when the next reagent is introduced to the clean chamber, surface reactions occur only on the surface. This process ensures that only a mono-layer of the targeted material is deposited per cycle. Figure 2.13 1illustrates an example of a ZnO-ALD process reactions.

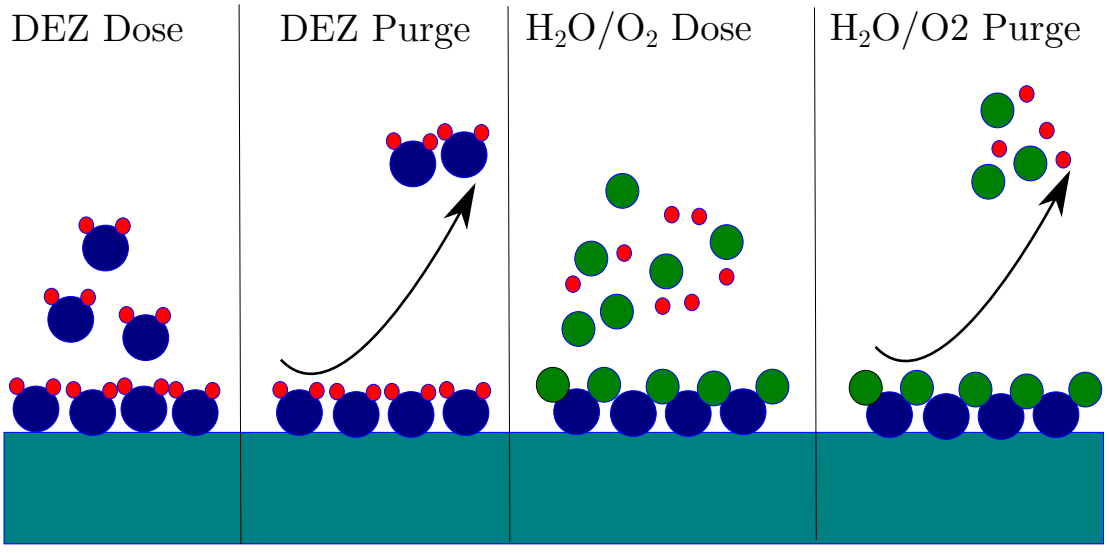


FIGURE 2.13: Schematic diagram of plasma-enhanced atomic layer deposition of zinc oxide.

The growth rate of an ALD deposition is constant across a certain range of process temperatures, commonly known as the ALD temperature window [74, 73]. Outside the ALD window, the reactions become CVD-like due to unsaturated or over-saturated surfaces. For example, Figure 2.14 shows that a precursor or surface species are likely to decompose at high temperatures outside the ideal ALD window. If the surface species decompose, this may lead to additional adsorption and hence higher growth rate; while, if the surface species break from the surface (desorption), the reaction with the reagent cannot be completed and the growth rate decreases. On the other hand, at low temperatures, two outcomes are possible. The first possibility is for the reactant to condense on the surface and hence the growth rate increases. While the second possibility is the lack of thermal energy that is required to initiate surface reactions; this effect leads to a reduction in growth rate [74].

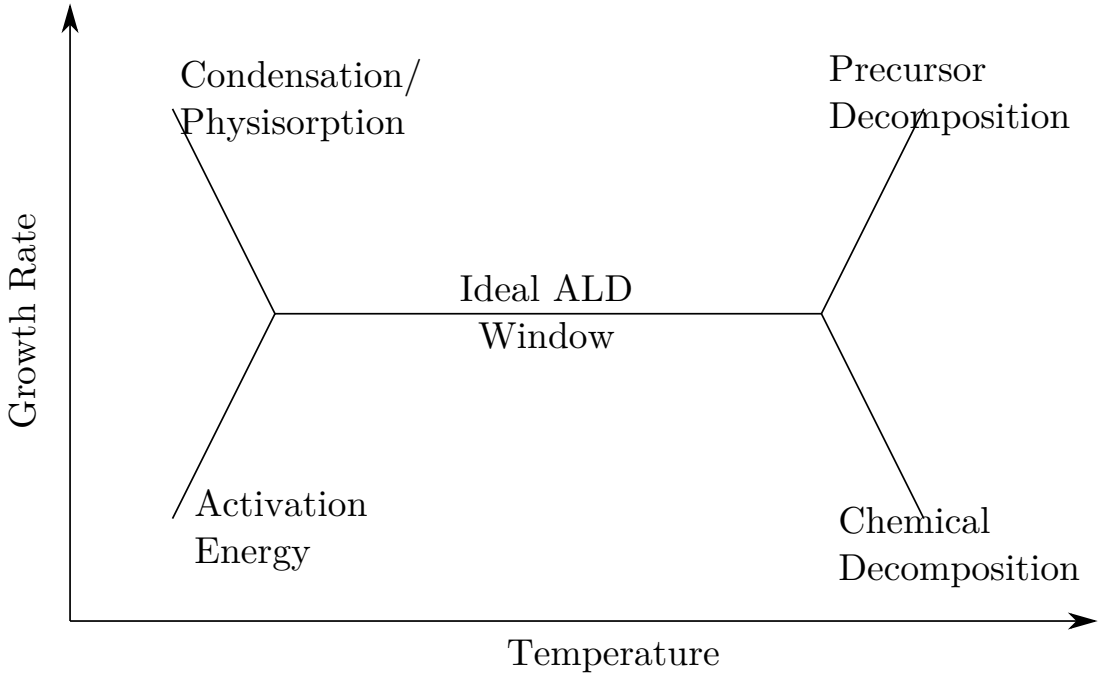


FIGURE 2.14: Phase diagram of the dependence of the growth rate on temperature. The ideal ALD window is where the growth rate remains constant within a range of temperatures [74].

An important parameter in the ALD process is the precursor's dose time which is governed by the saturation density and the total surface area [75]. The reaction zone must be exposed to a precursor for sufficient time such that the substrate is fully saturated. Moreover, in order to avoid CVD-like reactions, overlap between the two precursors must be prevented. This can be achieved by sufficient purging time [76]. However, over-purging may lead to counter-effective results. The dependence of the growth rate on the purging time follows a similar pattern to the temperature window [76]. If the purging time is longer than needed, thermal decomposition or desorption may occur. However, if the purge time is short, the precursors can involve in a gas reaction above the substrate's surface resulting in a reduction of growth rate and potential contamination. Further, the plasma's power and time determines the defects in the ZnO lattice, normally induced by ion bombardment.

As with any micro-fabrication processes, ALD has its limitations. The obvious disadvantage is its slow deposition rate; a typical cycle time is ≥ 6 seconds. However, ALD is primarily used to

deposit dielectric oxides films which need to be thin (i.e. where $t \leq 100nm$). Another limitation of ALD is its poor selectivity caused by the process's dependence on the surface's chemisorptive nature and not its composition [75].

2.6 Summary

Table 2.6 summarises the silicon-based electro-optical modulators reviewed in this chapter. Although there are more devices worth mentioning, the performance they exhibited is similar to the ones mentioned in this review. It is important to monitor the performance of modulators in terms of their electrical or optical structures rather than their individual characteristics.

Generally, electro-absorption devices offer broader bandwidths and smaller footprint than electro-refraction devices. However, MZI-based modulators tend to be faster and have lower insertion loss than electro-absorption devices. Resonant-based modulators are generally more efficient than other types of devices due to their small footprint. Nonetheless, the bandwidth of resonant-based modulators is small ($< 1 \times 10^{-3}\,\mu$m) and they also tend to be temperature sensitive. Electrically, depletion-based devices are faster but less efficient than injection-based devices.

Author	Type	Modulation Depth	Footprint/length	Speed	Power Consumption	Insertion Loss	Bandwidth
Treyz, May, and Halbout	Absorption	6.2 dB	1000 μm	20 MHz			
Elshaari and Preble	Absorption	4.6 dB	100 μm	10 Gb/s	–	1.98 dB	0.1 μm
Liu, M et al.	Absorption	0.1 dB μm	–	1 GHz	–	–	0.25 μm
Sorger, V. et al	Absorption	1 dB μm	5 μm	–	–	–	1 μm
Soref et al.	MZI	–	1000 μm	–	–	1 dB	–
Liu, A. et al.	MZI	–	2500 μm	1 GHz	–	6.7 dB	–
Green et al.	MZI	3.6 V.cm	200 μm	10 Gb/s	5 pJ/bit	–	–
Watts et al.	MZI	1 V.cm	500 μm	10 Gb/s	–	–	–
Jiang et al.	MZI	92%	80 μm	–	–	–	–
Nguyen, H. et al.	MZI	0.028 V.cm	200 μm	10 Gb/s	–	–	–
Cutolo, A. et al.	Bragg Grating	3 dB	3200 μm	–	–	–	–
Liu and Chou	Fabry-Perot	100%	18.3 μm	–	–	–	–
Barrios and Lipson	Fabry-Perot	86%	–	31 MHz	–	–	
Schmidt et al.	Fabry-Perot	6.6 dB	6 μm	300 MHz	–	–	–
Schmidt et al.	Ring Resonator	15 dB	Diameter = 12 μm	1.5 Gb/s	–	9 dB	0.0004 μm
Xu et al.	Dual Ring Resonator	–	–	40 Gb/s	–	–	–
Ben Masaud T.	Electro-absorption	10 dB	1000 μm	0.9 MHz	1 μJ	1.2 dB/cm	–

Table 2.1: Summary of performance characteristics of key silicon photonics optical switches

Chapter 3

Theoretical Background

3.1 Introduction

This chapter aims to introduce the physical principles underlining the operation of an integrated waveguides and silicon optical switches. The first section of this chapter presents the physics of guided wave theory. Then, the focus shifts to the plasma dispersion effect whereby the optical properties of silicon waveguides can be altered. The following section considers the electrical structures required to induce the plasma dispersion effect in silicon waveguides. Finally, the Fabry-Perot structure, used to realise optical switching, is introduced.

3.2 Silicon Waveguides

In this section, the fundamentals of guided optics theory are briefly introduced. Firstly, the corner stone of guided optics, the total internal reflection, is explained using ray optics. Secondly, the guided optical modes of a planar waveguide are derived using the electromagnetic theory. Unlike ray optics, electromagnetic theory can fully explain the behaviour of guided waves. Then, the effective index method, used to approximate the propagation constant for a two dimensional waveguide, is introduced. Finally, the sources of optical losses in a typical waveguide are introduced.

3.2.1 Total Internal Reflection

An optical signal can be confined to a medium by means of a phenomenon known as the *total internal reflection* (TIR). With the aid of ray optics, total internal reflection can be explained without the need for understanding the electromagnetic theory. When an optical wave is incident on the interface of two different media with two distinct refractive indices, reflection or refraction or both occurs at the interface as illustrated in Figure 3.1. The refractive indices of the two media and incident angle determine the characteristics of the reflected and refracted waves [78].

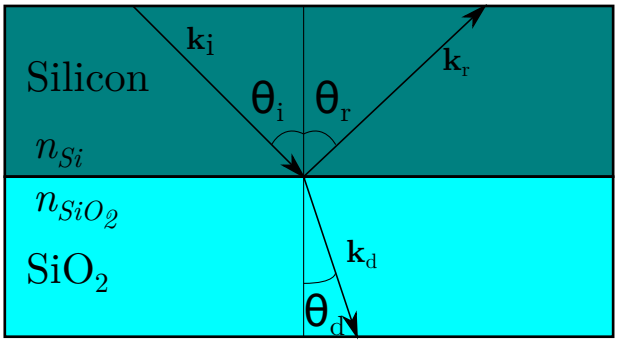


FIGURE 3.1: Reflection and refraction of an optical wave incident at an interface of two media having different refractive indices. The value of the refractive indices determine the critical angle.

Total internal reflection occurs when the incident angle is larger than the *critical angle*, θ_c, identified by the relation [78]:

$$\theta_c = \sin^{-1} \frac{n_2}{n_1} \tag{3.1}$$

where the refractive indices $n_1 > n_2$.

Silicon waveguides are normally fabricated on top of a SiO_2 layer. The refractive indices of silicon and silicon dioxide are $n_{Si} = 3.47$ and $n_{SiO_2} = 1.45$, respectively. Using Equation 3.1, the critical angle at the Si/SiO_2 interface is $\sim 24.7°$ while it is $\sim 16.75°$ at the Si/air interface.

3.2.2 Modes of a Planer Waveguide

Figure 3.2 illustrates a one dimensional planar waveguide indicated by a refractive index n_1. The direction of propagation is along the z axis. The guiding medium is sandwiched between two media of refractive indices n_2 and n_3, where $n_1 > n_2 > n_3$. This configuration, known as asymmetric planar waveguide, is typical of silicon waveguides fabricated on the silicon on insulator (SOI) platform.

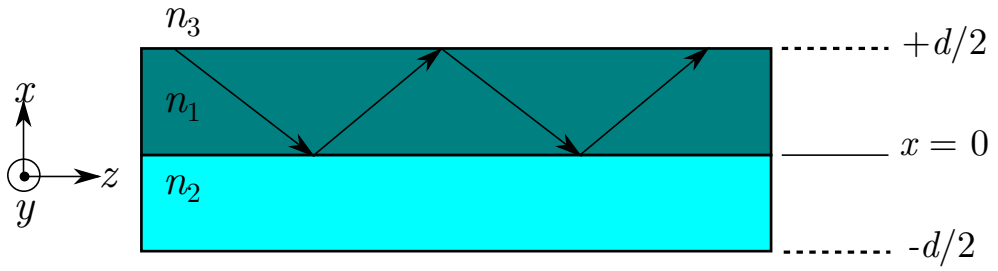


FIGURE 3.2: Propagation of an optical wave in a planar waveguide.

A planar waveguide can support a number of optical modes which can generally be categorised into two groups; namely transverse electric (TE) or transverse magnetic (TM) modes. A transverse electric wave is an electromagnetic wave whereby the electric field component in the direction of propagation is zero, i.e. $\mathcal{E}_z = 0$. Similarly, a transverse magnetic wave is an electromagnetic wave where its magnetic component is always perpendicular to the direction of propagation, i.e. $\mathcal{H}_z = 0$.

All waveguide parameters for a transverse mode can be determined by knowing the propagation constant, β, of that mode in addition to refractive indices and dimensions of a planar waveguide. The following derivation for the propagation constants considers only the fundamental TE mode and is based on [79]. A similar derivation will result the propagation constants for TM modes.

In order to find the propagation constant for TE guided modes, the wave equation for a planar waveguide must be solved with the appropriate boundary conditions. The wave equation for a planar waveguide is given by [79]:

$$\frac{\partial^2 \mathcal{E}_y}{\partial x^2} + \left(k^2 - \beta^2\right) \mathcal{E}_y = 0 \tag{3.2}$$

where $\mathcal{E}_y$ is the electric field component in the y-axis, and k is the wavenumber which is given by:

$$k = \frac{\omega^2}{c^2} n^2(x) \tag{3.3}$$

where ω is the angular frequency of the electromagnetic wave, c is the speed of light in vacuum, and n is the refractive index of the guiding medium.

For TE guided modes, there are three non-vanishing field components; namely the electric field component along the y-axis $\mathcal{E}_y$, the magnetic field component along the x-axis $\mathcal{H}_x$, and the magnetic field component along the z-axis $\mathcal{H}_z$. The later two field components can be expressed in terms of $\mathcal{E}_y$ as:

$$\mathcal{H}_x = -\frac{\beta}{\omega \mu_0} \mathcal{E}_y \tag{3.4}$$

$$\mathcal{H}_z = \frac{1}{j\omega\mu_0} \frac{\partial \mathcal{E}_y}{\partial x} \tag{3.5}$$

Before solving the wave equation, it is useful to introduce the dimensionless *normalised waveguide parameters* (V and b) and the *mode parameters* (${h_1}^2$, ${\gamma_2}^2$, and ${\gamma_3}^2$).

3.2.2.1 Normalised Waveguide Parameters

Normalised waveguide parameters are frequently used to describe the mode properties of a waveguide [79]. The first waveguide parameter is the *normalised frequency and waveguide thickness* (the V number) defined as:

$$V = \frac{2\pi}{\lambda} d\sqrt{{n_1}^2 - {n_2}^2} = \frac{\omega}{c} d\sqrt{{n_1}^2 - {n_2}^2} \tag{3.6}$$

where d is the thickness of the guiding medium as shown in 3.2.

Moreover, the *normalised guide index*, b, relates the propagation constants of a mode and is defined as:

$$b = \frac{\beta^2 - {k_2}^2}{{k_1}^2 - {k_2}^2} \tag{3.7}$$

where k_1 and k_2 are the wavenumbers of media with refractive indices n_1 and n_2, respectively (Figure 3.2).

It is useful to parametrise the asymmetric structure of the planar waveguide shown in Figure 3.2 in terms of TE modes. The *asymmetry factor* a reflects the unequal refractive index between the top and bottom claddings (i.e. $n_2 \neq n_3$). The asymmetry factor for TE modes, a_E, is defined as:

$$a_E = \frac{{n_2}^2 - {n_3}^2}{{n_1}^2 - {n_2}^2} \tag{3.8}$$

3.2.2.2 Mode Parameters

Provided that $k_1 > \beta > k_2 > k_3$, three transverse positive parameters, h_1, γ_2, and γ_3, can be defined for a guided mode as:

$${k_1}^2 - \beta^2 = {h_1}^2 \tag{3.9}$$

$$\beta^2 - {k_2}^2 = {\gamma_2}^2 \tag{3.10}$$

$$\beta^2 - {k_3}^2 = {\gamma_3}^2 \tag{3.11}$$

Note that because $\beta = k_1 \sin\theta$, where θ is the incident angle, h_1 represents the transverse component of the wavevector in the guiding medium.

3.2.2.3 Solution to TE Guided Modes

Using Equations 3.4 and 3.5, a solution to the wave equation for a planar waveguide (Eq. 3.2) can be found. The boundary conditions specify that $\mathcal{E}_y$, $\mathcal{H}_x$, and $\mathcal{H}_z$ must be continuous at the upper (n_3/n_1) and lower interfaces (n_1/n_2). Solving Equation 3.2 for $\mathcal{E}_y$ results in the following field distribution:

$$\mathcal{E}_y = C_{TE} \begin{cases} \cos\left(h_1 d/2 - \psi\right) \exp\left[\gamma_3 \left(d/2 - x\right)\right] & x > d/2 \\ \cos\left(h_1 x - \psi\right) & -d/2 < x < d/2 \\ \cos\left(h_1 d/2 + \psi\right) \exp\left[\gamma_3 \left(d/2 + x\right)\right] & x > -d/2 \end{cases} \tag{3.12}$$

where ψ is the phase of the electromagnetic wave and C_{TE} is found by normalising the mode field to yield:

$$C_{TE} = \sqrt{\frac{\omega\mu_0}{\beta d_E}} \tag{3.13}$$

where the *effective waveguide thickness* d_E for the TE mode is defined as:

$$d_E = d + \frac{1}{\gamma_2} + \frac{1}{\gamma_2} \tag{3.14}$$

The boundary conditions also produce the following eigenvalue equation:

$$\tan h_1 d = \frac{h_1 \left(\gamma_2 + \gamma_3\right)}{{h_1}^2 - \gamma_2\gamma_3} \tag{3.15}$$

Equation 3.15 is a transcendental equation for which the permitted solutions can be found graphically by plotting the left- and right-hand sides. Moreover, equation 3.15 is normally plotted in terms of the V number and the normalised guide index b as:

$$\tan\left(V\sqrt{(1-b)}\right) = \frac{\sqrt{\frac{b}{1-b}} + \sqrt{\frac{b+a_E}{1-b}}}{1 - \frac{b(b+a_E)}{1-b}} \tag{3.16}$$

Figure 3.3 shows the permitted values for β. Each permitted β value reflects a supported TE mode. The three supported TE modes shown in Figure 3.3 can be denoted as TE_0 (fundamental mode), TE_1, and TE_2.

The asymmetry factor for a crystalline SOI waveguide with air as the upper cladding is ~ 0.11.

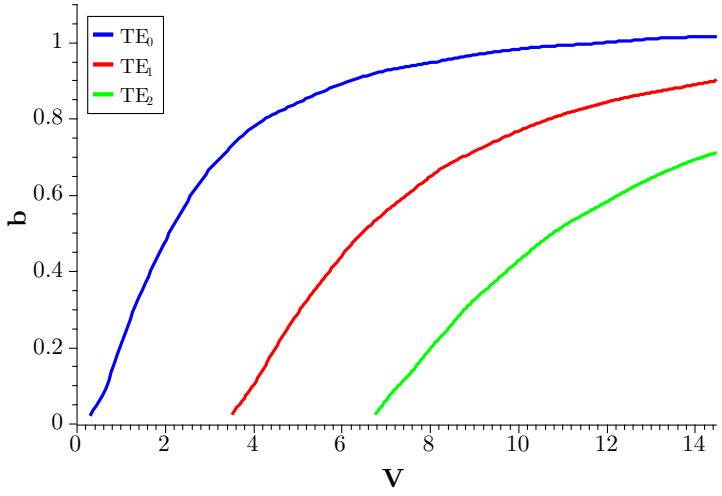


FIGURE 3.3: Permitted values of the normalised guide index b as a function of the V number. The figure shows the dispersion curve of the first three TE modes.

3.2.3 Two Dimensional Waveguides

The propagation constant for a two dimensional waveguide is difficult to obtain analytically. However, a simple procedure, known as the *effective index method*, can be used to approximate the propagation constant for a two dimensional waveguide. The procedure can be briefly described as follows. The structure is converted into two planar waveguides; the propagation direction of one of the planar waveguide is horizontal while the other is vertical. The solution to the wave equation in the horizontal planar waveguides are used to calculate those of the vertical planar waveguide and vice versa. This procedure is repeated until a the value of the propagation constant starts to converge; for more details on the effective index method [33].

The solution to the wave equation for two dimensional waveguides can also be evaluated numerically. Several numerical methods, such as the finite difference time domain method (FDTD), the beam propagation method (BPM), and the full-vector film mode matching method (FMM), are available to solve the two dimensional wave equation.

In this project, the finite difference time domain method (FDTD) was used to calculate the mode solutions to the sub-micron silicon waveguides. FDTD is implemented by the commercial photonics simulation package *Lumerica FDTD*. Lumerical FDTD provides an easy and quick solution to the mode characteristics of silicon waveguides in 2D and 3D designs.

3.2.4 Losses in an Optical Waveguide

Optical loss can be caused by three sources: radiation, scattering, and absorption. This section introduces these losses with reference to sub-micron silicon waveguides.

3.2.4.1 Radiation

Radiation is a design dependent loss and is mainly caused by the evanescent field of the propagating mode. For a straight waveguide, with no bends, the radiation loss should be minimal for the fundamental mode. However, if the evanescent field extends beyond the optical isolation medium (the claddings), the radiation loss can be significant. Leaky modes are particularly prone to radiation losses.

Silicon waveguides fabricated using SOI must ensure that the *buried oxide* (BOX) is thick enough to prevent mode leakage to the silicon substrate. The thickness of the BOX layer depends on the thickness of the silicon waveguide and the mode number. In this project, SOI wafers with two ($2\,\mu$ and $3\,\mu$) BOX thickness were used.

3.2.4.2 Scattering

Scattering loss can be caused by irregularities either within the guiding medium or at the interfaces of the waveguide. A common scattering mechanism is the sidewall scattering due to rough sidewalls, normally caused by imperfections in the fabrication process. Sidewall and top surface scattering loss can be very significant even for small value of *root mean square* (RMS)

roughness. For example, an RMS roughness of 8 nm to the top surface of a waveguide can result in an optical loss in excess of 9 dB/cm [59].

Scattering within the guiding material, also known as volume scattering, is minimal in intrinsic crystalline silicon. However, polysilicon shows significant volume scattering due to grain boundaries. Scattering of an optical wave depends on the relative size of the irregularity and the wavelength of that wave. It is normally challenging to quantify the scattering loss experimentally. However, numerical simulation methods can be used to estimate the scattering loss [80].

3.2.4.3 Absorption

Absorption is another important loss mechanism in optical guides. Two types of absorption exist. Firstly, free carrier absorption is caused by electrons and holes in doped silicon and is explained in detail in section 3.3. Secondly, interband absorption is caused by photons with energy larger than the bandgap energy of the guiding medium. This type of absorption loss determines the operational wavelength range. In silicon photonics, the telecommunications wavelengths (1.3 and 1.55 μm) lie far from the absorption edge of silicon near 1.1 μm. Absorption in polysilicon waveguides can be significant due to non-negligible absorption coefficient α at the telecommunications wavelengths. According to [81] (Fig. 3.4), the absorption coefficient for crystalline silicon can vary in the range from 1×10^{-3} to 1×10^{3}.

3.3 Introduction to Optical Switch in Silicon Based on the Free Plasma Dispersion Effect

Since the successful realisation of densely integrated electronic circuit on silicon platforms in the second half of the last century, interest in the optical properties of silicon grew dramatically [1]. However, it was mid-1980s that witnessed serious research steps and attempts to realise waveguide-based silicon optical modulators [2]. [81] experimentally evaluated the change in the refractive index of silicon as a result of free carrier change [81]. It was experimentally found that the change in the real part of the refractive index at 1550 nm wavelength can be written as [33]:

$$\Delta n = -\left[8.8 \times 10^{-22} \times \Delta n_e + 8.5 \times 10^{-19} \times (\Delta n_h)^{0.8}\right] \tag{3.17}$$

where Δn_e is the local fractional change in the concentration of electrons, while Δn_h is the local fractional change in the concentration of holes. Additionally, the corresponding change in the absorption coefficient at is given by:

$$\Delta \alpha = -\left[6.0 \times 10^{-18} \times \Delta n_e + 4.0 \times 10^{-18} \times \Delta n_h\right] \tag{3.18}$$

Optical modulation can be achieved by exploiting the change in the real part of the refractive index or the change in the absorption coefficient. Although the results shown in Figure 3.4 apply

to bulk silicon, they can be used for silicon waveguide structure if an appropriate electrical bias is applied.

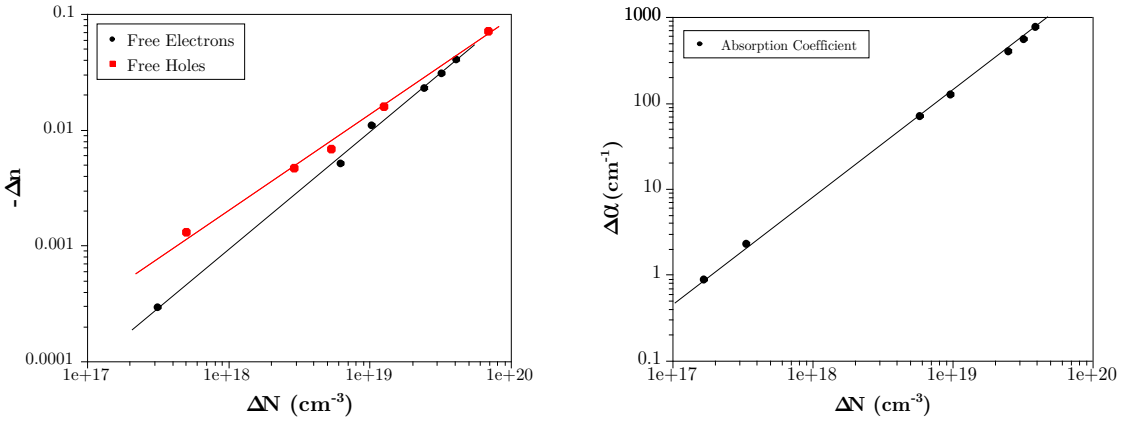


FIGURE 3.4: The change in the refractive index (a) and absorption coefficient (b) as a function of free carrier change at a wavelength of 1550 nm [81].

Electro-absorption devices directly reduce the intensity of the propagating mode by introducing more free carriers in the waveguide active region. Because of the positive sign of the right hand term in Equation 3.18, the absorption coefficient increases as the free carrier density increases. The transmission of an optical signal, expressed in terms of the absorption coefficient, can be written as [82]:

$$T = e^{-\alpha L} \tag{3.19}$$

where L is the effective length of the device. Thus, intensity reduction can be achieved by increasing either the absorption coefficient or the active length of the modulator. Free carrier absorption occurs as photons transfer their energy to electrons and holes. Photons usually have lower energy than that of the bandgap of silicon and hence result in intraband transition of holes and electrons [82]. Electromagnetic theory can be used to derive an expression for the absorption coefficient ensued from free carriers [82]. This derivation is important because it also provides an insight into the origin of the change in the refractive index caused by altering the free carrier concentration. The following derivation calculates the change in refractive index and the absorption coefficient due to change in free electrons and is based on [82]. Under the influence of an electric field, the motion of electron can be described by the following inhomogeneous differential equation [82]:

$$m^* \frac{\mathrm{d}^2 x}{\mathrm{d}t^2} + m^* g \frac{\mathrm{d}x}{\mathrm{d}t} = q E_0 e^{j\omega t} \tag{3.20}$$

where m^* is the effective mass of an electron, x is the displacement, q is the electric charge of an electron, and g is the damping coefficient. The term on the right hand side represents the applied electric force; the first term in the left hand side represents the force resulting from the acceleration of the electron; the second term denotes the damping force caused by collisions with the lattice. The steady state solution to Equation 3.20 is [82]:

$$x = \frac{qE_0}{m^* \left(\omega^2 - j\omega g\right)} e^{j\omega t} \tag{3.21}$$

The permittivity of a material can be written as:

$$\frac{\epsilon}{\epsilon_0} = 1 + \frac{\vec{P}}{\epsilon_0 \vec{E}} \tag{3.22}$$

where ϵ_0 is the permittivity of free space and $\vec{P}$ is the polarisation of the dielectric. The presence of an electric field $\vec{E}$ polarises the electron cloud and hence $\vec{P}$ changes to:

$$\vec{P} = \vec{P_0} + \vec{P_1} \tag{3.23}$$

where $\vec{P_0}$ is the polarisation in the absence of free carriers; while $\vec{P_1}$ is the additional polarisation ensued by free carriers. Equation 3.22 can be rewritten as:

$$\frac{\epsilon}{\epsilon_0} = 1 + \frac{\vec{P_0}}{\epsilon_0 \vec{E}} + \frac{\vec{P_1}}{\epsilon_0 \vec{E}} \tag{3.24}$$

Since the refractive index can be written as:

$$n_0 = \sqrt{\frac{\epsilon}{\epsilon_0}} = \sqrt{1 + \frac{\vec{P}}{\epsilon_0 \vec{E}}} \tag{3.25}$$

Equation 3.24 becomes:

$$\frac{\epsilon}{\epsilon_0} = {n_0}^2 + \frac{\vec{P_1}}{\epsilon_0 \vec{E}} \tag{3.26}$$

Silicon is an isotropic material; hence $\vec{P_0}$ and $\vec{E_0}$ are in the same direction. Moreover, $\vec{P_1}$ can be expressed as [82]:

$$\vec{P_1} = -Nq\vec{x} \tag{3.27}$$

where N is the concentration of free carriers. Equations 3.21 and 3.27 can be substituted into Equation 3.26:

$$\frac{\epsilon}{\epsilon_0} = {n_0}^2 - \frac{Nq^2}{m^* \epsilon_0 \left(\omega^2 - j\omega g\right)} \tag{3.28}$$

The real parts is:

$$\left(\frac{\epsilon}{\epsilon_0}\right)_r = {n_0}^2 - \frac{Nq^2}{m^* \epsilon_0 \left(\omega^2 + g^2\right)} \tag{3.29}$$

while the imaginary part is:

$$\left(\frac{\epsilon}{\epsilon_0}\right)_i = {n_0}^2 - \frac{Nq^2}{m^*\omega\epsilon_0\left(\omega^2+g^2\right)} \tag{3.30}$$

Applying the boundary condition information to Equation 3.21, the damping coefficient g can be expressed as:

$$m^* g\frac{\mathrm{d}x}{\mathrm{d}t} = qE \tag{3.31}$$

since

$$\frac{\mathrm{d}x}{\mathrm{d}t} = \mu m^* \tag{3.32}$$

where μ is the mobility of the free carrier. Equation 3.31 becomes:

$$\text{damping coefficient, } g = \frac{q}{\mu m^*} \tag{3.33}$$

For example, consider an n-type silicon film with $\mu_e = 1400\ \mathrm{cm}^2.(\mathrm{Vs})^{-1}$, $m^* = 0.16m_0$, and $g = 0.116167 \times 10^6\ \mathrm{s}^{-1}$. The value of g is insignificant when compared to $\omega = 10^{15}\ \mathrm{s}^{-1}$ at telecommunication frequencies. Hence, g^2 in Equations 3.29 and 3.30 can be ignored. Substituting for g using 3.33, the real and imaginary parts of the permittivity become:

$$\left(\frac{\epsilon}{\epsilon_0}\right)_r = {n_0}^2 - \frac{Ne^2}{m^*\epsilon_0\omega^2} \tag{3.34}$$

and

$$\left(\frac{\epsilon}{\epsilon_0}\right)_i = \frac{Ne^3}{{(m^*)}^2\epsilon_0\omega^3\mu} \tag{3.35}$$

The absorption loss coefficient, α, can be expressed in terms of imaginary part of the dielectric constant as:

$$\alpha = \left(\frac{\epsilon}{\epsilon_0}\right)\frac{|\vec{k}|}{n} \tag{3.36}$$

where $\vec{k}$ is the wavevector and n is the refractive index. Substituting Equation 3.35 into Equation 3.36 and using the approximation $k \simeq \frac{\omega}{c}$:

$$\alpha = \frac{Ne^3}{{(m^*)}^2\epsilon_0 n\omega^2\mu c} \tag{3.37}$$

which can be re-written as:

$$\boxed{\text{AbsorptionCoefficient, } \alpha = \frac{Ne^3\lambda_0^2}{4\pi^2 n(m^*)^2\epsilon_0\mu c^2}} \tag{3.38}$$

where $c = \nu\lambda_0$ and $\omega = 2\pi\nu$ were used; where ν is the frequency, and λ_0 is the wavelength in free space. For example, the change in the absorption coefficient at $\lambda_0 = 1550$ nm in a p-type silicon with hole concentration of $N_h = 1 \times 10^{18}$ is $\Delta\alpha = 5 \times 10^{-19} \times N_h = 50$. Furthermore, it can be noted from equation 3.34 that the change in the refractive index is:

$$\Delta\left(\frac{\epsilon}{\epsilon_0}\right)_r = -\frac{Ne^2}{m^*\epsilon_0\omega^2} \tag{3.39}$$

which can be rewritten as:

$$\boxed{\Delta\left(\frac{\epsilon}{\epsilon_0}\right)_r = \frac{Ne^2{\lambda_0}^2}{4\pi^2 m^*\epsilon_0 c^2}} \tag{3.40}$$

which relates the free carrier concentration N to change in the dielectric constant, $\Delta\left(\frac{\epsilon}{\epsilon_0}\right)_r$, or proportional to the refractive index Δn. According to equation 3.40, a change in free electron concentration results in a larger refractive index change than that produced by free holes for the same concentration change. However, [81] experimentally showed that the effect of holes is greater than that of electrons on the refractive index when the free-carrier concentration is around $1 \times 10^{17}\text{cm}^{-3}$. Moreover, absorption at this concentration level is higher for electrons than holes. Therefore, p-type silicon has been dominantly used as the primary active medium for silicon-based electro-optical switches. Therefore, p-type silicon was chosen to form the silicon waveguides in this project. Another reason for using p-type silicon was the intrinsic n-type doping of ZnO (i.e. only when the silicon is p-type doped, a functional n-ZnO/p-Si heterojunction can be made).

In order to induce free carrier change within silicon (free plasma dispersion effect), an electric field has to be applied to the active area. Several microelectronic devices allow the application of an electric field to certain parts of the devices. Examples of these devices include p-n and p-i-n junctions, and MOS capacitors. The advantages and disadvantages of these devices are beyond the scope of this theoretical review. Nonetheless, a p-n junction provides the simplest design and fabrication processing. Hence, a n-ZnO/p-Si heterojunction was proposed to show the effectiveness of integrating transparent semiconductor with the existing silicon photonics technology.

3.4 P-N Junction

Optical modulation in silicon can be realised through a change in the free carrier density in the guiding medium. One structure that enables free carrier change in a semiconductor such as silicon is the *p-n junction*. A p-n junction is semiconductor structure where free carriers exist in two distinct regions as shown in Figure 3.5.

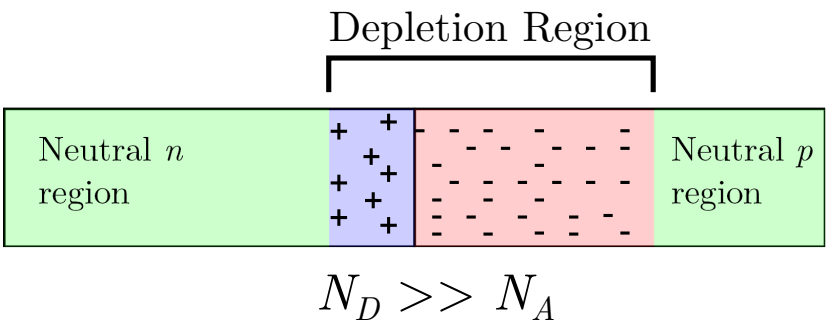


FIGURE 3.5: Depletion region at equilibrium. Because the donor concentration N_D is higher than the acceptor concentration N_A, the depletion region extends further into the p region than it does in the n region.

The free carriers, namely electrons and holes, exist in all semiconductors. However, undoped semiconductors are electrically neutral and thus the concentration of electrons are equal to that of holes. Excess charge, negative or positive, can be realised through doping the semiconductor with appropriate materials. For instance, the concentration of electrons in silicon can be increased by doping with phosphorus. In contrast, the concentration of holes can be increased by doping silicon with boron.

For a p-n junction under equilibrium (Fig. 3.5), a depletion region exists at the interface between the two doped regions. The potential difference across the p-n junction causes the accumulation of free carriers on either side of the junction. The free carriers rearrange such that they cancel out the potential difference across the depletion region.

The width of the depletion region depends on the potential difference across it. The extension of the depletion region into the n-type or p-type region depends on the relative carrier concentration on both sides. For example, if the carrier concentration on the n-type region is higher than that of the p-type region, the depletion region extends further into the p-type region than it does in the n-type region as shown in Figure 3.5.

The potential across a p-n junction can be altered by application of an external voltage. Changing the width of the depletion region provides a mechanism of changing the free carrier concentration in a confined region. The dependence of the of the width W of the depletion region on the applied external voltage is expressed by the following equation [5]:

$$\boxed{W = \sqrt{\frac{2\epsilon_s}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi} - V)}} \tag{3.41}$$

where:

- W is the total width of the depletion region.
- ϵ_s is the dielectric permittivity of silicon.
- q is the electron charge equal to 1×10^{-19} C
- N_A is the acceptor concentration in the p-type region.
- N_D is the donor concentration in the n-type region.
- V_{bi} is the depletion region's built-in voltage.

- V is the external applied voltage.

Optical modulation in silicon relies on changing the bias across the waveguide-integrated p-n junction so that the free carrier concentration changes, incurring a phase shift or absorption change on the optical wave. The *active area* of an electro-optical switch refers to the cross-sectional area of the waveguide where the change in the free carrier concentration occurs. For efficient operation, the active area must be maximised; this can be done by careful design of the waveguide structure. Moreover, the contrast in the free carrier concentration between the ON and OFF state should also be maximised; this can be realised by carefully choosing the doping level of the active area and the dimensions of the waveguide. Figure 3.6 (a) shows a common p-n configuration used in silicon optical modulators.

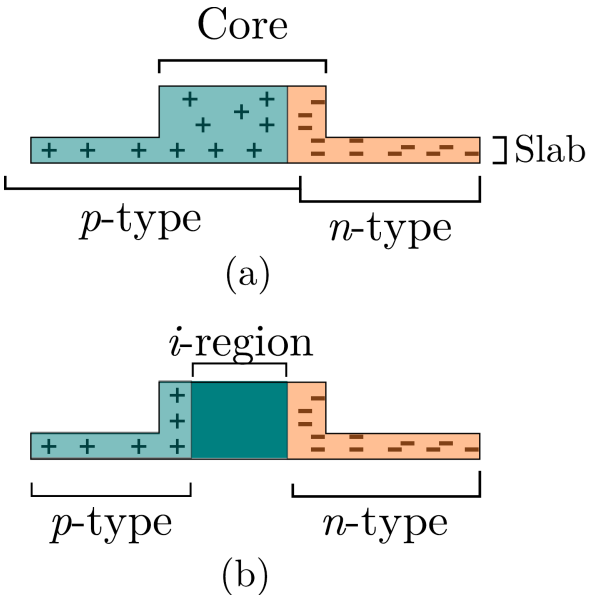


FIGURE 3.6: (a) a schematic diagram of a p-n junction integrated in a slab waveguide to form an electro-optical modulator. (b) a schematic diagram of a p-i-n structure

A common issue with the design shown in Figure 3.6 (a) is the overlapping/proximity of the doped region with the core of the waveguide. These doped region induce free carrier absorption loss. A possible solution to this issue was implemented by introducing an intrinsic (buffer) region in the core of the waveguide separating the two doped regions forming a p-i-n junction (Fig. 3.6 (b)) [35]. Although this design improves the insertion loss of the active region, it dramatically increases the capacitance and resistance of the p-n junction. Hence, the maximum switching speed is inferior to that of p-n junctions. Another possible solution is to use devices with short active lengths. However, this requires high contrast in the optical transmission properties of the materials forming the active length. Some transparent conductive oxides (TCOs) and graphene dramatically change their optical properties under the application of an electric field. Zinc oxide is a TCO that can provide short silicon-based electro-optical switch. The source of the unintentionally n-type doping exhibited by ZnO films is not fully understood [65]. However, interstitial zinc and hydrogen are suspected to from shallow donor sites that result in the n-type characteristics of as-grown ZnO. Because the nature of the free carriers in ZnO and n-type silicon is different, the optical absorption loss in ZnO might be lower than that exhibited by n-type silicon. To demonstrate the low optical loss characteristics of ZnO, it is proposed in this

project to integrate it with silicon to form a n-ZnO/p-Si heterojunction whereby the free carrier can be changed.

3.4.1 Heterojunctions

A p-n junction can be formed by two different materials in which case the p-n junction is called a heterojunction. The difference in the band gap energy between the two materials means that band gap engineering is possible. Moreover, because of the different material properties, the extension of the depletion region in each material is different from that of monojunctions. The widths of the extention of the depletion region in two materials forming a p-n junctions are given by:

$$W_1 = \sqrt{\frac{2\epsilon_1\epsilon_2 N_2 (V_{bi} - V)}{qN_1 (\epsilon_1 N_1 + \epsilon_2 N_2)}} \tag{3.42}$$

$$W_2 = \sqrt{\frac{2\epsilon_1\epsilon_2 N_1 (V_{bi} - V)}{qN_2 (\epsilon_1 N_1 + \epsilon_2 N_2)}} \tag{3.43}$$

- ϵ_1 is the dielectric permittivity of material 1.
- ϵ_2 is the dielectric permittivity of material 2.
- N_1 is the dopant concentration in material 1.
- N_2 is the dopant concentration in material 2.

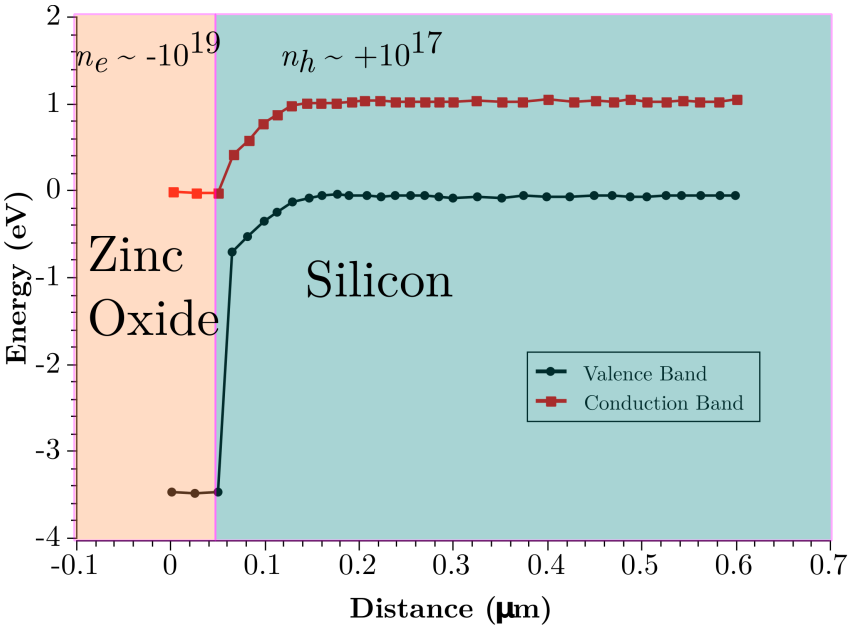


FIGURE 3.7: Energy band diagram of a n-ZnO/p-Si heterojunction. Note that the junction is abrupt and it reflects the actual proposed device where ZnO tends to exhibit high carrier concentration (i.e. $n_e \simeq 1 \times 10^{19}$).

As an example, consider the n-ZnO/p-Si heterojunction shown in Figure 3.7 where the free electron concentration in the ZnO is $n_e = 1 \times 10^{19}$, the free hole concentration in the Si region

is $n_h = 1 \times 10^{17}$, and the relative permittivity of Si and ZnO was 11.68 and 8.12, respectively. The built-in voltage, V_{bi}, can be calculated using [5]:

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{N_A N_D}{{n_i}^2}\right) \tag{3.44}$$

where k_B is Boltzmann constant, T is temperature, and $n_i(T = 300K) \simeq 9.65 \times 10^9$ is the intrinsic carrier concentration for silicon. Note that the following evaluation of the built-in voltage is not accurate as only the intrinsic carrier concentration of silicon is used; ZnO's intrinsic carrier concentration is unknown. However, the value of the built-in voltage should be reasonably close to the theoretical one. Using Equation 3.44 and assuming taht $n_e \simeq N_D$ and $n_h \simeq N_A$, the built-in voltage (or turn-on voltage) is $V_{bi} \simeq 0.96$ V. Using this value of the built-in voltage and Equation 3.42 and 3.43, the depletion region's width in the Si and ZnO regions were found to be $1.12 : \mu$m and 11.2 nm, respectively.

3.5 Photonic Devices

The objective of an electro-optical modulator is to change the output intensity of the guided wave according to the controlling electrical signal. The intensity of the guided wave can be changed by two methods: direct alteration of the intensity of the wave, or indirect alteration by changing the phase of the wave and then rely on a specific interference effect to produce a corresponding change in the intensity of the wave.

Phase modulation is important and is the most common adapted technique in silicon photonics technology. This section briefly introduces the most common optical device configuration to exploit the phase change in an optical silicon waveguide to produce intensity modulation. However, phase modulators have several drawbacks such as temperature dependence and limited operating bandwidth.

3.5.1 Fabry-Perot Interferometer

A Fabry-Perot (FP) structures can be used to achieve phase modulation. The principle of operation relies on multiple interferences of light resulting from successive partial reflections. The interferences occur in a partially optically-isolated region known as a cavity. The cavity is bounded by two mirrors that cause successive partial reflections as shown in Figure 3.8.

The transfer function of the Fabry-Perot interferometer can be analysed as follows; the analysis is based on [83]. Assuming identical Bragg reflectors, a wave suffers a constant amplitude reduction at each mirror in addition to equal phase difference incurred by the optical path difference of successive waves travelling in the cavity. The repetitive decrease in the amplitude U_n of a wave can be described by a geometric series:

$$U_1 = \sqrt{I_0}, \;\; U_2 = h\sqrt{I_0}, \;\; U_3 = hU_2, \;\; U_n = hU_{n-1} \tag{3.45}$$

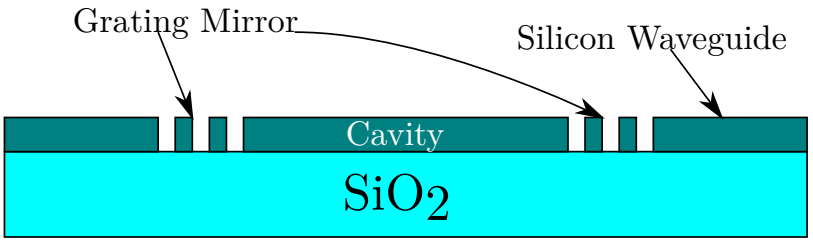


FIGURE 3.8: A longitudinal cross-section of a Fabry-Perot structure integrated in a silicon waveguide. The cavity is bounded by two Bragg grating reflectors that act as partially transmitting mirrors.

where $h = |h|e^{j\phi}$ is the initial intensity of the wave. The superposition of infinite number of successive reflected waves can be expressed by the addition of individual complex amplitudes:

$$U_{total} = U_1 + U_2 + U_3 + \cdots U_n = \sqrt{I_0}\left(1 + h + h^2 + \cdots\right) \tag{3.46}$$

Also, since:

$$\left(1 + h + h^2 + \cdots\right) = \frac{1}{1-h} \tag{3.47}$$

hence

$$U_{total} = \frac{\sqrt{I_0}}{1-h} = \frac{\sqrt{I_0}}{1 - |h|e^{j\phi}} \tag{3.48}$$

The total intensity can be written as:

$$I = |U_{total}|^2 = \frac{I_0}{|1 - |h|e^{j\phi}|^2} = \frac{I_0}{\left(1 - |h|e^{j\phi}\right)^2 + |h|^2 \sin\phi^2} \tag{3.49}$$

from which:

$$I = \frac{I_{max}}{1 + \left(\frac{2F}{\pi}\right)^2 \sin\frac{\phi}{2}^2} \tag{3.50}$$

where:

$$I_{max} = \frac{I_0}{\left(1 - |h|\right)^2} \tag{3.51}$$

and:

$$\mathcal{F} = \frac{\pi\sqrt{|h|}}{1 - |h|} \tag{3.52}$$

The quantity $\mathcal{F}$ is an indication of the quality of Fabry-Perot interferometers and is known as the finesse. The finesse specifies the sharpness of the transmission peaks and can be evaluated using the relation:

$$\mathcal{F} = \frac{FSR}{FWHM} \tag{3.53}$$

where FSR is the free-spectral range (i.e. wavelength spacing between adjacent peaks), and $FWHM$ is the Full-Width-Half-Maximum of the resonant peaks.

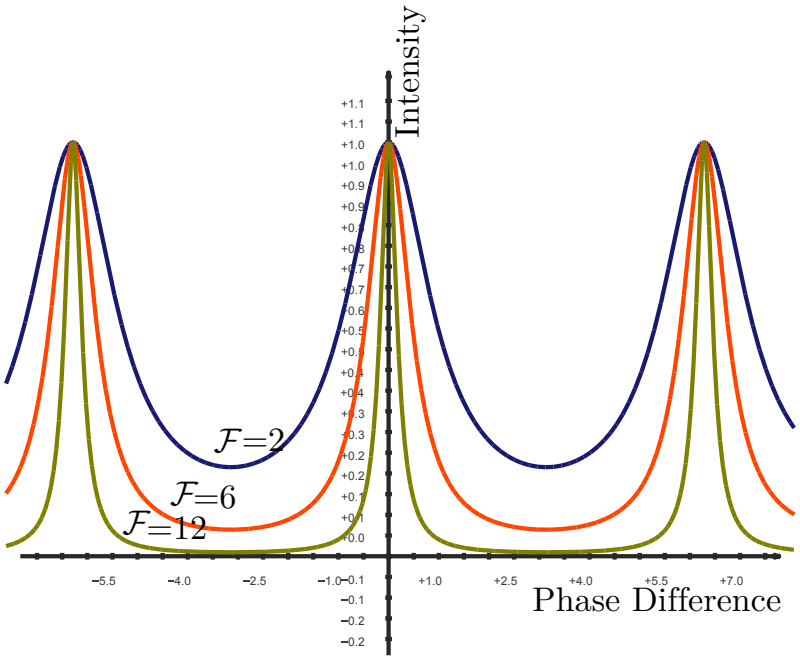


FIGURE 3.9: Transmitted intensity as a function of the phase difference in a Fabry-Perot structure. The finesse determines the shape of the resonant peaks.

The intensity transmitted by an F-P interferometer as a function of phase difference ($Delta\phi$) is displayed in Figure 3.9. Furthermore, waves of dissimilar wavelength experiences different phase shifts as they travel inside the cavity. Therefore, the transmission characteristics of an F-P interferometer as a function of wavelength will be the same as the one shown in 3.9.

3.6 Conclusion

In this chapter, the guided mode theory was presented briefly. The free plasma effect and its impact on the refractive index of silicon was also presented. In addition, the common structures used to realise the free plasma effect were mentioned. Finally, the photonic devices commonly used to realise intensity modulation in silicon photonics were highlighted. An example was provided in almost every section of this chapter to highlight the n-ZnO/p-Si electro-optical switch that was proposed in Chapter 2. The aim of these example was to demonstrate the viability of using n-ZnO/p-Si heterojunction in silicon photonics devices, particularly as an electro-optical switches. The structures mentioned in this chapter will be simulated in the following chapter, using *Silvaco Atlas* and *Lumerical FDTD*, to investigate the viability of using n-ZnO/p-Si heterojunction-based optical switches.

Chapter 4

Simulations of an Electro-Optical Switch Based on Crystalline Silicon

4.1 Introduction

In this chapter, the design and simulation of a hybrid n-ZnO/p-Si electro-optical switch are detailed. The objective of this chapter is to predict the viability of the heterojunction design and its integration with silicon photonics. The conclusions drawn from this chapter will be applied in chapters 5 and 6 where the fabrication development of the n-ZnO/p-Si optical switch is detailed. Section 4.2 details the design and structure of the proposed n-ZnO/p-Si optical switch. The section also investigates the single mode condition and the expected propagation loss for the waveguide design. Section 4.3 presents the electrical simulation results of the integrated n-ZnO/p-Si while section 4.3.3 details the electro-optical characteristics of a simple n-ZnO/p-Si optical switch. The chapter ends with a discussion on the results obtained from the simulation work. Two commercial software packages, Silvaco ATLAS and Lumerical FDTD, were used to simulate the electrical and optical response of the proposed device. In addition, the author coded a software, using C#, to facilitate the interaction between ATLAS and Lumerical FDTD: details of this software can be found in Appendix C.

4.2 Optical Switch Design

The design of a hybrid n-ZnO/p-Si electro-optical switch is discussed in this section. The input to an electro-optical modulator is a continuous electromagnetic wave on which a binary stream of data is to be superimposed. The output should reflect the superposition of the oncoming electrical binary data as shown in Figure 4.1. The structure of an electro-optical switch must enable the transition of the continuous input wave to the output, with minimal propagation loss, while simultaneously superimposing the electrical data. In order to electrically control the

output, an active electrical device, capable of inducing free carrier change, must be integrated within the waveguide structure. The electrical structure can be for example a p-n or p-i-n junctions or MOS structures.

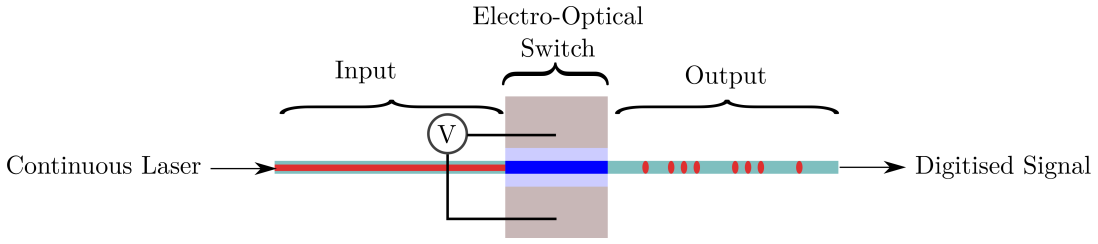


FIGURE 4.1: A schematic diagram showing the inputs and output of a typical electro-optical modulator.

Waveguide-based electro-optical switches can be realised using a ridge waveguide design (Fig. 4.2) which have two distinctive regions, namely: the core and the side slabs. The core generally has a rectangular cross-section defined by w and h_c. The side slabs are defined by their height h_s and are needed to conduct the electrical signal to the core region; hence, enabling the integration of lateral p-n junctions. The optical travelling mode should be mainly supported within the core region. Waveguides can be bent, enlarged, transformed, and periodically disconnected to facilitate certain functions. For example, the width of a waveguide is normally gradually tapered to aid in coupling into/from an optical fibre. Interference-based modulators generally require one or more transformation to enable interference of light.

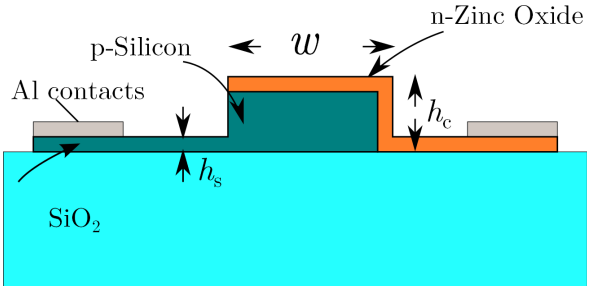


FIGURE 4.2: Cross-section schematic of a semi-lateral p-n junction integrated into a sub-micron rib waveguide.

In this project, silicon-on-insulator (SOI) wafers, with a silicon over-layer of $t \simeq 220$ nm and $N_A = 3.3 \times 10^{17}\,\mathrm{cm}^{-3}$, were available for the fabrication of the proposed n-ZnO/p-Si electro-optical switch. Therefore, in the following sections and chapters, the thickness and dopant level of the silicon waveguide core are always assumed to be 220 nm and $3.3 \times 10^{17}\,\mathrm{cm}^{-3}$, respectively, unless otherwise stated. Note that the design concerns the active area only and hence can be used in any optical configuration such as Fabry-Perot, Mach-Zehnder or straight absorption-based devices.

4.2.1 Patterning of the P-N Heterojunction Switch

The design of the proposed optical switch requires multiple fabrication steps. In each processing step, features have to be patterned to varying dimensions. There are two available patterning

techniques: e-beam lithography and photolithography.

All features would ideally be patterned using e-beam lithography because it offers high resolution (~ 5 nm) and highly accurate automatic alignment capabilities. Nonetheless, the disadvantages of using e-beam stem from these same advantages. Because of its desirability amongst cleanroom users, the waiting time for an e-beam job can be weeks. The queue on the e-beam tool does not help in a cleanroom environment where other tools occasionally break down. Furthermore, it was noted early in the project that patterning ZnO using the e-beam resist ZEP 520A imposed difficulties with the resist's adhesion to ZnO: it is not feasible to use other types of resist because of etching requirements and contamination.

Photolithography offers a much reduced resolution (~ 1000 nm) compared to e-beam lithography. However, the availability of four photolithography tools in the SNC cleanrooms means congestion is unlikely and processing proceeds smoothly from one layer to the next.

In this project, whenever time permitted, e-beam lithography was used to fabricate the waveguide layer while other layers were processed using photolithography. However, at certain points through the course of the project, photolithography had to be used with respect to time constraints. Indeed, all features of the latest batch of devices, from which was the electro-absorption switch reported here, had to be patterned using photolithography.

4.2.2 Single-Mode Zinc Oxide/Silicon Waveguides

As its name suggests, a single-mode waveguide supports the fundamental mode only. The absence of higher order modes reduces intermodal dispersion. The fundamental mode also has the lowest propagation loss. Therefore, it is important to ensure single-mode operation when designing a waveguide. Moreover, a two-dimensional strip waveguide supports at least two modes: TE_0 and TM_0.

The supported modes for a silicon waveguide of a given thickness can be identified by plotting the effective index of the waveguide structure against the width of the waveguide. Establishing the effective index of a two dimensional waveguide structure normally requires numerical solutions to the wave equation. Lumerical FDTD was used to simulate the structure shown in Figure 4.2 with the following dimensions: $h_s = 80$ nm, $h_c = 220$ nm, and $w = 220 - 1000$ nm; the width was varied to establish the relationship between the effective index and the width.

Figure 4.3 shows the three supported modes between $w = 220$ and $w = 1000$ nm. The waveguide becomes multimode when $w \geq 220$ nm. However, the waveguide strongly supports and favours the TE_0 mode. Note that the difference in the effective index between the TE_0 mode and the other two modes is greatest when $w \simeq 500$ nm. This large difference reduces the likelihood of supporting the other two modes. Therefore, the width of the electro-optical switch should be $w = 500$ nm. However, the minimum feature size achievable by the photolithography system available at the Southampton Nanofabrication Centre (SNC) is 1000 nm. Therefore, the proposed prototype optical switch has a width of $w = 1000$ nm. Table 4.1 summarises the design of the prototype n-ZnO/p-Si optical switch.

Notice that simulations showed that the inclusion of the ZnO film with thickness up to $h_{ZnO} \leq 50$ nm, as shown in Figure 4.2 has negligible effect on the refractive index plot in Figure 4.3 because

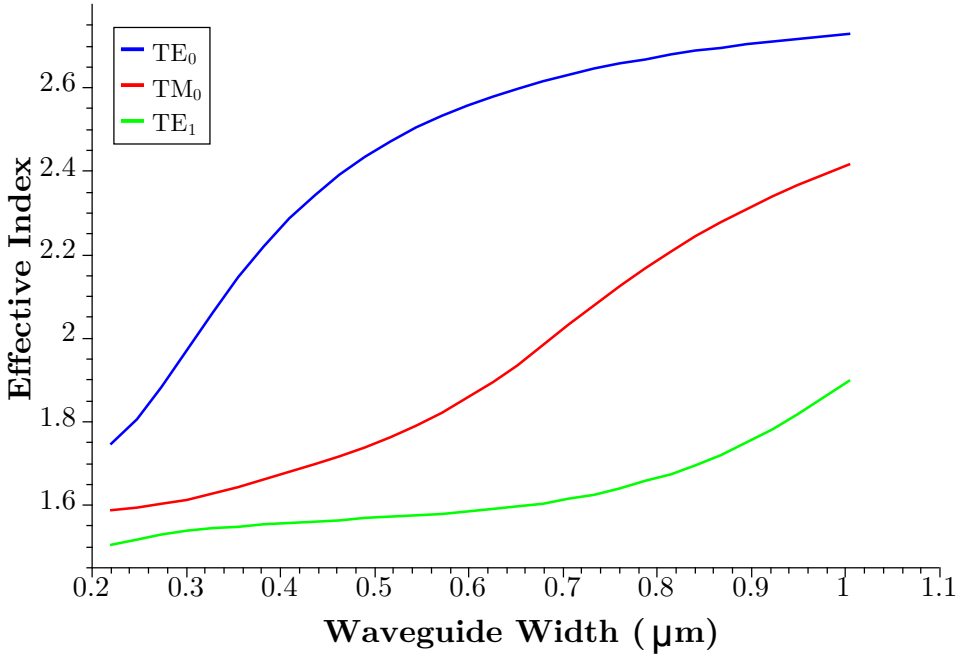


FIGURE 4.3: The effective index of the first three supported modes in a 220 nm thick silicon rib waveguide with a 10 nm layer of ZnO as a function of waveguide width.

	Value
Core Width (nm)	1000
Core Height (nm)	220
Slab Height (nm)	80
ZnO Thickness (nm)	10

TABLE 4.1: Summary of the design of the proposed prototype n-ZnO/p-Si optical switch simulated in this chapter.

of ZnO's low refractive index and thickness compared to the Si core. Nonetheless, the thickness of the ZnO layer has significant impact on the propagation loss as will be shown in section 4.4.

4.3 Electrical Simulations

Electrical simulations were performed using the two-dimensional commercial simulation package *ATLAS* from *SILVACO*. The material properties, used for the electrical simulations, of the zinc oxide (ZnO) and silicon (Si) regions are outlined in Table 4.2. Newton's method was used to solve Poission's equation for the current density within the junction. The resolution of the mesh depends on a region's dimensions. For example, the Si and ZnO regions require a high meshing resolution because most of the electrical properties change occurs in these regions. The maximum mesh size in the ZnO and Si regions was 5×10 nm. In contrast, the SiO_2 has a reasonably low meshing resolution because it only acts as an electrical isolation layer. Similarly, the Al electrodes also have reduced meshing because ATLAS only considers the working function of the metal at the metal/semiconductor interface; the spatial properties of metal beyond the metal/semiconductor interface are ignored. External biasing was performed in discrete steps

to reach the desired bias. The largest voltage step used was 10 mV in order to ensure proper conversion to the solutions.

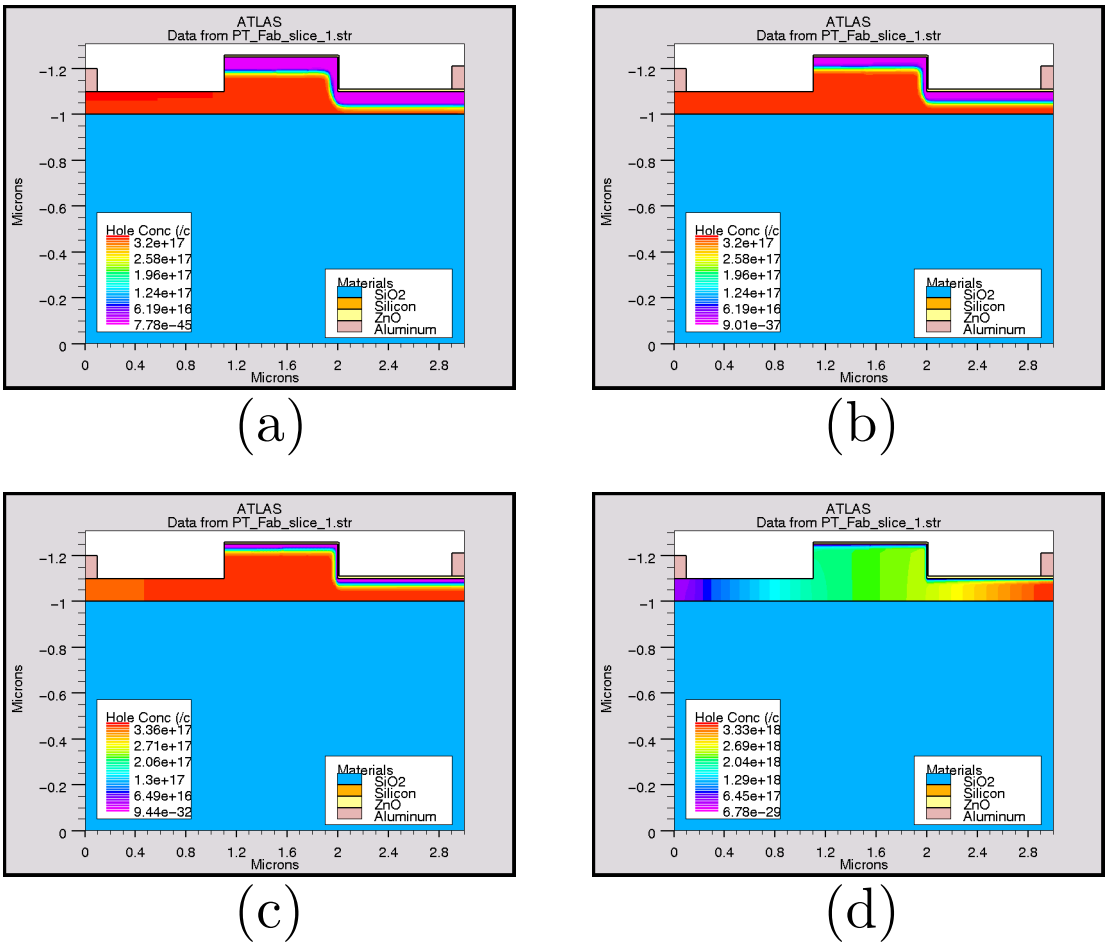


FIGURE 4.4: ATLAS simulation of the free hole concentration distribution within the n-ZnO/p-Si heterojunction under (a) equilibrium, (b) 0.5 V forward bias, (c) 0.8 V forward bias, and 1 V forward bias.

	Zinc Oxide	Silicon
Affinity (eV)	4.29	4.05
Permittivity	8.12	11.68
Donor/Acceptor Concentration (cm^{-3})	1×10^{20}	3.17×10^{17}
Mobility ($cm^2/V.s$)	5	450

TABLE 4.2: Material properties used in electrical simulations using ATLAS.

Two optical structures were investigated to produce optical simulation. The first structure relies on phase modulation and implements an integrated Fabry-Perot optical structure while the second employs optical absorption in a simple straight waveguide. The electrical structure of the Fabry-Perot electro-optical switch is essentially the same as that of the electro-absorption switch discussed in the next section. The only difference was in the dimensions of some of the heterojunction's regions. The thickness of the ZnO layer in the Fabry-Perot optical switch was 50 nm compared to the 10 nm thickness employed in the electro-absorption switch. The different thickness signifies the operation of the devices. The Fabry-Perot optical switch was designed to

operate in depletion mode where a thick ZnO layer is needed to drive free holes in the silicon waveguide away from the core region. For the injection-based electro-absorption switch, a 10 nm ZnO layer was sufficient for switching-on the device in forward-bias conditions. The second difference was the width of the waveguides. The Fabry-Perot optical switch was based on a 500 nm wide silicon waveguide while the electro-absorption switch was based on a 1000 nm waveguide. The difference in width was not intentional and was mainly a subject of e-beam availability.

4.3.1 Fabry-Perot Optical Switch

Figure 4.5 (b) shows the heterojunction when a 4 V reverse-bias is applied. The free holes has receded from their equilibrium positions, Figure 4.5 (a), towards the metal contact. Note that the slab to the right of the core region is not needed. In fact, the increased interface area between the ZnO film and the silicon region increases the capacitance of the device; hence reducing the potential maximum speed of the depletion-based modulator. Moreover, unlike the first generation switches increasing the reverse-bias voltage will further deplete the core from holes. There is approximately a 50% change in the area of the free holes profile in the silicon region.

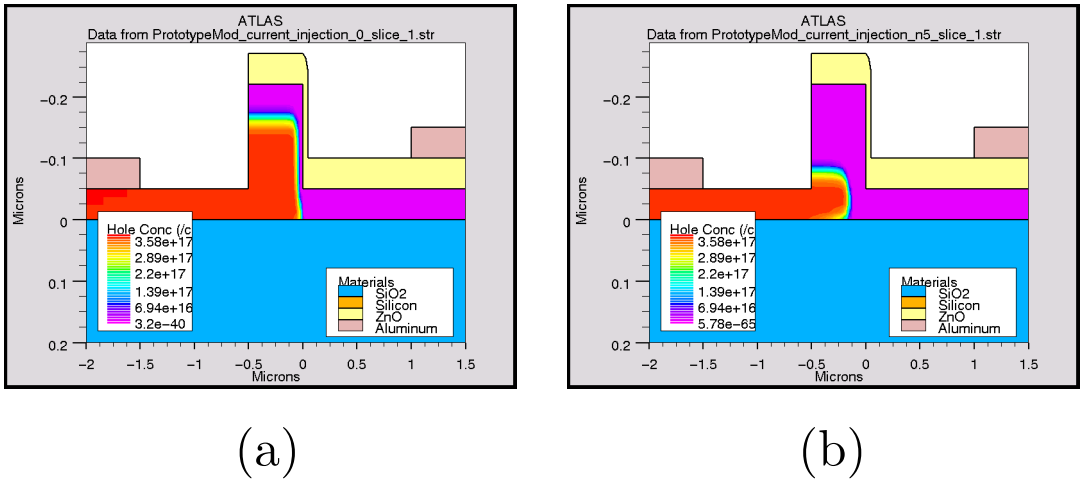


FIGURE 4.5: Evolution of free carrier (holes) change in the core as the junction is reverse biased. (a) zero biased junction. (b) 4 V reverse biased junction.

Note that the I-V characteristics of the heterojunctions used for the Fabry-Perot and electro-absorption switch are almost identical. Hence, only the I-V characteristics of the electro-absorption switch are reported in the next section.

4.3.2 Absorption Optical Switch

Figure 4.4 shows the free hole distribution simulations of the n-ZnO/p-Si heterojunction under different bias conditions. Under equilibrium conditions, 80% of the silicon waveguide core is filled with holes with a concentration equal to the dopant concentration, i.e. $n_h \simeq N_A = 3.17 \times 10^{17}$ cm^{-3}. As the junction is forward-biased, the depletion region gradually shrinks

along the core's top and sidewalls until the junction is turned on around 0.9 V at which carrier injection across the depletion region occurs. Once injection due to carrier diffusion starts, the concentration of free carriers in the core rises significantly.

Figure 4.6 shows the I-V curve of the diode shown in Figure 4.4 in the voltage range between -5 V and 1.5 V. The I-V indicates excellent diode characteristics in the forward and reverse biases. Note that the turn-on voltage was approximately 1 V which is in a good agreement with the calculations made in Chapter 3. At 1.5 V forward bias, the current passing through the junction was 1.1 A, which corresponds to a current density of 9.166×10^4 A/cm^2. The current in the reverse bias regime shows almost perfect characteristics with minimal leakage current $I_0 = 1 \times 10^{-15}$ A.

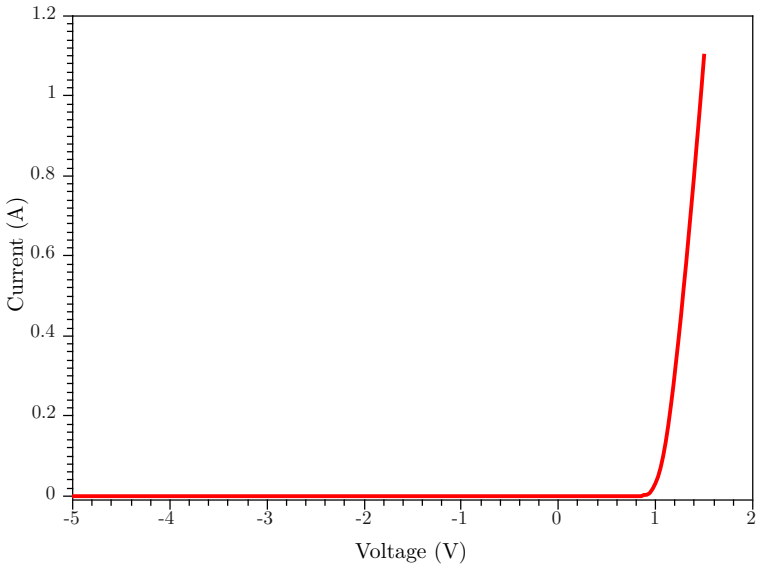


FIGURE 4.6: Simulated I-V characteristics of the n-ZnO/p-Si heterojunction shown in 4.2.

4.3.3 Electro-Optical Response of the n-ZnO/p-Si Modulator

4.3.3.1 Fabry-Perot Electro-Optical Switch

The optical response of a Fabry-Prot cavity with a length of $L = 50\,\mu$m is shown in Figure 4.7. The resonance peaks exhibit the following characteristics:

FWHM	2.06 nm
Quality Factor	2547.4583
Finesse	2.699
FSR	5.56 nm

TABLE 4.3: Resonance characteristics of the simulated Fabry-Perot optical switch.

The peaks exhibit red-shifts of $1.65 \times 10^{-3}\,\mu$m and $2.56 \times 10^{-3}\,\mu$m when the junction is reverse-biased at -4 V and -10 V, respectively. Modulation depths of 7.4 dB and 10.23 dB were calculated for -4 V and -10 V biases, respectively.

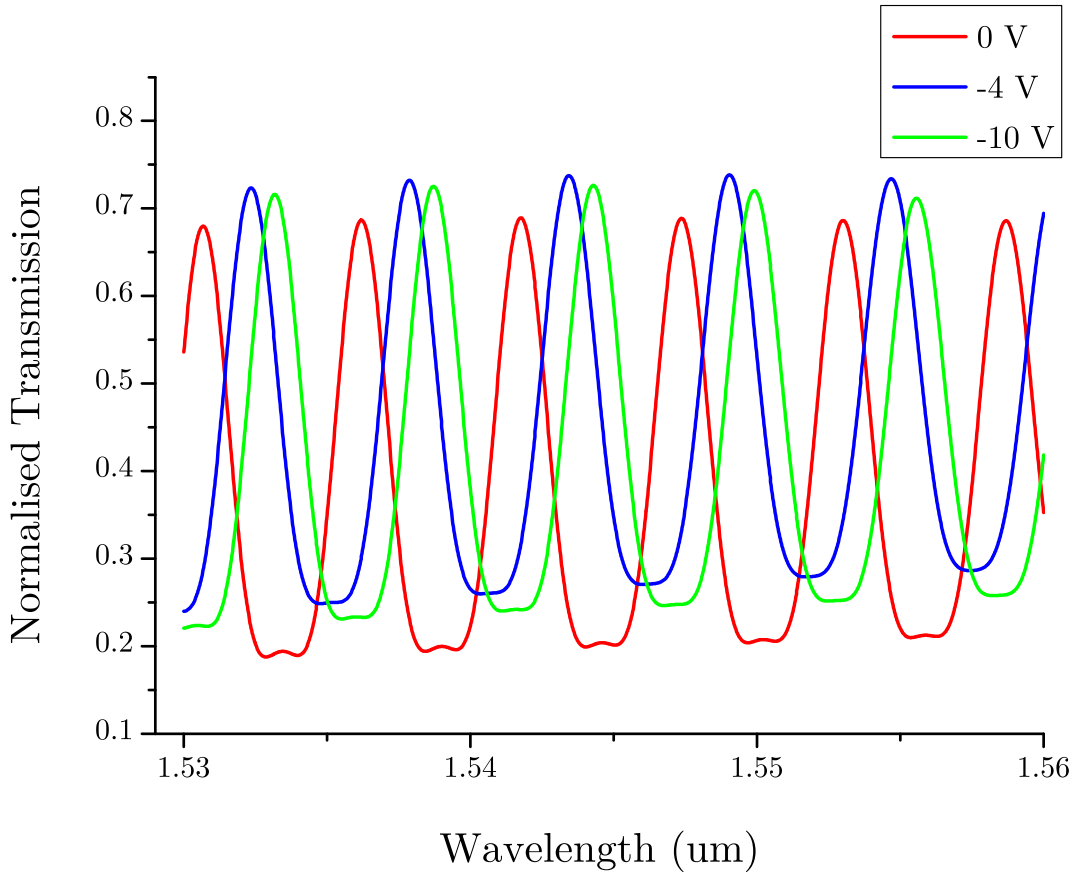


FIGURE 4.7: The simulation results of the transmission response as a function of wavelength as the hybrid-silicon switch was reverse-biased. The switch exhibited a red-shift of $1.65 \times 10^{-3}\,\mu$m and $2.56 \times 10^{-3}\,\mu$m as the heterojunction is reverse-biased at -4 V and -10 V, respectively.

4.3.3.2 Electro-Absorption Switch

The electrical simulation of the integrated n-ZnO/p-Si heterojunction device, described in sections 4.2 and 4.3, were used in to explore the device's performance as an electro-absorption optical switch. Optical simulations were performed using the commercial Lumerical FDTD 3D optical simulation package. The change in the refractive index and absorption coefficient, as a result of free carrier concentration change in the silicon regions, were computed using Equations 3.17 and 3.18. The simulation data, produced by ATLAS Silvaco, were read, interpreted, and transformed to $(n,\ k)$ data using a software developed by the author and which is called AtlasToLumerical. Details of the operation of AtlasToLumerical can be found in Appendix C.

The electro-optical response of the device can be depicted in terms of change in the insertion loss of the device as a function of forward bias. Figure 4.8 shows the effective index and insertion loss of the proposed prototype device as a function of forward bias voltage. The effective index clearly decreases as the forward bias increases. In contrast, the absorption loss increases with the forward bias. It is important to note the correlation between the change in the optical properties and the I-V curve of the device. The change in the effective index between 0 V and 1 V was $\Delta n_{eff} = 6.51 \times 10^{-3}$. The change in the insertion loss between 0 V and 1 V was $\Delta L = 116.5$

dB/cm. For a 1 mm long device, an extinction ratio of 11.65 dB can be achieved if the device was to be switched between 0 V and 1 V.

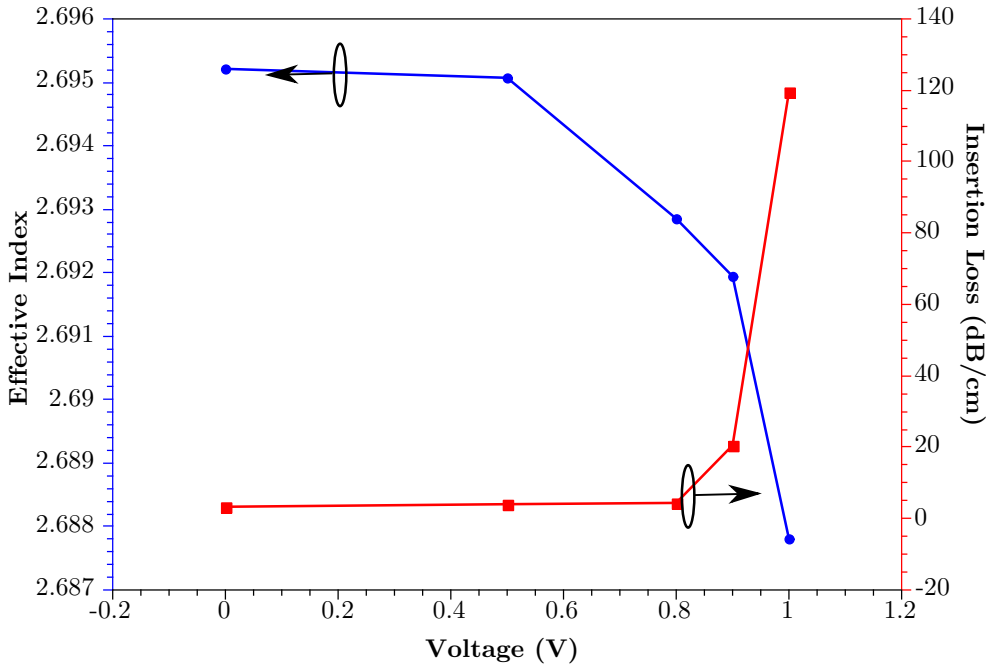


FIGURE 4.8: The refractive index and insertion loss change in the device, described in section 4.2.2, as a function of forward bias voltage.

4.4 Discussion

For absorption-based operation, the waveguide's core of an ideal device would comprise of intrinsic silicon which does not only ensure minimum optical loss when the device is in the OFF state, but it also guarantees a maximum contrast in the concentration of free carriers in the core region. However, as stated previously, the only available SOI had a silicon over-layer with $n_h \simeq 3.17 \times 10^{17}$ cm^{-3}. Operating the heterojunction in the depletion mode raises a number of issues. Firstly, a depletion device requires the utilisation of a phase-based electro-optical switch design such as Mach-Zehnder interferometer or a Fabry-Perot etalon. Mask layouts of these designs were unavailable for the over-layer thickness and operating wavelength (i.e. $\lambda = 1550$ nm). Secondly, the efficiency of depletion strongly depends on the fabrication tolerance. In the design shown in Figure 4.2, the ZnO layer stops at the left edge of the silicon core region. Unless the ZnO layer and the left edge of the silicon core were defined during the same etch step, aligning the ZnO layer to the right edge is extremely difficult. Thus, two possibilities must be considered: the ZnO layer is stopped at some distance before the core's edge; the ZnO layer extends beyond the right edge of the core. The former significantly reduced the efficiency of the device by reducing the junction area: using photolithography, alignment would still be challenging in this case. The latter leads to *pinching-off* the slab as shown in Figure 4.9.

The thickness of the ZnO layer, used in the simulated device, was only 10 nm. Increasing the ZnO's thickness leads to reduced sheet resistance according to Equation 6.1. Thick ZnO films

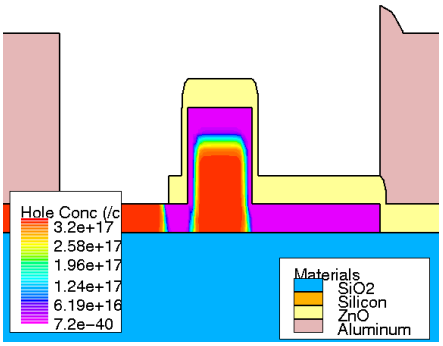


FIGURE 4.9: Pinch-off effect in a device where the ZnO layer extends beyond the left sidewall of the core while attempting to deplete the junction.

also exhibit higher free carrier concentration than those having smaller thickness: high carrier concentration is desirable as it compensates the ZnO's thickness compared to the silicon core. However, the thickness of the ZnO layer directly influences the insertion loss of the device. Figure 4.10 shows the insertion loss of the prototype n-ZnO/p-Si optical switch as a function of ZnO layer thickness: the (n, k) data for the ZnO film was obtained from ellipsometer measurement. Figure 4.11 shows a graph of the optical constants n and k as obtained from ellipsometer measurement. The difference in the insertion loss (L_i) between the case where no ZnO is used and when a 90 nm thick layer of ZnO is used to cover the top and left sidewall of the core is $\Delta L_\mathrm{i} \simeq 5$ dB/cm. Clearly, the thickness of the ZnO has a considerable impact on the insertion loss of the device. In order for ZnO to be considered for silicon photonics applications, it must induce the smallest optical loss possible. The film, from which the (n, k) data was obtained, had not been optimised in terms of the crystalline quality. In fact, all reported ZnO films deposited by atomic layer deposition (ALD) have been poly-crystalline [17, 19, 73, 72, 84, 85, 86, 71, 87]. Crystalline ZnO cannot currently be deposited on Si substrates using ALD. Even with the optimisation of the ALD process, ZnO is still believed to induce absorption loss because of the naturally high density of free carriers. Therefore, a compromise has to be made between the sheet resistance of the ZnO film and the induced optical loss by ZnO. A 20 nm ZnO film will induce a ~ 0.2 dB while exhibiting a ZnO sheet resistance of $\sim 30\,\Omega$ for the prototype device.

The width of the core has an impact on the efficiency, optical loss, and speed of the proposed device. Clearly, as the width of the device decreases, so does its capacitance which can limit the switching speed and switching power of the device [88]. For instance, the capacitance of a 500 nm wide waveguide is approximately 40% of that of a 1000 nm wide waveguide. Moreover, the width also influences the impact of the ZnO layer on the insertion loss. For example, the optical mode of a 500 nm wide waveguide has a greater interaction with the ZnO layer than that of a 1000 nm wide waveguide (Fig. 4.10). The height of the waveguide's core as well as the doping also impact the performance of the prototype electro-absorption switch. However, only one type of SOI wafers were available for the fabrication of the prototype optical switch. The slab height determines the silicon sheet resistance and affects the propagating mode. A thicker slab would result in smaller sheet resistance than a thinner one. In contrast, a thicker slab would also have a greater impact on the propagating mode than a thinner one. The capacitance of the device is proportional to the thickness of the slab. Therefore, a compromise between capacitance, sheet resistance, and impact on the propagating mode must be made. The effect

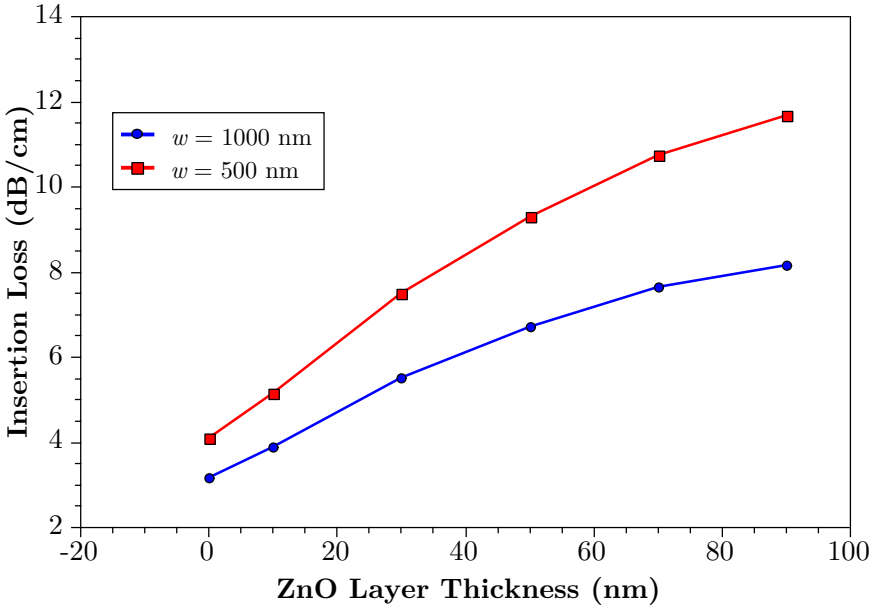


FIGURE 4.10: Effect of the waveguide's width on the impact of thickness of the ZnO layer on the insertion loss.

of the slab thickness on the capacitance, sheet resistance, and the propagating mode was not investigated in this project. The prototype optical switch design adapted a slab thickness of 80 nm: the value of the thickness is slightly greater than the normally used slab thickness of 50 nm [88, 89, 90]. However, the slab thickness, used in the prototype optical switch, was chosen to favour the reduction of the sheet resistance because of two reasons. Firstly, the distance from the Al metal contacts to the silicon core in the mask layout is 6 μm. In addition, no p^+ region can be fabricated because it would violate the low temperature processing argument of this project. Secondly, while any impacts on the capacitance and the propagating mode can be compensated for by changing the design of the core, the silicon sheet resistance mainly depends on the design of the slab of the silicon slab. Therefore, the sheet resistance was prioritised over the capacitance and the propagating mode.

4.5 Conclusion

In this chapter, the effect of the design parameters on the performance of a n-ZnO/p-Si FP and electro-absorption switches were investigated through electrical and optical simulations. However, a number of design parameters were not considered in the investigation as they were defined by the available SOI wafers. The two parameters that could not be changed were the waveguide core's height and the level of free carrier concentration. The highly doped silicon over-layer is more suited to depletion-based devices than injection-based devices. However, operating the device in the depletion mode raises issues such as the pinching-off the silicon slab and the unavailability of phase-based optical structures. The thickness of the ZnO layer was also found to have an effect on the insertion loss of the device. A compromise must be made between sheet resistance of the ZnO film and the insertion loss induced by the ZnO film. An ideal device would have a small ZnO thickness as well as a high free carrier concentration: this structure would

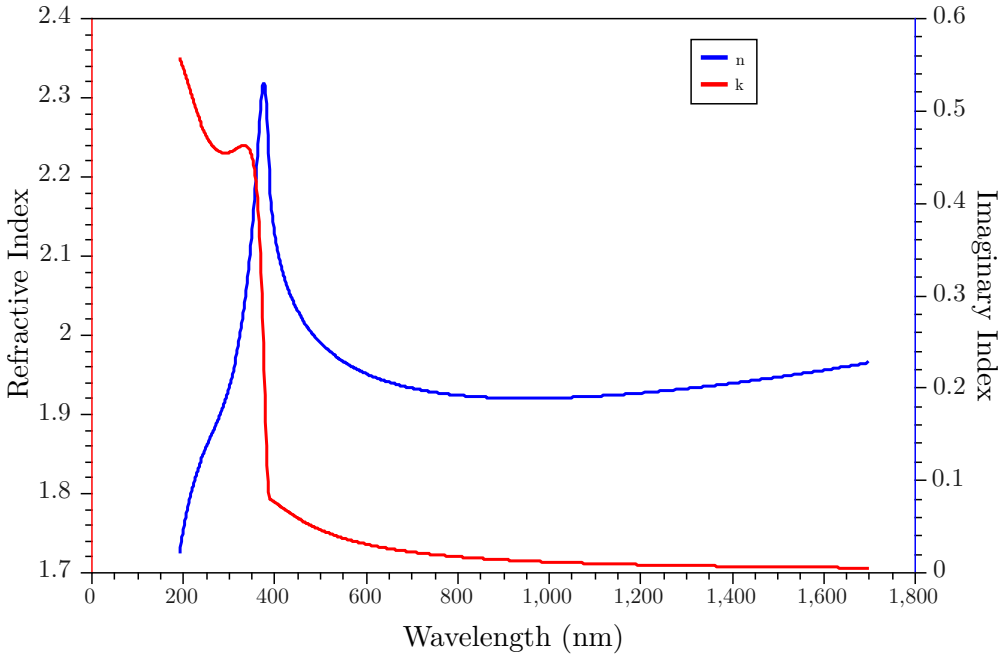


FIGURE 4.11: The real part of the refractive index (red) and the imaginary part of the refractive index (blue) as a function of the wavelength in the visible and near-Infrared range.

minimise the impact of the ZnO layer on the insertion loss while maintaining low resistivity in the ZnO film. A 10 nm thick ZnO layer with an electron concentration of $\geq 1 \times 10^{20}$ cm^{-3} constitutes a reasonable compromise. The thickness of the silicon slab also have an impact on a number of the device's characteristics such as the silicon sheet resistance, capacitance, and propagation mode. The slab thickness chosen (80 nm) favoured the sheet resistance because of its significant impact on the series resistance of the device.

Chapter 5

Development of Atomic Layer Deposition for Zinc Oxide

5.1 Introduction

This chapter aims to introduce atomic layer deposition (ALD) as an important deposition technique for multi-layered integrated optical structures. ZnO is a semiconductor that is naturally n-type doped. It can be used to form the n-type of an active device such as a hybrid n-ZnO/p-Si diode or a MOS transistor. The low absorption loss of ZnO at the telecommunications wavelengths can potentially be beneficial for the formation of electro-optical devices such as Si-based optical switches.

The chapter focuses on optimising the electrical properties of the ZnO films deposited using two variants of ALD: namely, plasma-enhanced ALD (PE-ALD) and thermal ALD (TH-ALD). The optimisation strategy employed the concept of design of experiment (DoE) to minimise the number of experiments while exploring multiple process parameters.

5.2 Atomic Layer Depostion of Zinc Oxide

Investigation of the optimal ALD process parameters for ZnO thin film deposition initiated considerable research efforts. The majority of the scientific community have been concerned with the effect of temperature [19, 84, 73, 72, 71, 85, 87, 91]. It is widely accepted that the ZnO ALD window is between 100°C and 300°C [73]. Moreover, diethylzinc (DEZ) dose time is equally important and various values have been reported [73, 72]. Nonetheless, the conclusive factor has been the use of different reagents (known as the oxidants) for the second reaction. The traditional reagent for ZnO ALD has been DI water (H_2O) and the reaction is normally thermally activated in which case the deposition process is termed thermal-ALD (TH-ALD). In plasma-based ALD, oxygen (O_2) and ozone (O_3) have also been used as oxidants. UV radiation and plasma are used as the activation methods for ozone (O_3) and oxygen (O_2), respectively [73, 72].

Before commencing with optimising the ZnO ALD process, the targeted physical quantities to be optimised must be selected. The growth rate is an important merit of any ALD process recipe. The growth rate can be used to distinguish an ALD process from a CVD process [74]; e.g. deviation from the ideal growth rate implies operating outside the ALD window. Furthermore, the electrical properties of ZnO thin film are crucial for any active device performance. The electrical properties to be monitored in the development process are carrier concentration, sheet resistance, and mobility. Finally, the crystallinity of ZnO films is an important characteristic because it can indicate the level of material-induced loss in a hybrid n-ZnO/p-Si optical switch.

The optimal conditions for the highest growth rate may not necessarily be the same as those required for the best crystalline quality. Understanding the effect of process parameters on targeted results requires comprehensive experiments and mathematical modelling, which is beyond the scope of this project. Nonetheless, preliminary conclusions and a general trend can be identified from a small set of experiments. Design of experiment (DoE) was used to create a minimum set of experiments to explore the effect of some ALD parameters.

5.3 Experimental Procedure

In the SNC cleanrooms, two ALD systems are available for ZnO deposition. The first system, FlexAl from Oxford Instruments, is capable of depositing ZnO using PE-ALD. The second system, Savannah from Cambridge Nanotech, can deposit ZnO using a TH-ALD process. Both systems were used to deposit ZnO thin films for applications in hybrid silicon optical modulators. Sections 5.3.1 and 5.3.2 detail the experimental procedure to establish the optimal ZnO deposition parameters using both methods, i.e. PE-ALD and TH-ALD.

5.3.1 Plasma-Enhanced ALD Deposition of Zinc Oxide

In a PE-ALD process, oxygen radicals, produced by O_2 plasma, are used as the second reagent (oxidant). With the use of plasma, additional process parameters, such as the RF power and plasma pressure, must be considered during the development process. There is limited information in literature on the effect of the O_2 plasma (i.e. second reaction) on the ZnO film properties. Therefore, the investigation focused on the parameters of the second reaction. The investigated parameters can be listed as:

1. Plasma exposure duration.
2. Pressure.
3. RF power.

Design of experiment (DoE) was used to create a set of experiments by which the effects of the above listed parameters on critical film properties can be identified quantitatively. A *Box-Behnken* design was used to create a set of 13 experiments [92]. The initial minimum and maximum bounds for the tested factors are detailed in Table 5.1.

The recipe parameters of the centre point (Tab. 5.2) of the DoE was based on the standard recipe devised by Oxford Instruments. Apart from the investigated factors, all other process

	RF Power (W)	Plasma Time (s)	Pressure (mTorr)
Maximum	400	10	100
Minimum	100	2	15

TABLE 5.1: Maximum and minimum values of the investigated factors in the development process of ZnO PE-ALD deposition.

parameters were kept constant as shown in Table 5.2. Note that the temperature was kept at 150°C, which lies in the middle of the expected ALD temperature window [73, 93].

Parameter	Value	Parameter	Value	Parameter	Value
Temperature (°C)	150	Dose Time (ms)	30	DEZ Purge Time (s)	2
O_2 Plasma Time(s)	4	O_2 Purge Time (s)	3	Pressure (mTorr)	80

TABLE 5.2: Standard ZnO PE-ALD recipe supplied by Oxford Instruments.

Two types of substrates were used; namely silicon and glass. The silicon samples were used to measure film thickness because of the high contrast of the optical properties between ZnO and Si. Compared to silicon, ZnO and glass have similar optical constants. Glass substrates were used for thin film electrical measurement. If the ZnO/Si samples were used in the thin film electrical characterisation, a false reading is likely due to probes penetrating the ZnO film to Si substrate.

The sample preparation procedure can be described as follows. Firstly, a 6 inch silicon wafer and a glass substrate (3×5 cm) were diced into 1×1 cm pieces. Then, the samples were ultrasonically cleaned in acetone and then IPA for an equal period of 60 seconds. The ALD deposition was carried out immediately to avoid contaminating the samples.

PE-ALD processes were carried out using the FlexAl ALD system manufactured by Oxford Instruments. The deposition process inside the FlexAl system can be described according to the schematic shown in 2.13. Prior to the start of the ALD process, the substrate is heated to a specific temperature in order to initiate chemisorptive surface reactions. Then, the first metal precursor Diethyl Zinc (DEZ) is introduced to the chamber via a fast switching valve. Driven by heat, chemisorptive bonds form on the surface between the molecules of silicon and those of DEZ. Subsequently, the DEZ valve is closed and the chamber is emptied of excess molecules, as shown in Figure 2.13 (b).

The second reaction starts after the first purging step. The second reagent, oxygen, is introduced to the chamber through a fast switching valve. Oxygen molecules react with those of DEZ to form a monolayer of ZnO on the surface of the substrate. The excess O_2 molecules and the desorbed reaction byproducts are purged in the next step. After purging, the chamber is ready to the start of the next repetition of the sequence illustrated in Figure 2.13.

5.3.2 Thermally-Assisted ALD Deposition of Zinc Oxide

In a thermally-assisted ALD process, heat is used to activate the second reagent (*cf.* plasma). In other words, the first phase reactions in both PE-ALD and TH-ALD are theoretically identical.

Two reasons led to initiate another set experiments to explore the effect of deposition parameters on the ZnO film properties:

1. The PE-ALD optimisation process focused on the parameters governing the second phase reaction.
2. The TH-ALD process is carried out using a different system (*e.g.* chamber size, temperature tolerance, precursor source *etc*).

Unlike the FlexAl, the Savannah has no mechanism by which the pressure inside the chamber can be controlled. Nonetheless, the flow rate of the carrier gas (Nitrogen) can be altered. Savannah also offers the possibility of operating the tool in the so-called *expo-mode*. The expo-mode allows efficient use of the precursor gases. In expo-mode, the valve connecting the chamber pump is closed prior to opening the precursor valve. Then, the precursor valve is opened for a short period (e.g. 15 ms). The short exposure introduces sufficient precursor into the chamber but it may not be enough for saturating the surface of the sample. Thus, after closing the precursor valve, the pump valve is kept closed for additional time (e.g. 2 s) to allow saturation of the sample's surface. In contrast, this procedure is difficult to implement using the FlexAl.

	Nitrogen Flow Rate (sccm)	Temperature (°C)
Minimum	5	140
Maximum	20	190

TABLE 5.3: Maximum and minimum values of the investigated factors in the development process of ZnO TH-ALD deposition.

A *central composite* DoE was used to optimise two deposition parameters, namely: flow rate, and temperature. Note that a Box-Behnken design requires a minimum of three factors. The investigated range is outlined in Table 5.3. The central point of the composite design was loosely based on a recipe developed by Lee, Im, and Hahn where the dose and purge times were set to 5 s and 10 s, respectively [87]. The recipe for the central point is summarised in Table 5.4.

Parameter	Value	Parameter	Value	Parameter	Value
Temperature (°C)	165	Dose Time (s)	2	DEZ Purge Time (s)	4
H_2O Exposure Time(s)	4	H_2O Purge Time(s)	10	N_2 (sccm)	12.5

TABLE 5.4: Deposition recipe for the central point in the DoE design

5.4 Results

The quality of an ALD depostion can be measured by examining a number of physical properties. Characterisation of semiconductor thin films include the material's growth rate, its free carrier concentration, and mobility. The free carrier density and mobility of the ZnO films were measured using the *Nano Metric HL5550 LN2 Cryostat* Hall measurement system.

The growth rate was evaluated using *J.A. Woollam* spectroscopic ellipsometry system (192-1700 nm) where a theoretical model was used to approximate the thickness of the film. The real (n)

and imaginary (k) parts of the refractive index can also be induced form the ellipsometer measurement. However, the primary objective of the DoE was to optimise the electrical properties of the ZnO ALD films and hence the analysis of the n and k values was not considered.

5.4.1 Characteristics of Plasma Enhanced ALD Deposition of Zinc Oxide

Zinc oxide films, deposited by PE-ALD, were characterised in terms of the following physical properties: growth rate, carrier concentration, and mobility. A surface response model was used to compile and analyse the DoE data. The following sections detail the results of the DoE.

5.4.1.1 Growth Rate

The growth rate is an important characteristic of ALD deposition because it indicates the quality of the deposition process [74]; i.e. deviation from the ideal growth rate implies operating outside the ALD window. In the DoE experiments, the growth rate ranged from 0.628 to 1.377 Å/cycle.

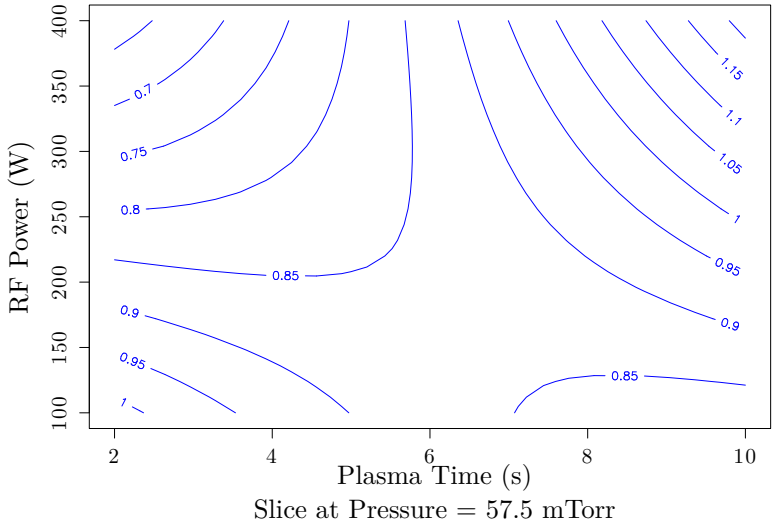


FIGURE 5.1: Surface response plot of the effect of plasma exposure time and power on the growth rate (Å/cycle). The analysis was carried out at a pressure of 75.5 mTorr.

Figure 5.1 shows that at a given constant pressure, the highest growth rate was obtained when the pressure and power were maximum. In contrast, the lowest growth rate occurred when the pressure was minimum while the power was maximum. Moreover, the contour plot implies a zero growth rate in the central region of the graph. Although possible, zero growth rate is unlikely and the central region of the plot requires further investigation. Nonetheless,the objective of the DoE was to assess the overall change in the ZnO's properties over a large range of process parameters and not to focus on a small range. Therefore, further investigation into the central region was not carried out. The overall contour plot shows a symmetry in the growth rate about the diagonal axes. The steepest ascend in growth rate occurs along the upper portion of the diagonal connecting the bottom left corner to the top right corner.

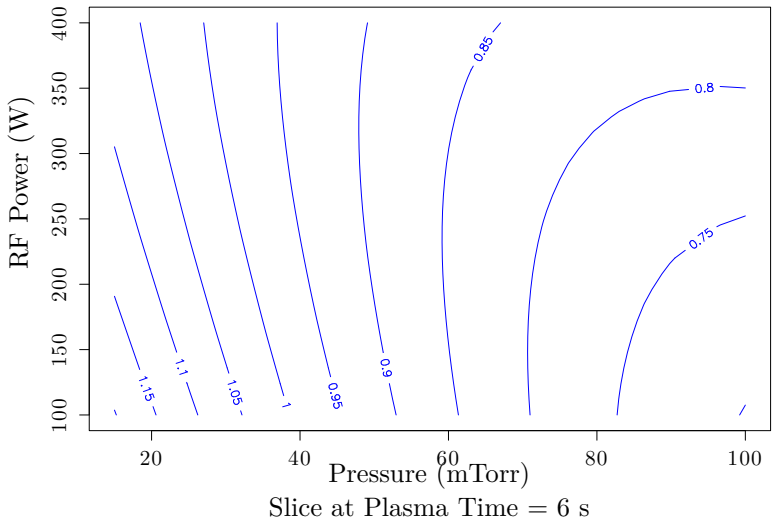


FIGURE 5.2: Surface response plot of the effect of the pressure and power on the growth rate (Å/cycle). The analysis was carried out at a plasma time of 6 s.

Figure 5.2 shows that the RF power had a negligible effect on the growth rate when the plasma exposure time was kept constant. The figure also indicates an inversely proportional relationship between the pressure and the growth rate. Furthermore, the steepest ascend in the growth rate occur at low pressures (i.e. $P \leq 40$ mTorr).

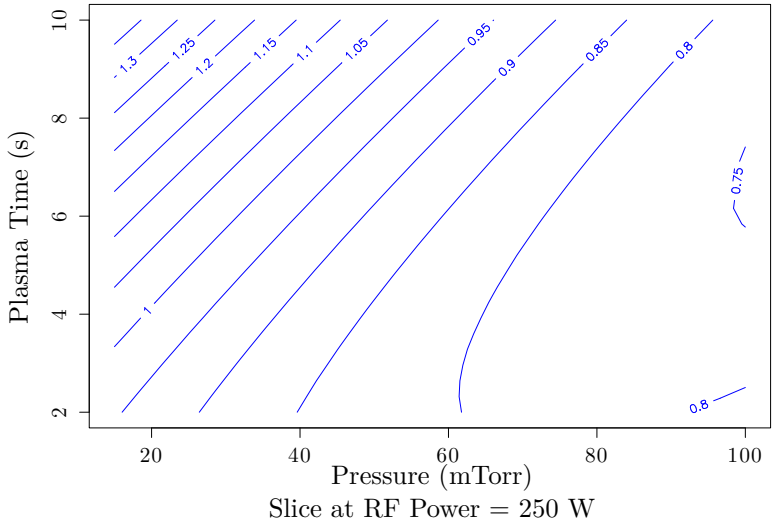


FIGURE 5.3: Surface response plot of the effect of plasma exposure time and power on the growth rate of ZnO at the central point pressure.

Figure 5.3 shows that a maximum growth rate, at a given RF power, was obtained when the pressure was minimum while the plasma exposure time was maximum. In contrast, the growth rate was minimum when the pressure was maximum and the plasma exposure time was $\sim$ 6s. The steepest ascend in the growth rate occurred in the upper portion of the diagonal connecting the bottom left corner to the top right corner of the plot.

5.4.1.2 n-type Carrier Concentration

Control over the carrier concentration of ZnO is critical to allow for more design flexibility. Generally, high free carrier concentration is desirable to minimise the sheet resistivity of ZnO films. However, a high carrier concentration may lead to an increased optical transmission loss due to free carrier absorption. For the heterojunction optical switch proposed in section 4.2, the desirable free electron carrier concentration was $\sim 1 \times 10^{20}$.

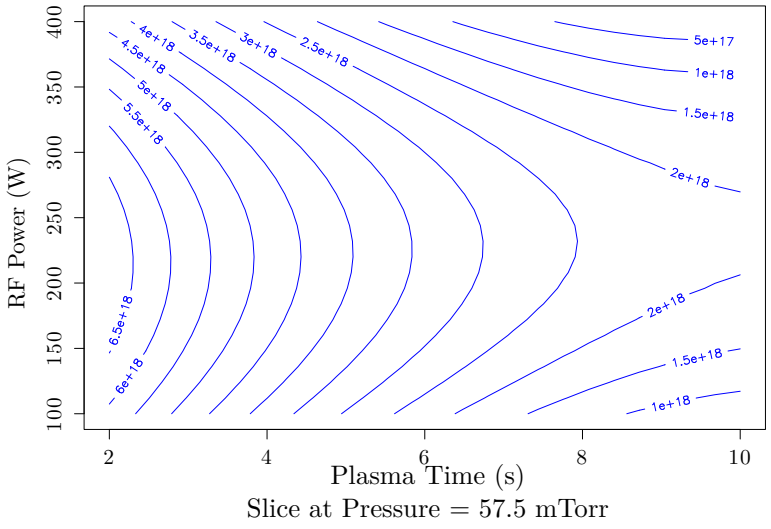


FIGURE 5.4: Surface response plot of the effect of plasma exposure time and power on the free carrier concentration. The analysis was carried out at the pressure of the central point.

Figure 5.4 shows that the free carrier concentration strongly depends on the plasma exposure time, particularly for plasma exposure times between 2 and 8 seconds. The greatest variation in the free carrier concentration ($\Delta n_e \simeq 4 \times 10^{18}$ cm^{-3}) occurred at the maximum RF power (i.e. 400 W). Furthermore, while the top right corner of the plot (Plasma = 10 s and Pressure = 400 W) shows the lowest free carrier concentration, the bottom left corner of the plot (Plasma = 2 s and Pressure = 150 W) shows the highest free carrier concentration measured.

Figure 5.5 shows a strong interaction between the pressure and power. The figure also indicates a maximum in the value of the free carrier concentration at the point (Pressure = 80 mTorr, Power = 225 W). In general, low pressures resulted in low carrier concentration while high pressures resulted in high free carrier concentration.

Figure 5.6 shows that high free carrier concentration can be obtained when the pressure is approximately 100 mTorr and the plasma exposure time is 2 s. The greatest change in the electron free carrier concentration ($\Delta n_e \simeq 7 \times 10^{18}$ cm^{-3}) occurs along the line defined by *Pressure* = 100 mTorr.

5.4.1.3 Bulk Mobility

The mobility of the ZnO film is important because it indicates the crystalline quality of the film. If the crystal grains are large and few in number, the free carrier charges will have to pass through few boundary grains (c.f. smaller crystals with more boundary grains).

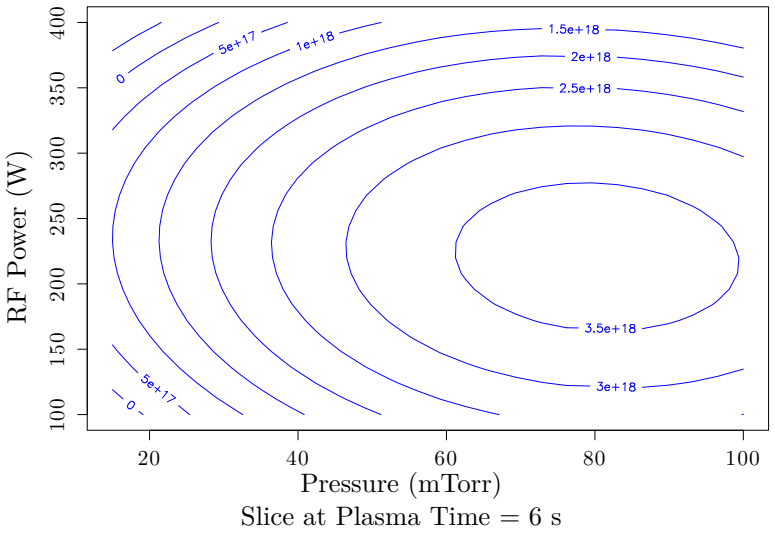


FIGURE 5.5: Surface response plot of the effect of pressure and power on the free carrier concentration. The analysis was carried out at the pressure of the central point.

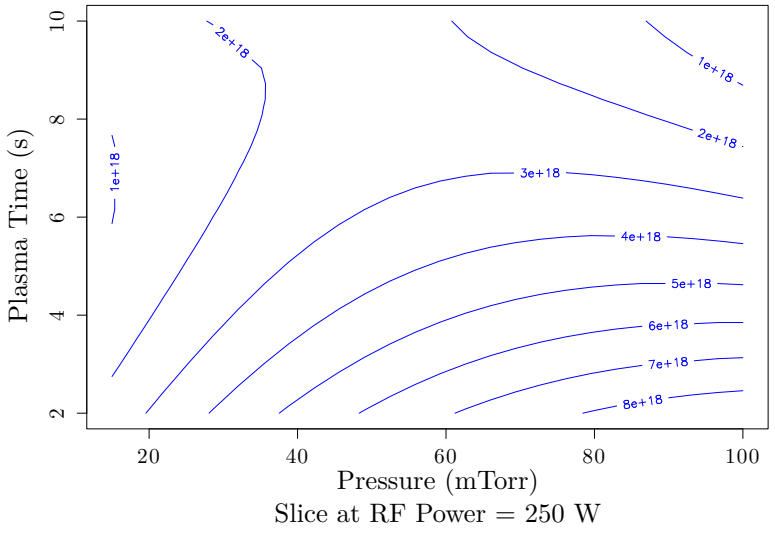


FIGURE 5.6: Surface response plot of the effect of pressure and plasma exposure time on the free carrier concentration. The analysis was carried out at the pressure of the central point.

Figure 5.7 demonstrate the effect of the plasma exposure time and RF power on the mobility. The figure shows that a maximum mobility of ≈ 4.0 cm^2/V.s can be obtained at short plasma exposure times (i.e. ≤ 4 s). The surface response plot also indicates a local minimum in mobility towards long plasma exposure times (i.e. $t \geq 6$ s). Overall, the RF power seem to have negligible effect of the mobility, particularly at left hand side of the plot (i.e. $t \leq 4$ s).

Figure 5.8 shows the effect of pressure and power on the mobility of the ZnO thin films. The contour plot shows a strong interaction between the two variables. The highest value in mobility ($\Delta\mu 2.4$cm^2/V.s) can be obtained when the pressure is at its minimum value (i.e. ≤ 20 mTorr). It is evident from the plot that low mobility values can be obtained when the pressure range is between 40 and 80 mTorr. The greatest ascend in the plot occurs along the line *Power* ≈ 225 W

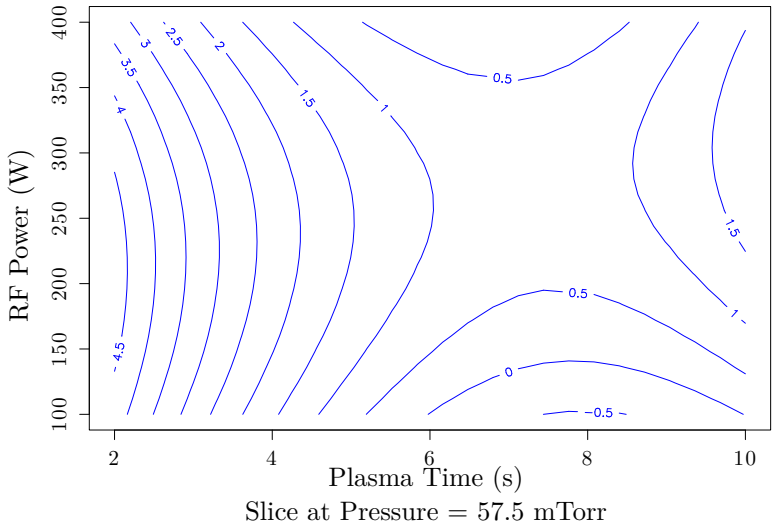


FIGURE 5.7: Surface response plot of the effect of plasma exposure time and power on the bulk mobility ($cm^2/V.s$) of ZnO.

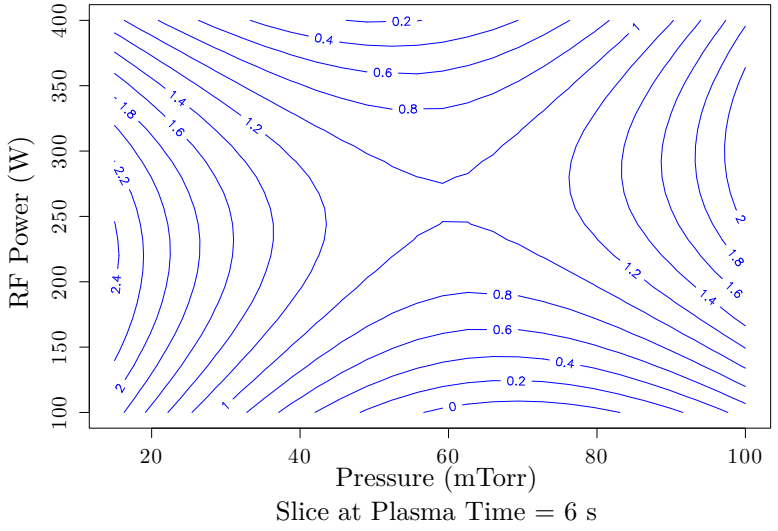


FIGURE 5.8: Surface response plot of the effect of pressure and power on the bulk mobility ($cm^2/V.s$) of ZnO.

when the pressure changes from 40 to $\leq$ 20 mTorr. Generally, pressure appears to be the decisive factor in determining the value of the mobility, assuming constant plasma exposure time.

Figure 5.9 shows the effect of pressure and plasma exposure time on the mobility, when the RF power is kept constant. The plot shows that the plasma exposure time has a stronger impact on the mobility than the pressure. The highest mobility can be obtained when the pressure and the exposure time are set to minimum (i.e. Pressure $\approx$ 20 mTorr and plasma exposure time $\approx$ 2 s).

5.4.1.4 Effect of Temperature on the Crystallinity of the ZnO Films

In order to examine the effect of process temperature on the crystallinity of ALD-grown ZnO, x-ray diffraction (XRD) measurement were obtained from four samples deposited at 100, 150,

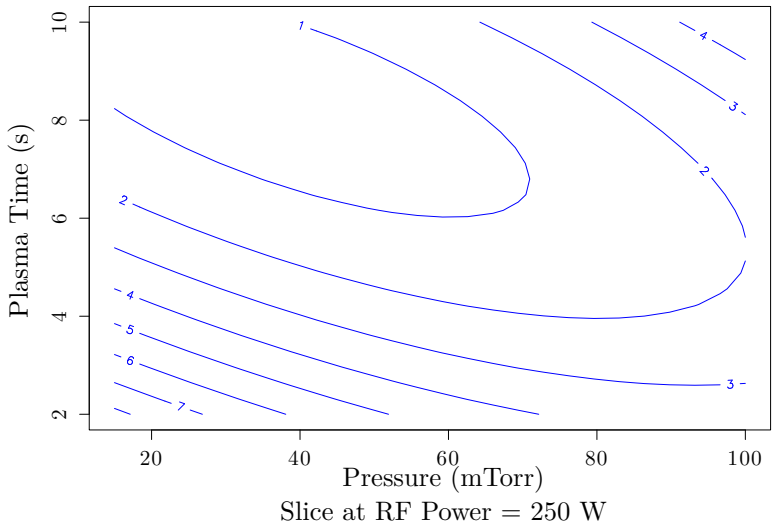


FIGURE 5.9: Surface response plot of the effect of pressure and plasma exposure time on the bulk mobility ($cm^2/V.s$) of ZnO.

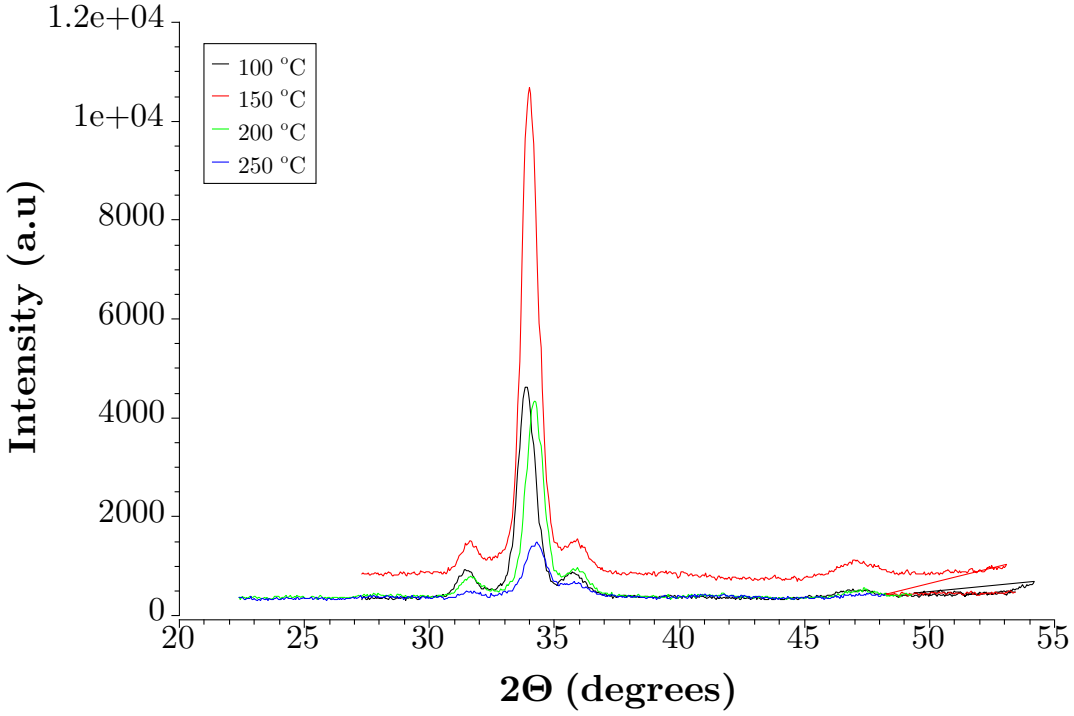


FIGURE 5.10: X-ray diffraction (XRD) spectra of ZnO films grown at several process temperatures of 100, 150, 200, and 250 °C.

200, and 250 °C. The thickness of ZnO films was approximately . The intensity of diffraction is shown in 5.10. High diffraction intensity for the central lobe and small side lobes are indicators of superior crystallinity. It can be seen from Figure 5.10 that films deposited at 150 °C have superior crystallinity than other. The figure also shows that all films have poly-grains where c-axis (002) orientation is dominant. Moreover, the worst crystallinity is exhibited by films deposited at 250 °C. Therefore, it can be concluded that the ALD window for optimal ZnO crystallinity is around 150 °C.

5.4.2 Characteristics of Thermally-Assisted ALD Deposition of Zinc Oxide

5.4.2.1 Growth Rate

Figure 5.11 shows the analysis plot of the effect of the flow rate and temperature on the growth rate of ZnO-TH-ALD. The linear response plot shows that a maximum growth rate can be obtained when the temperature and flow rate are both minimum (i.e. $T \approx 140$°C, $FR \approx 5$ sccm). Moreover, the contour lines signify a linear relationship between the temperature and flow rate for any given growth rate. For example, for a growth rate of ~ 0.215 Å/cycle, the relationship between the temperature and the flow rate can be expressed as $FR \approx -0.5T + 92$.

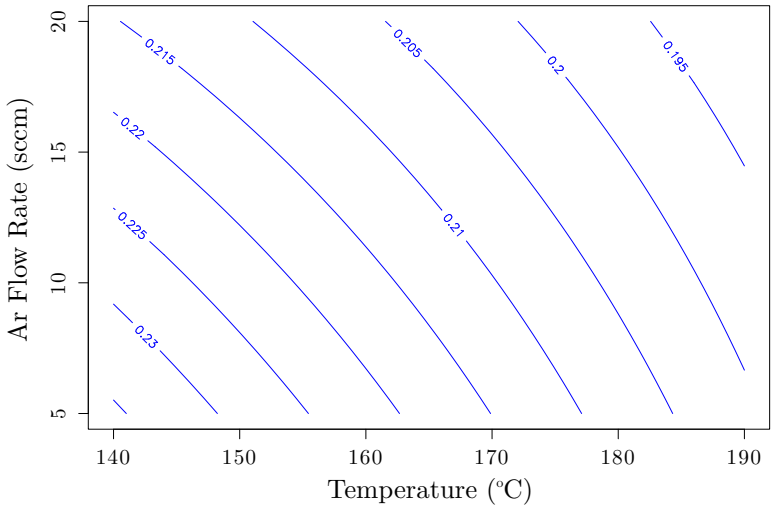


FIGURE 5.11: Linear response plot of the effect of flow rate and temperature on the growth rate of ZnO.

5.4.2.2 Free Carrier Concentration

Figure 5.12 shows the effect of the flow rate and temperature on the free carrier concentration in ZnO-TH-ALD. The region with the highest free carrier concentration ($\sim -3 \times 10^{21}$) is evidently where both temperature and Ar flow rate are minimum (i.e. $T \approx 140$°C, $FR \approx 5$ sccm). Note that this region also represented the highest growth rate in Figure 5.11. Although the relationship between the temperature and Ar flow rate for a given free carrier concentration cannot be described by a linear relationship, the overall trend resembles that of the growth rate.

In other words, the region for the maximum free carrier concentration coincides with that of the highest growth rate; this is also the case for the minimum free carrier concentration and growth rate.

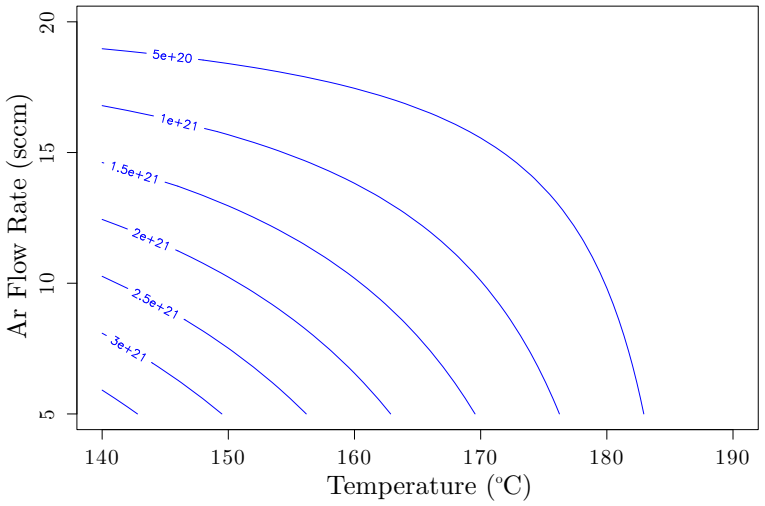


FIGURE 5.12: Linear response plot of the effect of flow rate and temperature on the carrier concentration of ZnO.

5.4.2.3 Bulk Mobility

Figure 5.13 shows the effect of the temperature and the Ar flow rate on the mobility of the ZnO-TH-ALD. The contour plot demonstrate that the highest mobility region ($\mu \simeq 12\,\mathrm{cm}^2/(\mathrm{V.s})$) is where the temperature is maximum ($T \geq 180°\mathrm{C}$) and the Ar flow rate is minimum ($FR \leq 10$ sccm). It is evident from the plot that the Ar flow rate has negligible effect on the mobility at low temperatures ($T \leq 160°\mathrm{C}$).

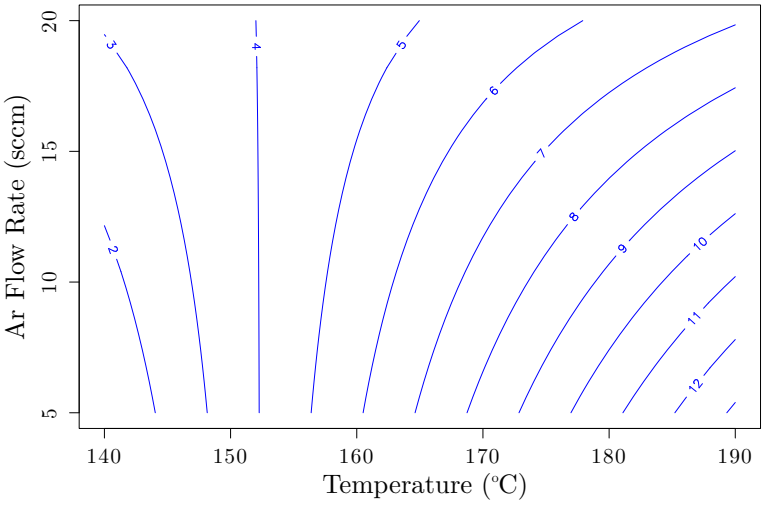


FIGURE 5.13: Linear response plot of the effect of flow rate and temperature on the mobility of ZnO.

5.5 Discussion

5.5.1 Analysis of PE-ALD of Zinc Oxide Films

5.5.1.1 Growth Rate

Figures 5.1 and 5.3 show that a long plasma time (e.g. $\sim$ 10 s) generally produces higher growth rate than a short plasma exposure (e.g. $\sim$ 2 s). A long exposure to oxygen plasma induces lattice damage to the the previously formed ZnO film. The damage is manifested by irregularities in the film topography (i.e. increased roughness) as shown in Figure 5.14. With subsequent cycles, the effect of depositing rough atomic films on top of each other is an apparent increase in the film thickness as Figure 5.16 shows. However, the density of the film is expected to be less because of the increased number of interstitial sites. Figures 5.15 (b) and 5.17 (b) show that the crystal volume fraction (CVF) of the ZnO film decreases with increasing plasma exposure time, thus indicating the existence of more voids (amorphous). On the other hand, short plasma exposures ($\leq$ 3 s) do not inflict noticeable damage to the lattice and hence the growth rate appears to be slower than that when the plasma exposure is long.

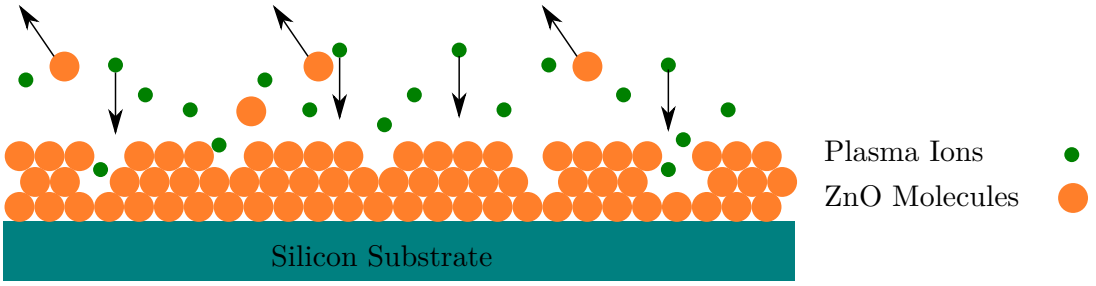


FIGURE 5.14: Schematic showing the effect of ion damage on the crystallinity of ZnO films.

The RF power seems to have little effect on the growth rate of ZnO PEALD as Figures 5.1 and 5.2 show. Nonetheless, Figure 5.1 exhibit a directly proportional relationship between the RF power and the growth rate. It is known that increasing the RF power of plasma results in an increase in the energy of the plasma's radicals. The increase in the radicals' energy lead to an increase in the net number of radicals bombarding the substrate's surface per unit time. Therefore, the outcome is similar to that of increased plasma exposure time (i.e. increase in the surface roughness and hence apparent increase in the film thickness).

Figures 5.2 and 5.3 indicate an inversely proportional relationship between the pressure and the growth rate of ZnO PEALD. This relationship can also be interpreted in terms of increased roughness. A rise in pressure increases the number of particles. Although the number of radicals having sufficient energy to reach the substrate is primarily governed by the RF power, an increase in the number of particles due to a rise in pressure will lead to an increase in the radicalisation probability (i.e. the probability of gaining sufficient energy to form energetic radicals that can reach the substrate's surface).

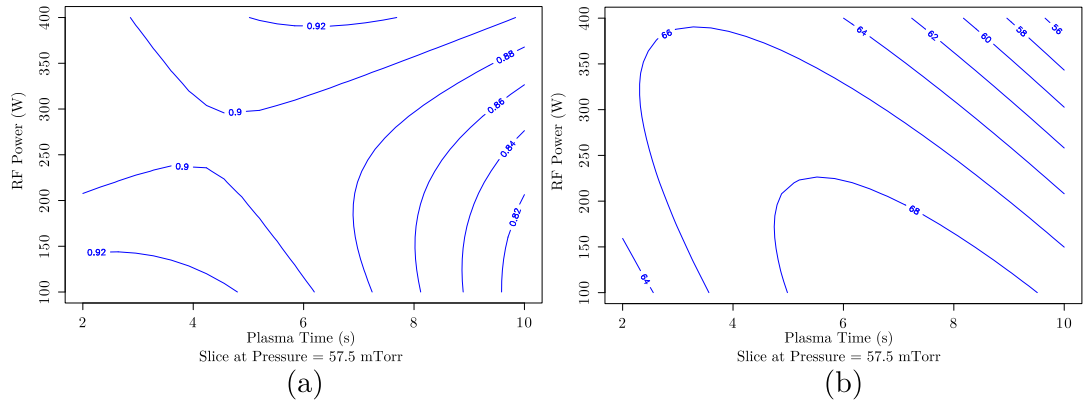


FIGURE 5.15: Effect of the RF power and plasma exposure time on the Zn/O ratio obtained from XPS measurement (a) and on the crystal volume fraction obtained from Raman measurement (b).

5.5.1.2 Carrier Concentration

A high carrier concentration is preferred because of the small thickness of the ZnO layer in the electro-optical switch design (section 4.2). The desire for high carrier concentration in the ZnO films should not undermine the fact that with increased carrier concentration, the optical absorption increases. Therefore, a control over the the free carrier concentration is crucial. For the heterojunction optical switch detailed in section 4.2, the desired free electron concentration in the ZnO layer was $1 \times 10^{20} \text{cm}^{-3}$.

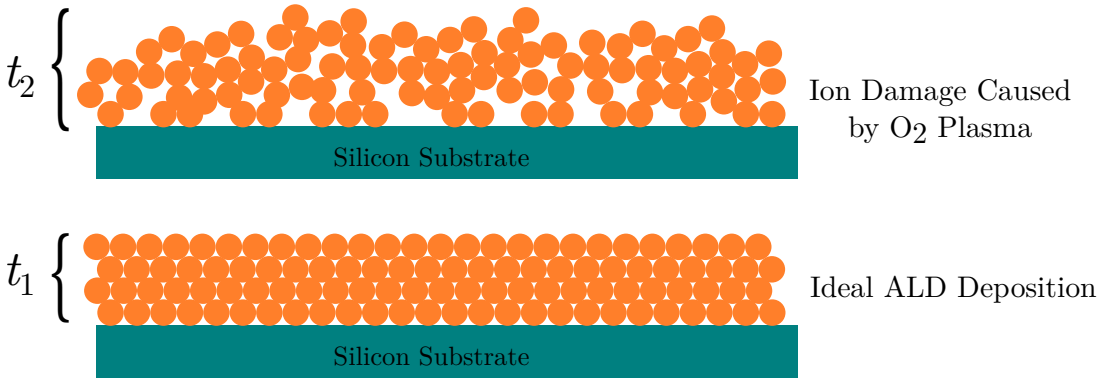


FIGURE 5.16: Schematic showing the effect of ion damage on the growth of ZnO PE-ALD films.

The fact that higher pressures produce denser films than lower pressures is reinforced in Figures 5.5 and 5.6. Voids between molecules in a denser film are fewer than those in a less-denser films (Fig. 5.16). Therefore, closely adjacent molecules result in a high free carrier density per unit volume. The CVF as a function of pressure is shown in Figures 5.17 (b) and fig:ALD:Dis:ZnOPowerPressure (b): the two figures show that high pressures (100 mTorr) produce films with a higher CVF than low pressures (20 mTorr). A film with a high CVF normally indicates high compactness and a low density of voids and hence to higher free carrier density. Note also that the Zn to O_2 ratio approaches unity at higher pressures (Fig. 5.17 (a) and 5.18

(a)). Therefore, most of zinc and oxygen atoms bond with each other and thus indicating a superior film quality and denser film.

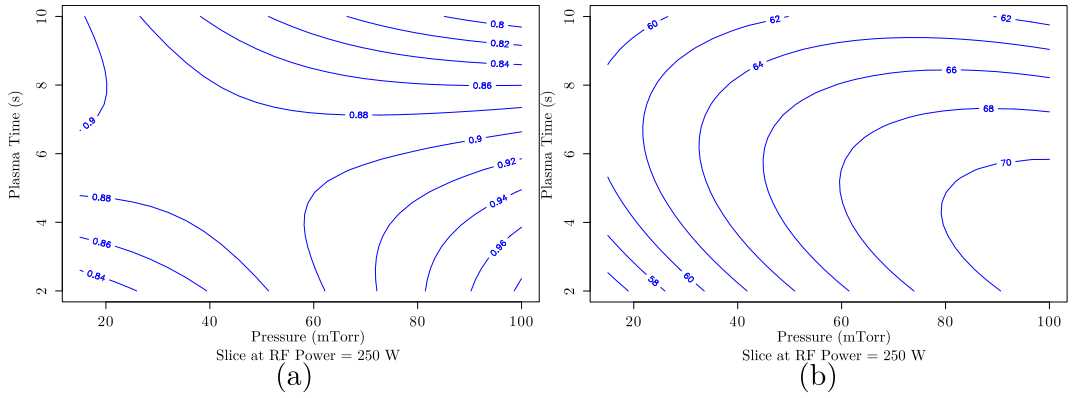


FIGURE 5.17: Effect of the plasma exposure time and pressure on the Zn/O ratio obtained from XPS measurement (a) and on the crystal volume fraction obtained from Raman measurement (b).

In Figures 5.4 and 5.5, it is evident that a power of $\sim$ 250 W produced the highest free carrier density. Although it is not physically certain why this power value produces the highest carrier concentration, it might be explained as follows. High power values might induce ion-damage (irregularities and voids) to the ZnO film and hence reduce the density (and free carrier concentration) of the film. Low power values might not be sufficiently high to break all molecular bonds of elemental oxygen (O_2). In fact, Figures 5.15 (b) and 5.18 (b) show that an increased power results in a film with a higher CVF and thus confirming the suggestion that low RF power (i.e. $<$ 250 W) is less efficient in breaking the molecular bond of oxygen.

Note also that the content of oxygen is high for low pressures and RF powers (Fig. 5.15 (a), 5.17 (a), and 5.18 (a)). This suggests that oxygen interstitial sites might be the cause of the n-type free carriers in ZnO.

5.5.1.3 Mobility

The free mean time between free carrier collisions is directly related to the mobility of a semiconductor [5]. Therefore, mobility can be used to qualitatively infer the crystalline quality of the film. High mobility values indicate low scattering probabilities. Scattering can be caused by lattice vibrations, grain boundaries, or impurities. In ZnO films, there are no impurities and the source for the n-type characteristics is not fully understood [65]. It is therefore assumed that the majority of free carrier scattering is caused by lattice vibrations, free carrier, and grain boundaries. The latter indicates the crystalline quality of the ZnO films.

The crystalline quality is not only important for the electrical characteristics of a heterojunction device but also for its optical transmission properties. Mobility indicates the ability of an electric field to affect the motion of free carriers [5]. Lower mobility values imply that the electric field has weaker effect on the movement of free charges than higher mobility values. Moreover, a low quality crystalline ZnO film has a large number of grain boundaries and irregularities in the crystal lattice. These imperfections cause optical scattering and thus increase the optical transmission loss.

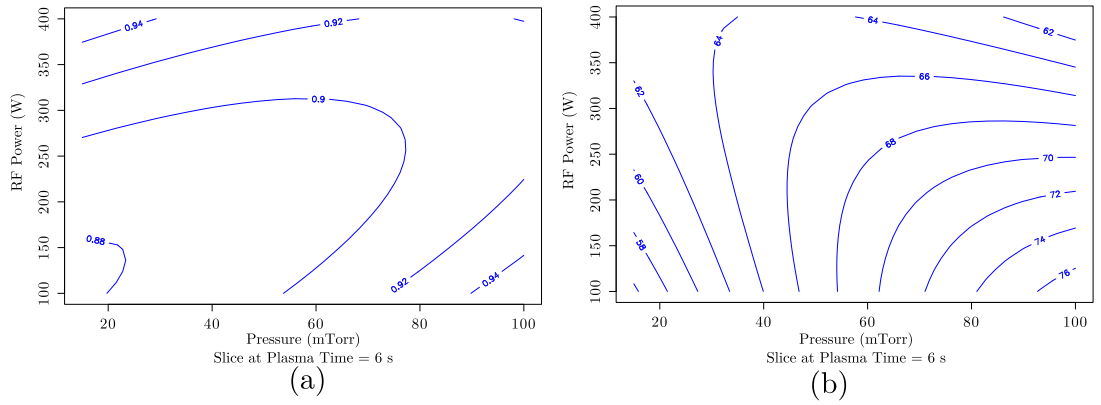


FIGURE 5.18: Effect of the RF power and pressure on the Zn/O ratio obtained from XPS measurement (a) and on the crystal volume fraction obtained from Raman measurement (b).

Figures 5.7 and 5.3 indicate that lower plasma exposure time resulted in higher mobility than longer exposure times. Notice that these regions also specify high carrier concentrations. Low mobility indicates damaged lattice films which is believed to be caused by long plasma exposure times (Fig. 5.14). This is confirmed by the Raman measurement and the CVF analysis shown in Figures 5.15 (b) and 5.17 (b).

Figures 5.9 and 5.8 show that lower pressures result in a slightly improved mobility over higher pressures. Generally, pressure appears to have low impact on the ZnO's mobility. In a polycrystalline film, mobility is affected not only by the level of free carrier concentration but also by the crystalline quality (i.e. concentration and size of polycrystalline grains).

As the pressure increased from 80 to 100 mTorr, the free carrier concentration also increased (Fig. 5.6 and 5.5); while the crystalline quality also improved (Fig. 5.17 (b) and 5.18 (b)). Although mobility is inversely proportional to the level of free carrier concentration, the results suggest that the improvement in mobility due to improved crystalline quality outweighs the deterioration in mobility caused by increased free carrier concentration [5]. In the low pressure region between 20 and 40 the reverse effect occurs (i.e. the improvement in mobility due to the decline in the free carrier concentration outweighs the deterioration in mobility due to the decline in the crystalline quality of the film).

It is worth noting that mobility increases when the oxygen content in a ZnO film increases. This can be explained by size of oxygen and zinc atoms. The radius of a zinc atom is approximately 135 pm, while that of an oxygen atom is 60 pm [94]. The smaller size of oxygen atoms means that the free mean path of free carriers is reduced and more collisions occur.

5.5.2 Analysis of TH-ALD of Zinc Oxide Films

Figure 5.11 shows an inversely proportional relationship between the carrier gas's flow rate and the temperature. The slightly increased growth rate at low temperatures in Figure 5.11 is believed to be caused by precursor condensation (or physisorption) as in Figure 2.14. In the other hand, the flow rate controls the residence time of the precursor's molecules inside the chamber. High flow rate, under constant chamber pressure, results in precursor molecules being pushed

out of the chamber as new mass of precursor is fed into the chamber. Therefore, precursor molecules have insufficient duration to saturate the substrate's surface which consequently leads to a reduction in the growth rate.

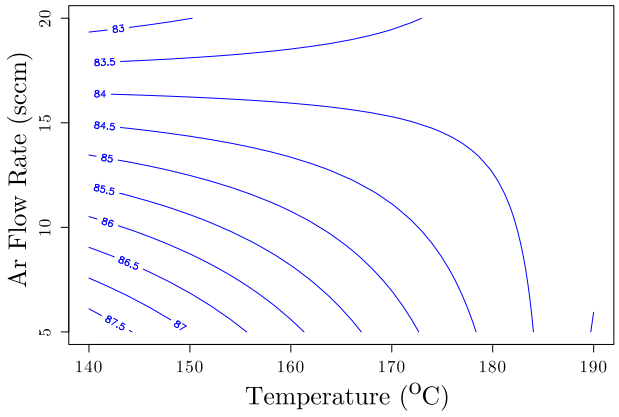


FIGURE 5.19: Schematic showing the effect of ion damage on the crystallinity of ZnO films.

Notice that the free carrier concentration in Figure 5.12 shows similar pattern to the growth rate in Figure 5.11. Specifically, the region where temperature and flow rates were minimum, the free carrier concentration and growth rate exhibit maxima. Contradictory to Figure 5.12, it is widely believed that the free carrier concentration of ZnO is proportional to the temperature. This contradiction can be explained as follows. In order to determine the growth rate and ensure consistency in the development process, all deposition experiments were ran for 250 cycles. Furthermore, because the growth rate was different, some ZnO films were inevitably thicker than others; this is reflected in Figure 5.11. It is known that thicker films exhibit higher free carrier concentration than thinner films [95]. The free carrier concentration measurement could have been different if the all films had exactly the same thickness.

Figure 5.13 shows that the highest mobility values was obtained at the highest temperatures. The flow rate seemed to have negligible effect, particularly at low temperatures (i.e. $T \leq 160\,^{\circ}\mathrm{C}$). Note that at high temperatures ($\sim 190\,^{\circ}\mathrm{C}$) the free carrier concentration is high, mobility and free carrier concentration are inversely proportional; this explains the pattern seen in Figure 5.13. However, Figure 5.19 shows that the CVF decreases as the deposition temperature increases. Although this observation contradicts the generally expected enhancement in crystal quality as the deposition temperature increases, the reactions that occur at temperatures higher than $170\,^{\circ}\mathrm{C}$ are expected to be CVD-like (not ALD). Thermal ALD has a narrow ALD window (Fig. 2.14). The flow rate in Figure 5.19 also shows a counter-intuitive pattern. While the CVF is expected to increase with higher flow rates, it decreases as the flow rate increases. Again, this might have been caused by CVD-like reactions and not ALD reactions.

5.5.3 PE-ALD Versus TH-ALD

Both methods (PE-ALD and TH-ALD) show a reasonable degree of controllability over the electrical properties of ZnO films. Table 5.5 provides a summary of the achieved ranges for the growth rate, free electron concentration, and mobility using PE-ALD and TH-ALD. Thermal ALD appears to generally result in larger values than Plasma-Enhanced ALD for all examined

quantities. While the growth rate of the TH-ALD process closely match those reported in literature, the growth rate for PE-ALD appears to be less than expected [84, 87]. In fact, the growth rate of the PE-ALD process should be greater than that of TH-ALD: the expected growth rate range for PE-ALD is $2 - 2.75$ Å/cycle [84]. The cause for the low deposition rate for the PE-ALD is unknown but it could have been caused by deposition parameters that were not investigated such as the DEZ pressure and dose time.

	PE-ALD	TH-ALD
Growth Rate (Å/cycle)	$0.7 - 1.3$	$1.95 - 2.3$
Free Electron Concentration (cm^{-3})	$5 \times 10^{17} - 8 \times 10^{18}$	$5 \times 10^{20} - 3 \times 10^{21}$
Mobility (cm^2/V.s)	$0.2 - 7$	$2 - 12$

TABLE 5.5: Achieved ranges for growth rate, free electron concentration, and mobility using PE-ALD and TH-ALD.

According to Table 5.5, the free electron concentration is always higher for TH-ALD than PE-ALD processes. In other words, the maximum density level of electron in PE-ALD processes is less than the minimum density of electrons in TH-ALD processes. Indeed, previous studies showed that TH-ALD produces higher free carrier concentration than PE-ALD in ZnO films [84]. In a previous study, it was found that interstitial oxygen states are higher in PE-ALD processes than in those of TH-ALD [84]. It is also believed that interstitial oxygen states act as an electron compensator [84]. Therefore, the low free electron concentration in PE-ALD ZnO films can be attributed to high levels of interstitial oxygen states.

Thermal-ALD showed a slightly higher mobility average than plasma-enhanced ALD. The maximum achieved mobilities with TH-ALD and PE-ALD were 12 and 7 cm^2/V.s, respectively. High mobility is desirable and hence TH-ALD would result in a superior device characteristics than PE-ALD. Note also that the bulk mobility can be as low as 0.2 for the PE-ALD process. The cause of inferior mobility for PE-ALD is unknown but it closely matches observations in another study [84].

The desired electrical properties of ZnO films were outlined in Chapter 4. From Table 5.5 and the discussion above, it was concluded that TH-ALD results in properties that are more suitable for the formation of a n-ZnO/p-Si heterojunction. Moreover, the FlexAl ALD tool has a rich history of developing faults especially within the vacuum system: this has resulted in changes in the processing outcomes. On the other hand, the Savannah ALD tool appears to be stable and processing outcome is more consistent than that of FlexAl. Therefore, TH-ALD was selected for the fabrication of the hybrid n-ZnO/p-Si electro-optical switch. The only drawback of using TH-ALD is its small ALD windows shown in Figure 5.20 where it is evident that at high temperatures (i.e. $T > 180°C$), the process become CVD like because of precursor decomposition (Fig. 2.14). At low temperatures (i.e. $T < 130\,°C$), the thermal energy is insufficient to activate surface reactions. Therefore, in the fabrication of the n-ZnO/p-Si heterojunction optical switch, a temperature of 150 °C was chosen because it lies inside the ALD window.

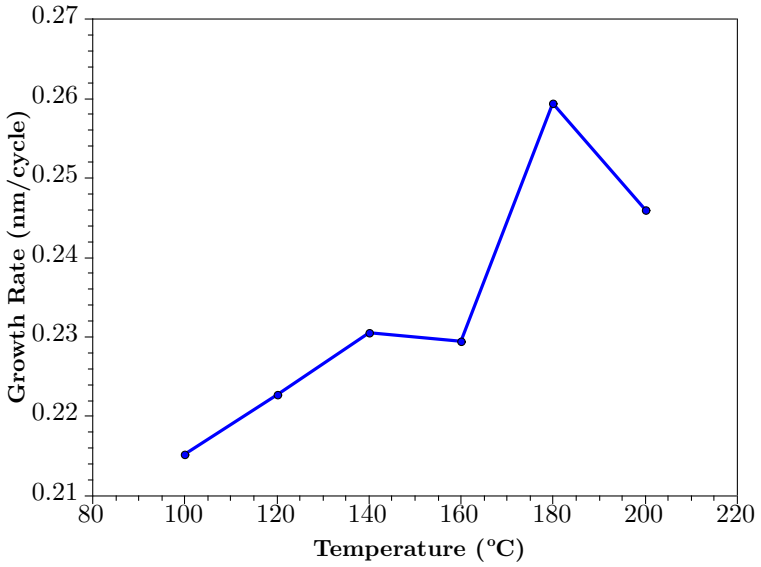


FIGURE 5.20: Growth rate of TH-ALD as a function of temperature. The ALD window seem to fall between 140 °C and 160 °C.

5.6 Conclusion

The effect of some of the deposition parameters of ALD on the electrical properties of ZnO films has not been investigation sufficiently in the scientific community. The availability of two different deposition systems/methods in the SNC cleanrooms required a detailed examination of the deposition parameters/recipes to establish which system/method meets the requirements for the fabrication of a n-ZnO/p-Si electro-optical switch. The parameters of significance for each deposition methods and the targeted electrical properties to be optimised were identified. Then, the design of experiment (DoE) methodology was used to devise and analyse the effect of deposition parameters.

The analysis of the results showed that TH-ALD resulted in superior electrical film properties than PE-ALD. Furthermore, the fact that the TH-ALD deposition system (Savannah) was more stable than FlexAl (PE-ALD deposition system) reinforced the conclusion to use TH-ALD for the fabrication of the hybrid n-ZnO/p-Si electro-optical switch.

Chapter 6

Electro-Optical Switch Based on Crystalline Silicon

6.1 Introduction

In this chapter, the design and characterisation of a hybrid n-ZnO/p-Si electro-optical switch are detailed. The objective of fabricating a hybrid silicon-based electro-optical modulator was to demonstrate the viability of using ZnO in silicon photonics applications. In particular, ZnO is a low optical loss material at $\lambda = 1550$ nm that can be deposited at low temperatures. For CMOS back-end integration, low temperature deposition materials are attractive because they are compatible with the existing fabrication processes. Moreover, ZnO can be particularly useful for future multi-layered silicon photonics platform. Because ZnO is naturally highly n-type doped, artificial doping and activation through high temperature processing is unnecessary.

The chapter starts by presenting the device structural design. Then, the experimental procedure used to fabricate the electro-absorption switch is highlighted in section 6.3. After that, the characterisation results are outlined in section 6.4. Finally, the results are discussed and summarised in sections 6.5 and 6.6.

6.2 Optical Switch Design

A schematic view of the cross-section of the prototype crystalline silicon electro-absorption switch is shown in Figure 6.1. The core width for the Fabry-Perot (FP) prototype switch was 500 nm while that for the electro-absorption switch was 1000 nm. The two devices had the same core and slab thickness, 220 nm and 80 nm, respectively. The thickness of the zinc oxide (ZnO) layer was ≈ 50 nm and ≈ 10 nm for the FP and electro-absorption switches, respectively. The metal contacts were 6μm away from the core on either side.

It is acknowledged that a 1000 nm wide and 220 nm height waveguide is multi-mode (Fig. 4.3). However, the utilisation of photolithography system (EVG 620T) available in the SNC

cleanrooms at the time of fabrication limits the minimum feature size to approximately 1000 nm, especially with small chips.

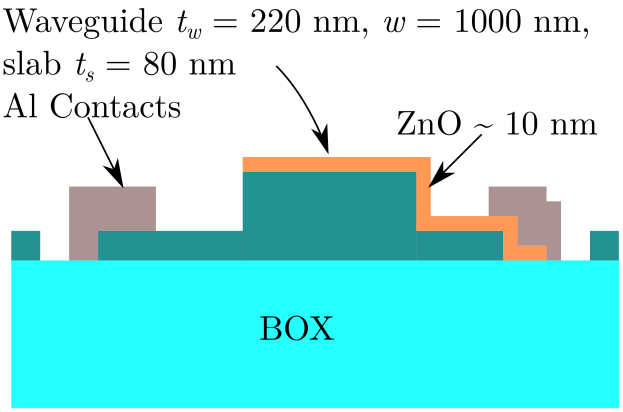


FIGURE 6.1: Cross-section of the default design of the n-ZnO/p-Si electro-optical switch.

The ZnO film starts from the edge of the core and ends in the contact area, forming the n-type region of the integrated n-ZnO/p-Si diode. In this experiment, the device design is not ideal for depletion operation because minor errors in the fabrication could lead to *pinching-off* the silicon slab and hence preventing efficient carrier movement as described in Chapter 4.

6.3 Experimental Procedure

6.3.1 Sample Preparation

Samples (1.5×1.5 cm) from an SOI wafer with a silicon overlayer of 220 nm and a BOX layer of 2000 nm were used. The overlayer was p-typed doped to approximately $3 \times 10^{17}\text{cm}^{-3}$. Prior to patterning the first layer (forming core/slab of the waveguide), the samples were cleaned using FNA. Moreover, the samples were given an adequate dip (20 s) in HF 20:1 before depositing the ZnO layer. The samples were also oven-baked at 210°C for at least 10 minutes to evaporate moisture before spinning resists; the adhesion of certain resists such as the AZ 701MiR are particularly prone to H_2O moisture in the samples. In these instances, an adhesion promoter (TI-prime) was used.

6.3.2 Overall Process Flow

The fabrication process of the optical switch is illustrated in Figure 6.2. The waveguide for the FP optical switch were defined using e-beam lithography using the positive tone resist *ZEP 520A*. Recipe details of using ZEP 520A can be found in table in A.4 Appendix A. Photolithography was used to pattern the waveguides instead of e-beam lithography because of time limitations. A photoresist, *S1813*, was spun at 6000 rpm for 30 s on a SOI sample (1.5×1.5 cm). The waveguide features were then transferred to the photoresist using EVG 620T photolithography aligner system. For full details of the photolighography recipe, please see section A.1.0.1.

The waveguide pattern was transferred into the silicon using conventional reactive-ion etching (RIE) techniques. The RIE silicon etching recipe is summarised in Table A.8. After dry etching, the ZEP 520A/S1813 photoresist was stripped using the Tepla asher; the plasma ashing recipe can be found in Table A.10. The waveguide had widths of approximately 490 nm and 1170 nm for FP and electro-absorption switches, respectively. Figure 6.3 shows an SEM image of a 20 μm Fabry-Perot cavity fabricated using e-beam lithography.

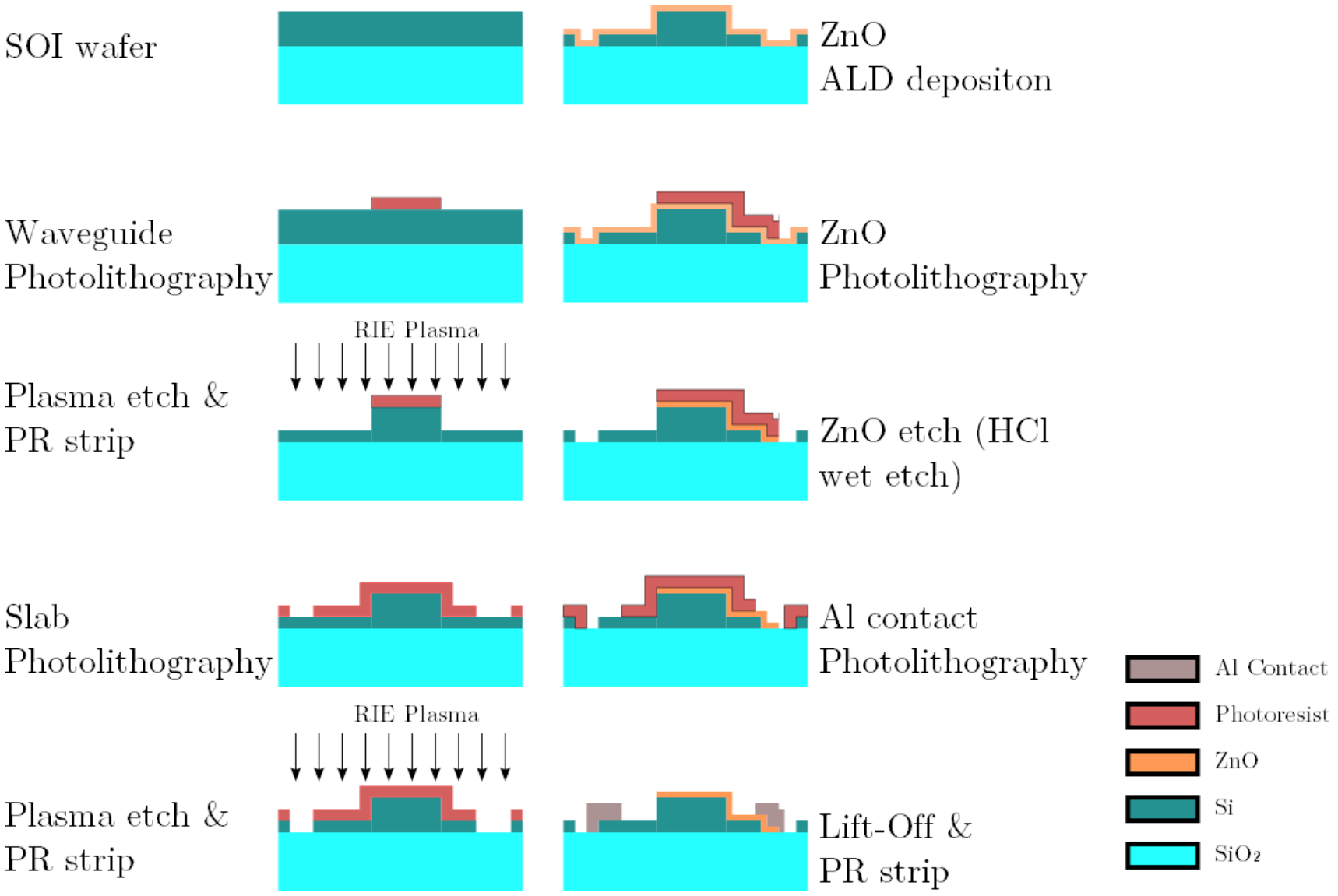


FIGURE 6.2: Fabrication steps for the c-Si based electro-optical switch.

Following the definition of the silicon waveguides, an isolation region was also defined using photolithography to improve the electrical and optical isolation between the two sides of the junction (Fig. 6.4). The isolation regions ensure that the silicon and ZnO layer overlap only around the waveguide core and that the active part of the silicon slab is confined to the area beneath the metal contacts. The silicon etch into the slab region was realised using the default RIE silicon-etch recipe; the slab was etched for 60 seconds to ensure complete removal of the silicon slab.

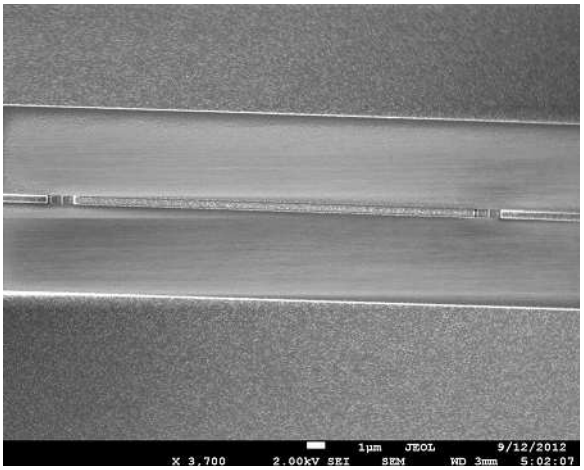


FIGURE 6.3: SEM image of a 20 μm Fabry-Perot cavity in a single mode silicon waveguide. The waveguide and Bragg gratings were defined using e-beam lithography.

Then, the sample was dipped into an HF (7 : 1) acid for $\sim$ 5 seconds to remove all the native oxide on the silicon waveguide prior to ZnO deposition. Then, a thin layer (50 nm and 10 nm) of ZnO was deposited using Savannah ALD at 150°C. The deposition rate was $\sim$ 0.2 nm/cycle: for details, please see Chapter 5. The ZnO features were then defined using photolithography and wet etching. HCl, diluted in water (180 : 1), was used to transfer the pattern to the ZnO. For details on the HCl etch recipe and characteristics, please see Table A.7.

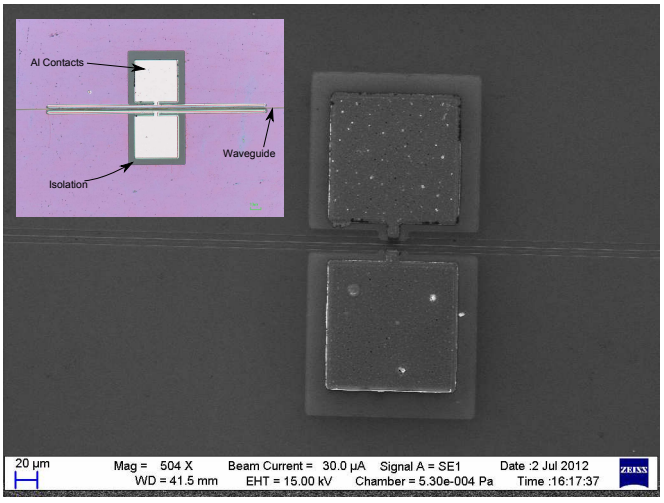


FIGURE 6.4: SEM image of the smallest electro-absorption switch $L = 10$ μm. The inset shows a microscopic top view of the 500 μm optical switch. The SEM shows how the ZnO layer unintentionally extends beyond the silicon core.

Later, a 500 nm layer of aluminium (Al) was deposited using *Leybold BAK* 600 evaporator to define the metal contacts. The metal contact features were defined using a negative tone photoresist *AZ*2070: details of the processing recipe can be found in Table A.3. NMP solution was used in the lift-off process of Al. Finally, the sample was diced at the start and end of the waveguide devices and then polished using the recipe outlined in Table A.4.

6.4 Results

In this section, the characterisation results of the fabricated device are outlined. The results include the sheet resistance of the silicon slab and ZnO film, the contact resistance between the metal (Al) and both the Si and ZnO, the I-V characteristics of the hybrid n-ZnO/p-Si junction, and the electro-optical response of the devices. Note that the sheet resistance and contact resistance results applies to both the FP and electro-absorption devices because the same SOI wafer and ZnO deposition recipe were used to fabricate both devices.

6.4.1 Series and Contact Resistances

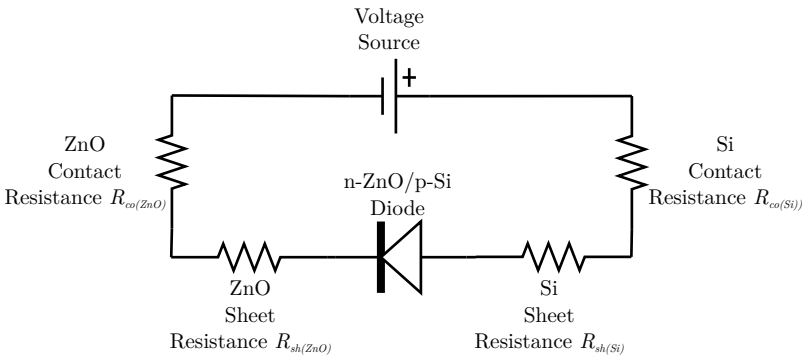


FIGURE 6.5: Circuit model of the heterojunction diode under forward bias conditions.

The electrical circuitry for the device under forward bias can be modelled as shown in Figure 6.5. As the model shows, there are four important series resistances associated with the metal contacts and the semiconductor sheets. The interfaces between the Al contacts and both the ZnO film and the Si slab constitute the contact resistances $R_{\mathrm{co_{ZnO}}}$ and $R_{\mathrm{co_{Si}}}$, respectively. It is challenging to model the contact resistance theoretically [96]. Thus, it is normally measured experimentally by using the *transmission line model* (TLM) structures [96]. There is a variety of TLM structures. However, the basic idea is to measure the current flow between two metal terminal while varying the distance between the two terminals. In this project, O-ring and disc-shaped contacts were used to find the contact resistance at the Al/ZnO and Al/Si interfaces. A top-view schematic of the structures is shown in Figure 6.6. The radial separations between the contacts were $20, 40, 60, 80$, and $100\,\mu$m. The main advantage of using circular TLM structures is that physical (electrical) isolation of the structure is unnecessary as the current can only flow between the two co-centric metal terminals [96]. Details of the TLM analysis can be found in [96].

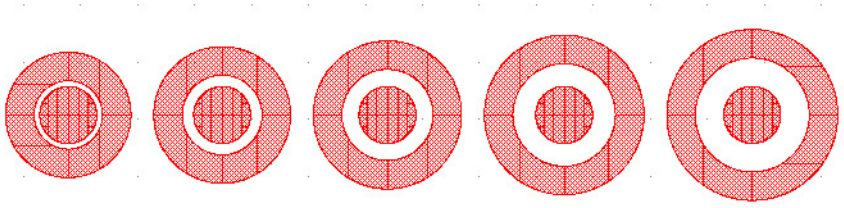


FIGURE 6.6: Mask layout of the circular TLM structures used to determine the contact resistance.

The sheet resistance can be easily computed using Hall measurement where a four point contacts structure is normally used. Details on the Hall measurement can be found in [5]. From the sheet resistance, the resistivity can be computed and from which the series sheet resistance R_{sh} can be estimated.

6.4.1.1 Zinc Oxide Series and Contact Resistances

The resistivity of the ZnO film, ρ_{ZnO}, was measured using the *Nano Metric HL5550 LN2 Cryostat* Hall measurement system and was found to be $R_{sh} \simeq 10 \times 10^{-3}\,\Omega$.cm. Taking into account that the Al/p-Si contacts were $\sim 6.5\mu$m and the ZnO film was 10 nm thick, the series sheet resistance can be computed according to:

$$R = \rho \frac{\ell}{A} \tag{6.1}$$

where R is resistance, ρ is the resistivity, ℓ is the length of the film form the contacts to the core region.

Since the fabricated chip had a number of devices with different active lengths, it is useful to rewrite Equation 6.1 as:

$$Rl = \rho \frac{\ell}{t} \tag{6.2}$$

where l is the active length, and t is the thickness of the ZnO film. Using the aforementioned values, it is possible to calculate R as:

$$Rl = 10 \times 10^{-3} \times \frac{6.5 \times 10^{-4}}{10 \times 10^{-7}} = 6.5\,\Omega.\text{cm} \tag{6.3}$$

For example, the longest active length is 1 mm long; this corresponds to a series sheet resistance of $6.5/0.1 = 65\,\Omega$.

The contact resistance at the Al/ZnO interface was determined using TLM structures (Figure 6.6). The resistance was evaluated by computing the slope of the I-V plot according to Ohm's law (i.e. $R = V/I$). The resistance for different spacing between the circular contact terminals is plotted in Figure 6.7. The intersect of the linear fit of the data with the y-axis (resistance)

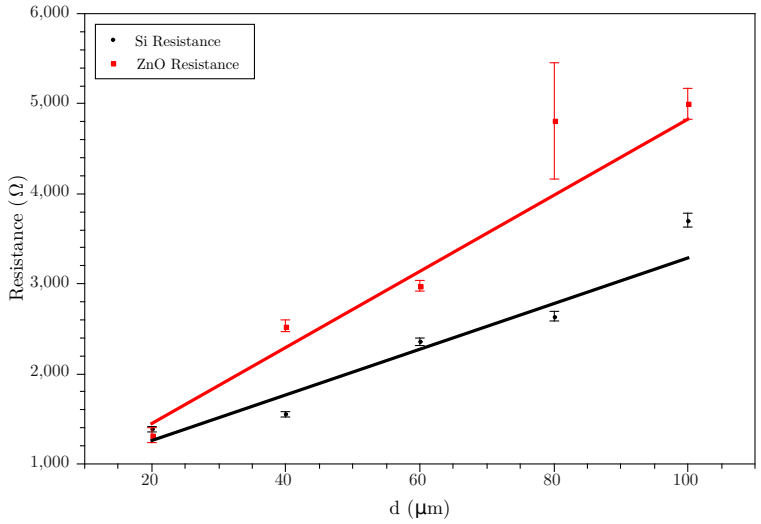


FIGURE 6.7: Resistance as a function of the distance between Al contacts on TH-ALD ZnO and silicon. The contact resistance is double the value of the intersect point of the linear fit of the data.

is double the value of the series contact resistance. From the equation of the linear fit, the intersect was found to be $\sim 610.22 \pm 95.8\,\Omega$; this value leads to a series contact resistance of $R_{co(ZnO)} \simeq 305 \pm 47\,\Omega$.

6.4.1.2 Silicon Series and Contact Resistances

Similar analysis to that in section 6.4.1.1 can be carried out to determine the series sheet resistance of the Si slab. Using Equation 6.2 with $\rho = 88.5 \times 10^{-3}\,\Omega$.cm, $\ell = 6.5 \times 10^{-4}$ cm, and $t = 220 \times 10^{-7}$ cm, the series sheet resistance of the silicon slab is approximately $Rl \simeq 57.5\,\Omega$.cm. For instance, the longest device ($l = 1$ mm), the series sheet resistance is $R \simeq 570\,\Omega$.

The series contact resistance at the Al/Si interface was evaluated using the same procedure outlined in section 6.4.1.1. Figure 6.7 shows a graph of the resistance against the spacing between the two circular Al contacts on a 220 nm silicon overlayer with a carrier concentration of 3×10^{17} cm^{-3}. The contact resistance from the linear fit in Figure 6.7 was calculated to be $378 \pm 17.5\,\Omega$.

	Sheet Resistance	Contact Resistance
Zinc Oxide	$10 \times 10^{-3}\,\Omega$.cm	$305 \pm 47\,\Omega$
Silicon	$88.5 \times 10^{-3}\,\Omega$.cm	$378 \pm 17.5\,\Omega$

TABLE 6.1: Summary of sheet and contact resistances for ZnO and Si.

6.4.2 Electrical Characteristics

In this section, the I-V characteristics of the electro-absorption optical switch will be outlined. Note that the I-V characteristics of the FP optical switch are almost identical to those of the electro-absorption switch and hence were omitted. However, these results can be found in Figure

B.2 in Appendix B. The same conclusions drawn from the discussion of the I-V characteristics of the electro-absorption switch are applicable to those of the FP optical switch. The electrical characteristics of the FP device of 50 μm long is summarised in Table 6.2.

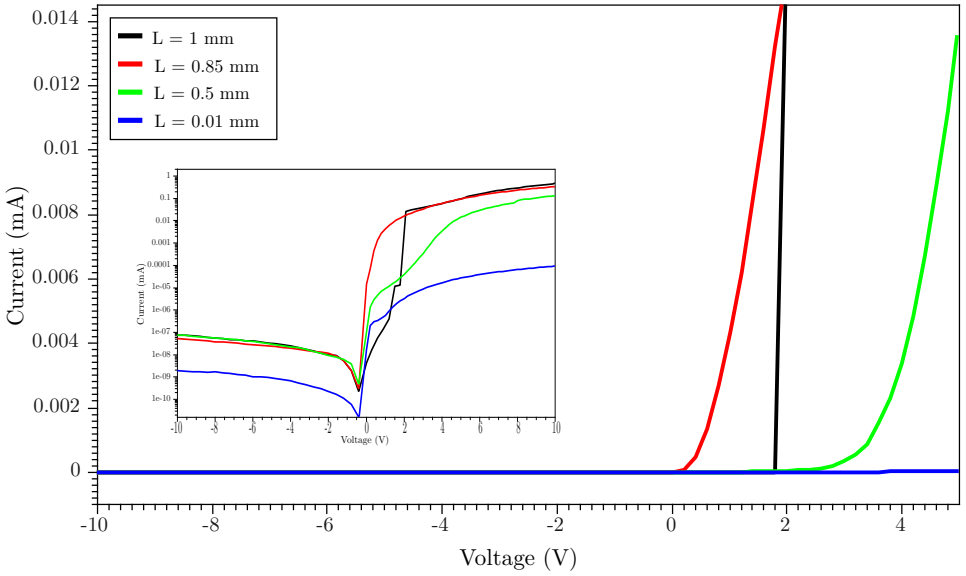


FIGURE 6.8: I-V characteristics of the n-ZnO/p-Si electro-absorption switch.

The I-V characteristics of the heterojunction were obtained using Agilent semiconductor analyser. Figure 6.8 shows the I-V curve of the four devices with different active lengths. Clearly, for a constant voltage, the current is proportional to the active length. Moreover, the longest device, where $L = 1$ mm, shows Schottky characteristics around the forward bias $V_F \simeq 2V$. The turn-on voltage was different for all devices. Table 6.2 lists information regarding the structural and electrical characteristics of the measured devices.

	Length (mm)	r_s (kΩ)	Ideality Factor	Turn-On Voltage
Fabry-Perot	0.08	134	22	2.8
Electro-absorption 1	1	13.41	-	2
Electro-absorption 2	0.85	18.33	4.5	1.5
Electro-absorption 3	0.5	50	16.5	4
Electro-absorption 4	0.01	≥ 60	14.3	3

TABLE 6.2: Summary of the structural and electrical characteristics of the measured devices. The series resistance was evaluated in the high injection region where $V \geq 5$ V.

The series resistance of the n-ZnO/p-Si heterojunction devices can be deduced from Figure 6.9. At high currents, the resistance of the device is dominated by the series resistance, r_s, which in the case of Figure 6.9 can be evaluated using the slope of the **log(I) vs. voltage** plot at $V_F \geq 7$ V.

6.4.3 Electo-Optical Response

The insertion loss and electro-optical response of the of the devices were measured using the optical set-up shown in Figure 6.10. Agilent 8164B Lightwave Measurement System was used to

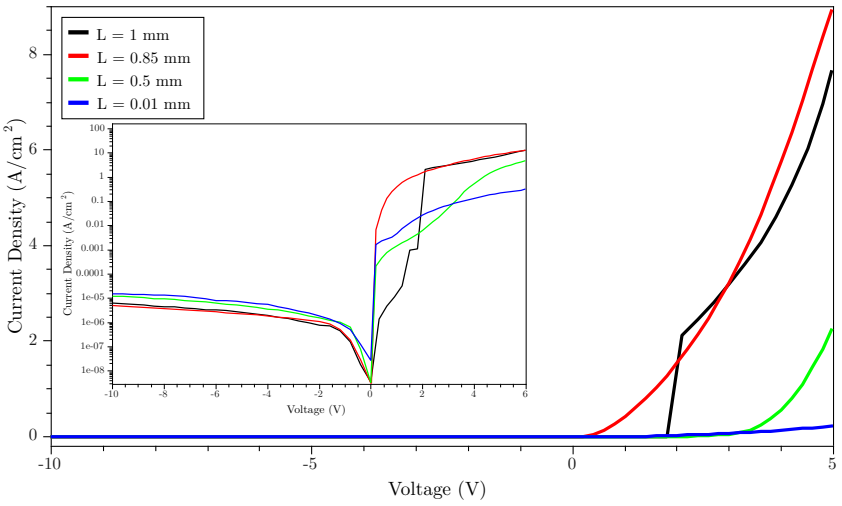


FIGURE 6.9: JV characteristics of the n-ZnO/p-Si electro-optical switch.

generate and detect the optical signal. The Agilent module contains a compact tunable laser with a wavelength range between $1520-1620$ nm. The module also contains an InGaAs photodetector with a sensitivity of ± 110 dBm. Although devices of variable length were available, the insertion loss could not be measured using the cut-back method because of the low absorption loss induced by the ZnO film. The variance in the coupling loss, between devices of different lengths, exceeds that of the insertion loss. However, the loss was estimated using the *(n, k)* data obtained from ellipsometry measurement (Fig. 4.11). The *(n, k)* was fed into Lumerical FDTD software to calculate the insertion loss which was found to be $Loss_{\mathrm{OFF}} \simeq 1.5$ dB/cm, where $Loss_{\mathrm{OFF}}$ is the total insertion loss, including absorption, when the device is in the **OFF** state.

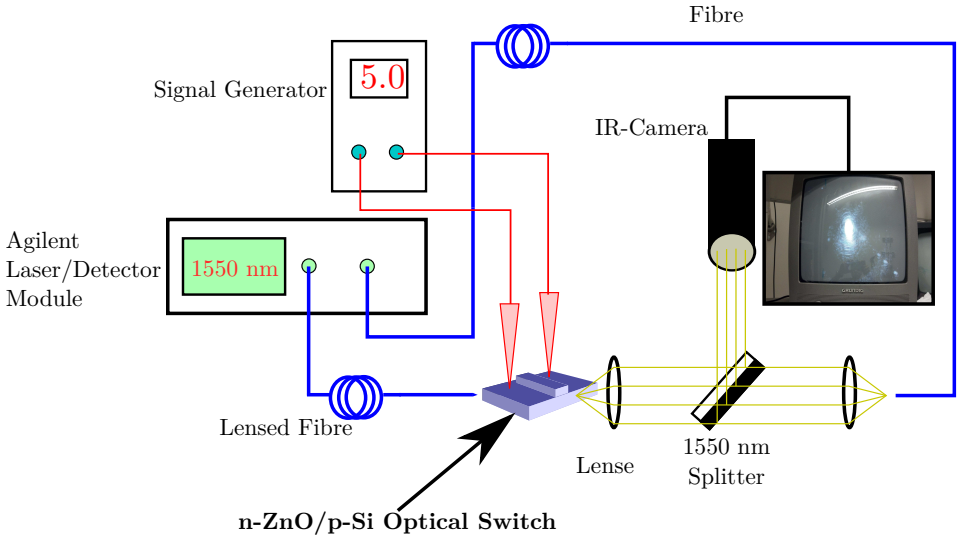


FIGURE 6.10: The optical setup used to characterise the optical and electro-optical response of the device.

6.4.3.1 Fabry-Perot n-ZnO/p-Si Optical Switch

If the cavity was depleted of carriers, the effective index of silicon increases according to Equation 3.17 and the wavelength spectrum shifts towards longer wavelengths; this effect is called red-shift. In contrast, if free carriers were injected into the cavity, the effective index of the silicon decreases and blue-shift is ensued.

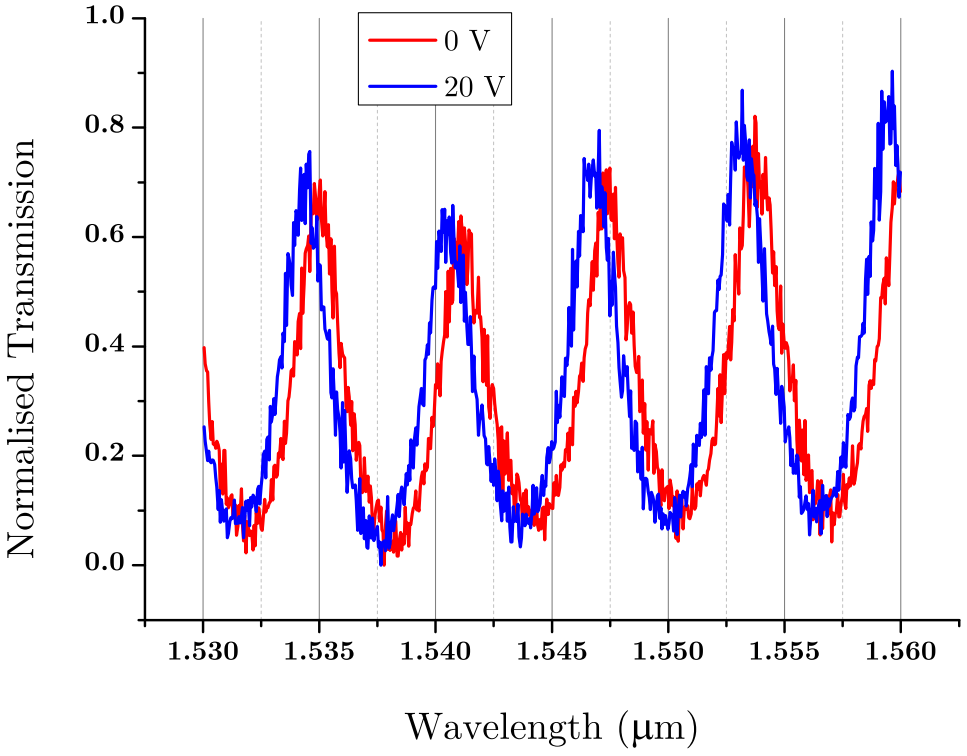


FIGURE 6.11: Blue-shift as the cavity was forward biased at 20 V. The maximum of the resonant wavelengths cannot be seen due to under sampling.

When the heterojunction was forward biased at 20 V, a blue-shift of 6×10^{-4} μm was observed (Fig. 6.11). The full width half maximum (FWHM) was $\approx 1 \times 10^{-4}$ μm. Because the current density even at 20 V was small (1.388×10^{-3} A.cm^{-1} , cf. 1.5×10^{3} A.cm^{-1} at 0.93 V for simulated ideal device), the shift cannot be attributed to increase in the device's temperature. Note that the device was meant to be operated in the depletion mode. However, no shift was observed when the heterojunction was reverse-biased. The absence of a shift when the junction was reverse-biased can be attributed to a number of factors. Firstly, it is believed that ZnO layer extended beyond the silicon core and pinched-off the silicon slab, preventing the depletion of the silicon core (Fig. 6.4). This was confirmed with microscopic images that shows the extension of the ZnO. Secondly, since the free electron concentration was high ($> 1 \times 10^{19}$ cm^{-3}), the core region of the waveguide was depleted of free holes even at equilibrium (i.e. 0 V bias). Thirdly, the high sheet resistance of the silicon and ZnO films, mainly due to the distance between the metal contacts and the active region, could have resulted in the poor efficiency of the electro-optical switch. While all mentioned factors contributed to the inferior efficiency of the switch,

it is believed that the sheet resistance of the silicon and ZnO films was the main reason. Part of these results were presented in [97].

6.4.3.2 Electro-Absorption n-ZnO/p-Si Switch

The electro-optical responses of the four electro-absorption devices are shown in Figure 6.12. The devices were forward-biased from $V_F = 0$ V to $V_F = 20$ V. Since the density of free carriers is proportional to the forward bias voltage, the absorption coefficient increases with V_F according to Equation 3.18. Therefore, the optical absorption loss per unit length increases with applied forward bias as shown in Figure 6.12. The absorption loss of a device at a given forward bias is referred to as the extinction ratio.

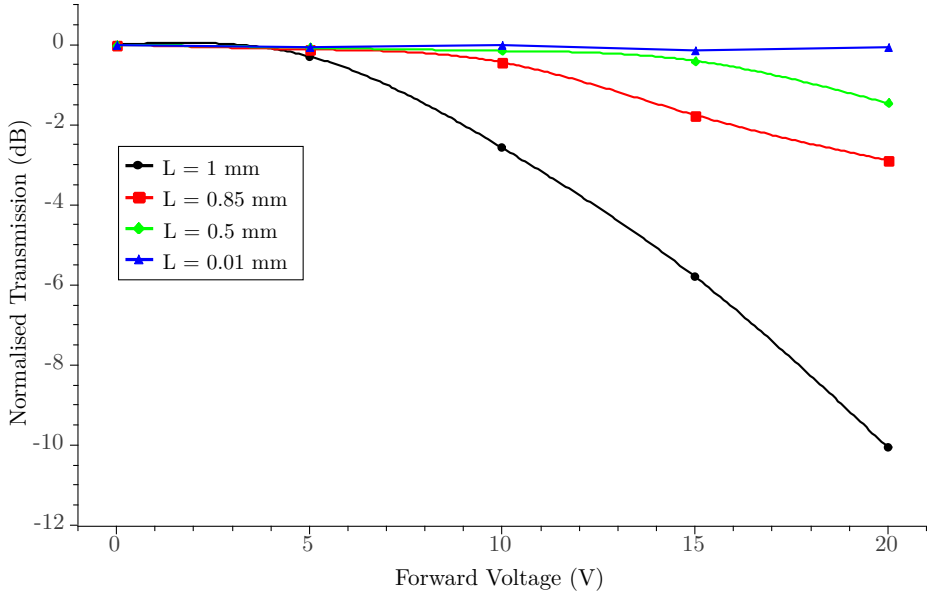


FIGURE 6.12: Normalised optical transmission as a function of the forward bias voltage.

Given a forward bias voltage, the absorption loss was greater for longer devices than that for shorter devices. In other words, Figure 6.12 illustrates that a trade-off exists between the device footprint and extinction ratio. For instance, at 10 V forward bias, the extinction ratio of the longest device ($L = 1$ mm) was 2.5 dB, while that of the second longest device ($L = 0.8$ mm) was 0.5 dB. An acceptable extenction ratio can be obtained by using the longest device ($L = 1$ mm) at a forward bias $V \geq 15$ V.

The AC response (i.e. switching speed) of a diode is governed by the recombination rate of the minority carriers in the lightly doped region (i.e. p-type silicon where $n_h = 3.7 \times 10^{17}$) [98, 99, 100]. The evaluation of the minority carrier lifetime can be estimated using a number of measurement methods [96]. One method is to modulate the electro-optical switch while monitoring the eye-diagram until it closes. However, the bias voltage needed to achieve reasonable extinction ratio is high (20 V) and cannot be obtained from off-the-sehlf signal generators. To determine the recombination rate, high-frequency measurement was carried out using the circuit configuration shown in Figure 6.13. A *Thurlby Thandar Instrument TG120* signal generator was used to produce a square wave signal with an amplitude of $\sim 2.8\ V_{pp}$ and varying frequency.

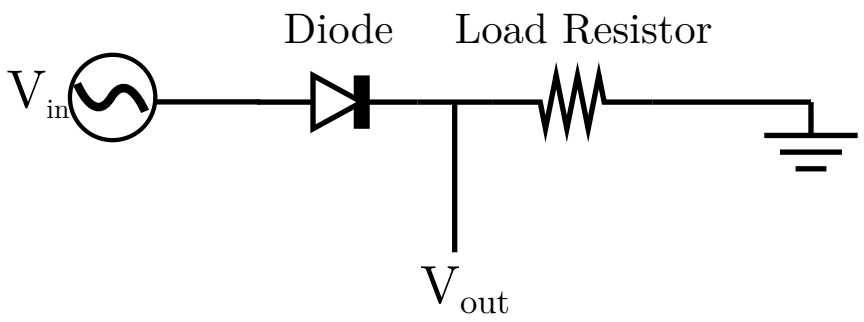


FIGURE 6.13: Circuit diagram of high frequency measurement. The load resistor had a value of 500 Ω

A $V_F = 2.8$ V is sufficient for demonstrating the AC response of the device since the diode is switched on and is in the high injection region (Fig. 6.8). The output was monitored using an *Agilent 54621D* oscilloscope.

The input and output signals of a 0.85 mm long n-ZnO/p-Si electro-optical switch connected with a 220Ω termination resistor are shown in Figure 6.14. The peak-to-peak (V_{pp}) voltage across the load resistor is significantly reduced because of the large series resistance of the heterojunction. The output signal is distorted by the noise because of its small V_{pp}. The switching speed, when $R_{load} = 3.3\,k\Omega$, was ~ 18.5 kHz. The switching is greater than ~ 18.5 kHz when the load resistor was reduced. However, due to the diminished voltage across the load resistor, the switching speed was difficult to measure accurately. Note also that when the 50 Ω typical termination load was used, the output waveform was undetectable because of the high impedance mismatch between the termination load and the diode's series resistance.

6.5 Discussion

In the results section, the electrical and electro-optical characteristics of a n-ZnO/p-Si absorption-based optical switch were presented. In this section, the results will be discussed and interpreted with reference to the simulation results in Chapter4 and similar devices reported in literature. Note that the discussion considers only the electro-absorption device since all issues raised in the discussion are applicable to the FP optical switch are principally related to the electrical structure of the device rather than the optical structure.

6.5.1 I-V Characteristics of the n-ZnO/p-Si heterojunction

The I-V characteristics of the heterojunction device reflects the quality of the materials (ZnO in particular) as well as that of the interfaces between ZnO/Si and Al. The electrical response of the four reported devices can be objectively compared in terms of current density (J) against applied voltage (i.e. J-V characteristics). The current density of each device is computed using $J = I/A$, where A is the area of the heterojunction. Figure 6.9 shows the J-V characteristics of the four reported devices in Figure 6.8. It is notable that all devices have different turn-on voltages. Despite normalising the current with respect to the devices' areas, the turn-on voltage is apparently greater for shorter devices (i.e $L = 0.5, 0.01$ mm). According to Equation

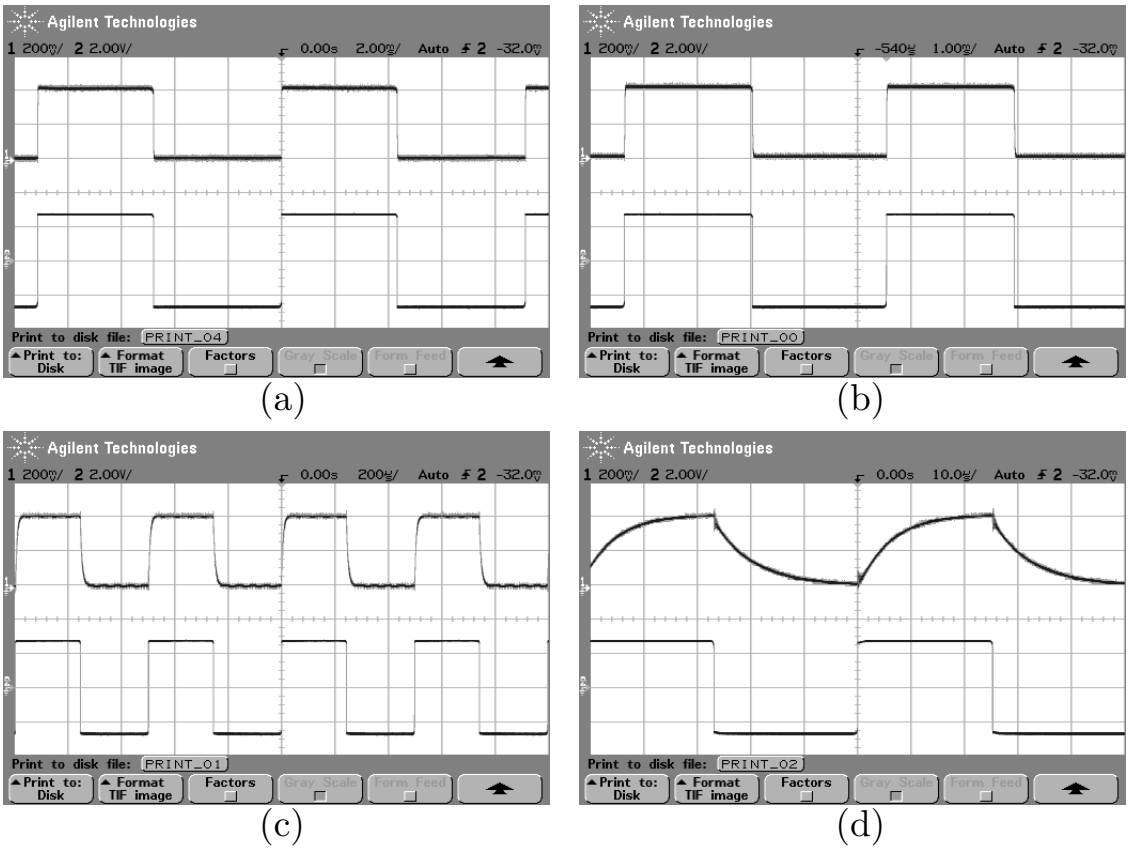


FIGURE 6.14: AC response of the circuit shown in Figure 6.13 with $R_{\text{load}} = 10\,\text{k}\Omega$. (a), (b), (c), and (d) show the output waveform across the diode when the frequency of the input signal was $0.11, 0.2, 2$, and 17 kHz, respectively

3.44, the turn-on voltage mainly depends on the material properties of the ZnO and Si. Hence, the cause of the increased turn-on voltage for the shorter devices can be attributed to length-dependent resistances across which potential drops. Shorter devices have greater resistance than the longer ones. Figure 6.15 shows a simulated J-V characteristics of two identical n-ZnO/p-Si heterojunctions with different lengths: $L = 1, 0.5$ mm. Note that the absolute values of the turn-on voltages, in the simulation, is not important. The turn-on voltage clearly seems to depend on the length of the device. It is believed that the increased turn-on voltage for the short devices is caused by the increased resistance of the quasi-neutral region, which is inversely proportional to the length of the device (Eq. 6.1). In other words, some of the externally applied voltage is wasted across the series resistance of the quasi-neutral region (i.e. the thin waveguide slab) [101].

A careful comparison between the I-V characteristics of the simulated n-ZnO/p-Si heterojunction in section 4.3 and that of the fabricated device in Figure 6.8 reveals a significant discrepancy: both simulated device had a length of $L = 0.85$ mm. The simulation results exhibit higher currents than those measured. Moreover, the turn-on voltage of the simulated device was lower than that of the fabricated device. There are two possibilities that can explain this discrepancy.

Firstly, the material parameters and properties used in the simulations were assumed to be perfect in comparison to the experimental ones. The material properties of importance are the

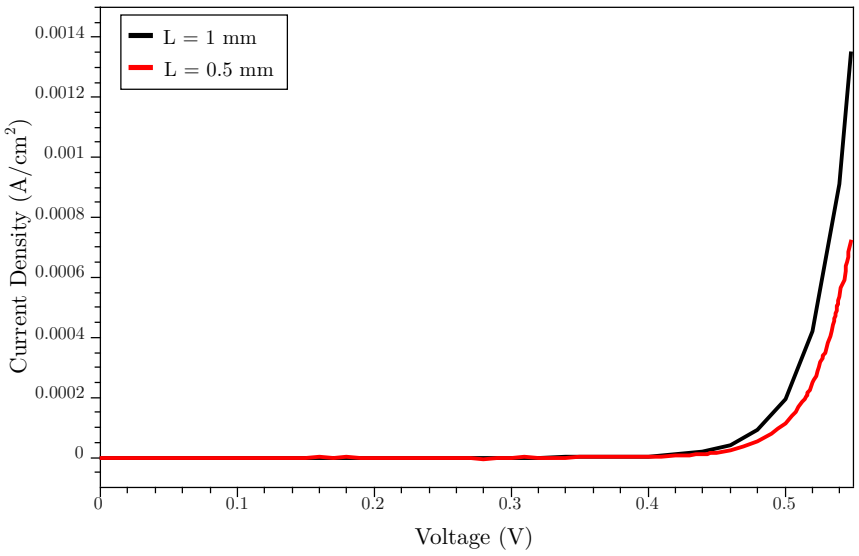


FIGURE 6.15: J-V characteristics of two ATLAS-simulated n-ZnO/p-Si optical switches with different lengths. The two devices have different turn-on voltages.

	Zinc Oxide
Free Electron Concentration (cm^{-3})	2×10^{14}
Mobility ($cm^2/V.s$)	0.5

TABLE 6.3: Material properties used in the modified electrical simulations using ATLAS.

ZnO's mobility and free carrier concentration. The silicon's properties should be reasonably accurate as they were of high quality SOI wafers. Note also that the ZnO's material properties used for simulation were obtained from thin film characterisation measurement. However, these properties might have been different for the fabricated device. Indeed, the mobility value used in Table 4.2 was the measured bulk mobility rather than the device mobility. The ZnO's device mobility is normally lower than that of the bulk mobility [102]. The free carrier concentration could also have been different because of the extremely thin thickness of the ZnO. The simulated I-V characteristics can approximate those of the fabricated device if some of ZnO's mobility and free electron concentration were changed according to Table 6.3. Figure 6.16 (a) shows the I-V characteristics of the fabricated device as well as that of the modified simulated device. Secondly, the I-V characteristics of the fabricated device might have been caused by other effects such as high contact resistance, deep-level-assisted tunnelling, or SiO_2 layer at the ZnO/Si interface[17, 103].

The ideality factor is a measure that can be used to investigate some of these defects. Table 6.2 shows that the 0.85 mm long device had the best ideality factor ($\eta = 4.5$). However, according to the Sah-Noyce-Shockley theory, even this value is worse than the worst case ($\eta = 2$) [104, 103]. High ideality factors ($\eta \geq 2$) are normally attributed to high non-linearities and/or high contact resistances and high levels of recombination[104]. Indeed, the Al/Si contact resistance ($378 \pm 17.5\ \Omega$) computed in section 6.4.1.2 is significantly larger than typical values where the contact resistance is approximately only $0.8\ \Omega$ [96]. The high contact resistance at the Al/Si interface is believed to form Schottky diodes each of which has its own ideality factor. Therefore,

the ideality factors calculated in Table 6.2 are the sum of the ideality factors of the n-ZnO/p-Si heterojunction as well as those of the Schottky diodes formed at the Al/Si interface: i.e. $\eta_{\text{device}} = \sum_{i=1}^{n} \eta_i$.

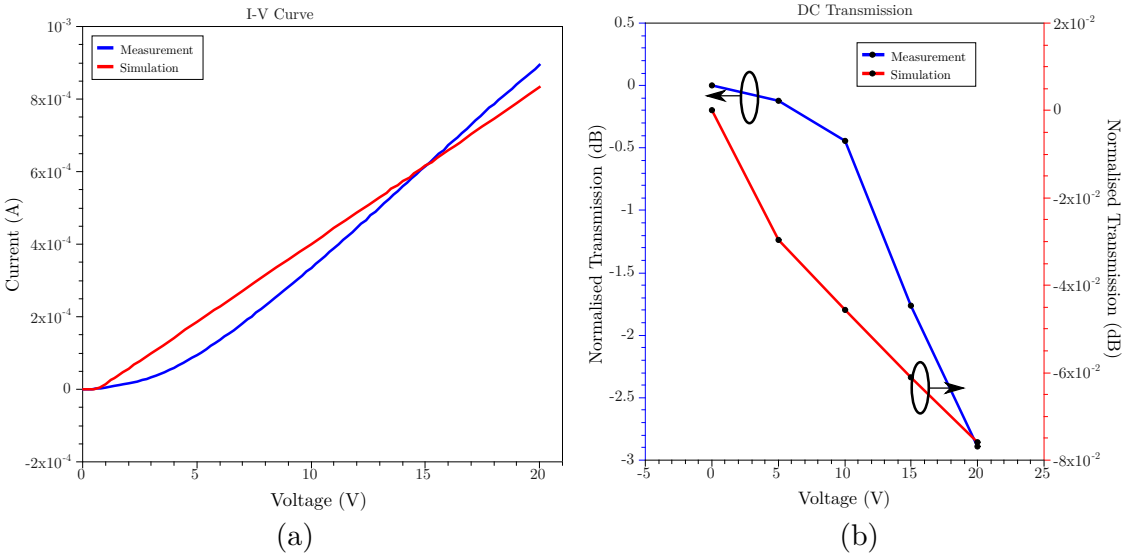


FIGURE 6.16: A comparison between the measured and simulated device. The measured and simulated device had identical designs and dimensions and had a length of 0.85 mm. (a) shows the I-V characteristics of the measured (blue-line) and simulated (red-line) devices. (b) shows the optical transmission of the measured (blue-line) and the simulated (red-line) devices as a function of forward-bias.

6.5.2 DC Optical Response

The optical response of the devices was shown in Figure 6.12. Figures B.1 and 6.12 show a strong correlation between the extinction ratio and the current density. Therefore, plasma dispersion effect is likely to have caused the absorption along the devices' length. In order to investigate the effect of the current density on the results shown in Figure 6.12, the modulation depth as a function of forward-bias, for the 0.85 mm long device, was simulated using Atlas Silvaco, AtlasToLumerical, and Lumerical FDTD 3D. Further details on the AtlasToLumerical software can be found in Appendix C. Figure 6.16 (b) shows the extinction ratio of the measured and simulated devices. A large discrepancy can be observed between the DC responses of the measured and simulated devices. It appears that the density of free carriers in the silicon core region is greater in the measured device than it is in the simulated device. Because the current densities in the two devices are virtually the same, the absorption loss was likely not all caused by carrier injection. The additional charge might have been caused by carrier accumulation in the p-type silicon core. It is unlikely that the additional loss was caused by the thermo-optical effect or other electrical effect because of the low electrical field and current densities across the device.

Figure 6.17 shows the extinction ratio as a function of device length for different forward-bias voltages. From this graph, the extinction ratio can be normalised in terms of device length. Analysis of the data shows that the electro-absorption switch has a normalised extinction ratio of ≈ 100 dB/cm at 20 V forward-bias.

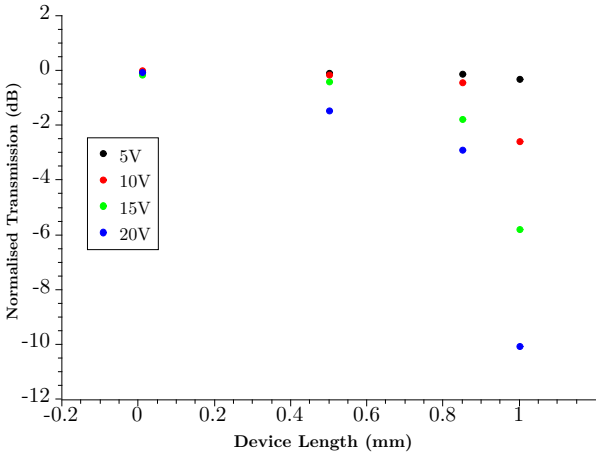


FIGURE 6.17: Transmission as a function of device length for different forward-bias voltages.

6.5.3 Switching Characteristics

The AC response of the 0.85 mm long device was shown in Figure 6.12. Clearly, the device was capable of switching at speeds higher than 18.5×10^3 Hz when the load resistor was 3.3 kΩ. However, it was also noted that the switching speed depends on the load/termination resistor. The switching speed increased to 0.25×10^6 Hz when the load resistor was reduced to 220 Ω.

Under forward-bias conditions, the diffusion capacitance becomes significant [5]. The diode can then be modelled using its equivalent circuit which can be represented as the diode's series resistance connected in parallel with its diffusion capacitance. Modelling the circuit shown in Figure 6.13 allows the determination of the diffusion capacitance. The high-frequency circuit (Fig. 6.13) was modelled using the free SPICE software *LTSpice*. The series and load resistances were set to 18.8 kΩ and 3.3 kΩ, respectively. The diffusion capacitance was varied until the AC voltage response across the load resistor resembled that shown in Figure 6.14 (d).

Figure 6.18 (a) shows the waveform of the AC circuit with $R_{\text{load}} = 3.3\,\text{k}\Omega$ and when the input signal frequency was 20 kHz. The waveform closely resembles that shown in Figure 6.14 (d). The capacitance that resulted in this waveform was $C_{\text{d}} \simeq 2.5$ nF. The capacitance value was also used to find the transient response when the load resistor was 220 Ω (Fig. 6.18 (c)). Figure 6.18 (b) shows the transient response of the circuit when the load/termination resistor was set to 220 Ω. The frequency and amplitude of the waveform in Figure 6.18 (b) closely matches those of the waveform shown in Figure B.4 in Appendix B.

6.5.3.1 Carrier Injection

The operation of the heterojunction optical switch in this project was based on carrier injection where the switching speed is governed by the recombination time of the minority carriers (electrons) in the p-type silicon core. The recombination time is subject to the carrier lifetime as well as the current density [5]. Furthermore, the current density directly depends on the total resistance of the circuit. The transient time due to carrier recombination can be expressed as:

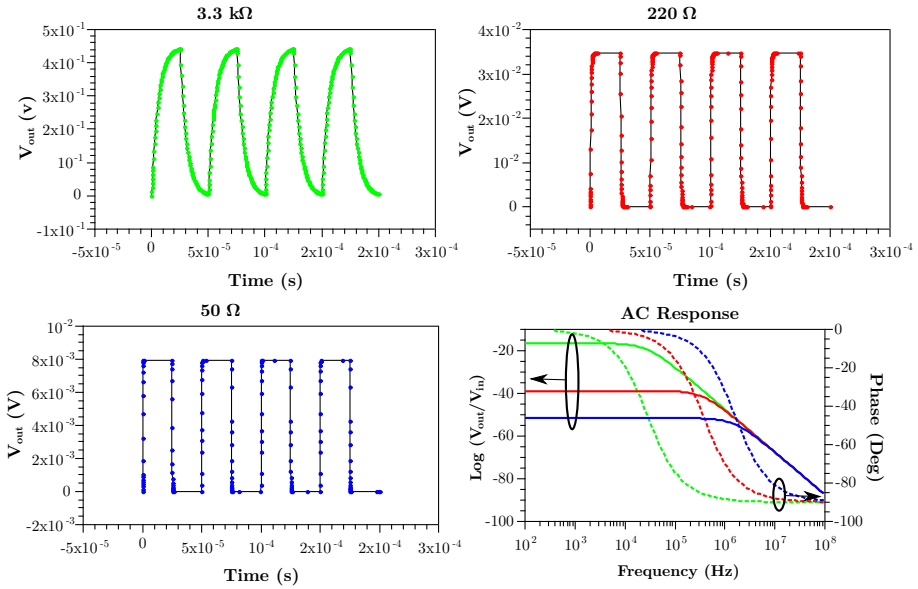


FIGURE 6.18: The simulated transient response of the 0.85 mm long device with different termination load resistor. The AC response (magnitude and phase) as a function of frequency are also shown.

$$t_{\text{trans}} = \tau_n \frac{I_F}{I_R} \tag{6.4}$$

where t_{trans} is transient time for minority carrier depletion, τ_n is the lifetime of electrons in the p-type silicon core, I_F is the forward current, and I_R is the reverse current. The forward and reverse currents were estimated to be 2.0×10^{-5} A and 1.427×10^{-8} A, respectively, when a $3\,V_{pp}$ wave pulse was applied to the circuit shown in Figure 6.13 where $R_{\text{load}} = 3.3\,\text{k}\Omega$. Equation 6.4 results in $\tau_n \simeq 19.26$ ns. Therefore, ignoring the RC time constant of the heterojunction, the maximum theoretical switching speed is expected to be ~ 11.25 MHz. Note that the rise time needed for the charge to reach 90% of its saturation value was $\sim 2.3\tau_n \simeq 44.3$ ns. This rise time is substantially longer than a similar device where the rise time was evaluated to be ~ 1 ns [89]. Note that the short recombination time in [89] was a result of the proximity of the highly doped regions to the core of the waveguide. Other studies reported recombination times ($\tau_n = 700$ nm) that are longer than the one reported in this study [105].

The carrier injection mechanism does not explain the discrepancy in the optical transmission between the measured and simulated devices shown in Figure 6.16. The density of free carriers under the same current density appears to be higher in the measured device than it is in the simulated device. The additional free electrons in the measured device might be described in terms of free carrier accumulation.

6.5.3.2 Carrier Accumulation

Instead of injecting free carriers across the depletion region, carriers can accumulate at either side of the junction. Devices based on such mechanism are commonly referred to as free carrier accumulation switches/modulators. Nevertheless, an isolation layer, such as SiO_2, is required

at the junction's interface to prevent carrier injection across the depletion region (Fig. 6.19). Ideally, no injection of charges across the isolation layer should occur. Moreover, depending on the material and thickness of the isolation layer, a portion of the electric field applied to the device is lost across the isolation layer.

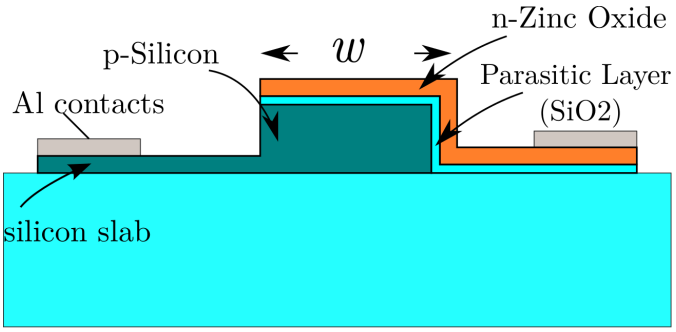


FIGURE 6.19: A cross-section of an accumulation-based electro-optical switch.

The performance and characteristics of the reported devices imply that an isolation layer might have formed at the ZnO/Si interface (Fig. 6.19). Firstly, the current density of the reported heterojunction is substantially lower than that of typical monojunctions devices [77, 105, 106, 100]. Typical densities of injected carriers in absorption based devices are $\geq 10^4$ A/cm^2 [107]. The 0.85 mm long device showed only $J = 81$ A/cm^2 at 20 V forward-bias voltage. Secondly, the turn-on voltage of the measured devices ($1.5 - 3.5$ V) was slightly higher than the one (0.96 V) calculated in section 3.4.1. Although it was previously argued that the increased turn-on voltage could have been caused by high contact resistance and other imperfections at the metal/semiconductor interface, the existence of a thin isolation layer at the ZnO/Si junction's interface would also increase the turn-on voltage. Thirdly, the estimated diffusion capacitance of the device (2.5 nF at 3 V) is even greater than that of typical reverse-biased junctions [10, 108, 109]. The unusually high capacitance can be attributed to an isolation layer at the heterojunction's interface. In fact, transmission electron microscope (TEM) of a similar n-ZnO/p-Si heterojunction showed that a 1.8 nm SiO_2 layer was formed at the heterojunction's interface [17]. The thickness of the defective SiO_2 was attributed to the deposition temperature of the ZnO [17].

In brief, it seems that the n-ZnO/p-Si heterojunction functions as both injection and accumulation electro-absorption device. The cause of the suspected accumulation operation of the device is believed to be an additional SiO_2 layer at the ZnO/Si interface formed during the ALD process. The parasitic SiO_2 is thought to contribute to the low current density, high turn-on voltage, and the high junction capacitance. Nonetheless, the parasitic SiO_2 layer can be useful if the design of the device intentionally includes an isolation layer that facilitates carrier accumulation operation under which switching speed is expected to increase [110]: the design would resemble a MOS structure. Note that ZnO can behave as a metal if the carrier concentration is sufficiently high: high concentration can be achieved by incorporating aluminium (Al:ZnO). Table 6.4 summarises the performance of the 0.85 mm and 1 mm long devices.

	0.85 mm Device	1 mm Device
Turn-on Voltage (V)	1.5	2
Current Density at 20 V (A/cm^2)	81	101
Series Resistance (kΩ)	18.8	13.41
Diffusion Capacitance (nF)	2.5	2.7
Ideality Factor	4.5	-
Insertion Loss (dB)	0.102	0.12
Modulation Depth at 20 V (dB)	2.9	10
Switching Speed (MHz)	1	0.89
Switching Energy at 20 V (μJ)	1	1.08

TABLE 6.4: Summary of the characteristics and performance of the 0.85 mm and 1 mm long devices.

6.6 Conclusion

The objective of this chapter was to demonstrate the viability of using n-ZnO/p-Si heterojunction as a silicon-based electro-optical switch. The objective of using ZnO was its low deposition temperature using ALD. Low temperature processing is vital for the integration of silicon photonics to the existing CMOS technology. The maximum temperature used to fabricate the devices reported in this chapter was 150 °C. The n-ZnO/p-Si heterojunction induced negligible insertion loss (1.2 dB/cm). The I-V characteristics of one of the devices exhibited Schottky contacts: contact annealing was not performed due to the high temperature required ($\geq$ 425 °C). The I-V characteristics and DC optical response of the diodes showed strong correlation. The high-frequency response of the devices is thought to be limited by the RC time constant of the junction rather than the minority carrier lifetime. Detailed review of the I-V characteristics and transient behaviour of the device revealed important imperfections. In particular, the series resistance of the devices was considerably high. High contact resistance as well as the existence of a suspected defective SiO_2 layer at the ZnO/Si interface are believed to cause the high series resistance and capacitance. The lateral distance of the contacts from the heterojunction is also believed to contribute to the large series resistance of the devices. Due to the formation of a parasitic SiO_2, the electro-absorption switch is believed to induce optical loss by two mechanisms: carrier injection and accumulation. The design can be improved by intentionally operating the heterojunction as an accumulation device as well as reducing the distance between the contacts and the heterojunction.

Chapter 7

Hot-Wire Chemical Vapour Deposition for Silicon Photonics Technology

7.1 Introduction

In Chapter 2, the potential benefits of using polysilicon (poly-Si) thin films in silicon photonics technology were reviewed in relation to multi-layered structures. The realisation of poly-Si films has been relying on high temperature processing in order to improve the optical and electrical properties of deposited films. For example, PECVD-deposited poly-Si films are normally annealed at high temperatures ($\geq 900^{o}$C) to reduce the amorphous proportion in the films. Nevertheless, low temperature deposition is desirable for multi-layered electro-optical structures and back-end integration. Post-processing annealing at high temperatures may damage temperature-sensitive materials and/or devices on a multi-layered structure.

Hot-wire Chemical Vapour Deposition (HWCVD) has been widely used to deposit amorphous-based solar cells due to its high deposition rate and unlimited deposition area. Moreover, a distinctive feature of HWCVD is its low temperature requirement. No scientific work has been reported on using HWCVD to deposit poly-Si films for silicon photonics technology. The work presented in this chapter details the first demonstration of HWCVD poly-Si films for use in the silicon photonics technology [59]. In this chapter, the development process of fabricating and characterising poly-Si waveguides deposited using HWCVD is explained in detail. This work was carried out in collaboration with *Echerkon Technologies* Ltd using the *HWCVD Nitron System*.

7.2 Single-Mode Waveguide

As its name suggests, a single-mode waveguide supports the fundamental mode only. The absence of higher order modes reduces intermodal dispersion. The fundamental mode also has the lowest

propagation loss. Therefore, it is important to ensure single-mode operation when designing a waveguide. Moreover, a two-dimensional strip waveguide supports at least two modes: TE_0 and TM_0.

The supported modes for a HWCVD polysilicon waveguide of a given thickness can be identified by plotting the effective index of the waveguide structure against the width of the waveguide. Establishing the effective index of a two dimensional waveguide structure normally requires numerical solutions to the wave equation. Lumerical FDTD was used to simulate polysilicon strip waveguides with a fixed thickness; the width was varied to establish the relationship between the effective index and the width. Figure 7.1 shows the supported modes for a waveguide of thickness of 220 nm at a wavelength $\lambda = 1550$ nm. The waveguide becomes multimode at width of ~ 420 nm. However, the waveguide strongly supports and favours the TE_0 mode.

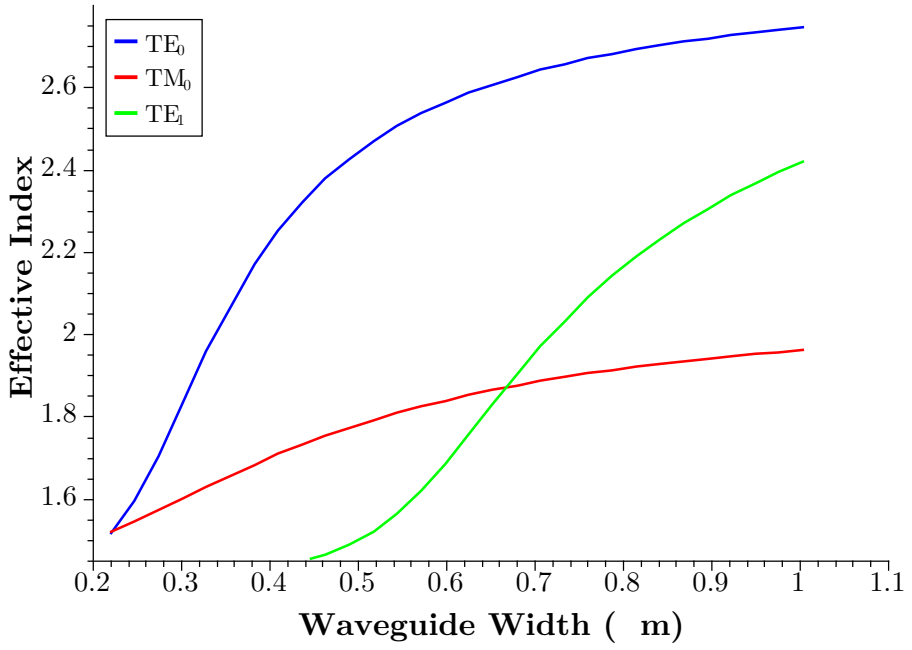


FIGURE 7.1: The effective index of the first three supported modes in a 220 nm thick polysilicon waveguide as a function of waveguide width at a wavelength $\lambda = 1550$ nm.

Figure 7.2 shows the first three supported modes as a function of the waveguide's width for a waveguide thickness of 400 nm at a wavelength of 1550 nm. Clearly, the waveguide supports at least two modes until the width is larger than ~ 550 nm where it becomes multimode. However, it is important to note that TM_0 and TE_1 are weakly supported compared to TE_0. The high effective index of the TE_0 mode means it has the highest confinement factor; hence, it has the smallest propagation loss. Therefore, waveguides of widths ranging from 400 to 600 nm with different lengths will be fabricated to investigate the optical propagation characteristics of HWCVD poly-Si waveguides.

7.3 Experimental Procedure

In this section, the fabrication process of HWCVD Poly-Si waveguides is explained in detail. Firstly, the sample preparation and the deposition procedures are introduced. Secondly, the

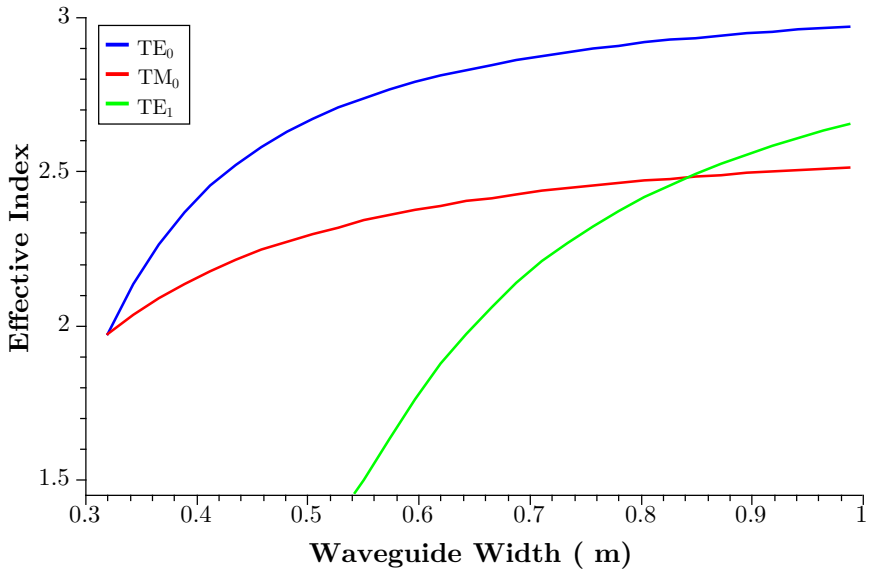


FIGURE 7.2: The effective index of the first three supported modes in a 400 nm thick polysilicon waveguide as a function of waveguide width.

pattern transfer process is discussed in terms of e-beam lithography and RIE dry etching. Finally, the tools and measurement setup for characterising the Poly-Si thin film properties as well as the optical transmission properties of the Poly-Si waveguides.

7.3.1 Sample Preparation

Prior to poly-Si deposition, a SiO_2 layer must be deposited to form the buried oxide (BOX) layer. The thickness of the BOX layer should be sufficient for providing optical isolation between the Poly-Si waveguides and the silicon substrate. A 2000 nm SiO_2 was deposited using plasma enhanced chemical vapour deposition (PECVD). The thickness was chosen because it is commonly found in commercial SOI wafers for optical waveguide applications.

The samples were always cleaned using acetone and IPA to remove any organic particles and general dust from the samples before deposition and lithography. The samples were dipped in acetone and then IPA for an equal duration of 30 seconds. Moreover, Water was occasionally used to rinse off sticky particles using the pressure of the water guns. The acetone/IPA cycle would be repeated as necessary. Oxygen plasma and NMP were used to strip e-beam resists (e.g. PMMA and ZEP) as it is difficult to remove it using only acetone/IPA.

7.3.2 Fabrication of Standard HWCVD poly-Si Waveguides

Thin intrinsic polysilicon films (220 nm thick) were deposited by *Echerkon's Nitor 301* HWCVD system at a substrate temperature of 240 °C with a silane and hydrogen gas mixture. Silane (SiH_4) decomposition was achieved by 75 μm thick tantalum filaments heated at 1850 °C. A 2000 nm thick PECVD silicon dioxide (SiO_2) layer was first deposited at 350 °C prior to polysilicon deposition to form optical isolation. Sub-micron waveguides were then realized using e-beam

lithography and conventional RIE etch with fluorine-based chemistry. The waveguides were then covered with a 700 nm PECVD SiO_2 layer that was deposited at a temperature of 350 °C, as shown in Figure 7.3.

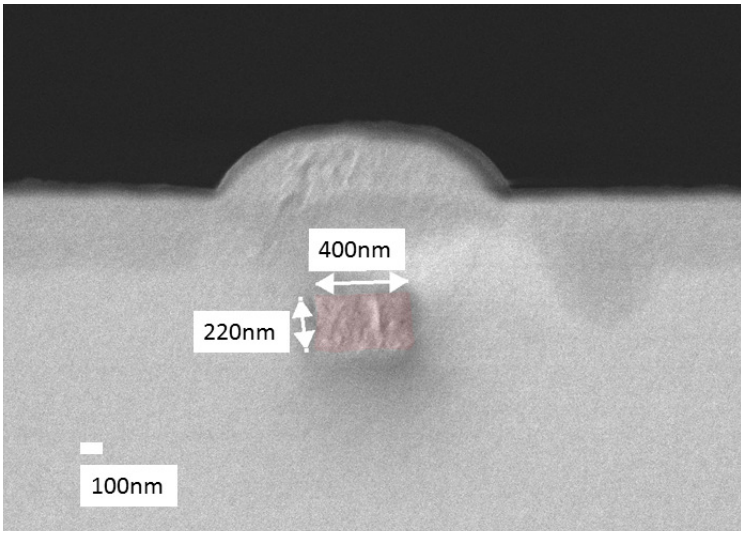


FIGURE 7.3: An SEM cross-section of the polysilicon waveguide covered with PECVD SiO_2.

7.3.3 Optimisation of the poly-Si HWCVD

The deposition of Poly-Si films were realised using Echerkon's *Nitor 301* HWCVD system. The samples were mounted inversely in a chamber were precursor gases were fed from the bottom of the chamber. Tantalum and tungsten were used as the heated wire elements. The temperature of the substrate was controlled by the heated wire array; the orthogonal distance between the heated wires and the substrate provides a temperature gradient by which the substrate temperature can be controlled. Silane (SiH_4) and (H_2) were used as precursor gases.

The investigated deposition parameters were temperature, pressure, and the dilution of SiH_4 in H_2. The set of experiments was designed using full factorial design and considered two pressure regimes. The investigated ranges of temperature and SiH_4 dilution are summarized in Table 7.1. Note that the lower bound for the SiH_4/H_2 dilution ratio in the low pressure regime was set to 2 because it was not possible to maintain a pressure of 0.01mBar while keeping the dilution at 1.

TABLE 7.1: Investigated range of deposition parameters.

	Temperature (°C)	SiH_4/H_2
High Pressure (0.048 mBar)	325-442	1-25
Low Pressure (0.01 mBar)	325-442	2-25

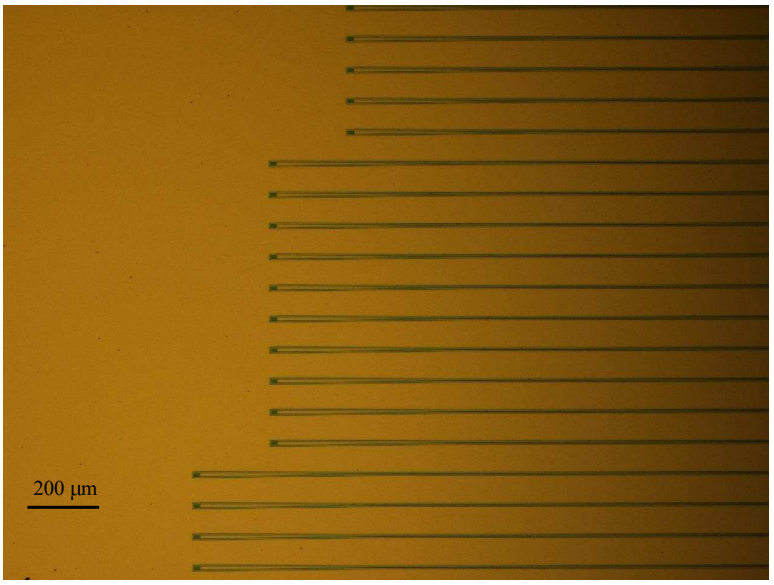


FIGURE 7.4: Microscopic view of the input section of the optimised HWCVD waveguides.

7.3.4 Planarisation Process of the Top Surface Roughnes

Depositing silicon on SiO_2 results in poly-crystalline silicon films which tend to have rough topographies. Poly-Si normally results in rougher topography than amorphous silicon (α-Si) because of its large grain size. Surface roughness control was thus essential to improve the optical loss transmission. The planarisation process targets the poly-Si film and is carried out prior to waveguide/cladding formation.

The smoothing process involves successive reactive ion etching steps. Each step starts by cleaning the sample and then spinning a ≈ 50 nm thick poly-methyl-methacrylate (PMMA); 50 nm thick PMMA results from spinning it at 3000 rpm. Then, the sample is baked using *Sawatec HP-401-Z* hotplate at 170 °C for 70 seconds to harden the PMMA. Finally, the sample is etched using RIE whereby the etch recipe was tuned to produce a $\approx 1:1$ selectivity.

Three samples, 1×1 cm^2, received a different number of planarisation steps. The samples were cleaved from the same wafer on which a 800 nm thick HWCVD p-Si film had been previously deposited.

7.3.5 Fabrication of Optimised HWCVD poly-Si Waveguides

An intrinsic poly-Si film was deposited on a 42×25 mm sample with deposition parameters derived from results in sections 7.4.2 and 7.4.3. The temperature of deposition was set to 360°C, the SiH_2 dilution ratio in H_2 was set to 2, and the pressure was set to 0.024 mBar. After deposition, the film thickness was measured using ellipsometer and found to be $\approx 800 \pm 15$ nm; the deposition rate was 1.02 Å/s.

Following deposition, a thinning process was carried out using RIE to reduce the thickness of the film to 550 nm. The thinning process was necessary to ensure that the thickness of the

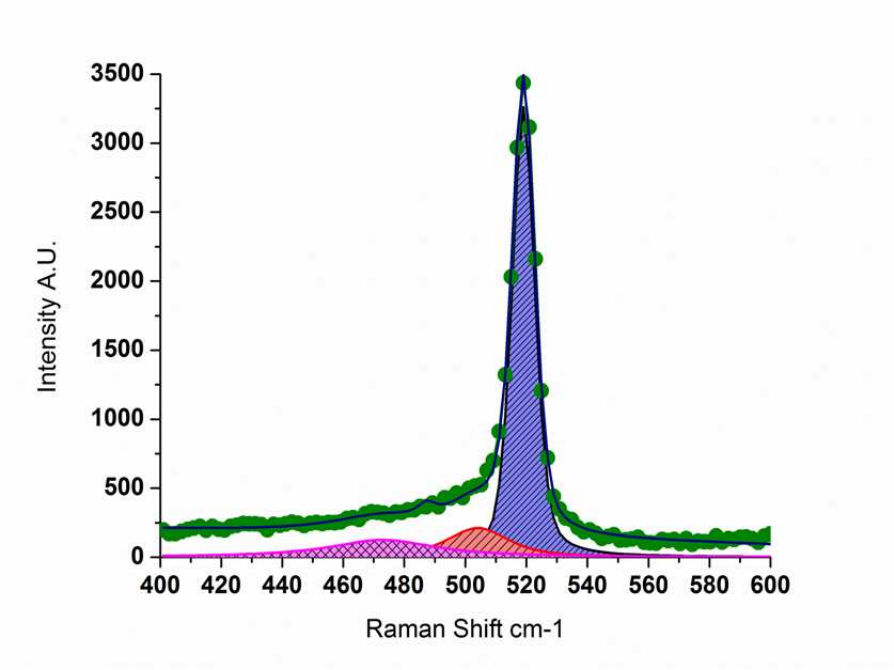


FIGURE 7.5: Raman spectrum of the polysilicon film. Curve-fitting shows a crystalline volume of 91% (blue-shaded area).

film after planarisation was approximately the desired thickness (i.e. $\approx$ 400 nm). Then, three successive planarisation steps were carried out on the sample. The RMS value of the top surface roughness (TSR) of the film was then characterised using AFM and was found to be $\approx$ 2.8 nm. The thickness of the film after planarisation was found to be 400 ± 10 nm. The high error in the thickness value was due to imperfections in the ellipsometer model for poly-Si films.

After planarisation, 400 nm wide, single-mode waveguides, were fabricated using e-beam lithography and RIE etching; refer to sections A.1.0.1 and A.2.2 for recipes parameters. Figure 7.4 shows a microscopic image of the fabricated waveguides. 5 waveguide lengths, 0.1, 0.25, 0.5, 0.85, and 1.3 cm, were fabricated to calculate the propagation loss and photonic crystal waveguide couplers were used to couple the light into the waveguides.

7.4 Results

7.4.1 Standard HWCVD poly-Si Waveguides

The crystallinity of the polysilicon layer was analysed using Raman spectroscopy with a 532 nm excitation laser. The crystalline volume fraction, X_c, of the film was calculated using [111]:

$$X_c = \frac{I_{c-Si}}{I_{c-Si} + I_{a-Si}} \tag{7.1}$$

where I_{c-Si} and I_{a-Si} are the sum of the deconvoluted intensities for the crystalline silicon peaks, centred at 520 and 510 cm^{-1}, and the amorphous silicon peak centred at 480 cm^{-1}, respectively.

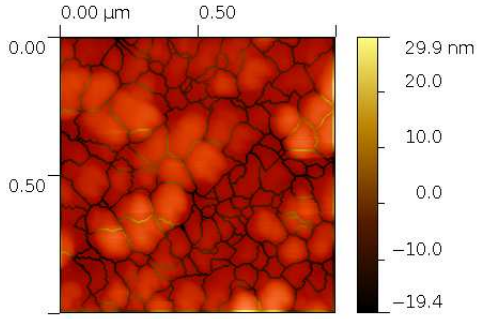


FIGURE 7.6: Grain boundaries as estimated by the watershed algorithm extracted from AFM topography measurement.

The crystalline volume was found to be 91%, as shown in Figure 7.5. The average grain size was obtained from AFM data and using the watershed algorithm and was found to be $\sim$ 100 nm. Figure 7.6 shows the estimated grain boundaries using the watershed algorithm.

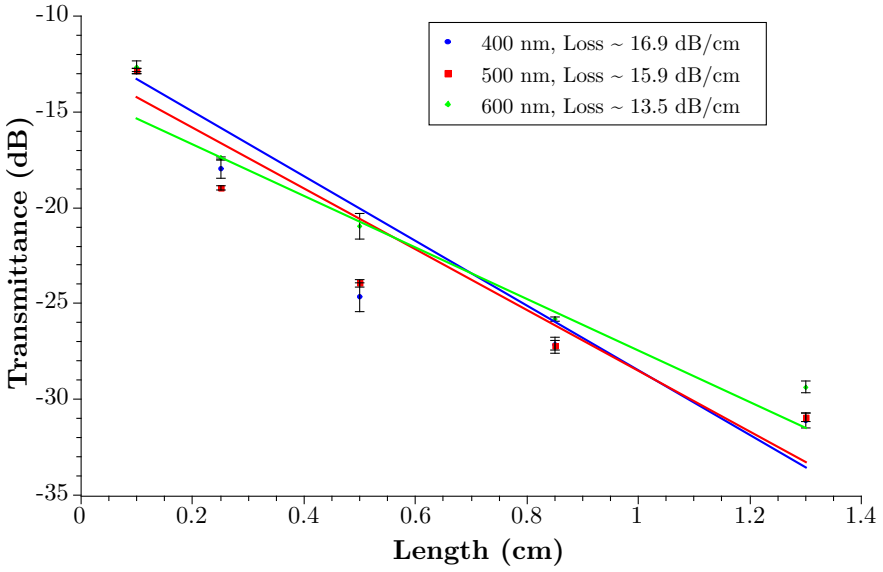


FIGURE 7.7: Transmission characteristics of the TE mode of the polysilicon waveguides of widths 400, 500, and 600 nm [59].

The transmission properties of the single-mode HWCVD polysilicon waveguides were characterized using the cut-back method at a wavelength of 1550 nm. An *Agilent Lightwave 81949A* C/L band was used as a laser source. The coupling loss of the nanohole grating couplers was estimated to be approximately 10 dB. The design of the nanohole grating couplers allows coupling of TE mode only. The fabricated waveguides had lengths of 0.1, 0.25, 0.5, 0.85, and 1.3 cm and widths of 400, 500, and 600 nm. Fig. 7.7 shows that the linear fit of the extracted transmission losses of the TE mode of the 400, 500, and 600 nm waveguides were found to be 16.9 ± 0.4, 15.9 ± 0.2, and 13.5 ± 0.3 dB/cm, respectively. It can be seen that the loss reduces for wider waveguides due to reduced interaction of the optical mode with the sidewall and top surface roughness (Fig. 7.13).

7.4.2 Reducing Top Surface Roughness

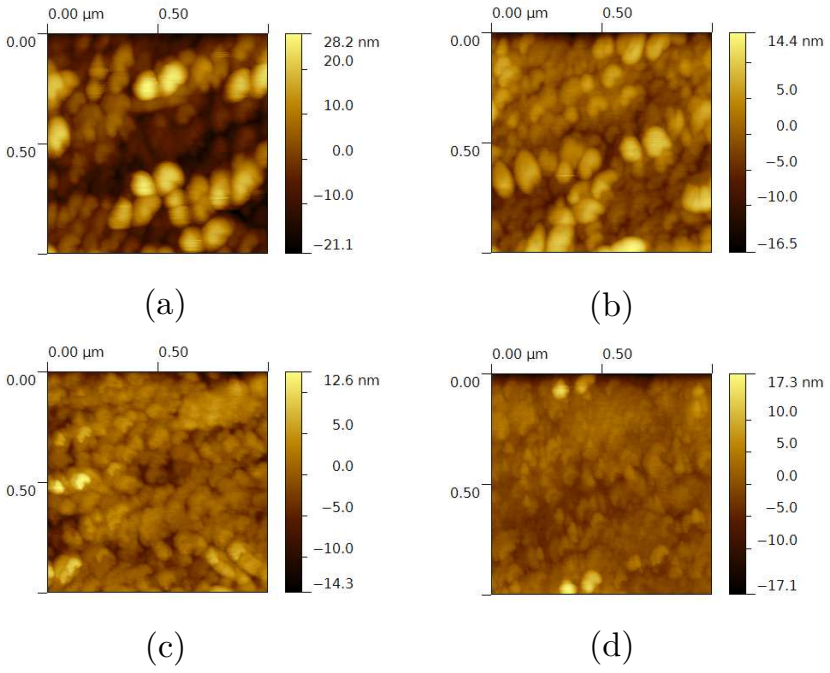


FIGURE 7.8: AFM images of intrinsic poly-Si showing the surface topography of different samples. (a) Topography of as-deposited poly-Si film. (b) Topography after one planarisation step. (c) Topography after two planarisation steps. (d) Topography after three planarisation steps.

The top surface roughness was characterised using the Veeco Multimode atomic force microscopy (AFM) system. The AFM system was operated in tapping mode. In addition to the nine samples that received a varying number of polishing steps, three samples of as-deposited *i*-/*p*-/*n*-type HWCVD films were also scanned. Figures 7.8 and 7.9 show the effect of successive planarisation steps on the top surface roughness of the three types of HWCVD p-Si films. A significant reduction in the root-mean-square (RMS) value of the top surface roughness (TSR) is evident across all types of the p-Si films. The reduction in TSR in the p-type films exhibited a linear relationship with the number of planarisation steps. In contrast, the TSR of the intrinsic and n-type films declined logarithmically with the number of planarisation steps. Note that after three planarisation steps, the TSR of all film types plateaued out around $RMS \approx 2.8$ nm.

7.4.3 Optimisation of the HWCVD

The crystallinity of the deposited polysilicon films were characterized using Raman spectroscopy. The crystal volume fraction was calculated using Equation 7.1 [111]:

Figure 7.10 shows that the crystallinity improves as the temperature increases from 325 to 442 °C irrespective of the dilution and pressure. The figure also shows that a low dilution ratio results in a superior crystallinity than high dilution ratio. Interestingly, Figure 7.10 (c) shows that for a 0.01mBar pressure and a dilution ratio of 2, the temperature has limited effect on the crytallinity. Moreover, Figure 7.10 (c) shows that a high contrast in crystallinity can be

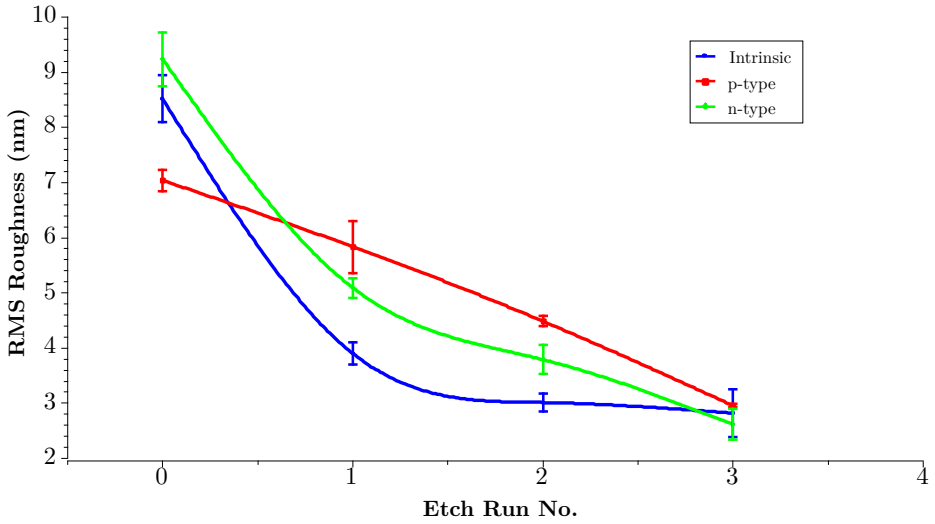


FIGURE 7.9: The effect of successive planarisation steps on the top surface roughness.

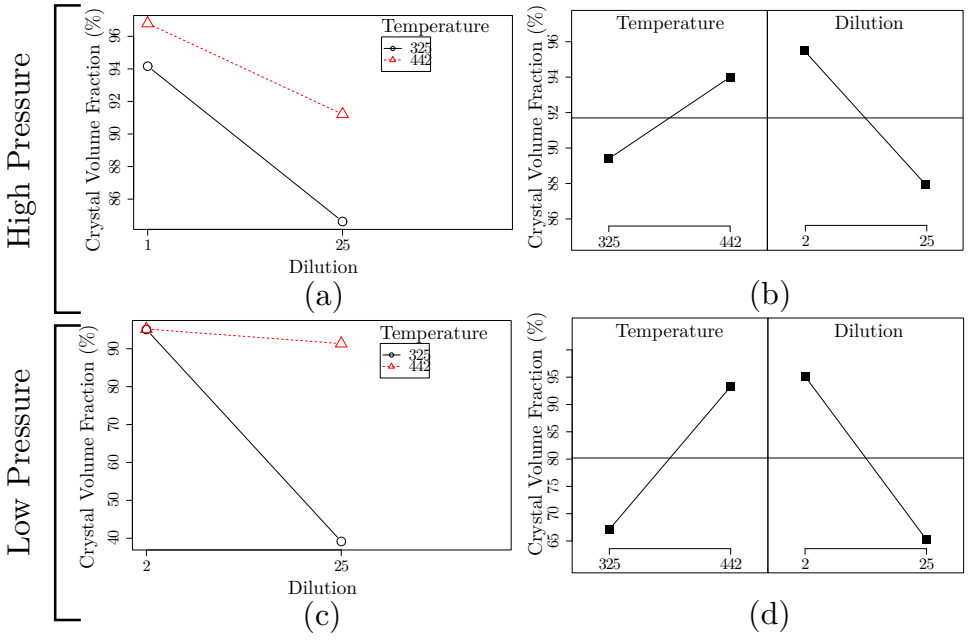


FIGURE 7.10: Crystal volume fraction under high and low deposition pressures. Illustrations (a) and (c) show the crystallinity interaction plot between temperature and SiH_2 dilution ratio for the high pressure and low pressure regions, respectively. Illustrations (b) and (d) show the main effect plot for the crystallinity for high and low pressure regions, respectively.

obtained by changing the temperature while maintaining a high dilution ratio (25) and a low pressure (0.01)mBar. Overall, a high crystal volume fraction (CVF) ($\geq$ 96%) can be obtained by a combination of high temperature, high pressure, and a low dilution ratio.

7.4.4 Propagation Loss of Optimised HWCVD p-Si Waveguides

The crystallinity of the polysilicon layer was analyzed using Raman spectroscopy with a 532 nm excitation laser. The crystalline volume fraction, X_c, of the film was calculated using Equation 7.1 and was found to be 95.4 %.

The transmission properties of the optimised HWCVD poly-Si film are shown in Figure 7.11. Only one width (400 nm) was investigated and only the TE mode was measured. Five waveguides with lengths 0.1, 0.25, 0.5, 0.85, and 1.3 cm were used to determine the propagation loss. As Figure 7.11 shows, the linear fit of the measured propagation loss was $\sim$ 8.5 dB/cm. The estimated coupling loss was $\sim$ 10 dB per facet.

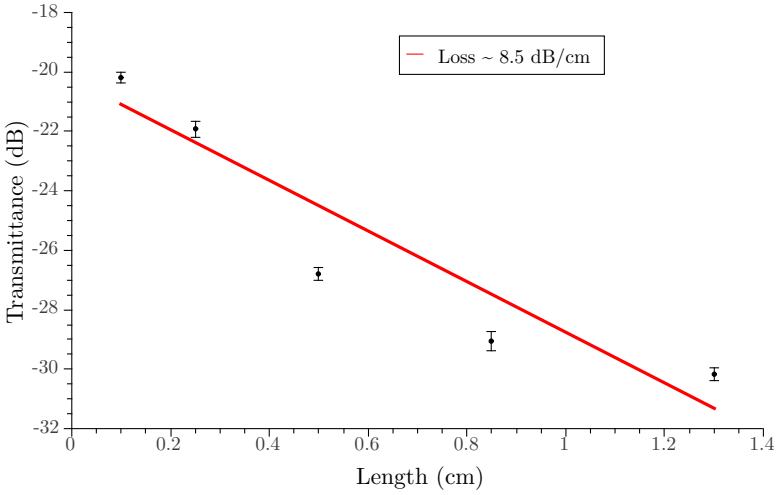


FIGURE 7.11: Transmission characteristics of the TE mode of the 400 nm wide polysilicon waveguides.

7.5 Discussion

7.5.1 Standard HWCVD p-Si Waveguides

Several loss mechanisms may contribute to the total propagation loss. The absorption loss L_{Absorp} is minimal because of the hydrogen-terminated dangling bonds. The RMS roughness of the SiO_2 PECVD was less than 0.5 nm. Hence, the scattering loss due the bottom polysilicon-SiO_2 interface roughness was assumed to be minimal. However, scattering loss from the grain boundaries, sidewall roughness, and top surface roughness can be significant. Scattering loss is generally a function of the confinement factor, Γ, which is in turn a function of the waveguide width, $\Gamma(w)$, for a given thickness. Hence, the propagation loss can be expressed as:

$$P_{\text{Loss}} \approx L_{\text{MatScatt}}\left(\Gamma(w)\right) + L_{\text{TopScatt}}\left(\Gamma(w)\right) + L_{\text{SideScatt}}\left(\Gamma(w)\right)$$

where L_{MatScatt}, L_{TopScatt}, and $L_{\text{SideScatt}}$ are the scattering losses due to grain boundaries, top roughness, and sidewall roughness, respectively.

3D finite-difference time-domain (FDTD) method was used to estimate the loss produced by both the top surface and sidewall roughness. FDTD Solutions by Lumerical Inc. was used to simulate a 220 nm thick and 500 nm wide waveguide with propagation lengths of 0.25, 0.5, 0.75, and 1 cm. The propagation loss was evaluated using the cut-back method. The geometry of the waveguide supports TE mode only and the confinement factor was estimated to be 0.95. The roughness parameters, extracted from AFM measurements, such as the RMS value and the auto-correlation length were incorporated into the roughness model. The sidewall roughness of the waveguide had an RMS value of 4 nm with an auto-correlation length of 120 nm. The sidewall roughness was computed by using both AFM and SEM measurements (Fig. 7.12). The material-induced absorption loss was excluded from the model. The simulation mesh had a resolution of 2 nm. Simulation results showed that the loss caused by the top surface and sidewall roughness were 9.2 and 3.1 dB/cm, respectively.

In order to confirm our simulation estimates, a 2D Fourier method was also used to calculate the loss contributions from the sidewall and the top surface roughness using the same structure and parameters used in the FDTD method [80]. Table 7.2 summarises the simulation results of the 3D FDTD and the 2D Fourier methods. The table shows that there is a discrepancy of only ±0.2 dB/cm between the two methods. The results from the two simulation methods show that the roughness of top surface has a higher impact on the transmission loss than that of the sidewall.

TABLE 7.2: Contribution of the scattering losses due to the top surface and sidewall roughnesses.

	L_{TopScatt} (dB/cm)	$L_{\text{SideScatt}}$ (dB/cm)
FDTD	9.2	3.1
2D Fourier	9.4	2.9

The material-induced loss can be calculated using the extinction coefficient, k. We used a *J.A. Woollam* spectroscopic ellipsometry system (192-1700 nm) and a multi-layer model to calculate the extinction coefficient from which the material-induced loss was found to be approximately 5.1 dB/cm. Provided the scattering loss is completely eliminated, the material-induced loss is similar to those of previously reported polysilicon waveguides [25, 28]. The loss can be further reduced by surface planarization by means of chemical mechanical polishing or similar methods. The grain boundaries scattering loss can be improved by deposition at higher temperatures than 240 °C.

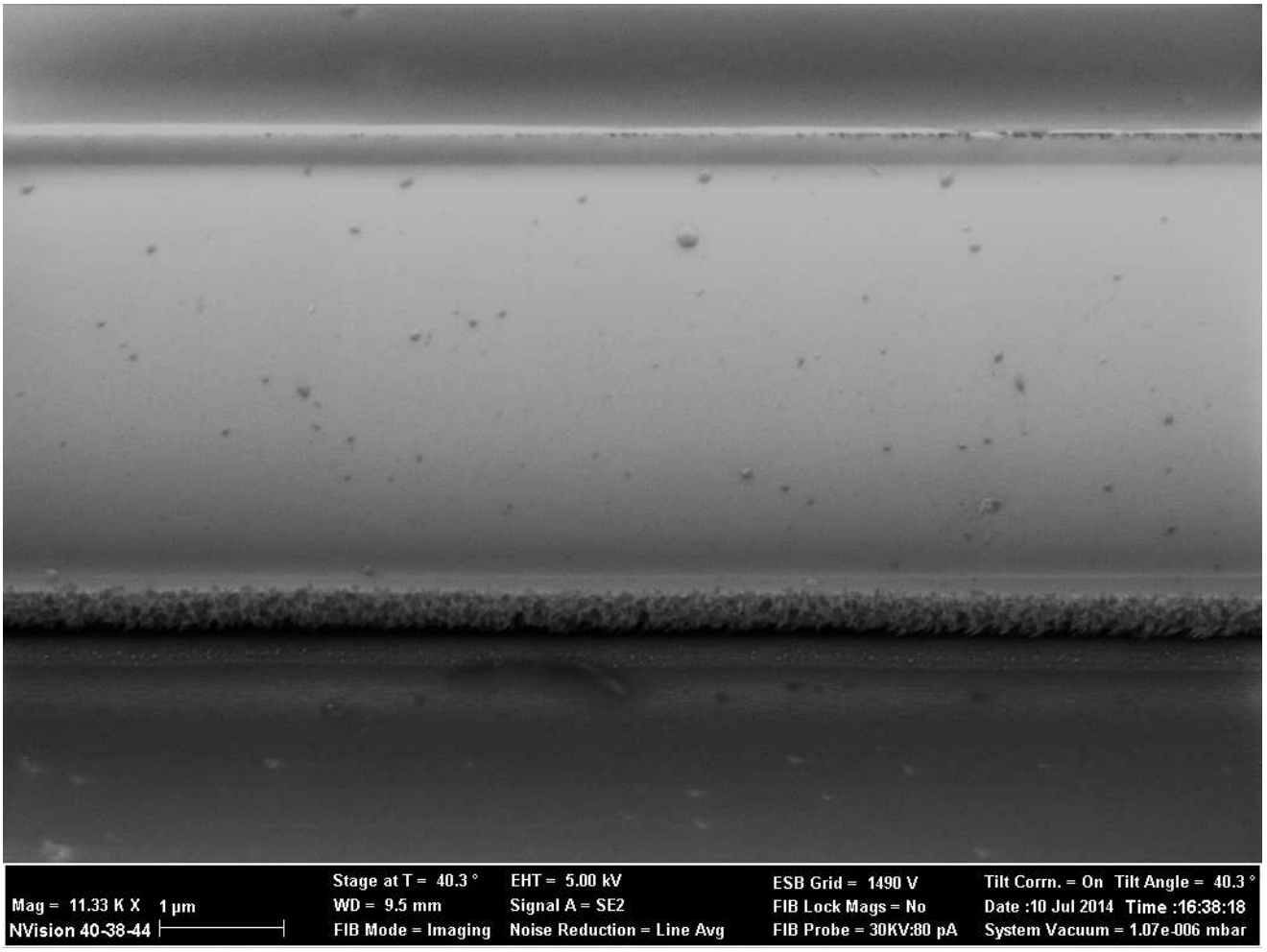


FIGURE 7.12: SEM image of the sidewall roughness of a multi-mode poly-Si waveguide (tapered section).

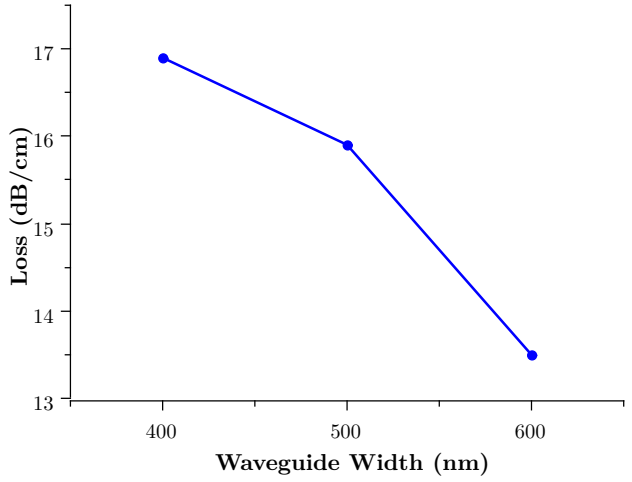


FIGURE 7.13: Transmission loss of the TE mode of the polysilicon waveguides with different widths. The inset shows the confinement of the TE mode in a 500 nm polysilicon waveguide in FDTD Solutions

7.5.2 Top Surface Roughness

Figure 7.9 showed approximately 45% decrease in the RMS roughness in the fist planarisation step for the intrinsic and n-type poly-Si films. An illustration of the planarisation process is shown in Figure 7.14. The as-deposited poly-Si films exhibit significant irregularities on the top as shown in 7.8 (a); a schematic diagram showing these irregularities is schematically shown in 7.14 (a). The protrusions are narrower towards their tips. Hence, the etch rate of these highly distorted and thin features is greater than that of smoother features due to more exposed surface area. As a result, the first planarisation step eradicate a significant portion of these protrusions and the surface is left smoother than before. Subsequent steps will be less efficient in reducing the RMS roughness because there is more material left to remove per volume of resist.

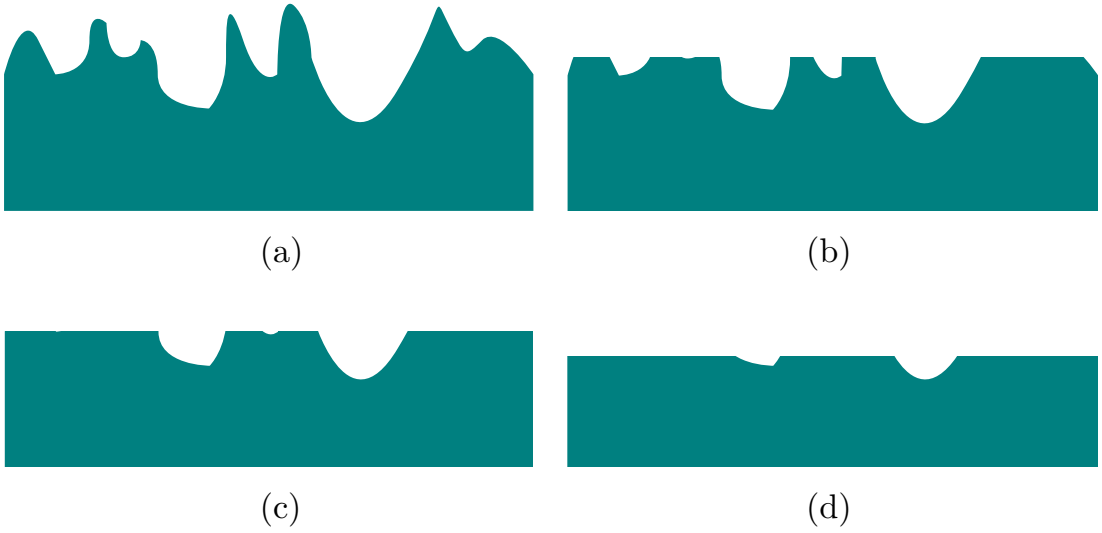


FIGURE 7.14: Illustration of the reduction in the top surface roughness by successive steps of RIE-based planarisation.

The reduction trend in the RMS roughness for the p-type poly-Si showed a linear and gradual decrease. The as-deposited p-type poly-Si film had smaller RMS roughness value than the intrinsic and n-type poly-Si films. These observation imply that the p-type film's protrusions have small aspect ratio (i.e. protrusions tend to be rounder); unlike those for the intrinsic and n-type poly-Si films. The reason for the trends noted in the p-type poly-Si film might be related to the integration mechanism of boron's atoms in the poly-Si's crystal structure.

The RMS roughness reduction appear to settle around $RMS \simeq 2.5$ nm. It is thought that this was a direct result of the viscosity and uniformity of the PMMA film. In other words, the ability of the PMMA resist to uniformly cover uneven features declines as the features' size approaches a limit: in this case it was ≈ 2.5 nm. One way to reduce the this limit is to decrease the viscosity of the PMMA resist by diluting it in DI water. Furthermore, spinning the resist at speeds higher than 5000 rpm might improve the uniformity of the PMMA resist over small features.

7.5.3 Optimisation of HWCVD Process

The results shown in Figure 7.10 confirm the strong dependency of the crystalline quality on the deposition temperature. High temperatures signify that the energy at the bonding sites on the substrate is higher than that of lower temperatures. Increased energy of the bonding sites leads to a proportional increase in the number of Si atoms bonding on the substrate surface (Figure 7.15). This, in turn, results in dense Si films. Moreover, the probability that a dissociated Si atom bonds with another one on the substrate surface (i.e. poly-silicon) increases with respect to the probability of that atom bonding to another dissociated atom above the surface (i.e. forming amorphous-silicon).

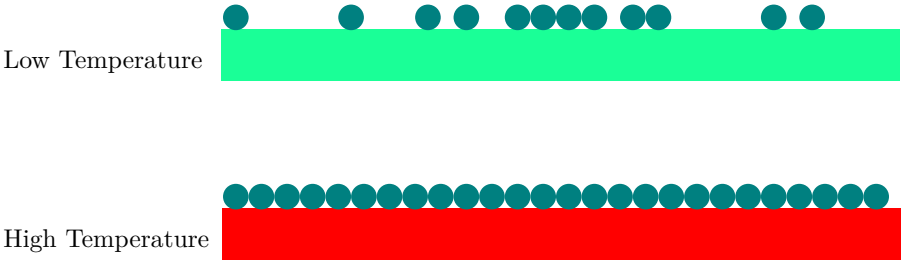


FIGURE 7.15: Illustration of the effect of temperature on the rearrangement of Si atoms on the surface of a substrate for HWCVD.

Figure 7.10 shows that under high and low pressure conditions, high dilution rate results in superior crystallinity than low dilution ratios. It is known that H_2 functions as a surfactant on silicon surfaces [112]. In other words, high H_2 content leads to high chemical etching of Si atoms on the surface. Thus, increasing the percentage of H_2 in the precursors mix results in lower deposition rates.

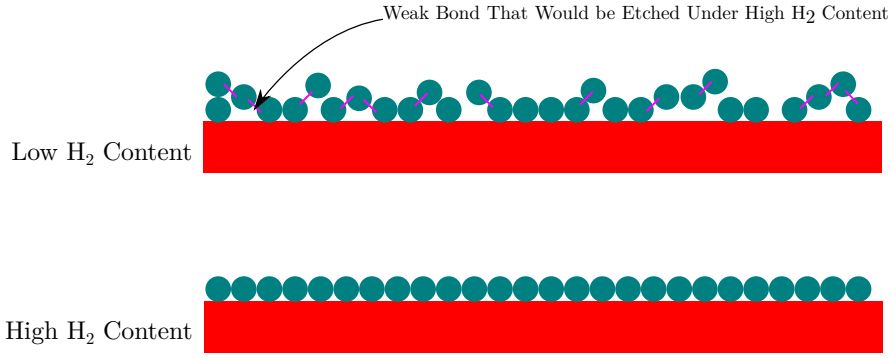


FIGURE 7.16: Illustration of the effect of H_2 content on the rearrangement of Si atoms on the surface of a substrate for HWCVD.

Hydrogen atoms have a stronger impact on weak Si bonds on the surface. Only strong Si bonds, which implies enhanced crystallinity, remain when the H_2 content is high (Figure 7.16). Consequently, low deposition rates yield denser films and hence the density of voids and tangling bonds decreases. In contrast, low content of H_2 results in the accumulation of weak Si bonds on the surface of the substrate. Weak Si bonds have detrimental impact on the crystalline quality of the poly-Si films.

It is clear from Figure 7.10 that the high pressure regime resulted in superior crystalline quality than the low pressure regime. Under the same flow rate of precursors, a high pressure environment means more atoms exist in the processing chamber per unit time than when the pressure is low. In other words, an atom stays longer inside the processing chamber under high pressure than low pressure environments. The additional time gained by the atoms increases their probability of settling on the substrate surface [113]. When the number of settled atoms increase, so does the density of the film and therefore the crystallinity improves as the number of voids and tangling bonds decrease.

The increase of the settling time should enhance the uniformity of the film (Figure 7.17). Atoms tend to flow towards and bond on high energy sites (i.e. high temperature) [113, 114]. Since the temperature gradient across the substrate is not uniform, this imperfection will transfer to the uniformity of the film thickness. However, increased settling time means that all energy sites, including low energy ones, have the chance to be filled as Figure 7.17 shows. Thus, the uniformity of the film's thickness improves.

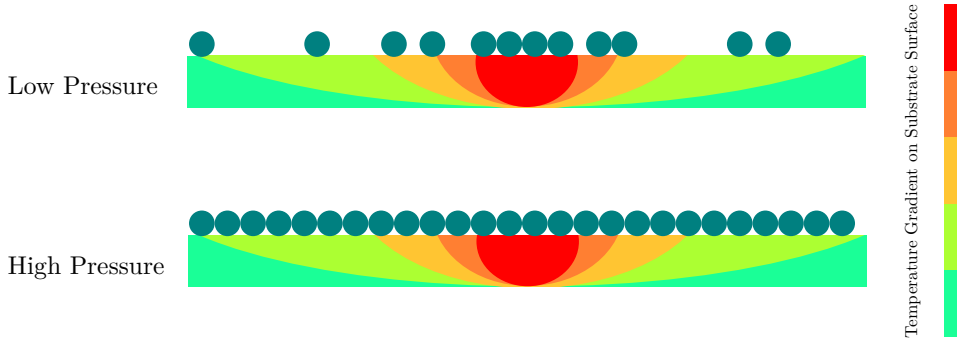


FIGURE 7.17: Illustration of the effect of chamber's pressure on the rearrangement of Si atoms on the surface of a substrate for HWCVD.

7.5.4 Polished HWCVD p-Si Waveguides

The preliminary measurement of the propagation loss of the improved HWCVD waveguide shows a significant improvement over the standard HWCVD waveguides detailed in section 7.4.1. The improvement in propagation loss is approximately 8.4 dB/cm. In other words, the improved waveguides exhibit approximately half of the propagation loss of that of the standard waveguides. However, a direct comparison between the standard and improved waveguides is disproportionate because the design of the two waveguides was different. While the standard waveguide had a cross-sectional dimensions of 220 by 400 nm, the improved waveguide had cross-sectional dimensions of 400 by 400 nm.

The enlarged thickness of the improved waveguides confinement within the core of the strip waveguides and reduces the interaction of the optical mode with the surface roughness. Moreover, the surface roughness of the improved waveguide was $\sim 27\,\%$ of that of the standard waveguide (i.e. the roughness was improved by 73 %). Furthermore, the HWCVD film was deposited at a higher temperature (360°C) than that of the standard waveguide (240°C).

7.6 Conclusion

This chapter showed that HWCVD is a viable and promising deposition process for silicon optical waveguides. As-deposited film (no post-treatment) was used to fabricate a reasonably low loss waveguides ($Loss \simeq 16.9$ dB/cm). Complications with the as-deposited film were analysed in detail in section 7.5.1 where two major loss mechanisms were identified; top surface scattering and sidewall scattering. It was also concluded that the top surface roughness constituted the majority of the scattering loss. Hence, work was carried out to planarise the top surface roughness using microelectronic processing. An etch recipe was developed and resulted in reducing the top surface roughness by approximately 70%. Using these planarisation results, slightly increased waveguide thickness, and a higher deposition temperature, a set of improved waveguides was fabricated and characterised. The propagation loss of the optimised waveguides was approximately 8.5 db/cm; i.e. a 50% improvement over the standard waveguides. This loss figure brings HWCVD-based poly-Si waveguide in a competitive position with the high-temperature-processed PECVD-based poly-Si waveguides which can exhibit losses of ~ 6 dB/cm [25].

The RMS roughness of the top surface roughness can be further reduced by chemical mechanical polishing (CMP) while the sidewall roughness can be reduced by etch recipe optimisation. Moreover, the sidewall roughness can be eliminated by patterning the waveguide on the SiO_2 layer first (i.e. trench) and then deposit the poly-Si film and carry out CMP to flatten the features. Because the sidewall of the SiO_2 layer is normally smooth, this will force the sidewall of the poly-Si film to be smooth as well.

Chapter 8

Conclusions and Future Work

This chapter briefly reviews the conclusions from this project and then proposes a roadmap for the future of the hybrid and low-temperature silicon-based optical devices investigated in this project.

8.1 Conclusions

- **Importance of Silicon Photonics**:
  The interest of using silicon as an optical material stems from its good optical properties around the telecommunication wavelengths, and the advanced silicon fabrication technology. Besides, the use of silicon offers direct integration route for optical and electrical integrated circuits; thus, reducing the cost of fabrication and development. This is arisen by the fact that the most successful microelectronic technology (CMOS) is based on silicon. Due to the relatively high refractive index of silicon ~ 3.5 at wavelengths above 1100 nm, light confinement can be realised in a submicron cross-sectional dimensions. Therefore, high density silicon optical interconnects can be fabricated on chip. Although some non-silicon optical materials are compatible with CMOS technology and can offer greater optical advantages than silicon, integrating them within silicon platforms induces higher costs that may not be justified [6].

- **Simulations**:
  The effect of the design parameters on the performance of a n-ZnO/p-Si FP and electro-absorption switches were investigated through electrical and optical simulations. The highly doped silicon over-layer is more suited to depletion-based devices than injection-based devices. However, operating the device in the depletion mode raises issues such as the pinching-off the silicon slab and the unavailability of phase-based optical structures. The thickness of the ZnO layer was also found to have an effect on the insertion loss of the device. A compromise must be made between sheet resistance of the ZnO film and the insertion loss induced by the ZnO film. An ideal device would have a small ZnO thickness as well as a high free carrier concentration: this structure would minimise the impact of the ZnO layer on the insertion loss while maintaining low resistivity in the ZnO film. A

10 nm thick ZnO layer with a free carrier concentration of $\geq 1 \times 10^{20}$ cm^{-3} constitutes a reasonable compromise. The thickness of the silicon slab also have an impact on a number of the device's characteristics such as the silicon sheet resistance, capacitance, and propagation mode. The slab thickness chosen (80 nm) favoured the sheet resistance because of its significant impact on the series resistance of the device.

- **Atomic Layer Deposition of Zinc Oxide**:
  The availability of two different deposition systems/methods in the SNC cleanrooms required a detailed examination of the deposition parameters/recipes to establish which system/method meets the requirements for the fabrication of a n-ZnO/p-Si electro-optical switch. The parameters of significance for each deposition methods and the targeted electrical properties to be optimised were identified. Then, the design of experiment (DoE) methodology was used to devise and analyse the effect of deposition parameters. The analysis of the results showed that TH-ALD resulted in superior electrical film properties than PE-ALD. Furthermore, the fact that the TH-ALD deposition system (Savannah) was more stable than FlexAl (PE-ALD deposition system) reinforced the conclusion to use TH-ALD for the fabrication of the hybrid n-ZnO/p-Si electro-optical switch.

- **Electro-Optical Switch Based on n-ZnO/p-Si**:
  The maximum temperature used to fabricate the devices reported in this project was 150 °C. The n-ZnO/p-Si heterojunction induced negligible insertion loss (1.2 dB/cm). The I-V characteristics and DC optical response of the diodes showed strong correlation for the electro-absorption switch. The high-frequency response of the devices is thought to be limited by the RC time constant of the junction rather than the minority carrier lifetime. Detailed review of the I-V characteristics and transient behaviour of the device revealed important imperfections. In particular, the series resistance of the devices was considerably high. High contact resistance as well as the existence of a suspected defective SiO_2 layer at the ZnO/Si interface are believed to cause the high series resistance and capacitance. The lateral distance of the contacts from the heterojunction is also believed to contribute to the large series resistance of the devices. Due to the formation of a parasitic SiO_2, the electro-absorption switch is believed to induce optical loss by two mechanisms: carrier injection and accumulation. The design can be improved by intentionally operating the heterojunction as an accumulation device as well as reducing the distance between the contacts and the heterojunction.

- **Low Temperature, Low Loss Poly-Silicon Waveguides Deposited Using Hot-Wire Chemical Vapour Deposition**:
  As-deposited film (no post-treatment) was used to fabricate a reasonably low loss waveguides ($Loss \simeq 16.9$ dB/cm). Complications with the as-deposited film were analysed in detail in section 7.5.1 where two major loss mechanisms were identified; top surface scattering and sidewall scattering. It was also concluded that the top surface roughness constituted the majority of the scattering loss. Hence, work was carried out to planarise the top surface roughness using microelectronic processing. An etch recipe was developed and resulted in reducing the top surface roughness by approximately 70%. Using these planarisation results, slightly increased waveguide thickness, and a higher deposition temperature, a set of improved waveguides was fabricated and characterised. The propagation loss of the optimised waveguides was approximately 8.5 db/cm; i.e. a 50% improvement over the

standard waveguides. This loss figure brings HWCVD-based poly-Si waveguide in a competitive position with the high-temperature-processed PECVD-based poly-Si waveguides which can exhibit losses of ~ 6 dB/cm [25].

8.2 Future Work

- **Design of the hybrid n-ZnO/p-Si electro-optical switch**:
  The analysis of the fabricated n-ZnO/p-Si electro-optical switches revealed critical issues with the electrical structure. Notably, the series resistance and capacitance were considerably high. In order to reduce the series resistance of the device, future work should focus on reducing the distance between the heterojunction and the metal contacts (d_c). Currently, $d_c = 6\ \mu$m and should be reduced to $\sim 0.5 - 1\ \mu$m. Moreover, using a capacitor design rather than a p-n junction would make the switch act as an accumulation device where the speed is only limited by the RC time constant and should improve the the power efficiency of the device. Furthermore, with the use of e-beam lithography and a capacitor design, the heterojunction device can also be operated in depletion mode. Other optical structures such as Mach-Zehnder interferometer should also be examined in future work.

- **Multi-layered poly-silicon platform for future silicon photonics systems**:
  Multi-layered structures add another dimension of design flexibility and enable the realisation of complex 3D optical structures. For example, light can be coupled from one layer to another where each layer processes the input light differently (e.g. modulate at different speeds). Multi-layered structures can potentially reduce the footprint of silicon photonics devices by spreading the operation over many layers. Future work should focus on examining and optimising the waveguide structures and the vertical coupling between layers. Future work should also examine the available technology to introduce active doping into poly-silicon films at low-temperatures. Most importantly, the integration of ZnO and poly-silicon to form active optical devices (switches) must considered in any future work.

- **Amorphous Silicon and Silicon Nitride**:
  In addition to the poly-Si, amorphous silicon (a-Si) and silicon nitride (SiN_x) low loss waveguide can be investigated to comprise passive structures. An advantage of HWCVD is that it can be used to deposit a-Si, poly-Si and SiN_x.

- **Chemical Mechanical Polishing**:
  In addition to the planarisation process developed in this project, chemical mechanical polishing (CMP) can be used in the future to reduce the surface roughness of poly-Si waveguides to RMS ≈ 0.2 nm.

Appendices

Appendix A

Fabrication Recipes

A.1 Lithography

A.1.0.1 Photolithography

Table A.1 shows the default S1813 recipe used for pattern transfer of some fabrication layers.

Spin Speed (rpm)	6000
Pre-Exposure Bake Temperature (°C)	110
Pre-Exposure Bake Time (s)	60
Exposure Time (s)	2
MIF 319 Development Time (s)	30

TABLE A.1: Positive Tone S1813 Default Recipe.

Table A.2 shows the default AZ MiR701 recipe used for pattern transfer of some fabrication layers.

TI-Prime Spin Speed (rpm)	3000
Spin Speed (rpm)	6000
Pre-Exposure Bake Temperature (°C)	100
Pre-Exposure Bake Time (s)	90
Exposure Time (s)	$5-6$
Post-Exposure Bake Temperature (110°C)	
Post-Exposure Bake Time (s)	60
AZ 726MIF Development Time (s)	90

TABLE A.2: Positive Tone AZ MiR701 Default Recipe.

Table A.3 shows the default AZ2070 recipe used for pattern transfer of some fabrication layers.

A.1.0.2 E-Beam Lithography

Table A.4 shows the default ZEP recipe used for pattern transfer of some fabrication layers.

Spin Speed (rpm)	6000
Pre-Exposure Bake Temperature (°C)	115
Pre-Exposure Bake Time (s)	90
Exposure Time (s)	$4-5$
Post-Exposure Bake Temperature (150°C)	
Post-Exposure Bake Time (s)	90
AZ 726MIF Development Time (s)	75

Table A.3: Negative Tone AZ2070 Default Recipe.

Spin Speed (rpm)	3565
Pre-Exposure Bake Temperature (°C)	180
Pre-Exposure Bake Time (s)	180
Exposure Dose (J/cm^2)	190
ZED-50 Development Time (s)	$90-120$

Table A.4: Positive Tone ZEP Default Recipe.

Table A.5 shows the default PMMA recipe used for pattern transfer of some fabrication layers.

Spin Speed (rpm)	5000
Pre-Exposure Bake Temperature (°C)	170
Pre-Exposure Bake Time (s)	90
Exposure Dose (J/cm^2)	$400-500$
ZED-50 Development Time (s)	75

Table A.5: Negative Tone PMMA Default Recipe.

A.2 Etching

A.2.1 Wet Etching

Table A.6 shows the etch characteristics of different materials in hydrogen fluoride (HF).

Material	HF 7:1 (nm/s)	HF 20:1 (nm/s)
SiO_2	≈ 1.7	≈ 0.5
Al_2O_3	≈ 0.1	-

Table A.6: HF Wet Etch.

Table A.7 shows the etch characteristics of different materials in hydrochloric acid (HCl).

Material	HCl 46% DI-Water Diluted to 1:180 (nm/s)
ZnO	≈ 50

Table A.7: HCl Wet Etch.

A.2.2 Dry Etching

Table A.8 shows the dry etch characteristics of crystalline silicon (c-Si).

O_2 Flow (sccm)	12
SF_6 Flow (sccm)	12
Pressure (Torr)	30
Power (W)	100
Etch Rate (nm/s)	≈ 3.1

TABLE A.8: Recipe 1: RIE recipe for smooth sidewall etching of c-silicon.

Table A.9 shows the dry etch recipe used for poly-silicon top roughness planarisation.

O_2 Flow (sccm)	16
SF_6 Flow (sccm)	36
Pressure (mTorr)	30
Power (W)	200
poly-Si Etch Rate (nm/s)	≈ 8
PMMA Etch Rate (nm/s)	≈ 8

TABLE A.9: Recipe 2: RIE recipe for planarising top surface roughness of poly-Si HWCVD films.

Table A.10 shows the dry etch recipe used for stripping resists.

O_2 Flow (sccm)	600
Power (W)	0.8
Pressure (mbar)	95
Photoresist Etch Rate (nm/s)	≥ 25

TABLE A.10: Tepla Asher recipe for stripping photoresists/e-beam resists.

A.3 Deposition

A.3.1 Plasma-Enhanced Chemical Vapour Deposition (PECVD)

Table A.11 shows the default SiO_2 deposition recipe using PECVD.

Temperature (°C)	350
Pressure (mTorr)	1000
SiH_2 Flow (sccm)	80
H_2 Flow (sccm)	400
Deposition Rate (nm/s)	1

TABLE A.11: PECVD recipe for SiO_2 deposition.

A.3.2 Hot-Wire Chemical Vapour Deposition (HWCVD)

Table A.12 shows the default poly-silicon deposition recipe using HWCVD.

Temperature (°C)	360
Pressure (mbar)	0.024
SiH_2 Flow (sccm)	6
H_2 Flow (sccm)	294
Deposition Rate (nm/s)	0.06

Table A.12: Standard poly-Si HWCVD Recipe.

A.3.3 Atomic Layer Deposition (ALD)

Table A.13 shows the default zinc oxide deposition recipe using TH-ALD.

Parameter	Value	Parameter	Value	Parameter	Value
Temperature (°C)	150	Dose Time (ms)	30	DEZ Purge Time (s)	2
O_2 Plasma Time(s)	4	O_2 Purge Time (s)	3	Pressure (mTorr)	80

Table A.13: Standard ZnO PE-ALD recipe supplied by Oxford Instruments.

A.4 Polishing

Table A.14 shows the default silicon waveguide polishing recipe.

	Polishing Grit (μm)	Time (minutes)
Step 1	3	0.5-1
Step 2	1	15
Step 3	1	15
Step 3	0.1	10

Table A.14: Polishing Recipe.

Appendix B

Additional Results

B.1 Chapter 6

Figure B.1 shows the extended I-V characteristics of the n-ZnO/p-Si electro-absorption switch.

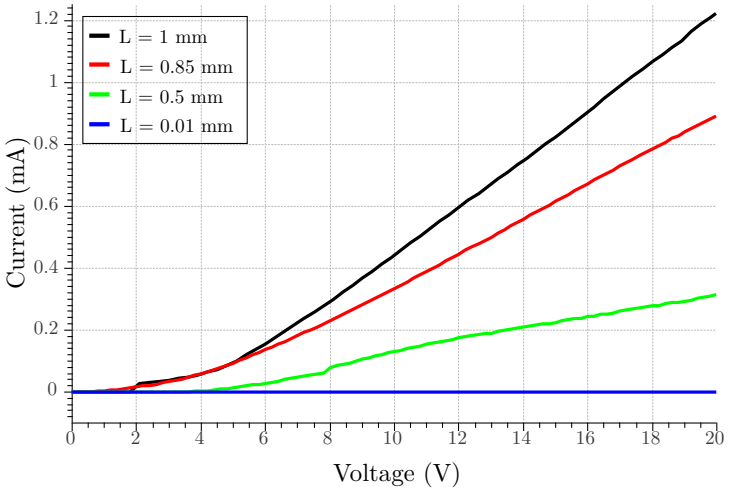


FIGURE B.1: Extended I-V characteristics of the n-ZnO/p-Si electro-absorption switch.

Figure B.2 shows the I-V characteristics of the n-ZnO/p-Si Fabry-Perot optical switch.

Figure B.3 shows the J-V characteristics of the n-ZnO/p-Si Fabry-Perot optical switch.

Figure B.4 shows the transient response of the circuit shown in Figure 6.13 with $R_{\text{load}} = 560\,\Omega$.

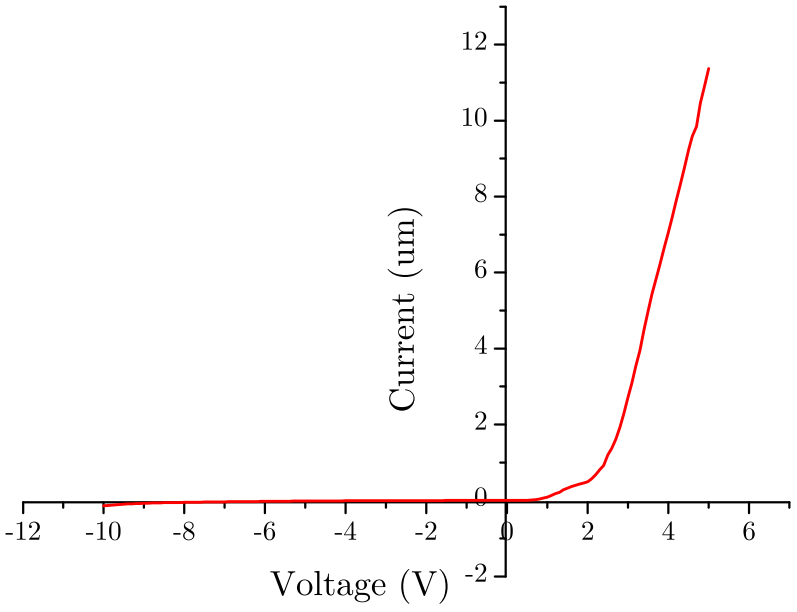


FIGURE B.2: I-V characteristics of the n-ZnO/p-Si Fabry-Perot electro-optical switch.

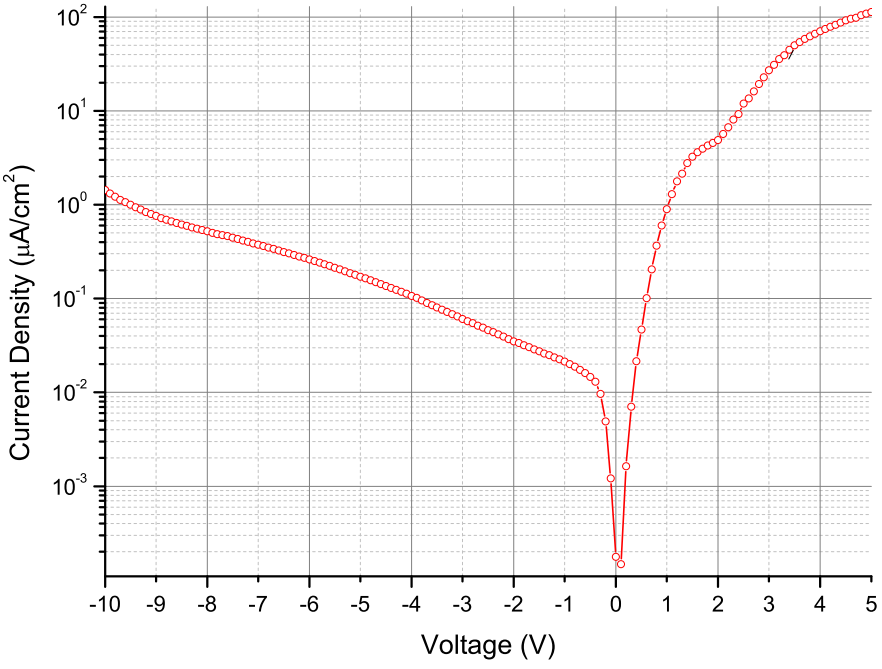


FIGURE B.3: J-V characteristics of the n-ZnO/p-Si Fabry-Perot electro-optical switch.

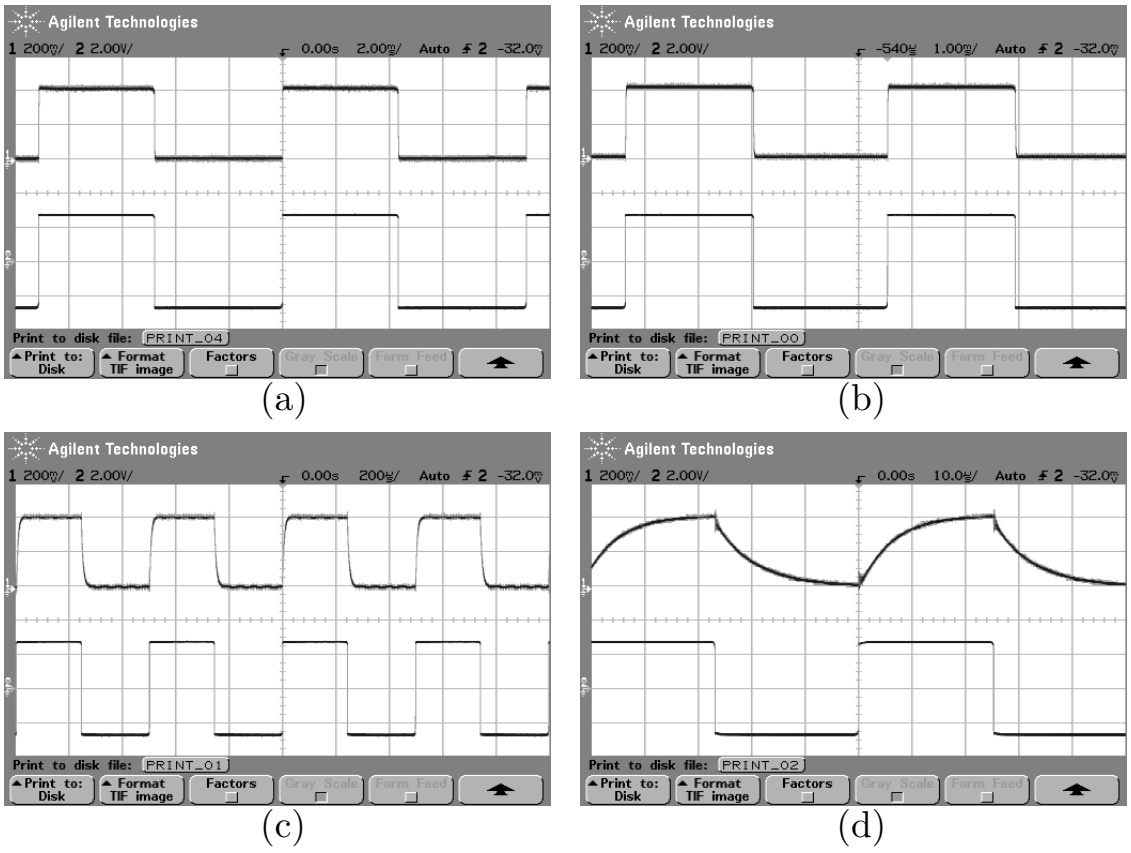


FIGURE B.4: Transient response of the circuit shown in Figure 6.13 with $R_{\text{load}} = 560\,\Omega$.

Appendix C

AtlasToLumerical User Manual

C.1 Introduction

Atlas Silvaco is a simulation package that can be used to simulate the behaviour of micro-electronic devices. Information about the characteristics of a device is normally obtained using TonyPlot. However, the data can only be extracted in a picture form. In other words, physical quantities calculated by Atlas cannot be accessed directly. For example, the concentration profile of carriers in the depletion region of a p-n junction device can only be represented as an image of concentration contours.

AtlasToLumerical can enables users to access the values of all physical quantities calculated by Atlas. It can also be modified to export to text files (or excel) in different data formats. However, it is currently being developed to output a data format that is compatible with simulation software that is used to simulate photonic devices (Lumerical). Currently, AtlasToLumerical obtains electron and hole concentration only from Atlas structure files.

C.2 User Interface

The user interface is self-explanatory and displays basic information imported from an Atlas structure file. The lower section of the form can be used to obtain advanced results based on the sampling capabilities of AtlasToLumerical.

C.3 Compatibility and Requirements

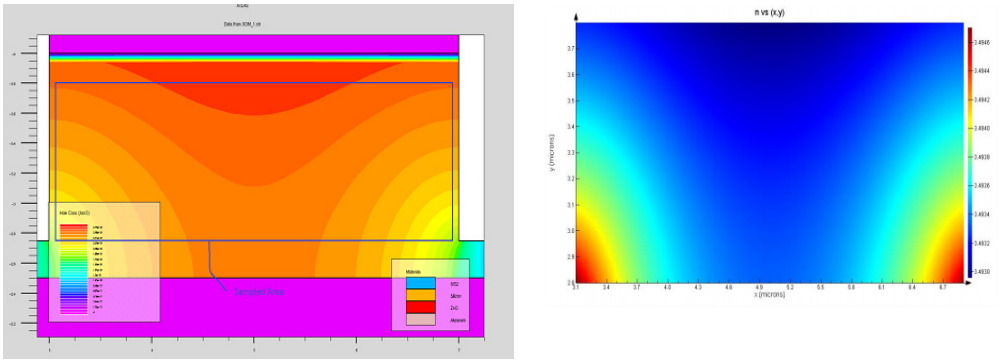
1. The material of the sampled area must be Silicon.
2. The y-coordinate scale must indicate negative values in Atlas.
3. The x-coordinate scale must indicate positive values in Atlas.

4. Care must be taken to indicate whether free carriers are depleted or injected into the area of interest.

C.4 Quick Operation Manual

1. Ensure that simulation results are stored in a structure (.str) file. Note that a basic .str file that contains only meshing information is not supported.
2. Click on the Load .str file button.
3. You can access basic information about each node/triangle forming the mesh from the Node/Triangle Info group boxes.
4. Hole and electron concentration at any point within the simulation area can be individually obtained using the Point group box. Note that the input XY coordinates must be within the area of simulation and the material is silicon.
5. Enter the sampling resolution in the x and y axis.
6. Specify a sub-area within the simulation area that you want to sample, as shown in Figure 58.
7. Click Export and define an output text file.

C.5 Examples

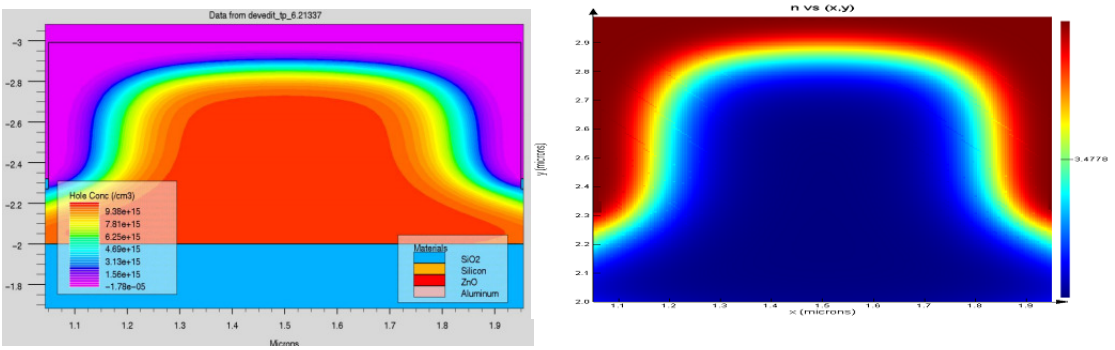


(a) (b)

FIGURE C.1: An example of how AtlasToLumerical is able to translate Atlas' simulation results to a format that can be read by Lumerical FDTD. (a) shows the distribution of free hole concentration within a silicon waveguide. (b) shows the corresponding distribution in the refractive index.

C.6 Sampling Strategy

The behaviour of several photonic devices is characterised by the gradient of carrier concentration which directly influences the refractive index of materials. This software was developed at the



(a) (b)

FIGURE C.2: Another example of how AtlasToLumerical is able to translate Atlas' simulation results to a format that can be read by Lumerical FDTD. (a) shows the distribution of free hole concentration within a silicon waveguide. (b) shows the corresponding distribution in the refractive index.

University of Southampton to overcome the lack of proper extraction tools in Atlas. Simulation results of electrical characteristics are extracted from an Atlas structure file and exported into (n, k) Material FDTD Lumerical file.

In Atlas, different regions in a device are divided into triangles of different shapes and areas. The electrical properties are calculated at the vertices of these triangles. For a given point that is not a vertex of any triangle, free carrier concentrations are calculated using the strategy described in the next sections.

C.6.1 Identifying the Triangle that Encompasses a Target Point

In order to determine whether a point is encompassed by a particular triangle, a simple approach that relies on the total area is employed. A target point is inside a triangle provided the area of that triangle is equal to the sum of the areas of the three triangles formed by the target point and each pair of vertices as shown in C.3 (a). However, due to the ability of computers to manipulate figures to a large number of decimal places, the area of the sum of the constituent triangles may not exactly equal the original triangle. For example, assume vertices are represented to three decimal places, and that due to high sampling requirement, a target point is represented by nine decimal places. The resultant sum would unavoidably have more decimal places than the original area.

It is, however, possible to limit the number of decimal places (or significant figures) when comparing two numbers within .NET environment. Nonetheless, the accuracy may be compromised; a target point could be allocated to the wrong triangle especially near the border of a triangle. Consequently, a compromise must be made. The number of decimal places to include depends on both the meshing and sampling resolutions. By default, five decimal places are used.

C.6.2 Calculation of Free Carrier Concentration at a Point

Assume that the free carrier concentration at point that is not a vertex is unknown. Moreover, assume that the properties of the triangle in which the point is inside are known. In other words, x-y coordinates and electrical properties at the three points constituting the triangle that encompasses the target point are known. Note that an area that is not a part of a simulated device is not meshed and hence a target point may not be encompassed by a triangle. In order to calculate the concentration at a target point, linear decay of concentration is assumed between adjacent nodes.

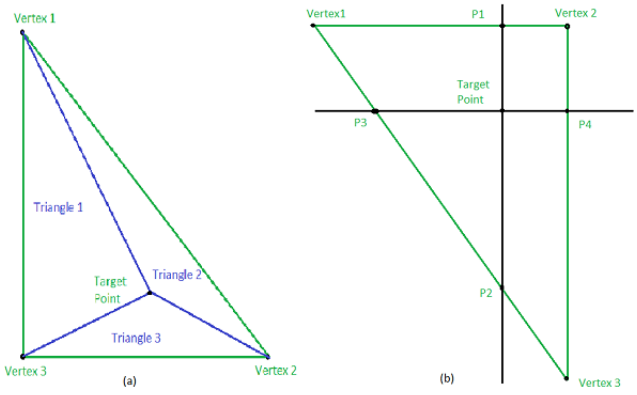


FIGURE C.3: (a) shows a diagram of the triangles formed by the target point with the vertices of the original triangle. (b) illustrates a triangle with its vertices and a target point.

For instance,C.3 (b) shows a triangle that includes a target point where free carrier concentration need to be calculated. First of all, the concentrations at the four points labelled P1, P2, P3, P4 are calculated by assuming linear decay between adjacent vertices. Then, the concentration at the target point is obtained by averaging the concentrations calculated vertically (P1 to P2) and horizontally (P3 to P4).

C.6.3 Exporting

Information acquired by AtlasToLumerical is outputted to a text file that conforms to the (n, k) Material file data format1. Free carrier concentration of silicon is converted into n and k using the refractive index change the absorption change equations [81]:

$$\delta n = -\left[8.8 \times 10^{-22} \times \delta n_e + 8.5 \times 10^{-19} \times (\delta n_h)^{0.8}\right] \tag{C.1}$$

$$\delta \alpha = -\left[6.0 \times 10^{-18} \times \delta n_e + 4.0 \times 10^{-18} \times \delta n_h\right] \tag{C.2}$$

The values of n and k exported to Lumerical do not merely depend on and but also on the starting values of n and k that correspond to the original free carrier concentration. For instance, assume a user wants to calculate the change in the real refractive index of silicon at a particular point.

Moreover, the users design is based on depleting a finite area of free carrier; this implies using doped silicon. AtlasToLumerical stores the real refractive index of intrinsic silicon and alters this value according to the change in the free carrier concentration. Hence, the user is obliged to enter the doping concentration before exporting. The software, in turn, calculates the change in the refractive index from the entered doping concentration. Then, the change in the spatial carrier concentration, imported from Atlas, is used to compute the final values of n and k.

C.7 Basic Interpretation of *.str* Files

Character Identifier	Interpretation
c	Provides x-y-z coordinates of a node
t	Provides information about a triangle
s	Provides information about the structure of the n identifier
n	Provides calculated values for different quantities at a node
r	Refers to a region

TABLE C.1: Character identifier information.

This section provides a preliminary translation of Atlas structure files. Each line in an Atlas structure file starts with a character identifier. Moreover, different quantities may be referenced using constant numbers, Table 4.

The s character identifier introduces information about the n character identifier line. For example, the first number indicates the number of quantities following the n identifier. The number of the numbers following the first number will be equal to the first number. Moreover, the following numbers will be constants that indicate different quantities. For instance, the constant 121 refers to electrons concentrations while the constant 224 refers to hole concentration. Finally, the n character identifier is followed by values calculated from Atlas at each node. Note that these start with 0 while the c starts with 1.

C.8 Common Problems

A numerical value sometimes cannot be computed because of several reasons:

1. A target point cannot be found inside any triangle.
2. A target point may be misplaced in the wrong region.

To overcome these faults, it is important to consider the following recommendations:

1. If the sampled region borders an insulator or metal regions, it is best to start and end sampling within the silicon region (NOT exactly at the border).
2. It is advised to mesh the region in interest such that the triangles heights and widths are comparable. In other words, if a triangle has an acute angle, the error in determining whether a point is inside it increases.

Appendix D

Introduction to the Design of Experiment (DoE)

Research is primarily based on simulation or practical laboratory experiments. The yield of carrying out experiments should be an improved understanding about the nature of a physical phenomenon. Therefore, it is important to design a set of experiments that sufficiently scan the domains of the factors influencing the output or the physical quantity under investigation. Although some factors may be uncontrollable, such as environmental noise, replicate experiments are utilised to account for uncontrollable varying quantities.

An intuitive approach to determining the effects of several factors on the output of an experiment is to vary the value of one factor at a time and observe the deviation in the output. This process continues until no changes are observed in the output and is known as the COST-approach. Despite being the natural way of scanning the domain of the output variables, this approach does not guarantee accurate information about the optimum [92]. Figure D.1 shows how varying two variables independently does not guarantee the identification of the optimum.

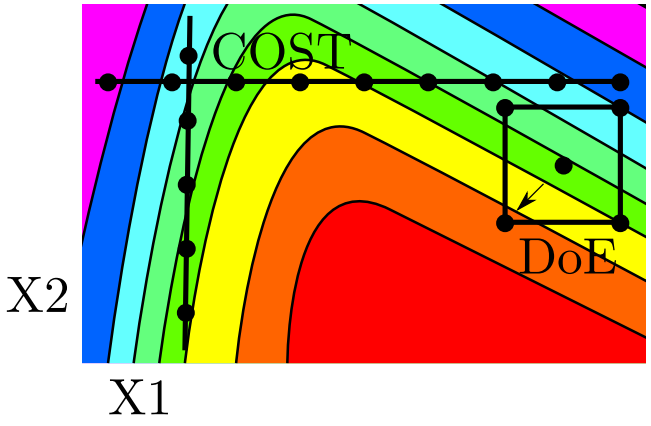


FIGURE D.1: An example of the COST-approach versus design of experiment (DoE) approach. The optimum found by varying the two factors independently (COST) is not guaranteed to be the global optimum. Because the set of experiments in a DoE is defined in a rectangular fashion, the direction towards the optimum can be inferred easily (see arrow) [92].

A superior approach is to vary all input factors simultaneously using predefined rules governing incremental change in each factor [92]. This approach is known as statistical experimental design or more commonly known as design of experiment (DoE) (Fig. D.1). In a DoE design, the experiments form a rectangle in the factors experimental space in the case of two factors: in a multi-factors investigations, all experiments are orthogonal to each other. This constraint guarantees the identification of the optimum or at least a direction towards the optimum region.

Another important advantage of using DoE is that only a few experiments needed to establish some information about the investigated space. In the COST approach, each factor may require at least 3 to 5 experiments to explore its effect. With three factors to investigate, this number can rise up to 15 experiments with uncertainty of optimum position remains. In the DoE approach, three factors require approximately 8 experiments ($2^3 = 8$), depending on the type of DoE used.

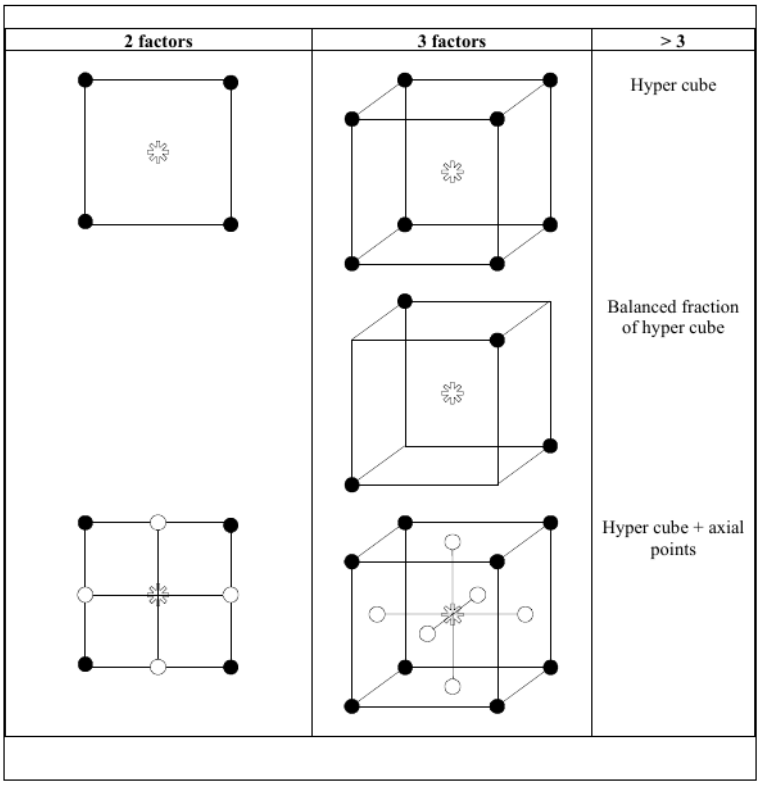


FIGURE D.2: Examples of *full factorial designs*, *fractional factorial designs*, and *composite designs* [92].

There is a number of statistical designs used in DoE such as *full factorial designs*, *fractional factorial designs*, and *composite designs* [92]. The choice of the design depends on the number of factors as well as the purpose of the investigation. For example, a fractional factorial design is appropriate when the number of input factors is large or when quick screening of the investigation space is needed. On the other hand, a composite design would be preferred for optimisation or when the effects of factors are interlinked. Figure D.2 shows some examples of those three statistical designs.

The analysis of the effects of the investigated factors on each experimental outcome is carried out using linear, interaction, and quadratic models. One of the most commonly used response

models is called the surface response model (RSM). The RSM model is a second order regression model with coefficients that best explain the behaviour of the DoE responses. RSM models normally constitute a number of terms for of which some are quadratic, some are linear, and some are constants. The quadratic terms may involve the square response of the factors or the multiplication of two factors to establish the interaction relationship between two factors. For more details on the RSM, please see [92].

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