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UNIVERSITY OF SOUTHAMPTON

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Optoelectronics Research Center

**Erasable Diffractive Grating Couplers in Silicon on
Insulator**

By Rob Topley

Thesis submitted for the degree of Doctor of Philosophy

October 2014

“The trouble is, you think you have time.” - *Jack Kornfield*

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING

Optoelectronics Research Center

Doctor of Philosophy

ERASABLE DIFFRACTIVE GRATING COUPLERS IN SILICON ON INSULATOR

This doctoral project investigates the design, fabrication and characterisation of germanium implanted grating couplers in silicon on insulator and their subsequent removal by laser annealing. The application for these devices is dominantly seen to be in wafer scale testing for optical integrated circuits, though the planar surface may offer benefits in other areas such as 3 dimensional optical circuits. Wafer scale testing is critical to reducing production costs and increasing production yield. In this thesis a method that allows testing of individual optical components within a complex optical integrated circuit is described. The method is based on diffractive grating couplers, which can be used to efficiently couple light from an optical fibre to a silicon waveguide. In this work gratings are fabricated by the introduction of lattice disorder, induced by ion implantation of germanium opposed to the typical surface relief structure typically used. The lattice damage alters the crystalline structure of silicon, hence causing a change in the refractive index. Coupling performance determined empirically, showed a 5.5dB loss between the fibre and planar waveguide modes, which is not dissimilar to the performance of typical uniform surface relief gratings currently used.

Gratings fabricated using this method can be erased via localised laser annealing after device testing is completed. Annealing is shown to reduce the outcoupling efficiency of the gratings fabricated by ~21dB. Laser annealing was achieved by employing a continuous wave laser, operating at visible wavelengths thus reducing equipment costs compared with traditional annealing systems, which use a pulsed, deep ultra violet laser. The process developed retains CMOS compatibility which enables the design to be used in current microelectronics fabrication facilities.

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Academic Thesis: Declaration of Authorship

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Erasable Diffractive Grating Couplers in Silicon on Insulator

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Journal Papers

1. **R. Topley**, L. O'Faolain, D. J. Thomson, F. Y. Gardes, G.Z. Mashanovich, G.T. Reed, "Planar surface implanted diffractive grating couplers in SOI," *Optics Express*, vol. 22, pp. 1077-1084, 2014.
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Chapter 1 - Introduction

1.1 Optical Communications

Optical communication allows data transmission at much faster rates than is possible with electrical connections. Electrical connections have a non-negligible resistance which introduces noise to the system as well as being affected by electro-magnetic interference. Electrical connections at high frequency also have problems with skin effect which increases resistance proportionally with frequency and in turn increases interference. Optical communications do not suffer from these issues allowing a higher data bandwidth over a longer distance by comparison to electrical connections. Electrical data networks are failing to meet demand with ever growing needs for high bandwidth communications to allow, among other things, simultaneous use of the internet, on demand high definition television and consumer video calling.

In order to realise a fully optical system with no electrical bottle necks, optical integrated circuits are required, allowing data to be passed directly into a processing unit optically. This is of particular significance for data centres, where high data throughput is critical. Though the back bone and cross connects in a data centre are typically already optical, the data transport to the server is typically over copper wires to reduce costs, introducing a troublesome bottle neck. Low cost, low power integrated optics technologies such as silicon photonics are key to delivering data at high speeds directly to the processor. It has been suggested by the UK minister of state for industry and the regions, Margaret Hodge MBE MP that photonics in the 21st century will be as significant as electronics was in the 20th century or steam in the 19th century [1].

1.2 Silicon Photonics

Silicon on insulator is just one of many technologies that is being used to develop integrated optical circuits. By using silicon to develop optical integrated circuits it is possible to utilise the current knowledge of manufacturing of silicon based microelectronics and transfer the same manufacturing techniques to photonic circuits. This will prevent the nanotechnology development process needing to be carried out again for a new material platform, also enabling easier integration between electronics and photonics. Together with the low cost of silicon and high volume manufacturing infrastructure, which is already in place, this presents a firm basis for continued

investigation. The drawback is that silicon is a poor optical material by comparison with several other more exotic materials and only operates over a limited range of infrared wavelengths. Despite the constraints imposed, silicon photonics has grown significantly in the past decade, adapting to suit a diverse range of applications. A wide range of integrated components can now be realised, including high speed modulators [2-5], low cost photo-detectors [6, 7], and monolithically integrated lasers [8]. Autonomous wafer scale testing is one of the few remaining challenges for a successful large scale silicon photonics platform to be realised.

Silicon photonics is already gaining traction with big names such as Intel, Hewlett Packard and Microsoft. Kushagra Vaid, the general manager of cloud server engineering at Microsoft said “We believe that MXC [Intel optical connector] along with Intel Silicon Photonics will be instrumental in shaping next generation high performance data centre architectures...”[9]. While HP have begun to redevelop a “stale, decades old” computer architecture[10], putting memristors and silicon photonics at the core of their new computer architecture, which they expect to perform faster than current architectures whilst using considerably less energy [10].

1.3 Erasable Grating Couplers for Wafer Scale Testing

Two significant problems arise when trying to pass an optical signal between a silicon waveguide mode and an optical fibre mode. A standard telecom optical fibre is not polarisation maintaining, which means the output from the end of a fibre is effectively of random polarisation; however an SOI strip waveguide is typically polarisation dependant. It is also apparent that high efficiency coupling is difficult between the two due to a mode size mismatch. Optical power is dominantly confined within the core of an optical fibre, which is typically around $10\mu\text{m}$ in diameter for telecommunications at 1550nm; this is compared to a silicon on insulator (SOI) waveguide mode which is dominantly confined within the waveguide and typically has cross sectional dimensions of around 220x400nm. Grating couplers are one method of coupling light from an optical fibre to a silicon waveguide. Grating couplers are very simple structures to utilise and alignment can typically be made manually within a matter of minutes, this could be made considerably faster by automation making them an ideal

basis for a quick testing mechanism in silicon photonics. Further details on grating couplers can be found later on in this thesis.

The real question is why one would want to remove the source of coupling to or from a waveguide. The answer is simple, unlike an electronic circuit it is not possible to apply a simple test probe to an optical waveguide to monitor the signal, which prevents automated optical integrated circuit testing. This is a problem that makes quality control very difficult in a manufacturing environment. Processed silicon has a relatively high cost associated with it. If a fabrication error occurs, the early identification of the problem could lead to significant cost savings.

Maximising wafer yield is essential for cost reduction and introducing silicon photonics to the mainstream [11], yet currently very few options are available to ensure the integrity of an optical device until the device is fully processed and fully functional. Test points are essential in allowing optical circuits or individual components on a wafer to be autonomously tested after selected manufacturing steps, hence allowing poor performance or device failures to be detected early so that either production can be ceased or the damaged device repaired using direct write methods [12]. Optical assessment could be performed under a microscope by an operator or a computer vision system, though this would be expensive and time consuming in a manufacturing environment and would only provide very limited information such as component dimensions or a dramatic processing error, such as a significant under or over etch.

In 2008 a method was suggested of incorporating a metal grating coupler directly onto the end of a fibre facet, effectively creating a test probe [13]. The probe created had limited durability due to the fragile nature of the unprotected metal thin film, and the probe had to be placed within 200nm of the waveguide surface to achieve efficient coupling. Such close proximity thus prevents testing if the waveguide is coated with any cladding and could result in the samples being contaminated with gold, preventing this technique from being used in CMOS fabrication facilities, though other materials may be used to overcome this issue [14].

Simulations for flexible waveguide probes have been presented on multiple occasions with the most recent results quoted in 2011 [15-17], the probes are made of SU8

photoresist and operate using the same principle as an on chip directional coupler. In certain cases a silicon waveguide is also embedded into the flexible film to enhance the coupling efficiency. Simulations have demonstrated efficiencies as high as 95% [15] for this style of device, however empirical results have not stretched beyond 4% [16]. Much like the metal grating probes, efficiency drops off rapidly for separations above 200nm. The method relies on flexing a thin film, which is also likely to give rise to issues with durability and the physical contact required with an unclad waveguide may also give rise to contamination issues.

Also in 2011 a CMOS compatible wafer scale testing methodology was presented utilising erasable Bragg reflectors [18, 19]. Bragg grating reflectors reflect light back along a waveguide and data can be collected by connecting the input fibre to a detector via a circulator, opposed to grating couplers which allow light to be directly coupled out of the waveguide. Erasable Bragg reflectors have the potential to offer a useful wafer scale testing methodology for devices spanning a small wavelength range, with typical erasable Bragg reflectors offering up to a few nanometers wavelength reflectivity, though wider channels could be interrogated using longer Bragg reflectors, lengths of $\sim 400\text{-}600\mu\text{m}$ per nanometre of channel bandwidth to be interrogated would be required [19]. The other disadvantage to monitoring a reflection is it may not depict the operation of devices which have asymmetrical transmission characteristics accurately, such as optical modulators. However, by moving to a scheme using an erasable grating coupler, the single pass transmission characteristics can be easily obtained. Unlike Bragg reflectors, grating couplers direct light towards the superstrate as opposed to relying on transmitting a reflection back through the circuit to the input surface relief grating coupler to obtain the test data. Grating couplers are relatively easy to fabricate and they allow light to be coupled out from any location on the device without the need for polishing, thus making them a good candidate for an optical test point.

1.4 Aims and Objectives

The aim of this work is to devise, design and fabricate a device to facilitate wafer scale testing in the silicon on insulator platform.

In order to realise a device to facilitate wafer scale testing, a thorough understanding of coupling methods must be established along with methods of altering the refractive index in silicon. Once viable coupling methods have been established, a literature review must be undertaken to uncover prior art, with a view to delivering a device which improves upon current testing methods. Strengths and drawbacks of the proposed solution must also be taken into account. Relevant simulations will be performed to optimise the structures before fabrication is undertaken. Devices must subsequently be characterised and relevant investigations undertaken. The coupling performance of the devices in this work will aim to be comparable to surface relief grating couplers, the typical method used for coupling to an optical circuit today.

Chapter 2 - Background and Theory

2.1 Silicon Photonics

To enable silicon photonics to become a mainstream technology there are six main areas which are requisite for a successful platform, each area is depicted in Figure 2.1.

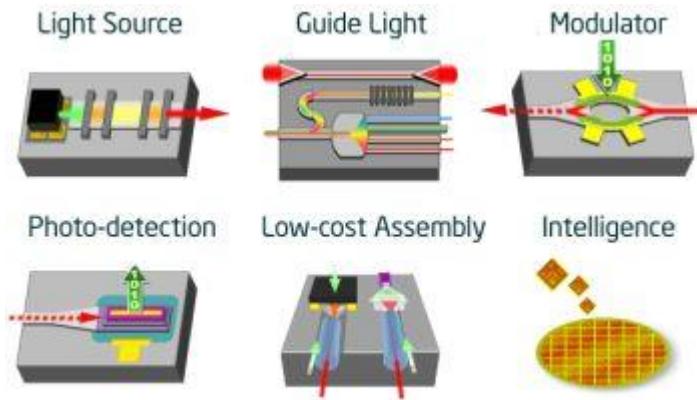


Figure 2.1 - Main building blocks of silicon photonics [20]

Light Source: A light source, typically a laser is essential to the operation of any integrated photonic circuit. A silicon based laser is well known to be very challenging but may provide advantages against an off chip laser. A silicon based laser would allow the light source to be integrated to the silicon wafer thus reducing cost, overall power consumption and reduce the complexity of the device, but it may also add localised power consumption and heat which may be an issue in a microprocessor which is already limited by hot spots and localised heating.

Mechanisms of light emission in silicon currently under development include doped nanocrystals [21], integration of III-V devices onto silicon [22], Raman scattering [23-25] and dislocation loops [26, 27] of which the latter two options are most desirable as they allow monolithic integration with silicon. Due to the inherent difficulty involved with lasing in silicon, promising hybrid devices are also under investigation [28].

Guide Light: Waveguides are analogous to electrical wires and are used to transport data around the optical integrated circuit (OIC) for processing. Waveguides are well understood at near infrared wavelengths and numerous forms of filters, couplers and multiplexers allow light transport to be manipulated in a more sophisticated manner

and enable multiple data streams to be transported simultaneously. With many sophisticated devices being fabricated, it becomes inevitable that some of the devices will suffer errors or imperfections in fabrication, this is where the wafer scale testing (WST) is useful. The end goal would be to enable errors to be identified quickly without a prohibitively high cost to do. Once errors are identified they could be readily corrected using direct write techniques [12] or wafers could be removed from the processing run, saving money by preventing further unnecessary processing steps being performed on an already irreparably faulty wafer.

Modulation: One of the main drivers of silicon photonics is its potential to offer considerably faster data transfer than purely electronic systems offer. The speed per channel at which data is transported is largely down to the modulator technology available. Optical modulators add a data signal onto a beam of light ready for transport; the dominant measures of quality are the extinction ratio which is an indicator of how far the modulated signal can travel without amplification and the bandwidth which describes the maximum speed. Currently the silicon modulators in the literature achieve a data rates of around 50 Gbps to 60 Gbps [29, 30], though complex coding schemes can boost this data rate to values as high as 224 Gbps [31].

Photo Detection: Photo detection is of fundamental importance if silicon photonics is to become truly integrated. Silicon is inherently unable to detect infrared light as it is transparent at these wavelengths. However, this is an important property to enable guiding of light in silicon. Thus to produce a successful detector silicon will have to be doped or adjusted using another element. The current methods under investigation for integrated photo detection include, the integration of III-V devices onto silicon [32], ion implanted defect detectors [33] and germanium detectors [34]. Germanium based detectors demonstrate detection bandwidth of up to 49GHz [35] and responsivities of up to 1.16A/W [36] at $\lambda = 1.55\mu\text{m}$.

Low Cost Assembly: Silicon is a low cost raw material, and the vast majority of the cost associated with semiconductors is attributed to the processing, with each processing stage costing significant amounts of money. To enable low cost assembly the number of processing steps must be minimised, human interaction reduced and fabrication faults must be detected as close to the point of creation as possible, such

that they can be corrected using methods such as those described in 2009 by Howe et al [12] or removed from the fabrication line before further expensive processing is performed on waste devices. In modern semiconductor photonic devices a plethora of individual process steps are utilised for a single active device wafer. Early detection of errors is essential to reducing cost, if there is an error which cannot be rectified in the first processing step a very significant cost saving can be made by disposing of the wafer rather than continuing with processing the wafer. These errors could potentially be discovered by using Wafer Scale Testing (WST). The other aspect of low cost assembly would rely on finding a method of passive alignment, that is communications between the outside world and the OIC would have to be self-aligning, otherwise manual alignment would be necessary and this adds significant cost in both skilled man hours and additional hardware requirements. The most well-known passive alignment structure currently is the V-groove [37].

Intelligence: The final step to commercially available mainstream silicon photonics is intelligent control of all of the above building blocks, which will come with integration. An intelligent device in this context, is defined as a device which has a computing capability. The difference between silicon photonics being a set of individual working components and a set of components which work together is the key development to ensure future implementation of the technology platform [38].

2.2 Light propagation and modes

The propagation constant denoted by κ , defines the phase change per meter of a given ray of light and is given by equation 2.1.

$$\kappa = \frac{2\pi}{\lambda} \quad (2.1)$$

Where κ is the propagation constant, and λ is the wavelength within a material. The propagation constant is usually described in free space and given the notation k_0 ; this requires using the free space wavelength denoted by λ_0 . The relation between the propagation constant and the free space propagation constant is $\kappa = n\kappa_0$, where n is the refractive index of the medium and hence the free space propagation constant can be described by equation 2.2.

$$\kappa_0 = \frac{\kappa}{n} = \frac{2\pi}{\lambda n} = \frac{2\pi}{\lambda_0} \quad (2.2)$$

Considering the simple ray optics model for a waveguide the free space wavevector (κ_0) of the light ray in Figure 2.2 has a component in the direction of propagation (z) and a component perpendicular to the direction of propagation (y).

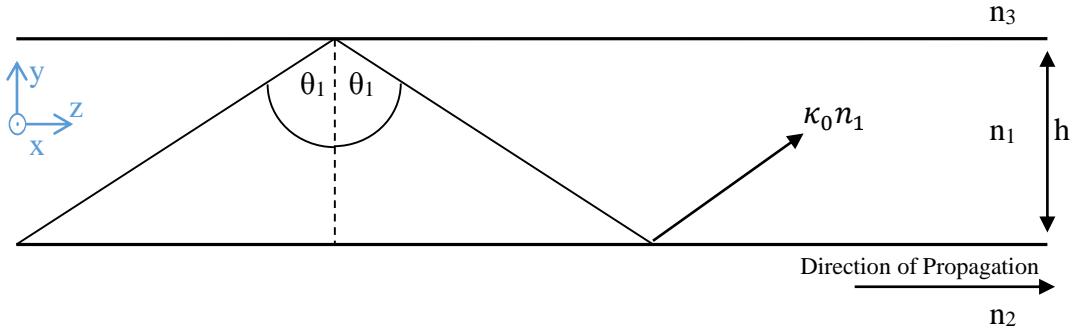


Figure 2.2 - Propagating light ray

Using trigonometry, where z is the direction of propagation and y is perpendicular to the direction of propagation. The z and y components of the wavevector κ can be described by equations 2.3 and 2.4 respectively.

$$\kappa_z = n_1 \kappa_0 \sin \theta_1 \quad (2.3)$$

$$\kappa_y = n_1 \kappa_0 \cos \theta_1 \quad (2.4)$$

Using the equation for κ_y it is possible to calculate the total phase change a propagating wave encounters by travelling a complete trip from the lower boundary to the upper boundary and back. If the phase change component is not a multiple of the free space wavelength of light λ_0 propagating along the waveguide, a phase shift will occur which causes destructive interference that will attenuate the travelling wave preventing it from successfully propagating along the waveguide .

Equation 2.5 describes the phase change incurred by travelling from one boundary to another.

$$\phi_h = \kappa_y h = \kappa_0 n_1 h \cos \theta_1 \quad (2.5)$$

The waveguide is crossed twice in a complete trip. There is also a recognised phase shift at each boundary known as the Goos-Hänchen shift [39] and hence the complete phase change in one complete trip across the waveguide is given by equation 2.6.

$$2\phi_h - \phi_u - \phi_l = 2h\kappa_y - \phi_u - \phi_l = 2\kappa_0 n_1 h \cos \theta_1 - \phi_u - \phi_l = 2m\pi \quad (2.6)$$

Where κ_0 is the free space propagation constant, n_1 is the refractive index of the guided layer, h is the waveguides height, ϕ_u and ϕ_l is the upper and lower boundary phase changes respectively and θ is the travelling waves angle of incidence with a waveguide boundary. To allow propagation without destructive interference m must be an integer such that the total phase change is equal to a multiple of the free space wavelength and thus this equation defines all of the supported modes in the given waveguide. In integrated photonics it is generally the case that the waveguide is designed to allow only the fundamental mode ($m=0$) to propagate, this eliminates the limitations introduced by intermodal dispersion.

2.3 Coupling to the optical integrated circuit

In order to confine light it must be placed into a waveguide as discussed previously, however passing light into a waveguide is a non-trivial task. The difficulty in coupling light into an integrated optical circuit comes with the size mismatch between the integrated waveguides which are typically 220nm – 400nm in height to the optical fibre which is typically 10 μ m in diameter. There are several methods of passing light into a waveguide of which the most common 4 are discussed here.

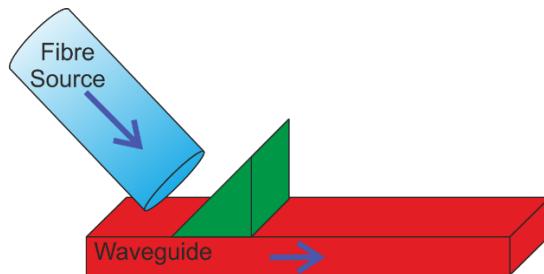


Figure 2.3 - Prism waveguide coupler [40]

Prism coupling shown in Figure 2.3 is not very useful for coupling into silicon due to the condition which requires the prism to be of a greater refractive index than the waveguide in order to achieve a phase match between input and waveguide modes. In the case of silicon the refractive index is 3.48 and very few practical materials have a higher refractive index than this. The other 3 methods to be discussed are far more useful for silicon.

Butt coupling and end-fire coupling are in essence the same. A fairly intuitive method of coupling to the waveguide by simply shining accurately positioned light into the

end of the waveguide. The difference is that butt coupling, shown in Figure 2.4 directly attaches the source such as an optical fibre to the waveguide. Given the small size this is very difficult to perfect and potentially may not be capable of exciting every mode in the waveguide; it is possible to buy fibres for this purpose which have a lens moulded onto the tip to improve coupling efficiency. End-fire coupling shown in Figure 2.5 is the same as butt-coupling however a lens is inserted between the fibre and integrated optical waveguide; this causes the light to be focussed which enables more precise coupling to the waveguide and potentially enables all modes to be excited in the waveguide.

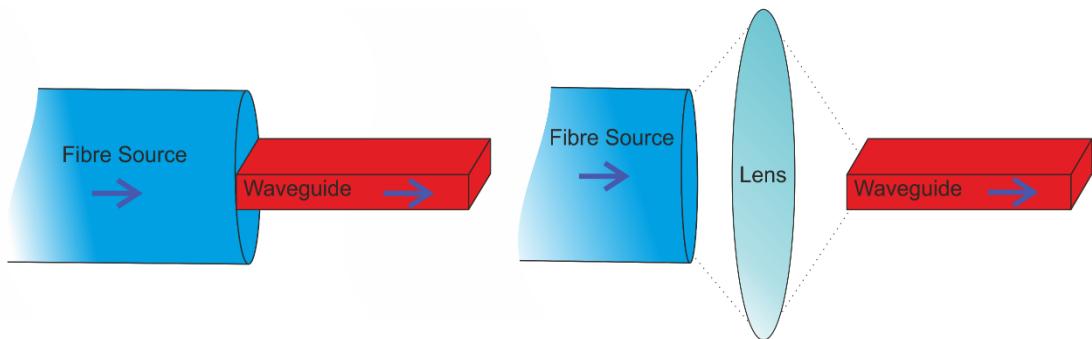


Figure 2.4 - Butt waveguide coupling

Figure 2.5 - End-fire coupling

In cases of butt coupling or end fire coupling, a taper is utilised to increase the cross sectional area of the waveguide facet which in turn increases the coupling efficiency. A taper is a simple V shape which has a large facet for the input which then gradually decreases in size until reaching the dimensions of the waveguide to be used. The taper would ideally exist in both the X and the Y directions to maximise the coupled light; however in reality tapering the Y axis is very difficult and leads to a graduated line which does not confine light very well and surface roughness increases losses significantly. Thus an X axis taper is utilised commonly and alternative methods of effectively tapering the Y axis are utilised when required.

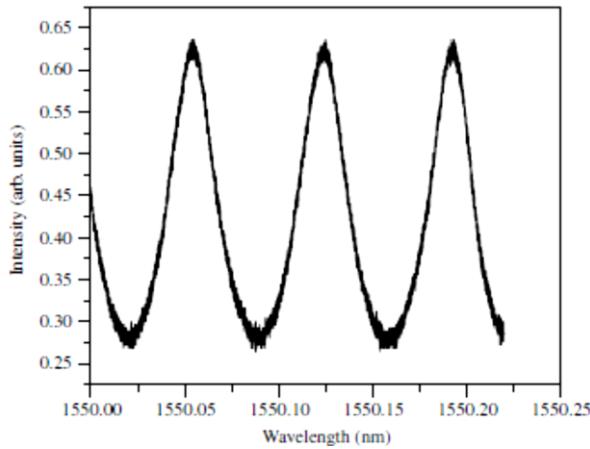


Figure 2.6 - Fabry Perot Resonance in a single mode waveguide [40]

When coupling light and taking measurements it is important to also be aware of Fabry Perot resonant cavities which can impact results. Fabry-Perot resonant cavities are synonymous with laser cavities and are caused by partial reflections at interfaces between dissimilar refractive indices. At an air to silicon interface a 31% reflection of infrared light can be expected, thus any small gaps or even the silicon waveguide itself can effectively become a Fabry Perot cavity if not carefully designed and manufactured. The Fabry Perot cavity causes a wavelength dependant output due to the reflected waves adding to the transmission with a different phase relationship. The expected output due to a Fabry Perot cavity being present is shown in Figure 2.6. Coating waveguides facets with anti-reflection coatings can reduce the reflection from 31% to below 1%; this will reduce the possibility of producing an undesirable Fabry Perot effect within the test setup giving more reliable results.

Further to the coupling methods described here, gratings can also be utilised for coupling. The theory of grating couplers is covered in detail in the next section.

2.4 Gratings

Gratings are formed using a periodic change in refractive index along a waveguide. The grating period is the dominant factor influencing how the structure interacts with the electromagnetic waves which pass through them. Two periodic structures are relevant for discussion in this thesis, which are the Bragg grating and the diffractive grating coupler.

2.4.1 Bragg Grating

A Bragg grating is used as a spectral filter and is based on a principle known as Bragg reflection.

Bragg gratings are periodic structures with a refractive index change introduced to alter the effective index of the material. The grating period to reflect a specific wavelength is calculated using the phase matching condition given in equation 2.7 [41].

$$\Lambda = \frac{m\lambda_{Bragg}}{2n_{eff}} \quad (2.7)$$

Where Λ is the grating period, m is the order of the grating, λ_{Bragg} is the free space wavelength to be reflected and n_{eff} is the effective index of the waveguide mode. The performance metrics of a Bragg grating are coupling efficiency, extinction ratio, frequency response or bandwidth.

If a broadband light source is passed into the Bragg grating device, a select wavelength will be reflected back toward the input light source whilst allowing the remaining wavelengths to be transmitted through the device unimpeded as illustrated in Figure 2.7.

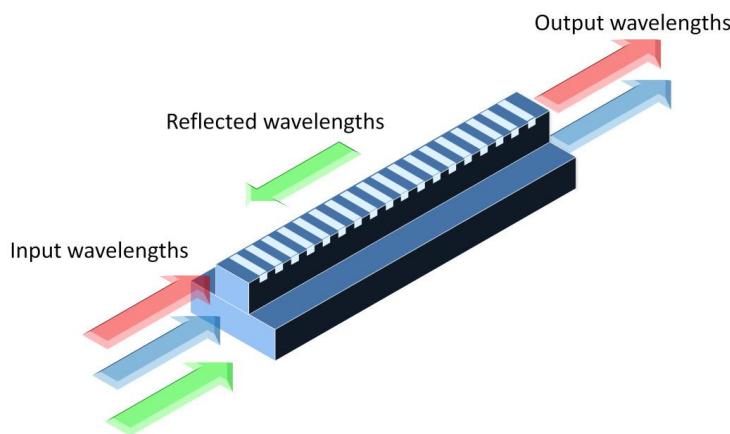


Figure 2.7 - Bragg grating concept illustration [42]

This style of device can be made in a number of ways; typically the surface of a waveguide is etched periodically, though other solutions include limiting the refractive index modulation to the cladding [43], or etching a rectangular profile in the sides of the rib as opposed to the top [44]. Both of the latter methods allow a Bragg grating and

rib waveguide to be fabricated using a single stage etch making fabrication cheaper and simpler at some cost to performance. An alternative method exists in using ion implantation [18, 19, 45, 46]. This approach allows erasability characteristics as are demonstrated in this body of work.

2.4.2 *Grating Couplers*

A grating waveguide coupler as shown in Figure 2.8 is a very useful coupling method allowing coupling of a single optical mode for analysis.

A grating coupler allows the fibre an extra degree of freedom in alignment when compared with end-fire coupling. Not only must it be directed at the correct position on the waveguide but it must also be tilted at the correct angle to the waveguide. If the angle is not set correctly the coupling efficiency may be reduced or in the worst case light may fail to propagate. A grating coupler may prove useful in wafer scale testing as it removes the need for cleaving and facet polishing of samples before testing, reducing sample preparation time and also allowing further processing after a measurement has been taken. Gratings do have some weaknesses compared with end-fire and butt coupling. Gratings operate over a limited wavelength range and typically have a 1 dB bandwidth of around 40nm [47-51], though with more complex designs ~50-60nm has been demonstrated [52, 53]. Gratings also require very precise fabrication compared with other methods, with a 1nm error in fabrication giving approximately 1nm error in operational wavelength.

Figure 2.8 shows the detailed structure of a grating coupler for coupling between the mode of an optical fibre and the propagating mode in the waveguide; this is achieved by modulating the effective index periodically by a period Λ . This can be achieved using an etch to alter the effective index, in this case the region labelled F. h is the grating height, θ_i is the angle of an input beam in the case of an input coupler and θ_o is the angle of a collecting fibre in the case of an output coupler. Both angles are shown for reference with regard to β_m , where β_m is the propagation constant of the guided mode. For a given grating coupler design the angle is the same for the input beam and the collecting fibre hence $\theta_i = \theta_o$. The duty cycle, otherwise known as the filling factor, is given by the ratio of $\frac{h}{\Lambda}$ such as in [54] (see Figure 2.8). This is the most common definition in the literature, though some authors however, use the definition

$\frac{F}{\Lambda}$ such as in [55]. This discrepancy is easily overlooked as the filling factor of grating couplers is usually 0.5, in this specific case both definitions are identical.

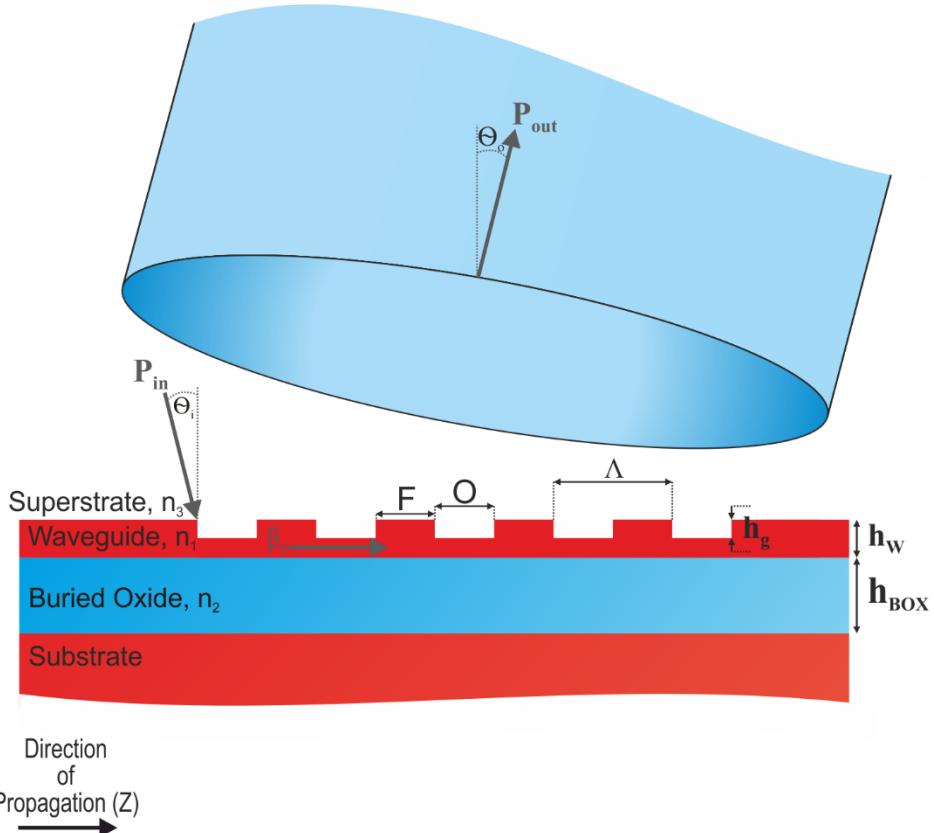


Figure 2.8 - Grating Coupler Structure

The operation of a grating coupler is based around a phenomenon called phase matching. At this point it is also imperative to note that grating couplers are reciprocal [56] such that if a grating is optimised for the input of a given wavelength it is also optimised for the output of the same given wavelength, thus designs and simulations need only be run in one direction, as input or output couplers. Phase matching between two waveguides, in this case matching the phase of the guided silicon waveguide mode to the guided optical fibre mode, ensures all interacting waves have the correct phase relationship at a desired position to allow constructive interference. For phase matching to be achieved the phase velocity, and in this case the propagation constant in the z direction of both of the waves must be identical in both the confined waveguide mode and the superstrate mode intended to couple into the fibre. For successful coupling to occur between a planar waveguide, and the superstrate mode the phase matching condition must be met, this means $\kappa_z = \beta_m$ must be true, where κ_z is the

propagation constant of the required in the superstrate and β_m is the propagation constant of the waveguide mode.

$$\beta_m = \kappa_0 n_3 \sin \theta_i \quad (2.8)$$

The condition shown in equation 2.8 cannot be met in a standard silicon waveguide, to demonstrate this, the effective index must be considered. The effective index corresponds to the equivalent refractive index a wave would experience if it travelled directly along a waveguide instead of following a typical total internal refractive index pattern.

The effective index n_{eff} can be defined by equation 2.9.

$$n_1 \sin \theta_1 = n_{eff} \quad (2.9)$$

Substituting this into equation 2.3, whilst also noting the relationship to β_m gives equation 2.10, which describes the propagation constant of the guided mode.

$$\beta_m = \kappa_z = n_1 \kappa_0 \sin \theta_1 = n_{eff} \kappa_0 \quad (2.10)$$

β_m has an upper and lower limit, defined by the angle of θ_1 . Outside of these limits light will escape the waveguide and hence the mode will not be confined. Clearly the largest angle that can occur is $\theta_1 = 90^\circ$ for a wave propagating directly down the waveguide, the lower limit of the propagation angle θ_1 is defined by the critical angle for the waveguide boundary with the lowest refractive index contrast between the waveguide core and cladding. Using Snell's law and assuming n_3 has the lowest refractive index contrast shows the lower limit of the propagation constant can be given by equation 2.11.

$$n_1 \kappa_0 \sin(\sin^{-1}(\frac{n_3}{n_1})) = k_0 n_3 \quad (2.11)$$

Thus the range of values for β_m is given by equation 2.12.

$$\kappa_0 n_1 \geq \beta_m \geq \kappa_0 n_3 \quad (2.12)$$

The angle θ_i must be lower than 90° as otherwise the fibre mode would be parallel to the planar waveguide and not enter the silicon waveguide, thus $\sin \theta_i < 1$. The lowest value for β_m is $\kappa_0 n_3$ from equation 2.12, hence it is demonstrated that equation 2.8 cannot be true as for any practical value $\beta_m \neq \kappa_0 n_3 \sin \theta_a$, this is why a prism or

grating is required to achieve successful phase matching. As previously discussed the prism coupler is of little use in silicon photonics, so only the grating coupler is considered. Given that β_w is the propagation constant when the grating is not present and β_m is the propagation constant when the effective index is modified by the grating then the propagation constant of the guided mode in a grating is given by equation 2.13 [40].

$$\beta_m = \beta_w + \frac{2m\pi}{\Lambda} \quad (2.13)$$

Where m is the mode number of the wave travelling through the altered effective index part of the grating and can take any negative integer value, positive values will not result in a phase match unless the fibre angle is considered to be negative to give a field profile which radiates back toward the input. It is normally desirable to design a grating to only couple the fundamental diffraction order as this offers the greatest efficiency and also prevents multimode propagation thus let m = -1.

The phase matched condition can be obtained by substituting equation 2.13 into the original phase matching condition given in equation 2.8.

$$\beta_w - \frac{2\pi}{\Lambda} = \kappa_0 n_3 \sin\theta_0 \quad (2.14)$$

Writing β_w in terms of effective refractive index and substituting $\kappa_0 = \frac{2\pi}{\lambda_0}$ gives rise to a general equation for calculating the period of a grating coupler as shown in equation 2.15. This equation makes it is possible to calculate the optimal grating period for a given wavelength.

$$\Lambda = \frac{\lambda_0}{n_{eff} - n_3 \sin\theta_0} \quad (2.15)$$

It is also important to note that a grating coupler can be designed to couple a mode using $\theta_0 = 0^\circ$ to make alignment simpler, however this will give rise to a large second order reflection which will cause a significant loss in the system and is far from optimal unless the grating is modified to account for this using methods such as chirping.

When testing a grating coupler it is useful to reduce the number of refractive index changes which occur outside of the waveguide as each change will reduce the efficiency by reflection. Index matching fluid can be utilised to match the fibre index

to the cladding of the waveguide and thus reducing the power lost and improving performance.

The efficiency of a grating coupler is defined using one of two methods in the literature. The first method (e.g. [57]) is given in equation 2.16.

$$\eta_o = \frac{P_o}{P_o + P_s} \quad (2.16)$$

Where η_o is the output efficiency, P_o is the output power to the superstrate and P_s is the output power to the substrate. This method is not suitable for use in experiments on silicon photonic grating couplers as it is very difficult to measure power output to the substrate in these devices. This method is also more accurately described as the directionality, it assumes a perfect coupling device, which gives a higher efficiency than the second method shown in equation (2.17). This occurs because it ignores other losses such as reflections or light scattered away from the fibre.

The second method is more simply given by equation 2.17.

$$\eta_o = \frac{P_o}{P_w} \quad (2.17)$$

Where η_o is the output efficiency, P_o is the output power to the superstrate and P_w is the power in the waveguide which is incident upon the grating. This will produce a smaller value for efficiency but is a more realistic measure for the devices to be fabricated as it takes into account all losses of the grating.

2.5 Refractive index variation in silicon

2.5.1 Doping and Thermal Effects

At the communications wavelength of $1.55\mu\text{m}$, silicon has a refractive index of 3.48. The ability to alter the refractive index of Silicon is crucial to the design of a range of active devices such as modulators or optical switches. The refractive index (n) can be altered using a range of techniques, though Δn is typically very small compared with the refractive index of silicon. For instance, the thermo-optic effect in silicon is described by equation 2.18, as shown by Clark et al [58].

$$\frac{dn}{dT} = 1.86 \times 10^{-4}/K \quad (2.18)$$

Which means a 1°C temperature increase, results in a refractive index change of 1.86 x 10⁻⁴.

A similar magnitude refractive index change can be observed for carrier injection using the plasma dispersion effect, which is defined for the real part of refractive index [59] by equation 2.19.

$$\Delta n = \frac{-e^2 \lambda_0^2}{8\pi^2 c^2 \epsilon_0 n} \left(\frac{N_e}{m_{ce}^*} + \frac{N_h}{m_{ch}^*} \right) \quad (2.19)$$

Using empirical data measured at 1.55μm Soref and Bennett [60] confirmed the relationship for electrons but showed a $(\Delta N)^{0.8}$ dependency for holes. Giving rise to equation 2.20, which is a more accurate model.

$$\Delta n = -[8.8 \times 10^{-22} \Delta N_e + 8.5 \times 10^{-18} (\Delta N_h)^{0.8}] \quad (2.20)$$

Using a typical value of 5×10^{17} injected carriers, which can be ascertained for both electrons and holes [40] a refractive index change of -1.17×10^{-3} is achieved.

These methods of altering refractive index are very useful for modulators where a small refractive index change is acceptable. For the implementation of a wafer scale testing device however they do not offer a prominent enough refractive index change to form a strong grating and the large number of free carriers introduced to the structure may lead to a high insertion loss, hence reducing the performance of the final device. The loss introduced from implanted carriers is permanent and cannot be reversed.

2.5.2 *Ion implantation*

2.5.2.1 *Introduction*

Another approach to altering the refractive index of Silicon is lattice disorder, otherwise known as lattice damage. Silicon with a disordered lattice can either be deposited or introduced into silicon via ion implantation.

Ion implantation irradiates the surface of the sample with ions accelerated by a large electromagnetic field. Typically ion implantation in the microelectronics industry is used for doping by introducing elements from group III or group VI to alter the free carrier concentration. To introduce lattice disorder however, the implanted element is selected so as not to alter the charge present within the sample. Instead the energy from

implantation is used to disrupt the crystalline lattice. Work carried out by Baranova et. al quantified the change in refractive index in silicon due to a selection of implanted elements as shown in Figure 2.9 [61].

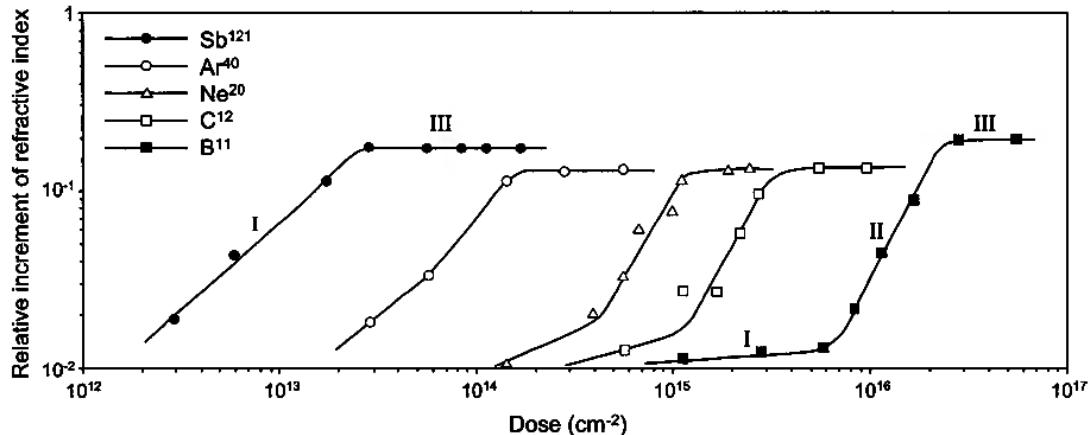


Figure 2.9 - Refractive index change in silicon introduced by a range of implanted elements [61]

For the elements tested, the difference between the maximum refractive index change in each case is shown to be very small, suggesting an independence from the implanted element. This evidence shows the refractive index change is not caused by the formation of an intricate compound but instead something inherent in the silicon. In ionically bonded crystals a refractive index increase is linked to an increase in density, but this is not the case when implanting ions into covalently bonded crystals such as silicon or germanium. A density reduction of 2% has been shown to increase the refractive index of silicon and germanium by 11% and 8% respectively [62-65]. The refractive index change is instead attributed to less stable features from broken bonds, a large enhancement in bond polarisability and an extended band edge absorption tail [66]. Collectively these changes are a direct result of alterations in the crystalline lattice, hence the refractive index change is due to lattice damage [61, 66-68].

It is clear from Figure 2.9 that elements with a larger mass require lower doses to achieve the refractive index change. This is because energy can be transferred from the accelerated ions to the sample matter in two different ways, electronic or nuclear stopping. Electronic stopping is an inelastic interaction which excites electrons in the target matter, the energy is subsequently dissipated as vibrations and ultimately heat. Electronic stopping is not suitable for lattice disorder formation. Nuclear stopping (recoil loss) can be described by kinematic theory, it is an elastic interaction in which

the accelerated ion impact the nuclei of the target matter. The nucleus is subsequently recoiled away from its lattice position, and if it receives sufficient recoil energy (i.e an average of 24 ± 2 eV for silicon [69], dependant on crystal orientation), it will be permanently displaced from the lattice site creating a point defect. A single displaced nucleus can create a cascade of further collisions called damage or collision cascades. Damage cascades are the main cause of damage production in semiconductors. Due largely to the cascaded nature of lattice damage, defects occur more frequently at the end of the implantation range.

Ion implantation may remove the need to etch grating couplers to change the effective index. Instead the effective index will be altered by creating a periodic amorphous silicon profile which has a significantly different refractive index from that of crystalline silicon. Implantation brings with it precise and repeatable depth control which is more difficult to obtain with a standard etching process especially on small features such as gratings.

2.5.2.2 *Lattice Damage*

Point defects in a crystal lattice can be more specifically characterised into three major types, lattice substitution, interstitial and vacancy point defects as illustrated in Figure 2.10. Vacancy defects are caused by an atom situated on the lattice being removed from the site and not subsequently being replaced. If the atom removed from the lattice is subsequently replaced by an implanted ion a substitutional defect is formed. Finally interstitials occur when an atom, implanted or native to the lattice, occupies non-conventional position within the lattice.

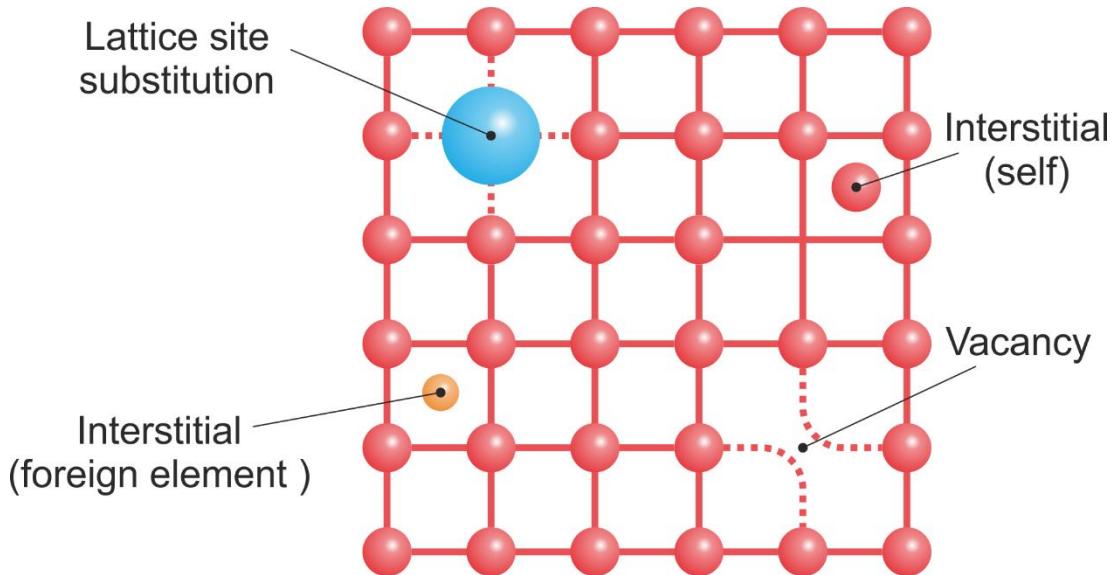


Figure 2.10 - Illustration of point defects which occur in Silicon

More complex defects exist than the point defects discussed here, though they are formed fundamentally of point defects. For instance in silicon Frenkel pair defects are often discussed in literature, which are simply a combination of the vacancy and self-interstitial point defects. Complex defects occur because at the instant that point defects are first created in the lattice, they are not in thermal equilibrium due to the statistical nature of electronic stopping. This in turn leads to a high probability of defect migration which leads to the formation of localised damage clusters [66] and with sufficient damage, extended defects and amorphisation [70]. The threshold level of lattice disorder required for amorphous silicon formation varies in the literature (e.g. [71-73]) with a more detailed explanation given in [74]. However, there is good agreement in the literature to suggest that when the threshold for amorphisation is calculated with a defect density model, that the crystalline – amorphous transition occurs with a critical point defect density of $1.15 \times 10^{22} \text{ cm}^{-3}$ [72, 75].

Typically lattice disorder is not desirable during implantation and so an element of low relative atomic mass (atomic weight) is utilised to maximise electronic stopping and minimise nuclear stopping. In order to develop substantial lattice damage with ion implantation, nuclear stopping must be dominant, and therefore this requires an element of higher relative atomic mass to be used.

Lattice disorder has previously demonstrated far greater refractive index changes in silicon than doping or thermal effects. A lattice disorder of 80% has demonstrated a refractive index change of ~ 0.5 on multiple occasions [18, 19, 42, 45, 46, 76, 77]. Figure 2.11 shows the change in the real and imaginary parts of the refractive index possible via lattice damage caused by ion implantation with Germanium.

For typical isotopes, the relative atomic mass of germanium is ~ 2.6 times that of silicon which suggests that nuclear stopping will be the dominant energy absorption mechanism in the implanted silicon.

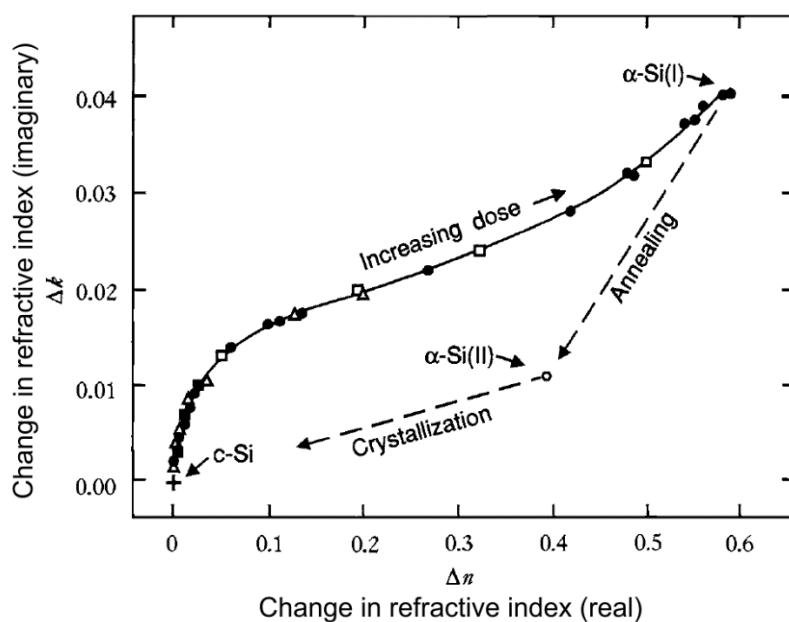


Figure 2.11 - Refractive index change in silicon due to amorphous damage [78]

At the maximum point in Figure 11, a significant change of 0.585 is present in the real part of the refractive index (Δn) which is substantial, especially when compared with the changes obtained from the thermo-optic or plasma dispersion effect. Only a small increase occurs in the material loss performance from the implantation process, inferred from the change in the complex part of the refractive index (Δk). The graph also shows that both Δn and Δk can be reversed. During annealing two stable states of amorphous silicon can be seen. It is expected that annealing from one state of amorphous silicon to another will give a wavelength shift in the response of the grating and offer a lower coupling strength. Furthermore annealing past this point will return

the silicon to a crystalline state as shown, thus offering the potential of removing the grating profile entirely.

Heidemann confirmed empirically that the refractive index change observed in damaged silicon closely followed the anticipated nuclear collision damage depth profile [68]. The results shown in Figure 2.12 also show that the refractive index of the region beyond the amorphised region drops off exponentially, offering a relatively sharp refractive index boundary for both real and complex parts.

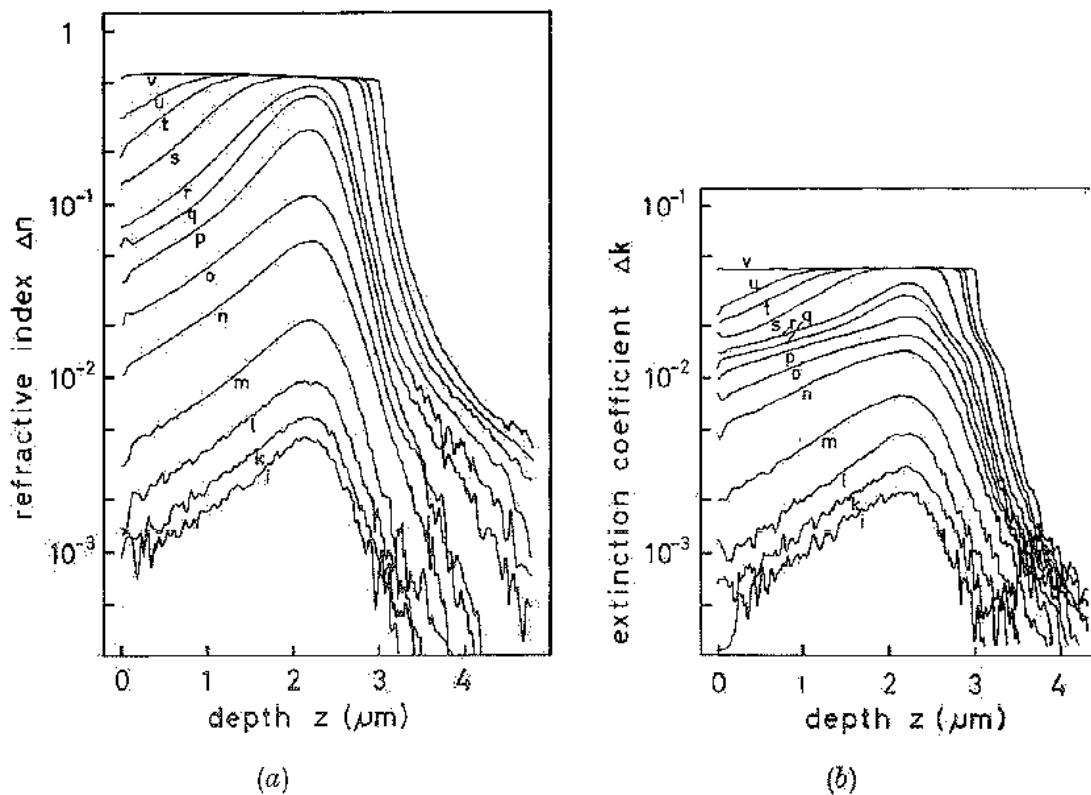


Figure 2.12 - Refractive index depth profile for Ge implants into Si at 4MeV with doses given in ions cm^{-2} (i) 1.8×10^{12} (k) 2.4×10^{12} (l) 3.7×10^{12} (m) 7.2×10^{12} (n) 2.0×10^{13} (o) 4.0×10^{13} (p) 6.1×10^{13} (q) 9×10^{13} (r) 1.1×10^{14} (s) 1.9×10^{14} (t) 2.8×10^{14} (u) 3.6×10^{14} and (v) 1.0×10^{16}

It is logical that amorphisation is not reliant purely on the dose condition to be used (ions per cm^2) but instead amorphisation occurs as a result of ions per cm^3 . The dominant factor in the implantation depth is the energy parameter. This prevents the dose conditions given in Figure 2.12 from being compared directly with the doses required for implanted grating couplers due to a an order of magnitude difference in implantation energies and hence amorphous layer depths. A guide translation can be established using the effective damage density as shown in equation 2.21 [79].

$$\frac{Dose \times Energy}{Implant\ Depth} = Effective\ Damage\ Density \quad (2.21)$$

The effective damage density for the curve plotted in Figure 2.12 as “u” is 4.5×10^{21} keV cm⁻³. This is the minimum level of effective damage density that provides a near constant layer of refractive index change.

Ion implantation is typically a temperature dependant process, for instance doses required to amorphise sapphire with cromium have been reported as 2×10^{17} ions cm⁻² and 2×10^{15} ions cm⁻² for room temperature and 77K respectively [66]. This demonstrates that low temperature implants reduce the required dose by two orders of magnitude and hence reduce the implant time. However, low temperature implant requirements increase the utilisation time of the ion implantation hardware significantly and hence increase the cost due to the time taken to reduce the sample temperature which must subsequently be raised to near room temperature before removal of the sample from the system. Silicon implants have often been performed at low temperature in the literature (for example 200K [68]) and hence most simulation software is most accurate at low temperatures, this would suggest that a similar temperature should be used in experimental work despite cost. However lattice disorder per ion in silicon has been shown to have only a very mild temperature dependency below 323K [80] allowing room temperature implants to be used to reduce cost whilst maintaining the advantages of accurate simulation and reference to prior literature.

2.5.2.3 Annealing

As shown previously in Figure 2.11, the lattice damage induced refractive index change in silicon can be reversed by annealing assuming the amorphous layer is still in contact with crystalline silicon seed. Amorphous silicon is recrystallized from the amorphous to crystalline interface, not from the nucleation of new crystals within the amorphous layer [81]. The regrowth rate of the interface has been shown to follow a standard Arrhenius equation of the form equation 2.22.

$$r = Ae^{\frac{-E_a}{k_b T}} \quad (2.22)$$

Where r is the rate of reaction, A is the pre-exponential factor, E_a is the activation energy, k_B is the Boltzmann constant and T is the temperature. The results have been confirmed by Raleigh Back Scattering[82] and TEM [83] with an activation energy E_a determined to be between 2.3 and 2.9eV [82, 83]. Appreciable rates of recrystallization for temperatures as low as 500°C have been demonstrated for amorphous silicon [84]. Another study has shown that a 110nm deep amorphous region was reduced to a depth of 40nm following 20minutes in an oven at 550°C, after a subsequent 20 minutes the amorphous region was decreased to almost zero, suggesting an annealing rate of $\sim 3.5\text{nm min}^{-1}$ at 550°C [42].

The high temperatures required for annealing, which is likely to be a back end process, presents an issue; if the anneal is global i.e. performed on the entire circuit, it is likely that active devices will be affected detrimentally. Hence, recrystallization by an oven based annealing process is only suitable for passive circuits. Laser annealing provides the ability to solve this critical issue. Laser annealing has been demonstrated to provide recrystallization faster than oven based annealing in similar devices [46], however in this specific case the annealing was demonstrated over a relatively large area of $3\times 3\text{mm}^2$. In the case of most optical integrated circuits $3\times 3\text{mm}^2$ may be considered a global anneal condition and does not solve the issue. This work will concentrate on a localised anneal, a $10\mu\text{m}$ spot size or smaller is required to enable erasability at a device level.

2.6 Simulation Methods Overview

2.6.1 *Grating couplers*

Gratings are notoriously time consuming to simulate though many approximations are available. Equation 2.15 gives a very good approximation of the grating period required for a given wavelength. It does not however include information on the required etch depth directly. Instead this is accounted for in the N (effective index) term. Perturbation theory can be utilised to obtain an approximation of grating efficiency based on the period and grating height relatively quickly, however this is still only an approximation and is only accurate for relatively long gratings [85]. A detailed description of perturbation analysis can be found here [56].

Grating structures are very sensitive to feature size. In order to arrive at an accurate grating design there are three rigorous methods of finding a solution which are eigenmode expansion, Finite Difference Time Domain (FDTD) and Finite Element Method (FEM). Eigenmode expansion yields good results and free tools are available such as Camfr, however an angled fibre is not straight forward to simulate as the design is split into discrete layers in the z-direction, thus angled fibres would be the result of a potentially coarse staircase approximation. The FDTD method of simulation is used in many commercial software packages such as Fullwave by Rsoft and FDTD Solutions by Lumerical, both of which are rigorous solvers. The FDTD method breaks the problem into small sections called a mesh, each small section of which is discrete in both time and space. Maxwell's equations are then used to solve each section resulting in a computationally complex and time consuming solver. However, this method gives accurate results for any given problem and the results are given in the time domain. The last method to consider is FEM, which also breaks the problem into small sections. After breaking the problem down it attempts to eliminate differential equations as completely as is possible for steady state problems or alternatively completing the partial differential equations to enable them to be successfully converted to ordinary differential equations which are then easier to solve. Solutions from FEM are based in the frequency domain.

Essential information to reduce the computational complexity when simulating grating couplers is that grating couplers are reciprocal [56], thus both the input and output coupler can be optimised with a single series of simulations. Also if a waveguide is sufficiently wide compared to its height the effective index of the waveguide in 2D will be very similar to the 3D waveguide, allowing the use of a 2D simulation to replace the more time consuming 3D simulation[47].

2.6.2 Ion implantation

Typically there are two methods for simulating ion implantation into solids which are the analytical approach and the Monte Carlo methods. Initially an analytical method was used due to its speed; the software package used for this was Suspre. These software packages use a statistical approach and require relatively little CPU time yielding a fast result. This method is useful to obtain an indication of the depth profile

of the implantation to be performed but it does not offer the precession of Monte Carlo simulations which is required in this work. Once preliminary conditions had been established with Suspree, KING and KING 3D were used to implement Monte Carlo simulations. King 3D is the method of choice as it is able to simulate a complete damage profile of ion implantation through a masked slit, with the width of the slit specified as well as the thickness of the mask accounted for.

2.7 Outcomes and Summary

This chapter has delivered a basic knowledge and understanding of the field of silicon photonics, how silicon photonics can be used to overcome the electrical bandwidth bottle neck for modern technology needs, and how wafer scale testing aligns itself with the needs of industry, in improving wafer yield and reducing device cost.

An overview of the potential coupling method candidates has shown the options for accessing intermediate points on a waveguide to be limited, with grating couplers the only method which is possible to fabricate in a cost effective manner, which also allows coupling without dicing the wafer or polishing waveguide facets.

The theory behind grating coupler operation has been explained by deriving the phase matching condition building upon the basic waveguide theory which has also been covered. Temperature, carrier injection and lattice damage have been discussed as key methods for refractive index engineering to avoid the irreversible process of material removal, with the semi-permanent refractive index change induced by lattice disorder showing the largest change and offering the most promise for wafer scale testing devices. Finally simulation methods are briefly discussed.

Chapter 3 - Literature Review

Silicon photonics is a very current topic with universities as well as several large companies currently carrying out research in the field including IBM, Oracle and Intel [86]. Conventional photonic devices are typically fabricated using exotic materials such as gallium arsenide, indium phosphide and lithium niobate. These materials are not ideal as they can be expensive to manufacture and cannot be easily integrated with electronic devices. Silicon however is abundant and cheap with several methods of processing already available. Silicon processing is also well characterised due to its extensive history in integrated electronics. This makes silicon a much more desirable material to use for implementation of photonic circuits; silicon also potentially enables monolithic integration of electronics and photonics.

One of the current issues in electronics is data transfer into and out of computer processors and memory. Silicon photonics is a very convenient way to increase the data bus speed into and out of a processor as silicon can be a foundation for electronics or optics so no change is required in the manufacturing of the processor core. However, an additional input and output stage would be required to convert the signals to and from light. The limitation of getting data into and out of processors was noted as early as 1997 by A. V. Krishnamoorthy, et al [87] with a publication titled “CMOS Static RAM Chip with High-Speed Optical Read and Write”. This showed a need for electro-optical modulation at a time when processors were boasting a single 450MHz core, as even then data could not be retrieved from RAM fast enough for optimal processing. At the time of writing processors for the consumer market have moved on significantly, clock speeds up to 4GHz and up to 8 cores can be integrated on a single chip highlighting a significant need to make the transition to optical interconnects.

3.1 Coupling Methods

It is important to observe the different types of coupling between optical fibres and silicon waveguides that are possible currently to ensure that there is not already an inherent solution to test integrated optical circuits during manufacture utilising other methods of coupling. This will also ensure that grating coupling is the most suitable type of coupling for implementing erasable test points. The most common methods of coupling are discussed earlier in section 2.3.

The core of a typical single mode optical fibre for use at near infrared communications wavelengths is $10\mu\text{m}$ in diameter which is an order of magnitude larger than integrated on-chip waveguides. Due to this large mode mismatch coupling efficiency may be

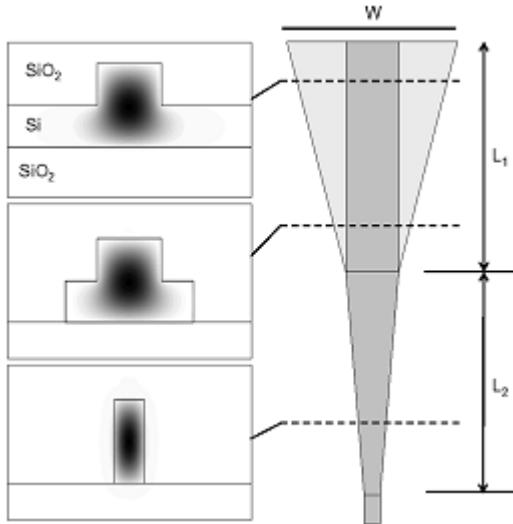


Figure 3.1 - Two Stage taper device [88]

expected to be relatively low. However Winn and Harris suggested an interesting horn shaped structure to increase efficiency in 1975 [89]. This structure has become widely known as a waveguide taper, and they also suggest that when coupling efficiencies of over 90% are required the taper must be in the order of 2000 wavelengths long. Robert and Jay demonstrated their horn shaped structure to combine different widths of integrated

waveguide and in 1991 Y.S Shani et al showed taper devices could be made adiabatic[90]. This means that no mode conversion occurs within the device. Furthermore, in recent years two stage tapers have been used to reduce device length [88, 91] as illustrated in Figure 3.1. This is because the taper flare angle is more critical at the smallest extreme of the device. Less than 0.2dB of loss can be observed in simulations with a $20\mu\text{m}$ long two stage taper converting from $25\mu\text{m}$ to $0.8\mu\text{m}$, experimentally the loss increased to 0.4 dB . Each stage was $10\mu\text{m}$ long, initially reducing the width from $25\mu\text{m}$ to $2\mu\text{m}$ and then from $2\mu\text{m}$ to $0.8\mu\text{m}$ [88]. To achieve similar results with a single taper Winn and Harris suggested a device must be $2000 \times 1.5\mu\text{m}$ long, showing the significant improvement demonstrated by the two stage taper. The use of tapers can be extended beyond waveguide dimensional changes on chip, to coupling from optical fibres or lenses. In 2005 Choudhury et al characterised the losses incurred from end fire coupling. The results showed coupling between a high numerical aperture optical fibre, with a mode field diameter of $3.7\mu\text{m}$, and an integrated rib waveguide with a width of $0.75\mu\text{m}$ and a height of $1.5\mu\text{m}$, resulting in a loss of 8dB . Adding a $250\mu\text{m}$ 1D taper with a starting width of $4\mu\text{m}$, reduced this figure to between 4 and 5 dB . Further modifying this taper to add a $3\mu\text{m}$ starting height

to create a 2D taper reduced this further to 2dB [92]. These results highlight the significance of tapers in reducing coupling loss.

Another loss to be factored into endfire and butt coupling methods is that at the facet of a waveguide there is a silicon to air interface which for infrared wavelengths gives a reflected power of around 31% [40], though anti-reflection coatings can be used to significantly reduce this value.

Many advances have been made in the core technology of end-fire and butt coupling and they both can be made relatively efficient but they are very limited by their nature when considering making test points on an optical circuit. End-fire and butt coupling can only be placed at the optical integrated circuit edge, which means a section of waveguide would have to be physically cut with high precision without introducing excess roughness to envisage a practical erasable wafer scale testing method and the number of test points would be severely limited. This is not practical and hence unsurprisingly no erasable or removable methods can be found in any material using end-fire or butt coupling.

Prism coupling in allows light to be coupled at any point on a waveguide and can in principle be made very efficient with Yong-Le [93] showing efficiencies of 75% in 2002. However prism coupling requires the prism to be made from a material with a higher refractive index than the waveguide [40] making this method impractical in silicon due to its high refractive index. Searches revealed no form of erasable or removable prism coupler in any material platform. It appears that prism coupling has a very limited use with waveguides of any material with very few papers utilising the technology compared to other coupling methods. This could be due at least in part to the more complex and expensive processing required to add a prism of different material for prism coupling compared to the relative ease of fabricating a grating coupler which results in similar efficiencies [94].

3.2 Grating Couplers

Grating couplers were first realised by Dakss et al in 1970. The investigation showed coupling efficiencies of the order of 40% using a substrate of corning 8390 dense flint glass film and a guiding medium of Corning 8390 with a refractive index of 1.73. The

grating in this case was formed from photoresist [95]. This initial study showed good efficiency making grating coupling a viable alternative to butt coupling for photonic devices. Grating couplers have the advantage of being relatively simple to fabricate and can be placed anywhere on a chip to couple light, overcoming the problem with butt coupling. In practice they are also typically easier to align.

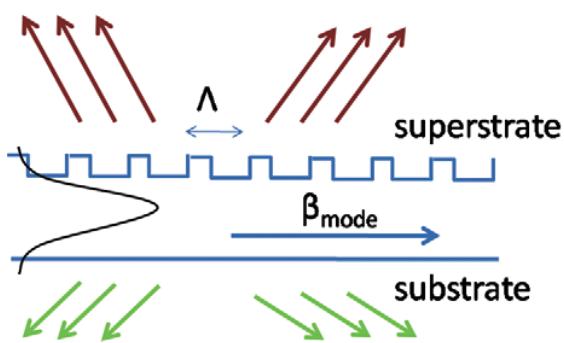


Figure 3.2- Grating coupler showing all leaky modes [96]

Tamir and Bertoni moved on in a theoretical paper published in 1971 to show that light could be coupled out from the waveguide into the superstrate in a leaky mode either in the direction of the propagating light or alternatively it could be coupled to the superstrate back in a direction opposing the direction of propagation based on the grating period selected

[97]. This showed that grating couplers are more versatile than first expected. Figure 3.2 shows the direction of the leaky modes which can be made available by appropriate design.

Ulrich also published a theoretical paper which discussed the maximum efficiency of a grating coupler [94]; the findings were that 80% efficiency was obtainable assuming that the guided mode only interacted with one free wave. Stone and Austin followed this up in 1976 with a theoretical and experimental study of loss on grating couplers [98] which suggested that the largest factor in guided wave attenuation within the devices fabricated was actually caused by residual photo resist (Shipley AZ 1350B) rather than the imperfect grating teeth shape [99]. It is quoted that the residual resist on the grating coupler devices discussed can cause significant performance reductions. This is due to two factors, the Δn value between filled and etched regions of the grating is reduced, though perhaps more significantly the resist increases surface reflections.

Finally in 1977 Tamir et al produced a paper on generalised design of dielectric grating couplers [56]. The paper used perturbation theory and network based analysis to greatly simplify the design procedure. Though the results were not an optimised design, the calculations allow a relatively quick design process and good output efficiency.

Grating couplers have been implemented in various material platforms and use various

configurations as shown in [101-106]. This demonstrates that gratings are well known photonic structures which are both functional and useful in many material systems such as LiNbO₃, InGaAsP and InP.

In 1991 Emmons et al began considering uniform grating couplers in silicon

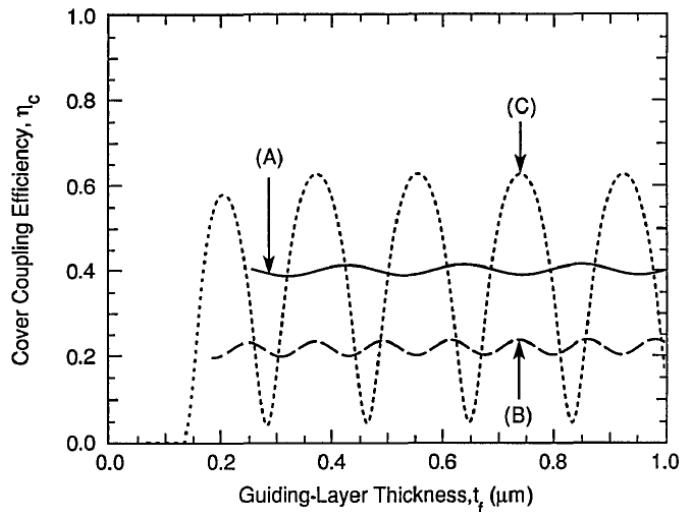


Figure 3.3 - Superstrate Coupling efficiency for a) Glass b) GaAs c) SOI [100]

based photonics theoretically [100]. This paper also considers a glass based waveguide and a GaAs based waveguide, and the results of coupling efficiency against waveguide height are shown in Figure 3.3 for comparison. It is clear that SOI is found to be significantly more sensitive to waveguide height than the other material structures considered. The author attributes the increased sensitivity to the larger interface reflections, which are caused by a greater refractive index contrast in the SOI platform. It is also apparent from Figure 3.3 that the interface reflections can be utilised constructively to achieve higher coupling efficiencies in SOI compared with the other material platforms if designed correctly. With SOI reaching efficiencies above 60%, compared with around 40% for glass and around 25% for GaAs. Conveniently the optimal guiding layer thickness for SOI falls very close to the two common heights of 220nm and 400nm that SOI is produced in. Following the initial theoretical predictions of Emmons et al in 1991, Emmons went on to publish 2 further papers in 1992 [107,

108]. The results from [107] show in detail a comparison between modes supported and waveguide thickness. It is deduced that SOI can support low loss leaky modes and allow substrate losses of below 1dB/cm as well as showing improved mode discrimination when compared with silicon on sapphire geometries. Emmons et al [108] went on to demonstrate that in waveguide geometries with high index contrasts such as silicon on insulator, both coupling efficiency and required coupling length is highly dependent on accurate design with sensitivity to variations in grating period and layer thicknesses especially. They followed up their earlier predictions of maximum efficiency of 60% to be more specific. In excess of 60% efficiency is achievable in uncoated gratings yet with an additional buffer layer of silicon nitride applied to the surface of the grating it is claimed that efficiencies of 90% are achievable though this has not yet been demonstrated in practice and requires grating lengths in excess of 100 μ m. They also include an analysis of substrate coupling and suggest that over 95% is achievable in uncoated systems though this is not particularly useful as the objective is to minimise light into the substrate to maximise light into the Superstrate though it does perhaps suggest a grating on the bottom of the waveguide may offer better efficiencies than the current topology.

All of the gratings analysed in SOI by Emmons et al utilised a sinusoidal profile, fabrication of which would be achieved by holographic interference patterning and reactive ion etching. This method would have been used for many of the previous papers discussed however it is limited in performance with regard to resolution; accuracy of positioning and most importantly it can be difficult to obtain deep and accurate gratings. Etched rectangular gratings are the typical topology seen in current designs for SOI grating couplers as demonstrated by Hagberg et al in 1995 [109]. This style is a more desirable profile as it is easier to fabricate at the same time as other devices due to the use of vertical side walls opposed to the curved profile of sinusoidal gratings. Vertical side walls can also be produced using photolithography or electron beam lithography accompanied by an inductively coupled plasma or reactive ion dry etch enabling higher resolution features with improved uniformity and hence yield. Hagberg et al [109] investigated surface gratings with an aim to achieve high efficiency surface emitting lasers. The rectangular gratings were defined in poly(methyl methacrylate) (PMMA) and achieved an efficiency of 63%. However in

the same publication Hagberg et al also investigate the effects of detuning the second order grating coupler from the laser wavelength to reduce reflection which is perhaps the most interesting result from this publication and the result is shown in Figure 3.4.

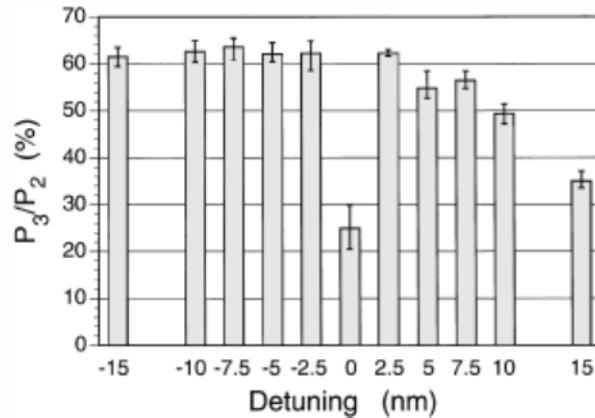


Figure 3.4 - Measured efficiency of detuned gratings, P_2 and P_3 represent transmission through the grating and outcoupled power respectively [109]

The results showed that for negative detuning output efficiencies are improved compared with those obtained for the calculated grating period. A small positive detuning of 2.5nm showed similar results however positive detuning beyond 2.5nm was found to reduce the overall coupling efficiency which is attributed to the introduction of a second order diffraction into the substrate. Detuning in this work is alternatively explained by the coupling angle from the relationship given earlier in equation 2.15. At a detuning of 0nm the coupling angle is 0° , this simultaneously excites a reflection through second order diffraction [109] explaining the finding of lower efficiency at that coupling angle, positive detuning is synonymous with a positive coupling angle and negative detuning a negative coupling angle. 4.5nm detuning is specified as a coupling angle change of 2.8° , though even detuning by half that amount in InGaAs/AlGaAs shows the second order diffraction has been removed with only a first order diffraction present with only two remaining radiated beams, one into the superstrate and the other into the substrate. This shows a small coupling angle is essential in removing the second order diffraction and achieving a high coupling efficiency. This is a similar outcome to the work performed by Hardy et al [110] who found the peak response did not occur at the calculated wavelength for vertical coupling. Similar devices presented by Mehuy [111] quote reflectivities simulated at 10^{-8} and in practice show reflectivity's of 3×10^{-5} , the difference between simulation

and empirical data being accounted for by considering the added etch step, though both figures show better than the 53% reflection quoted for the on resonance, vertical coupling devices.

Fabricating structures with accuracies near 2.5nm is very challenging. Second order gratings have been proposed to allow larger feature sizes and more tolerant fabrication however they offer a lower efficiency compared with a first order grating as can be seen in literature. Sun [112] analysed the differences between first and second order gratings for use as couplers and concluded that when the grating period of a coupler is doubled as is the case with a second order grating compared with its first order counterpart, the required coupling length L_c is increased by a factor of 16. The lower efficiency however is acceptable in certain cases for instance if the first order grating period would be too small to fabricate or when working with an application in which back reflection is critical such as a master oscillator power amplifier as it is also shown that second order gratings have a lower reflected power. Hagberg et al also found that grating efficiency is strongly dependant on the shape of the grating teeth which is in agreement with other literature [110, 113, 114].

Ang et al [115] demonstrated very high efficiency grating couplers using silicon on insulator reaching efficiencies of 70% which were accurately predicted by K C Chang's perturbation theory [116]. The highest experimental data point from the paper showed 70% efficiency which correlated with the relevant theory, though the theory also showed potential for efficiencies reaching 80%. This work comes as part of a PhD thesis [117]. The thesis covers different grating profiles in silicon on insulator in great depth. Superstrate coupling efficiencies achieved by Ang are 71% for a rectangular profile and 84% for blazed grating couplers, the blazed coupler was also a much shallower etch at a mere 80nm compared with the rectangular coupler at 140nm. This shows that very high efficiencies are possible with the rectangular profile and demonstrates that although blaze profiles are more difficult to fabricate they are capable of even greater efficiencies, due to the leakage factor being 1.75 times larger than that of rectangular gratings[118, 119]. Ang also used very large rib waveguides with a height of 1 μ m as well as very long coupling lengths, with the blazed grating having a length of 114 μ m and the rectangular grating having a length almost double

that. This is a problem as even the blazed grating is over 10 times larger than the mode of a single mode optical fibre which is typically the desired coupling target now.

Vivien et al [120] showed 55% coupling efficiency for a smaller device with a coupling length of 100 μ m and a width of 30 μ m but this still emits a mode larger than that of a single mode fibre. To date the most comprehensive simulations found to be published were from Kopp and Chelnokov, the simulations show a maximum of 53% efficiency to be achievable from a rectangular grating coupling to a fibre [121] which is in agreement with the simulations shown later in this thesis.

It is possible to improve on the efficiency offered by Kopp and Chelnokov results. One method was mentioned as early as 1990 by Parke et al [122], where a super lattice reflector was added to the substrate to improve the superstrate coupling efficiency in a grating array, with a similar result also achieved by Mehuys in 1991 [111]. Eriksson et al [123] went on to improve on Parke and Mehuys' modest numbers achieving a coupling efficiency of 94% in a 320 μ m long second order grating. This shows the significance of this technique as, although the grating is very long, it is also second order which should offer lower efficiency than a first order grating. Orobctchouk took a novel approach in 2000 [124]. In this case a silicon on insulator grating was fabricated and an aluminium top mirror was added, then coupling was achieved via the substrate layer, which proved to be effective measuring a 60% efficiency, though calculations showed up to 80% efficiency should be achievable in the structure. Though the top mirror approach showed good results, the bottom mirror still offers better performance. In 2006 Cheben et al showed results in silicon on insulator using a bottom mirror. The results showed greater than 90% efficiency with a coupling length of 80 μ m [52] again utilising a second order grating in the device. Cheben included simulation results for both before and after adding the grating mirror, showing the same coupler to offer a mere 30% without the sub wavelength grating mirror. In 2007 Van Laere used a similar principle to realise a 69% efficient grating coupler in silicon on insulator with a gold bottom reflector, devices were also fabricated without the bottom mirror which again showed a severely reduced efficiency of 26%, the bottom mirror was investigated with regard to the input coupler only in this paper. Unfortunately when considering wafer scale testing this approach

would not be possible as gold is not CMOS compatible. In 2009 similar results were demonstrated by Selvaraja et al [51] achieving the same measured 69% in a device length of $15.75\mu\text{m}$ using a bottom Bragg mirror constructed with amorphous silicon which is CMOS compatible, though the alterations to the buried oxide may affect other devices. This coupler offers very high efficiency and simulations show that 82% should be achievable for TE polarised light with devices of this structure. Further work into this style of device has demonstrated the best grating coupling performance available in SOI, Zaoui et al [125] demonstrated coupling loss results of only 0.62db (87% efficiency) per coupler empirically. The main problem with these styles of high efficiency devices lies in the very complex fabrication of the bottom mirrors, Zaoui overcame this issue by simply etching a window the silicon substrate to deposit the aluminium bottom mirror.

Another very important factor in grating couplers is the field profile of the optical mode. The field profile is important when considering coupling to a fibre as the mode profile adopts a Gaussian shape in the fibre whereas a uniform grating coupler output field profile is an exponential decay, with the first period of the grating extracting the most power, and a reduced power coupled out for each successive period. This mode mismatch reduces performance; this problem can be solved using a technique known as apodization. Apodization is the process of changing the shape of a mathematical function in this case changing the field profile of a grating coupler from an exponential decay to a Gaussian distribution. Taillaert et al provides an interesting publication on this [47], numerical optimisation is used to achieve a Gaussian field profile and a Bragg reflector is added to the substrate. The simulated results show for a $13\mu\text{m}$ device length, an efficiency of 61% is achievable in silicon on insulator without the Bragg mirror and up to 92% is achievable with the Bragg mirror. The etch profile is still rectangular and without the Bragg mirror the complexity of the fabrication process is no different to the device by Kopp et al [121] mentioned earlier, though the critical feature size would be lower in the apodized design. This shows that apodization is an improvement on earlier designs, although the gain in efficiency does cost a reduction in 1dB bandwidth down to 35nm from as high as 60nm published in some non apodized grating papers. Devices from Taillaert et al [48] showed an improved bandwidth of 40nm for the apodized coupler. Chen et al provided some of the most

recent apodized devices [54] claiming a coupling loss of only -1.2dB per coupler in the best devices corresponding to an efficiency of 75.9% with devices without a bottom mirror achieving a coupling performance better than -2dB (63.1%). Chen et al also noted that this method reduces back reflection into the waveguide which is highly desirable to reduce noise experienced by other integrated devices.

Other optimisations of grating couplers that are worth noting are the silicon overlayer gratings which improve efficiency by increasing the directionality of the output field shown by Roelkens et al [53]. Although only 55% efficiency was demonstrated empirically it is suggested that 80% efficiency should be attainable in such structures. Also of great interest are slanted grating couplers by Wang et al [126], though these are not fabricated in silicon on insulator and are potentially difficult to fabricate. Efficiencies of 80% are seen in a material structure with a very low refractive index contrast which is a fantastic achievement; if the devices were to be designed in a higher index contrast material platform the results may be even higher, though fabrication would be very challenging.

The efficiency of a grating coupler is a very important performance metric, though it is not the only way to improve a grating coupler. Alignment is important in all methods of coupling but as the tolerance is more relaxed for grating couplers compared to other methods of coupling it is rarely quoted. The coupling angle can still prove to be difficult to optimise on grating couplers. When considering mass production this can become an issue as alignment must be a simple process that can easily be achieved on a production line. Chirped gratings reduce the coupling alignment challenge by allowing the fibre to be positioned vertically without introducing the second order diffraction [109] discussed earlier, whilst also avoiding coupling power into forward and reverse travelling modes simultaneously. Taillaert et al [127] demonstrated the principle in GaAs on Oxidised Aluminium Arsenide (commonly abbreviated to AlOx) waveguides, with the demonstrated devices showing only 19% efficiency for vertical coupling without chirp though this was in line with the simulations which suggested a 20% efficiency for coupling to a vertical fibre. This decrease in efficiency may be acceptable in production for the increased ease of alignment, however adding a chirp improved these results substantially. Chirp is a term usually used to describe an

increase in frequency; in this case the vertical coupling efficiency is improved by the addition of a first order grating reflector which is added to the end of the structure. This gives rise to a physical structure with a decreasing grating period, and hence is described as a chirped grating. This modification saw the efficiency jump from 20% to 37% in simulations [127] and it was also predicted that this efficiency could be improved to 74% by adding a Bragg reflector to the substrate. More details of the structures design can be found in a slightly later paper from the same author [85]. This principle was replicated in silicon on insulator by Chen et al in 2008 [128] where it was shown that 34% efficiency was achievable using a chirped grating in SOI to aid in vertical coupling. This efficiency is significantly larger than without the chirp which showed only 20% efficiency for the same grating. This demonstrates chirping can add approximately 15% efficiency when considering vertical coupling. This method also reduces the back reflection which is a major concern when the fibre is introduced vertically with no offset angle. Chen et al measured a 5dB reduction in back reflections using the chirped grating compared with a uniform grating. Though the chirped gratings offer a lower efficiency than detuned uniform gratings, it may be an acceptable loss if it makes packaging considerably easier for mass production.

Silicon real estate is very expensive; this means miniaturisation of devices is essential to producing low cost optical integrated circuits. Couplers not only require a $10\mu\text{m}$ wide waveguide but also an adiabatic taper to reduce the waveguide to a width which only supports a single mode to reduce loss in the structure. This leads to device lengths of well over $100\mu\text{m}$ including the taper. For this reason reduced total device length is of great importance. To address this issue Laere et al formulated the focussing grating coupler in 2007 [49] based in silicon on insulator. The total device length was only $28\mu\text{m}$ which is up to eight times shorter than many similar devices; this was achieved by integrating the grating and the taper, the device achieved a respectable coupling efficiency of 30%.

In order to fabricate a silicon on insulator device using photolithography a mask is required. A mask is required for every different depth of etch or implantation step utilised within the design. Masks can be very expensive to produce and also create added complexity within the design due to alignment between masks amongst other

issues. A grating has been realised that utilises a single etch for both waveguide and grating definition. This allows a cost reduction by using only a single mask and single etch. The earliest example of this in silicon on insulator was reported by Chen and Tsang in 2009 achieving 34% efficiency for the TE mode [129]. This was followed up by Halir et al in 2011 with a similar device but for TM polarisation which achieved a slightly lower efficiency at 28% [130]. This device is shown in Figure 3.5. Unfortunately this type of structure which is etched completely through the silicon cannot be paralleled in erasable implanted gratings, as there will not be enough silicon below the implanted regions to recrystallize the amorphous damage created. Chiu and Huang [131] demonstrated a similar structure in 2010, without using a single etch. This device design was optimised for polarisation independent coupling, with efficiencies of 33% and 32% for TE and TM respectively. Polarisation independent coupling can be a “double edged sword”. In one respect it removes the need for concern of the polarisation output of a fibre, yet equally there is no awareness of the polarisation within the waveguide which can affect device design and performance of other devices.

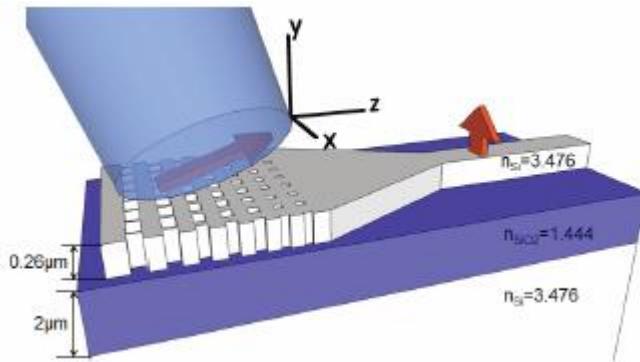


Figure 3.5 - Single etch grating coupler [130]

3.3 Wafer Scale Testing

Wafer scale testing approaches in the literature can be broken down into two distinctive categories. One approach is, as described earlier, to extract the optical signal from the waveguide and measure it directly. The other approach is to interrogate the waveguide and measure a metric which is proportional to the optical power propagating within the waveguide in order to infer data from the optical signal indirectly. In this section the merits of both options will be considered.

3.3.1 *Indirect optical measurements*

Near-field scanning optical microscopy (NSOM) is a non-invasive method, which is able to determine both the field amplitude and phase of light propagating in a waveguide [132]. In the context of wafer scale testing however, NSOM, though a powerful testing technique in its own right, is of limited use. NSOM offers a small field of view, along with limited probe lifetime [133], which combine to offer a fairly slow and expensive measurement technique for a full wafer.

Alternatively, perhaps the fastest and cheapest way to measure an optical circuit is electrically. In 2008 Baehr-Jones et al reported a responsivity of 36 mA W^{-1} in a contacted, unimplanted waveguide. A relatively low insertion loss of 0.2dB per test point was also documented [134]. Unfortunately they were unable to establish the mechanism that generated the photocurrent in the test point, which prevents accurate determination of the potential bandwidth of the device, though the device reported was limited to a bandwidth of only 60 MHz. A similar device was presented later in 2014 by Morichetti et al. This device focussed on measuring the impedance of the waveguide, removing the need to contact the waveguide directly and hence the insertion loss attributed to this device is negligible [135]. Although optimisations of these methods may yield speed increases beyond 60MHz, it is unlikely that the full speed of a several gigabit per second optical modulator could be accurately measured by either of these proposed methods. For this reason it becomes apparent that though electrical test points may form an integral part of a complete testing system, a method of monitoring the optical signal directly is a key aspect to testing high speed components such as modulators.

3.3.2 *Direct optical measurements*

For a direct measurement to be possible light must be extracted from the waveguide. Initially all gratings were constructed using an overlayer opposed to an etch, including the first grating coupler implemented by Daks et al [95]. However efficiencies were low and errors in fabrication could lead to high losses. Non-etched gratings are especially useful for wafer scale testing as they have the potential to be removed unlike their etched counterparts. Etched gratings which have material permanently removed pose an issue for wafer scale testing, it is desirable to remove the test point after it has

been measured to prevent permanent loss of light power from the waveguide and the resulting reductions in the performance of the final optical integrated circuit. Kurmer et al demonstrated an implanted grating coupler in 1983 [136] using a nitrogen based implant in both corning 7059 glass and LiNbO₃ the efficiencies demonstrated are 6% and 4% respectively with a device length of 5mm, compared with the 30% efficiency expected from the theory. The authors did not investigate the potential of these devices for wafer scale testing but were instead looking at alternate methods of fabrication. This demonstrates the feasibility of etchless, implanted grating couplers in other material structures, albeit for very long devices with weak performance.

Scheerlinck et al [14] demonstrated a grating coupler in 2007 without etching by using an over layer of metal. Simulation results are presented for silver, gold, aluminium and copper at 1.55μm with the best result coming from silver at 60% efficiency. The same author went on to fabricate a device with gold and demonstrated 34% efficiency which is in good agreement with their simulation results. Metal can be removed by selective etching in an appropriate acid such as acetic acid (CH₃COOH) which etches aluminium at approximately 7nm per minute without etching cladding layers at a significant rate; this allows removal of the metal grating leaving only the waveguide though this application is not mentioned by the author. This method of wafer scale testing would however only be a suitable method of wafer scale testing for passive devices as otherwise essential metal contacts would be removed when removing the test points, which limits its usefulness considerably. In 2008 Scheerlinck took this work further so show a novel approach to wafer scale testing [13]. The metal grating was moved from the optical integrated circuit to the fibre facet, enabling coupling at any point on the waveguide. This is a novel approach and achieved 15% coupling efficiency, and though this is not a particularly high efficiency, it may be enough for the application depending on the situation and also allows testing at any point on the optical circuit. The grating was fabricated using Nano imprint and transfer lithography. There are however severe limitations to this method of coupling. Firstly the waveguide could not be coated with a cladding for protection leaving fragile devices exposed during testing. The devices rely on the metal grating interacting with the evanescent field of the waveguide, because of this efficiency drops off sharply if the separation exceeds 200nm. This also means the fibre tip carrying the grating cannot be coated for

protection either, resulting inevitably in a residual trace of gold being left on the device under test. With a gold layer of only 20nm thick on the fibre tip, this would make the fibre probes deteriorate very quickly. Perhaps more importantly, gold is not CMOS compatible and is considered a serious contaminant thus following testing with this method a chip may not be able to have further processing completed in a CMOS fabrication facility.

Between 2007 and 2011 another novel solution was also developed by Panepucci and Zakariya et al. [15-17]. This method uses the principle of a directional coupling between two waveguides in close proximity. A flexible waveguide is placed on top of the waveguide with the coupling length controlled by the downward pressure applied to the probe. The most efficient iteration of their design showed simulated efficiencies of 95%, though in practice the highest efficiency demonstrated in this body of work was 4%. This large discrepancy is not explained in the publications, nor are simulations of alignment tolerance provided. However, based simply on the principle behind the directional coupling method used, and its sensitivity to alignment error it becomes apparent that alignment would be a very challenging feat. Coupling length, separation and skew errors would all be heavily detrimental to the empirical coupling performance. The proposed method may prove to be very powerful if these issues could be addressed in the future.

Bulk et al used a new approach for fabricating gratings using implantation; this can be applied to the field of wafer scale testing. Bragg gratings are well-known structures which operate as a wavelength selective mirror. Bulk et al demonstrated implanted Bragg gratings using silicon implanted into silicon and oxygen implanted into silicon though the goal was to maintain a planar surface for further processing rather than the objective considered here of wafer scale testing. The silicon implantation into silicon results [137] presented in 2007 show 5 and 2 dB extinction ratios for TE and TM respectively. The refractive index achieved in this work due to ion implantation was only 3.75, which is an increase of 0.25 from silicon's typical 3.5, this is due to incomplete amorphization. Much higher index changes should be achievable by lattice damage in silicon, based on results from several authors [18, 19, 61, 66, 68, 76] which would lead to devices of superior performance. A dose of 10^{15} ions cm^{-2} was used to create

the index change to 3.75, and this dose has been used to demonstrate an index change to 3.94 at room temperature with other implanted elements [42] though the lower relative atomic mass of oxygen is likely to have prevented complete amorphisation in this work. Bulk et al followed up in a paper in 2008 [138] which also demonstrated oxygen implanted gratings. Implantation by oxygen was expected to reduce the refractive index. The oxygen implanted gratings achieved a 10dB extinction ratio which improved on the silicon results and becomes a useable device but did not touch on the simulations that showed an extinction ratio in excess of 50dB. Again the problem appeared to be implantation. Room temperature implants were utilised but continuous regions of SiO_2 were not formed causing such a poor response. Also in 2008, Waugh demonstrated both oxygen implanted gratings and gratings fabricated using thermal oxidation, reported in his PhD Thesis [139]. Oxygen implanted gratings typically offered better results using attenuation and full width half maximum (FWHM) bandwidth as performance metrics. A 1000 μm long oxygen implanted grating showed a FWHM of 1nm and an attenuation of 16.8dB in the best case compared with 1nm and 3.7dB for the thermally oxidised case. These results are an improvement on previous implanted Bragg grating results.

Bragg gratings can be used for wafer scale testing if used in conjunction with an etched grating coupler. This wafer scale testing configuration was put forward by Loiaccono, an image clearly depicting this is found in his PhD thesis [42] and reproduced in Figure 3.6.

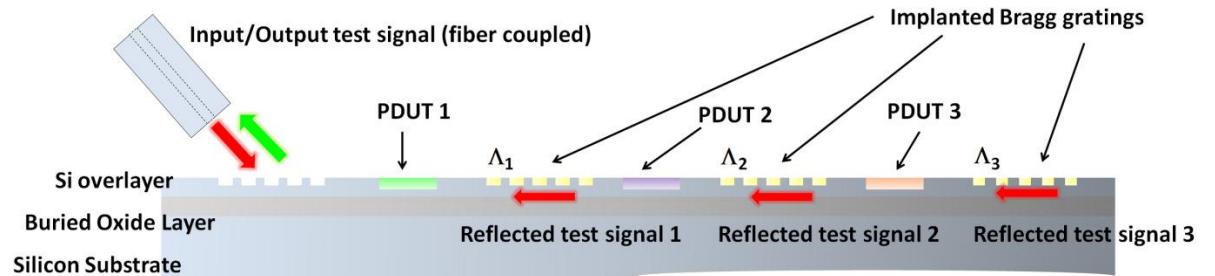


Figure 3.6 - Wafer Scale Testing Using Bragg Gratings[42]

Bragg grating reflectors reflect light back along a waveguide and data can be collected by connecting the input fibre to a detector via a circulator. The etched input/output coupler allows reflected light to be subsequently coupled into and out of the optical

integrated circuit. The Bragg gratings can then be positioned after the device to be tested by reflecting a specific test wavelength. Erasable Bragg reflectors have the potential to offer a useful wafer scale testing methodology for devices spanning a small wavelength range, with typical erasable Bragg reflectors offering up to a few nanometres wavelength reflectivity bandwidth, though wider channels could be interrogated using longer Bragg reflectors. The other disadvantage to monitoring a reflection is it may not depict the operation of devices which have asymmetrical transmission characteristics accurately, such as optical modulators. In 2010 Loiacono et al discussed Bragg gratings created using germanium implants using 90Kev implants with a dose of 10^{15} ions cm^{-2} [45]. A 30dB extinction ratio was achieved using a $2000\mu\text{m}$ grating. Furthermore the same author discussed the full wafer scale testing methodology [42]. Those results have been superseded by a paper describing a 15kev grating which, at $600\mu\text{m}$, achieves a 35dB extinction ratio, which is the best result for an implanted Bragg grating to date presented by the same author [140]. The devices were also shown to be erasable over an area of $3\times 3\text{mm}^2$ using a 248nm excimer laser.

3.4 Conclusion

The literature relevant to this work has been reviewed, and grating couplers have been highlighted as a powerful technology which have been successfully shown to achieve efficient coupling between an optical fibre and an integrated optical waveguide without the need to cleave the wafer. Spectral bandwidth is often not explicitly mentioned in papers but $\sim 40\text{nm}$ appears to be a typical 1dB bandwidth for a uniform grating [47-51], increasing to 60nm for more complex structures [52, 53].

Wafer scale testing is not mentioned in the literature in any great detail and it seems there is no commercially viable method for testing the transmission characteristics of an individual optical device. The implanted Bragg method is a useful wafer scale testing technique, however only a reflection is measured. In the absence of transmission based results, assumptions must be made of the device characteristics rather than exact, accurate measurements, giving rise to ambiguity. Metal grating faceted fibre probes offer the only wafer scale methodology with direct outcoupling with empirical results of 15% [13]. Implanted grating couplers may be able to remove

the ambiguity of implanted Bragg gratings and enhance the outcoupling efficiency of a single test point compared with other methods without introducing contaminates to the device under test.

Chapter 4 - Device Design

This chapter provides a detailed explanation of the design process associated with creating an optical test point based on an implanted grating coupler, for use in the silicon on insulator platform. A test structure has been devised which is able to ensure the test point is able to offer useful data during its operational mode and also allows verification of successful removal after testing. The single mode condition is established to ensure only a single mode is passed into the device which mimics the expected practical conditions. Tapers are designed to minimise any mode conversion losses and both implanted and etched grating couplers are designed. Finally the ion implantation conditions are designed to ensure sufficient amorphisation occurs, while minimising lateral straggling to minimise any duty cycle skewing effects.

4.1 Device Structure

Characterising an erasable grating coupler with only a single measurement at the grating output before and after it is annealed does not demonstrate erasability. Using only direct measurements of the implanted grating would require measuring an absence of light from the annealed grating coupler to demonstrate that the grating coupler was erased successfully. An absence of light from the annealed grating coupler could be caused by several factors other than a successful removal of the grating coupler. Other less desirable scenarios which lead to an absence of light at the output include, but are not limited to absorption or scattering due to laser ablation damage, failed positional alignment, debris on the fibre or grating coupler, or coupling the power to other leaky modes due to a refractive index variation or partial annealing.

To ensure that the experiment is performed with scientific validity, which demonstrates beyond doubt that the device does or does not work, the concept of a “bow tie” structure is introduced. The devised structure is shown in Figure 4.1, it allows the erasable grating to be characterised as a three port device. The additional grating coupler allows transmission through the implanted region to be measured, which accounts for waveguide damage or other issues which may prevent outcoupling after an attempt to erase the implanted grating coupler. More specifically the bow tie structure allows optical characterisation to be performed for both coupling into a conventional etched grating coupler and outcoupling through the implanted grating

coupler, as well as allowing characterisation of coupling from a conventional etched grating, through the implanted region and out through another etched coupler. A successfully erasable device will show both a substantial decrease in the optical power in the etched to amorphous grating profile and a subsequent increase in optical power in the etched to etched grating profile through the implanted region .

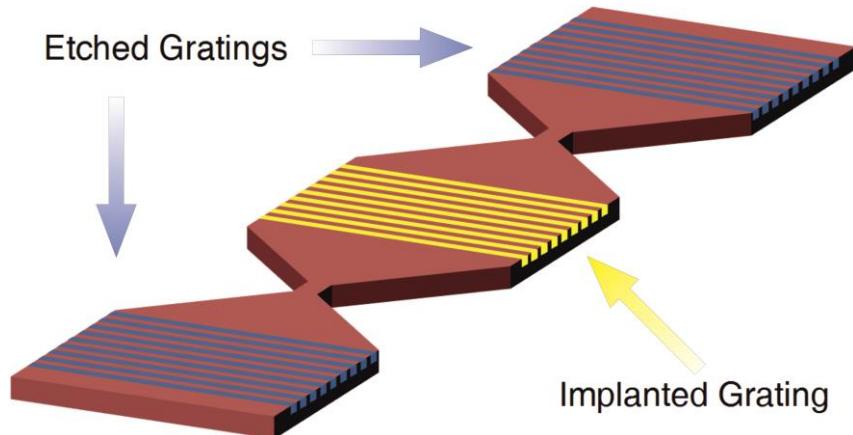


Figure 4.1 - Bow tie silicon waveguide structure (red) for characterising erasable gratings. Blue coupler regions represent surface relief gratings, the yellow grating region represents an erasable implanted coupler.

The bow tie structure can be represented by a series of standard components in a block diagram as shown in Figure 4.2. The device is symmetrical around the implanted coupler, the implanted coupler transmission can be measured by the etched couplers at either end of the device enabling accurate characterisation of the novel implanted coupler.

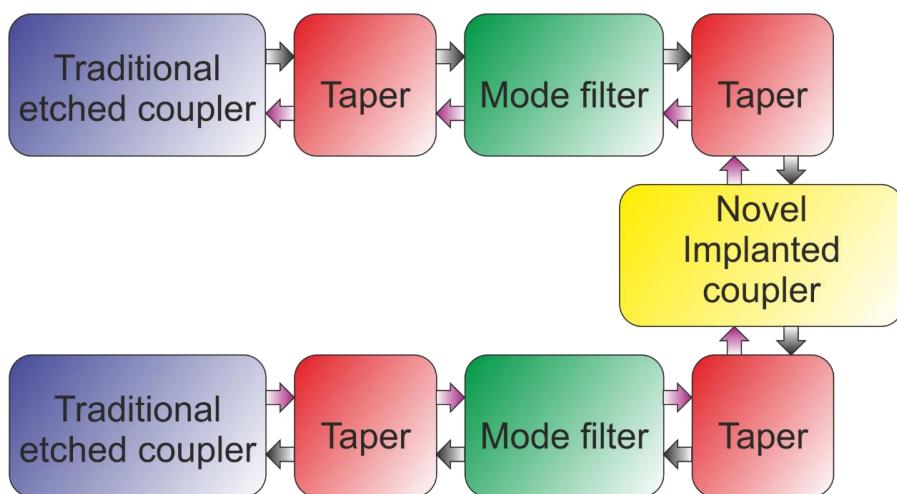


Figure 4.2- Block diagram of bow tie structure

4.2 Mode Filter Design

When dealing with wide planar waveguide structures such as those required for grating couplers, modal interference can become problematic if multiple modes are excited. Designing a waveguide such that it supports only a single mode enables light to be passed around the optical circuit solely in the fundamental mode, filtering out higher order modes thus removing modal interference to enable low loss transport. A simple equation to ensure single mode operation of silicon waveguides was originally proposed by Soref in 1991 [141] as shown below in Equation 4.1.

$$\frac{W}{H} \leq 0.3 + \frac{r}{\sqrt{1-r^2}} \quad \text{For } 0.5 \leq r \leq 1 \quad (4.1)$$

In which W and H are the width and height of the rib respectively and r is the ratio of the slab height to the rib height. This equation breaks down when r is smaller than 0.5. For the strip waveguides to be used in this work, this simple equation is invalid as $r=\infty$. Hence, a full simulation method is required to find the single mode conditions accurately.

To reduce fabrication costs, and ensure high quality material, the optical circuit design in the Silicon photonics platform is typically constrained by standard material topologies in which the silicon wave guiding layer has a height of either 220nm or 400nm. In this work a 220nm waveguiding layer will be used, with the slab completely removed in order to achieve a silicon strip waveguide configuration. Silicon strip waveguides offer very strong optical confinement, allowing for especially small bend radii and high integration densities [142].

Simulations were performed in the Rsoft BeamPROP [143] software package to determine the multimode boundary width for the 220nm silicon strip waveguide as shown in Figure 4.3. The light source must not be centred on the waveguide facet for this simulation, as this may prevent higher order modes being excited and hence deliver false results for the single mode conditions. The plot shows the effective index. When the effective index is around 1.4, it is clear that the optical mode is propagating in the buried oxide and not interacting with the silicon waveguide, and as the waveguide width becomes larger the effective index of the propagating mode increases

which shows that the mode is interacting with the silicon guiding layer. The simulations show that multiple transverse electric (TE) modes may begin to propagate in the silicon guiding layer for waveguide widths above 550nm. The grating coupler has been designed to couple only TE polarised modes, as grating couplers are polarisation dependant [47]. Furthermore the 220nm guiding layer will not support a low loss TM mode at a wavelength 1550nm [144], which has been verified using Rsoft BeamPROP simulations. These simulations were performed with a 400 μ m length mode filter.

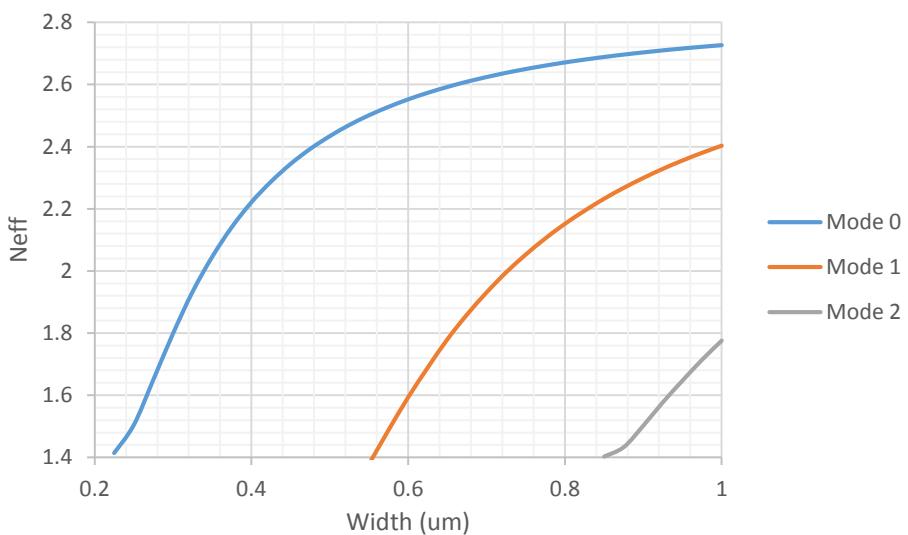


Figure 4.3 - Effective index of TE modes against waveguide width for a 220nm silicon wire waveguide

The tolerance of the fabrication facility must be accounted for when designing an optical circuit, a 550nm width waveguide would offer the lowest loss waveguide, however this risks multimode conditions arising if the fabrication is as little as 10nm outside of the design. Using a 400nm wide waveguide design offers resistance to fabrication errors without incurring an excessive amount of loss over waveguide lengths below 1mm. The loss attributed to a 220nm \times 400nm silicon waveguide in the literature using 248-nm deep UV lithography, the waveguide fabrication method to be used in this work, is 33.8 ± 1.7 dB cm $^{-1}$ [145]. These results are in close agreement with work from Bogaerts et al [146]. Small waveguide dimensions increase the confinement factor, which in turn increases the scattering losses attributed to sidewall roughness. Grillot et al has performed a theoretical study on the effects of waveguide dimension against scattering loss showing dramatic differences between sidewall roughness

values of 2nm and 10nm [147]. Recent advances in fabrication technology, namely immersion lithography, has seen the loss of a 220nm \times 400nm waveguide decrease to below 1dB cm⁻¹ due to a decrease in sidewall roughness [148].

4.3 Taper Design

To enable efficient coupling between an optical fibre and a grating coupler, the overlap integral of the two modes must be maximised. In order to achieve a high level of overlap the silicon waveguide width must be increased from the width of a single mode waveguide, to a size comparable to the optical fibre mode. A spot size converter such as a taper is required to facilitate this waveguide width transition in order to mitigate the losses incurred in the transition. In this case the taper is required to transition between the 400nm wide single mode waveguide and the 10 μ m wide grating coupler. If the spot size converter is adiabatic, it will maintain the power in a specific eigen mode without any interaction between different propagating modes. This behaviour is beneficial when considering a transition from a multimode to a single mode waveguide, as any power transferred to higher order modes is lost.

The complexity of an adiabatic spot size converter varies dependant on the tolerable taper length. While short tapers are desirable, taper length is inversely proportional to complexity. Advanced structures such as lensed tapers, demonstrated by Acoleyen [149] allow taper lengths below 22 μ m for a transition between 12 μ m and 500nm, with losses as low as 0.5dB. Using experimental technology however may detract from the erasable grating device being tested. In order to minimise risk a linear taper design will be utilised for these structures, chosen for its relative simplicity and very high efficiency, which is well suited to demonstrate the proof of the principle. Tapers are well known structures with the only critical design factor, as described by R. Winn and J Harris [89], being the flare angle of the taper. The flare angle will dictate the length and loss of the device. Linear tapers are relatively very long, which increases the total device length significantly. In this work the length of the device is not critical for the initial proof of concept, with the primary objective being to demonstrate an implanted grating coupler. As device length is unimportant for a proof of principle, the taper may be able to offer efficiencies which allow the taper to be considered as lossless to allow

characterisation of the grating coupler. In the longer term however, it would be desirable to reduce the device length.

For accurate simulation results tapers must be simulated in 3D FDTD, although this leads to excessively long simulation times for linear tapers. 2D FDTD offers a reasonable approximation for taper structures. 2D and 3D FDTD simulations of lensed taper structures have been presented by Acoleyen and Baets [149], which show for TE modes that the focal length of the etched lens for a given curvature is in close agreement between the two simulation methods, though the calculated efficiencies can vary significantly. Transmission efficiencies of 95% and 87% were found for the same device geometries using 2D FDTD and 3D FDTD simulation methods respectively.

Lumerical offer a 2.5D FDTD package which aims to combine the speed of 2D simulations and the improved accuracy of 3D simulations [150], this can be achieved by using a 2D effective index approximation of the 3D structure [151], though 3D FDTD remains the gold standard. Taper transmission efficiency has been simulated using Lumerical's 2.5 FDTD for a variety of taper lengths to transition from a $10\mu\text{m}$ wide silicon waveguide into a 400nm wide silicon single mode waveguide, the simulated results are shown in Figure 4.4. The simulations show that transmission efficiencies in excess of 98% are calculated for device lengths greater than $250\mu\text{m}$.

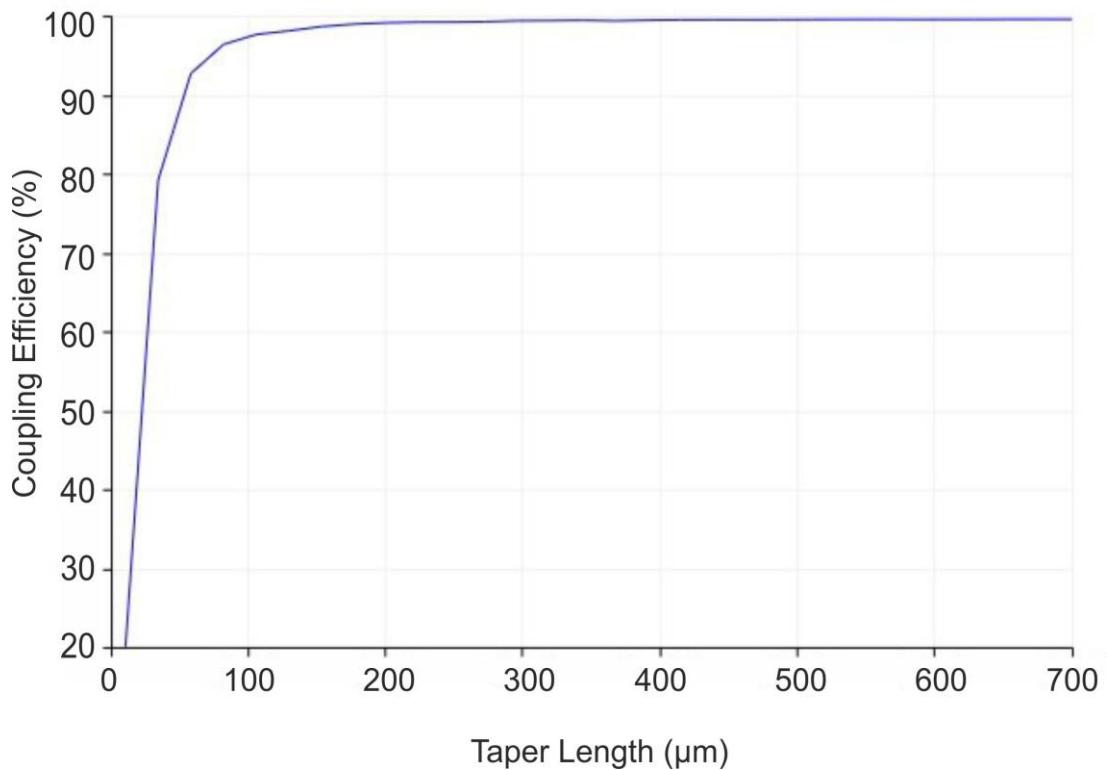


Figure 4.4 - 2.5D FDTD simulation of taper efficiency vs length for a 220nm taper transitioning between 10μm and 400nm

Simulations showing the transmission power as a function of the distance travelled in a short taper gives an insight into exactly where the power is lost in a waveguide taper as shown in Figure 4.5. The results show the vast majority of the loss occurs in the last 5μm of the 40μm taper, which suggests that the taper is more sensitive to large flare angles as the taper approaches the single mode condition.

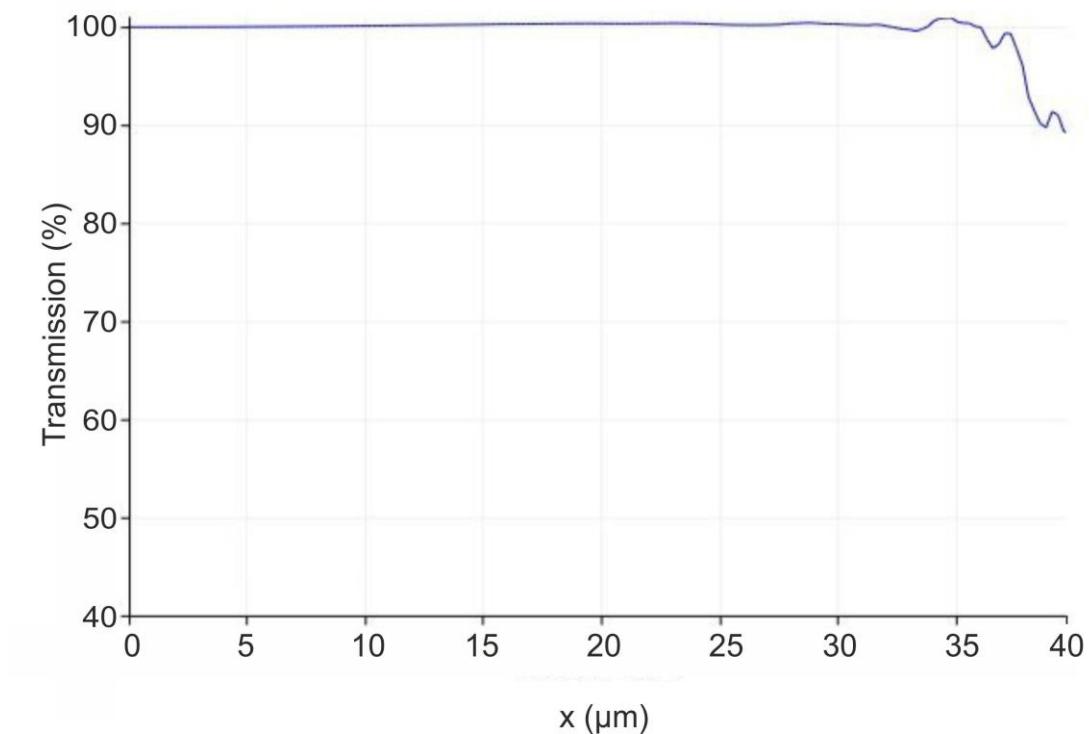


Figure 4.5 – Transmission power as a function of distance travelled in a 30 μm long taper transitioning from 10 μm to 400nm, x represents the direction of propagation

The Epixfab platform offers a library of standard components including a tried and tested linear taper structure. The taper is made up of 2 sections, the first section transitions from 10 μm to 3 μm with a flare angle of 0.6° which corresponds to a length of 350 μm . The second section makes the final transition from the 3 μm section to the 400nm single mode waveguide at a shallower angle of 0.2° which corresponds to a length of 350 μm . This leads to a taper structure more than twice as long as the simulations in Figure 4.4 suggest are necessary for a lossless adiabatic taper, although this ensures the taper will perform very well, which is more important than device length at the concept stage. The reference 700um taper described will be used in this work, as a lossless taper allows the gratings under test to be characterised without any need to attempt to distinguish the loss characteristics of the taper from the grating.

4.4 Grating Couplers

4.4.1 Implanted Grating Coupler Design

When considering wafer scale testing it may not be desirable to have a coupler design with the highest optical power extraction possible. If 100% of the light exits the

waveguide at the location of the test point there will be no remaining optical power to interrogate devices positioned beyond the initial test point, without removing the test point before subsequently testing the next. Consequently it is possible to split the power in the guided mode by design such that a controlled proportion of light is coupled out of the waveguide to a fibre and the remaining power continues along the waveguide. However, with regard to the proof of principle, obtaining the highest output coupling possible is the larger technical challenge. Reducing the outcoupled light is simply a matter of reducing the number of periods or designing a grating with a central wavelength offset from the operating wavelength.

Simulations were performed in Lumerical with a grating coupler configured in an output coupling regime as shown in Figure 4.6. A rectangular profile represents the ideal profile of the amorphous regions. The simulations show that the actual amorphous region is likely to be a slightly rounded profile, though the computational complexity associated with simulating a large range of gratings with the exact amorphisation profile is prohibitive. This approximation has been used successfully before, but on a smaller scale [77].

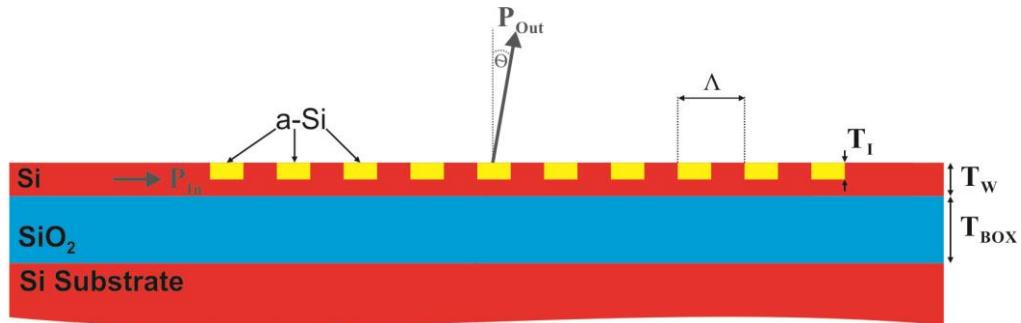


Figure 4.6 - 2D Simulated implanted grating coupler structure

A guided mode was launched at P_{in} and subsequently collected at P_{out} . T_w is the waveguide height and was set at 220nm and T_{box} is the buried oxide thickness which was set at 2 μ m. The grating period is represented by Λ and the implant depth is denoted by T_l . The performance metric used was the output efficiency, η_{out} which is given by equation 4.2.

$$\eta_{out} = \frac{P_{out}}{P_{in}} \quad (4.2)$$

Optical power can be observed leaving a grating coupler in one of four directions as depicted by Figure 4.7. Light can be transmitted, reflected, or coupled to either the substrate or the superstrate. The objective is to maximise coupling to the superstrate for coupling to an optical fibre to allow interrogation of the optical circuit. Transmitted light is not desirable, though would not be considered loss as the power can continue to other devices in the optical circuit, ultimately to the circuit output or the next test point. Reflections and substrate coupling do however both contribute to lost power. Substrate power can be harnessed through the use of a bottom reflector, though this would dramatically increase complexity to what may be impractical for wafer scale testing.

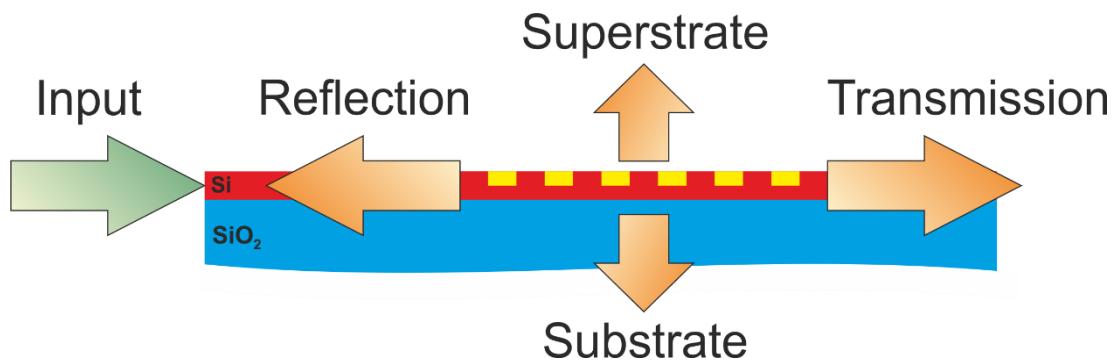


Figure 4.7 - Propagation directions for optical power leaving a grating coupler

Only the case of the output coupler was considered in simulations as grating couplers are reciprocal [56]. 2D simulations are often used in the literature to reduce computational complexity as the waveguide width used for a grating coupler is sufficiently wide (typically 10 μ m), the effective index does not vary significantly between a 2D and 3D case [47]. However, code in Lumerical's FDTD engine utilises the powerful server hardware available at Southampton University very well, and allows advanced boundary conditions and an intelligent non-uniform mesh, which work in tandem to drastically reduce the computational complexity. An optimised 3D simulation of a 10 μ m long grating coupler with 4 transmission monitors can run in under 5 minutes on a 24 processor core server with 64GB of random access memory. Hence, the simulations were performed in Lumerical's 3D FDTD engine to maximise efficiency, the simulation design can be seen in Figure 4.8.

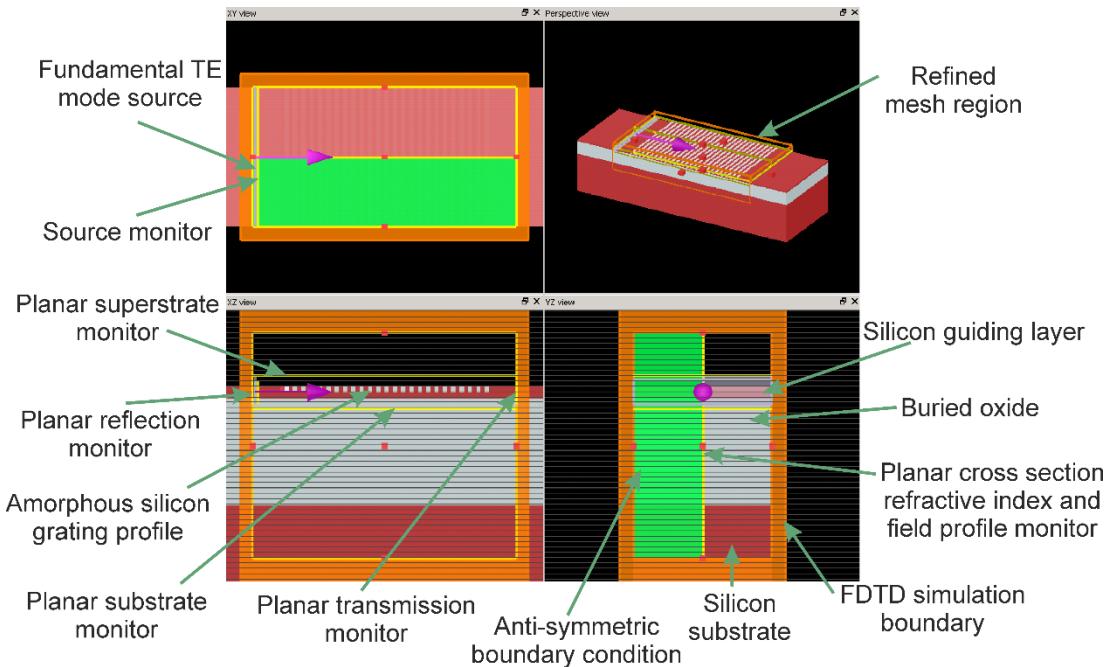


Figure 4.8 - Grating coupler simulation layout in Lumerical FDTD

The light green region in the simulation window shown in Figure 4.8 highlights the anti-symmetric boundary condition selected, allowing the computational complexity to be reduced by a factor of 2. The electric field propagates transversely across the waveguide in the case of a TE mode, without a discontinuity of the field in the mode profile. An anti-symmetric boundary condition at $y=0$ can be used to describe this relationship between the two waveguide sections and thus half the required simulation time. To demonstrate the difference between the symmetric and anti-symmetric boundary conditions, mode profiles for a $10\mu\text{m}$ wide waveguide with a height of 220nm are shown in Figure 4.9 using both symmetric and anti-symmetric boundary conditions. The symmetric boundary condition shows a very different profile to that simulated without the boundary condition, demonstrating the field reaching zero at $y=0$ whereas the anti-symmetric boundary condition matches the profile displayed by the full simulation exactly.

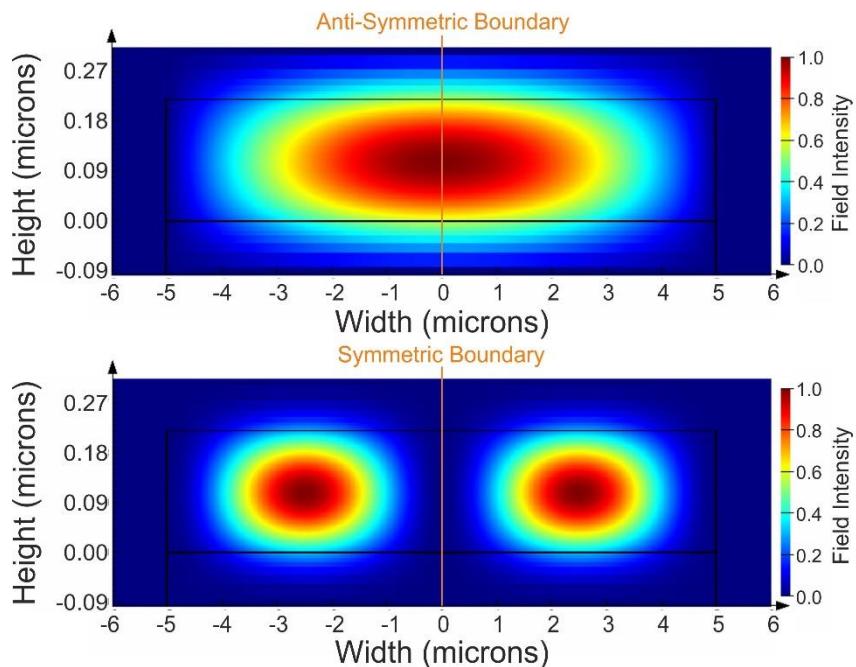


Figure 4.9 - Mode profiles of a 10μm wide, 220nm waveguide, using anti-symmetric (Top) and symmetric (Bottom) boundary conditions

Three distinctive regions of strong outcoupling emerge as shown in Figure 4.10, each region representing a different superstrate diffraction order. Region one consists of periods between 420nm and 510nm, region 2 consists of periods between 510nm and 540nm and region 3 encompasses periods between 540nm and 690nm.

A successful grating design can be obtained by monitoring the transmission through 4 simple monitors setup to monitor light leaving the grating as described earlier in Figure 4.7. Initially we take a look at the outcoupled transmission results for a 10μm long grating coupler with a range of amorphous depths and grating periods in the format of a contour plot as shown in Figure 4.10.

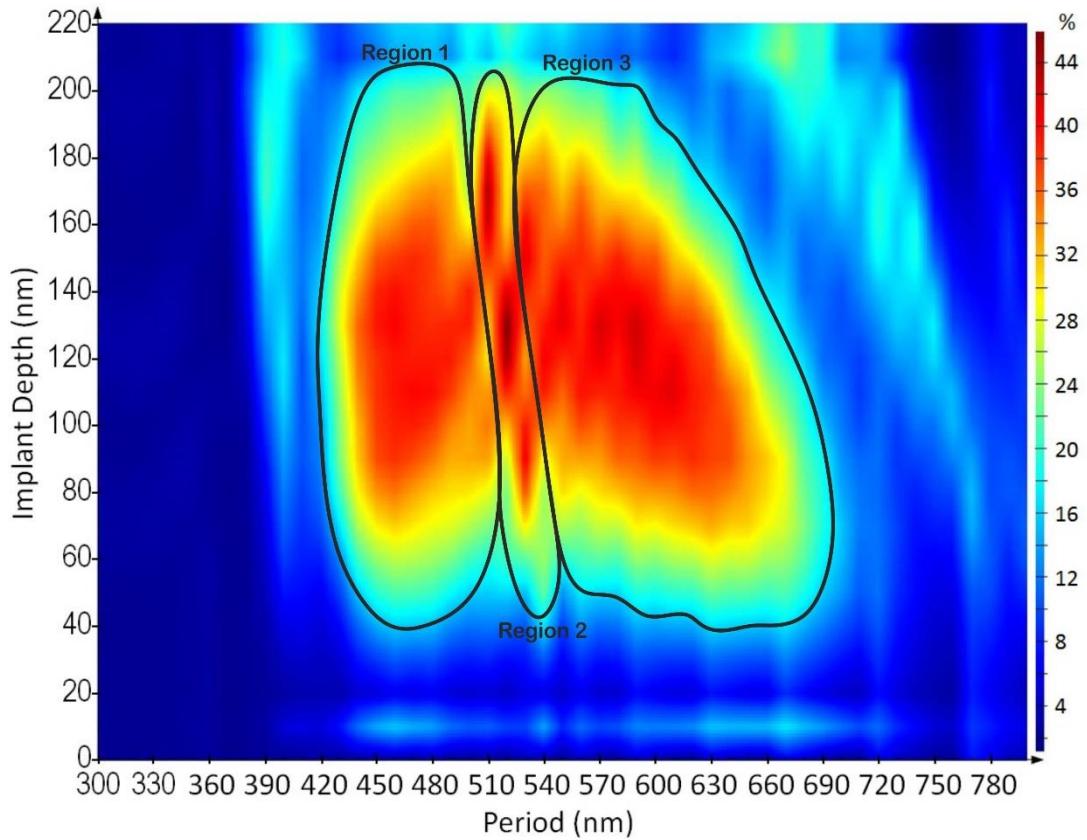


Figure 4.10 - 220nm Thick silicon ion implanted grating coupler, with a 2um buried oxide simulated over a range of periods and implant depth. Diffraction orders 1,0, and -1 are labelled as Regions 1, 2, and 3 respectively.

The diffraction order of a grating determines the direction of the coupled mode, Figure 4.11 shows superstrate diffraction orders in green and substrate diffraction orders in purple, where D is a diffracted wave. Analysis of the relevant grating superstrate far field profiles shows that region 1 corresponds to a grating diffraction order of 1, region 2 corresponds to a grating diffraction order of 0 and region 3 corresponds to a grating diffraction order of -1. The grating designed in this work targets a diffraction order of -1. A diffraction order of 0 typically results in large undesirable back reflections into the optical circuit [152] and a diffraction order of 1 would result in a cumbersome test setup, however there is no reason an implanted grating coupler could not be designed for any diffraction order if it were required.

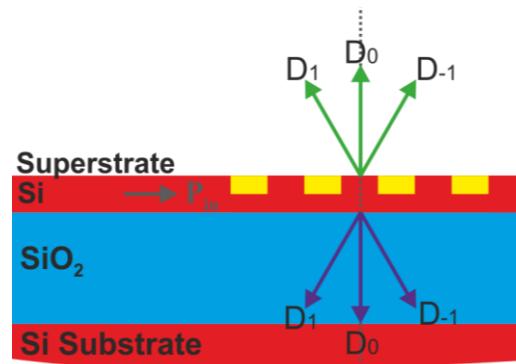


Figure 4.11 - Illustration of grating diffraction orders, Superstrate diffraction is shown in green, and substrate diffraction is shown in purple, where D is a diffracted wave.

Next we inspect the substrate loss as shown in Figure 4.12. Regions of very high loss are shown both for very low and very high periods, and though these are not regions of interest, it is interesting to see that a surface grating coupler can be designed to couple around 70% of the input power to the substrate, whereas a uniform grating coupling to the superstrate only achieves a maximal power of 45%.

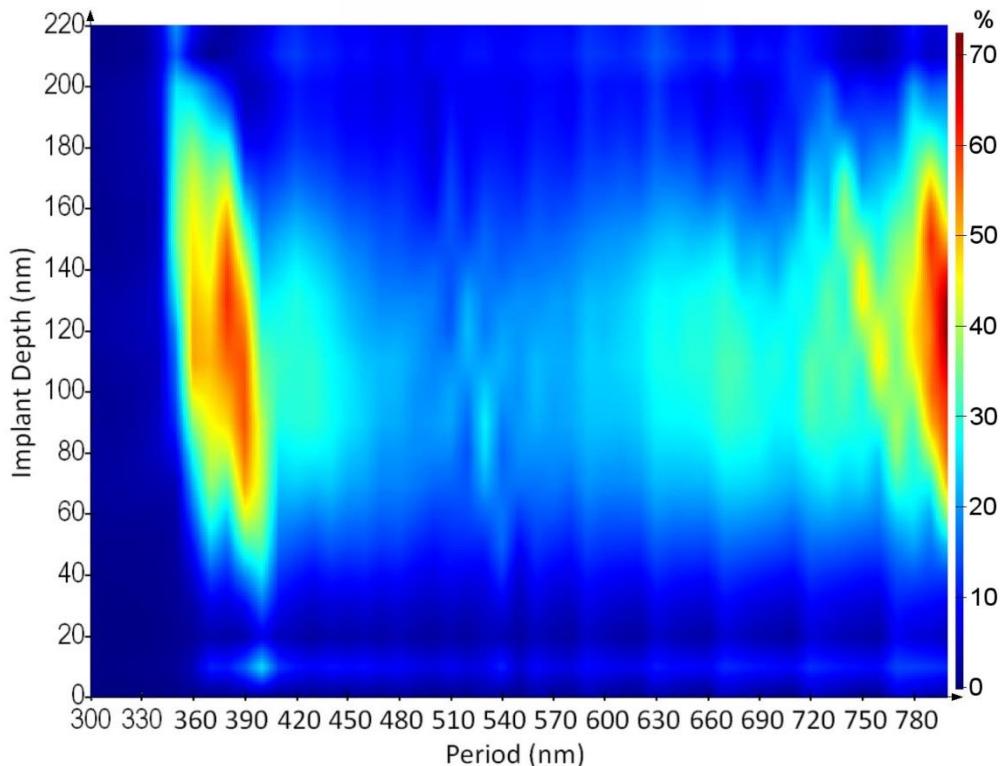


Figure 4.12 - Substrate loss for a 220nm thick silicon grating coupler with 2um buried oxide for a range of periods and implant depths

If we consider the superstrate data in conjunction with the substrate data, we see a localised maximum occurs with a period of 600nm and implant depth of 130nm in the outcoupling results, due to the reduced substrate losses within the region. Furthermore if we also consider the simulated reflection data given in Figure 4.13 and simulated transmission data given in Figure 4.14 we see minima at the same point suggesting that these parameters allow the device to function with minimal wasted power. This demonstrates congruency between the simulated results and suggests that optimal performance would be obtained with these parameters

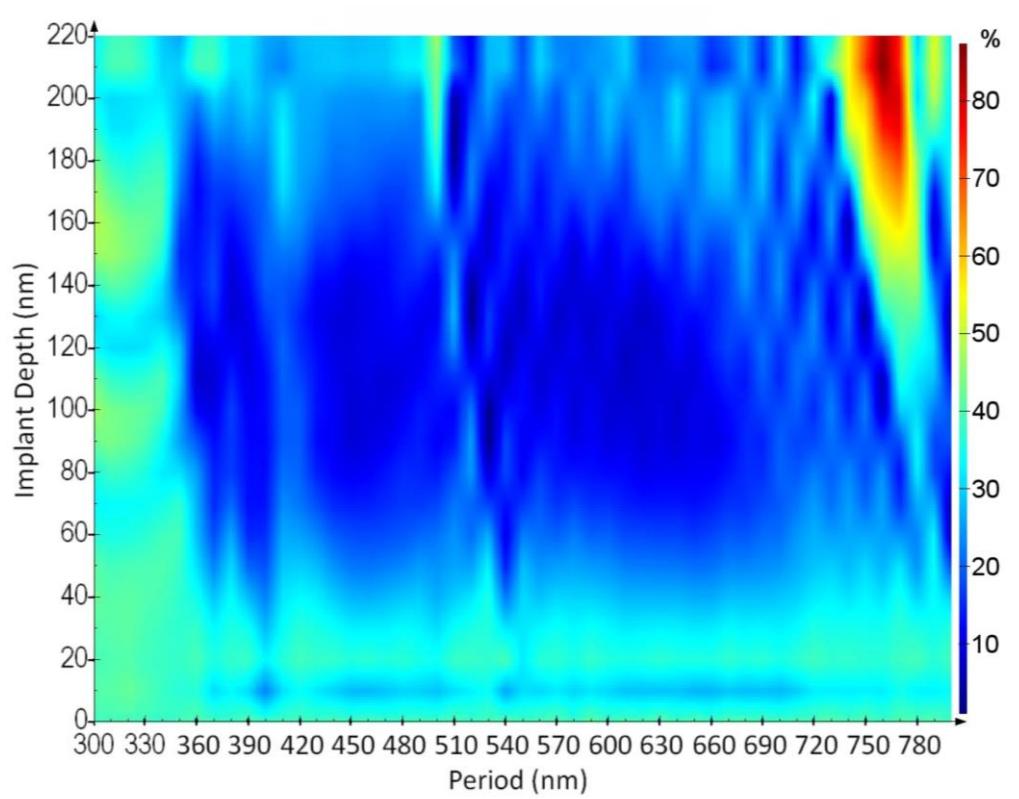


Figure 4.13 - Reflected power for a 220nm thick silicon grating coupler with 2um buried oxide for a range of periods and implant depths

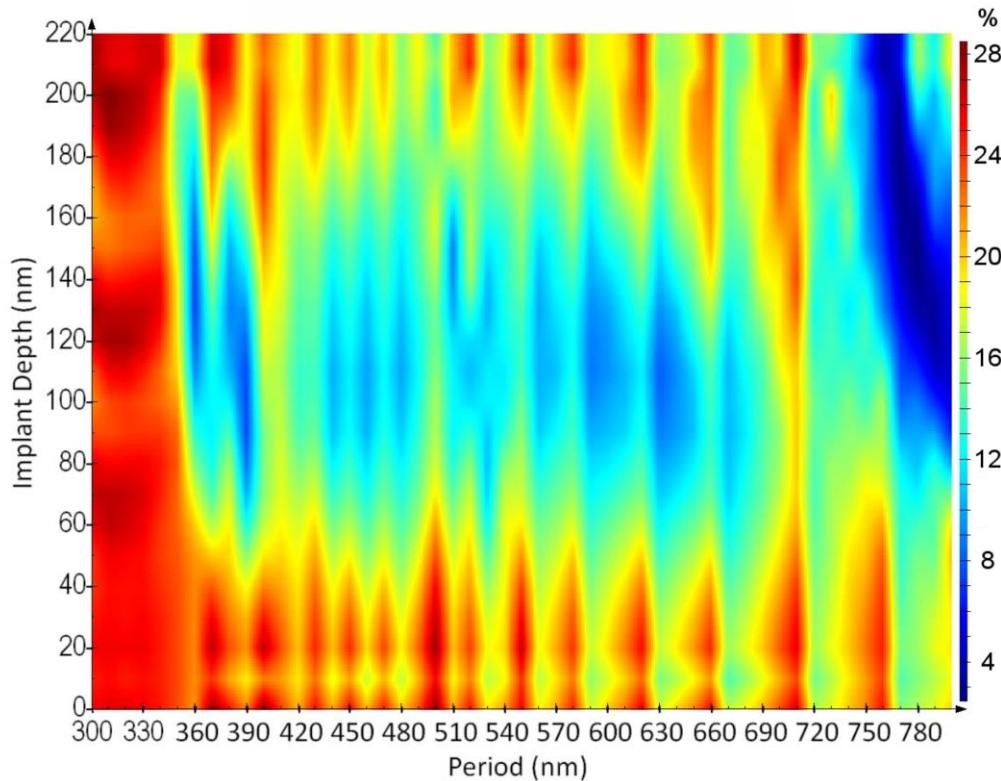


Figure 4.14 - Transmitted power for a 220nm thick silicon grating coupler with 2um buried oxide for a range of periods and implant depths

At this point all simulations performed so far use a duty cycle of 0.5. To assess the optimal duty cycle, simulations were performed for an implanted grating coupler with a period of 600nm and implant depth of 130nm while varying the duty cycle as shown in Figure 4.15. The result shows a duty cycle of 0.49 provides the best performance, though there is very little performance variation in the duty cycle range of 0.45 to 0.55.

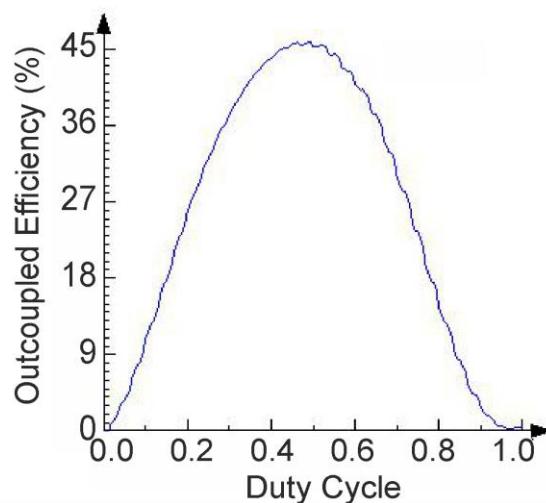


Figure 4.15 - Implanted grating coupler duty cycle vs output efficiency for a 600nm period grating coupler with an implant depth of 130nm

The final factor that affects a uniform grating coupler is the thickness of the buried oxide. This parameter has been fixed at $2\mu\text{m}$ for all simulations. The outcoupling efficiency for a variety of buried oxide thicknesses is shown in Figure 4.16, using a 600nm period implanted grating, 130nm implant depth and 0.5 duty cycle. The results show that buried oxide height is clearly a key factor in the performance of an implanted grating coupler. Very low buried oxide thicknesses result in no outcoupling as expected, as without an insulator, light is not confined tightly into the silicon guiding layer and hence divergence prevents strong interaction with the grating profile. Beyond the very thin buried oxide layers, peak performance is observed periodically, with a period of $\sim 600\text{nm}$. Unfortunately the buried oxide is not a parameter that is easily varied in device fabrication, the buried oxide thickness is set by the SOI wafer which is purchased, typically supplied with buried oxide thicknesses of $1\mu\text{m}$ or $2\mu\text{m}$. Fixing the buried oxide thickness at $2\mu\text{m}$ throughout the simulation process has allowed the other grating parameters to be optimised around the constraints of the buried oxide thickness, with a definitive peak observed for a $2\mu\text{m}$ buried oxide thickness.

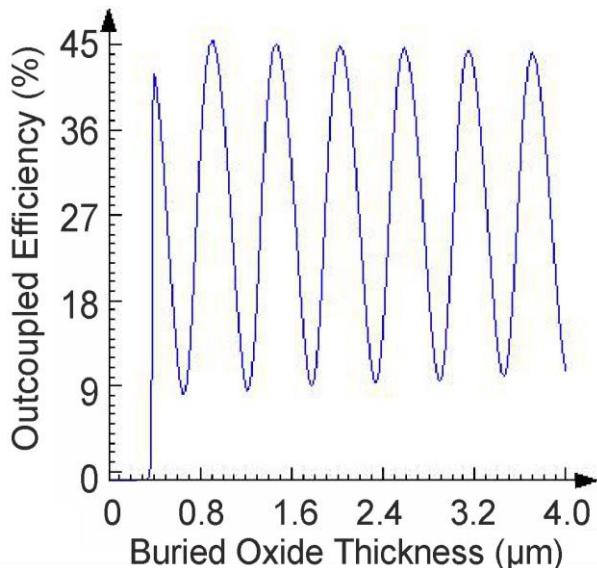


Figure 4.16 - Output efficiency vs buried oxide height for a 600nm period implanted grating coupler with a 130nm implant depth and a 0.5 duty cycle

4.4.2 Surface relief grating coupler comparison

There are few discernable differences between an implanted grating coupler and the traditional surface relief grating coupler. An implanted grating coupler uses lattice disorder to introduce a positive refractive index change of ~ 0.5 while retaining the planar surface. There is little interaction with the superstrate in an implanted grating coupler, leading to uniform performance regardless of the cladding used. An etched grating coupler however, uses an etch to create the refractive index change. The superstrate material fills the etched regions, which leads to an index change and hence grating performance which is dependent on the cladding material used for the optical circuit due to the high superstrate interaction. For the simulations in this section an air cladding has been assumed, which gives a refractive index contrast of 2.48, the highest refractive contrast that may be seen in practice. Figure 4.7 in the previous section shows that optical power can leave the grating in one of four directions, and hence all four (outcoupled, box coupled, reflected and transmitted optical power) will be considered for the surface relief grating coupler as a direct comparison to the implanted results shown in the previous section. Furthermore it is important to note that as grating couplers are reciprocal [56], the surface relief grating coupler will be considered only in its output coupler configuration.

The outcoupled power for a surface relief grating coupler with a 220nm guiding layer and $2\mu\text{m}$ buried oxide layer is shown in Figure 4.17. Comparing the simulation data of the surface relief grating seen here and the implanted grating coupler simulation data presented earlier in Figure 4.10 shows the surface relief gratings are able to couple more light into the superstrate which is to be expected due to the higher refractive index change in this device topology. The optimal coupling period and etch depth are shown to be 660nm and 80nm respectively, which achieves an outcoupling efficiency of 55%, compared with the implanted grating coupler at 45%. In a typical processed device, the surface relief grating structures would be filled with SiO_2 , despite decreasing the absolute refractive index, this does not alter the efficiency achievable, 55% is achieved with the same period, but an increased etch depth of 88nm.

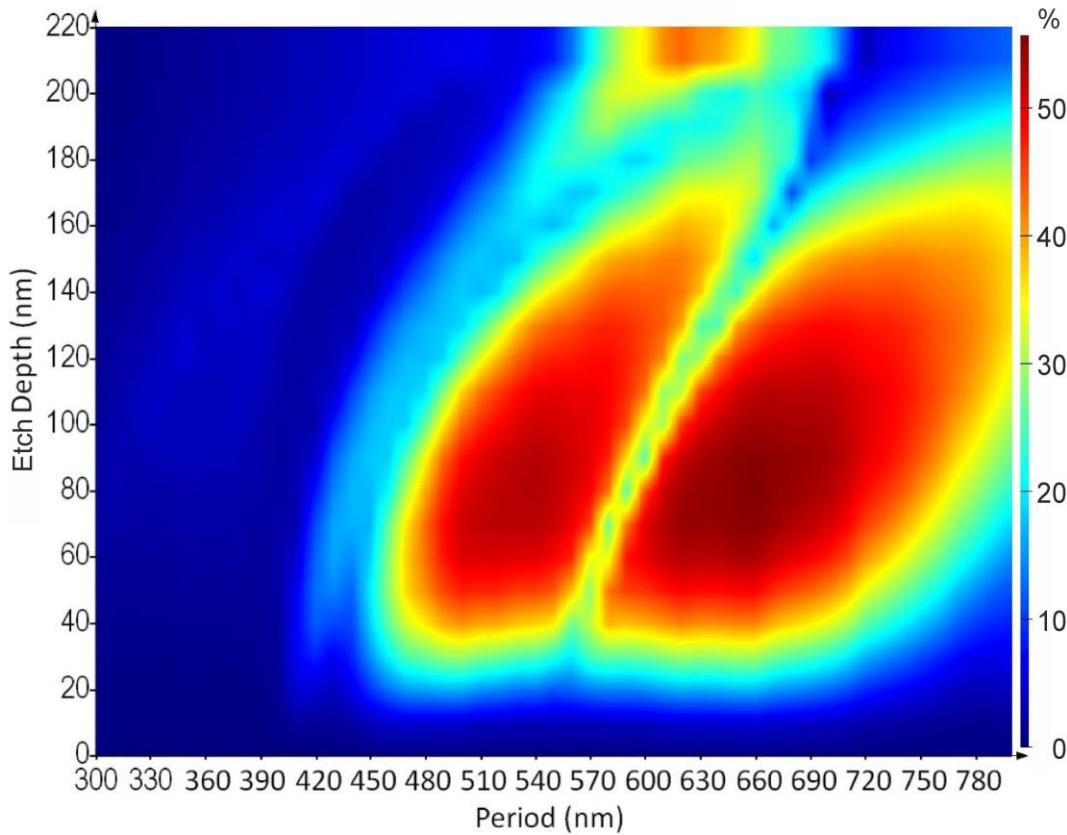


Figure 4.17 – Outcoupled power for a 220nm SOI surface relief grating coupler with 2um buried oxide for a range of periods and etch depths

Figure 4.18 shows the variation in outcoupled power for different buried oxide heights with a 660nm surface relief grating with an 80nm etch depth. This also shows that the period and etch depth have been successfully optimised with respect to the fixed buried oxide height.

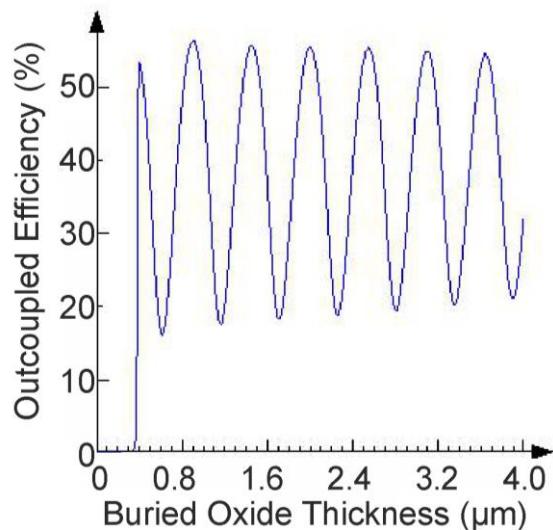


Figure 4.18 -Output efficiency vs buried oxide height for a 660nm period implanted grating coupler with an 80nm implant depth and a 0.5 duty cycle

It is important to note that as in the case of the implanted coupler, it is possible to couple more optical power into the substrate than the superstrate, with a maximum of 80% of the input power coupled to the substrate as shown in the contour plot of substrate loss in Figure 4.19. For the range of etch depths and grating periods simulated in Figure 4.17, the etch depth and period which result in the highest outcoupling efficiency (a period of 660nm and etch depth of 80nm), also result in 41% of the input power coupled to the substrate compared with only 25% of the input power coupled to the substrate in the implanted case, which results in negligible transmission for the etched coupler at this point as shown in Figure 4.20. This is another strength of the implanted grating coupler when considering wafer scale testing, the power transmitted will allow the next device in the circuit to be tested before any test points are removed from the optical circuit.

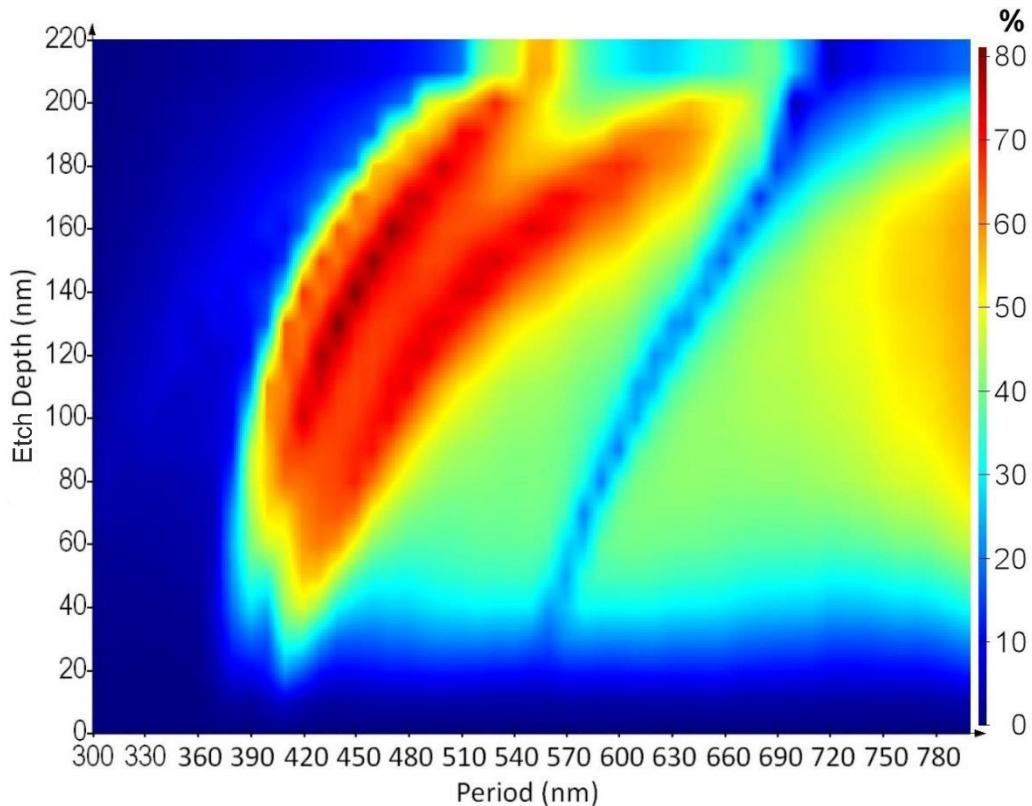


Figure 4.19 – Substrate loss for a 220nm SOI surface relief grating coupler with 2um buried oxide for a range of periods and etch depths

For completeness, the reflected power from a range of etch depths and periods is shown in Figure 4.21. In the position of maximum outcoupling, the reflected power is insignificant as would be expected from the earlier results with 96% of the input power

already accounted for. It is interesting to see there is a strong reflection for periods which correspond with a diffraction order of zero, which would be used to achieve vertical coupling. This strong reflection is not present in the implanted coupler, which alludes to the potential performance of implanted couplers in a vertical coupling scenario. Vertical coupling is desirable, as it presents a simpler packaging solution than coupling solutions which require more intricate angular alignment [128, 153].

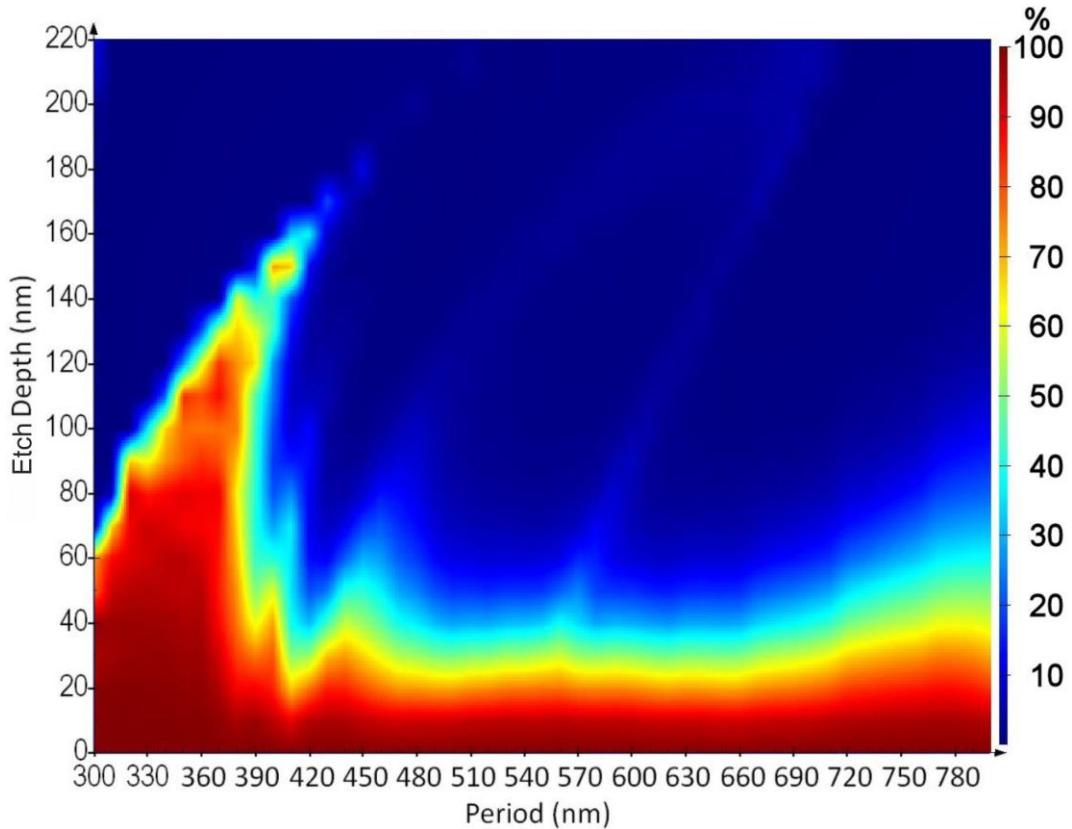


Figure 4.20 - Transmitted power for a 220nm SOI etched grating coupler with 2um buried oxide for a range of periods and etch depths

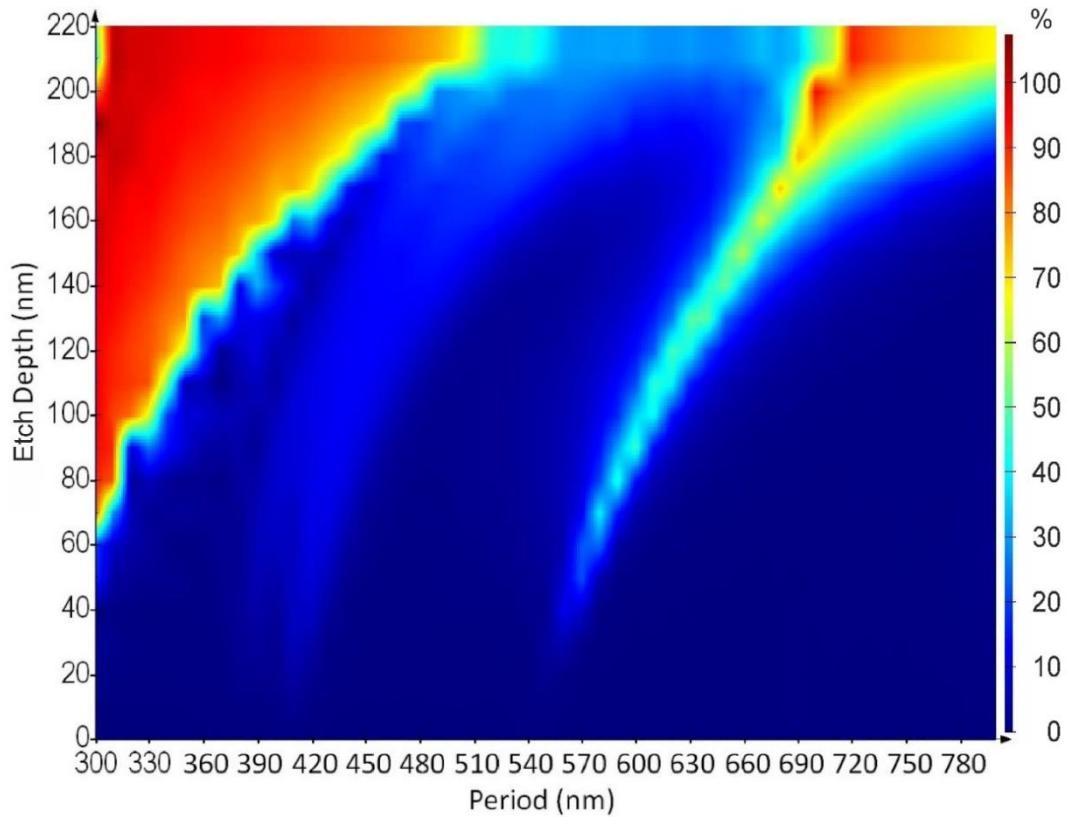


Figure 4.21 – Reflected power for a 220nm SOI etched grating coupler with 2um buried oxide for a range of periods and etch depths

4.5 Amorphization and Lattice Damage

Amorphization is the cornerstone of this device. The underlying theory is discussed in detail in section 2.5.2. This section will detail the implant design process used to achieve an amorphous grating profile in crystalline silicon, while ensuring the process does not leave significant residual effects such as losses. The first step in this process is selecting a suitable ion, followed by establishing a sufficient masking layer. Finally a suitable ion dose and implant energy are selected.

4.5.1 Ion Selection

The shape of the amorphous region has been modelled as a rectangle for the purposes of optical simulations, however the profile of implantation damage is not so straightforward. Loiacono et al showed a TEM image of a 30 kev implant through a small slit as shown in Figure 4.22 [42], the profile observed was akin to a rounded rectangle, the profile was also shown to be in good agreement with the simulated results from King 3D, confirming its accuracy for this application.

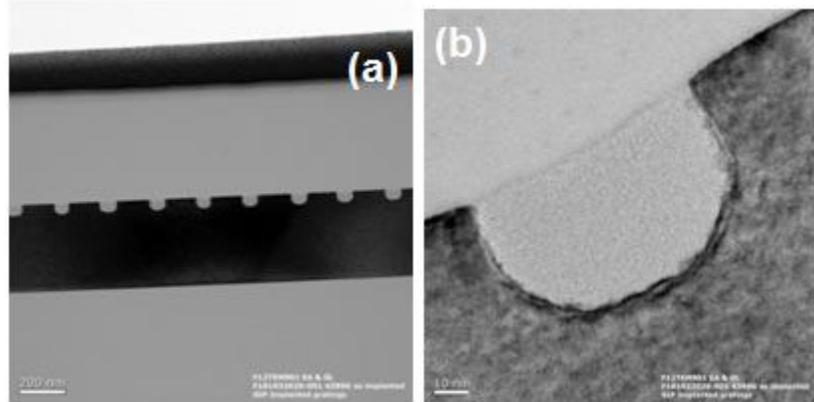


Figure 4.22 - TEM image of 30kev implants into Silicon [42]

The amorphous patterns shown in Figure 4.22 make up a Bragg grating which was also modelled successfully as a rectangular profile [77]. The refractive index change is large enough that it can be clearly imaged, even on an optical microscope.

The performance of an implanted grating relies heavily on the implant design. A well designed implant will not dope the waveguide, it will minimise broadening under the mask, and it will create a disordered lattice with a low dose to minimise any residual impurities in the waveguide.

Doping the waveguide introduces carrier dependant loss, which can be significant, especially if the implant is activated during the annealing stage. This limits the viable implant selection to elements with the same number of valence electrons as silicon, or elements with a complete valence shell to ensure no doping occurs.

To avoid impurities the use of a silicon implant to amorphise silicon has been considered to create the amorphous profile, however the atomic mass of silicon is too low. As discussed earlier in section 2.5.2.2, the energy from ion implantation is conventionally absorbed by electronic collisions and nuclear collisions, with the latter as the desirable mechanism when trying to create lattice disorder. Light ions such as silicon lead to very broad profiles due to a large number of collisions which do not deliver enough energy to displace the atoms in the target lattice, for higher energies amorphisation can even begin below the surface [77], preventing its use in the fabrication of the simulated amorphous grating configuration.

Simulations show that the amorphous profile, or more specifically the broadening below the implant mask is effected by the implantation energy, with higher energies leading to broader disordered regions. It is also clear from simulations that heavier ions require higher implantation energies to achieve the same depth of amorphization. The energies required to establish an amorphous layer of 74nm were found for Xenon, Tin and Germanium using KING software [154]. The required energies for a dose condition of 1×10^{15} ions cm^{-2} were found to be 71keV, 68keV, and 50keV respectively. The amorphous profile was then found using a masked implant in KING 3D for each element with its respective energy, the results of which are presented in Figure 4.23.

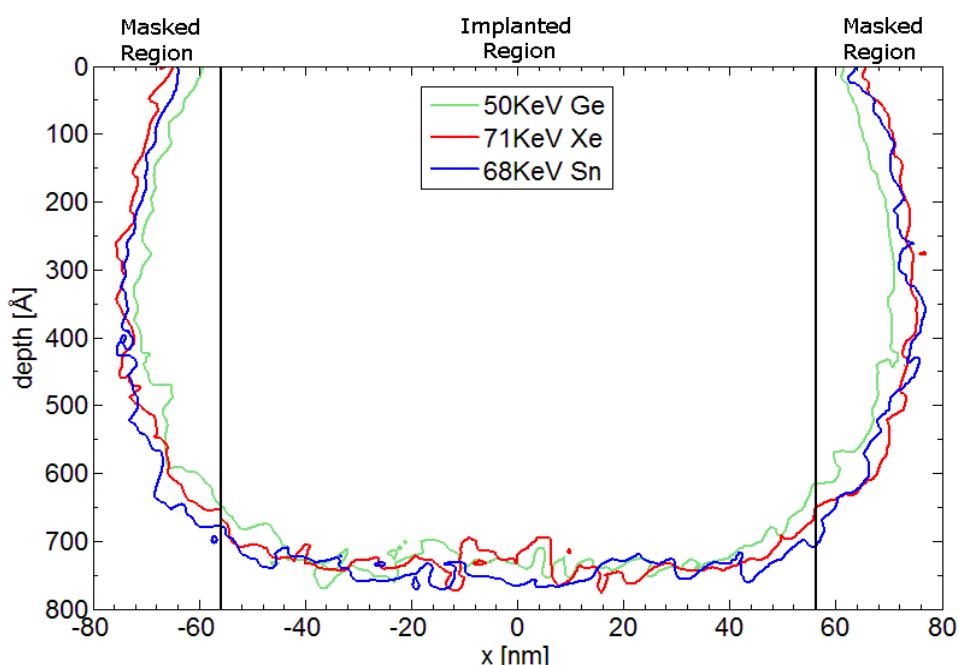


Figure 4.23 - Amorphous profiles for masked implants of Ge, Xe and Sn at a dose of 1×10^{15} ions cm^{-2}

The results in Figure 4.23 show the extent of lateral straggling for Ge, Xe and Sn when implantation conditions are selected to achieve a 74nm layer of amorphous silicon. The results show that Ge offers the most compact profile of the elements tested. Furthermore at a dose of 1×10^{15} ions cm^{-2} Dood et al show Xenon produces a Δn of only ~ 0.3 [155] compared with the same dose of Ge offering a Δn of ~ 0.5 [77]. Using Xenon with a higher dose condition may result in a higher refractive index change than 0.3, but this would lead to increased broadening under the implant mask. This shows that of the elements tested, germanium offers the best amorphization profile, and it is

also important to note that germanium is CMOS compatible enabling this process to be carried out in CMOS fabrication facilities without the risk of sample contamination.

4.5.2 *Implant masking*

Selection of an appropriate masking material is critical to preventing lattice damage occurring in the silicon regions underneath the mask. The mask must withstand the implantation conditions required to achieve an amorphous profile with a depth of 130nm; the value shown to offer the maximum outcoupling efficiency in simulations performed earlier in this chapter. Typically silicon dioxide would be an obvious choice for this task. Simulations show that the stopping range of ions in silicon dioxide are very similar to those of the stopping ranges of ions in silicon as shown in Figure 4.24.

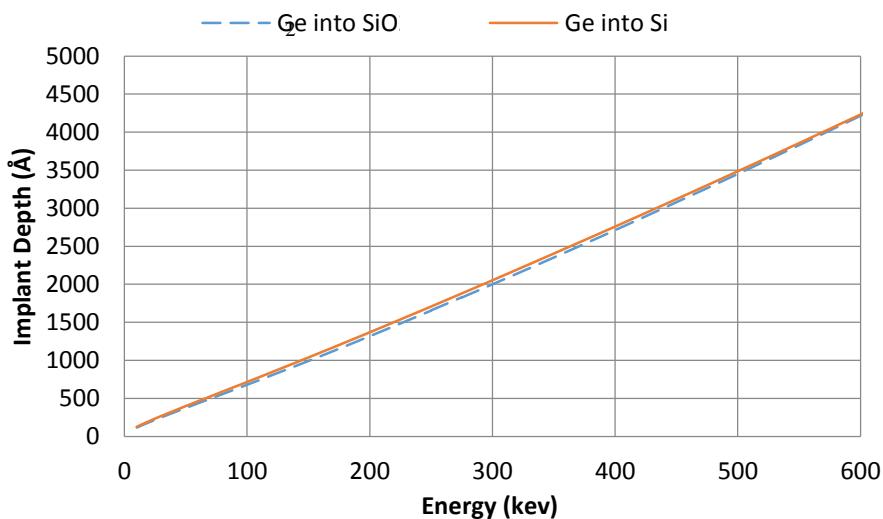


Figure 4.24 - Stopping Range of Ge into Si and SiO₂

Fundamentally, the wafer scale testing process must not risk any detriment to the optical circuit. Though the use of an oxide hard mask is not an issue, removing an oxide hard mask layer does present a problem when using strip waveguides, which is outlined in Figure 4.25. Using the same chemistry for the buried oxide layer and the hard mask means that when etch must be controlled in an incredibly accurate manner to achieve the correct etch to prevent under etching of the waveguide as shown in case B of Figure 4.25. Failure to achieve a perfect etch would result in under etching the waveguide due to removal of the buried oxide as shown in case C of Figure 4.25, in the worst case the waveguide may even become detached from the substrate.

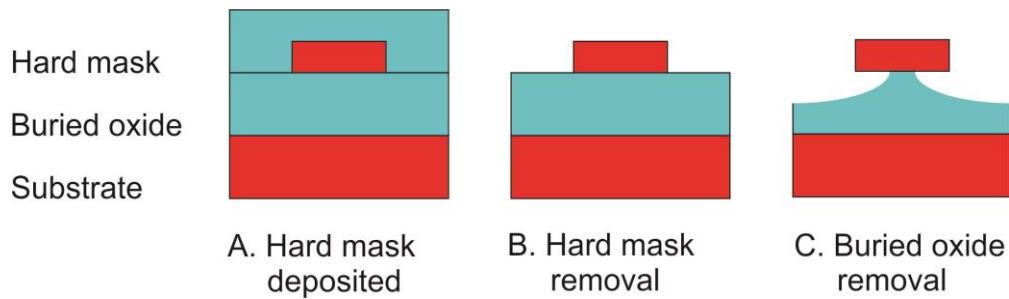


Figure 4.25 -Removal process of silicon dioxide from a silicon strip waveguide

Silicon nitride may be used as an alternative hard mask, as the chemistry of silicon nitride is different to that of silicon dioxide, though unfortunately silicon nitride exhibits similar chemistry to amorphous silicon with selectivity between the two compounds being relatively low. The literature shows the best selectivity achieved is 40:1 for silicon nitride to amorphous silicon [156], though this process would take over 14 hours for a 220nm layer and would still result in an unacceptable etch of 6nm into the amorphous silicon.

A successful wafer scale testing system relies on robust and simple fabrication. The simplest way to mask an implant is to use a photoresist or electron beam resist, as this removes the need for a complex etch process. A ZEP electron beam resist was considered as an implant mask using SRIM (Stopping Range of Ions in Matter) software [157] to simulate the ion implantation process as shown in Figure 4.26. Using a low spin speed, a ZEP resist thicknesses of 500nm can be readily achieved.

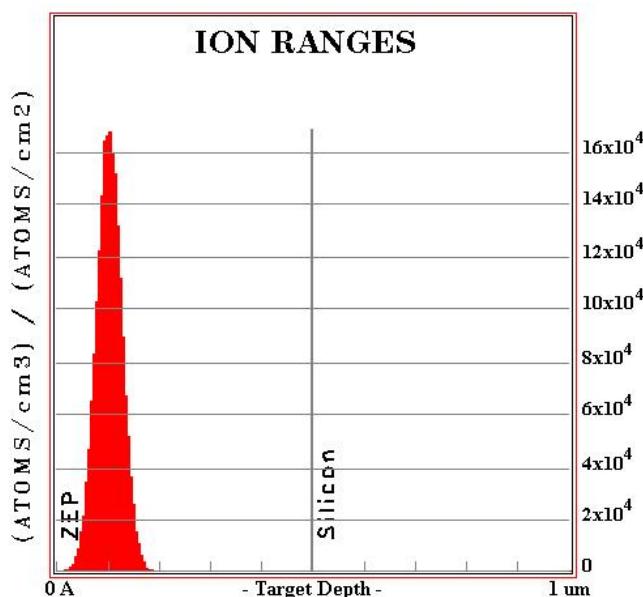


Figure 4.26 – Ion stopping range for 100kev Ge into 500nm ZEP resist.

In this simulation ZEP was modelled with a density of 1.220 g cm^{-3} and a composition of H33 C19 Cl1. The ion distribution peaks at 103nm and no ions pass beyond 200nm from the surface. This shows that ZEP is capable of successfully resisting the implant design to be used for the implanted grating coupler. The use of a ZEP resist as an implant mask does introduce some issues. The heat generated through the process of ion implantation further dehydrogenates the ZEP resist which can make removal slightly more difficult, though perhaps more significantly it introduces cross-links between the polymer chains within the resist in a process known as cross-linking, this process makes the resist very difficult to remove. Fully cross-linked polymers are almost insoluble in common solvents [158], cross-linked resist has even been known to be used structurally for Microelectromechanical Systems (MEMS) [159]. As the implant does not fully penetrate the resist, this should not present an issue for low beam currents (below $10\mu\text{A}$), high beam currents will however reduce the localisation of heating and thus produce a thicker carbonised layer. By using a low beam current the carbonised layer is localised to the implanted region, which allows solvents to remove the unaffected resist underlying the carbonised resist and hence separate the carbonised resist from the silicon surface, resulting in a clean surface with no risk to the optical circuit.

4.5.3 *Implant parameters*

King (2D) and King 3D use a Monte-Carlo Binary Collision approximation method for simulation, which does not account for dynamic annealing and the transport of defects [160], hence the simulation must be considered to be most accurate for samples cooled with liquid nitrogen. The simulation highlights large interface regions of lattice disorder, which are neither fully amorphous nor crystalline. Interface regions can be substantially reduced by implanting at room temperature. When the implant is performed at room temperature these regions are not present due to dynamic annealing effects which occur during implantation [161], as verified via TEM images of similar implant designs [19, 46]. Utilising room temperature implantation also reduces the time and cost of the implantation process.

Simulations to find the correct implant depth have been conducted in the KING (2D) software package to allow a range of implant energies to be tested for germanium

implantation into crystalline silicon with a dose condition of 1×10^{15} ions cm^{-2} as shown in Figure 4.27.

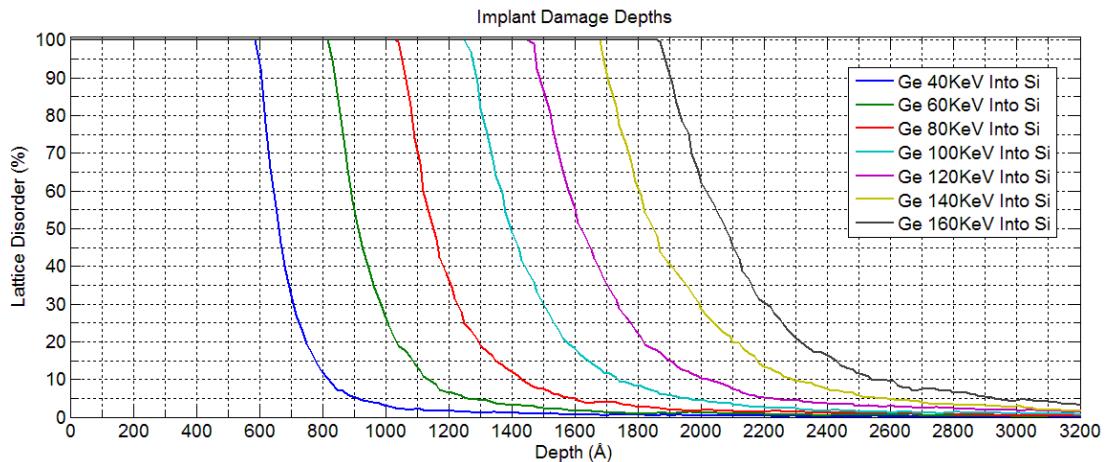


Figure 4.27 - Lattice disorder depths for a range of Ge implantation energies, all with a dose condition of 1×10^{15} ions cm^{-2}

Earlier in section 2.5.2.2 it was shown that a Δn of ~ 0.5 is achieved repeatedly for 80% lattice disorder, Figure 4.27 shows that at least 80% lattice disorder is achieved to the desired depth of 130nm with an implantation energy of 100keV. Now that the required implant energy has been established a KING 3D simulation can be performed to show the implant profile.

To aid in the analysis of the simulation data, Figure 4.28 shows a King 3D simulation with the key regions labelled in a manner consistent with this text.

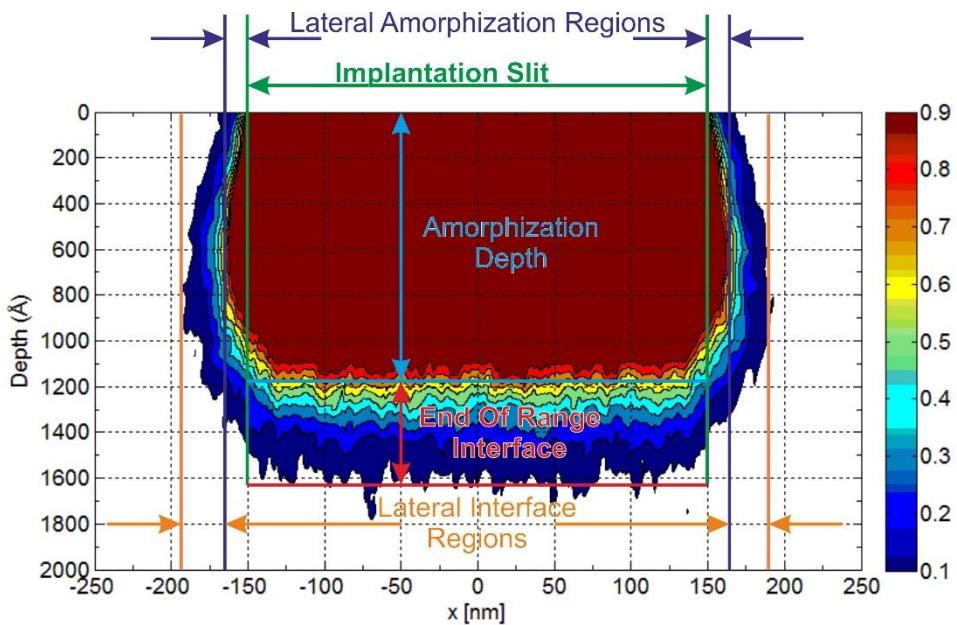


Figure 4.28 - Labelled KING 3D implant diagram (Ge into Si, 100kev, 1×10^{15} ions cm^{-2})

The implantation slit refers to the width of the gap in the mask for ion implantation, in this case the slit width is 300nm. Amorphization depth shows the thickness of the amorphous layer, while the lateral amorphization regions describe the amorphization which occurs laterally underneath the implant mask. Lateral straggling is typically associated with recoil collisions. Interface regions show the transition between fully amorphous silicon with a damage fraction > 0.8 and crystalline silicon which is shown as white with a damage fraction of 0. A damage fraction of 0.8 corresponds to 80% lattice disorder.

Figure 4.28 shows the implant profile for a 100keV implant of germanium into silicon with a dose of 1×10^{15} ions cm^{-2} implanted through a 300nm slit, this corresponds to a 600nm grating period with a duty cycle of 0.5.

At the widest point, 22nm of lateral amorphisation is observed, this will result in an increased grating duty cycle from the mask pattern. For a 600nm grating with a masked duty cycle of 0.5, this would result in a maximum device duty cycle of 0.57. The effective index change for the propagating optical mode at the maximum extent of lateral amorphisation however, will be very low with an effective index change of only 4.5% of the maximum effective index change observed within the grating. The effective index change reaches half of its maximal value at a lateral value of 14nm beyond the masked profile in either direction resulting in an effective duty cycle of 0.55. This shows the implanted grating will produce a duty cycle of less than 0.55 if the device is fabricated with a mask duty cycle of 0.5. Conversely, if the sample is not perfectly flat with respect to the ion beam, implant shadowing can occur. Implant shadowing will decrease the duty cycle observed. Hence, in this case a duty cycle of 0.5 strikes a balance between lateral amorphisation and implant shadowing effects resulting in a fabrication tolerant design. In this specific case, the effects of lateral amorphisation and implant shadowing are relatively small, however these effects may make small feature sizes such as those required for an apodized grating coupler exceedingly difficult to fabricate.

The final implantation condition to consider is the implantation dose, a lower dose offers faster fabrication times and hence cost savings. Higher implant doses can also increase the temperature required for subsequent annealing [162] which may be an

advantage or disadvantage depending on the application, higher annealing temperatures make the implanted grating more resilient to further fabrication processes whereas lower annealing temperatures make the devices easier to anneal. It was noted earlier that an amorphous layer with a refractive index change of ~ 0.5 corresponds to a lattice damage fraction of 0.8 in silicon, which has been verified by empirical results [42] [45] [46]. The data has also shown good agreement with damage simulations performed in King 3D. To investigate the critical dose of germanium required to amorphize silicon King 3D simulations have been performed for doses of 1×10^{14} ions cm^{-2} , 5×10^{14} ions cm^{-2} , 1×10^{15} ions cm^{-2} , and 5×10^{15} ions cm^{-2} as shown in Figure 4.29. The comparison clearly shows that a dose of 1×10^{14} ions cm^{-2} is not sufficient to achieve a continuous region with a minimum damage fraction of 0.8. Increasing the dose condition to 5×10^{14} ions cm^{-2} shows a continuous region of sufficient lattice disorder paired with a smaller level of lateral amorphization than the 1×10^{15} ions cm^{-2} condition initially considered, however the penetration depth is also reduced to 120nm which is insufficient. The amorphization depth could be increased for the given dose condition by increasing the implant energy, though this would in turn increase the lateral amorphization. It is also apparent that the size of the interface region is larger in the case of a dose condition of 5×10^{14} ions cm^{-2} when compared with larger doses.

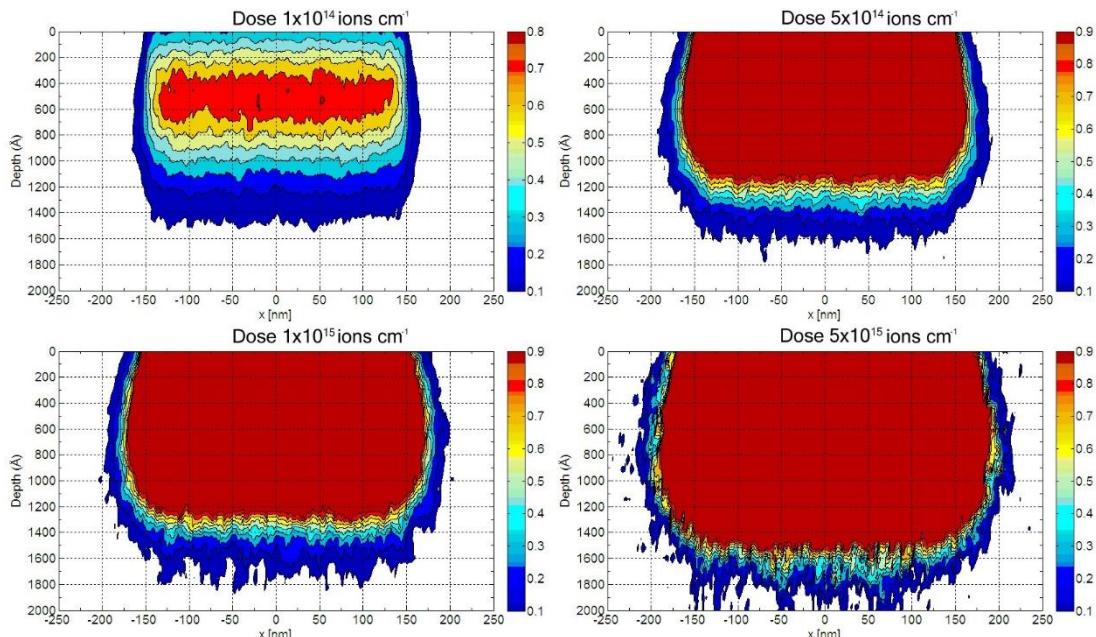


Figure 4.29 - Dose variations for 100kev germanium into silicon, the colour bar represents the damage fraction in which 80% lattice disorder corresponds with a damage fraction of 0.8

The comparison shows that increasing the implantation dose increases the lateral amorphization but reduces the size of the interface region. For the largest dose considered, 5×10^{15} ions cm^{-2} , lateral amorphization is double that of the 1×10^{15} ions cm^{-2} case. A dose of 1×10^{15} ions cm^{-2} offers a compromise, the impact of lateral amorphization is low enough that the duty cycle is not altered drastically whilst the interface region is constrained.

Implantation with heavy atoms which are required for amorphization can also result in significant sputtering effects. SRIM calculations show that statistically, each implanted ion will sputter 2.59 atoms from the silicon surface for a 100kev germanium into silicon implant. Using the dose condition of 1×10^{15} ions cm^{-2} shows that 2.59×10^{15} atoms cm^{-2} will be sputtered for the designed simulation parameters. The atomic volume of silicon is 5×10^{22} atoms cm^{-3} , raising this to the power of $2/3$ gives the number of atoms in a single atomic layer of silicon with a surface area of 1 cm^2 , which is 1.36×10^{15} . This shows the sputtering is limited to an insignificant 2 atom thick layer of silicon removed from the surface.

4.6 Conclusion

This chapter has taken the reader through the steps required to optimise an implanted grating coupler as a test point as well as the configuration of a bow tie test structure to ensure the device is successfully annealed. The waveguide width to ensure single mode operation is established as 400nm via effective index calculations to prevent modal interference within the device. An adiabatic dual stage taper with a total design length of 700 μm is discussed, along with an insight into where losses occur in a taper. The performance of both implanted grating couplers and surface relief grating couplers are analysed with a simulated maximum outcoupling performance of 45% and 55% demonstrated via FDTD simulations. Finally the implantation process is analysed, the implant mask is considered both on the merits of the ion stopping range, and risks associated with the removal of the implant mask. The implanted ion is discussed and the shortlist of xenon, germanium, silicon and tin are all considered with appropriate implant energies. Germanium offers the implant profile with the smallest lateral amorphization of the elements simulated, and a dose of 1×10^{15} ions cm^{-2} is shown to

offer the best trade-off between lateral amorphization and the size of the interface region with an insignificant amount of sputtering.

Chapter 5 - Fabrication

Gratings are very delicate structures which must be manufactured with very tight tolerances as every 1nm error in fabrication can generate errors in operational wavelength in excess of 2nm. There are several methods of fabricating gratings, for instance using holographic interference based lithography, standard deep UV photolithography or electron beam lithography. Holographic lithography is very limited for this application as the mask layer allows only one grating of a fixed periodicity and offers no significant advantages over photolithography for short gratings. Photolithography allows any period or shape to be used on a mask and allows variations of the design over the area of a chip, although accuracy may become an issue when considering the small feature sizes of the gratings simulated.

The 193nm deep UV process used imposes the following limits on feature sizes.

Feature	Minimum size	Guaranteed
Periodic structure	Pitch > 180nm	Pitch > 400nm
Holes	Diameter > 200nm	Diameter > 240nm
	Spacing > 120nm	Spacing > 160nm
Lines	Width > 120nm	Width > 200nm
	Spacing > 120nm	Spacing > 160nm
Trenches	Width > 140nm	Width > 200nm

The 248 nm deep UV process used imposes the following limits on feature sizes.

Feature	Minimum size	Guaranteed
Periodic structure	Pitch > 500nm	Pitch > 600nm
Holes	Diameter > 300nm	Diameter > 350nm
	Spacing > 250nm	Spacing > 300nm
Lines	Width > 250nm	Width > 300nm
	Spacing > 140nm	Spacing > 180nm
Trenches	Width > 250nm	Width > 300nm

Figure 5.1 - Process Limitations For LETI [163], period is referred to as “pitch”

An indication of the capability of deep UV lithography currently accessible for this project can be garnered from the minimum guaranteed and minimum allowable feature sizes offered at a commercial fabrication facility such as LETI, for 193 and 248nm deep UV lithography, the relevant data is shown in Figure 5.1. It is clear that the 600nm period required is on the limit of the technology capability of 248nm deep UV lithography, though the features required are readily achievable in 193nm deep UV lithography.

Photolithography is typically limited to a minimum feature size equal to the wavelength used for lithography, though resolution enhancement technologies such as

optical proximity correction and phase-shift masks allow for significant improvements in minimum feature sizes to be realised [164].

An alternative method of patterning a wafer is electron beam lithography. Electron beam lithography is far more accurate than 193nm photolithography, the only caveat is that it takes significantly more time to process a design and for larger devices stitching errors can also be a problem. Stitching errors occur when the beam window does not align perfectly between two successive exposures. Electron beam lithography writes a feature with a single beam of electrons allowing for excellent accuracy, though it also increases device cost due to the large amounts of time to expose a wafer.

5.1 Process flow

Complex fabrication processes increase the risk of failure. For a wafer scale testing component to be practical it must be high yield and simple to fabricate. Faulty test points could lead to optical circuits being marked as faulty in a situation where only the test point was defective, which would defeat the purpose of the wafer scale testing device.

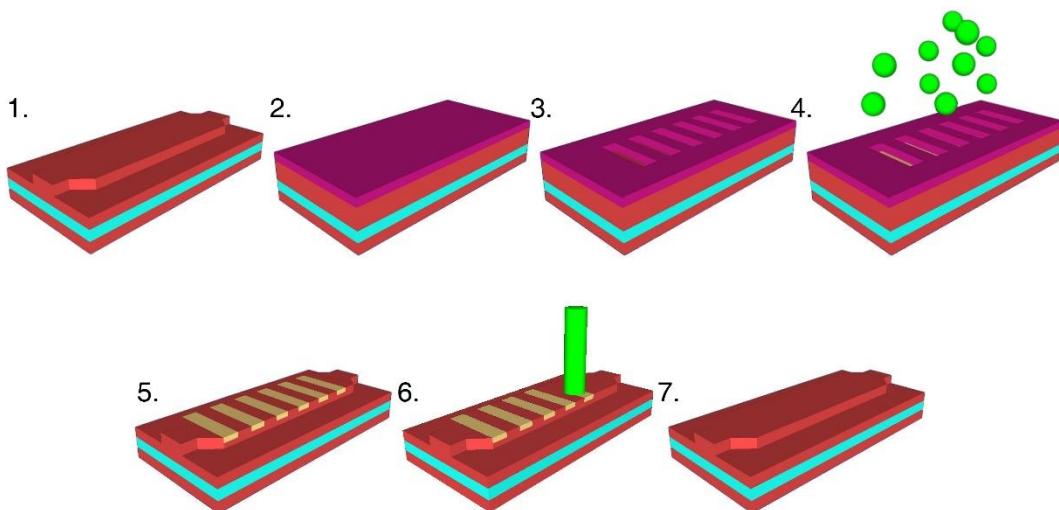


Figure 5.2 - Device fabrication process: 1. waveguide etch, 2. resist spin, 3. pattern and develop resist, 4. introduction of lattice disorder via Ge ion implantation, 5. resist removal and optical circuit testing, 6. laser annealing, 7. grating removed, waveguide operational regime

An outline of the fabrication process used is shown in Figure 5.2. Initially waveguides are fabricated, 220nm silicon strip waveguides were used for the devices in this work. Strip waveguides are defined using a silicon etch all the way to the buried oxide. The

waveguides were fabricated at the IMEC fabrication facility in Belgium. A deep 193nm UV photolithography process was used to pattern the waveguides and an inductively coupled plasma (ICP) etch was used for subsequent etch. To allow wafer sharing, the wafers were diced at this point though this is not necessary for the fabrication of the test points and hence is omitted from the general process flow in Figure 5.2. The waveguide sections comprised a 220nm thick silicon strip waveguide with a 400nm width to ensure single mode operation and the buried silicon dioxide layer had a thickness of 2 μ m. The waveguide grating width is increased to 10 μ m via a dual step taper to maximise the overlap integral between the fibre and grating modes, and to facilitate straightforward alignment between the optical fibre and silicon waveguide. The taper flare angle from 10 μ m to 3 μ m is set at 0.6° and the flare angle from 3 μ m to 400nm is set at 0.2° for adiabatic tapering.



Figure 5.3 - Leo Gemini 1530 SEM system at St. Andrews, Scotland

The samples are cleaned and primed before a ZEP 520A e-beam resist is spun onto the sample surface at 2000rpm to achieve a resist thickness of 500nm. The region to be implanted is sufficiently close to the sample centre to assume the resist thickness achieved is uniform and not affected by the edge bead around the small sample. Electron beam lithography was performed on the samples at St. Andrews University on a Leo Gemini 1530 SEM system as shown in Figure 5.3. To allow for inaccuracies in device fabrication and simulation, 5 different grating periods were placed onto the samples, 580nm, 590nm, 600nm, 610nm, and 620nm.

After exposure the resist is subsequently developed before the entire structure is implanted. Ion implantation was performed at The Surrey Ion Beam Centre. The structure was implanted with germanium ions using a dose of 1×10^{15} ions cm^{-2} to ensure amorphization [165]. The implantation energy can be varied depending on the required depth of amorphization, to achieve the 130nm depth required in this case, an energy of 100kev was used. Ion implantation is known to cause extensive cross-linking in ZEP resists, which makes it very difficult to remove. Cross-links can be either covalent or ionic bonds between resist polymer chains. Fully cross-linked polymers are almost insoluble in common solvents [158]. Structures have even been fabricated using resist which is described as having been cross-linked “to a different extent” [159]. In an attempt to mitigate cross-linking within the resist, the implant was performed with the beam current limited to $6.5\mu\text{A}$.

Following implantation the resist is removed using a 3 stage sequential solvent clean of acetone, isopropanol and deionised water for 2 minutes per bath, followed by a 10 minute O_2 plasma ash process. The oxygen plasma ash was performed using the standard recipe at 200°C with an oxygen flow rate of 800ml/min using an RF power of 800W. The amorphous grating can be tested an unlimited number of times during other manufacturing stages of the optical circuit. However, exposure to temperatures above 500°C for extended periods may reduce coupling efficiency [42].

After testing, the grating can be erased from the optical circuit via an annealing process, with an aim of returning the circuit to its peak performance, with no residual deficiency caused by the testing process. Annealing can either be carried out in an oven at a minimum temperature of 500°C or by a laser. Using oven annealing is not desirable as it heats the entire circuit, and the increased heat applied may cause damage to other fabricated devices and prevent successful operation of the whole circuit. Laser annealing offers an advantageous localised annealing process, which does not affect other fabricated devices. Further details on laser annealing can be found in chapter 6.

Chapter 6 - Localised Laser Annealing Results and Discussion

Implanted gratings for use with wafer scale testing take advantage of crystalline and amorphous allotropes of silicon offering a difference between their respective refractive indices. After the lattice is sufficiently damaged to generate a refractive index change, removal of the induced index change is achieved via the application of thermal energy. Applying thermal energy to the wafer can be achieved using an oven, at a risk to other devices in the optical circuit as discussed earlier. To eradicate this risk, and ensure the thermal energy is applied only to the vicinity of the grating to be removed, a laser can be used.

There are two key factors which must be addressed in order to achieve a localised anneal with a laser system, firstly the laser must be focussed to a spot no larger than the grating. The grating waveguide has a width of $10\mu\text{m}$ and hence the target is to apply a laser spot size that will deliver a spot with a $10\mu\text{m}$ diameter. The second challenge is to develop an alignment platform to enable the grating to be selectively annealed. High precision stages are commercially available to move a sample, however ensuring high accuracy laser alignment to a specific location on the sample can be less straightforward.

The investigations described henceforth aim to solve the pertinent issues, with an aim to anneal a single grating without affecting neighbouring devices, thus demonstrating local annealing.

6.1 248nm Pulsed Excimer Laser Annealing

Localised laser annealing of optical components has been attempted before for wafer scale testing, the results showing shallow implanted Bragg grating structures being annealed over a large area of $3\times 3\text{mm}^2$ [46]. This anneal is too general for wafer scale testing in a commercial environment as it possesses the negative attributes of an oven based anneal, since an anneal over an area of $3\times 3\text{mm}^2$ would affect a significant number of other devices, and the large instantaneous energy delivered by the laser is likely to prove catastrophic to the circuit as a whole. The catastrophic effects can be circumvented by confining the laser spot size to enable a more localised energy delivery system, with a target of annealing only a single grating at a time.

A Krypton fluoride Lambda Physik LPX 210i excimer laser operated at 10Hz with a pulse duration of 25ns and a wavelength fixed at 248nm has been used to maintain congruency with previous experiments into annealing of wafer scale testing devices. An additional lensing system has been utilised to reduce the target area irradiated by the laser system. The LPX 210i laser system is not targeted at accurate applications and preliminary results have shown at smaller sizes the irradiated spot is not circular due to the lensing system. In the smallest dimension of the annealed area, a diameter of 30 μm has been achieved; the results of this experiment are shown in Figure 6.1. These results show a trend between laser power and the heated spot size, an equation can be established to approximate the annealed spot size in the smallest dimension for a given input energy by applying curve fitting to the data. This yields equation 6.1, where D is the diameter in the smallest dimension in μm and E is input energy in mJ.

$$D = 55.283 \ln(E) + 226.34 \quad (6.1)$$

Heated spot size from DUV Laser

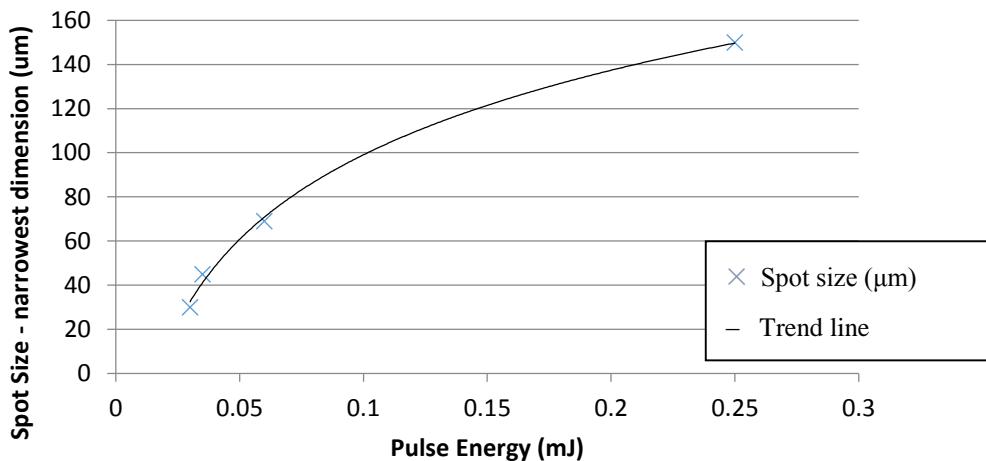


Figure 6.1 - Spot size vs applied energy at a wavelength of 248nm

The irradiated region observed in these experiments shows amorphous silicon Bragg gratings being heated beyond the temperature required for annealing, which leads to ablation of the material surface, the ablation profile demonstrating localised heating. Each individual anneal spans a single waveguide without affecting the adjoining waveguides which are spaced 25 μm apart.

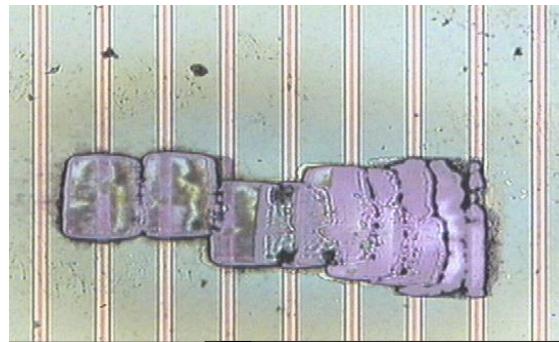


Figure 6.2 – Deformation caused by excimer laser irradiation

The ablation results in a visible spot as shown in Figure 6.2, which aids in alignment and measuring the heated region, though the power must be reduced in order to prevent the undesirable deformation and ablation of the waveguides.

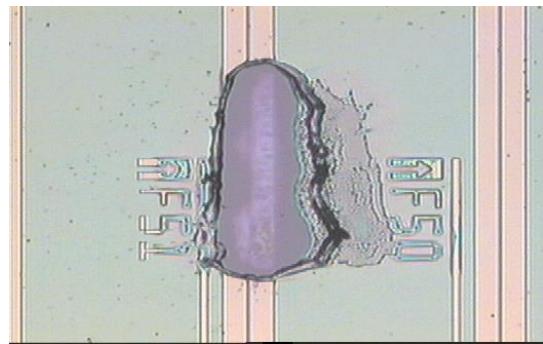


Figure 6.3 - Single grating annealing

Figure 6.3 shows the effects of laser irradiation with a spot formed with the lowest laser energy that can be obtained from this laser system, a laser energy of 0.03mJ. The dominant effect observed is still the undesirable laser ablation, though the size of the ablated region has decreased. Raman spectroscopy also suggests the formation of poly-silicon, which suggests the amorphous silicon has regrown to some extent. A comparison between the ablation effects seen in this experiment, and the ablation intentionally applied to a bulk silicon work piece, for an experiment into laser ablation drilling [166], is shown in Figure 6.4.

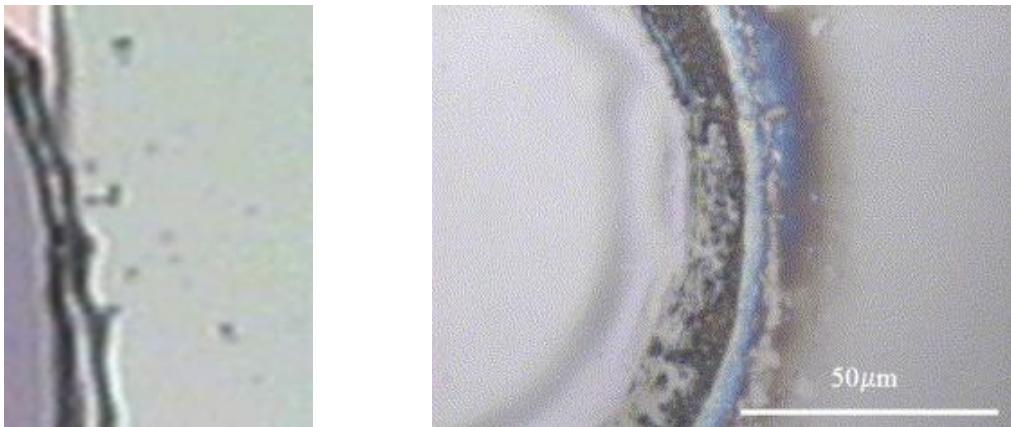


Figure 6.4 - Edge detail of DUV ablated silicon comparison – our result (left) and results from Choo et al [166] (right)

Figure 6.4 shows a comparable change in colour and topology between the intentionally ablated work piece and the irradiated amorphous grating. This provides further evidence of laser ablation and hence the instantaneous energy delivered by the laser is still too high, though the time average energy delivered per cycle (per 6 seconds) at the lowest laser energy tested is only $\sim 0.03\text{mJ}$. A detailed characterisation of silicon ablation with an excimer laser is given in [166]. A laser power that annealed the amorphous grating without ablating the surface could not be obtained in a small spot size from this laser setup, due largely to the high instantaneous energy delivered to the sample, which was exacerbated by the combination of the lensing system and short pulse duration.

Performing material analysis is essential before selecting a suitable laser. Ideally the wavelength selected will offer significantly more absorption in the amorphous material than crystalline silicon. Using a laser wavelength of 248nm for annealing brings a number of disadvantages to wafer scale testing in practical applications, dominantly in cost, optical hardware is more expensive at deep ultra violet wavelengths and it cannot be routed in a convenient manner using optical fibres.

6.2 Material Characterisation

To aid in the development of a more suitable laser annealing platform, the amorphous silicon region that was formed through ion implantation was characterised using spectroscopic ellipsometry. The characterisation data obtained can be used both to ascertain the depth of the amorphous profile and the absorption characteristics present

in the material formed by the ion implantation process, which was used to alter the refractive index.

Optical simulations of the grating coupler are based on an anticipated amorphous depth of 131nm based on KING 3D simulations and the refractive index of the amorphous silicon is expected to be 3.94 at 1550nm, in agreement with the results found in the literature for the implant dose utilised [77].

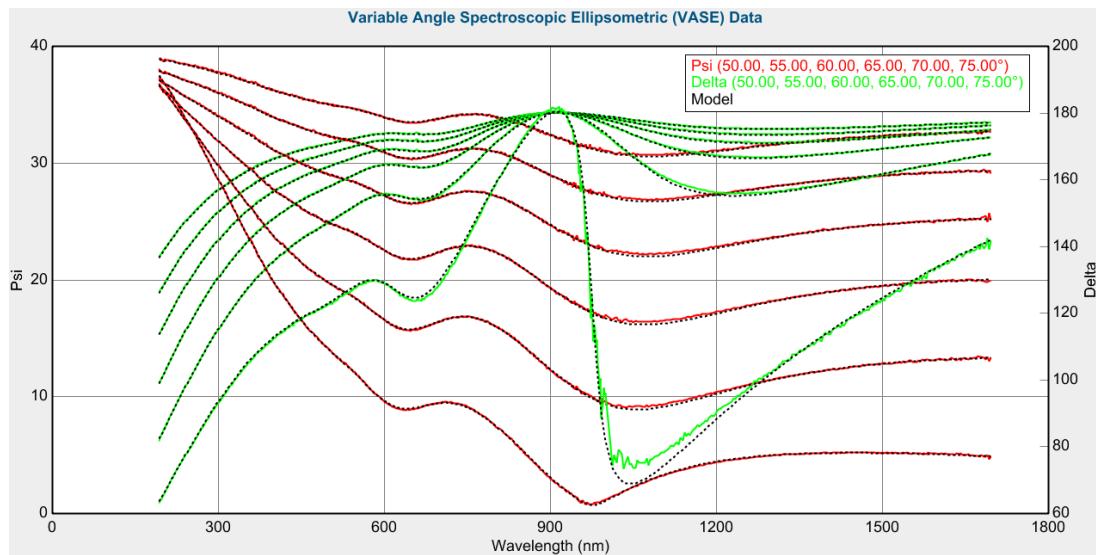


Figure 6.5 – Variable Angle Spectroscopic Ellipsometric data and fit for Ge implanted into silicon with an energy of 100kev and a dose of 1×10^{15} , where the dotted line represents the fitted data, the measured reflected amplitude is given by Phi and the measured reflected phase change is given by Delta. The average values for both Phi and Delta decrease as the measurement angle increases.

Ellipsometry was performed at 6 angles from 50° to 75° in 5° steps, the use of multiple angles ensures the data is verified against multiple measurements and allows the fit to be scrutinised more thoroughly to ensure an accurate result. The measured data was subsequently fitted with the CompleteEASE software package [167], using a B-Spline mathematical model to achieve data fitting. The measured data is shown by solid lines in Figure 6.5, the fitted data has also been superimposed as a dashed line to highlight the accuracy of the fit.

The model shows that the ion implantation depth simulations from the KING 3D software package [154] were accurate to within 1.6% in the samples tested. The amorphous layer thickness for an implant of 100kev at a dose of 1×10^{15} ions cm^{-2} ,

was shown to be 129nm by ellipsometry, which compares with a simulated result of 131nm.

The fitted results allow us to test the refractive index of the amorphous layer. The refractive index of the Ge implanted a-Si is shown in Figure 6.6, along with reference data plotted for Germanium, deposited a-Si and c-Si.

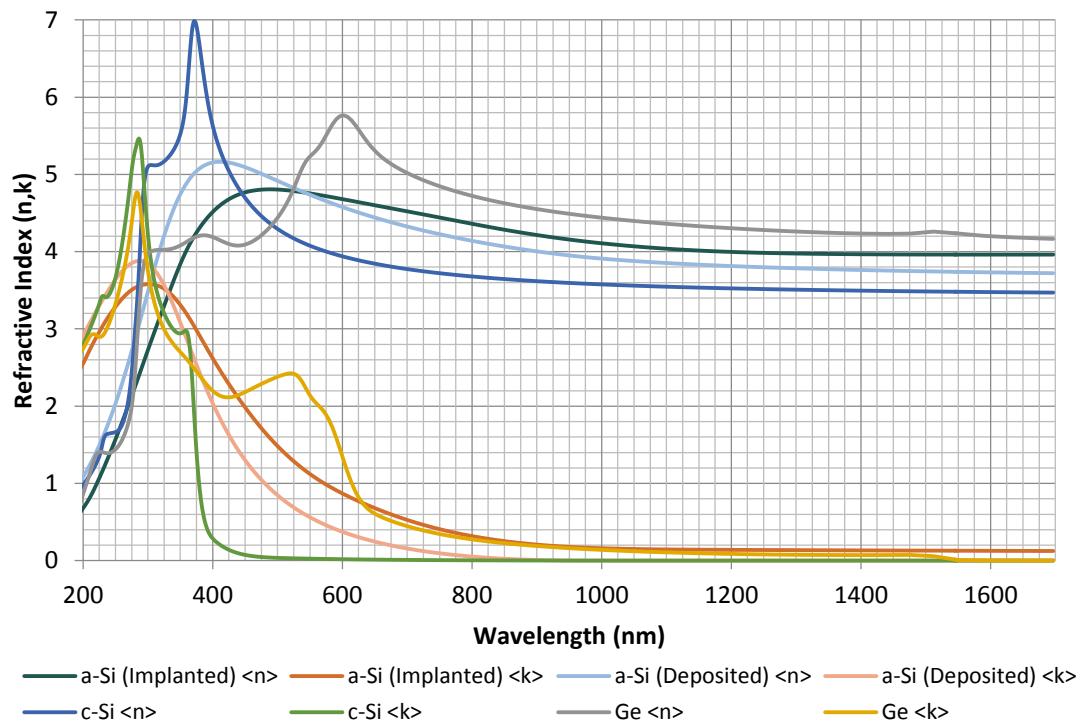


Figure 6.6 - Refractive index of ion implanted amorphous Silicon, compared with Ge, Si and deposited a-Si

The refractive index of the amorphous region formed by implanting a silicon substrate with 1×10^{15} ions cm^{-2} of germanium, accelerated by an energy of 100 keV, was found to be 3.96, which is in good agreement with previous work which showed a refractive index of 3.94 for similar implantation conditions [77]. The refractive index of the a-Si material formed through ion implantation is shown to have a slightly higher refractive index than that of the previous results for a-Si formed under similar implant conditions. This discrepancy could be caused by the improved measurement accuracy afforded by utilising a spectroscopic ellipsometer with analysis of measurements performed at multiple angles, or it may suggest a marginally higher defect density in the specific implanted case which, if true, would be due to the higher energy delivered from each

accelerated ion. Work by Heidemann suggests the refractive index of silicon can be raised to values as high as 4.1 by high dose ion implantation [68].

The complex part of the refractive index profile obtained can be used to find the wavelength dependant absorption coefficient using the Beer-Lambert law, which is given in equation 6.2:

$$\alpha = \frac{4\pi k}{\lambda} \quad (6.2)$$

Where α is the absorption coefficient, k is the complex part of the refractive index and λ is the free space wavelength. The absorption coefficient for a-Si (implanted) is shown in Figure 6.7, alongside reference data for c-Si [168], a-Si (deposited) [169], and crystalline Ge as tabulated at the University of Nebraska-Lincoln and shown in [170].

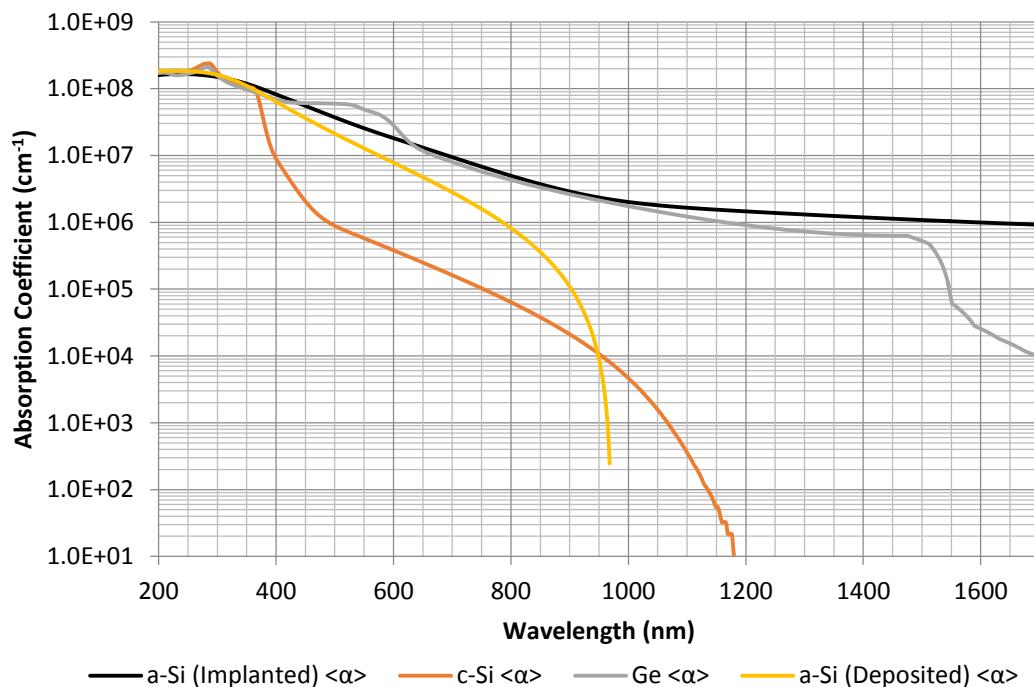


Figure 6.7 - Absorption coefficient data for deposited a-Si, Ge, c-Si, and Ge implanted a-Si

Figure 6.7 shows that at a wavelength of 248nm, all four materials compared have very similar absorption coefficients, most importantly implanted a-Si and c-Si with absorption coefficients of $1.65 \times 10^8 \text{ cm}^{-1}$ and $1.83 \times 10^8 \text{ cm}^{-1}$ respectively. The absorption coefficient for all of the compared materials is relatively high, though this is an unsurprising result due to the high energy per photon at a wavelength of 248nm.

Wavelengths above 400nm begin to display characteristics which are of interest for developing an annealing platform. At a wavelength of 450nm, c-Si shows more than an order of magnitude lower absorption coefficient than all of the other materials of interest. This means that when irradiating the sample, the implanted a-Si region will absorb significantly more energy than the c-Si material, resulting in the temperature increase being significantly greater in the amorphous regions, when compared with the c-Si regions irradiated by the same laser wavelength and power, which is conducive to annealing a-Si without damaging the c-Si. The absorption coefficient of silicon remains around an order of magnitude lower than the other materials analysed until 900nm at which point the absorption coefficient of a-Si (deposited) tends towards that of c-Si. However, Ge and a-Si (implanted) continue to display higher absorption coefficients than c-Si up to 1700nm, the end of the measurement range.

The data presented in Figure 6.7 is useful for assessing the wavelength of light best suited to the annealing application, however beyond that it highlights a clear difference between the absorption coefficient of the reference data for deposited a-Si and that of the a-Si material formed using ion implantation. There is a difference in the level of lattice disorder between the two materials, as inferred by the difference between the real part of the refractive indices. The results of Heidemann [68], suggests that the level of lattice disorder is lower in the case of deposited a-Si. This alone may present minor difference between the imaginary part of the refractive indices, however there is a clear mismatch between the general trends observed in the absorption profile data of the two materials. The only other apparent difference between the two materials is the content of impurities. Typically deposited a-Si becomes hydrogenated through the use of silyene (SiH_2) [171], trisilyamine (SiH_3) [172] or silane (SiH_4) [173] as a source of silicon in the deposition recipe. Though the level of hydrogen in the deposited a-Si data is not given [169], silane based films are expected to contain typically $\sim 10\%$ hydrogen as an atomic percentage, although slower deposition rate recipes using lower quantities of silane are able to reduce the hydrogen content present in the deposited film [174]. It can be deduced from Remes [175] (Figure 6.5), that the reference data is congruent with a-Si with hydrogen content of 10% or greater. The high hydrogen

concentration in deposited a-Si reduces the material density [169] and terminates a significant number of the dangling bonds [173], which in turn reduces the strength of the Bragg scattering from the crystal lattice [169] and hence increases the band gap of the material. As hydrogen pacifies the dangling bonds which are considered to be among the dominant mechanisms responsible for the refractive index change in amorphous silicon it is also unsurprising that the real part of the refractive index is lower in this case [66, 68].

Substitutional impurities with the same valency are known as iso-electronic. Iso-electronic impurities do not always give rise to localised electronic states, with a general exception if there is a significant difference in electronegativity between the elements, which does not exist between silicon and germanium. No occurrences of localised states are known for iso-electronic impurities within silicon or germanium [176]. This was thought to have removed any loss based restrictions from group IV elements in the design process, though this may have been naive. To establish with certainty, if there is a change in the absorption profile that is due to the use of an iso-electronic impurity in silicon introduced by implantation the germanium implanted silicon data must be compared with silicon which has been amorphized using a different implanted element. Silicon self-implantation offers a solution with no foreign elements involved, using a 100keV implant with a dose of 1×10^{15} ions cm^{-2} allows a region of amorphous silicon to be formed with lattice disorder above 80% equivalent to that of the Ge implanted Si. The amorphous layer was analysed using the same methods as discussed earlier in this chapter for the germanium implanted silicon. A 103nm thick amorphous layer was generated which begins 1nm below the silicon surface for the case of silicon implanted into silicon. The Ge implanted Si, and Si implanted Si show close agreement in the real part of the refractive index in the amorphous regions, which suggests both amorphous regions contain the same degree of lattice disorder.

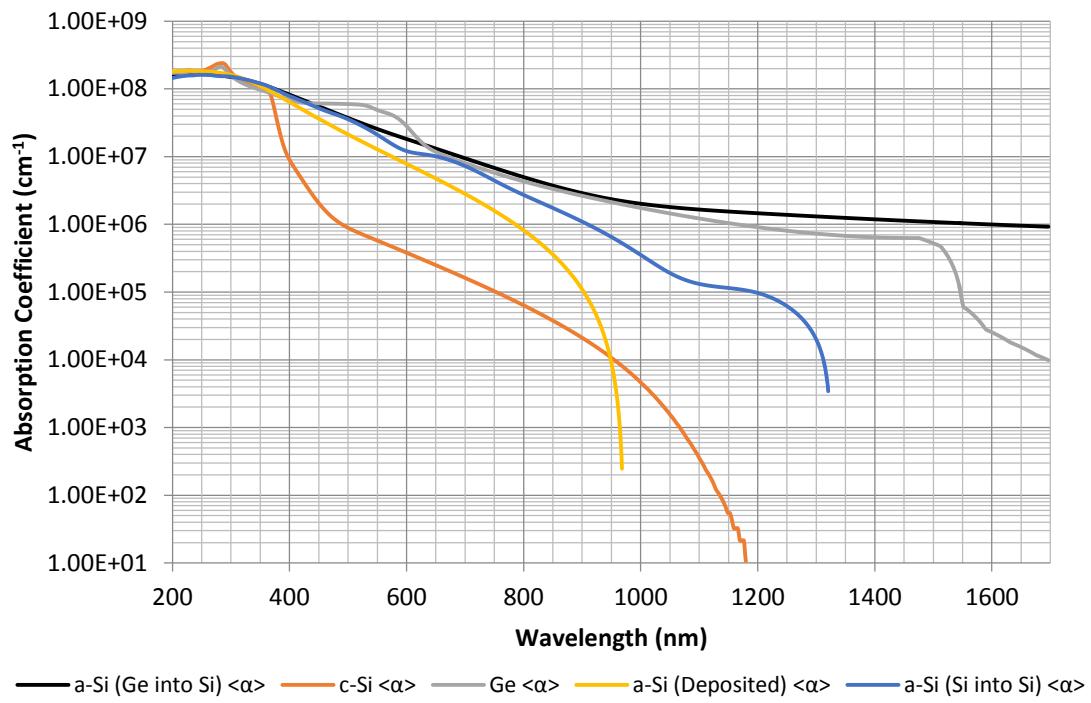


Figure 6.8 - Absorption Coefficient of Ge, c-Si and a-Si-formed using Ge implantation, Si implantation, and deposition

However, Figure 6.8 shows there is indeed a difference in the absorption coefficient between Si implanted Si and Ge implanted Si. It is difficult to ascertain with absolute certainty the mechanism causing a variation in the absorption profiles for different iso-electronic impurities without extensive analysis and a significantly larger pool of data, but the effects observed are, however, congruent with molecular vibrational modes. Vibrational modes can arise when there is a mass difference between the iso-electronic impurity and the host crystal, or with distortion of the lattice, both of which are present in the Ge into Si case while only the latter is true of Si into Si. The presence of vibrational modes exhibit strong effects in the optical absorption profile as observed in this data, though effects are not noted in the real part of the refractive index [176], which is in keeping with the observed data. Most importantly for the application in this work is that the imaginary part of the refractive index does return to closely match that of silicon as has been confirmed by ellipsometry in this work, along with other studies such as the results of Heidemann [68], which will prevent any significant residual loss from occurring after annealing.

6.3 488nm Continuous Wave Laser annealing

6.3.1 *Background*

The profile of implanted gratings couplers is more than 6 times deeper than the low energy implanted Bragg grating couplers [19]. Annealing these structures requires the delivery of more thermal energy which increases the risks of other effects associated with laser irradiation occurring, such as softening or ablation. Section 6.1 highlights that ablation is a significant risk when annealing with laser wavelengths of 248nm. Material analysis detailed in section 6.2, has shown that at a wavelength of 248nm the absorption coefficients of both amorphous silicon and crystalline silicon allotropes are very similar at $1.65 \times 10^8 \text{ cm}^{-1}$ and $1.83 \times 10^8 \text{ cm}^{-1}$ respectively. Similar material absorption coefficients result in stringent annealing requirements, which in turn requires a laser which is very stable with the capability of operating within very small power tolerances to enable the amorphous silicon to be fully annealed without any deformation of the silicon waveguide by processes such as ablation or softening of the crystalline silicon. The analysis shows that careful selection of the laser wavelength allows the laser power to be preferentially absorbed in the amorphous regions, allowing relaxed annealing conditions. At a wavelength of 488nm the absorption coefficient of amorphous silicon is 40 times greater than that of crystalline silicon, with absorption coefficients of $4.10 \times 10^7 \text{ cm}^{-1}$ and $1.02 \times 10^6 \text{ cm}^{-1}$ respectively. Instantaneous energy was also suspected to be a key factor in reducing the observed ablation. From the literature, it is worth noting that using lateral crystallization techniques, amorphous silicon films regrown using continuous wave lasers have demonstrated crystal sizes as large as $3 \times 20 \mu\text{m}$ [177]. Continuous wave lasers have been shown to produce larger silicon crystal grain sizes with fewer defects than those obtained by pulsed sources, resulting in higher quality material, which is attributed to the lower cooling rate after laser irradiation from continuous wave sources [177]. Thus a continuous wave source will allow for a qualitative improvement in recrystallization of amorphous silicon while simultaneously mitigating the risk of ablation of crystalline regions due to the significant reduction in peak laser power. The combination of reduced peak powers and preferential delivery of laser power to the amorphous regions will allow the developed annealing process to be more robust. Operating within the visible light spectrum also allows the use of cheaper optical hardware, as well as

offering the potential for annealing through thick layers of cladding or transmission of the annealing laser through an optical fibre.

6.3.2 Experimental Setup

Figure 6.9 shows the setup used for laser annealing of the implanted grating couplers, all of the major components of the setup are labelled with a key.

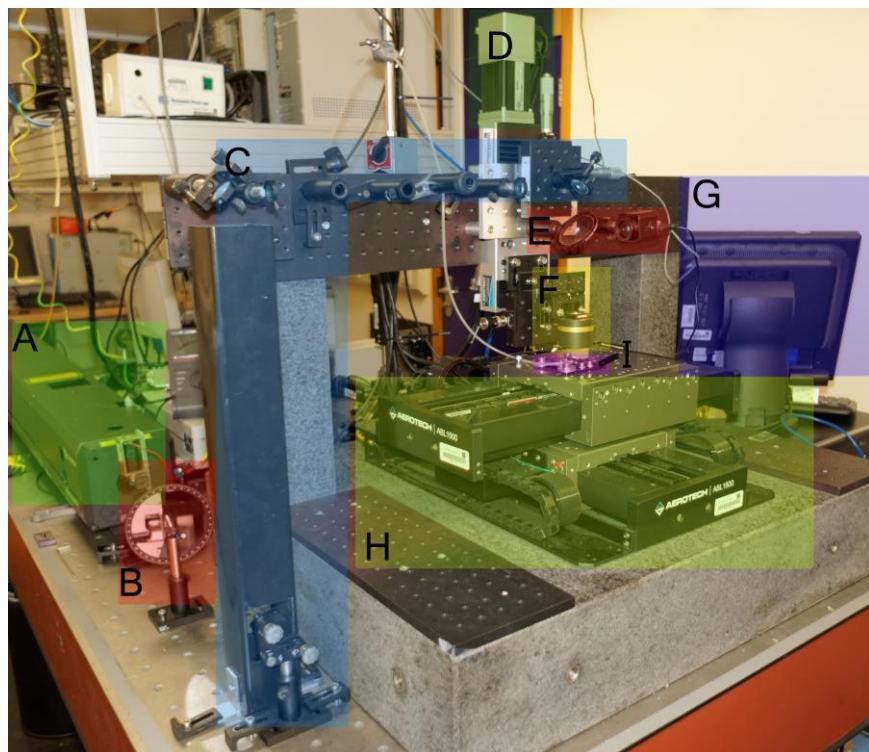


Figure 6.9 - Annealing setup

A) 488 nm Argon-Ion Laser	F) Mirror lens
B) Variable attenuator	G) Control computer
C) Beam steering equipment	H) Pneumatic XY stage
D) Lens adjustment motor	I) Vacuum sample mount
E) Beam splitter and sample alignment camera	

The experimental setup shown in Figure 6.9 is designed to deliver the laser power from a 488nm CW argon ion laser (A) to the amorphous grating coupler in a controlled and precise manner. The laser is used to recrystallize the amorphous grating coupler while the variable attenuator (B) provides fine control over the laser power which reaches the sample. This ensures successful annealing takes place without introducing undesirable effects such as laser ablation. The beam steering equipment (C) is implemented to provide greater flexibility in mounting the sample, enabling the sample to be mounted horizontally and thus removing any gravity related velocity variations in the sample movement, which may have been introduced if the sample were to be mounted vertically. The mirror lens (F) is used in conjunction with a stepper motor (D) to focus the light down to a small spot on the sample surface in order to minimise the region of the sample which is exposed to an elevated temperature. The beam splitter and camera setup (E) allows the laser spot to be observed on the sample before annealing, which enables positioning of the laser spot on the sample, it is important to note that the camera aperture must be covered during annealing to prevent damage to the CCD. The vacuum sample mount (I) holds the sample firmly in position while the sample is moved via the pneumatic XY stage (H). The position of the sample is computer controlled (G). The same computer also controls the vertical position of the mirror lens (F).

The sample mount is shown in greater detail in Figure 6.10, the sample can be seen with a small laser spot irradiating the sample. A small glass sample is used to ensure a good seal for the vacuum mount.

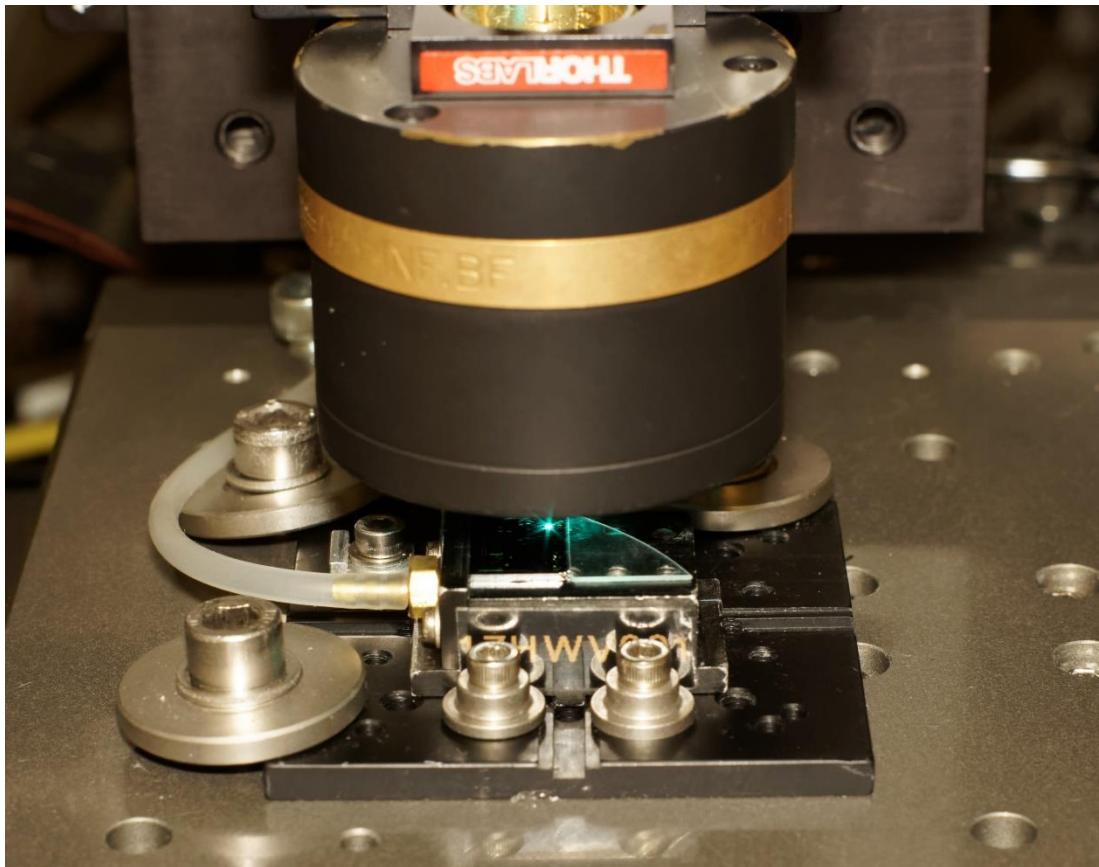


Figure 6.10 - Sample Mount on Vacuum stage

6.3.3 Preliminary Experiments and Calibration

Initially the sample was irradiated with a single laser spot to calibrate the threshold power which initiates damage in crystalline silicon. The laser was powered on and then immediately powered off, the results of this irradiation are displayed in false colour to improve the distinction between materials in Figure 6.11, black regions represent silicon, dark red is amorphous silicon and a pinky hue represents silicon dioxide. The mark observed in the centre of the $10\mu\text{m}$ waveguide and labelled A was formed using a short irradiation with a laser power of 500mW. This has heavily damaged the silicon in the centre. Interestingly a black halo has been formed around the burn, in this region the amorphous material has been recrystallized as confirmed by Raman spectroscopy. Further tests on a crystalline silicon waveguide showed powers in the region of 200mW do not damage the silicon. A 200mW laser irradiation was performed on the implanted grating sample, offset to the left of the initial irradiation and labelled B. The faded red in this region shows annealing has begun at this power, a longer annealing

time or marginally increased power may be sufficient to produce acceptable annealing conditions.

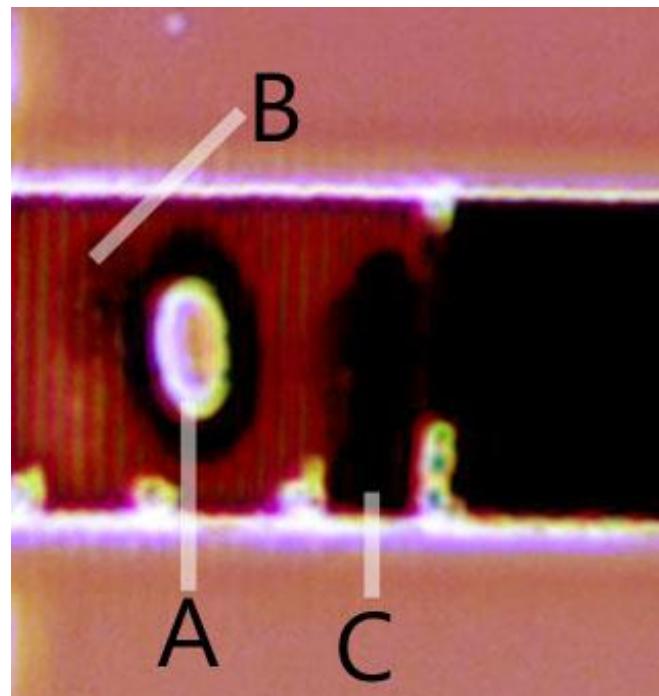


Figure 6.11 - Grating anneal test piece

A laser pass was performed at $10\mu\text{m/s}$ over a silicon waveguide sample, using a laser power of 200mW as shown in Figure 6.12 (in real colour). At this speed the laser power has exceeded the ablation threshold for crystalline silicon. The test is also a reminder of another important factor when developing an annealing process for silicon, its relatively high thermal conductivity of $149\text{ W m}^{-1}\text{ K}^{-1}$. A high thermal conductivity means that the parameters of the annealing process critically depend on the dimensions of the silicon region device being annealed. Conditions suitable for annealing a $10\mu\text{m}$ wide grating structure may evaporate a $2.5\mu\text{m}$ wide waveguide section as shown in Figure 6.12, due to different rates of heat dissipation. For this reason, annealing conditions are strongly device specific.

A scan rate of $10\mu\text{m/s}$ combined with an annealing power of 180mW was found to anneal the amorphous silicon regions. A single pass with these conditions is shown in Figure 6.11, labelled C. The single laser pass with this system highlights the annealing capability which can be achieved, the single pass has been stopped before the edge of the waveguide and the width of the annealed region is shown to be $1.45\mu\text{m}$. This is far

beyond the initial expectations set out for the annealing process, rather than annealing a single grating coupler, it is feasible to erase ~ 3 periods anywhere along the grating or perhaps more significantly a single period from one end of the grating by only overlapping a small portion of the laser spot with allowing the outcoupling performance of the grating to be gradually reduced while the transmission is gradually increased. The annealed linewidth of $1.45\mu\text{m}$ is in good agreement with the characterisation of the spot obtained from a beam profiler, which showed the spot size to be $1.5\mu\text{m}$. This also indicates that the annealing is localized to within the laser spot.

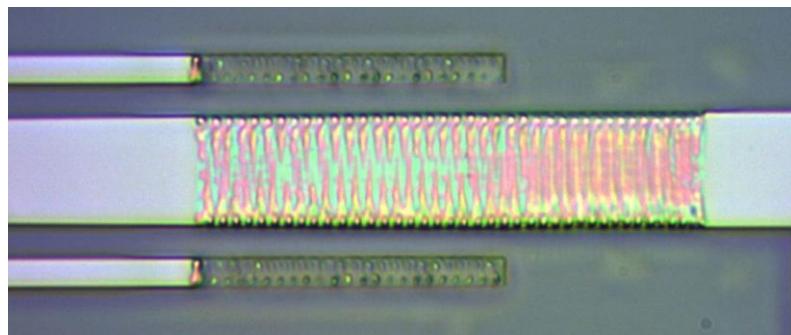


Figure 6.12 - Laser passes at 200mW with a scan speed of $10\mu\text{m/s}$

It has been discussed that for a wafer scale testing system to be viable, the locality of the annealing process is critical. The high temperatures required for the recrystallization of silicon would be detrimental to many fabricated optical devices such as modulators, photodetectors or metalisation layers. The localised anneal shown here demonstrates that annealing a single grating is well within the capabilities of this laser system.

6.3.4 Grating Coupler Annealing Results and Discussion

A set of conditions suitable for locally annealing an amorphous grating coupler have been established in the previous section. For the 488nm continuous wave laser used, when combined with a scan speed of $10\mu\text{m s}^{-1}$, a laser power of 180mW has been shown to anneal the amorphous material without any obvious detriment to the surrounding crystalline regions. Measurement of the laser profile shows a spot diameter of $1.5\mu\text{m}$ and the heating has been shown to remain localised to within the spot for the given laser parameters. In order to establish a regular crystal growth direction, the laser irradiation was performed with a raster scan configuration to anneal the grating, which ensures a regular crystal growth direction [178]. For practicality the

sample was moved with respect to the laser, due to the complexity associated with translating the position of the laser spot accurately. The annealing laser was positioned perpendicular to the waveguide and the path followed by the laser for annealing extended 20 μm beyond either side of the waveguide. It is necessary to extend the laser path to prevent variations in velocity that would otherwise lead to variations in laser exposure which may occur over the waveguide area. If the laser did not travel the extra distance, additional laser power would be delivered to the waveguide during periods of acceleration and during the dwell period, when the annealing laser changes direction to follow the raster pattern. It may be possible to optimise the annealing process such that the 20 μm exposure extending beyond the grating coupler to be annealed could be reduced or even removed by utilising a beam stop to block the laser beam during a change of velocity or direction. The separation between adjacent scans must be sufficiently small to ensure a continuous region of silicon regrowth, a separation value of 0.5 μm was selected, though this may make the annealing process marginally slower the 1 μm overlap between successive scans ensures each amorphous region receives multiple laser passes to minimise the risk of any level of silicon amorphization remaining after the anneal has been performed.

Images of the implanted region were taken with an optical microscope before and after a successful grating anneal and are shown in Figure 6.13 and Figure 6.14 respectively.

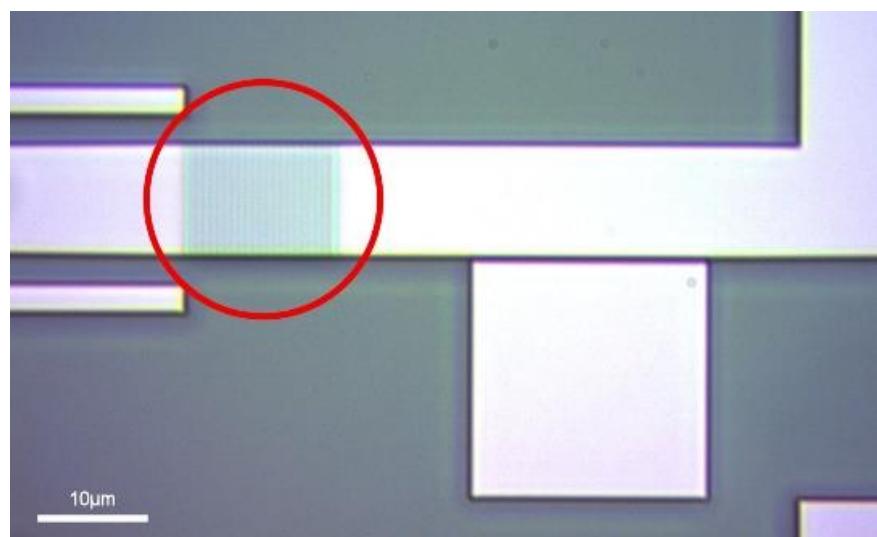


Figure 6.13 - Microscope image of an implanted grating before annealing.

Before annealing the grating coupler is clearly visible in Figure 6.13, after annealing the grating contrast is significantly reduced (but not removed) as shown in Figure 6.14.

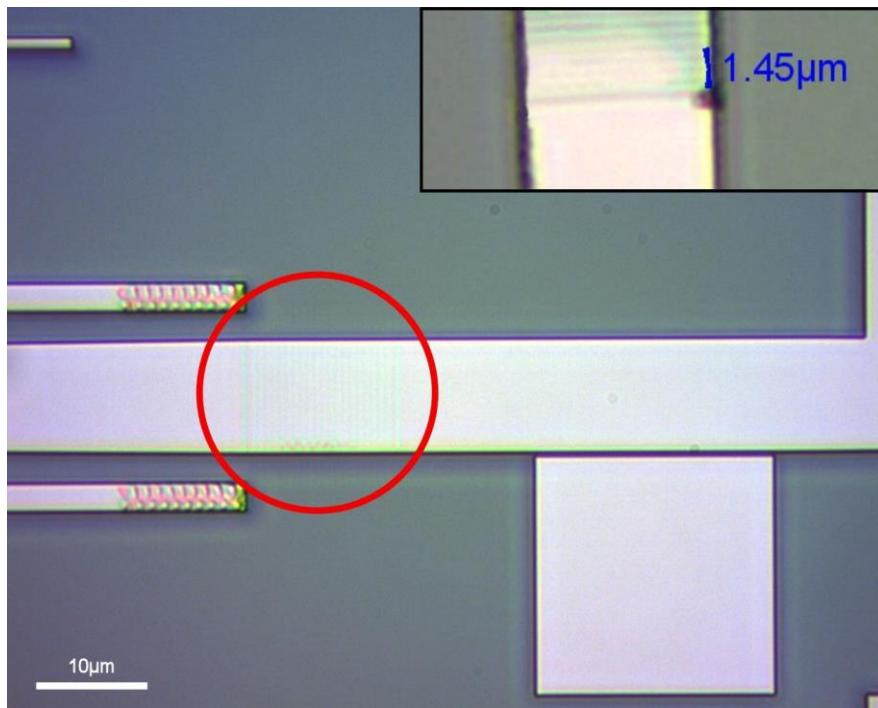


Figure 6.14 - Microscope image of an implanted grating after annealing. The inset image is a demonstration of the locality of the anneal with a single laser pass showing an annealing linewidth of 1.45μm.

The reduced grating contrast may be an indicator that the lattice disorder has been reversed to a degree, but the parameters may have fallen short of a complete anneal, and may correspond to the stable material state referred to by Heideman [68] as a-Si(II). To confirm the allotropy of the material both before and after annealing Raman spectroscopy was performed and compared with the same measurement taken before annealing, the results of this material interrogation are shown in Figure 6.15.

Characterisation data for Raman spectroscopy performed on amorphous semiconductors can be found in [179]. This data is essential for accurate identification of the allotropy of the materials present. A sharp peak is observed in Figure 6.15 at 520 cm^{-1} both before and after annealing, showing a contribution from crystalline silicon before annealing. A crystalline peak is observed in the amorphous data due to the Raman spot size being slightly larger than the width of an amorphous grating period region (300nm), as well as the 633nm Raman laser penetrating $\sim 3\mu\text{m}$ in to crystalline silicon, which is deeper than the 130nm implanted region.

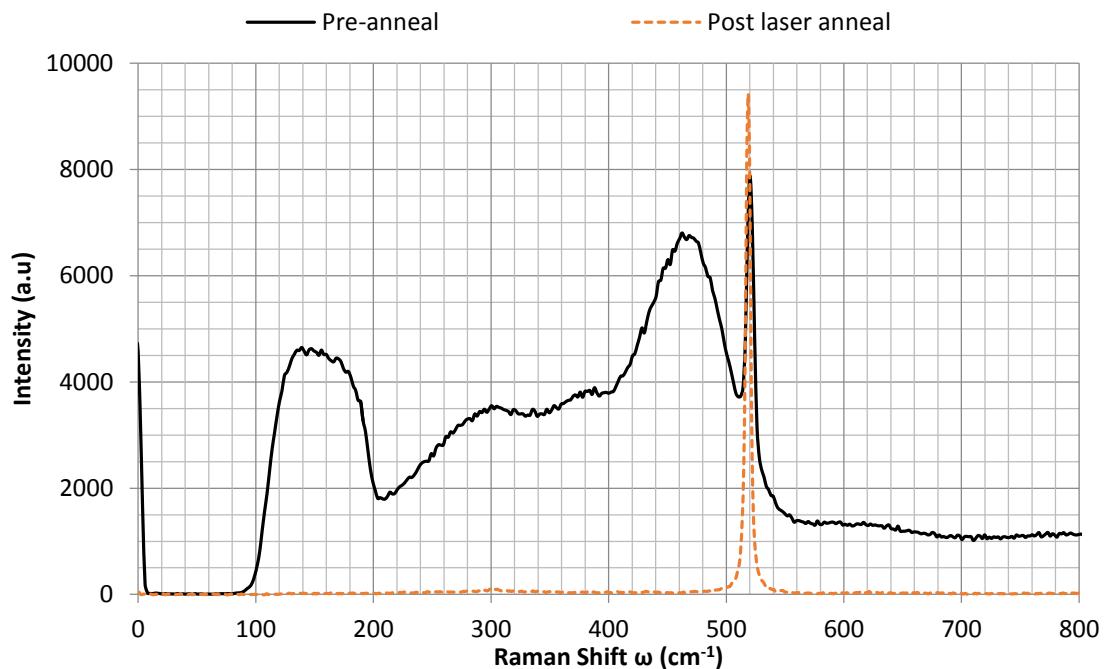


Figure 6.15 - Raman spectra of Ge implanted silicon before and after annealing

Comparing the measured Raman spectra with characterisation data shows that amorphous silicon had successfully been formed prior to laser annealing, which is confirmed by the broad peaks observed at 140 cm^{-1} and 480 cm^{-1} . The same characterisation data also highlights an absence of rounded peaks at 75 cm^{-1} or at 270 cm^{-1} , which if present, would represent the formation of amorphous germanium, and this gives strength to the conclusion that the quantity of germanium as an atomic percentage is insignificant. This is not surprising as based on the implantation conditions the atomic percentage of germanium present in the implanted region of a single grating period is only 0.045% for a $10\mu\text{m}$ wide, 600nm period grating with a 0.5 duty cycle. After annealing diffusion effects can make the localised atomic percentage of germanium up to 4 times lower.

Interrogating the same grating region with Raman spectroscopy post laser annealing shows only a single noticeable peak at 520 cm^{-1} exists. Upon close inspection a small germanium peak is observed at 302 cm^{-1} in the post-annealing Raman spectra, however the small concentration present makes it difficult to observe on a graph. The germanium and silicon intensity peaks are measured to be 112 and 9431 respectively. This demonstrates the amorphous regions have been successfully annealed and hence the retained low contrast grating profile observed in Figure 6.14 is not caused by

insufficient annealing parameters. A Voigt fit can be applied, which reveals a Lorentzian linewidth of 4.3 cm^{-1} for the annealed material, compared to 2.7 cm^{-1} for single crystal silicon. This shows that the annealed silicon is in fact polycrystalline, which is associated with higher waveguide loss values than single crystal silicon material. It is possible that the annealing process can be further optimised to improve the quality of the regrown material, though this is not of primary concern as Kwong et al have shown losses of 0.56dB cm^{-1} and 0.31 dB cm^{-1} for $10\mu\text{m}$ waveguides in polycrystalline silicon and crystalline silicon respectively which suggests very little bulk absorption in the polycrystalline case [180]. It has also been shown that the losses in polycrystalline silicon waveguides are not greatly dependant on grain size for grains in the range of $0.1\text{-}0.4\mu\text{m}$ [181], as the implanted regions in this case span only $0.3\mu\text{m}$ grain size is unlikely to make significant contributions towards the optical loss.

There are no clues in the data obtained by Raman spectroscopy as to the cause of the residual low contrast grating observed in Figure 6.14, which suggests that the material composition of the waveguide is not the cause. This suggests the observed low contrast grating may be due to surface effects. Atomic force microscopy was carried out to assess the effects of surface roughness and any potential of a periodic surface profile.

Figure 6.16 shows the atomic force microscopy scan, from which a thin film is seen to be remaining on the waveguide surface which has the same grating period and shape as the ZEP resist used to mask the implantation process. This suggests that the low contrast grating observed after annealing is due to a thin layer of hardened ZEP resist. ZEP has been shown to present a significantly increased etch resistance after exposure to heavy ion irradiation [182] due to cross-linking.

This disproves the hypothesis put forward that the resist below the surface could be removed using solvents, and in turn lift off the cross-linked resist. This has not prevented successful optical results from being obtained in this work, though future devices must look to deliver an adapted and improved implantation masking process. A more robust solution is envisaged by using a sacrificial thin film of silicon dioxide. 20nm of silicon dioxide between the waveguide and the ZEP resist layers would be sufficient to buffer the waveguide surface from the hardened resist caused by the harsh implantation conditions. The thin layer of silicon dioxide could then be removed using

a slow and precise etch, isotropic etches developed for inductively coupled plasma tools may offer enhanced protection against undercutting in the case of silicon strip waveguides.

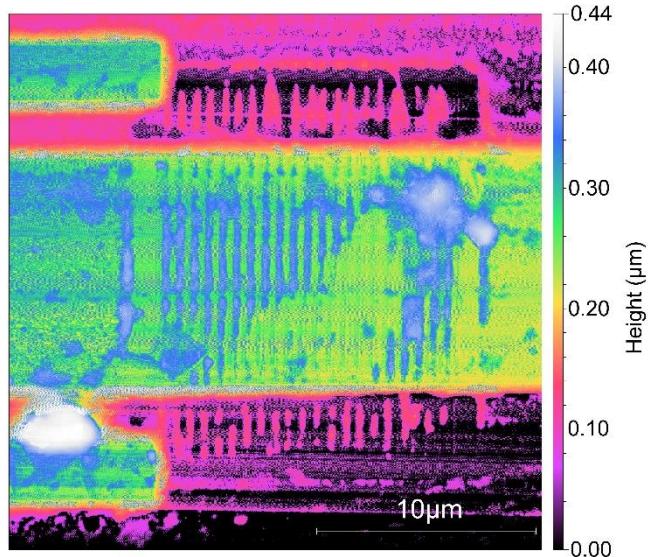


Figure 6.16 – Surface profile of annealed implanted grating coupler. Original implant was germanium at 100keV, 1×10^{15} ion cm^{-2}

6.4 Conclusion

This chapter has provided a comprehensive discussion of localised laser annealing. The advantages of localised annealing, such as zero interaction with other optical devices, have been highlighted and the downside of increased complexity can also be inferred from the details in the chapter.

Localised annealing using a pulsed laser at 248nm, as used previously for a large area (3mm^2) annealing of wafer scale testing devices has been attempted, though successful localised annealing using this system was thwarted by the prevalence of material ablation even at the lowest pulse energies that could be obtained from the system. The observed ablation is due to the high instantaneous energies from the system, which is compounded by similarities between the absorption coefficient of crystalline and amorphous silicon allotropes at this wavelength.

Variable angle spectroscopic ellipsometry has been performed to provide an insight to the behaviour of silicon and amorphous silicon at different wavelengths, and aid in the selection of a suitable laser wavelength for localised annealing. The real part of the

refractive index has been shown to be marginally higher at 3.96 than the predicted value of 3.94, although a small discrepancy in the refractive indices is to be expected, due to the lower implant energies used to obtain the predicted index data. The profile of the absorption coefficients was calculated from the complex part of the refractive index. For wavelengths above 450nm, the absorption coefficient of crystalline silicon was shown to be at least an order of magnitude lower than amorphous silicon formed using germanium implantation which is highly beneficial from the perspective of annealing of ion implanted grating couplers. The absorption coefficient is also noted to be significantly different based on the fabrication method used, with deposition, silicon and germanium implants considered.

Finally localised laser annealing has been demonstrated using a continuous wave laser at a wavelength of 488nm. The laser wavelength selected allows for an improved power tolerance, which works synergistically with the significant reduction in instantaneous power, compared with the previous 248nm pulsed laser, to prevent ablation and deliver successful laser annealing. At a speed of $10\mu\text{m s}^{-1}$ a laser power of 180mW was able to successfully anneal the grating, and the annealed line can be as narrow as $1.45\mu\text{m}$ which demonstrates successful localised annealing. Furthermore the change in material allotropy has been confirmed by Raman spectroscopy.

Chapter 7 - Optical Performance Results and Discussion

7.1 Experimental Setup

Figure 7.1 shows the setup used for optical characterisation of implanted grating couplers, with all of the major components of the setup labelled with a key.

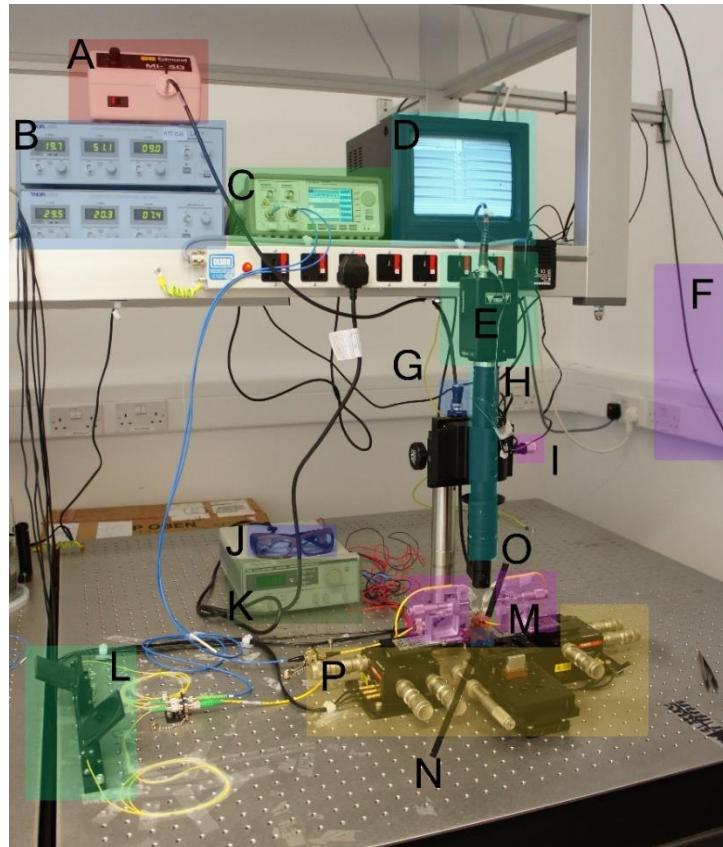


Figure 7.1 - Characterisation setup

A) Light box	J) Safety glasses
B) Piezoelectric controller	K) Thermoelectric cooling controller
C) Agilent 1550nm laser and photodetector package	L) Polarisation rotator
D) Optical chip layout monitor	M) Fibre angular alignment arm
E) Camera	N) Thermally controlled stage
F) GPIO computer interface lead	O) Device under test (Enlarged in Figure 7.2)
G) Camera focus	P) Positional alignment XYZ stages
H) Camera lens	
I) Horizontal camera adjustment	

The same equipment configuration is used to characterise both etched and amorphous grating couplers. The device under test (O) is mounted on a thermally controlled stage (N) which allows the sample temperature to be defined via the thermoelectric cooling controller (K). Fibre arms (M) can be positioned above the correct grating coupler using the camera (E) with a lens (H) used to magnify the chip layout for display on the monitor (D), illumination of the chip is provided from a light box (A), which is essential for a clear image. Once the course alignment of the fibres has been accomplished via the camera, accurate positional alignment can begin with donning the safety glasses (J), and turning on the laser (C). Alignment can then be achieved by adjusting the XYZ stages (P) to maximise the power reaching the photodetector (C). Once alignment is maximised, the polarisation controller (L) can be adjusted to ensure TE polarisation reaches the grating, which ensures maximum power. The alignment can subsequently be perfected by using piezoelectric alignment (B). Once optimal alignment has been obtained, a laser scan can be run using the computer (not pictured), which is interfaced via the GPIO (General Purpose Input/Output) lead (F). This records the device characteristics over a range of wavelengths.

The device under test, sample mount and fibre alignment arms are enlarged in Figure 7.2 for clarity.

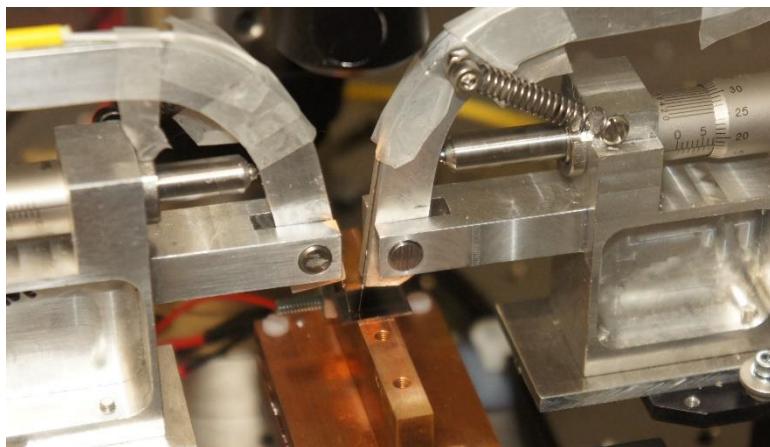


Figure 7.2 - Optical coupler sample configuration

7.2 Device optical characterisation

The implanted grating couplers were characterised using a tuneable wavelength source, and the wavelength of the laser was adjusted in steps of 25pm, whilst the power transmitted through the system was recorded. The optical characteristics of the

measurement setup were removed by normalising all of the results to a transmission measurement which used an optical fibre to bypass the grating couplers and optical device under test.

The implanted couplers were measured with a fibre at a 17° angle of incidence to the coupler, the angle is used to minimise back reflection and maximise power throughput for the designed structures. Five variations of the grating were tested in total with grating periods of 580nm, 590nm, 600nm, 610nm, and 620nm. All structures used a mask duty cycle of 0.5 with a ZEP resist implant mask. Surface relief grating couplers were also designed and fabricated alongside the implanted couplers, with identical waveguides and taper structures for use as a comparison to the implanted couplers. The period used for the surface relief gratings was 700nm and the etch depth used was 70nm, which corresponds to an outcoupling efficiency of 52% in simulations.

The efficiency of a single surface coupler is obtained by measuring a structure with a surface relief grating coupler for both the input and output coupler and dividing the result by 2. This method is only possible because the taper and waveguide section between the couplers are assumed to be lossless. The single mode waveguide is only $200\mu\text{m}$ long, but is required to ensure only the fundamental mode propagates through the device and to ensure the grating couplers are physically separated sufficiently as to allow measurement. The taper has also been designed to be sufficiently long to assume its loss is negligible hence the total loss measured can be assumed to be the loss contribution of the 2 surface relief couplers alone. Dividing this response by 2 gives the response of a single etched coupler. Measuring the same structure with the output surface relief coupler replaced by an implanted output coupler and subsequently subtracting the known value for a surface relief coupler results in the transmission response characteristics of a single implanted coupler. Figure 7.3 shows the transmission characteristics of a single surface relief grating coupler and a single 600nm period variant of the implanted grating coupler obtained using this method.

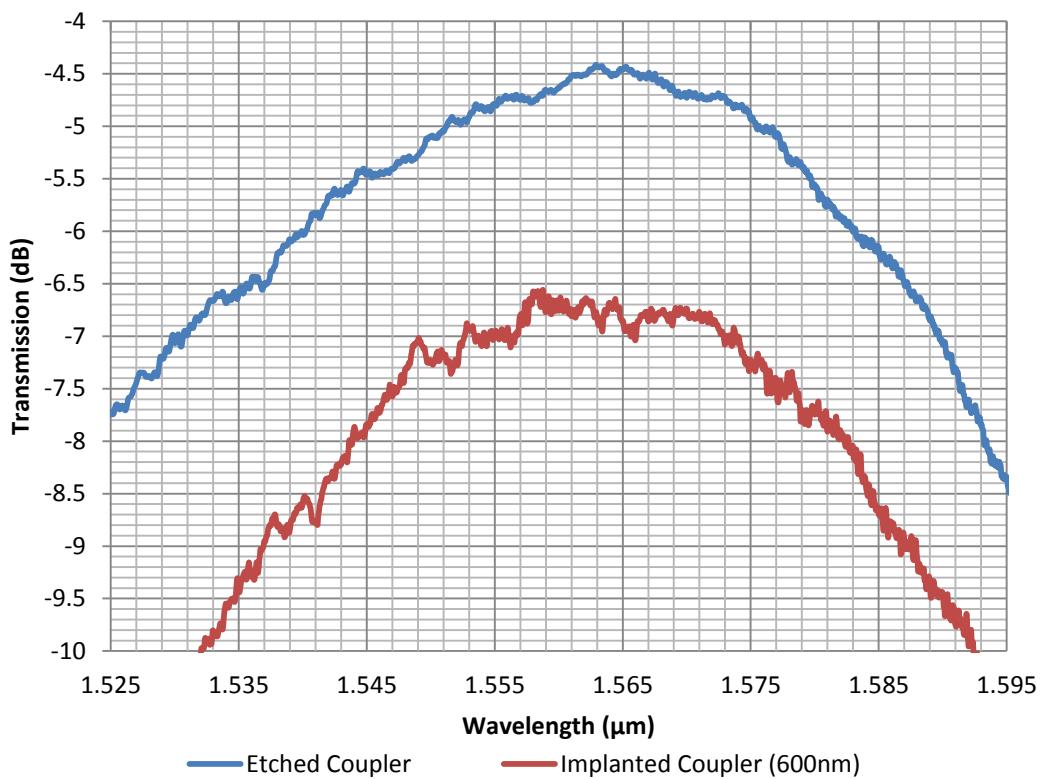


Figure 7.3 - Transmission characteristics of an implanted grating coupler and a surface relief grating coupler

It is clear from Figure 7.3 that the implanted coupler does not achieve the same output efficiency as its etched counterpart with a coupling loss of -4.5dB and -6.6dB for the surface relief and implanted couplers respectively. Interestingly at the peak of the output performance (within 0.25dB of the maximum) the implanted coupler displays a wider bandwidth than the surface relief grating coupler, with peak performance bandwidths of 16nm and 8nm respectively. Typically the performance metric used for grating couplers is the bandwidth at 1 dB below peak performance. The 1 dB bandwidth of the implanted and surface relief couplers are almost identical at 32nm and 30nm respectively. A 1 dB bandwidth of 30 nm is comparable to uniform surface relief gratings published in the literature [47, 51]. The results from interrogation of implanted couplers designed with different grating periods is shown in Figure 7.4. The results show different peak wavelengths for each period as would be expected. Simulated results show that the peak performance is at a period of 600nm, however the 590nm period demonstrates better experimental performance than both the 580nm and 600nm period. This shift in optimal grating period can be attributed to the small discrepancy in refractive index change. Simulations were performed using the

assumption that the refractive index in the implanted region was 3.94 as measured by Loiacono for similar conditions [77]. In this work the implant conditions use the same dose, but a higher implant energy. In this work the implanted region exhibits a refractive index of 3.96, simulations in Lumerical's FDTD package showing that an increase in the refractive index of 0.02 in the implanted region results in a change of 0.5° in the coupling angle for peak performance, which explains the small change in optimal period. The relationship between coupling angle and period was shown earlier in equation 2.15.

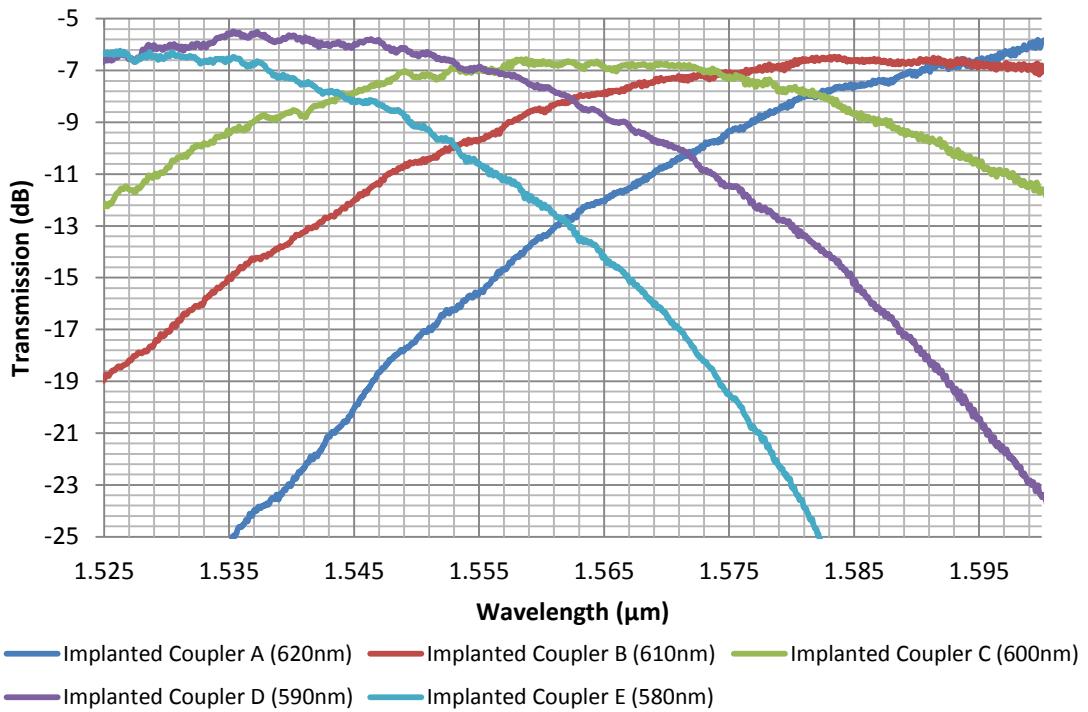


Figure 7.4 - Performance of implanted grating couplers at different central wavelengths

This shows the implanted grating couplers perform comparably with surface relief gratings as expected. The Δn of 0.48 which is introduced by the amorphous to crystalline interface is considerably lower than that of the silicon to air, with Δn of 2.48. The reduced index contrast reduces the coupling strength of the grating and in an attempt to compensate for this the amorphous region is made almost twice as deep as the comparable etched region, which maximises the effective index contrast. This results in the performance of the implanted coupler being only 1dB lower than the surface relief counterpart. The discrepancy between the expected refractive index change and the actual refractive index change produces a small shift of $\sim 7\text{nm}$ in the central wavelength of the grating, though the design could easily be adapted in a

subsequent device run by simulating the structures with a refractive index of 3.96 in the amorphous regions instead of the previous value of 3.94.

Raman spectroscopy has been used to show that the amorphous silicon regions have been successfully regrown to poly-crystalline silicon as shown and discussed earlier in section 6.3 demonstrating that the amorphous regions have been removed from a materials perspective. To demonstrate a successful device, ultimately it is necessary to show that the optical grating effects have been removed from the waveguide.

To demonstrate annealing from an optical device perspective, the bow structures shown earlier in Figure 4.1 are used to collect the required data. Initially the implanted grating outcoupling performance was measured before laser annealing, a subsequent measurement was taken to find the outcoupling performance after the annealing process had taken place. The results of these measurements are shown in Figure 7.5. All of the annealing results shown have been collected from implanted grating coupler “C” which has a period of 600nm.

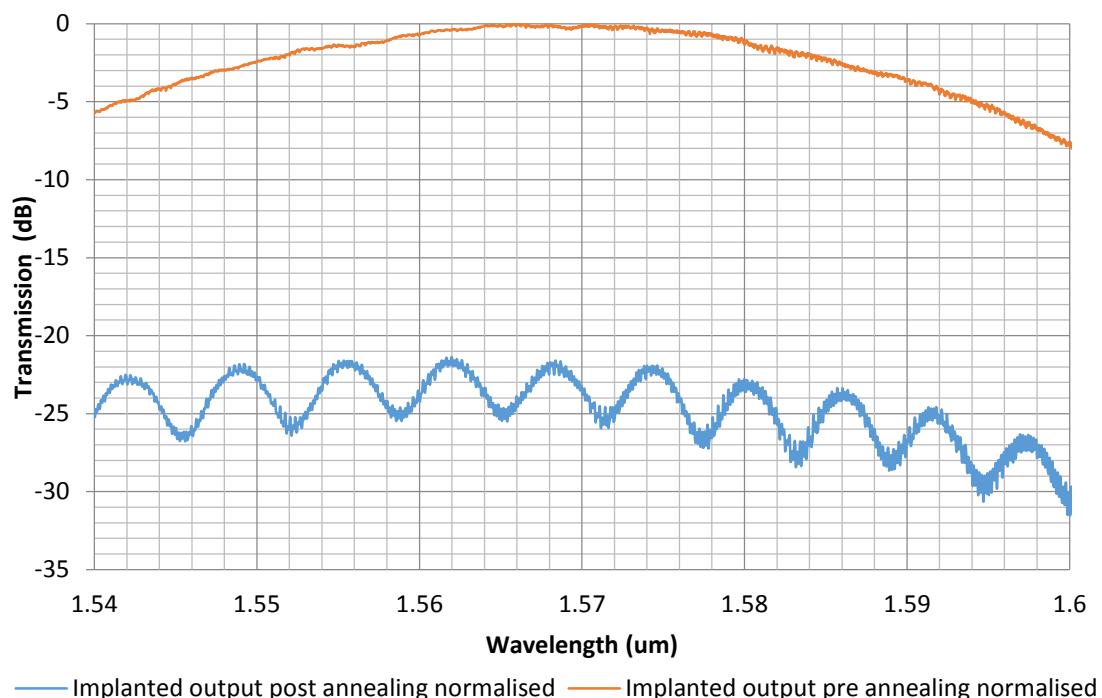


Figure 7.5 - 100kev implanted grating coupling before and after annealing a 100kev, 1×10^{15} ions cm^{-2} grating.

Figure 7.5 shows that annealing has affected the implanted grating outcoupling performance significantly, with a 21dB attenuation observed in the output laser power

collected. Curiously a periodic response occurs in the spectrum as shown in Figure 7.5. The free spectral range ($\Delta\lambda$) of the spectral peaks is 7nm. The cause of this periodic response is suspected to be a resonant Fabry-Pérot cavity forming within the device. The length of a Fabry-Pérot etalon can be expressed in terms of the free spectral range of the periodic response using the equation shown in equation 7.1.

$$l = \frac{\lambda_0^2 - \lambda_0 \Delta\lambda}{2\Delta\lambda n_{eff} \cos\theta} \quad (7.1)$$

where θ is the angle of propagating light through the cavity, which for a waveguide is 0. Also, as the correctional term in the numerator of $-\lambda_0 \Delta\lambda$ gives an adjustment of less than one percent of the final value, it can be ignored for practical purposes, resulting in the simplified equation given in equation 7.2.

$$l = \frac{\lambda_0^2}{2\Delta\lambda n_{eff}} \quad (7.2)$$

Assuming that the refractive index of the annealed silicon region is 3.48, the effective index of the 10 μm waveguide is 2.84. At the transmission central wavelength (λ_0) of 1.57 μm , the calculated cavity length is 62 μm . This length is of the same order as the 50 μm length of the mid-section of the bow tie. This indicates that the Fabry-Pérot etalon is formed from reflections originating from the tapers either side of the central region, as other circuit components are all considerably longer than the etalon length calculated. This can be further verified. Test structures with the central region replaced by single mode waveguide were measured, and these structures did not show the resonance observed in the annealed bow-tie structures. It is not unreasonable to assume that the effective length of the etalon may be effectively extended beyond the 50 μm central section by 6 μm in both directions by an initial low reflection region in the 0.6° flare angle taper. This shows the importance of considering Fabry-Pérot etalons in future device designs, improved tapers may reduce the effects experienced by reducing the amplitude of the resonance and reducing the 50 μm grating region to 10 μm may make the $\Delta\lambda$ large enough that it is not an issue for practical purposes.

The Fabry-Pérot cavity alone is not likely to cause a measurable output at the grating coupler however, it is possible that the residual grating coupler pattern of hardened

ZEP resist found on top of the waveguide in the atomic force microscopy results shown in Figure 6.16 may cause this effect. Gratings formed from a periodic refractive index change upon the waveguide surface have been demonstrated previously, [14] with layer thicknesses as low as 5nm demonstrating coupling properties. Thus methods to ensure the complete removal of the implant mask layer must be put in place in future process flows to avoid any residual coupling after testing, and to obtain optimal performance of the circuit.

From an optical device perspective, the grating outcoupling performance has been removed to a degree that there is no significant light leaving the circuit at the test point though this does not definitively state that the device has been removed in the desired fashion. Coupling could have been removed by means which are not immediately obvious such as damage to the waveguide or grating region. To ensure the grating has been effectively removed and the initial waveguiding characteristics restored, it is essential to check that the throughput of optical power increases. The transmission results through the implanted region are shown in Figure 7.6, the results have been normalised to the peak transmission power before annealing.

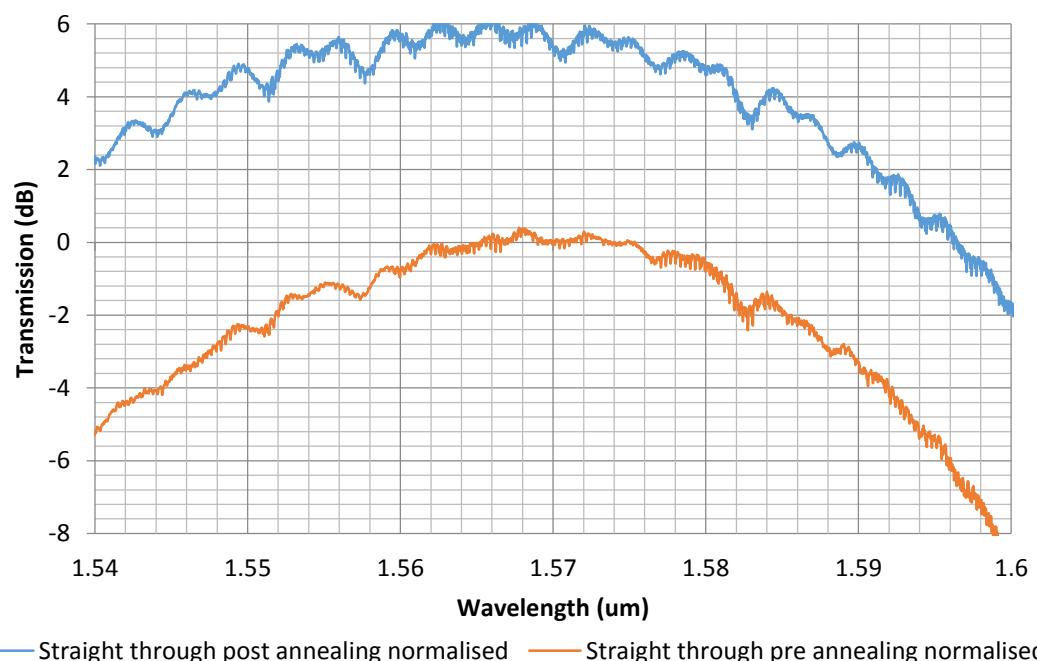


Figure 7.6 - Fixed couplers end to end performance before and after annealing a 100kev, 1×10^{15} ions cm^{-2} implanted grating, results are normalised to the peak performance before annealing.,

Figure 7.6 shows the fixed end-to-end coupler response increasing by 5.7dB following annealing, clearly showing the grating was annealed and that the power diverted to the test point has successfully been reintegrated to the waveguide.

The transmission measurement also allows any additional loss introduced by the implantation and annealing process to be characterised. Residual losses could potentially arise within the test point creation and removal process from mechanisms such as increased surface roughness due to sputtering during implantation or laser ablation during annealing or alternatively a decrease in material quality. To estimate any residual loss contributions that may occur, transmission measurements of annealed bow tie structure were compared with measurement data recorded from control bow tie structure that has not been implanted at any stage. Subtracting the control data from the transmission data measured through a bow tie structure that has previously contained an implanted grating coupler which has been removed via laser annealing, allows an estimate of any residual losses. The measured residual loss was 0.3 dB this is an indicator that there is no significant residual loss, but is not adequate to offer a reliable residual loss contribution data. As two separate devices have provided this information, minor fabrication variations could easily produce a difference of 0.3 dB furthermore alignment variations could also produce this level of variation. A more accurate measurement would be obtained by extrapolating the data for a single grating from a long cascade of annealed test points.

7.3 Conclusion

Optical characterisation data has been presented in this chapter for ion implanted grating couplers before and after annealing, along with a surface relief grating coupler for reference. The best implanted grating coupler demonstrates a loss of only 5.5 dB compared with a loss of 4.5 dB shown for the surface relief grating coupler. The coupling loss data obtained for the respective grating couplers demonstrates a performance reduction of only 1dB for the ion implanted case when compared with its surface relief counterpart. The 1 dB bandwidth of both grating couplers has also been shown to be very similar at 30nm and 32nm for surface relief and implanted gratings respectively.

The localised laser annealing performed has been proven to be effective for removal of the optical characteristics of the implanted grating coupler. The performance of the implanted coupler decreases by 21dB after annealing, while the transmission through the annealed regions increases by 5.7dB when compared with the grating transmission performance before annealing. Initial studies into the residual loss caused by the implantation and annealing process have also been performed and suggest there is no significant residual loss from the process.

Chapter 8 - Conclusions and Future Work

8.1 Summary and Conclusions

Optical technology is key to overcoming the bottlenecks caused by electrical bandwidth limits and may also facilitate the current drive towards lowering the power consumption of computing. A limiting factor in optical technology reaching the mainstream is cost, and maximising wafer yield is essential to reducing the cost per chip. Unlike an electronic circuit it is not possible to apply a simple test probe to an optical waveguide to monitor the signal, which prevents traditional automated optical integrated circuit testing. Potential testing methods from the literature have been discussed. The literature on the subject highlights that the methods available for accessing intermediate points on a waveguide are very limited, with no methods viable for large scale testing. This means characteristics of an optical circuit are unknown until it is fully processed and functional. This is a problem that makes quality control very difficult. Without the ability to test circuits, it is very difficult to establish where devices fail during manufacturing, which in turn introduces a levy to the working devices to cover the cost of those which fail during manufacture, increasing chip costs and limiting the viable system complexity.

In this work a novel erasable grating coupler has been presented as a device to enable wafer scale testing. The device design, fabrication, characterisation, and removal via laser annealing have been performed. The implanted grating coupler structures have demonstrated coupling efficiencies competitive with their surface relief counterparts. The bandwidth measured from the implanted structures is also in line with the bandwidth measured from comparable surface relief structures. These results are interesting in their own right, demonstrating an alternative method of fabrication for diffractive grating couplers which result in a planar waveguide surface [165]. A planar surface can be of paramount importance to obtain high quality epitaxially grown or deposited layers which can be useful for multilayer optical integrated circuits or sensing applications, though speciality low temperature growth processes would be required to prevent recrystallization of the amorphous silicon regions [183-185]. The impact of implanted grating couplers reaches far beyond this however. The ability to

subsequently remove the grating coupler after measurement allows a temporary coupling structure to be formed, which is suitable for use in wafer scale testing.

The implanted grating coupler in this work has been optimised for use at a wavelength of 1550nm by the use of FDTD simulations, which yielded a period of 600nm and an implant depth of 130nm. To minimise the fabrication time and hence cost of the testing process, all test points could make use of a single implant depth and the period varied to adjust the coupled wavelength to ensure only a single implant process is required. A rigorous testing methodology was devised for the proof of principle implanted gratings, involving the use of a bow tie structure. The bow tie structure shown in Figure 4.1 is akin to the envisaged wafer scale testing schematic shown later in Figure 8.1, but includes only a single test point. This configuration was sufficient to confirm that the implanted grating coupler had both been created and removed successfully, with no significant residual losses introduced by the testing process, though a cascade of test points would be necessary to establish an exact value of the residual losses incurred through the addition and subsequent removal of the implanted grating device.

An adiabatic dual stage taper with a total design length of 700 μm is used to transition between the grating coupler region and a single mode waveguide, this transition is required both into the 10 μm waveguide which houses the implanted grating and to subsequently transition back into a single mode waveguide. Including the 50 μm waveguide region used to house the grating coupler, this gives a total device length of 1.45mm for an implanted grating coupler test point. This is a very large device compared to other integrated optical components. To allow an increased packing density, this taper length must be reduced for any future test point designs, simulations suggested the taper length can be reduced by at least a factor of 2 while retaining the same performance, curved tapers or other more advanced spot size converters may prove key to future device miniaturisation. The 50 μm waveguide housing the grating could also be reduced in length without any significant detriment. Though this would not impact the device length significantly compared with the tapers, it may provide additional benefits in diminishing the effects of the observed Fabry–Pérot resonance, by increasing the free spectral range ($\Delta\lambda$) as $l \propto \Delta\lambda^{-1}$, where l is the length of the Fabry–

Pérot etalon. Reducing the etalon by a factor of 5 would increase the $\Delta\lambda$ to a value larger than a grating couplers 1dB bandwidth.

The crux of this device is the refractive index change introduced by amorphization with an iso-electronic impurity. Amorphization of grating regions via the use of ion implantation was simulated using KING and KING 3D. Germanium was shown to offer the implantation profile with the smallest lateral amorphization for a given implant depth when comparing implant profiles of Si, Ge, Sb and Xe. A dose of 1×10^{15} ions cm^{-2} is shown to offer the best trade-off between lateral amorphization and the size of the interface region for Ge. Sputtering for these conditions was also shown to be insignificant which is critical for maintaining a planar surface.

The implant mask material was ZEP photo resist, selected on the merits of its ion stopping range and simple processing. The risks associated with the removal of the implant mask were considered to be low, though atomic force microscopy showed this was not the case. A residual layer of ZEP resist was found near the grating which could not be removed, which is thought to be caused by extensive cross-linking between polymers of the resist. Though some cross-linking was expected at the surface of the 500nm resist, the effects were not expected to penetrate significantly beyond the 130nm range of ion implantation. Future devices must revisit the implant masking step to provide a more suitable mask or alternatively more advanced chemistry should be investigated for removal of the cross-linked ZEP resist. One option would be to use a thin silicon dioxide layer underneath the ZEP resist, which would allow removal of any residual electron beam resist by removing the underlying silicon dioxide with hydrofluoric acid.

Variable angle spectroscopic ellipsometry was performed to provide an insight to the behaviour of silicon and amorphous silicon at different wavelengths, and aid in the selection of a suitable laser wavelength for localised annealing. The real part of the refractive index was predicted to be 3.94, though it was shown to be marginally higher at 3.96. Though this relatively small discrepancy is unsurprising as the prediction was based on the effects from implant conditions with a lower acceleration energy, it is enough to shift the central wavelength by $\sim 7\text{nm}$, which would be significant in a multiple channel system.

The absorption coefficients of amorphous and crystalline silicon was calculated from the complex part of the refractive index. The results showed that for wavelengths above 450nm, the absorption coefficient of crystalline silicon was shown to be at least an order of magnitude lower than amorphous silicon formed using germanium implantation, which is highly beneficial from the perspective of annealing of ion implanted grating couplers as the annealing process becomes more tolerant to small variations in scan speed and laser power. Previously a wavelength of 248nm was used for annealing, which requires stringent annealing conditions to ensure annealing occurs without the undesirable effects such as softening or ablation. The absorption coefficient is also noted to be significantly different based on the amorphization method used, with amorphous silicon deposition, as well as amorphization via Silicon and Germanium implants considered. As the implants are iso-electronic the implanted Silicon sample is not doped and hence no increase in loss was expected. Though there is no permanent increase in loss observed in the data as expected, effects are observed within the data which are congruent with molecular vibrational modes, displaying an increase in absorption while in the amorphous phase for the amorphous material formed using ion implantation. Molecular vibrational modes are not observed in the deposited amorphous silicon due to the presence of hydrogen, which terminates the dangling bonds. Though the optical results suggest this increase in material absorption for the amorphous phase does not impart any significant detrimental effects to the coupling performance, it does show that this mechanism of increasing the refractive index would be less useful for devices requiring longer propagation lengths through the amorphous region such as waveguides.

Optical characterisation data has been presented for ion implanted grating couplers alongside comparable surface relief grating coupler results. Simulation data suggests that the outcoupling efficiency of the implanted gratings and surface relief gratings used in this work should be 45% and 52% respectively. The best implanted grating coupler demonstrates a loss of only 5.5 dB (28% coupling efficiency) compared with a loss of 4.5 dB (35% coupling efficiency) shown for a comparable surface relief grating coupler, a difference of 7%. The measured efficiency value is lower than the simulated value in both implanted and surface relief grating coupler cases, this is dominantly due to the difference in the modal overlap between the fibre mode and the

mode exiting the grating coupler, though the difference between the measured results is in agreement with the difference expected from simulations, which suggests that the implanted grating coupler did not have any additional unexpected loss mechanisms compared with the surface relief case. Modal overlap calculations can be integrated into grating simulations to improve the accuracy, though it significantly increases the simulation volume and hence simulation time. The coupling performance obtained from the implanted coupler is more than sufficient for use as an optical test point. The 1 dB bandwidth of both surface relief and implanted grating couplers has been shown to be very similar at 30nm and 32nm respectively, which shows a test point is able to measure any signal that is passed in to the circuit via an implanted or surface relief grating coupler, provided both are designed with the same central wavelength. Also like its surface relief counterpart, the implanted grating coupler can be interrogated an unlimited number of times before removal, though exposure to temperatures above 500°C may be detrimental to the coupling efficiency of the implanted coupler.

Finally localised laser annealing was used to permanently remove the implanted grating coupler after the device testing was completed. Localised annealing using a pulsed laser at 248nm, as used previously for a large scale annealing of wafer scale testing devices has been attempted. Successful localised annealing using this system was thwarted by the prevalence of material ablation, which is due to high instantaneous energies delivered by a pulsed laser in conjunction with similarities between the absorption coefficient of crystalline and amorphous allotropes of silicon. Localised laser annealing was successfully demonstrated using a continuous wave laser at a wavelength of 488nm. The laser wavelength selected allows for an improved power tolerance, which works synergistically with the significant reduction in instantaneous power, compared with the previous 248nm pulsed laser, to prevent ablation. At a speed of $10\mu\text{m s}^{-1}$, a laser power of 180mW was able to successfully anneal the grating. The annealed linewidth can be as narrow as $1.45\mu\text{m}$, which demonstrates successful localised annealing is possible even for devices 5 times smaller than the implanted grating couplers shown in this work. Furthermore the change in material allotropy caused by the laser annealing process has been confirmed by Raman spectroscopy. A Voigt fit can be applied to the Raman data, which reveals a Lorentzian linewidth of 4.3 cm^{-1} for the annealed material, compared to 2.7 cm^{-1} for single crystal silicon. This

shows that the annealed silicon is polycrystalline, which is associated with higher waveguide loss values than single crystal silicon material. It is possible that the annealing process can be further optimised to improve the quality of the regrown material, though the exact grain size garnered in the relatively small implanted regions would be difficult to determine. This is not of primary concern as it has been shown that the losses in polycrystalline silicon waveguides are not greatly dependant on grain size for grains in the range of 0.1-0.4 μ m [181], as the implanted regions in this case span only \sim 0.3 μ m, grain size is unlikely to make significant contributions towards the optical loss. The move from a pulsed 248nm laser source to a 488nm continuous wave laser presents some very significant advantages beyond the increased power tolerance, dominantly in cost. In the wavelength and power range required, cheap solid state lasers are available such as a frequency doubled “Nd:YAG” (532nm). It is also feasible that a laser at visible wavelengths could be delivered via fibre to reduce the physical size of the system.

The localised laser annealing performed has been demonstrated to be effective for removal of the optical characteristics of the implanted grating coupler. The advantages obtained from localised laser annealing over oven based annealing, such as zero interaction with other optical devices, is critical to process adoption by industry. The performance of the implanted coupler decreases by 21dB after annealing, while the transmission through the annealed regions increases by 5.7dB when compared with the grating transmission performance before annealing. Initial studies into the residual loss caused by the implantation and annealing process have also been performed and suggest there is no significant residual loss from the process. This potential wafer scale testing method results in a waveguide with an unperturbed surface, and an optical circuit that is not impeded by the erased test point.

One possible envisaged wafer scale testing configuration using implanted grating couplers is shown in Figure 8.1. In this example three wavelengths are passed into the circuit, represented by orange, purple and green arrows or λ_O , λ_P , and λ_G . The wavelengths do not need to be different if the device has only a single narrow operational channel, though care must be taken in the design process to ensure power

reaches the third test point using measures such as a reduced coupling length, unless the process erases each test point before measuring the successive test point.



Figure 8.1 – Schematic representation of the envisaged wafer scale testing configuration

The proposed wafer scale testing method in Figure 8.1 uses the implanted grating coupler structures which have been formed using ion implantation to couple light out at intermediate points along the waveguide labelled as Test Point O, P and G to represent the wavelength they monitor. Two methods can be applied to test a device, option one would align an input fibre to the grating directly preceding the device and an output fibre to the grating directly succeeding the device, e.g. to measure the optical device under test (ODUT) P, the input fibre would be positioned at test point O and the output fibre would be positioned at test point P. This method requires two alignment steps, which is not desirable, as alignment is the most time consuming part of the process. A single alignment step can be used to enable a faster measurement time, an input light source would be aligned to the fixed input grating coupler, and a test probe would be aligned to the implanted grating coupler test point. The components can then be measured and characterised successively and the individual component characterisation data extrapolated by subtracting the measured data for the proceeding components.

Test points such as those demonstrated here are essential in allowing optical circuits or individual components on a wafer to be autonomously tested after selected manufacturing steps. Testing will allow poorly performing devices to be detected early, such that processing of that wafer can be terminated or the damaged devices

modified or repaired using direct write methods. The results shown in this work suggest that implanted grating couplers offer a very powerful wafer scale testing method that will directly enable an increased yield of optical integrated circuits and allow an increased complexity of photonic circuit designs.

8.2 Future Work

The results shown in this work open up a series of questions as to how to take this technology forward in the future, what can be done differently to improve the current device, and what could change to improve wafer scale testing technology.

On reflection, it is clear that the implant masking technique must be addressed. Though ZEP did provide sufficient implant resistance, it proved difficult to fully remove it afterwards. Two options arise, one is to design a more rigorous ZEP removal process though this may prove very complex. Alternatively another implant mask topology could be used. A combination of a thin silicon dioxide layer with a thick ZEP top coating may be a suitable solution. The thin oxide layer would allow a very slow etch to be performed after implantation to remove the oxide, which would ensure undercutting is avoided but also ensure ZEP is removed fully. Better still, moving to a rib waveguide would allow the silicon slab to act as an etch stop, which would ultimately allow a silicon dioxide implant mask to be used followed by removal using a relatively standard hydrofluoric acid etch.

Optical simulations were simplified in this work; the implanted regions were treated as idealised structures, rectangles, opposed to the complex statistical shape observed in the real case. Simulation accuracy would undoubtedly be improved if the exact profile of the implant were to be used, though this would be no simple task. To do this on an individual case by case basis may be possible using matlab scripts, though the import of multiple accurate profiles for different implant energies and dose combinations, which would be required for device optimisation, would require the involved development of proprietary software.

Looking forward, we can consider improvement of the dominant performance metrics associated with grating couplers which are efficiency, bandwidth and device length. Apodization may marginally improve both efficiency and bandwidth parameters,

however to gain more significant improvements in both metrics, subwavelength gratings offer a more potent approach. The couplers discussed in Halir 2014 [186] offer double the bandwidth of uniform surface relief grating couplers along with a 1dB improvement in coupling efficiency. The implant design would be the limiting factor in achieving the minimum feature sizes required for such structures, but the advantages could be very significant.

The large length of the device presented is a significant issue if multiple test points were required on a densely integrated optical circuit. It would be trivial to shorten the central region for the grating from 50 μm to 10 μm as the fibre core diameter typically used for measurement is less than 10 μm . The taper length is of course far more significant. Grating couplers have previously been integrated into a taper [49]. The grating in this case is simultaneously used as a coupler and as a lens to focus light into the waveguide, allowing significant reductions in the taper lengths required. If this style of device could be replicated for implanted grating couplers the device lengths required may be reduced by an order of magnitude.

The annealing process for wafer scale testing has moved forward significantly, but there is still huge potential for making it cheaper and simpler. In this work a high power argon ion gas laser was used. As the power that was necessary was lower than expected, a cheaper solid state laser such as a frequency doubled Nd:YAG could provide sufficient power for annealing at a similar wavelength (532nm). Another significant improvement in the annealing would arise from removing the necessity of the complex alignment required, which could be done by adding resistive heaters in the vicinity of the grating. The large contact pads would reduce any alignment difficulties, though the elements may struggle to deliver sufficient heat, especially if the speed of annealing was important. Alternatively delivering the annealing laser through the measurement fibre or alternatively a fibre which mimics the alignment of the measurement fibre would remove the need for a separate annealing alignment process.

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