UNIVERSITY OF SOUTHAMPTON

Faculty of Engineering and the Environment

Engineering Materials Group

Development of Amorphous SiC Based Resistive Memories

by

Le Zhong

Thesis for the degree of Doctor of Philosophy

August_2014

UIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF ENGINEERING AND THE ENVIRONMENT

Doctor of Philosophy

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As Flash memory is approaching physical scaling limit, there is great interest in the research of the next generation non-volatile memory. In addition to replacing Flash memory in data storage applications, the next generation non-volatile memory is also expected to have improved performance, especially more cycle endurance and faster read/write operation, so that it may eventually be the “universal" memory. Resistive memory (RM) is widely considered to be the overall most promising emerging non-volatile memory. This project focused RMs based on Cu and amorphous silicon carbide (a-SiC) following the recent reports of excellent retention and stabilities of such RMs, which was attributed to the advantageously low Cu diffusion rate in SiC. Material properties, namely chemical composition, structural properties and electrical conduction properties of the sputtering deposited a-SiC and a-SiC/Cu solid electrolytes were firstly analysed in this project. This project has then developed Cu/a-SiC RMs with via-stack and crossbar structures, with a-SiC and a-SiC/Cu as solid electrolytes and Au, W and TiN as counter electrodes. The switching characteristics of the obtained devices have then been thoroughly investigated. All devices based on Cu and a-SiC with different structure and material configurations have shown repeated resistive switching behaviour, with each batch showing certain unique features in their switching behaviour. Nonpolar resistive switching was observed in the Cu/a-SiC/Au and Cu/a-SiC:Cu/Au via-stack devices, while coexistence of bipolar and unipolar switching was observed in RMs with TiN and W counter electrodes. Our devices also exhibited significantly improved ON/OFF current ratio and great state retention performance. Furthermore, the switching mechanisms and conduction mechanism of these RMs were analysed based on their I-V characteristics. These results suggest promising application potentials for RMs based on Cu and a-SiC.

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Declaration of Authorship

I,……Le Zhong……

declare that this thesis and the work presented in it are my own and has been generated by me as the result of my own original research.

Development of Amorphous SiC Based Resistive Memories .....

.....

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Acknowledgements

These few lines cannot give all my gratitude to so many people that made this PhD possible. Firstly I would like to express my special appreciation and thanks to my supervisor Dr. Liudi Jiang, who cared so much about this project throughout these years and was always around for advice. I would also like to thank my secondary supervisor Prof. Philippa Reed, who helped me tremendously when I started my PhD and Dr Jiang was taking her maternity leave. I'm also indebted to the School of Engineering Sciences and later Faculty of Engineering and the Environment who funded my PhD.

Many thanks go to Prof. Kees de Groot, whose close and unselfish collaboration was vital to this project. Ruomeng Huang helped me enormously in the experimental works, and even I sometimes felt I asked too much. In addition, Dr. Yudong Wang, Longtao Dong, Dr. Owain Clark, Dr. Kian S Kiang and many more people in ECS helped me in the nanofabrication centre.

Zondy Webber deserves his special thanks because he singlehandedly trained and helped me with all the equipment I used in the nanomaterial rapid prototyping facility.

Dr. Nick Alderman, Dr. Shuncai Wang, Yang He, Mauro Callisti, and many more people in the Engineering Material group offered me great help with material characterisation, which I'm fairly unfamiliar with.

And last but not least, I wish to thank my parents, although words can never be enough for what they have done for me over the years. They convinced me to study abroad and pursue my PhD, and they spent years without having me around.

特别感谢我的父母：钟长文，龙滨。

Definitions and Abbreviations

AE	Active Electrode
AFM	Atomic Force Microscopy
a-SiC	Amorphous silicon carbide
Au	Gold
Bipolar switching	During a resistive switching cycle, SET and RESET require voltage bias of opposite polarity.
CE	Counter Electrode
CMOS	Complementary Metal-Oxide-Semiconductor
Cu	Copper
DRAM	Dynamic Random Access Memory
ECM	ElectroChemical Metallisation
EDS	X-ray Energy Dispersive Spectrometer
FIB	Focused Ion Beam
HRS	High Resistance State
I-V	Current-voltage
LRS	Low Resistance State
Nonpolar switching	The coexistence of all four possible switching modes: +bipolar, +unipolar, -bipolar and –unipolar.
ON/OFF Ratio	The ratio of LRS current to HRS current, equivalently the ratio of HRS resistance to LRS resistance
PCM	Phase Change Memory
RESET	The transition from LRS to HRS in a resistive memory
RM	Resistive Memory
R_{OFF}	Resistance of a RM in HRS
R_{ON}	Resistance of a RM in LRS
SEM	Scanning Electron Microscope

SET	The transition from HRS to LRS in a resistive memory
SMU	Source-Monitor Unit
SRAM	Static Random Access Memory
TEM	Transmission Electron Microscope
TiN	Titanium nitride
Unipolar switching	SET and RESET require voltage bias of the same polarity.
V_{RESET}	The voltage at which RESET process occurs in a RM
V_{SET}	The voltage at which SET process occurs in a RM
W	Tungsten
XPS	X-ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
+bipolar switching	SET occurs with positive bias on AE and RESET negative bias on AE.
+unipolar switching	SET and RESET both occur with positive bias on AE
-bipolar switching	SET occur with negative bias on AE and RESET positive bias on AE
-unipolar switching	SET and RESET both occur with negative bias on AE

Chapter 1. Introduction

1.1 Overview of the Project

Currently, Flash memory is the dominant non-volatile memory technology, largely because of its high storage density and low cost. Being non-volatile, Flash memory can hold information over 10 years without additional power supply [1]. Although broadly applied for data storage in computers and electronic products, Flash memory has low endurance and slow read/write operation, compared to other memory technologies. More importantly, Flash memory is rapidly approaching its scaling limit, at which point the continuous increase of storage density and decrease of cost can no longer persist, and further scaling below 20nm requires enormous effort in material engineering and re-design of Flash memory structure [2-5].

Among a number of emerging memory technologies, non-volatile memory cells based on resistive switching have attracted particular interest in recent years due to their significant potential to replace both conventional non-volatile memory and volatile memory (e.g. Dynamic Random Access Memory). Resistive memories (RMs) offer promising properties such as fast switching speed, low power consumption, long retention lifetime and excellent down-scalability, leading to multi-bit data storage with high density[6, 7]. A RM also presents a simple device structure which usually consists of a solid electrolyte material sandwiched between two metal electrodes [8, 9]. Material properties of the solid electrolyte are directly linked to the corresponding switching performance, and have thus been the focus of RM researches. Ease of integration of these materials with CMOS (Complementary Metal-Oxide-Semiconductor) technology is also a practical consideration to ensure future low cost memory fabrication and for integration with essential logic circuitries.

Si based amorphous materials such as amorphous Si [10-13] or SiO_2 [14-17] have been explored in multiple studies as potential CMOS-compatible solid electrolyte material, and RM devices based on these materials have exhibited certain promising features such as high switching speed. However, instability and poor retention characteristics are key drawbacks for these devices. Amorphous silicon carbide (a-SiC) as a new electrolyte material has been recently reported [18, 19] to show excellent retention and stabilities

due to the advantageously low Cu diffusion rate in SiC [20, 21]. However, with only limited reports on Cu/a-SiC RMs focusing on the studies of retention and stability properties, other crucial aspects of such RMs, such as switching polarity, device structures, counter electrode materials and doping of a-SiC solid electrolyte material, remain to be investigated. From analysis of the influence of these factors, a better understanding of the switching mechanisms of these RMs can also be gained. In addition, there's also room for improvement in the switching performance of reported Cu/a-SiC RMs, in particular the ON/OFF ratio.

According to these limitations of current studies on Cu/a-SiC RMs, this project have focused on development of Cu/a-SiC RMs with distinct structures and counter electrode materials, including CMOS-compatible materials. Cu doped a-SiC film has also been explored as solid electrolyte material, as metal dopant has been reported to improve device performance in multiple studies. The corresponding switching mechanisms has also been discussed based on detailed analysis of the switching I-V data.

1.2 Aims and Objectives

The overall aim of this project is to develop novel RM devices based on a-SiC with overall superior performance, and to further investigate their switching mechanisms and the possible factors that regulate their performance. The objectives are as follows:

• To deposit and characterise material properties of a-SiC and Cu doped a-SiC as solid electrolyte layers.

• To develop room temperature fabrication routes for RMs based on aforementioned solid electrolytes.

• To develop the relevant testing procedures for obtained RM devices.

• To thoroughly test the resistive switching performance of obtained devices.

• To analyse the respective influence on switching properties of device structure, solid electrolyte materials and counter electrode materials.

1.3 Organisation of Thesis

Following introduction, chapter 2 gives a comprehensive review of the development and the state of the art of resistive memories, in particular resistive memories based on a-SiC. Chapter 3 presents the relevant experimental methodologies involved in the project, namely the deposition and material characterisation of a-SiC and a-SiC/Cu solid electrolytes, and the fabrication and characterisation of RMs based on said solid electrolytes. In chapter 4, relevant material properties of the obtained a-SiC and a-SiC/Cu films are discussed, including their composition, structural properties and electrical conduction properties. Resistive switching characteristics from Cu/a-SiC/Au RMs in a via-stack structure are shown in Chapter 5, which also includes detailed analysis of the conduction mechanisms and switching mechanisms. Furthermore, a-SiC based RMs with modified device structure, solid electrolyte materials and counter electrode materials were fabricated and their resistive switching properties measured. These results are presented in chapter 6. Finally chapter 7 draws conclusion to research and provides suggestions for appropriate directions for future research.

Chapter 2. Literature Review

This chapter presents a comprehensive review of the development and the state of the art of resistive memories, in particular resistive memories based on a-SiC. An overview of semiconductor memory technologies and the need for novel non-volatile memory technology are discussed in Section 2.1. Section 2.2 gives a brief review of the history of resistive memories. The operation principles and several key aspects of the operation of resistive memories are discussed in Section 2-3, including the conduction mechanisms, multi-level switching, scaling behaviour and electroforming processes. The common device structures are discussed in Section 2.4 Furthermore, the material choices of metal electrodes and solid electrolytes are reviewed in Section 2.5. And finally in Section 2.6, there is a discussion of the state of the art of a-SiC based RMs and the merits of a-SiC as the solid electrolyte material.

2.1 Overview of Semiconductor Memory Technologies

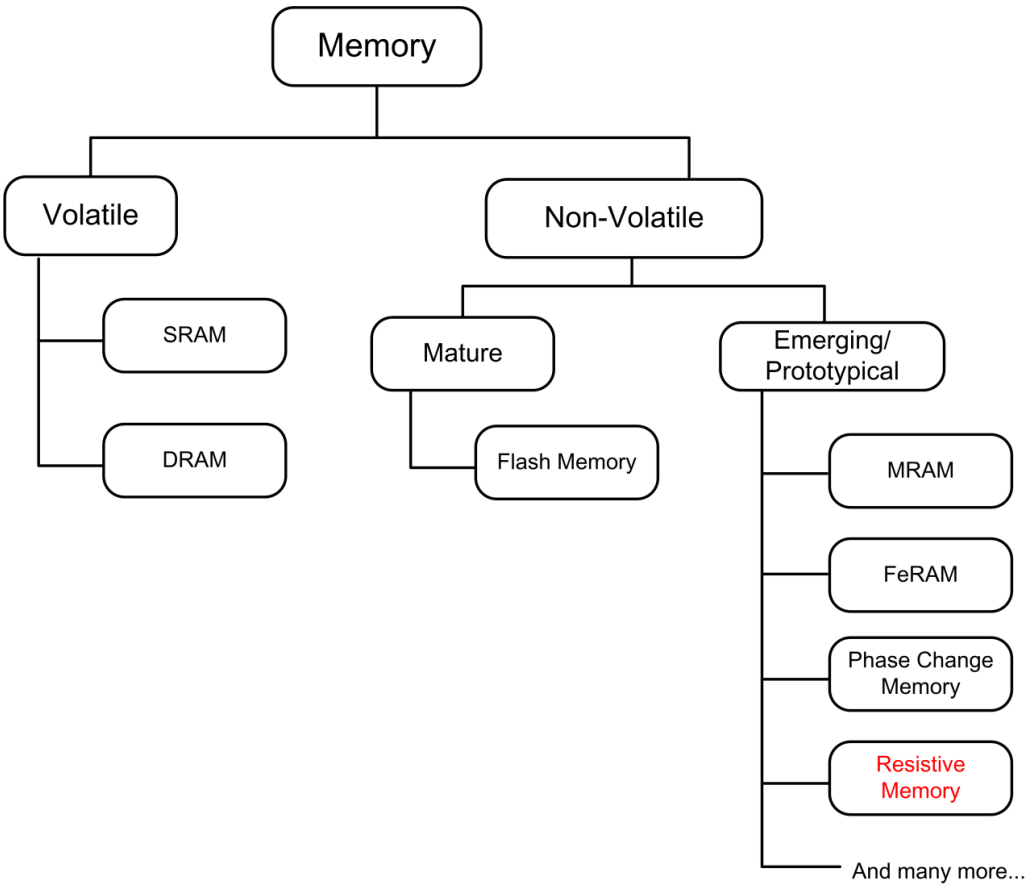


Figure 2-1 Categories of semiconductor memory technologies [22].

As is shown in Figure 2-1, semiconductor memories can be divided into two main groups: volatile and non-volatile memories, based on the retention of stored information. For volatile memories, constant power supply is required to maintain stored information, while in non-volatile memories the stored information remains even when power is turned off [8]. The figure also shows that most semiconductor memory technologies are also named Random Access Memory (RAM). As the name suggests, information can be read/written to RAM cells randomly, as opposed to sequentially in hard disks.

- **DRAM**

Dynamic RAM (DRAM) and Static RAM (SRAM) are the two essential volatile memories that are currently employed across a wide spectrum of electronic devices. A typical DRAM cell has a 1T1C configuration: 1 transistor and 1 capacitor. Cell state is set by whether there's charge stored in the capacitor. With the constant demand of scaling down, tremendous effort has been put into innovating capacitor structures and developing high-K materials, to maintain the capacitance of DRAM capacitor. Due to leakage, a DRAM cell has to be regularly set to its previous stored state. This process is referred to as "refresh". During memory refresh, no normal reading or writing is allowed. This poses a fundamental limitation to its read/write time [23, 24].

- **SRAM**

A SRAM cell is essentially a flip-flop circuit consist of 6 transistors. The transistor configuration is shown in Figure 2-2: PL, NL forms an inverter and PR, NR a second inverter. The two transistors AL and AR control access to the memory cell. As long as external power supply is sustained, the two inverters of the flip-flop circuit will constantly re-enforce the state of each other, and the state of the memory cell is maintained. SRAM has a much larger unit cell size compared to DRAM, and hence much more expensive per unit storage capacity, but read/write in SRAM can be significantly faster because it’s not limited by the refresh time. SRAM is generally used as cache memory where access time is critical [24, 25].

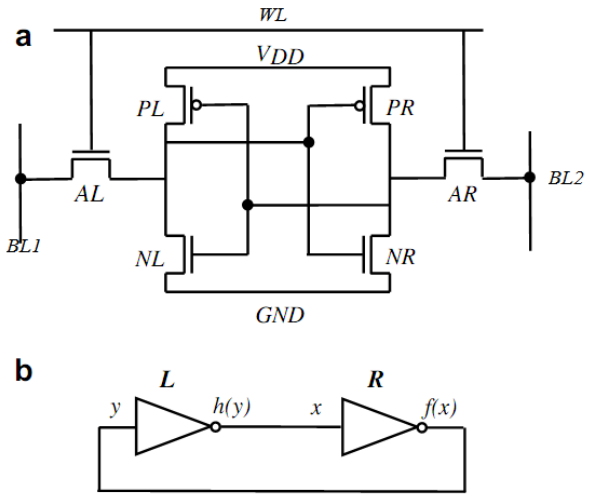


Figure 2-2 (a)Configuration of transistors and (b) equivalent circuit of a typical SRAM cell [26].

- **Flash Memory**

Flash memory is currently the most widely used non-volatile memory technology [4, 27, 28]. Its building block is floating gate transistor shown in Figure 2-3. Compared to a normal CMOS transistor, the main difference is the additional "floating gate", i.e. the gate between tunnel oxide and the inter poly insulator. By applying voltage at the control gate, source and drain, electrons can be injected into/extracted from the floating gate. The stored electrons will then influence the threshold voltage of the floating gate transistor, and its state can be read by applying a control gate voltage between the two threshold voltage values [29].

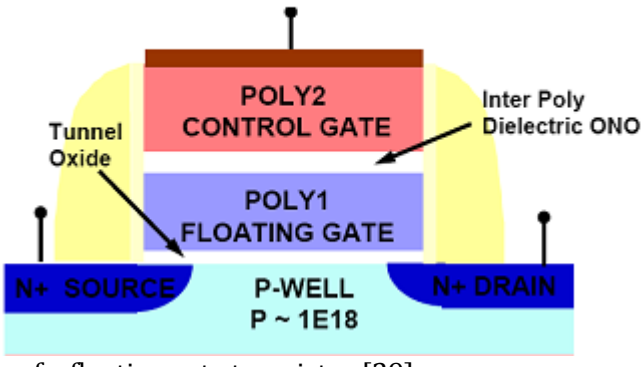


Figure 2-3 Structure of a floating gate transistor [29].

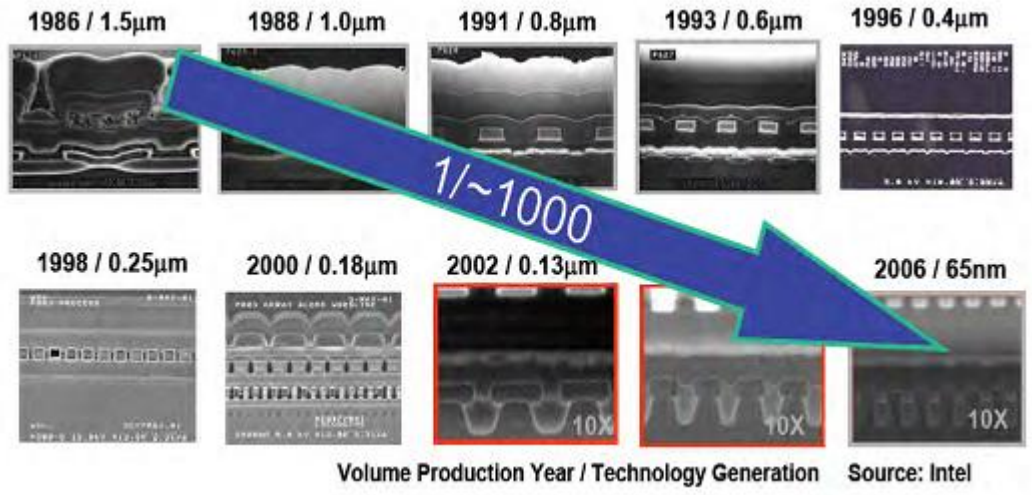


Figure 2-4 Scaling of Flash memory.

As Figure 2-4 shows, the feature size of Flash memory shrinks from 1.5µm in 1986 to 65nm in 2006, and as the result, cell area of a Flash memory cell is reduced more than 500 times. The continuous scaling down process directly leads to continuously improved storage capacity of Flash memory, which is a key reason for its wide adaption in modern electronic products.

Nevertheless, it is generally believed scaling of Flash memory is reaching physical limitations [3, 5, 30].In addition to the difficulties involved in fabrication of transistors with scaled dimensions, certain physical effects associated with reduced channel length, reduced dielectric isolation between adjacent cells and reduced gate oxide dimensions also challenges Flash memory scaling.

A fundamental limit to further scaling of Flash memory is the thickness of the tunnel oxide layer and the interpoly insulator. A critical parameter of Flash memory is gate coupling ratio, which is defined as the ratio of the capacitor between control gate and floating gate to the total floating gate capacitance (control gate to floating gate + floating gate to substrate). This ratio has to be over 0.6 to ensure enough voltage drop across the tunnel oxide. In practice, this is achieved by wrapping the control gate around the floating gate. Due to the requirement of state retention, the thickness of tunnel oxide scales very slowly and so does the interpoly insulator. A minimum of 10nm thick interpoly insulator is still currently required, therefore to achieve the wrapping gate structure, the total channel length of the floating gate transistor has to be over 20nm [31]. Moreover, the amount of electrons stored in floating gate is linearly proportional to the gate area, and the change of threshold voltage is determined by this amount of electrons. Essentially, the difference

between states will be more difficult to sense and more sensitive to electron leakage from floating gate [4, 32, 33]. These limitations of further scaling of Flash memories are the primary motivation for the development of novel non-volatile memories.

- **Novel Non-volatile Memories**

Due to these challenges in further scaling of Flash memory, ITRS (International Technology Roadmap for Semiconductors) 2013 are calling for novel non-volatile memories to replace Flash memory as data storage by 2018 [6]. Furthermore, novel non-volatile memories are also sought after as a "universal memory". At present, due to the long write/erase time of Flash memory, non-volatile memory can only serve as data storage, while the main memory is limited to volatile memories, namely DRAM and SRAM. If a novel non-volatile memory can have overall performance comparable to DRAM, then it will be possible to serve as both data storage and main memory. In this way the overall power consumption can be reduced, as the refreshing of DRAM is no longer needed [34]. The system performance may also be improved as the data does not have to be transferred between storage and main memory any more.

There are more than a dozen non-volatile memories based on different mechanisms. The main candidates that are being considered as the next generation non-volatile memory, however, are limited to Magnetic RAM (MRAM), Ferroelectric RAM (FeRAM), Phase Change Memory (PCM) and resistive memory (RM)[25, 32, 35-37]. A brief comparison of these memories and the mature memory technologies are listed in Table 2-1:

Type	Volatile		Non-volatile				
	SRAM	DRAM	Flash	MRAM	FeRAM	PCM	Resistive Memory
Mechanism	Flip-flop	Capacitor	Floating gate	Magneto resistance	Polarization change	Phase change	Resistive switching
Cell Elements	6T	1T1C	1T	1(2)T1R	1T1C	1T1R /1D1R	1T1R /1D1R
Minimum Cell Size	$140F^2$	$6\ F^2$	$5\ F^2$	$20\ F^2$	$10\ F^2$	$4\ F^2$	$4\ F^2$
Write/erase time	0.3ns /0.3ns	<10ns /<10ns	1ms /1ms	10ns /10ns	10ns /10ns	20ns /50ns	5ns /5ns
Cycle Endurance	$>10^{16}$	$>10^{16}$	$>10^5$	$>10^{16}$	10^{14}	10^8	10^{10}

Table 2-1 Comparison of mature and emerging memory technologies [6].

In this table, T stands for transistor, C capacitor, R resistor and D diode. For example a resistive memory cell typically has a 1T1R or 1D1R configuration, which means 1

transistor and 1 resistor or 1 diode and 1 resistor. And F is the minimum feature size. Compared to FeRAM and MRAM, phase changing memory and resistive memory clearly exceeds in scalability, as their cell area can be the same as a single transistor. Considering the limitation of scaling Flash memory is the most direct motivation for the next generation non-volatile memory, PCM and resistive memory appear to be more promising candidates. Compared to PCM, resistive memory has also demonstrated shorter write time, higher cycle endurance. Resistive memory also doesn't have the heat crosstalk issue that may limit the density of PCM[38]. All these features indicate the overall superior potential of resistive memory as the next generation non-volatile memory [6, 31].

2.2 History and Development of Resistive Memories

In the late 1960s, there have already been reports of resistive switching behaviour observed in metal-insulator-metal structures, such as Al/SiO_2/Au and Ti/Ti2O3/Au [39]. These structures had distinctive high and low resistance states, and could switch between the two states under applied voltage bias. Figure 2-5 shows the I-V curves of the two resistance states of a Ti/TiO_2/Ti structure. Clearly after switch the conduction changed from non-linear to linear, and the resistance of the structure was much lower. In this case, resistive switching was achieved by 2V~4V voltage between the two metal electrodes [40]. Although the exact mechanism of resistive switching was not clear at the moment, it was proposed such phenomenal could be the basics of high density memory devices [41, 42].

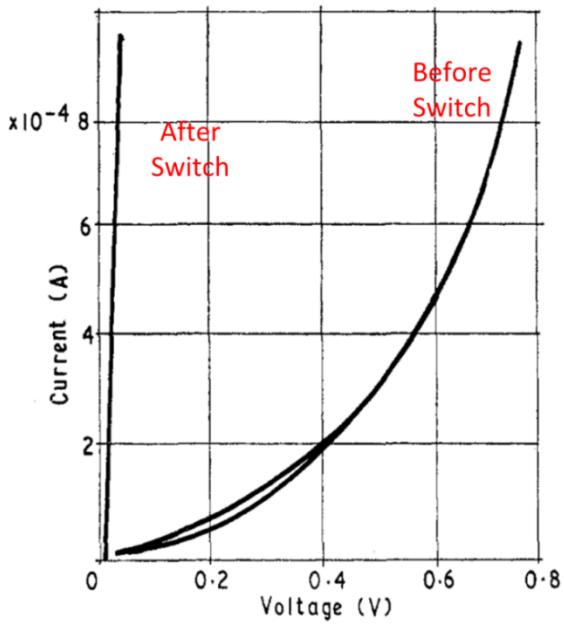


Figure 2-5 I-V curves showing the two resistance states of a Ti/TiO2/Ti structure, the resistance after switch is significantly reduced [40].

In 1976, it was firstly reported by Hirose et al that resistive switching was related to the formation and dissolution of metal conductive filaments between the two metal electrodes [43]. As can be seen in Figure 2-6, after resistive switching, the two metal electrodes were bridged by a thin filament. Additionally, measurement of temperature dependency of resistance in low resistance state indicated the filament most likely consisted of metallic Ag. This was also the first direct observation of conductive filament in resistive switching devices.

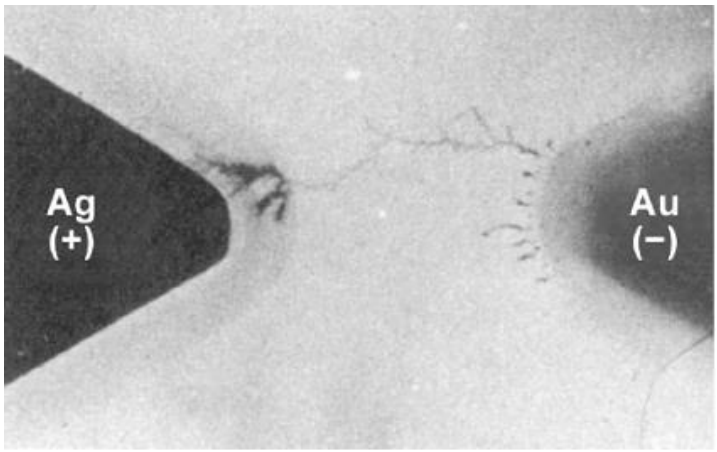


Figure 2-6 Optical microscopy image of Ag filament formed after switching in a lateral $Ag/Ag_2S_3/Au$ structure [43].

Subsequently, since the 1990s, there were many reports of resistive memories utilizing Ag and chalcogenide electrolyte material, such as GeSe[44, 45], Ag_2S[46] and ZnCdS [47]. Due to the practical difficulties of integrating Ag and chalcogenide materials with standard CMOS processes, later research on resistive memories turned focus on Cu and CMOS-compatible materials such as a-Si and SiO_2 [16, 48]. Since 2005, there have been several demonstrations of integration of resistive memory cell and standard CMOS processes [49-51]. In 2012, resistive memory was firstly commercialized by Adesto® technology, as shown in Figure 2-7. The RM cell was referred to as CBRAM (conductive bridge RAM), which emphasises the role of conductive filament in resistive switching. The final product was a 2Mbit memory integrated with standard 130nm CMOS processes.

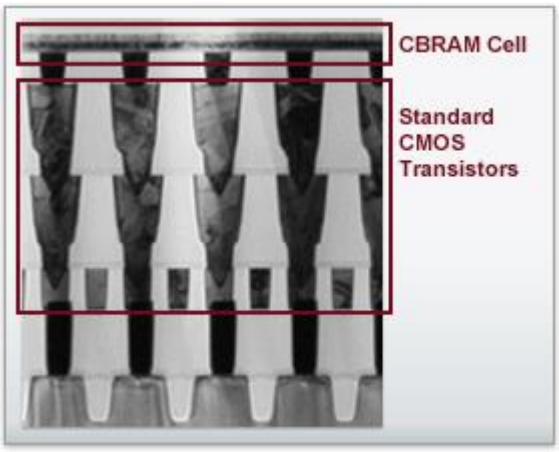


Figure 2-7 SEM image of RM cells integrated with standard 130nm CMOS transistors, from Adesto® website.

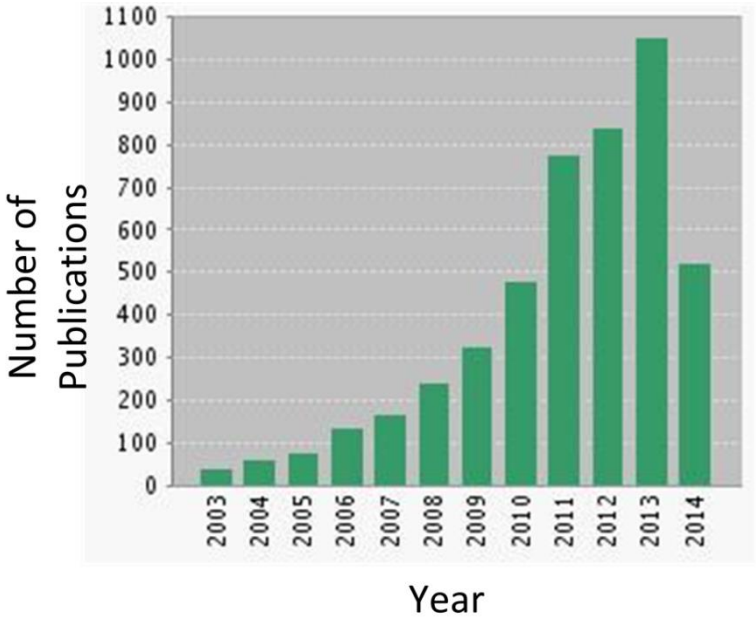


Figure 2-8 Number of articles related to resistive memories published each year since 2003, graph generated by Web of Science.

As shown in Figure 2-8, resistive memory has remained a popular research topic since 2003, with publications on the subject steadily increasing every year and totalling over 8000 in the last 10 years.

2.3 Operation of Resistive Memories

2.3.1 Resistive Switching Mechanism

Since the early observations in 1960s, a large number of metal-insulator-metal structures have been reported to show resistive switching behaviour, and several mechanisms have

been proposed to explain the resistive switching phenomenon [52-56]. Overall, resistive memories (RMs) based on electrochemical metallisation (ECM) effect are better understood, more mature with respect to industrialization and have proven scalability potential [7]. Consequently a large number of works focus on ECM RMs, and so does this project.

As an example, Figure 2-9 shows the operation of a generic RM cell: In an ECM RM cell, one of the metal layers is more chemically active and acts as active electrode (AE), and the other counter electrode (CE). The insulator layer between the two electrodes is usually referred as the solid electrolyte, although this layer may not contain metal ions, unlike conventional electrolyte.

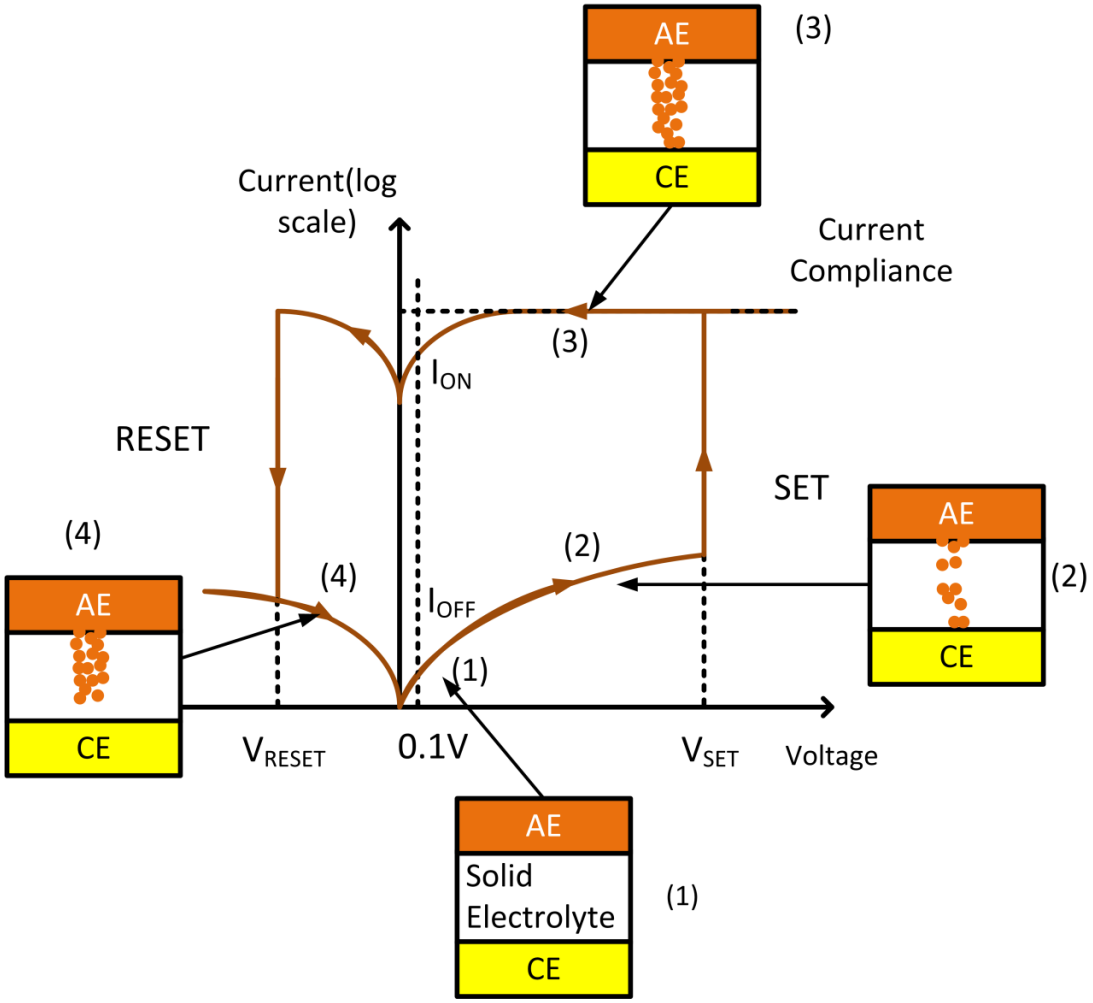


Figure 2-9 Operation of a generic RM cell. The switching directions are shown in arrows and the schematic drawings show the formation/dissolution of conductive filament at different stages of resistive switching cycle [7].

The operation shown in Figure 2-9 can be discussed in four stages:

1) Before applying voltage bias or when a small bias is applied, the as-fabricated RM cell starts in high resistance state (HRS), as the two electrodes are separated by the solid electrolyte layer.

2) When applied voltage exceeds a threshold, metal atoms at the AE is oxidized, and the metal cations migrate through the electrolyte to the CE. At the CE, metal cations are reduced to metal atoms.

3) The accumulation of metal atoms in the solid electrolyte eventually produces a conductive filament between the AE and CE and the resistance is significantly lowered [9, 57, 58]. The RM is now in low resistance state (LRS). The transition from HRS to LRS is referred to as SET and the voltage at which SET occurs is denoted as V_{SET}. This two-state resistivity can be electrically detected and serve as the basic of a memory device. Once the conductive filament is established, it remains stable without additional power supply, thus making the memory non-volatile.

4) To switch the memory to off-state, a reverse voltage is applied and the metal filament is electrochemically dissolved [59, 60]. The transition from LRS to HRS is referred to as RESET and the voltage at which RESET occurs is denoted as V_{RESET}.

In addition, to protect a RM device, during operation the current through device is usually limited by either a serial resistor or compliance current setting in the current source. The maximum current during SET is often referred to as programming current. R_{ON} and R_{OFF} are the resistance values of the RM in LRS and HRS, respectively. These values are normally measured by applying a small voltage bias (0.1V in Figure 2-9) and measure the corresponding current. Another key parameter of RM performance is ON/OFF ratio, which is the ratio of LRS current to HRS current, or equivalently R_{OFF}/R_{ON}.

The Electroforming Cycle

For a number of RMs, an initial electroforming cycle is needed before the device shows any switching behaviour. In this electroforming cycle the voltage required for SET and the OFF state resistance are both higher than in the subsequent cycles. As an example, Figure 2-10 shows a comparison of I-V curves from the electroforming cycle and the subsequent cycle of a $Cu/Ta_2O_5/Pt$ RM. The generally explanation for the differences of the electroforming cycle and subsequent cycles is as follows: In the electroforming cycle, a conductive filament is formed that connects the two electrodes. During the first RESET cycle, the

conductive filament is only partially dissolved, and the remnant of the conductive filament acts as a preferred path for the formation of filament in the subsequent cycles. Therefore in the subsequent cycles V_{SET} may be lower. The remnant of filament also reduces the overall distance between the two electrodes, and thus lowering the OFF state resistance. The formation and partial dissolution of conductive filament has been directly observed, as shown in Figure 2-11. After the first electroforming cycle, an Ag filament is formed between the Ag and Pt electrodes. And after the first RESET process, the filament largely remains and only the tip near the Pt electrode dissolves. The gap between the remnant and the Pt CE is clearly shorter than the thickness of the solid electrolyte. Electroforming cycle is usually undesirable for the application of RMs, as it creates a large discrepancy of switching parameters between the first cycle and the following cycles.

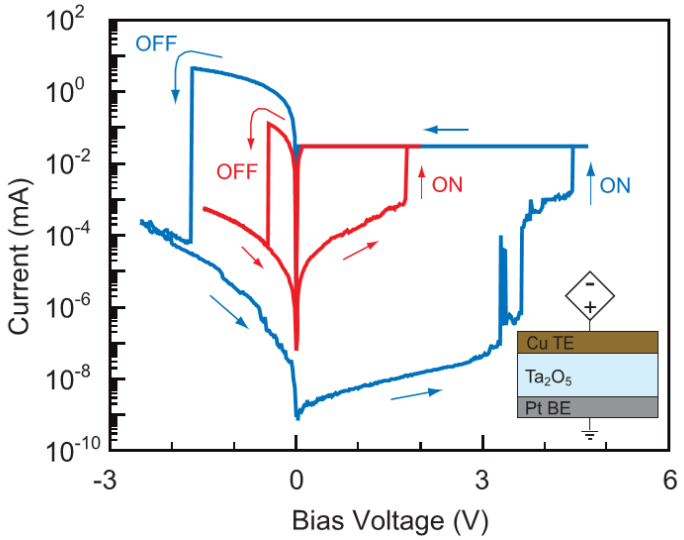


Figure 2-10 I-V curves of the electroforming cycle and the subsequent switching cycle from a $Cu/Ta_2O_5/Pt$ RM [61].

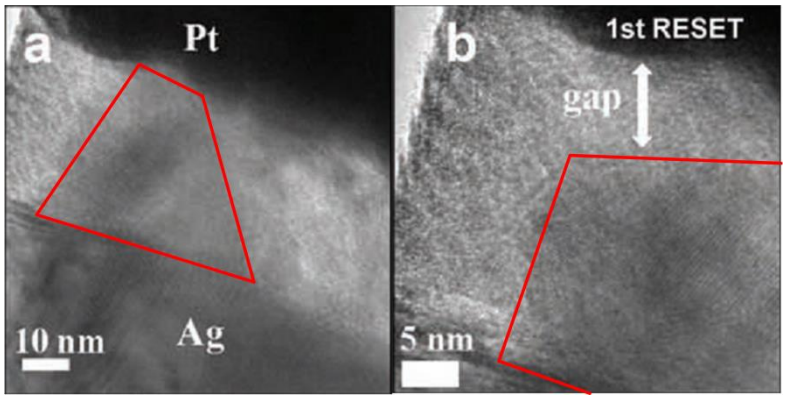


Figure 2-11 TEM observation of conductive filament after first electroforming cycle (a) and after first RESET (b) in a $Ag/ZrO_2/Pt$ RM, the red lines shows the outlines of the conductive filaments [62].

2.3.2 Switching Polarities

On the basis of I–V characteristics, the switching behaviours can be classified into three types: unipolar, bipolar and nonpolar [63]. As Figure 2-12 shows, in a bipolar switching cycle, SET and RESET processes require opposite voltage bias on the AE. On the other hand, in a unipolar switching cycle, SET and RESET can occur with voltage bias of the same polarity. A typical bipolar switching I-V curve is shown in Figure 2-13. The majority of RMs are reported to show bipolar resistive switching behaviour [61, 64-66], which can be expected from the ECM switching mechanism: conduction filament forms when AE is positive biased, and dissolves when negative biased.

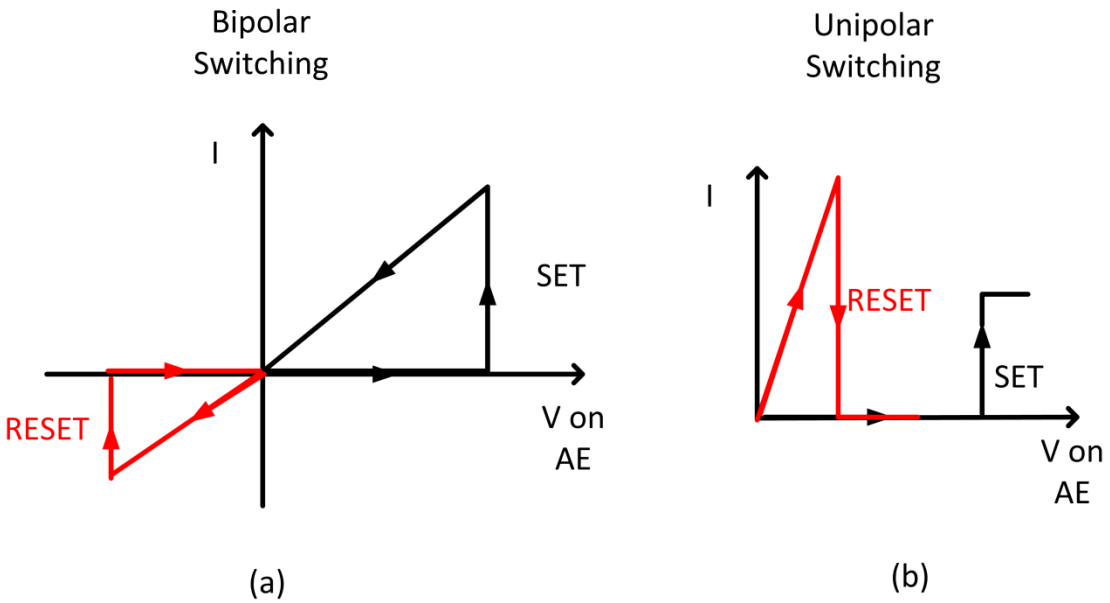


Figure 2-12 Simplified I-V characteristics of (a) bipolar resistive switching and (b) unipolar resistive switching.

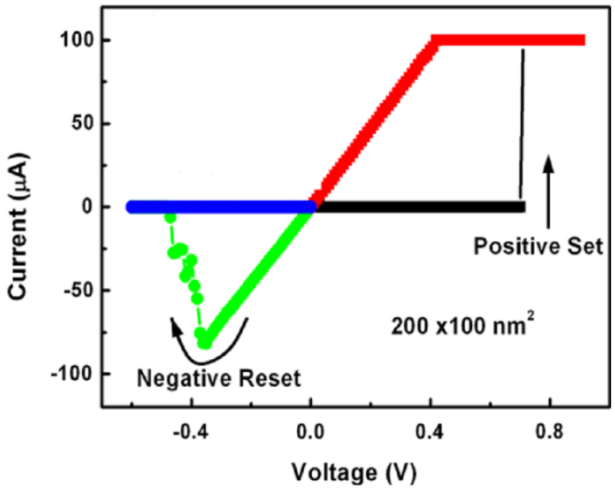


Figure 2-13 Bipolar resistive switching observed in a Ag/ZrO_2/Pt RM [67].

A number of RMs have also exhibited unipolar switching behaviour, as shown in Figure 2-14: SET and RESET can both occur when AE is positive biased [14, 65, 68-70]. The dissolution of conductive filament with positive bias is likely caused by Joule heating induced thermal diffusion [65, 68, 71]: the dimension of the conductive filament in RMs is generally in the order of several nms to 10s nms, therefore the Joule heating may raise the local temperature of the conductive filament to over 1000K [71, 72].

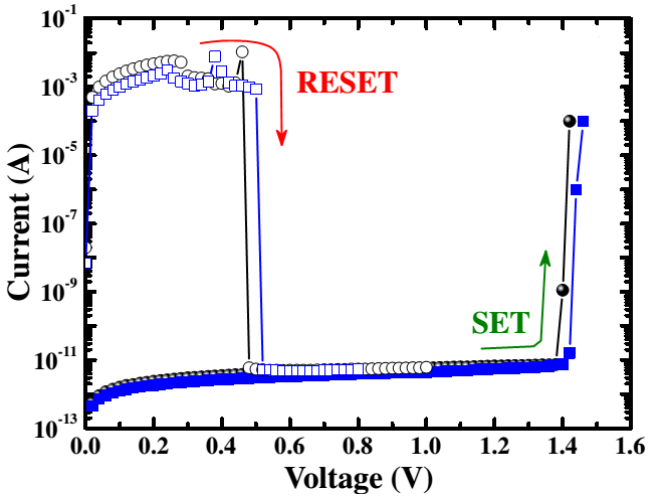


Figure 2-14 Unipolar resistive switching observed in a Cu/GeO_X/W RM [69].

Nonpolar switching typically means the coexistence of all four possible combinations of SET and RESET polarities, as shown in Figure 2-15 [73-75]:

- +bipolar: positive SET, negative RESET
- +unipolar: positive SET, positive RESET
- -unipolar: negative SET, negative RESET
- -bipolar: negative SET, positive RESET

RMs exhibiting nonpolar behaviour usually have a symmetric structure, or their solid electrolyte is doped with active metal [76, 77]. Relatively speaking, bipolar switching features faster switching speed, better uniformity and lower operation power[78], while unipolar switching presents higher ON/OFF ratios and presents advantages for high density integration[79]. Thus nonpolar RMs which exhibit both unipolar and bipolar switching behaviours have been considered advantageous as they can potentially expand application scopes of RMs[80].

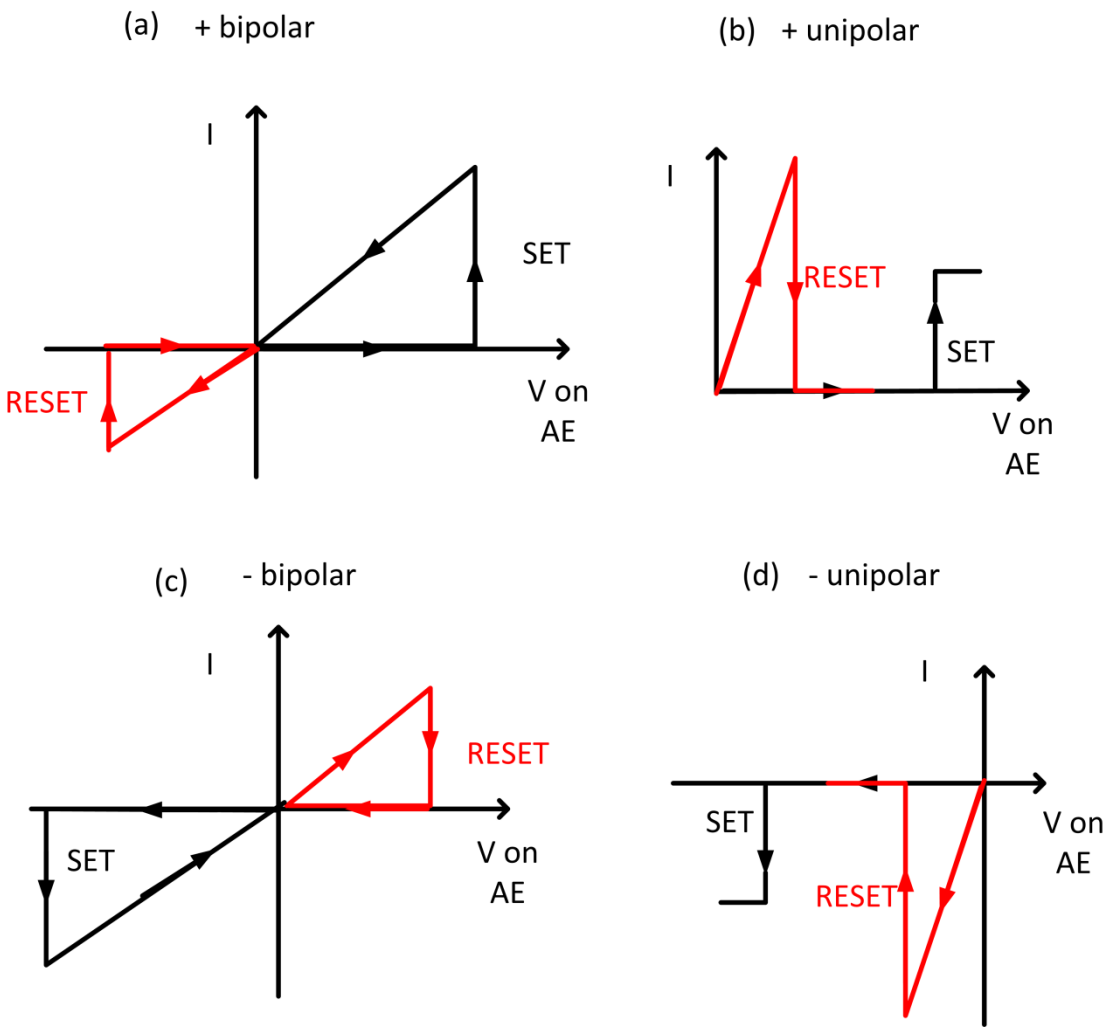


Figure 2-15 I-V characteristics of all four possible switching modes of nonpolar switching: (a) +bipolar, (b) +unipolar, (c) –bipolar and (d)-unipolar.

2.3.3 Conduction Mechanism of LRS

As discussed in the operation principle of RM, at LRS, the two electrodes are connected by a conductive filament composed of the active metal. Direct observations of these metallic filaments have been reported in a few studies, as shown in Figure 2-16 [62, 67, 81]: The TEM image clearly shows the existence of a nanoscale filament connecting the two metal layers. Furthermore, the EDS mapping confirms that the filament is largely consist of Ag. As LRS current is mostly conducted by the metallic filaments, RMs typically exhibit metallic Ohmic conduction at LRS.

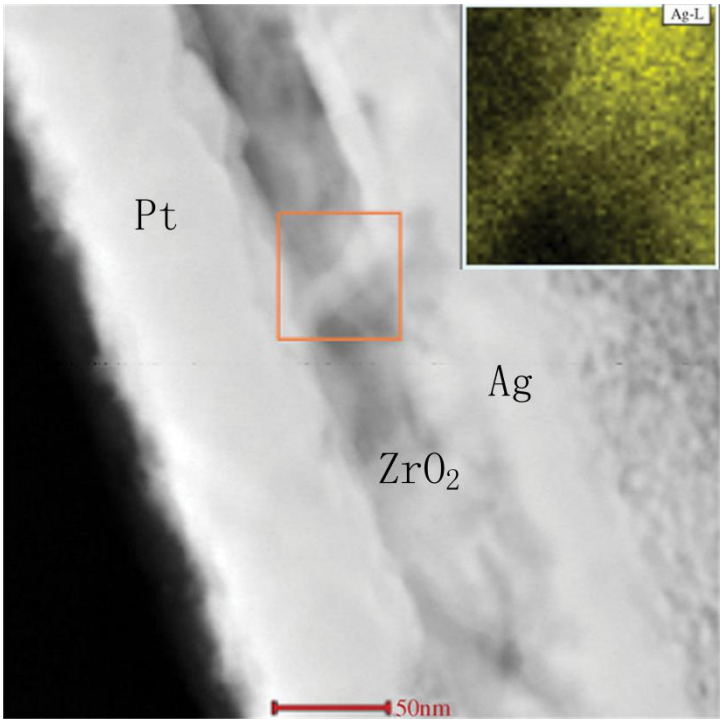


Figure 2-16 High resolution TEM image of the conductive filament in a Ag/ZrO_2/Pt RM, The inset is the EDS elemental mapping image of Ag element around the filament region [67].

To confirm Ohmic conduction mechanism at LRS, I-V curves of a RM device are often plot in log-log scale, as shown in Figure 2-17. From the plot, it is clear that at LRS, $\ln(I) \propto \ln(V)$, therefore $I \propto V$, indicating Ohmic conduction. Moreover, the temperature dependency of R_{ON} and R_{OFF} are often studied to investigate current conduction at LRS. Typically R_{ON} of a RM shows positive temperature coefficient, as can be expected from the metallic filament conduction. For example, as shown in Figure 2-18, in a Cu/NiOx:Cu/Pt RM, at HRS, the negative temperature coefficient of resistance clearly shows semiconductive behaviour, while at LRS, the linear relationship between resistance and temperature shows metallic characteristic.

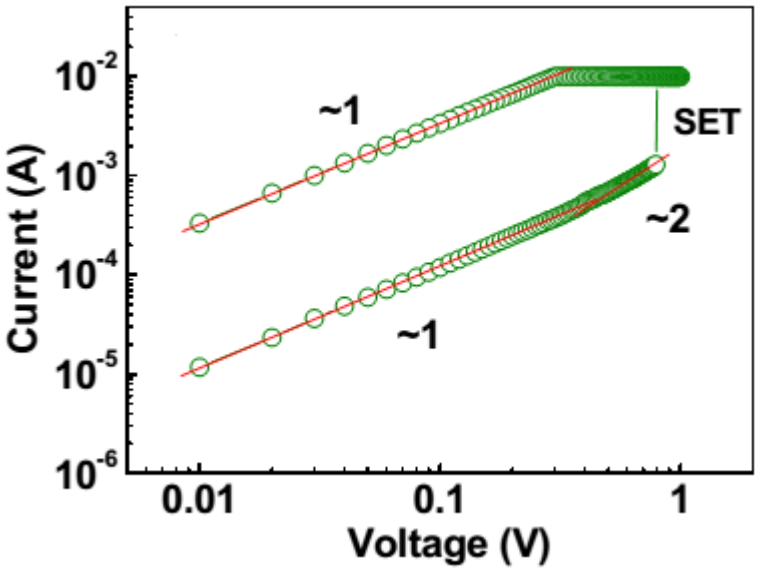


Figure 2-17 I-V curves of a Cu/graphene oxide/Pt RM, plotted in log-log scale with linear fittings [82].

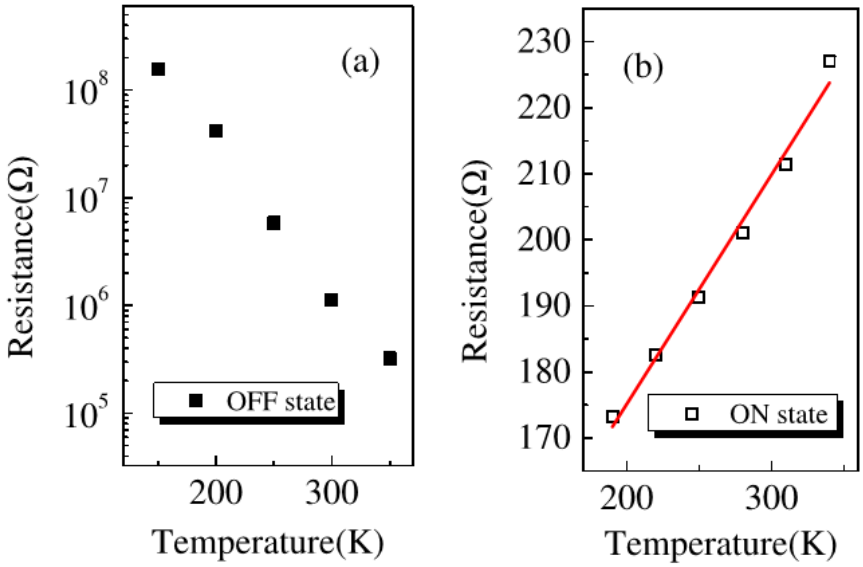


Figure 2-18 Temperature dependence of R_{OFF} (a) and R_{ON}(b) of a Cu/NiOx:Cu/Pt RM device [83].

On the other hand, as metal filament in a RM cell is quite challenging to be observed directly, analysis of LRS conduction, especially the different temperature dependence of R_{ON} and R_{OFF}, is often presented as indirect proof of filament resistive switching mechanism.

2.3.4 Conduction Mechanisms of HRS

A number of mechanisms may account for the HRS conduction, depending on the barrier height between metal and insulator, trap states in the insulator layer, temperature and

applied voltage[84, 85]. The followings are the more commonly reported HRS conduction mechanisms of RMs:

- **Fowler-Nordheim Tunnelling**

In F-N tunnelling, a high electric field is applied across the metal/insulator/metal structure, which creates a trapezoidal shaped barrier, and significantly reduces the effective thickness of the barrier. Electrons from metal are then much more likely to tunnel through the barrier, into the conduction band of the insulator. The expression for F-N tunnelling mechanism is [86]:

$$J = \frac{q^3 m_{eff}}{8\pi m_{diel} h q \phi} E^2 \cdot exp\left(-\frac{4\sqrt{2\pi m_{diel} q \phi^3}}{3\hbar q E}\right) \quad (2\text{-}1)$$

Where J is current density and E is applied electric field, m_{eff} is effective mass of electron in electrode, m_{diel} is electron effective mass in insulator, q is the unit charge of an electron, ϕ is the energy barrier height, h is the Plank constant and $\hbar$ is $h/2\pi$. From the equations, it's clear the current density is only dependent on the barrier height and applied voltage, and there is no contribution from trap states. The equations can be simplified to $\ln(I/V^2) \propto V^{-1}$, which can be used for linear fitting of I-V curves. An F-N tunnelling plot is shown in Figure 2-19:

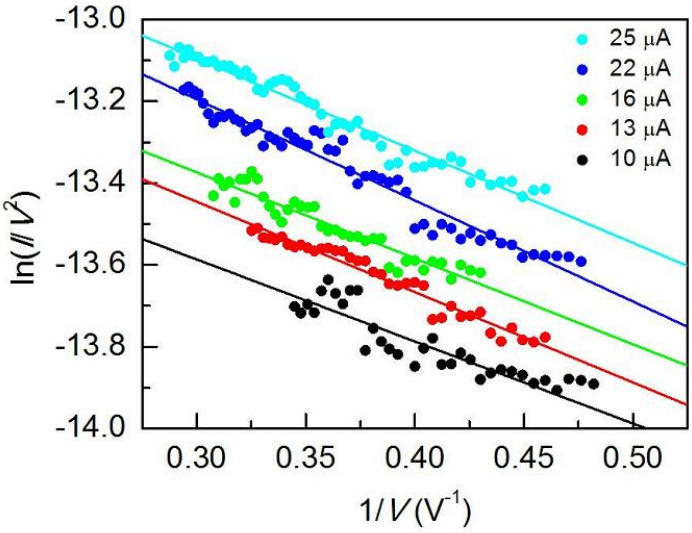


Figure 2-19 F-N tunnelling plot of HRS I-V observed in Cu/a-Si/p-Si RMs [87].

- **Poole-Frenkel Emission**

Similar to F-N tunnelling, P-F emission may dominate when there is energy barrier at metal and insulator interface, only P-F emission is due to field enhanced excitation of trapped electrons in the insulator layer to its conduction band. With the help of applied electric field, electrons from trapped states may be thermally excited into the conduction band of the insulator, and contribute to electric conduction. It is therefore often observed in insulators with a high degree of structural defects. The expression for P-F emission is[84]

$$J \propto E \cdot \exp\left[\frac{-q(\phi_B - \sqrt{qE/\pi\varepsilon_0\varepsilon_r})}{kT}\right] \quad (2\text{-}2)$$

Here J is current density, E is the electric field, q is the electronic charge, which are the same as in F-N tunnelling. ϕ_B is the depth of the trap potential well, e.g. energy difference between trap state and conduction band of the insulator. ε_0 is the permittivity of free space, ε_r is the relative dielectric constant, k is the Boltzmann's constant and T is the temperature. The equations can be simplified to $\ln(I/V) \propto V^{1/2}$, and from the slope of the linear fit ε_r of the particular solid electrolyte can be obtained. An example of such P-F emission plot is shown in Figure 2-20:

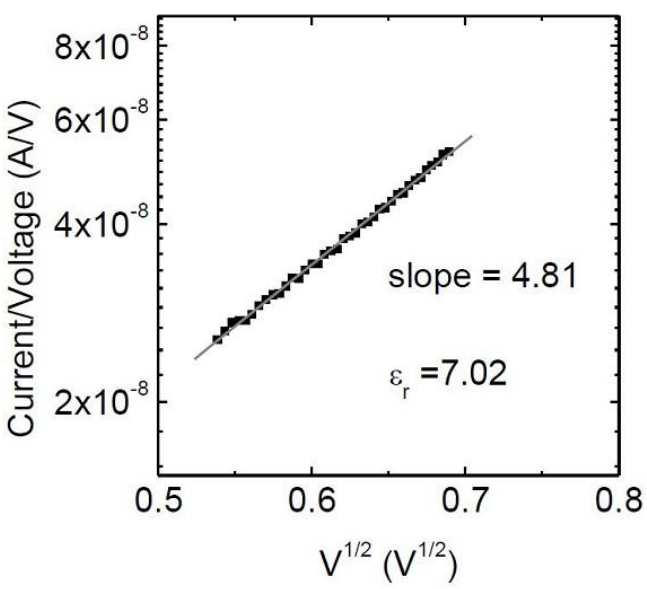


Figure 2-20 P-F emission plot of HRS I-V observed in a Cu/TaOx/Pt RM [61].

- **Schottky Emission**

The energy barrier at metal/insulator interface can also be overcome by the thermal energy of the charge carriers, and the thermal energy may come from high temperature

and applied electric field. This process is known as thermionic emission. Schottky emission is similar to thermionic emission process, only the Schottky effect of lowered barrier height by applied electric field is considered in Schottky emission theory. The expression for Schottky emission is [88]:

$$\mathrm{J} = A^* \cdot T^2 exp\left[\frac{-q(\phi_B - \sqrt{qE/4\pi\varepsilon_0\varepsilon_r})}{kT}\right] \quad (2\text{-}3)$$

Same as in F-N tunnelling, here J is current density, E is the electric field, q is the electronic charge, which is the same as in F-N tunnelling. ϕ_B is still the barrier height at metal/insulator interface. ε_0 is the permittivity of free space, ε_0 is the relative dielectric constant, k is the Boltzmann's constant and T is the temperature. A* here is effective Richardson constant, which is determined by the emitting material. The equation can be simplified as $\ln(I) \propto V^{1/2}$, as shown in Figure 2-21:

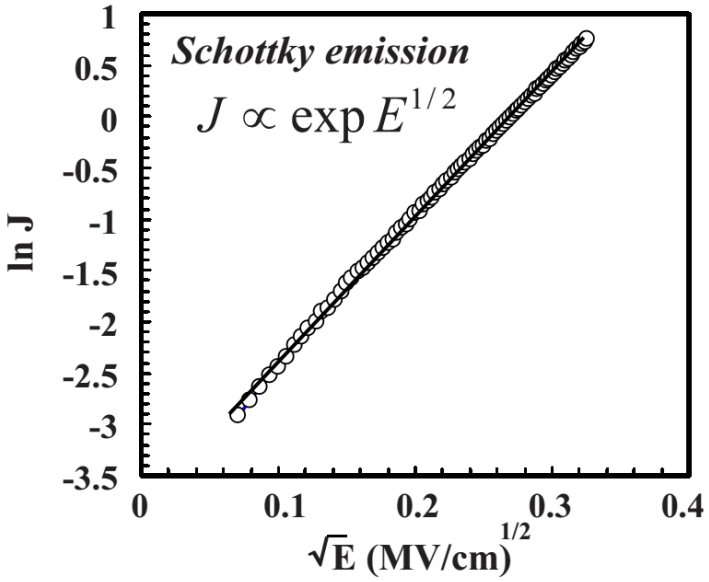


Figure 2-21 Schottky emission fitting of HRS I-V observed in a PT/SnO2/Pt RM [89].

Furthermore, from the Y-axis intercept of Schottky emission fitting, the barrier height at the interface can be estimated because $\ln(J_0) = \ln(A^* \cdot T^2) - \frac{q\phi_B}{kT}$.

- **Space Charge Limited Current**

All the above three mechanisms deal with scenarios where there is significant energy barrier between metal and insulator. If there is small or no barrier between metal and insulator, i.e., electrons from metal can be easily injected into the insulator, the electric

conduction is often dominated by space charge limited current. Assuming a completely undoped solid electrolyte, where all current is due to injected charge carriers, then the field inside the insulator will be the sum of externally applied field and the electric field from the injected charge carriers. Total current through insulator will be the equilibrium result from the electric field. The expression for space charge limited current is [90]

$$J_{SCLC} = \frac{9\varepsilon_0\varepsilon_r\mu V^2}{8d^3} \tag{2-4}$$

Here J_{SCLC} is the space charge limited current, ε_0 is the permittivity of free space, ε_0 is the relative dielectric constant, μ is the carrier mobility, V is the applied voltage across the solid electrolyte and d is the thickness of the electrolyte. This relationship is also known as Child's law. In addition, as dopant (intentional or unintentional) is usually present in the solid electrolyte layer, at low field, doping-induced carriers also contribute to the current. These carriers will not introduce space charge, as they are balanced by counter-ions from dopant. So when current conduction is dominated by space charge limited current, there is often a transition from ln(I)∝ln(V) at low voltage to ln(I)∝2ln(V) at higher field, as shown in Figure 2-22:

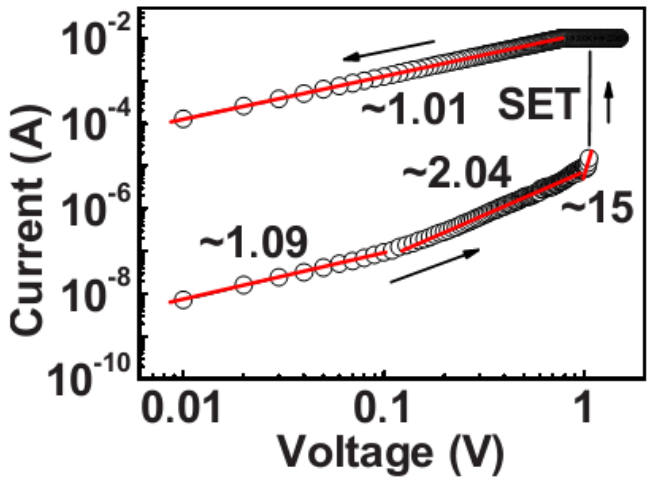


Figure 2-22 I-V curves in log-log plot, showing space charge limited current at HRS, observed in a Cu/a-C/Pt RM [91].

As can be seen from above discussions, analysis of HRS conduction mechanisms is not limited to electrical conduction only, but may also provide information on the properties of the solid electrolyte and the electrolyte/electrode interfaces. Fitting to Schottky emission mechanism has also been applied in this project to study the interface barrier

between a-SiC solid electrolyte and metal electrodes, and the results are shown in Chapter 5 and 6.

2.3.5 Effect of Programming Current

R_{ON} of a RM is often found to be strongly dependent on programming current, as is shown in Figure 2-23. This is probably because the total volume of metal filament is determined by the total amount of metal ions migrating through the solid electrolyte layer, which in turn is limited by the total charge transferred through the cell. Hence R_{ON} is dependent on programming current [60, 92].

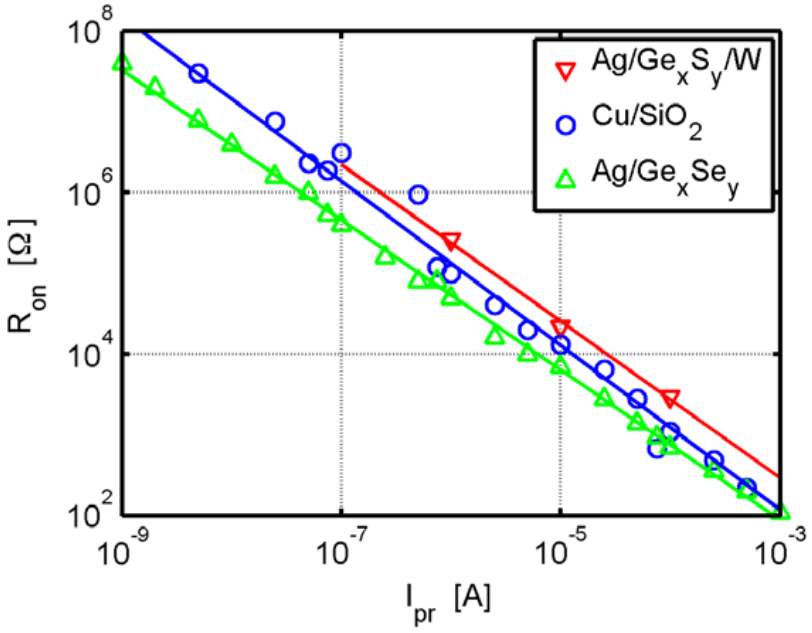


Figure 2-23 R_{ON} as a function of programming current [7].

Direct observation of dependence of filament size on the programming current has been recently reported, as shown in Figure 2-24. As the current compliance increases from 0.24nA to 20nA, the resulting filaments between the two electrodes clearly increase in volume. This relationship also presents the possibility of multi-bit storage in one RM device. In addition to HRS and LRS, by adjusting programming current, a RM device can be set to several intermediate states, which greatly increases storage density. On the other hand, as can be expected, when programming current is too low, LRS set in a RM device will become unstable, as the weak metal filament will quickly dissolve due to diffusion, even without external electric field [15].

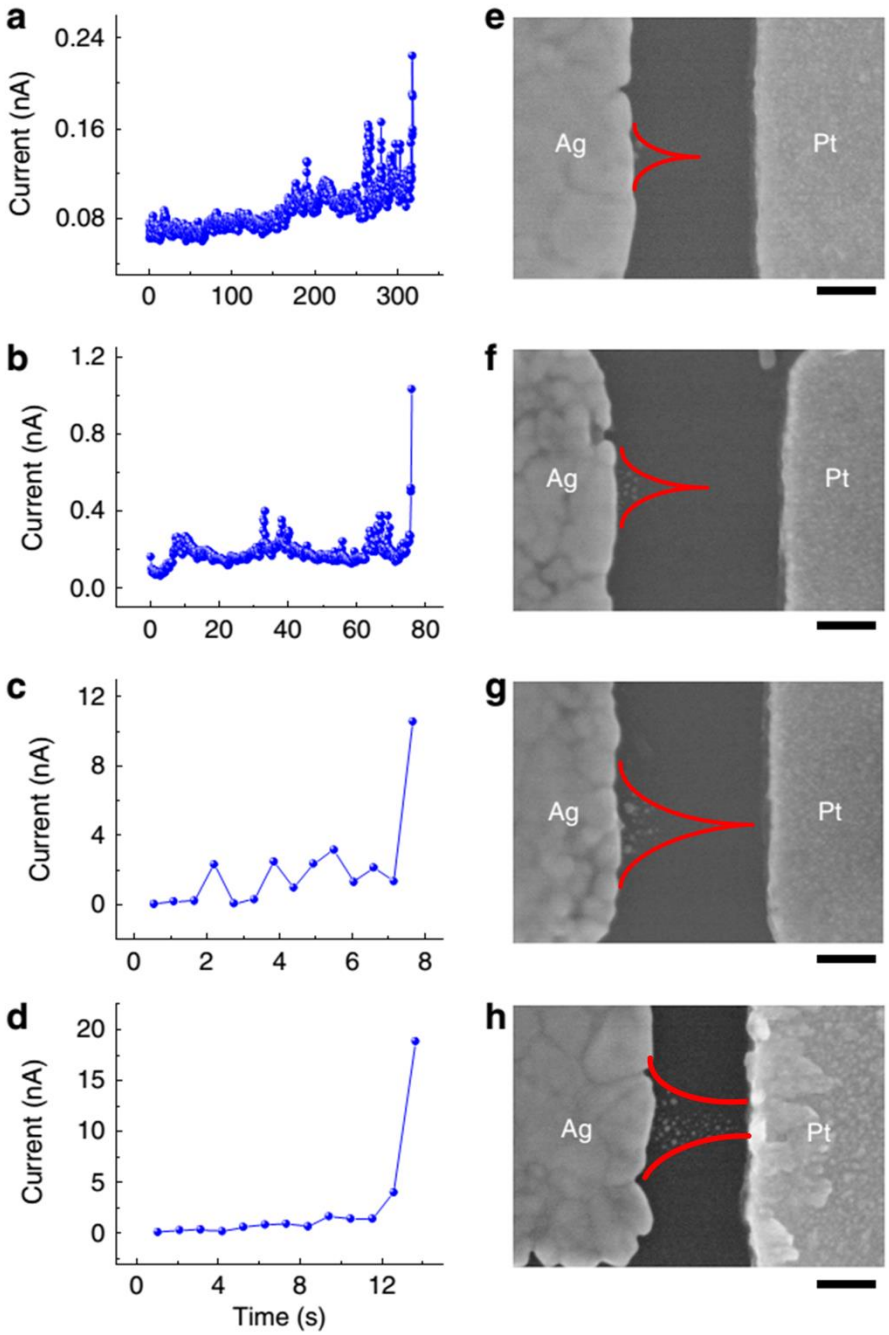


Figure 2-24 Observation of filament size controlled by the programming current: (a-d) I-t curves with different programming currents during the forming process and (e-h) the corresponding SEM images of the devices after SET [81]. The red lines are added to show the outlines of visible Ag filaments.

There have also been reports of R_{ON} being independent from programming current, especially with programming current lower than 1mA [93-95]. This is generally believed to be caused by current overshoot during the SET process. Due to various reasons such as parasite capacitor in the measurement setup, the actual current through RM during SET process can momentarily exceed the current compliance, as shown in Figure 2-25: The current compliance is 100μA while the maximum current during SET is near 1mA.

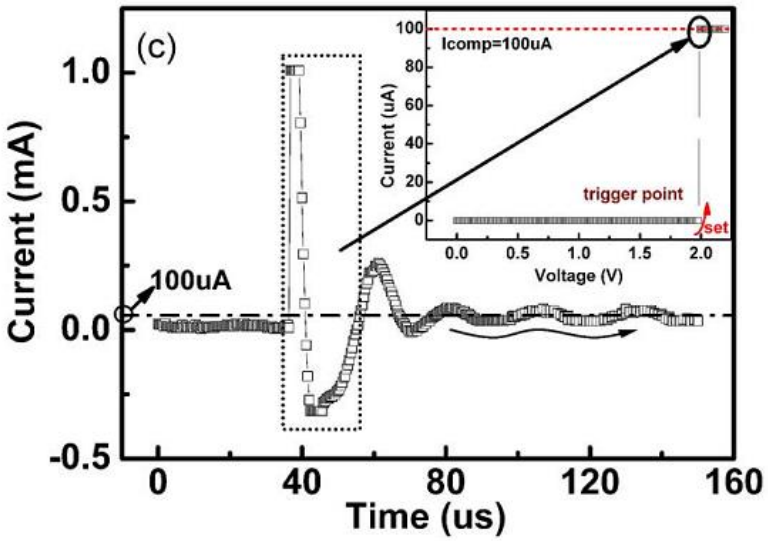


Figure 2-25 Current overshoot phenomenon observed in a TaN/Cu_xO/Cu memory device: The current compliance is 100μA while the maximum current during SET is near 1mA [93].

2.3.6 Effect of Device Area

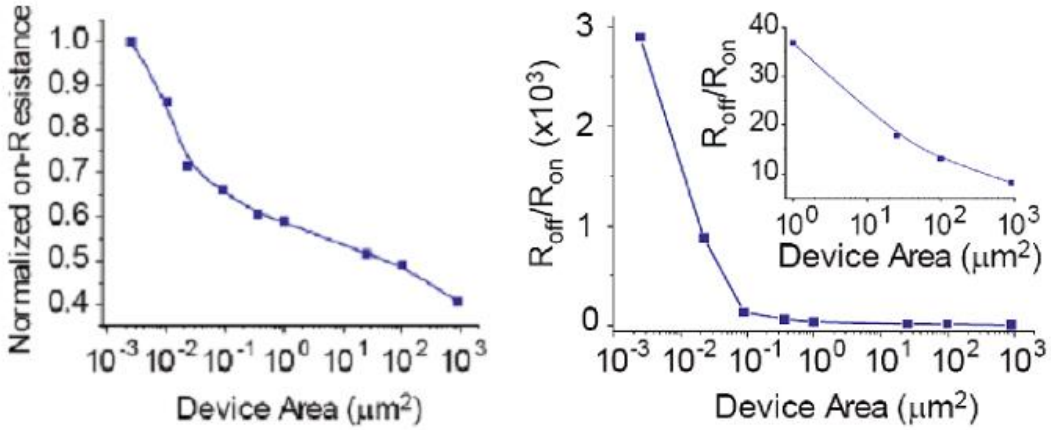


Figure 2-26 (a) R_{ON} independent on device area (b) R_{OFF} dependent on device area, data from a series of Ag/a-Si/p-Si RM devices.

Another characteristic of RM device is that its on-state resistance is in principle independent on device area, while its off-state resistance is dependent on device area, as shown in Figure 2-26. In Figure 2-26(a), R_{ON} change less than 2.5 times while the device area change over 6 orders of magnitude. On the other hand, in Figure 2-26(b), ON/OFF ratio of devices change over 300 times, indicating R_{OFF} is strongly linked to device area. This is directly caused by its conduction mechanism at two states: at LRS, the current is carried by a metal filament, and it's generally agreed the diameter of the metal filament is in the order of several nanometers to tens of nanometers, which is independent to the device area. At HRS, without metal filament, current through solid electrolyte layer is due

to tunnelling current, which is directly proportional to the overlay area of the two metal electrodes.

The independence of R_{ON} on device area gives RM devices great potential of scalability, as the ON/OFF ratio actually improves while the devices shrink down. Also, this suggests that in principle, device areas can be potentially as small as the metal filament, which is generally believed in the nm range. Recent simulation of resistance of nanoscale filament puts the lower limit of lateral area of RM at 3~5nm^2 [96]. This leads to the great potential of RM in high density data storage. Furthermore, as direct observation of metallic filament (using AFM or TEM) is quite challenging, this independence of R_{ON} and dependence of R_{OFF} to device area is often used as supporting evidence to demonstrate filament switching mechanism in RMs.

2.3.7 Effect of Solid Electrolyte Thickness

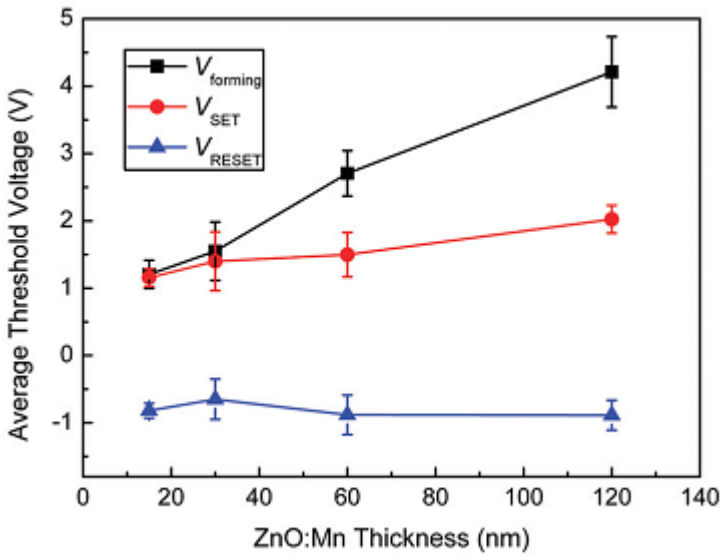


Figure 2-27 Forming voltage and subsequent switching voltages as a function of solid electrolyte thickness, observed in Cu/ZnO:Mn/Pt RMs [65].

Several studies have reported a correlation between the electroforming voltage (V_{form}) and solid electrolyte layer thickness [65, 97]. As shown in Figure 2-27. forming voltage is linearly proportional to solid electrolyte thickness, while the subsequent setting voltages are almost independent on the solid electrolyte thickness. The linear relationship between V_{form} and solid electrolyte thickness indicates the forming process is determined by the electric field across the solid electrolyte layer. As for the independence of set voltage on solid electrolyte thickness, a likely explanation is that after the first forming cycle, the metal filament is not completely dissolved, i.e. the filament only breaks at certain points.

The subsequent set processes will only have to provide metal ions to connect these broken links.

2.3.8 Retention Tests of RMs

For novel non-volatile memories, state retention over 10 years at 85°C is required to be competitive against Flash memory, and this standard has been widely accepted to assess and compare stabilities of various RMs [1, 98]. As the LRS conduction of a RM relies on nano scale conductive filaments, the main failure mechanism for RM is generally believed to be the dissolution of metal filament due to diffusion [99]. In line with this, it has been reported that the HRS of conductive filament based RMs is quite stable for an extended period of time, even at elevated temperature. Nevertheless, LRS resistance of these RMs [7] suffer from rapid increase with time following the power-law:

$$R_{ON} = Bt^m \tag{2-5}$$

where m is larger than 0 [99], leading to poor stability and retention. A commonly adopted method of predicting retention performance is to monitor device's resistance over a short period of time at elevated temperature, and extrapolate the power-law dependence to 10 years' time. Figure 2-28 shows an example of this method.

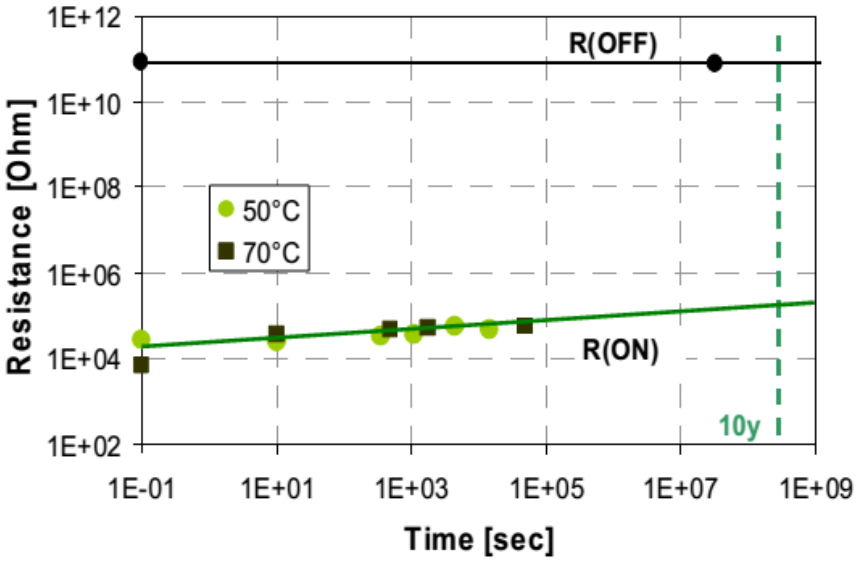


Figure 2-28 State retention measured at elevated temperatures and estimation of retention over 10 years of a Ag/GeSe/W RM [100].

2.4 Device Structures and Possible Memory Architectures

The structures of actual reported devices are largely determined by consideration of potential integration of RM elements and CMOS circuitry. A working RM can be formed by an active array of RM cells or a passive array, and accordingly most of the reported RM element have either a via-stack structure or a crossbar structure [101]. Figure 2-29 shows the schematics of these two structures: in a via-stack RM, the device active area is defined by the via-hole in the insulator layer, and the two metal electrodes are usually part of the CMOS metallization layers. In a RM with cross-bar structure, the device active area is defined by the overlay area of the two thin lines of AE and CE.

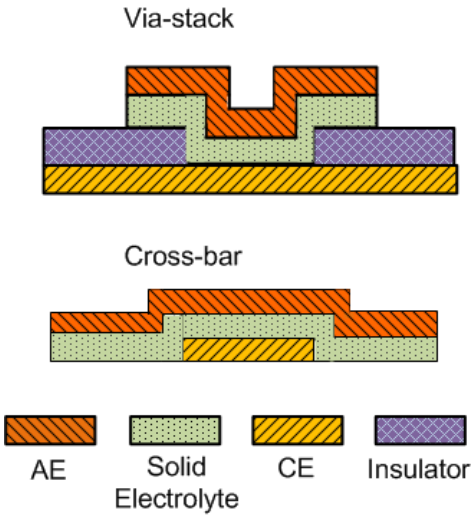


Figure 2-29 Schematic of cross-section of RMs with via-stack structure and cross-bar structure. .

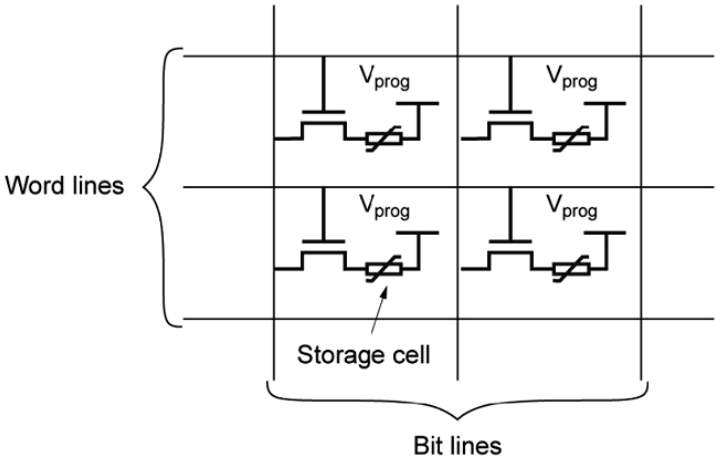


Figure 2-30 Active array of "1T1R" (1 transistor, 1 resistor) RM cells [7].

In an active array, a RM cell consists of a RM element and a selection transistor, as shown in Figure 2-30. The word lines are connected to the gates of selection transistors, and the

bit lines to the drains. An individual RM element can be selected by applying voltage bias on its word line and its bit line, and the state of the RM element is controlled by the programming voltage.

A number of studies have demonstrated typical via-stack RMs in this configuration, as shown in Figure 2-31 [48, 66]: The $Cu/Cu_2O/TiN$ RM element is formed in the via holes. The Cu and TiN electrodes are both the intrinsic elements of the CMOS metallization layers, only the Cu_2O solid electrolyte requires extra fabrication steps. RMs in this via-stack structure are therefore relatively easy to be integrated in the conventional CMOS fabrication process [16]. As the RM element is directly on top of CMOS circuitry, the area of an individual 1T1R cell is limited by the dimensions of the CMOS transistor.

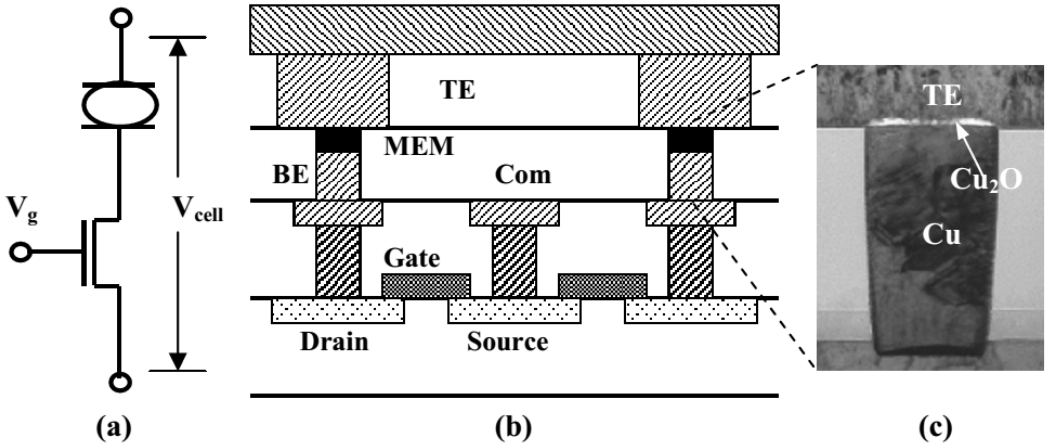


Figure 2-31 (a) illustration of a "1T1R" RM cell, (b) schematic drawing of the structure of a cell array, (c) TEM image of a integrated Cu_2O RM cell [49].

On the other hand, RM cells are generally expected to scale even further than CMOS transistors. Therefore to maximise the scaling potential of RMs, a large number of studies focus on RMs with a crossbar structure, such as the one shown in Figure 2-32 [12, 66, 101-104]. In an array of crossbar structured RMs, each overlapping area of electrodes is one RM element, and there is no longer a transistor in each memory cell (hence the array is "passive"). Scaling of crossbar RMs is therefore not limited by the scaling of CMOS circuitry, and it is generally believed crossbar structures present the highest possible device density [12]. In addition, as the CMOS selection circuitry is no longer integrated in the individual memory cells, three dimensional integration of crossbar RM layers and the CMOS circuitry has been proposed, as shown in Figure 2-33. Clearly such three dimensional RMs will further improve the storage density.

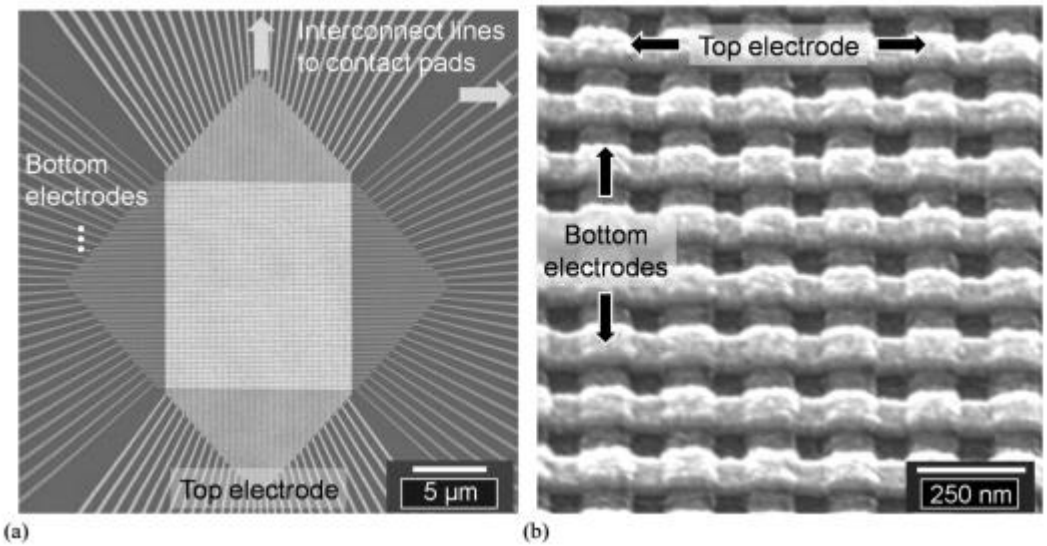


Figure 2-32 (a) SEM top view of a 64 by 64 crossbar RM array, and (b) a detailed side view of the array [104].

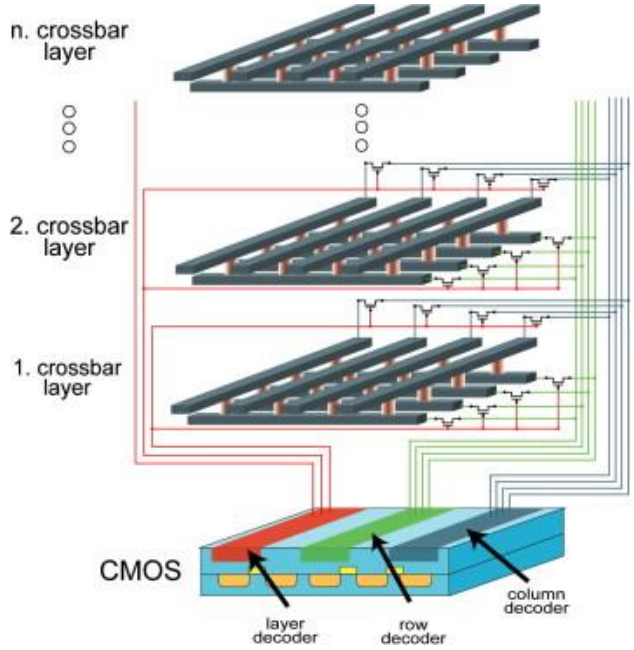


Figure 2-33 A proposed three dimensional configuration of crossbar RMs coupled with CMOS circuitry [102].

Despite the clear advantage in storage density, crossbar RM elements are not isolated from each other, and this creates the possible issue of sneak current, as shown in Figure 2-34 [105, 106]: The red element is at HRS and all green elements are at LRS. When the red element is chosen by the applied bias, the read current should be very low to reflect the HRS. However as all the surrounding elements are at LRS, there will be sneak current through these elements and the resulting read current will indicate the selected element is at LRS. To eliminate such sneak current in crossbar RM arrays, several methods have been proposed, for example a diode can be integrated in a RM cell to only allow current flow in

one direction [13, 53, 107]. As both via-stack structure and crossbar structure has its unique advantages and disadvantages, RMs of both structures will be explored in this project.

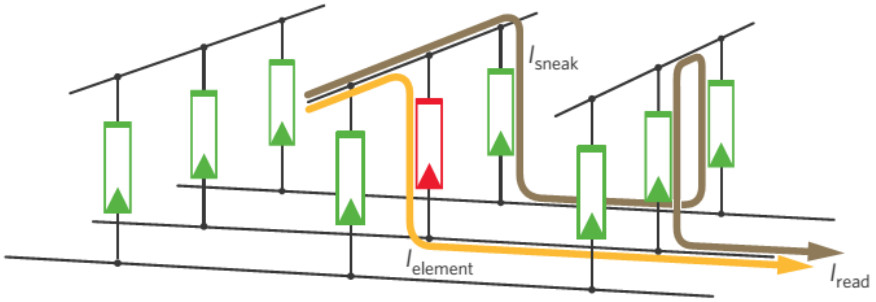


Figure 2-34 Sneak path in a passive crossbar RM array. The red element is at HRS and all green elements are at LRS. The yellow arrow shows the intended read current and the brown arrow the sneak current [105].

2.5 Materials for Resistive Memory

Active Electrode Material	Solid Electrolyte	Counter Electrode Material	References
Cu	SiO_2	Al	[108]
	WO_3	W	[48]
	a-C	Pt	[91]
	a-Si	Doped Si	[87]
	a-SiC	Pt	[18, 19]
	ZrO_2	Pt	[73, 109]
	ZnO	Pt	[65, 110, 111]
	HfO_2	Doped Si	[59]
	HfO_2	Pt	[83, 112]
	AlO_X	W	[113]
	GeO_X	W	[114]
	Cu-Ge-S	Pt	[115, 116]
	GeTe	TaN	[117]
Ag	GeSe	W	[98, 118]
	GeS	W	[51]
	As_2S_3	Au	[119]
	a-Si	Doped Si	[11, 120, 121]
	ZrO_2	Pt	[67]
	ZrO_2	Au	[122]
	ZnO	Pt	[123]
Ni	HfO_2	Doped Si	[59]

Table 2-2 Summary of reported typical combinations of RM materials.

As a very wide variety of materials have exhibited resistive switching behaviour, Table 2-2 only shows a limited selection of the more typical combinations of RM materials to present an overview of RM materials.

2.5.1 Metal Electrode

- **Active Electrode**

The active metal in an ECM RM need to be easily electrochemically oxidized to metal ions and the ions needs to be reduced at the counter electrode. The oxidation and reduction reactions also need to be controlled by a reasonable voltage bias. Due to these requirements, most RMs are based on Ag or Cu as the active metal, although other electrochemically reactive metals, such as Ni, have also been explored as RM active metal. Moreover, Cu is now widely used in CMOS metallization, and its relevant fabrication processes, such as diffusion barrier, are well developed [20, 124, 125]. Therefore Cu as active electrode material has the additional benefit of CMOS compatibility.

- **Counter Electrode**

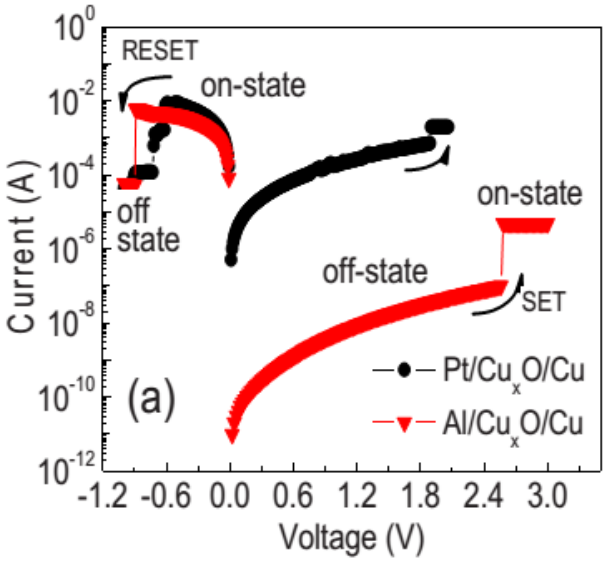


Figure 2-35 Comparison of I-V curves of Cu/CuxO/Pt and Cu/CuxO/Al RMs [126].

On the other hand, a larger selection of materials has been used as counter electrodes. In most studies, CE materials were chosen largely for their chemical stability. Nobel metals such as Pt and Au are therefore a very common choice among fundamental researches. W and TiN are also often seen in researches aiming for CMOS compatibility. The influence of CE material on device performance, however, has not received much attention among

studies. As the LRS current is mostly conducted by metallic filament, CE material has limited effect on LRS conduction, but CE material can have a significant impact on HRS conduction, as shown in Figure 2-35 and Figure 2-36.

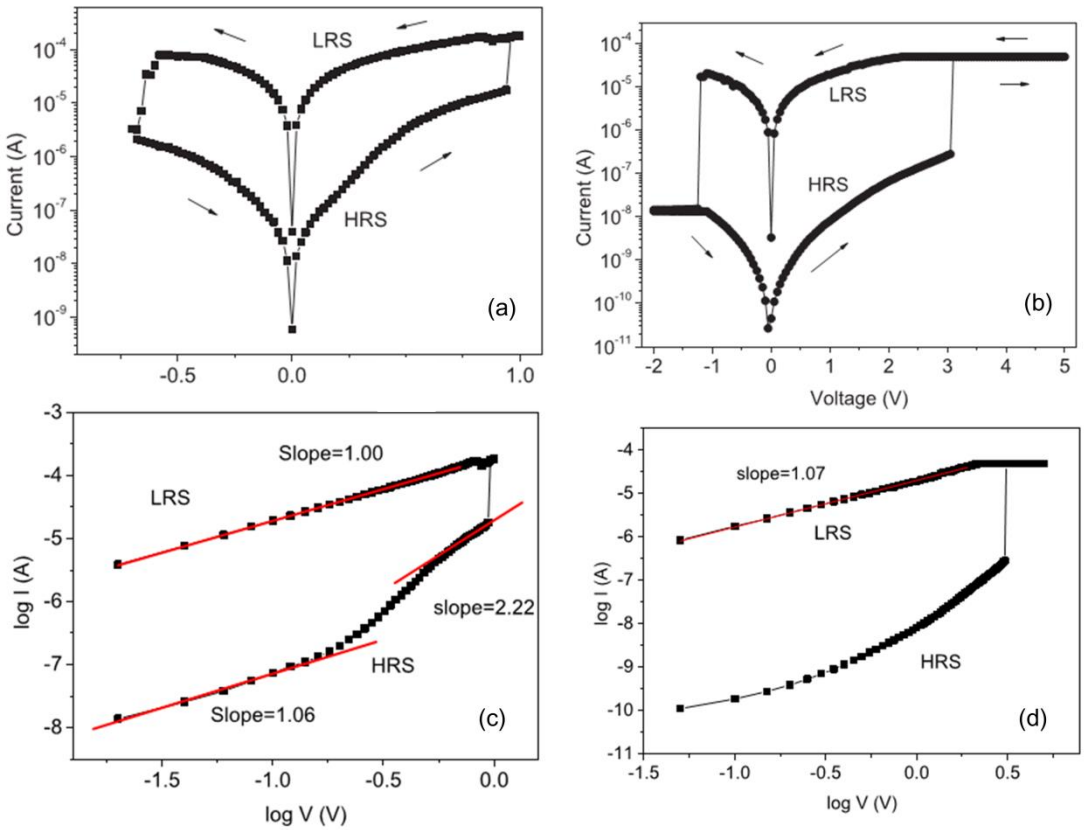


Figure 2-36 (a) I-V curves and (c) I-V curves in log-log scale of a Cu/SiO_2/Pt RM and (b) curves and (d) I-V curves in log-log scale of a Cu/SiO_2/Al RM [108].

In Figure 2-35, the ON-state I-V of the two RMs with different CE materials are quite similar, while the R_{OFF} and V_{SET} of the one with Al CE is considerably higher. This is possibly caused by a thin layer of Al oxide at the interface between Al CE and Cu_xO solid electrolyte. Similarly in Figure 2-36, the R_{OFF} and V_{SET} of the one with Al CE is also noticeably higher and was also attributed to the Al oxide layer. The two RMs also shown different conduction mechanisms at HRS: space charge limited current for the one with Pt CE, and Schottky emission for Al CE. From these examples, it can be seen that HRS current can be limited, and therefore ON/OFF ratio increased, by engineering the solid electrolyte/CE interface.

2.5.2 Solid Electrolyte

- **Chalcogenides**

In the earlier researches on RM devices, the solid electrolyte layer is often chalcogenides with active metals (Ag or Cu) dissolved in them [115, 127-129] The metal atoms react with the chalcogen to form metal ions, therefore there is already metal ions in the solid electrolyte layer before the electrochemical oxidation of active electrode. When relative negative voltage is applied to the counter electrode, the mobile metal ions in the solid electrolyte near CE can start the reduction reaction and nucleation on CE in nanoseconds, and the metal filament gradually grows from CE to AE to form a complete conduction path. Diffusion of metal ions from AE to CE is less likely to be the limiting factor of switching speed. Also, the metal filament does not need to penetrate the whole solid electrolyte layer, but only need to connect the ion rich regions. All these features enable RM devices based on metal doped chalcogenides to switch fast (several ns) at low voltage (<1V) [9].

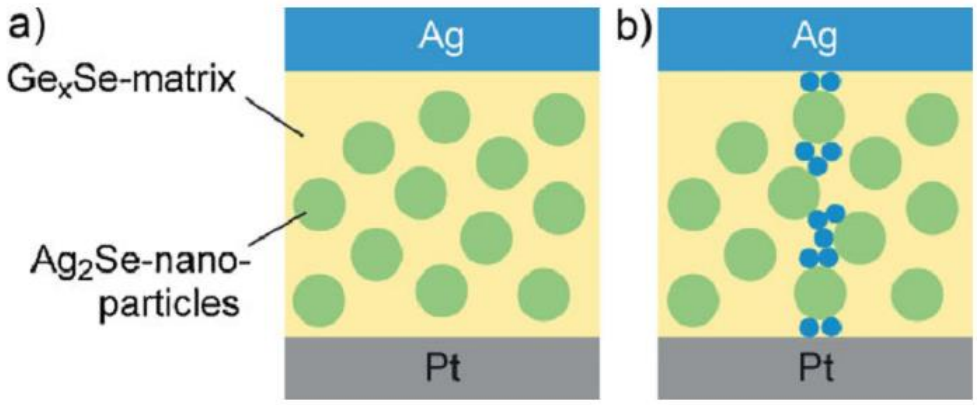


Figure 2-37 Sketch of filament formation in a GeSe matrix with Ag rich regions with (a) showing HRS and (b) LRS [9].

- **Amorphous Insulators and Oxides**

Despite these advantages from metal doped chalcogenides as solid electrolyte material, the process of dissolution of metal into chalcogenide can be challenging for the process integration with CMOS [7, 10]. Moreover, V_{SET} and V_{RESET} of RM_S based on chalcodenides can be undesirably low (<0.2V), that these devices may be incorrectly switched during normal operation [130]. Later researches therefore turned focus onto some of the well-studied insulator/semiconductor as solid electrolyte material, such as SiO_2 [14, 15, 17, 97], ZrO_2 [67, 73, 109, 131, 132] and a-Si [10, 12, 87, 100, 133]. One definitive difference of

these materials usually do not contain ions of active metal. An electroforming process is therefore often required before the device can perform normal resistive switching.

In addition, in RM devices lacking metal ions in the solid electrolyte layer, diffusion of metal ions is more likely to be the limiting factor in the SET process. Figure 2-39 shows a series of TEM images taken during the SET process of an Ag/a-Si/W. The filament growth is found to start from the Ag AE, and the filament has an overall cone-like shape, with the narrow end near W CE. Similar growth pattern has been observed in several other RMs [62, 64, 134], and the filament growth mechanism is summarized in Figure 2-39. Essentially due to the relatively low ion mobility in these amorphous materials, the metal ions will only travel a short distance from the AE when they encounter the tunnelling electrons and are reduced back to metal atoms. The accumulation of metal atoms then serve as a preferred site for further ion migration/reduction, as the effective distance between electrodes is reduced and the electrical field is enhanced locally.

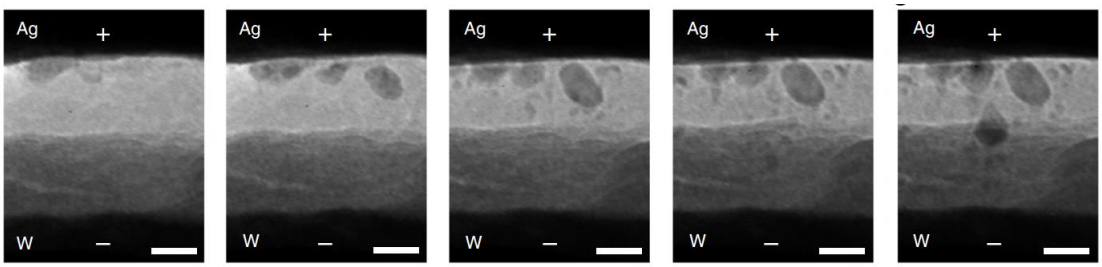


Figure 2-38 Real-time observation of filament formation in an Ag/a-Si/W RM [81].

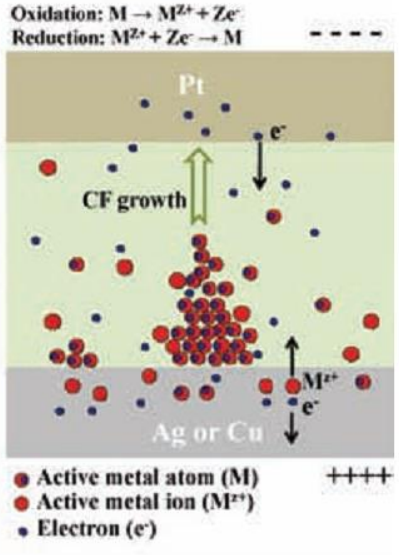


Figure 2-39 Sketch of filament formation in an Ag/ZrO_2/Pt RM, summarised from TEM observation [62].

- **Doping of Solid Electrolyte Layer**

Due to the limitations of amorphous insulators and oxides as solid electrolyte, there has been great interest in improving RM device performance by doping solid electrolyte material with metals. The most obvious reason to add metal in the solid electrolyte layer is to provide active metal ion during filament formation. Without the additional metal-rich regions or metal nano particles, all metal ions are supplied by the active electrode, and driven to the counter electrode. This requires higher voltage, especially during the first switching cycle [129].

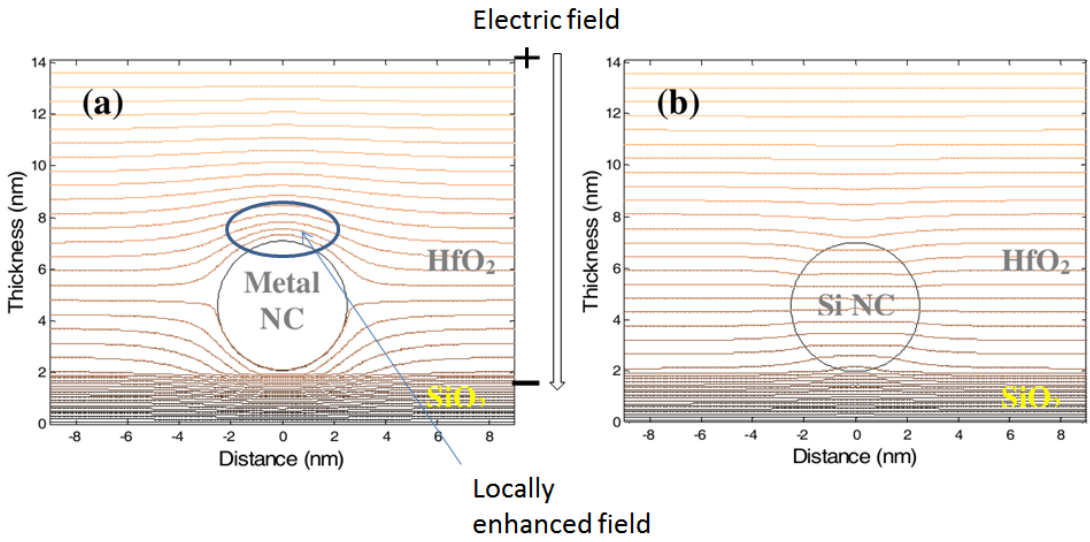


Figure 2-40 Simulated electric field distribution in HfO_2 with (a) metal nano crystal and (b) silicon nano crystal [3].

The existence of metal rich regions within the solid electrolytes can potentially promote metal filament formation through the following possible mechanisms [135-138]:

• Increase structural defects in the solid electrolyte.

• Reduce effective thickness of solid electrolyte layer.

• Enhance the local electric field.

Figure 2-40 shows the effect of electric field enhancement in HfO_2 with embedded metal nano crystal [3]. The direction of electric field is from the top of the figure to the bottom. Each spacing between the contour lines represents 0.2V electric potential. The spacing between the contour lines around the top of metal nano crystal are significantly narrower than in the other regions of HfO_2 layer, indicating the electric field around this point is higher. This effect is simply caused by the fact that there is no internal electric field in metal object placed in electric field, as electrons in metal can move freely. With higher

electric field around metal nanoparticles, metal filament is more likely to form in this region during switching, thus reducing the randomness of forming process in repeated cycles.

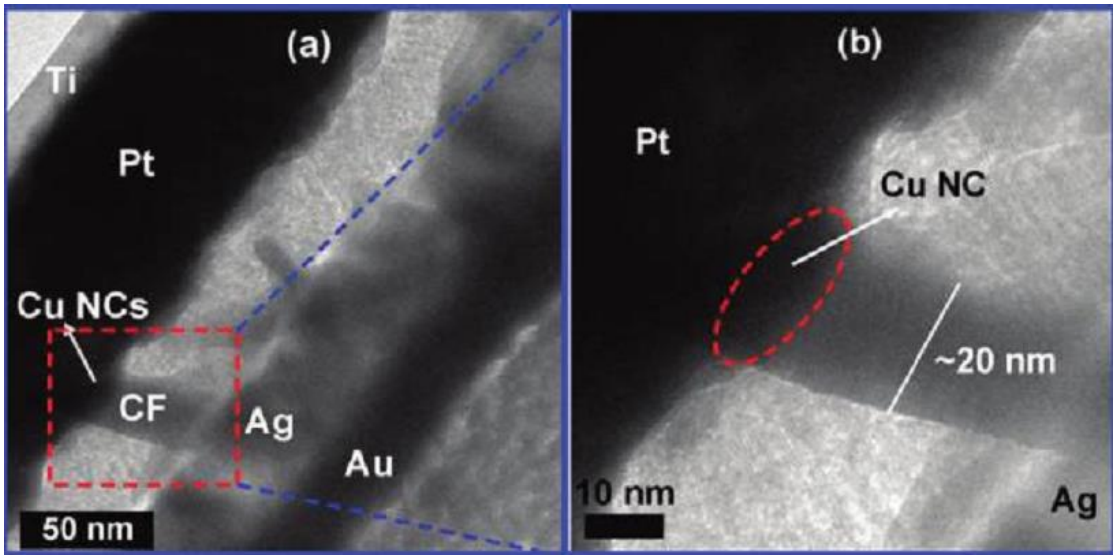


Figure 2-41 TEM images showing guided filament growth by Cu nanocrystal in Ag/ZrO_2/Pt RM [139].

Due to these effects, metal dopant in solid electrolyte often acts as growth seed, or preferred growth site for metal filaments. Figure 2-41 shows an example of guided filament formation in Ag/ZrO_2/Pt cell. The bottom electrode (Pt) is decorated with Cu nano crystals, and the TEM image shows Ag filament is indeed formed at the site of Cu nano crystal [139]. Such guided filament formation has also been referred as "lightning rod effect" [140].

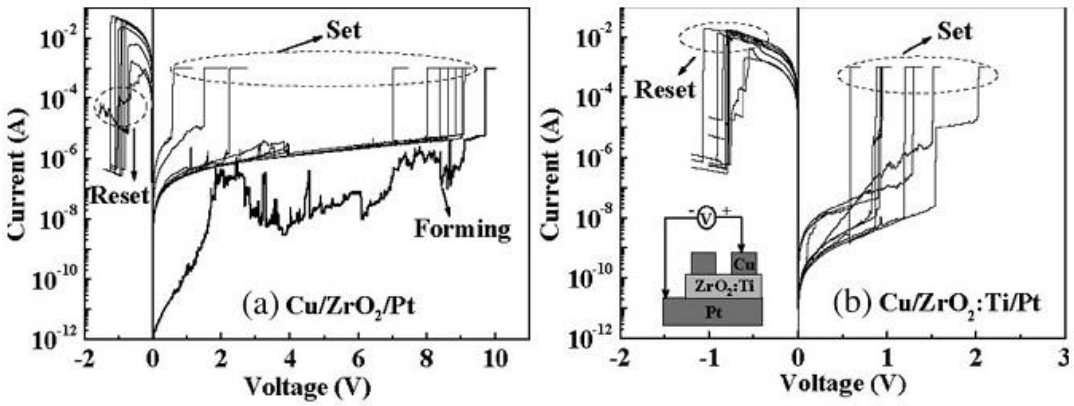


Figure 2-42 Improved switching uniformity in Cu/ZrO_2/Pt PMC by implanting Ti ions in ZrO_2 [141].

With dopant metal creating preferred growth path for the metal filament, the randomness of filament growth during resistive switching can be reduced, and the uniformity of switching parameters can be improved. Moreover, with effective thickness of the solid electrolyte reduced and local electric field enhanced, the switching voltage can also be reduced. Figure 2-42 shows the effects of implanting Ti ions in ZrO_2 solid electrolyte layer in Cu/ZrO_2/Pt RM device [141]. In device without Ti ion implant, the forming voltage is close to 10V, and V_{SET} in the subsequent cycles can range from <1V to >9V. While in device with Ti implanted ZrO_2 layer, forming voltage is reduced to ~2V, and V_{SET} in subsequent cycles are between 0.6V to 1.5V. Clearly the uniformity of switching voltage is greatly improved, and switching voltage is significantly reduced.

2.6 a-SiC based Resistive Memories

2.6.1 SiC Material Properties

Because of its unique properties, such as high breakdown field (4 x10^6 V/cm [142]), high chemical stability even at elevated temperature (CVD SiC films have shown thermal stability up to 1573K [143]), SiC has received great interest for its application in high power electrical devices since 1990s [142]. Moreover, the following properties of SiC make it a particular promising choice as solid electrolyte material:

- **Low Diffusivity of Cu**

In Cu metallization process, SiC has been studied as a low-k Cu diffusion barrier between Cu wire and the surrounding Cu substrate [20, 124]. Using isotope tracing method, copper diffusion coefficient in CVD-SiC can be expressed as [21]:

$$D_{Cu} = 8.2 \times 10^{-16} exp\left(-41kJ/mol/RT\right) m^2/s \tag{2-6}$$

In which R is the gas constant (8.314J/K mol), and T is temperature in Kelvin. At room temperature (T=300K):

$$D_{Cu} = 8.2\times10^{-16} exp\left(-41kJ/mol/(8.314J/K \cdot mol * 300K)\right) m^2/s = 5.92\times10^{-23} m^2/s = 5.92 \times 10^{-19} cm^2/s \tag{2-7}$$

For comparison, Cu diffusion coefficient in a-Si at room temperature is 2×10^{-16}cm^2/s , and the value for crystalline silicon is at least one order higher [144]. Low Cu diffusivity is

expected to improve retention time of RM device using Cu AE, as the main failure mechanism for RM is believed to be the dissolution of metal filament due to diffusion [99].

- **Schottky Contact**

Furthermore, it is well-established that without high temperature annealing, Schottky contact, instead of Ohmic contact, typically forms at the interface between SiC and metals [145, 146]. As shown in Figure 2-43, contacts between SiC and a wide range of metals are found to be Schottky contact. In particular, for metals with work function in the range of ~4.2eV to 5.3eV, measured Schottky barrier height is between 0.6eV to 1eV. These noticeable Schottky barriers may contribute to higher R_{OFF} and overall ON/OFF ratio of RMs based on a-SiC.

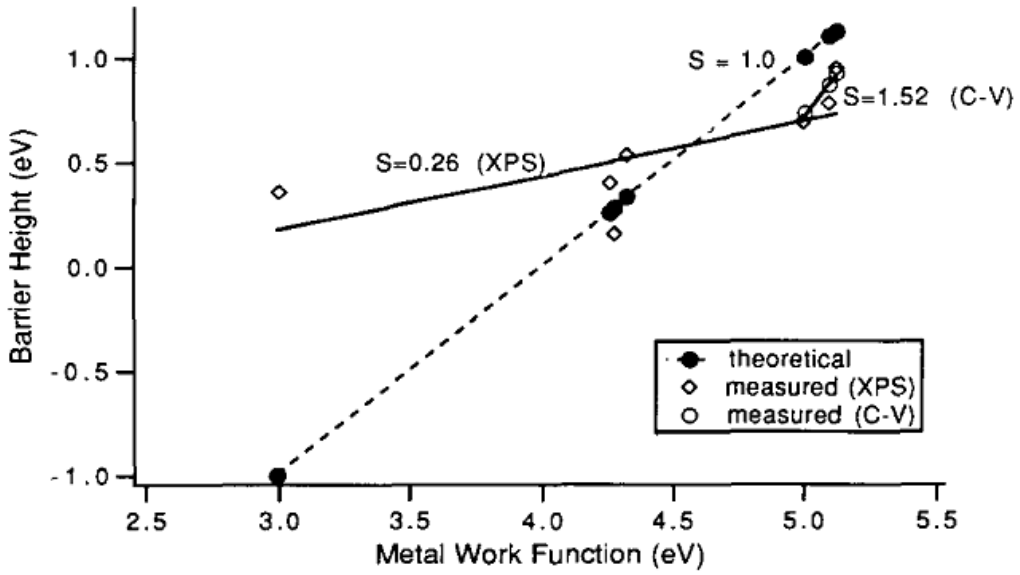


Figure 2-43 Theoretical and measured Schottky barrier height as a function of metal work function of metal to 3C-SiC Schottky contacts [145].

- **High Intrinsic Resistivity**

Room temperature electrical resistivity of sputtering deposited a-SiC has been reported to be up to $10^8 \sim 10^{10} \Omega \cdot \text{cm}$ [147-149]. In comparison, resistivity of typical p-type Si wafer is $1 \sim 20 \Omega \cdot \text{cm}$, and resistivity of amorphous Si can be up to $10^4 \Omega \cdot \text{cm}$ [150]. Again, such high resistivity is likely to lead to high R_{OFF} and high ON/OFF ratio of a-SiC based RMs.

2.6.2 SiC Based RMs

SiC based RMs have shown some outstanding features, namely long data retention time and stable operation at elevated temperature [18, 19]. Lee et al demonstrated Cu/SiC/Pt RM devices fabricated at room temperature with over 10 years data retention time at 85°C, and operation temperature up to 150°C [18]. As the inset of Figure 2-44 (a) shows, the device is composed of metal Pt CE, sputtered a-SiC solid electrolyte layer, and sputtered metal Cu AE. In four repeated switching cycles, V_{SET} is around 1.2V, V_{RESET} -0.8~-0.9V, and ON/OFF ratio around 10^2. The device can also operate normally at 125°C, as the inset of Figure 2-44 (b) shows. R_{ON} and R_{OFF} do not show significant fluctuation during 10^4s at 125°C or 150°C, either.

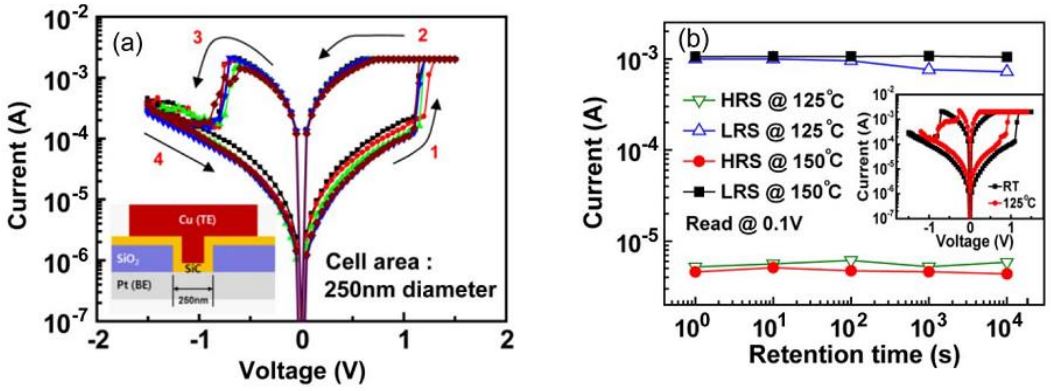


Figure 2-44 (a) Structure and switching behaviour of Cu/SiC/Pt RM device, (b) data retention test and high temperature operation [18].

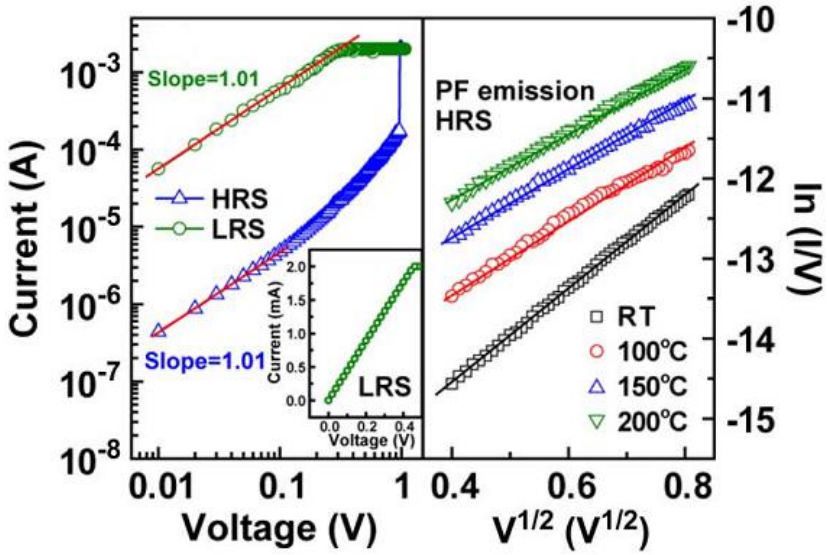


Figure 2-45 (a) HRS and LRS I-V in a log-log plot and (b) HRS I-V data fitted to P-F emission model [18] .

Analysis of HRS and LRS I-V of a-SiC RM is shown Figure 2-45. At LRS, it's clear $\ln(I) \propto 1.01\ln(V)$, hence $I \propto V^{1.01}$, indicating metallic conduction at LRS. At HRS, at very low voltage (0.01V~0.1V), I-V relationship also appears linear, suggesting HRS current at low voltage may be conducted by carrier from unintentional dopant in SiC. At higher voltage, $\ln(I/V) \propto V^{1/2}$, which indicates P-F emission dominates current conduction at HRS.

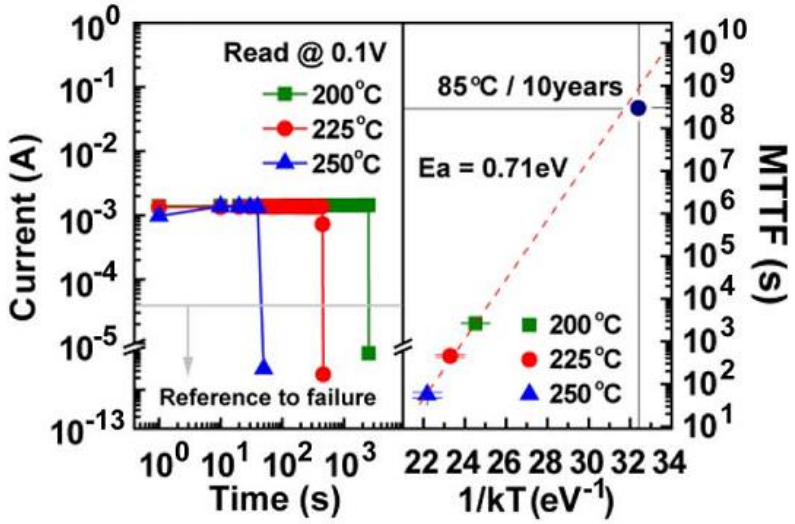


Figure 2-46 Retention time of a-SiC based RM device tested at elevated temperature [18].

Figure 2-46 shows the retention characteristics of SiC based RM devices. The device is set to LRS, and then placed at elevated temperature to accelerate device failure. With device retention time at 200°C, 225°C, 250°C measured, a linear extrapolation is used to estimate device retention time at 85°C. Clearly the estimated retention time exceeds 10 years.

However, these reported Cu/a-SiC based RMs exhibit relatively low ON/OFF ratio in the order of 10^2~10^3. As one of the key performance attributes for any RMs, high ON/OFF ratios present great advantages in future applications as it not only enables fast and reliable detection of the states of memory cells, but also simplifies the periphery circuit to distinguish the storage information [123]. Furthermore, with this only report on Cu/a-SiC RMs focusing on the studies of retention and stability properties, in-depth studies in the switching mechanism are still required. Also, Cu/a-SiC RMs need to be CMOS compatible for practical applications.

2.7 Summary

In summary, due to the physical limitation of tunnel oxide thickness and decreasing number of electrons stored in the floating gate, Flash memory is facing ever increasing difficulties in further down-scaling. A number of novel non-volatile memories have been suggested as potential replacement for Flash memory, and among them resistive memory is particularly promising thanks to its scalability, fast operation and low voltage requirements. A resistive memory has a simple metal-insulator-metal structure, and its resistive switching relies on formation/dissolution of metallic filament caused by electrochemical reactions.

Although RMs with a range of solid electrolyte materials have been reported, suitable electrolyte materials that lead to these desirable performances (e.g. high ON/OFF switching current ratio, reliability, retention and coexistence of bipolar and unipolar behaviours etc.) are yet to be found. Amorphous SiC (a-SiC) as a new electrolyte material has been recently reported to show excellent retention and stabilities due to the advantageously low Cu diffusion rate in SiC. However, with only limited reports on Cu/a-SiC RMs focusing on the studies of retention and stability properties, other crucial aspects of such RMs, such as switching polarity, device structures, counter electrode materials and doping of a-SiC solid electrolyte material, remain to be investigated. From analysis of the influence of these factors, a better understanding of the switching mechanisms of these RMs can also be gained. In addition, there's also room for improvement in the switching performance of reported Cu/a-SiC RMs, in particular the ON/OFF ratio.

Chapter 3. Experimental Methodologies

This chapter presents the main experimental details involved in the project: the structural design of RMs, the fabrication routes and relevant microfabrication processes are discussed in Section 3.1. The structural and electrical characterizations of obtained devices are then discussed in Section 3.2. Finally the material characterization methods of the thin films involved in the project are discussed in Section 3.3.

3.1 Fabrication of Resistive Memories

3.1.1 Design of Device Structures

Via-stack Devices

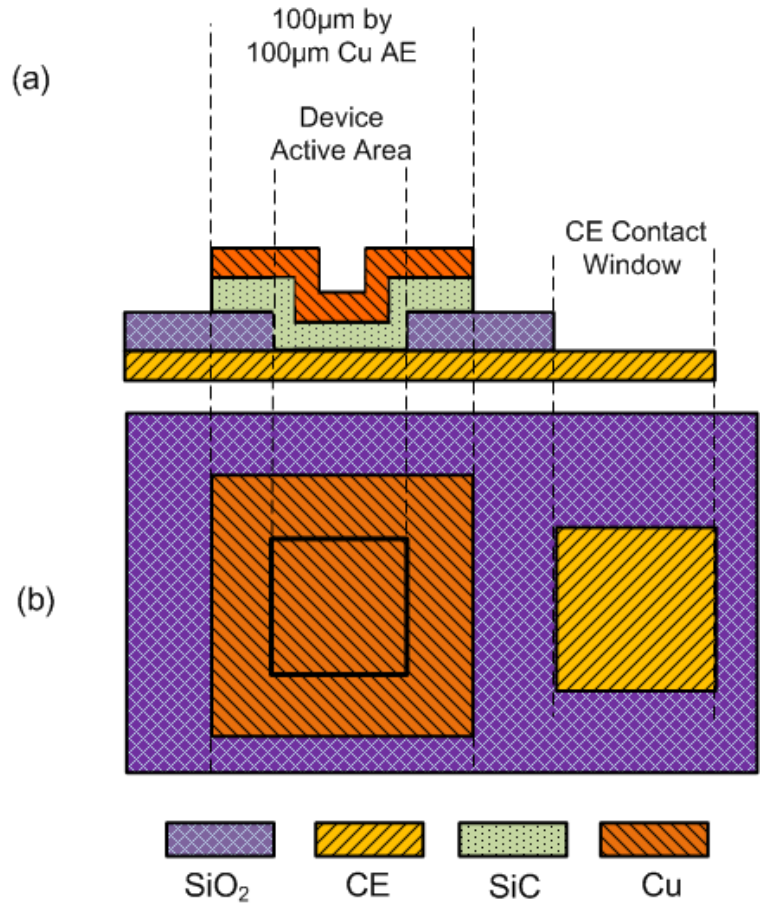


Figure 3-1 Schematic design of the via-stack devices: (a) cross-section view and (b) top view. The Cu AE is constantly 100μm by 100μm square, and the via hole in the SiO_2 layer have different dimensions. The thickness of layers is not drawn to scale.

As discussed in Section 2.7, this project will involve resistive memories of both via-stack structure and cross-bar structure. Figure 3-1 shows the design of via-stack structured devices. The Cu AE and CE layers are both approximately 300nm thick, and the a-SiC solid electrolyte layer approximately 40nm. The device active areas are defined by via holes in the layer of 250nm thick SiO_2. The device active areas are designed to be squares with side length of 1, 2, 4, 5, 6, 8, 10, 20, 40, 50, 60, 80 and 100μm, and the top Cu electrodes are constantly 100μm by 100μm squares. With device area ranging from 1μm^2 to 10^4 μm^2, the area dependency of device performance can also be investigated.

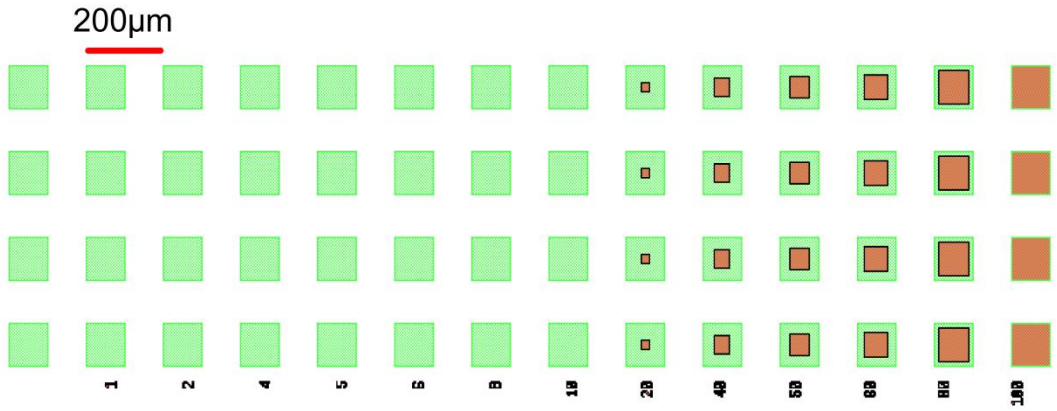


Figure 3-2 Lithography mask design for in-via devices.

The lithography mask design is shown in Figure 3-2. The red patterns are the first layer, which will be the via holes in the SiO_2 layer, i.e. the device active areas when finished. In Figure 3-2 only device active areas larger than 20μm by 20μm are visible. There are four identical devices of the same dimensions, and the dimensions are marked in the mask for identification. The green squares will define the Cu and a-SiC layer, and all top Cu contacts will be 100μm by 100μm square. The CE contact windows are not shown in Figure 3-2. The CE layer will be shared by all the devices on one wafer, as the CE will be constantly grounded during electrical testing. The CE contact windows will be squares of 0.5mm by 0.5mm, and 6 sets of devices shown in Figure 3-2 will have a common CE contact. There is also one line of Cu contacts on top of SiO_2 layer that has no openings. These areas will have Cu/a-SiC/SiO_2/Au structures, like the areas surrounding the active areas of normal devices. These structures have also been tested to confirm the switching behavior is from the active areas only, and the results are shown in subsection 3.2.2.

Cross-bar Devices

On the other hand, the design of RM devices of cross-bar structure is shown in Figure 3-3. Laser direct write lithography was used for the fabrication of these devices (more details are in subsection 3.1.2 and 3.1.3). The CE layer and the Cu/a-SiC layer share the same dumbbell-like pattern: two large square contacts with a thin line in the middle. The actual device active area is where the two thin lines overlay, and the dimensions of the active areas can be adjusted by changing the width of the two thin lines during lithography. The size of contact pads is 250μm by 250μm, and device active areas were designed to be 9μm^2, 25μm^2, 49μm^2, 100μm^2, 196μm^2. With contact pads on both sides of a device, even when metal connection is broken on one side of the device, the device can still be tested using the other pad. This design also leaves enough room for misalignment of lithography patterns: as long as there is overlay area of the two thin lines, and the four contact pads are separated, a functional device is formed.

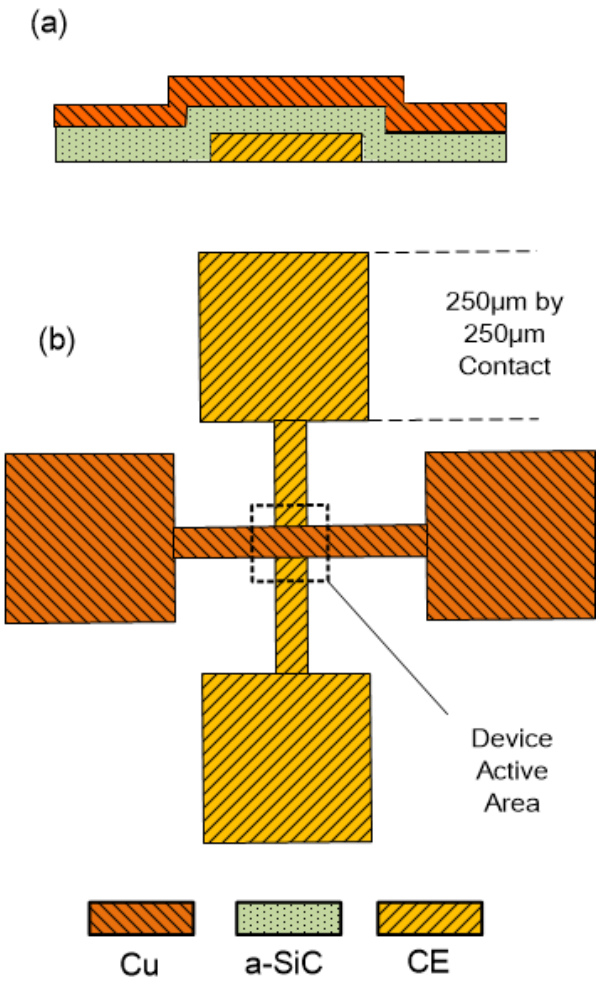


Figure 3-3.Schematic design of the cross-bar structured devices: (a) cross-section view of the active area, (b) top view of one device.

3.1.2 Fabrication Route

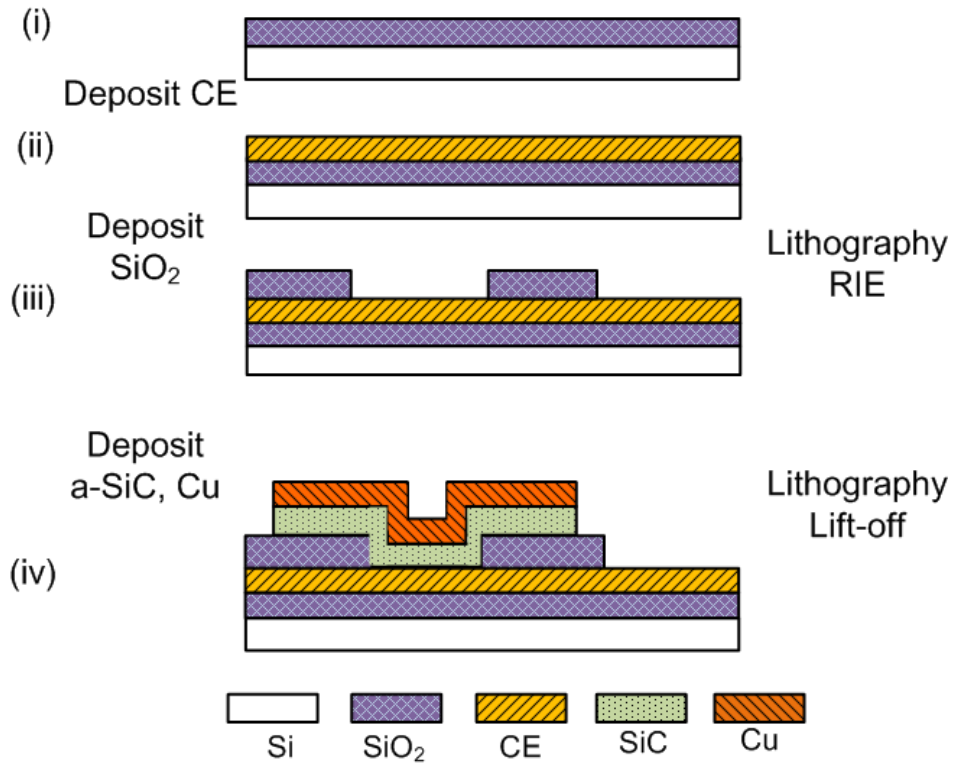


Figure 3-4 Schematic drawings of fabrication process flow for the via-stack structured resistive memory devices.

The overview of fabrication routes of the two types of devices are shown in Figure 3-4 and Figure 3-5, respectively. For both types of devices, the fabrication route started from Si substrates with 1μm SiO_2 layer on top, so that the fabricated devices would be electrically insulated. For the via-stack structured devices, the bottom electrode layer was then deposited on top of SiO_2 layer (Figure 3-4 (ii)). A second 250nm SiO_2 layer was then deposited by reactive sputtering Si target in oxygen plasma. The SiO_2 layer was patterned by UV lithography and RIE to expose the bottom electrode in device active areas and contact windows (Figure 3-4 (iii)). The dimensions of the active areas were from 1μm in diameter to $10^4 \mu m^2$, so the scaling effect on device performance could be studied and the results are shown in section 5-4. A second UV lithography process left a photoresist layer with patterns of the Cu top electrodes. The a-SiC solid electrolyte layer and Cu top electrode were deposited by sputtering subsequently without breaking vacuum seal. This is to minimize possible contamination between Cu and a-SiC when exposed to ambient environment. Finally a lift-off process was conducted to remove excessive a-SiC and Cu layers between devices, and thus obtaining the final Cu/a-SiC/BE devices (Figure 3-4 (iv)).

The SEM images of the obtained devices and the cross-section view of the device active areas are shown in Section 5-1.

For the cross-bar structured devices, bottom electrode material was deposited on the substrates using sputtering, followed by a photolithographic lift off process to achieve a patterned bottom electrode (Figure 3-5 (ii). Subsequently, a-SiC solid electrolyte layer followed by Cu top active electrodes were deposited using RF and DC sputtering, respectively, without breaking the vacuum in the sputtering chamber. A final lift off process was conducted to obtain the cross-bar structured resistive memory cells (Figure 3-5 (iii). The SEM images of the obtained devices and the cross-section view of the device active areas are shown in Section 6-1.

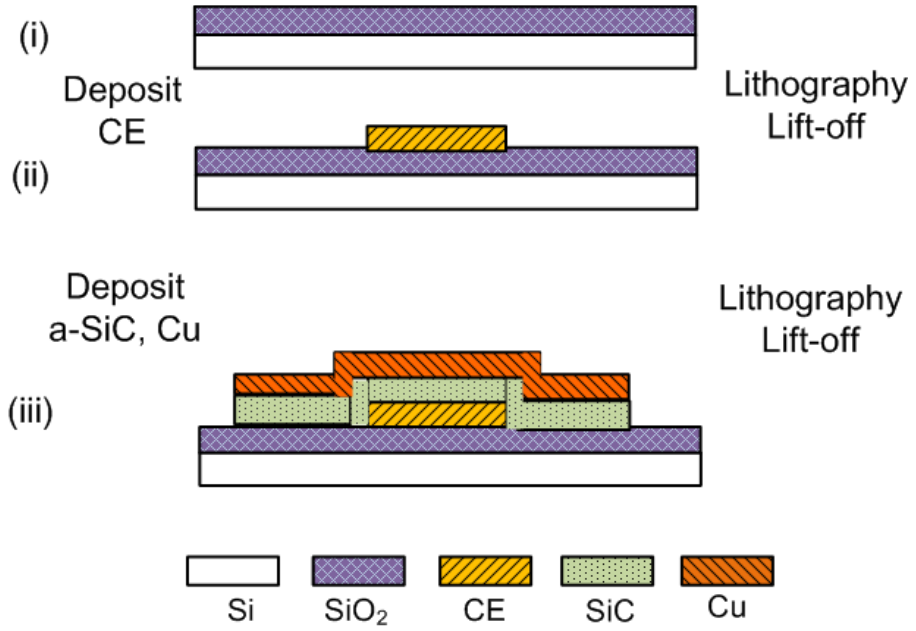


Figure 3-5 Schematic drawings of fabrication process flow for the cross-bar structured resistive memory devices.

In the fabrication routes of both types of devices, the counter electrode material, a-SiC solid electrolyte and Cu active electrodes were all deposited by sputtering deposition. All sputtering deposition processes were carried out using Ar gas, with chamber pressure $<1\times10^{-6}$ mBar before deposition and 5×10^{-3} mBar during deposition. The thickness of the counter electrodes and the Cu active electrodes were both approximately 300nm. The thickness of the a-SiC layer was 40nm for most devices, although devices with 50 and 80nm were also fabricated and tested. The effects of a-SiC layer thickness are briefly discussed in section 6-1. In both fabrication routes the Cu top electrodes were defined by lithography and lift-off process, so that etching of Cu was avoided.

3.1.3 Relevant Fabrication Techniques

Sputtering Deposition

Sputtering deposition is the primary technique applied in this project for thin film deposition. Compared to evaporation, plasma sputtering has better step coverage, better film adhesion due to higher kinetic energy of sputtered atoms, and can work in ambient temperature. All these features make sputtering a very widely adapted deposition technique in micro fabrication processes [147, 151, 152]. In addition, co-sputtering of multiple materials has also been widely used in creating composite materials [85, 153-158]. The composition of such co-sputtered materials can be readily tuned by adjusting the sputtering power configuration according to application requirements, which make it particular suitable for the preparation of functional materials for resistive memories.

Depending on the material to be deposited, one of two types of plasma sputtering can be chosen: Direct Current (DC) sputtering or Radio Frequency (RF) sputtering. The application of DC sputtering is limited to conductive materials: if the target material is insulator, the positive ions will quickly build up on the target, neutralising the applied voltage. RF sputtering overcomes this obstacle by applying an RF voltage instead of DC voltage to the electrodes. When RF voltage is applied, the two electrodes act as anode and cathode alternately. During the half circle with positive voltage on an electrode, electrons are drawn to its surface, while during the other half circle positive ions are drawn to the surface. Electrons, being much lighter than positive ions, will arrive at the electrode surface in much larger number, until a sufficiently large negative potential is established, which draws more positive ions and repels more electrons. Once the negative potential is established, the plasma sustains by the same mechanism in DC sputtering.

The a-SiC and a-SiC/Cu solid electrolytes and various electrodes were all deposited by a Kurt J. Lesker sputter system shown in Figure 3-6. The system is equipped with two Huttinger PFG 1500 DC power supplies and two PFG 600 RF power supplies. The maximum power for the DC power supplies is 1000W, and the maximum power for the RF power supplies is 400W. With these power supplies, the system is capable of simultaneously sputtering four targets: two on DC mode and two on RF mode. The chamber pressure before and during deposition, the argon gas flow, rotation of the substrates, and the output power of the power sources are all controlled by the main

control interface shown in Figure 3-7. The substrates can also be cooled by liquid nitrogen or heated electrically if necessary.

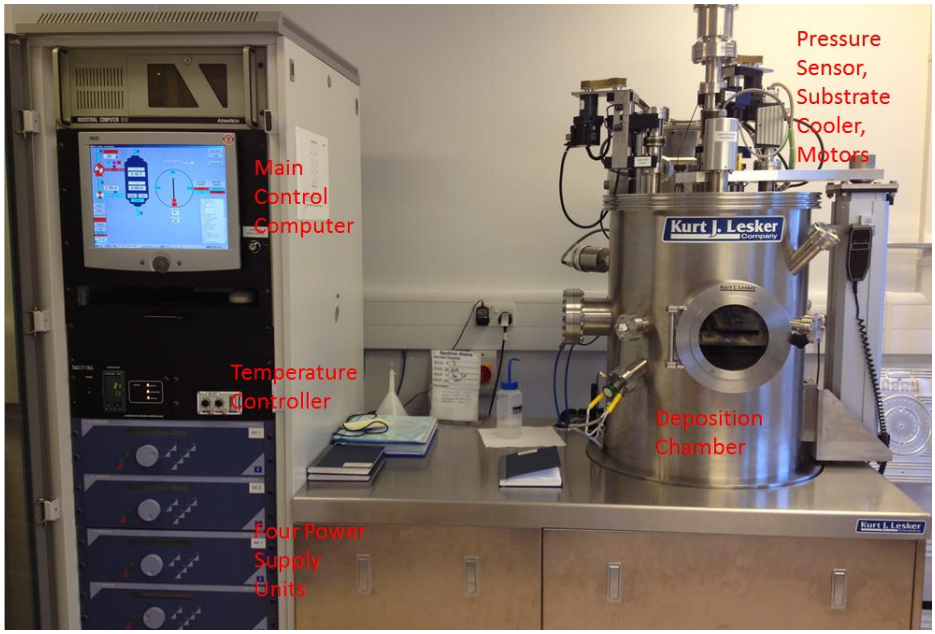


Figure 3-6 Photo of the Kurt J. Lesker sputter system.

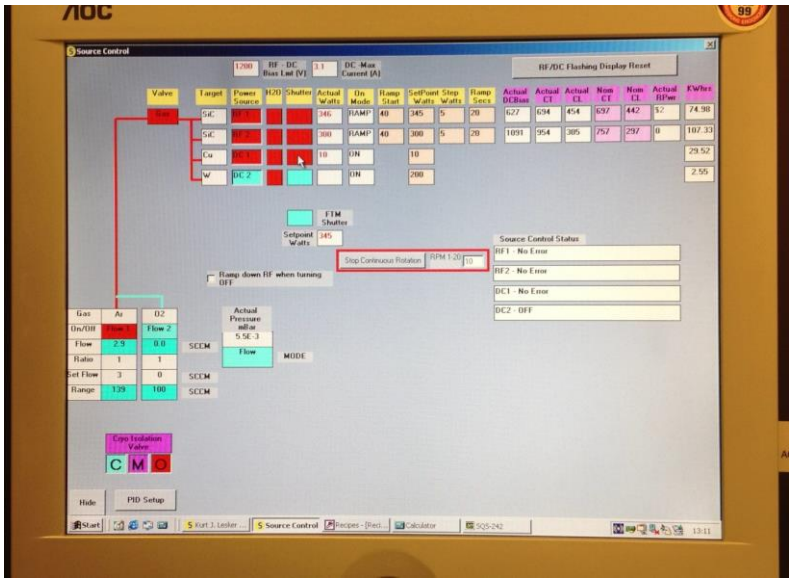


Figure 3-7 The main control interface of the sputter system.

The universal deposition conditions for all the thin films involved are as follows: Before all the actual sputtering deposition, the deposition chamber was pumped down to $< 1 \times 10^{-6}\ mBar$ to minimize possible contamination. During sputtering the Ar flow was set to 3 sccm, which corresponds to $4.5\sim5.5\times 10^{-6}\ mBar$ chamber pressure. The substrate holder was set to 10 rpm rotation for better uniformity of obtained films. The depositions

were all performed at room temperature. Furthermore, the specific deposition conditions are listed in Table 3-1.

Deposited Film	**Sputtering Target**	**Sputtering Mode**	**Power(W)**	**Deposition Rate (nm/min)**
a-SiC	99.5% SiC	RF	250	4.5~6
a-SiC/Cu	1 or 2 SiC + 1 Cu	RF + DC	SiC power up to 340W, Cu power up to 35W, see table 4-1	4.5~13
Au	99.99% Au	DC	110	30
Cu	99.999% Cu	DC	110	16
TiN	99.5% TiN	RF	250	3.6
W	99.9% W	DC	210	12.5

Table 3-1 Specific sputtering deposition conditions of thin films involved in the project.

Lithography

In general, lithography process consists of three main steps:

1. Spin coating of photoresist: In this step the substrate is thoroughly cleaned and coated with a photoresist layer by spin coating. The spin speed is chosen according to the specification of the photoresist and the desired thickness of the photoresist layer.
2. Exposure: Sample coated with photoresist is exposed to patterned radiation, typically UV light. During the exposure process, the resist undergoes a chemical reaction. Depending on the chemical composition of the resist, either the exposed region of resist will become less stable (positive resist) or more stable (negative resist) upon radiation.
3. Development: For positive photoresist, the exposed part is dissolved by the developer and for negative resist the unexposed part is dissolved. A hard bake process is usually performed after development to further harden the patterned resist layer and remove the residual solvent.

For example, the process of a lithography process using S1813 positive photoresist and laser direct writer is as follows:

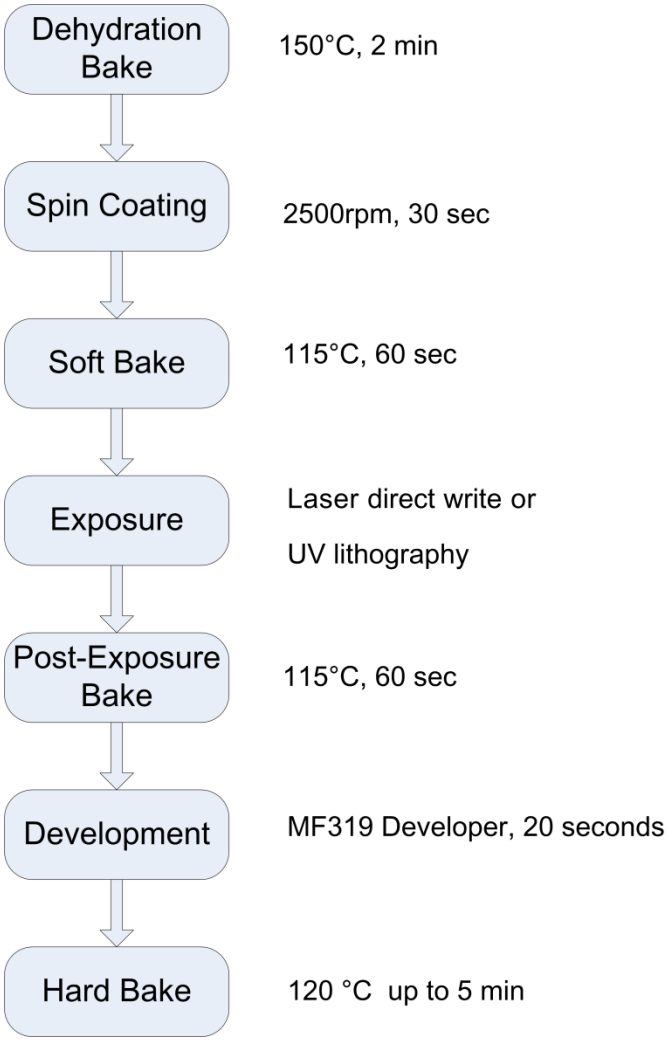


Figure 3-8 Flow chart of a typical lithography process using S1813 photoresist.

In this project, both conventional UV-lithography and mask-free laser direct-write lithography was used for the exposure process, for they each has their respective advantages and shortcomings, as discussed below.

Laser Direct-Write Lithography

The direct writer used is a Zeiss LSM 510 confocal microscope. Its principle is shown in Figure 3-9 and its key components are shown in Figure 3-10. In the lithography mode, a UV laser source is firstly chosen according to the photoresist to expose. The laser is then fed to the confocal microscope. The microscope focuses the laser onto the surface of the sample, and the scanning mirror is controlled by a computer to only expose desired pattern on the sample. In this way, lithography can be carried out without a premade mask.

To expose S1813 photoresist, the light source is 458nm Ar laser. An exposure scan of 1mm*1mm area takes 8min 16sec, regardless of the specific pattern.

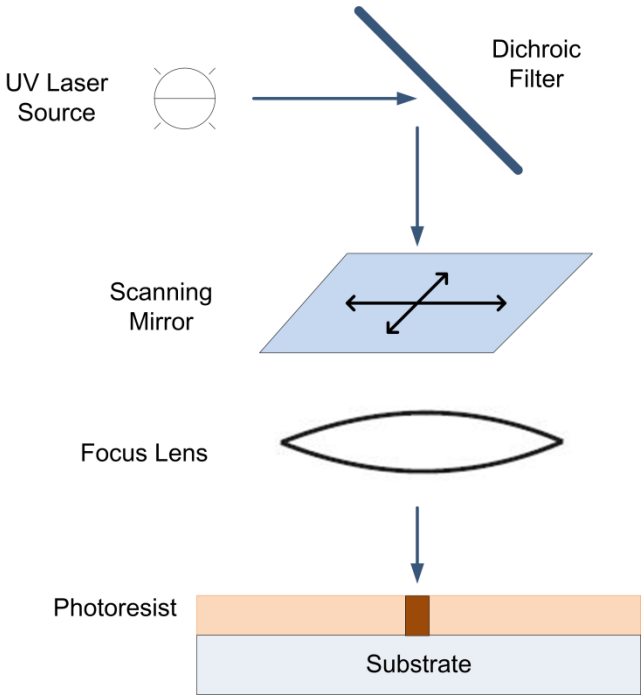


Figure 3-9 The principle of laser-direct write lithography, which requires no mask.

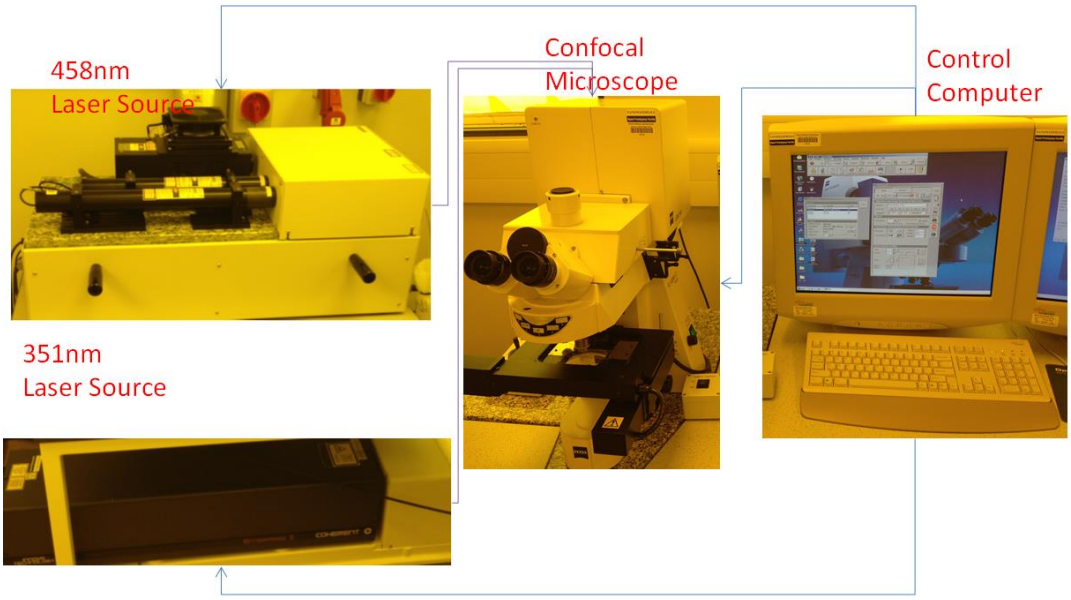


Figure 3-10 Components of the laser direct writer system.

There are however several limitations on the exposure pattern for the direct writer: firstly one scan covers 1mm*1mm area. If larger pattern is required, one can try the step-scan process. Secondly the reflector should be turned on/off no more than 10 times in during one horizontal scan, which limits the complexity of the pattern. Finally the control system has no specialized software that can be used to define the pattern. The pattern is defined

by simply setting the coordinates of the vertices of polygons. This also limits the complexity of the pattern. Despite these limitations and its relatively slow scan speed due to its serial scan mechanism, being mask-free makes it a very valuable tool for prototyping. Designs of lithography pattern can be changed within hours. As discussed in the fabrication route, the cross-bar structured devices were fabricated using the laser direct-write lithography. Practically, in one batch of the via-stack devices it's possible to fabricate over 1000 devices, while only 20~40 cross-bar devices can be made in a similar time frame.

Figure 3-11 shows a 3μm wide S1813 resist bar structure produced by laser direct writer lithography. Except for the rounded corners, the developed pattern shows minimum distortion. Features of 3μm wide are currently the minimum size that has been realized using this technique, and the theoretical resolution limit is 0.5μm. This system was mostly used in the fabrication of cross-bar structured devices.

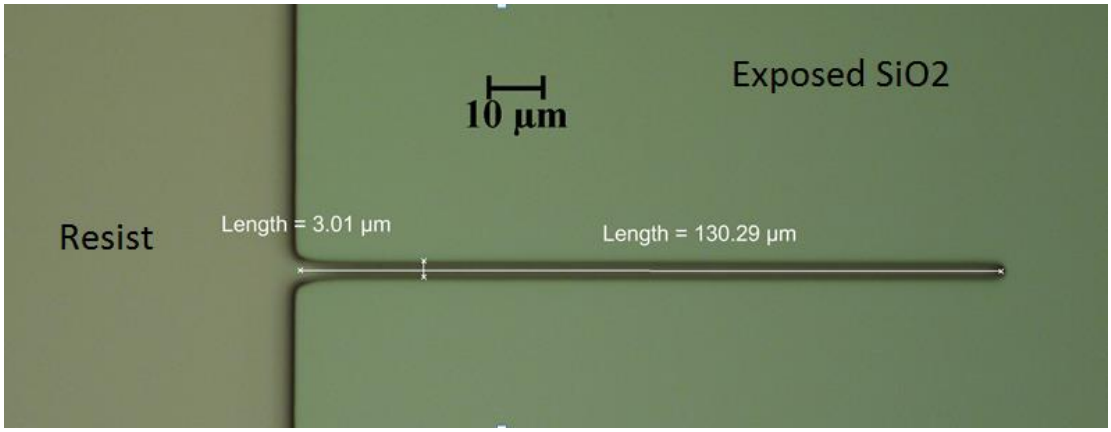


Figure 3-11 3μm wide S1813 resist bar produced by laser direct writer lithography.

UV lithography

In addition to the laser direct writing lithography, an EVG 620T contact aligner was also used for conventional UV lithography. This aligner is capable of handling 6 inch wafers and the masks used were also designed for 6 inch wafers. Therefore the device output of UV lithography is significantly higher than laser direct writing lithography. However it offers no flexibility once the mask is made, and the fabrication process can only start when the mask is ready. These characteristics make it unsuitable for prototyping of devices in limited quantity. Using I-line light source (365nm wavelength) and contact exposure mode, this system is capable of producing features smaller than 1μm.

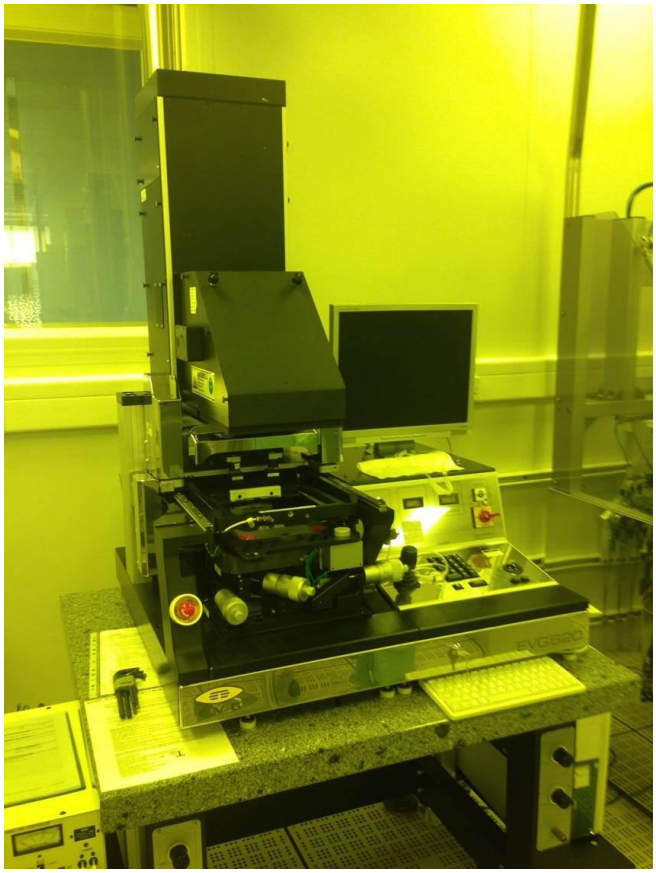


Figure 3-12 Photo of EVG 620T aligner used for UV lithography.

In this project UV lithography was used for the via-stack structured devices. Two lithography masks were designed, one for the openings in the SiO_2 layer (Figure 3-4(iii)) and one for the top Cu electrodes (Figure 3-4 (iv)). The mask designs are shown in Section 5.1

Reactive ion etching (RIE)

In this project, the patterning of metal electrodes and a-SiC solid electrolytes were all achieved by lithography and lift-off processes. Reactive Ion Etching (RIE) has been used mainly for the etching of SiO_2 insulating layer. Unlike wet etching, the start/finish time of RIE can be accurately controlled, and RIE is not sensitive to substrate temperature. The repeatability of RIE is therefore better than wet etching. RIE is also usually highly anisotropic, producing much sharper side walls than wet etching.

The main etching mechanism of RIE is chemical reaction between ions produced in the plasma and the surface material. The reactive ions are attracted to the sample surface by negative electric potential generated by the applied RF voltage. Consequently RIE etching

is highly anisotropic. Depending on the gas used in chamber, ion sputtering may also be involved in the etching process.

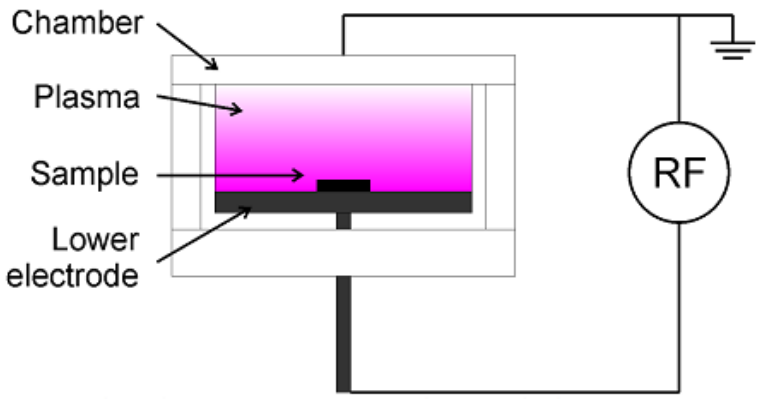


Figure 3-13 Electrical configuration of an RIE chamber.

A Plasmalab 80+ RIE system is used for etching of SiO_2 layers (step ii to iii shown in Figure 3-4), the photo of which is shown in Figure 3-14.

Figure 3-14 Photo of Oxford Plasmalab RIE80+ RIE system used for etching of SiO_2.

3.2 Characterization of Resistive Memories

3.2.1 Device Structure

To examine the results of the steps of the fabrication process, such as lithography, and the end results, several optical microscopes and scanning electron microscopes (SEM) were used. The most frequently used SEM was the Leo 1455VP SEM in the Nanomaterials rapid prototyping facility (Figure 3-15), which is a 30kV, tungsten filament scanning electron microscope equipped with an Everhart-Thornley secondary electron detector and a Cambridge four quadrant backscatter detector.

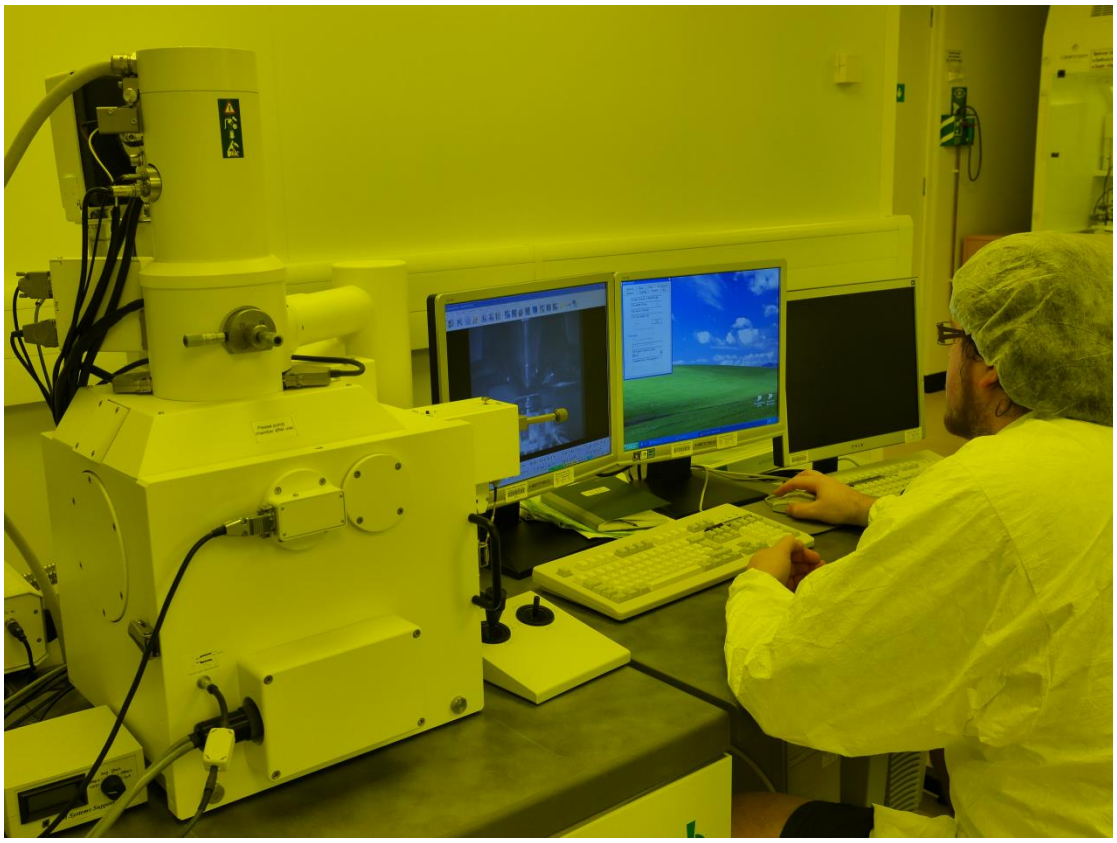


Figure 3-15 Leo 1455VP SEM

In addition, to examine the cross-section of the device active areas, a Zeiss NVision 40 CrossBeam FIB System (Figure 3-16) was used. This system is capable of milling, imaging and deposition by Focused Ion Beam (FIB) and SEM imaging. As shown in Figure 3-17, in FIB milling mode, the sample was titled by 54°, so that the sample surface was perpendicular to the ion beam. Firstly the SEM image was used to locate the area of interest. The ion beam was then used to create a trench on the sample surface, exposing the layers beneath the surface. To have a smooth cross-section, at first ion beam with

higher energy (~3kV) was used to get a rough cut and then a series of lower energy beam (~0.5kV) were used to polish the surface. After polishing, the exposed surface was examined by SEM. The results are shown in Section 5.1, 6.1 and 6.2.

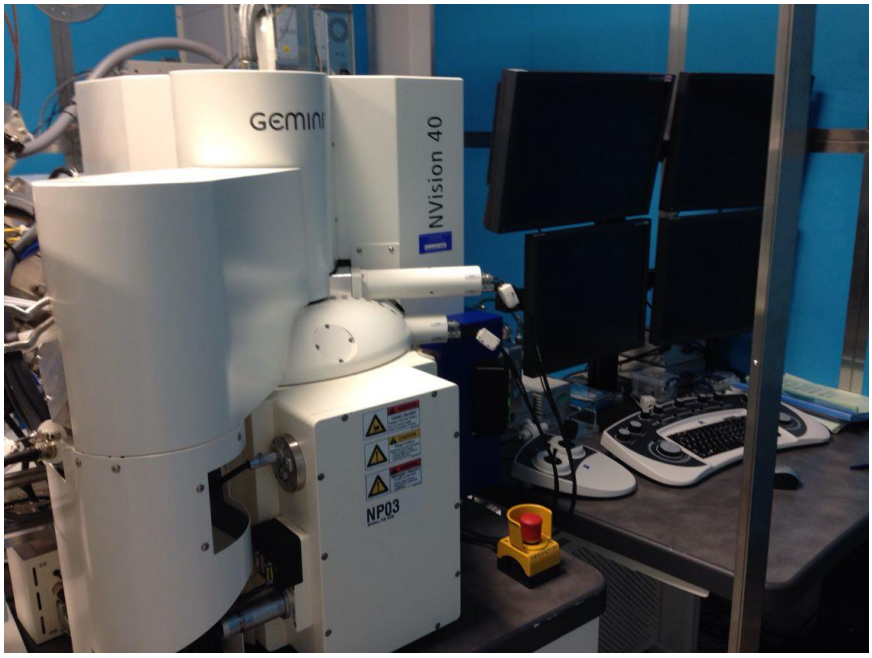


Figure 3-16 Photo of Zeiss NVision 40 CrossBeam FIB System.

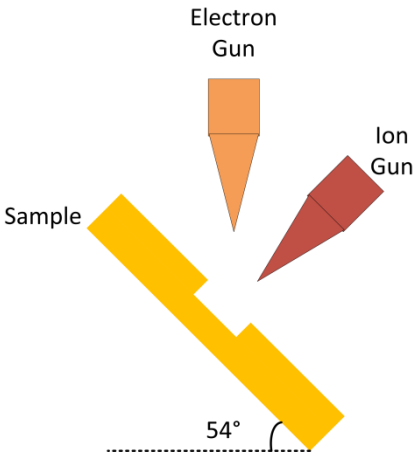


Figure 3-17 Schematic drawing of the arrangement of sample, electron gun and ion gun in the FIB system during FIB milling.

3.2.2 Switching Behaviour

Experimental Setup

I-V testing is the fundamental testing for a resistive memory, as resistive switching controlled by applied voltage is its basic function. The principle of I-V testing for resistive memory is shown in Figure 3-18: A sweeping voltage is applied on the AE with the CE grounded, and the sweeping voltage and current through device is simultaneously

measured. The main set-up used in this project for switching behaviour testing is shown in Figure 3-19. It's composed of an Agilent B1500A semiconductor device parameter analyser and a 5-channel probe station. The optical microscope enables the precise positioning of probe needles on the device under test. During testing, two probe needles are placed onto the AE and CE of device under test, respectively. Each of the two needles is connected to a Source Monitor Unit (SMU) in Agilent B1500A.

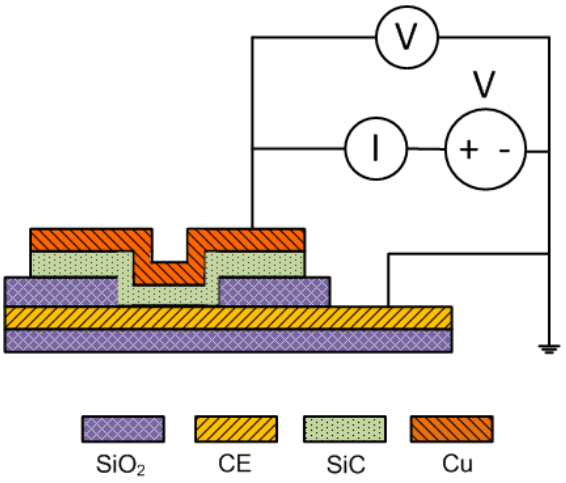


Figure 3-18 Schematic drawing of the principle of switching behaviour testing.

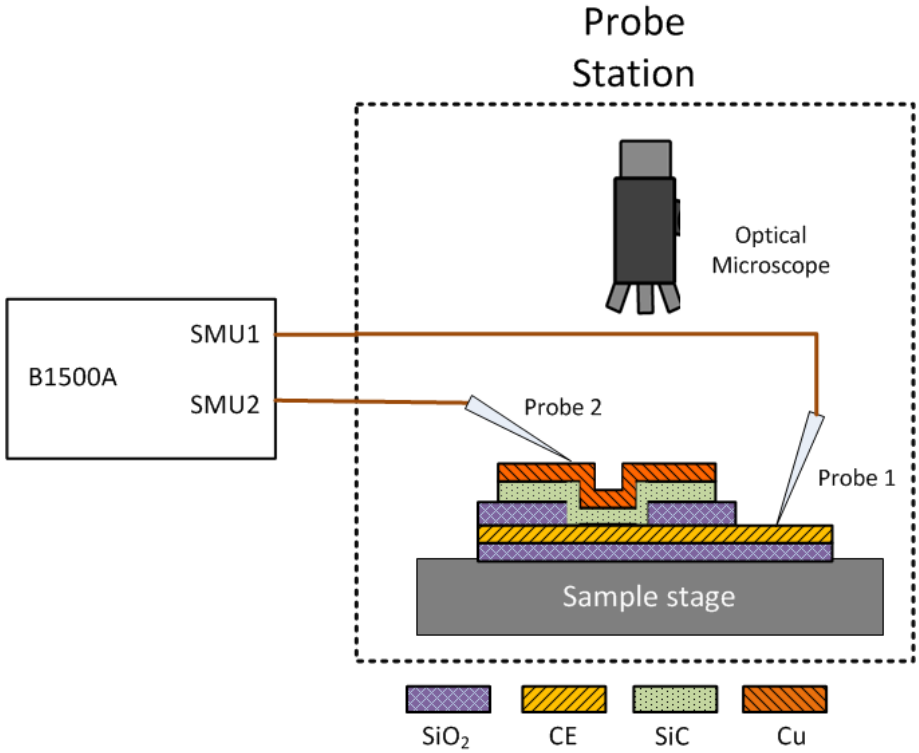


Figure 3-19 Schematic drawing of the electrical testing setup with an Agilent B1500A device analyser and a probe station. The dotted line shows a Faraday cage used to shield the sample and probes from electromagnetic interference.

In Figure 3-19, SMU1 is connected to the CE and SMU2 connected to the AE. Therefore, SMU1 is grounded during the test and sweeping voltage is applied through SMU2. The current through SMU1 and SMU2 are both recorded for to the following reason: In principle the current through two SMU should be of equal magnitude but different direction. If there's noticeable divergence between the two values, then there is certain parasitic current path in the testing setup that needs to be eliminated. In the results shown in this thesis, current through SMU2 are presented as it has the same polarity as the applied voltage.

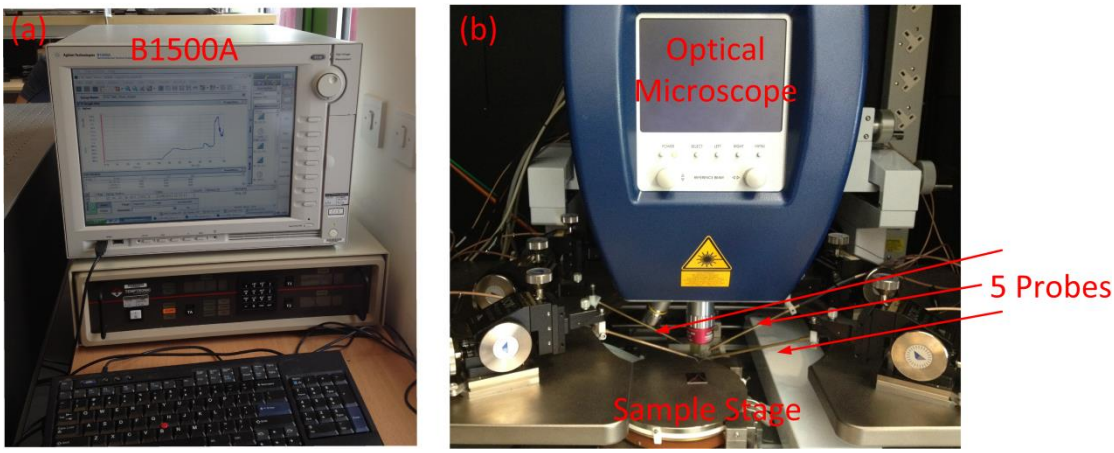


Figure 3-20 photos of the main components of the electrical testing setup: (a) Agilent B1500A device analyser and (b) sample stage with 5 probes and an optical microscope.

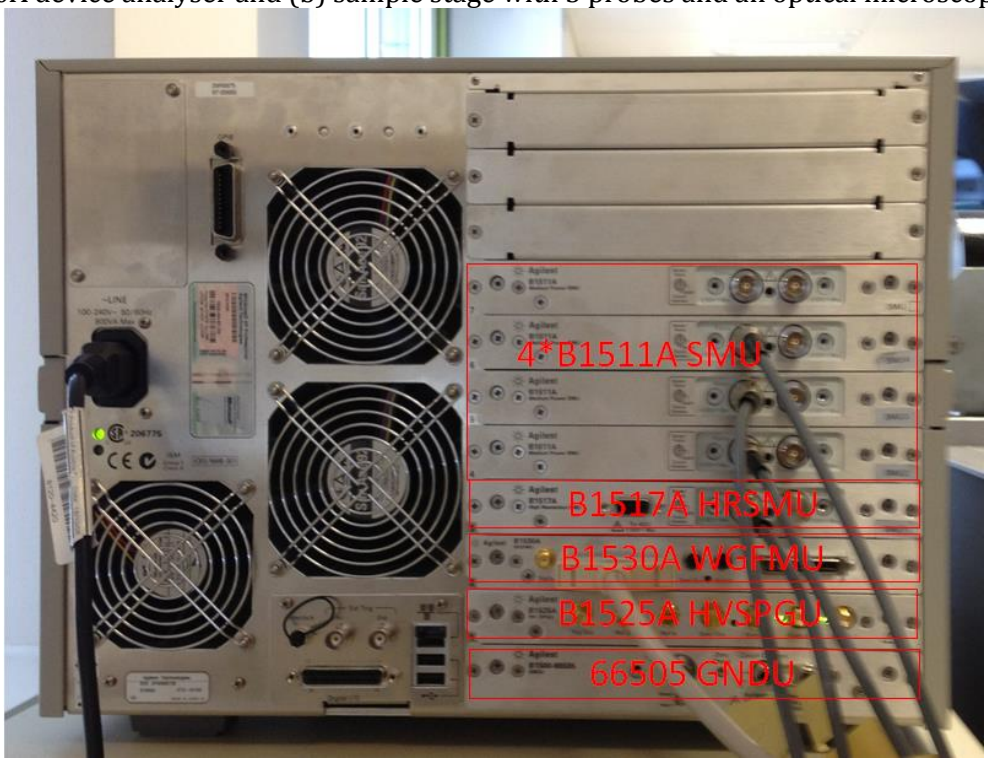


Figure 3-21 Photo of all modules installed in the B1500A parameter analyser.

In addition to the switching behaviour measurement, in this project, the B1500A parameter analyser has also been used for resistivity measurement of pure sputtered a-SiC films, where measurement of current below 10^{-12}A is needed. The B1517A HRSMU (High Resolution HMU) module of the B1500A has proven particularly helpful in measurement of such low currents.

As shown in Figure 3-21, the current available modules of the B1500A parameter analyser are:

- 4*B1511A SMU Each SMU is capable of independently supplying current/voltage and monitoring corresponding voltage/current.
- B1517A HRSMU high resolution SMU,
- B1530A WGFMU Waveform Generator and Fast Monitor Unit, is capable of simultaneously generating short, arbitrary voltage waveforms and monitoring current response.
- B1525A HVSPGU High Voltage Short Pulse Generator Unit, is capable of generating arbitrary voltage pulses with 40V peak voltage and 10ns duration. It has no monitor unit built in, so it can only generate pulse but not measure response.

66505 GNDU A designated ground unit.

Sweeping Voltage

The input voltage signal is usually a double sweep voltage wave, as shown in Figure 3-22. The start value, stop value, step value, and hold time, delay time of the double sweep signal can all be customized. For example, to get the I-V plot shown in Figure 3-23, sweep voltage is configured to start from 0V, increase to 4V with 20mV step, and reduce to 0V. At the beginning of the I/V sweep, device is clearly at HRS. It is then switched to LRS when applied voltage on Cu reaches ~3.8V. Device then maintains LRS during the remainder of the I/V sweep. From the I-V curves, the switching parameters, namely V_{SET}, V_{RESET}, R_{ON} and R_{OFF} can be determined. More detailed analysis of the I-V data can also help reveal the conduction mechanisms at LRS and HRS.

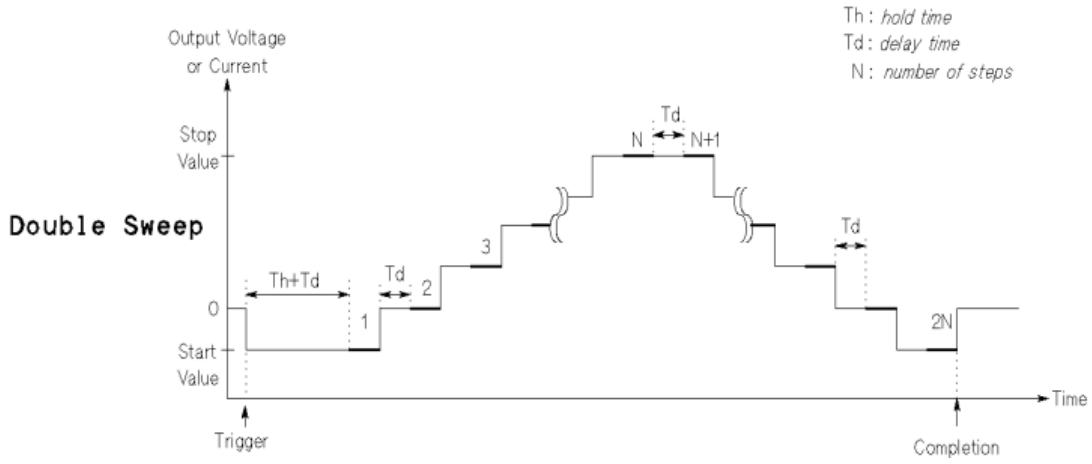


Figure 3-22 Waveform of a double sweep signal from the B1500A.

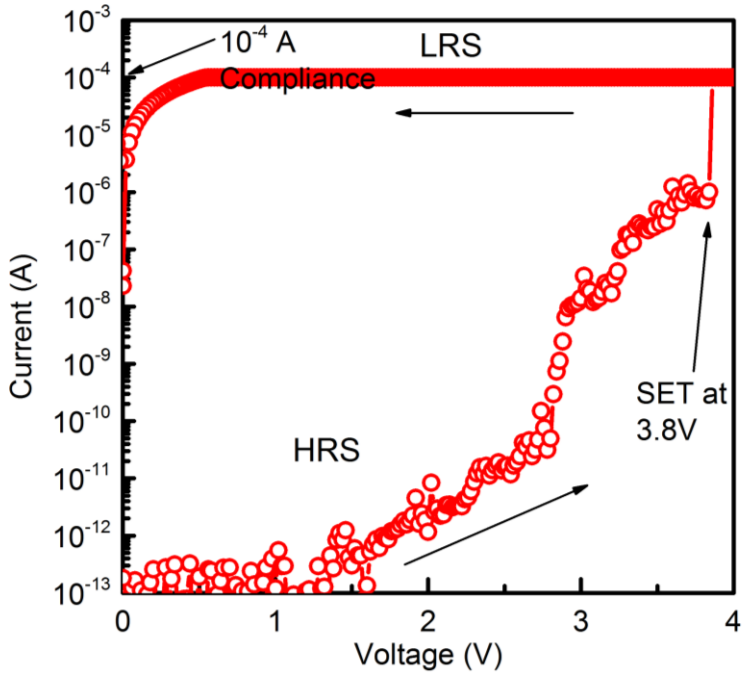


Figure 3-23 Current response to a 0-4V-0 double sweep voltage from a fresh Cu/a-SiC/Au RM device. The sweeping directions are indicated by arrows.

Current Compliance

Setting of current compliance also plays a key role in the I/V sweep of PMCs. This value sets a maximum of current amplitude during measurement. A current compliance is set primarily to protect the device under test during set process. An excessively high current compliance may cause damage to device. On the other hand, a too cautiously set current compliance may lead to a non-stable LRS, as too few metal ions are transported to form the filament. On the other hand, the primary reason that a current compliance was applied

in the SET cycles is to prevent permanent breakdown of the device. In most studies of RMs [10], current compliance by the measurement equipment or a serial resistor to limit current was used for this purpose. However the exact current compliance values can vary several orders of magnitudes among studies, so the reported compliance cannot be directly adopted for these Cu/a-SiC/Au devices.

So far in this project, proper setting of current compliance for a particular PMC can only be achieved by starting from a low compliance, and gradually increasing the compliance until stable and repeatable switching is observed. The results of such testing for the Cu/a-SiC/Au via-stack devices are shown in Figure 3-24.

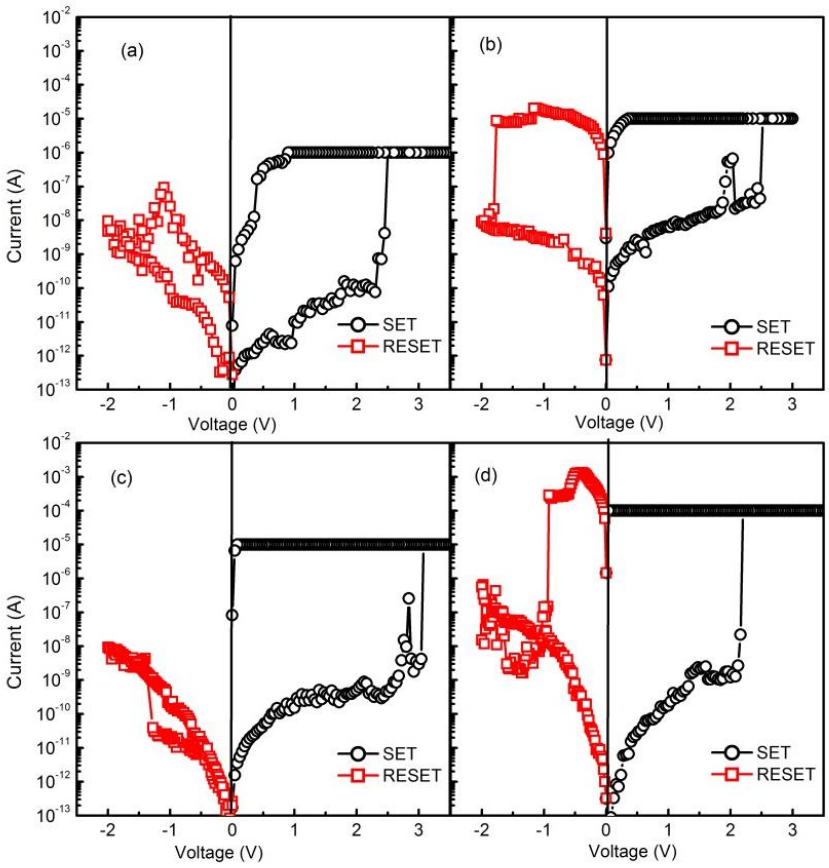


Figure 3-24 LRS stability resulted from different current compliance settings: (a) unstable LRS, 1μA compliance. (b) stable LRS, 10 μA compliance. (c) unstable LRS, 10μA compliance. (d) stable LRS, 100μA compliance.

In Figure 3-24 (a), the current compliance was 1μA during SET. The transition from HRS to LRS was clearly observed in the SET cycle, but a stable LRS was not observed in the RESET cycle. Similar results were found in several other devices, indicating 1μA compliance was

not sufficient to achieve stable LRS in these Cu/a-SiC/Au devices. Figure 3-24 (b) and (c) shows 10μA compliance could lead to stable LRS, but unstable LRS like the one in Figure 3-24 (c) would still occur. When current compliance was increased to 100μA, as shown in Figure 3-24 (d), the resulting ON-states were mostly stable in repeated cycles, and therefore current compliance of 100μA was chosen for most of the switching testing.

Possible Contributing Factors to I-V Data

Two initial measurements were performed to examine the possible contributing factors to the obtained I-V data, and the results are shown in Figure 3-26 and Figure 3-28.

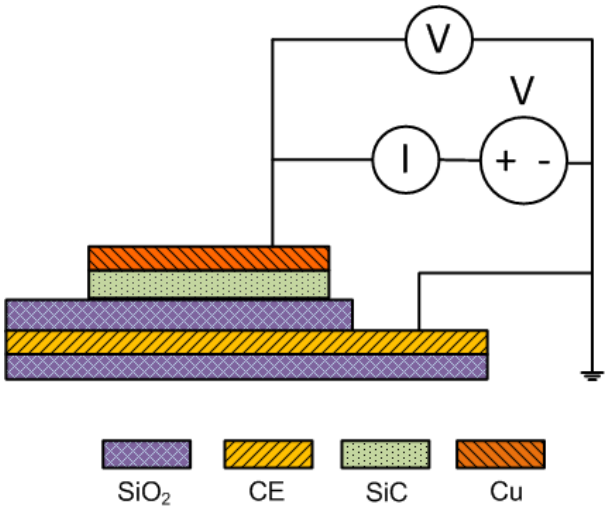


Figure 3-25 Schematic drawing of the test of leakage current through SiO_2.

Firstly, as discussed in Section 3.1, the active areas are surrounded by 250nm SiO_2 layer, which is also covered by Cu and a-SiC layers (see Figure 3-1). Therefore effectively the device under test will be the Cu/a-SiC/Au device and a Cu/a-SiC/SiO_2/Au structure connected in parallel. So the possible contribution of Cu/a-SiC/SiO_2/Au structures surrounding the actual device has to be tested. A 100μm by 100μm Cu/a-SiC/SiO_2/Au structure, shown in Figure 3-25, was tested for this purpose and the I-V results are shown in Figure 3-26. The voltage bias was applied on the Cu contact, and Au layer grounded. Clearly, there was no sign of break-down even at 15V bias, which far exceeds the typical switching voltage of 2V~4V. In this range, the leakage current through the structure is below 5 pA, which is negligible compared to the actual current through the RM devices. From these results, it is reasonably to believe the surrounding SiO_2 areas had no noticeable contribution to the switching I-V data.

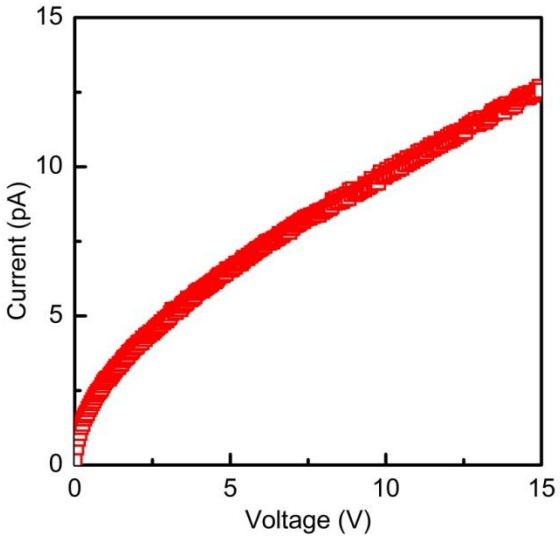


Figure 3-26 I-V curve of a 100μm*100μm Cu/a-SiC/SiO_2/Au structure.

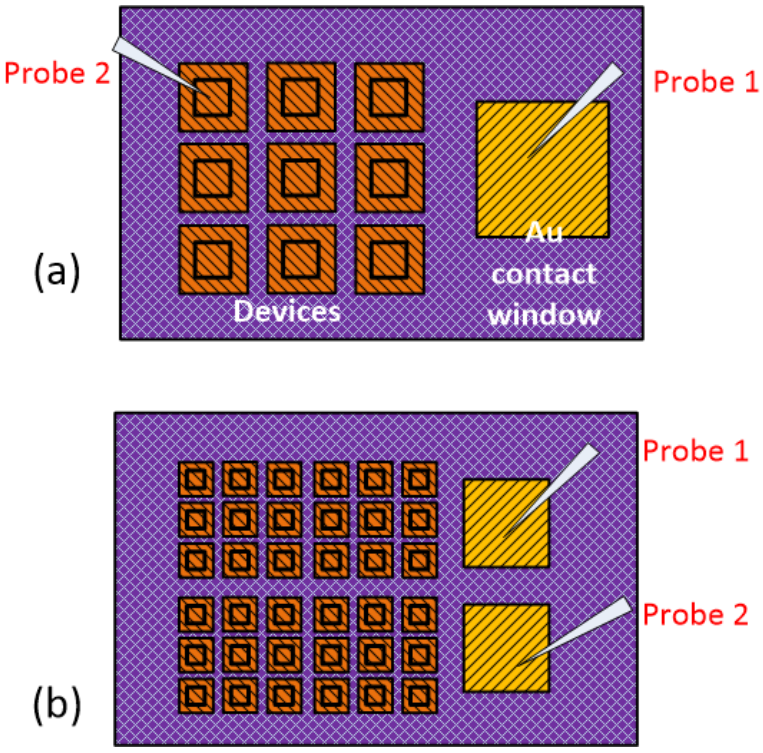


Figure 3-27 Schematic drawing of probe placement during (a) normal measurement of devices and (b) test of Au CE resistance.

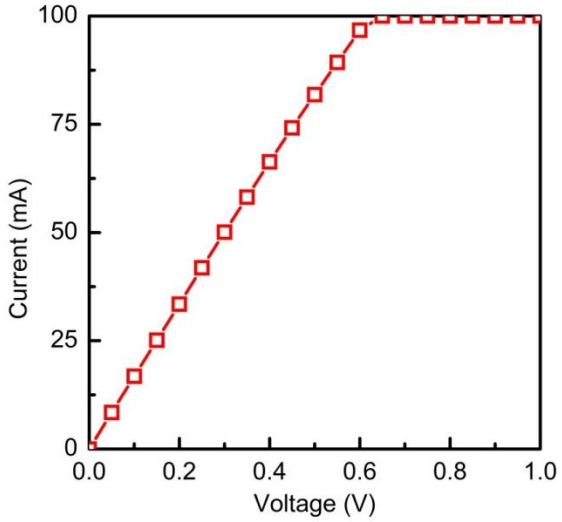


Figure 3-28 I-V curve of two probe needles placed on two adjacent Au contact windows.

Moreover, as shown in Figure 3-27 (a) there is certain lateral distance between the device active area and the Au contact windows. And the resistance from this Au layer and the contact resistance between the Au layer and the probe needle will also add to the apparent resistance of the device. Results shown in Figure 3-28 was obtained with two probe needles placed on two Au contact windows approximately 3 millimetres apart (Figure 3-27(b)), and the resistance from this Au layer and two contact resistance was 6.20Ω, which is negligible compared to the resistance of the Cu/a-SiC/Au devices. With the possible contribution from contact resistance, Au layer resistance and SiO_2 layer eliminated, the I-V data shown later can be expected to be from the actual Cu/a-SiC/Au devices only.

3.2.3 Temperature Controlled Tests

Temperature controlled tests are required in two aspects of characterization of RMs: retention performance and temperature dependency of R_{ON} and R_{OFF}.

As discussed in Section 2.3, a commonly adopted method of predicting retention performance is to monitor device's resistance over a short period of time at elevated temperature, and extrapolate the power-law dependence to 10 years' time [98, 159]. To assess the retention performance of our RMs, for each batch of devices, two identical devices have been used with one in LRS and the other HRS. Subsequently, the R_{ON} and R_{OFF} from these stable LRS and HRS respectively, have been measured using 0.1V over a period of time at 85°C to enable power law extrapolation analysis of the device retention.

Moreover, as discussed in Section 2.3, RMs typically show metallic conduction at LRS and semiconductor/insulator conduction at HRS. And this feature is commonly used to

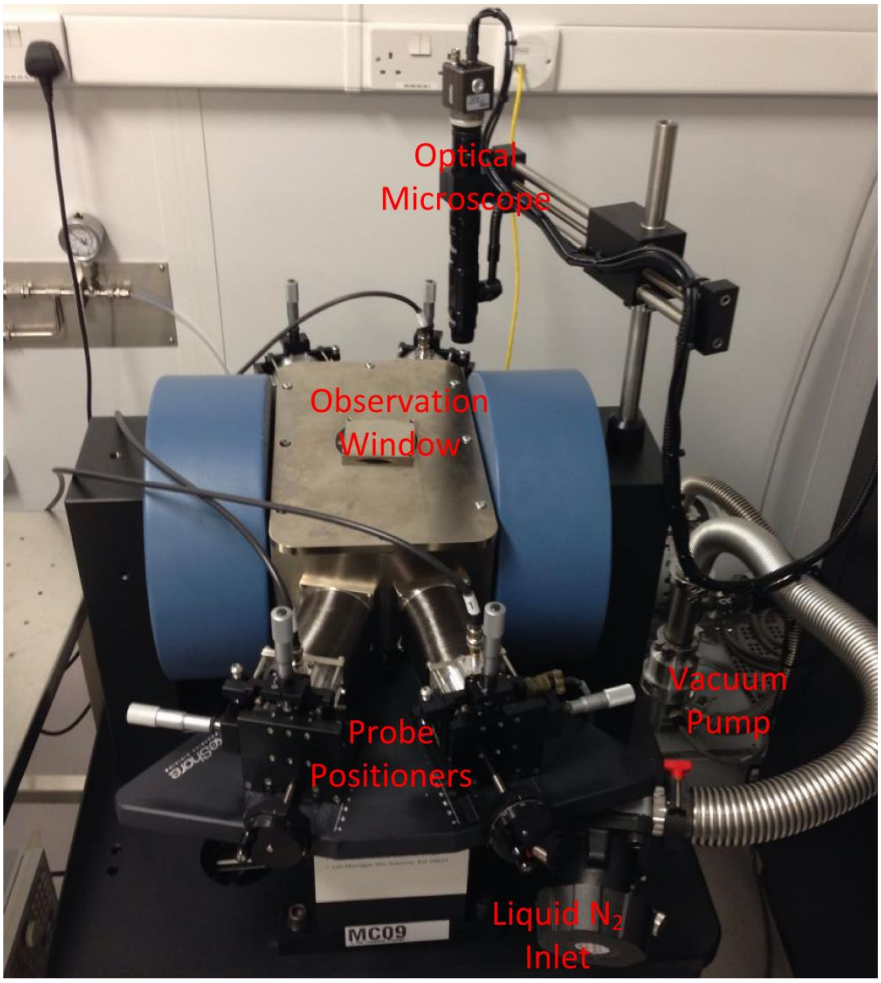


Figure 3-29 Photo of the temperature controlled chamber for I-V measurement.

In these tests the switching I-V and R_{ON} and R_{OFF} were still measured by an Agilent B1500A. And the samples were placed in a temperature controlled chamber shown in Figure 3-29. The schematic diagram of the whole setup is shown in Figure 3-30.

As Figure 3-29 shows, the sample chamber has four probes that are connected to the Agilent B1500A. There is a small observation widow on top of the chamber, and an optical microscope is used to help the positioning of probes. The samples are placed on top of a copper plate, which has a heater resistor and a thermistor attached. The inflow of liquid N_2 can only be manually adjusted, but it is usually set to a steady flow during low temperature test. The temperature control unit will automatically adjust the heater resistor according to the set temperature point and current temperature. To prevent icing on sample surface during low temperature tests, the chamber is pumped below 10^{-5} mBar before and during tests, which usually takes over two hours. So far temperature range

between 140K and 358K has been achieved by this setup. This setup was also used to measure the temperature dependence of resistivity of the a-SiC and a-SiC/Cu films.

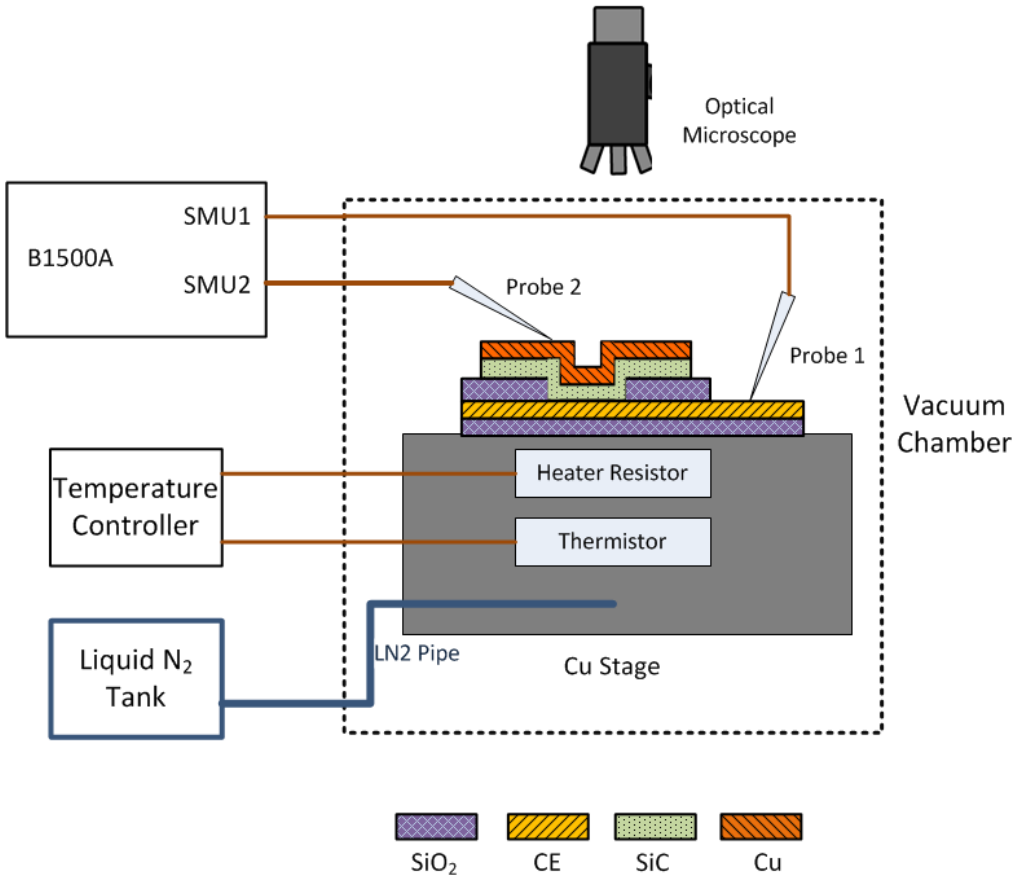


Figure 3-30 Schematic drawing of the temperature controlled electrical testing setup.

3.3 Material Characterization of Sputtered Thin Films

3.3.1 Characterization of Chemical Composition

X-ray Energy Dispersive Spectrometer (EDS)

X-ray Energy Dispersive Spectrometer (EDS or EDX) determines the composition of sample by measuring the energy of X-ray radiation resulted from the bombardment of electrons to the specimen. When the incident electron has high enough energy, there is a certain chance that the incident electron will knock an inner orbit electron out of its orbit, leaving a vacancy in the inner electron shell. The vacancy will then be filled by an electron from outer electron shell, and the excessive energy of the electron is dispersed as X-ray radiation. The energy of such X-ray radiation is therefore determined by the electron shell energy level, and can be used to qualitatively determine the elemental composition. By

measuring the number of X-ray photons with specific energy, the relative ratio of elements can also be determined.

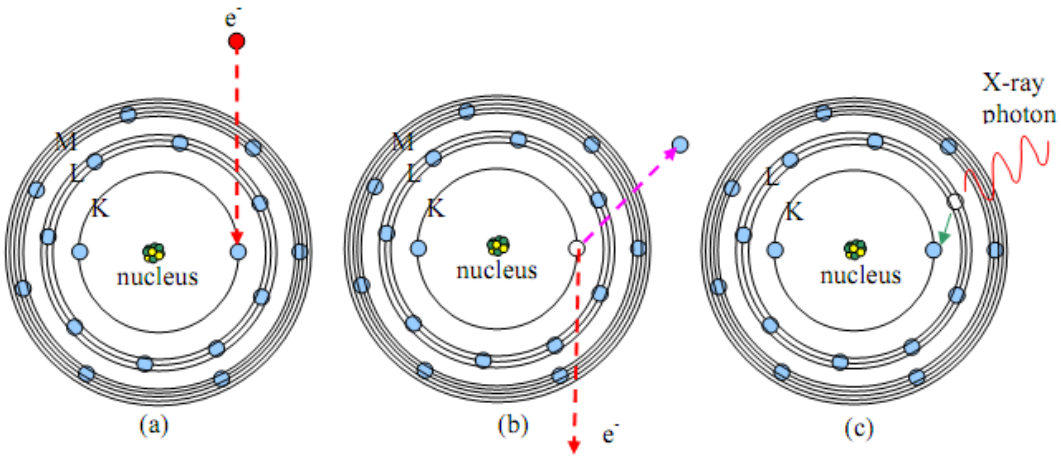


Figure 3-31 Production of K_α X-ray by an incident electron [93].

An Oxford Inca 300 X-ray Energy Dispersive Spectrometer system attached to a JSM 6500F filed emission scanning electron microscope is used to measure the composition of the deposited films. In the measurement an area of 1mm*1mm is scanned by the electron beam for 1 minute, and one of the accumulated X-ray energy spectrum is shown in Figure 3-32. The energy of the Kα line associated with Si atom is 1.74 KeV, C atom 0.277 KeV, and Cu atom has a Lα line of 0.93 KeV [160]. The results show excessive C in the film, possibly due to surface contamination. The results of EDS measurement on all the a-SiC/Cu films are shown in Section 4.1

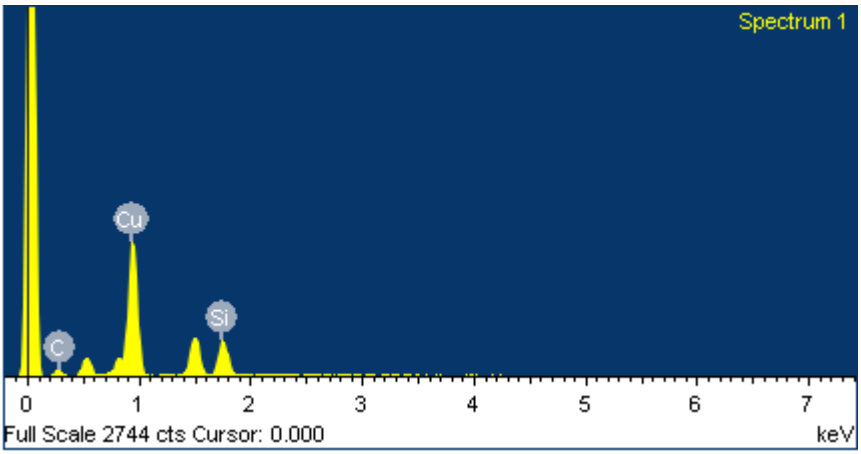


Figure 3-32 EDS spectrum of sample coated with a-SiC/Cu film, the atomic percentage of Cu is 41.6%, Si 18.6%, C 39.2%.

X-ray photoelectron spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) is a quantitative surface analysis technique developed in the 1960s. XPS is capable of measurement of elemental composition, chemical states and electron states. In XPS analysis, monoenergetic X-rays (this project used Al-Kα photons with an energy of 1486.6eV) are used to irradiate the surface of the sample. Electrons are then emitted from the surface as a result of the photoelectric effect. The emitted electrons are collected and their number and kinetic energies measured. The kinetic energy (KE) of emitted electrons is given by:

$$\mathrm{KE} = h\upsilon - \mathrm{BE} - \phi_s \qquad (3\text{-}1)$$

Here $h\upsilon$ is the energy of the X-ray photon, BE is the binding energy of the atomic orbital from which the electron originates, and ϕ_s is the spectrometer work function. With known $h\upsilon$ and ϕ_s, BE can be determined from the measured kinetic energy of emitted electrons. As each element has a unique set of binding energies, XPS spectrum can be used to identify the chemical composition of the sample, and the chemical states of elements in the sample can be determined by the variations in the binding energies.

Although the X-ray photons can penetrate several micrometers into the sample surface, only electrons that originate within several nanometers of the surface can escape the sample without energy loss, because the electrons have a much higher probabilities of interaction with matter than the photons. The electrons that escape the sample without energy loss form the peaks in the XPS spectra, and the other electrons constitute the background. As a result XPS is a surface sensitive technique, and surface contamination may be detrimental for XPS analysis. To limit the effect of surface contamination, in addition to employing an ultra-high vacuum environment, XPS systems are often fitted with an Ar^+ ion sputtering gun. The ion gun can be used to remove a thin layer of surface material, and a depth profile of chemical composition may also be achieved by repeated sputtering/XPS analysis.

In this project XPS analysis of a-SiC and a-SiC/Cu films were performed by Thermal Scientific ® Theta Probe XPS system (Figure 3-33) equipped with an Al-Kα X-ray source ($h\upsilon = 1486.6$eV). Ar surface sputtering was also applied to reduce surface contamination. The results of XPS measurement on selected a-SiC and a-SiC/Cu films are shown in Section 4.1

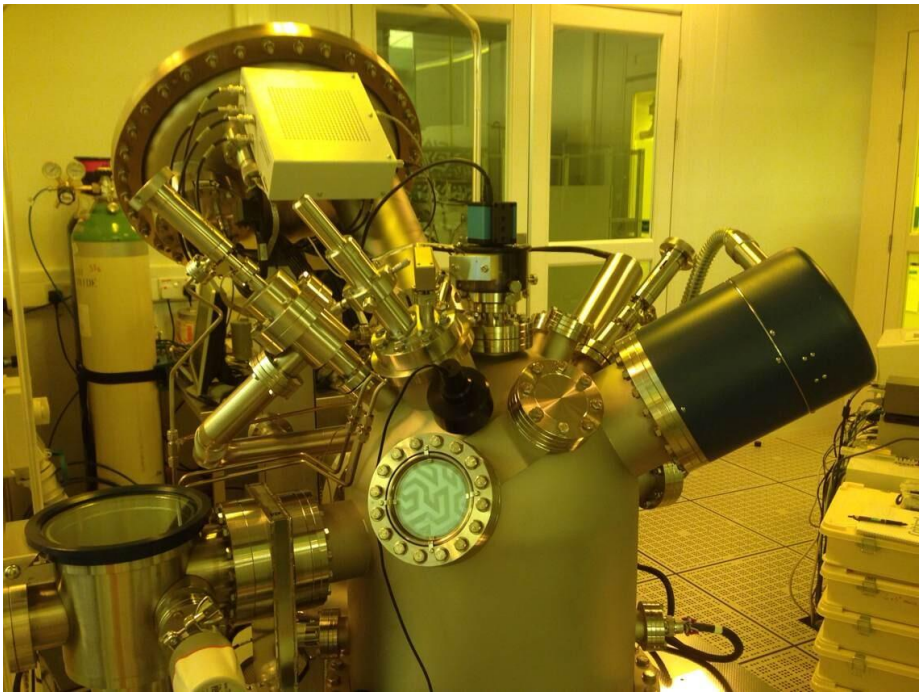


Figure 3-33 Photo of the Thermal Scientific ® Theta Probe XPS system.

3.3.2 Characterization of Structural Properties

Film Thickness

Film thickness is an important factor in both constructing the switching devices and calculating material properties of obtained films. In the project, thickness of deposited films is measured by a Tencor P-11 stylus surface profiler. In thickness measurement, the stylus scans around the edge of deposited films while continuously recording the surface height and current scan position. The profiler measures film edges created by either lift-off or shadows of sample holder. The touch-down force of the stylus is set to 0.5mN, scan speed 50~100 μm/sec and sampling rate 100~200 Hz. For each film, measurement is performed at three different locations to reduce error.

To measure the deposition rate of a-SiC, several test runs were conducted. In the test runs sputtering deposition was conducted for 30 minutes, and the resulting film thickness was measured by the surface profiler. The average deposition rate was then used to determine the actual deposition time of resistive memory devices.

X-ray Diffraction (XRD)

X-ray Diffraction (XRD) is a widely applied technique that determines the crystal structures of materials. To have significant diffraction effect, the incident waves must have wavelengths comparable to the distance between obstacles. In XRD measurements, X-rays are commonly produced by bombarding a Cu or Mo solid target with a focused electron beam, which emit X-rays with wavelength of 1.54Å and 0.8Å, respectively. XRD is fundamentally based on Bragg diffraction, shown in Figure 3-34. The incident X-ray is partially scattered by atoms when they strike the surface of a crystal. The part of the X-ray that is not scattered passes through to the next layer of atoms, where again part of the X-ray is scattered and part passes through to the next layer. This causes an overall diffraction pattern, and the constructive diffraction peaks can only occur when [161]:

$$n\lambda = 2d\sin\theta \tag{3-2}$$

Where n is an integer, λ is the wavelength of the incident X-ray, θ is the scattering angle, and d is the distance between atom layers. The diffraction pattern is therefore determined by the crystal structure of the sample, and can be used to identify unknown crystals.

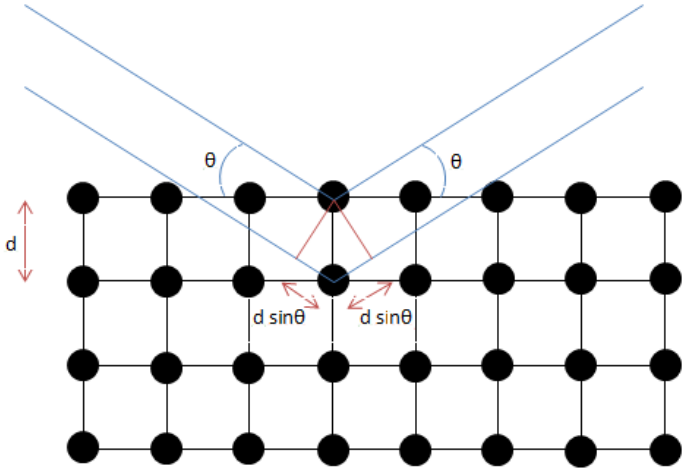


Figure 3-34 Bragg diffraction in a crystal.

In addition to single crystal samples, XRD can also be applied to samples that contain many individual crystals of random orientation. This technique is called powder XRD. In powder XRD, diffraction of all angles of 2θ happens simultaneously because of the random orientation of crystalline domains, therefore in a powder X-ray diffractometer, the X-ray source is normally placed at a fixed angle relative to the sample, while the detector rotates to measure the diffraction. In addition, the grain size L of the crystalline domains

can be determined by the Scherrer's formula [162] when L is sufficiently small (<100s nm):

$$B(2\theta) = \frac{K\lambda}{L\cos\theta} \tag{3-3}$$

Where B is the peak width at half the maximum intensity (FWHM), K is the shape factor close to 1, λ is the X-ray wavelength, and θ is the Bragg angle.

In this project XRD analysis was performed on the a-SiC and a-SiC/Cu film with a Rigaku Smartlab XRD system shown in Figure 3-35. This system used a Cu X-ray source with 1.54Å wavelength. The scan range was set to 20° to 80°, with scan step being 0.02°. The scan rate was 7° per minute. As the deposited a-SiC and a-SiC/Cu films were only 200~500nm thick, the incident X-ray would penetrate these films and pick up signal from the substrate. The incident angle was therefore set to 1° to minimize the possible contribution from the Si substrates. Figure 3-35(b) shows the arrangement of the sample state, X-ray source and detector: the X-ray source and sample stage remain still during the scan so the incident angle remains 1° and the detector rotates to receive the diffracted X-ray at different angles. The results of XRD measurement on all the a-SiC and a-SiC/Cu films are shown in Section 4.2

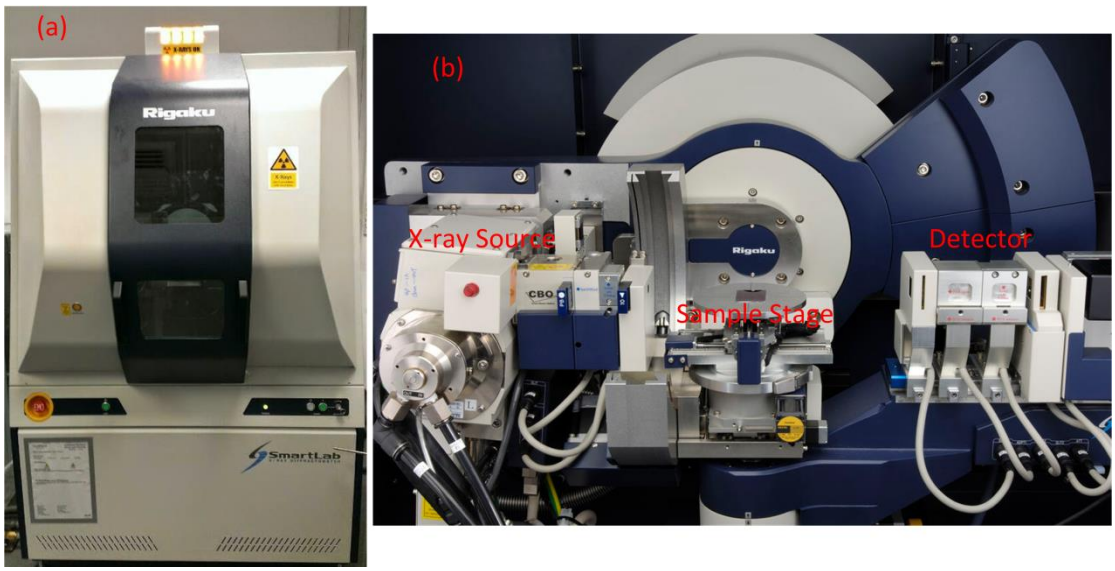


Figure 3-35 (a) photo of the Rigaku Smartlab XRD system and (b) detailed photo of the sample stage, X-ray source and detector.

Atomic Force Microscopy (AFM)

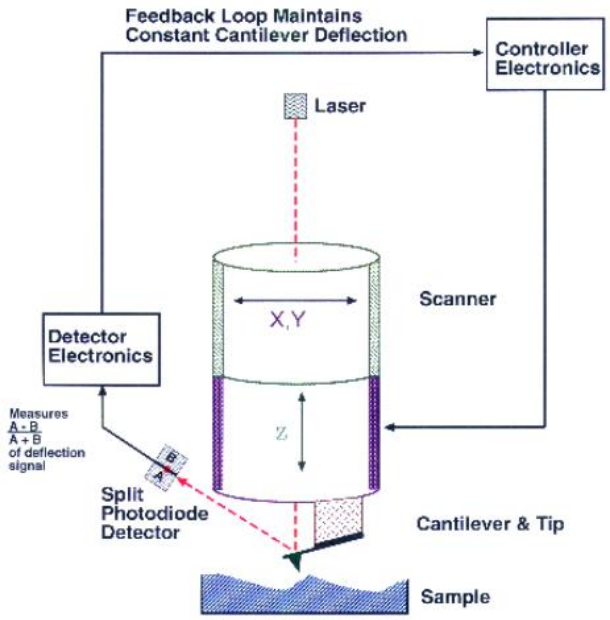


Figure 3-36 Schematic diagram showing the operating principles of atomic force microscopy in contact mode [163].

Atomic Force Microscopy (AFM) is capable of imaging material surface morphology with atomic resolution on a wide range of conductive and insulating materials. An AFM is usually capable of several imaging modes, and the operating principle of contact mode is shown in Figure 3-36: A cantilever with a sharp tip is driven by a piezoelectric actuator. At the beginning of the imaging process, the probe tip is brought into a close distance with the sample surface, where the sample exerts a weak repulsive force in the order of 10^{-9}N on the probe tip. As the probe scans through the sample surface, the deflection of the cantilever is monitored by a laser beam reflected from the back of cantilever, and the monitored deflection is feedback to a controller circuit to drive the piezoelectric actuator to maintain a constant deflection. The movement of the piezoelectric actuator in the Z direction is therefore a measure of the height of sample surface.

In contact mode, the probe tip is constantly in a very short distance from the sample, abrupt change of surface height may cause damage to the sample or the tip. Consequently, tapping mode is more commonly used instead. In tapping mode, the cantilever is driven by the piezoelectric actuator to oscillate with an amplitude of ~100s nanometres. The oscillating tip is then moved toward the surface until it begins to lightly touch, or tap the surface. As the oscillating cantilever begins to intermittently contact the surface, the amplitude of cantilever oscillation is reduced due to energy loss caused by the tip

contacting the surface. The reduction in oscillation amplitude is used to identify the surface features.

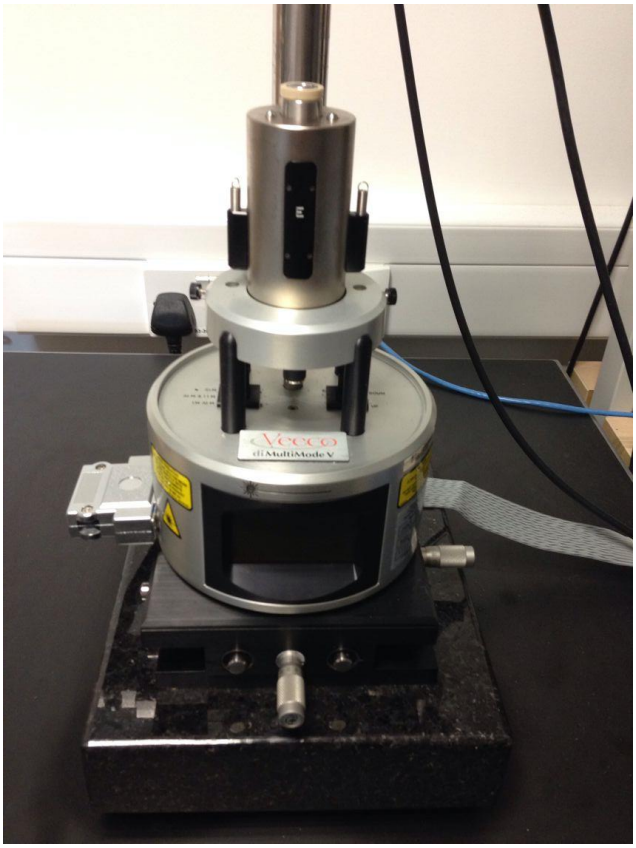


Figure 3-37 photo of the Veeco Multimode V AFM used for AFM surface study.

In this project, surface image of a-SiC and a-SiC/Cu films have been acquired by a Veeco Multimode V AFM (shown in Figure 3-37) operating in tapping mode. The scan area size was set to 1μm by 1μm square. The images were composed of 512 lines and each line had 512 data points. The scan rate was 0.5 line per second. The AFM images obtained are shown in Section 4.2. For future studies, conductive AFM may be worth exploring as a tool to directly identify the conductive filament of a RM device.

3.3.3 Characterization of Electrical Properties

Van der Pauw method and Hall Effect

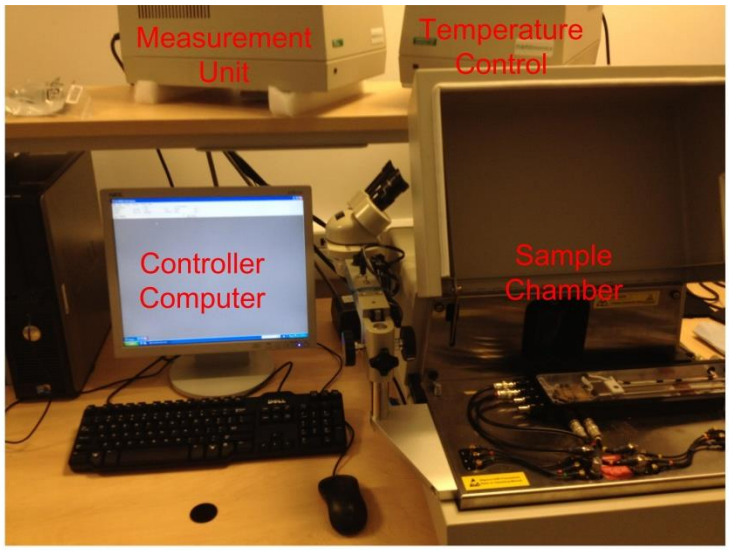


Figure 3-38 photo of the main components of the HL5500PC system.

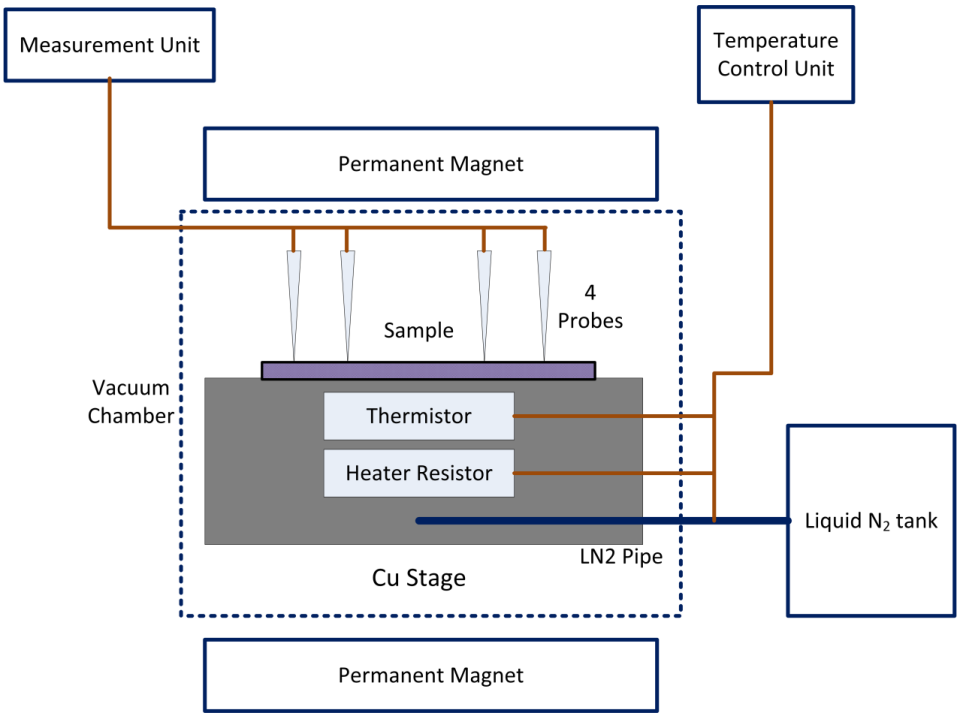


Figure 3-39 Schematic drawing of the HL5500PC system, including the details of the sample chamber.

The electrical conductivity of obtained films is primarily measured by a HL5500PC system in ECS measurement lab. The HL5500PC system is capable of both Van der Pauw method

of resistivity measurement and Hall Effect measurement for carrier mobility and carrier concentration measurement.

As shown in Figure 3-38 (a), HL5500PC system is composed of a controller computer, a measurement unit, a temperature controller unit and a sample chamber. The system is capable of resistivity and Hall Effect measurement at 77K to 550K. The upper limit of sample resistivity is 100 GΩ/square and the lowest measurable current is 1pA. Figure 3-38 (b) shows a more detailed view of sample chamber. The sample is to be placed on the central copper plate, the temperature of which is measured by a thermal couple attached to its back side. The temperature control unit controls both the liquid N_2 flow and the heater resistor to maintain the desired temperature. And the whole sample chamber is vacuum sealed during temperature controlled measurements. Due to the size of the sample chamber, sample cannot exceed 15mm*15mm. Finally a U-shaped permanent magnet are extended to supply the magnetic field required for Hall Effect measurement.

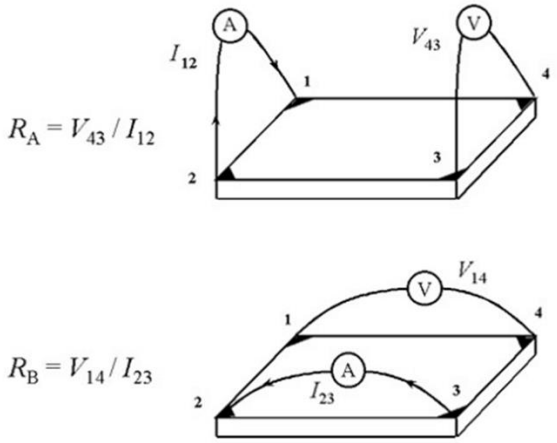


Figure 3-40 I/V measurement configurations in Van der Pauw method .

For resistivity measurement, HL5500PC system uses a standard Van der Pauw method. L.J. van der Pauw proved for a flat sample with arbitrary shape, if these conditions are met:

• The contacts are at the circumference of the sample.

• The contacts are sufficiently small.

• The sample is homogeneous in thickness.

• There are no isolated holes in the sample.

Then we have the following equation [164]:

$$\exp(\frac{-\pi \cdot R_A \cdot d}{\rho}) + \exp(\frac{-\pi \cdot R_B \cdot d}{\rho}) = 1 \quad (3\text{-}4)$$

Where d is the thickness of the sample, ρ the resistivity of the sample, and R_A, R_B measured in the configuration shown in Figure 3-40. With R_A, R_B measured and known thickness, the resistivity of the sample can be calculated numerically. In the HL5500PC system, only the amplitude of applied current needs to be set to an appropriate value, and the system will automatically switch I/V pairs and calculate the resistivity of the sample.

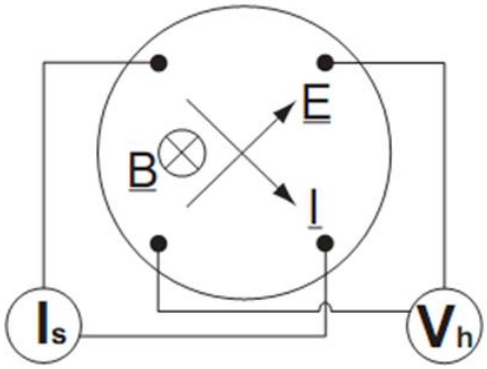


Figure 3-41 Illustration of the principle of Hall Effect measurement.

The HL5500PC system measures carrier concentration and carrier mobility by Hall Effect, the principle of which is shown in Figure 3-41: An adjustable current (I) is applied through the sample, and a magnetic field (B) is applied perpendicular to the sample. Due to Lorentz force, current carriers will drift in a direction perpendicular to the current in plane. Eventually the accumulation of carriers will create an electric field which balances the Lorentz force. The Hall voltage (V_h) is therefore the voltage between two contacts perpendicular to the direction of I. From these values, the Hall Efficient (R_H) is defined as:

$$R_H = \frac{V_h \cdot t}{I \cdot B} \quad (3\text{-}5)$$

Where t is the thickness of the sample. And by assuming there's only one type of carriers (electrons or holes), the carrier concentration (n_c) is given by:

$$n_c = -\frac{1}{eR_H} \tag{3-6}$$

And the carrier mobility is:

$$\mu = |R_H| \cdot \sigma \tag{3-7}$$

Where σ is the conductivity of the sample, which can determined by Van der Pauw method.

In practice, because the a-SiC and a-SiC/Cu films have relatively low carrier concentration or carrier mobility, the measured Hall voltage is only in the range of 10^{-3} to 10^{-5}V. Such low Hall voltage can be susceptible to noise and other issues during measurement such as contact misalignment (the contact pair for current supply is not perpendicular to the pair for Hall voltage measurement). In future work, it may be worthwhile to deposit metal contacts at the edges of the thin film samples to ensure better contact between sample and contact needles, and to reduce contact misalignment.

Transfer length method

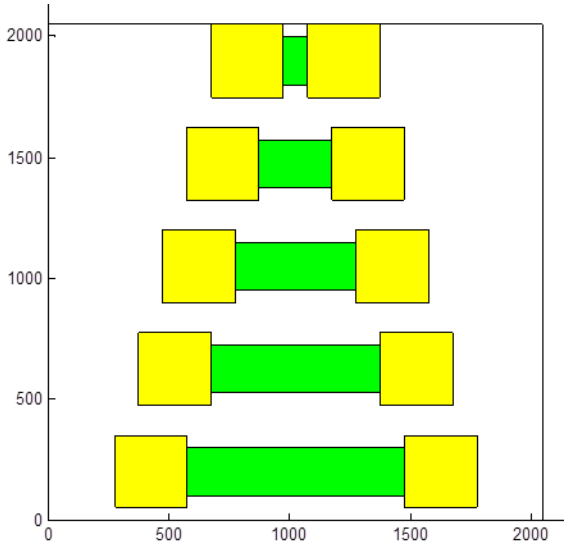


Figure 3-42 Design of Cu/a-SiC/Cu test structures for the resistivity measurement using transfer length method. The green region will be sputtered a-SiC, and the yellow region will be Cu electrodes on top of a-SiC. The numbers are pixel counts and each pixel corresponds to 0.5μm*0.5μm dot in laser direct-writer lithography.

For sputtered pure SiC film, due to its very high resistivity, HL5500PC system cannot produce repeatable results. Transfer length method [165] was therefore used to measure

the resistivity of sputtered pure SiC film, and the possible contact resistance between SiC layer and sputtered metal Cu layer.

Assuming:

• Resistance of SiC strips increases linearly with the length of the strips.

• Resistivity of sputtered SiC stays consistent across strips.

• Contact resistance from two copper/SiC contacts stays consistent.

Then with known dimensions of the sputtered SiC strips, both film resistivity and contact resistance can be calculated by measuring the resistance values of a series of test structures with different length but consistent contact area. The design of the test structures are shown in Figure 3-42. The green region will be sputtered SiC, and the yellow region will be Cu electrodes on top. The patterns are defined by laser direct writer lithography and lift-off after sputtering. All the test structures are fabricated on Si substrates with 1μm thermal oxide layer, so the structures are electrically insulated. The width of the SiC strips is constant 50μm. The contact area between Cu and SiC is 25μm*50μm; and the length of the SiC stripes is 50μm, 150μm, 250μm, 350μm and 450μm, respectively. The results from these electrical property characterizations are shown in Section 4.3.

Chapter 4. Material Properties of a-SiC Films

As stated in earlier chapters, the main objectives of this project require fabrication and testing of resistive memory devices with sputtered a-SiC and co-sputtered a-SiC/Cu as solid electrolyte. It is therefore essential to investigate the relevant material properties, such as composition, morphology and electrical conduction properties, of the obtained a-SiC and a-SiC/Cu films, to have a more complete understanding of the behaviour of corresponding devices. Moreover, metal doped SiC thin films have recently been studied for their magnetic [166-168], optical [157, 167, 169] and electrical properties [166, 170-172]. The characterization of these a-SiC/Cu films may contribute to this field. The characterization of these a-SiC/Cu films may also promote the understanding of related nano-scale phenomenon such as electrical conduction in metal/insulator composite films. The results of material characterization on a-SiC and a-SiC/Cu films so far are presented in this chapter.

4.1 Deposition Conditions and Film Composition

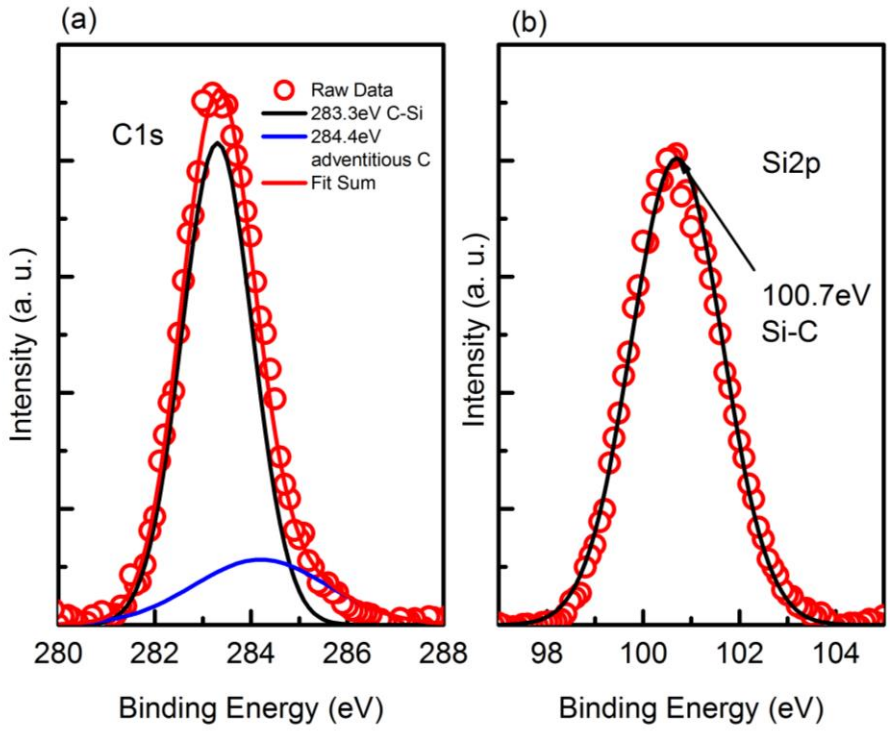


Figure 4-1 (a) C 1s and (b) Si 2p curve fitted XPS spectra of as-deposited a-SiC film.

The general deposition conditions and relevant equipment for the sputtering deposition of a-SiC thin films in this project have been discussed earlier in Section 3.1. To examine the

composition of obtained film, XPS measurement was performed on an as-deposited a-SiC layer and the results are shown in Figure 4-1. Binding energies of Si2p and C1s peaks are at 100.7 eV and 283.3 eV respective which are expected from a-SiC films [173]. Peak fittings in Figure 4-1 also suggested the bonding components in the as-deposited SiC films are predominantly Si-C bond. Moreover, from the area of the fittings and atomic sensitivity factors of C 1s and Si 2p, the Si to C atomic ratio can be estimated to be 1.1:1.

The sputtering power configurations and the corresponding deposition rate and adjusted Cu atomic percentage of a-SiC/Cu films are listed in Table 4-1. The minimum stable sputtering power for Cu target was 10W, therefore co-sputtering of two SiC targets and one Cu target has been adopted in attempt to lower the Cu content of resulting films, as indicated by two values in the SiC power column. For instance, the maximum sustainable sputtering power for SiC targets was one at 340W and the other 300W, i.e. 340+300 (W). Thickness of obtained films was measured by stylus profiler, and deposition rate for each power configuration was then attained.

Sample Batch	**SiC Power (W)**	**Cu Power (W)**	**Deposition Rate (nm/min)**	**Adjusted Cu atomic %**	**Resistivity (Ω·cm)**
SiCCu04	250	0	4.19	0	7.67E7
SiCCu08	340+300	10	12.99	18	6.05E2
SiCCu09	300+300	10	12.12	20	10.3
SiCCu10	250+250	10	10.54	21	7.07
SiCCu11	200+200	10	7.8	25	4.71
SiCCu05	250	15	5.23	28	0.069
SiCCu13	150+150	10	5.68	38	0.15
SiCCu06	250	25	8.89	43	0.026
SiCCu07	250	35	9.65	53	0.016

Table 4-1 Sputtering power configurations and corresponding deposition rates and estimated Cu atomic percentage of undoped a-SiC and a-SiC/Cu films.

As discussed in Section 3-3, the composition of obtained a-SiC/Cu films were analysed by EDX. The composition readings directly from the analysing software, however, usually showed noticeably higher carbon atomic percentage than silicon, possibly due to surface contamination. Copper atomic percentage listed in Table 4-1 are therefore adjusted by assuming a 1:1 Si to C ratio, i.e.:

$$\text{Adjusted Cu at.}\% = \frac{Cu\ at.\%}{Cu\ at.\% + 2 * Si\ at.\%} \tag{3-1}$$

Cu 2p XPS spectra from a-SiC/Cu films with 28, 43 and 53 at. % Cu are shown in Figure 4-2. The spectra were calibrated using O 1s peak: Assuming the oxygen content was from silicon oxide, the O1 s peaks are expected to be at 532.9 eV. The spectra were all obtained after 2 minute Ar sputtering etch to remove surface contamination. From Figure 4-2, it can be seen that after calibration all three Cu spectra show $2p_{3/2}$ peaks at 932.6~932.9 eV, which correlates to possibly Cu or Cu_2O states. Nevertheless, no Cu_2O peak at 530.5 eV was observed in the O 1s spectra. Therefore it is reasonable to believe the added copper did not react with a-SiC or oxygen, but remained as metallic Cu. The absolute intensity of the Cu peaks does not correlate to the Cu at.%. The exact cause for this is still unknown but it's possibly related to the distance between the sample surface and the detector.

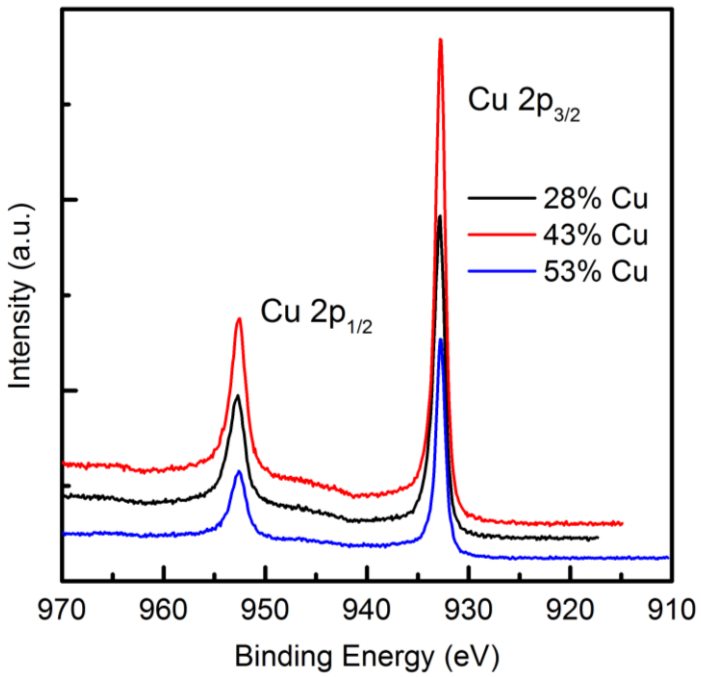


Figure 4-2 Cu 2p XPS spectra of a-SiC/Cu films.

4.2 Structural Characterization

4.2.1 XRD Spectra

Figure 4-3 shows the XRD spectra of the SiC sputtering target and as-deposited SiC film. The spectra of the SiC film were amplified by 200 times to be comparable to that of SiC target. The characteristic 3C-SiC (111) XRD peak at 35.7° [174] is clearly observed from the SiC target, while no peaks are shown from the as-deposited SiC layer, suggesting amorphous status of the as-deposited SiC.

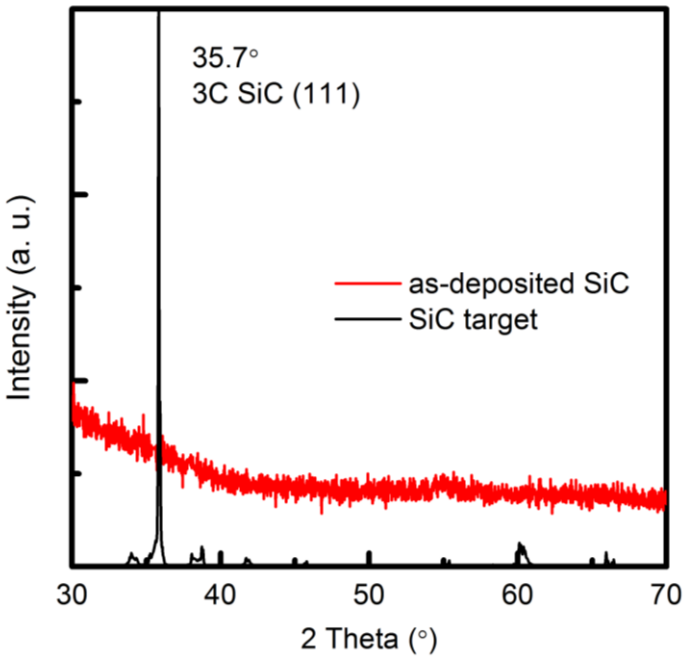


Figure 4-3 XRD spectra of SiC sputtering target and as-deposited SiC film.

The XRD spectra of a-SiC/Cu films deposited with different Cu sputtering power are shown in Figure 4-4. The intensity of peaks around 43° clearly increases as the Cu sputtering power increases.

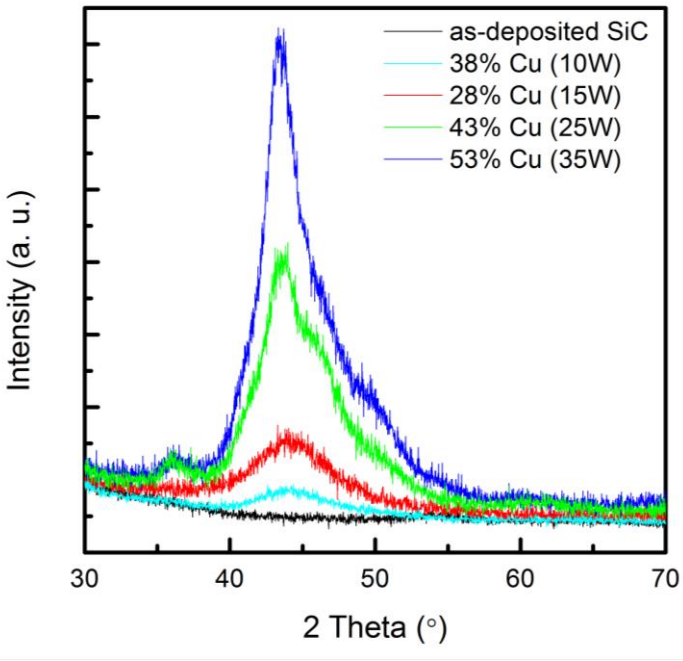


Figure 4-4 XRD spectra of a-SiC and a-SiC/Cu films deposited with different Cu sputtering power.

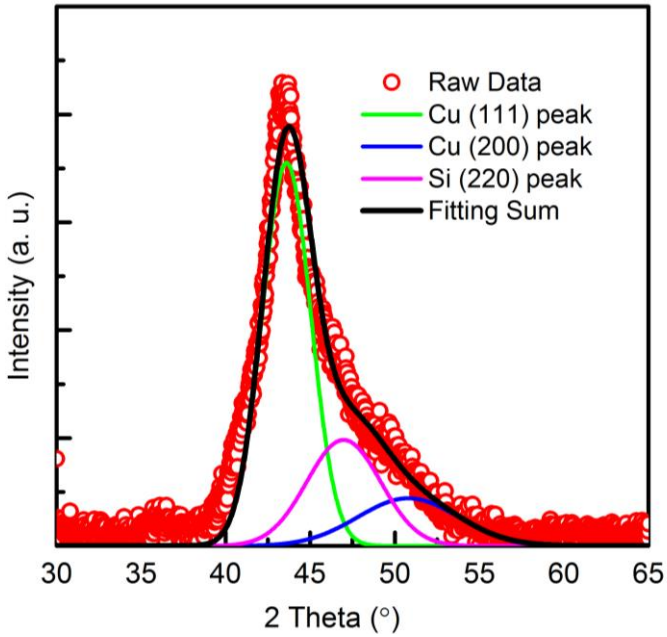


Figure 4-5 Curve fitted XRD spectra of a-SiC/Cu film deposited with 35W Cu sputtering power (53 at. % Cu).

The deconvolution of such peak of the 53 at. % Cu a-SiC/Cu film is shown in Figure 4-5. The spectra is mainly consist of Cu (111) peak at 43.6° and weak Cu (200) peak at 50.8° [175], with possible Si (220) peak from nano-crystalline Si at 46.0° [176]. The full width at half maximum of the Cu (111) peak is 3.36°. And using Scherrer's formula (eq. 3-3) [162], the estimated Cu particle size is approximately 2.7nm. The peaks widen at half maximum as the Cu sputtering power decreases. Therefore lower Cu power leads to smaller Cu

particle size, and the minimum size is ~0.9nm. The relatively small particle size is promising for the possible application of a-SiC/Cu films as solid electrolyte layer in resistive memories, because the particle size is considerably smaller than device dimension, and the added Cu can be expected to distribute evenly in the device active area.

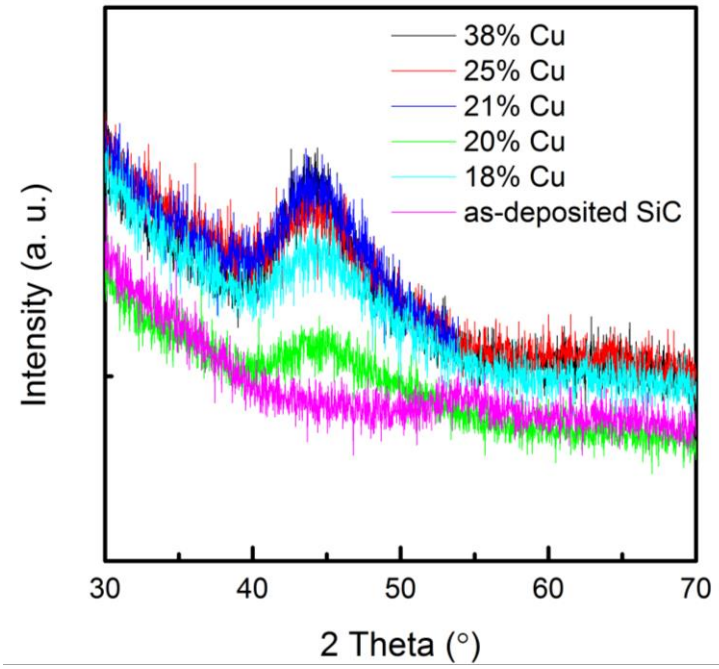
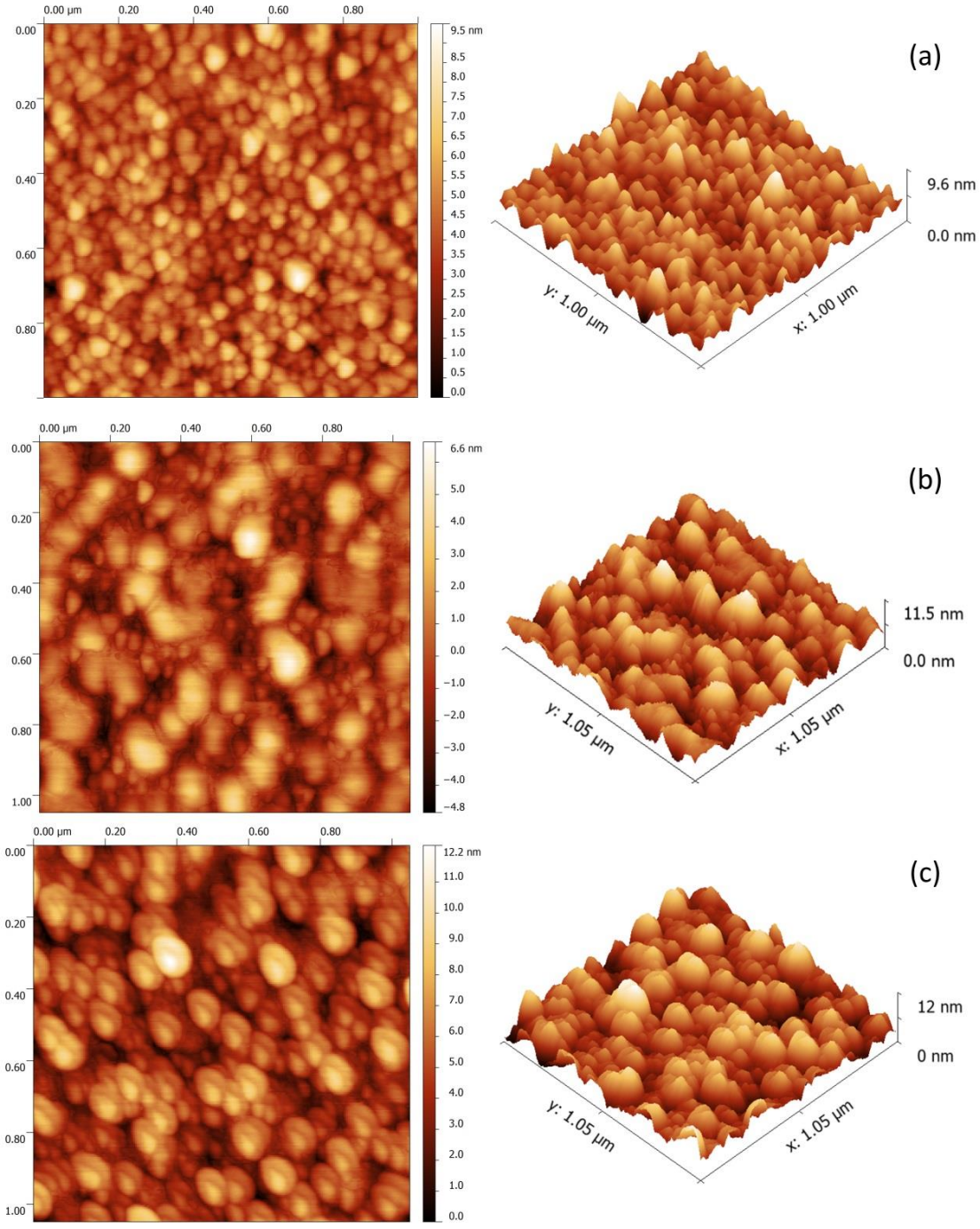


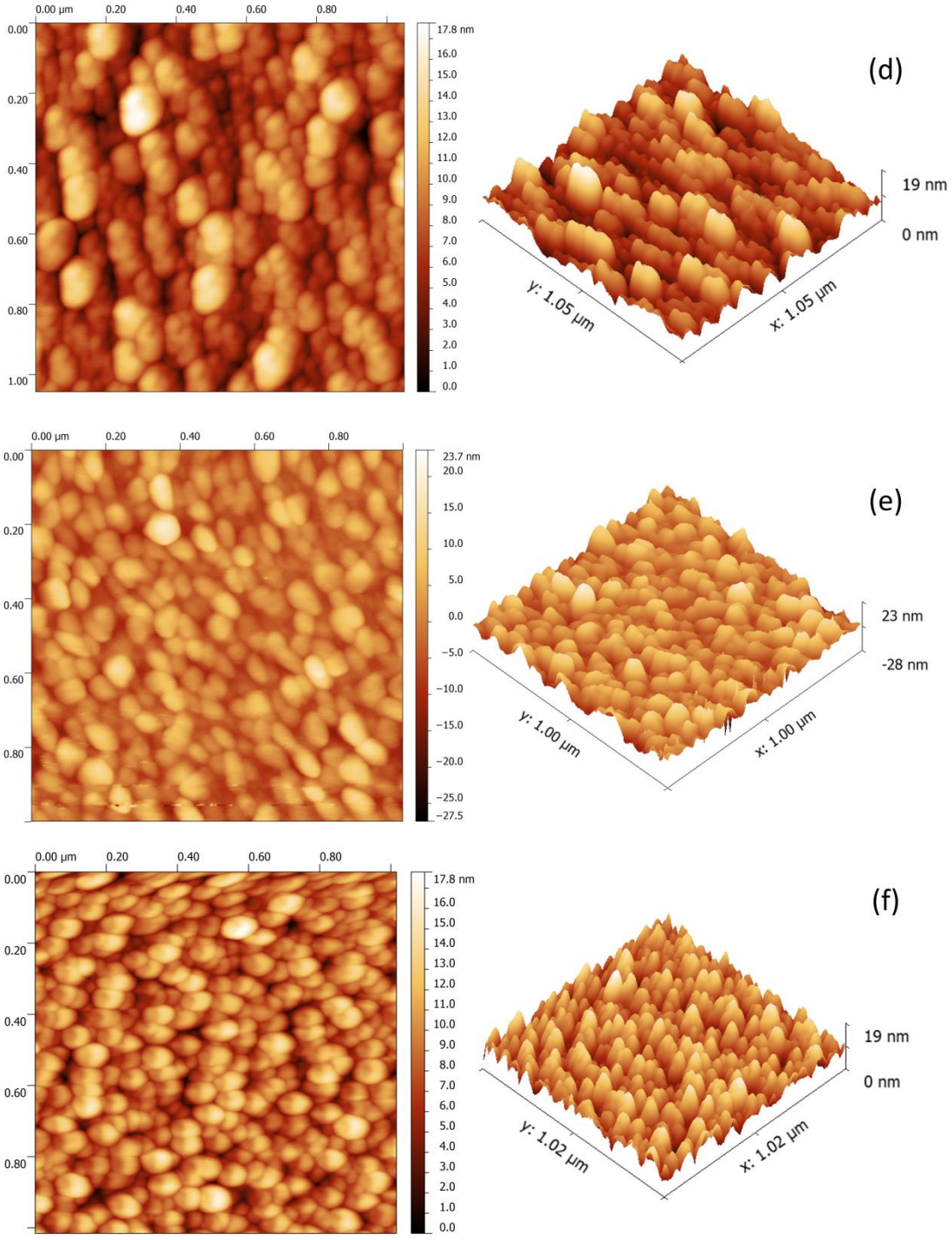
Figure 4-6 XRD spectra of a-SiC and a-SiC/Cu films of different Cu percentage but same Cu sputtering power (10W).

The a-SiC/Cu films deposited with the same 10W Cu sputtering power exhibited very similar XRD spectra, as shown in Figure 4-6. This indicates crystallization of deposited Cu is only related to the Cu sputtering power and is not affected by the SiC sputtering power. In the fabrication of RMs based on a-SiC/Cu, Cu sputtering power was 10W~15W, so the resulting Cu particle size can be expected to be around 1nm.

4.2.2 AFM Imaging

From the AFM images shown in Figure 4-7, the surface roughness and grain size of the a-SiC and a-SiC/Cu films both noticeably increase as the Cu percentage increases. The grain size of the undoped a-SiC film is around 20~30 nm, and grain size of the 53 at. % Cu a-SiC/Cu film is around 100 nm. The RMS roughness increases from 1.2 nm to over 4 nm, as shown in Figure 4-8.


0.00 µm
0.20
0.40
0.60
0.80
9.5 nm
6.6 nm
12.2 nm
(a)
(b)
(c)
9.6 nm
0.0 nm
11.5 nm
0.0 nm
12 nm
0 nm
y: 1.00 µm
x: 1.00 µm
y: 1.05 µm
x: 1.05 µm


0.00 µm
0.20
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(d)
19 nm
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y: 1.05 µm
x: 1.05 µm
23.7 nm
20.0
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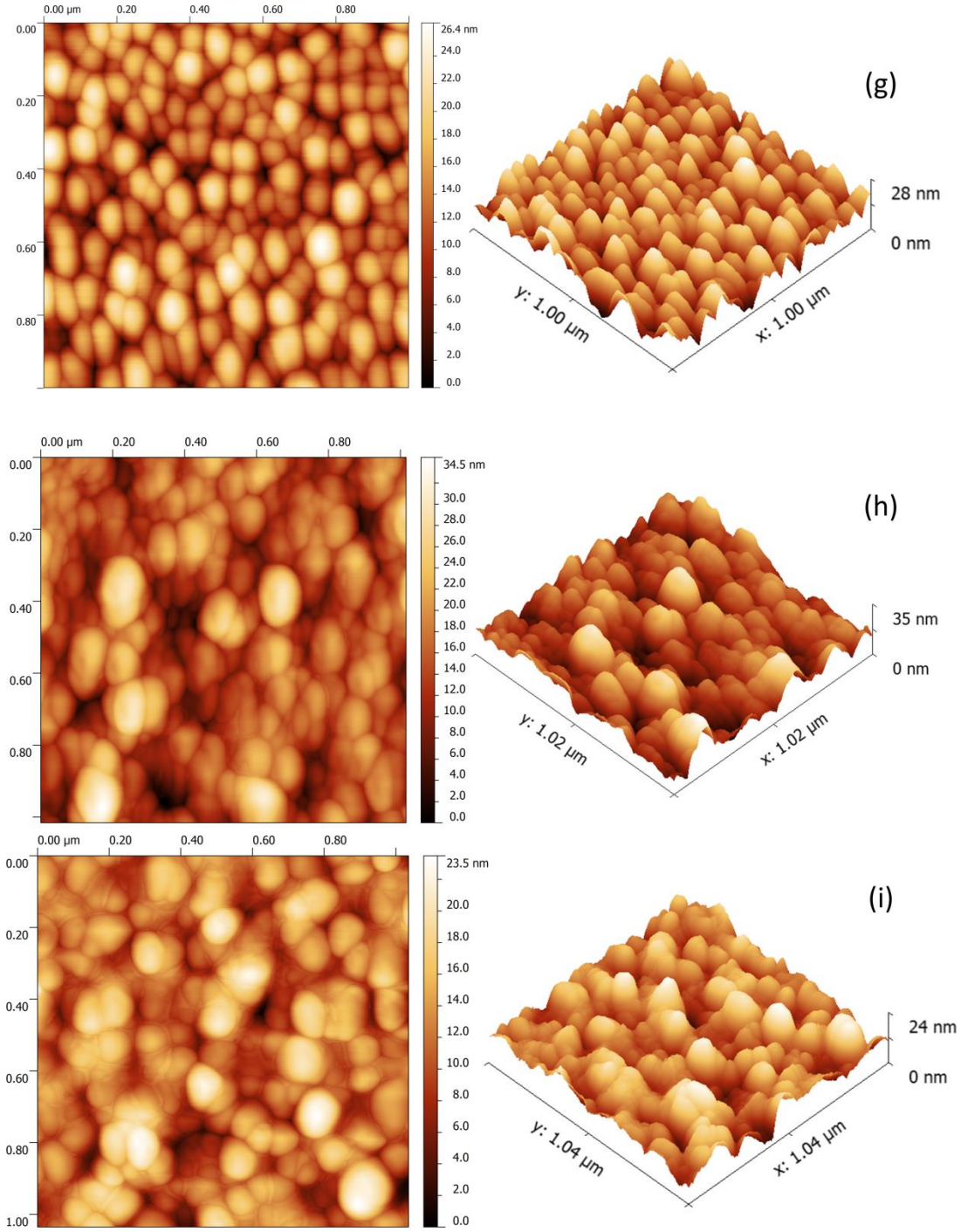

Figure 4-7 Top view (left) and corresponding 3-D view (right) 1µm by 1µm AFM images of (a) a-SiC and (b) 18 at. % Cu, (c) 20 at. % Cu, (d) 21 at. % Cu, (e) 25 at. % Cu, (f) 28 at. % Cu, (g) 38 at. % Cu, (h) 43 at. % Cu, and (i) 53 at. % Cu a-SiC/Cu films.

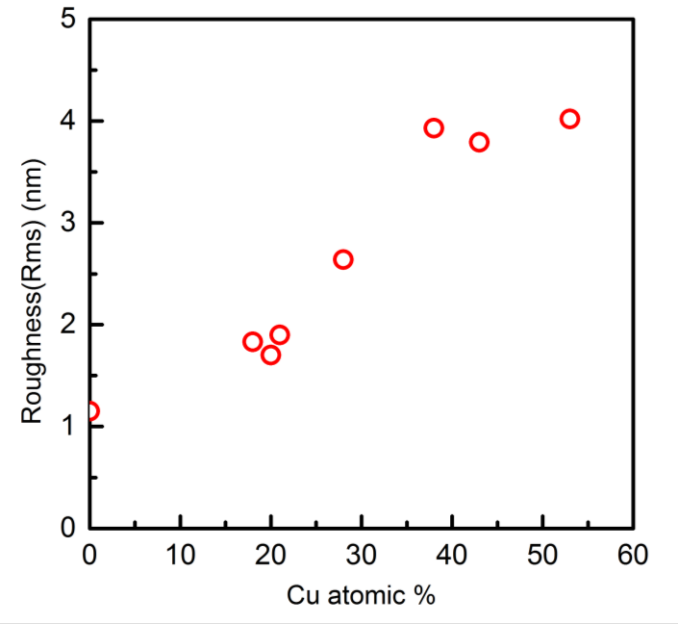

Figure 4-8 Rms surface roughness of a-SiC and a-SiC/Cu films as a function of Cu atomic percentage.

4.3 Electrical Properties

4.3.1 Resistivity of a-SiC Film

As mentioned in Section 3.3, the HL5500PC system is capable of resistivity measurement by Van der Pauw method and carrier concentration and carrier mobility measurement by Hall Effect. But the resistivity of undoped a-SiC film was too high to be reliably measured by this system, and had to be measured by transfer length method [177]. The results of these measurements are shown in Figure 4-9. The I-V curves were measured from the SiC strip structures discussed in chapter 3. From the slope of the I-V curves, the resistance of the test structure can be calculated, and the calculated resistance values were plotted in Figure 4-9 (b) as a function of the strip length. Clearly the calculated resistance values show a good linear correlation to the strip length. From the linear fit, 1μm long, 100μm wide, 0.25μm thick a-SiC film has an electrical resistance of $3.05 \times 10^{10}\Omega$, therefore the resistivity of as-deposited a-SiC film is $7.66 \times 10^{7}\Omega \cdot \mathrm{cm}$. In comparison, the reported resistivity of a-SiC films is in the range of 10^{5}~10^{9} Ω·cm [148, 149]. Therefore the resistivity of our a-SiC films is reasonably high, and there is not noticeable unintentional doping in the deposition process.

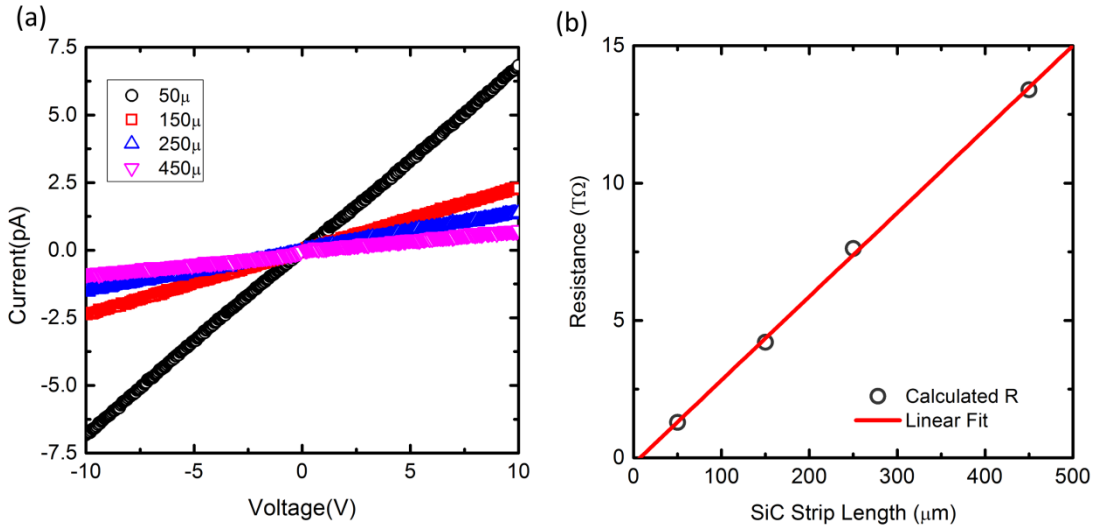

Figure 4-9 (a) I-V curves of a-SiC strips of increasing length and (b) calculated resistance as a function of a-SiC strip length, with linear fit to calculate a-SiC film resistivity.

4.3.2 Resistivity of a-SiC/Cu Films

The transfer length method of resistivity measurement has also been applied to determine the resistivity of several a-SiC/Cu films, and the results were in good agreement with those from Van der Pauw method using HL5500PC system. This can be expected as the resistivity of a-SiC/Cu films are several orders lower than a-SiC. Nevertheless, the good agreement validates the Van der Pauw method for a-SiC/Cu films, which is much more convenient as fabrication of test structures is not required. The resistivity of a-SiC, a-SiC/Cu and sputtered Cu films are shown in Figure 4-10. Here the resistivity of a-SiC is from transfer length method, and all other data is from Van der Pauw method. It can be seen that the resistivity of a-SiC/Cu film with lowest Cu percentage is still 4 orders of magnitudes lower than that of as-deposited a-SiC. The reduction of resistivity is undesirable for the application in resistive memories, as it may reduce the OFF-state resistance of the device. As discussed in Section 4-1, the combination of the lowest stable Cu sputtering power and the highest sustainable SiC sputtering power has been adopted in deposition of the a-SiC/Cu films, therefore there is practical limit in further lowering the Cu percentage. In future work, it may be worthwhile to explore altering sputtering conditions such as chamber pressure [178] to increase the resistivity of obtained films.

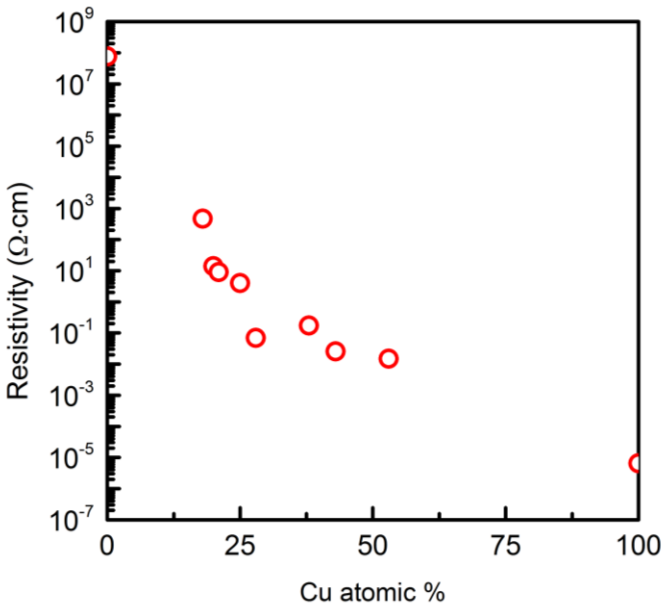

Figure 4-10 Resistivity of a-SiC, a-SiC/Cu and sputtered Cu films as a function of Cu atomic percentage.

Electrical conduction of disordered metal-insulator composite has been studied in many cases, although some phenomena still remain incompletely understood. Conductivity of such systems is generally expected to follow a percolation mechanism [179]:

$$\sigma \approx \sigma_0 (1 - \frac{1-x}{1-x_c})^t \qquad (4\text{-}2)$$

Here σ is the conductivity of the composite, σ_0 is the conductivity of the high conductivity phase (metal), x is the volume fraction of the high conductivity phase, and x_c is the critical volume fraction for the high conductivity phase. From percolation theory, x_c is expected to be 0.16 and t approximately 2 [179]. However in previous studies a much wider range of x_c and t have been reported. x_c can be in the range of 0.05 to 0.6 , and t in the range of 1.5 to 11 [179]. In our case, a good fitting was obtained with $x_c = 0.1$ and t=5, as shown in Figure 4-11. It was suggested that a t value larger than 2 indicates tunnelling conduction. I.e., the electric conduction is due to both percolation and tunnelling between metallic particles [180]. On the other hand, it has been proposed that the lower than theoretical x_c may be related to the geometry of the metal and insulator particles. The theoretical x_c is obtained under the assumption that both metal and insulator particles are spheres of the same radius. If the radius of metal particles are smaller than insulator particles, x_c may be lower than 0.16 and can be as low as 0.03 [181]. This explanation is in agreement with the results shown in previous section: From the XRD results, the Cu particles are found to be smaller than 3nm; and from the AFM

images, the overall grain size is in the range of 20~100nm. Therefore it is likely that Cu particle size is significantly smaller than that of a-SiC.

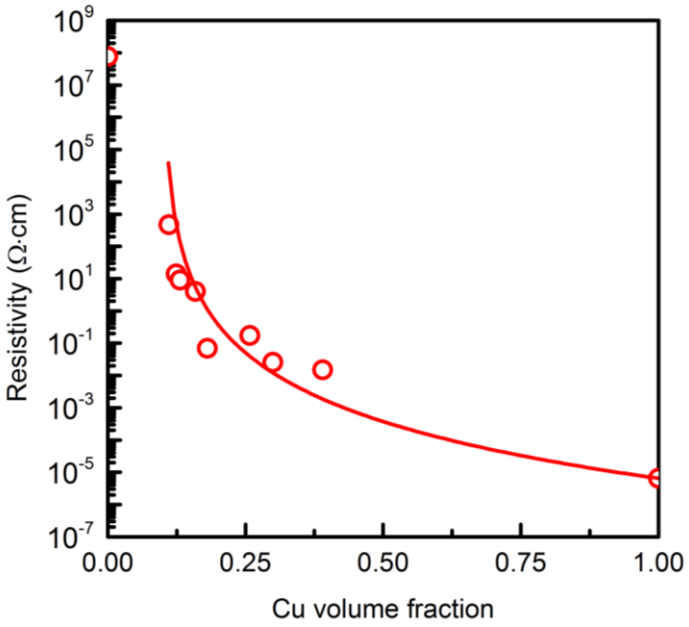

Figure 4-11 Resistivity of a-SiC, a-SiC/Cu and sputtered Cu films as a function of Cu volume fraction, fitted to the percolation equation (eq. 4-2). The Cu volume fraction was estimated using density of 3C-SiC (3.17g/cm^3) and bulk Cu (8.96 g/cm^3)

4.3.3 Carrier Concentration and Carrier Mobility

Carrier concentration and carrier mobility of the a-SiC and a-SiC/Cu films have also been measured by Hall Effect using the HL5500PC system, and the results are shown in Figure 4-12. The addition of Cu increased carrier concentration by up to 8 orders of magnitude, while the carrier mobility remained in a relatively limited range. The carrier concentration of as-deposited a-SiC is approximately 2×10^{14}/cm^3, which is slightly lower than the reported value of 10^{15} to 10^{16}/cm^3 of chemical vapour deposition SiC thin films [182]. The low carrier concentration and the high resistivity of as-deposited a-SiC shows unintentional doping in the deposition process was relatively under control. Carrier mobility of all the a-SiC and a-SiC/Cu films are significantly lower than that of crystalline semiconductors (~100s cm^{2}V^{-1}s^{-1}) [183, 184] and is more comparable to amorphous semiconductors and metal/insulator composites (<1 cm^{2}V^{-1}s^{-1}) [185, 186]. This again indicates the disordered structure of a-SiC and a-SiC/Cu films. The low carrier mobility is also advantageous for maintaining resistivity of the a-SiC/Cu films.

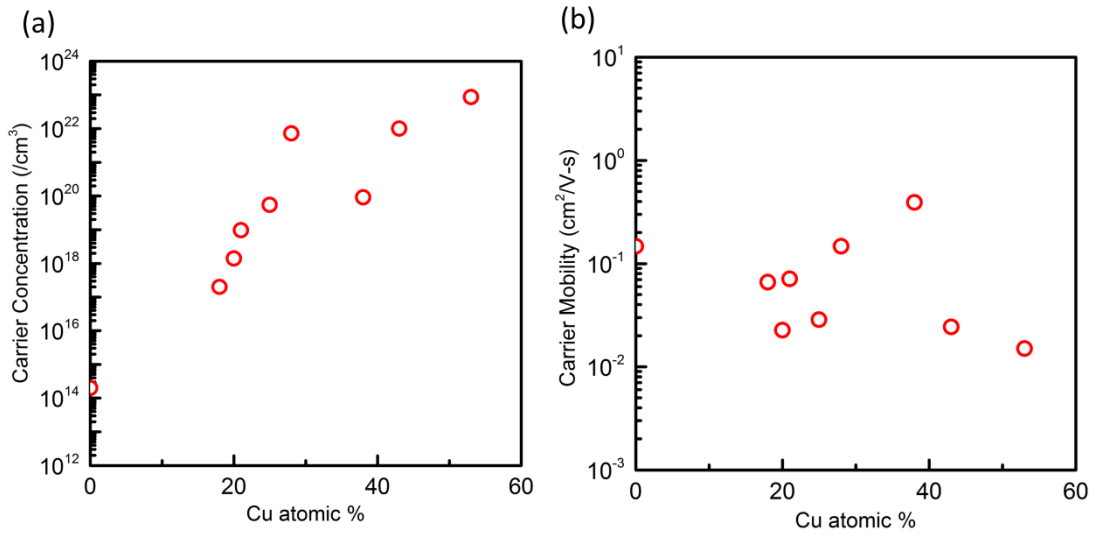

Figure 4-12 (a) carrier concentration and (b) carrier mobility of a-SiC and a-SiC/Cu films, measured by Hall Effect.

4.3.4 Temperature Dependency of Resistivity

Temperature dependency of resistivity of the a-SiC/Cu films has also been evaluated, as shown in Figure 4-13. Due to practical limitations, the Van der Pauw method could not be adopted in this measurement. Instead two probe needles were placed directly on the films, and the resistance was measured by applying a 3V voltage between the two probes. (The resistivity of undoped a-SiC film was too high so results are limited to a smaller range of temperature.) Therefore in this measurement the contact resistance between the probe and the a-SiC/Cu films were not eliminated, however these results can still provide certain insights into the conduction mechanism of the a-SiC/Cu films.

From Figure 4-13, it can be observed that only the one film with 53 at. % Cu shows positive temperature coefficient of resistivity, i.e. metallic conduction. This is in contradiction to the percolation fitting discussed earlier. From the fitting, the critical volume fraction is 0.10, which corresponds to ~16 at. % Cu. For films with higher Cu percentage, percolation theory predicts metallic conduction, which isn't observed in Figure 4-13. This discrepancy is possibly due to that in addition to standard percolation conduction, tunnelling conduction is involved in the a-SiC/Cu films.

Temperature dependence of resistivity of many metal/insulator composite films has been found to follow the Arrhenius law [187]:

$$\rho = \rho_0 \cdot exp\left[\frac{E_A}{k_B \cdot T}\right] \tag{4-3}$$

Here ρ is resistivity, ρ_0 is a temperature independent, k_B is the Boltzmann constant, T is temperature and E_A is the activation energy of carriers. As Figure 4-14 shows, such relationship has also been observed in our a-SiC/Cu films. From the slope of linear fits, the activation energy for the films with 18% Cu, 21% Cu and 37% Cu is 56.6meV, 39.7meV and 23meV, respectively.

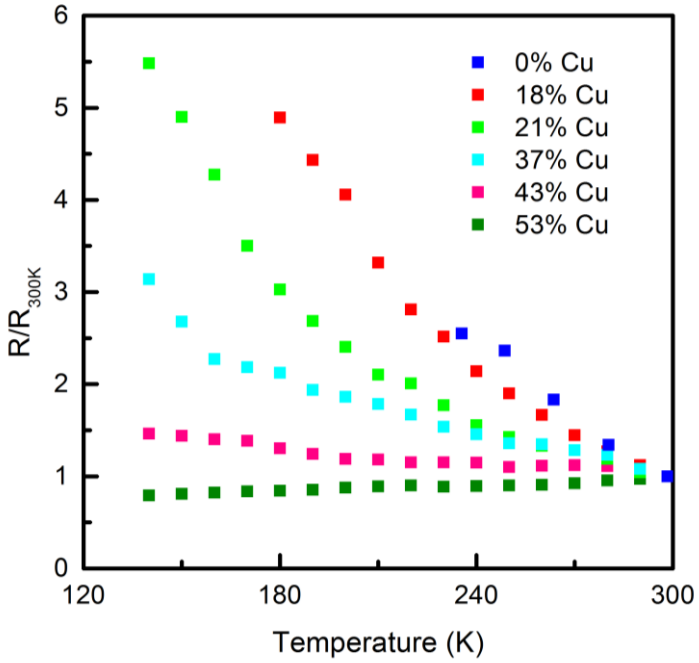

Figure 4-13 Unified resistance (R/R_{300K}) of a-SiC/Cu films as a function of temperature.

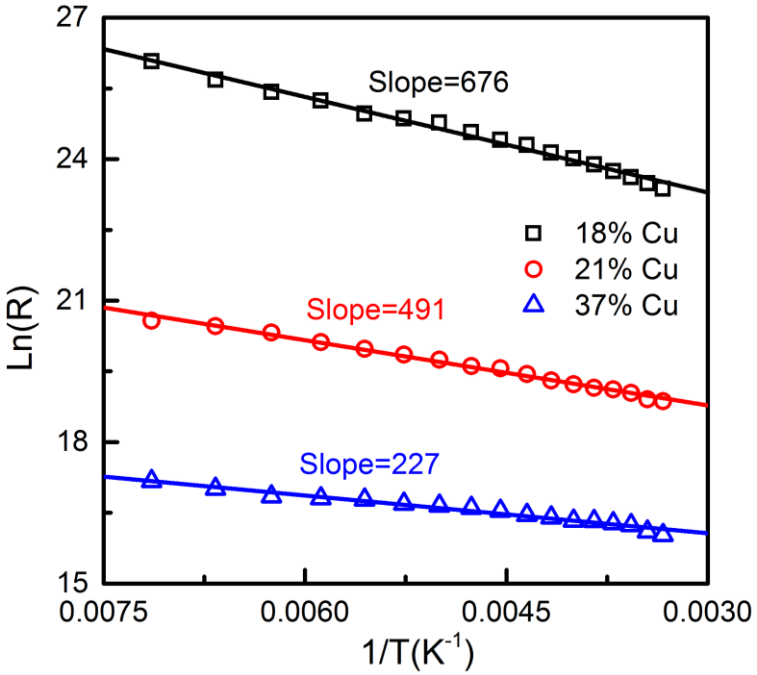

Figure 4-14 ln(R) vs T^{-1} plot of a-SiC/Cu films. The linear fittings indicate the conductivity obeys the Arrhenius law [187].

4.3.5 Dielectric Properties

At last, after the fabrication of resistive memories based on a-SiC and a-SiC/Cu, the capacitance of these devices was also measured, as shown in Figure 4-15 (a)-(c). With known device area and dielectric thickness, the dielectric constant can be obtained from the slope of linear fittings. The dielectric constant of the a-SiC film is found to be approximately 6.5, which leads to a refractive index of 2.55. Both are in agreement with previous reported values [18]. The dielectric constant of the two a-SiC/Cu films appears to be decreasing as the Cu percentage increases. This is also possibly related to the increase of grain size in the a-SiC/Cu films. With increasing grain size, the films may be less densely packed, and films with higher porosity generally have lower dielectric constant [188].

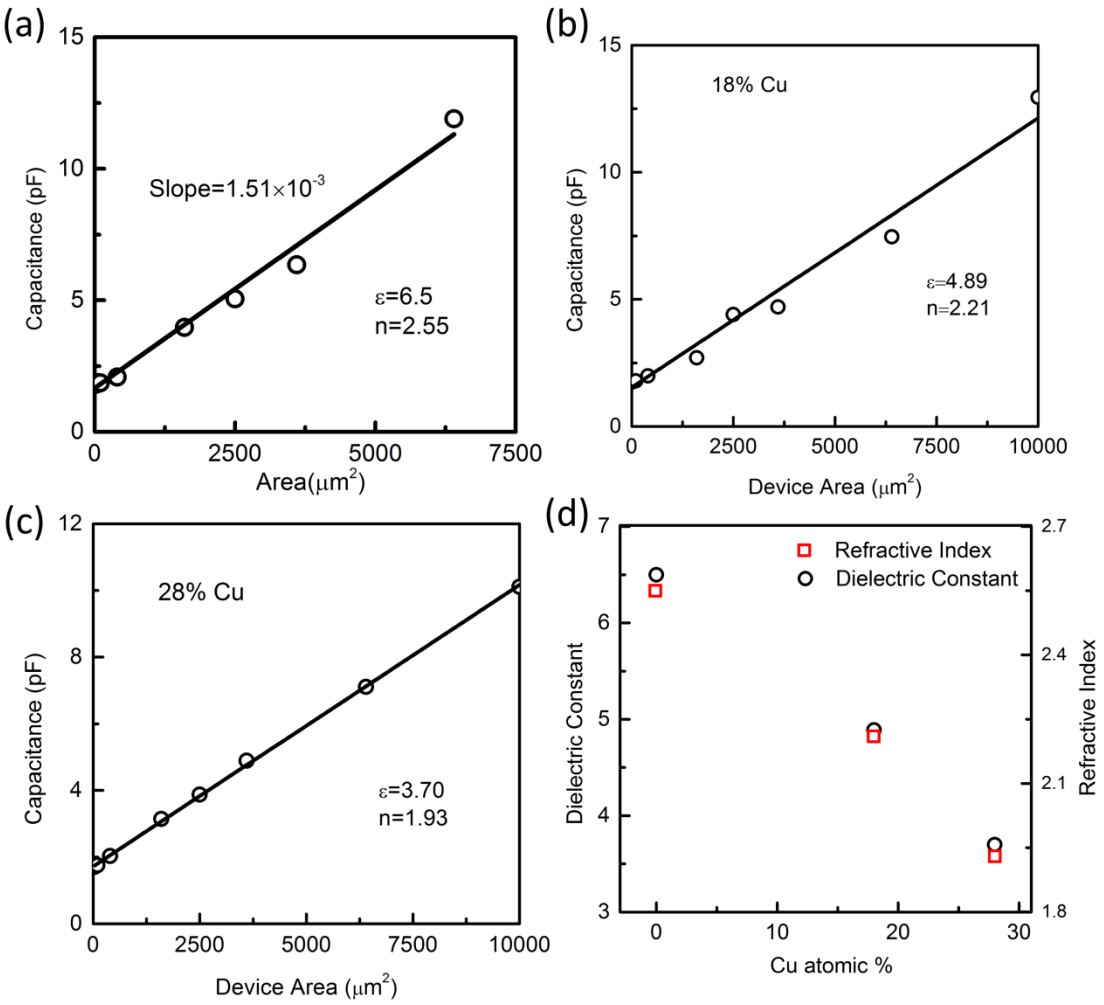

Figure 4-15 capacitance as a function of device area, from Cu/a-SiC/Au devices with (a) a-SiC, (b) a-SiC/Cu with 18 at. % Cu and (c) a-SiC/Cu with 28 at. % Cu. The refractive index and dielectric constant obtained from linear fittings are plotted in (d).

4.4 Summary

In summary, material properties, namely chemical composition, structural properties and electrical conduction properties of the sputtering deposited a-SiC and a-SiC/Cu are presented in this chapter. The deposited SiC films are of amorphous structure, with Si to C ratio close to 1, and have very high resistivity of $7.66 \times 10^7 \Omega \cdot \text{cm}$.. All these properties are suitable for the intended application as solid electrolyte material for resistive memories. As for the a-SiC/Cu films, the added Cu remains metallic and the Cu particle size is below 3nm. Films with higher Cu percentage also exhibit larger grain size, which may lead to more porous films and lower dielectric constant. The added Cu also greatly reduced the resistivity of a-SiC/Cu films, which may be undesirable for the application in resistive memory, and it may be worthwhile to explore sputtering conditions to increase the resistivity of obtained films in future studies. The percolation fitting of resistivity vs Cu volume fraction and temperature dependence of resistivity indicate coexistence of percolation and tunnelling conduction in the a-SiC/Cu films, which may be of interest for future studies.

Chapter 5. Resistive Memories Based on a-SiC

5.1 Fabricated Devices

The chip containing Cu/a-SiC/Au RM devices discussed in this chapter is shown in Figure 5-1. This chip has been cut into three pieces for various tests, due to the practical limitations of the test equipment. According to the lithography mask design shown in Section 3.1, there are ideally 120 devices of each dimension on this chip. The actual yield was dependent on the device dimensions. The smaller devices, e.g. 1μm diameter and 2μm by 2μm devices had a much higher yield rate, with approximately 90% being successfully fabricated. Only the ones near the edge of the chip are visibly incomplete. The larger devices, especially the 100μm*100μm and 80μm*80μm devices, had a much lower yield of approximately 50%. The reason for such difference is discussed later.

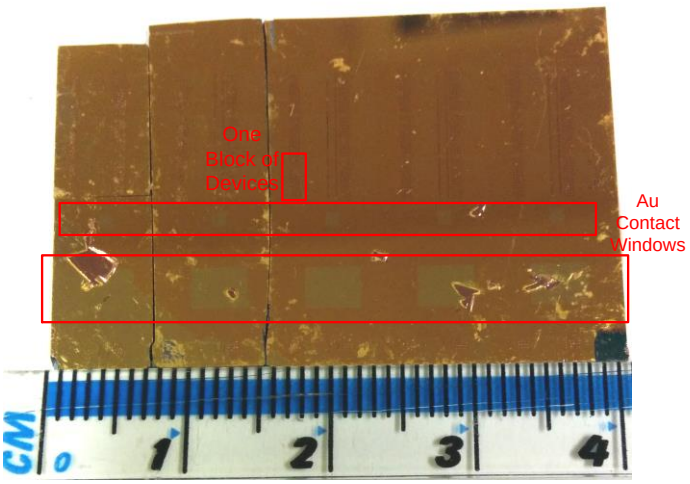

Figure 5-1 Photo of the chip with Cu/a-SiC/Au RM devices, the lighter colered rectangles are Au contact windows, and the darker colored dots are the Cu contacts.

The top view optical microscope image of obtained devices is shown in Figure 5-2. Following the lithography masks, the area of Cu contacts is constantly 100μm * 100μm, as shown in Figure 5-2. From left to right, the 5 columns of devices have active area dimensions of 6, 5, 4, 2, 1 μm respectively, and the dimensions are clearly marked beside each column. The 1μm diameter active areas are still visible under this microscope, which can help ascertain the device under test was successfully fabricated.

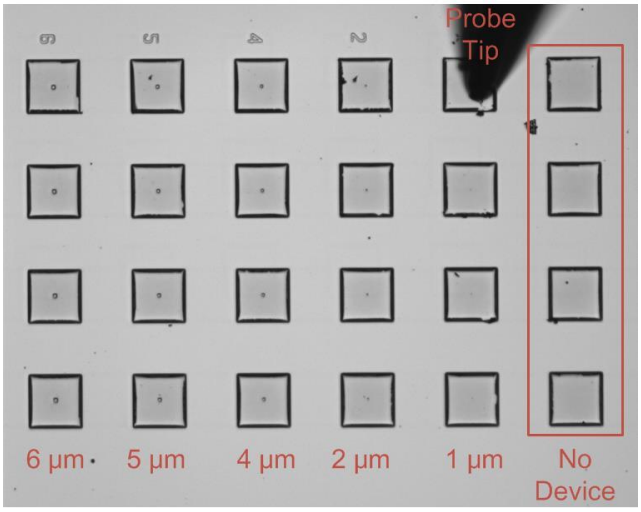

Figure 5-2 Optical microscope image of obtained devices and probe tip placed on Cu contact.

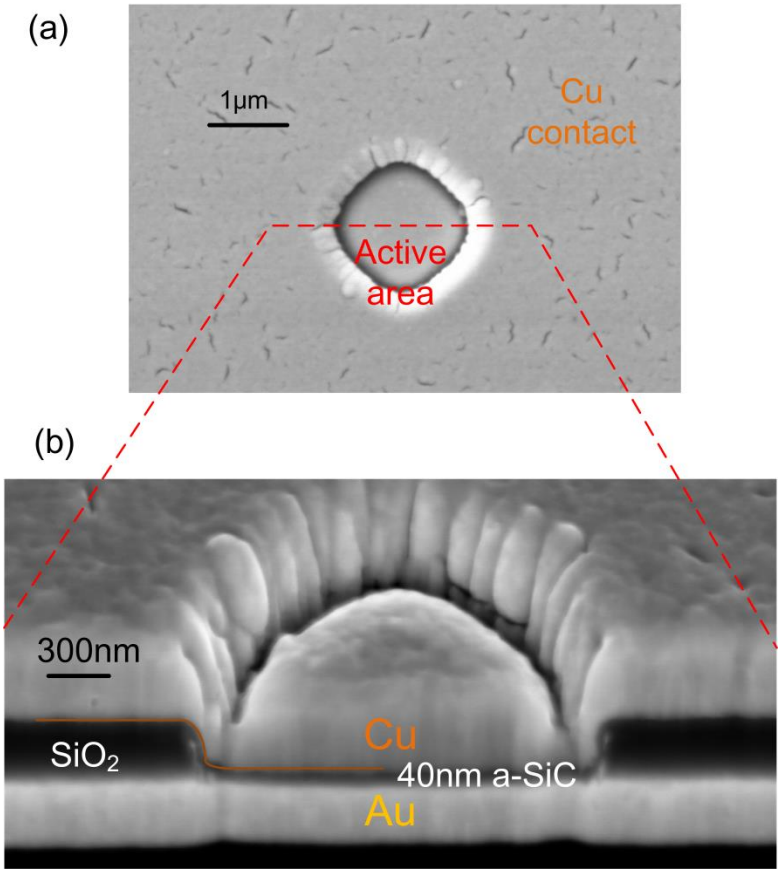

Figure 5-3 (a) Top-view and (b) cross-section SEM image of a 2µm diameter Cu/a-SiC/Au device.

To examine the cross-section of obtained devices, FIB-milling was performed to expose the cross-section at precisely the active area, and the resault is shown in Figure 5-3. The sample was tilted 52 degrees, therefore the image shows both the cross-section view and

the top Cu layer. The dark a-SiC layer is clearly visible between two bright metal layers. According to SEM measurements, the thickness of a-SiC layer is approximately 40nm, Au layer 290nm, SiO_2 layer 250nm and Cu layer 350nm. These measurements also agree with the estimations based on deposition rates. The image also shows clear continuous coverage of Cu layer on the SiO_2 step (outlined by a thin brown line). This ensures good electrical conduction between the device active area and the surrounding Cu layer used as connection pads.

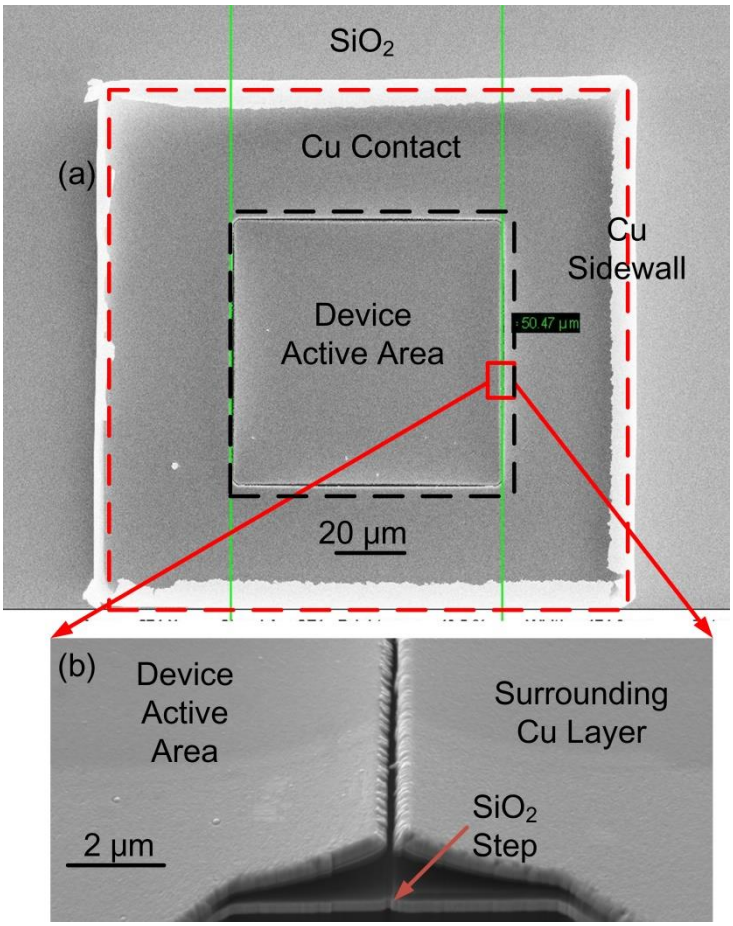

Figure 5-4 (a) top view SEM image of a 50µm*50µm device. (b) tilted view of the area around SiO_2 step, showing clear buckling and discontinuation of the Cu layer. The opening was created by FIB milling.

Among larger devices (over 20×20 μm^2), buckling of the Cu layer and resulting discontinuation of the Cu layer around the SiO_2 steps was observed, as shown in Figure 5-4. Because of the discontinuation, test on the larger devices cannot use the surrounding Cu layer for electrical connection, and a probe has to be placed directly on top of device active area. This method is more likely to cause physical damage to the device under test and may potentially influence the device switching behaviour. The exact cause of such

phenomena is still unknown, and further optimization of deposition conditions may be needed to reduce this effect[189].

5.2 Bipolar Switching Behaviour

5.2.1 Electroforming Cycle

As the starting state of pristine Cu/a-SiC/Au RMs is always HRS, typically a first electroforming process is required to obtain the initial LRS, as shown in Figure 5-5. The forming voltage for the pristine device was approximately 3.8V, which was noticeably higher than V_{SET} in the typical switching cycle. Moreover, HRS current of pristine device was significantly increased after electroforming process. Similar results have been frequently observed in many RMs [136, 138, 190], and were generally attributable to the forming process: In the electroforming cycle, the applied voltage has to cause soft-breakdown of the whole solid electrolyte layer to induce the formation of the first conductive filament [75]. In the following RESET process, the conductive filament is only partially broken at the weak point instead of completely eliminated, and the remnant of filament serves as easy path for filament formation in following switching cycles [9, 62]. Therefore the typical switching cycles have lower V_{SET} and R_{OFF}. The switching mechanisms are discussed further in section 5.6.

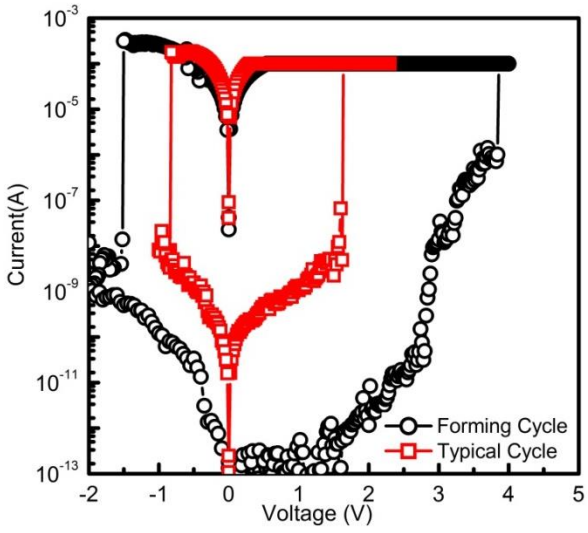

Figure 5-5 I-V curves of an electroforming cycle and typical switching cycle from a 1μm diameter Cu/a-SiC/Au device.

5.2.2 Typical Switching Cycle

The previous studies on Cu and a-SiC based RMs reported bipolar switching behaviour, where device SET to LRS with positive bias on Cu, and RESET to HRS with negative bias on Cu. Such behaviour has also been observed in our Cu/a-SiC/Au devices, and the typical bipolar switching I-V curves are shown in Figure 5-6. As discussed in Section 3.2.2, sweeping voltage was applied on the Cu contact, while the Au layer was grounded. The sweeping voltage applied was 0V → 2.4V → 0V→ -1V → 0V. The device was originally in HRS (low current), and the current through device increased sharply at approximately 1.7V to the compliance current 10^{-4}A. The device was thus switched from HRS to LRS, and V_{SET} was approximately 1.7V.

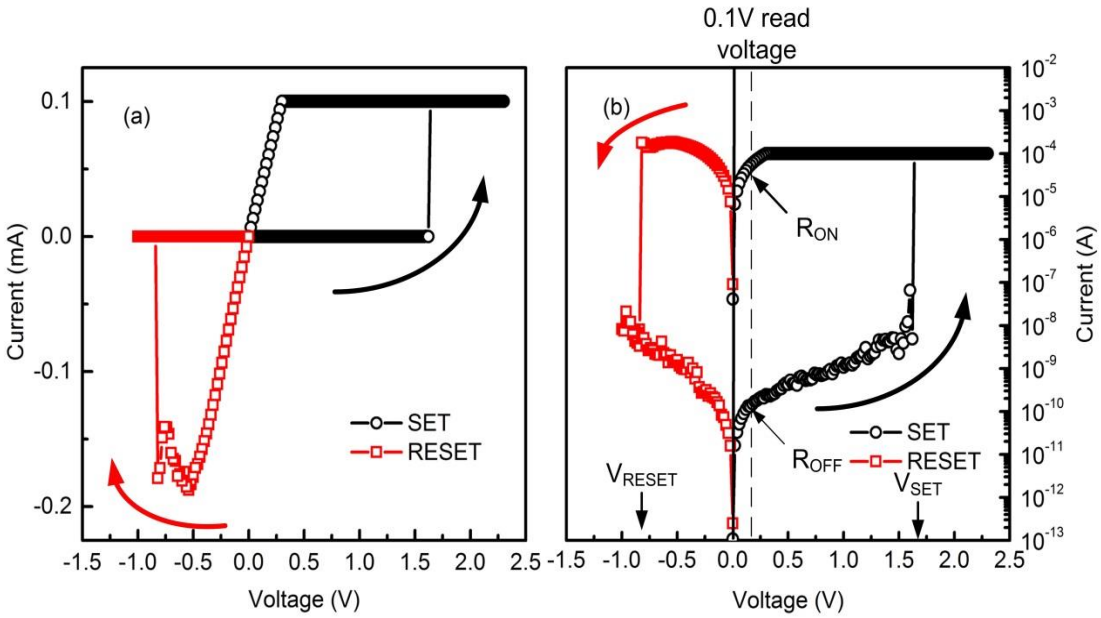

Figure 5-6 Typical bipolar switching I-V curves of a 1μm diameter Cu/a-SiC/Au device, in (a) linear plot and (b) logarithmic scale plot, with arrows indicating switching directions. The switching parameters, namely R_{ON}, R_{OFF}, V_{SET} and V_{RESET} are also marked.

From Figure 5-6 (a), it can be observed that LRS had a linear I-V behavior, and LRS was maintained in the following voltage sweep until applied voltage reached approximately -0.8V, when the current dropped sharply and the device was switched back from LRS to HRS. The V_{RESET} was therefore approximately -0.8V. The HRS resistance R_{OFF} and LRS resistance R_{ON} can be calculated from I_{OFF} and I_{ON} at 0.1V read voltage, and the values are approximately $10^{9}\Omega$ and $10^{3}\Omega$, respectively. Accordingly the ON/OFF ratio was approximately 10^{6}. Due to such high ON/OFF ratio, in a linear plot like Figure 5-6 (a), the details of HRS current cannot be observed, therefore the switching I-V data are normally

presented in a logarithmic scale plot. From Figure 5-6 (b) it can also be observed that the HRS current before and after SET/RESET cycles were at very similar levels, which is necessary for the switching repeatability over multiple switching cycles.

It is worth noting that, although R_{ON} (10^3 Ω) of our Cu/a-SiC/Au devices is in the similar order of magnitude as in comparison to R_{ON} in these reported Cu/SiC/Pt devices [18], R_{OFF} of our devices (approximately 10^9 Ω) is several orders of magnitudes greater than the reported R_{OFF} (approximately 10^5 Ω) in Ref.[18], ultimately leading to significantly improved ON/OFF switching ratios. The high R_{OFF} achieved in our devices is most likely attributable to two factors: Firstly the as-deposited a-SiC layer exhibited very high resistivity in the order of 10^8 Ω•cm; secondly analysis of HRS current shows possible Schottky contacts formed at the interface between metal electrodes and a-SiC solid electrolyte, which are discussed in detail later in section 5.5.

5.2.3 Distribution of Switching Parameters

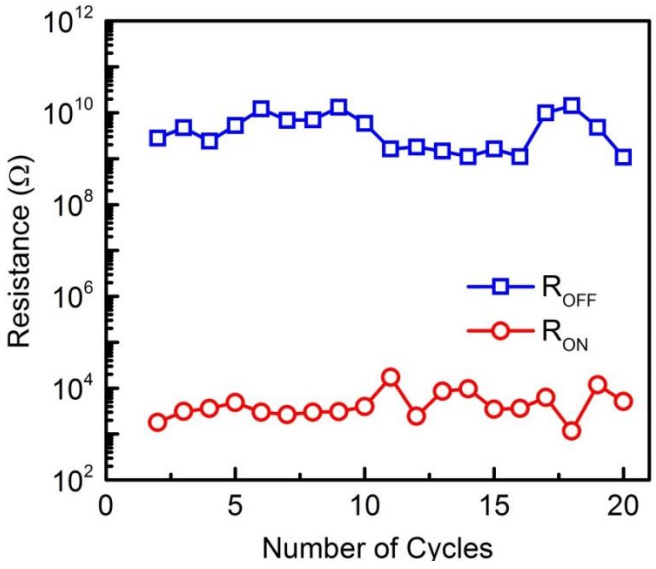

Figure 5-7 R_{ON} and R_{OFF} values over 20 cycles from a 1μm diameter Cu/a-SiC/Au device.

The R_{ON} and R_{OFF} values of a 1μm diameter Cu/a-SiC/Au device in 20 switching cycles are extracted and plotted in Figure 5-7. R_{ON} over 20 cycles are in the range of 10^3~10^4Ω, and R_{OFF} has a slightly wider dispersion, in the range of 5×10^{10}~10^9Ω. The typical ON/OFF ratio is in the order of approximately 10^6, and the minimum ratio is still over10^5, which is a significant improvement over the previously reported Cu/a-SiC/Pt devices. In 20 cycles, there was no noticeable decrease of R_{OFF}, which can often be observed in repeated cycle operation of RMs. In addition to the relatively small dispersion of R_{ON} and R_{OFF}, these

preliminary results show good repeatability of Cu/a-SiC/Au RMs. Further tests, especially switching driven by pulse voltage instead of sweeping voltage, may help fully evaluate the switching repeatability and cycle endurance.

5.3 Non-polar Switching Behaviour

5.3.1 Observation of Four Switching Modes

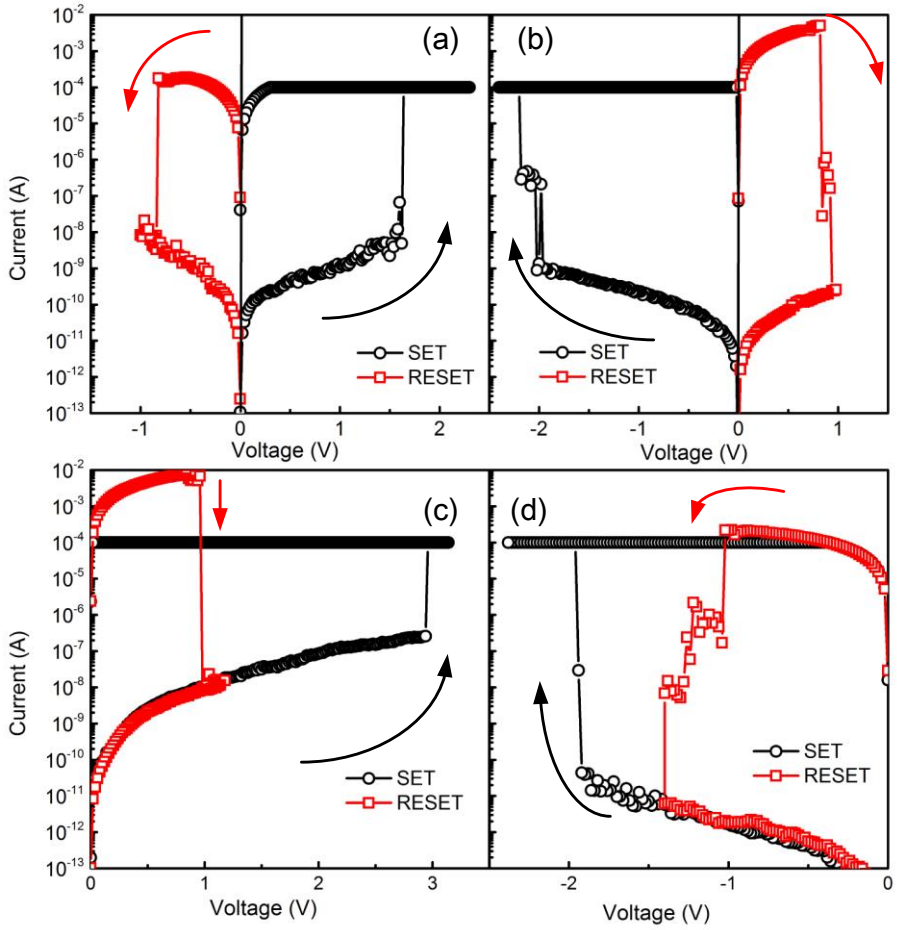

Figure 5-8 Typical switching cycles of all four switching modes: (a) +bipolar, (b), -bipolar, (c) +unipolar and (d) –unipolar, with arrows indicating switching directions.

In addition to positive bipolar switching, in which SET is triggered by positive voltage on Cu electrode and RESET negative voltage, all three other possible switching polarity have been observed in the Cu/a-SiC/Au devices, as shown in Figure 5-8. To avoid any possible influence from switching history, each of the four switching mode i.e. +bipolar, -bipolar, +unipolar, -unipolar was conducted using a pristine Cu/a-SiC/Au device with identical device structures i.e. each device has only been tested using its respective switching mode, including the first electroforming cycle. From I-V curves shown in Figure 5-8, it is

observed that typical V_{SET} and V_{RESET} are around or below 2V. It can also be observed that R_{ON} values in –bipolar mode and +unipolar mode appear to be noticeably lower than other two modes. In –bipolar and +unipolar mode positive bias on Cu electrode triggers RESET, while in the other two modes negative bias triggers RESET. Therefore the differences of RON are most likely related to the different switching mechanisms, and are discussed later in section 5.6. It is also worth noting that, high switching ratios in the range of 10^6~10^8 were obtained for all four modes.

5.3.2 Distribution of Switching Parameters

The distribution of R_{ON} and R_{OFF} over 20 cycles in four switching modes are shown in Figure 5-9. R_{ON} in +bipolar mode and –unipolar mode lies between 10^4 ~ 10^3 Ω, and R_{ON} in –bipolar and +unipolar mode is slightly lower, in the range of 10^3 ~ 10^2 Ω. For all switching modes, the variation of R_{ON} in each mode is around one order of magnitude, which is reasonably limited among Cu-based RMs [17, 80, 111]. From the figure, the minimum of R_{OFF} is >10^8Ω, and the minimum of OFF/ON ratio is approximately 10^5, while typical ratio is around 10^6~10^8. Again, these ratios are a significant improvement compared to the previous RMs based on Cu and a-SiC, which exhibited a typical ON/OFF ratio of approximately 10^3. .

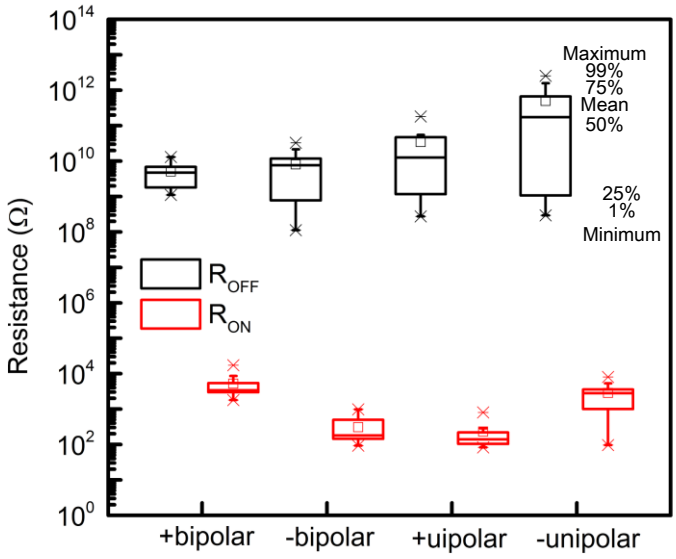

Figure 5-9 Distribution of R_{ON} and R_{OFF} over 20 cycles in four switching modes.

The distribution of V_{SET} and V_{RESET} over 20 cycles in four switching modes is shown in

Figure 5-10. The positive SET voltage centres around 2V and 2.5V for bipolar and unipolar mode, respectively, and the negative SET voltage -2.5V and -2V. The reset voltage is

around -1V for +bipolar and –unipolar modes, and 1V for +unipolar and –bipolar modes. The amplitudes of V_{SET} and V_{RESET} are all comparable to previous studies on Cu RMs, and well below the typical 5V~12V required for Flash memory. This suggests Cu/a-SiC/Au RMs can potentially serve as relatively low voltage and low power non-volatile memories. It can also be observed that V_{SET} has larger variation in –bipolar and +unipolar modes, in which positive voltage triggers RESET process. This is possibly related to the positive RESET process, and is discussed further in section 5.6.

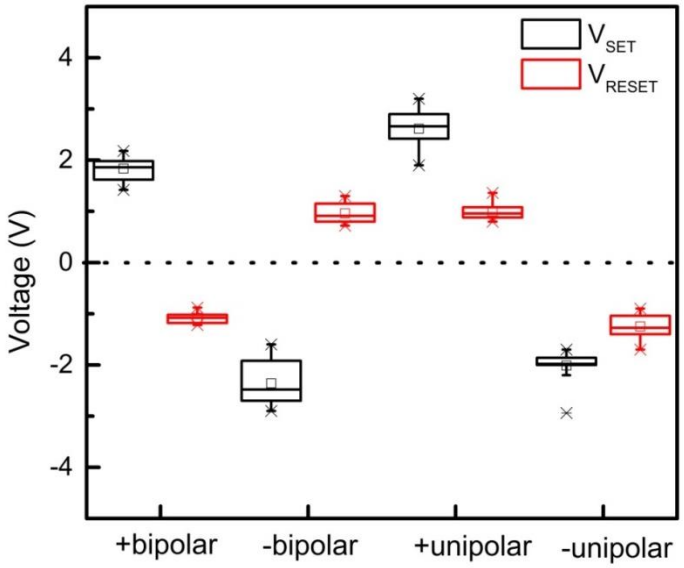

Figure 5-10 Distribution of V_{SET} and V_{RESET} over 20 cycles in four switching modes.

5.3.3 Nonpolar Switching in Single Device

The switching behaviour of four switching modes shown in Figure 5-8 were observed from four identical devices. So that each individual device only went through one switching mode and there was no interference between different modes. These results established that Cu/a-SiC/Au RMs could exhibit all four switching modes, and further tests were carried out to ascertain whether all four modes could co-exist in one single device. The results of such test are shown in Figure 5-11. The four switching cycles were performed in a-b-c-d order, one immediately after another. Clearly the four switching mode can co-exist in a single device, however there is quite noticeable variation in the R_{ON} and R_{OFF} values. And the transition between LRS and HRS appears to be more noisy. This indicates that operating one device in different switching modes may have adverse effect on switching performance, likely because the alteration to the a-SiC solid electrolyte layer after switching in one mode may affect switching in another mode.

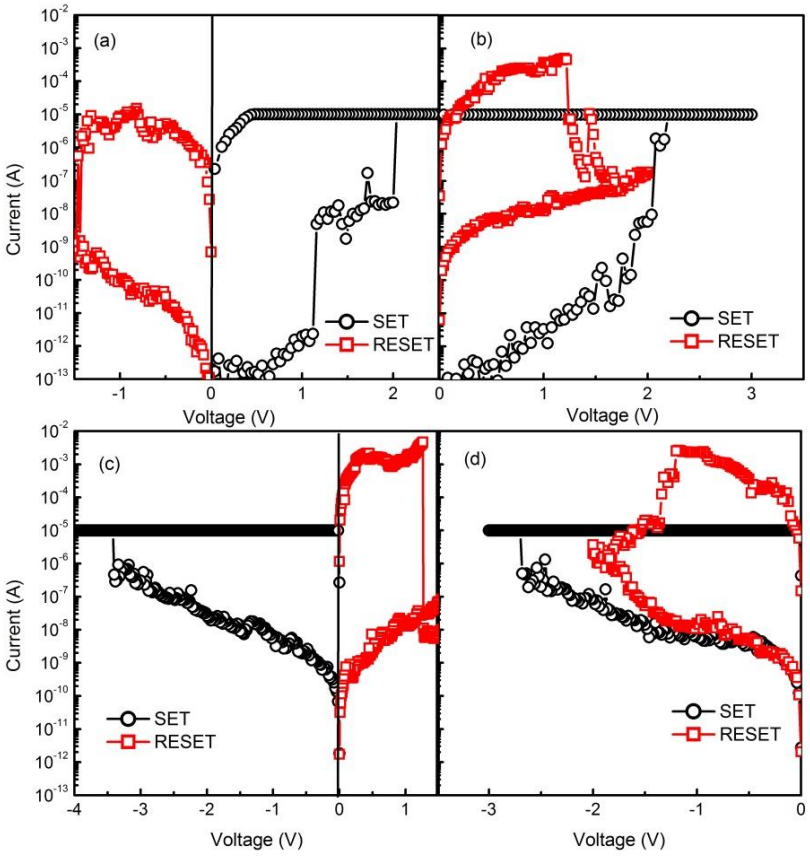

Figure 5-11 Four switching modes observed in a single 1μm diameter Cu/a-SiC/Au RM. a) +bipolar, (b), -bipolar, (c) +unipolar and (d) -unipolar switching.

5.4 LRS Conduction Analysis and LRS Resistance

5.4.1 Ohmic I-V Behaviour

As discussed in Section 2.3, due to the great difficulty to observe the conduction paths in real time, detailed studies of I-V characteristics have been widely exploited to decipher the conduction and switching mechanisms of RMs in general [65, 76]. I-V characteristics of the Cu/a-SiC/Au RMs ON-state for all four switching modes are shown in Figure 5-12 in a Ln(I)-Ln(V) scale. The slopes of the linear fittings are very close to unity, i.e.

$$Ln(I) \propto 0.99\sim1.01\,\mathrm{Ln}(V)\,, \therefore I \propto V^{0.99\sim1.01} \qquad (5\text{-}1)$$

which suggests Ohmic conduction in all ON-states [88, 89]. In RMs with metal electrodes, Ohmic conduction is most likely an indication of metallic filaments. Additionally, it can also be seen from Figure 5-12 that ON-state current in +unipolar and –bipolar modes is quite

similar and higher than the other two modes. This is possibly related to the switching mechanisms, and is further discussed in Section 5.6.1.

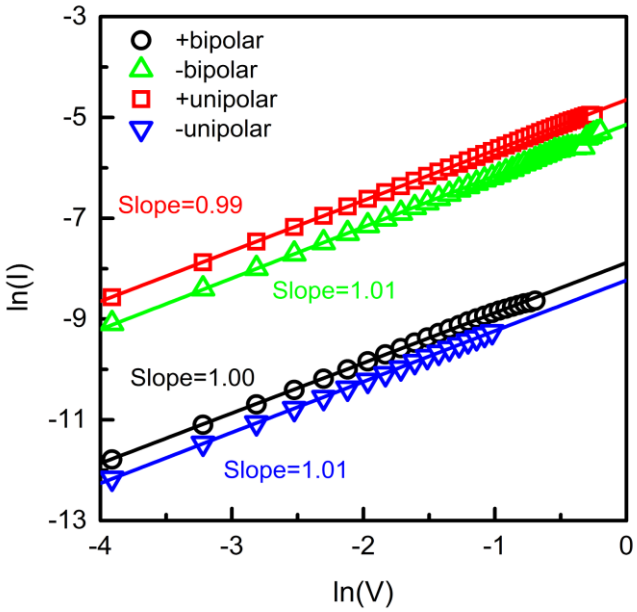

Figure 5-12 LRS I-V data from 4 switching modes (4 1μm diameter devices). in Ln(I)-Ln(V) plots, with respective linear fittings.

5.4.2 Positive Temperature Coefficient of R_{ON}

ON-state resistance over a range of temperature points has been commonly used to extract properties of the conduction filaments [80, 111]. Such testing has also been undertaken in this work, using the set-up discussed in Section 3.3. Figure 5-13 shows R_{ON} as a function of temperature. In agreement with LRS I-V data, metallic conduction behaviour is observed for the LRS resistance for both positive (R_{ON+}) and negative (R_{ON-}) switching modes. Through linear fitting, the temperature coefficient of R_{ON+} and R_{ON-} are extracted to be 2.4×10^{-3} K^{-1} and 2.7×10^{-3} K^{-1}. These values are in agreement with reported values for Cu nanowires (2.5×10^{-3} K^{-1})[191] and Au nanowires (2.3×10^{-3} K^{-1})[192], respectively. These results also discard the possibility of any oxygen vacancy conduction as its temperature coefficient should be at least an order of magnitude smaller than metal filaments [193]. The R_{ON} values ($10^{2}\sim10^{4}\Omega$) also match other metallic filament based RMs [9, 64, 194-196]. Metallic filament is therefore most likely to be the conduction mechanism for LRS of all switching modes.

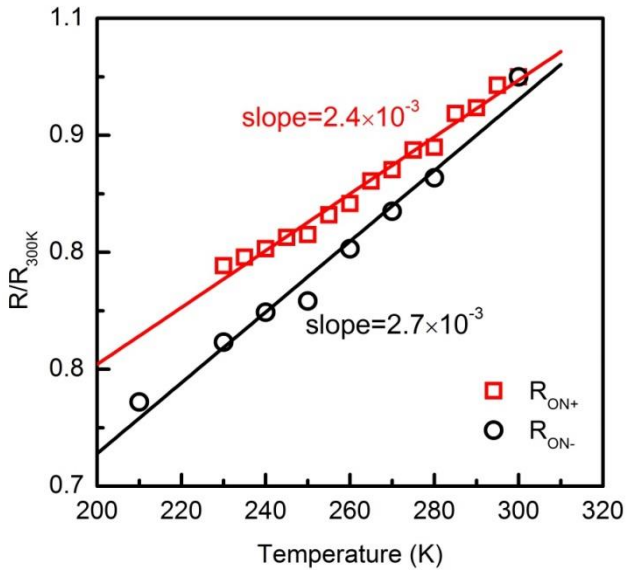

Figure 5-13 Normalized R_{ON} values versus temperature, with the straight lines being their respective linear fittings.

5.4.3 Effect of Device Areas

The dependence of R_{OFF} and R_{ON} on device size also agrees with metallic filament conduction. As shown in Figure 5-14, R_{ON} values are largely independent from device size, while R_{OFF} values slightly decrease as the device size increases. As discussed in Section 2.3.3, dimension of metallic filament in RMs is usually in the range of several nanometers to 10s of nms, which is significantly smaller than the total device active area, and therefore LRS conduction is generally believed to be independent from device size [81, 137, 197, 198]. Moreover, at HRS, without metal filament, the possible conduction mechanisms in a metal-insulator-metal structure all result in current being proportional to the overlay area of the two metal electrodes. With R_{OFF} dependent on device size, and R_{ON} independent from device size, ON/OFF ratio of filament based RMs actually improves as the device scales down. This is one of the main reasons why RMs are generally considered to have great down scalability. . Our devices further prove this unique merit of filament RMs.

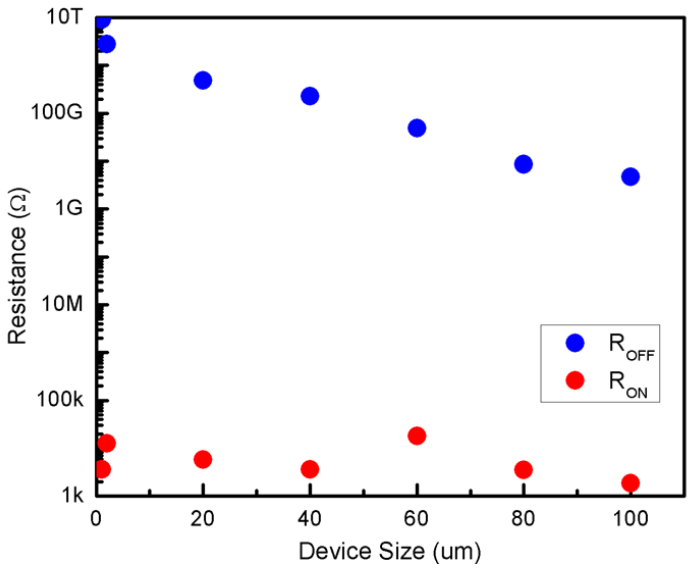

Figure 5-14 Dependence of R_{OFF} and R_{ON} on device active area size.

5.4.4 Effect of Programming Current

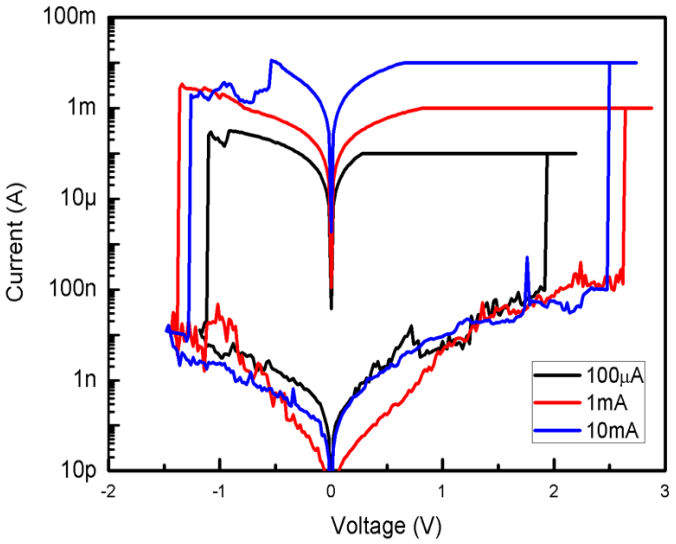

Figure 5-15 I-V curves of three switching cycles with different current compliance during SET process, obtained on a single 80µm by 80µm device.

Another advantage of RMs is the possibility of controlling R_{ON} with programming current, as discussed in Section 2.3. This leads to possible multiple ON-states in a single RM device, and the storage density can be greatly increased. Although the exact mechanism of such effect is still under debate, it is generally agreed [69, 83, 93, 199] that current compliance during SET cycles may relate to the strength of conductive filaments, and therefore the R_{ON} values. Similar effects have been observed in the Cu/a-SiC/Au devices, as shown in Figure 5-15. With 100µA, 1mA and 10mA current compliance, the resulting R_{ON} from this device can be tuned in the range of ~3000Ω to ~50Ω. Typically a ratio of 10 is required to

differentiate resistance states [9], and therefore this device can potentially exhibit three distinguishable ON-states.

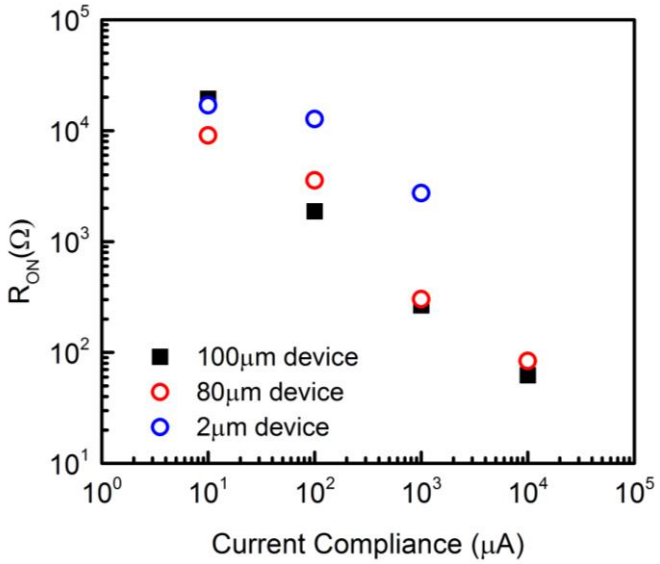

Figure 5-16 R_{ON} values achieved by different current compliance in three devices.

The effect of current compliance on ON-state resistance has been tested on three devices with different dimensions, as shown in Figure 5-16. For all three devices, the general trend is clearly that ON-state resistance decreases as current compliance increases, in agreement with previous studies [10, 11] on metallic filament based RMs. The range of R_{ON} of the two larger devices can be over 2 orders of magnitudes, while decrease of R_{ON} of the device with 4μm^2 area is less significant, partially due to that device could not repeatedly switch at 10mA current compliance. These results suggest the potential of multi-level storage of Cu/a-SiC/Au RM devices, although further testing is still needed to determine the details of multi-level operation, such as the possible range of ON-state resistance.

5.5 HRS Conduction Analysis

Similar to the case of LRS conduction, analysis of HRS conduction mechanism is also mainly dependent on the details of I-V characteristics. And HRS conduction can usually be explained by the mechanism discussed in Section 2.3.4. Figure 5-17 shows the HRS I-V characteristics of all the 4 switching modes in a Ln(I)-$V^{1/2}$ plot. Good linear fitting is obtained for all switching modes which strongly suggest a conduction mechanism dominated by thermo-ionic field emission over a Schottky barrier (Schottky emission) as displayed in Eq 5-2 [84]:

$$I = AA^*T^2 exp[\frac{-q\Phi_B}{kT} + \frac{q\sqrt{q/4\pi\epsilon_i}}{kT}\sqrt{E}] \quad (5\text{-}2)$$

$$\Rightarrow ln(I) = Ln(AA^*T^2) + \frac{-q\Phi_B}{kT} + \frac{q\sqrt{q/4\pi\epsilon_i}}{kT}\sqrt{E} \quad (5\text{-}3)$$

$$\therefore ln(I) \propto \sqrt{V} \quad (5\text{-}4)$$

And the Y-intercept is:

$$Ln(I_0) = Ln(AA^*T^2) + \frac{-q\Phi_B}{kT} \quad (5\text{-}5)$$

Where A is the conduction area, A^* is Richardson's constant, Φ_B is Schottky Barrier Height (SBH), E is electrical field, q is the electronic charge, k is the Boltzmann's constant, ϵ_i is dielectric constant of the film and T is absolute temperature.

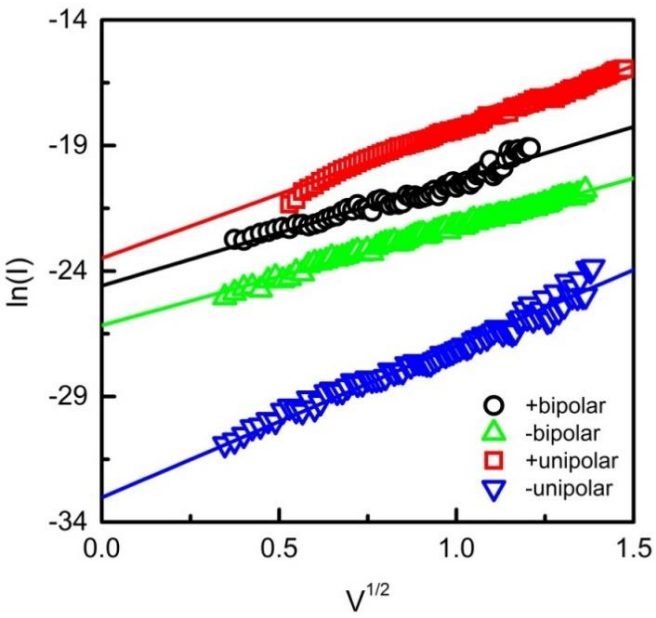

Figure 5-17 HRS I-V data from 4 switching modes (4 1μm diameter devices) in Ln(I)-$V^{1/2}$ plots, with linear fittings to the Schottky emission equation.

Schottky emission mechanism has been observed in some RMs, and was attributed to the Schottky barrier at the metal to solid electrolyte interface [145]. This can be expected as SiC have been widely exploited for Schottky diode applications, and the formation of Ohmic contacts between SiC and metals typically requires high temperature annealing [145]. The existence of Schottky barrier between the metal electrodes and a-SiC in this case is advantageous for Cu/a-SiC/Au RMs as it contributes to the high R_{OFF}, leading to high switching ratios.

Furthermore, assuming the a-SiC layer is n-type semiconductor after electroforming cycles, Schottky contact between counter electrode Au layer and the a-SiC layer will be reverse-biased when positive sweeping voltage is applied, and this contact dominates the HRS conduction. From the y-intercepts in Figure 5-17, the Schottky barrier height is calculated to be between 0.6eV to 0.9eV, with SBH in –unipolar mode noticeably higher than other three modes. The variation of SBH in different switching modes is likely an indication of the alteration to the a-SiC/Au interface caused by the SET/RESET cycles: Only in –unipolar mode the device was never subjected to positive bias on Cu electrode. In all other three modes, positive bias on Cu was involved in a full SET/RESET cycle. And this positive bias may promote the electrochemical migration of Cu atoms into the a-SiC layer, changing the a-SiC/Au interface. As work function of Au (5.1 eV) is higher than Cu (4.6 eV), presence of Cu at the interface may reduce the SBH.

5.6 Discussion of Switching Mechanisms

5.6.1 SET Process

As discussed in section 5.4, metallic filament is the most likely conduction mechanism in LRS. For RMs with Cu as active electrode (Cu positive biased during SET), numerous previous studies agree metallic filament is formed by electrochemical reaction of the Cu electrode: in essence, during the SET process, anodic dissolution of Cu according to the reaction: $Cu \rightarrow Cu^{Z+} + Ze^-$ takes place when Cu active electrode is under positive bias. Subsequently, Cu^{Z+} cations are driven by the electric field across the Cu and Au electrodes, and eventually reduced into Cu atoms according to the reaction $Cu^{Z+} + Ze^- \rightarrow Cu$, forming Cu conductive filaments for the LRS. These Cu filaments remain stable for the LRS even after removal of the external electric field, forming non-volatile characteristics. Recently real time observation of Cu filaments has been achieved using high resolution TEM [62, 81, 200].

In comparison with Cu, Au has a much higher reduction potential and thus has mainly been used as inert counter electrodes in RMs. Nevertheless, real time TEM observation of Au filaments has been recently reported, and the formation of Au filaments was attributed to electrochemical reaction similar to the formation of Cu filaments [201]. For the Cu/a-SiC/Au devices, when negative voltage is applied to the Cu electrode during SET process i.e. negative bipolar and negative unipolar modes, the Au electrode is subject to a

positive electrical field where Au atoms can be oxidized to Au^+ ions which reduce to Au atoms at the Cu counter electrode and thus form Au conductive filaments.

In most of the switching cycles, the SET processes appear to finish in one step: the current abruptly increases several orders of magnitudes, until the compliance was triggered. In addition, two step SET has also been observed, as shown in Figure 5-18. The current firstly increased from 10^{-11}A to 10^{-7}A, then from 10^{-6}A to 10^{-4}A. Similar two step switching behaviour has been reported in other metallic RMs, and it was suggested to be an indication of the formation of multiple conductive filaments [109]. As formation of multiple filaments may likely increase the fluctuation of switching parameters such as V_{SET} and V_{RESET}, suppressing such effect may worth further study in order to improve the switching uniformity of Cu/a-SiC/Au RMs.

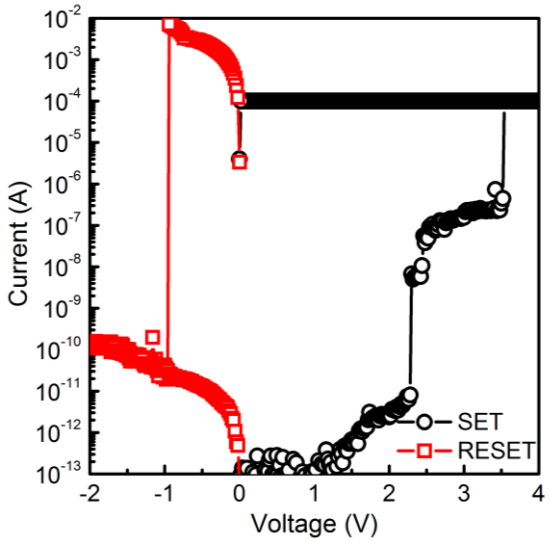

Figure 5-18 Two-step switching behaviour observed in a 1μm diameter device.

5.6.2 RESET Process

Reset process in RMs is essentially the rupture of the conductive filaments, and two mechanisms have been widely reported: electrochemical reaction and Joule heating induced diffusion [65, 68, 71, 72, 202]. In the +bipolar mode, it is reasonable to believe reversal of the electrochemical reaction leads to dissolution of the Cu filament and thus RESET of the device. On the other hand, in the +unipolar mode, where no reverse voltage was applied, Joule heating accelerated diffusion is most likely to cause rupture of the Cu filaments. As shown in Figure 5-19, the RESET power ($V_{RESET} \times I_{RESET}$) of +unipolar mode ($\sim 10^{-2}$W) is almost two orders of magnitude higher than +bipolar mode ($\sim 2 \times 10^{-3}$W).

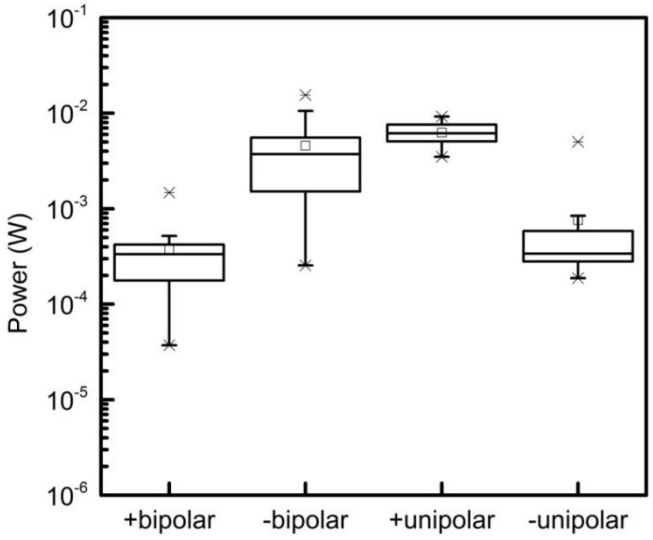

Figure 5-19 Distribution of RESET power (V_{RESET} × I_{RESET}) of four switching modes during 20 switching cycles.

Regarding the negative switching modes, similar mechanisms, i.e. electrochemical reaction for bipolar switching and Joule heating accelerated diffusion for unipolar switching, can be expected to apply. But in contrast to the positive modes, RESET in –bipolar mode requires higher power than –unipolar mode. A possible explanation is this: in –bipolar and +unipolar modes, RESET is triggered by positive sweeping voltage, under which electrochemical reaction leads to Cu filament formation. And this likely enhances the existing conductive filaments. Therefore the RESET process in these modes will require rupture of these newly formed filaments and hence higher power. This explanation is also supported by the calculated HRS Schottky barrier heights and comparison of R_{ON} of four switching modes: HRS of +bipolar, +unipolar and –bipolar have similar SBH while SBH in –unipolar mode is noticeably higher. In –unipolar mode, positive bias was never applied on Cu electrode, therefore there is no Cu presence at the a-SiC/Au interface. In all other three modes, Cu may be introduced to the a-SiC/Au interface to lower the SBH, as positive bias is applied at least once in the switching cycle. The addition of Cu atoms during –bipolar and +unipolar RESET may also enhance the conductive filament in the next SET cycle, so R_{ON} of these two modes can be lower, as shown in Figure 5-9.

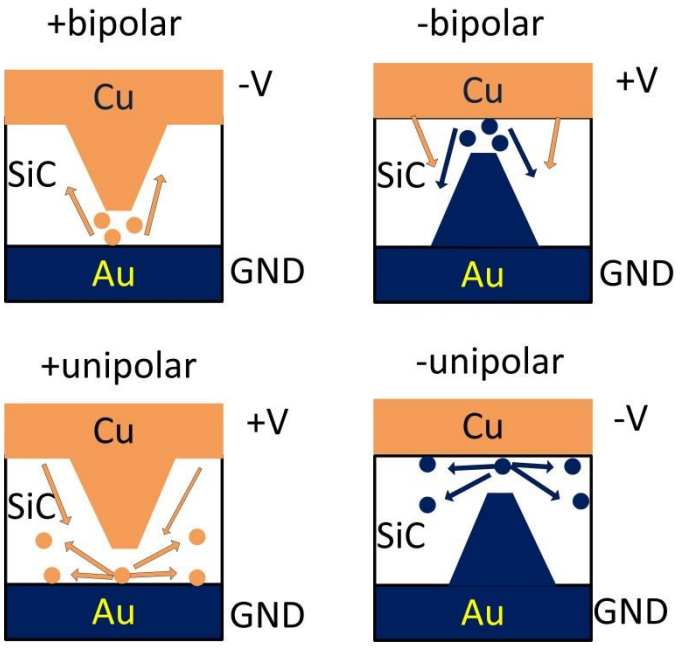

Figure 5-20 Schematic of likely RESET processes of four switching modes. The applied voltage bias was marked next to the metal electrodes. Cu electrodes, filaments and migration direction of Cu atoms are orange coloured, and dark blue colour for the Au electrodes, filaments and migration direction of Au atoms.

In summary, metallic filament formation by electrochemical reaction of Cu and Au electrodes is presumably the dominant mechanism for the SET processes. For RESET processes, in +bipolar mode electrochemical reaction is likely to dominate while Joule heating accelerated diffusion appears to be involved in all other three modes. It's also worth mentioning that our devices have clearly demonstrated stable resistive switching when Cu and Au electrodes are subjected to positive electrical fields suggest that the Au electrode is not only inert enough to enable +bipolar and +unipolar switching cycles, but also active enough to allow -bipolar and -unipolar switching behaviours.

5.7 Retention Performance

Figure 5-21 shows the retention performance of R_{ON+}, and R_{OFF} states. There is no noticeable deterioration over the measurement duration at 85°C. The power-law extrapolation suggests that the ON/OFF switching ratio after 10 years can still be expected to be greater than 10^7, implying excellent stability and retention of these devices. This might be attributable to the high chemical stability of SiC material as well as the low Cu and Au diffusion in SiC [20, 21, 203].

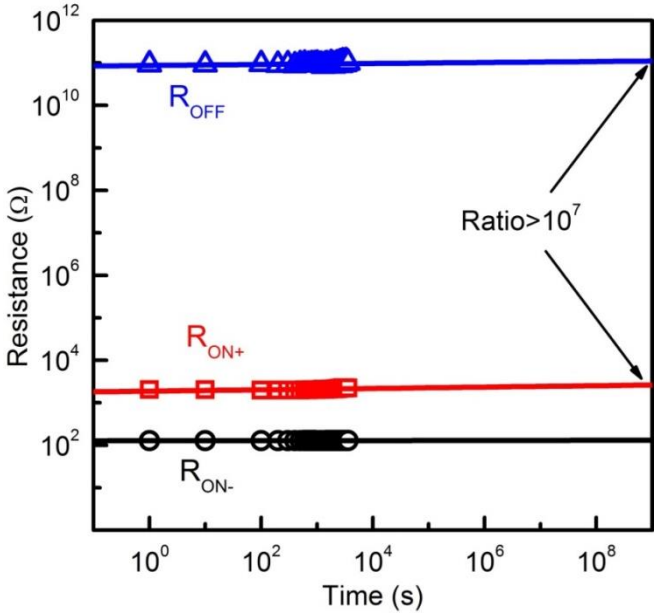

Figure 5-21 R_{ON} and R_{OFF} values versus time measured at 85°C, with power law extrapolation to 10 years.

5.8 Summary

In summary, a series of Cu/a-SiC/Au devices with different device dimensions were obtained and their resistive switching behaviour analysed. All 4 possible switching modes are presented with high ON/OFF ratios in the range of 10^6~10^8 for all modes. Distribution of switching parameters (V_{SET}, V_{RESET}, R_{ON}, R_{OFF}) during repeated cycles are also presented. Detailed I-V characteristics analysis suggests that the conduction mechanism in LRS is due to the formation of Cu or Au filaments. Schottky emission is proven to be the dominant conduction mechanism in HRS which results from the Schottky contacts between the metal electrodes and SiC. As for the rupture of the filaments in the RESET processes, in +bipolar mode electrochemical reaction is likely to dominate while Joule heating accelerated diffusion appears to be involved in all other three modes. The combination of Cu and Au as electrodes in the a-SiC RM has proven to be effective in enabling all 4 possible nonpolar switching modes. The Cu/a-SiC/Au devices also show excellent retention performance. These results suggest promising application potentials for Cu/a-SiC/Au RMs.

Chapter 6. Influence of device Structures and Materials on Switching Properties

To further investigate the switching properties of a-SiC based resistive memories, a-SiC based RMs with modified device structure, solid electrolyte materials and counter electrode materials were fabricated and their resistive switching properties measured and discussed. By exploring the effects of device structures and materials on the performance of a-SiC based RMs, it is envisaged their possible applications can be further optimized and expanded. Moreover, additional insight into the switching mechanism of a-SiC based RMs can also be gathered in the process.

6.1 Influence of Device Structure

In addition to the via-stack structure discussed in chapter 5, cross-bar structure is frequently opted in previous studies on resistive memories as illustrated in Section 2.4. While the via-stack structure is generally believed to offer simple integration with CMOS circuits, the cross-bar structure may lead to higher storage density, which is a key requirement for the next generation non-volatile memories. Therefore testing of cross-bar structured RMs is essential for the future applications of a-SiC based RMs. In addition, in previous studies of RMs, typically only one type of device structure was investigated for a certain combination of RM materials. By comparing RMs with the same material configuration but different device structure, possibly further indications of switching mechanisms can be gained.

6.1.1 Fabricated Cross-Bar Structured Devices

One substrate with fabricated devices is shown in Figure 6-1. The substrate is 1cm by 1cm square Si chip with 1000nm thermal oxide. In one batch usually 4 to 6 chips were used, and each chip has maximum of 11 devices on it. Although the number of devices in one batch is quite limited, the overall process time is relatively short and therefore three batches of cross-bar structured device with a-SiC thickness being approximately 35nm, 50nm and 80nm. In this way the possible influence of a-SiC film thickness on the switching behaviour may also be investigated. Figure 6-2 shows an SEM image of a 5μm *5μm device. The four large squares are 250μm*250μm contacts, and the overlapping area of the two thin strides are the device active region. The cross-section view of the active region is

shown in Figure 6-3, which clearly shows the two metal layers separated by the thin dark layer of a-SiC. Similar to the cross-section view of the via-stack device as shown in Figure 5-3, this image was also obtained through FIB-milling.

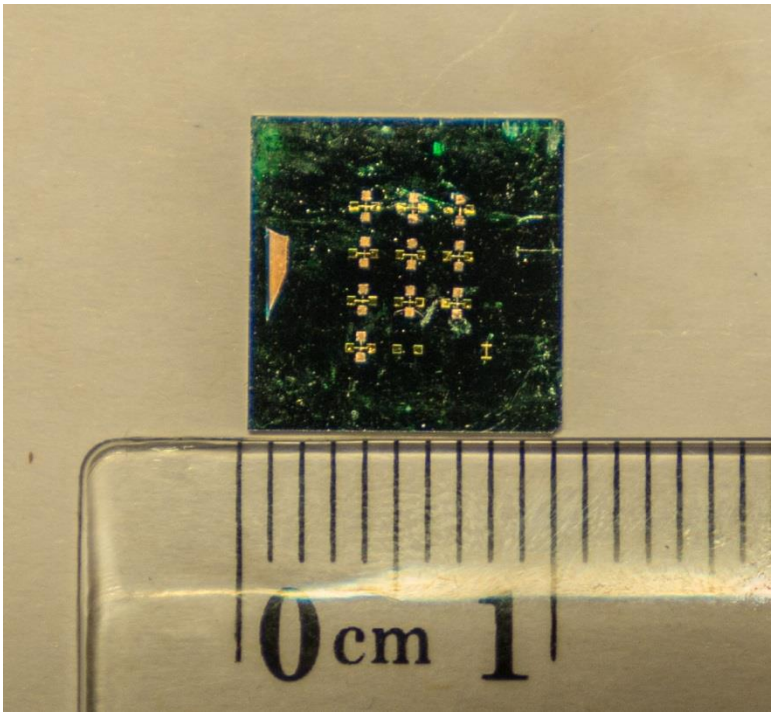

Figure 6-1 Photo of one square substrate with 11 cross-bar structured Cu/a-SiC/Au devices.

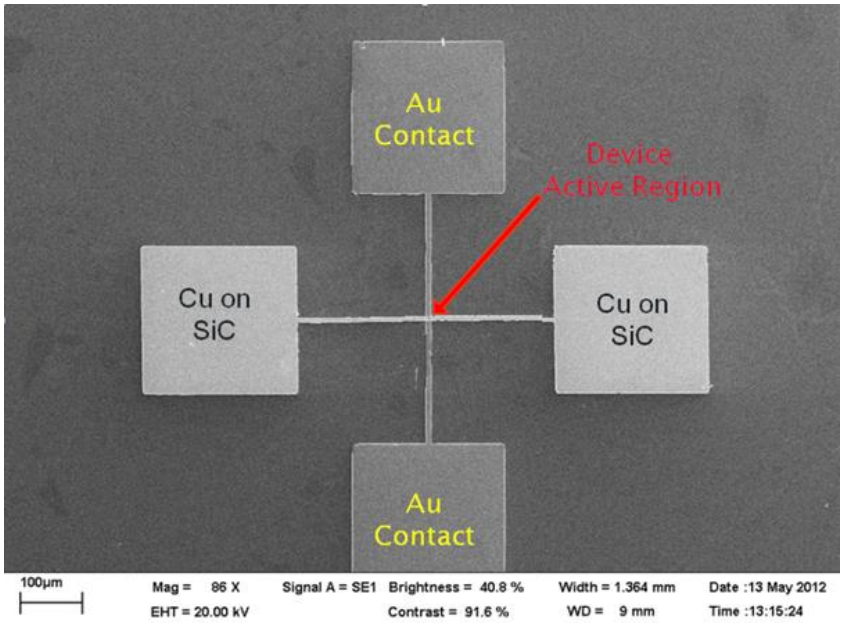

Figure 6-2 Top-view SEM image of a cross bar structure Cu/a-SiC/Au RM device. The intersection of the two bars is the device active region. The bars are connected to their respective contact pads.

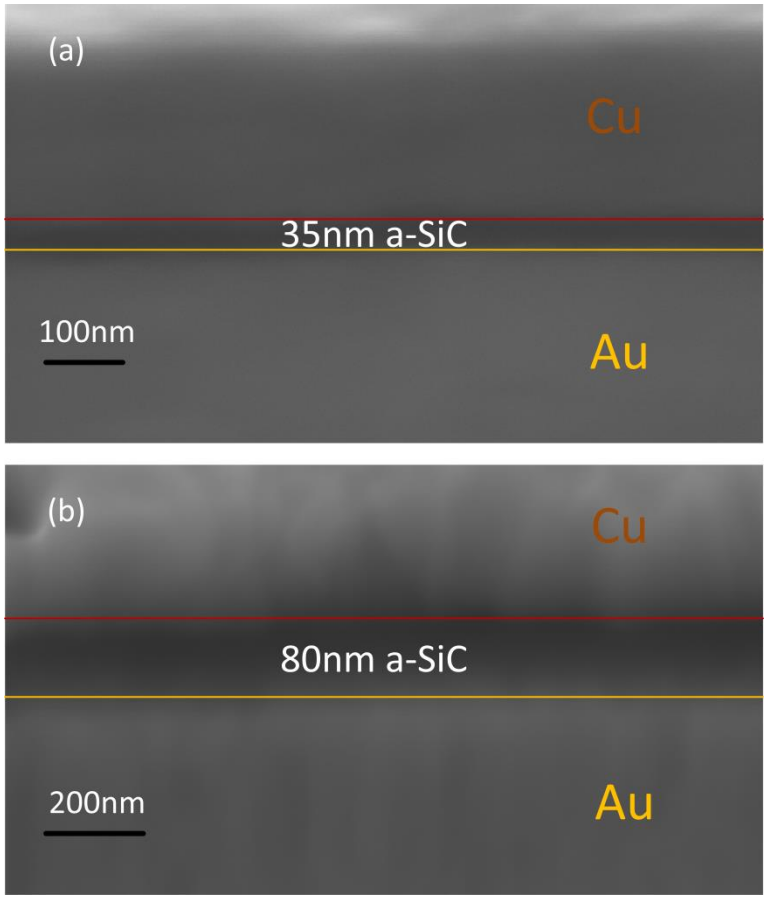

Figure 6-3 Cross-section SEM image of device active region of a (a) 35nm thick a-SiC and (b) 80nm thick a-SiC cross-bar structure Cu/a-SiC/Au RM device.

6.1.2

6.1.3 Switching Behaviour of Cross-Bar Structured Devices

The first four positive bipolar switching cycles of three 5μm*5μm cross-bar structured RMs with 80nm, 50nm and 35nm a-SiC layer are shown in Figure 6-4, Figure 6-5 and Figure 6-6, respectively. In all these figures, the transition from HRS to LRS can be clearly observed in the positive cycles, but the obtained LRS appear less stable in the 80nm and 50nm a-SiC devices. This is consistent with the previous observation of unstable LRS from lower compliance in the via-stack RMs shown in chapter 5, and may also be explained by the conductive filament formation mechanism. With the same current compliance setting, the total volume of Cu filament in devices of different a-SiC thickness can be expected to be comparable, and the Cu filament in thicker devices may be thinner. Therefore the random diffusion of Cu atoms may have a greater impact on the LRS of thicker devices, leading to unstable LRS. The electroforming voltage also generally decreases from approximately 6V~5V to ~4V as the a-SiC thickness decreases from 80nm to 35nm.

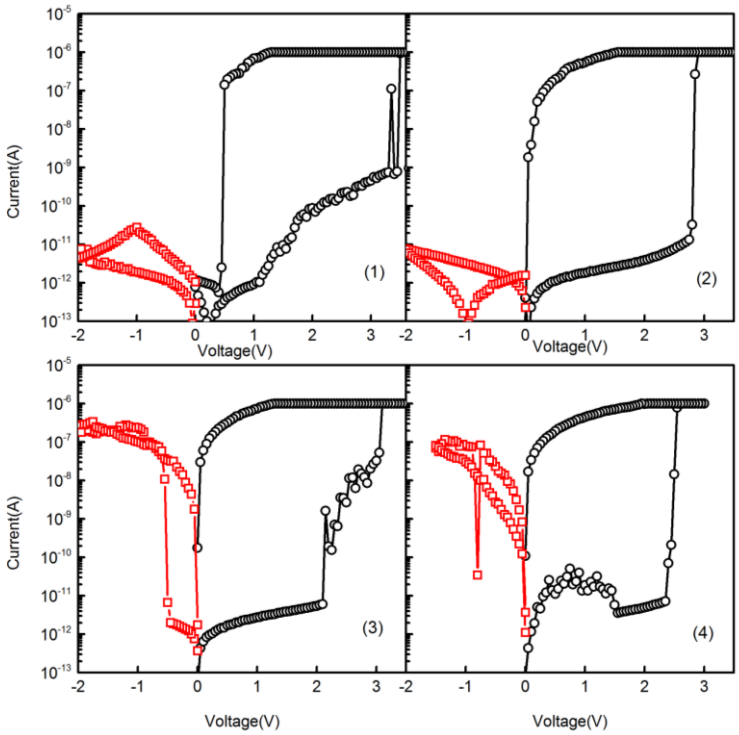

Figure 6-4 Four consecutive switching cycles from a 5μm*5μm, cross-bar device with 80nm thick a-SiC solid electrolyte.

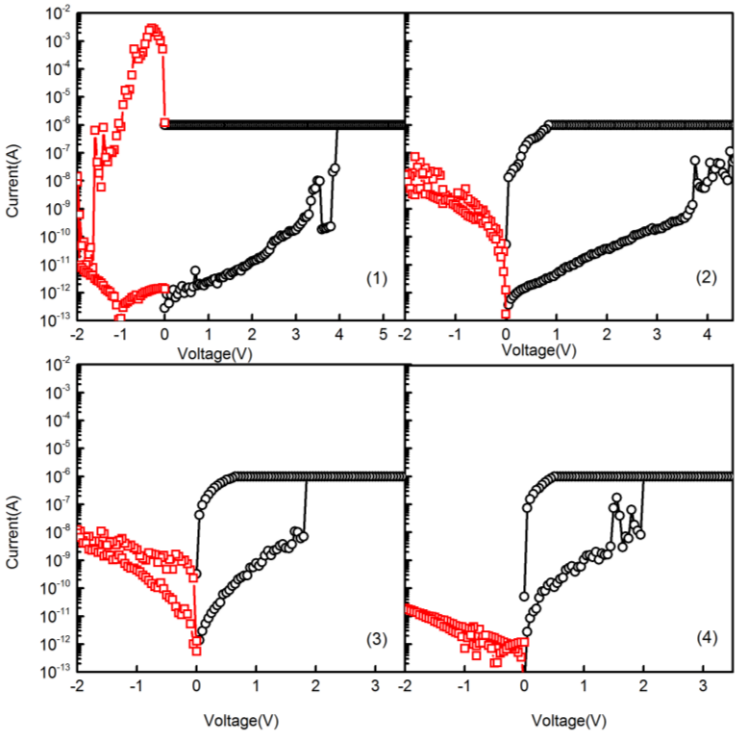

Figure 6-5 Four consecutive switching cycles from a 5μm*5μm, cross-bar device with 50nm thick a-SiC.

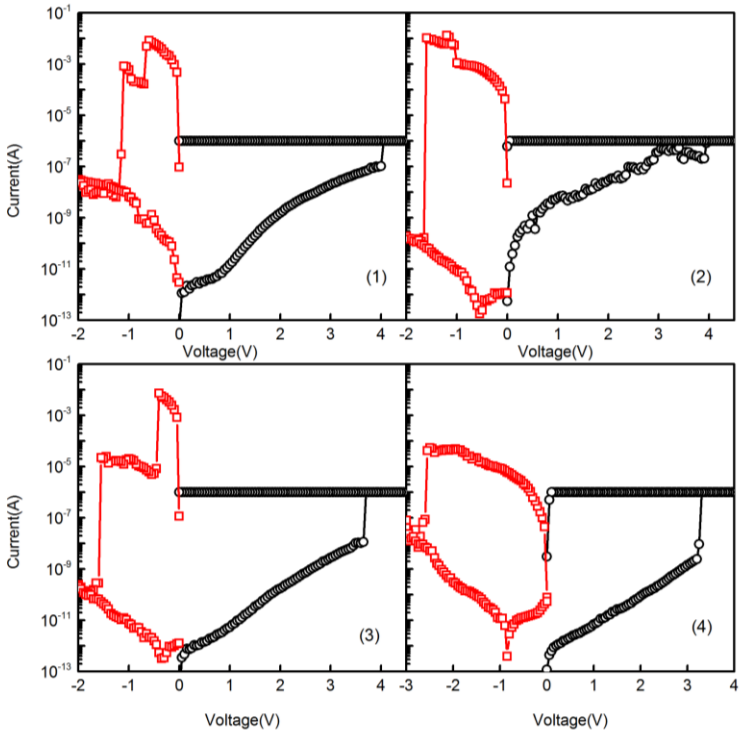

Figure 6-6 Four consecutive switching cycles from a 5μm*5μm, cross-bar device with 35nm thick a-SiC solid electrolyte.

In the a-SiC devices with 35nm a-SiC solid electrolyte, the LRS resistance was found to be largely independent from the current compliance, as shown in Figure 6-7. The current compliance was 10^{-6}, 10^{-5}, 10^{-4} and 10^{-2}A, and the resulting R_{ON} was approximately 100Ω, 50Ω, 200Ω and 20Ω. Such discrepancy has been observed in previous studies [93-95], and is likely to be related to the current overshoot during SET process. Essentially, the consensus is that the formation of conductive filament occurs in a timeframe of several to 10s of nanoseconds, and consequently, the current through device increase several orders of magnitudes in similar short time [193]. It is therefore possible in a very short period, the actual current through device is significantly over the compliance due to the response time of the equipment, and this current over-shoot may further promote the growth of conductive filament and lead to lower R_{ON}.

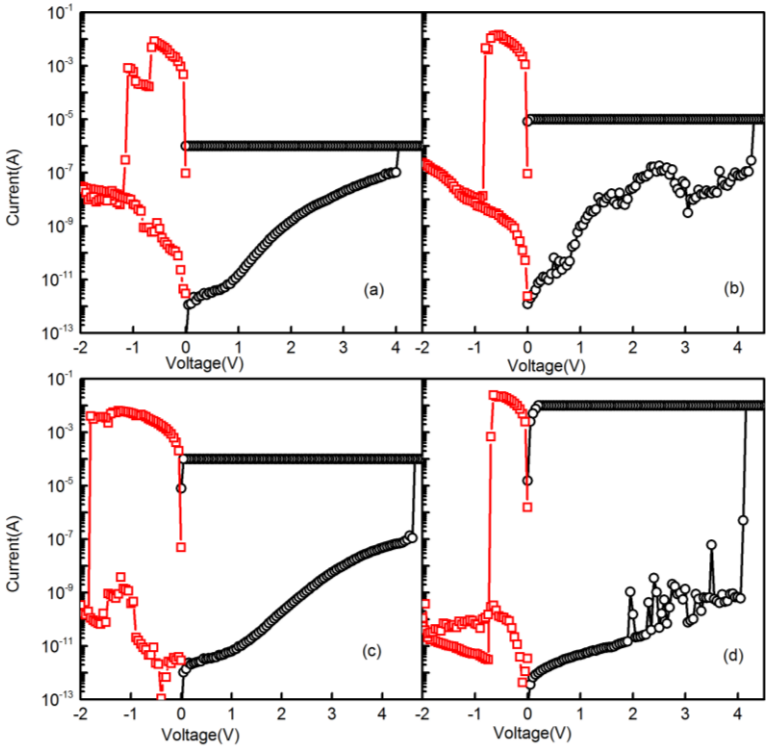

Figure 6-7 Four switching cycles from a 5μm*5μm cross-bar device with 35nm a-SiC , with different current compliance: (a) 10^{-6}A, (b) 10^{-5}A, (c) 10^{-4}A, (d) 10^{-2}A.

As presented in Section 5.2, the via-stack devices can operate steadily with current compliance of 10^{-4}A. The cross-bar structured devices with 35nm a-SiC, on the other hand, can operate steadily at current compliance of 10^{-2}A, as shown in Figure 6-8. Such high compliance leads to very low R_{ON} of ~100Ω. With the combination of low R_{ON} and high R_{OFF}, these cross-bar structured RMs show very high OFF/ON ratio in the range of 10^{8}~10^{9}. These ratios are not only a great improvement over previous reported values of a-SiC RMs (~10^{3}), but also higher than the via-stack structured RMs discussed in chapter 5 (~10^{7}). The following results are all from 35nm a-SiC, 5 μ m*5 μ m cross-bar device with current compliance being 10^{-2}A.

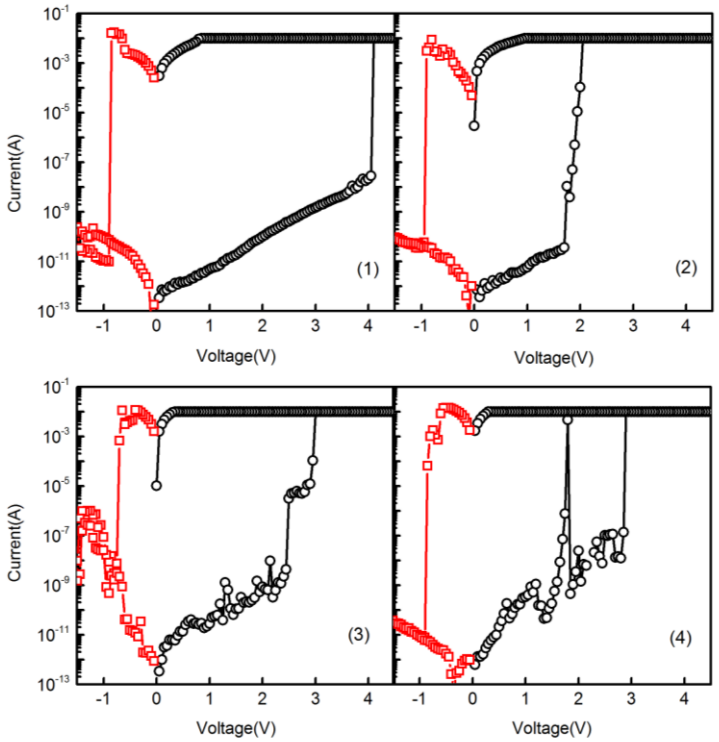

Figure 6-8 Four consecutive switching cycles from a 5μm*5μm 35nm thick a-SiC cross-bar device, with 10^{-2}A current compliance.

6.1.4 Distribution of Switching Parameters

The R_{ON} and R_{OFF} values of 5μm*5μm, 35nm thick a-SiC cross-bar device in 20 switching cycles are extracted and plotted in Figure 6-9 and their distribution shown in Figure 6-10. R_{ON} over 20 cycles are in the range of 10^{2}~$10^{3}\Omega$, and R_{OFF} has a slightly wider dispersion, in the range of 10^{12}~$10^{9}\Omega$. The typical ON/OFF ratio is in the order of approximately 10^{8}, and the minimum ratio is over 10^{6}. In general, as the cross-bar structured devices can sustain higher current compliance during SET, their R_{ON} can be lower than that of the via-stack devices, and consequently the ON/OFF ratio can be further improved. In 20 cycles, there also was no noticeable decrease of R_{OFF}. The reason that cross-bar structured device may sustain higher current may be related to the difference in heat dissipation around device active region due to the different device structures. Furthermore, no repeatable –bipolar and –unipolar switching has been repeatedly observed in these cross-bar devices, which may also be due to less thermal accelerated diffusion of Au in the cross-bar devices. In future work, simulation of heat dissipation process in the device active region may provide a better understanding of the resistive switching process.[68, 72, 204]

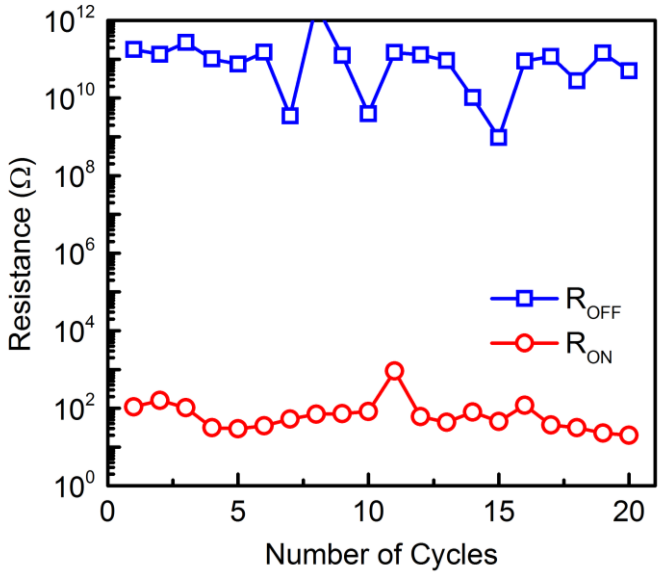

Figure 6-9 R_{ON} and R_{OFF} values over 20 cycles from a 5µm*5µm, 35nm thick a-SiC cross-bar device, with 10^{-2}A current compliance.

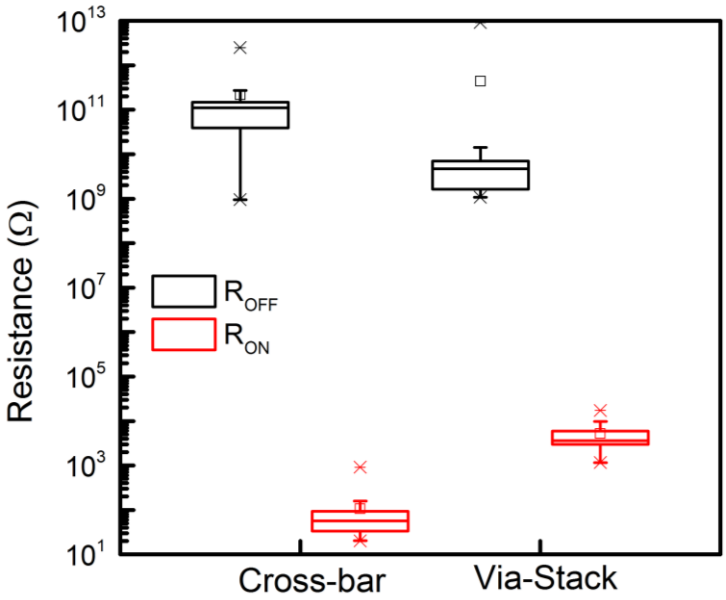

Figure 6-10 Distribution of R_{ON} and R_{OFF} over 20 cycles a 5µm*5µm, 35nm thick a-SiC cross-bar device.

As shown in Figure 6-11, V_{SET} of cross-bar devices are slightly higher than via-stack devices (~2.5V as to ~2V), and V_{RESET} is slightly lower (~-0.8V as to ~-1.2V). The lower V_{RESET} is probably related to the lower R_{ON} and therefore higher LRS current, which may promote the dissolution of conductive filament. The cause of the higher V_{SET}, on the other hand, requires further study.

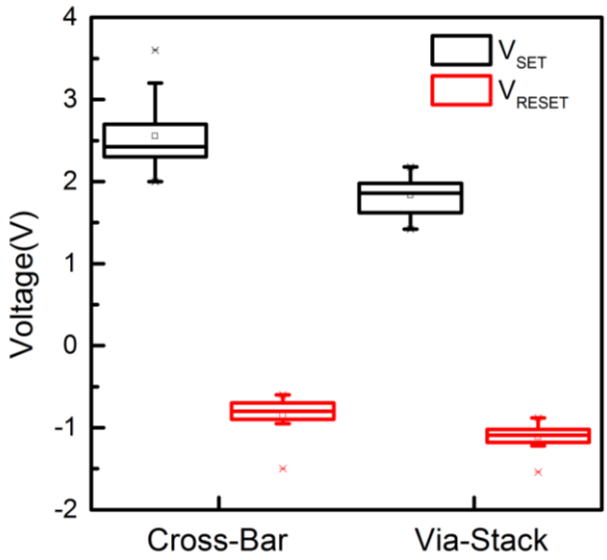

Figure 6-11 Distribution of V_{SET} and V_{RESET} over 20 cycles a 5µm*5µm, 35nm thick a-SiC cross-bar device.

6.1.5 LRS Conduction of Cross-Bar Structured Devices

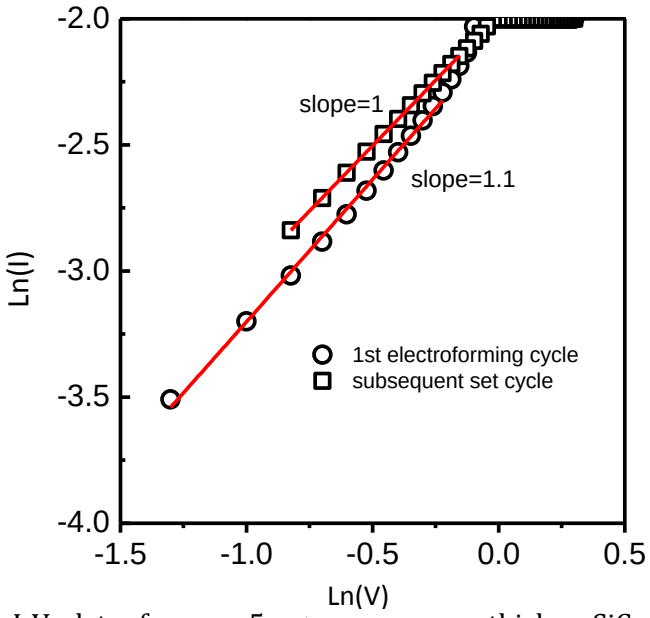

Figure 6-12 LRS I-V data from a 5µm*5µm, 35nm thick a-SiC cross-bar device in Ln(I)-Ln(V) plots, with respective linear fittings.

As can be expected, the LRS conduction mechanism of the cross-bar devices is most likely Cu filament. Same as the via-stack devices, the cross-bar devices clearly show Ohmic conduction, as shown in Figure 6-12. In addition, Figure 6-13 shows R_{ON} as a function of temperature, where R_0 is the resistance at room temperature T_0=300K. In agreement with the linear LRS I-V data, metallic conduction behaviour is observed for the LRS resistance, with the temperature co-efficient found to be $3.2\text{x}10^{-3}$ K^{-1}. This value is slightly higher than $2.4\text{x}10^{-3}$ K^{-1} found in the via-stack devices, but still in agreement with reported

values for Cu nanowires [191]. It has also been reported that temperature co-efficient of resistance of Cu nanowires may decrease as the dimension of nanowires decrease [191], which may apply here as the lower R_{ON} of cross-bar devices is likely related to larger dimension of Cu filament.

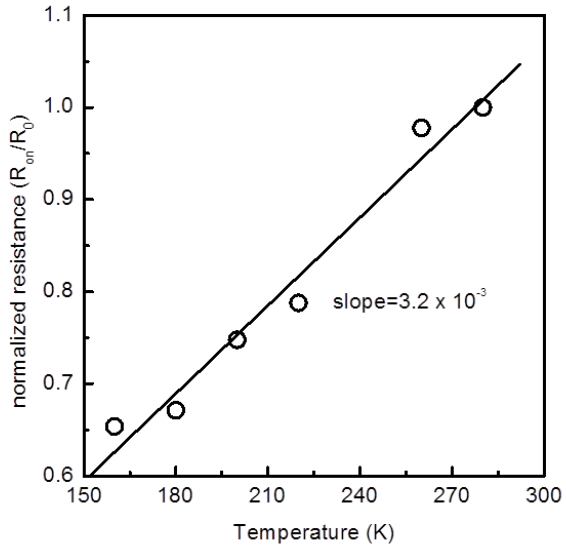

Figure 6-13 Normalized R_{ON} vs temperature. Circles are experimental data and the solid line is a linear fit.

6.1.6 HRS Conduction of Cross-Bar Structured Devices

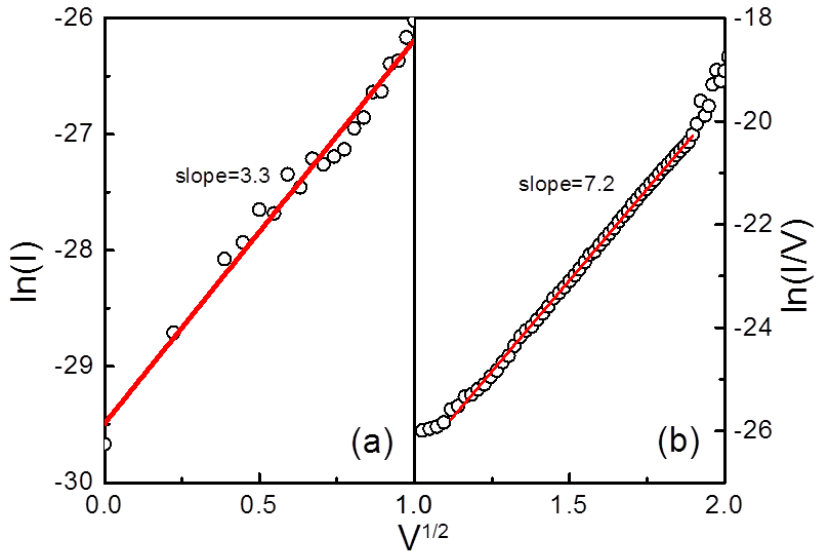

Figure 6-14 Typical HRS I-V characteristics in an electroforming cycle from a 5μm*5μm, 35nm thick a-SiC cross-bar device in the (a) V<1V region and (b) V>1V region. Symbols are measured data and lines are linear fittings.

Figure 6-14 shows a typical HRS I-V curve of a pristine Cu/a-SiC/Au RM device, suggesting Schottky Emission for voltage below 1V and P-F emission for voltage above 1V. Using the

Schottky emission equation discussed in Section 2.3, linear fitting leads to the estimation of zero bias Φ_B =0.79 eV. For V>1V region, P-F emission, as a bulk material dominant conduction, follows [84],

$$\ln\left(\frac{I}{V}\right) \propto \frac{\sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r d}}}{kT}\sqrt{V} \tag{6-1}$$

A slope of 7.2 was obtained in Fig. 8 (b). By inputting the value of the slope and the thickness of the a-SiC layer d=35 nm into Eq. (2), ε_r =5 is obtained. Subsequently, a refractive index n (n = $\sqrt{\varepsilon_r}$) of approximately 2.2 is obtained. This value is in excellent agreement with the value of 1.9~2.4 reported for a-SiC thin films. For the subsequent SET/RESET switching cycles no P-F Emission is found across the entire voltage range, and the HRS conduction was dominated by Schottky emission, similar to the via-stack structured devices. The different conduction mechanisms of the pristine devices are possibly a result of difference in the Au/a-SiC interface caused by the different fabrication processes [145, 146, 205].

6.1.7 Retention Test

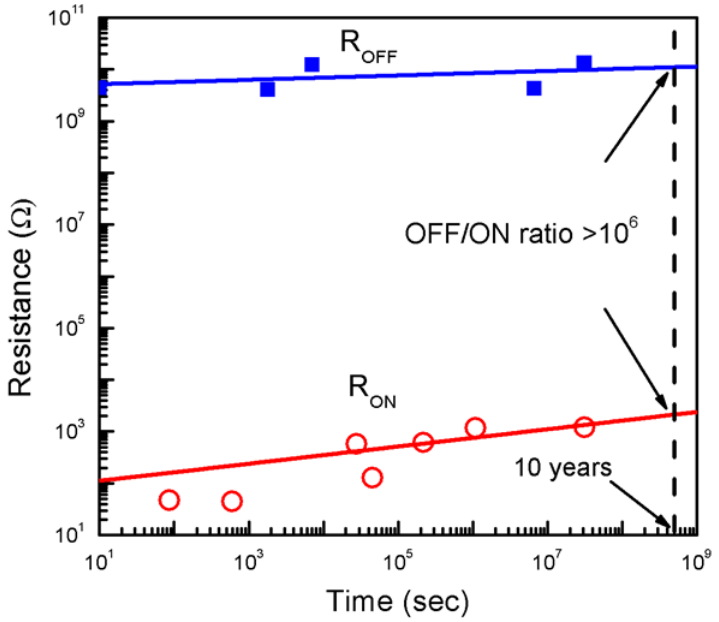

Figure 6-15 Estimation of device retention by linear extrapolation. Circles are experimental data and solid lines are liner fits.

In Section 5.7, the retention time of Cu/a-SiC/Au RMs were estimated by extrapolating R_{ON} and R_{OFF} measured in a relatively short period at elevated temperature. For the cross-bar devices, R_{ON} and R_{OFF} were measured over 1 year period at room temperature [100], and

the results are shown in Figure 6-15. The linear extrapolation also shows in 10 years' time the ON/OFF ratio can still be expected to exceed 10^6. This indicates excellent stability and retention of these cross-bar structured devices and also further demonstrates the excellent retention of RMs based on Cu and a-SiC.

6.1.8 Summary

In summary, three batches of cross-bar structured Cu/a-SiC/Au devices were fabricated and their resistive switching behaviour tested. +bipolar switching has been observed in all three batches, with the ones with thinnest a-SiC layer showing most stable resistive switching behaviour. The cross-bar devices could sustain higher current compliance during SET, which led to lower R_{ON} and higher ON/OFF ratio. The cross-bar devices also had slightly higher V_{SET} and no repeatable negative switching. These differences may be related to the difference in heat dissipation due to the different structure of device active regions. And in future work thermal simulations may prove useful for a better understanding of the SET processes in different structured devices. After electroforming, the conduction mechanisms for the HRS and LRS of the cross-bar devices are the same as the via-stack devices, which implies similar Cu filament formation/dissolution switching mechanism. The cross-bar devices also exhibited great state retention, similar to the via-stack devices, which further demonstrates the excellent retention of RMs based on Cu and a-SiC.

6.2 Influence of Cu Incorporation in a-SiC Solid Electrolyte

6.2.1 Fabricated RMs Based on a-SiC/Cu

As discussed in Section 2.5, a great number of dielectric materials have been explored as the solid electrolyte material for resistive memories, and many studies have reported improved performance from doping the solid electrolyte layer with various forms of metal dopant. By adding Cu in SiC solid electrolyte, additional Cu ions may be provided during switching, and the switching voltage may be reduced. In addition, added Cu may also enhance local electrical field and provide preferred formation path for Cu filament, so that the randomness of formation process may be reduced, and the switching parameters may exhibit a more uniform distribution.

In this project, co-sputtered a-SiC/Cu was investigated as solid electrolyte material, and the deposition and material properties of a-SiC/Cu films were presented in Chapter 4.

Based on the composition, resistivity and composition rate results in Section 4.3, 3 batches of Cu/a-SiC/Au RM devices with a-SiC/Cu as solid electrolyte were fabricated. The deposition power configurations were chosen for the lower end of Cu atomic percentage, mostly because as shown in Figure 4-10 the addition of Cu reduced the resistivity of a-SiC films by several orders of magnitudes, and low resistivity of a-SiC/Cu films may lead to reduced R_{OFF} and consequently lower ON/OFF ratio. The deposition time were also determined from the deposition rate shown earlier, so that the total thickness of the solid electrolyte layer remains approximately 35~40nm. These devices have the same via-stack structure as discussed in Chapter 5, so the fabrication route remained mostly the same. Only the deposition of a-SiC/Cu was the different step. The deposition conditions are listed in Table 6-1. The Cu atomic percentage shown in table is an estimation from results shown in Chapter 4, assuming the film composition remains the same for the same deposition conditions.

SiC Power(W)	**Cu Power(W)**	**Deposition Time (s)**	**Estimated Cu at. %**
340+340	10	150	18
250+250	10	210	21
250	15	400	28

Table 6-1 Deposition conditions and estimated Cu atomic percentage of the co-sputtered a-SiC/Cu solid electrolyte used in three batches of devices.

The top-view and cross-section SEM image of a 1μm diameter Cu/a-SiC:0.18Cu/Au device are shown in Figure 6-16. Same as Figure 5-4, the cross-section in Figure 6-16 was also revealed by FIB-milling. Compared to the undoped a-SiC layer shown in Figure 5-3, the Cu doped a-SiC layer appears to be in lighter shade, which may be related to the higher conductivity of the doped a-SiC. In this batch the larger devices also had the similar discontinuation and buckling up of Cu layers around the SiO_2 steps as discussed in Chapter 5. Clearly the optimisation of Cu deposition to eliminate or reduce such effect should be considered in future work on the via-stack structured RMs. In the fabrication process, the

lift-off of second doped batch was not very successful and the device yield was quite low. Although resistive switching was observed in some of the remaining devices from that batch, those results are not included in this section. As the switching behaviour of 1µm diameter devices was most thoroughly tested among the undoped devices, the testing of devices with Cu doped solid electrolyte was also concentrated on 1µm diameter devices.

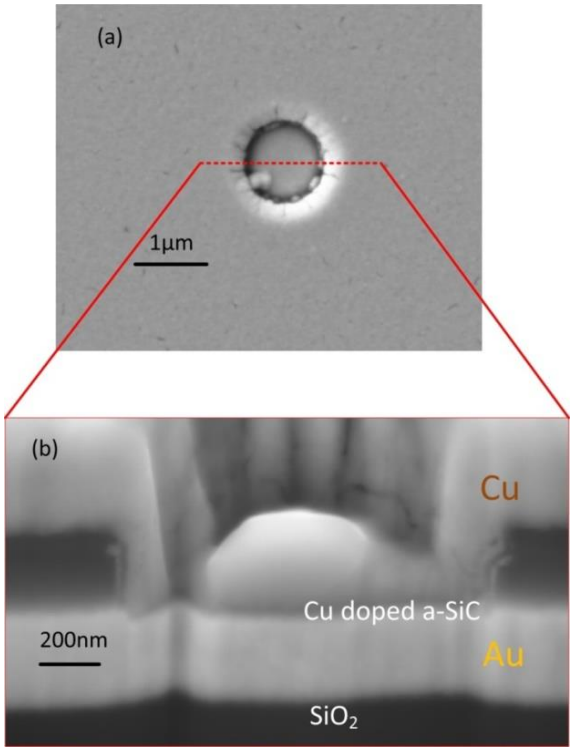

Figure 6-16 (a) Top-view and (b) Cross-section SEM image of a 1µm diameter Cu/a-SiC:Cu/Au device.

6.2.2 Nonpolar Switching Behaviour

In both batches of Cu/a-SiC:0.18Cu/Au and Cu/a-SiC:0.28Cu/Au devices, four modes of resistive switching have been observed, as shown in following Figure 6-17 to Figure 6-20. The existence of the four switching modes can be expected as the undoped devices have already shown nonpolar switching behaviour. However the exact resistive switching mechanisms of the doped devices may not be the same and still requires further study. It is possible that the Cu content in the a-SiC layer, instead of the Au electrodes, may form the conductive filament when negative bias on Cu AE is applied. The most noticeable feature in these results is that HRS current is comparable and occasionally lower than the undoped devices. This was unexpected as the resistivity of co-sputtered a-SiC/Cu films are at least over 4 orders of magnitudes lower than the as-deposited a-SiC film, as shown in Section 4.3.2. This most likely suggests that in these devices HRS conduction is limited by

the interface between solid electrolyte and metal electrodes, other than the solid electrolyte layer itself. A few rapid fluctuations of HRS current can also be observed, especially in the Cu/a-SiC:0.18Cu/Au devices, which may be an indication that the added Cu may re-arrange under the applied voltage.

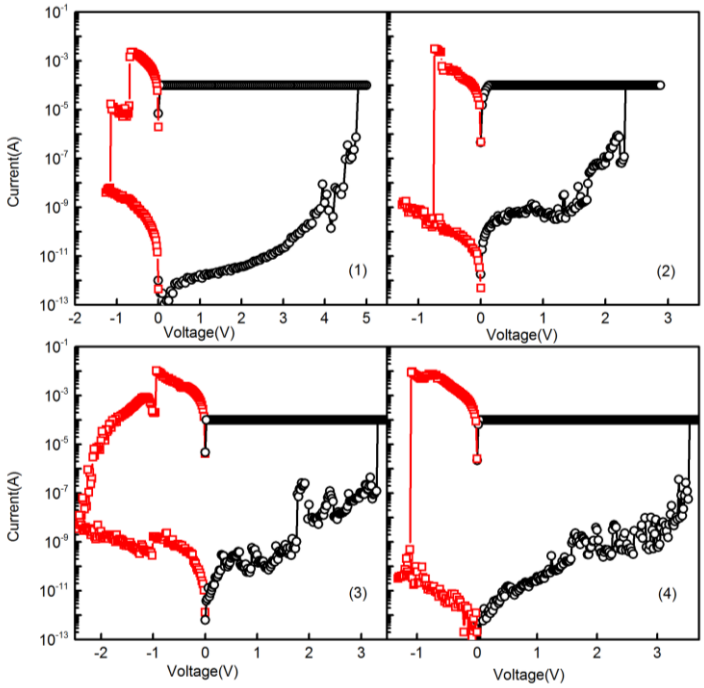

Figure 6-17 Four consecutive switching cycles from a 1μm diameter, Cu/a-SiC:0.18Cu/Au device.

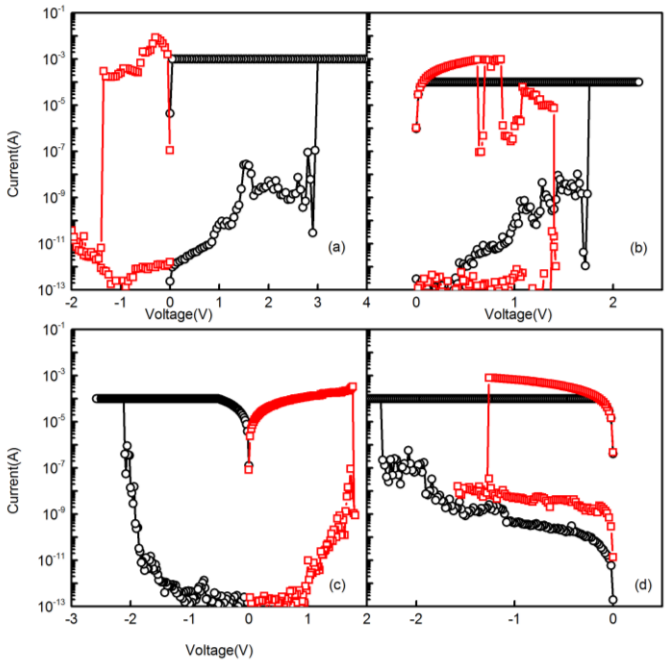

Figure 6-18 Switching cycles of all four switching modes: (a) +bipolar, (b), +unipolar, (c) -bipolar and (d) –unipolar observed in 4 1μm diameter, Cu/a-SiC:0.18Cu/Au devices.

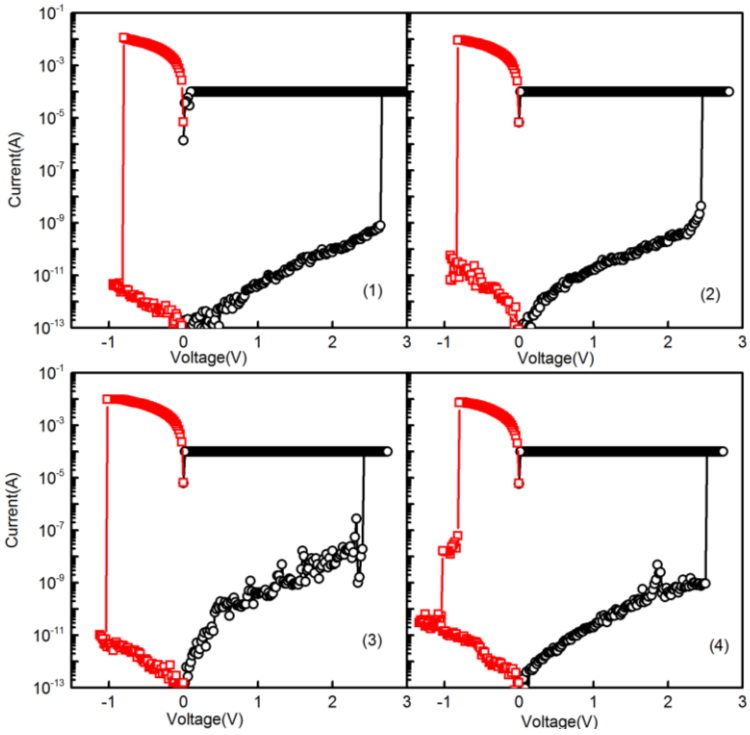

Figure 6-19 Four consecutive switching cycles from a 1μm diameter, Cu/a-SiC:0.28Cu/Au device.

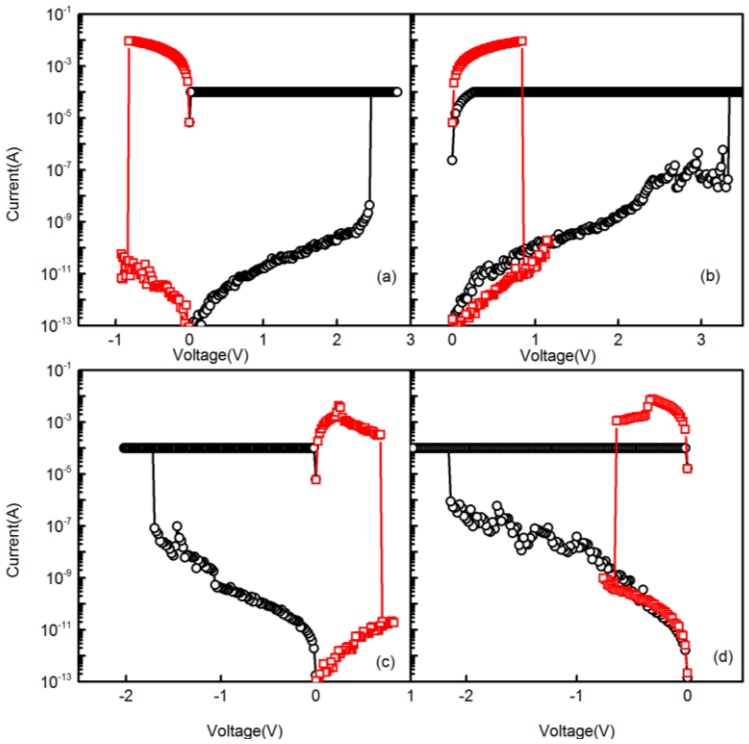

Figure 6-20 Switching cycles of all four switching modes: (a) +bipolar, (b), +unipolar, (c) -bipolar and (d) –unipolar observed in 4 1μm diameter, Cu/a-SiC:0.28Cu/Au devices.

6.2.3 Distribution of Switching Parameters

The distribution of V_{SET}, V_{RESET}, R_{ON} and R_{OFF} in +bipolar switching modes are shown in Figure 6-21 and Figure 6-22, with comparison to the undoped devices. These results are preliminary and further testing is still required to get a full picture of the performance of the doped devices. However, a few observations can still be made. Overall the switching parameters are not significantly different between three batches of devices. The Cu/a-SiC:0.18Cu/Au device has noticeably wider distribution of switching voltages and R_{OFF}. A possible cause is that with additional Cu in the solid electrolyte layer, there may be multiple possible formation paths for the Cu filament with locally enhanced electrical field. This could increase the randomness of the switching process. Another apparent trend is that R_{ON} generally decreases for the RM devices with higher Cu content in the a-SiC:Cu composites. This may be expected as the additional Cu content can complement the total volume of the conductive filament, and thus reduces R_{ON}. As discussed earlier, R_{OFF} of the doped devices was not reduced, which suggests HRS conduction was more likely to be interface limited instead of bulk limited. Consequently, possibly a-SiC films with higher Cu content may still work as solid electrolyte layer, as the devices based on them may show higher ON/OFF ratios than expected from their resistivity values.

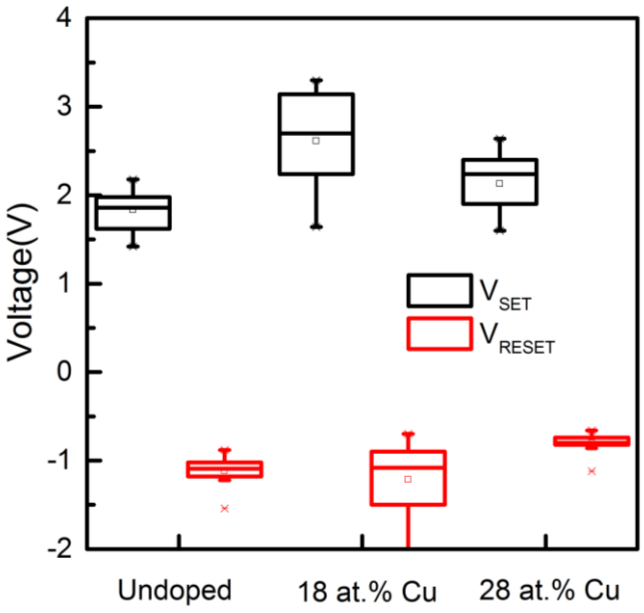

Figure 6-21 Distribution of V_{SET} and V_{RESET} in +bipolar switching modes from 1μm diameter devices.

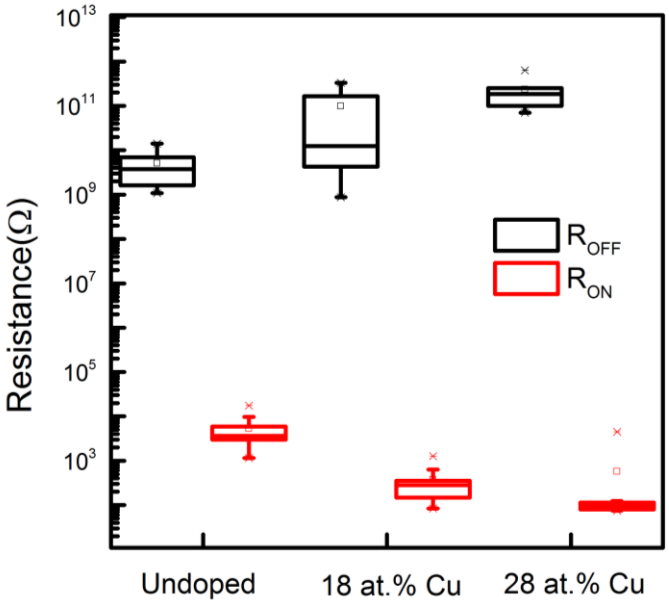

Figure 6-22 Distribution of R_{ON} and R_{OFF} in +bipolar switching modes from 1μm diameter devices.

6.2.4 HRS Conduction Analysis

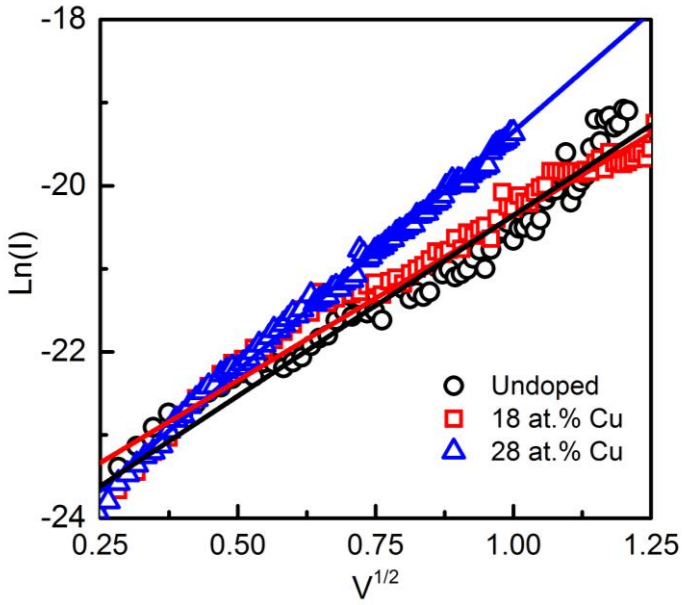

Figure 6-23 HRS I-V data of doped and undoped 1μm diameter device after +bipolar switching in Ln(I)-$V^{1/2}$ plots, with linear fittings to the Schottky emission equation.

The HRS I-V characteristics of doped and undoped 1μm diameter device after +bipolar switching in a Ln(I)-$V^{1/2}$ plots are shown in Figure 6-23. As discussed earlier, the higher than expected R_{OFF} values indicates the HRS conduction being interface limited, and the good linear fittings of HRS I-V data again strongly suggest a conduction mechanism dominated by Schottky emission. The HRS I-V data and fittings also almost overlap, showing the three devices have very similar Schottky barrier height. Using the method

discussed in Section 5.5, the Schottky barrier height of the two doped devices was found to be ~0.7eV.

6.2.5 Summary

In summary, three batches of Cu/a-SiC:Cu/Au devices were fabricated, with the Cu/a-SiC:0.21Cu/Au batch having quite low yield due to unsuccessful lift-off. The resistive switching behaviour of 1μm diameter Cu/a-SiC:0.18Cu/Au and Cu/a-SiC:0.28Cu/Au devices has been tested and the preliminary results shown in this section. Nonpolar switching behaviour has been observed in both batches. The R_{OFF} values are significantly higher than expected from the resistivity of co-sputtered a-SiC/Cu films, which suggests interface limited conduction mechanism. The analysis of HRS I-V confirms the conduction was dominated by Schottky emission and the barrier height of the doped devices is similar to the undoped devices. Overall the performance of doped devices are comparable to the undoped devices, with slightly improved ON/OFF ratio. The distribution of switching parameters of the Cu/a-SiC:0.18Cu/Au devices appears to be wider, the reason for which still requires further study. Future work is also needed for determining the optimal operation conditions of the doped devices, and possibly the optimal Cu content for optimal device performance. For a broad view, future work on the devices with a-SiC/Cu solid electrolytes may also help our understanding of the role of additional metal in solid electrolyte during the switching processes.

6.3 Influence of Counter Electrode

6.3.1 Fabricated Devices with W and TiN CE

As discussed in Section 2.1, one of the key requirements of the next generation non-volatile memory is the compatibility with conventional CMOS fabrication process. This requirement certainly applies to resistive memories. Although the Cu/a-SiC/Au RMs have shown some very promising performance, the Au counter electrode is not CMOS compatible. As discussed in Section 2.5, besides noble metals, tungsten and conductive nitrides were also often used as counter electrode in previous studies of RMs, because of their stability and CMOS-compatibility. In this project, two batches of Cu/a-SiC RM devices with sputtering deposited W and TiN as counter electrodes have also been fabricated and testing of switching behaviour has been performed on a small number of these devices. These results are presented in this section.

The Cu/a-SiC/W and Cu/a-SiC/TiN devices were also in the via-stack configuration, so the fabrication route and lithography mask discussed in Section 3.1 were used. The W and TiN thin films were deposited by sputtering deposition with a 99.999% W target and 99.99% TiN target, respectively. The obtained chips with the two batches of devices are shown in Figure 6-24. The TiN film appears to be in darker colour, and the lift-off process of that batch left some excessive Cu residue on the chip, as can be seen from the photo. Overall the fabrication process for the two batches was reasonably successful, as most devices appear intact under optical microscope of the probe station.

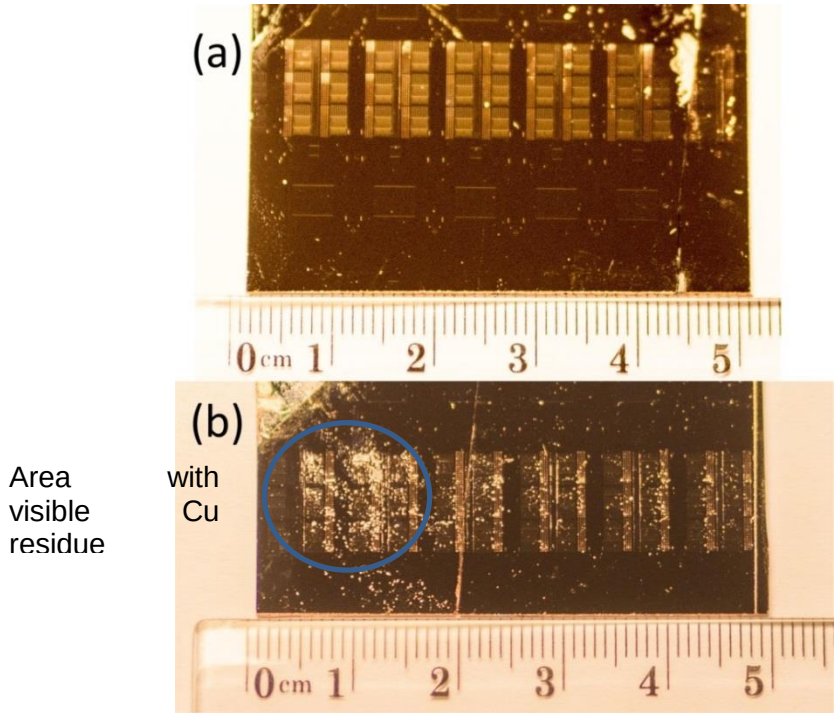

Figure 6-24 Photo of the chip with (a) Cu/a-SiC/W and (b) Cu/a-SiC/TiN RM devices.

6.3.2 +Bipolar and +Unipolar Switching of Cu/a-SiC/W RMs

+bipolar and +unipolar resistive switching behaviour have been observed in both Cu/a-SiC/W and Cu/a-SiC/TiN devices in the preliminary testing, as shown in Figure 6-25 to Figure 6-28. This suggests the potential of fully CMOS-compatible RMs based on Cu and a-SiC. Moreover, further choices of counter electrode material may also be worth exploring considering so far resistive switching has been observed in all batches of Cu and a-SiC based RMs with different counter electrodes.

Four consecutive +bipolar switching I-V curves observed in a 1μm diameter Cu/a-SiC/W device is shown in Figure 6-25. The SET voltage is around +1V and RESET voltage around

-1V. The R_{ON} and R_{OFF} values are in the same order of magnitude of that of Cu/a-SiC/Au devices shown in Chapter 5, and the ON/OFF ratio is also in the range of 10^8.

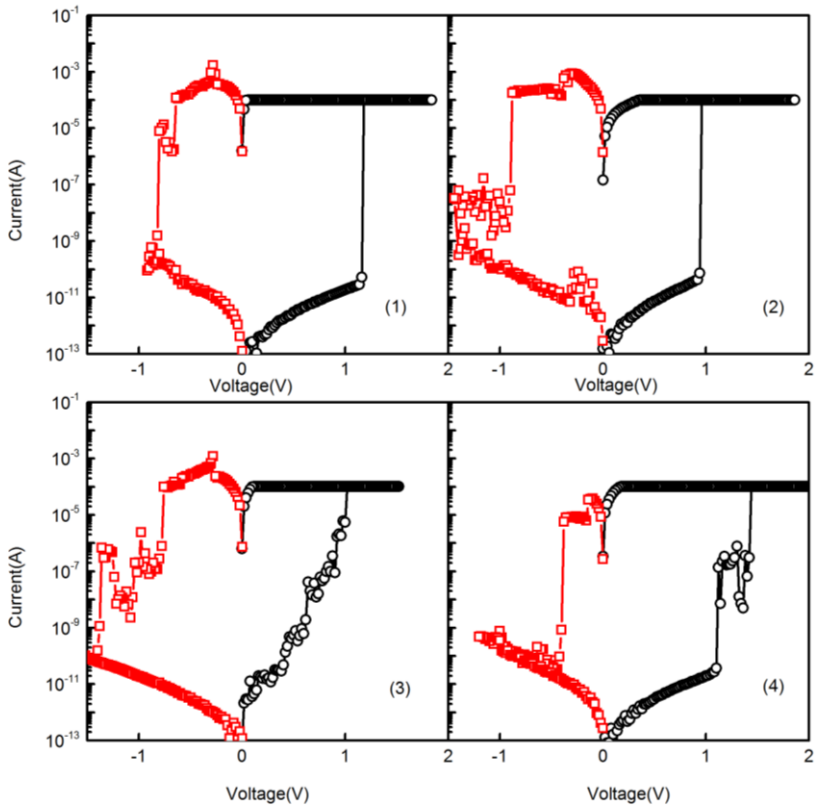

Figure 6-25 Four consecutive +bipolar switching cycles observed in a 1μm diameter Cu/a-SiC/W RM device.

+unipolar switching has also been observed in this batch of Cu/a-SiC/W devices, as shown in Figure 6-26. However compared to the Cu/a-SiC/Au devices, +unipolar switching in Cu/a-SiC/W devices appear to be less reliable, as abrupt increase and decrease of current may occur within a small range of applied voltage. In Figure 6-26, the current dropped from ~10^{-4}A to 10^{-12}A around +0.5V but immediately increased to 10^{-6}A at around +0.6V. This may be due to the competing process of filament formation/dissolution at positive bias. Nevertheless, further testing is still needed to verify the repeatability of +unipolar switching in Cu/a-SiC/W devices. In general, in +bipolar and +unipolar switching modes, the behaviour of Cu/a-SiC/W devices is not noticeably different from the Cu/a-SiC/Au devices, especially the R_{ON} and R_{OFF} values. This can be expected as the W and Au electrodes only act as simple resistors and are not involved in the resistive switching processes in these modes.

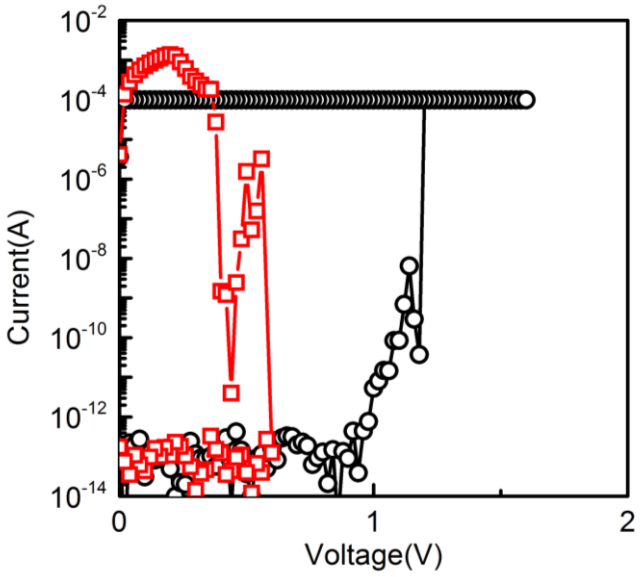

Figure 6-26 +unipolar switching cycles observed a 1μm diameter Cu/a-SiC/W RM device.

6.3.3 +Bipolar and +Unipolar Switching of Cu/a-SiC/TiN RMs

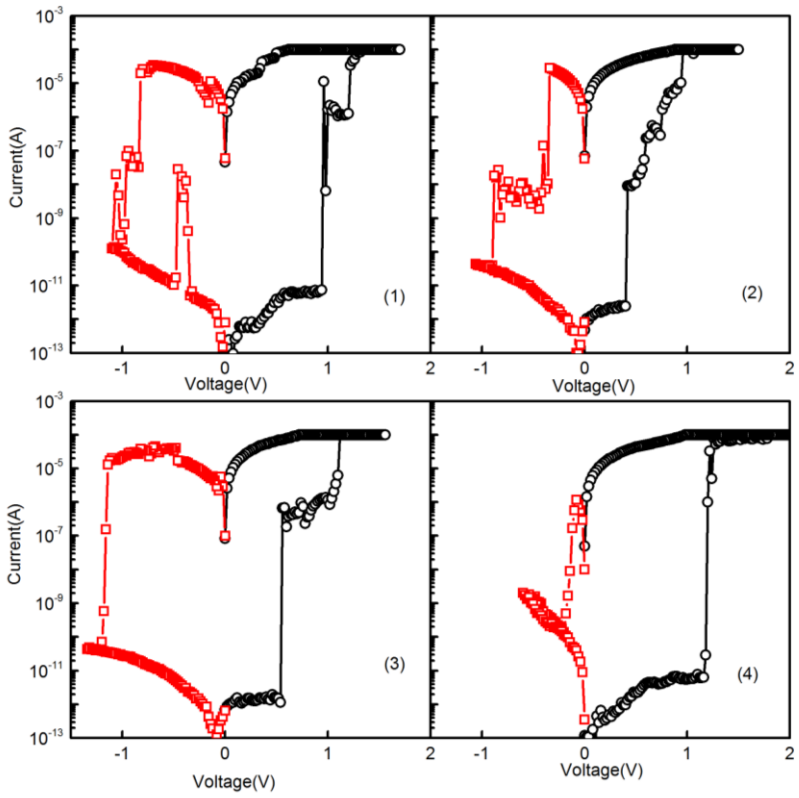

Figure 6-27 Four consecutive +bipolar switching cycles observed in a 1μm diameter Cu/a-SiC/TiN RM device.

The +bipolar switching of Cu/a-SiC/TiN devices, on the other hand, shows some noticeable differences compared to that of the Cu/a-SiC/W and Cu/a-SiC/Au devices. As shown in Figure 6-27, During the SET cycle, the current does not directly increase from ~10^{-11}A to

current compliance of 10^{-4}A, but increases from ~10^{-11}A to ~10^{-6}A and gradually reaches the current compliance. Also the R_{ON} is relatively higher as at around +1V the LRS current already drops below the compliance.

Most likely these differences are related to the higher resistivity of sputtered TiN film. Using Van der Pauw method, the resistivity of sputtered TiN film was found to be approximately 10^{-2} Ω•cm, while the resistivity of sputtered Au film is approximately 10^{-6}Ω•cm. As discussed in Chapter 5, the resistance of Au film between the device under test and the probe needle is negligible compared to the R_{ON} and R_{OFF} of devices. But for the Cu/a-SiC/TiN devices, resistance of TiN film may be in the range of 10^{3}~10^{4}Ω, which is comparable to the R_{ON} values of actual devices. As the measured resistance is the sum of the actual device resistance and the resistance of TiN film, high resistivity of TiN clearly set a higher limit of minimum R_{ON}. More importantly, the resistance of TiN film may serve as a serial resistor during SET process, so that current through device was not only limited by the current compliance but also by this additional resistance. The possible current over-shoot may therefore be avoided. With the current limited by TiN film during the initial SET, it's likely the initial filament was also limited in volume so that formation of multiple filaments or enhance of formed filament may occur before the current reaches compliance. As discussed in Chapter 2, such processes may appear as the multiple step SET shown in Figure 6-27. Moreover, with the additional resistance of TiN film, the 10^{-4}A current compliance that was suitable for the Cu/a-SiC/Au and Cu/a-SiC/W devices may not be the optimal value for the Cu/a-SiC/TiN devices. Further testing will be required to find the operation conditions for peak performance. It is also possible that the Cu/a-SiC/TiN devices may prove to be better choice for pulse-driven switching, as the resistance from TiN film may act as built-in serial resistor that may help prevent device breakdown during switching.

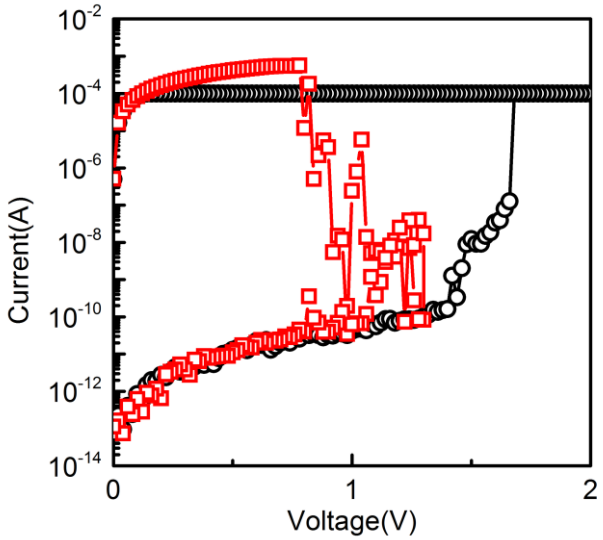

Figure 6-28 +unipolar switching cycles observed in a 1μm diameter Cu/a-SiC/TiN RM device.

+unipolar switching has also been observed in Cu/a-SiC/TiN devices, as shown in Figure 6-28. Similar to the Cu/a-SiC/W devices, there were also sudden fluctuations of current in the RESET cycle. This is also possibly related to the higher R_{ON}, which limited the Joule heating required for the positive RESET process. Again, further testing is necessary for a more complete evaluation of +unipolar switching in Cu/a-SiC/TiN devices.

Furthermore, -bipolar and –unipolar switching has been tested on both Cu/a-SiC/W and Cu/a-SiC/TiN devices, but repeatable switching has not been observed. The tested devices could be switched to LRS by negative bias, but the LRS could not be reversed by applying either positive or negative bias. So the apparent LRS was most likely permanent dielectric breakdown instead of resistive switching. This is consistent with the chemical stability of W and TiN electrodes reported in previous studies . This also suggests that –bipolar and –unipolar switching observed in Cu/a-SiC/Au devices is due to the Au electrode instead of resistive switching phenomenon within the a-SiC layer.

6.3.4 Distribution of Switching Parameters

The distribution of V_{SET}, V_{RESET}, R_{ON} and R_{OFF} in +bipolar mode from RM devices with Au, W and TiN counter electrodes is presented in Figure 6-29 and Figure 6-30. It can be seen that the V_{SET} values of devices with W and TiN counter electrodes are slightly lower than the ones with Au electrodes. And the distribution of V_{SET} and V_{RESET} of the W and TiN devices are noticeably wider than the Au devices. The ON/OFF resistance ratio of W and TiN devices are in the same order as the Au devices ($\sim 10^7$). Overall the results so far suggest

the switching repeatability of Cu/a-SiC/Au devices is slightly better than the Cu/a-SiC/W and Cu/a-SiC/TiN devices, however further testing is still required. On the other hand, in general these devices with three different electrodes have all shown relatively low voltage resistive switching behaviour with very high ON/OFF ratio. This suggests the combination of Cu and a-SiC can be reliably applied as functional material for resistive memories, and possibly further performance improvement can be achieved by exploring other counter electrode materials.

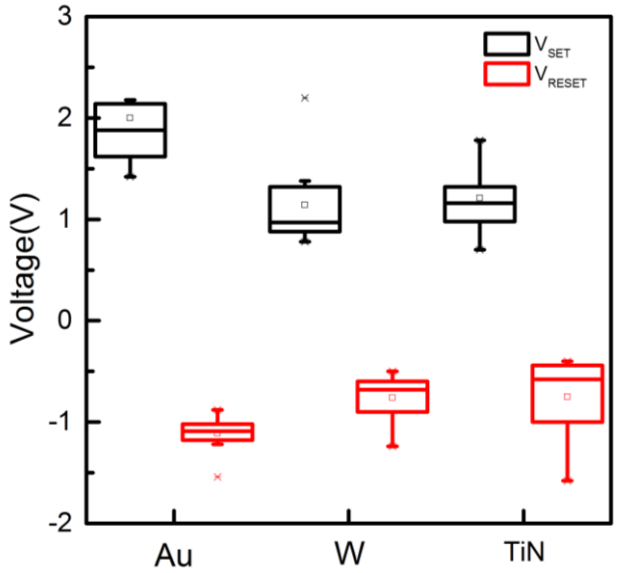

Figure 6-29 Distribution of V_{SET} and V_{RESET} in +bipolar mode from 1 μm diameter RM devices with different counter electrodes.

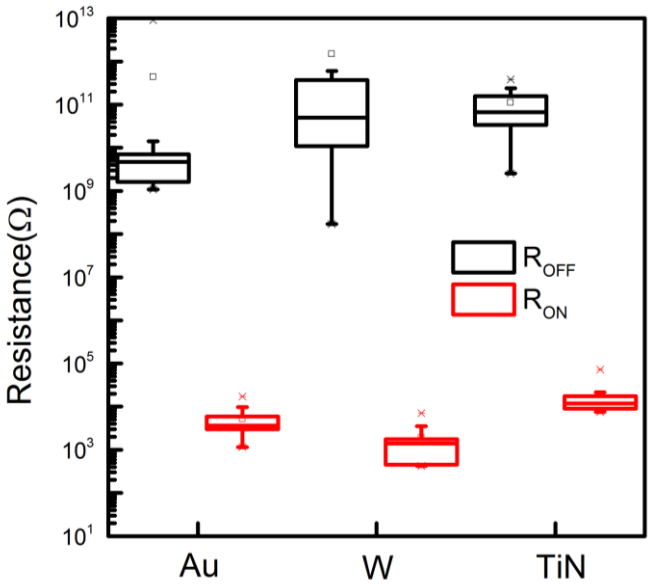

Figure 6-30 Distribution of R_{ON} and R_{OFF} in +bipolar mode from 1 μm diameter RM devices with different counter electrodes.

6.3.5 HRS Conduction Analysis

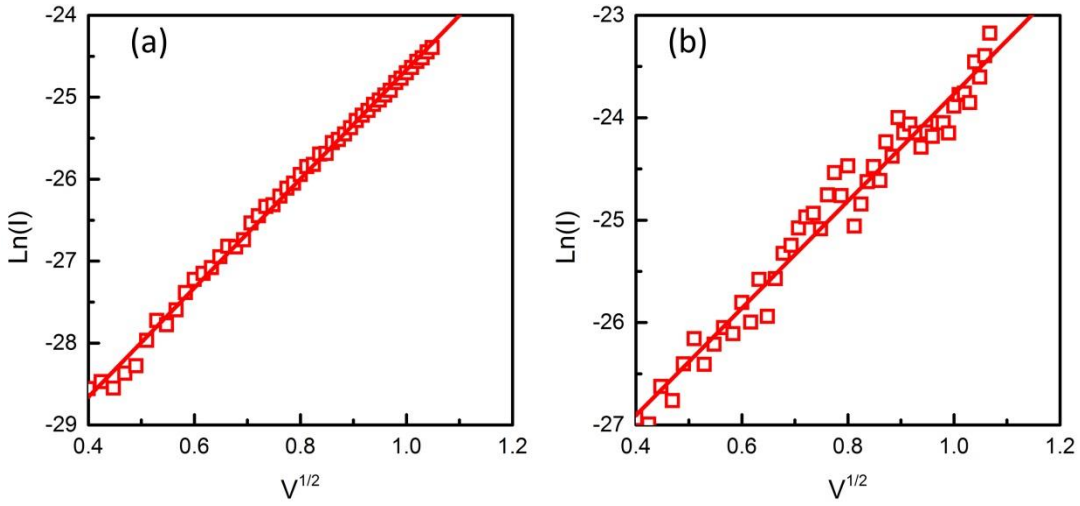

Figure 6-31 HRS I-V data of (a) Cu/a-SiC/W device and (b) Cu/a-SiC/TiN device in Ln(I)-$V^{1/2}$ plots, with linear fittings to the Schottky emission equation.

As Figure 6-31 shows, the HRS I-V data of W and TiN devices also fit the Schottky emission equation quite well, and the calculated Schottky barrier height is still in the range of 0.7eV~0.9eV, similar to the values of Cu/a-SiC/Au devices. This apparent independence of Schottky barrier height from the electrode material is in agreement with previous reports [145] that Schottky barrier between SiC and metals were only weakly related to the metal work function and more closely related to the deposition process of SiC film[145, 206]. This also indicates that such barrier is likely to exist in SiC contact with other counter electrode materials, and consequently similar high ON/OFF ratio can be expected.

6.3.6 Summary

In summary, Cu/a-SiC/W and Cu/a-SiC/TiN devices were fabricated and preliminary results of their resistive switching behaviour are presented in this section. Only +bipolar and +unipolar mode switching has been repeatedly observed in these devices, implying the –bipolar and –unipolar switching observed in Cu/a-SiC/Au devices was most likely due to the Au electrodes. The +bipolar switching behaviour of the Cu/a-SiC/W devices was quite similar to the Cu/a-SiC/Au devices, while the Cu/a-SiC/TiN devices exhibited higher R_{ON} and multi-step switching, probably due to the high resistivity of sputtered TiN film.

6.4 Summary

In summary, several batches of RM devices based on Cu and a-SiC with different device structure, solid electrolyte and counter electrode material were fabricated and tested in

order to study the possible influence of these factors on the device switching behaviour. Resistive switching behaviour has been observed in all these batches, with each batch showing certain unique features in their switching behaviour. The most notable ones are: The cross-bar structured devices could sustain higher current compliance during SET, which led to lower R_{ON} and ON/OFF ratios. The devices based on a-SiC/Cu solid electrolytes also showed reduced R_{ON} but also more fluctuations in the HRS current and wider distribution of switching parameters. The Cu/a-SiC/TiN devices exhibited higher R_{ON} and multi-step switching. The possible causes of these features were briefly discussed in this chapter, but more future work is needed for better understanding of these phenomena. Also more testing is needed to get a more complete picture of switching performance of these devices. Overall, it's worth noticing that all these devices based on Cu and a-SiC with different structure and material configurations have shown repeated resistive switching behaviour. This suggests the potential of Cu and a-SiC based RMs functioning with other structures and material configurations, which may be worth exploring in future work.

Chapter 7. Conclusion and Future Work

7.1 Conclusion

In conclusion, as Flash memory is approaching physical scaling limit, there is great interest in the research of the next generation non-volatile memory. In addition to replacing Flash memory in data storage applications, the next generation non-volatile memory is also expected to have improved performance, especially more cycle endurance and faster read/write operation, so that it may eventually be the “universal" memory that also replaces volatile memory such as DRAM. Resistive memory is widely considered to be the overall most promising emerging non-volatile memory.

This project focused on Cu/a-SiC RMs primarily because of the recent report of excellent retention and stabilities of such RMs, which was believed to be due to the advantageously low Cu diffusion rate in SiC.

Material properties, namely chemical composition, structural properties and electrical conduction properties of the sputtering deposited a-SiC and a-SiC/Cu solid electrolytes were firstly analysed in this project. This project has then developed Cu/a-SiC RMs with via-stack and crossbar structures, with a-SiC and a-SiC/Cu as solid electrolytes and Au, W and TiN as counter electrodes. The switching characteristics of the obtained devices have then been thoroughly investigated.

The deposited SiC films are of amorphous structure, with Si to C ratio close to 1, and have very high resistivity of $7.66 \times 10^7 \Omega \cdot \text{cm}$. All these properties are suitable for the intended application as solid electrolyte material for resistive memories. As for the a-SiC/Cu films, the added Cu remains metallic and the Cu particle size is below 3nm. Films with higher Cu percentage also exhibit larger grain size, which may lead to more porous films and lower dielectric constant. The added Cu also greatly reduced the resistivity of a-SiC/Cu films, which may be undesirable for the application in resistive memory.

In the obtained Cu/a-SiC/Au via stack devices, nonpolar switching was observed with high ON/OFF ratios in the range of $10^6 \sim 10^8$ for all four modes. Detailed I-V characteristics analysis suggests that the conduction mechanism in LRS is due to the formation of Cu or Au filaments. Schottky emission is proven to be the dominant conduction mechanism in HRS which results from the Schottky contacts between the metal electrodes and SiC. As for

the rupture of the filaments in the RESET processes, in +bipolar mode electrochemical reaction is likely to dominate while Joule heating accelerated diffusion appears to be involved in all other three modes.

Furthermore, all devices based on Cu and a-SiC with different structure and material configurations have shown repeated resistive switching behaviour, with each batch showing certain unique features in their switching behaviour. Compared to the Cu/a-SiC/Au via-stack devices, the cross-bar structured devices could sustain higher current compliance during SET, which led to lower R_{ON} and higher ON/OFF ratios. The devices based on a-SiC/Cu solid electrolytes also showed reduced R_{ON} but also more fluctuations in the HRS current and wider distribution of switching parameters. Only +bipolar and +unipolar switching were repeatedly observed in the Cu/a-SiC/TiN and Cu/a-SiC/W devices, which supports that nonpolar switching in the Cu/a-SiC/Au devices is most likely due to the Au electrodes. The Cu/a-SiC/TiN also devices exhibited higher R_{ON} and multi-step switching, likely due to the high resistivity of sputtering deposited TiN film.

7.2 Future Work

Future research on a-SiC based RMs can potentially be carried out in a number of directions: Firstly, pulse-driven switching test is essential to establish the switching speed and cycle endurance of a-SiC based RMs. The challenge of such test mostly lies in setting a current compliance during pulse-driven switching. The most common method is to attach a serial resistor to the RM, which may require wire-bonding process. Secondly, RMs based on a-SiC/Cu solid electrolytes showed relatively limited alteration in switching behaviour compared to a-SiC based RMs, despite that the resistivity of a-SiC/Cu was significantly lower. This may be related to the distribution of Cu particles in the a-SiC matrix, and further investigation may be worthwhile to improve the Cu doping method. Thirdly, as discussed in Chapter 6, switching behaviour of the Cu/a-SiC/TiN may worth further study, as the high resistance of TiN electrode may serve as serial resistor that can limit current through RM during pulse-driven switching. Finally, considering that so far all devices based on Cu and a-SiC with different structure and material configurations have shown repeated resistive switching behaviour, other structures and material configurations may also be worth exploring in future work, especially the complementary structure that can eliminate sneak current in crossbar RM array.

List of Publications

- **Journal Publications:**

1. **Zhong, L.**, Jiang, L., Huang, R., & de Groot, C. H. (2014). Nonpolar resistive switching in Cu/SiC/Au non-volatile resistive memory devices. *Applied Physics Letters*, 104(9), 5

2. **Zhong, L.**, Reed, P. A., Huang, R., de Groot, C. H., & Jiang, L. (2014). Resistive switching of Cu/SiC/Au memory devices with a high ON/OFF ratio. *Solid-State Electronics*, 94(0), 98-102.

3. **Zhong, L**., Reed, P. A., Huang, R., de Groot, C. H., & Jiang, L. (2014). Amorphous SiC based non-volatile resistive memories with ultrahigh ON/OFF ratios. *Microelectronic Engineering*, 119(0), 61-64.

4. Jiang, L., **Zhong, L.**, Fan, J., Huang, R. & de Groot, C. H. Microstructure and electrical properties of co-sputtered amorphous SiC:Cu composites. In preparation, to be submitted to *Materials Letters*.

- **Conference Publications:**

1. **Zhong, L.**, Reed, P. A., Huang, R., de Groot, C. H., & Jiang, L. (2013) Amorphous SiC Based Non-Volatile Resistive Memories With Ultrahigh OFF/ON Resistance Ratios. In: 39th International Conference on Micro and Nano Engineering (Invited Talk).

2. **Zhong, L.**, Jiang, L., Reed, P. A., Huang, R., & de Groot, C. H., (2013) Resistive Non-Volatile Memories Based on Amorphous SiC. In: 7th International Conference on Materials for Advanced Technologies.

3. **Zhong, L.**, Jiang, L., Reed, P. A., Huang, R., & de Groot, C. H., (2014) Resistive Non-Volatile Memories Based on Amorphous SiC. In: 2014 Materials Research Exchange.

4. **Zhong, L.,** Fan, J., Reed, P. A., Jiang, L., Huang, R., Morgan, K., and de Groot, C. H. (2014). Pulsed resistive switching of amorphous SiC memory devices with a high ON/OFF ratio. Submitted to 2014 MRS Fall Meeting & Exhibit.

5. Jiang, L., **Zhong, L.**, Reed, P. A., Taysir, S., Bosi, M., & Attolini, G. (2013, March).

Electrical characterisation of epitaxially grown 3C-SiC films. In Materials Science Forum (Vol. 740, pp. 617-620).

Appendix

APPLIED PHYSICS LETTERS **104**, 093507 (2014)

Nonpolar resistive switching in Cu/SiC/Au non-volatile resistive memory devices

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(Received 4 December 2013; accepted 13 February 2014; published online 4 March 2014)

Amorphous silicon carbide (a-SiC) based resistive memory (RM) Cu/a-SiC/Au devices were fabricated and their resistive switching characteristics investigated. All four possible modes of nonpolar resistive switching were achieved with ON/OFF ratio in the range 10^6–10^8. Detailed current-voltage I-V characteristics analysis suggests that the conduction mechanism in low resistance state is due to the formation of metallic filaments. Schottky emission is proven to be the dominant conduction mechanism in high resistance state which results from the Schottky contacts between the metal electrodes and SiC. ON/OFF ratios exceeding 10^7 over 10 years were also predicted from state retention characterizations. These results suggest promising application potentials for Cu/a-SiC/Au RMs. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4867198]

Conventional Si charge-storage-based non-volatile memories are running into serious limitations as further down-scaling leads to difficulties in retaining reliable performance.[1] In recent years, this dilemma has triggered great interest and development of resistance random access memory for next generation non-volatile memory due to its promising performance and potentials including down-scalability, excellent endurance, simple structures, fast speed, low power consumption, and back-end of line compatibility.[2] A resistive memory (RM) usually consists of an insulating or semiconducting material which is sandwiched between two metal electrodes. Reversible resistive switching is modulated by applying a voltage across the metal electrodes to achieve the transition from high (HRS) to low (LRS) resistance state (SET) or the transition from LRS to HRS (RESET). Resistance of device at LRS and HRS are often noted as R_{ON} and R_{OFF}, respectively.

A number of RMs has been reported with resistive switching behaviour. Based on current-voltage (I-V) characteristics, the switching modes can be classified into three main types: unipolar, bipolar, and nonpolar. Unipolar resistive memories refer to RMs which can be SET and RESET by applying voltages with the same polarity, while bipolar RMs require opposite voltage polarities to SET and RESET for each switching cycle. A typical bipolar RM usually contains two different electrodes as one is electrochemically active and the other is inert.[2] This is to enable the voltage polarity dependant filamentary formation during SET and rupture during RESET based on electrochemical reaction in the middle solid electrolyte layer.[3,4] On the other hand, the same metal is generally used for both electrodes in a typical unipolar RM to enable SET/RESET under the same voltage polarity.[5,6] Relatively speaking, bipolar switching features faster switching speed, better uniformity, and lower operation power,[7] while unipolar switching presents higher ON/OFF ratios (R_{OFF}/R_{ON}) and presents advantages for high density integration.[8] Thus nonpolar RMs which exhibit both unipolar and bipolar switching behaviours have been considered advantageous as they can potentially expand application scopes of RMs.[9] It is worth noting that there can be two possible bipolar switching modes in one device which can be defined as positive bipolar achieved by positive SET voltage (V_{SET}) followed by negative RESET voltage (V_{RESET}) and negative bipolar achieved by negative V_{SET} followed by positive V_{RESET}. Similarly two possible unipolar switching modes can exist in one device which can be defined as positive unipolar (positive V_{SET} followed by positive V_{RESET}) and negative unipolar (negative V_{SET} followed by negative V_{RESET}). Nonpolar devices ideally should present all these four possible switching modes.

Only a limited number of nonpolar RMs have been reported to present all four possible switching modes. Most of them are transition metal oxide based RMs[4,5] or insulating material based RMs with metal dopants or particles embedded in the switching layers.[6,8] However, introduction of dopants into the switching layers can reduce the resistance in HRS, leading to limited ON/OFF ratios.[10] Furthermore, despite of different device configurations, most reported nonpolar RMs are attributable to the same conductive filaments when subject to positive V_{SET} or negative V_{SET}, hence similar resistant states, i.e., R_{ON}, R_{OFF}, and switching ratios were observed.[5,8] For example, positive bipolar and negative bipolar switching performance can be similar or symmetric.[6] If the change of polarity could also induce asymmetric switching performance such as R_{ON}, R_{OFF}, and switching ratios, this may be further exploited to expand the potential programmable range of future RMs.

Amorphous silicon carbide (a-SiC) based RMs has recently been reported to show very promising resistive switching behaviours.[3,11] Our previous results also suggest that ultrahigh switching ratios in the range of 10^8–10^9 can be achieved.[12] In this paper, we report a-SiC based RMs which exhibit nonpolar switching characteristics, high ON/OFF ratios, and excellent retention performance. Asymmetric bipolar and unipolar switching behaviours are investigated based

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on the formation and rupture of conductive filaments in all four switching modes.

Cu/a-SiC/Au RM cells were fabricated on Si wafers covered with a 1 μm thick thermal SiO_2 layer. 300 nm Au was deposited by magnetron sputtering followed by the deposition of a 250 nm thick SiO_2 layer. Photolithography and reactive ion etching were then conducted to pattern and expose the active device areas. Subsequently, 40 nm thick a-SiC and 300 nm thick Cu layers were deposited without breaking the sputtering chamber vacuum on the patterned substrates. A final lift off process was used to achieve the Cu/a-SiC/Au RM devices. All processes were conducted at room temperature. I-V characteristics were measured by voltage sweeps using an Agilent B1500A semiconductor device parameter analyser. All voltage sweeps were conducted by grounding the Au electrode while applying polarized voltages on the Cu electrode. A current compliance of 100 μA was applied for all SET switching process, and no compliance current was applied during RESET. A cross-section view of a typical device and the schematic of voltage application are shown in the inset of Figure 1(d).

Material composition of the as-deposited a-SiC has been characterised by X-ray photoelectron spectroscopy (XPS). Figures 1(a) and 1(b) show that Si 2p and C 1s peaks are at 100.7 eV and 283.3 eV, respectively, which corresponds to stoichiometric a-SiC.[13] High resolution X-ray diffraction (XRD) spectra have been obtained from both the SiC sputtering target as well as as-deposited SiC layer, as shown in Figure 1(c). The characteristic 3C-SiC (111) XRD peak at 35.7° (Ref. 14) is clearly observed from the SiC target, while no peaks are shown from the as-deposited SiC layer, suggesting amorphous status of the as-deposited SiC. Furthermore, by analysing the capacitance of pristine Cu/a-SiC/Au devices with varied device areas, as shown in Figure 1(d), dielectric constant ε and refractive index n of the a-SiC layer can also been estimated to be 6.5 and 2.55, respectively, which also corresponds to C/Si ratio of 1.[15]

To avoid any possible influence from switching history, in this work, each of the four switching mode i.e., positive bipolar (+bipolar), negative bipolar (−bipolar), positive unipolar (+unipolar), negative unipolar (−unipolar) was conducted using a pristine Cu/a-SiC/Au device with identical device structures, i.e., each device has only been tested using its respective switching mode. In order to ensure the uniformity of the device performance, at least five identical devices have been measured for each switching mode, and for each switching device, at least 20 cycles have been conducted. All four switching characteristics have been observed over a range of devices, respectively, which have also shown reliability over repeated switching cycles (not shown here). As the starting state of pristine Cu/a-SiC/Au RMs is always HRS, a first electroforming process is observed for all these switching mode to obtain the initial LRS with the forming voltage in the range of 4–5 V, as shown in Figures 2(a) and 2(b). Higher forming voltage for a pristine device as in contrast to V_{SET} in the subsequent SET and RESET cycles has been frequently observed in many RMs, which is attributed to the requirement to induce the

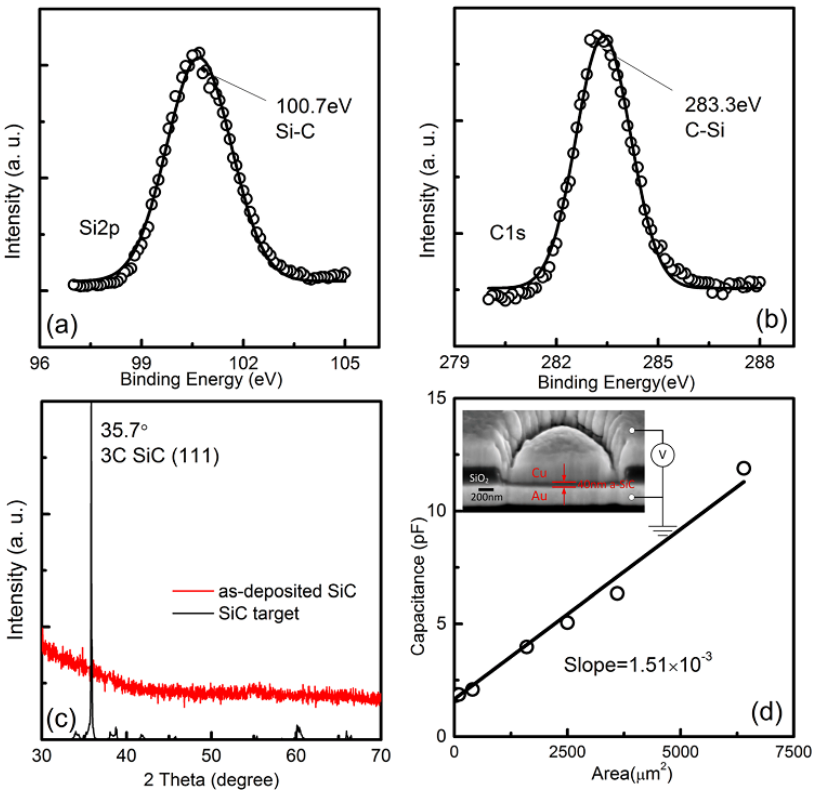

FIG. 1. (a) Si 2p and (b) C 1s XPS spectra of as-deposited a-SiC film, with peak binding energy labelled. (c) XRD spectra of SiC sputtering target and as-deposited a-SiC film. (d) Capacitance of pristine Cu/a-SiC/Au devices with varied device area. The inset shows the cross-section of a typical device with a schematic indication of electric connection configuration for the switching tests.

conductive paths through the entire thickness of the device layer.[16] Typical I-V characteristics of the stable switching cycles of the Cu/a-SiC/Au devices with 1 μm^2 device area are also shown in Figures 2(c) and 2(d), presenting all four unipolar switching modes, respectively. It is observed that typical V_{SET} and V_{RESET} are around or below 2 V. It is worth noting that, high switching ratios in the range of 10^6–10^8 were obtained for all four modes. Asymmetric switching performances between positive bipolar and negative bipolar cycles as well as between positive unipolar and negative unipolar cycles are observed. For instance, switching ratios for negative bipolar and negative unipolar are approximately two orders of magnitude higher than positive bipolar and positive unipolar modes, respectively.

To investigate the switching mechanisms, detailed I-V characteristics for LRS and HRS are plotted in Figure 3. Straight lines with slope of approximately unity are obtained for all LRS in a double logarithmic plot (Figure 3(a)), which indicates Ohmic conduction, most likely due to filamentary conduction.[2] It is believed that, when the device is subject to an applied electrical field during SET process, conductive filaments are formed by redox reaction of the electrochemically active metal electrode followed by ion migration and deposition within the insulating layer. For the herein reported Cu/a-SiC/Au devices, when positive voltage is applied to the Cu electrode, i.e., SET processes for positive bipolar and positive unipolar modes, Cu atoms are oxidized to Cu^{z+} ions which migrate through the a-SiC layer and subsequently reduce to Cu atoms at the Au counter electrode and eventually form Cu filaments. Cu as an electrochemically active material has been widely used in many RMs[2–4,11] with real time observation of Cu filaments observed using high resolution transmission electron microscopy (TEM).[17] In comparison with Cu, Au has a much higher reduction potential[18] and thus has mainly been used as inert counter electrodes in RMs.[19] Nevertheless, real time TEM observation of Au filaments has been recently reported.[20] For our Cu/a-SiC/Au devices, when negative voltage is applied to the Cu electrode during SET process, i.e., negative bipolar and negative unipolar modes, the Au electrode is subject to a positive electrical field where, we believe, Au atoms can be oxidized to Au^+ ions which reduce to Au atoms at the Cu counter electrode and thus form Au conductive filaments. To further clarify these conduction mechanisms, Figure 4 shows R_{ON} as a function of temperature. As expected, metallic behaviour is observed for the LRS resistance for both positive (R_{ON+}) and negative (R_{ON-}) switching modes. Through linear fitting, the temperature coefficient of R_{ON+} and R_{ON-} are extracted to be 2.4×10^{-3} K^{-1} and 2.7×10^{-3} K^{-1}. These values are in agreement with reported values for Cu nanowires (2.5×10^{-3} K^{-1})[21] and Au nanowires (2.3×10^{-3} K^{-1}),[22] respectively. These results also discard the possibility of any oxygen vacancy conduction

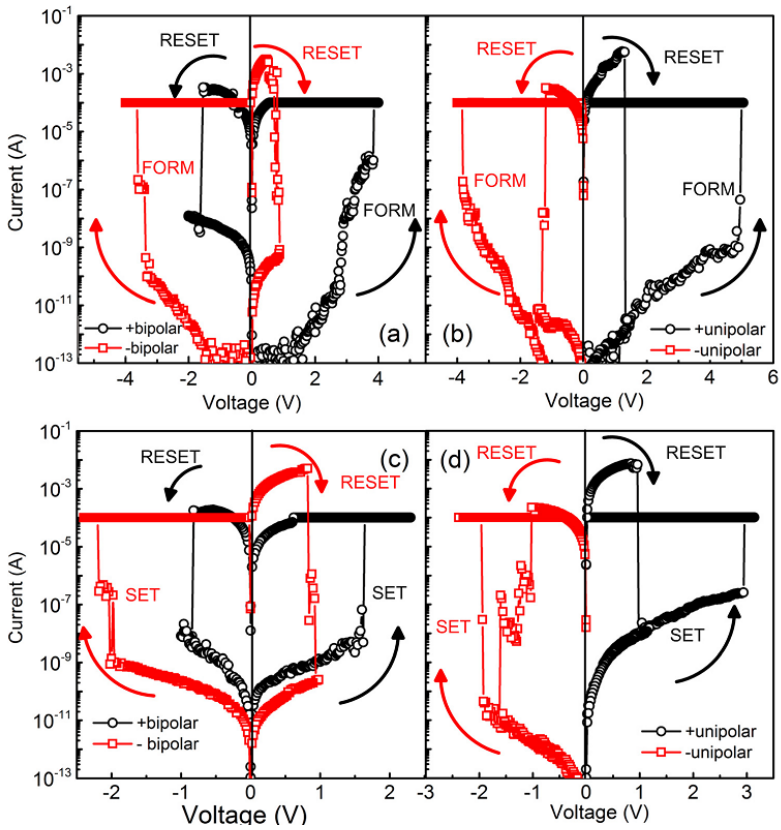

FIG. 2. I-V curves of electroforming cycles and typical switching cycles of all four possible switching modes: (a) electroforming cycles of +bipolar and −bipolar modes, (b) electroforming cycles of +unipolar and −unipolar modes, (c) typical switching cycles of +bipolar and −bipolar modes, (d) typical switching cycles of +unipolar and −unipolar modes. The arrows indicate the respective voltage sweeping directions.

as its temperature coefficient should be at least an order of magnitude smaller than metal filaments.[23]

Figure 3(b) shows the HRS I-V characteristics of all the four switching modes which can be explained by Schottky Emission mechanism following:[24]

$$I = AA^*T^2 \exp\left[\frac{-q\Phi_B}{kT} + \frac{q\sqrt{q/4\pi\varepsilon_i}}{kT}\sqrt{E}\right], \quad (1)$$

where A is the conduction area, A^* is Richardson's constant, Φ_B is Schottky Barrier Height (SBH), E is electrical field, q is the electronic charge, k is the Boltzmann's constant, ε_i is dielectric constant of the film, and T is absolute temperature. This is expected as SiC have been widely exploited for Schottky diode applications.[25] The existence of Schottky contacts between the metal electrodes and a-SiC in this case is advantageous for Cu/a-SiC/Au RMs as it contributes to the high R_{OFF}, leading to high switching ratios. Furthermore, it is observed that the R_{OFF} values for negative bipolar and negative unipolar modes are over an order of magnitude higher than positive bipolar and positive unipolar modes, respectively. This is probably due to the higher work function of Au nanowires in the negative bipolar and negative unipolar modes in comparison with Cu nanowires in positive bipolar and positive unipolar modes, which leads to higher

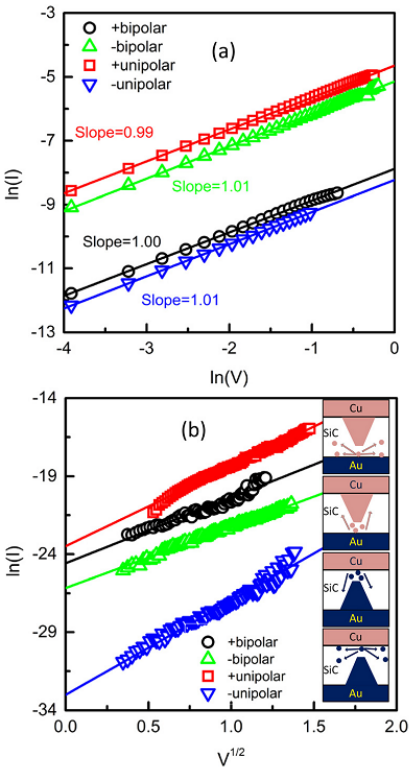

FIG. 3. (a) LRS I-V data in Ln(I)-Ln(V) plots, with respective linear fittings. (b) HRS I-V data in Ln(I)-$V^{1/2}$ plots, with linear fittings to the Schottky emission equation. The insets illustrate the possible RESET mechanisms for each switching mode: +unipolar, +bipolar, −bipolar, and −unipolar in top-down sequence.

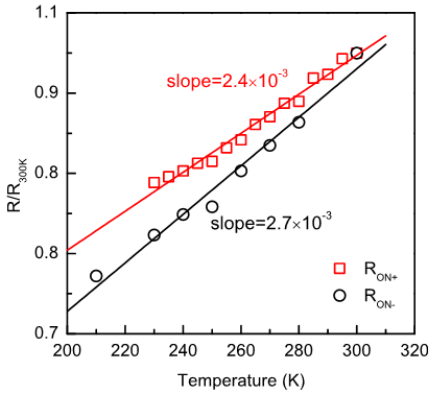

FIG. 4. Normalized R_{ON} values versus temperature, with the straight lines being their respective linear fittings.

Φ_B when in contact with a-SiC in HRS. Rupture of the conductive filaments has been reported to underpin the RESET process. We believe that in our Cu/a-SiC/Au devices, electrochemical dissolution of the metal filaments plays the dominant role in bipolar switching,[2] while Joule heating enhanced lateral diffusion dominates RESET in unipolar switches. The fact that our devices have clearly demonstrated stable resistive switching when Cu and Au electrodes are subjected to positive electrical fields suggest that the Au electrode is not only inert enough to enable positive bipolar and positive unipolar switching cycles but also active enough to allow negative bipolar and negative unipolar switching behaviours. Furthermore, both Cu and Au have very low diffusion coefficients in SiC,[26,27] suggesting Cu or Au ions are apt to be reduced before they reach their respective counter electrode and thus result in a cone-shaped filament with the narrowest point near the counter electrode.[15,28] We thus believe that the rupture of the filaments for Cu/a-SiC/Au RMs is likely to occur at this narrowest point, as insets in Figure 3(b) illustrate the possible RESET mechanisms for each switching mode.

Figure 5 shows the retention performance of R_{ON} and R_{OFF} states. There is no noticeable deterioration over the

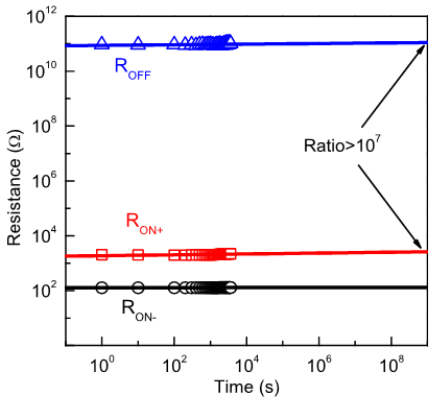

FIG. 5. R_{ON} and R_{OFF} values versus time measured at 85 °C, with power law extrapolation to 10 years.

measurement duration at 85 °C. The power-law extrapolation[29] suggests that the ON/OFF switching ratio after 10 years can still be expected to be greater than 10^7, implying excellent stability and retention of these devices. This might be attributable to the high chemical stability of SiC material as well as the low Cu and Au diffusion in SiC.[26,27] As a result, these a-SiC based RMs using Cu and Au electrodes demonstrate significant advantages and potential for future applications.

In summary, Cu/a-SiC/Au devices with nonpolar resistive switching characteristics are obtained and analysed. All four possible switching modes are present with asymmetric switching performance, such as R_{ON}, R_{OFF}, and switching ratio between positive bipolar and negative bipolar modes as well as between positive unipolar and negative unipolar modes. Detailed I-V characteristics analysis suggests that the conduction mechanism in LRS is due to the formation of Cu or Au filaments. Schottky emission is proven to be the dominant conduction mechanism in HRS, which results from the Schottky contacts between the metal electrodes and SiC. The rupture of the filaments in the RESET process is likely to be attributable to electrochemical dissolution for bipolar modes and Joule heating assistant diffusion for unipolar modes. The combination of Cu and Au as electrodes in the a-SiC RM has proven to be effective in enabling all four possible nonpolar switching modes. The Cu/a-SiC/Au devices also show excellent retention performance. These results suggest promising application potentials for Cu/a-SiC/Au RMs.

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Solid-State Electronics 94 (2014) 98–102

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Resistive switching of Cu/SiC/Au memory devices with a high ON/OFF ratio

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ARTICLE INFO

Article history:
Received 3 October 2013
Received in revised form 24 January 2014
Accepted 27 February 2014

The review of this paper was arranged by Y. Kuk

Keywords:
Resistive memory
Amorphous silicon carbide
Conduction mechanism

ABSTRACT

Resistive memories (RMs) using amorphous SiC (a-SiC) as the solid electrolyte material have been developed with a Cu/a-SiC/Au stack configuration. Excellent non-volatile bipolar switching characteristics have been observed. An extremely high ON/OFF current ratio in the order of 10^9 has been observed corresponding to distinctive low (LRS) and high (HRS) resistance states, which is potentially beneficial for future RM applications with reliable state detection and simple periphery circuits. The deposited a-SiC has been extensively characterised for its micro/nanostructures, chemical composition as well as electrical properties. The switching mechanism is investigated through detailed analysis of corresponding *I–V* curves. The results imply a filamentary conduction mechanism at LRS and Schottky emission mechanism at HRS, especially in the subsequent switching cycles. The contrasting conducting material properties and mechanisms at LRS and HRS contribute to the high ON/OFF ratio. Overall, Cu/a-SiC based RMs demonstrate a number of high performance potentials.

1. Introduction

Non-volatile memory cells based on resistive switching have attracted considerable interest in recent years due to their significant potential to replace both conventional non-volatile memory (e.g. Flash memory) and volatile memory (e.g. Dynamic Random Access Memory). Resistive memories (RMs) offer promising properties such as fast switching speed, low power consumption, long retention lifetime and excellent down-scalability, leading to multi-bit data storage with high density [1,2]. A RM also presents a simple device structure which usually consists of a solid electrolyte material sandwiched between two metal electrodes. ON and OFF states correspond to a low (LRS) and a high (HRS) resistance state, respectively. Generally speaking, a pristine device starts in the HRS. A subsequently applied electrical bias can induce a reversible transition from HRS to LRS. For most reported RMs, it is observed that conductive paths are formed from mobile species within the electrolyte active layer, which accounts for the low resistance R_{ON} at LRS. Depending on the mobile species in the electrolyte layer, RMs can be classified to be anion based (e.g. oxygen anions) and cation based (e.g. metal cations) devices [3]. Cation based devices are often called electrochemical metallization memory, or programmable metallization cells, which usually have an active electrode made from an electrochemically active material such as Cu [4], Ag [5] and a counter electrode made from electrochemically inert metals e.g. Pt [6], Au [7]. Cation based devices have generated promising results as next generation memory devices while retention is still a main challenge [3]. Material properties of the solid electrolyte are directly linked to the corresponding switching performance. Ease of integration of these materials with CMOS technology is also a practical consideration to ensure future low cost memory fabrication and for integration with essential logic circuitries.

Among a number of solid electrolyte materials reported for RMs including sulphides [8], chalcogenides [9], oxides [4], amorphous materials [6], Si based amorphous materials such as amorphous Si [10] or SiO_2 [11] have attracted particular interest for their CMOS fabrication compatibility as well as their potential as non-volatile memory alternatives in terms of low-power switching, speed, retention, and endurance. However, instability and poor retention characteristics are key drawbacks for these devices. Amorphous SiC (a-SiC) as a new electrolyte material has been recently reported [12] to show excellent retention and stabilities due to the advantageously low Cu diffusion rate in SiC [13]. However, these reported Cu/a-SiC based RMs [12] exhibit relatively low ON/OFF current ratio (equivalent to R_{OFF}/R_{ON} at 0.1 V) in the order of 10^2 between the two states. As one of the key performance

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http://dx.doi.org/10.1016/j.sse.2014.02.013
0038-1101/

attributes for any RMs, high ON/OFF ratios present great advantages in future applications as it not only enables fast and reliable detection of the states of memory cells, but also simplifies the periphery circuit to distinguish the storage information [14,15]. Furthermore, with this only report [12] on Cu/a-SiC RMs focusing on the studies of retention and stability properties, in-depth studies in the switching mechanism are still required.

This work focuses on the study of Cu/a-SiC/Au RMs. Typical bipolar resistive switching characteristics have been observed with ultrahigh ON/OFF ratios ($\sim 10^9$) and excellent retention. *I–V* transport properties for both LRS and HRS have been studied in detail with a view to investigating respective conduction and switching mechanisms.

2. Experiment

Crossbar structures present the highest possible device density and the simplest interconnect configuration for future memory applications [16]. In this work, all Cu/a-SiC/Au RMs are designed in crossbar configuration and fabricated at room temperature. Si wafers covered with 1 μm thick thermal SiO_2 were used as substrates. A 300 nm thick Au layer was deposited on the substrates using DC sputtering followed by a photolithographic lift off process to achieve a patterned Au bottom counter electrode. Subsequently, a 35 nm thick a-SiC active layer followed by 300 nm Cu as top active electrodes were deposited using RF and DC sputtering, respectively, without breaking the vacuum in the sputtering chamber. This is to minimize possible contamination between Cu and a-SiC when exposed to ambient environment. A final lift off process was conducted to obtain the Cu/a-SiC/Au resistive memory cells. All sputtering deposition processes were carried out using Ar gas, with chamber pressure $<1 \times 10^{-6}$ mbar before deposition and 5×10^{-3} mbar during deposition. Fig. 1(a) shows a top view of a typical device using a scanning electron microscope (SEM). A cross section view of the device active region in the crossbar area was prepared and observed by using Focused Ion Beam (FIB) milling processes, as shown in Fig. 1(b). All Cu/a-SiC/Au RMs have an active crossbar device area of 25 μm^2 (5 μm × 5 μm).

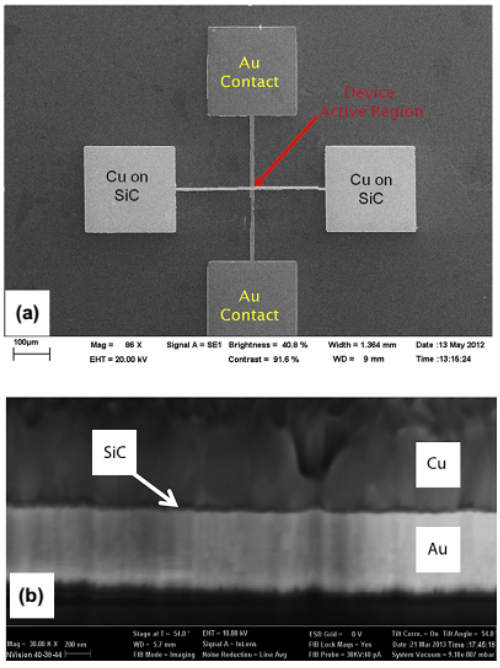

Fig. 1. (a) Top-view SEM image of a cross bar structure Cu/a-SiC/Au RM device. The intersection of the two bars is the device active region. The bars are connected to their respective contact pads. (b) FIB cross-section of the device active region as indicated by the arrow in (a).

Current–voltage (*I–V*) characteristics of the Cu/a-SiC/Au devices were measured by sweeping the voltage across the Cu and Au electrodes using an Agilent B1500A semiconductor parameter analyser. The sequence of each voltage sweep is 0V → +V → 0V → −V → 0V to obtain the SET (HRS to LRS) and RESET (LRS to HRS) cycles, while the first sweep cycle for a pristine device is denoted as the initial electroforming cycle. The voltage polarity is denoted by the voltage applied on the Cu electrode while Au electrode was grounded, i.e. +V denotes Cu as anode and vice versa. During SET cycles, a current compliance of 10 mA was adopted to avoid permanent dielectric breakdown of the device; while no current compliance was employed during RESET processes. R_{OFF} and R_{ON} were measured by applying a small voltage of 0.1 V with a 100 ms pulse across the electrodes to avoid any possible influence on the state of the devices. Chemical bonding states and composition of the deposited a-SiC layers were investigated using X-ray photoelectron spectroscopy (XPS) and Fourier Transform Infrared Spectroscopy (FTIR). Electrical properties of the as-deposited a-SiC layer have also been characterised using van der Pauw method.

3. Results and discussion

XPS results obtained from an as-deposited a-SiC layer are shown in Fig. 2. Binding energies of Si2p and C1s peaks are at 100.7 eV and 283.3 eV, respectively, which is expected from a-SiC films [17]. Deconvolution analysis of these XPS peaks in Fig. 2 also suggested the bonding components in the as-deposited SiC films are predominantly Si–C bond. Furthermore, FTIR result in Fig. 3 shows the co-existence of several Si–C stretching modes at approximate wave numbers of 740, 790, and 814 cm^{-1}, suggesting that the as-deposited films are amorphous SiC with stoichiometric Si:C ratio close to 1 [18]. High resistivity of the a-SiC layer in the order of 10^8 Ω cm was obtained from van de Pauw measurements, which agrees well with reported resistivity of RF sputtered a-SiC [19]. The high resistivity is attributable to the near stoichiometric compositions of the a-SiC layer as demonstrated by XPS and FTIR results as well as the relatively low RF power (250 W) and high Ar pressure used during the sputtering deposition of a-SiC, leading to reduced space defects in a-SiC [19].

Resistive switching behaviour was observed in all Cu/a-SiC/Au memory cells, as typical *I–V* characteristics for the first electroforming cycle and the subsequent SET/RESET switching cycles are shown in Fig. 4 with the voltage sweep sequence indicated by the arrows. Excellent bipolar switching characteristics are observed with repeated sharp transition between HRS and LRS. The initial electroforming process for the pristine device is achieved at $V_{form} = 4.6$ V, while the subsequent set voltage V_{set} is 2.3 V and reset voltage V_{reset} is −1.5 V. Higher V_{form} in contrast to subsequent V_{set} has been frequently observed in many RMs, which is attributed to the requirement to induce the conductive paths in the pristine device [3]. Extremely high ON/OFF switching ratios in the range of 10^8 to 10^{10} were observed with an average ON/OFF ratio of 3.5×10^9 which was obtained from over 20 continuous SET/REST cycles. To the best of our knowledge, this presents one of the highest ON/OFF switching ratios reported to date, which is advantageous for future RMs with high signal-to-noise ratios as

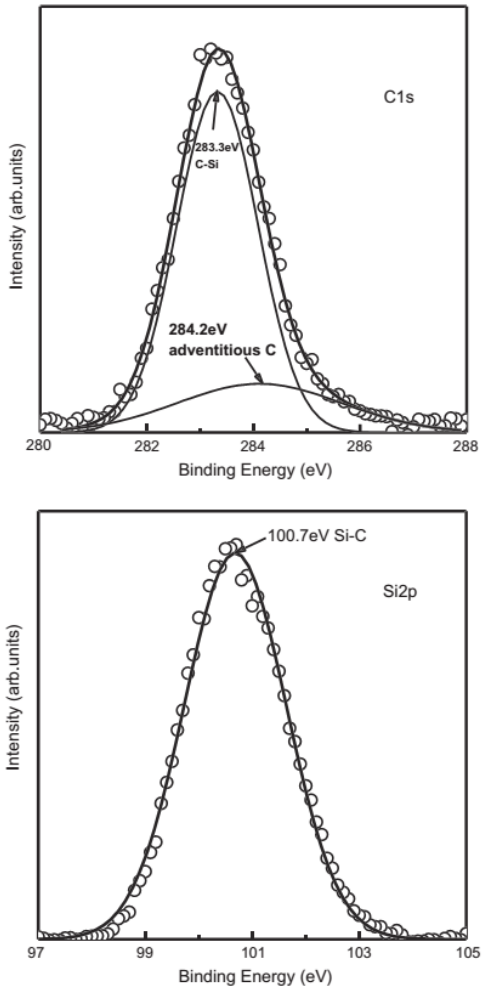

Fig. 2. C 1s and Si 2p XPS core level spectra of the as-sputtered a-SiC film.

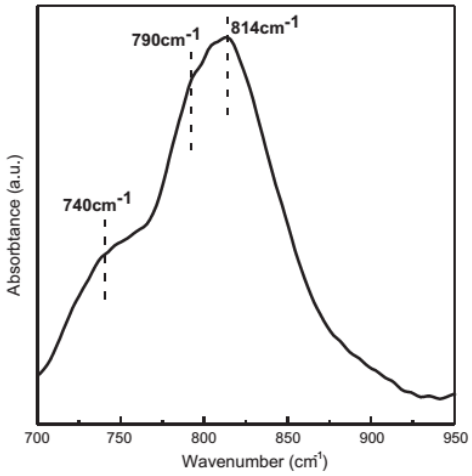

Fig. 3. FTIR absorption spectrum of the as-sputtered a-SiC film.

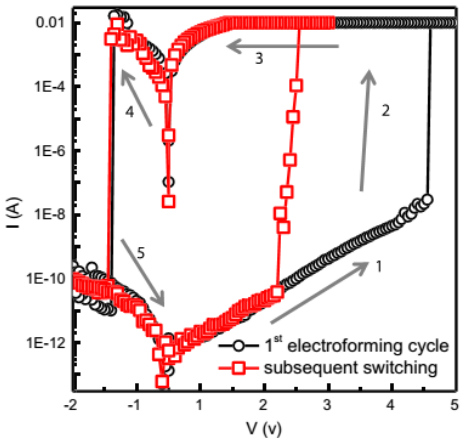

Fig. 4. Typical switching behaviour of a Cu/a-SiC/Au device. Arrows indicate the *V* sweep sequence.

well as simplified process of reading memory states [20], suggesting a significant potential of Cu/a-SiC/Au RMs. It is worth noting that, R_{OFF} of the pristine device is approximately 2 orders of magnitudes higher than the estimated resistance of the as-deposited a-SiC material which can be calculated using the measured a-SiC resistivity and known device dimensions. This indicates the possible role of Schottky contacts at HRS for Cu/a-SiC/Au device structure. On the other hand, the low R_{ON} value may indicate very conductive paths at LRS. Indeed, the distinctive resistive contrast leads to the high ON/OFF switching ratio observed in Fig. 4. By linear extrapolation of R_{ON} vs. time, stability and retention characteristics of resistive memories can be briefly evaluated [21]. Based on this method, Fig. 5 shows a linear extrapolation of R_{ON} from a typical Cu/a-SiC/Au memory cell at room temperature. It is observed that, even in 10 years' time, our ON/OFF ratio should still exceed 10^6, implicating excellent stability of these devices. The excellent stability and retention properties align with recently reported observation of a-SiC based RMs [12]. Nevertheless, it is worth noting that, although R_{ON} (10^2–10^3 Ω) of our Cu/a-SiC/Au devices is in the similar order of magnitude as in comparison with R_{ON} in these reported Cu/SiC/Pt devices [12], R_{OFF} of our devices ($\sim 10^{11}$ Ω) is several orders of magnitudes greater than the reported R_{OFF} ($\sim 10^5$ Ω) in Ref. [12], ultimately leading to significantly improved ON/OFF switching ratios. The high R_{OFF} achieved in our devices, we believe, is mainly attributable to the high resistivity (10^8 Ω cm) of the as-deposited a-SiC layer as well as the Schottky contacts formed at the interface between metal electrodes and the a-SiC device layer.

The *I*–*V* curves for LRS are shown in Fig. 6 by a double logarithmic plot. Straight lines with slopes ~1 are obtained which shows Ohmic conduction indicating that the conduction at LRS can be explained by the formation of metal filaments. R_{ON} as a function of temperature is also measured as shown in Fig. 7. The increase of R_{ON} with an increasing temperature is typical for electronic transportation in a metal. Linear fitting in Fig. 7 is also shown according to [22],

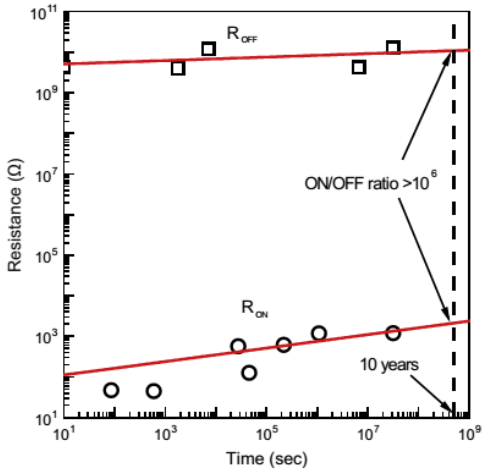

Fig. 5. Estimation of device retention by linear extrapolation. Circles are experimental data and solid lines are liner fits.

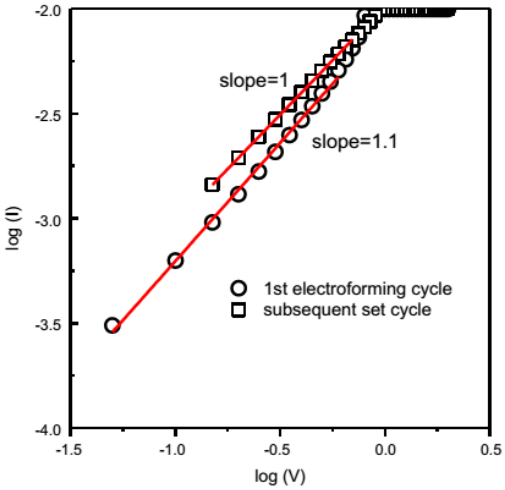

Fig. 6. Logarithm *I–V* relationship for LRS. Symbols are experimental data and lines are linear fittings.

$$R(T) = R_0[1 + \alpha(T - T_0)] \tag{1}$$

where R_0 is the resistance at room temperature T_0 = 300 K. α is the resistance temperature coefficient. From the slope of the linear fitting, we can calculate the temperature coefficient of R_{ON} to be $\alpha = 3.2 \times 10^{-3}$ K^{-1}. This resistance temperature coefficient value is in agreement to that of reported Cu nanowires [23]. Therefore we can conclude that LRS of Cu/a-SiC/Au devices have Ohmic and metallic characteristic due to the formation of conducting Cu nano-filaments.

Conduction mechanism in HRS is more complex and could follow one of the following widely reported mechanisms [24], including space-charge-limited conduction, trapping assisted tunnelling, Schottky emission, or Poole–Frenkel emission. The mechanism can be deciphered by the corresponding *I–V* characteristics. Fig. 8 shows a typical HRS *I–V* curve of a pristine Cu/a-SiC/Au

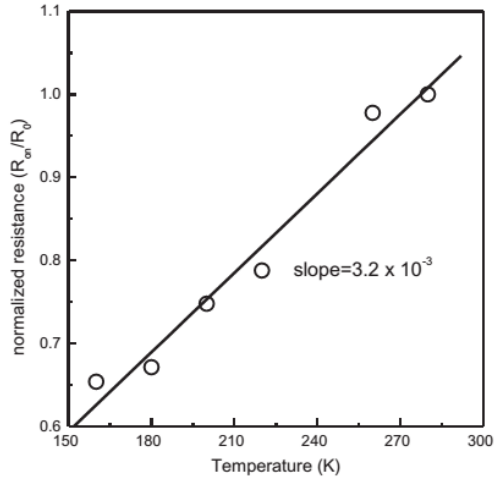

Fig. 7. Normalized R_{ON} vs temperature. Circles are experimental data and the solid line is a linear fit.

RM device, suggesting Schottky Emission for voltage below 1 V and P–F emission for voltage above 1 V. For $V < 1$ V region, the following is for the known Schottky emission Equation [25]:

$$I = AA^*T^2 \exp\left[\frac{-q\Phi_B}{kT} + \frac{q\sqrt{q/4\pi\epsilon_i}}{kT}\sqrt{E}\right] \tag{2}$$

where A is the active area of 25 μm^2, A^* is Richardson's constant, Φ_B is Schottky Barrier Height (SBH), E is electrical field, q is the electronic charge, k is the Boltzmann's constant, ϵ_i is dielectric constant of the film and T is absolute temperature. Linear fitting in Fig. 8(a) leads to the estimation of zero bias Φ_B = 0.79 eV. For $V > 1$V region, P–F emission, as a bulk material dominant conduction, follows [25],

$$\ln\left(\frac{I}{V}\right) \propto \frac{\sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r d}}}{kT}\sqrt{V} \tag{3}$$

A slope of 7.2 was obtained in Fig. 8 (b). By inputting the value of the slope and the thickness of the a-SiC layer d = 35 nm into Eq. (2), $\varepsilon_r = 5$ is obtained. Subsequently, a refractive index n ($n = \sqrt{\varepsilon_r}$) of approximately 2.2 is obtained. This value is in excellent agreement with the value of 1.9–2.4 reported for a-SiC thin films [26].

The HRS *I–V* curves for the subsequent SET/RESET switching cycle are shown in Fig. 9. Linear fittings in both positive and negative bias regions show $\ln(I) \propto V^{1/2}$ suggesting Schottky Emission following Eq. (2). No P–F Emission is found across the entire voltage range. The extremely low diffusion rate of Cu in SiC [13] indicates, driven by the electric field, there is relatively slow transport of Cu ions within the a-SiC layer, leading to longer time to reach the counter Au electrode. During this transportation period, Cu ions are apt to reduce to Cu atoms before reaching the counter Au electrode, likely forming a cone shape filament with narrowest point near the Au electrode [27]. Similar directional growth of Cu filaments in Cu/ZrO_2/Pt RM devices has been observed in real time by in situ transmission electron microscopy (TEM) [28]. As a result, the rupture is likely to happen at this narrowest point near the Au electrode during the RESET process, leading to Cu filament/a-SiC/Au contact configuration in HRS as indicated in the inset of Fig. 9. Various in situ TEM results [28,29] have reported metal conductive filament with radius ranging from approximately 5 nm to 20 nm. Even if we input the higher end contact area value A = 400 nm^2 in Eq. (2), based on data in Fig. 9, a SBH of Φ_B = 0.52 eV

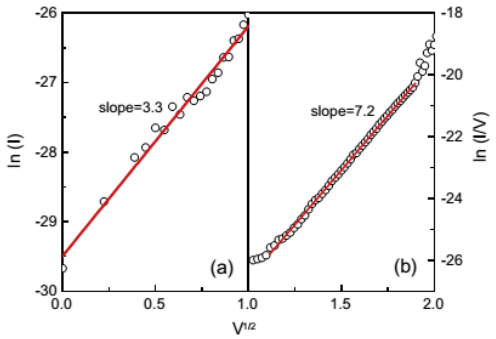

Fig. 8. Typical HRS *I–V* characteristics of a pristine Cu/a-SiC/Au device in the (a) $V < 1$ V region and (b) $V > 1$ V region. Symbols are measured data and lines are linear fittings.

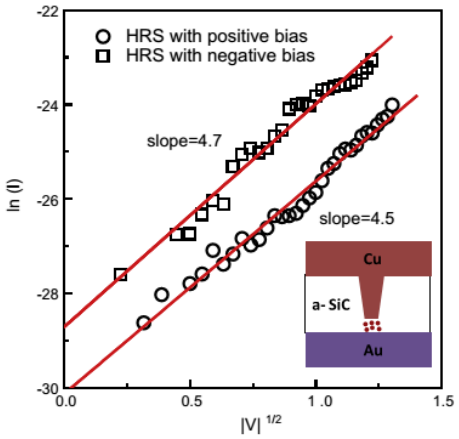

Fig. 9. *I–V* characteristics of HRS in both *–V* and *+V* zones for the subsequent switching cycle. Symbols are experimental data and the solid lines are linear fits. The inset is a schematic drawing to show the possible nanostructures at HRS.

and 0.49 eV can be extracted for the HRS with positive and negative bias, respectively. These SBHs present significant reduction in comparison with that of the pristine device (Φ_B = 0.79 eV). This may be attributable to the residual Cu nano clusters existing in the ruptured region of the a-SiC under RESET operation, which may alter the defect charges and work function in the localised a-SiC region, potentially lowering the SBH. Such a possible modification of localised a-SiC is further indicated by the clear difference between the liner fitting slops of Fig. 8a from pristine a-SiC material (slope = 3.3) and Fig. 9 from locally modified a-SiC with ruptured region (slope = 4.5–4.7) as Eq. (2) indicates that the slope value directly reflects the dielectric constant ε_i of the conducting material. Finally, the SBH Φ_B difference for the HRS with positive (0.52 eV) and negative (0.49 eV) voltage bias in Fig. 9 also indicates that the filament is likely to be ruptured at the bottom Au counter electrode as the ruptured SiC region forms different Schottky contact with top Cu filament and bottom Au electrodes, respectively, as depicted in the inset of Fig. 9. Direct in situ observation of this switching mechanism is practically challenging due to the small dimension of the filaments in the range of a few nms and will be included in our future works. Thus, *I–V* characteristics have been commonly used to decipher the switching mechanisms [3,6,27].

For our Cu/a-SiC/Au devices, the observed metallic conduction as well as the resistance temperature coefficient of R_{ON} provides a good indication of Cu filamentary switching mechanism. Furthermore, while in oxide based RMs where the conductive filaments can be potentially formed by either metal ions [28] or oxygen vacancies [30] or both [31], the lack of oxygen in our devices further support the Cu filamentary switching mechanism.

4. Conclusion

Cu/a-SiC/Au RMs with an ultrahigh ON/OFF switching ratio greater than 10^9 were fabricated and characterised. LRS and HRS *I–V* characterisation in both electroforming and subsequent switching cycles are investigated in detail with a view to understanding the relevant conduction and switching mechanisms in Cu/a-SiC/Au RMs. The results suggest that the high resistivity of the as-sputtered a-SiC as well as the Schottky contact between metal electrode/a-SiC contribute to the extremely high R_{OFF} in HRS, while the Cu conductive filaments in LRS led to stable and low R_{ON}. SBH lowering was observed after the first electroforming process, indicating possible nanostructural changes at the localised switching region within a-SiC. This favourable HRS and LRS combination essentially leads to one of the highest ON/OFF RM switching ratios obtained in both electroforming and subsequent cycles, compared with other reported cation based RMs. The high ON/OFF ratio as well as excellent retention and stability properties indicate considerable performance potentials of the Cu/a-SiC/Au RM devices.

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Microelectronic Engineering 119 (2014) 61–64

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Amorphous SiC based non-volatile resistive memories with ultrahigh ON/OFF ratios

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ARTICLE INFO

Article history:
Available online 14 February 2014

Keywords:
Resistive memory
Silicon carbide
Schottky emission
Resistive switching

ABSTRACT

Amorphous SiC based resistive memory Cu/a-SiC/Au devices were fabricated and their resistive switching characteristics investigated. Co-existence of bipolar and unipolar behavior has been observed with ON/OFF current ratio in the range of 10^8–10^9. These high ratios are due to the conduction in the OFF state being dominated by the Schottky barrier between the Au and SiC. ON/OFF ratios exceeding 10^7 over 10 years were predicted from retention characterization. The unique performance combination of the extremely high ON/OFF ratio, coexistence of bipolar and unipolar switching modes as well as excellent stability and retention suggest significant application potentials of Cu/a-SiC/Au RM devices.

1. Introduction

Non-volatile resistive memories (RMs) have attracted great attention in recent years as they show considerable potentials to replace conventional Flash memories which face stringent scaling and performance difficulties in the near future [1,2]. As the resistive switching is governed by formation/dissolution of nano-scale metallic filaments, RMs also exhibit considerably greater down-scaling potential than Flash memories, leading to a promising solution for future high density data storage [2]. RMs usually consist of simple metal-solid electrolyte-metal stack structure configuration. The ON and OFF states are distinguished by low (R_{ON}) and high (R_{OFF}) resistance of the devices which can be electrically achieved by applying voltages across the metal electrodes. Based on the polarity of applied voltage, resistive switching can be broadly classified into two modes: bipolar and unipolar switching [3,4]. For bipolar switching, the switching direction is dependent on the polarity of applied voltage, i.e., SET (OFF to ON) and RESET (ON to OFF) process require opposite voltage polarities. On the contrary, in unipolar mode SET and RESET process can occur under the same voltage polarity. RMs operating in unipolar mode are particularly advantageous for high density integration, as the peripheral circuits can be simplified [4]. On the other hand, bipolar switching RMs feature faster switching speed, better uniformity and lower operation power [5]. While most RMs reported to-date exhibit either bipolar or unipolar behavior, it is envisioned RMs with both switching modes may fit a broader range of operation requirements [5,6]. High ON/OFF current ratios are also one of the key RM performances for their future applications as they not only enable fast and reliable detection of the states of memory cells, but also simplify the periphery circuit to distinguish the storage information [7].

Although RMs with a range of solid electrolyte materials have been reported [2,8], suitable electrolyte materials that lead to these desirable performances (e.g. high ON/OFF switching current ratio, reliability, retention and coexistence of bipolar and unipolar behaviors etc.) are yet to be found. Recent studies show that amorphous SiC (a-SiC) based RMs exhibit bipolar switching characteristics with excellent retention properties [9]. Nevertheless, only bipolar switching characteristics were observed with relatively low ON/OFF ratio in the order of 10^2–10^3 [9].

This work focuses on the study of Cu/a-SiC/Au RMs. Coexistence of typical non-volatile bipolar and unipolar resistive switching characteristics have been observed with ultrahigh ON/OFF switching ratios (~10^9). *I–V* transport properties for both ON-state and OFF-state have been systematically studied with a view to investigating their respective switching mechanisms. Device stability and retention properties have also been studied.

2. Experimental

The schematic fabrication route of the Cu/a-SiC/Au RM devices is shown in Fig. 1. Si wafers with 1 μm thermally grown SiO_2 layer

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http://dx.doi.org/10.1016/j.mee.2014.02.004
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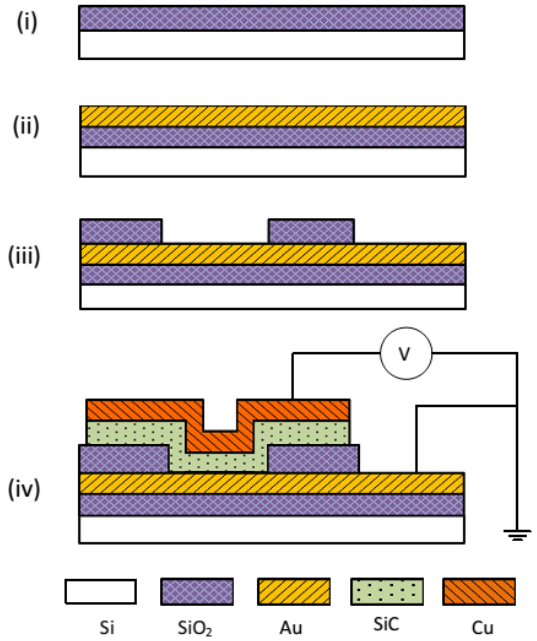

Fig. 1. (i–iv) Schematic drawings of fabrication process flow for the Cu/a-SiC/Au resistive memory devices, with (iv) also showing the electric connection configuration during the switching tests.

on top were used as starting substrates. Firstly a 300 nm thick Au layer was deposited by magnetron sputtering followed by a reactively sputtered SiO_2 layer of 250 nm in thickness. Photolithography and Reactive Ion Etch (RIE) were then applied to define the device active areas. Subsequently, a 40 nm a-SiC layer and a 300 nm Cu layer were deposited using sputtering without breaking the chamber vacuum. This is to minimize any possible contamination at a-SiC/Cu interface. Finally a lift-off process was performed to form the devices. All processes were carried out at room temperature.

Cross-sectional view of a typical Cu/a-SiC/Au device was obtained by Focused Ion Beam (FIB) milling and Scanning Electron Microscope and is shown in Fig. 2. The dark a-SiC layer is clearly visible between two bright metal layers. Switching performance of these Cu/a-SiC/Au RMs has been characterized by sweeping voltage across the top Cu active electrode and bottom Au counter

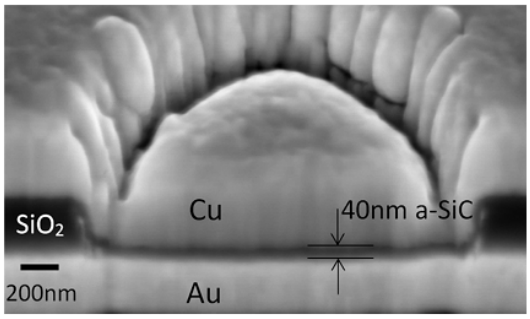

Fig. 2. Cross-sectional view of a typical Cu/a-SiC/Au device.

electrode as depicted in Fig. 1(iv), using an Agilent B1500A semiconductor device parameter analyzer. The Au electrode was constantly grounded during testing, while sweeping voltage was applied on the Cu electrode. To test bipolar mode switching, the voltage sweeping sequence was 0 V → +V → 0 V → −V → 0 V, while for unipolar mode, the sweeping voltage was 0 V → +V → 0 V → +V → 0 V. Current compliance was applied during SET cycles to prevent permanent breakdown.

3. Results and discussion

Coexistence of bipolar and unipolar resistive switching with ultrahigh ON/OFF ratios in the range of 10^8–10^9 has been observed, as is shown in Fig. 3. The results were acquired from a Cu/a-SiC/Au device with device active area of 1 μm diameter and 40 nm thick a-SiC layer. The SET voltages in both switching modes were approximately +2.4 V, while the RESET voltages were approximately −1 and +0.9 V for bipolar and unipolar modes, respectively. In bipolar mode, R_{ON} and R_{OFF} measured at 0.1 V were typically 7×10^2 and 6×10^{11} Ω, respectively, leading to extremely high ON/OFF ratio of approximately 8×10^8. Similarly, the ON/OFF ratio for unipolar switching was approximately 5×10^8. R_{OFF} for unipolar devices is slightly lower than that for bipolar devices which we believe is likely caused by the different RESET mechanisms in the two modes, as will be discussed later. Furthermore, it is important to note that, once the device has undergone the first SET process with positive voltage sweep, for the subsequent cycles, the bipolar switching modes could also be observed using negative voltage SET processes, i.e. 0 V → −V → 0 V → +V → 0 V; similarly, unipolar switching mode could also be obtained through negative voltage SET, i.e. 0 V → −V → 0 V → −V → 0 V. Again, we believe this likely indicates localised rupture of the filament during RESET process which leaves residue Cu at the Au electrode. Such residue Cu can then act as an effective electrode in the subsequent cycles. More details will be included later. Nevertheless, since all switching cycles present similar behavior for bipolar and unipolar switching, respectively, typical bipolar and unipolar cycles are presented in Fig. 3 for clear comparison. To the best of our knowledge, our Cu/a-SiC/Au devices present the highest ON/OFF ratio reported to date among devices exhibiting coexistence of bipolar and unipolar

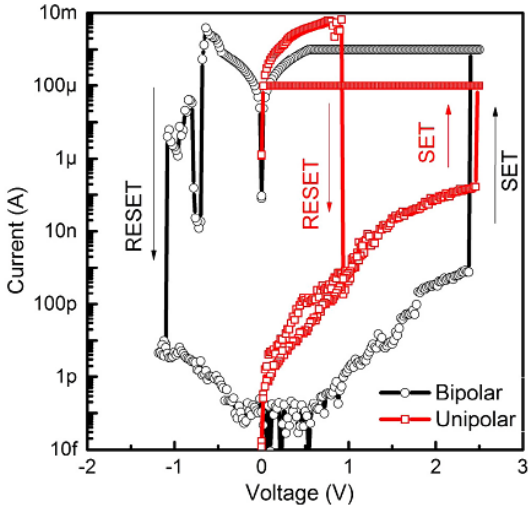

Fig. 3. Typical bipolar and unipolar switching behavior observed in a typical Cu/a-SiC/Au RM. The set and reset processes in both modes are also indicated.

modes, which suggest a significant potential of these memory devices.

Due to the great difficulty to observe the conduction paths in real time, detailed studies of *I–V* characteristics have been widely exploited to decipher the conduction and switching mechanisms of RMs in general [5,7,9]. *I–V* characteristics of the Cu/a-SiC/Au RMs ON-state for both bipolar and unipolar switching are shown in Fig. 4(a) in a Log(*I*)–Log(*V*) scale. The slopes of the linear fittings are very close to 1, which suggests metallic Ohmic conduction in both bipolar and unipolar ON-states. R_{ON} values for both bipolar and unipolar devices are of the order of $10^2\ \Omega$, indicating a similar conduction mechanism in the ON-states. Normalized R_{ON} vs. temperature results in Fig. 4(b) also show the increase of R_{ON} with temperature, further implying metallic conductions in the ON-states. Through linear fitting in Fig. 4 (b), a positive temperature coefficient of $3 \times 10^{-3}\ K^{-1}$ is obtained, which is in agreement with the reported value of be $2.5 \times 10^{-3}\ K^{-1}$ for Cu nanowires of diameter $\geqslant 15$ nm [10]. It is thus plausible to believe that Cu metallic filaments provide the conduction path in the ON-states for both bipolar and unipolar cases which agrees with numerous previous studies on RMs with Cu as active electrodes [3,9,11]. Furthermore, in this temperature range (200–300 K), since the temperature coefficient of Cu nanowires generally increases with the wire dimensions [12], we believe that the conducting Cu filament in our device is likely to be approximately tens of nanometers in diameter, similar to reported real-time TEM observations [13]. The formation of Cu filaments is generally attributed to electrochemical reactions [7]: in essence, during the SET process, anodic dissolution of Cu according to the reaction: $Cu \rightarrow Cu^{Z+} + Ze^-$ takes place when Cu active electrode is under positive bias. Subsequently, Cu^{Z+} cations are driven by the electric field across the Cu and Au electrodes, and eventually reduced into Cu atoms according to the reaction $Cu^{Z+} + Ze^- \rightarrow Cu$, forming Cu conductive filaments for the ON states as shown in the inset of Fig. 4(b). These Cu filaments remain stable for the ON states even after removal of the external electric field, forming non-volatile characteristics. It is worth noting that sharp switching from OFF-state to ON-state have been observed in all our SET processes, as shown in Fig. 3 without multi-step transition features which have been reported in some RMs [14]. This indicates that it is likely single Cu filament is formed during our SET processes.

Although the similar SET mechanism for both bipolar and unipolar have been widely accepted [2,3], their different RESET mechanisms have been recognized [15]. In order to understand the RESET mechanism, the OFF-state *I–V* characteristics in a $Ln(I)–V^{1/2}$ plot is shown in Fig. 5. Good linear fitting is obtained for both switching modes which strongly suggest a conduction mechanism dominated by thermo-ionic field emission over a Schottky barrier (Schottky emission) as displayed in Eq. (1) [16]:

$$I = AA^*T^2 \exp\left[\frac{-q\Phi_B}{kT} + \frac{q\sqrt{q/4\pi\epsilon_i}}{kT}\sqrt{E}\right] \quad (1)$$

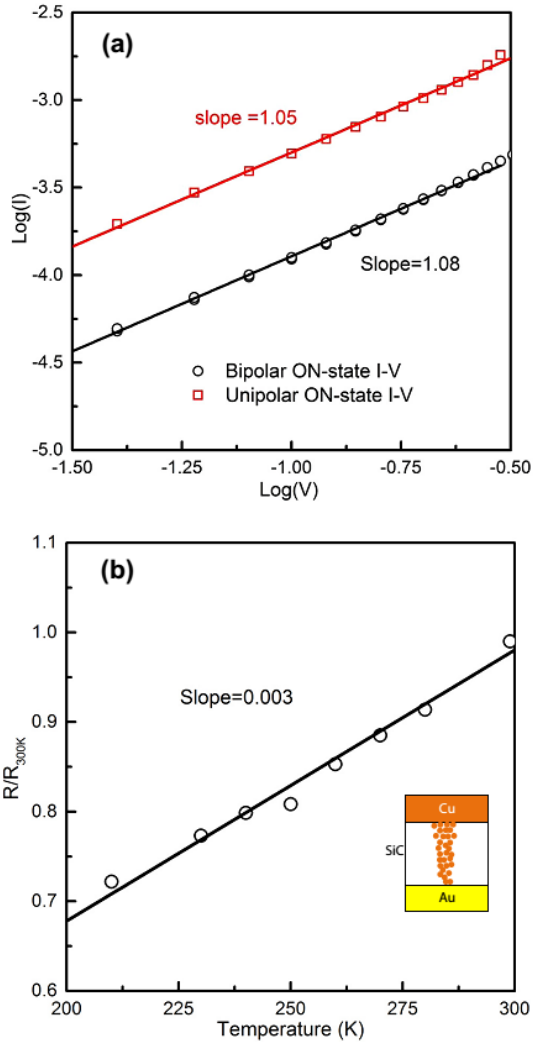

Fig. 4. (a) Log(*I*)–log(*V*) plot showing the ON-state *I–V* data of both bipolar and unipolar switching modes obtained from a Cu/a-SiC/Au RM., with the straight lines being their respective linear fittings. (b) Normalized R_{ON} values versus temperature, with the straight line being a linear fit. The inset shows the probable Cu nanofilament conduction mechanism at ON-states.

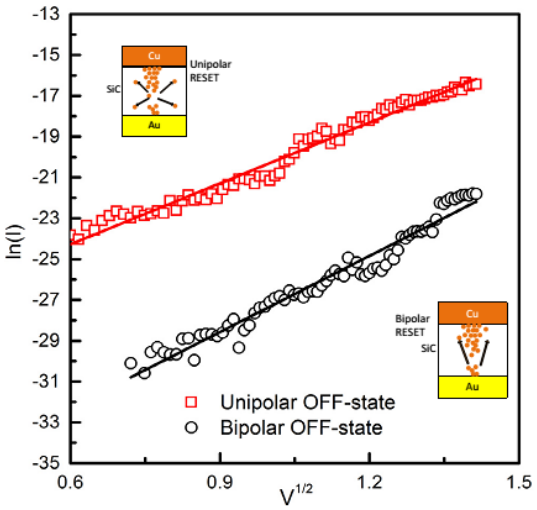

Fig. 5. $Ln(I)–V^{1/2}$ plot showing the OFF state *I–V* data for both bipolar and unipolar switching modes obtained from Cu/a-SiC/Au RM cells. The straight lines are linear fittings. The insets show the possible mechanisms of the RESET processes in bipolar and unipolar modes, respectively.

A is the active area of 1 μm^2, A^* the Richardson's constant, Φ_B the Schottky Barrier Height (SBH), E the electrical field, q the electronic charge, k the Boltzmann's constant, and ϵ_i is the dielectric constant of the film. The extracted values for the Schottky barrier height are 0.94 eV for the OFF state obtained by bipolar RESET process (in the negative V range), and 0.70 eV for the OFF state achieved by unipolar RESET process (in the positive V range). Schottky emission mechanism has been observed in some RMs, and was attributed to the Schottky barrier at the metal to solid electrolyte interface [17]. Our results suggest a dominant contribution of Schottky barrier at the metal/a-SiC interfaces to the overall conduction at OFF states. The noticeable Schottky barrier is likely a contributing factor to the high R_{OFF}, and consequently high ON/OFF ratio of our devices. The herein observed SBH difference for the OFF states between bipolar and unipolar Cu/a-SiC/Au RMs indicates the different rupture mechanisms of the Cu nanofilaments. With negative voltage applied to the Cu electrode, electrochemical dissolution of the Cu filament is widely accepted as the dominating rupture mechanism which follows reaction of $Cu \rightarrow Cu^{z+} + Ze^-$ [7]. However, with positive voltage applied to the Cu electrode during RESET process, it is reported that Joule heating plays a key role leading to the rupture of metal filaments for unipolar switching [11,14]. We believe that this localized heat treatment may alter the interface between the Cu filaments and a-SiC, much like annealing processes exploited for the reduction of Schottky contacts between metal and semiconductor contacts [18], leading to the lowered SBH for unipolar switched devices. This lower SBH in unipolar switching mode may contribute to the relatively lower R_{OFF} ($\sim 10^{11}\ \Omega$) in comparison of that of bipolar R_{OFF} ($\sim 10^{12}\ \Omega$) as mentioned earlier. Schematic illustrations of the RESET mechanisms for bipolar and unipolar modes, respectively, are also shown in Fig. 5 insets. It is also important to note the Cu residue on Au electrode during the RESET process which is likely to act as active electrodes if negative voltage SET process is applied as mentioned earlier.

For novel non-volatile memories, state retention over 10 years at 85 °C is required to be competitive against Flash memory, and this standard has been widely accepted to assess and compare stabilities of various RMs [7]. Although it has been reported that the OFF-state of conductive filament based RMs is quite stable for an extended period of time, even at elevated temperature, ON-state resistance of these RMs [19] suffer from rapid increase with time following the power-law: $R_{ON} = Bt^m$, where m is larger than 0 [2,19], leading to poor stability and retention. A commonly adopted method of predicting retention performance is to monitor device's resistance over a short period of time at 85 °C, and extrapolate the power-law dependence to 10 years' time [2]. To assess the retention performance of our Cu/a-SiC/Au RMs, two identical devices have been used with one SET to ON-state and the other RESET to OFF-state. Subsequently, the R_{ON} and R_{OFF} from these stable ON and OFF states, respectively, have been measured using 0.1 V over a period of time at 85 °C to enable power law extrapolation analysis of the device retention [2]. The results in Fig. 6 clearly show that there is no noticeable deterioration of R_{ON} during the measurements and as a result, the power-law extrapolation ($m = 0.18$) suggest that the ON/OFF switching ratio after 10 years can still be expected to be greater than 10^7, implicating excellent stability and retention of these devices. Such an excellent stability and retention properties agree with the previous literature on a-SiC based RMs, and is believed to be largely attributable to the extremely low diffusion rate of Cu in the a-SiC solid electrolyte layer [9].

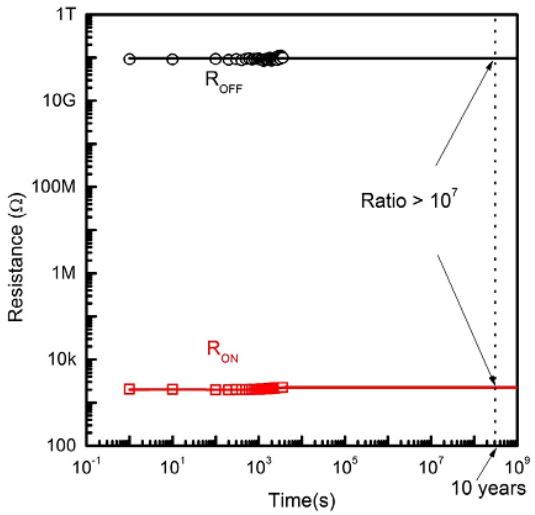

Fig. 6. R_{ON} and R_{OFF} versus time measured at 85 °C, with power law extrapolation to 10 years.

4. Conclusion

Co-existence of bipolar and unipolar behavior has been observed in Cu/a-SiC/Au RM devices with highest ON/OFF ratio of the order of 10^8–10^9. Detailed analysis of I–V switching characteristics in both switching modes suggests Cu metallic filament conduction at ON-state and a Schottky barrier limited conduction mechanism in the OFF states. The different RESET processes during the unipolar and bipolar switching modes leads to the SBH difference. Furthermore, the presented Cu/a-SiC/Au RM devices show excellent state stability and retention with predicted 10 year ON/OFF current ratios exceeding 10^7. The unique performance combination of the extremely high ON/OFF ratio, coexistence of bipolar and unipolar switching modes as well as excellent stability and retention suggest significant application potentials for these Cu/a-SiC/Au RM devices.

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