UNIVERSITY OF SOUTHAMPTON

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING
Electronics and Computer Science

Investigation into Yield and Reliability Enhancement of TSV-based Three-dimensional Integration Circuits

by Yi Zhao

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ABSTRACT

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Three dimensional integrated circuits (3D ICs) have been acknowledged as a promising technology to overcome the interconnect delay bottleneck brought by continuous CMOS scaling. Recent research shows that through-silicon-vias (TSVs), which act as vertical links between layers, pose yield and reliability challenges for 3D design. This thesis presents three original contributions.

The first contribution presents a grouping-based technique to improve the yield of 3D ICs under manufacturing TSV defects, where regular and redundant TSVs are partitioned into groups. In each group, signals can select good TSVs using rerouting multiplexers avoiding defective TSVs. Grouping ratio (regular to redundant TSVs in one group) has an impact on yield and hardware overhead. Mathematical probabilistic models are presented for yield analysis under the influence of independent and clustering defect distributions. Simulation results using MATLAB show that for a given number of TSVs and TSV failure rate, careful selection of grouping ratio results in achieving 100% yield at minimal hardware cost (number of multiplexers and redundant TSVs) in comparison to a design that does not exploit TSV grouping ratios. The second contribution presents an efficient online fault tolerance technique based on redundant TSVs, to detect TSV manufacturing defects and address thermal-induced reliability issue. The proposed technique accounts for both fault detection and recovery in the presence of three TSV defects: voids, delamination between TSV and landing pad, and TSV short-to-substrate. Simulations using HSPICE and ModelSim are carried out to validate fault detection and recovery. Results show that regular and redundant TSVs can be divided into groups to minimise area overhead without affecting the fault tolerance capability of the technique. Synthesis results using 130-nm design library show that 100% repair capability can be achieved with low area overhead (4% for the best case). The last contribution proposes a technique with joint consideration of temperature mitigation and fault tolerance without introducing additional redundant TSVs. This is achieved by reusing spare TSVs that are frequently deployed for improving yield and reliability in 3D ICs. The proposed technique consists of two steps: TSV determination step, which is for achieving optimal partition between regular and spare TSVs into groups; The second step is TSV placement, where temperature mitigation is targeted while optimizing total wirelength and routing difference. Simulation results show that using the proposed technique, 100% repair capability is achieved across all (five) benchmarks with an average temperature reduction of 75.2℃ (34.1%) (best case is 99.8℃ (58.5%)), while increasing wirelength by a small amount.

Content

Declaration of Authorship

I, Yi Zhao, declare that this thesis entitled *Investigation into Yield and Reliability Enhancement of TSV-based Three-dimensional Integration Circuits* and the work presented in it are both my own, and have been generated by me as the result of my own original research. I confirm that:

• This work was done wholly or mainly while in candidature for a research degree at this University;

• Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;

• Where I have consulted the published work of others, this is always clearly attributed;

• Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;

• I have acknowledged all main sources of help;

• Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;

• Parts of this work have been published as listed in Chapter 1 Section 1.5

Signed: Date:

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Chapter 1

Introduction

Over the past few decades, great efforts have been made to miniaturize microelectronic circuits. Microelectronic circuits are required to have higher performance, increasing functionality, and low power consumption. The International Technology Roadmap for Semiconductors (ITRS) predicts that the performance enhancement due to CMOS transistor scaling will be significantly reduced unless a new design methodology shift from current IC paradigm takes place. Continuous shrinking of CMOS transistor feature size enables performance enhancement of gates, however, interconnects delay rapidly increase as well which lead to system performance bottleneck [1]. As illustrated in Figure 1.1, gate delay drops with shrinking technology nodes whereas the interconnect delay increases [2].

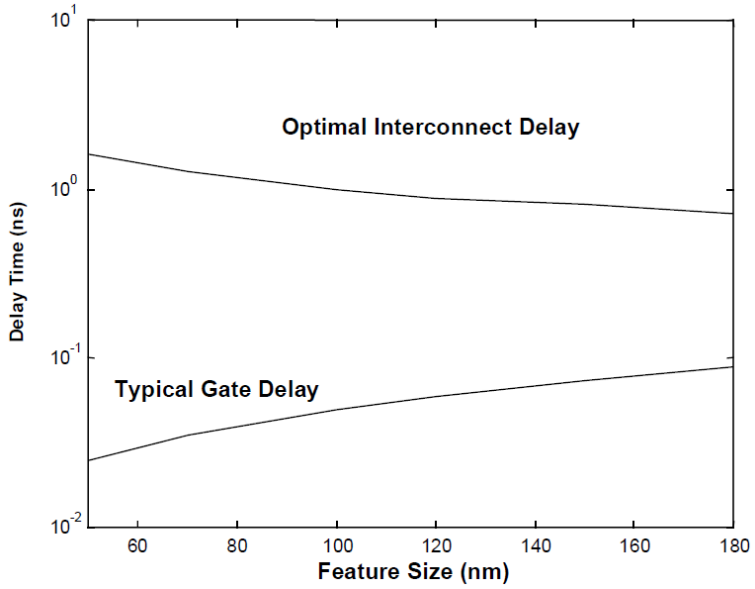


Figure 1.1: Interconnect Delay and Gate Delay for different CMOS feature sizes [2].

Although, repeaters and flip-flops can be inserted to make long global interconnection delay tractable to prevent system performance degradation, the additional power consumption of these components is very large, and can be a major fraction of system power consumption [3, 4]. Three-dimensional Integrated circuits (3D-ICs) has been acknowledged as a promising technology to overcome this performance bottleneck. A three-dimensional integrated circuit is any circuit in which devices are not restricted to be placed on a single plane. Such a circuit can be regarded as a stack of individual conventional two-dimensional (2D) integrated circuits (ICs), each of which is called a “device layer”, “tier”, or simply a “silicon die” [1], where through silicon vias (TSVs) are used for communication between different device layers, as shown in Figure 1.2.

3D integration technology intuitively enables a larger device density under a given footprint area when compared to conventional planar ICs. Moreover, by using vertical inter-layer connection instead of the long horizontal wires [5, 6, 7], aggressive reduction in interconnects length can significantly improve the system performance (wire delay) and reduce the power consumption. Integration of heterogeneous technology, such as logic and memory, analog device, RF circuits, and MEMS, can also be realized using 3D integration (Figure 1.2). Heterogamous integration also means incorporating different technology nodes such as 180nm and 90nm in the same device. TSVs are critical components which guarantee that all stacked device layers work as expected. However, recent research has highlighted that TSVs failures are either due to manufacturing defects or thermal-induced aging defects resulting in yield and reliability issues in 3D circuits. This thesis focuses on investigating and developing cost-effective solutions targeting yield and reliability issue brought by TSVs to ensure that communication between dies using TSVs interconnects is not affected.

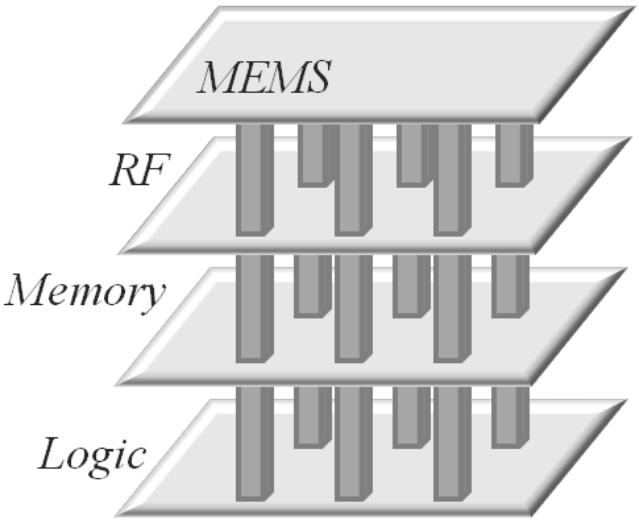


Figure 1.2: Schematic diagram of a 3D-IC with heterogeneous technology integration.

This chapter provides preliminary information for the subsequent chapters in this thesis. An overview of the state-of-the-art 3D-ICs fabrication process is discussed in Section 1.1. Section 1.2 elaborates on the reported benefits brought by moving from 2D to 3D integration. Section 1.3 outlines the challenges of adapting 3D-ICs and explains the challenges that are targeted in this thesis. The motivation for this research in the subsequent chapters is discussed in Section 1.4 while Section 1.5 provides the outline of this thesis. Finally, the list of publications generated from the research in this thesis is given in Section 1.6. Note that a journal paper with the title of ‘Thermal-aware fault tolerance scheme of TSV-based 3D-ICs with global sharing of redundant TSV’ is under prepared based on the research in this thesis.

1.1 Introduction to 3D-IC Structure and Fabrication Process

Enabling 3D integration in microelectronic design has recently become an active research area, motivated by the need to achieve higher performance in a smaller system. Current 3D integration technologies can be classified into two categories: 1) Packing-based technology [8, 9], and 2) TSV-based 3D integration technology [10].

1.1.1 Packaging-based 3D Integration Technology

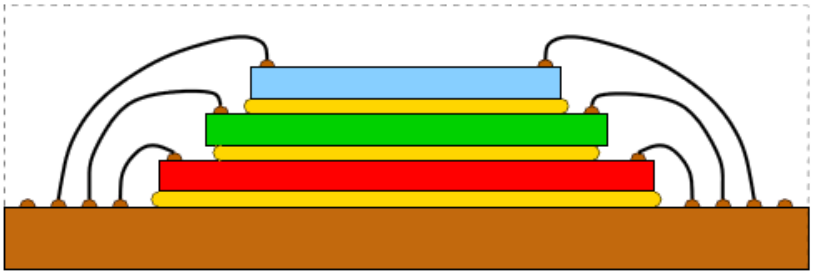


Figure 1.3: System-in-Package (Die stacking using wire-bonding) [11].

This type of technology achieves three-dimensional integration at package level which stacks fabricated 2D chips through wire-bonding and flip-chip bonding methods [1, 12], including System-in-Package (SiP) and Package-on-Package (PoP) structures. Multi-chip-module (MCM) is a popular method to form SiP by stacking of chips using wire-bonding, as shown in Figure 1.3. This type of technique is widely used in the telecommunication industry for smaller portable products (e.g., stack of 16 NAND flash dies in a signal multichip package for a 16GB memory by Samsung Electronics [13]). PoP technology allows for the stacking of multiple chip packages by connecting them with solder-bumps, which offers higher interconnect density than the MCM-based SiP Chip. Note that each single chip of a PoP stack can be a wire-bonding based MCM as well (Figure 1.3). Package-based 3D integration does not introduce new manufacturing process and can use the existing assembly process enabling short time-to-market. However, its interconnect density is limited to package level which prohibits performance enhancement achieved by this type of 3D integration technology. Thus, a new promising 3D integration technology which is TSV-based 3D-ICs is favoured by the industry. In comparison to package-level stacking technology, the TSV-based 3D chip provides higher bandwidth and lower power consumption with a smaller chip footprint, as shown in Figure 1.4. The benefits brought by TSV-based 3D integration technology are discussed in detail in Section 1.2.

1.1.2 Overview of TSV-based 3D Integration

There are two main technologies that employ TSVs for 3D integration, as illustrated in Figure 1.5. The first is the interposer-based 3D integration, where multiple chip slices are integrated

side-by-side on a passive silicon interposer (Figure 1.5(a)). The passive interposer contains high density interconnections (TSVs) and no active device in the silicon substrate [14]. The key innovation is to augment the standard I/Os with thousands of die-to-die connections

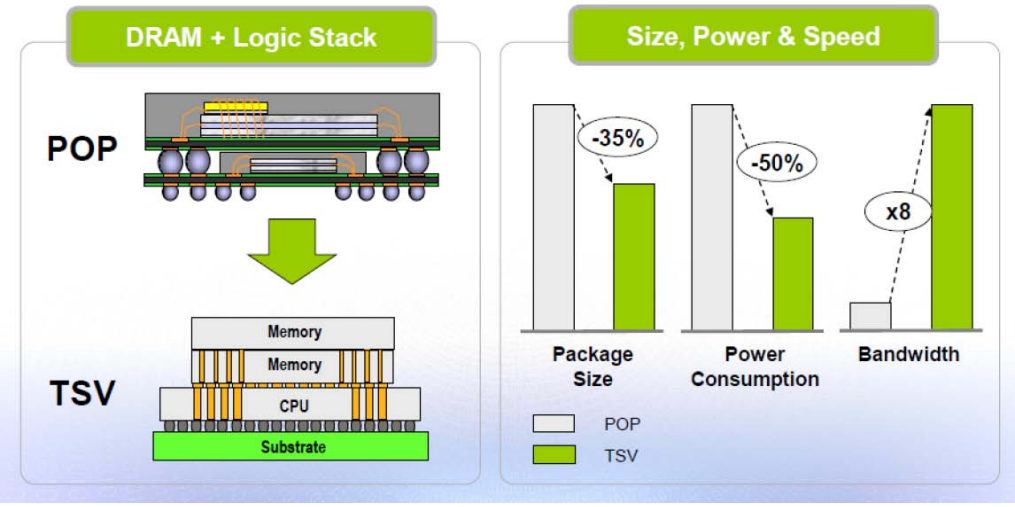
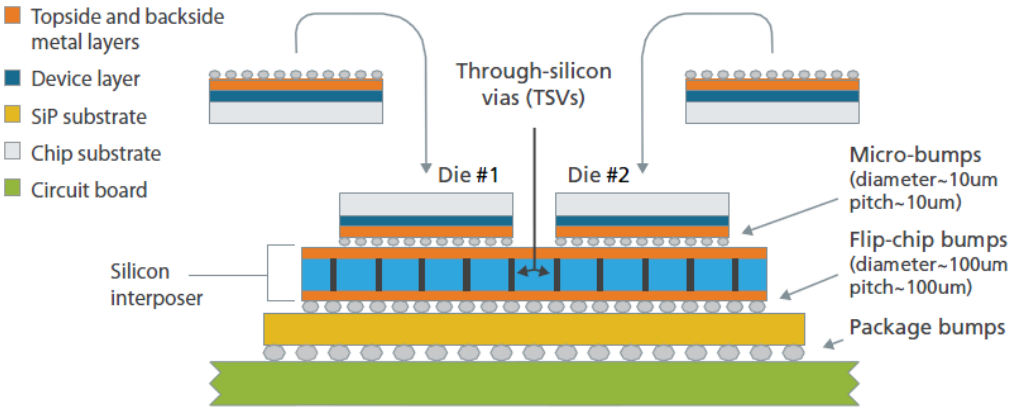
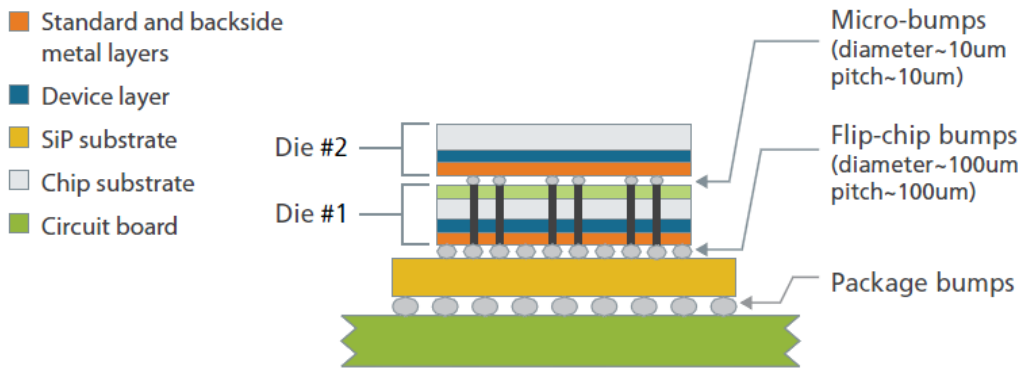


Figure 1.4: Comparison between PoP-based and TSV-based 3D integration technologies.

through passive traces fabricated on the silicon interposer. This approach provides high connectivity (more than 10,000 connections between two dice) and low latency (~1nS) without incurring the power penalty of traditional I/O structures. Sometimes this technology is referred to as 2.5D integration [15]. However, a true 3D integration can integrate chips with TSVs directly and no interposer layer is needed (Figure 1.5(b)). The true 3D integration allows even higher interconnects density and the TSV diameter can range from 1 to 30 microns [15]. In this research, there is no distinguish between the interposer-based 2.5 integration and the true 3D integration, since they both employ TSV interconnects for communication between dies. Furthermore, the research work proposed in this thesis is to address the yield, reliability and thermal issue for both types of TSV-based 3D circuits.



(a) Interposer-based 3D integration



(b) True 3D integration using TSVs

Figure 1.5: TSV-based 3D integration technologies [15].

1.1.3 Various Implementation Technologies of TSV-based 3D Integration

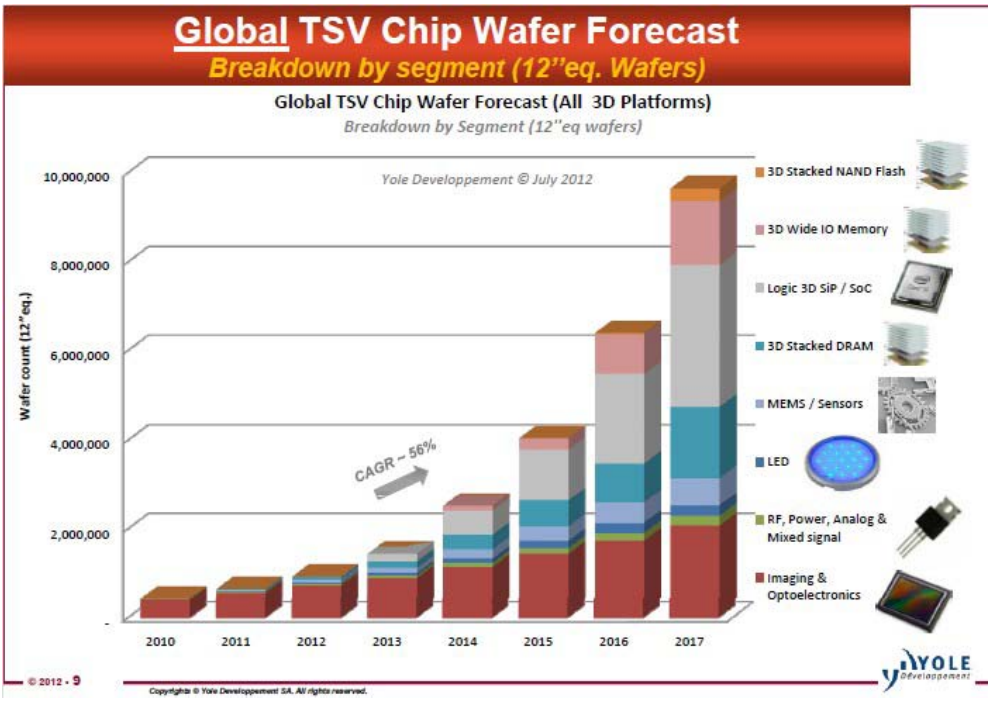


Figure 1.6: Forecast of TSV-based 3D products [16].

Nowadays, TSV-based 3D integration has drawn extensive attention from the industry, as predicted by [16], the digital produce market can be boosted by TSV-based 3D chips (Figure 1.6). Nowadays, research organizations across academic and industry have reported a number of TSV-based 3D technologies with a plethora of alternative implementation process flows in terms of substrate types, stacking methods, via process flows, and bonding approaches [10]. Wafers can have silicon-on-insulator (SOI) substrate or thicker bulk substrate. Due to the removal of entire substrate in the upper layers (Figure 1.8) of the SOI-based design, finer size

and shorter TSVs can be realized when compared to the bulk Si substrate 3D integrated circuits. However, its fabrication process is more costly and requires extremely aggressive alignment accuracy [10]. Existing TSV-based 3D integration technologies differ from each other in terms of stacking methods, bonding orientation and via formation procedure, and bonding methodologies.

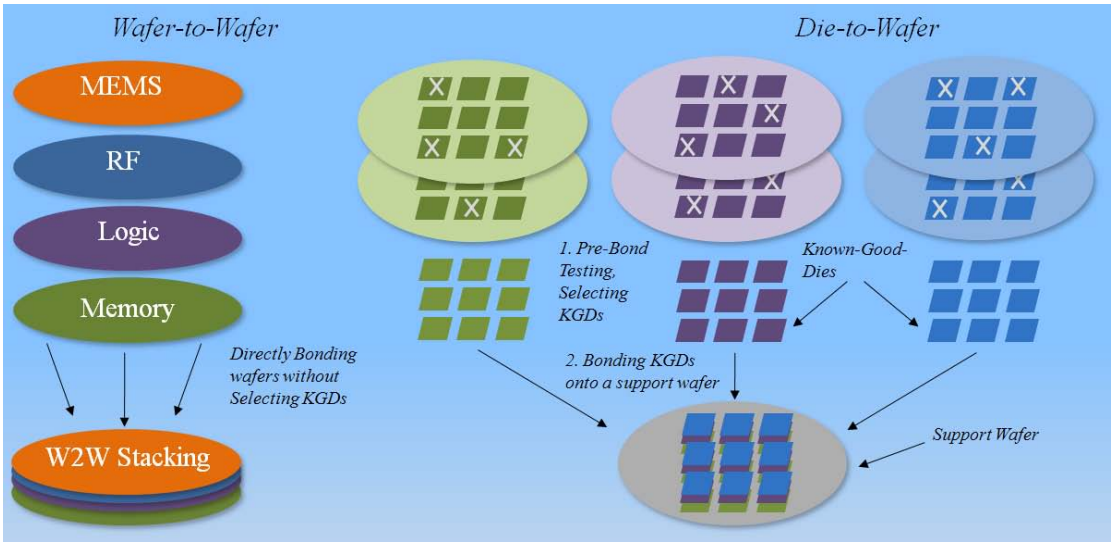


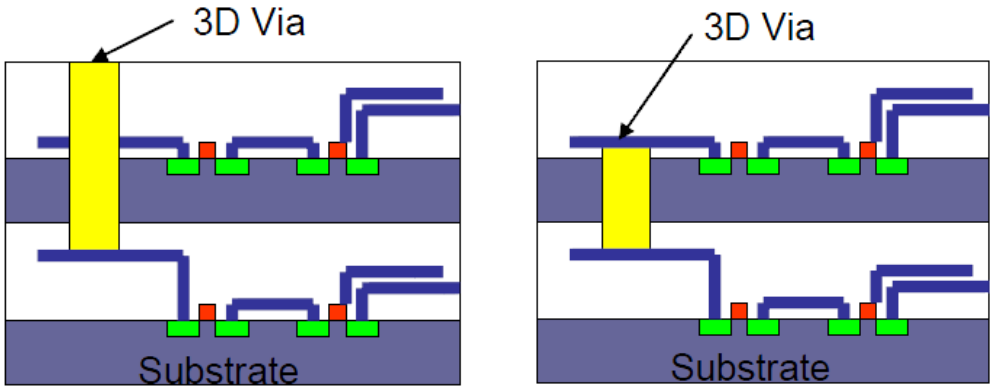
Figure 1.7: Demonstration of D2D (D2W) and W2W bonding approaches. W2W bonding directly stacks multiple wafers while D2D (D2W) introduces the KGD test prior to the bonding process.

Stacking Method

Depending on the individual units to be stacked, 3D-ICs stacking methods can be categorized into: wafer-to-wafer (W2W), die-to-die (D2D) and die-to-wafer (D2W). In W2W stacking, entire wafers are directly bonded together, and then cut into dies [17]. Due to the elimination of the die selecting procedure prior to bonding, W2W offers the highest throughput. However, it involves yield issue as prior to bonding, it is not ensured that all dies are good, bad dies may be stacked with good dies and one bad die may fail the whole design. |The D2W(D2D) stacking method allows the diced dies to be tested individually, such that only Known-Good-Dies (KGDs) are used in the 3D integration (Figure 1.7), which improves the overall chip yield. Moreover, D2W(D2D) has a higher flexibility in die size. However, the testing and pre-selection of KGDs decreases throughput thus increasing the manufacturing time and cost [17].

Die stacking orientation and Via formation process

There are two types of stacking manners with respect to stacking orientation of two dies during bonding: Face-to-Back (F2B) and Face-to-Face (F2F) processing. Structures in Figure 1.8(a)-(c) are implemented in F2B fashion, where the bottom die places its face (device layer) up and is connected to the upper (second) die with its back side (metal layer) down. F2B bonding is easier to scale to a stack containing more than two dies, while F2F bonding orientation is limited to the stacking of two dies (Figure 1.8(d)). Additionally, the F2F process has finer inter-die interconnects (i.e., higher density of inter-layer interconnects), nevertheless



(a)

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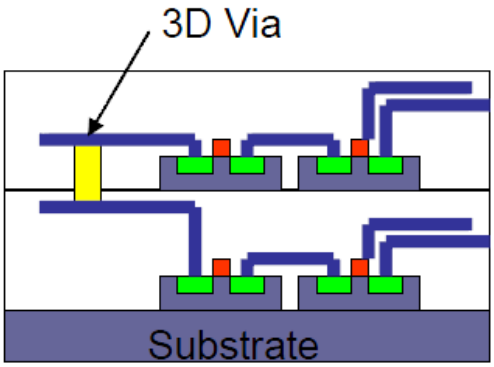

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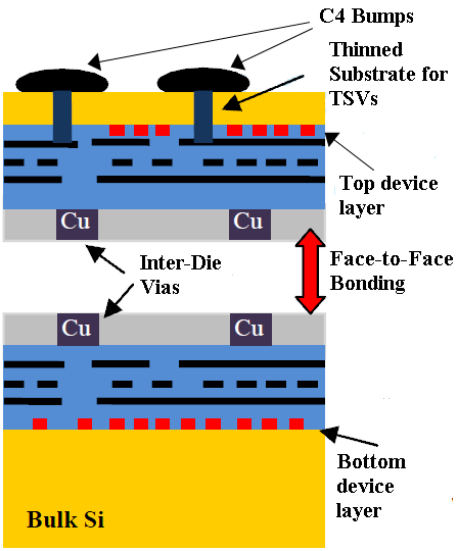


(d)

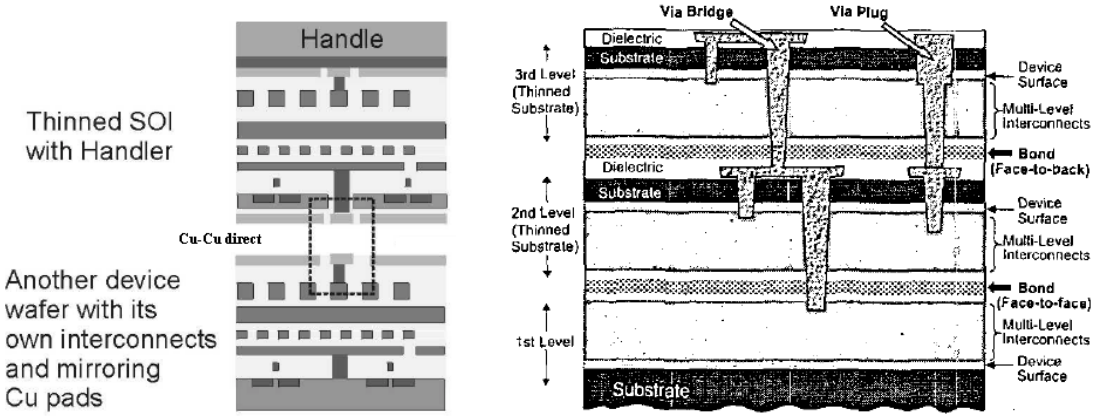
Figure 1.8: Schematic diagrams for (a) F2B, Via-last bulk Si 3D-ICs [18], (b) F2B, Via-first bulk Si 3D-ICs [18], (c) F2B, Via-last SOI-based 3D-ICs [168] and (d) F2F bulk Si 3D-ICs [19]. Note that Via-first and via-last terminologies are usually for F2B stacking orientation technologies.

it requires deep and large area-consuming vias for power and I/Os of package (Figure 1.8(d)). In terms of the through-silicon-via fabrication process, recent research proposed two main TSV manufacturing processes: Via-first and Via-last TSV formation flow, where the main difference is the order of TSV processing. In the via-first TSV process, as shown in Figure 1.8(b), 3D vias are etched and deposited before the front-end-of-line (FEOL, i.e., building device layer) process and the back-end-of-line (BEOL) metal layer formation process. However, in via-last TSV process TSVs are formed after FEOL and BEOL process, as shown in Figure 1.8(b). Via-first process has little impact on the device layer and metal layer formation, and is effective for creating higher 3D via density when compared to the via-last process, however, it requires more complex process resulting in higher cost [20]. Via-middle process flow also appeared in recently published result [21], where TSV formation is after FEOL process but prior to BEOL process. Note that Figure 1.8(c) illustrates the SOI based 3D structure proposed by IBM [22] which uses via-last process as well, however, it has the smallest via size and shortest distance between layers, due to the removal of the entire silicon substrate. [10].

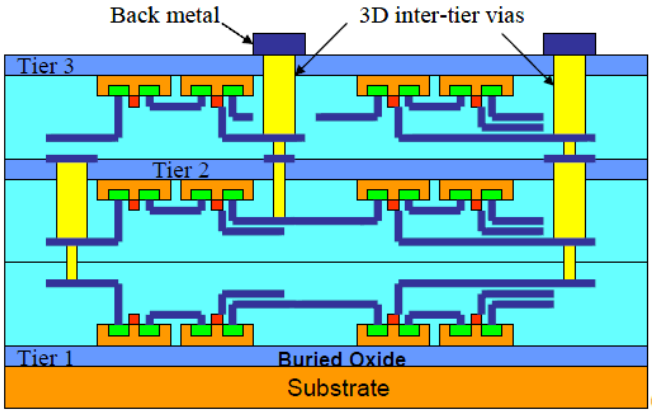
The filling of TSVs uses various materials, such as Cu [23, 24, 25], W [26], and poly-Si [27, 28]. Poly-Si, as a doping material, is a stable material which can avoid metal atom contamination and affect device features less than other material [27, 28]. However, Cu filling can enable even lower interconnection resistance and finer via size. Additionally, via diameter size varies with different 3D-IC schemes from 0.4um to 140um [22, 29].

3D-ICs Bonding approach

There are primarily three types of bonding approaches, referred to as, thermal-compression Cu-Cu bonding, dielectric adhesive bonding, and oxide-oxide (oxide-fusion) bonding. Thermal compression Cu-Cu [24] bonds layers with inter-die vias with Cu pads, as shown in Figure 1. 9(a), where a F2B stacking fashion is used. Two layers are bonded at 400 ℃ to achieve mechanically reliable Cu-Cu boding interface and to minimize metal oxidation at the interface. Mechanical properties of Cu-Cu bonding and possible bonding conditions and procedures are investigated in reference [30]. Cu-Cu bonding is preferred by industries, as it introduces low contact resistance at the bonding interface. Adhesive bonding uses an additional glue layer, such as Benzocyclobutene (BCB) to bond the adjacent layers, as shown in Figure 1.9(b) [31, 32]. It can achieve good bonding interface strength, however, the bonding accuracy using adhesive glue may be degraded, as adhesive may become viscous which can cause unexpected alignment patterns shift. Direct oxide-oxide bonding approach bonds two adjacent layers immediately without introducing any extra bonding material [33], as illustrated in Figure 1.9(c). A study [22] implemented oxide-oxide bonding by oxide fusion at room temperature, which is better than the temperature required in Cu-Cu bonding, thus the status of the bonding interface remains solid and stable during bonding, unlike it is in the adhesive bonding. There is also a hybrid bonding approach (Figure 1.9(d)) which combines Cu-Cu bonding and adhesive bonding methods which employs the advantages of both



(a) (b)



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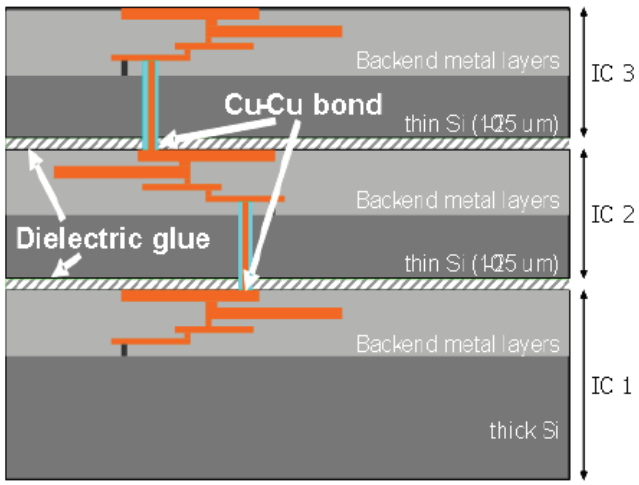


(d)

Figure 1.9: Four main bonding approaches: (a) Cu-Cu bonding [24], (b) adhesive bonding [32], (c) direct oxide-oxide bonding [18], and (d) Hybrid bonding which combines adhesive and Cu-Cu bonding method [34].

methods [34, 35]. A typical 3D integration process that uses the hybrid bonding method is illustrated in Figure 1.10. As shown, TSVs are formed using via-first TSV formation process flow. Then, device and metal layers are created, followed by the bonding stage where dies are stacked together using both Cu-Cu bonding and an adhesive glue layer. Because the top die needs to be thinned for exposing TSV tips, a handle wafer is required to provide the necessary mechanical support for the thinned die as it is very fragile [36]. This thesis focuses on the hybrid bonding-based 3D integration process, as it offers high TSV density with via-first process and good bonding quality resulting from a combined bonding fashion. The Cu-filled TSVs have good thermal conductivity, thus benefiting the thermal management of 3D design. Moreover, it is well studied regarding its electrical property [37], therefore facilitating further defect and fault modeling research [38].

Current 3D integration includes various implementation processes. To under different fabrication processed, reported methodologies from both academic and industry are summarized in Table 1.1. Besides the organizations listed in Table 1.1, extensive exploration in 3D architecture has also been done, such as quality research on 3D microprocessor design (Pennsylvania State University [3, 36, 39], Intel [25, 40]), 3D signal processing circuits (North Carolina University [41]), 3D Processor-Memory architecture exploration (NEC Electronics [28]), EDA tools (3D layout tools provided by Massachusetts Institute of Technology [6, 7], 3D floorplanning/placement tool provided by Georgia Institute of Technology [42], thermal-aware floorplanning program presented by University of California, Los Angeles [43, 44]). The first 3D products would be extremely high density memory stacks (e.g., flash memory from Samsung Electronics [45].

Table 1.1: 3D integration technologies summary (extracted from organizations across academic and industry)

Company /University	TSV size (um)	TSV process		Bonding Orientation	Bonding Method	Stacking Method	Status
		Via formation	Filling material				
Tezzaron [47]	~1.2	Via-first	W/Cu	F2F/F2B	Cu-Cu	W2W	Processor-Memory Stack
MIT Lincolin Lab [26]	1.5	Via-last	W	F2F/F2B	Oxide -fusion	W2W	3D CMOS Image Sensor [48]
IMEC [49]	5	Via-first	Cu	F2B	Cu-Cu /Hybrid	D2D /D2W	Prototype test chip
Tohoku [31]	2	Via-last	W	F2F/F2B	Metal -Metal	D2D /D2W	3D shared Memory test chip [50]
Fraunhofer IZM [17]	1-3	Via-last	Cu/W	F2B	Metal -Metal	D2W /W2W	Prototype test chip
IBM [10]	<1	Via-last	Cu	F2B	Oxide fusion	W2W	3D Prototype test vehicle
STM [18] & CEA-LETI [27]	0.75-3	Via-last	Cu	F2F	Oxide fusion	D2W /W2W	Prototype test chip
Honda [51]	-	Via first	W	F2F	Adhesive	D2W /W2W	Processor-Memory Stack [52]
RPI [35]	-	Via first	Cu	F2F/F2B	Hybrid	W2W	Prototype test chip

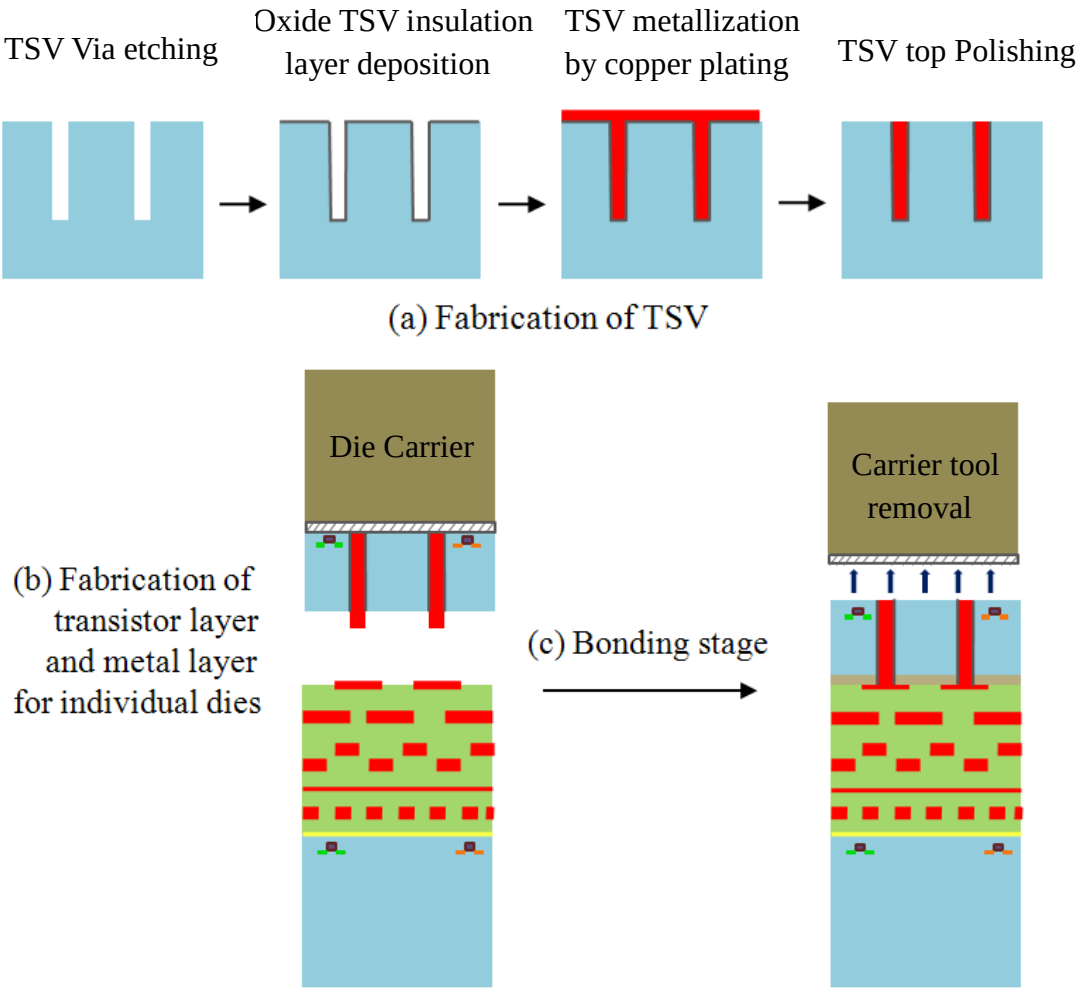


Figure 1.10: Flow chart of a hybrid bonding based 3D-ICs fabrication process [46].

1.2 Benefits of 3D-ICs

The industry paradigm shifting from conventional planar ICs to 3D-ICs is stimulated by its potential benefits. This section explains these benefits from four key aspects wirelength and interconnect RC delay, power consumption, chip footprint, and heterogeneous technologies integration, along with recently published results showing the progress.

1.2.1 Wirelength Reduction and Performance Enhancement

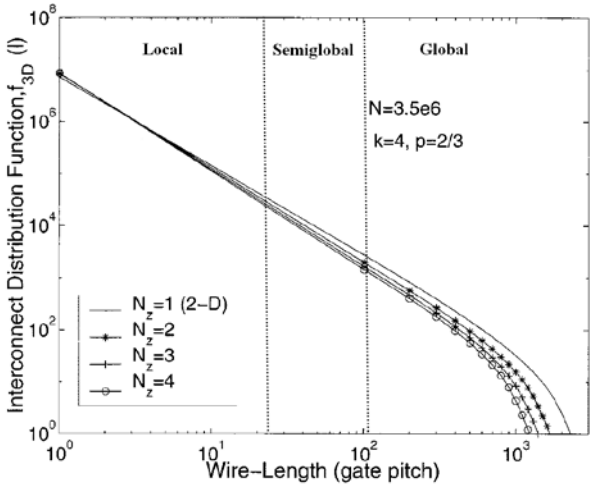


Figure 1.11: The wire-length distribution of 3D-IC for a varying number of integrated layers [53].

The intuitive benefit of 3D integration is the reduction in wirelength due to adoption of 3D stacking to shorten the long horizontal interconnects. It is investigated in a study [54] that the 3D stacking mechanism enables the wirelength to drop by a factor of square root of device layers $\sqrt{N_z}$ in the best case scenario. However, to gain a deeper observation on how 3D structure affects interconnects length. Another study [53] provided an analysis on the interconnect distribution which show how local, semi-global, and global interconnects vary across different number of device layers. An estimation of interconnect distribution of a 3D design of 3.5 million gates implemented in up to four layers is shown in Figure 1.11, where N_z=1 indicates the circuit in 2D implementation while N_z= (2, 3, 4) indicates the number of layers in respective 3D designs. Wirelength is divided into three regions which represent local, semi-global, and global interconnects respectively, as depicted in Figure 1.11. Wirelength is measured in gate pitches where gate pitch is the distance between adjacent logic gate which is equal to $\sqrt{A_c/N_{gates}}$, where Ac is the chip area, N_{gates} is the total number of gates within the design. As shown in Figure 1.11, 3D design gains little reduction in local interconnects amounts, whereas significant reduction has been achieved in number of semi-global and global interconnects. However, wire length distribution depends on the actual circuit implementation and layout methodology. By applying a placement tool [6], PR3D, proposed by Das *et al.*, on ISPD placement benchmark circuits [55], 28% to 51% reduction in total

wirelength is achieved by using two to five device-layer 3D implementation in comparison to the 2D case. During placement, a typical criterion is interconnect delay performance. Through analyzing the circuit performance of a 32-bit Fast-Fourier-Transform (FFT) datapath, an implementation of the DES cryptographic algorithm, and a 64-bit multiplier-accumulator (MAC) chip, Reference [1] reported up to 54% reduction in wire-delay performance. From layout perspective, the performance improvement of interconnect delay is also demonstrated in another study [7] for a 8-bit encryption processor mapped into 3D layout using 3D Magic [7] which is an extension of the existing layout tool Magic [56]. Similarly, 31%-58% and 28%-51% reduction in longest wire length and total wire length respectively, are demonstrated in two studies [5, 6] that employ 3D Magic layout tool.

Since 3D technology enables memories to be stacked on logic circuits, high performance microprocessor architecture can be generated by taking advantage of bandwidth increment based on processor-memory stack system [57]. The access time between cache and processors is critical to the design performance. Using 3D Cacti, a cache performance analysis tool [36], the evaluation of how to partition caches across dies in a 3D processor for maximizing the performance (delay) can be achieved. Kiran *et al*., showed that [58] a 3D implementation of a 256-entry physical register file composed of two layers achieved a 24% reduction in latency. Moreover, the clock frequency in a 3D processor can also be increased due to the higher bandwidth of 3D integration.

1.2.2 Power Reduction of 3D-ICs

The benefit of wire-length reduction not only translates into shorter wire-delay and higher bandwidth, but also into power savings, as interconnects contribute a large portion to system power consumption. The total interconnect power consumption of a chip ($P_{interconnect}$) is calculated as [59]:

$$P_{interconnect} = \frac{\alpha}{2} C_{int} (L_{total} P_{gate}) V_{DD}^2 f_{clock} \quad (1.1)$$

where α is the switching activity factor, C_{int} is the capacitance per unit interconnect length, L_{total} is the total interconnect length in gate pitches and gate pitch P_{gate}, f_{clock} is the chip clock frequency, and V_{DD} is the power supply voltage. In this expression, L_{total}, and P_{gate} refer to the interconnect dominated parameters, which will be simultaneously reduced when interconnects length drops, hence decreasing power consumption.

Meanwhile, due to smaller wirelength, the requirement of repeater associated with long global interconnects in 2D circuits can also be decreased as well. This leads to a significant reduction in total power dissipation of a design. Nevertheless, 3D integration with reduced interconnects length results in smaller wire capacitance, therefore transistor feature size and its driving current will be scaled down to achieve more overall power saving. The

interconnect power reduction is roughly determined by a factor of square root of device layers in a 3D circuit (i.e., 3D design implemented with four layers can reduce the total interconnect power by 50%) [59]. However, this is a rough estimation from system-level modeling analysis the actual result will vary according to different types of design. For instance, a register file designed for a 3D microprocessor implemented in a two-die stack and four-die stack shows 58.5% and 58.2% power reduction respectively [58]. Intel reported a iA32 microprocessor using 3D integration of two dies with simultaneous 15% power savings and 15% performance enhancement [40].

1.2.3 Footprint and Device Density of 3D-ICs

A planar IC can be partitioned and allocated on multiple dies, resulting in smaller footprint and greater device density. The ideal footprint area of a 3D design can be derived according to a shrinking factor related to the number of device layers to be stacked which can be expressed as $A_{3D}=A_{2D}/N_{layer}$, where A_{3D} and A_{2D} are the areas of the 3D and 2D chips respectively, and N_{layer} is the number of dies. However, in practice, the scaling speed of footprint area shrinking with increasing number of layers will depend on the actual layout and may not be as high as expected. Figure 1.12 shows the layouts of a 2D inverter and a 3D inverter, of which n-FET is placed over a p-FET for the 3D inverter layout. It is shown that the total area including device area and the metal routing area of the 3D inverter is 30% less than the 2D one. This also predicts that for a given footprint, significant device density increase can be achieved due to the ability of stacking circuit components. It should be noticed that chip area consists of two parts: the device area and the interconnect area. Wirelength reduction due to 3D integration also contributes to reduction in chip area. However, as device layer increases, the chip area becomes more device-limited, which means that design routing plays an important role in reducing chip area [53].

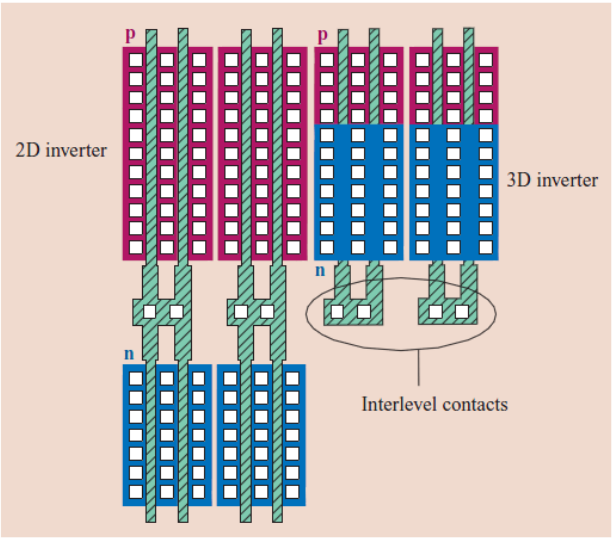


Figure 1.12: Layout of 2D and 3D inverters showing 30% areal reduction in 3D case [10].

1.2.4 Heterogeneous System Integration

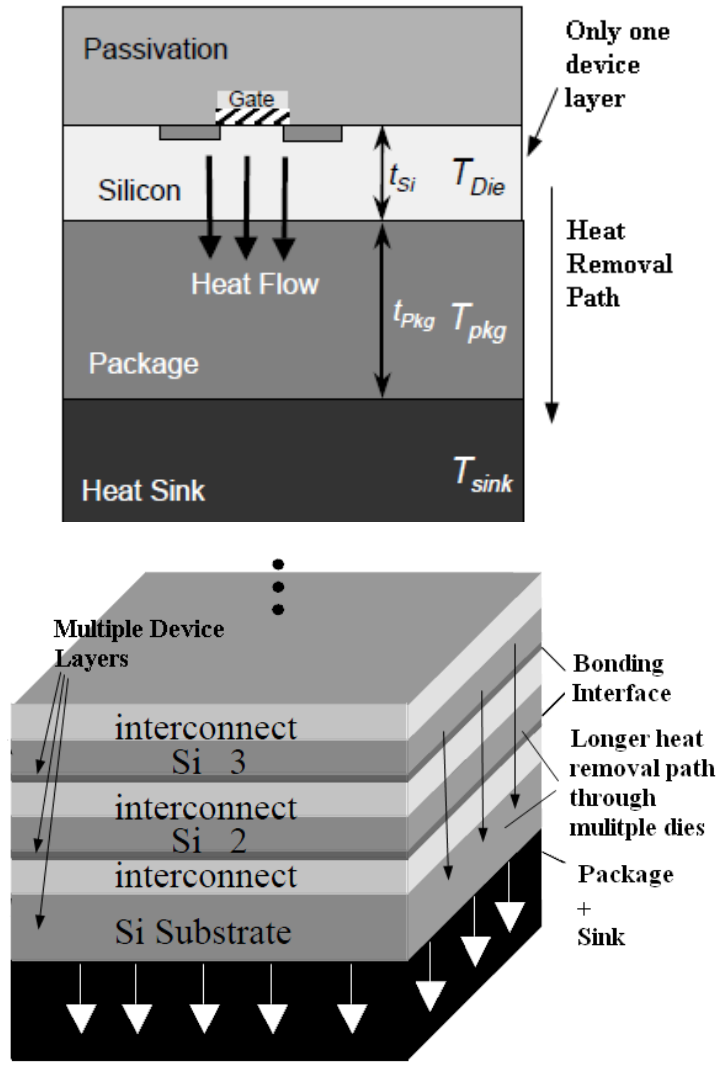
With the demand for higher functionality in a single microelectronic design, heterogeneous technologies including logic and memory, analog RF, opto-electronic, and MEMS can be integrated in a single 3D integration design. These technologies may involve different processes, hence to fabricate them on a single die is difficult and may result in malfunction during operation. However, using 3D integration, each die contains unique functional circuit which is fabricated separately, and then stacked together to form a complete system. This allows, for instance, the noise isolation between the communication of a digital circuit and a noise-sensitive RF circuit, as they are placed onto different dies with separate substrates [60]. Additionally, due to the shorter interconnects and its consequent lower load capacitance in 3D integrated circuits, the noise due to simultaneously switching events and noise-coupling between signal interconnects will be reduced, providing better signal integrity for same die or inter-die communication.

1.3 Design and Test Challenges in 3D-ICs

Even though great improvements have emerged with 3D-ICs, there are still some challenges which need to be addressed with respect to both design and testing issues. This section firstly discusses the thermal management issue in 3D integration (Section 1.3.1) and system level design exploration with respect to how to partition circuits across different layers in a 3D design (Section 1.3.2). Then 3D yield and reliability problem are explained in Section 1.3.3 and Section 1.3.4 respectively. Finally, this section discusses the testing and fault tolerance challenges of 3D-ICs.

1.3.1 Thermal Management in 3D-ICs

Similar to conventional planar IC, thermal dissipation has been addressed as a critical issue which significantly affects the system performance and reliability. However, this is more serious in 3D integration, as the power density of a 3D chip is much higher when compared to the 2D integration. Furthermore, the temperature removal path in a 3D chip is much longer than it is in a 2D one because of the stacking of multiple dies, as shown in Figure 1.13.



(a) (b)

Figure 1.13: (a) Schematic diagram of heat removal path of a planar chip [61], and (b) longer heat dissipation path of a 3D design with multiple device layers [62].

Lower thermal dissipating efficiency in 3D-ICs affects the system in three ways: Firstly, in the case of interconnect performance, the resistance of interconnects increases with higher temperature leading to a higher wire delay. This is more severe in 3D-ICs, as TSVs have bigger resistance and capacitance, thus the effect of varying temperature scales faster than it is in normal 2D designs. Secondly, the chip reliability affect system performance, particularly due to interconnects reliability. Interconnects may fail during the design lifetime due to thermal-induced reliability issue. TSV, as a new component in 3D-ICs, can have latent defects due to thermal load (e.g., crack in TSV, delamination between TSV, and its landing pad). TSV related reliability problems are discussed in Chapter 2. Thirdly, high temperature impacts chip clock performance [63]. As stated in a study [10], 15% increase in temperature decrease the clock buffer performance by 1.2% and 1.32% for SOI and bulk silicon based devices respectively. Also, high thermal gradient, namely, variation in temperature across dies affects the clock-tree performance (i.e., in the case of a 60 ℃ gradient over a 1000 um clock tree,

the clock skew will have 5% clock-driver-to-load-delay degradation, which is a considerable amount compared with nominal skew [64]. Therefore, good thermal management in 3D-ICs is critical. Early thermal optimization work for 3D NOC design has been proposed in [65, 66] for improve on-chip design reliability and computational performance for 3D NOC circuit. Recent work has been done on thermal-aware floorplanning strategies and embedded microfluid cooling channel in 3D chip, which are discussed in Chapter 2.

1.3.2 Design Exploration of 3D Architecture

3D IC design flow is different from 2D ICs because it introduces more complex task when determining components to be placed on separate device layers as it involves various partitioning granularity. Generally, there are four partitioning granularity levels: core-stacking level, core-splitting level, functional block splitting level, and logic gate splitting level. For core stacking level 3D design, entire cores are placed on different dies, therefore, most of the existing 2D design methodologies can be leveraged. Core-splitting level, where cores are split across layers while entire functional blocks are still on the same layer, this finer partitioning granularity level introduces more vertical interconnects, providing more space in wirelength reduction. In functional block splitting based 3D circuit, each functional block is divided onto different layers. At this granularity, even the functional block itself contains incomplete function prior to bonding which provide a greater challenge to validate the block function before bonding. As testing, even access to the incomplete functional circuit block is difficult. At the gate splitting level, which is the finest level of 3D circuit partitioning, design validation at this partitioning level is no longer a trivial thing. Even gate logic function is not complete prior to bonding. There is no integral logic gate on a single layer, each gate is implemented with the P-MOS transistor on one layer, while the N-MOS transistor is implemented on another layer.

The determination of partitioning strategy can be considered in line with the floorplanning and placement step to meet the various objectives and constraints, such as hardware cost (i.e., total wirelength, chip area, TSV usage, etc.), and thermal-awareness. As mentioned earlier (Section 1.2.3), placement and routing significantly affects the design wirelength and final chip area. TSVs consume more area than other devices, so the usage of TSVs should be reduced to save design cost. However, this brings a trade-off in the floorplanning/placement stage whereby more TSVs will reduce the total wirelength which is also a dominant cost factor. In a recent study [6], the wirelength reduction can be deemed from 51% to 17% if the aim of TSVs volume minimization has been taken into consideration. The floorplanning/placement strategies will become even more complicated if temperature is taken into consideration as better thermal profile of a 3D chip may require more hardware cost. Lack of EDA tools is another barrier when adopting 3D integration.

1.3.3 Yield Challenges in 3D-ICs

Yield modeling is a relatively mature topic in traditional integrated circuit design. A commonly used yield model for integrated circuits is the Poisson model [67]. It assumes defects to be point-like, and randomly distributed across the wafer. Following this, early work in yield modeling of integrated circuits assumes defects has the same distribution property. Let λ be the average number of defects on a chip, where the chip is partitioned into n small areas. The probability of having k defects on a chip P(X=k) (X denotes the number of defects) follows binomial distribution [68]:

$$P(X=k)=C_n^k \left(\frac{\lambda}{n}\right)^k \left(1-\frac{\lambda}{n}\right)^{n-k} \quad (1.2)$$

If the partitioned area is small enough to let $n\rightarrow\infty$, the probability of having X=k defects becomes the Poisson distribution which is commonly used to model chip yield that can be expressed as:

$$P(X=k) = \frac{e^{-\lambda}\lambda^k}{k!} \quad (1.3)$$

Hence, the chip yield when k=0 equals to:

$$Y_{chip} = P(X=0) = e^{-\lambda} \quad (1.4)$$

To clearly show the relationship between chip yield and chip area, we convert λ into A_cD_0, where A_c and D_0 denote the chip area and average defect rate, respectively. Thus, the chip yield can be modeled as a function of defect rate and chip area:

$$Y_{chip} = P(X=0) = e^{-A_cD_0} \quad (1.5)$$

However, Murphy claimed that the value of D_0 varies from chip to chip (area to area) [69], such that the overall yield of a chip is:

$$Y_{2D\text{-}IC} = \int_0^\infty e^{-DA_{2D-IC}} f(D)\, dD \quad (1.6)$$

where f(D) is the normalized defect rate distribution and $A_{2D\text{-}IC}$ is the overall chip area. It is found that the Poisson model is not accurate and gives a pessimistic estimation of yield, since defects tend to cluster to some extent rather than randomly distributed [70, 71]. In reference [71], the clustering effect in defect distribution is accounted for, thus the probability of having k defects is:

$$P(X=k) = \frac{\Gamma(k+\alpha)}{k!\Gamma(\alpha)} \frac{(A_{2D-IC}\beta)^k}{(A_{2D-IC}\beta+1)^{k+\alpha}} \quad (1.7)$$

Eq. (1.7) is known as the negative binomial yield formula, where $\Gamma(\alpha)$ is the Gamma function, and α and β are two distribution parameters, such that the yield of integrated circuits is:

$$Y_{2D\text{-}IC} = P(X=0) = \frac{1}{(A\beta+1)^{\alpha}} = (1 + \frac{A_{2D-IC}D_0}{\alpha})^{-\alpha} \quad (1.8)$$

where, average defect density $D_0 = \alpha\beta$, α can be regarded as the parameter to model the clustering extent in defect distribution.

To obtain the yield of 3D-ICs, $Y_{3D\text{-}ICs}$, the following aspects should be taken into consideration: 1) Individual dies to be stacked: each die can be regarded as a planar 2D chip, of which the yield can be obtained using Eq. (1.8). 2) The bonding process, for stacking n dies together, n-1 bonding procedures will take place, and each time the bonding process is implemented, this can cause yield loss to the final 3D design. 3) TSVs which undertake the vertical communication between dies, a defective TSV in any layer will damage the overall 3D chip yield.

Thus, the final yield of 3D-ICs, $Y_{3D\text{-}ICs}$, can be derived based on the cumulative yield property [72] as follows:

$$\begin{aligned} Y_{3D\text{-}ICs} &= Y_{2D\text{-}stack} \cdot Y_{overall\text{-}bonding} \cdot Y_{TSVs} \\ &= \prod_{i=1}^{N} Y_{2D-IC_i} \cdot \prod_{i=1}^{N-1} Y_{bond_i} \cdot \prod_{i=1}^{N-1} Y_{TSV_i} \end{aligned} \quad (1.9)$$

where N is the number of device layers in a 3D chip, $Y_{2D\text{-}stack}$ is overall yield of N dies to be stacked, $Y_{overall\text{-}bonding}$ is the cumulative yield of N-1 bonding procedures while $Y_{bond(i)}$ denotes the yield of the *i-th* bonding process, and Y_{TSVs} is the yield of all TSVs while $Y_{TSV(i)}$ denotes the yield of the TSVs on *i-th* layer. Note that the bottom layer does not include any TSVs.

In this thesis, we focus on improving the yield of 3D-ICs in terms of overall TSVs yield, as the other two parts in Eq. (1.9) can be improved by either a better fabrication process or the existing 2D defect tolerance technique. However, TSVs, which are new components in 3D-ICs, involve new defect types, testing challenges, and reliability issues that are elaborated in the following sections. The cost for yield improvement pays off as yield directly impacts the overall cost [73, 74], as shown in Figure 1.14. It can be seen that by introducing fault tolerance structure, the yield of TSVs can be improved thus reducing the overall cost, however, the hardware cost of a fault tolerance scheme should be accounted for as well.

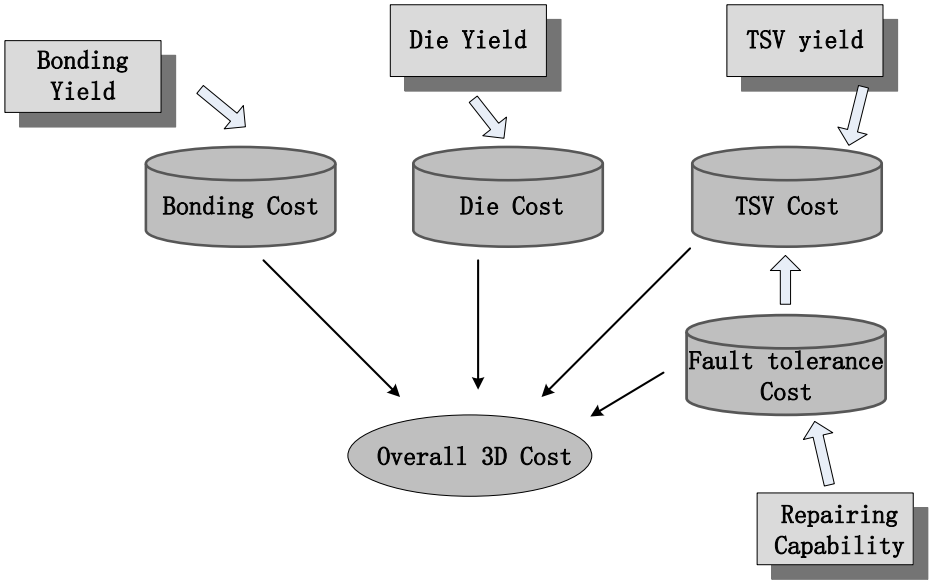


Figure 1.14: Cost factors in 3D-ICs.

1.3.4 Reliability challenges of 3D-ICs

Reliability has been acknowledged as a major concern when moving from traditional IC design to 3D-ICs. This is mainly due to two reasons: 1) Firstly, devices (transistors) and interconnects on individual dies to be stacked suffer critical reliability issue due to higher thermal density and lack of efficient thermal dissipation path, particularly for the devices and wires placed on the top die. 2) The TSV interconnect itself introduces new defect mechanisms due to imperfect fabrication process or thermal load during operation. Since 3D integration is composed of traditional components (transistors and horizontal wires) and newly introduced TSVs, the reliability issues related to each part in 3D chip are shown in Figure 1.15. As can be seen that Electromigration (EM) and thermal-induced stress are two main driving force under thermal stimulation that cause reliability problems.

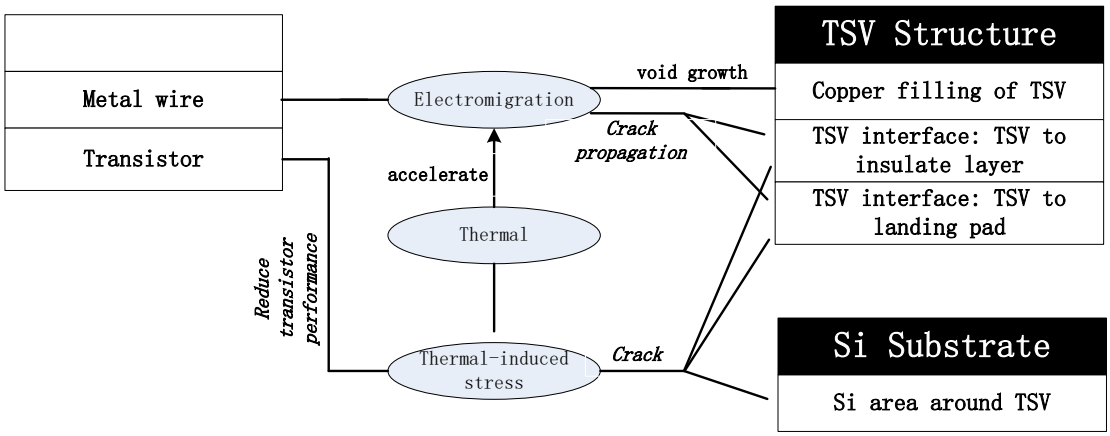


Figure 1.15: Different positions in a 3D structure that suffers from reliability issue.

Horizontal wire interconnects (2D) (Figure 1.15) involve the EM problem as in 2D integrated circuits. Electromigration is the gradual displacement of metal atoms in a semiconductor. It occurs when the current density is high enough to cause the drift of metal ions in the direction of the electron flow, and is characterized by the ion flux density. There are two failure mechanisms caused by EM [75]: 1) void in metal wires, due to the outgoing ion flux exceeds the incoming ion flux, resulting in an open interconnect defect, and 2) hillock (short circuit) that creates short between interconnects because the incoming ion flux exceeds the outgoing ion flux. The EM phenomenon is mainly affected by current density and temperature. Black *et al*. [75] claimed that the meantime to failure (MTTF) of a metal interconnect subjected to EM effect can be expressed as:

$$MTTF = \frac{A}{J^N} \exp^{\frac{E_a}{k\,T}} \qquad (1.10)$$

where the parameters of the equation are defined as:

A	Cross-section area-dependent constant
J	Current density
N	Scaling factor, usually set to 2
E_a	Activation energy for electromigration
k	Boltzmann constant
T	Temperature

A study [76] has shown, however, that Black's equation can be improved to take stress gradient induced migration and atomic migration due to atomic concentration gradient into consideration.

Performance of transistors (Figure 1.15) placed near TSVs is affected by TSV-induced thermal mechanical stress [77, 78, 79]. Such stress is induced due to the mismatch between coefficients of thermal expansion (CTEs) of copper-filled TSV and silicon substrate around TSVs, as the CTE of copper is $17*10^{-6}$ K^{-1} at 20℃ and the CTE of Si is $3*10^{-6}$ K^{-1} at 20 ℃. An analytical model of TSV stress-induced mobility variation in [78] indicated that the tensile stress on silicon can change mobility of carriers, where the hole mobility of PMOS transistors can vary from -22% to +10% while the electron mobility of NMOS transistors can increase up to +24%, causing more than 20% variation for single cell delay. Moreover, if cells on a critical path are placed near TSVs, the path delay will be affected as well. However, carrier mobility change not only depends on TSV-induced stress but also on the orientation between the stress and the channel position in PMOS/NMOS transistor. By taking this into consideration, recent work in [78] proposed a layout algorithm that can improve the cell delay and critical path delay by 14% and 6.5% respectively, where results are obtained from the presented analytical model. It should also be noted that during cell placement, it is suggested that cells are placed at a minimum distance from the TSVs which is implied by the

Keep-out-Zone (KOZ) [80]. A larger KOZ can reduce the impact of TSV stress on surrounding cells, however, it costs higher area overhead. This trade-off is analyzed in [80] when guiding the overall 3D placement strategy. Moreover, when considering the TSV-induced stress, the work presented in [78] and [80] do not consider the isolation layer between TSV and the silicon substrate which is formed by silicon oxide (SiO_2), of which the CTE is $0.5*10^{-6}$ K^{-1} at 20 ℃ and lower than that of both TSV and Si substrate. By taking this into account the timing variation of cells can be as much as ±15% [79].

TSV structure, as a new component in 3D integration, can introduce new reliability challenges in four aspects (Figure 1.15): Firstly, the imperfect TSV formation process can introduce a void inside the TSV, and void growth can be driven by EM effect [81], moreover, this EM effect will be accelerated by temperature load during operation. Secondly, due to the mismatch of CTE between TSV and silicon, the thermal-induced stress can drive crack growth between isolation dielectric layer and silicon substrate [79, 82]. This interface crack is analyzed in a study [83] by taking the impacts of TSV pitch, KOZ size, TSV dimension, dielectric layer thickness, and TSV placement. It is known that such a TSV isolation layer crack should be considered from the full-chip scale, incorporating multiple TSV structure influence instead of a single TSV. Thirdly, cracks can happen at the TSV interface between TSVs and its landing pad leading to delamination defect due to the thermal-induced stress during fabrication or normal operation [84, 85, 86]. For a TSV interface that employs microbumps, studies [87, 88, 89] show that its reliability is also at risk due to both TSV-induced stress and EM effect, and cracks can occur in the joints [90, 91]. Lastly, due to the large size discrepancy between TSVs and the connected metal wires (Figure 1.16), the current density in the metal interconnects is much larger than it is in TSVs, leading to a serious EM issue [92, 93]. Meanwhile it is shown by reference [93] that thermal-induced stress is the dominant contribution factor to EM performance rather than current density. Electromigration is modeled at the joint between wires and TSVs (landing pad) in reference [94] for investigating the impact of size of a TSV and its landing pad.

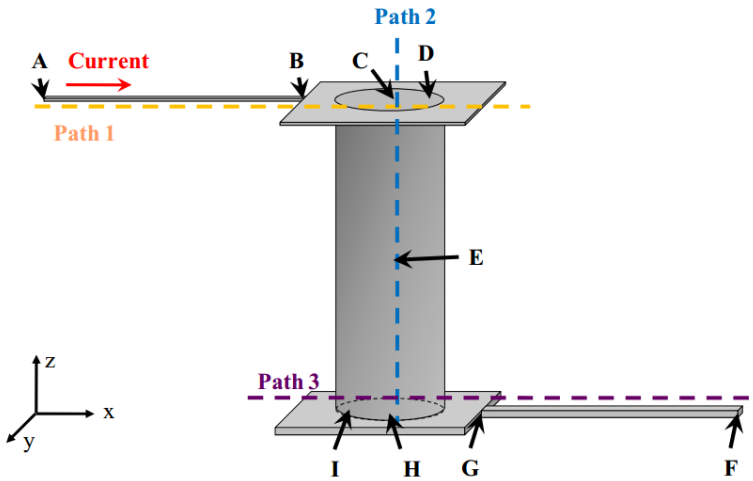


Figure 1.16: Illustrative diagram of metal layers connected to a TSV structure containing TSV and its landing pad.

1.3.5 Testing and Fault Tolerance for 3D-ICs

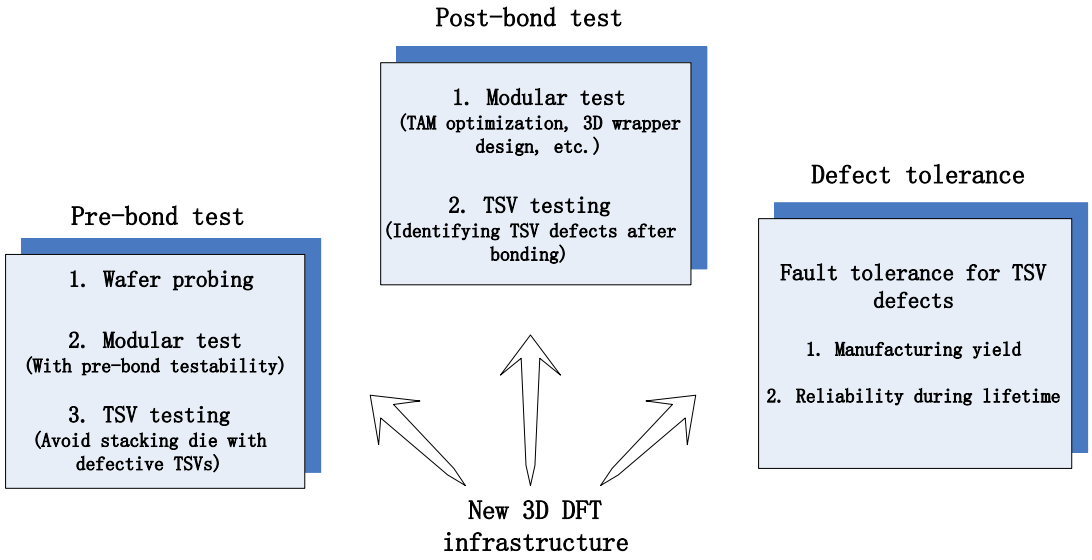


Figure 1.17: Testing and fault tolerance issues of 3D-ICs.

As can be seen in Figure 1.17, 3D-ICs involve various yield and reliability issues. Thus, fault detection and tolerance mechanisms are essential for 3D-ICs. Providing testability for 3D-ICs comprises three stages: pre-bond test, post-bond test and fault tolerance (Figure 1.17). Pre-bond testing undertakes defect detection for individual dies to be stacked before they are bonded together, which ensures that dies to be stacked are known-good dies (KGDs), while post-bond testing is used to ensure that all partitioned circuits across dies work properly. Additionally, post-bond test also targets testing of vertical interconnects defects (i.e. TSVs defects) as defects can be introduced during bonding stage. However, it is not trivial to implement pre-bond and post-bond tests, as a great deal of work needs to be investigated regarding new die probing equipment, new test infrastructure design, new test access optimization scheme, and etc. Moreover, as TSVs are critical to the 3D system, providing fault tolerance scheme for TSVs will significantly increase the yield of 3D-ICs and extend the design lifetime.

Pre-bond testing – Firstly, for pre-bond testing, the wafer probing poses many challenges. It is extremely different to probe TSVs directly due to their tiny size and access ability. Current probing technology requires a minimum pitch of 35um, however, a TSV has a diameter size of 5um and pitch size of 10um [21]. Also, the probe force is too large for thinned wafers to be probed, low contact force is necessary as the thinned wafer is fragile [95]. A possible solution is to introduce contactless probing based on capacitive or inductive coupling [96, 97]. Secondly, because 3D design has different partitioning granularities which split and place partitioned cores or functional blocks on different dies (as discussed in Section 1.3.2), such that it is difficult to implement pre-bond testing on these partial circuits without complete functionality. A scan-island based test method has been developed in recent study [98], to

achieve the pre-bond testability for split cores (i.e., functional blocks spread across multiple dies) by employing a dedicated controller and scan chains on each die. For circuits partitioned at a finer level, such as split adder or register file, Dean *et al*. [99] proposed a test methodology using a partitioned eight bit Kogge-Stone adder and a port-split register file, to investigate the pre-bond testability at functional block splitting level. Finally, testing of TSVs prior to bonding has to be investigated. Since prior to bonding a TSV only has one end, it is difficult to detect defects of this single end component. Moreover, the test circuits which are dedicated to pre-bond testing of TSVs may become useless after the bonding stage and manufacturing stage of a 3D chip [19]. Some recent published work on pre-bond testing of TSVs is reviewed in Section 2.3.

Post-bond testing – Post-bond testing should be incorporated to ensure the function of both blocks placed across dies and the TSVs between dies. Firstly, new test infrastructure and optimization methods (with new objectives, e.g., TSV usage) are required for post-bond testing when employing modular test in 3D design, such as TAM optimization and wrapper design for a 3D system [100, 101]. Xie *et al*. [102] developed an integer-liner-program (ICP) based algorithm to minimize the test time under a constraint of TAM width and TSV usage. Besides TAM optimization, a IEEE.Std.P1500 wrapper design methodology is proposed in reference [103] to minimize the length of wrapper chain under a constraint of TSVs number. Secondly, post-bond TSV testing is inevitable, since pre-bond TSV testing does not scale well when TSVs suffer from defects during bonding process or thermal-induced latent defects in use. Prior work on both pre-bond and post-bond TSV testing is studied in Section 2.3. Note that post-bond testing should be implemented for n-1 times for a design with n stacked dies [21].

Fault tolerance – Even though pre-bond and post-bond TSV testing can avoid the case of bad dies being stacked on good dies. Without fault tolerance schemes, the cost due to dumping bad dies with defective TSVs can still be high, particularly for 3D design with high TSV density and high defect rate. There are two main fault tolerance methods for implementing fault tolerance for TSV-based 3D-ICs: 1) Fault tolerance technique that is implemented without using redundant TSVs, such as signal recovery for faulty TSVs. In a recent study [104], each TSV is connected to a built-in-self-test/repair block, targeting detection of a short TSV defect causing signal degradation. Once a defective TSV is found, the output signal of that defective TSV is recovered through using of a dedicated level converter circuit embedded in the self-repair circuit. This method eliminates the usage of redundant TSVs, however, the tuning of the level converter circuit will affect the signal recovery quality. Moreover, fault tolerance method presented in reference [104] has a limitation that if the defect size in a TSV exceeds the tolerant range, such defective TSV cannot be repaired. 2) TSV repair with TSV redundancy [105, 106, 107, 134], where redundant TSVs are employed to replace the defective ones. It is acknowledged that TSV repair can be realized at two stages: One is for improving the TSV yield by repairing defective TSVs after manufacturing test that provides a defective TSV map. This stage is relatively simple for implementation because it does not

have to consider the repair task for latent defect tolerance during the lifetime of the design. The other stage is for in-field reliability to extend design lifetime, which can tolerate the TSVs aging defects. Existing fault tolerance work in terms of TSV repair for improving yield and in-field reliability are discussed in Section 2.4.2 and Section 2.5.2 respectively.

1.4 Motivation and Thesis Outline

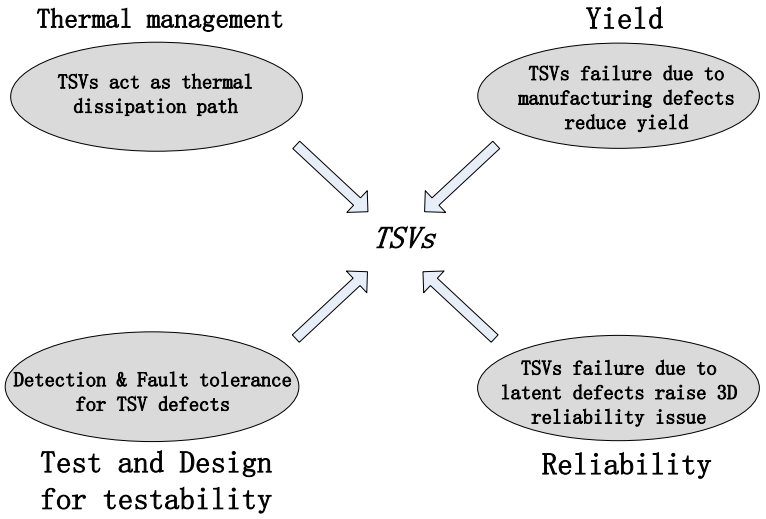


Figure 1.18: Illustration of critical issues in 3D-ICs that are related to TSVs.

As a concluding remark after the discussion about critical issues in 3D-ICs, it is easy to establish that TSVs play a critical role related to thermal management, yield and reliability, and testing challenges of 3D-ICs, as illustrated in Figure 1.18. Existing work revealed that voids inside the TSV [109] and TSV short to substrate defect [110] are two main TSV manufacturing defect types [38, 104, 111, 112], which cause significant yield loss thus increasing the manufacturing cost. Although, in conventional planar design, open and bridge defect of interconnects are well studied, testing of TSV voids and short to substrate defects raise new challenges to be explored. Meanwhile, as TSV is a major cost of 3D integration, when employing TSV redundancy for TSV repairing, we have to examine the trade-off between TSV usage and the yield improvement brought by redundant TSVs. Furthermore, 3D chip involves a critical thermal issue, and latent defects such as void growth and delamination between TSV and its landing pad can happen during its lifetime resulting in 3D reliability challenges. All these problems motivate this thesis to develop high quality and cost-effective solution for improving yield and reliability of 3D-ICs.

The rest of the thesis is organized as follows:

Chapter 2 presents a literature review on TSV defects modeling, existing testing methodology for TSV defects, and existing work on improving yield and reliability from design and test

points of view respectively. This chapter also outlines a number of important research problems that are addressed in this thesis to develop a cost-effective fault tolerance scheme for TSV-based 3D-ICs.

Chapter 3 presents a redundant TSVs grouping technique, which partitions regular and redundant TSVs into groups. For each group, a set of multiplexers is used to select good signal paths while avoiding defective TSVs. Probabilistic models for yield analysis under the influence of independent and clustering defect distributions are proposed to investigate the impact of grouping ratio (regular-to-redundant TSVs in one group) on trade-off between yield and hardware overhead. Simulation results show that for a given number of TSVs and TSV failure rate, careful selection of grouping ratios lead to achieving 100% yield at minimal hardware cost, in comparison to a design that does not exploit TSV grouping ratios.

Chapter 4 presents the design, validation and evaluation of an efficient online fault tolerance technique for fault detection and recovery in the presence of three TSV defects: voids, delamination between TSV and landing pad, and TSV short-to-substrate. Unlike the work presented in Chapter 3, where the TSV repair is only for yield improvement, the proposed fault tolerance technique also copes with in-field reliability concern. The proposed efficient technique requires a small (2 x number of TSVs per group) number of clock cycles for fault detection and recovery. Simulations using HSPICE and ModelSim are carried out to validate fault detection and recovery. Results show that regular and redundant TSVs can be divided into groups to minimize area overhead without affecting fault tolerance capability of the proposed technique. Synthesis results using 130-nm design library show that 100% repair capability can be achieved with low area overhead (4% for the best case).

Chapter 5 presents a scheme with joint consideration of temperature mitigation and fault tolerance for TSV based 3D ICs, as TSV failures due to manufacturing defects and thermal-induced latent defects result in yield and reliability issues in 3D-ICs. This is achieved by reusing spare TSVs that are frequently deployed for improving yield and reliability in 3D ICs. The spare TSVs are placed in such a way that temperature is reduced without affecting fault tolerance capability, since TSVs are effective in reducing temperature by providing thermal conductivity. The proposed scheme consists of two steps: The first step is TSV determination step, which provides optimised allocation between regular and spare TSVs into groups to achieve expected repair capability. The second step is TSV placement, where temperature mitigation is targeted while optimizing total wirelength and route difference, where route difference takes into account the additional routing overhead due to transferring signals from regular to spare TSV as in the case of bypassing a defective TSV. Results show that, using the proposed technique, 100% repair capability is achieved across all (five) benchmarks with an average temperature reduction of 34.1% (75.2℃) (best case is 58.5% (99.8℃)), while increasing wirelength and route difference by a small amount.

Chapter 6 summarizes the contributions presented in this thesis along with the description of how the objectives of this research have been achieved. This chapter also outlines research issues that merit further investigation to develop efficient and cost-effective solutions for improving yield and reliability of future 3D integrated circuits.

1.5 Publications

Contributions of the research work presented in this thesis have been published as follows:

1. Y. Zhao, S. Khursheed, B. Al-Hashimi, “Cost-Effective TSV Grouping for Yield Improvement of 3D-ICs”, *Asian Test Symposium*, 2011

2. Y. Zhao, S. Khursheed, B. Al-Hashimi, “Online Fault Tolerance Technique for TSV-based 3D-IC”, *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 2013.

3. Y. Zhao, S. Khursheed, B. Al-Hashimi, “Joint Consideration of Fault Tolerance and Temperature Mitigation for TSV-based 3D-ICs”, *DATE*, 2015 (Under review)

Chapter 2

Literature Review

This chapter presents a detailed literature review of the state-of-the-art research that is related to this thesis and that has been carried out in recent years. Figure 2.1 shows the structure and main topics covered in this chapter. As can be seen, before looking into the yield and reliability issues of 3D-ICs, the fundamental work of TSVs characterization and modeling is firstly studied in Section 2.1. This is followed by a description of the electrical models of major TSV defect types: such as voids, delmination between TSV and its landing pad, and TSV short to substrate. Section 2.3 summarizes the available testing techniques targeting these types of TSV defects. As discussed earlier (Section 1.3.5), 3D testing strategies can be applied at pre-bond and post-bond stage. In Section 2.3 TSV testing under both testing strategies are investigated. Published work on techniques for improving yield and reliability of 3D-ICs is reviewed from both design and test perspective in Section 2.4 and Section 2.5 respectively. Finally, Section 2.6 identifies the gaps in recent research and outlines the research objectives of this thesis in light of reviewed research. Note that, to complement this literature review, each of Chapter 3, 4, and 5 has its own brief literature review along with the contributions described in these chapters.

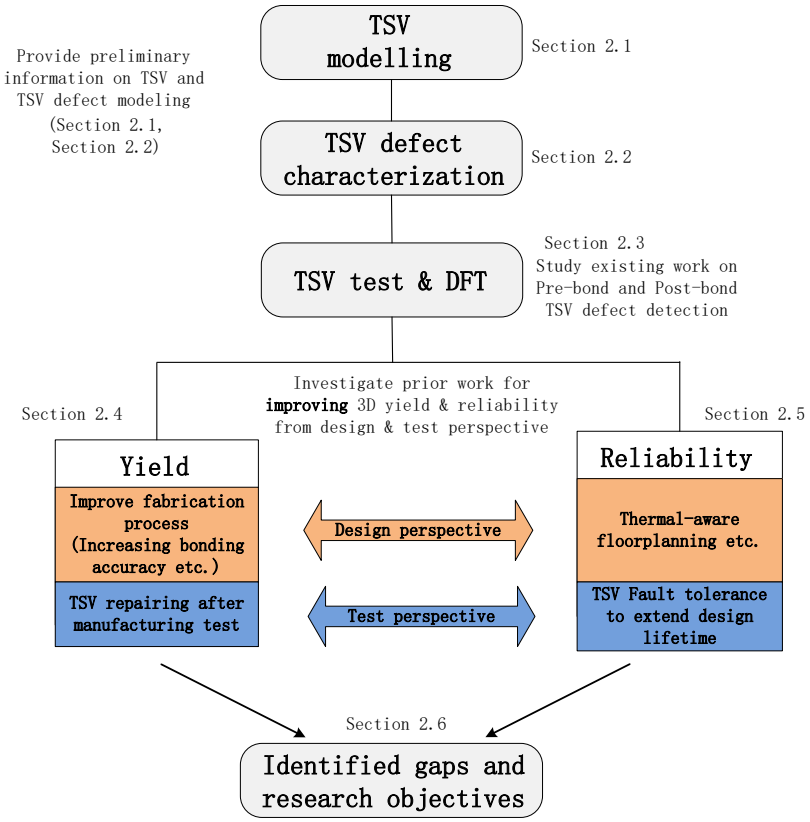


Figure 2.1: Summary of reviewed problems in Chapter 2.

2.1 TSV Modeling

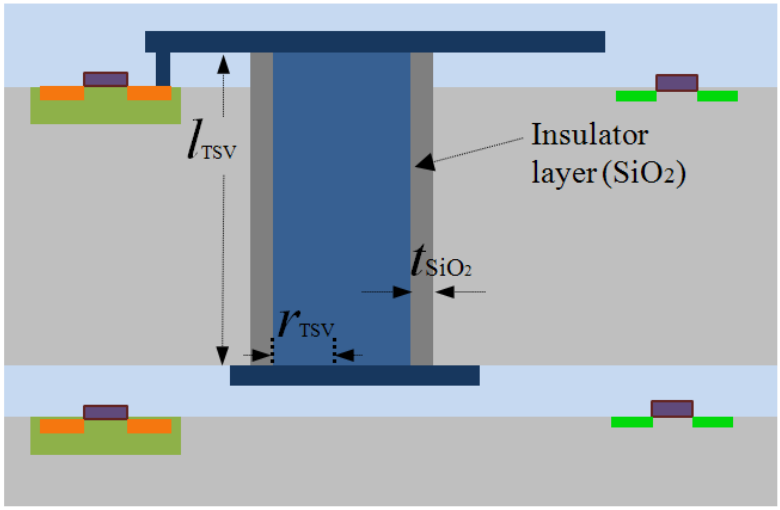


Figure 2.2: A general schematic diagram of TSV architecture.

A number of studies have shown that TSV can be modeled using its physical dimensions and material characteristics. Resistance (R_{tsv}) and Capacitance (C_{tsv}) should be derived to observe the equivalent circuit of TSV using a lumped RC model. The analytical expression of the resistance of TSV (R_{tsv}) and capacitance of TSV (C_{tsv}) are given by [37]:

$$R_{tsv} = \frac{\rho\, l_{tsv}}{A_{tsv}} = \frac{\rho\, l_{tsv}}{\pi\, r_{tsv}^2} \tag{2.1}$$

$$C_{tsv} = \frac{2\,\pi\,\varepsilon_{SiO\,2}\, l_{tsv}}{\ln\frac{(t_{SiO\,2}+r_{tsv})}{r_{tsv}}} \tag{2.2}$$

where ρ is the resistivity of the TSV conducting material, in this work, copper is used as commonly used in practice [113], A_{tsv} represents the area of the TSV bottom side, r_{tsv} and l_{tsv} are the radius and length of TSV respectively (Figure 2.2), ε_{SiO_2} is the dielectric constant of the SiO_2 isolation layer between TSV and Si substrate, and t_{SiO_2} is the thickness of the dielectric isolation layer. Eq. (2.1) implies that any defects that lead to change in r_{tsv} and l_{tsv} can be a resistive defect. The capacitance equation (Eq. (2.2)) shows that C_{tsv} is directly proportional to the length of TSV and inversely proportional to the TSV dielectric layer thickness, which implies that the defect in the dielectric layer can cause conductor defect resulting in change of C_{tsv}. With the modelling of TSV resistance and capacitance, the equivalent circuit of TSV can be achieved based on T-model [37] which is widely used in modelling the interconnect in 2D circuit, as illustrated in Figure 2.3(a), where R_{pull} denotes the pull-up resistance of the driving gate.

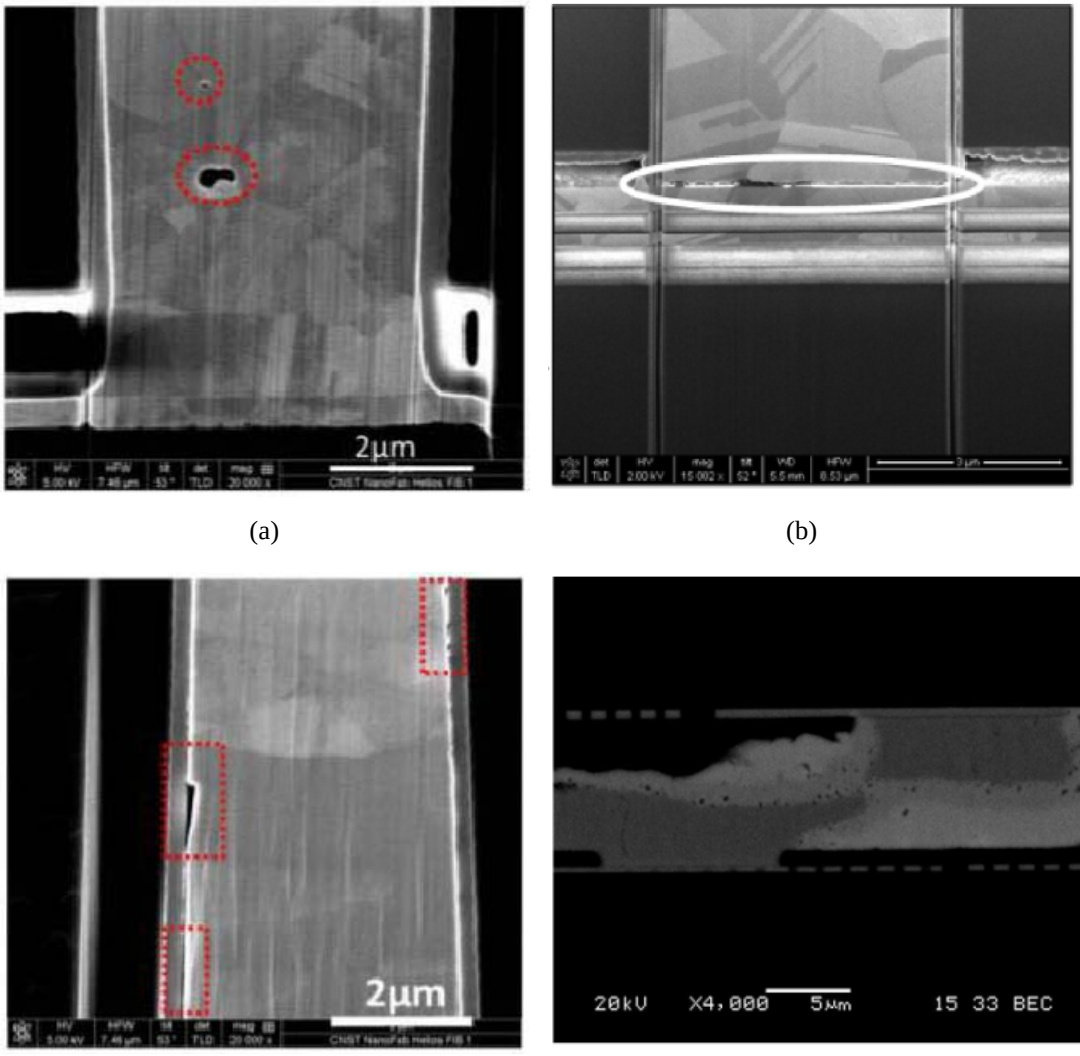
2.2 TSV Defects Characterization and Modeling

In a recent study [114], various types of TSV defects are investigated, some are due to the imperfect fabrication process, while others can happen during the lifetime of 3D design. By applying manufacturing test, some invisible small defects that may escape the detection process can be identified. Nevertheless, these invisible defects may become large enough to cause system malfunction due to thermal and mechanical stress as discussed in Section 1.3.4. Table 2.1 shows four important TSV defect types. For those manufacturing defects that may become latent defects, the stimulus turning them into latent defects are also shown.

Table 2.1: Four TSV defect types summary.

Defect	**Reason** (during fabrication)	Conversion to **latent defect**		**Characterization**
		Possibility	Reason (in use)	
Void	Insufficient plating/filling [109]	Yes	void growth due to electromigration (EM)	TSV resistance increase
Short to substrate	Non-conformal sidewall deposition [115, 116]	Yes	crack induced by thermal-stress due to mismatch in coefficient of thermal expansion (CTE) of TSV structure	Leakage from TSV to Si substrate (short path)
Delamination	Thermal-stress due to mismatch in CTE of TSV structure [84, 86]	Yes	crack growth due to EM/thermal-stress	TSV resistance increase
Misalignment	Weak bonding accuracy [117]	-	-	TSV interface contact resistance increase

* Note that this table can be linked with Figure 1. 13 which shows 3D reliability issues, nevertheless, this table provide details of the defects that occurred in TSV structure (Figure 1.13) from both manufacturing defect and latent defect points of view.



(a) (b)

(c) (d)

Figure 2.4: Examples of TSV defects: (a) Void inside TSVs [118], (b) Delamination at bottom of TSV [119], (c) TSV short to substrate defect (Crack in sidewall of TSV) [118], and (d) Misalignment at TSV bonding interface [120].

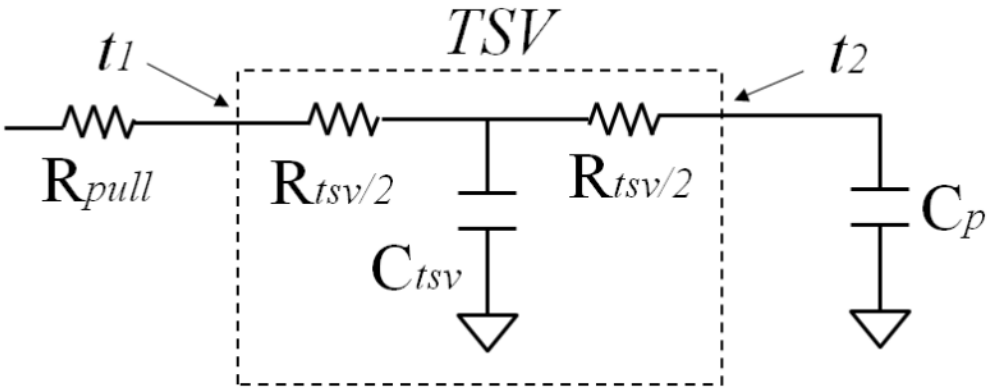
Void inside TSVs (Type I) can result from an imperfect TSV fabrication process such as insufficient via copper doping [109]. Void growth driven by electromigration can happen during operation converting small voids inside TSVs into a bigger void. A detailed TSV failure analysis [118] revealed that after 2000 thermal cycles, a void with ~0.5um width is found inside the TSV structure (Figure 2.4(a)). Note that a thermal cycle is defined as driving the sample circuit from 30 ℃ to 150 ℃ and this then cooled back to 30 ℃ in five minutes [118]. This type of defect increases the TSV resistance [121] and causes a delay fault.

The second type of defect is delamination at the TSV interface, as shown in Figure 2.4(b), which usually occurs between TSV and its landing pad. This type of defect is either due to voids existing at the bottom of the TSV (Figure 2.4(b)) or cracks caused by thermal-induced stress during operation. Delamination also causes TSV resistance to increase, such that

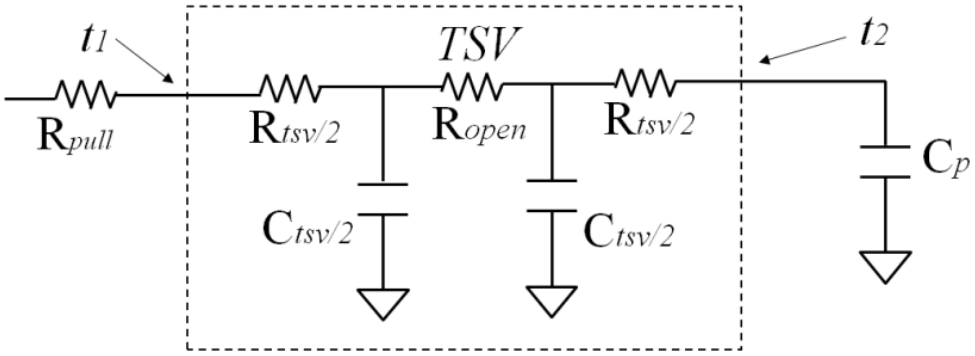
delamination between TSV and its landing pad and void inside TSV are modelled as the same type of open resistive defect. The equivalent electrical model of void/delamination TSV defect is shown in Figure 2.3(b). It can be seen that a resistor (R_{open}) is added to the TSV model (Figure 2.3(a)). HSPICE description of void/delamination TSV defect is in Appendix A. Note that C_p denotes the parasitic capacitance of the circuit and it is assumed that signal is transmitted from TSV terminal in die 1 (referred as terminal *t1*) by a driving gate to the TSV terminal in die 2 (referred as terminal *t2*).

The third type of TSV defect is TSV short to substrate defect, in which the sidewall isolation layer between TSV and Si substrate is broken due to either a non-conformal isolation layer or Cu diffusion from TSV to Si substrate [116]. Moreover, a small crack in TSV sidewall can become a large crack due to thermal-induced stress due to CTE (coefficient of thermal expansion) mismatch in TSV material (copper) and sidewall material (SiO_2). Results reported in reference [118] show that after 1000 thermal cycles, cracks can be found at the TSV sidewall. Most of the cracks are pin-hole like, while the largest crack has a length of ~0.35um (Figure 2.4(c)). This type of defect forms a short path between TSV and substrate, leading to leakage when transmitting signals. The electrical equivalent of this defect is shown in Figure 2.3(c) [104]. A resistor, denoted by R_{short}, is added to the TSV model (Figure 2.3(a)), which represents the leakage current path between TSV and substrate and reduces the TSV charging current. HSPICE description of this type of TSV defect is in Appendix A.

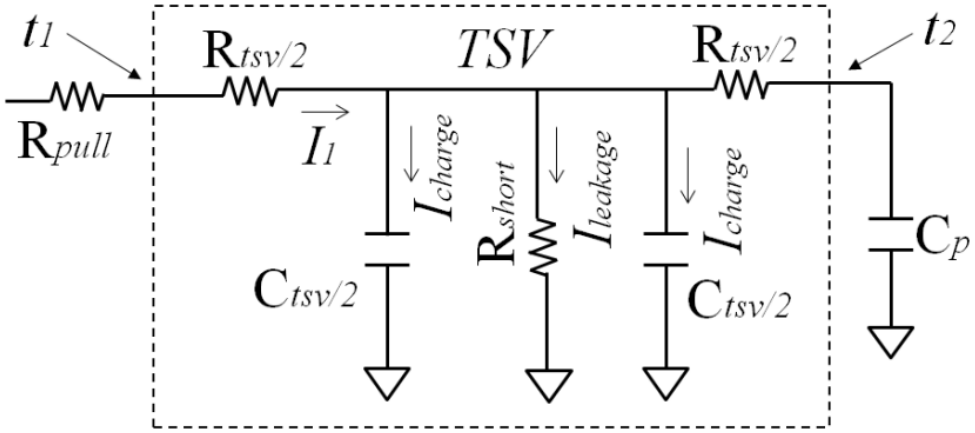
The last type of TSV defect is misalignment due to inaccurate bonding process (Figure 2.4(d)), which increases the contact resistance at the TSV bonding interface because misalignment reduces the contact area between TSV and its landing pad. Note that, for the TSV structure using micro-bump for bonding, misalignment increases the resistance as well. Misalignment can be addressed by improving the bonding accuracy as shown in [117]. Thus, in this research, we focus on void, delamination, and short to substrate TSV defect types. Note that there are some other TSV defect types that differ in their physical mechanisms, for example a crack at the microbump and a crack at the edge of TSV structure corner [114]. However, as studied in [91], their properties at logic level are similar to the defects listed in Table 2.1, which means that they can be modelled in the same way using the equivalent circuit models shown in Figure 2.3 and can be detected and repaired using the methods proposed in this thesis.



(a) TSV T-model [37]



(b) Equivalent circuit model: Void/delamination defect [121]



(c) Equivalent circuit model: TSV short to substrate [104]

Figure 2.3: Electrical equivalent circuit models for TSV with defects. Note that HSPICE description of these models is shown in Appendix A.

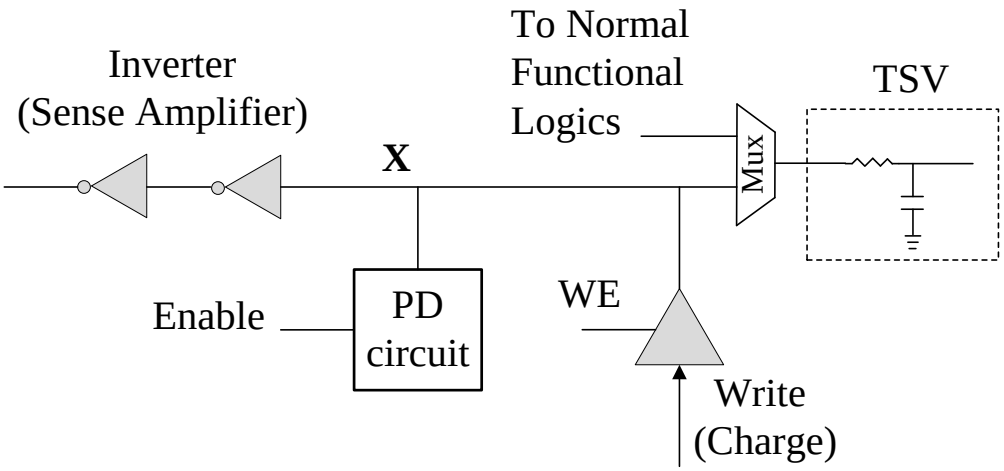
2.3 TSV Defect Testing

As discussed in Section 1.3.5, testing of 3D-ICs can be implemented at two stages: pre-bond testing and post-bond testing. This applies to TSV testing as well. Pre-bond testing of TSV ensures that dies to be stacked contain only good TSV interconnects. However, as TSVs prior to bonding are not integrated within a complete signal path, such a TSV is a single end component, requiring new test mechanisms. Moreover, post-bond TSV testing is equally important as thermal-induced latent defects occur after dies are bonded together.

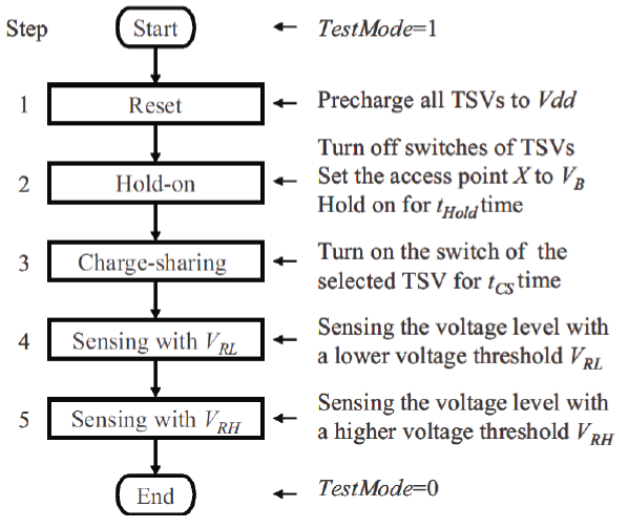
TSV open defect (void or delamination) and short to substrate defect (crack in TSV sidewall) are targeted in recent research from the pre-bond test perspective [104, 112, 115, 122, 123]. Chen *et al*. [115] presented an on-chip sense amplification methodology for detecting capacitive TSV faults due to open cracks inside TSVs. Since the TSV at the pre-bond stage only has a single end. Chen *et al*. [115] focused on the capacitance floating due to open crack. As shown by Eq. (2.2), TSV capacitance is reduced as the effective TSV length is decreased due to crack. The test infrastructure and testing flow are shown in Figure 2.5(a) and Figure 2.5(b) respectively. Each TSV is regarded as a DRAM cell that will be charged and discharged. The charging unit and pull-down network for discharging is shown in Figure 2.5(a). Since the discharge time can be manipulated and pre-determined, the capacitance of TSV will determine the voltage at node X (Figure 2.5(a)) after it has been discharged for a pre-set t_{cs} period. In the meanwhile, a tuned sense amplifier determines whether the voltage at node X is within an acceptable range, thus reflecting whether the TSV capacitance falls into an unaccepted range. However, this technique is limited because the bounds on TSV capacitance must be pre-defined. The test quality of this method is sensitive to the circuit environment as well because the error due to unstable circuit variability results from process variation must be considered. Another method for pre-bond testing of TSV capacitive defects is proposed in a recent study [112], which employs a capacitor bridge for each TSV to test the change in TSV capacitance. The capacitance of the TSV is compared with a on chip reference capacitor to determine whether it is defective or not. However, this method requires a large area overhead for each single TSV testing and uses many analog elements such as capacitors which affect test quality. Additionally, with the process variation, the reference capacitor is also an uncertain factor for testing.

For testing short to substrate defects in the pre-bond stage, some work has been done in reference [104], where a voltage divider is connected to a TSV, as shown in Figure 2.6. It can be seen that the voltage at node OB is divided between the short resistor due to short to substrate TSV defect and the on resistance of the inverter (TSV-Test-Inverter) (Figure 2.6). To determine whether the short to substrate defects exist, the voltage at node OB is compared with a reference voltage through a dedicated voltage comparator. Obviously, this method requires a large number of additional circuits for testing each TSV. The need for tuning the voltage divider and analog voltage comparator impacts on the test accuracy. Furthermore, this testing method [104] only detects large TSV defect size that results in significant signal

degradation at node OB (i.e., signal integrity is dramatically decreased when passing from one end to the other).



(a) Sensing amplification circuit for pre-bond testing of TSV capacitive defects [115].



(b) Test flow for sensing amplification circuit based method [115].

Figure 2.5: Pre-bond test mechanism for TSV capacitive defect, infrastructure and test flow.

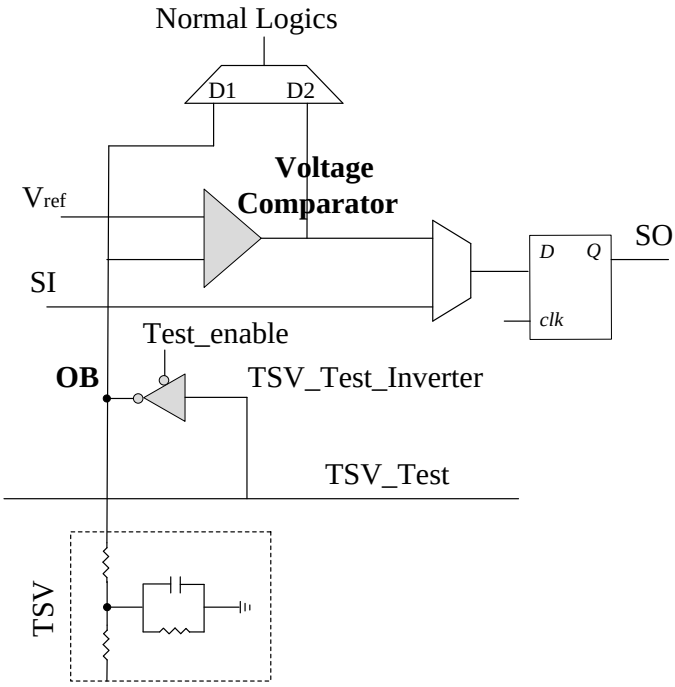


Figure 2.6: Pre-bond test infrastructure for TSV short to substrate defect [104].

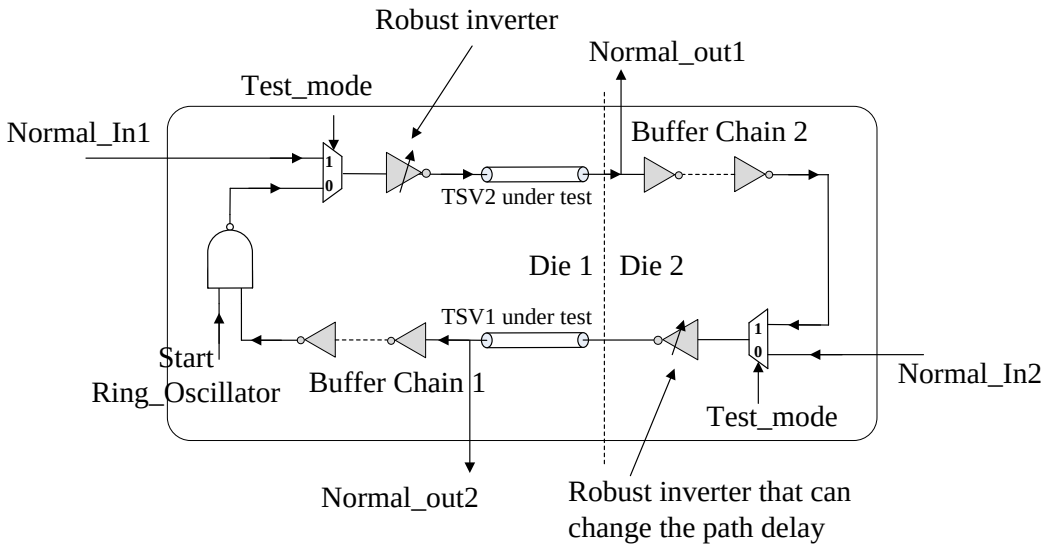


Figure 2.7: Ring Oscillator Structure for testing of small delay TSV defects [123]

In terms of the post-bond testing of TSV, existing work has focused on the delay fault caused by the resistive open defects of TSV such as void and delamination [122, 123]. A ring oscillator is used for TSV delay fault detection [123]. The proposed Ring Oscillator structure is illustrated in Figure 2.7, which is composed of two buffer chains (one on the top layer and another on the bottom layer) and two TSVs under test. The length of each buffer chain can be manipulated through some peripheral control circuits connected to the buffer chain. By measuring the difference in delay of the buffer chains, the difference in delay between the two

TSVs can be addressed, thereby addressing the potential defects in TSVs. However, this method uses a large number of additional components for detecting two TSVs at a time. In reference [122], resistive open defects of TSVs are also evaluated, with the consideration of IR-drop issue taken into account by carefully placing the probe-pads. For testing both resistive open and short to substrate TSV defects, a cost-effective test method which is based on the delay test is presented in Chapter 4.

As can be seen, the testability of the above methodologies is limited as available methods require large area overhead. The total amount of on-die area used for TSV defect detection grows with the number of TSVs. Since TSVs density can be 10,000/mm^2 or more [21], these test methods are pulled back due to their low cost-efficiency.

2.4 Prior Work on Improving Yield of 3D-ICs

Yield of 3D-ICs can be improved from both design and test perspectives. Various yield improving techniques are described in this section. This section is divided into techniques for improving yield from the design and test points of view.

2.4.1 Yield Improvement from Design Perspective

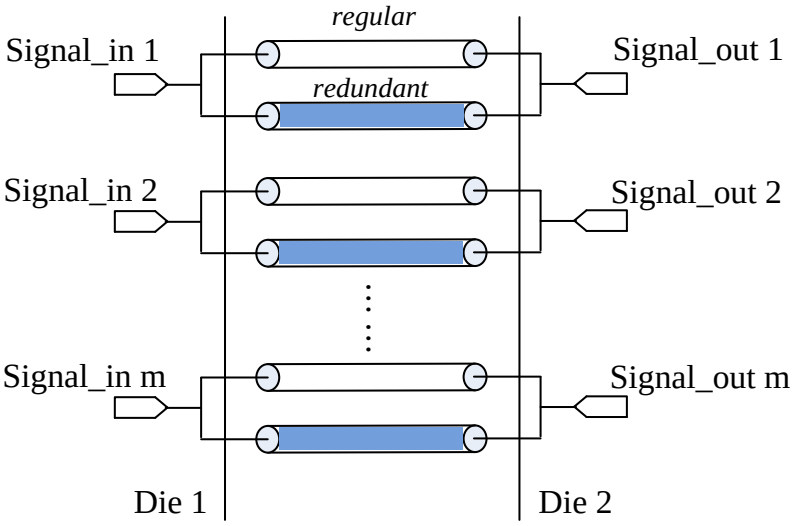
Since yield is directly related to the manufacturing process, design experts are trying to increase it by introducing better fabrication technologies including improving the bonding accuracy, developing better TSV fabrication process, and wafer matching techniques. Misalignment refers to unsuccessful wafer alignment during the bonding process, which results in reducing contact area between TSV and its landing pad. Current demand in TSV density (up to 10,000 per mm^2 [125]) is very high, for pursuing high bandwidth and finer partitioning granularity which splits smaller blocks across dies requiring more inter-die interconnects. Such high TSV density demand requires high alignment accuracy. For wafer-to-wafer alignment, a dedicated structure that does not contain any 3D circuit can be used for the sole purpose of improving alignment accuracy [10]. The minimum TSV pitch is affected by misalignment. As reported in reference [125], the mean wafer misalignment of wafer bonded in the clean room environment is 0.4um with a 0.7um standard deviation. This could lead to the minimum TSV pitch being approximately 6.5um. The achieved alignment accuracy in the state-of-the-art bonding process [10, 47] can significantly reduce the probability of misalignment. The delay increase caused by TSV misalignment is evaluated in reference [117], which suggested that under current alignment accuracy condition, the misalignment induced delay increment can be smaller than 1%, which means that only by improving bonding accuracy in 3D-ICs fabrication process, misalignment defect can be addressed. A void-free TSV fabrication technology is investigated in references [127, 128] to avoid imperfect filling of TSV. Another way of improving yield through design perspective is employing wafer matching technique, where a dedicated wafer matching program is

introduced to avoiding stacking good and bad dies together [129, 130]. Despite the fact that wafer matching is also helpful for yield improvement, its effectiveness is intuitively restricted unless we can reuse the bad dies.

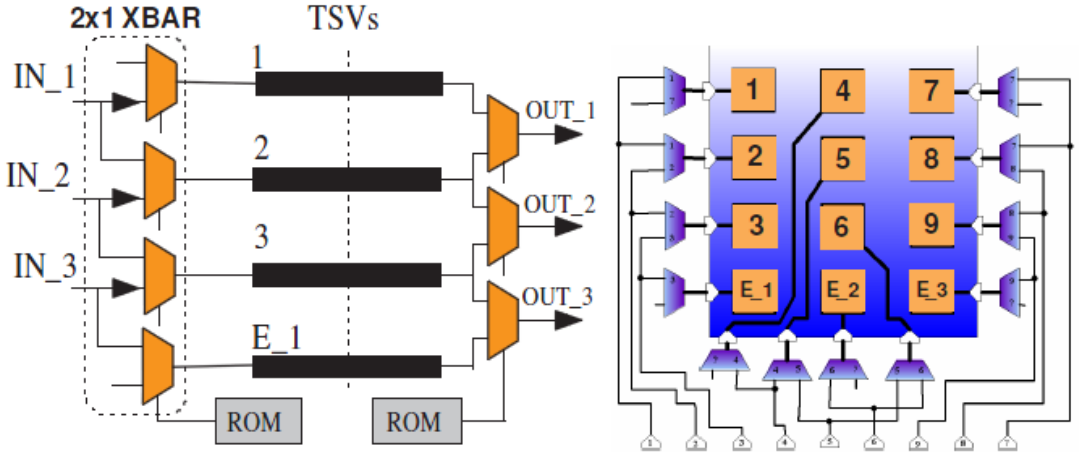
2.4.2 Yield Improvement from Test Perspective

By applying the TSV test methods described in Section 2.3, dies with defective TSVs can be identified thus avoiding them being stacked with good dies. However, without TSV repairing, TSV failures may still cause a large cost due to the dumping of bad dies. The idea of redundancy has been used for tolerating 2D interconnect defects for decades. Therefore, in 3D technology, TSV redundancy is employed for solving its yield problem. Existing structures that adopted redundant TSVs for TSV repair are shown in Figure 2.8(a)-(c), which represent three types of TSV redundancy configuration strategies: Duplicate, Signal switching, and Enhanced signal switching.

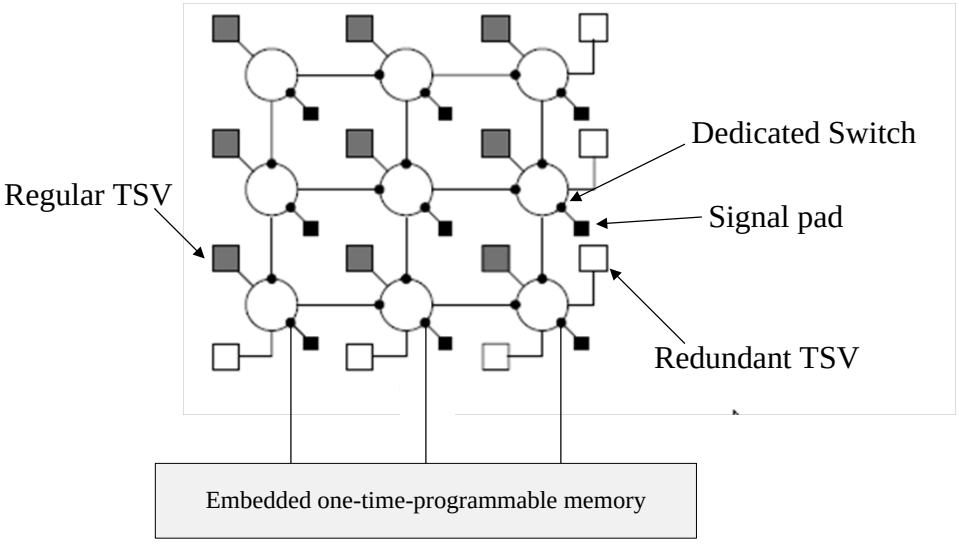
As illustrated in Figure 2.8(a), each signal is connected to a double TSV structure. If any one of the two TSVs is defective, there is still a functional TSV for transmitting signal. The advantage of this type of structure is that the implementation logic is quite simple; however, the cost of TSVs is extremely large, for a design with a large signal number (regular TSVs). Moreover, any such structure can only tolerate maximum one defective TSV. If more than one defective TSV occurs within a double-TSV structure, the whole design cannot be repaired. Igor *et al*. [117] proposed a signal switching-based defect tolerance scheme (Figure 2.8(b)) for 3D network-on-chip (NoC) links. For a TSV grid where TSVs are used as NoC links, one redundant TSV is added to each column of regular TSVs, thus each column can tolerate one defective TSV. Reference [131, 132] looked into Igor's structure, and partitioned TSVs into blocks, within each block one spare TSV is allocated, and when the block has one defective TSV, signals can be shifted using multiplexers to bypass the defective TSV. A recent study [131] demonstrated that for a design consisting of a small number of TSVs (up to 500), allocation of one TSV in each TSV block is efficient enough for improving yield to 99.99%. However, the study in [117, 131] ignored clustering effect, where TSVs are affected by nearby defective TSVs, defective TSVs tend to occur in the same block area. To overcome the clustering defect, it is helpful to increase the fault tolerance capability. For this purpose, an enhanced switching-based structure was proposed [133] (Figure 2.8(c)) based on dedicated switches and redundant TSVs, of which a defective TSV can be replaced by a 'distant' spare TSV through the dedicated routing switch (Figure 2.8(c)). Note that, the above TSV repair techniques [117, 131, 132, 133] mainly use the on-chip one-time-program (OTP) (i.e., e-fuse) memory for storing the control signals for configuring multiplexers or dedicated switches. Moreover, these methods require off-chip infrastructure for computing the control signals which incurs extra cost when conveying and diagnosing the TSV fault map using a computing server.



(a) Double-TSV structure for TSV [134]



(b) Switch-based TSV repairing structure [117]



(c) Enhanced switch based TSV repairing structure [135]

Figure 2.8: Three redundant TSV based TSV repairing structure.

2.5 Prior Work on Improving Reliability of 3D-ICs

Reliability of 3D-ICs can be improved through both design and test perspectives. Since thermal-induced reliability issue is a major concern in 3D-ICs, provisions should be made at the early design stage, such as integrating the microchannel cooling technique and thermal-aware floorplanning. As mentioned in Section 1.3.5, TSV repairing can be leveraged for in-field reliability concerns with the purpose of fault tolerance of thermal-induced latent TSV defects.

2.5.1 Microchannel Cooling and Thermal-aware Floorplanning

Force convective fluid-flow has been used for decades for heat dissipation within microelectronic systems [136, 137, 138]. The integration of microfluidic channel as a thermal management infrastructure is shown in literature [139, 140, 141, 142]. However, it cannot directly transferred to the 3D design with multiple stacked dies including poor thermal conducting interface and limited surface area available for cooling. To introduce a microchannel with fluid-flow in each die, as shown in Figure 2.9 [143], the detrimental thermal effect can be significantly removed for a 3D chip. Koo *et al*. [143] proposed thermal analysis of a 3D design using microchannel cooling technique and shows that an individual layer within the 3D integration can obtain a removal of heat densities up to 135 W/cm^2, achieving a maximum circuit temperature of 85℃. In this calculation, the uniformity of power distribution across layers is considered, nevertheless, the in-plane non-uniformity of power consumption is not targeted. Kim *et al*. [144] considered the impact of planar non-uniformity of power consumption-induced spatially distributed hot-spots when incorporating microfluidic cooling architecture, and dealt with hot-spots with power density up to 300 W/cm^2. Although the microfluid cooling technique is attractive, it incurs extensive cost when incorporating it in current 3D technology. Meanwhile, the reliability of such a structure needs to be well studied. Due to the generic characterization of the microfluidic channel (with a height around 100 um [145]) it may not scale well in the thinned wafer containing 3D circuits.

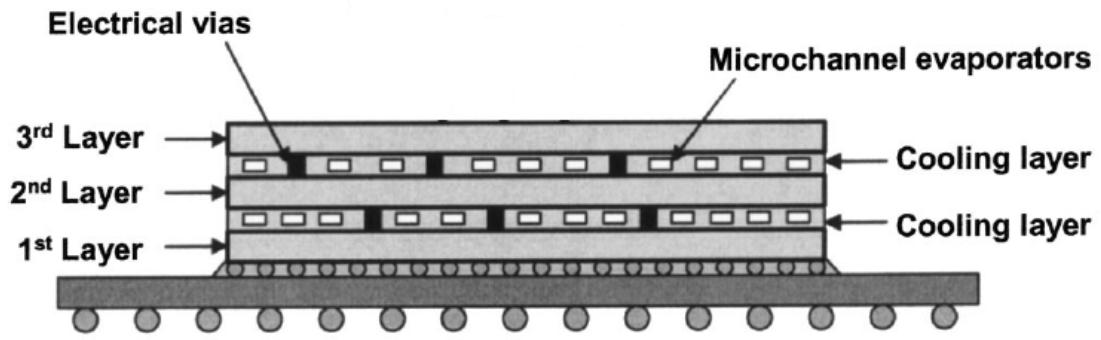


Figure 2.9: 3D circuits with a microchannel cooling system [143].

Rather than introducing a complicated cooling architecture, a simple way is to improve the existing 3D design flow by implementing thermal-aware floorplanning/placement strategies. Numerous papers have been published in recent research on this topic [43, 44, 146, 147, 148]. Cong *et al*. [146] firstly presented a 3D thermal-aware floorplanning algorithm based on a 3D compact thermal model which is for achieving 3D profile. It can simultaneously achieve a 29% reduction in total wirelength in comparison to a reported floorplanner for multi-layer design and 56% degradation in maximum chip temperature. Goplen *et al*. [147] provided a force-directed placement scheme with awareness of moving cells away from hotspots. The resulting placement can realize a reduced temperature to ~150℃ along with a slight increase in total wirelength. Even at the routing stage, thermal-aware routing method can be applied in-line with routing wirelength cost optimization [148]. However, these works do not consider the impact of TSV thermal effect which can lead to inaccurate thermal profiles, as conventional thermal floorplanning usually aimed to achieve uniform power distribution map across a chip as it leads to minimal chip temperature [43]. However, with the consideration of the thermal effect of TSVs, the overall thermal map can be significantly affected due to the improper TSV placement resulting in an unexpected higher temperature. Reference [44] designed a cell and TSV co-placement technique for alleviating the thermal load of 3D designs. Apart from its accurate final 3D thermal profile, the TSV usage can be reduced as well due to its contribution in reducing temperature. However, the above work does not scale well for increasing demand in device density of current 3D circuits leading to higher thermal density. A new temperature reduction technology is required, as temperature reductions achieved by existing thermal-aware floorplanning/placement approaches are still harmful for chip operation and lead to TSV delay faults. Therefore, to reduce temperature further, reference [126, 149] decided to add dummy vias which serve as additional thermal dissipation tunnels. As shown in a recent study [126], with these dummy TSVs, the chip temperature can be reduced further to ~77℃. However, these dummy TSVs have two limitations. Firstly, introducing a large number of dummy vias adds a significant cost, consuming additional routing area and thus increasing the routing congestion. Secondly, since these dummy TSVs have no practical connection to signals, they cannot be reused for any other purpose during operation. These dummy vias cannot help when any TSV failure involves either manufacturing defects or latent defects,. In response to this gap, a more cost-effective and high-quality mechanism is investigated in Chapter 5, for reducing thermal load and improving the thermal-induced reliability problem.

2.5.2 TSV Repair for In-field Reliability Improvement

Unlike TSV repair for improving yield of 3D-ICs (as described in Section 2.4.2) that can be used to repair defective TSVs only after the manufacturing test. TSV repairing scheme can be extended for reliability-awareness (i.e., tolerating aging TSV defects in the 3D design lifetime). This scheme should introduce a control block which adaptively generates control signals for switch-based TSV redundancy architecture, which means that the OTP

(one-time-programmable) memory will be replaced by robust on-chip circuits that work during operation. Jiang *et al*. [151] proposed a TSV repair scheme which uses the dedicated-switch based TSV redundancy architecture (as shown in Figure 2.8(c)) and an on-chip processor which provides control signals for routing switches that routes signals through good TSVs while avoiding defective ones. Figure 2.10 shows the schematic diagram of this technique. It can be seen that the test results are fed into the processor for computing configuration signals for routing switches (Figure 2.10). It can address lifetime reliability issue, as once defective TSVs are identified, the router configuration block can be reconfigured for TSV repair under the corresponding TSV fault map. The main change in this technique from the one shown in Figure 2.8(c) is the replacement of OTP memory by an on-chip processor. However, such an on-chip processor is not available. Moreover, the time consumption for computing configuration signals and area overhead result from the employment of such processor-based architecture is also large. Similarly, in a recent study [150] an online monitoring and correction system is presented. Open resistive TSV defects can be detected and repaired by employing the switch-based TSV redundancy structure presented in reference [135]. Reference [150] and [151] have a common idea in TSV redundancy organization, they partition regular and spare TSVs in a bundle, within which defective TSVs can be repaired using available spare ones. Reference [152] reported that such a bundle-based structure is not efficient enough, since once one bundle cannot be repaired due to lack of spare TSVs in that budle, the whole design fails. Thus authors of [152] provided a TSV fault tolerance technique whereby the entire set of TSVs in one layer is assigned a number of spare TSVs for defect tolerance purpose (Figure 2.11). It can be seen that the multiplexer-based cross switch block is similar to the structure presented in reference [117] (Figure 2.8(b)). However, there is no TSV group or TSV bundle, thus, it (structure of reference [152]) can tolerate more defective TSVs by providing the same number of total redundant TSVs. The limitation is that, the cost of such a multiplexer-based block is too large, as each multiplexer is a big unit with a large fan-out number (1-to-n). Moreover, the control signals for all multiplexers incur an inevitable large hardware cost, as each set of control signals for one individual multiplexer contains more bits in comparison to the case when regular and spare TSVs are partitioned into groups.

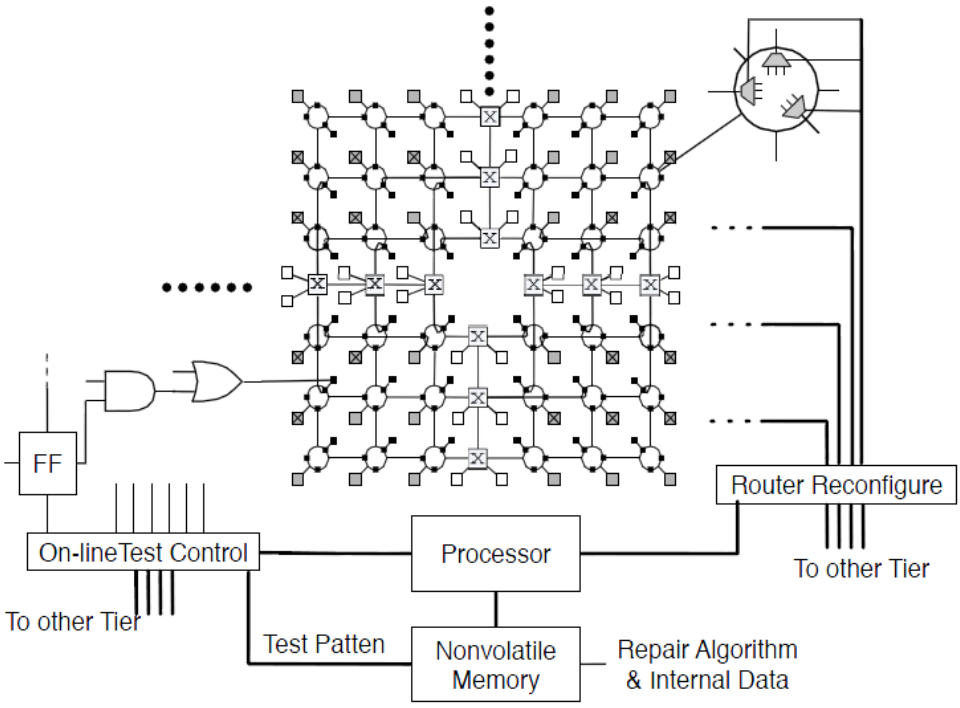


Figure 2.10: Processor based TSV repairing architecture [151].

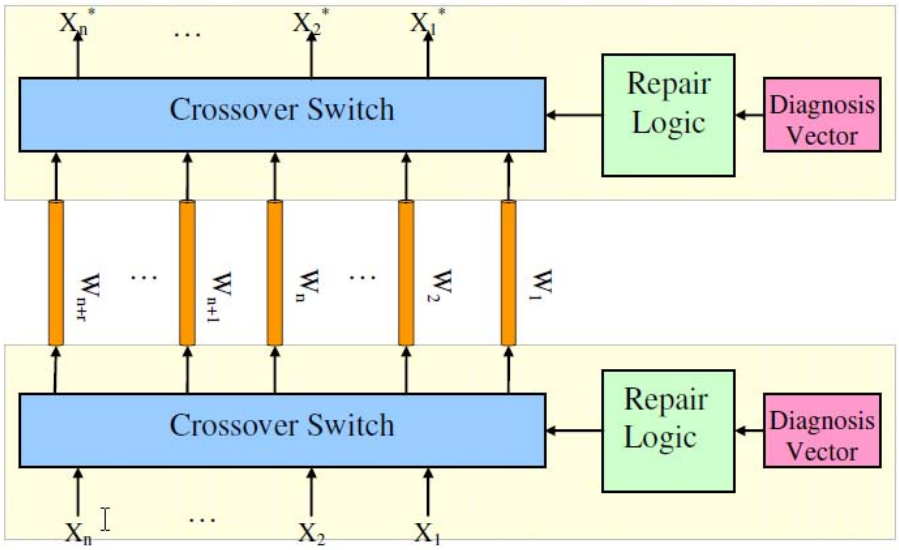


Figure 2.11: TSV fault tolerance architecture without TSVs partitioning [132].

2.6 Concluding Remarks and Research Objectives

This chapter has presented an overview of recent work on TSV defects characterization and defect modeling methodology. Meanwhile, existing work on TSV test and repair has also been studied. Research on TSV defect detection has suggested that void, delamination, and TSV short to substrate are three main TSV defect types that should be addressed [104, 112, 115, 122, 123]. A post-bond TSV test should be incorporated as these TSV defect types can happen after the bonding process and during operation. However, existing work on TSV defect detection requires large amount of analog devices which affect the test quality [115, 123]. The hardware cost for testing TSV is very high, as in reference [104], a ring oscillator based architecture (Figure 2.7, Section 2.3) is provided to test two TSVs, which implies that for testing a 3D circuit containing a large number of TSVs, the area overhead is considerably high. Therefore, in Chapter 4, a cost-effective TSV detection circuit is proposed for detection all three types of TSV defects.

There is a number of published papers on TSV repair based on redundant TSVs. Reference [117, 131, 132] aim to use redundant TSVs to improve yield of 3D-ICs (Section 2.4.2). However, due to clustering TSV defect distribution, where defects tend to cluster together, the work presented in [117, 131, 132] may not scale well due to the lack of repair capability. There should be a method which can provide sufficient repair capability with cost-effective implementation. Thus, it is essential to undertake a trade-off analysis between the yield improving of 3D-ICs and its corresponding hardware cost which will be presented in Chapter 3. The improvement of yield of 3D-ICs is not enough as latent TSV defects may result in critical reliability issue of 3D-ICs. The work in [151] presented a processor-based TSV repairing technique, where the processor can work during operation to provide configuration signals to control routing switches leading signals avoiding defective TSVs (Section 2.5.2, Figure 2.10). Nevertheless, such online processor (Figure 2.10) is not available, and the time consumption of the processor-based scheme is not efficient. Additionally, to the best of our knowledge, no work has combined the online test and repair for TSV defect tolerance. This motivates us to provide a high-efficient online fault tolerance technique which is capable of TSV defect detection and fault recovery to cope with both of TSV manufacturing defects and latent defects.

As discussed in Section 1.3.4 and Section 2.3, thermal is a critical factor to the reliability of 3D-ICs. Design experts tried to relieve temperature pressure of 3D circuits by providing thermal-aware floorplanning mechanisms [43, 44, 145, 146, 147, 148] and dummy vias for extra thermal dissipation channel [126, 149]. However, these methods cannot ensure that TSVs are not going to involve latent defects during use, as once defective TSVs are found, these dummy vias cannot help. From this point of view, this research aims to provide a technique which jointly considers both temperature mitigation and fault tolerance for 3D circuits, which means that the temperature is reduced to relieve the thermal load of a chip, and in the meanwhile TSV failures either due to manufacturing defects and latent defects can be

addressed. This thesis aims to provide solutions for addressing both yield and reliability issues of 3D-ICs by investigating a high-quality and cost-effective online fault tolerance technique aiming to address the above issues. The objectives of the research in this thesis are listed as follows and shown in Figure 2.12.

1. Study the defect mechanism of TSV voids, short to substrate, and delamination defects. Characterize their properties in order to explore their fault behavior and correspond models, this is presented in Chapter 2.
2. To improve the yield of 3D-ICs by employing TSV redundancy, and provide a mathematical model for yield analysis of 3D design under independent and clustering TSV defect distributions. Analyze the trade-off between achieved yield and the hardware cost. The developed technique is presented in Chapter 3.
3. Develop an infield infrastructure for improving reliability of 3D design which is also capable of both detection and recovery for TSV defects. The proposed technique is presented in Chapter 4.
4. Develop a scheme that undertakes both temperature mitigation and fault tolerance of 3D-ICs which are capable of repairing TSV failures either due to manufacturing defects or latent TSVs defects. The proposed methodology is in Chapter 5.

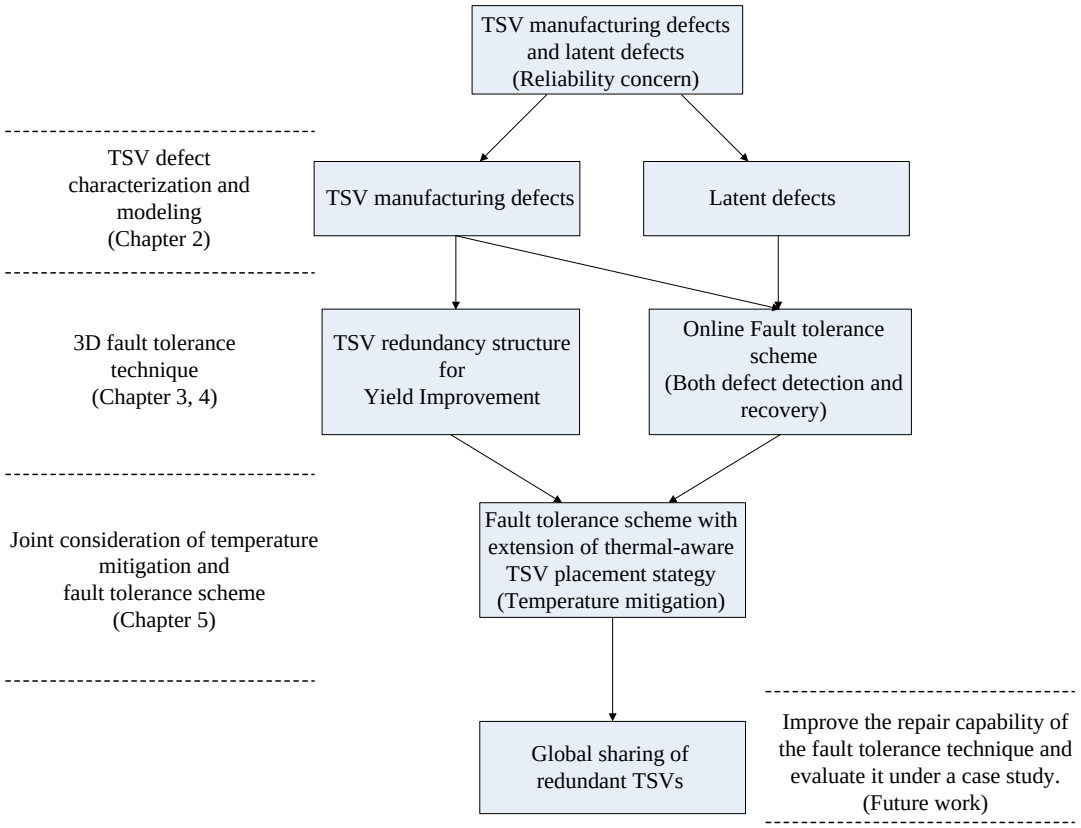


Figure 2.12: Research Objectives.

Chapter 3

Grouping-based TSV Repairing for Yield Improvement of 3D-ICs

Chapter 2 highlighted the need for high repair capability and a cost-effective method for improving yield of 3D-ICs in the presence of manufacturing defect. This chapter presents a redundant TSVs grouping technique, which partitions regular and redundant TSVs into groups. For each group, a set of multiplexers is used to select good signal paths away from defective TSVs. We investigate the impact of grouping ratio (regular-to-redundant TSVs in one group) on trade-off between yield and hardware overhead. Probabilistic models for yield analysis under the influence of independent and clustering defect distributions are presented. Simulation results show that for a given number of TSVs and TSV failure rate, careful selection of grouping ratio leads to achieve 100% yield at minimal hardware cost (number of multiplexers and redundant TSVs) in comparison to a design that does not exploit TSV grouping ratios.

The publication related to this chapter is list in Chapter 1 Section 1.5 (Publication 1) and its corresponding key contributions are:

- A mathematical probabilistic model is provided for TSV yield analysis under the influence of independent and clustering TSV defect distribution.

- A grouping method which partitions regular and redundant TSVs into groups, and multiple spare TSVs are used to repair defective TSVs in that group through re-routing multiplexer. An optimization between yield and hardware cost (redundant TSVs, multiplexer) is achieved through careful selection of grouping ratio.

3.1 Introduction

As shown in Chapter 1, three-dimensional Integrated Circuits (3D-ICs) is a promising technology to overcome performance bottleneck of traditional integrated circuits due to higher interconnect delay [60]. Section 1.1 shows different technologies developed by a number of research organizations to implement TSV-based 3D integration (Table 1.1, Chapter 1). Using TSVs technology, a very high interconnects density, millions of TSVs in a design, can be realized [48]. However, yield of TSVs based 3D-ICs is limited under the current manufacturing process. As discussed in Section 1.3.3 (Eq. (1.9), yield of a 3D chip is composed of three parts: devices (transistors & horizontal wires) in each die, bonding process, and TSVs. Only one defective TSV can fail the entire chip with all known-good dies [51]. Figure 3.1 shows the yield of TSV-based 3D chips under three implementation technologies [106]: HRI [51], IBM [22], and IMEC [113]. Note that in Figure 3.1, only random TSV open defects are considered, since misalignment can be well controlled during the bonding phase. Thus, yield improvement methods with respect to ensuring good TSV interconnections should be introduced when adopting 3D integration.

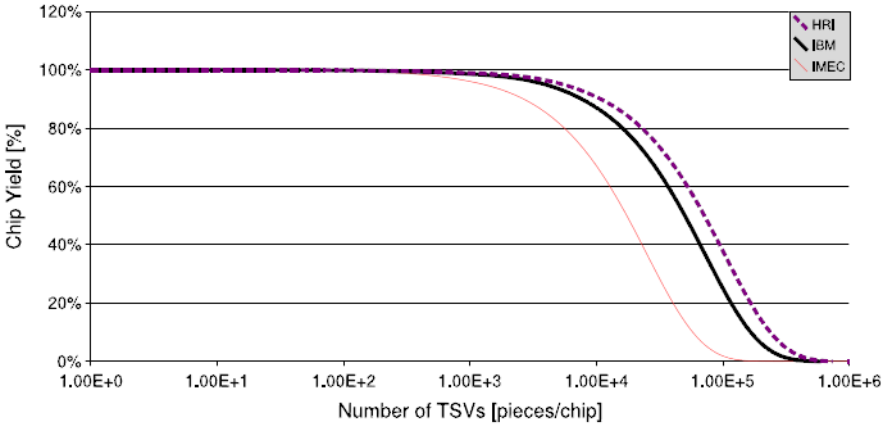


Figure 3.1: Yield of 3D chips under three different processes: HRI, IBM, and IMEC [106].

As highlighted in Section 2.4.2, redundant circuits can be an efficient solution to improve the yield of 3D-ICs [107, 108, 117, 131, 134]. For example, a recent study [108] increases the yield of 3D-stacked memory by sharing the redundant memory rows/columns across neighboring dies. Reference [107] attempts to improve the yield by providing wireless redundant TSVs. However, extra cost will be introduced to ensure the functionality of the employed wireless redundant TSVs. Besides that the manufacturing of wireless TSVs using current 3D fabrication technologies needs more investigation. Reference [117] proposes a fault tolerance scheme based on redundant TSVs and multiplexers, to ensure availability of good signal paths between layers by rerouting signals through non-defective redundant TSVs. [131] looks into repair mechanism, considering designs with a small number of TSVs (up to 500) and partitions TSVs into blocks and assigns each block with one spare TSV for repairing

the faulty link in that block. However, the repair capability of [131] is limited if a design with larger number of TSVs still partitions TSVs into blocks, within which only one spare TSVs is comprised.

Hence, this chapter focuses on providing higher repair capability when introducing a TSV repairing mechanism. The work is also based on utilizing redundant TSVs, regular and redundant TSVs are partitioned into groups using a specified grouping ratio (regular-to-redundant), where each group can have multiple spare TSVs, and multiplexers are used to reroute signals through a good TSV path in case defective TSVs exist in that group. Due to the allocation of multiple TSVs in a group, the repair capability can be significantly increased. Clustering defects have been acknowledged in traditional semiconductor manufacturing to cluster in an area rather than randomly distributed, for memory chips clustering defects have been reported in literature [133, 153, 154]. With such clustering effect, more defective TSVs are likely to occur in a group, thus further reducing the overall yield. Clustering defects are also considered in this chapter to analyze their affect on yield of 3D-ICs. To the best of our knowledge, this is the first study to model clustering defects and to analyse yield in the presence of clustering defects in 3D-ICs. By allocating more TSVs in a group, higher yield can be guaranteed even under clustering defects distribution. However, this is ensured by a higher hardware cost. Thus, in this chapter investigation into yield improvement and hardware cost is also presented. Simulation results evaluate the trade-off between yield and hardware cost (number of multiplexers and spare TSVs) under the influence of independent and clustering defect distributions, and show that it is possible to achieve 100% yield at minimal hardware cost through careful selection of grouping ratios and redundant TSV percentage.

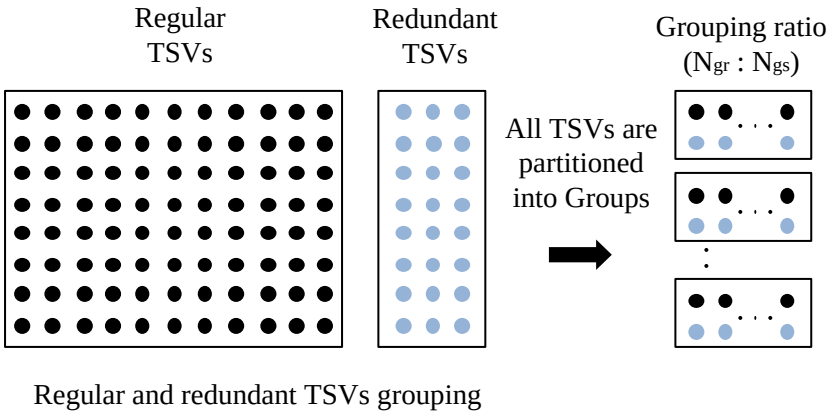
This chapter is organized as follows: Section 3.2 uses an example to illustrate the trade-off between yield and hardware cost brought by grouping ratio that is examined in this chapter. Section 3.3 presents the TSV redundancy modeling methodology and the yield analysis approach. Section 3.4 presents simulation results by exploring the yield of a number of regular TSVs under different grouping ratios. Finally, Section 3.5 concludes this chapter.

3.2 Motivation and Problem Formulation

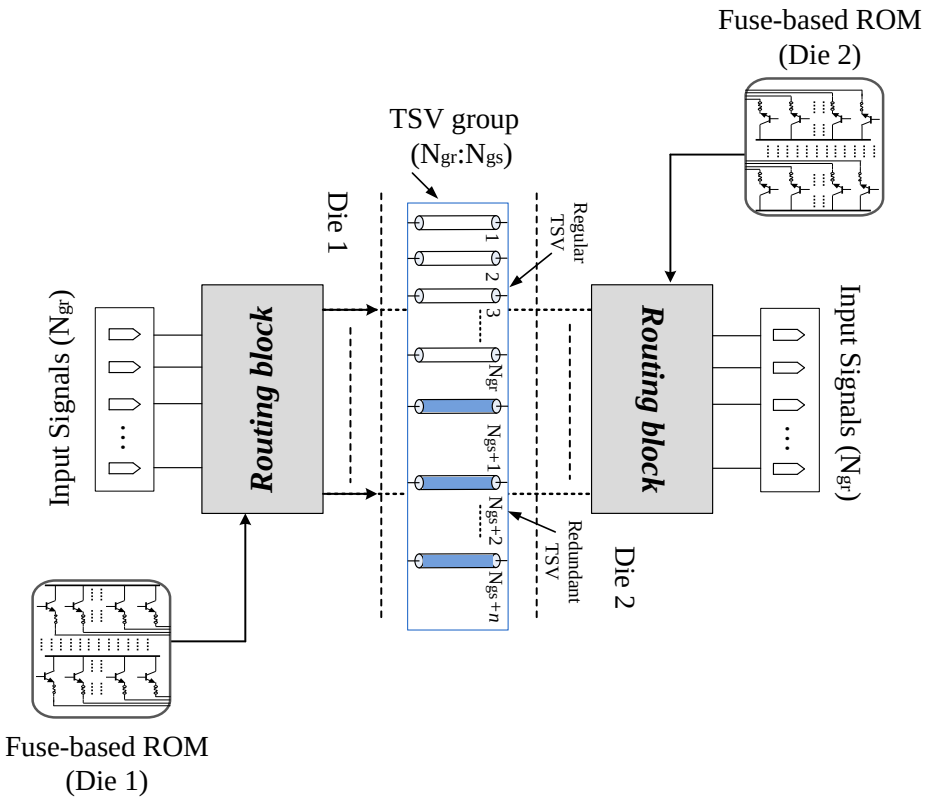
3.2.1 Motivation

As described earlier (Figure 1.8, Chapter 1), the manufacturing process of TSVs based 3D-ICs can be summarized into three stages. Firstly, the fabrication of individual dies to be stacked, which involves transistor layer and metal layers construction. Secondly, the fabrication process of TSV, which involves via etching and filling procedures [113]. Finally, the bonding stage, which bonds TSV with the bonding pad to form the communication link between dies. These steps can also be re-ordered to build TSVs before transistors and metal layers. As highlighted in Section 2.2, TSVs random open defects can happen in TSV

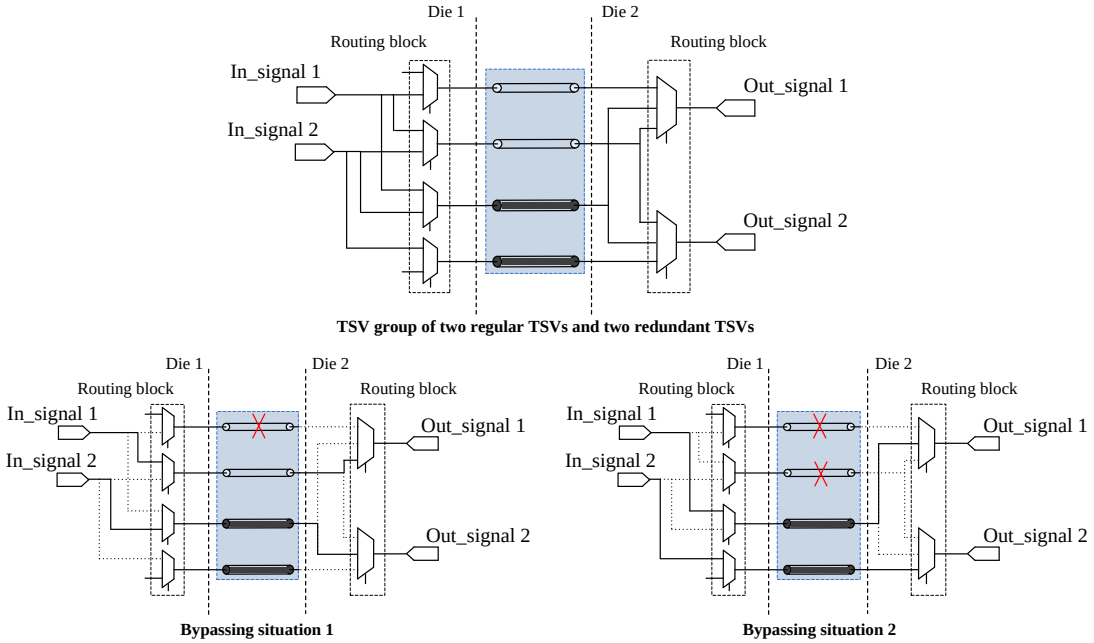
fabrication process, due to processing variants such as insufficient filling creating voids inside TSVs, delamination between TSV and its landing pad, etc. Similarly in the bonding process, random open defects may be caused by foreign particles [21]. Misalignment is due to incorrect wafer alignment during bonding, which results in shift of TSV tips from their bonding pads. Misalignment can be addressed by increasing the bonding accuracy [155], and therefore this chapter focuses on random open defects that lead to yield loss in 3D-ICs.



(a) TSVs into groups



(b) Architecture of a TSVs group containing routing block and control block.



(c) Illustration of how routing multiplexers avoid defective TSVs in a group, TSV grouping ratio is chosen to be 2:2 for illustration purpose.

Figure 3.2: Architecture and working principle of TSV grouping method.

Figure 3.2(a) illustrates the basic idea of our proposed grouping technique. For a design with a number of regular TSVs, redundant TSVs are provided. Then they are partitioned into groups according to **grouping ratio** (gr=N_{gr}: N_{gs}) which accounts for the number of regular TSVs (N_{gr}) and redundant TSVs (N_{gs}) to be placed in a group. The architecture of a group is depicted in Figure 3.2(b), as can be seen, there is a routing block which undertakes rerouting signals avoiding defective TSVs. Also, a fuse-ROM based block is for providing the control signals to routing blocks. In the proposed technique, the routing block is implemented by multiplexers, which are used to select good signal paths bypassing the defective TSVs (Figure 3.2(c)). As an example, see Figure 3.2(c) where each group contains two regular and two redundant TSVs, It is shown that, once defective TSVs are found in a group redundant TSVs can be used to repair the group. Clearly, with a grouping ratio of 2:2, it is able to repair the group in case of one or two faulty TSVs through rerouting signals using good TSVs.

Next, the demonstration of how organization between redundant TSVs with regular ones has an impact on the yield and hardware cost (redundant TSVs and multiplexers) is presented. Note that in this Chapter, hardware cost does not contain the fuse-ROM based block, as that is assumed to be embedded in the test circuits generated for gaining the TSVs faulty map. It is assumed that the test results (TSVs fault map) is provided, then the proposed TSV grouping scheme is used for repairing TSVs. However, in Chapter 4, detection of TSVs faults are also embedded within a TSVs fault tolerance technique. Assuming that there are eight regular

TSVs and four spare TSVs in total, which can be organized in two grouping ratios, as shown in Figure 3.2.

- Organization 1: Grouping ratio is 2:1. Four groups are obtained, with two regular TSVs and one redundant TSV in each group.
- Organization 2: Grouping ratio is 4:2. Two groups are obtained, each with four regular and two redundant TSVs.

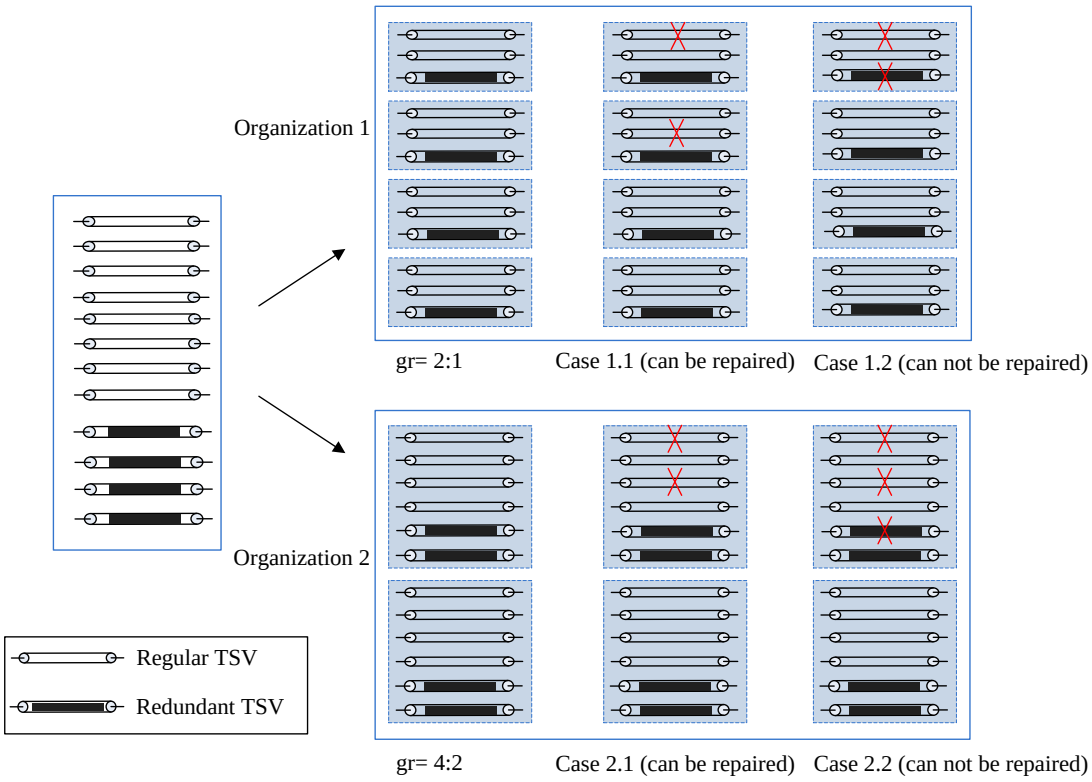
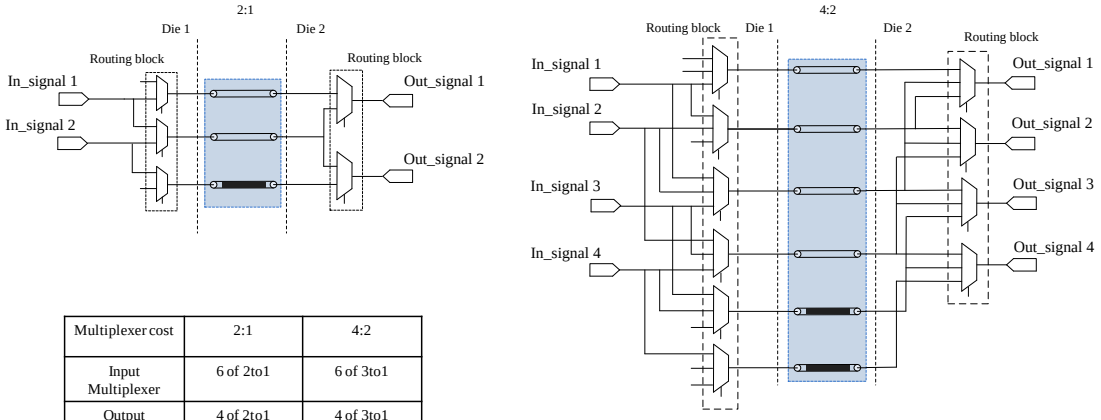


Figure 3.3: Eight regular and four redundant TSVs partitioned using two grouping ratios (Regular: Redundant, 2:1 and 4:2), grouping ratio of 4:2 implies higher yield (repair capability)

Organization 1 allows maximum one defective TSV within a group, such that the group can be repaired (case 1.1). If two defective TSVs are found within one group, such as in case 1.2, the group cannot be repaired. However, with the same redundancy percentage, organization 2 tolerates maximum two defective TSVs in one group, which indicates that, if only two defective TSVs exist, organization 2 can always be repaired (case 2.1). If more than two defective TSVs exist in one group (case 2.2), organization 2 cannot be repaired. It is clear that higher grouping ratio (4:2) implies higher yield. The cost of this grouping technique involves spare TSVs and multiplexers. Figure 3.4 illustrates the multiplexer configurations for both grouping ratios 2:1 and 4:2, and summarizes the multiplexer cost in the Table (Figure 3.4). Although grouping ratio 4:2 implies higher yield (Figure 3.3), it requires higher multiplexer cost in terms of area overhead. It is needed to evaluate how redundant TSVs should be grouped with regular ones to achieve the best yield with the lowest possible hardware cost

(redundant TSVs and multiplexers) for a given fault rate. In terms of placement of timing critical signals, there is a method proposed in a recent study [131] that shows a timing-aware TSV arrangement method such that if signal rerouting is required due to defective TSV in a group then the most timing critical signal is least affected. Moreover, in Chapter 5, a TSVs fault tolerance scheme that incorporates a TSVs placement strategy to reduce the impact due to rerouting signals between regular TSVs and redundant ones is proposed.



Multiplexer cost	2:1	4:2
Input Multiplexer	6 of 2to1	6 of 3to1
Output multiplexer	4 of 2to1	4 of 3to1

Figure 3.4: Illustration of multiplexer cost under two different grouping ratios (2:1 and 4:2)

3.2.2 Problem Formulation

The problem addressed in this chapter can be formulated as:

Problem Given:

- The number of regular TSVs N_R;
- The failure rate of a single TSV p;

Analyze the yield under different grouping ratios (regular: redundant TSVs in one group) and aim to achieve a target yield with the lowest possible hardware cost (redundant TSVs and multiplexers). The best grouping ratios to achieve highest yield and lowest hardware cost is determined through an exhaustive search algorithm (Section 3.3.3) which exhaustively searches across all possible grouping ratios until 100% yield is achieved. This is further explained in Section 3.4.

To solve this problem, how to model TSV redundancy is firstly investigated, and then a probabilistic method to achieve the yield in the presence of independent and clustering defects is presented

3.3 TSV Redundancy Modeling and Yield Analysis

This section firstly considers each TSV to have independent failure rate. TSV redundancy modelling for independent defect distribution is in Section 3.3.1. The overall yield $Y_{independent}$ can be obtained based on a probabilistic model. Next, in Section 3.3.2 clustering defects when modelling TSV redundancy is introduced, which means that the defective probability of a TSV increases due to existing defects (defect correlation). TSV location is required in this model and an algorithm to calculate the yield of TSV redundancy for clustering defect distribution denoted by $Y_{clustering}$, is proposed.

3.3.1 TSV Redundancy Modeling and Yield Analysis for Independent Defect Distribution

For independent defect distribution based TSV redundancy model, the basic modelling features are (1) *redundancy percentage rd* is the usage of redundant TSVs (Redundant/Regular), and (2) *grouping ratio*, regular to spare TSVs ratio (N_{gr}: N_{gs}) in a group. The total number of spare TSVs is N_s=N_r·*rd*. All TSVs are then partitioned into groups according to *grouping ratio*, and the number of groups is given by $gn = \frac{N_r}{N_{gr}}$. The post-partition groups are denoted by G_1, , G_i, , G_{gn}. The uniform group size is N_{gr} + N_{gs}. Each group is independent from the others. Once achieving the yield of one group Y_{group}, then the overall yield of all *gn* groups $Y_{independent}$ can be obtained by multiplying all individual group yields, expressed as:

$$Y_{independent} = (Y_{group})^{gn} \tag{3.1}$$

Each TSV within a group is independent and has a uniform failure rate *p*. Thus, the number of defective TSVs in a group follows binomial distribution, which is: Assuming *X* is the variable of defective TSV number in a group, then the probability of having *x* defective TSVs is expressed as:

$$P(\mathrm{X}=x) = C_{N_{gr}+N_{gs}}^{x} \cdot p^{x} \cdot (1-p)^{(N_{gr}+N_{gs}-x)} \tag{3.2}$$

where $C_{N_{gr}+N_{gs}}^{x}$ is a combination of *x* and (N_{gr}+N_{gs}) which shows all the possible situations of having *x* defective TSVs in a group of (N_{gr}+N_{gs}) TSVs. Clearly if the number of defective TSVs in a group is smaller than the number of spare TSVs N_{gs}, such a group can be repaired. Therefore, the yield of a group Y_{group} is:

$$Y_{group} = \sum_{x=0}^{N_{gs}} \left[C_{N_{gr}+N_{gs}}^{x} \cdot p^{x} \cdot (1-p)^{(N_{gr}+N_{gs})-x} \right] \tag{3.3}$$

Eq. (3.3) calculates the overall probability of having x ($0\cdots N_{gs}$) defective TSVs in a group. The yield of TSV redundancy for independent defect distribution can be achieved by substituting Eq. (3.3) into Eq. (3.1).

3.3.2 TSV Redundancy Modeling and Yield Analysis for Clustering Defect Distribution

In this section clustering defects are considered, where all TSVs are correlated, and therefore the modeling method is different from the independent defect distribution (Eq. (3.1)). This modeling scenario has to take TSV locations into account. Firstly, the clustering effect is discussed before explaining the model.

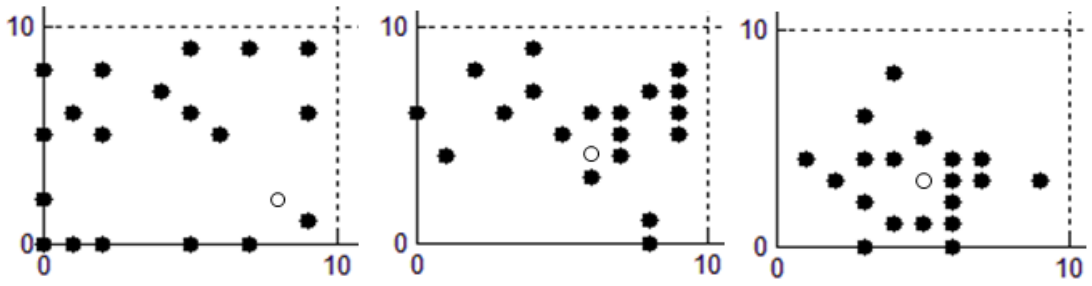
Clustering defects means that defects tend to cluster together to some extent rather than randomly distributed. It models the scenario, where the presence of single defect increases the likelihood of more defects in close vicinity. Reference [67, 71, 156] described this clustering effect as defect probability of node i (P_i) is inversely proportional to the distance from the existing defect node j, that is expressed as

$$P_{\mathrm{i}} \propto (\frac{1}{d_{\mathrm{ij}}})^{\alpha} \qquad (3.4)$$

where, d_{ij} indicates the distance between node i and defective node j, and α is the clustering coefficient indicating clustering extent, a larger α implies higher clustering. By employing the concept 'cluster center' [157], in this chapter a cluster center represents one defective TSV, where all defective TSV tend to exist around this center. The defective probability of TSV_i P_{i} will be increased, which can be expressed as

$$P_{\mathrm{i}}=p\cdot(\ 1+(\frac{1}{d_{\mathrm{ic}}})^{\alpha}\ ) \qquad (3.5)$$

where p is the single TSV failure rate, and d_{ic} is the distance between TSV_i and cluster center. This is illustrated in Figure 3.4(a)-(c), where hollow node represents the cluster center defective TSV, solid nodes denote the other nearby defective TSVs. By taking the clustering effect into consideration, the distribution of defective TSVs tends to cluster around a center and this becomes higher with a larger clustering coefficient.



(a) No clustering (b) α =1 (c) α =2

Figure 3.4: Defective TSV pattern illustrating clustering effect

The clustering TSV redundancy model assigns all TSV groups $\{G_1 \cdots G_i \cdots G_{gn}\}$ into '*blocks*', and each *block* refers to a wafer area that contains TSV groups. A defect cluster can happen in one block and cluster within a *block* is regarded as small cluster. Therefore, each *block* is independent and clusters within different *blocks* do not affect each other [158, 159]. The size of the *block*, namely how many TSVs there are in a *block*, is uniform denoted as $|Q|$, such that all groups $\{G_1 \cdots G_i \cdots G_{gn}\}$ are located into *qn blocks*, where $qn = \frac{N_r + N_s}{|Q|}$. Each *block* is assigned with a N×N grid with x and y orientation coordinates are within the range of ($0<=x<=\sqrt{|Q|}-1$, $0<=y<=\sqrt{|Q|}-1$) respectively. It is assumed that each TSV is located on the integral coordinates, this regular placement scenario also complies with the fabrication process. A *block* size $|Q|$ =100 is used in this chapter as this size meets the requirement of having small size defects cluster in a block. Under this *block* setting, each TSV_k placed in this *block* has its unique properties denoted as $TSV_k\{X_k, Y_k, group\_index_k\}$, where k is the TSV subscript, X_k and Y_k are its horizontal and vertical coordinates respectively which will be used to calculate the distance between two TSVs, and $group\_index_k$ indicates the group G_i it belongs to.

The overall yield of TSV redundancy for clustering defect distribution, denoted by $Y_{clustering}$ can be obtained by multiplying all individual *block* yield as

$$Y_{clustering} = (Y_{block})^{qn} \tag{3.6}$$

If a block contains a defective TSVs cluster with more than N_{gs} (redundant TSV number in one group) defective TSVs found in a group, then it cannot be repaired. Let $P_{non\text{-}repair}$ indicates the probability that a block cannot be repaired, thus the yield of a *block* is expressed as

$$Y_{block} = 1\text{-}P_{non\text{-}repair} \tag{3.7}$$

An algorithm is proposed to calculate $P_{non\text{-}repair}$ by identifying all cases that a *block* containing a cluster with groups that cannot be repaired and summing up the probability of each case. Figure 3.7 shows the algorithm for calculating $P_{non\text{-}repair}$. It begins by TSV setup process (Step 1) which assigns coordinates to TSVs within a *block*. TSVs are not randomly assigned a coordinate, for the sake of simplification, this is done in a group-by-group manner. Once a group of TSVs is located then it deals with another group. An example of TSV placement in *block* is illustrated in Figure 3.5. Note that, it is assumed in this chapter that there are pre-defined block area on dies for placing TSVs groups. However, in practice, TSVs may be placed randomly across dies which means that even TSVs that belonging to the same group can be far away from each other. With such a placement step, the routing paths length of a signal using regular and spare TSVs within a group that are connected to it can be significantly different which raises a problem related to delay when signals have to switch from one routing path to another. In this chapter, this is addressed by placing TSVs belong to the same group into the pre-defined block area, while in Chapter 5 a TSV placement strategy

is proposed which takes into account the routing path difference issue. Moreover, placing TSV groups into blocks helps us gain yield analysis for clustering TSV defects distribution.

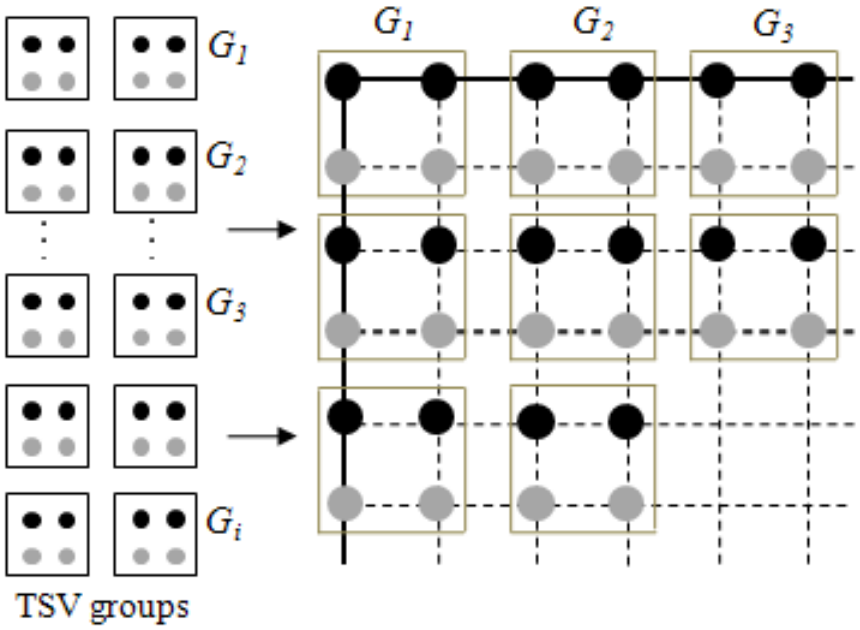
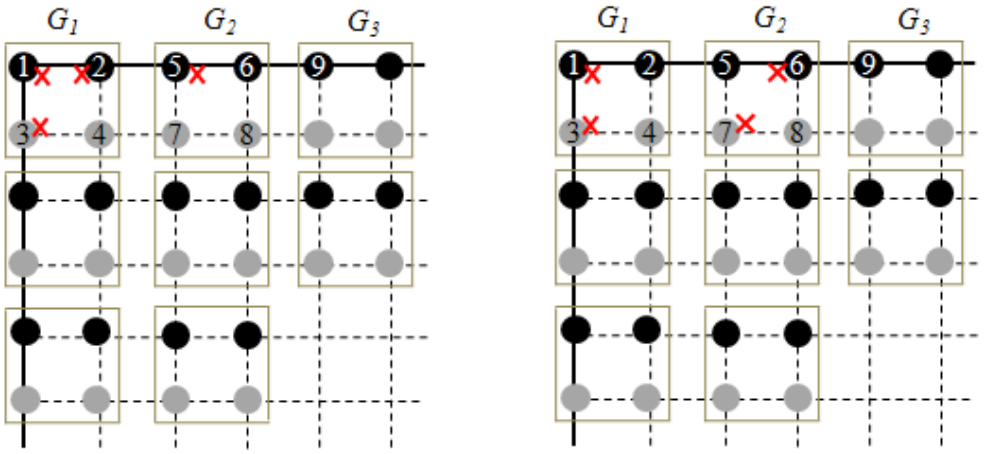


Figure 3.5: TSVs are placed in the block group by group, grouping ratio=2:2, black node and grey node denotes regular and redundant TSVs respectively.



(a) {(TSV$_1$, TSV$_2$, TSV$_3$),(TSV$_5$)} (b) {(TSV$_1$, TSV$_3$), (TSV$_6$, TSV$_7$)}

Figure 3.6: Examples of defective TSV patterns

The next step is to find out all the possible situations where a block containing a cluster with more than one group and cannot be repaired (Step 2). To ensure that at least one group that cannot be repaired exists, the possible defective TSV number of one *block*, denoted by N_d, should be larger than N_{gs}. However, a *block* containing more than N_{gs} defective TSVs may be repaired. A defective TSV pattern gives the defective TSV distribution in a *block*. Using *block* in Figure 3.5 as an example, if total defective TSV number in that *block* is four, two possible defective TSV patterns are {(TSV$_1$, TSV$_2$, TSV$_3$),(TSV$_5$)} and {(TSV$_1$, TSV$_3$), (TSV$_6$,

TSV_7)}, as shown in Figure 3.6. Defective pattern {(TSV_1, TSV_3), (TSV_6, TSV_7)} can be repaired, as no group contains more than two defective TSVs. All possible defective patterns that represent the case of a block that cannot be repaired are then stored into variable *non_repair_pattern*. Then, starting calculating $P_{non\text{-}repair}$, by summing up the probability of each defective pattern in *non_repair_pattern* (Step 3- Step 7). All TSVs in a defective TSV pattern are divided into two parts, N_d defective TSVs and $|Q|$-N_d non-defective TSVs, which are denoted as *defective_part* and *non_defective_part* respectively. Based on the multiplication principle the probability of a defective pattern can be achieved by multiplying the probability of N_d defective TSVs ($P_{defective\_part}$) and $|Q|$-N_d non-defective TSVs ($P_{non\_defective\_part}$). Also, as mentioned earlier (Section 3.3.2), a cluster center refers to a defective TSV, and its distribution is uniform, indicating any defective TSV could be cluster center. If the cluster center varies, the defective probability of each TSV changes which results in different $P_{defective\_part}$ and $P_{non\_defective\_part}$. Therefore, the probability of a defective TSV pattern containing N_d defective TSV is expressed as

$$\sum_{i=1}^{N_d}(P_{defective\_part} \cdot P_{non\_defective\_part})_i \cdot \frac{1}{N_d} \qquad (3.8)$$

where i=(1$\cdots N_d$) implies each defective TSV has been considered to be the cluster center, '$\frac{1}{N_d}$' implies that cluster center follows uniform distribution and the probability equals to 1/N_d. The probability of N_d defective TSVs, $P_{defective\_part}$, is achieved by the product of defective probability of each defective TSV which is expressed as

$$P_{defective\_part} = p \cdot \prod_{m=1}^{N_d-1} defective\_prob(TSV_m) \qquad (3.9)$$

where p is the defective probability of cluster center and equals to TSV failure rate. '$defective\_prob(TSV_m)$' is the defective probability of defective TSV_m excluding cluster center, based on Eq. (3.5), it equals to p·(1+($\frac{1}{d_m}$)$^{\alpha}$), where d_m is the distance between TSV_m and the cluster center.

Similarly, the probability of $|Q|$- N_d non-defective TSVs $P_{non\_defective\_part}$ is the product of probability of the remaining non-defective TSVs which is

$$P_{non\_defective\_part} = \prod_{n=1}^{|Q|-N_d} non\_defective\_prob(TSV_n) \qquad (3.10)$$

where 'non_defective_prob(TSV_n)' denotes the probability of non-defective TSV_n, which equals to 1- p·(1 + ($\frac{1}{d_n}$)$^{\alpha}$), and d_n is the distance between TSV_n and the cluster center.

Algorithm The probability that a *block* cannot berepaired

1 Place TSVs into block, each TSV_k has its property $TSV_k(X_k, Y_k, group\_index_k)$;
2 Find out all cases of a block that cannot be repaired, which are stored in *non_repair_pattern*
// Calculate $P_{non\text{-}repair}$ by summing up the probability of each defective TSV pattern from step 2
3 $P_{non\text{-}repair} = 0$
4 **for** each *pattern* ∈ *non_repair_pattern* **do**
// Calculating the probability of one defective TSV pattern
5 $P_{pattern}$ =probability of a defective TSV pattern
6 $P_{non\text{-}repair} = P_{non\text{-}repair} + P_{pattern}$
7 **end for**
8 **Return** $P_{non\text{-}repair}$

Figure 3.7: Algorithm for calculating the probability that a block cannot be repaired

3.3.3 Exhaustive search for best grouping ratio

Section 3.3.1 and Section 3.3.2 explain how yields of 3D-ICs can be calculated under two types of TSVs defects distribution: independent distribution and clustering distribution for a number of TSVs with specified grouping ratio. To obtain the best grouping ratio which can achieve 100% yield while achieving minimum hardware cost, an exhaustive search algorithm is presented in Figure 3.8. The algorithm analyses the yield and hardware cost for grouping ratios belonging to the pre-defined redundancy percentages. In this Chapter, it is set to be 100%, 50%, 25%, and 10%. Note that this grouping ratio searching algorithm can be applied for both independent and clustering TSV defects distributions, only the yield analysis (Step 2) is obtained using the corresponding calculation method presented in Section 3.3.1 and Section 3.3.2. In terms of hardware cost of proposed TSV repairing architecture (as illustrated in Figure 3.2), it can be seen that, for a given grouping ratio m:n, each group consume 2m+n (n+1)-to-1 multiplexers. To simplify the rerouting cost, (n+1)-to-1 multiplexer can be replaced by n 2-to-1 multiplexers. Such that it is able to compare the rerouting cost in terms of number of 2-to-1 multiplexers. And for a grouping ratio m:n, the total rerouting cost within one group is (2m+n)·n 2-to-1 multiplexers. For a given number of total regular TSV N_R and grouping ratio m:n, the total rerouting cost is $\frac{N_R}{m}$·(2m+n)·n 2-to-1 multiplexers, where $\frac{N_R}{m}$ is the group number. This will be used to calculate the rerouting cost in the simulation section (Section 3.4).

Algorithm Exhaustive search for best grouping ratio

Input: Regular TSV number m, TSV faulty rate p, pre-set target yield Y_{target}, pre-set redundancy percentages

Output: *best grouping ratio*

1 Start from initial redundancy percentage Rd= 100%

2 **For** grouping ratios $\in Rd$ do

Analyse the yield Y (Section 3.3.1 for independent defect distribution) & (Section 3.3.2 for clustering defect distribution)

Calculate the hardware cost (Section 3.3.3)

3 **Repeat** step 2 for each pre-set redundancy percentage

4 Compare all the searched grouping ratios with $Y > Y_{target}$ in terms of hardware cost

5 **Return** *best grouping ratio*

Figure 3.8: Exhaustive searching algorithm for best grouping ratio.

3.4 Simulation Results

In this section, firstly, a simulation flow for evaluating the proposed grouping-based TSV repairing technique is introduced in Section 3.4.1 (Figure 3.9). Secondly, in Section 3.4.2, two sets of simulations are conducted to evaluate the performance of the proposed grouping technique of regular and redundant TSVs. The objective of both simulations is to maximize yield and minimize hardware cost (multiplexer and spare TSV), where TSV failure rate is a constraint. The objectives are achieved through careful selection of grouping ratios and redundancy percentage of spare TSVs. The first simulation examines the effect of grouping ratios on different number of regular TSVs affected by various TSV failure rates when considering independent defect distribution. The second simulation evaluates the trade-off between yield and hardware cost (multiplexer and spare TSV), when considering both independent and clustering defect distributions.

3.4.1 Simulation Flow

All simulations are conducted on Intel Xeon Quad Core 2.7 GHz processor with 12 GB RAM. A simulation flow for generating a best grouping ratio for a design with a number of regular TSVs is shown in Figure 3.9. The flow inputs are the design specification refers to total number of TSVs, Nr and TSV fault rate *p*. The flow is based on the exhaustive grouping ratio search algorithm described in Section 3.3.3,

which is implemented using MATLAB. The flow can analyze the trade-off between yield and hardware cost for various grouping ratios. By using the method described in Section 3.3.1 and Section 3.3.2, yield can be achieved for independent defect distribution (Eq. (3.1) – Eq. (3.3)) and clustering defect distribution (Eq. (3.4) – Eq. (3.10), Figure 3.7) respectively. The output of the flow is an optimized grouping ratio with respect to yield and corresponding hardware cost.

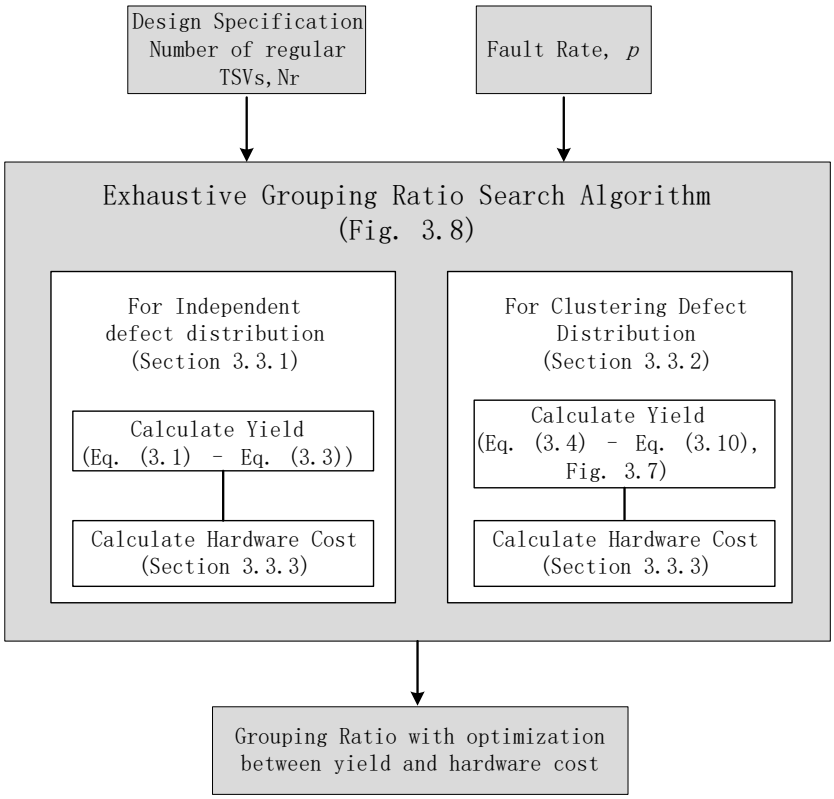


Figure 3.9: Proposed simulation flow for generating best grouping ratio with optimization between yield and hardware cost.

3.4.2 Evaluation of Proposed Grouping-based TSV Repairing Technique

The first set of simulation analyses the effect of independent defect distribution on yield and hardware cost, where hardware cost is expressed in terms of spare TSVs and multiplexers. Yield and hardware cost is analyzed by varying the number of regular TSVs and failure rates for two grouping ratios 5:4 and 10:4 respectively. These two grouping ratios are chosen for illustration purposes. The results are shown in Table 3.1 for 10,000 and 1,000,000 regular TSVs with TSV failure rate of 0.001, 0.005, and 0.01. The number of regular TSVs is chosen because recent designs have millions of regular TSVs [48, 51]. The TSV failure rate is not exactly known and recent publications have chosen various failure rates from 10^{-4} [10] to 0.05 [107] and in this work it is up to 0.01 to account for increased TSV count in recent designs. In

this case (independent defect distribution), yield is calculated by using Eq. (3.1) and Eq. (3.3). Table 3.1 analyses the two groups of regular TSVs (10,000 and 1,000,000) separately to examine the trade-off between hardware cost and yield. In case of 10,000 regular TSVs, it can be seen that for all TSV failure rates (0.001 to 0.01), 100% yield is achieved by both grouping ratios 5:4 and 10:4. However grouping ratio 5:4 requires higher hardware cost than the grouping ratio of 10:4, as it requires additional 4,000 spare TSVs and 16,000 multiplexers. This is because under binomial distribution and given failure rate (as input), grouping ratio of 10:4 gives enough spare TSVs in one group and more spare TSVs do not lead to yield improvement. In the case of 1,000,000 regular TSVs, failure rate starts to show its effects on yield. As can be seen, at TSV failure rate of 0.001, 100% yield is achieved using the grouping ratio of 10:4 (lower hardware cost), however this trend changes at higher failure rates (0.005 and 0.01) and yield drops by up to 2%. This means that for 100% yield, the grouping ratio of 5:4 is better than 10:4. This table clearly shows the trade-off between yield and hardware cost and demonstrates that it is possible to achieve 100% yield at lower hardware cost by careful selection of grouping ratios. Grouping ratios and redundancy percentage are determined through an exhaustive search to achieve highest yield and lowest hardware cost as shown in the next simulation.

Table 3.1: Trade-off analysis between yield and hardware cost (number of multiplexers and spare TSVs) when considering independent defect distribution.

Grouping Technique	Number of regular TSVs					
	10,000			1,000,000		
	TSV failure rate *p*					
	0.001	0.005	0.01	0.001	0.005	0.01
Grouping Ratio (*gr*)	5:4					
Redundancy percentage (%)	80%					
Yield (%)	100	100	100	100	100	100
Spare TSV	8,000			800,000		
Multiplexer (2-to-1)	1.12×10^5			1.12×10^7		
Grouping Ratio (*gr*)	10:4					
Redundancy percentage (%)	40%					
Yield (%)	100	100	100	100	99	98
Spare TSV	4,000			400,000		
Multiplexer (2-to-1)	9.6×10^4			9.6×10^6		

Table 3.2: Trade-off analysis between yield and hardware cost when considering independent and clustering defect distribution， regular TSV number is 6000, TSV fault rate is 0.01.

Redundancy percentage (%)		Grouping ratio (*gr*)	Yield (%) under Two types of defect distributions			Multiplexer cost (2-to-1)	Runtime (s)
			Independent	Clustering			
				α=1	α=2		
1	100% (6000 spare TSVs)	1:1	55	31	7.0	6000	430
2		2:2	99	96	87	24000	300
3		3:3	100	100	99	42000	288
4		**4:4**	**100**	**100**	**100**	**60000**	139
5		5:5	100	100	100	78000	133
6	50% (3000 spare TSVs)	2:1	41	20	4.0	15000	568
7		4:2	97	91	79	30000	303
8		6:3	100	99	98	45000	296
9		**8:4**	**100**	**100**	**100**	**60000**	286
10		10:5	100	100	100	75000	272
11	25% (1500 spare TSVs)	4:1	23	9.0	1.0	13500	831
12		8:2	96	79	57	27000	356
13		12:3	99	98	94	40500	315
14		16:4	100	100	99	54000	302
15		**20:5**	**100**	**100**	**100**	**67500**	282
16	10% (600 spare TSVs)	10:1	4.3	<<1	<<1	12600	1493
17		20:2	66.9	37.8	5.3	25200	621
18		30:3	93.7	89.1	79.2	37800	372
19		40:4	98.8	98.3	96.6	50400	338
20		50:5	99.7	99.6	99.3	63000	319

The second set of simulation analyses the trade-off between yield and hardware cost, when considering clustering defect distribution and it is shown that grouping ratios and redundancy percentages can be used to achieve 100% yield and reduce hardware cost, when considering clustering defects. In this case (clustering defect distribution) yield is calculated using the algorithm shown in Figure 3.7. For this simulation, the number of regular TSVs and failure rate is fixed and for illustration purposes, 6000 regular TSV and 0.01 failure rate are considered. The simulation results are shown in Table 3.2. This set of simulation considers three sets of redundancy percentages (100%, 50% 25% and 10%) as shown in the first column, and for each set of redundancy percentages, five grouping ratios are considered as shown in

the second column. These five grouping ratios are used because the yield saturates at 100%. Yield is calculated for two clustering coefficients (α =1 and α =2) and for each clustering coefficient, the results are shown in the third column along with yield results for independent defect distribution for comparison. In this work, only two clustering coefficients are analyzed and other clustering coefficients can be similarly analyzed. The last two columns show 2-to-1 multiplexer overhead for each grouping ratio and redundancy percentage, and run time for the yield calculation algorithm (for the case of setting α=1) respectively.

From Table 3.2, the following three observations can be found. Firstly, it can be seen that to achieve 100% yield, independent defect distribution incurs lower hardware cost in comparison to clustering defect distribution. For example, as shown in Table 3.2, when considering 100% redundancy, independent defect distribution obtains 100% yield using a grouping ratio of 3:3, which requires 42,000 (2-to-1) multiplexers, while at α =2 clustering coefficient, 100% yield is obtained by using 4:4 grouping ratio, which requires (60,000-42,000) 18,000 additional multiplexers. This trend continues with the other two sets of redundancy percentages.

Secondly, when observing the yield drop across the two defect distributions (independent and clustering), it can be observed that in cases of a small number (less than 2) of spare TSV per group, the yield drop is more drastic than groups with additional spares. For example, in the case of 100% redundancy and grouping ratio of 1:1, the yield is only 31% and 7% in case of two clustering coefficients (α =1 and α =2), while at grouping ratio of 3:3, it is 100% and 99% respectively when considering the two clustering coefficients. This is because in case of clustering defects, as shown in Figure. 3.4, the defect probability of a TSV increases if that is close to clustering center. The probability of a cluster with more than three defective TSVs is much smaller than a cluster of more than one defect (Eq. (3.8)). This is why the defective probability increment is much smaller in the case of 3:3 grouping ratio in comparison to 1:1 grouping ratio leading to higher yield in the case of 3:3 grouping ratio. Finally, it is observed that despite the yield loss due to clustering defects, it is still possible to reduce hardware cost (number of spare TSVs) by careful selection of grouping ratio and redundancy percentages. For example, from Table 3.2, it can be seen that 100% yield is possible for all defect distributions across all three sets of redundancy percentages. In the case of 100% redundancy and grouping ratio of 4:4, 6,000 spare TSVs and 60,000 (2-to-1) multiplexers are needed to obtain 100% yield. The hardware cost in terms of spare TSVs can be reduced by using 50% redundancy and grouping ratio of 8:4, which achieves 100% yield using the same number (60,000) of multiplexers but with only 3,000 spare TSVs thereby saving 50% spare TSVs without affecting targeted (100%) yield. Moreover, additional spare TSV savings are possible by using 25% redundancy and grouping ratio of 20:5, but that comes at the cost of (67,500-60,000) 7,500 additional multiplexers. These two sets of simulations clearly demonstrate the trade-off between yield and hardware cost (number of multiplexer and spare TSVs) and show that careful selection of grouping ratio and redundancy percentage (spare TSV) can reduce the number of multiplexers and spare TSVs without affecting yield, when

considering independent and clustering defect distributions. For illustration purpose, the trade-off analysis has also been done for various design size. Table 3.3 and Table 3.4 show similar results when considering regular TSV to be 1,000 and 10,000. The key findings holds, as for regular TSV number of 1,000 (Table 3.3), when considering independent defect distribution, grouping ratio of 12:3 is the best grouping ratio for achieving 100% yield with least number of multiplexers, while 40:4 is the best grouping ratio for achieving 100% yield with minimized number regular TSVs. Additionally, for large number of regular TSVs (10,000 in Table 3.4), when considering clustering distribution (α=1), grouping ratio of 20:5 is selected to be best grouping ratio for achieving 100% yield with minimized hardware cost (total number of spare TSVs and number of multiplexers).

Table 3.3: Trade-off analysis between yield and hardware cost when considering independent and clustering defect distribution，regular TSV number is 1,000, TSV fault rate is 0.01.

Redundancy percentage (%)		Grouping ratio (*gr*)	Yield (%) under Two types of defect distributions		Multiplexer cost (2-to-1)
			Independent	Clustering α=1	
1	100% (1000 spare TSVs)	1:1	90	82	1,000
2		2:2	100	99	4,000
3		3:3	100	100	7,000
4		4:4	100	100	10,000
5		5:5	100	100	13,000
6	50% (500 spare TSVs)	2:1	86	77	2,500
7		4:2	100	98	5,000
8		6:3	100	100	7,500
9		8:4	100	100	10,000
10		10:5	100	100	12,500
11	25% (250 spare TSVs)	4:1	78	66	2,250
12		8:2	99	96	4,500
13		**12:3**	**100**	100	**6,750**
14		16:4	100	100	9,000
15		20:5	100	100	11,250
16	10% (100 spare TSVs)	10:1	59	38	2,100
17		20:2	94	85	4,200
18		30:3	99	98	6,300
19		**40:4**	**100**	100	**8,400**
20		50:5	100	100	10,500

Table 3.3: Trade-off analysis between yield and hardware cost when considering independent and clustering defect distribution，regular TSV number is 10,000, TSV fault rate is 0.01.

Redundancy percentage (%)		Grouping ratio (*gr*)	Yield (%) under Two types of defect distributions		Multiplexer cost (2-to-1)
			Independent	Clustering α=1	
1	100% (10,000 spare TSVs)	1:1	37	21	10,000
2		2:2	100	94	40,000
3		3:3	100	100	70,000
4		4:4	100	100	100,000
5		5:5	100	100	130,000
6	50% (5,000 spare TSVs)	2:1	22	10	25,000
7		4:2	95	87	50,000
8		6:3	100	99	75,000
9		8:4	100	100	100,000
10		10:5	100	100	125,000
11	25% (2,500 spare TSVs)	4:1	9	2	22,500
12		8:2	93	70	45,000
13		12:3	99	97	67,500
14		16:4	100	99	90,000
15		**20:5**	100	**100**	**112,500**
16	10% (1,000 spare TSVs)	10:1	1	<<1	21,000
17		20:2	51	21	42,000
18		30:3	90	83	63,000
19		40:4	98	97	84,000
20		50:5	100	99	105,000

3.5 Concluding Remarks

TSV based 3D-ICs lead to low yield in current fabrication process. This chapter proposes a TSV grouping technique for allocating spare TSVs with regular ones in order to achieve highest possible yield at lowest possible hardware cost (number of multiplexers and spare TSVs) under independent and clustering defect distributions. To the best of our knowledge, this is the first study to propose a modeling mechanism for clustering defects on TSVs, furthermore it shows how yield can be calculated using clustering defect distribution. Simulation results show that for a given number of regular TSVs and failure rate, it is possible to achieve 100% yield while minimizing hardware cost (number of multiplexers and spare TSVs) both under independent and clustering defect distributions. This is achieved through careful selection of grouping ratios and redundancy percentage of spare TSVs. Note that the hardware cost is in terms of number of multiplexers and number of spare TSVs, it is not a combined parameter.

This chapter examines a mathematical yield analysis for both independent and clustering defects distribution. However, the defect mechanism and its fault modelling method is not addressed. Therefore, Chapter 4 takes into account TSV defects mechanisms and their modelling method (as discussed in Section 2.2), and produce an online fault tolerance technique for detection and recovery in the presence of TSV defects.

Chapter 4

Online Fault Detection and Recovery for TSV-based 3D-ICs

Chapter 3 presents a technique that addresses the yield issue of 3D-ICs. This chapter presents a technique that addresses both yield and reliability issue of 3D ICs. It presents the design, validation and evaluation of an efficient online fault tolerance technique for fault detection and recovery in the presence of three TSV defects: voids, delamination between TSV and landing pad, and TSV short-to-substrate. The technique employs transition delay test for TSV fault detection. Fault recovery is carried out by employing redundant TSVs and rerouting input/output signals to fault-free TSVs. This technique is efficient because it requires small (2 x number of TSVs per group) number of clock cycles for fault detection and recovery. Simulations are carried out using HSPICE and ModelSim to validate fault detection and recovery. Synthesized RTL model of this fault tolerance technique is used to evaluate the area overhead. It is shown that regular and redundant TSVs can be divided into groups to minimize area overhead without affecting fault tolerance capability of the technique. Synthesis results using 130-nm design library show that 100% repair capability can be achieved with low area overhead (4% for the best case).

The publication related to this chapter is listed in Chapter 1 Section 1.5 (Publication 2) and its corresponding key contributions are:

- An online fault tolerance technique is generated for fault detection and recovery in the presence of three TSV defects: voids, delamination between TSV and landing pad, and TSV short-to-substrate.

- Through the validation and evaluation of the proposed fault tolerance technique, the effectiveness and efficiency of the technique is demonstrated and it is shown that regular and redundant TSVs can be divided into groups to minimize area overhead without affecting the fault tolerance capability of the technique.

4.1 Introduction

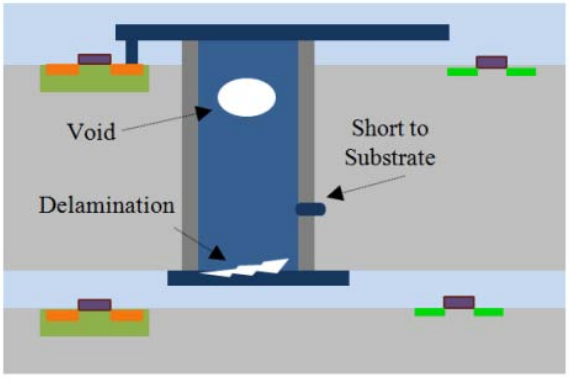


Figure. 4.1. Three types of TSV defects that are targeted in this Chapter.

Chapter 2 has shown that the yield of TSV based 3D-ICs is affected by TSV manufacturing defects and its reliability is affected by thermal stress induced during fabrication process and normal operation [22, 51, 91, 104, 114, 115, 121, 123]. TSV manufacturing defects are introduced in the bonding stage of the fabrication process when different dies are bonded together and one defective TSV can potentially fail the entire design along with known-good dies. These challenges are highlighted and novel solutions have been proposed for improving testability, yield and reliability [22, 81, 91, 104, 114, 115, 117, 121, 123, 131, 135, 151, 160, 161]. Various types of TSV defects caused by manufacturing process and thermal stress are highlighted in [91, 114] such as: improper TSV filling, cracks and delamination between TSV and landing pad, pinhole defect (short between TSV to substrate) and voids growth due to electromigration. Out of all these defects, three types of defects have been identified as major TSV defects: void, delamination and TSV short to substrate [91, 104, 114, 115, 121, 123] (Figure 4.1). This chapter focuses on these three defect types, which have been studied from both pre-bond and post-bond test point of view [91, 104, 114]. One known issues with pre-bond testing is that it does not scale well, because defects can be introduced during bonding stage as well as during normal operation, for example due to thermal stress as shown in Section 2.2. Research reported in [91] shows that thermal stress can damage TSV interconnects, leading to delamination at TSV interface with the bonding pad. It is reported in [81] that void growth can also occur during normal operation due to thermal load. This means methods for improving in-field reliability are needed.

A popular method for improving yield is to introduce redundant TSVs and associated control logic [17, 160, 162, 163, 164, 165]. References [117, 131, 161] utilized redundant TSVs in a TSV block for improving yield by repairing defective TSVs. The work presented in Chapter 3 and published in [160] employs redundant TSVs (as in [106, 156, 161]) and partition multiple regular and redundant TSVs into TSV groups using a grouping ratio, where redundant TSVs are used to repair defective TSVs in a group. This is used to improve yield and reduce hardware overhead. The only work that focuses on improving in-field TSV reliability is presented in [151], which uses on-chip processor for online fault detection and recovery.

However, available literature does not show any hardware based infield fault tolerance technique for TSV fault detection and recovery where such an on-chip processor is not available.

The aim of this chapter is to present an efficient and cost-effective online fault tolerance technique capable of TSV fault detection and recovery for designs with detailed evaluation and validation. TSV Fault detection is realized using transition delay test based on scan chains which are widely used in 2D circuits for detecting interconnects delay faults as studied in Section 4.2. The proposed technique is efficient because it provides hardware based solution which requires only 2 clock-cycles for fault detection and recovery per TSV, leading to faster detection and recovery than available methods [135, 151]. It is cost-effective because the hardware overhead is minimized (without affecting repair capability) by selecting the best grouping ratio through an exhaustive search method described in Chapter 3. Using Synopsys design compiler, it is shown that the hardware overhead of the proposed technique is lower than available techniques [104, 121, 135, 151], while also achieving 100% repair capability. This chapter presents the following contributions:

1. An efficient online fault tolerance technique, which requires only a small number of clock cycles (twice the number of TSVs in a group, 2x(m+n)) for fault detection and recovery in the presence of three latent TSV defects: void, delamination and short-to-substrate.
2. Electrical and logical simulations to demonstrate correct operation of detection and recovery using realistic fault models and synthesized RTL model of this technique.
3. The trade-off between repair capability and area overhead of this technique is evaluated with a 130-nm technology and using Synopsys design compiler. It is shown that the area overhead can be reduced without affecting repair capability through appropriate grouping of regular and redundant TSVs.

This chapter is organized as follows: Preliminaries on fault modelling and detection method for interconnects are presented in Section 4.2. The online fault tolerance technique is described in Section 4.3. Simulation results are presented in Section 4.4 and Section 4.5 concludes the chapter.

4.2 Preliminaries

In traditional 2D integrated circuits, the complex digital logic that constitutes an electronic design will be tested to ensure that the design operates correctly and the expected specification is met before the design shipped to the customers. Since TSVs are vertical interconnects in 3D circuits and can be regarded as traditional interconnects when testing them. Existing fault modelling and test method can be leveraged to testing TSV interconnects. Regarding moving from testing 2D interconnects to TSVs, several issues should be investigated:

- Fault modeling: Fault models are used to study and simulate the defects behavior.

With respect to 2D interconnects, resistive open [166, 167] and resistive short [168] are two main defect types. As discussed in Section 2.2, void and delamination TSV defect types can be modeled as resistive open defects as they both increase the TSV resistance. TSV short to substrate defect is similar to traditional resistive short defect in 2D wires as they both cause leakage and affect signal integrity when transmitting a signal. The difference is that TSV short to substrate involves the leakage current from TSV to silicon substrate whereas for 2D wires the short defect can usually be created when two wires are accidentally connected to each other. Since the physical behavior of TSV defects and 2D interconnects defects is similar. Fault models of 2D interconnects can also be used, there are stuck-open and stuck-short fault models. Stuck-open fault can happen in 3D circuits when TSVs involve either large void inside TSVs due to an imperfect TSV manufacturing process or complete TSVs delamination between TSV and its landing pad resulting in no contact at the interface. Stuck-short fault can happen when the pin-hole in TSV isolation layer is quite large leading to TSV short to silicon substrate.

- Delay fault: In 2D wire interconnects, delay faults result in additional circuit delay

which causes the failure of the circuit due to cannot meet the performance requirements. This means that when conveying a rising or falling transition, the rising (falling) time will be longer than expected. This can happen in TSVs which are suffering from partial open defects (i.e. small voids inside TSVs). Additionally, when TSVs have small size short to substrate (pin-hole) defect, due to the leakage current, the rising time taken to transmit a rising transition will increased. Note that the falling time for propagating a falling transition will be shorter as leakage current to silicon substrate accelerates the voltage drop at the TSV end (Figure 2.3(c)). Thus when detecting TSV short to substrate defect, only signal rising time is used as criteria, as discussed in Section 4.3.

- Test point insertion and Scan chains: Besides employing the fault modeling techn-

ique in 2D test, a general test method which uses test point insertion and scan chain is also helpful to 3D TSV testing. Test point insertion is a technique which adds logic elements, referred to as test points to increase controllability or observability of a node [169]. A scan cell feeding multiplexer has been used in test community to improve controllability of a node, as shown in Figure 4.2. Meanwhile an observation point constituting a scan cell can be added to improve the observability of a node. Scan chains are constructed by connecting a number of scan cells together. A scan cell is a flip-flop which allows propagating test inputs or test results. The test pattern can be loaded into the scan chain, while test results can be captured by scan cells and shifted out to storage units when needed.

- Delay fault: The delay test employ delay fault model to detect defect that involves

additional delay when transmitting signals. The time taken for a signal transition to pass the TSV interconnect is compared to a specified test clock period by capturing the logic value at

the TSV output into scan flip-flop after a set time corresponding to the test clock period. The implementation of delay test on detecting void, delamination, and TSV short to substrate defects is further elaborated in Section 4.3.

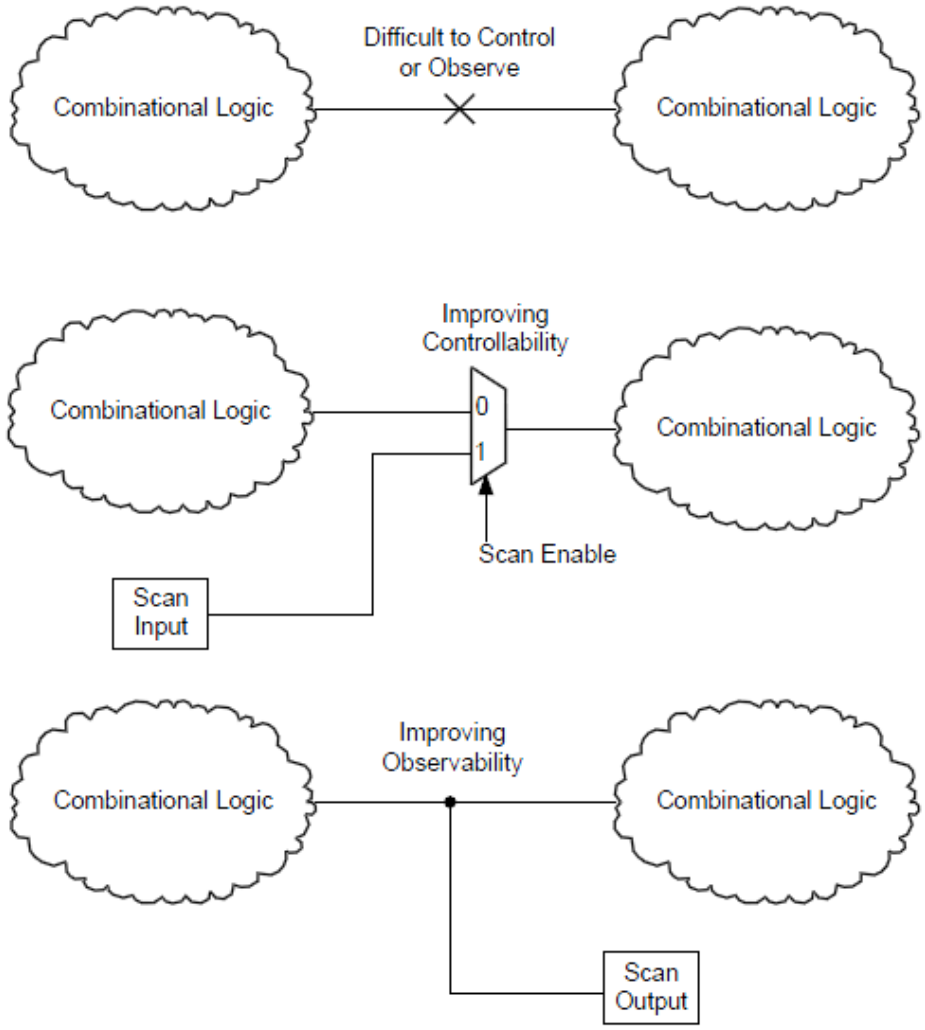


Figure. 4.2: Test point insertion [170].

4.3 TSV Fault Tolerance Technique

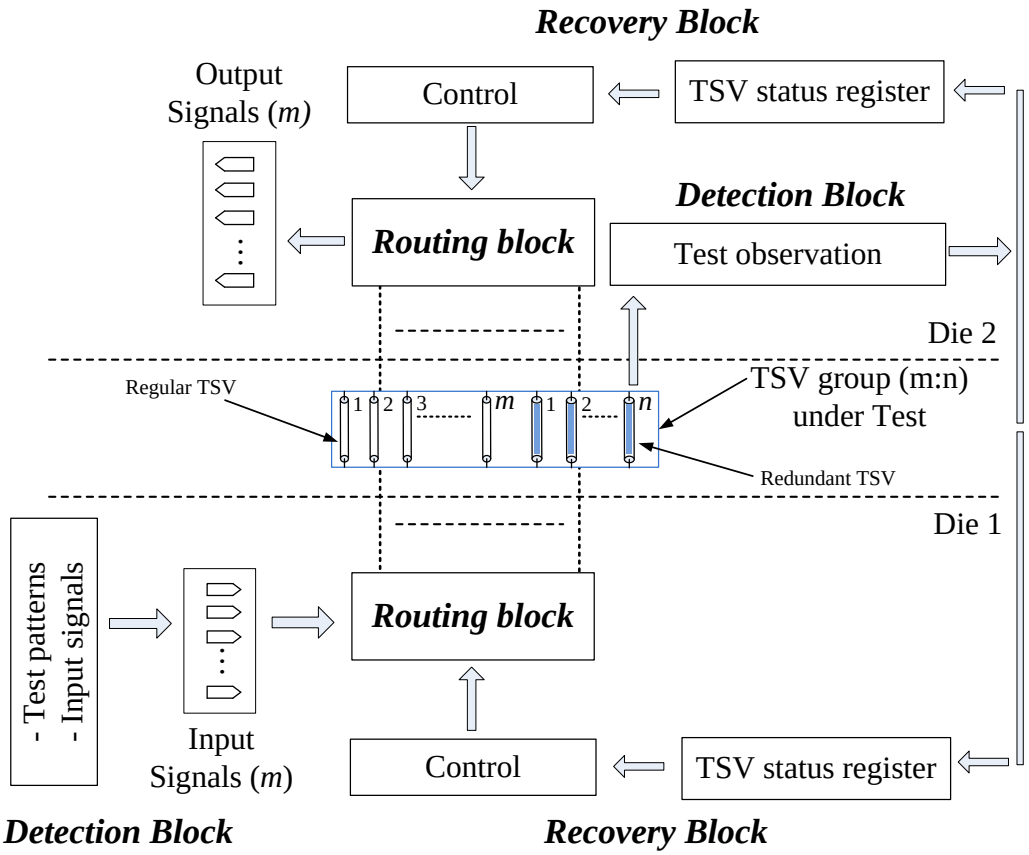


Figure 4.3: Architecture of the proposed online fault tolerance technique

Figure 4.3 shows the block diagram of the proposed fault tolerance technique to test and repair a single TSV group. It consists of three blocks: detection block, recovery block and routing block. These blocks are used to test and repair a group of TSVs (referred as TSV group). A TSV group with a grouping ratio of *m:n*, consists of *m* input (output) signals, *m* regular TSVs, and *n* redundant TSVs, where each TSV group can tolerate up to *n* TSV defects. The number of redundant TSVs in a design has an effect on yield, repair capability and hardware cost. For a given fault rate, recent papers have proposed algorithms to determine grouping ratio to minimize hardware cost and maximize yield [135] and the work presented in Chapter 3. In this chapter, it is assumed that at design time, TSVs are divided into groups.

The detection block (Figure. 4.3) is used for testing each TSV in a group. Input test patterns are applied from a die (Die 1) and output test response is observed through Test observation block located on subsequent die (Die 2). The detection block uses delay test to differentiate between faulty and fault-free TSVs, where each TSV is tested for void, delamination and short-to-substrate defects (Figure 4.1). The status of each TSV is updated in TSV status registers, which are located on both dies and hold the number and location of all faulty TSVs in a group. In case, a faulty TSV is found, fault recovery is initiated after identifying the

number and location of all faulty TSVs in a group. Section 4.3.1 and Figure 4.5 provide detailed description of the detection block. Note that the detection block does not distinguish between different defect types, as that is typically required for diagnosis. The recovery block is used to bypass defective TSVs with fault-free TSVs. The recovery block is implemented on both dies that are connected by the TSV group. As shown in Figure 4.3, it consists of TSV status register and control. TSV status register holds fault status of each TSV (‘1’ represents faulty TSV and ‘0’ represents fault-free). Control provides appropriate control signals to bypass faulty TSVs and it is used to configure the Routing block. The routing block consists of a set of multiplexers and de-multiplexers to connect each signal line to a TSV. The control signals of these multiplexers (de-multiplexers) are provided by the control unit of the Recovery block. Section 4.3.2 and Figure 4.8 provide detailed description of the recovery and routing blocks.

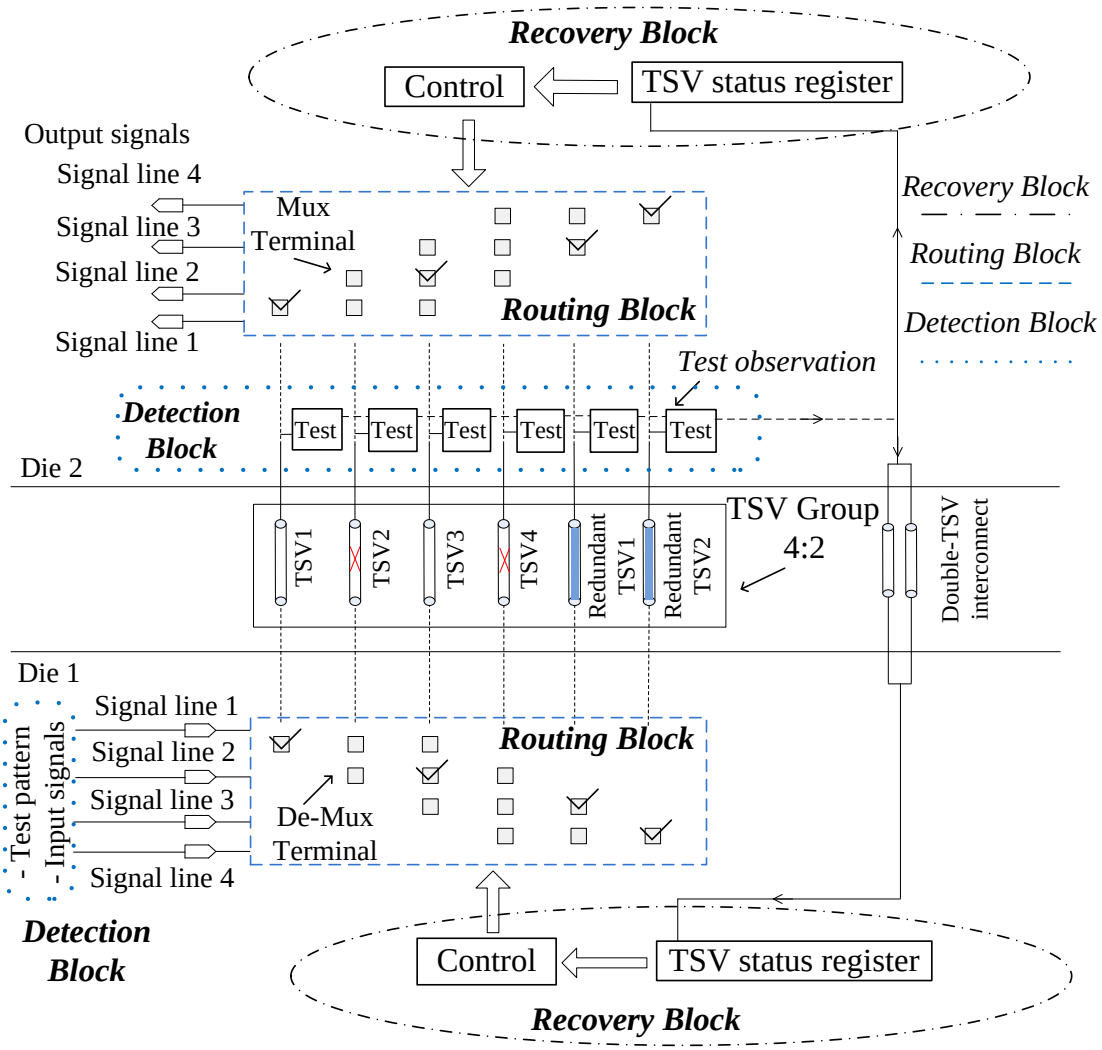


Figure 4.4: Detection and recovery blocks for a grouping ratio of 4:2.

Figure 4.4 shows the detection, recovery and routing blocks of the proposed fault tolerance technique. For illustration purpose, a grouping ratio of *4:2* is used, where each group consists

of 4 regular TSVs and 2 redundant TSVs, therefore it can tolerate up to two defective TSVs. Test input and Test observation blocks are used for testing each TSV for three defects (three defects shown in Figure 4.1); test results are stored in TSV status registers on both dies. A double TSV interconnection is used to update the TSV status register on die 1. This concept was also used in [51] for error communication between dies. Once fault detection is complete, recovery is initiated to reroute signals through fault-free TSVs (replacing defective TSVs) by reconfiguring the routing block between signals and TSVs (Figure 4.4). The control unit is used to generate the selection signal for each signal line to connect it with the appropriate TSV. The connection boxes (de-Mux terminal within routing block) shown in Figure 4.4 are implemented by using de-multiplexers between input signals and TSVs (Figure 4.5). The connection for input (Die 1) and output (Die 2) signals is similar, the only difference is that de-multiplexers are used with input signals and multiplexers are used with output signals. For a grouping ratio of *4:2*, each signal can use one of three possible TSVs; hence a 1-to-3 de-multiplexer is needed. The control is also used to report when the number of defective TSVs is higher than the maximum tolerance limit of a TSV group.

To illustrate the working of the recovery block for a grouping ratio of 4:2, assume there are two defective TSVs (TSV2 and TSV4) in a group (Figure 4.4). The reconfiguration circuit on both dies (Die 1 and Die 2) are similar and for illustration, thus only the one on Die 1 is explained. It follows the following two connection rules. Firstly, once a TSV has been used by a signal line (shown as a tick in the connection box), no other signal line can use that TSV. This is because one TSV can only be occupied by only one signal line. Secondly, if a TSV is defective, all connection boxes (de-Mux or Mux terminals, Figure 4.4) that correspond to that TSV cannot be used. Based on the connection rules and test results stored in the TSV status register, the availability of a TSV is found. Once the first signal line is connected, the method moves to the next signal line until all input signals are connected to a TSV. Next the operation of the detection and recovery blocks will be discussed.

4.3.1 Detection Block

Figure 4.5 shows the detection block for a single TSV, as an example. It consists of an input signal unit for test patterns and input signals, where transition signals are stored for test application. Figure 4.5 also shows the test observation block (Figure 4.3), where test output is observed in a flip-flop and stored in TSV status registers. The *SI* signal and NAND gate are used to initialize TSV status registers. The detection block applies a transition signal on a die (Die 1) and the output is observed on the subsequent die (Die 2). Next the working of the detection block when considering three defects (shown in Figure 4.1) is explained.

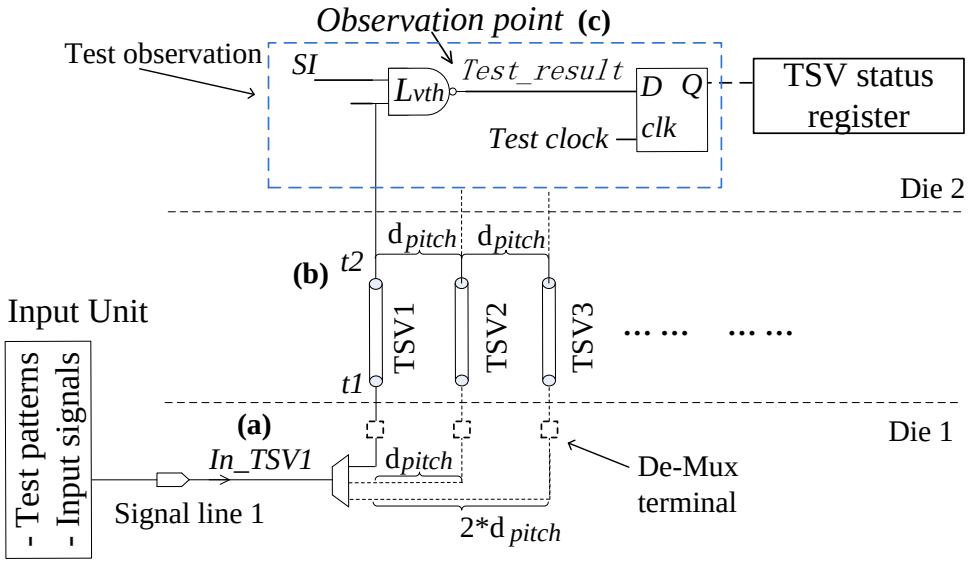


Figure 4.5: Detection block for a single TSV.

I. Void or delamination defect

As described in Section 2.2 void and delamination defects increase TSV resistance forming a higher resistance TSV path, thus increasing RC delay. To derive RC delay at *t2* end (Figure 2.3) of the TSV, a TSV electrical model with void or delamination defects is employed as shown in Figure 2.3(b). The RC delay of TSV at *t2* end is:

$$\left(R_{pull} + \frac{1}{2}R_{TSV} + \frac{1}{2}R_{open}\right)C_{TSV} + \left(R_{pull} + R_{TSV} + R_{open}\right)C_p \qquad (4.1)$$

where, R_{open} denotes the open resistance due to void or delamination defect, R_{pull} denotes the resistance of the pull-up network driving the TSV (de-multiplexers, Figure 4.5) and *Cp* denotes the parasitic capacitance of the test circuit. When the TSV is fault-free R_{open}~0, the TSV resistance is small (in hundreds mΩ) and can be ignored when compared to the pull- up resistance of driving gate R_{pull}, which is usually several kΩ, such that the path delay is not effected by the TSV resistance. However, in case of void or delamination defects, open resistance of a TSV (R_{open}) can be up to 1MΩ [123], which is significantly higher than the accumulative effect of R_{TSV} and R_{pull}.

Assuming the NAND gate (Figure 4.5) with logic threshold voltage denoted by L_{vth}, where L_{vth} of a gate input is the input voltage at which the output voltage reaches half of the supply voltage, while the other gate input(s) are at non-controlling value(s) [171]. A rising transition is applied to the TSV from *In_TSV1* (Figure 4.5), since the delay at t2 end is dependent on the value of R_{open}, the rising transition at *t2* becomes slower, such that at a given capture time, the voltage at the *t2* is lower than L_{vth}, as illustrated in Figure 4.6.

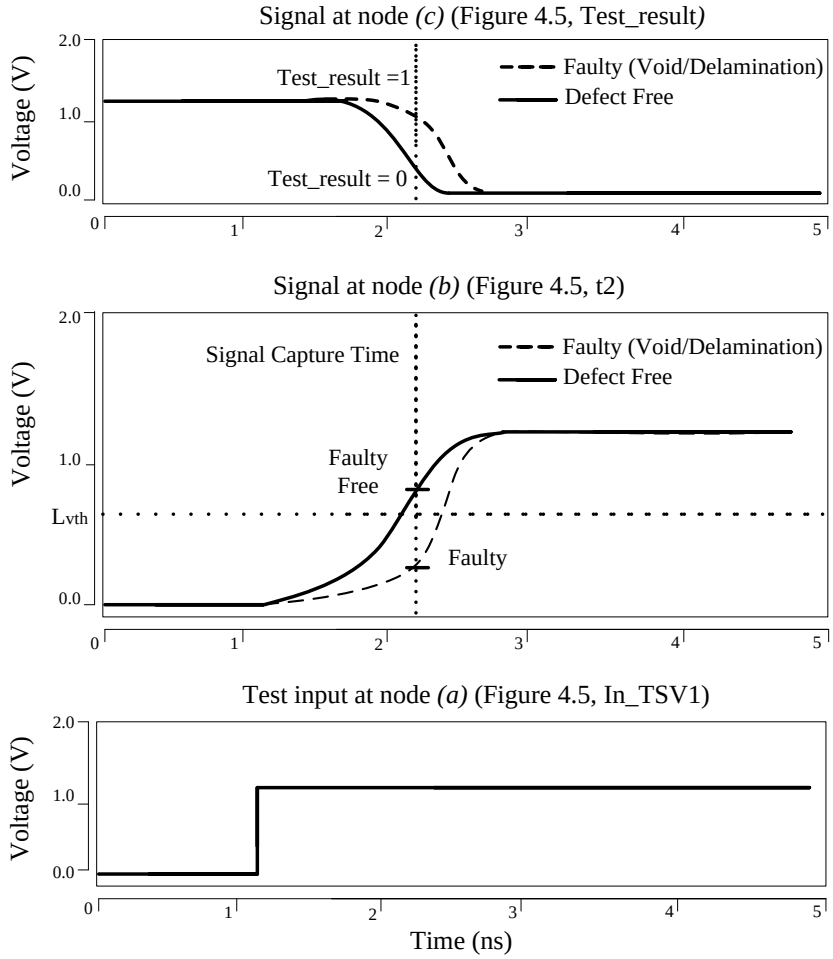


Figure 4.6: Test pattern for detection of void or delamination defect.

Therefore, if TSV open resistance due to void or delamination defect exceeds a critical value $R_{open\text{-}critical}$, the voltage at *t2* is lower than the L_{vth} at a given signal capture time and therefore the test detects a faulty signal Test_result=1 (Figure 4.6). Signal capture time represents the test clock frequency, which is applied to the flip-flop shown in Figure 4.5. Note that the internal clock may be used as a test clock to avoid overhead of a separate DFT clock [172].

TSV open critical resistance $R_{open\text{-}critical}$ is a function of logic threshold voltage L_{vth} and signal capture time (denoted by test clock frequency F_{clock}), where L_{vth} is kept at 50% of Vdd for illustration, otherwise it varies per gate input and is also effected by process variation [172]. The range of TSV open resistance [0, $R_{open\text{-}critical}$] is referred as the benign region, which means if $R_{open}<R_{open\text{-}critical}$, TSV is regarded as fault-free. whereas, when $R_{open}>R_{open\text{-}critcal}$, a defective TSV with void or delamination defect can be detected. In the first set of simulation results (Section 4.4.2), the delay of TSV as a function of R_{open} and evaluate $R_{open\text{-}critical}$ with respect to test clock frequency F_{clock} is investigeated.

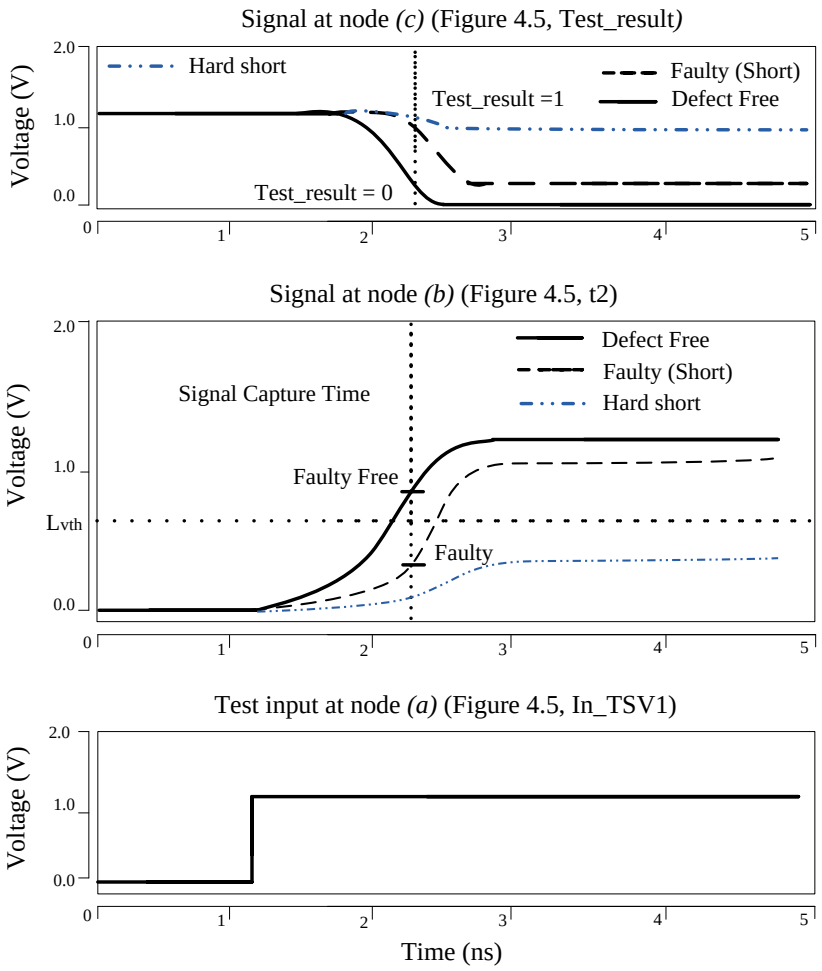


Figure 4.7: Test pattern to detect short-to-substrate TSV defect

II. Short to substrate defect

Short-to-substrate TSV defect leads to a resistive path between TSV and substrate and causes current leakage as shown in Figure 2.3(c), leading to reduced TSV charging current. Assume a rising transition is applied from *In_TSV1* (Figure 2.3(c)), which can be expressed as, $I_{charge} = I_1 - I_{leakage}$, where, I_1 is the input current at *t1* and $I_{leakage}$ is the leakage current from TSV to substrate through the short resistor (Figure 2.3(c)). Due to lower TSV charging current (I_{charge}), the rising transition time observed at *t2* increases with increase in defect size. The testing method is similar to that of void or delamination defect. In this case, critical resistance $R_{short\text{-}critical}$ is the maximum detectable R_{short} resistance, which is in the range [0, $R_{short\text{-}critical}$] and resistance higher than $R_{short\text{-}critical}$ is not detectable. This is detected by voltage at *t2* (Figure 4.5), which is compared with the logic threshold voltage (L_{vth}) at a given capture time, as illustrated in Figure 4.7. Note that the short-to-substrate resistance degrades the voltage level at both ends of TSV, which means that R_{short} forms a voltage divider between R_{short}, R_{pull} and R_{tsv}.

It is clear that with smaller R_{short}, the voltage at *t2* (Figure 4.5) is lower, such that for a rising transition signal, the voltage at *t2* is lower than L_{vth}, at signal capture time (Figure 4.7).

Simulation results using different defect sizes and test clock frequencies for detecting this type of defect are presented in Section 4.4.2.

4.3.2 Recovery Block

The recovery block (Figure 4.3) is used to bypass defective TSVs with fault-free TSVs and it is implemented on both dies that are connected by the TSV group. Recovery is initiated after completing the test for three defect types (shown in Figure 4.1) and it is used to reconfigure connections between input/output signals with fault-free TSVs. This section has two objectives. First, it describes the working of the reconfiguration process by considering a design with a grouping ratio of *4:2*. Second, it shows how the proposed technique can be scaled to any grouping ratio *(m:n)*.

The circuit for reconfiguring input and output signals are similar and therefore only input part is shown in Figure 4.8(a). As can be seen, it consists of the following six components: 1) A routing block consisting of de-multiplexers to connect signal lines with TSVs; 2) A latch chain that stores the selection signals for de-multiplexers; 3) TSV status register which stores faulty status information for each TSV, where a '0' indicates fault-free and '1' indicates faulty TSV; 4) A signal line counter to indicate the number of signals that have been configured, it is also used to update the latch chain through "enable"; 5) An adder "Faulty TSV accumulator", which can count faulty TSV number and provides input to the latch chain; 6) A comparator which compares the existing faulty TSV number with the tolerance limit of the TSV group, and reports an error in case of exceeding the tolerance limit. RTL description using Verilog hardware description language of the circuits for the illustrated group with a grouping ratio of 4:2 (Figure 4.8(a)) is shown in Appendix B.

In this example (Figure 4.8(a)), each input signal can be routed to three possible TSVs, which is why the selection signal for each de-multiplexer has two bits. Two latches are required in the latch chain to store the selection signal of each de-multiplexer. The top two latches are used for storing selection signals for the first de-multiplexer (signal line 1), and the remaining pairs (latches) are for rest of the de-multiplexers (signal line 2 to signal line 4). The selection signals for the first de-multiplexer are scanned in to the latch chain from bottom, and it is shifted up such that after completing the configuration process, it moves to the pair of latches on top. The proposed reconfiguration method sets the selection signals for de-multiplexers sequentially. This is managed by signal line counter, it receives (shifted out) values from TSV status register, if a '0' is received, it means that a fault-free TSV is found and a signal line can be configured. It outputs an "enable" signal, which triggers the latch chain to scan in new values from faulty TSV accumulator. It is referred as an accumulator because as soon as '1' is received, it means that for all the remaining signal lines (to be configured), their default TSV connection is not available. Signal line counter is also used to count the number of signal lines that have been configured.

For a grouping ratio of *4:2*, only four signal lines have to be configured, such that once the signal line counter reaches the count of four, it disables the latch chain, which means that the configuration process is complete.

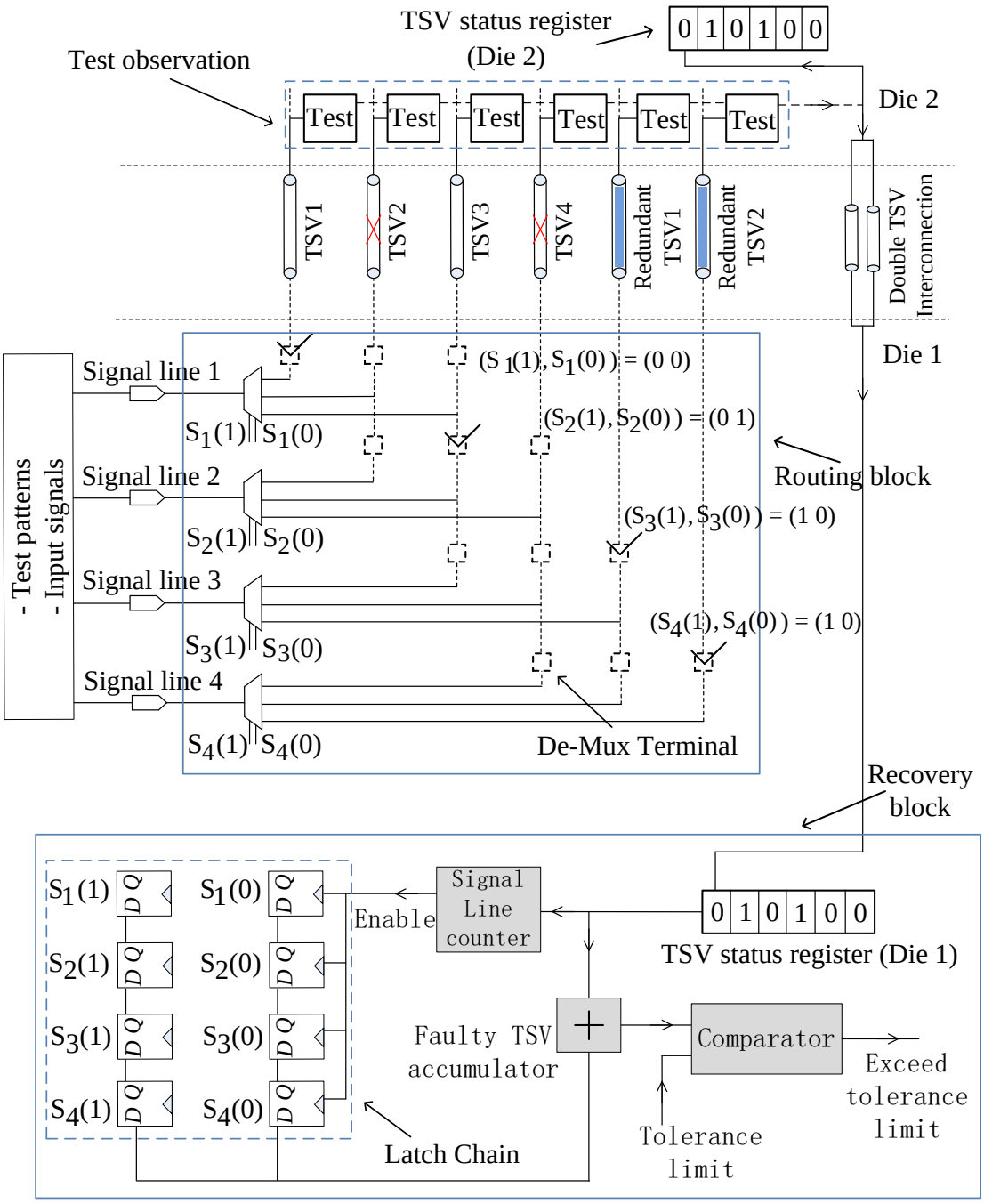


Figure 4.8(a): Reconfiguring a faulty design with a grouping ratio of 4:2

	TSV status register chain shift out	**Signal line counter**	**Enable (Latch chain)**	**Faulty TSV accumulate adder**	**Latch chain** $S_1(1), S_1(0)$ $S_2(1), S_2(0)$ $S_3(1), S_3(0)$ $S_4(1), S_4(0)$
Clock cycle 1	0	1	Yes	00	00 00 00 00
Clock cycle 2	1	1	No	01	00 00 00 00
Clock cycle 3	0	2	Yes	01	00 00 00 01
Clock cycle 4	1	2	No	10	00 00 00 01
Clock cycle 5	0	3	Yes	10	00 00 01 10
Clock cycle 6	0	4	Yes	10	00 01 10 10

Figure 4.8(b): Reconfiguring process per clock cycle

Figure 4.8(b) shows a reconfiguration process in detail (per clock cycle), when assuming a design with a grouping ratio of *4:2*, with two defective TSVs (TSV2 and TSV4). Reconfiguration process is initiated after the detection phase with '010100' as the initial value of TSV status register. In total, four signal lines have to be reconfigured by updating the latch chain, which holds the selection signals of all de-multiplexers. As can be seen, in the first clock cycle, the first shifted out value from the TSV status register is '0', which is sent to the faulty TSV accumulator and signal line counter. This means that the output of faulty TSV accumulator is '00' and the value of the signal line counter becomes '1', which means that the first signal line can use TSV1. Signal line counter asserts the enable signal, and the latch chain scans in new values for the first signal line from the faulty TSV accumulator. As shown in Figure 4.8(b), the status of logic values in the latch chain becomes '00' for all four latch pairs. In the second clock cycle, the shifted out logic value from TSV status register is '1', the

faulty TSV accumulator becomes '01' and the signal line counter value stays at '1' because Signal line 2 is not yet configured, and the enable signal is set to low, which keeps the latch chain at the same logic values as the previous clock cycle. As shown in Figure 4.8(b), signal line 2 is configured in the third clock cycle, when the shifted out value from TSV status register is '0', and the logic values in the latch chain becomes '00', '00', '00', '01'. The value of the signal line counter becomes 2, which means that 2 (out of four) signal lines have been configured. This process continues until all four signal lines are configured in the sixth clock cycle, and the latch chain holds '00', '01', '10', '10' in each of the four latch pairs. The resultant reconfiguration of signal lines is shown in Figure 4.8(a), where all defective TSVs are bypassed. In Section 4.4.3, functional validation of this design is also demonstrated using ModelSim.

Figure 4.9 shows the architecture of the proposed fault tolerance technique with a grouping ratio of m:n. As can be seen, each group contains m+n TSVs with m input/output signal lines. The TSV status register consists of m+n bits. Each signal line can have n+1 TSVs for communication, such that 1-to-(n+1) de-multiplexer is needed. Selection signal for signal line i will need $k=\lceil \log_2(n+1) \rceil$ bits, which are Si(0), Si(1), …, Si(k-1). Therefore, for each signal line the latch chain consists of k latches, which holds the de-multiplexer selection signal. The signal line counter generates m latch renew enable signals. The comparator is used to report if the number of faulty TSVs in a group exceeds the maximum tolerance limit.

Overall, for a grouping ratio of m:n, this technique requires m+n clock cycles to test m regular and n redundant TSVs serially and $m+n$ clock cycles for repairing all TSVs in the presence of defects. Therefore in total it requires only $2.(m+n)$ clock cycles for fault detection and recovery. Theoretical lower bound to test and repair all TSVs per design is 2 clock cycles, assuming an infrastructure to test and repair all TSV in parallel. The proposed technique approaches theoretical lower bound by using only $2.(m+n)$ clock cycles. The area overhead of the fault tolerance technique (detection, recovery and routing blocks on both dies) is:

$$
\begin{aligned}
Area = \; & A_{detection} + A_{routing} + A_{recovery} + A_{redundant\ \ TSV} \\
& = (m+n) \quad Nand\ gates \\
& + \{3(m+n) + 2m\lceil log_2(n+1)\rceil\} \quad FlipFlop \\
& + (m)\ demux_{1-to-(n+1)} + (m)\ mux_{(n+1)-to-1} \\
& + (2)\ signal\ line\ counter_{m-bit} + (2)\ accumulator \\
& + comparator + A_{redundant\ \ TSV}
\end{aligned} \tag{4.2}
$$

where, "A" denotes area overhead of a TSV group with a grouping ratio of *m:n*; all other notations have their usual meaning. It can be seen that this technique can be easily scaled to suit a generic design with any specified grouping ratio. Simulation results presented in Section 4.4.4 demonstrate how area overhead can be reduced without affecting fault tolerance and repair capability for various grouping ratios.

The wirelength overhead can be understood from Figure. 4.5, this increase is due to alternative route paths from signals to TSVs. For a general grouping ratio of m: n, one signal has *n*+1 possible route paths (*n* alternative routes). The lower bound of the wirelength overhead can be achieved based on an assumption that, within a group TSVs are located next to each other with a minimum pitch, denoted as d_{pitch}, and this is applicable to each group (Figure 4.5). Such that for *M* total number of signals (*M* regular TSVs) organized with grouping ratio of *m: n*, the wirelength overhead is:

$$M*(\sum_{i=1}^{n} i * d_{pitch}) \quad (4.3)$$

This wirelength overhead includes routing block, which dominates the wirelength overhead due to the TSV redundancy. The wirelength overhead due to recovery block is not included in this equation. Moreover, wirelength overhead is not a critical issue in the proposed technique, because in this work these wirelength increase are mainly due to the alternative routing paths for signals for bypassing defective TSVs. However, in practice, for each signal there is only one active route path during operation, which means that those alternative routing paths do not contribute to signal latency, as they may not be in use.

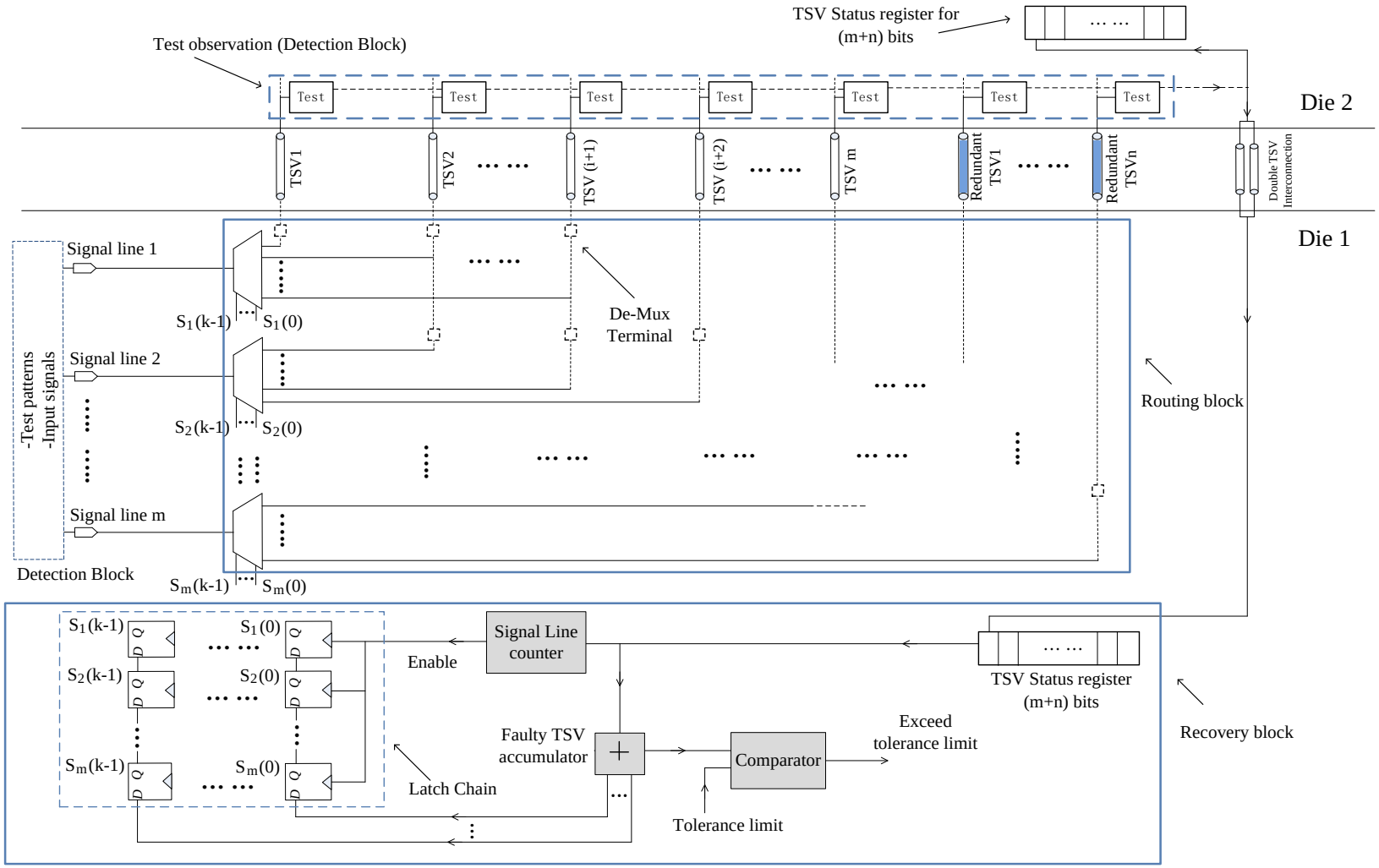


Figure 4.9: Architecture of fault tolerance technique with grouping ratio of *m:n*.

4.4 Simulation Results

In this section, firstly, a simulation flow of the proposed fault tolerance is presented in Section 4.4.1. Then, three sets of simulations are conducted to validate and evaluate the fault tolerance technique. The first set of simulation (Section 4.4.2) validates the detection block through HSPICE and characterizes detectable resistance range for three defects: void, delamination and short-to-substrate. The second set of simulation (Section 4.4.3) functionally validates the recovery block through RTL model implementation of fault tolerance technique using Modelsim. The last set of simulation (Section 4.4.4) analyses the trade-off between area overhead and repair capability of this technique through synthesis using Synopsys design compiler.

4.4.1 Proposed Fault Tolerance Technique Simulation Flow

All simulations are conducted on Intel Xeon Quad Core 2.7 GHz processor with 12 GB RAM. Figure 4.10 shows a simulation flow which undertakes both TSV defects detection and recovery. It takes three inputs for the detection validation (Figure 4.10), which are TSV defect models, logic threshold of the NAND gate in detection block (Figure 4.5), and test pattern generator. Three types of defects (Figure 4.1) are modeled by incorporating open resistor R_{open} and short resistor R_{short} (Figure 2.3). The logic threshold voltage L_{vth} is used as a criteria to detect the targeted three types of TSV defects using delay test method as described in Section 4.3.1. A test pattern generator (Figure 4.5) is used to provide rising transition for detection process. The detection is based on delay test which will simulate the TSV delay behavior using HSPICE. The HSPICE description for test circuits and TSV defect models are shown in Appendix A. By selecting the test clock frequency (Signal capture time, Section 4.3.1), critical open resistance $R_{open\text{-}critical}$ and critical short resistance $R_{short\text{-}critical}$ can be determined. Once the fault map is obtained, the simulation flow goes to fault recovery process, of which fault tolerance circuits are implemented using RTL models (Verilog Hardware Description Language) and the recovery process is mimicked using ModelSim simulation tool. RTL description of a group with grouping ration of 4:2 is shown in Appendix B. The simulation flow outputs a reconfiguration solution for the routing multiplexers in the group as demonstrated in Figure 4.8(a). Furthermore, the best grouping ratio for a design with specified number of total number of regular TSVs can also be addressed using the exhaustive search method described in Chapter 3.

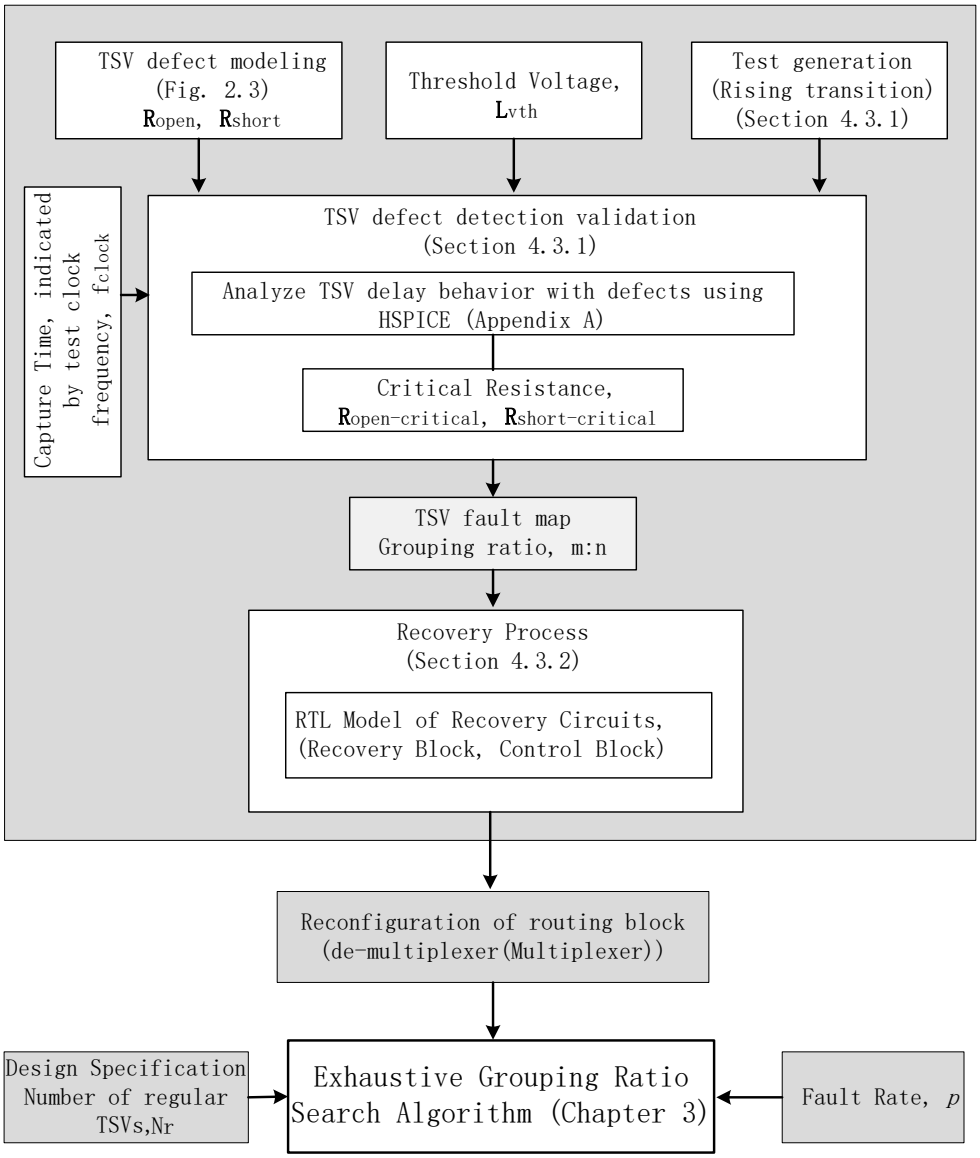


Figure 4.10: Simulation flow of the proposed fault tolerance technque.

4.4.2 Detection Block Validation

This simulation employs the electrical models of TSV and three defect types shown in Figure 4.1. The test circuit (Figure 4.5) is modelled with HSPICE using 65-nm ST Microelectronics gate library (see Appendix A for details). All simulations are carried out at 25°C and 1.2-V. For illustration, the defect free TSV resistance and capacitance is 200-mΩ and 200-pF respectively, as they represent typical values [37]. The test clock frequency is F_{clock} is 1.5 GHz. It was shown in [172] that when considering process variation with $\pm 3\sigma$ variation effects, logic threshold voltages of all gates (in a gate library) are within 20%-80% of V_{dd}. This means

that for a rising transition, logic-1 is guaranteed at V_{Out} > 80% of V_{dd}, similarly, logic-0 is guaranteed at V_{Out} < 20% of V_{dd}. Therefore, the rising (falling) transition delay is equal to the time taken for TSV voltage to rise (falls) from 20% (80%) to 80% (20%).

Table 4.1: Void or delamination defect characterization

Defect type	**R_{open}**	**Transition Delay T2 node (ns)**		**Classification**
		Rising	**Falling**	
Void/ Delamination	Defect free 0Ω	0.242	0.160	Faulty-free
	1kΩ	0.311	0.225	
	2kΩ	0.419	0.339	
	3kΩ	0.541	0.469	
	4kΩ	0.667	0.608	
	5kΩ	0.805	0.743	Faulty
	10kΩ	1.492	1.441	
	50kΩ	7.085	7.033	
	100kΩ	14.121	14.030	
	1MΩ	Stuck-open	Stuck-open	

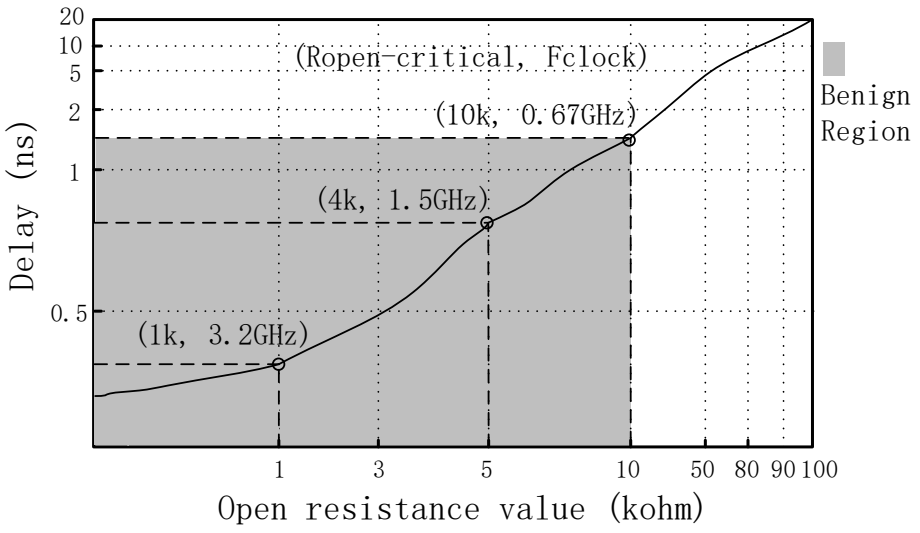


Figure 4.11: Delay (Rising) as a function of open resistance showing critical open resistances for three test clock frequencies: 0.67GHz, 1.5GHz, 3.2GHz.

Table 4.1 shows the simulation results when considering void or delamination defects. It shows the transition delay behaviour of open resistance due to void or delamination defects. R_{open} is in the range of [0, 1MΩ], where 0Ω is in case of fault-free TSV behaviour (with only TSV resistance of 200-mΩ) and 1MΩ represents full-open TSV defect, beyond which it can

be treated as a stuck-open fault. From Table 4.1, it can be seen that the rising (falling) transition delay increases from 0.242-ns (0.160-ns) to 14.12-ns (14.03-ns), when R_{open} of TSV increases from fault-free to 100-KΩ. Moreover, when R_{open} is 1-MΩ, it behaves as stuck-open fault. These results indicate that the detection block is capable of detecting void or delamination defects with R_{open} > 4-KΩ. This is because beyond this resistance value, the rising delay takes longer than $\frac{1}{1.5*10^9}$ = 0.67-ns to reach 80% of V_{dd} as shown in Table 4.1. This open resistance is referred as resistive open critical resistance ($R_{open\text{-}critical}$ is 4kΩ). Note that this value changes with F_{clock}. When testing resistive open defects, it is desirable to have lower $R_{open\text{-}critical}$, which is possible by using higher test clock frequencies. The relationship between test clock frequency and detectable defect size is well-studied [172, 173], it is quantized for Void/delamination TSV defects by considering three test frequencies. Figure 4.11 shows an analysis of test clock frequency and critical open resistance ($R_{open\text{-}critical}$) where delay (Rising) is depicted as a function of open resistance R_{open}. Test clock frequency is set to be 0.67GHz, 1.5GHz, and 3.2GHz, and the critical open resistance value are 10kΩ, 4kΩ, and 1kΩ respectively. The shaded areas denote benign regions with respective test clock frequencies, and as expected, higher test clock frequency allows for higher detectable range.

Table 4.2: Short-to-substrate defect characterization

Short to substrate defect type R_{short}	**Rising transition delay (ns)**	**Voltage level at TSV end (V)**	**Classification**
0Ω	Stuck-open	0	Faulty
500Ω	Stuck-open	0.38	
900Ω	Stuck-open	0.60	
1kΩ	0.758	0.64	
2kΩ	0.665	0.87	Faulty-free
3kΩ	0.551	0.97	
4kΩ	0.379	1.03	
5kΩ	0.336	1.06	
10kΩ	0.279	1.13	
100kΩ	0.245	1.19	
1MΩ	0.242	1.19	

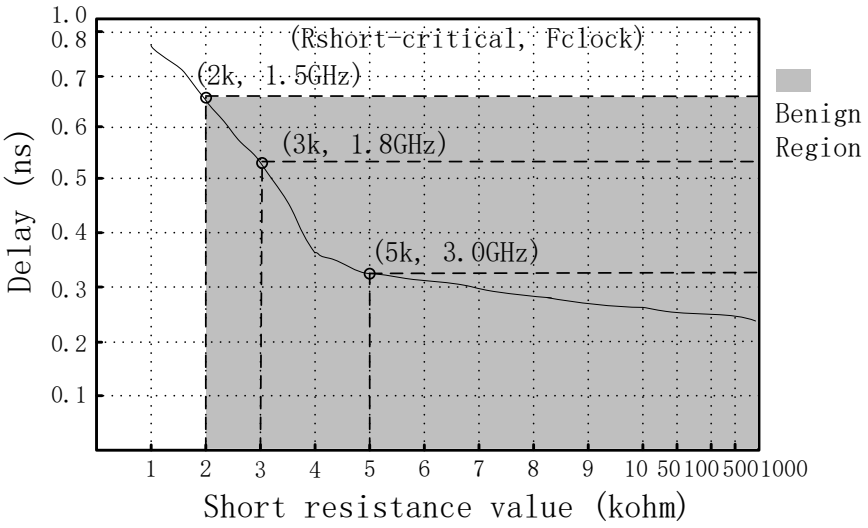


Figure 4.12: Delay (Rising) as a function of short-to-substrate resistance showing critical resistances for three test clock frequencies: 1.5GHz, 1.8GHz, 3.0GHz.

Table 4.2 shows simulation results when considering short-to-substrate defect. It shows the rising transition delay, along with degraded TSV voltage due to short-to-substrate defect, referred as R_{short}. It can be seen that the delay increases from 0.242-ns when R_{short} is 1-MΩ and it behaves as stuck-open defect for resistance value ≤ 900-Ω. When comparing Table 4.1 and Table 4.2, it can be observed that R_{short} of 1-MΩ has about the same delay as that of fault-free TSV. It can be seen from Table 4.2 that for test clock frequency of 1.5GHz, TSV with R_{short} < 2KΩ are detectable and referred as critical short resistance ($R_{short\text{-}critical}$ is 2KΩ). When the resistance value is smaller than 900Ω, the degradation of TSV voltage is more than 50% of the supply voltage 0.6V (V_{dd}=1.2V), which is regarded as stuck-open defect. Figure 4.12 shows the critical resistance relationship between short-to-substrate defect and test clock frequency. The delay (Rising) is depicted as a function of R_{short}. Test clock frequency is set to 1.5GHz, 1.8GHz, and 3GHz (for illustration), which leads to $R_{short\text{-}critical}$ of 2kΩ, 3kΩ, and 5kΩ respectively. It can be observed that the delay increment is faster when short-to-substrate resistance is smaller. This is due to higher leakage current with bigger defect size (i.e., smaller R_{short}), which leads to smaller TSV charging current.

4.4.3 Recovery Block Validation

This set of simulation is used to functionally validate the recovery block and reconfiguration process of the proposed technique (Section 4.3.2) using ModelSim. For illustration, the reconfiguring process is simulated for a group with grouping ratio of 4:2 (four regular and two redundant TSVs), for the schematic shown in Figure 4.8(a), with two defective TSVs (TSV2 and TSV4) as shown by the contents of TSV status register. RTL description using Verilog description language of the recovery block is detailed in Appendix B. The grouping ratio and locations of faulty TSV are selected for ease of process (per clock cycle) shown in Figure 4.8(b). Figure 4.13 shows simulation results for every clock cycle, the initial status of

TSV status register is ‘010100’. From simulation results, it can be observed that after first clock cycle, the first value of TSV status register is shifted out and the TSV_status (TSV status register) becomes ‘101000’, which initiates the reconfiguration process. Signal_line_counter (Figure 4.9) indicates the number of signal lines that have been configured and after six clock cycles, all four signal lines are configured with its value equal to ‘4’. As expected, each time “enable (Latch chain)” signal is asserted, the latch chain scans in the output of faulty TSV accumulate adder and after six clock cycles the latch chain holds the selection signals for all de-multiplexers, which are $S_1(1)$, $S_1(0) = (0,0)$; $S_2(1)$, $S_2(0) = (0,1)$; $S_3(1)$, $S_3(0) = (1,0)$; and $S_4(1)$, $S_4(0) = (1,0)$. When comparing these with expected results shown in Figure 4.8(b), it can be observed that the signal lines are correctly configured.

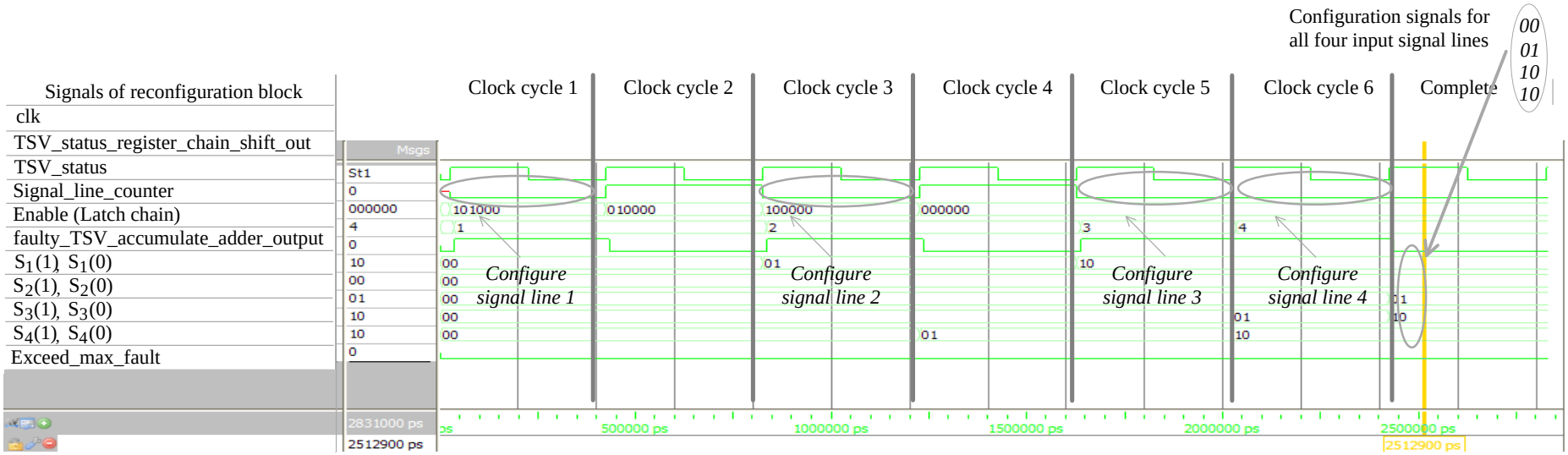


Figure 4.13: ModelSim functional validation of recovery block and reconfiguration process.

4.4.4 Repair Capability and Area Overhead

Table 4.3: Trade-off between repair capability and area overhead (regular TSV number is 6000, fault rate is 0.01).

Redundancy percentage	Grouping ratio	Total redundant TSVs	Area overhead per die (um^2)	Repair capability (%)
100%	1:1	6,000	73,350	55
	2:2		84,300	99
	3:3		85,993	100
50%	2:1	3,000	57,525	41
	4:2		66,088	97
	6:3		67,252	100
25%	12:3	1,500	48,069	99
	16:4		57,554	100
10%	40:4	600	52,287	99
	50:5		**56,235**	**100**
5%	100:5	300	54,301	96
	120:6		58,302	99

This simulation aims to evaluate the area overhead and repair capability of the fault tolerance technique. As mentioned in Section 4.3, grouping ratios are fixed during design time. This simulation shows that an optimal grouping ratio can be selected to achieve the target repair capability while using minimal area. For illustration, regular TSV number used in this simulation is 6000. Area overhead of the proposed technique is computed through synthesis using the Synopsys Design Compiler and STMicroelectronics 130-nm gate library. The diameter of a TSV is 5-um [62], such that for each redundant TSV, the area overhead is 25 um^2. The second last column of Table 4.3 shows the overall area overhead per die, which is the sum of redundant TSVs, detection, recovery and routing blocks. This can also be estimated using Eq. (4.2) (Section 4.3.2). For a given fault rate of 0.01, repair capability of different grouping ratios is calculated using the method described in Chapter 3 Section 3.3.1 (for independent TSV defect distribution), and results are shown in the last column. It can be seen (Table 4.3) that for 100% redundancy percentage, grouping ratios are varied (from 1:1 to 3:3) until 100% repair capability is found. As can be seen, the repair capability is 100% for a grouping ratio of 3:3, but the area overhead increases with grouping ratios (2:2, 3:3) for a given redundancy percentage (100%). This is because of more complex control and routing block (Figure 4.3). To reduce hardware overhead, the method reduces redundancy percentage. In the case of 50% redundancy percentage, the grouping ratio of 6:3 achieves lower area overhead (than 3:3) while achieving 100% repair capability. For 25% redundancy percentage,

grouping ratio of 16:4 achieves 100% repair capability but uses higher area than 6:3. Overall, the best grouping ratio, which achieves the lowest area overhead with 100% repair capability, is 50:5, as in the case of 10% redundancy percentage. This clearly shows that for a given fault rate, area overhead can be reduced while achieving 100% repair capability by carefully selecting the grouping ratio.

Table 4.5: Comparison between the proposed technique and [104, 121, 135, 151] (regular TSV number 1000).

Technique		Proposed technique	TSV repairing [135, 131]	Test method	
				[104]	[121]
Objective		Detection (open and short to substrate defect) and Repairing	Repairing	Detection (short to substrate)	Detection (open)
Cost	No. redundant TSV	25 (grouping ratio 80:2)	128	N/A	N/A
	Routing	1000 Mux	3000 Mux	N/A	N/A
	Recovery	13*Signal line counter +13*Faulty TSV adder +13*comp+3025*FF	On-chip microprocessor + Router configuration block	N/A	N/A
	Detection (testing logic)	1025*Nand + 1025*FF	On-chip test block	1k*voltage comp + 2k*INV+ 1k*FF+ 2k*Mux	1k*voltage comp + 1k*INV+ 1k*FF+ 1k*Mux

The cost-effectiveness of the grouping based fault tolerance technique is evaluated with five benchmark circuits from IWLS 2005 [174]. Table 4.4 shows the results in terms of hardware cost of the proposed technique on the benchmark circuits. Area overhead of the proposed technique is achieved from both calculation using Eq. (4.2) (Calculation results in Table 4.4) and synthesis using STMicroelectronics 130-nm gate library (Synthesis results, Table 4.4). The diameter of a TSV is 5-um [94], such that for each redundant TSV, the area overhead is 25 um^2. Regular TSV number for each design is obtained from [44] where the selected circuits are synthesised under130-nm Cell library as well. For design with a given number of regular TSVs, the best grouping ratio can be found through an exhaustive search method in Chapter 3 with the objective of minimizing area overhead without affecting the target repair capability, as shown in the fourth column in Table 4.4. Cost of each block in the proposed fault tolerance technique is shown individually for calculation results. The overall area overhead results (last column Overall percentage) indicate that the area overhead of the proposed technique can be 3.34% for the best case (circuit *netcard*). Notice that this amount

of area overhead is sacrificed for 100% repair capability and the fault rate of TSV is assumed to be 0.001 for illustration purpose.

The comparison with recent reported techniques [104, 121, 135, 151] is shown in Table 4.5. For illustration purpose, a design with regular TSV number 1000 is assumed. In [104, 121] test mechanisms for detecting open TSV defects and short-to-substrate defects are reported. As can be seen, the proposed structure has a lower area overhead for detection logic when compared with the one reported in [104, 121]. The ideas presented in [135, 151] utilise an on-chip microprocessor to implement control logic for repairing. The proposed work is the first to show detailed hardware solution for designs, where such an on-chip microprocessor is either not employed or cannot be used for TSV repairing.

Table 4.4: Benchmark circuits incorporating the proposed fault tolerance technique (TSV failure rate 0.001)

Circuits	Design area (um^2)	regular TSV (signal TSV)	best grouping ratio (Chapter 3)	No. of Spare TSV	Area Overhead per die (calculation) /um^2							Synthesis results / um^2	
					Spare TSV area	Double-TSV structure	Detection	Recovery	Routing	Total (calculation)	Overall percentage	Total (synthesis)	Overall percentage (synthesis)
aes_core	818,750	1,362	80:2	34	850	850	16,857	81,832	28,874	129,264	15.79%	143,007	17.4%
ethernet	2,858,975	3,782	80:2	94	2,350	2,350	46,809	227,232	80,178	358,920	12.55%	397,080	13.8%
des_perf	3,428,571	3,678	80:2	92	2,300	2,300	45,522	220,983	77,974	349,079	10.18%	386,190	11.2%
vga_lcd	4,400,000	7,356	240:3	93	2,325	1,550	89,934	408,738	252,311	754,857	17.16%	828,748	18.8%
netcard	28,034,722	9112	240:3	114	2,850	1,900	111,403	506,310	312,542	935,005	3.34%	1,133,868	4.0%

4.5 Concluding Remarks

This chapter has presented a cost-effective and efficient online fault tolerance technique, with detailed validation and evaluation of fault detection and recovery for improving the in-field reliability of TSV based 3D IC design. Three important latent TSV defect types have been considered: void, delamination and TSV short-to-substrate. Fault detection is carried out using (detection block) transition delay test. Fault recovery is carried out using redundant TSVs and rerouting input/output signals to fault-free TSVs. It is efficient because it requires only $2(m+n)$ clock cycles for fault detection and recovery for a design with m regular and n redundant TSVs in a group. The proposed technique is implemented on a 130-nm design library. Detailed electrical and logical simulations are carried out to validate the working of detection and recovery blocks. It is shown that the area overhead can be reduced without affecting repair capability through appropriate grouping of regular and redundant TSVs.

Comparing to the work presented in Chapter 3 which is dedicated for improve the yield of 3D-ICs. This Chapter extend the grouping based TSV technique in Chapter 3, to let it become capable of tolerating manufacturing defects and thermal-induced latent defects. Thus, both yield and reliability are targeted. Moreover, the fault tolerance technique in this Chapter incorporated the online TSV defect detection as well.

Chapter 5

Joint Consideration of Fault Tolerance and Temperature Mitigation for 3D-ICs

TSV failures due to manufacturing defects and thermal-induced latent defects result in yield and reliability issues in 3D-ICs. Meanwhile, thermal issue are acknowledged to be a growing concern in 3D integration. Chapter 4 has proposed a fault tolerance technique that can address three types of TSV defects which are thermal relevant as discussed in Chapter 2 Section 2.2. Recent work has shown different temperature mitigation techniques and it is well known that TSVs are effective in reducing temperature by providing thermal conductivity. To the best of our knowledge this is the first work that jointly considers temperature mitigation and fault tolerance for TSV based 3D ICs without introducing additional redundant TSVs. This is achieved by reusing spare TSVs that are frequently deployed for improving yield and reliability in 3D ICs. The spare TSVs are placed in such a way that temperature is reduced without affecting fault tolerance capability. The proposed technique consists of two steps: First is TSV determination step, which provides optimised allocation of regular and spare TSVs in groups to achieve expected repair capability. Second step is TSV placement, where temperature mitigation is targeted while optimizing routing difference and total wirelength. Simulation results show that using the proposed technique, 100% repair capability is achieved across all (five) benchmarks with an average temperature reduction of 34.1% (best case is 58.5%), while increasing wirelength and route difference by a small amount.

The publication related to this chapter is listed in Chapter 1 Section 1.5 (Publication 3) and its corresponding key contributions are:

- A fault tolerance technique that combines tolerating TSV failures either due to manufacturing defects or latent defects and relieving the thermal problem of 3D circuits.
- An efficient grouping ratio searching algorithm to obtain optimal grouping ratio under target repair capability with minimized hardware cost.
- Enhanced thermal-aware TSV placement strategy with objective of co-optimizing between temperature, wirelength, and routing difference.

5.1 Introduction

Recent research has shown that TSV failures occur either due to manufacturing or latent defects leading to yield and reliability issues respectively [51, 91]. These issues are frequently addressed by fault tolerance architectures with spare TSVs [117, 131, 151, 160]. Reference [117, 131] utilize redundant TSVs in a TSV block for improving yield by repairing defective TSVs. The work presented in Chapter 3 employs redundant TSVs (as in [117, 131]) and partitions multiple regular and redundant TSVs into groups according to a specified grouping ratio, where redundant TSVs are used to repair (bypass) defective TSVs in that group, which is used to optimize yield and reduce hardware overhead. Reference [151] targets improving in-field TSV reliability by using an on-chip processor for online fault detection and recovery.

Thermal issues are important as they cause performance degradation and TSV defects (for example, void growth and delamination between TSV and its landing pad) [86, 114]. Therefore, it is important to maintain temperature during normal operation of design. An indirect way often employed to reduce overall chip temperature at a physical design stage is thermal-aware floorplanning/placement strategy [146, 147, 149]. With the reported floorplanning/placement methods, the overall chip temperature can be reduced. However, new and innovative methods are needed for further temperature reduction [175]. To reduce temperature further, reference [149, 176] use dummy vias (TSVs) which serve as additional thermal dissipation tunnels. However, these dummy vias which are high cost in terms of chip area cannot be reused when regular TSVs suffer from either manufacturing or latent defects. This chapter proposes joint consideration of fault tolerance and temperature mitigation by reusing spare TSVs that are otherwise used only for tolerating TSV failures (due to manufacturing or latent defects). This is the first work, which utilises redundant TSVs for temperature mitigation and this chapter presents the following contributions:

1. The proposed fault tolerance technique makes dual use of the redundant TSVs by carefully allocating and placing spare TSVs in two steps. First is TSV determination step in which redundant TSVs are allocated to optimize hardware cost for a given (targeted) repair capability. The second step is TSV placement step, in which TSVs are carefully placed for reducing chip temperature.

2. The proposed technique is cost-effective, because in the TSV determination step, an efficient algorithm is employed to achieve targeted reparability with minimized hardware overhead.

3. The second step (TSV placement) is based on a simulated-annealing algorithm, which is used for optimizing temperature, route difference, and total wirelength, where route difference takes into account the additional routing overhead due to transferring signals from regular to spare TSV as in the case of bypassing a defective TSV.

The rest of this chapter is organized as follows: Section 5.2 describes the proposed TSV fault tolerance technique Simulation results are presented in Section 5.3 and Section 5.4 concludes this chapter.

5.2 Proposed TSV Fault Tolerance Technique

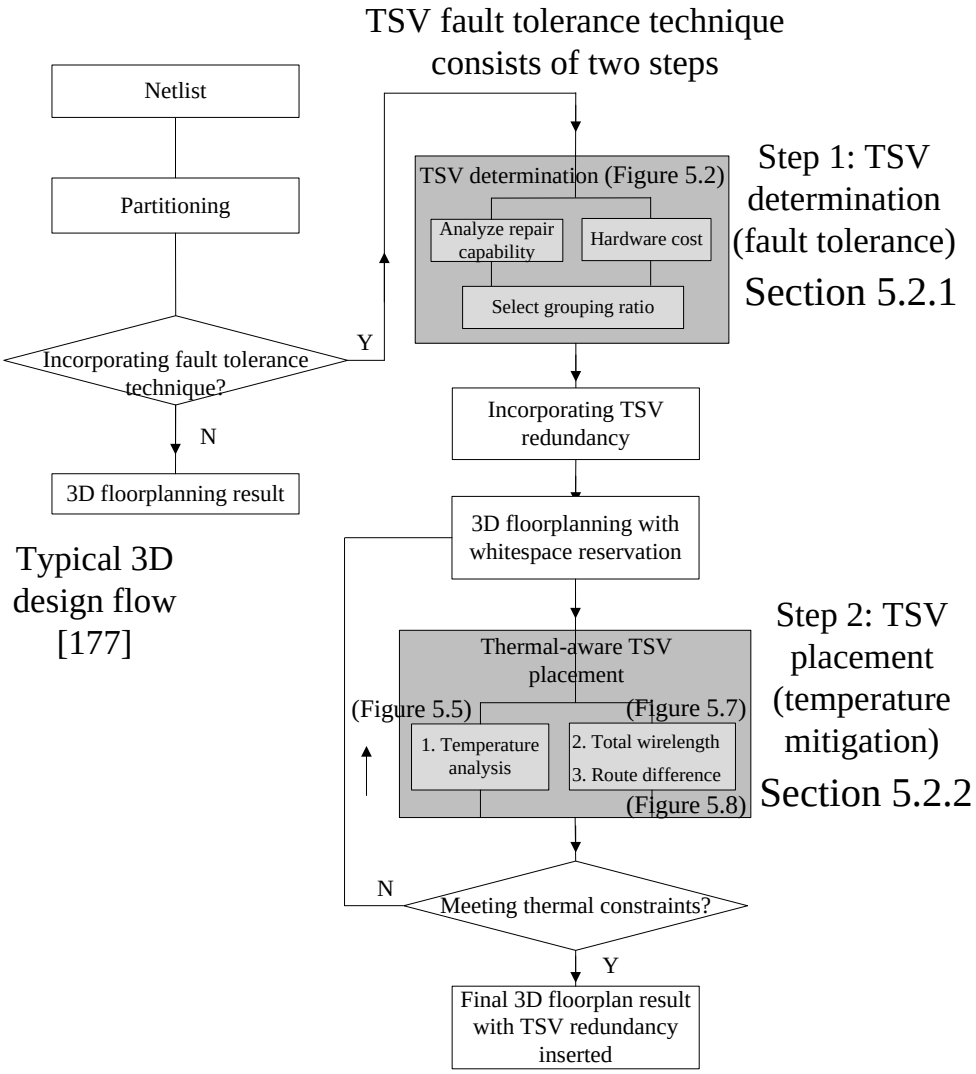


Figure. 5.1: Proposed technique with joint consideration for fault tolerance and temperature mitigation

Figure 5.1 shows the flow of the proposed fault tolerance technique with joint consideration of tolerating TSV faults and temperature mitigation. The joint consideration is achieved through two steps which are the TSV determination step (Section 5.2.1) and the TSV placement step (Section 5.2.2, shaded boxes in Figure 5.1). Recent research has shown partitioning mechanism to determine the number of signal TSVs [178, 179, 180] and cell placement [42, 146, 181] for each layer of a 3D design. TSV determination step aims to provide optimal balance between target repair capability and the hardware cost by finding the best grouping ratio between signal (regular) and spare TSVs. This is determined through a

robust algorithm described in Section 5.2.1. Then, logic blocks are placed using existing 3D floorplanning mechanism where whitespace is reserved for TSV placement [181]. Next step is TSV placement, where TSVs (regular and spare) are placed through an iterative process to optimise temperature, wirelength, and route difference. Finally, a floorplan of a design with dedicated TSV redundancy structure is obtained. As expected, this technique can cope with both fault tolerance (Step 1, Figure 5.1), and temperature mitigation (Step 2, Figure 5.1).

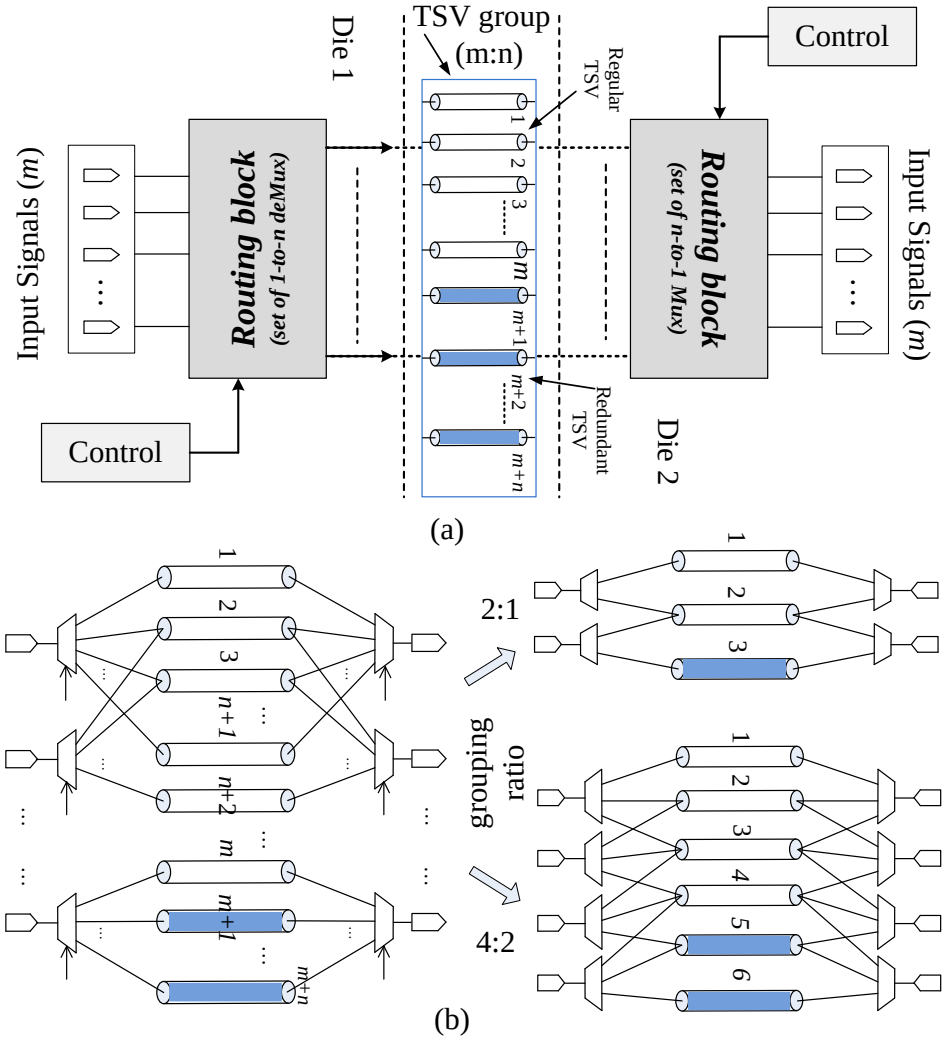


Figure. 5.2: TSV redundancy architecture (grouping ratio): (a) Block diagram of a group (b) Illustration of configuration for two grouping ratios.

5.2.1 TSV Determination Step

The proposed fault tolerance technique uses the concept of grouping ratio described in Chapter 3, which allocates multiple regular and spare TSVs into groups according to a grouping ratio. Such that signals within a group can select defect free TSVs to replace faulty ones. Figure 5.2 (a) shows the architecture of the grouping based TSV fault tolerance structure (of one TSV group) with grouping ratio of *m: n*, which comprises of *m* input (output) signals, *m* signal (regular) TSVs and *n* spare TSVs. It consists of two blocks: routing block

and control block. Routing block can be configured by control block to reroute signals bypassing defective TSVs during operation, thus this architecture can be used to repair a group of TSVs in case of *n* defective TSVs, see Chapter 4 for details. The routing block can be implemented by a set of 1-to-(n+1) de-Multiplexers (n+1-to-1 Multiplexer) for input (output) signals to select fault free TSVs (Figure 5.2(b)). Clearly, the control block generates $k=\lceil \log_2(n+1) \rceil$ bits for each de-Multiplexer (Multiplexer) associated to one signal for selecting *n+1* TSVs. The hardware cost of routing and control blocks can be compared in terms of length of control signals and number of routing de-multiplexers (multiplexers). For a general grouping ratio of *m*:*n*, the cost is:

*2m*k* bits selection signals + [m*(1-to-n+1)] deMux+ [*m** (n+1-to-1)] Mux (5.1)

To calculate the repair capability for a group with a given grouping ratio of *m*: *n*, where *m* and *n* is the regular and spare TSV number in a group. Assuming that each TSV within a group is independent and has a uniform failure rate *p*, then the probability of having *x* defective TSVs is expressed as:

$$P(X = x) = C_{m+n}^{x} \cdot p^{x} \cdot (1-p)^{(m+n-x)} \quad (5.2)$$

where C_{m+n}^{x} is a combination of *x* and (*m*+*n*) which shows all possible situations of having *x* defective TSVs in a group of (*m*+*n*) TSVs. Clearly if the defective TSV number in a group is smaller than the spare TSVs number *n*, such group can be repaired. The overall reparability of the design *R* is $(R_{group})^{gn}$ [160], where R_{group} and *gn* denote repair capability of one group and total group number in a design respectively. R_{group} can be expressed as [160]:

$$R_{group} = \sum_{x=0}^{n} \left[C_{m+n}^{x} \cdot p^{x} \cdot (1-p)^{(m+n)-x} \right] \quad (5.3)$$

The trade-off between repair capability and hardware cost is illustrated in Figure 5.2(b) where eight regular TSVs with 50% redundancy percentage are organized in grouping ratio of 2:1, and 4:2. It is obvious that 4:2 shows a higher repair capability, however, it results in higher hardware cost (8, two-bit control signals; 8, 1-to-3 deMux; 8, 3-to-1 Mux). In this chapter, an robust algorithm is proposed to analyse the repair capability and hardware cost for a design with different allocation of spare TSVs to regular ones (grouping ratio) and then select the best grouping ratio to optimize the target reparability and hardware cost. The proposed best grouping ratio search algorithm is shown in Figure 5.3. The algorithm is more efficient than the exhaustive search algorithm described in Section 3.3.3, Chapter 3. It is more efficient because it employs binary search algorithm (Step 4, Figure 5.3). Parameter λ is the coefficient for reducing TSV redundancy percentage and is set to be 0.5 in this work. Note, that the hardware cost is composed of two parts, one is circuits for bypassing defective TSVs (routing de-multiplexers (multiplexers) and control signals, Eq. (5.1)) while the other is the total spare TSVs. When addressing the optimization of hardware cost it is able to let the user decide which one has higher priority (Step 9, Figure 5.3).

Algorithm Robust search for best grouping ratio

Input: Regular TSV number *m*, TSV faulty rate *p*, pre-set target reparability R_{target}

Output: *best grouping ratio*

1 Start from initial redundancy percentage Rd= 100%
2 **For** grouping ratios$\in Rd$ do
  Analyse the repair capability R
  Calculate the hardware cost
3 **If** $R>R_{target}$
4 Change the reduced redundancy percentage $Rd=\lambda*Rd$
  best grouping ratio =current grouping ratio
  break
  end for
5 **For** grouping ratio with the same spare TSV number as *best grouping ratio*$\in$new Rd **do**
  Analyse the repair capability R
  Calculate the hardware cost
6 **If** $R>R_{target}$
7 Jump to step 4
8 **else**
9 **If** user decide to sacrifice TSV cost for less routing hardware cost found *best grouping ratio*
10 **else** sacrifice routing hardware cost for TSV reduction
  Set the best grouping ratio to be the first one achieving target repair in this redundancy percentage
11 **Return** *best grouping ratio*

Figure 5.3: TSV determination algorithm for searching the best grouping ratio to provide required (100%) repair capability for given fault rate.

5.2.2 TSV Placement Step

Algorithm Proposed SA-based TSV placement algorithm

Input: flooplan with cells position and whitespace detail
Output: best *TSV placement best_Placement*

1 Build an initial TSV placement
2 Set an initial annealing temperature T_{anneal}
3 **While** $T_{anneal} > \varepsilon$ do //when not frozen
4 **for** I = 1 to k do //*k* iterations in every internal annealing
5 Pertub the TSV placement from current *Placement* to *Placement´*
6 Update cost function *Cost*(*Placement´*)
7 ΔC= *Cost*(*Placement´*)- *Cost*(*Placement*)
8 **if** $\Delta C <= 0$ then // Accept move
9 *Placement* = *Placement´*
10 **elseIf** random pending number < $e^{-\Delta C/T_{anneal}}$
// Pending rejection, accept with probability of $e^{-\Delta C/T_{anneal}}$
Placement = *Placement´*
11 **end if**
12 **If** *Cost*(*best_Placement*) > *Cost*(*Placement*)
13 *best_Placement* = *Placement*
14 **end if**
15 **end for**
16 $T_{anneal} = \eta T_{anneal}$ // Reduce annealing temperature
17 **end while**
10 **Return** *best_Placement*

Figure 5.4: Proposed simulated-annealing based TSV placement algorithm.

In this step, it is assumed that cells and macros are firstly placed and whitespaces are reserved for TSVs using the existing 3D floorplanning methods [42, 146, 181]. Note, that the placement of cells can be either wirelength-driven [181] or thermal-driven [146] along with the subsequent TSV placement procedure. A TSV placement algorithm is used to optimize between multiple objectives including temperature, wirelength, and route difference. The algorithm is based on the simulated-annealing approach to perturb one TSV placement to another TSV placement. The final TSV placement result is determined by the following cost function:

$$Cost = \alpha*T + \beta*WL + \gamma*(route\text{-}D) \quad (5.4)$$

where, T is the chip peak temperature, WL is the total wirelength, and *route*-D is the overall route difference. α, β, and γ are user specified coefficients which are used to control weights of these three parameters. Simulated-annealing based TSV placement algorithm is shown in

Figure 5.4, where cost of each TSV placement is analysed by Eq. (5.4) (Step 6). Parameter η indicates the speeding of temperature annealing and higher η gives better annealing quality by analysing more TSV placement perturbations. The following section will demonstrate how these three cost factors in the simulated-annealing algorithm can be obtained for a specified TSV placement.

5.2.2.1 Temperature Analysis

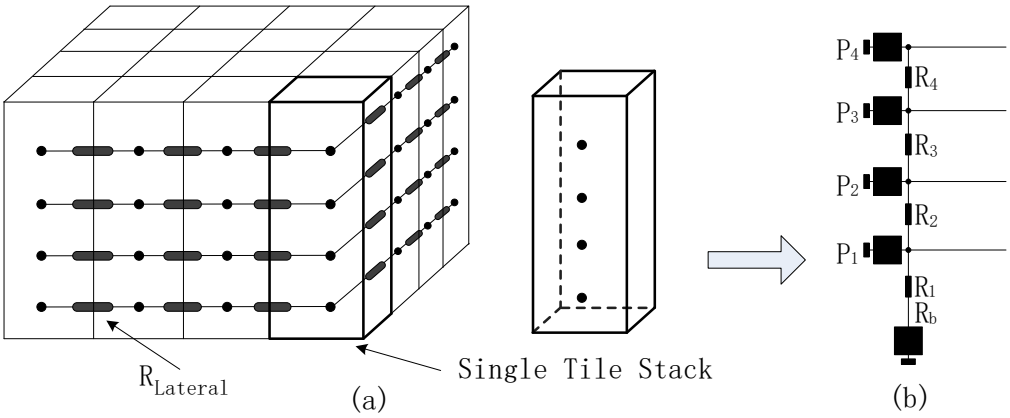


Figure 5.5: Resistive thermal model for 3D-ICs [146].

To estimate the temperature profile and the TSV impact on thermal dissipation, the thermal resistive model presented in [146] is employed. In the thermal resistive model, chip is divided into tile columns, where a single tile is composed of vertical stacked tiles from each layer (Figure 5.5(a)). Figure 5.5 (a) shows a 4×4×4 chip partitioning for illustration purpose. However, in this work, 32×32 partitioning strategy is used as recommended in [182]. For each tile column, thermal resistance of each tile is calculated, such that the column can be modelled as a resistive chain as shown in Figure 5.5 (b), where R_i denotes thermal resistor of the tile at the *i*-th device layer and the thermal resistance of the bottom layer (silicon substrate) is modelled as R_b. The power density of each tile (P_i) can be treated as a current source, which is an assumption of total power of each tile and is set to be between 10^5 (w/m^2) and 10^7 (w/m^2) using information from [149]. The influence of adjacent tiles in the same layer is modelled as lateral resistor connected between tiles, denoted as $R_{lateral}$. It is known that vertical heat dissipation dominates the overall temperature; therefore the impact of $R_{lateral}$ can be ignored [183]. Since power density is regarded as current source, temperature of each tile can be represented by the node voltage. Thus, the maximum chip temperature *T* can be written in an Elmore-Delay like closed-form formula as [149]:

$$T = \sum_{i=1}^{k}(R_i \sum_{j=i}^{k} P_j) + R_b \sum_{i=1}^{k} P_i \qquad (5.5)$$

where, R_b is fixed resistance decided by the device material. However, the effective tile thermal resistance R_i is determined by device material and TSVs, which contains TSV material specification from the fabrication process. In this work, these material-specified

parameters are taken from reference [146] for illustration. It is obvious that, if more TSVs are within one tile, the thermal resistance of tile R_i will be decreased since it can be modelled as a parallel connection between R_{eff} (effective thermal resistance of a tile without TSVs which is determined by the material property and tile size) and multiple TSV thermal resistance R_{TSV}. Using Eq. (5.5), it is able to obtain the temperature of each tile column and the highest temperature is regarded as the total temperature of the chip.

In microelectronic design, high temperature may cause delay faults. This is illustrated in Figure 5.6, where TSV delay is analysed using the T-model [121] (for TSV equivalent circuit, see Figure 2.3(b)) and SPICE simulation. It is found that TSV delay increases with temperature and this increase becomes much worse when TSV contains void or delamination defects, which can be modelled as open resistive defects leading to TSV resistance increment [121]. Therefore, it is important to maintain temperature.

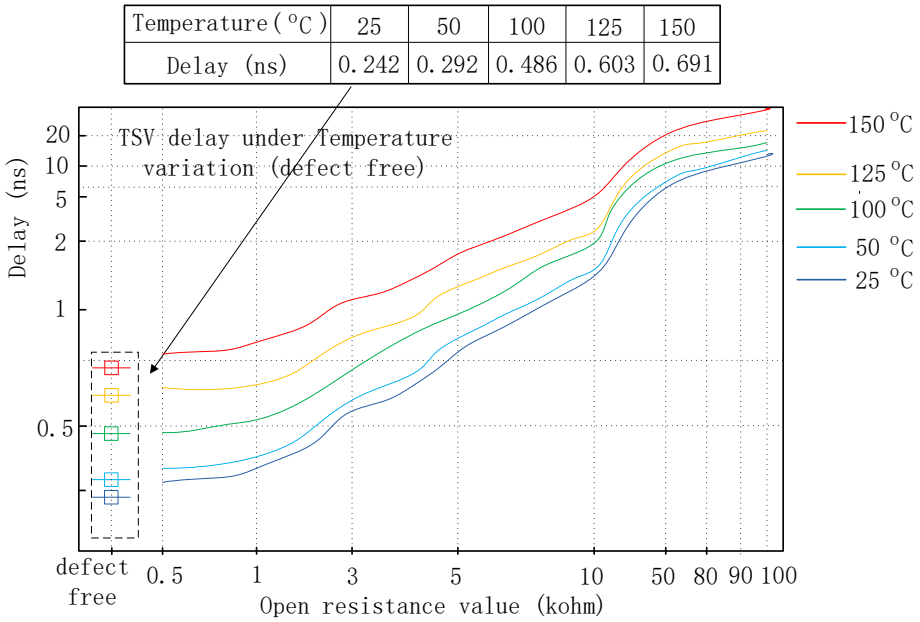


Figure 5.6: Illustration of TSV delay under temperature variation and resistive open defect.

5.2.2.2 Wirelength Calculation

Redundant TSVs introduce spare routing paths between signals and TSVs. The spare routing path acts as an alternative route path when signals have to switch from one TSV to another due to defective TSV. For a design with both regular and redundant TSVs, the total wirelength is composed of two parts: default routing wirelength and spare route wirelength, as illustrated in Figure 5.7(a). It shows a TSV placement case for a TSV group with grouping ratio of 2:1 (two regular and one spare TSV). Signal net A is connected to TSV1 using its default route path and to TSV2 using the spare route path. Signal net B is connected to TSV2 and Re_TSV1 using a default route path and a spare path as well. The default route wirelength is found by adding both default route paths of signal A and B, which are (2+TSV_height) and

(2+TSV_height) respectively (Figure 5.7(a)). The 3D wirelength is measured based on the half-perimeter-wirelength (HPWL) metric used in 2D design [24]. A 3D bounding box is used for wirelength estimation which takes both signal pin positions and TSV height into consideration (Figure 5.7(a), grey box). The spare route wirelength is calculated as follows: in case TSV1 is defective, signal A is rerouted to TSV2 leading to spare route wirelength of 4+TSV_height (Figure 5.7(a)). Similarly, when TSV2 is defective, spare route wirelength for signal B is 2+TSV_height (Figure 5.7(a)). Therefore, the total wirelength for this placement case takes both default and spare route wirelength into account which is 10+3TSV_height (Figure 5.7(a)).

Algorithm Route difference calculation

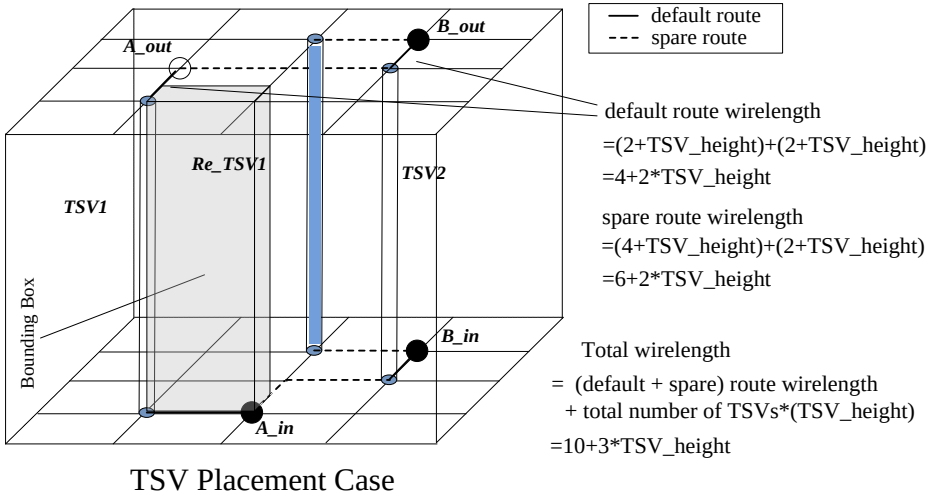
Input: TSV placement detail, grouping ratio m: n
Output: Average route difference avg_route_difference
// Overall route difference of a given TSV placement

1 Initial route_difference_sum =0; avg_route_difference =0
2 Calculate the default route wirelength default_WL
3 find out all possible bypassing situations BP*1* ~ BP*k* , k= $\sum_{x=1}^{n} C_{m+n}^{x}$
4 **for** BP*i* = BP*1* to BP*k* **do**
5 Calculate the probability of the bypassing situation BP*i* , P*i*(N)
// N is the defective TSV number of such bypassing situation,
where P*i*(N) can be obtained using Eq. (5.2)
6 Calculate the alternative route wirelength for bypassing situation BP*i*, alternative_WL*i*
7 Calculate route difference of the bypassing situation BP*i*, route_difference*i*
route_difference*i* = P*i*(N) * (alternative_WL*i* - default_WL)
8 Sum up the route difference
route_difference_sum = route_difference_sum + route_difference*i*
9 **endfor**
10 Obtain the average route difference for all bypassing situations

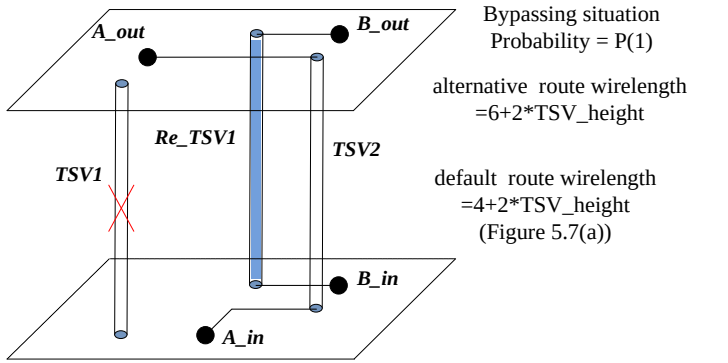
$$\text{avg\_route\_difference} = \frac{\text{route difference\_sum}}{P1(N)+P2(N)+\cdots\cdots Pk(N)}$$

11 **Return** avg_route_difference

Figure 5.8: Route difference calculation algorithm.



(a) Total wirelength calculation



(b) Illustration of calculation of route difference of a bypassing situation

Figure 5.7: Illustration of calculation method of wirelength and route difference for a given TSV placement,
(a) Wirelength calculation, (b)Route difference for a bypassing situation

5.2.2.3 Route Difference Calculation

To obtain the overall route difference for a given TSV placement case, a calculation algorithm is proposed in Figure 5.8. The algorithm starts from finding out all possible bypassing situations for the given TSV placement (step 3). The total number of bypassing situations is $\sum_{x=1}^{n} C_{m+n}^{x}$, where m and n are regular and spare TSV number in the group. Each bypassing situation represents a defective situation in a TSV group, such that the total number equals to all possible defective situations of having x defective TSVs (where x value is from 1 to n) in the group. Note that if the defective TSV number x > n, the group cannot be repaired. For each bypassing situation, there is a route difference, the weight of that route difference equals to the probability of the corresponding bypassing situation probability (step 5), P*i*(N). Here *i* denotes the i_{th} bypassing situation, and P*i*(N) can be calculated using Eq. (5.2), which equals to the probability of having N defective TSVs in the group. The route difference of a bypassing situation needs to compare between the alternative route wirelength under the bypassing situation and the default route wirelength of the TSV placement case (step 6 and step 7). An example of calculating the route difference of one bypassing situation for TSV placement case in Figure 5.7(a) is demonstrated in Figure 5.7(b), where the bypassing situation results from TSV1 is defective. The alternative route wirelength of such bypassing situation is 6+2TSV_height, while the default route wirelength is 4+2TSV_height (Figure 5.7(a)). This results in 2 unit length of route difference between them, which is then multiplied by the bypassing situation probability P(1) that equals to the probability of having one defective TSV in that group. Such that route difference of that bypassing situation is P(1)*2 (Figure 5.7(b)). After obtaining the route difference of all bypassing situations, it is needed to derive the average route difference, which is achieved through dividing the sum of these route difference by the overall probabilities of all bypassing situations (step 10, Figure 5.8). This average route difference denotes the overall route difference of a TSV placement case.

5.3 Simulation Results

In this section, firstly, a simulation flow for proposed technique with joint consideration of fault tolerance and temperature mitigation is shown in Figure 5.9 (Section 5.3.1). Then, three sets of simulations have been conducted to evaluate the performance of the proposed fault tolerance technique with joint consideration of fault repairing capability and temperature mitigation. First set of simulation (Section 5.3.2) is conducted to demonstrate the effectiveness of achieving 100% repair capability through optimised allocation of spare TSVs. The second set of simulation (Section 5.3.3) evaluates the SA-based TSV placement algorithm for optimizing between temperature, wirelength, and route difference. The last simulation (Section 5.3.4) demonstrates further analysis on the trade-off between wirelength and route difference.

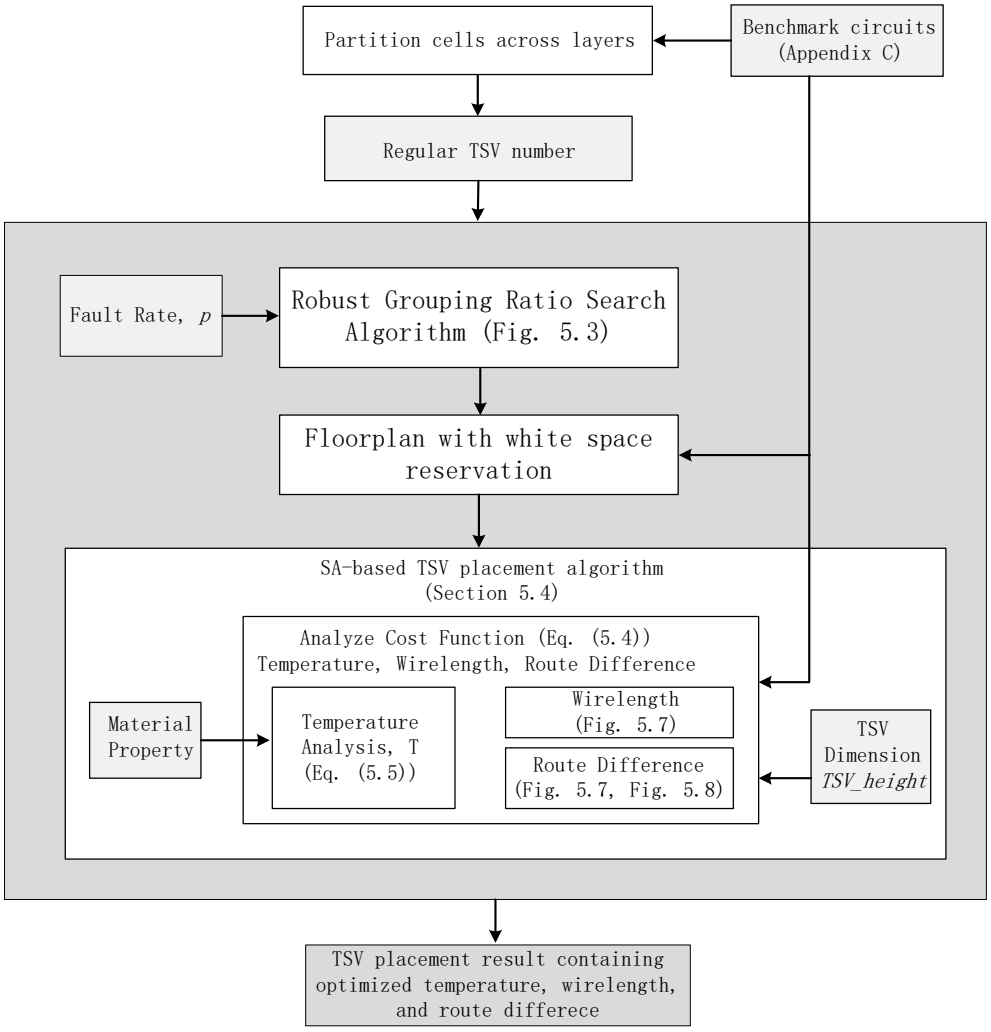


Figure 5.9: Proposed simulation flow for joint consideration of fault tolerance and temperature mitigation.

5.3.1 Proposed Simulation Flow

All simulations are conducted on Intel Xeon Quad Core 2.7 GHz processor with 12 GB RAM. A simulation flow is shown in Figure 5.9 for evaluating the proposed fault tolerance technique. Firstly, a cell portioning step is performed on MCNC/GSRC [184] benchmark circuits, which allocate cells across different layer, the partitioning is based on the method described in [178]. MCNC/GSRC benchmark circuits contain information of cell dimension and pin locations within the cells, which is further detailed in Appendix C. After partitioning step, the regular TSV number is derived and then fed into a proposed robust grouping ratio search algorithm (Figure 5.3). Comparing to the exhaustive search algorithm described in Chapter 3, this algorithm is more efficient as demonstrated in Section 5.3.2. To this point, the simulation flow has completed the TSV determination step (Figure 5.1). Next, TSV placement step (Figure 5.1) is evaluated using the proposed SA-based placement algorithm (Figure 5.4), which is implemented using C++ programme language. It uses the information in the benchmark

circuits (cell dimension) and TSV dimension (TSV_height) to obtain the wirelength (Figure 5.7) and route difference (Figure 5.7 and Figure 5.8) using the method presented in Section 5.2.2. Moreover, temperature modelling of the circuit is also implemented in C++ programme language and embedded in the SA-based TSV placement algorithm which is based on the thermal model discussed in Section 5.2.2. Finally, the simulation flow outputs a TSV placement result with an optimization between temperature, wirelength, and route difference.

5.3.2 Cost-effective TSV Determination Algorithm

Table 5.1: Choosing best grouping ratio for minimized hardware cost (Target repair capability 100%, regular TSVs 6000, fault rate 0.01).

Redundant percentage	Grouping ratio	Spare TSV	Repair capability	Hardware cost (control signal length; deMux/Mux)
100%	1:1	6,000	54.8%	12,000 one-bit;6,000/6,000
	2:2		98.8%	12,000 two-bit;12,000/12,000
	3:3		100%	12,000 two-bit;18,000/18,000
	4:4		100%	12,000 three-bit;24,000/24,000
	5:5		100%	12,000 three-bit;30,000/30,000
50%	2:1	3,000	41%	12,000 one-bit; 6,000/6,000
	4:2		97%	12,000 two-bit; 12,000/12,000
	6:3		**100%**	12,000 two-bit; 18,000/18,000
	8:4		100%	12,000 three-bit;24,000/24,000
	10:5		100%	12,000 three-bit;30,000/30,000
25%	4:1	1,500	23%	12,000 one-bit; 6,000/6,000
	8:2		92%	12,000 two-bit; 12,000/12,000
	12:3		99%	12,000 two-bit; 18,000/18,000
	16:4		**100%**	12,000 three-bit;24,000/24,000
	20:5		100%	12,000 three-bit;30,000/30,000

This simulation is carried out to observe the cost-effectiveness of the proposed TSV determination algorithm in finding a best grouping ratio for a given number of regular TSVs. For illustration purpose, the regular TSV number and TSV fault rate are set to be 6,000 and 0.01 respectively. Results are presented in Table 5.1, as described in Section 5.2.1, the algorithm starts from grouping ratio 1:1 in TSV redundancy percentage of 100%. Once the grouping ratio reaches the target repair capability of 100% is found, the algorithm jumps to the 50% redundancy percentage (1/2 of 100%) and start from grouping ratio 6:3. The searching process of best grouping ratio continues until it gets to grouping ratio of 12:3 in redundancy percentage 25% which cannot achieve the target repair capability. Then, the algorithm will decide whether to jump back to grouping ratio 6:3 and select it as the best grouping ratio for optimal hardware cost in terms of peripheral circuits (detection, recovery

and routing block). Otherwise, the best grouping ratio will be set as the first grouping ratio that achieves the target repair capability in redundancy percentage 25% which is 16:4. As can be seen, if this grouping ratio is selected as the best one, the 1,500 total redundant TSVs can be reduced when compared to the grouping ratio of 6:3, however, this is achieved with a higher hardware cost of peripheral circuits. Besides finding the best grouping ratio for target repair capability under minimized hardware cost, it is shown that the proposed TSV determination algorithm can achieve significant increment in searching efficiency. As shown in Table 5.1, 10% searching steps (grouping ratio in steps with grey colour) can be neglected when compared to the exhaustive searching algorithm presented in Section 3.3.3, Chapter 3, thus increasing searching efficiency by 66.7%.

5.3.3 Performance Evaluation of TSV Placement Algorithm

This set of simulation investigates the performance of the proposed TSV placement algorithm. Firstly, the TSV determination step is implemented on five popular benchmark circuits from MCNC/GSRC [184] (see Appendix C for detailed description of the benchmark circuit) which are meant for floorplanning evaluation, using the method shown in Section 5.2.1. In this work, circuits are partitioned into three-layer 3D designs using partition mechanism presented in [178]. Thus, the number of regular TSVs (signal TSVs) is derived, which is then fed into the TSV determination step (Figure 5.1). Robust search method described in Section 5.2.1 analyses the hardware cost and repair capability of different allocations of spare TSVs to regular ones, and generates the best grouping ratio. Results are shown in Table 5.2, which provides the optimal grouping ratio for each design while achieving 100% repair capability, where 1% TSV fault rate is used (for illustration), as in Chapter 3. Note that, whitespace is set to be from 15% to 20% as in [180].

Table 5.2: TSV determination (Step 1, Figure 5.1) for all designs. Repair capability is preserved (100%) for all designs with 1% fault rate.

Circuit	No. of regular TSV	Grouping ratio	No. of redundant TSV	Whitespace ratio	Repair capability
ami33	118	8:2	30	15%	100%
ami49	267	8:2	67	20%	
n100	926	4:2	463	15%	
n200	1,613	12:3	403	15%	
n300	1,921	12:3	480	20%	

After TSV determination step, the number of spare TSVs and grouping ratio are found for each design, which preserves the repair capability. Next, the SA-based TSV placement algorithm is evaluated, which aims to reduce temperature while optimizing wirelength and

route difference. Table 5.3 shows the TSV placement results for designs with and without TSV redundancy to examine the impact of TSV redundancy structure. All results are obtained using an average value from ten test runs.

Baseline case shows the placement results of design without TSV redundancy, where TSV placement is only wirelength driven, which is achieved by setting the weight coefficient of route difference, (γ=0) and chip temperature weighting parameter, (α=0), thus the influence of these two parameters is ignored. Temperature is derived using the thermal model described in Section 5.2.2.1 (Figure 5.5). To calculate temperature, each block in the circuit is assigned a power density value between 10^5 (w/m^2) and 10^7 (w/m^2) using information from [149]. Note that the total wirelength and chip temperature of baseline case is shown in the fourth column (Table 5.3), which is used as a reference for results with TSV redundancy structure. Due to spare TSVs, there is wirelength overhead, which is shown by the next column (Table 5.3). However, wirelength overhead is due to redundant TSVs for achieving 100% repair capability. The performance of the system may not be affected because extra wires are not in use during normal operation.

For placement results with TSV redundancy, three sets of results are shown which are: wirelength-dominant set that focuses on reducing wirelength (by setting weighting coefficients to be α=0.05, β=0.8, γ=0.15), temperature-dominant (using α=0.8, β=0.1, γ=0.1) which emphasises temperature reduction, while the last set is wirelength&temperature dominant (using α=0.45, β=0.45, γ=0.1) which provides moderate results by reducing both wirelength and temperature. Wirelength and route difference is derived using the method described in Section 5.2.2 (Figure 5.7 and Figure 5.8). As can be seen from Table 5.3, in case of n100, the maximum temperature reduction of 58.5% (from 246.1 ℃ to 101.5 ℃) is achieved with only 8% increase in wirelength (109,326 to 118,025) when implementing placement in temperature-driven manner rather than the wirelength-driven manner. Moreover, by comparing the results for n100 from wirelength-driven set and the wirelength&temperature-driven set, it is found that the wirelength increment can be reduced to 4.2% (from 109,326 to 113,926) while still achieving 40.5% temperature reduction (from 246.1 ℃ to 146.3 ℃). Meanwhile, the overall results across five designs show that, on average 34.1% (from 220.8 ℃ to 145.6 ℃) temperature reduction with 5.1% (252,379 to 265,143) increase in wirelength and 7.1% (from 18,987 to 20,339) increase in route difference. Note that, this 5.1% increase in wirelength is due to assuming 1% fault rate (for illustration) and as expected, this leads to higher number of spares per group to achieve 100% repair capability. This overhead reduces with reduction in fault rate, for example, 2.8% wirelength overhead was observed when considering 0.5% fault rate.

5.3.4 Effect on Wirelength and Route Difference

When using dummy TSVs for temperature mitigation, the wirelength and route difference are not calculated, because dummy TSVs are not connected with signals [126, 149]. In the

proposed technique, spare TSVs are used for temperature mitigation and have an effect on wirelength and route difference. The trade-off between wirelength, route difference, and temperature is examined for n100 (Figure 5.10). As can be seen, it is possible to achieve minimal temperature of 98 ℃ while having lowest route difference. However, there is another option to reduce 19% of wirelength by trading off temperature, (increases to 105.1 ℃) and route difference (increases by 2%).

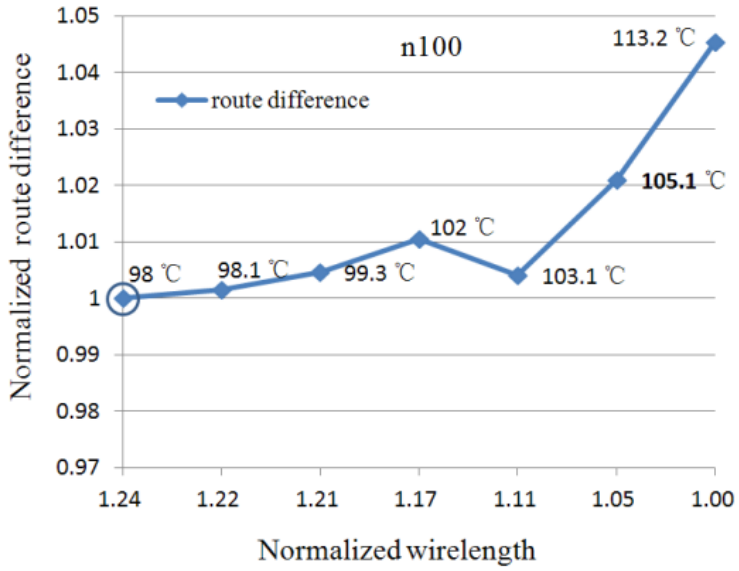


Figure 5.10: Trade-off analysis between wirelength and route difference, where route difference is routing overhead due to bypassing defective TSVs.

5.4 Concluding Remarks

This chapter has presented a TSV fault tolerance technique with joint consideration of tolerating TSV faults (due to manufacturing or latent defects) and temperature mitigation. This is the first work that reuses available redundant TSVs (without using any additional redundant TSV) for temperature mitigation without compromising fault tolerance capability. The temperature mitigation is achieved by careful TSV placement using a simulated-annealing algorithm, which co-optimizes temperature, wirelength and route difference. It is shown that the proposed technique can achieve 100% repair capability (Table 5.1), while in the best case temperature can be reduced up to 58.5% (99.8℃) ((n100, Table 5.3). Over all (five) benchmarks, an average temperature reduction of 34.1% (75.2℃) is achieved while increasing wirelength and route difference by a small amount.

Table 5.3: TSV Placement results (Step 2, Figure 5.1) for optimizing temperature, wirelength and route difference using TSV placement algorithm (Figure 5.4).

Circuit	No. of regular TSV	No. of spare TSV	Baseline (No spare TSVs, wirelength-driven)		With SA-based TSV placement (With Spare TSVs)								
					Wirelength-driven			Temperature-driven			Wirelength&Temperature driven		
			Total WL (um)	T(℃)	Total WL (um)	*route*-D (um)	T (℃)	Total WL (um)	*route*-D (um)	T (℃)	Total WL (um)	*route*-D (um)	T (℃)
ami33	118	30	23,719	197.3	28,397	2,512	193.5	31,298	2,832	123.8	30,384	3,791	153.3
ami49	267	67	502,308	183.1	573,253	41,515	177.3	632,136	48,539	117.2	608,751	45,668	142.1
n100	926	463	91,746	251.3	109,326	10,112	246.1	118,025	10,806	101.5	113,926	10,528	146.3
n200	1,613	403	176,809	241.7	233,657	15,982	236.3	256,751	17,952	93.6	249,876	16,089	138.6
n300	1,921	480	256,763	233.6	317,263	24,815	228.6	331,530	26,263	96.7	322,780	25,621	147.5
Average	-	-	210,269	221.4	252,379	18,987	220.8	273,948	21,278	106.6	265,143	20,339	145.6
Avg. percentage saving in comparison with wirelength driven case.								-8.5%	-12.1%	51.7%	-5.1%	-7.1%	34.1%

Chapter 6

Conclusions and Future Work

The aggressive scaling trend in modern VLSI circuits has required continuous shrinking of device feature size, resulting in performance enhancement of gates. However, the rapid increase in interconnects complexity and delay has become a major concern leading to a system performance bottleneck [60]. The three-dimensional (3D) IC which vertically stacks multiple silicon dies has been acknowledged as a promising technology to overcome this problem, while enabling the reducing in wirelength, power consumption, and allowing integration of heterogeneous technologies. Through-Silicon-Vias (TSVs) based technology is used to implement 3D integration, which stacks dies or wafers with vertical TSV interconnects. However, yield of TSV-based 3D-ICs is limited under current manufacturing process. Only one defective TSV can fail the entire chip with all known-good dies [51]. Moreover, thermal stress induced in fabrication process and during operation also causes TSV reliability issues [81, 86, 185].

6.1 Thesis Contributions

Recent research has highlighted that yield of 3D-ICs is affected due to manufacturing defects [51, 91, 121]. TSV defects can be introduced either from its fabrication process or the bonding process Firstly, random open defects can occur in TSV fabrication process, due to processing variants such as insufficient filling, voids formation, etc. Similarly in bonding process, random open defects may be caused by foreign particles [21]. Secondly, misalignment is due to incorrect wafer alignment during bonding, which results in shift of TSV tips with their bonding pads [21]. Random defects distribution is employed for yield analysis of 3D-ICs [107, 108, 117, 131]. Moreover, clustering defects distributions, which have been acknowledged in traditional semiconductor manufacturing to cluster in an area rather than randomly distributed [153] should also be taken into consideration to analyze their effect on yield of 3D-ICs. Major challenges are highlighted and objectives are designed in Section 2.6. These issues are addressed in each of three contribution chapters.

A mathematical yield modelling method which considers both random TSV defects distribution and clustering defects distribution is presented in Chapter 3, which aims to meet the second objective of this thesis (Chapter 2, Section 2.6). By using the binomial distribution, the yield under random TSV defects distribution can be obtained (Eq. (3.1), Eq. (3.3)). An algorithm is used (Section 3.3) to achieve the yield under clustering TSV defects distribution, where the impact of defective TSV on fault-free ones located around is modelled as a function of distance between them. With such yield modelling mechanism, a TSV redundancy based

technique is proposed to improve the 3D yield by repairing defective TSVs under the objective of optimizing yield improvement and hardware cost. The TSV redundancy structure is based on a TSV grouping method which aims to allocate spare TSVs with regular ones and partition them into groups, within each group multiplexers are used to reroute signals avoiding defective TSVs, in order to achieve the highest yield at the lowest hardware cost (number of multiplexers and spare TSVs) under independent and clustering defect distributions. An exhaustive search method can be used to achieve the best grouping ratio (regular TSV: spare TSV in a group) for target yield improvement under minimal hardware cost (Table 3.2). Simulation results show that for a given number of regular TSVs and failure rate, it is possible to achieve 100% yield while minimizing hardware cost (number of multiplexers and spare TSVs) both under independent and clustering defect distributions.

In addition to manufacturing defects, thermal stress induced in fabrication process and during operation also causes TSV reliability issues [81, 86, 91, 104, 115, 121, 122, 123, 185, 186]. TSV defects are studied in Chapter 2 Section 2.2, meeting the first research objective listed in Section 2.6. Research reported in [86, 185] shows that thermal stress during fabrication process and normal operation can cause damage to TSV interconnects, such as delamination of TSV interfaces. It is reported in [185] that void growth due to thermal-induced migration can also occur during operation resulting lifetime issue. Thus, reliability is a concern during design. [91, 185] summarized various types of TSV latent defects due to thermal load, among which void inside TSVs, delamination between TSV and its landing pad, and TSV short to substrate TSV defects are targeted as three main TSV defect types to be addressed [104, 121, 122, 123]. An online fault tolerance technique is proposed in Chapter 4 to meet the third research objective (Chapter 2 Section 2.6), for TSV defect testing and repairing either from manufacturing defects or thermal-induced latent defects. It utilizes the grouping method based TSV redundancy structure, and aims for both fault detection and recovery in the presence of three TSV defects: voids, delamination between TSV and landing pad, and TSV short-to-substrate. The three types of defects can be modelled as either interconnects short or open faults (fault models in Section 2.2). TSV defect detection and recovery are addressed through a dedicated embedded hardware solution, thus providing a fast test and repair process which needs only two clock cycles (one for detection, one for recovery) for each TSV. Detailed electrical and logical simulations are carried out to validate the working of detection and recovery blocks (Chapter 4). It is shown that the area overhead can be reduced without affecting repair capability through appropriate grouping of regular and redundant TSVs. The cost-effectiveness of the proposed online fault tolerance technique is demonstrated using Synopsys Design Compiler and STMicroelectronics 130-nm gate library. Simulation results show that the overall area overhead of the proposed technique can be 4% for 100% repair capability (Table 4.4).

Redundant circuits can provide an effective solution as a TSV repair technique for improving yield and reliability [105, 117, 135, 160]. However, all these previous work do not consider the thermal impact brought by the repair infrastructure such as redundant TSVs, which have a

significant influence on chip temperature. An indirect approach employed by design experts to reduce overall chip temperature thus relieving thermal reliability at the physical design stage is thermal-aware floorplanning or placement strategies [44, 146, 147, 183]. With the presented floorplanning/placement methods, the overall chip temperature can be reduced to 150°C [149]. However, it is still harmful for chip operation, which may cause delay faults (Figure 5.6, Section 5.2.2.1). To reduce temperature further, [126, 149] adds some dummy vias (TSVs) which serve as additional thermal dissipation tunnels. However, these dummy vias are high cost in terms of chip area and become useless when TSVs suffer from manufacturing defects.

In Chapter 5, a technique based on TSV redundancy, which is not only capable of tolerating TSV defects due to manufacturing issues and thermal-induced reliability problem, is proposed while meeting the fourth research objective of this thesis (Chapter 2 Section 2.6). The proposed fault tolerance technique makes dual use of the embedded redundant TSVs by carefully planning them at two steps. One is TSV determination step of which redundant TSVs serves as repairing components in case of defective TSVs with objective of optimizing hardware cost under target repair capability. The second step is TSV placement, in which TSVs act as main thermal dissipation tunnels and are carefully placed for reducing chip temperature. Unlike the dummy vias used in [126, 149], the proposed technique uses redundant TSVs for practical connection with signals, thus raising a new technical challenge with respect to the switching of signals from regular TSVs to spare ones for bypassing defective TSVs. That results in difference between the original route path length and the alternative route path length. A TSV placement algorithm therefore optimizes this routing difference and the total wirelength while reducing chip temperature. Simulation results shows that the proposed TSV placement algorithm achieves 100% repair capability (Table 5.1), while in the best case temperature can be reduced up to 58.5% (99.8℃) (n100, Table 5.3). Over all (five) benchmarks, an average temperature reduction of 34.1% (75.2℃) is achieved while increasing wirelength and route difference by a small amount. Moreover trade-off analysis between wirelength, temperature, and route difference shows that it is possible to reduce 19% wirelength by trading off temperature, (increases to 105.1 ℃) and route difference (increases by 2%).

The contributions of this thesis are to provide a novel fault tolerance technique for improving yield and reliability of 3D-ICs. Three TSV defect types include void, delamination, and TSV short to substrate are targeted. The developed techniques are supported by extensive and comprehensive simulation results. It is hoped that the developed TSV testing and repairing techniques in this thesis will make useful contributions towards improving yield and reliability of 3D-ICs designs. This is because the availability, efficiency, and cost-effectiveness demonstrated by the proposed fault tolerance technique can be easily incorporated into current 3D designs. In this case, those designs that incorporate the proposed fault tolerance technique can enjoy significant improvement in yield and reliability with a low hardware cost, which brings great benefits for current and future 3D integrated circuits.

6.2 Future work

This section introduces two pieces specific areas for future research. Firstly is the improved TSV fault tolerance technique. The online TSV fault tolerance technique in Chapter 4 is improved by incorporating a set of common redundant TSVs which can be used for multiple TSV groups. The block diagram of the technique is shown in Figure 6.1.

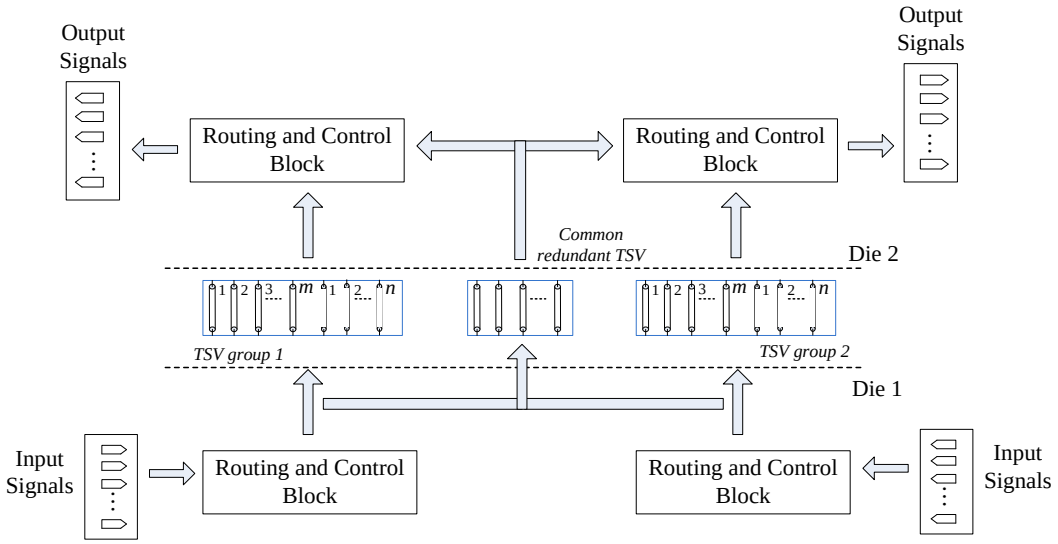


Figure 6.1: TSV fault tolerance technique with improved repair capability.

It can be seen that, unlike the proposed fault tolerance technique presented in Chapter 4. A set of common use redundant TSVs is incorporated. If a design with the grouping ratio of m:n has got a group with n+1 defective TSVs, based on the previous grouping TSV structure, the whole design cannot be repaired due to only one group that cannot be repaired. If such a design with 3D technology involves a high TSV defect rate that may cause this situation, to achieve 100% repair capability, it is needed to add more redundant TSVs to each group, based on the previous structure. However, if a set of common use redundant TSVs is added. These common redundant TSVs can be shared by multiple groups, that is, when one or more groups have more than n defective TSVs they can use the common spare TSVs, this significantly increase the repair capability while only incurring a small hardware cost. To realize this, the routing and control block within each group will be modified in comparison to the structure presented in Chapter 4.

The second piece of work can be thermal-safe test scheduling under the employment of the proposed online fault tolerance technique in this thesis. Thermal-safe scheduling is an important issue in 2D-IC. Thermal management in 3D-IC is much more challenge, therefore, 3D thermal-safe test scheduling is required inevitably. It should account for:

- Unlike 2D test scheduling, modules are now placed onto different layers. And test scheduling involves pre-bond and post-bond stages. How to implement 3D

thermal-safe test scheduling with a tradeoff between minimizing the total test length of both pre-bond and post-bond stages and minimizing the test resources cost (i.e. TAM width, Wrapper length) while achieving targeted fault tolerance capability.

- How to incorporate TSVs effect (both regular and spare TSVs) into the thermal analysis? How to consider TSVs throughout multiple layers as effective thermal dissipation paths to alleviate the temperature issue?

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Appendix A

HSPICE Simulation

Simulation results reported in Chapter 4 Section 4.4.2 for illustrating the defect detection of the proposed online fault tolerance technique used ST Microelectronics 65-nm gate library. In the following, HSPICE description of detection circuit (Figure. 4.5) for detecting both void/delmination and TSV short to substrate TSV defect are presented to provide detailed information.

```
********TSV test circuit Version 1.3 for void/delamination - resistive open TSV defect********

.option brief=1
.global vdd 0 vss
.param vdd=1.2
.param vss=0
.param rval=200m
.param cval=200f
.param ropen=1k

**** Voltage sources ****
Vdd Vdd 0 'vdd'
Vss Vss 0 'vss'

**** Devices Cell Library****
.include '65nm_bulk.pm'
.include '65nm.lib'

*****TSV model T model*******
Ctsv1          nc1          vss      '0.5*cval'
Ctsv2          nc2          vss      '0.5*cval'
Rtsv1          t1           nc1      '0.5*rval'
Ropen           nc1         nc2       'ropen'
Rtsv2          nc2          t2       '0.5*rval'
*****TSV model T model*******
```

```
*****to test void and short resistance*****
xgate_input_mux1 In_TSV1 Re_route_TSV2 Re_route_TSV3 sel0 sel1 t1 vss vdd HS65_LS_MUX31X9
xgate_nand1 t2 SI Test_result vss vdd HS65_LS_NAND2X2

**** Control Section ****
.option nomod
.temp 25

**** Measurements ****
.tran 10PS 81nS sweep ropen 0 1000k 1k

*********measure the delay void defect********
.measure tran rise_delay_t2 TRIG v(t2) VAL='vdd*0.2' TD=0NS RISE=1
+ TARG v(t2) VAL='vdd*0.8' TD=0NS RISE=1
.measure tran fall_delay_t2 TRIG v(t2) VAL='vdd*0.8' TD=0NS FALL=1
+ TARG v(t2) VAL='vdd*0.2' TD=0NS FALL=1
*********measure the delay void defect********

.END
********TSV test circuit Version 1.3 for void/delamination - resistive open TSV defect********


********TSV test circuit Version 1.3 for TSV short to substrate defect********
.option brief=1
.global vdd 0 vss
.param vdd=1.2
.param vss=0
.param rval=200m
.param cval=200f
.param rshort=1k

**** Voltage sources ****
Vdd Vdd 0 'vdd'
Vss Vss 0 'vss'


**** Devices Cell Library****
.include '65nm_bulk.pm'
.include '65nm.lib'

*****TSV model T model*******
```

```
Ctsv1          nc1        vss     '0.5*cval'
Ctsv2          nc1        vss     '0.5*cval'
Rtsv1          t1         nc1     '0.5*rval'
Rshort          nc1       vss      'rshort'
Rtsv2          nc1        t2      '0.5*rval'
*****TSV model T model*******

*****Test circuit to test short to substrate TSV defect*****
xgate_input_mux1      In_TSV1   Re_route_TSV2   Re_route_TSV3   sel0   sel1   t1   vss   vdd
HS65_LS_MUX31X9
xgate_nand1   t2 SI Test_result vss vdd HS65_LS_NAND2X2

**** Control Section ****
.option nomod
.temp 25

**** Measurements ****
.tran 10PS 51nS sweep rshort 0 1k 100

*********measure the delay under TSV short to substrate defect********
.measure tran rise_delay_t2 TRIG v(t2) VAL='vdd*0.2' TD=0NS RISE=1
+ TARG v(t2) VAL='vdd*0.8' TD=0NS RISE=1
.measure tran fall_delay_t2 TRIG v(t2) VAL='vdd*0.8' TD=0NS FALL=1
+ TARG v(t2) VAL='vdd*0.2' TD=0NS FALL=1
*********measure the delay under TSV short to substrate defect********

.END
********TSV test circuit Version 1.3 for TSV short to substrate defect********
```

Appendix B

RTL Description of Recovery Block

Simulation results reported in Chapter 4 Section 4.4.3 show the recovery process for a TSV group with grouping ratio of 4:2. The RTL description of each block in the proposed fault tolerance circuit is presented to provide detailed information in the following.

```
*****Top module reconfiguration circuit*******************
module reconfiguration_circuit1(clk, initial_TSV_status, deMux1, deMux2, deMux3, deMux4);
   input clk;
   input [5:0] initial_TSV_status;
   output [1:0] deMux1, deMux2, deMux3, deMux4;
   wire [1:0] faulty_TSV_accumulate_adder_output;
   wire [5:0] initial_TSV_status;
   TSV_status_chain1 TSV_status_chain(clk, initial_TSV_status, TSV_status_shift_out, TSV_status)
   linecounter1 linecount(clk, TSV_status_shift_out, Signal_line_count, Latch_renew_enable);
   Acc_adder1 Acc_adder(clk, TSV_status_shift_out, faulty_TSV_accumulate_adder_output);
   Latch_chain1 Latch_chain(Latch_renew_enable, clk, faulty_TSV_accumulate_adder_output,
   deMux1, deMux2, deMux3, deMux4);
   endmodule
*****Top module reconfiguration circuit*******************

*****Latch Chain *******************
module Latch_chain1(Latch_renew_enable, clk, faulty_TSV_accumulate_adder_output,
deMux1_S1S0, deMux2_S1S0, deMux3_S1S0, deMux4_S1S0);
input [1:0] faulty_TSV_accumulate_adder_output;
input clk, Latch_renew_enable;
output [1:0] deMux1_S1S0, deMux2_S1S0, deMux3_S1S0, deMux4_S1S0;
reg [1:0] deMux1_S1S0, deMux2_S1S0, deMux3_S1S0, deMux4_S1S0;
wire [1:0] faulty_TSV_accumulate_adder_output;
initial
begin
deMux1_S1S0=0;
deMux2_S1S0=0;
deMux3_S1S0=0;
```

```
deMux4_S1S0=0;
end
always @(posedge clk)
begin
if (Latch_renew_enable)
begin
deMux4_S1S0<=faulty_TSV_accumulate_adder_output;
deMux3_S1S0<=deMux4_S1S0;
deMux2_S1S0<=deMux3_S1S0;
deMux1_S1S0<=deMux2_S1S0;
end
end
endmodule
*****Latch Chain ********************
*****Accumulate Adder ********************
module Acc_adder1(clk, TSV_status_shift_out, faulty_TSV_accumulate_adder_output);
input TSV_status_shift_out, clk;
output [1:0]    faulty_TSV_accumulate_adder_output;
reg [1:0] faulty_TSV_accumulate_adder_output;
initial
faulty_TSV_accumulate_adder_output=0;
always @(posedge clk)
begin
if (TSV_status_shift_out)
faulty_TSV_accumulate_adder_output=faulty_TSV_accumulate_adder_output+1;
end
endmodule
*****Accumulate Adder ********************

*****Signal Line Counter ********************
module linecounter1(clk, TSV_status_shift_out, Signal_line_count, Latch_renew_enable);
input clk;
input TSV_status_shift_out;
output [2:0] Signal_line_count;
output Latch_renew_enable;
reg Latch_renew_enable;
reg [2:0] Signal_line_count;
initial
Signal_line_count=0;
initial
Latch_renew_enable=0;
always @(posedge clk)
```

```
begin
if (!TSV_status_shift_out)
begin
Signal_line_count=Signal_line_count+1;
Latch_renew_enable=1;
if (Signal_line_count>5)
Latch_renew_enable=0;
if (Signal_line_count>5)
Signal_line_count=5;
end
else
Latch_renew_enable=0;
end
endmodule
*****Signal Line Counter ********************

*****TSV Status Chain ********************
module TSV_status_chain1(clk, initial_TSV_status, TSV_status_shift_out, TSV_status);

input clk;
input [5:0] initial_TSV_status;
output TSV_status_shift_out;
output [5:0] TSV_status;
reg TSV_status_shift_out;
reg [5:0] TSV_status;
wire [5:0] initial_TSV_status;
initial
begin
TSV_status=6'b101000;
end
always @(posedge clk)
begin
TSV_status_shift_out<=TSV_status[5];
TSV_status[0]<=1'b0;
TSV_status[1]<=TSV_status[0];
TSV_status[2]<=TSV_status[1];
TSV_status[3]<=TSV_status[2];
TSV_status[4]<=TSV_status[3];
TSV_status[5]<=TSV_status[4];
end
endmodule
*****TSV Status Chain ********************
```

Appendix C

Simulation reported in Chapter 5 used MCNC/GSRC benchmark circuits, which are meant for floorplanning purpose. Description of benchmark circuits contain cell dimension and cell pins location. After partitioning these cell on different layers, signal (regular) TSVs can be used to link cells across layers. In the following, , the description one circuit model *aim33* is present for illustration purpose. Other benchmark circuits used in Chapter 5 Section 5.3 are in similar format and can be found in [184].

```
/* File name ami33.yal                                    */
/*
* BBL file bench.ami.scale read by version 0.82 at Tue Jan    5 15:29:44 1988
*/
MODULE bk1;
 TYPE GENERAL;
 DIMENSIONS 336 0 336 133 0 133 0 0;
 IOLIST;
  P_0 PWR 175 0 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
  P_1 PWR 105 0 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
  P_2 B 336 14 1 METAL2;
  P_3 B 0 14 1 METAL2;
  P_4 B 336 7 1 METAL2;
  P_5 B 0 7 1 METAL2;
  P_6 B 336 105 1 METAL2;
  P_7 B 0 105 1 METAL2;
  P_8 B 336 112 1 METAL2;
  P_9 B 0 112 1 METAL2;
  P_10 B 112 133 1 METAL2;
  P_11 B 0 42 1 METAL2;
  P_12 B 273 133 1 METAL2;
 ENDIOLIST;
ENDMODULE;
MODULE bk10a;
 TYPE GENERAL;
 DIMENSIONS 378 0 378 119 0 119 0 0;
 IOLIST;
  P_0 PWR 280 0 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
  P_1 PWR 70 0 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
  P_2 B 378 7 1 METAL2;
  P_3 B 0 7 1 METAL2;
```

```
   P_4 B 378 84 1 METAL2;
   P_5 B 0 14 1 METAL2;
   P_6 B 14 119 1 METAL2;
   P_7 B 378 105 1 METAL2;
   P_8 B 0 105 1 METAL2;
   P_9 B 378 112 1 METAL2;
   P_10 B 0 112 1 METAL2;
   P_11 B 0 84 1 METAL2;
   P_12 B 0 77 1 METAL2;
   P_13 B 0 42 1 METAL2;
   P_14 B 0 35 1 METAL2;
   P_15 B 0 70 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk10b;
  TYPE GENERAL;
  DIMENSIONS 161 0 161 140 0 140 0 0;
  IOLIST;
   P_0 B 161 133 1 METAL2;
   P_1 PWR 0 70 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
   P_2 B 0 133 1 METAL2;
   P_3 B 161 126 1 METAL2;
   P_4 B 0 126 1 METAL2;
   P_5 B 161 7 1 METAL2;
   P_6 B 0 7 1 METAL2;
   P_7 B 161 14 1 METAL2;
   P_8 B 0 14 1 METAL2;
   P_9 B 35 140 1 METAL2;
   P_10 B 161 70 1 METAL2;
   P_11 PWR 7 0 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
   P_12 B 70 0 1 METAL2;
   P_13 B 154 140 1 METAL2;
   P_14 B 126 140 1 METAL2;
   P_15 B 49 140 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk10c;
  TYPE GENERAL;
  DIMENSIONS 119 0 119 49 0 49 0 0;
  IOLIST;
   P_0 PWR 70 49 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
   P_1 PWR 0 21 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
```

```
    P_2 B 112 49 1 METAL2;
    P_3 B 112 0 1 METAL2;
    P_4 B 105 0 1 METAL2;
    P_5 B 35 49 1 METAL2;
    P_6 B 14 0 1 METAL2;
    P_7 B 7 49 1 METAL2;
    P_8 B 7 0 1 METAL2;
    P_9 B 91 0 1 METAL2;
    P_10 B 77 0 1 METAL2;
    P_11 B 98 0 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk11;
  TYPE GENERAL;
  DIMENSIONS 175 0 175 119 0 119 0 0;
  IOLIST;
    P_0 PWR 70 0 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_1 PWR 14 119 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_2 B 161 119 1 METAL2;
    P_3 B 175 112 1 METAL2;
    P_4 B 0 112 1 METAL2;
    P_5 B 175 105 1 METAL2;
    P_6 B 0 105 1 METAL2;
    P_7 B 175 7 1 METAL2;
    P_8 B 0 7 1 METAL2;
    P_9 B 175 14 1 METAL2;
    P_10 B 0 14 1 METAL2;
    P_11 B 175 49 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk12;
  TYPE GENERAL;
  DIMENSIONS 140 0 140 406 0 406 0 0;
  IOLIST;
    P_0 PWR 140 140 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_1 PWR 0 140 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_2 B 7 406 1 METAL2;
    P_3 B 7 0 1 METAL2;
    P_4 B 35 406 1 METAL2;
    P_5 B 133 406 1 METAL2;
    P_6 B 133 0 1 METAL2;
    P_7 B 119 406 1 METAL2;
```

```
    P_8 B 70 0 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk13;
  TYPE GENERAL;
  DIMENSIONS 140 0 140 497 0 497 0 0;
  IOLIST;
    P_0 PWR 140 210 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_1 PWR 0 210 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_2 B 112 497 1 METAL2;
    P_3 B 28 0 1 METAL2;
    P_4 B 35 497 1 METAL2;
    P_5 B 35 0 1 METAL2;
    P_6 B 140 441 1 METAL2;
    P_7 B 91 497 1 METAL2;
    P_8 B 133 0 1 METAL2;
    P_9 B 126 497 1 METAL2;
    P_10 B 126 0 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk14a;
  TYPE GENERAL;
  DIMENSIONS 196 0 196 119 0 119 0 0;
  IOLIST;
    P_0 PWR 70 119 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_1 PWR 70 0 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_2 B 196 14 1 METAL2;
    P_3 B 0 14 1 METAL2;
    P_4 B 196 112 1 METAL2;
    P_5 B 0 112 1 METAL2;
    P_6 B 196 28 1 METAL2;
    P_7 B 0 105 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk14b;
  TYPE GENERAL;
  DIMENSIONS 294 0 294 119 0 119 0 0;
  IOLIST;
    P_0 PWR 210 0 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
    P_1 PWR 35 0 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
    P_2 B 294 112 1 METAL2;
    P_3 B 0 112 1 METAL2;
```

```
    P_4 B 294 14 1 METAL2;
    P_5 B 0 14 1 METAL2;
    P_6 B 294 7 1 METAL2;
    P_7 B 0 7 1 METAL2;
    P_8 B 294 105 1 METAL2;
    P_9 B 0 105 1 METAL2;
    P_10 B 280 119 1 METAL2;
    P_11 B 245 119 1 METAL2;
    P_12 B 0 49 1 METAL2;
    P_13 B 77 119 1 METAL2;
    P_14 B 105 119 1 METAL2;
    P_15 B 49 119 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk14c;
  TYPE GENERAL;
  DIMENSIONS 161 0 161 119 0 119 0 0;
  IOLIST;
    P_0 PWR 70 119 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_1 PWR 70 0 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_2 B 161 7 1 METAL2;
    P_3 B 0 7 1 METAL2;
    P_4 B 161 112 1 METAL2;
    P_5 B 0 112 1 METAL2;
    P_6 B 0 42 1 METAL2;
    P_7 B 161 70 1 METAL2;
    P_8 B 161 63 1 METAL2;
    P_9 B 161 42 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk15a;
  TYPE GENERAL;
  DIMENSIONS 119 0 119 266 0 266 0 0;
  IOLIST;
    P_0 PWR 119 175 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_1 PWR 119 70 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_2 B 0 252 1 METAL2;
    P_3 B 0 168 1 METAL2;
    P_4 B 21 0 1 METAL2;
    P_5 B 7 266 1 METAL2;
    P_6 B 7 0 1 METAL2;
    P_7 B 105 0 1 METAL2;
```

```
    P_8 B 35 266 1 METAL2;
    P_9 B 21 266 1 METAL2;
    P_10 B 35 0 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk15b;
  TYPE GENERAL;
  DIMENSIONS 119 0 119 336 0 336 0 0;
  IOLIST;
    P_0 PWR 119 210 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_1 PWR 119 35 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_2 B 0 140 1 METAL2;
    P_3 B 0 28 1 METAL2;
    P_4 B 7 336 1 METAL2;
    P_5 B 7 0 1 METAL2;
    P_6 B 14 336 1 METAL2;
    P_7 B 112 336 1 METAL2;
    P_8 B 112 0 1 METAL2;
    P_9 B 0 329 1 METAL2;
    P_10 B 0 217 1 METAL2;
    P_11 B 35 0 1 METAL2;
    P_12 B 35 336 1 METAL2;
    P_13 B 28 336 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk16;
  TYPE GENERAL;
  DIMENSIONS 119 0 119 126 0 126 0 0;
  IOLIST;
    P_0 PWR 119 70 1 METAL2 CURRENT 0.001 VOLTAGE 2.100;
    P_1 PWR 0 70 1 METAL2 CURRENT 0.001 VOLTAGE 2.100;
    P_2 B 70 126 1 METAL2;
    P_3 B 70 0 1 METAL2;
    P_4 B 91 0 1 METAL2;
    P_5 B 105 0 1 METAL2;
    P_6 B 56 0 1 METAL2;
    P_7 B 63 0 1 METAL2;
    P_8 B 7 0 1 METAL2;
    P_9 B 14 0 1 METAL2;
    P_10 B 77 0 1 METAL2;
    P_11 B 21 0 1 METAL2;
    P_12 B 28 0 1 METAL2;
```

```
    P_13 B 112 0 1 METAL2;
    P_14 B 98 0 1 METAL2;
    P_15 B 35 0 1 METAL2;
    P_16 B 21 126 1 METAL2;
    P_17 B 14 126 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk17a;
  TYPE GENERAL;
  DIMENSIONS 371 0 371 182 0 182 0 0;
  IOLIST;
    P_0 PWR 140 182 1 METAL2 CURRENT 0.005 VOLTAGE 1.800;
    P_1 PWR 140 0 1 METAL2 CURRENT 0.005 VOLTAGE 1.800;
    P_2 B 371 21 1 METAL2;
    P_3 B 0 21 1 METAL2;
    P_4 B 371 14 1 METAL2;
    P_5 B 0 14 1 METAL2;
    P_6 B 371 168 1 METAL2;
    P_7 B 0 168 1 METAL2;
    P_8 B 371 175 1 METAL2;
    P_9 B 0 175 1 METAL2;
    P_10 B 371 98 1 METAL2;
    P_11 B 371 35 1 METAL2;
    P_12 B 0 84 1 METAL2;
    P_13 B 0 63 1 METAL2;
    P_14 B 0 77 1 METAL2;
    P_15 B 0 140 1 METAL2;
    P_16 B 0 98 1 METAL2;
    P_17 B 0 126 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk17b;
  TYPE GENERAL;
  DIMENSIONS 182 0 182 203 0 203 0 0;
  IOLIST;
    P_0 PWR 105 203 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_1 PWR 105 0 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_2 B 0 21 1 METAL2;
    P_3 B 182 14 1 METAL2;
    P_4 B 0 14 1 METAL2;
    P_5 B 0 168 1 METAL2;
    P_6 B 182 175 1 METAL2;
```

```
    P_7 B 0 175 1 METAL2;
    P_8 B 182 126 1 METAL2;
    P_9 B 182 119 1 METAL2;
    P_10 B 182 105 1 METAL2;
    P_11 B 0 147 1 METAL2;
    P_12 B 0 126 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk18;
  TYPE GENERAL;
  DIMENSIONS 182 0 182 203 0 203 0 0;
  IOLIST;
    P_0 PWR 105 203 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_1 PWR 105 0 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_2 B 182 35 1 METAL2;
    P_3 B 182 28 1 METAL2;
    P_4 B 182 21 1 METAL2;
    P_5 B 0 21 1 METAL2;
    P_6 B 182 14 1 METAL2;
    P_7 B 0 14 1 METAL2;
    P_8 B 182 168 1 METAL2;
    P_9 B 0 168 1 METAL2;
    P_10 B 182 175 1 METAL2;
    P_11 B 0 175 1 METAL2;
    P_12 B 182 147 1 METAL2;
    P_13 B 0 98 1 METAL2;
    P_14 B 0 35 1 METAL2;
    P_15 B 0 140 1 METAL2;
    P_16 B 0 126 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk19;
  TYPE GENERAL;
  DIMENSIONS 84 0 84 119 0 119 0 0;
  IOLIST;
    P_0 PWR 84 70 1 METAL2 CURRENT 0.001 VOLTAGE 2.100;
    P_1 PWR 0 70 1 METAL2 CURRENT 0.001 VOLTAGE 2.100;
    P_2 B 49 0 1 METAL2;
    P_3 B 35 0 1 METAL2;
    P_4 B 21 0 1 METAL2;
    P_5 B 7 0 1 METAL2;
    P_6 B 28 119 1 METAL2;
```

```
    P_7 B 14 119 1 METAL2;
    P_8 B 42 119 1 METAL2;
    P_9 B 70 119 1 METAL2;
    P_10 B 56 119 1 METAL2;
    P_11 B 77 119 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk2;
  TYPE GENERAL;
  DIMENSIONS 133 0 133 294 0 294 0 0;
  IOLIST;
    P_0 PWR 133 140 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
    P_1 PWR 0 140 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
    P_2 B 21 294 1 METAL2;
    P_3 B 21 0 1 METAL2;
    P_4 B 14 294 1 METAL2;
    P_5 B 14 0 1 METAL2;
    P_6 B 63 0 1 METAL2;
    P_7 B 112 294 1 METAL2;
    P_8 B 112 0 1 METAL2;
    P_9 B 119 294 1 METAL2;
    P_10 B 119 0 1 METAL2;
    P_11 B 84 0 1 METAL2;
    P_12 B 105 0 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk20;
  TYPE GENERAL;
  DIMENSIONS 182 0 182 350 0 350 0 0;
  IOLIST;
    P_0 PWR 0 280 1 METAL2 CURRENT 0.005 VOLTAGE 1.800;
    P_1 PWR 0 35 1 METAL2 CURRENT 0.005 VOLTAGE 1.800;
    P_2 B 21 350 1 METAL2;
    P_3 B 21 0 1 METAL2;
    P_4 B 14 350 1 METAL2;
    P_5 B 14 0 1 METAL2;
    P_6 B 119 0 1 METAL2;
    P_7 B 168 0 1 METAL2;
    P_8 B 175 350 1 METAL2;
    P_9 B 175 0 1 METAL2;
    P_10 B 182 70 1 METAL2;
    P_11 B 182 259 1 METAL2;
```

```
    P_12 B 147 0 1 METAL2;
    P_13 B 84 0 1 METAL2;
    P_14 B 63 0 1 METAL2;
    P_15 B 77 0 1 METAL2;
    P_16 B 140 0 1 METAL2;
    P_17 B 98 0 1 METAL2;
    P_18 B 126 0 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk21;
  TYPE GENERAL;
  DIMENSIONS 315 0 315 140 0 140 0 0;
  IOLIST;
    P_0 PWR 280 140 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_1 PWR 35 140 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_2 B 70 0 1 METAL2;
    P_3 B 315 112 1 METAL2;
    P_4 B 0 112 1 METAL2;
    P_5 B 315 105 1 METAL2;
    P_6 B 0 105 1 METAL2;
    P_7 B 315 7 1 METAL2;
    P_8 B 0 7 1 METAL2;
    P_9 B 315 14 1 METAL2;
    P_10 B 0 14 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk3;
  TYPE GENERAL;
  DIMENSIONS 133 0 133 315 0 315 0 0;
  IOLIST;
    P_0 B 119 315 1 METAL2;
    P_1 B 119 0 1 METAL2;
    P_2 B 126 315 1 METAL2;
    P_3 B 126 0 1 METAL2;
    P_4 B 28 315 1 METAL2;
    P_5 B 28 0 1 METAL2;
    P_6 B 21 315 1 METAL2;
    P_7 B 21 0 1 METAL2;
    P_8 B 133 21 1 METAL2;
    P_9 B 133 7 1 METAL2;
    P_10 PWR 0 280 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
    P_11 PWR 0 105 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
```

```
    P_12 B 0 7 1 METAL2;
    P_13 B 56 0 1 METAL2;
    P_14 B 70 0 1 METAL2;
    P_15 B 35 0 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk4;
  TYPE GENERAL;
  DIMENSIONS 560 0 560 133 0 133 0 0;
  IOLIST;
    P_0 PWR 105 133 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_1 PWR 105 0 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_2 B 560 21 1 METAL2;
    P_3 B 0 21 1 METAL2;
    P_4 B 560 14 1 METAL2;
    P_5 B 0 14 1 METAL2;
    P_6 B 560 112 1 METAL2;
    P_7 B 0 112 1 METAL2;
    P_8 B 560 119 1 METAL2;
    P_9 B 0 119 1 METAL2;
    P_10 B 560 49 1 METAL2;
    P_11 B 560 35 1 METAL2;
    P_12 B 560 28 1 METAL2;
    P_13 B 0 35 1 METAL2;
    P_14 B 0 49 1 METAL2;
    P_15 B 7 133 1 METAL2;
    P_16 B 0 98 1 METAL2;
    P_17 B 546 133 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk5a;
  TYPE GENERAL;
  DIMENSIONS 133 0 133 140 0 140 0 0;
  IOLIST;
    P_0 PWR 133 70 1 METAL2 CURRENT 0.001 VOLTAGE 2.100;
    P_1 PWR 0 70 1 METAL2 CURRENT 0.001 VOLTAGE 2.100;
    P_2 B 21 0 1 METAL2;
    P_3 B 14 140 1 METAL2;
    P_4 B 14 0 1 METAL2;
    P_5 B 112 140 1 METAL2;
    P_6 B 112 0 1 METAL2;
    P_7 B 119 0 1 METAL2;
```

```
   P_8 B 42 140 1 METAL2;
   P_9 B 77 140 1 METAL2;
   P_10 B 91 140 1 METAL2;
   P_11 B 98 140 1 METAL2;
   P_12 B 98 0 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk5b;
  TYPE GENERAL;
  DIMENSIONS 175 0 175 133 0 133 0 0;
  IOLIST;
   P_0 PWR 140 0 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
   P_1 PWR 35 0 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
   P_2 B 175 112 1 METAL2;
   P_3 B 0 112 1 METAL2;
   P_4 B 175 14 1 METAL2;
   P_5 B 0 14 1 METAL2;
   P_6 B 175 21 1 METAL2;
   P_7 B 0 21 1 METAL2;
   P_8 B 175 119 1 METAL2;
   P_9 B 0 119 1 METAL2;
   P_10 B 175 42 1 METAL2;
   P_11 B 175 70 1 METAL2;
   P_12 B 175 35 1 METAL2;
   P_13 B 175 77 1 METAL2;
   P_14 B 63 133 1 METAL2;
   P_15 B 175 91 1 METAL2;
   P_16 B 0 49 1 METAL2;
   P_17 B 35 133 1 METAL2;
   P_18 B 56 133 1 METAL2;
   P_19 B 70 133 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk5c;
  TYPE GENERAL;
  DIMENSIONS 133 0 133 231 0 231 0 0;
  IOLIST;
   P_0 PWR 133 140 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
   P_1 PWR 0 140 1 METAL2 CURRENT 0.003 VOLTAGE 2.000;
   P_2 B 119 231 1 METAL2;
   P_3 B 119 0 1 METAL2;
   P_4 B 126 0 1 METAL2;
```

```
    P_5 B 28 0 1 METAL2;
    P_6 B 21 0 1 METAL2;
    P_7 B 112 231 1 METAL2;
    P_8 B 84 0 1 METAL2;
    P_9 B 98 0 1 METAL2;
    P_10 B 63 231 1 METAL2;
    P_11 B 35 231 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk6;
  TYPE GENERAL;
  DIMENSIONS 133 0 133 315 0 315 0 0;
  IOLIST;
    P_0 B 84 0 1 METAL2;
    P_1 B 14 315 1 METAL2;
    P_2 B 7 315 1 METAL2;
    P_3 B 7 0 1 METAL2;
    P_4 B 28 315 1 METAL2;
    P_5 B 0 238 1 METAL2;
    P_6 B 105 315 1 METAL2;
    P_7 B 105 0 1 METAL2;
    P_8 B 112 0 1 METAL2;
    P_9 B 42 315 1 METAL2;
    P_10 B 49 315 1 METAL2;
    P_11 B 0 98 1 METAL2;
    P_12 B 49 0 1 METAL2;
    P_13 B 35 0 1 METAL2;
    P_14 B 70 0 1 METAL2;
    P_15 B 77 0 1 METAL2;
    P_16 B 56 0 1 METAL2;
    P_17 PWR 133 210 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_18 PWR 133 14 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_19 B 133 301 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk7;
  TYPE GENERAL;
  DIMENSIONS 182 0 182 98 0 98 0 0;
  IOLIST;
    P_0 PWR 182 84 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
    P_1 B 35 98 1 METAL2;
    P_2 PWR 0 84 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
```

```
    P_3 B 0 49 1 METAL2;
    P_4 B 168 98 1 METAL2;
    P_5 B 168 0 1 METAL2;
    P_6 B 175 98 1 METAL2;
    P_7 B 175 0 1 METAL2;
    P_8 B 49 98 1 METAL2;
    P_9 B 133 98 1 METAL2;
    P_10 B 7 0 1 METAL2;
    P_11 B 14 0 1 METAL2;
    P_12 B 119 98 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk8a;
  TYPE GENERAL;
  DIMENSIONS 210 0 210 210 0 210 0 0;
  IOLIST;
    P_0 PWR 105 0 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_1 PWR 0 105 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_2 B 210 112 1 METAL2;
    P_3 B 210 119 1 METAL2;
    P_4 B 210 126 1 METAL2;
    P_5 B 210 133 1 METAL2;
    P_6 B 210 140 1 METAL2;
    P_7 B 210 147 1 METAL2;
    P_8 B 210 154 1 METAL2;
    P_9 B 98 210 1 METAL2;
    P_10 B 112 210 1 METAL2;
    P_11 B 63 210 1 METAL2;
    P_12 B 70 210 1 METAL2;
    P_13 B 14 210 1 METAL2;
    P_14 B 21 210 1 METAL2;
    P_15 B 28 210 1 METAL2;
    P_16 B 42 210 1 METAL2;
    P_17 B 210 63 1 METAL2;
    P_18 B 210 70 1 METAL2;
    P_19 B 210 77 1 METAL2;
    P_20 B 210 84 1 METAL2;
    P_21 B 210 91 1 METAL2;
    P_22 B 210 98 1 METAL2;
    P_23 B 210 105 1 METAL2;
  ENDIOLIST;
ENDMODULE;
```

```
MODULE bk8b;
 TYPE GENERAL;
 DIMENSIONS 126 0 126 378 0 378 0 0;
 IOLIST;
  P_0 PWR 63 0 1 METAL2 CURRENT 0.003 VOLTAGE 2.100;
  P_1 PWR 126 175 1 METAL2 CURRENT 0.003 VOLTAGE 2.100;
  P_2 B 0 119 1 METAL2;
  P_3 B 0 126 1 METAL2;
  P_4 B 0 133 1 METAL2;
  P_5 B 0 140 1 METAL2;
  P_6 B 0 147 1 METAL2;
  P_7 B 0 154 1 METAL2;
  P_8 B 0 161 1 METAL2;
  P_9 B 14 378 1 METAL2;
  P_10 B 7 378 1 METAL2;
  P_11 B 35 378 1 METAL2;
  P_12 B 49 378 1 METAL2;
  P_13 B 63 378 1 METAL2;
  P_14 B 77 378 1 METAL2;
  P_15 B 0 70 1 METAL2;
  P_16 B 0 77 1 METAL2;
  P_17 B 0 84 1 METAL2;
  P_18 B 0 91 1 METAL2;
  P_19 B 0 98 1 METAL2;
  P_20 B 0 105 1 METAL2;
  P_21 B 0 112 1 METAL2;
 ENDIOLIST;
ENDMODULE;
MODULE bk9a;
 TYPE GENERAL;
 DIMENSIONS 182 0 182 119 0 119 0 0;
 IOLIST;
  P_0 PWR 140 0 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
  P_1 PWR 35 0 1 METAL2 CURRENT 0.002 VOLTAGE 2.100;
  P_2 B 182 7 1 METAL2;
  P_3 B 0 7 1 METAL2;
  P_4 B 182 14 1 METAL2;
  P_5 B 0 14 1 METAL2;
  P_6 B 182 105 1 METAL2;
  P_7 B 0 105 1 METAL2;
  P_8 B 182 112 1 METAL2;
  P_9 B 0 112 1 METAL2;
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    P_10 B 21 119 1 METAL2;
    P_11 B 182 35 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk9b;
  TYPE GENERAL;
  DIMENSIONS 119 0 119 119 0 119 0 0;
  IOLIST;
    P_0 PWR 105 119 1 METAL2 CURRENT 0.001 VOLTAGE 2.100;
    P_1 PWR 14 119 1 METAL2 CURRENT 0.001 VOLTAGE 2.100;
    P_2 B 119 112 1 METAL2;
    P_3 B 0 112 1 METAL2;
    P_4 B 119 105 1 METAL2;
    P_5 B 0 105 1 METAL2;
    P_6 B 119 7 1 METAL2;
    P_7 B 0 14 1 METAL2;
    P_8 B 119 14 1 METAL2;
    P_9 B 0 7 1 METAL2;
    P_10 B 7 0 1 METAL2;
    P_11 B 119 63 1 METAL2;
    P_12 B 56 0 1 METAL2;
    P_13 B 0 42 1 METAL2;
    P_14 B 0 49 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk9c;
  TYPE GENERAL;
  DIMENSIONS 357 0 357 119 0 119 0 0;
  IOLIST;
    P_0 PWR 210 119 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_1 PWR 14 119 1 METAL2 CURRENT 0.004 VOLTAGE 1.900;
    P_2 B 350 119 1 METAL2;
    P_3 B 357 112 1 METAL2;
    P_4 B 0 112 1 METAL2;
    P_5 B 357 105 1 METAL2;
    P_6 B 0 105 1 METAL2;
    P_7 B 0 77 1 METAL2;
    P_8 B 357 7 1 METAL2;
    P_9 B 0 7 1 METAL2;
    P_10 B 357 14 1 METAL2;
    P_11 B 0 14 1 METAL2;
    P_12 B 357 49 1 METAL2;
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    P_13 B 280 0 1 METAL2;
    P_14 B 0 21 1 METAL2;
    P_15 B 0 42 1 METAL2;
    P_16 B 7 0 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bk9d;
  TYPE GENERAL;
  DIMENSIONS 119 0 119 84 0 84 0 0;
  IOLIST;
    P_0 PWR 0 70 1 METAL2 CURRENT 0.001 VOLTAGE 2.100;
    P_1 B 7 0 1 METAL2;
    P_2 B 14 0 1 METAL2;
    P_3 B 112 0 1 METAL2;
    P_4 B 105 0 1 METAL2;
    P_5 B 98 84 1 METAL2;
    P_6 PWR 119 70 1 METAL2 CURRENT 0.001 VOLTAGE 2.100;
    P_7 B 119 7 1 METAL2;
    P_8 B 63 84 1 METAL2;
  ENDIOLIST;
ENDMODULE;
MODULE bound;
  TYPE PARENT;
  DIMENSIONS 2058 0 2058 1463 0 1463 0 0;
  IOLIST;
    VSS PB 1281 1463 1 METAL2;
    VDD PB 1687 0 1 METAL2;
    P9 PB 266 0 1 METAL2;
    P8 PB 168 0 1 METAL2;
    P7 PB 924 0 1 METAL2;
    P6 PB 826 0 1 METAL2;
    P5 PB 721 0 1 METAL2;
    P4 PB 1022 0 1 METAL2;
    P37 PB 945 1463 1 METAL2;
    P36 PB 714 1463 1 METAL2;
    POW PWR 350 1463 1 METAL2 CURRENT 0.100 VOLTAGE 1000.000;
    POW PWR 1960 0 1 METAL2;
    P35 PB 0 483 1 METAL2;
    P34 PB 0 343 1 METAL2;
    P33 PB 0 196 1 METAL2;
    P32 PB 0 623 1 METAL2;
    P31 PB 0 1225 1 METAL2;
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  P30 PB 518 1463 1 METAL2;
  P3 PB 1176 1463 1 METAL2;
  P29 PB 616 1463 1 METAL2;
  P28 PB 1484 0 1 METAL2;
  P27 PB 336 1463 1 METAL2;
  P26 PB 1267 0 1 METAL2;
  P25 PB 553 0 1 METAL2;
  P24 PB 2058 168 1 METAL2;
  P23 PB 2058 861 1 METAL2;
  P22 PB 2058 728 1 METAL2;
  P21 PB 1400 1463 1 METAL2;
  P20 PB 1645 1463 1 METAL2;
  P2 PB 1127 0 1 METAL2;
  P19 PB 2058 1421 1 METAL2;
  P18 PB 2058 1365 1 METAL2;
  P17 PB 2058 1106 1 METAL2;
  GND PWR 2058 140 1 METAL2 CURRENT 0.100 VOLTAGE 1000.000;
  GND PWR 0 1120 1 METAL2;
  P16 PB 0 763 1 METAL2;
  P15 PB 0 994 1 METAL2;
  P14 PB 2058 343 1 METAL2;
  P13 PB 2058 602 1 METAL2;
  P12 PB 2058 476 1 METAL2;
  P11 PB 455 0 1 METAL2;
  P10 PB 364 0 1 METAL2;
ENDIOLIST;
NETWORK;
  C_0 bk9d GND P2G P2F P1G P1F 399 POW 379 378;
  C_1 bk9c GND POW P30 P2G P2G P2F P2F P27 P1G P1G P1F P1F 46 46 399 391 291;
  C_2 bk9b GND POW P2G P2G P2F P2F P1G P1G P1F P1F 46 378 291 284 273;
  C_3 bk9a GND POW P2G P2G P2F P2F P1G P1G P1F P1F 391 198;
  C_4 bk8b GND POW 99 98 97 96 95 94 93 115 114 112 111 110 109 106 105 104 103 102 101 100;
  C_5 bk8a GND POW 99 98 97 96 95 94 93 88 87 86 85 84 83 55 25 106 105 104 103 102 101 100;
  C_6 bk7 GND VSS POW VDD P2G P2G P2F P2F P23 P22 P1G P1F 371;
  C_7 bk6 P2G P2G P2F P2F P21 P20 P1G P1G P1F P19 P18 P17 328 327 258 257 226 GND POW
  219;
  C_8 bk5c GND POW P2G P2G P2F P1G P1F 331 328 327 258 257;
  C_9 bk5b GND POW P2G P2G P2F P2F P1G P1G P1F P1F C54 C49 C49 C34 C307 C30 313 311
  258 257;
  C_10 bk5a GND POW P2G P2F P2F P1G P1G P1F C54 C34 C30 234 222;
  C_11 bk4 GND POW P2G P2G P2F P2F P1G P1G P1F P1F P14 P13 P12 DIR C36A 226 222 219;
  C_12 bk3 P2G P2G P2F P2F P1G P1G P1F P1F P16 P15 GND POW C36A 331 226 10;
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  C_13 bk21 GND POW P3 P2G P2G P2F P2F P1G P1G P1F P1F;
  C_14 bk20 GND POW P2G P2G P2F P2F P24 P1G P1F P1F 88 46 170 157 156 154 126 123 116;
  C_15 bk2 GND POW P2G P2G P2F P2F P28 P1G P1G P1F P1F C34 234;
  C_16 bk19 GND POW P35 P34 P33 P32 115 114 112 111 110 109;
  C_17 bk18 GND POW P37 P36 P2G P2G P2F P2F P1G P1G P1F P1F 170 159 158 126 116;
  C_18 bk17b GND POW P2G P2F P2F P1G P1F P1F DIR 7 371 170 116;
  C_19 bk17a GND POW P2G P2G P2F P2F P1G P1G P1F P1F 159 158 157 156 154 126 123 116;
  C_20 bk16 GND POW P2G P2G 88 87 86 85 84 83 7 55 53 51 50 25 115 114;
  C_21 bk15b GND POW P9 P8 P2G P2G P25 P1G P1G P11 P10 44 25 22;
  C_22 bk15a GND POW P7 P6 P5 P2G P2G P1G 44 29 10;
  C_23 bk14c GND POW P2G P2G P1G P1G 53 43 42 22;
  C_24 bk14b GND POW P2G P2G P2F P2F P1G P1G P1F P1F 51 50 46 43 42 38;
  C_25 bk14a GND POW P2G P2G P1G P1G 38 29;
  C_26 bk13 GND POW P4 P2G P2F P2F P26 P2 P1G P1F P1F;
  C_27 bk12 GND POW P2G P2G P2F P1G P1G P1F 46;
  C_28 bk11 GND POW P31 P2G P2G P2F P2F P1G P1G P1F P1F 46;
  C_29 bk10c GND POW P2G P2G P2F P2F P1G P1F P1F C74 282 198;
  C_30 bk10b P2G GND P2G P2F P2F P1G P1G P1F P1F C74 46 POW 46 280 273 273;
  C_31 bk10a GND POW P2G P2G P2F P2F P29 P1G P1G P1F P1F 379 284 282 280 273;
  C_32 bk1 GND POW P2G P2G P2F P2F P1G P1G P1F P1F C307 313 311;
 ENDNETWORK;
ENDMODULE;
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