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UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND APPLIED SCIENCE

School of Electronics and Computer Science

Development of High Yield Fabrication Technology
for Graphene Quantum Dots for Single Electron
Transistor applications

by

Nima Kalhor

Thesis for the degree of Doctor of Philosophy

August 2014

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ABSTRACT

FACULTY OF ENGINEERING AND APPLIED SCIENCE

School of Electronics and Computer Science

Doctor of Philosophy

DEVELOPMENT OF HIGH YIELD FABRICATION TECHNOLOGY FOR GRAPHENE
QUANTUM DOTS FOR SINGLE ELECTRON TRANSISTOR APPLICATIONS

by Nima Kalhor

Since the seminal work by Loss and DiVincenzo, quantum dots (QDs) have been extensively studied as building blocks for quantum information processing (QIP). Presently, the most advanced implementations of QD qubits are realised in III/V heterostructures (GaAs/AlGaAs). However, the strong spin-orbit and hyperfine interactions in these compounds pose fundamental limits to the spin coherence time, and so stimulating the search for alternative host materials.

Graphene, a two-dimensional single atomic layer of carbon atoms, was successfully produced for the first time in 2004. Despite its short history, its unique material properties have ensured a rapid growth of interest in several areas of science and technology. Spin-orbit coupling and hyperfine interaction with carbon nuclei are both small in graphene, and a very long spin relaxation length has been demonstrated, which make graphene a promising candidate for quantum information technology and spin qubit embodiment.

Superior transport properties of graphene encourage the downscaling of graphene devices to the regime where coherent nature of electronic and spin states can be fully exploited. This requires the development of ultrafine patterning technologies which enables accurate nanoscale fabrication beyond the present electron-beam lithography technique. Therefore, inspired by the on-going trend towards device miniaturization, we present a novel hybrid fabrication method for graphene nano devices (e.g. graphene QDs devices) with minimum feature sizes of ~ 3 nm (i.e. the gap between the graphene side-gates and channel). Here, for the first time we combine

conventional e-beam lithography and direct milling with the sub-nm focused helium ion beam generated by a helium ion microscope to fabricate high resolution graphene QDs devices, reliably and reproducibly. The highly controllable, fine scale fabrication capabilities offered by this approach could lead to a more detailed understanding of the electrical characteristics of graphene quantum devices and pave the way towards room-temperature operable graphene quantum dot devices.

Furthermore, we demonstrate successful fabrication of graphene QDs devices by means of e-beam lithography and RIE etch for the first time at Southampton Nanofabrication Centre. The electrical characterisations of the final fabricated devices at room temperature and cryogenic temperatures confirmed successful fabrication of graphene QDs devices, and so resulted in observation of Coulomb diamonds at ~ 6 Kelvin. The accurate optimisation of our fabrication process resulted in $\sim 80\%$ fabrication yield (from 57 fabricated devices) for graphene samples produced by mechanical exfoliation and $\sim 58\%$ fabrication yield (from 160 fabricated devices) for CVD graphene samples. These values represent the percentage of fabricated QDs devices which had to exhibit ambipolar behaviour, no observable current leakage from the channel, no observable current leakage between in-plane graphene side-gates, and no observable back gate leakage through the SiO_2/Si substrate.

Contents

1	Introduction	1
1.1	Quantum information technology.....	1
1.2	Graphene	2
1.3	Helium ion microscopy	4
1.4	Research motivations and contributions	5
1.5	Thesis overview	6
2	Graphene	10
2.1	Introduction.....	10
2.2	Atomic structure and carrier transport properties of graphene	11
2.3	Graphene production methods	15
2.3.1	Mechanical exfoliation	16
2.3.2	Epitaxial growth on SiC single crystal	16
2.3.3	Chemical vapour deposition (CVD)	16
2.4	Identifying graphene flakes.....	17
2.4.1	Optical microscopy	17
2.4.2	Atomic force microscopy	18
2.4.3	Raman spectroscopy	18
3	Single Electron Transistors with Quantum Dot	21
3.1	Single Electron Transistors (SETs).....	21
3.2	Single electron transistors with quantum dot	23
3.2.1	Coulomb blockade (CB)	24
3.2.2	Carrier transport in single electron transistors	26
3.2.3	Single electron transistors with double quantum dot (DQD)	29

3.3	An experimental review on graphene nano devices.....	37
3.3.1	Graphene nanoribbons.....	37
3.3.2	Graphene quantum dots devices.....	41
4	Fabrication of extremely downscaled graphene QDs by helium-ion beam milling.....	50
4.1	Introduction.....	51
4.2	Helium-ion microscopy	55
4.3	An experimental review on nanofabrication by HIM milling.....	59
4.3.1	Plasmonic nano devices.....	59
4.3.2	Graphene nano devices.....	60
4.3.3	Other applications.....	65
4.4	Fabrication of GDQD by HIM milling.....	66
4.4.1	Sample preparation.....	66
4.4.2	Setting-up a He-ion beam.....	67
4.4.3	HIM milling on pristine graphene samples.....	68
4.4.4	HIM milling on e-beam processed graphene samples.....	74
4.5	Challenges and issues associated with He-ion milling	80
4.6	Electrical characterisations and analysis.....	83
4.7	Conclusions.....	91
5	Fabrication of GQDs devices by electron-beam lithography and RIE etch.....	93
5.1	Introduction.....	93
5.2	Substrate preparation.....	95
5.3	Mechanical exfoliation of graphene	98
5.4	Patterning of graphene by e-beam lithography and RIE etch	103

5.5	Fabrication of metal contacts onto graphene samples	112
5.6	Issues associated with the EBL and RIE process	117
5.6.1	Impact of the bulk graphite pieces	117
5.6.2	Impact of metal contacts in the EBL process	118
5.7	Conclusions.....	119
6	Electrical characterisations and analysis of EBL/RIE fabricated GQDs devices	120
6.1	Room temperature characterisation	121
6.2	Cryogenic temperature characterisation.....	125
6.2.1	DQD devices fabricated in CVD grown graphene samples	127
6.2.2	QD devices fabricated in mechanically exfoliated graphene samples	140
6.3	Design and dynamic simulation of the fabricated GDQD devices by the EBL/RIE process..	147
6.3.1	Device design and capacitance simulation methodology	147
6.3.2	Equivalent circuit and device simulation methodology	151
6.4	Conclusions.....	158
7	Conclusions and future work	160
7.1	Conclusions.....	160
7.2	Future works	163
7.2.1	EBL/RIE fabrication method	163
7.2.2	HIM milling fabrication method	164
	Appendix A	167
	Appendix B	170
	Appendix C	173
	References	181

Declaration of Authorship

I, Author, declare that the thesis entitled ‘Thesis Title’, and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research.

I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
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- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as shown in the List of Publications that follows.

Signed:.....

Date:.....

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Chapter 1

Introduction

1.1 Quantum information technology

Since 1948, when the transistor was invented by J. Bardeen, W. Brattain and W. Shockley [1], many studies and experiments have focused to miniaturize these devices. The motivations for device miniaturization can be expressed as:

- I) The miniaturized devices have lower capacitances and shorter interconnects and yield to faster systems;
- II) Reducing the volume of transistors allows for lower power dissipation;
- III) The costs drop by more devices on chip sizes.

The quest for device miniaturization is governed by Moore's Law. This law states that the number of transistors that can be placed on integrated circuits doubles every two years [2].

Although owing to new fabrication technologies, presently, MOSFETs with 10 nm gate length can be fabricated [3], [4] but factors such as source to drain tunnelling and dopant fluctuations are setting the limits for device miniaturization [2]. Therefore, there is an intense on-going search for new device principles that not only allow for the scaling limits to be pushed even further but also make use of the quantized nature of the charge carriers evident in small device structures (i.e. 'Beyond CMOS' domain).

Single-Electron Transistors as one of the new device principles in ‘Beyond CMOS’ domain was first proposed in 1985. Averin and Likharev, at the University of Moscow, proposed the idea of a new type of transistor with three terminals called a Single-Electron tunnelling Transistor (SET). The potentials of the single electron concept are rather breath-taking and have made these devices a very hot topic in electronics. In contrast with field-effect transistors, single-electron devices are operating based on an intrinsically quantum phenomenon called the tunnel effect. The most fascinating property of single electron transistors is the possibility to switch the device by adding one electron to the gate electrode, whereas a common MOSFET needs about 1000-10,000 electrons. Downscaling of the island region of a SET (and so artificial confinement of electrons) results in a zero-dimensional electron system, commonly known as a Quantum Dot (QD).

Since the seminal work by Loss and DiVincenzo [5], quantum dots have been extensively studied as building blocks for quantum information processing (QIP). Because electron spin is a two level system (spin $|\uparrow\rangle$ or $|\downarrow\rangle$), it has become a popular candidate for realization of a qubit (a quantum bit) in quantum dots devices. Presently, the most advanced implementations of QD qubits are realised in III/V heterostructures (GaAs/AlGaAs) [6]–[8]. However, the strong spin-orbit and hyperfine interactions in these compounds pose fundamental limits to the spin coherence time, and so stimulating the search for alternative host materials.

1.2 Graphene

Recent discoveries of two-dimensional materials, such as graphene, have made a great impact in present science and technology.

Graphene, a two-dimensional single atomic layer of carbon atoms, was successfully produced for the first time in 2004. Despite the short history of graphene, its unique material properties have ensured a rapid growth of interest in several areas of science and technology. Its impact was recently highlighted by the 2010 Nobel prize for Kostya Novoselov and Andrea Geim for their ground breaking studies on graphene. Furthermore, huge investments by different

governments (e.g. British government) and particularly the US department of defence, signify the importance of graphene in the future of science and technology.

Although the future of graphene is still far behind the horizon which we cannot assess but, as the Si-based technology is reaching fundamental limits, graphene could be a promising material to take over. Experimental results have shown that graphene has a remarkably high electron mobility at room temperature (and in excess of $200,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at low temperatures [9]) which could pave the way for fabrication of room-temperature ballistic transistors. Unfortunately, the absence of a band gap and $4e^2/h$ minimum conductivity even at nominally zero carrier densities [10] prevent a graphene FET device to fully “gate” and limit the on-off ratio.

As mentioned, spin-orbit and hyperfine interactions in materials are two main mechanisms that pose fundamental limits in spin coherence time. This stimulates the search for host materials with smaller spin-orbit and hyperfine interactions for QIP. Graphene is considered as an exotic material for fabrication of quantum dots devices and spin qubit embodiment [10], [11] and a very long spin relaxation length has been demonstrated [12], [13]. That is due to (i) the absence of hyperfine interaction as carbon materials consist predominantly of the nuclear spin free ^{12}C isotope (99%) and, (ii) extremely weak spin-orbit coupling as the carbon nuclei is light [10], [12], [13]. In spin-orbit coupling (a relativistic effect), the electric field experienced by an electron is equivalent to $+Z|e|$ where Z is the atomic number of the host material [14], [15]. Therefore, spin-orbit coupling is weak for light materials [16]. The strength of intrinsic spin-orbit interaction in graphene, induced by the intra-atomic Coulomb potential, is estimated to be a very small energy of $\lesssim 24 \mu\text{eV}$ due to the small atomic number $Z = 6$ of carbon [17], [18]. However, in GaAs (the host material of the most advanced implementations of QD qubits so far [6]–[8]), the spin-orbit interaction (i.e. the Dresselhaus spin-orbit coupling) is significantly stronger (0.341 meV [19]) and dominates spin relaxation [20], [21]. These values provide a suitable comparison between these two host materials, and so suggesting graphene as an excellent material for realisation of spin qubits [10].

An interesting novel proposal for a graphene device with spin function is spin-based logic circuits which are expected to offer high-speed operation at low power dissipation [22]. Recently, graphene drums (i.e. graphene mechanical resonators) have been suggested to have

great potential as quantum memory chips in future quantum computers [23], [24]. It has been also demonstrated that under extremely powerful magnetic fields and at low temperatures graphene can effectively filter electrons according to the direction of their spin, resulting in an unusual conduction along the edge (virtually a one-dimensional wire) which can be used as a building block for realising novel quantum circuits [25], [26].

These superior transport properties encourage the downscaling of graphene devices further to the regime where the coherent nature of electronic and spin states can be fully exploited. However, this requires the development of ultrafine patterning technologies which enables accurate nanoscale fabrication beyond the present electron-beam lithography technique.

For research and prototyping, electron beam lithography (EBL) is the most established lithography method for fabrication of nano devices. Despite all the developments (e.g. 100 keV acceleration voltage), which have made EBL with sub-10 nm resolution in resist possible, the electron-resist interactions along with the resist development are limiting the resolution of this technique [27]. This stimulates the search for alternative high resolution patterning techniques.

1.3 Helium ion microscopy

In 2007, Carl Zeiss SMT introduced Helium-Ion Microscopy (HIM) as a new surface imaging technique [28]–[32]. It involves scanning a focused beam of helium ions across a surface to generate an image from the resulting secondary electron (SE) emission. An atomically sharp and extremely bright source, combined with the larger momentum (and so smaller de Broglie wavelength) of helium ions compared to electrons, enables a sub-nanometre probe size at the sample surface. Additionally, He ions produce far fewer collision cascades (and so low amount of beam divergence) in the first ~ 100 nm of entering the substrate. This results in a small interaction volume and so high resolution imaging routinely below 1 nm (edge resolution) and, with the latest versions of the tool, below 0.35 nm [33]–[35].

Helium ion microscopy was primarily developed and introduced as an ultra-high resolution imaging technology, with unique contrast mechanisms and imaging abilities. However, as it

produces an intense focused beam of He-ions, it is also capable of patterning (milling and lithography) and sputtering that are more commonly associated with a conventional Ga-ion beam. Therefore, shortly after its introduction, it was recognised as potential patterning tool for fabrication of state-of-the-art nano devices which, it has already made an exhilarating impact on fabrication of plasmonic nano devices [36]–[38].

However, it is worth mentioning that graphene samples are very susceptible to beam irradiations [39]–[44]. For instance, He-ion beam irradiation results in creation of defects (i.e. modification of the atomic lattice) and degradation of the electronic properties of graphene samples [39]. Hence, extra care is required to avoid/minimise beam irradiation damage on graphene samples during imaging.

1.4 Research motivations and contributions

In this work we aim to develop and demonstrate successful fabrication of graphene nano devices for the first time at Southampton Nanofabrication Centre (SNC). This is demonstrated by means of e-beam lithography followed by reactive-ion-etch (RIE) which is employed to fabricate single electron transistors with quantum dots devices with a better pattern resolution than that of demonstrated in majority of other reported works. The capability and high yield of our process is highlighted by successful fabrication of arrays of quantum dots devices on CVD graphene samples.

Although currently EBL/RIE method is the most established method for fabricating graphene devices but, we argue that the parameters such as e-beam spot size, proximity effect and undercutting of the resist layer during etching can limit the resolution of this technique. Furthermore, uneven thickness of the resist layer, which may be caused by the presence of graphite pieces and metallic alignment marks, can also limit resolution and affect the symmetry of the patterns fabricated by this method.

Therefore, inspired by the on-going trend towards device miniaturization, we present a novel hybrid fabrication method for graphene nano devices (e.g. graphene QDs devices) with

minimum feature sizes of ~ 3 nm (i.e. the gap between the side-gates and channel) and high yield. Here, for the first time, we combine conventional e-beam lithography and direct milling with the sub-nm focused helium ion beam generated by a helium ion microscope to fabricate high resolution graphene QDs devices, reliably and reproducibly. The highly controllable, fine scale fabrication capabilities offered by this approach could lead to a more detailed understanding of the electrical characteristics of graphene quantum devices and pave the way towards room-temperature operable graphene quantum dot devices.

The final fabricated devices by both fabrication methods are then electrically characterised at room temperature and cryogenic temperatures (only for EBL/RIE devices) to confirm successful fabrication of the desired devices. The cryogenic temperature measurements were conducted to verify the ability to control single electron tunnelling in the fabricated devices, and so observing Coulomb diamonds.

1.5 Thesis overview

This thesis consists of 7 chapters.

Chapter 2 introduces graphene and presents a brief review on some of its remarkable properties related to this work. This includes a discussion of graphene's atomic structure, electronic properties, production and identification methods.

Chapter 3 provides an extensive study on the operation of single electron transistors (SETs) with quantum dots (QDs) devices as building blocks for quantum information technology. The electron transport via Coulomb Blockade (CB), observation of Coulomb diamond and stability diagram are explained in detail. Furthermore, an experimental review on the behaviour of graphene quantum dots devices through a literature review, which highlights the most important experimental methods relevant to our work, is given.

Chapter 4 begins by highlighting the limitations of the EBL/RIE fabrication process and introducing helium ion microscopy (HIM) as an ultra-high resolution imaging tool. In addition, we discuss the capability of HIM milling for nanofabrication through a literature review which highlights the most interesting recent experimental works. We then propose our novel hybrid

fabrication method for extremely downscaled graphene quantum dots devices by combining conventional e-beam lithography and direct milling with a sub-nm focused helium ion beam for the first time. The helium ion milling is used to pattern graphene flakes with intricate QD devices, with sub-10 nm resolution and high fidelity. We established this novel fabrication approach for the first time and extensive effort was employed to overcome number of challenges, such as the He-ion beam drift during milling which can jeopardise pattern fidelity for long exposure times. To obtain the desired high resolution HIM milling, we suggest an annealing process in H_2/N_2 gas flow to remove the contamination produced during the e-beam lithography steps on the surface of the graphene samples. Furthermore, we highlight the limitations associated with this fabrication method. The chapter is then finalised by discussing the electrical measurements collected from the final fabricated devices. The electrical characterisation of the final device demonstrates the successful fabrication of the first electrically characterised He-ion beam patterned graphene device, which we published as a journal paper. Our novel approach could pave the way to a better understanding and more detail study of graphene quantum devices.

Chapter 5 explains our fabrication process for graphene QD devices by means of conventional e-beam lithography followed by RIE etch (i.e. EBL/RIE process). Our fabrication process, which can be also employed to fabricate variety of graphene nano devices, was developed and established for the first time at Southampton Nanofabrication Centre. All the steps involved in the fabrication process are explained systematically in great detail in order to pave the way for future graphene projects in Southampton Nano Group. To minimise e-beam induced damage on our graphene samples during e-beam lithography, we employ a single layer of *Methyl Methacrylate* (MMA) resist for the first time as a radical method for fabrication of metal contacts onto graphene devices. The high electron beam sensitivity of MMA resist allows the use of a dramatically lower e-beam dose to that of required for a bilayer resist layer (and so less beam induced damage onto the graphene samples) which, using our optimised process, also ensures consistent and successful lift-off outcome with minimum feature size of ~ 150 nm. This was achieved by simultaneous tuning of the resist thickness (i.e. MMA), e-beam lithography process, metal deposition conditions (i.e. metal deposition at a rate of $0.5 \text{ \AA}/\text{second}$), thickness of the deposited metal layer (i.e. Ti/Au 5 nm/ 60 nm), and performing the lift-off process in

warm *N-Methyl-2-Pyrrolidone* (NMP). Furthermore, we conclude this chapter by highlighting issues and limitations associated with the EBL/RIE fabrication process.

Chapter 6 concentrates on the electrical characterisations of the fabricated graphene quantum dot devices by our EBL/RIE process. Two different types of devices are discussed in this chapter. These are graphene double quantum dot (DQD) devices fabricated on CVD grown monolayer graphene samples and a GQD device fabricated on a mechanically exfoliated monolayer graphene sample. To our best of knowledge, this is the first attempt and demonstration ever of high-density arrays of graphene QD devices on CVD graphene. Also, our successful demonstration of fabrication of high-density arrays of QD devices on CVD graphene with high reproducibility highlights the versatility of our fabrication process with its well-optimised steps. The electrical characteristics of the devices are discussed at room temperature as well as cryogenic temperature (i.e. ~ 6 K). Room temperature measurements are used to justify the successful development of our EBL/RIE process and to calculate the statistical yield of our process. We estimated an $\sim 80\%$ statistical yield from 57 fabricated devices on graphene samples produced by mechanical exfoliation and $\sim 58\%$ from 160 fabricated devices on CVD graphene samples. These values represent the percentage of fabricated QDs devices which had to exhibit ambipolar behaviour, no observable current leakage from the channel, no observable current leakage between in-plane graphene side-gates, and no observable back gate leakage through the SiO_2/Si substrate. We attributed the lower fabrication yield on CVD graphene samples to the quality and consistency of the flakes. Cryogenic temperature measurements resulted in observation of complex and dense Coulomb diamond arrangements in the collected $V_{DS} - V_{BG} - I_{DS}$ plots, particularly for the devices fabricated on CVD graphene samples. We discuss these observations in detail and attribute them to formation of unintentional QDs along the etched patterns in graphene during RIE process and existence of grain boundaries in CVD graphene. Furthermore, to determine the feasibility of our DQD device design for single electron tunnelling behaviour (i.e. Coulomb blockade), we present a simulation study by means of COMSOL Multiphysics and Monte Carlo single electron circuit simulations (SETSPICE) to discuss the electrical behaviour of these devices in more detail.

Chapter 7 concludes this thesis by presenting a summary of our findings, including our extensive work in successful development of two fabrication methods for graphene nano devices. In addition, we introduce number of interesting future directions for this work.

Chapter 2

Graphene

Carbon-based materials play a major role in present science and technology. Graphene, a two-dimensional (2D) single atomic layer of graphite, had been initially predicted theoretically more than 60 years ago [45]. However, it was only about a decade ago that, using a scotch tape, scientists managed to discover a monolayer graphene sheet experimentally [46]. Despite its short history, its unique material features have ensured a rapid growth of interest in several areas of science and technology. In this chapter, we present a literature review on number of remarkable properties of graphene.

2.1 Introduction

Graphene was discovered by Andre Geim and Konstantin Novoselov in 2004 [46]. Graphene is an sp^2 bonded network of carbon atoms arranged in a shape of honeycomb lattice. It was initially produced by repeatedly peeling away graphite layers with a scotch tape to isolate a single atomic layer of carbon atoms [46]. It can be wrapped up into a zero dimensional fullerenes, rolled into one dimensional nanotubes or stacked into three dimensional graphite (Figure 2.1) [10]. Furthermore, charge carriers can travel thousands of interatomic distances without scattering.

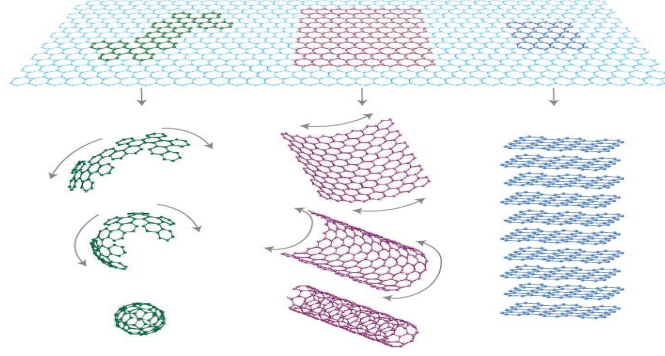


Figure 2.1 – Graphene is a two-dimensional single atomic layer of graphite but yet, it can be shaped into a zero, one and three-dimensional structure. Figure from ref. [10].

2.2 Atomic structure and carrier transport properties of graphene

A monolayer graphene flake consists of sp^2 carbon hexagonal networks and is characterized by two types of C-C bonds (σ , π). The carbon-carbon bond distance a_{C-C} in graphene is 1.42 Å. The strong three σ bonds connect a C atom to its three neighbouring atoms, resulting in optical-phonon frequencies much higher than observed in diamond [47]. The electronic characteristics of graphene is determined by the bonding π and antibonding π^* orbitals that construct wide electric valence and conduction bands. The schematic illustration of the carbon valence orbitals in graphene is shown in Figure 2.2(a). The bonding and the antibonding σ bands are separated by a large energy gap of ~12 eV, whereas the bonding and antibonding π bands lay in the vicinity of the Fermi level (E_F) (Figure 2.2(b)). Hence, to predict the electronic properties of graphene around the Fermi energy the σ bands are usually neglected. Theoretical calculations demonstrated that in graphite, the π band overlap fades away as the layers are further separated over their equilibrium distance, resulting in decoupled graphene layers. Because of this, graphene can be described as a zero-gap semiconductor [47], [48].

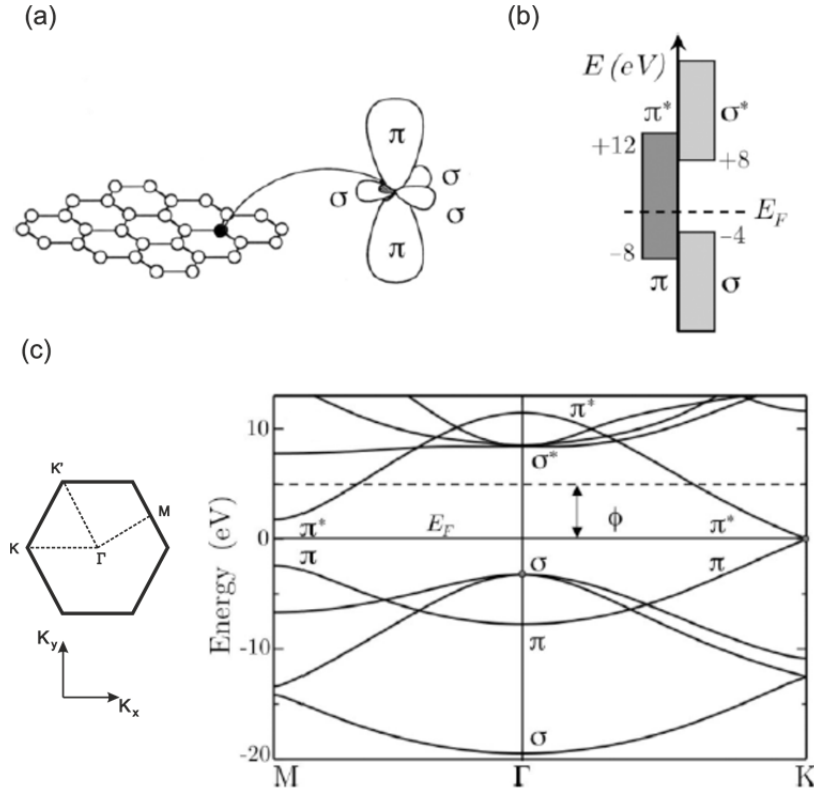


Figure 2.2 – (a) The schematic illustration of the carbon honeycomb network and the valence orbitals in a graphene sheet that is constructed from four valence orbitals, i.e. three in-plane σ orbitals and an π orbital perpendicular to the sheet. (b) The energy diagram of σ and π bonds. The σ and σ^* bonds have a large energy gap but π and π^* lie in the vicinity of Fermi level. (c) The dispersion relation of the electronic band structure at three high symmetry points within the first Brillouin zone of a monolayer graphene sheet. K_x and K_y correspond to the reciprocal space coordinate axes. Γ point is at the zone centre. M point is in the middle of the hexagonal side. K and K' points are at the corners of the hexagon cell. Note that ϕ is the work function. Figure from ref. [47].

The dispersion relation of the electronic band structure at three high symmetry points within the first Brillouin zone of a monolayer graphene sheet is shown in Figure 2.2(c). The dispersion relation reveals a large energy gap that separates the bonding σ and the antibonding σ^* bands. At the K and K' points, the bonding π (highest valence band) and the antibonding π^* (lowest conduction band) bands touch. In a typical band-gap diagram of neutral graphene, the filled valence band and the empty conduction band are drawn as two cones that meet at their apex at a point known as Dirac crossing (Figure 2.3) [10]. This is due to the linear slope of the π

band electronic dispersion curve near the corners of the Brillouin zone (e.g. K point) that can be observed in Figure 2.2(c). Hence, at low energies E near the Dirac crossing points, charge carriers mimic relativistic particles (known as massless Dirac fermions) that allows them to travel at an effective speed of light ($v \sim 10^6$ m/s) [10], [49].

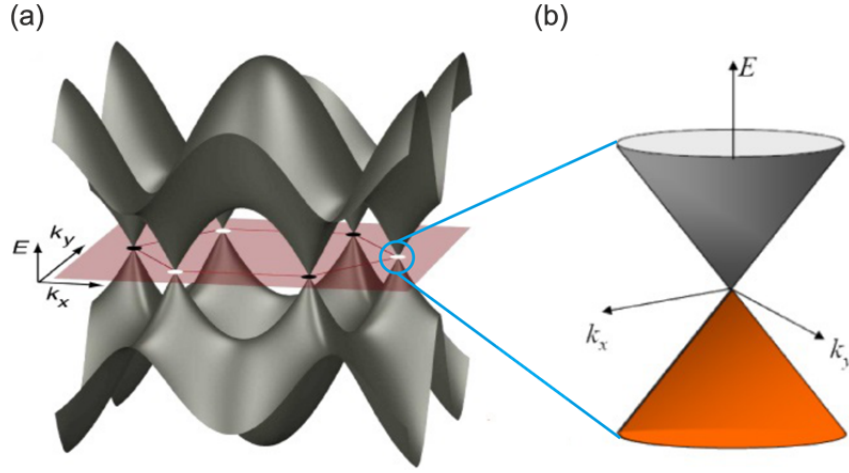


Figure 2.3 – (a) The Dirac crossing points at the corners of the first Brillouin zone (e.g. K point) in a graphene sheet. (b) A magnified area of the linear energy band at a Dirac crossing point, i.e. a Dirac cone. A modified figure from ref. [50].

One of many interesting electrical properties of graphene is its ambipolar electric field effect, shown in Figure 2.4(a). That is, charge carriers can be tuned continuously between electrons and holes under a varying gate voltage in concentrations ($n = \alpha V_g$, where $\alpha = 7.2 \times 10^{10} \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for graphene FET devices fabricated on a 300 nm-thick layer of SiO_2) as high as 10^{13} cm^{-2} , with their mobilities weakly dependent on temperature and can exceed $15,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ even under ambient conditions [10].

Weak carrier scattering is one of the most notable properties of graphene. Since graphene is a nearly perfect crystal and free of structural defects, it is suggested that scattering of charge carriers in graphene is mainly due to extrinsic sources [9], [10].

Carrier scattering mechanisms in graphene can be divided into two categories:

I) Intrinsic scattering mechanisms that arise from structural imperfections in graphene lattice, e.g. defect sites in the lattice, edge scattering, grain boundaries and phonon scattering [51]. Structural imperfections (i.e. intrinsic scattering) result in either a change in the local electronic structure or an injection of charges to the lattice, which in fact depends highly on graphene synthesis methods. That is, in exfoliated graphene samples, due to their high crystalline order, intrinsic defect density was found to be less than 10^{10} cm^{-2} [9]. However, for graphene samples produced by chemical vapour deposition (CVD) or by epitaxial growth on SiC, graphene exhibits multiple nucleation sites which in turn increase defect density [52], [53]. Furthermore, carrier scattering at the edges of a graphene ribbon (known as edge scattering) results in a size-dependent thermal conductivity [54] and degradation in carrier mobility [55], [56]. That is, carriers in graphene ribbons experience diffusive scattering (i.e. carriers scatter at rough edges with a loss in momentum) at the edges rather than specular scattering (i.e. carriers scatter at smooth edges without any loss in momentum in their direction of propagation). In fact, the effect of edge scattering in graphene ribbons can intensify after patterning/etching of graphene flakes due to increase in edge roughness. Edge roughness results in mixing of edge states which elevates semiconducting states and suppresses metallic states [57]. Therefore, improving current patterning methods to fabricate graphene devices with smoother edges, and so minimising the impact of edge roughness, is essential [58].

II) Extrinsic scattering mechanisms that arise from neighbouring materials, e.g. charged impurities on/under graphene and residues/contaminations produced by processing graphene [59], [60], defects in the underlying substrate and surface charge traps on substrates surface [9], [61]–[63], substrate stabilized ripples [64]–[66], interfacial phonons [9], [61]. It is worth mentioning that annealing graphene samples at elevated temperatures has been proposed as an effective method to remove surface contaminants resided/absorbed on graphene surface [64]. By suspending a graphene flake over a SiO_2/Si substrate (so minimising the substrate effects), as shown in Figure 2.4(b), and a current annealing at $\sim 130^\circ\text{C}$ in vacuum (so removing residues/contaminants on the suspended graphene flake) prior to the electrical characterisations, Bolotin *et al.* [9] recorded a mobility of $\sim 230,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at electron densities of $\sim 2 \times 10^{11} \text{ cm}^{-2}$ at $\sim 5 \text{ K}$.

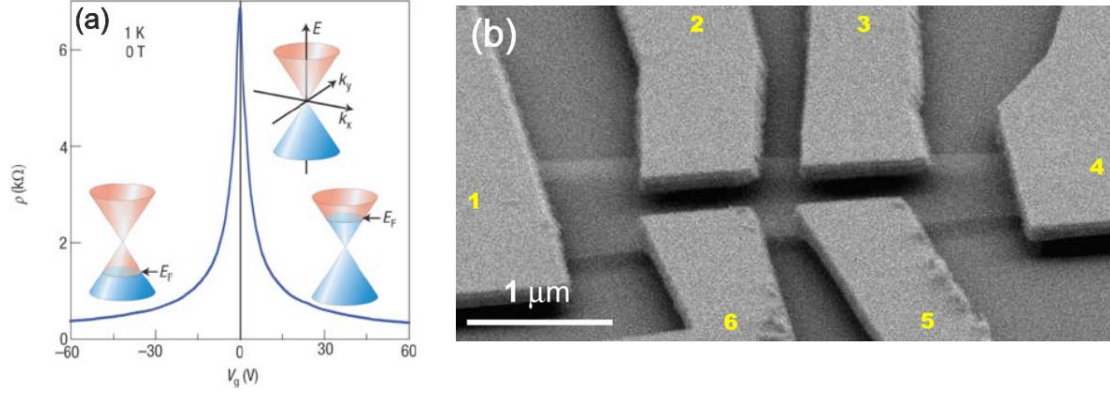


Figure 2.4 – (a) Ambipolar electric field effect in monolayer graphene, i.e. varying V_g tunes electrons and holes concentration in the flake. In addition, the figure shows the changes in the position of the E_F with changing of V_g . Figure from ref. [10]. (b) SEM image of a suspended graphene device with six probes, taken at 15° angle. Figure from ref. [9].

Another interesting electronic behaviour of graphene is its theoretical minimum conductivity of $\sigma_{min} = 4e^2/h\pi$ [10]. This means that it is impossible to fully “gate” a graphene FET device and the device will always exhibit a non-zero current flow even when tuned at the Dirac point (i.e. where concentration of charge carriers approaches zero). Furthermore, unlike all other materials in which such a low σ eventually results in metal-insulator transition at low temperatures, no sign of such transition has been seen for graphene. However, the experimental obtained values of σ_{min} are π times smaller than the theoretical value, i.e. $\sigma_{min} = 4e^2/h$, which different explanations have been reported regarding this discrepancy, e.g. charged-impurity scattering [67], electron-hole puddles around the charge neutrality point [10], [68], aspect ratio of the samples [69].

2.3 Graphene production methods

Large-scale (wafer-scale) production of high quality graphene sheets remains a challenge in the commercial-level manufacturability of graphene-based devices. In this section, we address the three most established production methods for graphene samples.

2.3.1 Mechanical exfoliation

This simple method, also known as scotch-tape technique, was discovered to produce monolayer graphene flakes for the first time [46]. As we will discuss in detail in section 5.3 of this report, this is also the method that we employed to produce our graphene samples. The method includes peeling away graphite layers with an adhesive tape. A piece of graphite consists of many graphene layers that are stacked and kept together by Van Der Waals force. Due to an inter-layer Van der Waals interaction energy of ~ 2 eV/nm², the magnitude of the force needed to exfoliate graphite is about 300 nN/ μm^2 . This very weak force can be easily applied to a piece of graphite with an adhesive tape. Despite the simplicity of the method, so far, the produced graphene samples have shown the highest electrical and structural quality compared to any other method. However, the produced flakes are limited in size (typically, a few micrometres) and not suitable for large-scale production.

2.3.2 Epitaxial growth on SiC single crystal

In this approach, graphene is produced from a silicon carbide (SiC) substrate. That is, silicon atoms are thermally desorbed from the surface layers at temperatures between 1250-1450 °C in an ultra-high vacuum chamber [70], [71]. A very recent work by Baringhaus *et al.* [72] reported epitaxial grown graphene nanoribbons with sheet resistances below 1 Ω /square, and so surpassing theoretical predictions for perfect graphene.

However, the major disadvantages of this method are (i) the high processing temperatures and (ii) the high cost of SiC wafers.

2.3.3 Chemical vapour deposition (CVD)

In this method, carbon atoms are grown onto a metal film (e.g. nickel, ruthenium, iridium, or copper) in an argon/methane/hydrogen gas mixture at different temperatures. The deposited graphene films are then transferred onto a desired substrate after etching the metal film layer. The process is fast but, CVD graphene is poly-crystalline and is not as pristine as mechanically

exfoliated flakes [73]. Furthermore, the transfer process may cause wrinkles in a grown graphene flake and leave organic residues/contaminants on the sample.

However, very recently, Samsung Co. reported uniform wafer-scale growth of single-crystal monolayer graphene sheets on germanium [74].

2.4 Identifying graphene flakes

The growing interest in remarkable properties of graphene asks for a reliable and appealing method to identify and characterise produced graphene samples. That is, the characterisation method must be quick, non-destructive and with high resolution. In this section, we address three main methods of identifying graphene flakes.

2.4.1 Optical microscopy

This was the method that helped scientists to discover monolayer graphene flakes for the first time [46], [75]. However, monolayer graphene flakes cannot be observed under an optical microscope, equipped with a white-light illumination, on most substrates. They only become visible when transferred onto a Si substrate with an accurately tuned thickness of an oxide layer, i.e. 90 or 300 nm SiO_2 . That is, at those oxide thicknesses, even a monolayer flake adds to the optical path of the reflected light, and so producing a feeble interference-like contrast compared to an empty substrate [10], [76], [77]. The thickness of the SiO_2 layer is a crucial factor to identify thin graphene flakes with this method successfully. For instance, even a 5% difference in the SiO_2 thickness can make a monolayer graphene completely invisible [10]. However, the major drawback of this method is the fact that the obtained images do not offer any useful information regarding the structural properties of graphene.

It is worth mentioning that graphene flakes were recently observed on other oxide layers too, i.e. Al_2O_3 [78] and HfO_2 [79].

2.4.2 Atomic force microscopy

Atomic force microscopy (AFM) is another technique that is employed to identify single and few layers graphene flakes [46], [75]. Because of its high imaging resolution, it can also be used as an imaging tool for etched patterns into graphene flakes [80]–[83]. However, its throughput is low and it can be destructive to the samples. Moreover, if graphene flakes contain folds or wrinkles, the accuracy of this technique limits only to distinguish between monolayer and bilayer flakes [76].

2.4.3 Raman spectroscopy

This technique is considered as the best way to characterise structural properties of produced graphene flakes with high accuracy that also offers high-throughput and is non-destructive to the samples [76].

The predominant mode of light scattering when it encounters atoms or molecules is elastic scattering, known as Rayleigh scattering. In this case, the scattered photons have the same energy (frequency) and wavelength as the incident photons. However, it is possible that a small fraction of the incident photons to interact with atoms in a fashion that energy is gained or lost. Consequently, the scattered photons are shifted in frequency and usually have lower frequencies than the incident photons. This inelastic scattering is called Raman scattering [84], [85]. The Raman spectra of all carbon materials show common features in the 1000-3000 cm^{-1} region. Figure 2.5(a) illustrates the main features (peaks) of Raman spectrum of a graphene flake.

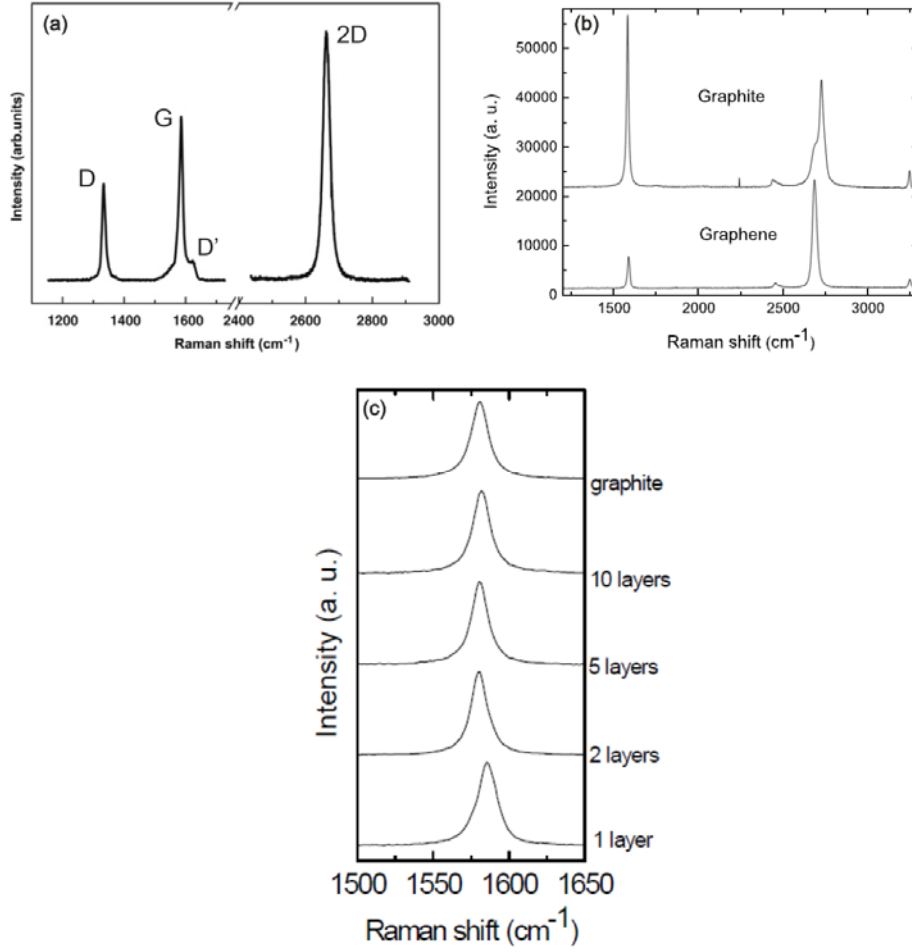


Figure 2.5 – (a) The main features (peaks) in Raman spectrum of graphene, with $E_{laser} = 2.41$ eV. Modified figure from ref. [86]. (b) Comparison of Raman spectra for bulk graphite and graphene at a 532 nm wavelength laser. Figures from ref. [76]. (c) Slight upshift in the position of the G peak by ~ 5 cm⁻¹ with the number of graphene layers. Figure from ref. [87].

The G peak (at ~ 1580 cm⁻¹ [88]) and the 2D (at ~ 2676 cm⁻¹ [88]) peak are the most important features in Raman spectrum of graphene. In the first-order Raman spectrum, the G-band corresponds to the in-plane optical phonons mode of two neighbouring carbon atoms on a graphene layer. Interestingly, the G-band frequency (ω_G) slightly upshifts with increasing the number of layers (β) and follows $1/\beta$ dependence [76], [89]. The slight upshift in ω_G , i.e. ~ 5 cm⁻¹, with the number of graphene layers can be seen in Figure 2.5(c). Unlike bulk graphite, the intensity of the 2D peak ($I(2D)$) is much larger than that of the G peak in graphene

(Figure 2.5(b)), i.e. $I(2D)/I(G) = 4$ in graphene [86]. Furthermore, the G peak intensity increases almost linearly with the number of graphene layers (observable in Figure 2.6).

The D-band and 2D-band originate from a second order process. That is, the ω_D and ω_{2D} vary as a function of the energy of the incident laser (E_{laser}). Such behaviour is understood to originate from a double resonance Raman process [86]. The 2D peak appears as a single peak in monolayer graphene but, according to Figure 2.6, it broadens as the number of layers is increased. In fact, the symmetric and sharp 2D-band ($\sim 30 \text{ cm}^{-1}$) is considered the best indicator of monolayer graphene flakes [88]. It is worth mentioning that, unlike the G peak and the 2D peak, the D peak (at $\sim 1350 \text{ cm}^{-1}$ [86]) intensity depends on the amount of disorder in a graphene sheet.

Note that the D' peak (see Figure 2.5(a)) is another weak disorder-induced feature in the Raman spectrum of graphene which appears at $\sim 1620 \text{ cm}^{-1}$ [86].

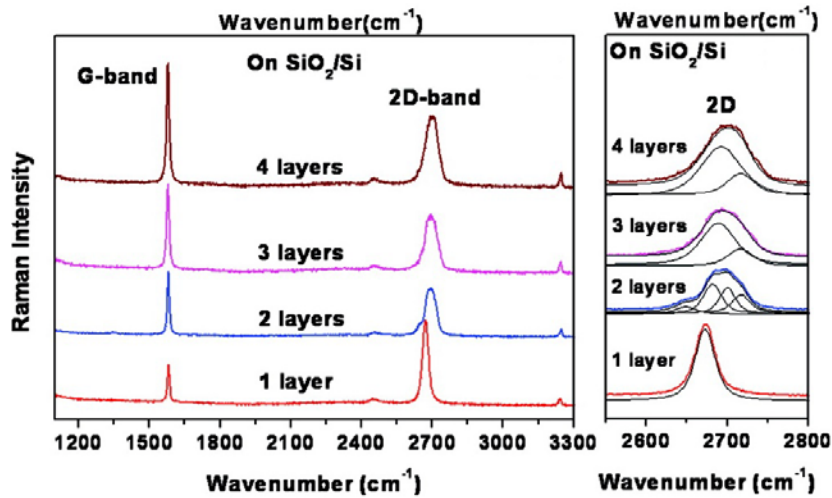


Figure 2.6 – The evolution in Raman spectrum of graphene as the number of layers is increased. Figure from ref. [88].

Chapter 3

Single Electron Transistors with Quantum Dot

This chapter provides an extensive study on the operation of single electron transistors (SETs) with quantum dot (QD) devices as building blocks for quantum information technology. The electron transport via Coulomb Blockade (CB) in such devices is discussed extensively. Furthermore, an experimental review on the behaviour of graphene quantum dots devices through a literature review, which highlights the most important experimental methods relevant to our work, is given.

3.1 Single Electron Transistors (SETs)

As explained in section 1.1, for years, the semiconductor industry has been trying to continue the downscaling trend (i.e. Moore's law) to improve the packaging density, circuit speed, power dissipation and cost. However, we discussed that the traditional scaling techniques are reaching their limits. Therefore, to find alternative methods to overcome the associated challenges is essential.

In 1985, Likharev and co-workers predicted the behaviour of a single nanometre-size tunnel junction in detail and proposed the idea of a single electron tunnelling Transistor (SET) [90]–[92]. Though, it must be mentioned that C. J. Görter initiated the study of single electron

effects by proposing the Coulomb blockade phenomena (see the discussion in section 3.2.1) as early as 1950s [92], [93]. However, it was in 1987 when the first SET device was fabricated by Fulton and Dolan at Bell labs in the US [92], [94]. Schematic illustration of a SET is shown in Figure 3.1. In a SET, there are two tunnel junctions which share one common electrode with a low self-capacitance, called the island. In addition, there are two tunnel junctions to prevent electrons entering or exiting the island unintentionally. The gate is connected to the island capacitively. Hence, by accurate tuning of the bias voltage (V_{SD}) and the gate voltage (V_g), electrons can propagate from source to drain via the island.

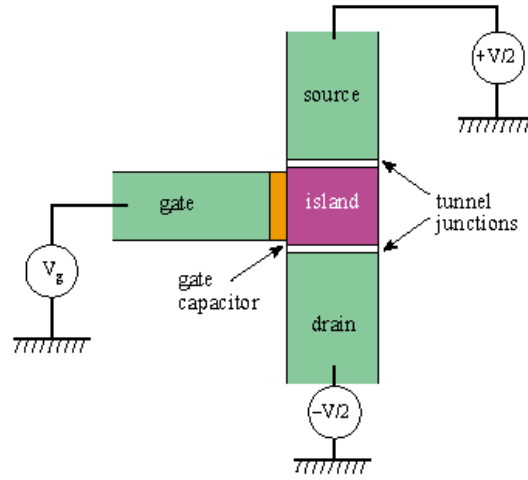


Figure 3.1 – A schematic illustration of a single electron transistor.
Figure from ref. [95].

The island consists of number of energy levels that are evenly spaced. The energy difference between the levels is equal to ΔE . ΔE is the energy needed to each subsequent electron to tunnel onto the island that acts as a self-capacitance C . Note that ΔE is inversely proportional to C , i.e. $\Delta E \propto \frac{1}{C}$. When there is no voltage at the gate electrode, no accessible energy level is within tunnelling range of the electrons on the source contact and all energy levels on the island with lower energies are occupied. By applying a positive voltage to the gate electrode

the energy levels of the island can be lowered. In this case, an electron can then tunnel into the island and occupy a previously vacant energy level.

Single electron transistors are considered as a promising candidate to replace standard MOSFETs. The most fascinating feature of SETs is the possibility to switch the device by adding one electron to the gate electrode. In contrast, a common MOSFET needs about 1000-10,000 electrons [96]. Indeed, the reduction in the number of electrons in a switching transition significantly lowers the circuit power dissipation, raising the possibility of even higher levels of circuit integration [97]. In addition, SETs have the potential to be much faster than conventional MOSFETs. That is, the switching time in SETs is determined by RC-time constants of the constrictions (i.e. tunnel junctions) that, thanks to improvements in nanofabrication and lithography tools, can be fabricated in very small dimensions [96].

3.2 Single electron transistors with quantum dot

The artificial confinement of electrons in a semiconductor structure leads to two-, one- or zero-dimensional electron systems. Quantum-mechanical effects become pronounced when extension of a structure in one dimension becomes of the order of the Fermi wavelength (i.e. de Broglie wavelength at the Fermi level) λ_F . In this case, the electronic density of states is distributed on discrete subbands with energy of E_i . The electrons occupy only the lowest subbands with energy of E_0 at sufficiently low temperatures. The system with such characteristics is called a two-dimensional electron system (2DES). A 2DES can be confined in one further dimension to become a one-dimensional electron system (1DES). Consequently, reducing the last free dimension leads to a 0DES, commonly known as a Quantum Dot (QD) [96], [98].

A QD device is modelled as a network of tunnel resistors and tunnel capacitors. A schematic circuit diagram of a SET with a single QD is shown in Figure 3.2. The electronic transport in a quantum dot device is influenced strongly by quantum mechanics at low temperatures that lead to formation of a discrete energy spectrum. An important phenomenon, which influences the electronic behaviour of quantum dot devices, is Coulomb Blockade (CB).

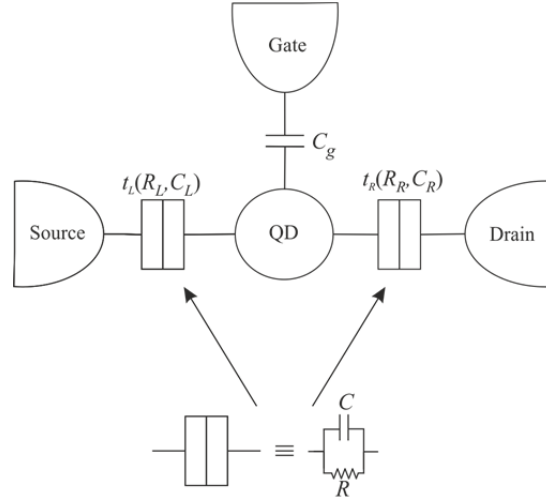


Figure 3.2 – A schematic circuit diagram of a SET with a single QD. The QD is connected to the source (drain) terminal via tunnel barrier $t_L(t_R)$. Tunnel barriers are represented by a tunnel resistance (R) and a tunnel capacitor (C) connected in parallel. Also, the QD is capacitively coupled to the gate terminal.

3.2.1 Coulomb blockade (CB)

Increase in resistance at small bias voltages of an electronic device with at least one low capacitance tunnel barrier is called Coulomb Blockade (CB). Because of this, the device resistance increases to infinity for a zero bias voltage and is also not constant at low bias voltages. Hence, the current flow through a tunnel barrier is a series of events which, only one electron tunnels through the tunnel barrier at a time. When an electron tunnels into a QD, part of the supplied energy by the voltage source (e.g. V_{DS}) is not immediately dissipated. A certain amount is used to charge the tunnel barrier capacitor (e.g. C_L) with an elementary charge. The build-up voltage in the capacitor will be large enough to prevent a new electron from tunnelling and is equal to $V_b = \frac{e}{C_{L(R)}}$, where e is the elementary charge. Therefore, at low bias voltages, the current flow is suppressed and the device resistance is not constant anymore. To tunnel an additional electron into the dot requires compensation of the repulsing electric field. The energy required to achieve this is called the charging energy of the dot (E_c) and is expressed by:

$$E_c = \frac{e^2}{2C_\Sigma}, \quad (3.1)$$

with

$$C_\Sigma = C_L + C_g + C_R. \quad (3.2)$$

To observe coulomb blockade effects and so ensuring a successful single electron tunnelling, there are two important criteria that must to be satisfied [98], [99]:

I) To ensure constant number of electrons in a QD (i.e. each electron in the system is localised), the tunnel barriers' resistance R_T (i.e. $R_{L(R)}$) must be larger than the quantum resistance:

$$R_T \gg R_Q, \quad (3.3)$$

where R_Q is the quantum resistance and is equal to $R_Q = h/e^2$. Based on Heisenberg time-energy uncertainty principle, we then have:

$$E_c \Delta t > \frac{h}{4\pi}, \quad (3.4)$$

where h is Planck's constant. Moreover,

$$\Delta t \cong R_T C_T, \quad (3.5)$$

where Δt is the time required by an electron to tunnel into or out of a QD with a charging energy of E_c . By combining Eqs. (3.1), (3.4), (3.5), the value of R_T can be calculated as:

$$R_T > \frac{h}{2\pi e^2} = 25813 \, \Omega \cong 26 \, \text{k}\Omega \quad (3.6)$$

II) To prevent the electrons entering or exiting the QD freely, the thermal energy must be much lower than the charging energy E_c . In other words, the charging energy must be large enough to suppress the thermal fluctuations which can be expressed as:

$$k_B T \ll E_c, \quad (3.7)$$

where k_B is Boltzmann constant and T is temperature in Kelvin.

3.2.2 Carrier transport in single electron transistors

The total energy of a QD system depends on polarisation, background charge (Q_0) and the number of electrons (N) that have tunnelled through the source and the drain tunnel barriers in direction of positive V_{DS} . Furthermore, the rate of single electron tunnelling per unit time through a potential barrier (i) can be expressed as [99]:

$$\Gamma_i^\pm = \frac{1}{e^2 R_i} \frac{\frac{\Delta E_i^\pm}{e}}{1 - \exp(\frac{-\Delta E_i^\pm}{k_B T})}, \quad (3.8)$$

where Γ_i corresponds to single electron tunnelling rate through source (Γ_L) or drain (Γ_R) tunnel barriers in positive direction (“+”) or negative direction (“-”) of a positive V_{DS} . R_i is the source (R_L) or the drain (R_R) tunnel barrier resistance. The four possible tunnelling transitions in a QD device are shown in Figure 3.3.

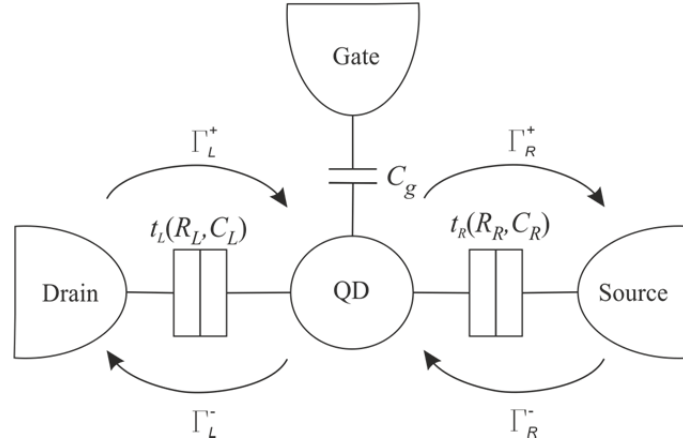


Figure 3.3 – The four possible tunnelling transitions in a SET with a single QD. The arrows show the direction of the electron tunnelling. That is, “+” (“-”) sign shows if the tunnelling is in positive (negative) direction with respect to polarity of the V_{DS} .

The expected $I - V$ characteristics of a QD device at a temperature of 4.2 K are shown in Figure 3.4. The blockade region in the $I_{SD} - V_{SD}$ characteristic, shown in Figure 3.4(a), reflects CB effect. That is, the conduction only occurs when V_{SD} is large enough such that the

electrons' energy at the contacts, e.g. source, exceeds the charging energy (E_c) of the QD. The energy required to add an additional electron into a QD with N electrons, e.g. $\mu_{QD}(N+1) - \mu_{QD}(N)$, equals to E_c . Note that μ_{QD} is the electrochemical potential of the dot. However, as we previously mentioned, the strong confinement in a QD leads to formation of a discrete energy spectrum. Therefore, the condition required to ensure successful single electron tunnelling via the tunnel barriers can be expressed as:

$$eV_{SD} > E_{add}, \quad (3.9)$$

where $E_{add} = \Delta E + E_c$ and ΔE is the energy spacing between two discrete quantum energy levels in a QD (Figure 3.4(b)). By varying the gate voltage (V_g), the electrochemical potential of the dot (μ_{QD}) can be tuned relative to that of the source and drain terminals. That is, for $V_g = 0$, there is no accessible energy level in the bias window, formed by $eV_{SD} = \mu_S - \mu_D$, for an electron to occupy (Figure 3.4(b)). However, for $V_g \neq 0$, a vacant energy level can be tuned in the bias window so that an electron can tunnel into the QD (Figure 3.4(c)). The electron can then tunnel into the drain via the t_R tunnel barrier. In the $I_{SD} - V_g$ output plot, single electron tunnelling events appear as pronounced peaks (known as CB peaks) that are evenly spaced by $\Delta V_g \approx \frac{e}{C_g}$ (shown in Figure 3.4(d)).

It is worth mentioning that such single electron transition in a QD device is considered as linear transport regime. That is, only the ground states (represented as black lines in the quantum dot region in Figure 3.4(b) and Figure 3.4(c)) contribute to the carrier transport and electrons tunnel elastically through the device.

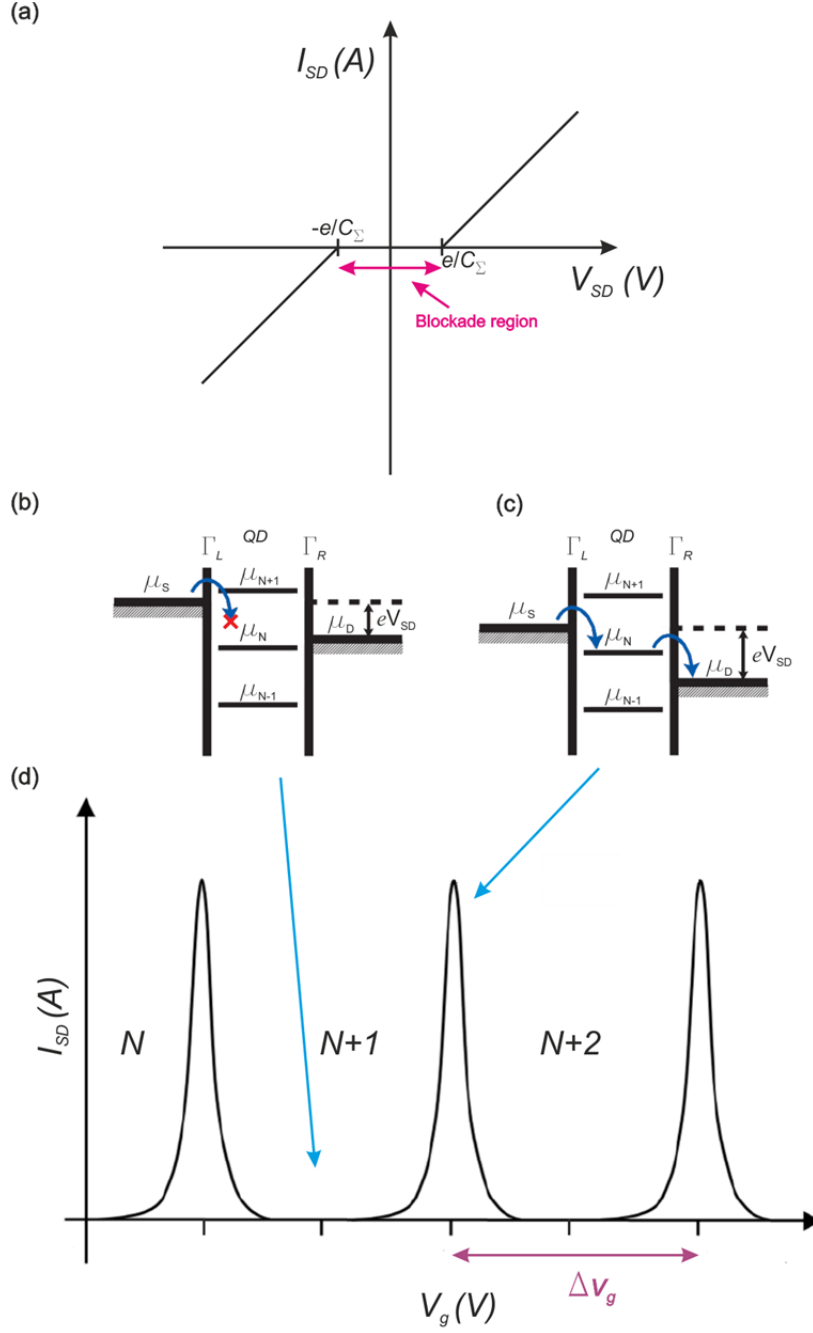


Figure 3.4 – $I - V$ characteristics of a QD device at a temperature of 4.2 K. (a) The $I_{SD} - V_{SD}$ output plot. For $|V_{SD}| < \frac{e}{C_{\Sigma}}$, the current flow is suppressed due to the E_c of the QD. (b) The energy level diagram of a QD device in its Coulomb blockade state. (c) The energy level diagram of a QD device in its single electron tunnelling state. (d) $I_{SD} - V_g$ output plot of the device where each single electron tunnelling event appears as a pronounced CB peak.

A stability diagram of a QD device is defined as the $V_{SD} - V_g$ output plot and is shown in Figure 3.5. The blockade regions (shaded regions in Figure 3.5) are called Coulomb diamonds. Note that we have not considered a background charge (Q_0) effect in Figure 3.5, i.e. $Q_0 = 0$. However, since Q_0 is a constant, it only shifts the diagram by $-\frac{Q_0}{C_g}$ in the negative direction of the V_g axis.

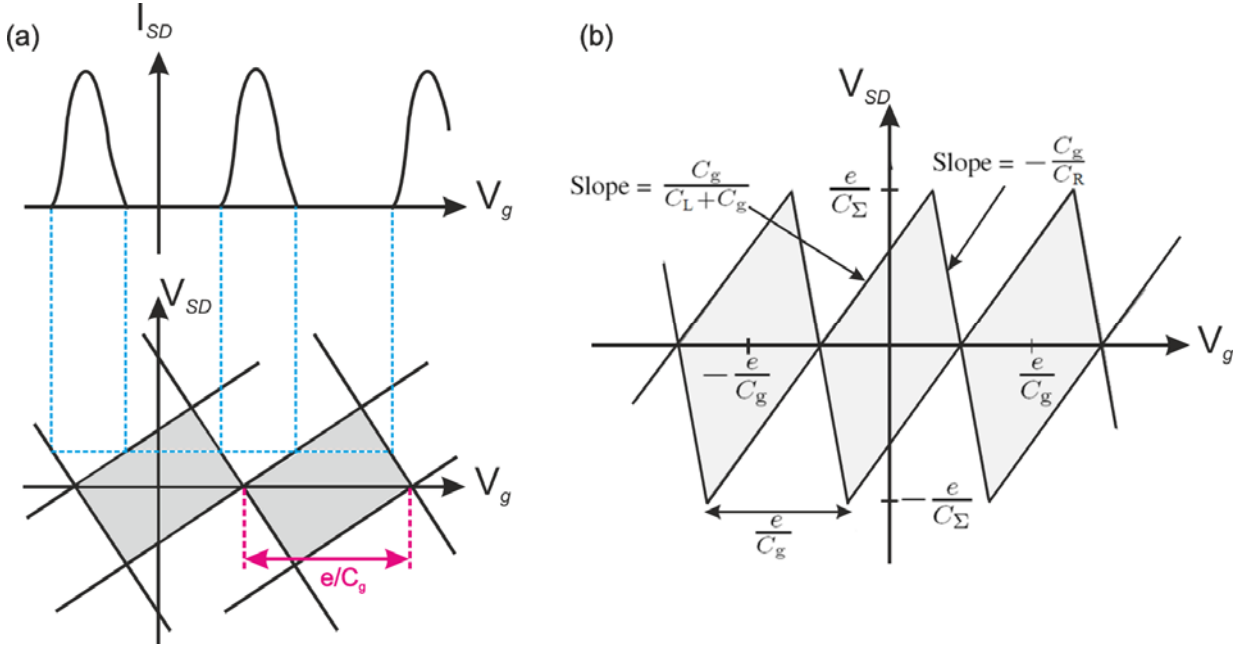


Figure 3.5 – (a) The appearance of Coulomb diamonds with respect to the Coulomb oscillation peaks, with a period of $\frac{e}{C_g}$. (b) Stability diagram of a QD device with $Q_0 = 0$. Note that the blockade regions are shaded. Also, the axes are arbitrary units.

3.2.3 Single electron transistors with double quantum dot (DQD)

Lateral double quantum dots (DQD) coupled in series is an interesting and popular SET device structure. DQD devices are considered as promising candidates for basic information storage elements in quantum computer architecture [100]. In this section, we concentrate on the electron transport in such devices.

A simplified schematic circuit diagram of a SET with DQD is shown in Figure 3.6.

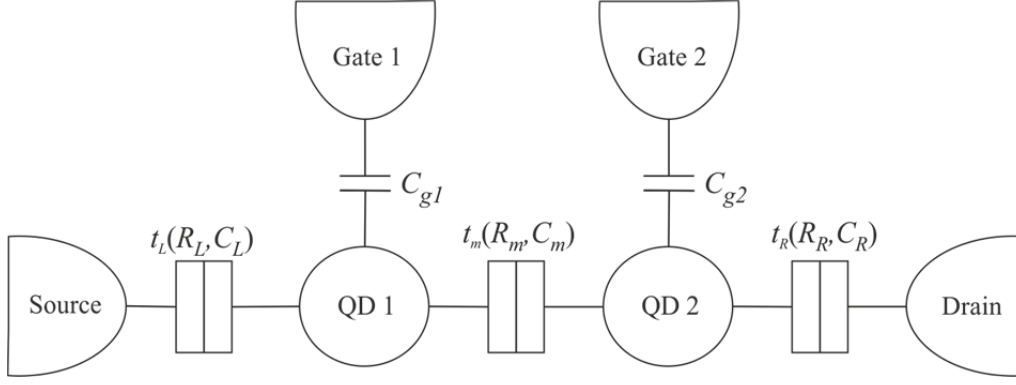


Figure 3.6 – A simplified schematic circuit diagram of a SET with double quantum dots (DQD). $t_m(R_m, C_m)$ is the coupling tunnel barrier (coupling resistance, coupling capacitance) between the two dots.

The schematic circuit diagram of a DQD device is similar to that of a QD device. Source (drain) terminal is connected via t_l (t_R) to the $QD\ 1$ ($QD\ 2$). The electrochemical potential of $QD\ 1$ ($QD\ 2$) is controlled capacitively via C_{g1} (C_{g2}) by a gate electrode V_{g1} (V_{g2}). In addition, the two quantum dots are coupled to each other by a tunnel barrier (i.e. t_m), known as interdot coupling tunnel barrier. Note that in Figure 3.6, we consider a simplified schematic circuit diagram of a DQD device. That is, in practice, there is a finite cross capacitance from each gate to the other which is known as gate cross capacitance. Moreover, the schematic does not take into account a back gate or a top gate.

The following discussion follows the approach from van der Wiel *et al.* [101]. We consider the following assumptions for a linear electron transport regime:

- I) The number of electrons in each QD is considered to be N_1 and N_2 , respectively.
- II) The electric charges of QDs are $Q_{QD1} = -N_1|e|$ and $Q_{QD2} = -N_2|e|$, respectively.
- III) Drain electrode is grounded and the bias voltage applied to the source electrode is zero, i.e. $V_L = V_R = 0$.
- IV) The gate cross capacitances are negligible.

Based on these assumptions, the total charge on each QD is written as:

$$Q_{QD1} = C_L(V_{QD1} - V_L) + C_{g1}(V_{QD1} - V_{g1}) + C_m(V_{QD1} - V_{QD2}), \quad (3.10)$$

$$Q_{QD2} = C_R(V_{QD2} - V_R) + C_{g2}(V_{QD2} - V_{g2}) + C_m(V_{QD2} - V_{QD1}). \quad (3.11)$$

where V_{QD1} and V_{QD2} are the voltages of the two QDs.

Based on Eqs. (3.10), (3.11), the electrostatic energy of the double dots circuit can be written as:

$$U(N_1, N_2) = \frac{1}{2}N_1^2 E_{C1} + \frac{1}{2}N_2^2 E_{C2} + N_1 N_2 E_{Cm} + f(V_{g1}, V_{g2}), \quad (3.12)$$

and

$$f(V_{g1}, V_{g2}) = \frac{1}{-|e|} \{C_{g1}V_{g1}(N_1 E_{C1} + N_2 E_{Cm}) + C_{g2}V_{g2}(N_1 E_{Cm} + N_2 E_{C2})\} + \frac{1}{e^2} \left\{ \frac{1}{2} C_{g1}^2 V_{g1}^2 E_{C1} + \frac{1}{2} C_{g2}^2 V_{g2}^2 E_{C2} + C_{g1}V_{g1}C_{g2}V_{g2}E_{Cm} \right\}, \quad (3.13)$$

with

$$E_{C1} = e^2 \frac{C_2}{C_1 C_2 - C_m^2}, \quad (3.14)$$

$$E_{C2} = e^2 \frac{C_1}{C_1 C_2 - C_m^2}, \quad (3.15)$$

$$E_{Cm} = e^2 \frac{C_m}{C_1 C_2 - C_m^2}. \quad (3.16)$$

E_{C1} (E_{C2}) is the charging energy of QD 1 (QD 2). The energy change of one dot when an electron is added to the other dot is denoted by E_{Cm} and is known as the electrostatic coupling energy. Note that the total capacitance applied to each dot is written as:

$$C_{1(2)} = C_{L(R)} + C_{g1(g2)} + C_m. \quad (3.17)$$

Based on Eqs. (3.1), (3.17), the charging energy of each QD and the coupling energy can be rewritten simply as:

$$E_{C1} = \frac{e^2}{C_1} \left(1 - \frac{C_m^2}{C_1 C_2}\right)^{-1}, \quad (3.18)$$

$$E_{C2} = \frac{e^2}{C_2} \left(1 - \frac{C_m^2}{C_1 C_2}\right)^{-1}, \quad (3.19)$$

$$E_{Cm} = \frac{e^2}{C_m} \left(\frac{C_1 C_2}{C_m^2} - 1\right)^{-1}. \quad (3.20)$$

In a DQD system, the electrochemical potential of the *QD* 1(2) is denoted as $\mu_{1(2)}(N_1, N_2)$ and is the energy required to add the $N_{1(2)}^{\text{th}}$ electron to 1(2), whilst having $N_{2(1)}$ electrons on the *QD*₂₍₁₎. The electrochemical potential of each dot (based on the electrostatic energy of the double dot system presented in Eq. (3.12)) can be written as:

$$\begin{aligned}\mu_1(N_1, N_2) &\equiv U(N_1, N_2) - U(N_1 - 1, N_2) \\ &= \left(N_1 - \frac{1}{2}\right)E_{C1} + N_2 E_{Cm} - \frac{1}{|e|} (C_{g1} V_{g1} E_{C1} + C_{g2} V_{g2} E_{Cm}),\end{aligned}\quad (3.21)$$

$$\begin{aligned}\mu_2(N_1, N_2) &\equiv U(N_1, N_2) - U(N_1, N_2 - 1) \\ &= \left(N_2 - \frac{1}{2}\right)E_{C2} + N_1 E_{Cm} - \frac{1}{|e|} (C_{g1} V_{g1} E_{C1} + C_{g2} V_{g2} E_{C2}).\end{aligned}\quad (3.22)$$

The stability diagram of a DQD system can be discussed based on the value of the coupling capacitance (C_m). Since no bias voltage is applied, we have $\mu_S = \mu_D = 0$. Therefore, the double dots' equilibrium charges are the largest integers N_1 and N_2 for which both $\mu_1(N_1, N_2)$ and $\mu_2(N_1, N_2)$ are less than zero. That is, electrons can escape to the left or right terminals if either $\mu_1(N_1, N_2)$ or $\mu_2(N_1, N_2)$ is larger than zero. Due to this, the stability diagram of the system is constructed in a hexagonal shape. The stability diagram is categorised into following three categories:

- I) The double dots behave as two independent dots if $C_m = 0$. That is, $E_{Cm} = 0$. The stability diagram of such a DQD system as a function of number of electrons in each dot (N_1, N_2) and applied gate voltages (V_{g1}, V_{g2}) is shown in Figure 3.7(a). Here, sweeping each gate voltage only affects the charge of its corresponding QD. Therefore, for a completely decoupled double dots system, the electrostatic energy in Eq. (3.12) can be written as a sum of the energies of the two dots. That is,

$$U(N_1, N_2) = \frac{(-N_1|e| + C_{g1}V_{g1})^2}{2C_1} + \frac{(-N_2|e| + C_{g2}V_{g2})^2}{2C_2}.\quad (3.23)$$

- II) If C_m becomes the dominant capacitance in the system, i.e. $C_m > C_{1(2)}$, the double dots behave as one big dot (Figure 3.7(b)). Therefore, Eq. (3.17) is simply:

$$C_{1(2)} = C_{1(2)} - C_m.\quad (3.24)$$

In this case, the electrostatic energy of the single big dot with charge N_1, N_2 can be written as:

$$U(N_1, N_2) = \frac{[-(N_1 + N_2)|e| + C_{g1}V_{g1} + C_{g2}V_{g2}]^2}{2(C_1 + C_2)}. \quad (3.25)$$

III) If $0 < C_m < 1$, the stability diagram forms an interesting arrangement of hexagons which is known as “honeycomb” pattern (Figure 3.7(c)). As Figure 3.7(c) illustrates, each hexagon is constructed by a number of small points (i.e. \bullet/\circ) that are known as “triple points”. The name comes from the fact that a conductance resonance occurs when an electron tunnels through both dots. This condition is satisfied at times that three charge states become degenerated. The black points (\bullet) and the white points (\circ) represent different type of tunnelling. As shown in Figure 3.7(d), a \bullet triple point represents an electron tunnelling event from the source to drain electrode. Therefore, the sequence of charge states can be written as:

$$U(N_1, N_2) \rightarrow (N_1 + 1, N_2) \rightarrow (N_1, N_2 + 1) \rightarrow (N_1, N_2). \quad (3.26)$$

However, a \circ triple point represents a ‘hole’ tunnelling event. Note that here ‘hole’ means reverse tunnelling of electrons from the drain to source electrode across both dots. Therefore, the sequence of charge states can be written as:

$$(N_1 + 1, N_2 + 1) \rightarrow (N_1 + 1, N_2) \rightarrow (N_1, N_2 + 1) \rightarrow (N_1 + 1, N_2 + 1). \quad (3.27)$$

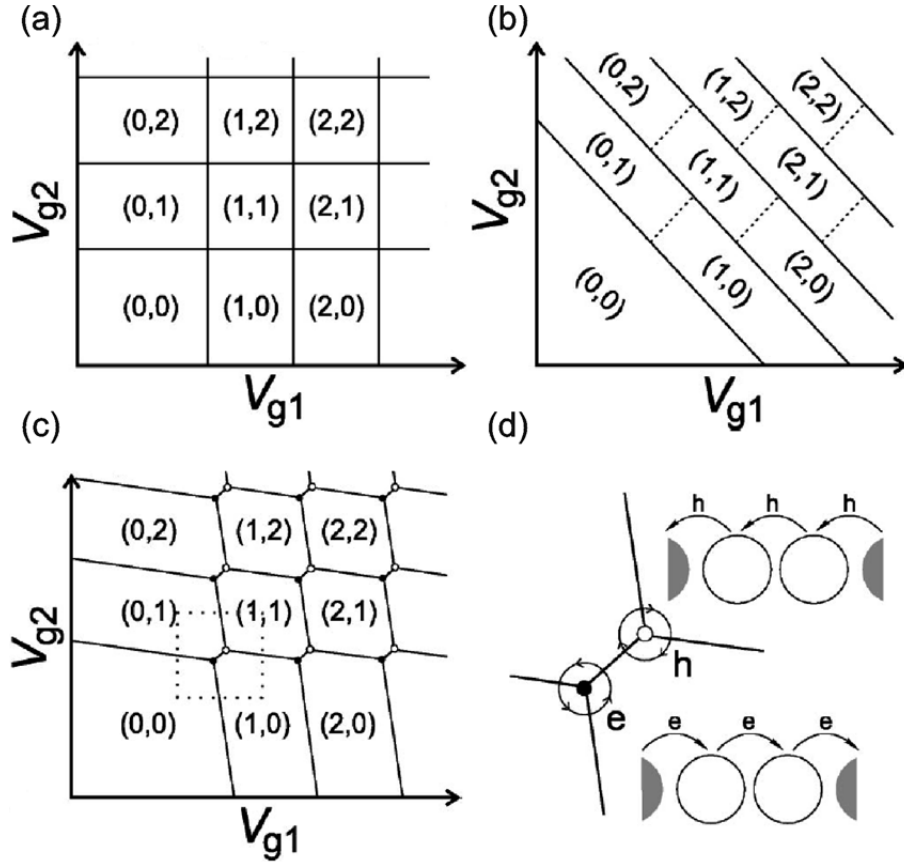


Figure 3.7 – Schematic of the stability diagram of a DQD system for, (a) completely decoupled double dots system (i.e. $C_m = 0$), (b) strong coupling capacitance (i.e. $\frac{C_m}{C_{1(2)}} \rightarrow 1$), (c) intermediate coupling capacitance (i.e. $0 < C_m < 1$). (d) The sequence of charge states at the \bullet/\circ triple points. The axes are arbitrary units. Figures from ref. [101].

It is worth mentioning that the sequential tunnelling events through double quantum dots coupled in series are only permitted at charge triple points. Because it is only at those points that μ_{QD1} , μ_{QD2} , μ_S and μ_D are aligned [101], [102]. Furthermore, geometry of a honeycomb cell in a stability diagram is shown in Figure 3.8(a). Geometry of the honeycomb cell can be expressed as [101]:

$$\Delta V_{g1} = \frac{|e|}{C_{g1}}, \quad (3.28)$$

$$\Delta V_{g2} = \frac{|e|}{C_{g2}}, \quad (3.29)$$

$$\Delta V_{g1}^m = \frac{|e|c_m}{c_{g1}c_2} = \Delta V_{g1} \frac{c_m}{c_2}, \quad (3.30)$$

$$\Delta V_{g2}^m = \frac{|e|c_m}{c_{g2}c_1} = \Delta V_{g2} \frac{c_m}{c_1}. \quad (3.31)$$

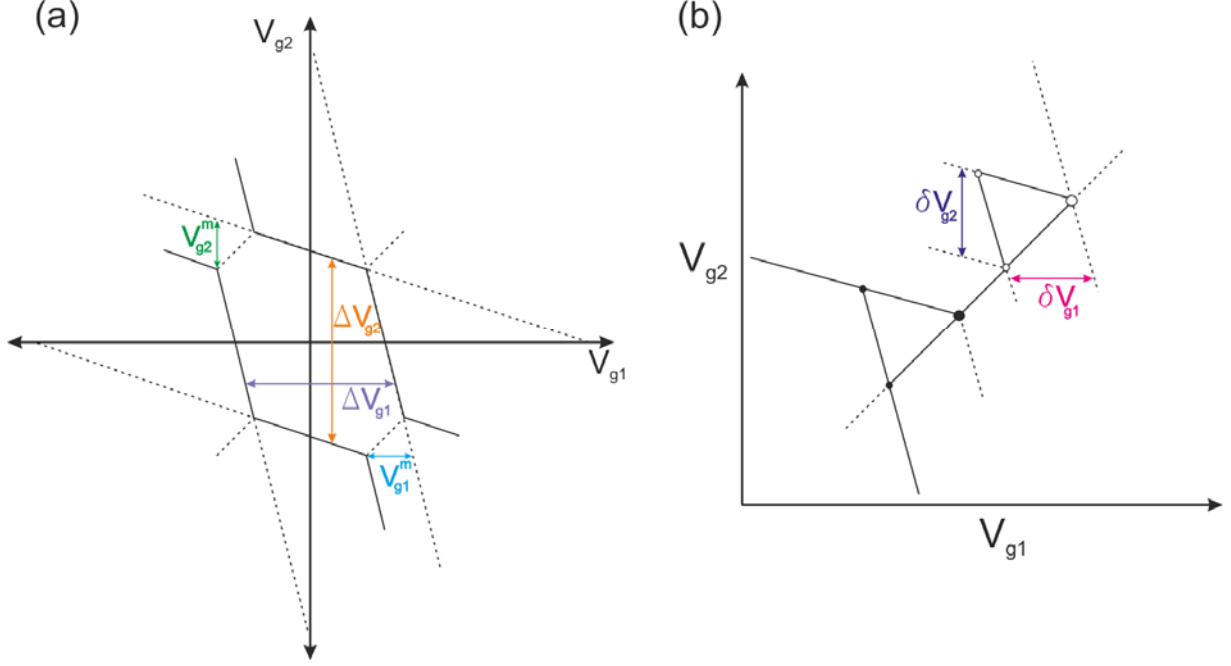


Figure 3.8 – (a) Geometry of a honeycomb cell of the stability diagram of a DQD device with an intermediate coupling capacitance. (b) Geometry of the bias triangles formed at the triple points at a finite bias voltage. The axes are arbitrary units.

At a finite V_{SD} (i.e. nonlinear transport regime), the conductance regions of the stability diagram, i.e. the triple points, change to triangular-shaped regions (shown in Figure 3.8(b) and Figure 3.9(a)). These regions are called bias windows or bias triangles. The weak-grey-colour regions of the bias triangles in Figure 3.9(a) are attributed to off-resonance current. The off-resonance conductance in the bias triangles is as a result of inelastic tunnelling (due to phonon or photon absorption or emission) [103], [104] and co-tunnelling [101]. Note that an inelastic tunnelling occurs when there is an energy mismatch between the energy levels of the two dots but, the energy levels still lie between $\mu_S - \mu_D$ (i.e. bias window).

The bias triangles correspond to the region in which, determining the detuning of the DQD potentials is in the range of the bias window. If we assume [101],

$$\text{I) } -|e|V_{SD} = \mu_S \geq \mu_1,$$

$$\text{II) } \mu_1 \geq \mu_2,$$

$$\text{III) } \mu_2 \geq \mu_D = 0,$$

then the dimensions of the bias triangles can be expressed as [101]:

$$\gamma_1 \delta V_{g1} = \frac{c_{g1}}{c_1} |e| \delta V_{g1} = |eV_{SD}|, \quad (3.32)$$

$$\gamma_2 \delta V_{g2} = \frac{c_{g2}}{c_2} |e| \delta V_{g2} = |eV_{SD}|. \quad (3.33)$$

γ_1 and γ_2 are the conversion factors between the gate voltage and energy.

The triangle regions grow in size with increasing the bias voltage. In addition, for a sufficiently large bias voltage, a number of discrete energy levels can appear between the ground states of the dots, known as excited states. These excited states can also contribute to the conductance. Hence, successive alignment of ground states and excited states leads to resonances within the bias triangles. These resonances are observed as lines with different colours (due to change in the current through the device) in the bias triangle. This is shown in Figure 3.9(b).

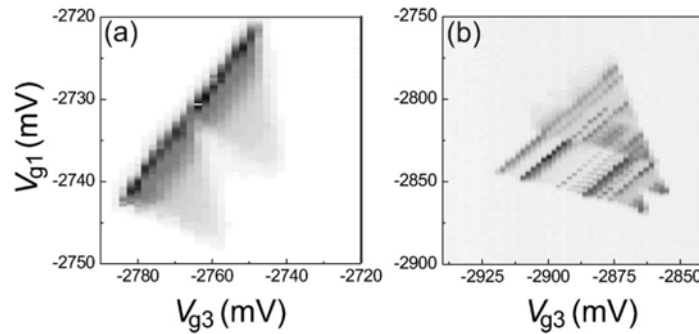


Figure 3.9 – (a) A pair of bias triangle with $V_{SD} = -200 \mu V$. The dark line is the elastic tunnelling via alignment of ground states in the two dots. The grey-colour region is the off-resonance current. (b) Observation of current resonance in the bias triangles due to the excited states. $V_{SD} = -1 mV$. Figures from ref. [101].

3.3 An experimental review on graphene nano devices

As discussed in section 1.2, spin-orbit coupling and hyperfine interactions with carbon nuclei are both small in graphene, and a very long spin relaxation length has been demonstrated [12], [13], which make graphene a promising candidate for Quantum Information Technologies (QIT) [11]. However, so far, to our best of knowledge, there are very few groups who are actively investigating graphene QDs (GQDs) devices. This is probably due to graphene's short history and its huge impact in several areas of science and technology. In this section, we present a brief literature review which highlights some of the conducted experiments on graphene nano devices relevant to our work.

3.3.1 Graphene nanoribbons

As mentioned in section 2.2, charge carriers mimic relativistic particles (i.e. massless Dirac fermions) in graphene. A direct consequence of this is one of the most counterintuitive phenomena in quantum electrodynamics known as Klein paradox (i.e. Klein tunnelling). Klein tunnelling refers to perfect tunnelling of relativistic carriers through arbitrary high and wide barriers [10], [105]. This means it is impossible to confine Dirac carriers by electrostatic potentials. In the case of a gapped semiconductor, electron transport can only occur by tunnelling through a potential barrier region and the tunnelling decreases exponentially with the height and width of the potential barrier [105]. However, due to pseudo-spin conservation and absence of a band gap in graphene, carriers transmit with probability of one when hit a potential barrier regardless of its geometry (i.e. height and width of the barrier) [105]. The chiral nature of carriers leads to matching of electron and hole wavefunctions across a potential barrier, and so resulting in a high-probability tunnelling [105], [106]. Consequently, the electron at a potential barrier can transform into a hole moving in opposite direction since they share the same pseudo-spin [105], [107]. It is worth mentioning that experimental observation of Klein tunnelling in graphene has been demonstrated by forming a potential step with a narrow top gate (width comparable to the mean free path of the charge carriers) [108], [109].

It has been demonstrated that etching graphene into nanometre size graphene ribbon structures (constrictions with widths below 100 nm) can overcome this obstacle. This is due to creation of a disorder-induced energy gap after etching that allows confinement of individual carriers in graphene [83], [110]–[112]. This makes this quasi-one-dimensional structure a promising candidate as tunnel barriers for graphene QDs devices. Therefore, it is important to address the I-V characteristics of graphene nanoribbons before discussing behaviour of graphene QDs devices.

Here, we now focus on the electrical characteristics of graphene nanoribbons. Unlike a pristine graphene flake which exhibits a linear dependence of conductance (i.e. current) with respect to an applied back gate voltage (i.e. carrier density), graphene nanoribbons exhibit a sub-linear dependence with an overall strongly reduced conductance. In addition, in contrast to the minimum conductance at the Dirac point, a region of strongly suppressed current (known as transport gap ΔV_{bg}) can be observed for graphene nanoribbons. This is shown in Figure 3.10(a) for a GNR with $W = 85$ nm and $L = 500$ nm. However, as it is evident in Figure 3.10(a), it is not a real energy gap because it contains a large number of reproducible conductance resonances.

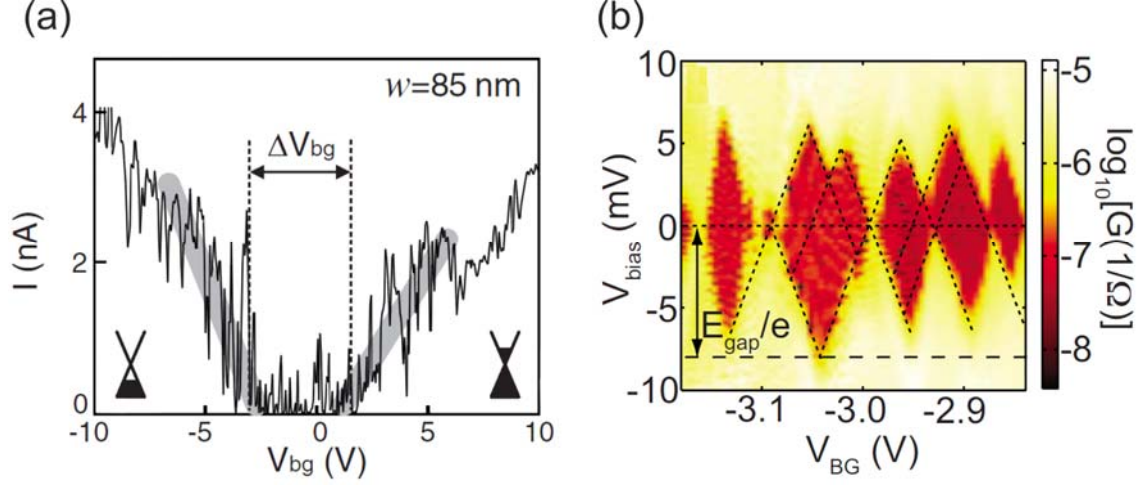


Figure 3.10 – (a) Formation of a transport gap with a size of $\Delta V_{bg} = 3.4$ V in the carrier transport of a GNR with $W = 85$ nm and $L = 500$ nm. Transport can be tuned from being hole (left inset) to electron dominated (right inset). Figure from ref. [82]. (b) Observation of Coulomb diamonds in a GNR. The measurements were conducted in a cryostat at $T \approx 2$ K. Figure from ref. [113].

Han *et al.* [114] demonstrated that a length-dependent transport gap can be formed at the charge neutrality point which its size is inversely proportional to the width of graphene nanoribbons (GNRs). However, the overall conductance level in the gap region depends strongly on the length of the GNRs [83]. Note that ΔV_{bg} is measured at constant V_b by varying Fermi energy (ΔE_F) in a GNR. The ΔE_F corresponding to ΔV_{bg} can be estimated as [81]:

$$\Delta E_F \approx \hbar v_F \sqrt{\frac{2\pi C_g \Delta V_{bg}}{|e|}}, \quad (3.34)$$

where C_g is the back gate capacitance per area.

On the other hand, at low temperatures, regions of suppressed current leading to an effective energy gap in bias direction inside the transport gap can be observed. This is shown in Figure 3.10(b). The energy gap can be expressed as [112]:

$$E_{gap} = \alpha / (W - W^*), \quad (3.35)$$

where $\alpha = 0.2$ eV.nm and $W^* = 16$ nm accounts for inactive edges.

Furthermore, the observation of distinguishable Coulomb diamonds (Figure 3.10(b)) indicate that transport is blocked by localised electronic states (i.e. quantum dots) [81], [82], [106]. It was also demonstrated that the observed Coulomb diamonds can be controlled via a side gate [81], hinting that in this case, only a single charged island is tuned. Experimental observation of (i) Coulomb diamonds (which vary in size as function of E_F), (ii) strong variation of the lever arms (i.e. slope of the edges of diamond patterns) of each current resonance and (iii) local charging islands inside the ribbon (which can be tuned via a side gate) provided solid evidence that the E_{gap} and the ΔE_F are related to charged islands/quantum dots [81], [82], [106].

It has been suggested that the observed disorder-induced energy gap (and so formation of quantum dots along graphene nanoribbons) originates from presence of a quantum confinement energy gap in combination with localisation due to strong bulk disorder and edge disorder, which replaces pseudo-relativistic Klein tunnelling by real tunnelling [81], [106], [114], [115].

Following Stampfer *et al.* [81], the quantum confinement energy (ΔE_{con}) can be estimated by

$$\Delta E_{con}(W) \approx \gamma \pi a_{C-C} / W, \quad (3.36)$$

where $\gamma = 2.7$ eV is hopping energy and $a_{C-C} = 0.142$ nm is carbon-carbon bond distance [81].

However, this energy cannot solely justify the observed energy scale ΔE_F and formation of quantum dots along graphene nanoribbons. Therefore, it has been suggested that the observation of the induced energy gap in etched graphene flakes is due to combination of ΔE_{con} with a strong bulk and edge-induced disorder [81], [82], [106], [114], [115].

Localisation due to bulk disorder arises from inhomogeneous impurity doping and interaction with the underlying substrate (e.g. SiO₂) in graphene. This type of disorder leads to formation of electron-hole puddles around the charge neutrality point (Dirac point) with Klein tunnelling occurring between those puddles [81], [115]. In narrow graphene nanoribbons (i.e. $W < 100$ nm) the puddles are spatially separated due to the quantum confinement energy (ΔE_{con}) and carriers can only propagate from one puddle to another by real tunnelling events, and so resulting in a series of individual quantum dots [81], [83]. Experimental observation of electron-hole puddles in graphene samples on a SiO₂ substrate has been demonstrated [68]. In fact, it has been shown that the underlying substrate (e.g. SiO₂) plays a significant role in the bulk disorder by introducing scattering impurities, remote phonons [61], [115], [116]. In addition, the

roughness of the substrate can break the symmetry of the lattice and contribute to additional scattering by corrugating graphene flakes [117].

Localisation due to edge disorder arises in the presence of rough graphene edges. It has been reported that even a slight deviation from perfect armchair or zigzag orientation at the edge of graphene ribbons results in disconnected edge states and localised states at low energies [118]. Furthermore, studies have demonstrated that even for weak edge disorder with several removed carbon atoms can result in formation of localised edge states around the charge neutrality point and significant modifications of the density of states [119]–[122] which in turn, leads to a depletion in the ribbon centre [115]. It is worth mentioning that the Coulomb charging energy of the smallest disorder induced charge island in graphene nanoribbons is determined by the width of a ribbon but the overall conductance level strongly depends on the length of a ribbon [83], [106].

It is worth mentioning that for graphene nanoribbons with $W < 20$ nm, disorder dominates the transport [112], [114], [123] and graphene nanoribbons with width of 20-40 nm have been suggested as tuneable tunnelling barriers for graphene quantum dot devices [123]–[127].

3.3.2 Graphene quantum dots devices

In this section, we discuss some of the conducted experiments on GQDs devices relevant to our work.

As we will explain in chapter 5, the most established method of fabricating graphene nano devices, in particular, GQDs devices, is by means of e-beam lithography and reactive-ion-etch (RIE). Although the focus of this work is to fabricate monolayer GQDs devices but, it is worth mentioning that for the case of bilayer graphene, where an energy gap can be introduced by applying an electric field, other fabrication methods can be used to define quantum dots devices. This includes gate defined quantum dots devices [128], [129].

Ponomarenko *et al.* reported that depending on the diameter of a graphene dot (island), GQDs devices exhibit three basic operational regimes [123]. That is, for large dots sizes (e.g. $D = 250$ nm), Coulomb blockade (CB) resonances occur periodically as a function the applied back gate voltage and smooth variations in the CB peaks heights were attributed to interference-induced

changes in the barriers' transparency. For a dots size smaller than ~ 100 nm, CB peaks were no longer a periodic function of V_{bg} and varied strongly in their spacing. In fact, the positions of CB peaks became completely random for $D \leq 40$ nm due to the pronounced quantum confinement. That is, the size quantization (and so energy level spacing δE) plays a greater role for graphene's massless carriers in a quantum box of size D ($\delta E \approx v_F \hbar / 2D$, $v_F \approx 10^6$ m/s is the Fermi velocity in graphene) than that of a massive carriers in other materials ($\delta E \approx \hbar^2 / 8mD^2$, m is the effective mass).

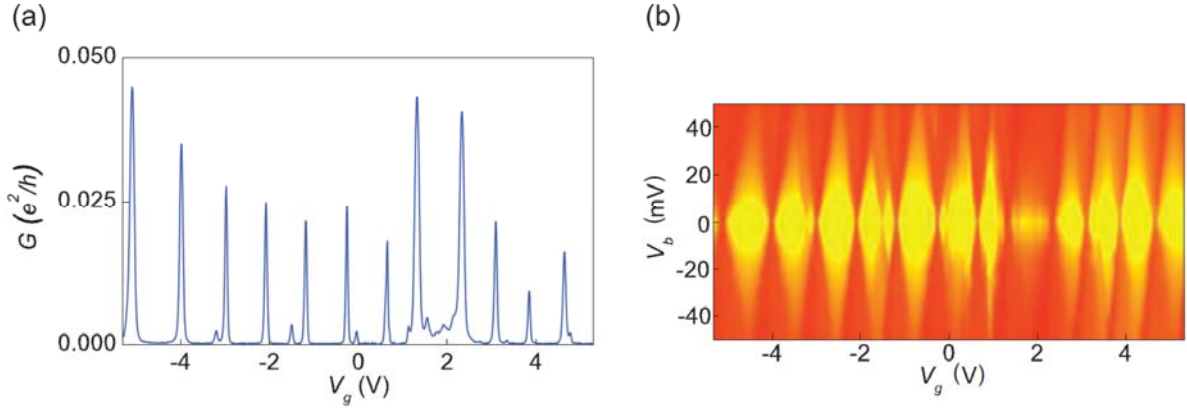


Figure 3.11 – (a) Coulomb blockade conductance resonances and (b) Coulomb blockade diamonds for a QD with an estimated $D = 15$ nm. The random spacing of CB peaks and random height of CB diamonds indicate that quantum chaos becomes dominant factor for small QDs. The measurements were conducted at $T \approx 300$ mK. Figures from ref. [123].

Therefore, the distance between CB peaks (ΔE) can be written as [123]:

$$\Delta E = E_c + \delta E, \quad (3.37)$$

where,

$$\delta E \approx \alpha / D, \quad (3.38)$$

with coefficient α varies around 0.5 eV.nm by a factor of 2 in different models. Furthermore, the authors revealed that δE grows approximately $\propto 1/D^2$ with decreasing D , indicating level repulsion effect, and so quantum chaos. Furthermore, for $D < 30$ nm, CB spacing was found to be completely dominated by quantum confinement and resulting in insulating regions as large as several volts. This is clearly observable in Figure 3.11.

Successful fabrication of GQDs devices and observation Coulomb diamond was demonstrated by Stampfer *et al.* [130], [131].

Güttinger *et al.* demonstrated successful charge detection of a GQDs using a GNR as a quantum-point-contact-like charge detector (CD) [124]. This was achieved by tuning the V_{bg} such that the GQD was close to its Dirac point as well as inside the transport gap of the CD. Figure 3.12(b) shows the GQD's CB peaks as a function of the PG gate (see Figure 3.12(a)) and their corresponding well aligned CD resonances. Figure 3.12(c) shows the contour plot of a set of traces corresponding to those shown in Figure 3.12(b) which interestingly, reveals that the slope (lever arm) of CB resonances ($\alpha_{PG,QD}/\alpha_{BG,QD} = 0.18$, highlighted by black dashed lines) differs from the slope of the lever arm of CD resonances ($\alpha_{PG,CD}/\alpha_{BG,CD} = 0.04$, highlighted by black dashed lines). This reduced slope is due to the larger distance between the CD and the PG gate relative to that of the QD and the PG gate [124].

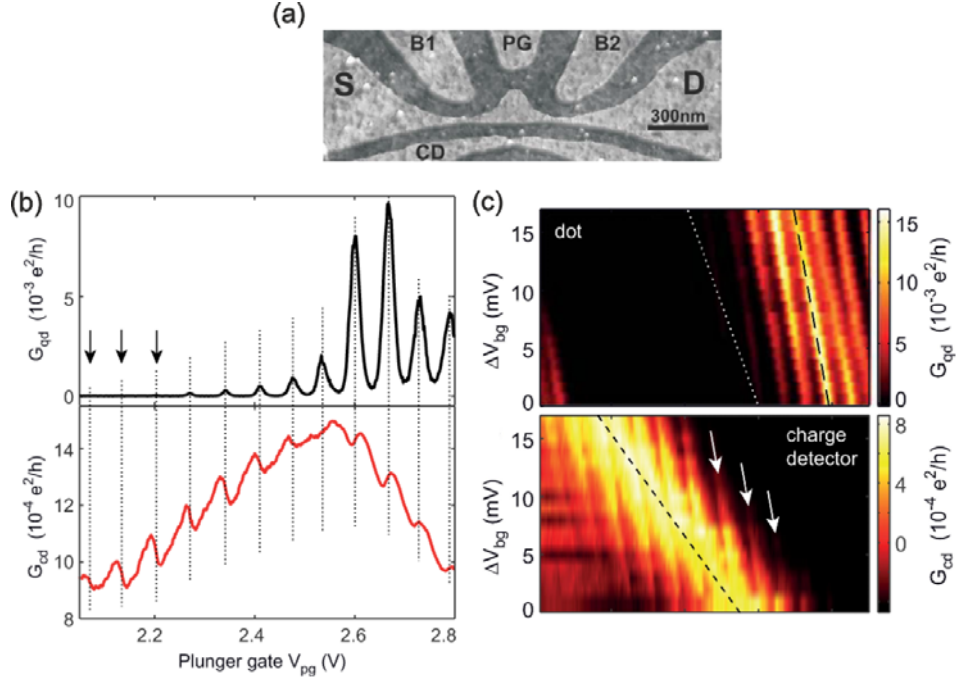


Figure 3.12 – (a) AFM image of the fabricated devices where S and D are the source and the drain, respectively. (b) Dot conductance (upper panel) and CD conductance (lower panel) as a function of the PG gate for a fixed back gate voltage. The dashed lines indicate the CB peaks and their corresponding CD resonance. (c) Differential conductance of the CB GQD (upper panel) and its corresponding CD resonance (lower panel). The arrows in the lower panel mark the CB resonances in the upper that are highlighted by black dashed line. The measurements were conducted at $T \approx 1.7$ K. Figures from ref. [124].

As mentioned in section 3.3.1, etched graphene nano devices suffer from potential disorder. This makes it hard to tune GQDs into few carrier regime. This was also pointed out by Güttinger *et al.* where modulation of CB resonances was attributed to conductance resonances in the tunnel constrictions (i.e. GNR channels). This is highlighted in Figure 3.12(c) (upper panel) with a white-dot line. One source of potential disorder is expected to arise from the substrate. It has been reported that graphene flakes on SiO_2 substrate exhibit charge puddles with diameters of the order of several tens of nanometre, whereas this value becomes an order of magnitude larger for graphene flakes on hexagonal boron nitride (hBN) [132].

Interestingly, Engels *et al.* reported that transport in GQDs fabricated on hBN flakes exhibit more stable single-dot characteristics even at high perpendicular magnetic fields, hinting at a

more homogeneous disorder landscape potential for GQDs on hBN compare to that of SiO₂ [132]. Furthermore, the authors revealed that unlike QDs on SiO₂ which their CB peak-spacing distribution exhibits no size dependence, the standard deviation of peak-spacing for GQDs on hBN showed a decrease with increasing the dot size. This indicated that edge roughness is the dominant source of disorder in GQDs on hBN with dots sizes below 100 nm. The standard deviation of the peak-spacing distribution for both types of devices is shown in Figure 3.13(b).

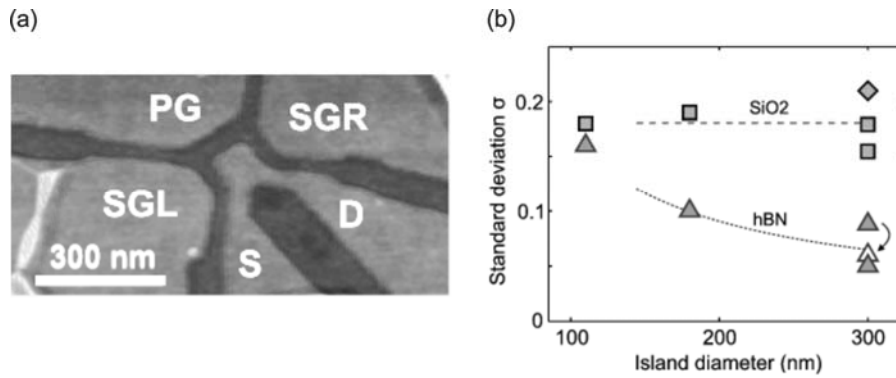


Figure 3.13 – (a) AFM image of an etched graphene quantum dot device on hBN. Here, *S* is the source, *D* is the drain, *PG* is the plunger gate, *SGL* and *SGR* are the left and right side gates, respectively. (b) summary plot of the standard deviation σ of the normalised peak-spacing distribution for different QD sizes on SiO₂ (rectangular data points) and hBN (triangular data points) substrate. The measurements were conducted at $T \approx 1.5$ K. Figures from ref. [132].

Successful fabrication and observation of stability diagram in GDQD devices has also been reported [125], [133]–[135]. The Coulomb blockade was tuned by in-plane graphene side gates and the collected stability diagram was studied by classical capacitance model [133], [134]. We discussed the interpretation of stability diagram of DQD devices extensively in section 3.2.3.

Interestingly, the interdot coupling (t_m in Figure 3.6) energy showed a strongly non-monotonic dependence of the applied gate voltage [133], [134]. Although the exact reason(s) behind this is still unknown but substrate effect and/or induced-disorder in graphene samples during fabrication process are expected to be possible contributing factors [134].

Observation of excited states in graphene DQD devices was reported by Molitor *et al.* [125] and by Liu *et al.* [126]. Molitor *et al.* demonstrated that despite the measured strong capacitive coupling between their double dots device, the estimated tunnel coupling (t_m) was low. The interdot tunnel coupling was estimated by tuning (i) the bias voltage so that to prevent expansion of triple points to triangles and, (ii) the back gate voltage so that the co-tunnelling was observable in the stability diagram. The stability diagram obtained after tuning of the bias voltage and back gate voltage is shown in Figure 3.14(b). In this case, a $t \leq 20 \mu\text{eV}$ was estimated from the rounded edges of the hexagons in the stability diagram (see Figure 3.14(c)).

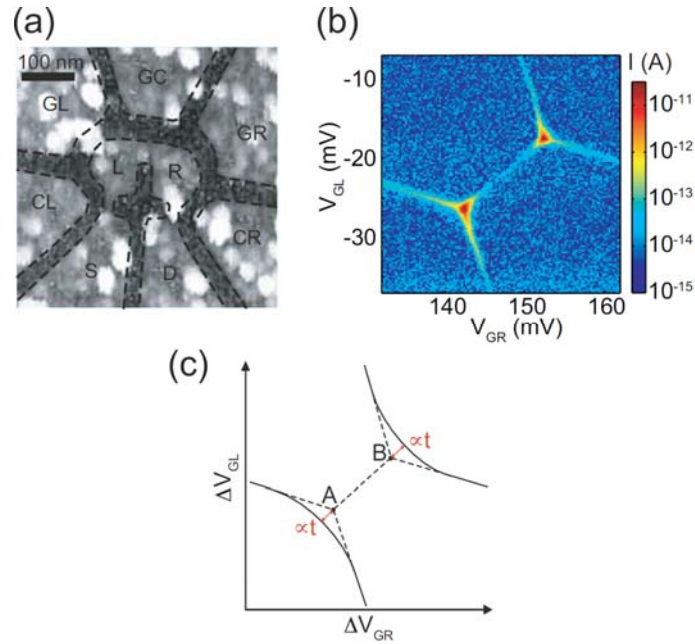


Figure 3.14 – (a) AFM image of the GDQD device fabricated by Molitor *et al.* (b) The collected stability diagram (honeycomb pattern) where the boundaries of the hexagons can be observed due to co-tunnelling effect. (c) A bias triangle for a positive bias voltage. The measurements were conducted at $T \approx 120$ mK. Figures from ref. [125].

The authors attributed the weak tunnel coupling to the geometry of the fabricated device (see Figure 3.14(a)). That is, the constriction between the two dots was not fabricated in the centre

of the two dots where the wave function is expected to be maximal, and so leading to a reduction in the tunnel coupling [125].

Here, we emphasize on the work by Liu *et al.* [126] due to their interesting/radical approach to fabricate a GDQD device as well as their detail analysis of the excited states.

Liu *et al.* reported the presence of excited states in a DQD device defined in a top-gated GNR. In this work, a graphene flake was patterned into a 800 nm long and 20 nm wide GNR. The top gates were constructed by e-beam evaporation of a SiO₂/Ti/Au layer (20 nm/5 nm/20 nm). Figure 3.15(a) shows SEM image of the fabricated device. In this device design, a double quantum dots system is formed when the applied voltages to all the three gates (i.e. G1, G2 and G3) are increased close to pinch-off. Figure 3.15(b) shows observation of the honeycomb pattern and charge triple points (as discussed extensively in section 3.2.3). However, due to co-tunnelling effect, a finite current along all boundaries of the hexagons can be observed. Note that a co-tunnelling event occurs when the energy level in one dot is aligned with the electrochemical potential in its corresponding lead. Co-tunnelling events can be suppressed by increasing the tunnel barriers (i.e. applying a higher gate voltage).

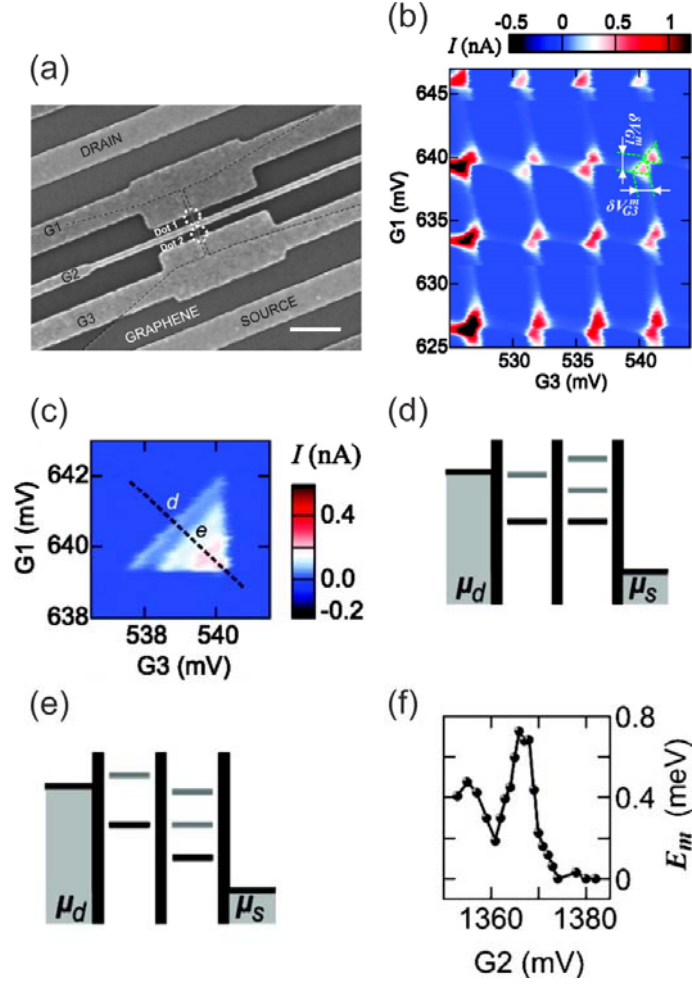


Figure 3.15 – (a) SEM image of a fabricated device by Liu *et al.*, similar to but smaller than the one reported in ref. [126]. Here, G1 and G3 are 600 nm-wide and G2 is 40 nm-wide. G2 is fabricated 80 nm away from G1 and G3. The scale bar is 400 nm. (b) The stability diagram (honeycomb pattern) where the boundaries of the hexagons can be observed due to co-tunnelling effect. (c) A bias triangle for a positive bias voltage. (d) and (e) are the energy level diagram of carrier transport at points d and e , respectively in Figure 3.15(c). (f) The interdot coupling energy E_m as a function of V_{G2} , suggesting that the change of interdot coupling is partially due to resonances induced by disorder close to gate G2. The measurements were conducted at $T \approx 50$ mK. Figures from ref. [126].

Furthermore, the authors reported that the extracted capacitance values from the stability diagram indicated that the dots were much bigger than intended, and so hinting the barriers were likely to be formed by disorder potential instead of being defined by electrostatic

potentials induced by the gates. Figure 3.15(c) shows an obtained bias triangle for a positive bias voltage where along the baseline of the triangle the ground states of the two dots are aligned. The ground states of both dots lie exactly in the middle of the bias window (Figure 3.15(d)) at the centre of the triangle baseline (point *d* in Figure 3.15(c)). Moving along the triangle (the detuning axis which is highlighted by a black dashed line in Figure 3.15(c)), at point *e* (Figure 3.15(c)), the ground state of dot 1 aligns exactly with the first excited state of dot 2 (Figure 3.15(e)), and resonant transport occurs. Therefore, by applying a positive (negative) bias voltage the energy level spacing of dot 2(1) can be calculated. Similar to the work by Molitor *et al.* [133] and Wang *et al.* [134], the interdot coupling was found to change non-monotonously as a function of V_{g2} (Figure 3.15(f)). In addition, Liu *et al.* demonstrated that dot-to-lead (source or drain) couplings also exhibit same non-monotonous manner as the interdot coupling. Consequently, this study and other works suggest that disorder substantially limits the control on couplings in graphene quantum dots devices [125], [126], [133], [134].

Therefore, disorder (parasitic localised states and edge disorder) poses a major obstacle in understanding of the behaviour of etched GQDs devices and their future applications. In addition, as we will discuss in chapter 4 and chapter 5, exposing graphene samples to a beam of highly accelerated particles (e.g. an electron beam and/or and ion beam) can induce further defects in graphene, and so result in degradation of electrical properties of final fabricated devices. Although current studies are encouraging but more efforts are required to minimise the amount of disorder in graphene nano devices. For instance, a comparison between the mobility of non-suspended and suspended graphene devices identified the underlying SiO_2 substrate as a major source of disorder and degradation in electrical properties of graphene devices [106], [115]. In this regard, hBN has been suggested as an interesting alternative substrate for graphene devices that the negative effect of substrate is greatly reduced [136]. On other hand, establishing an ultra-high resolution nanofabrication method to construct atomically sharp edges can be another way to minimise the disorder in graphene nano structures. For this very reason, we established our novel hybrid fabrication method for the first time by using a highly focused beam of He-ions with a sub-nm probe size (i.e. 0.35 nm) to fabricate extremely downscaled GQDs devices. This fabrication process and the corresponding results are explained in chapter 4.

Chapter 4

Fabrication of extremely downscaled graphene QDs by helium-ion beam milling¹

In this chapter, a novel hybrid fabrication method for graphene nano devices by means of helium-ion beam milling with sub-10 nm resolution and high yield is discussed. It is a combination of conventional e-beam lithography and direct milling with the sub-nm focused helium ion beam generated by a helium ion microscope. The method is used to fabricate graphene nano devices, e.g. DQD devices, contacted with metal to allow electrical characterization. The highly controllable, fine scale fabrication capabilities offered by this approach could lead to a more detailed understanding of the electrical characteristics of graphene nano devices and pave the way towards room-temperature operable graphene quantum dots devices.

¹ The work in this chapter has been published as Kalhor *et al. Microelectronic Engineering* **114**, 70

4.1 Introduction

As we explained in chapter 1, the on-going trend towards miniaturization and device performance is pushing current nano-manufacturing technologies to their limits in fabricating high resolution patterns at high densities in the sub-10 nm regime.

For research and prototyping, electron beam lithography (EBL) is the most established lithography method for fabrication of nano devices. Despite all the developments (e.g. 100 keV acceleration voltage), which have made EBL with sub-10 nm resolution in resist possible, the electron-resist interactions along with the resist development are limiting the resolution of this technique [27].

Graphene, a single atomic layer of graphite, with its unique electron-transport characteristics, that include the highest known intrinsic mobility (in excess of $200,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at low temperatures) [9], has attracted significant attention. Moreover, spin-orbit coupling and hyperfine interaction with carbon nuclei are both small in graphene, and a very long spin relaxation length has been demonstrated [12], [13], all of which make graphene a promising candidate material for Quantum Information Technologies (QIT) and spin qubit embodiment [11].

These superior transport properties encourage the downscaling of graphene devices further to the regime where the coherent nature of electronic and spin states can be fully exploited. Moreover, patterning graphene sheets into one-dimensional graphene nanoribbons (GNRs) with sub-10 nm widths and atomically smooth edges has been shown to create effective quantum confinement which opens up a finite band gap. It has been demonstrated that this approach can result in on-off ratios of $\sim 10^7$ in GNR transistors at room temperature [55], [137]–[139] and, as discussed in section 3.3.1, band gap of a GNR device is inversely proportional to its width. However, this requires the development of ultrafine patterning technologies which enables accurate nanoscale fabrication beyond the present techniques.

As we will discuss in chapter 5 of this report, e-beam lithography followed by reactive-ion-etch (RIE) is the most established method for fabricating graphene nano devices. However, e-beam spot size, proximity effect, resist development and eroding of the resist layer during etching can limit the resolution of this method [112], [135], [140], [141]. Eroding of the resist layer by

RIE also results in creation of disordered graphene edges. Furthermore, uneven thickness of the resist layer, which may be caused by the roughness of the SiO_2 surface layer and the presence of graphite pieces and metallic alignment marks, can also limit resolution and affect the symmetry of the patterns fabricated by this method [112], [135], [140], [141]. The resolution of this method is currently limited to a few tens of nanometres. GNRs with widths down to ~ 20 nm and with edge roughness on the order of a few nanometres were fabricated by this method [111], [112]. It is worth mentioning that this method is also not viable on suspended graphene samples. Figure 4.1 shows one of our GDQD devices fabricated by our EBL/RIE process. This fabrication method will be explained in section 5.4 in great detail. The asymmetry in the size of the fabricated features, i.e. DQD, and width-variations along the channel, are clearly evident.

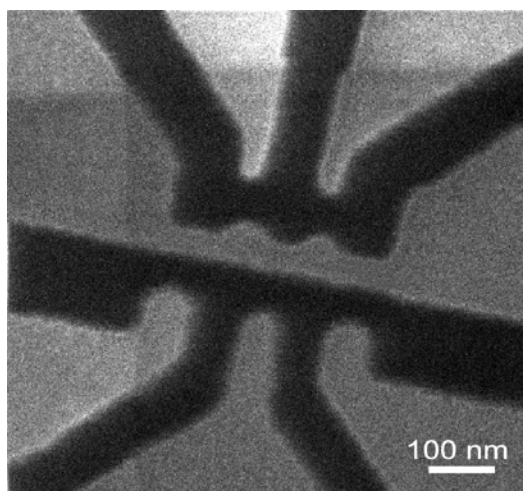


Figure 4.1 – HIM SE image of a GDQD device shows the asymmetry in the size of the fabricated features by e-beam lithography followed by RIE etch.

Transmission ion microscopy (TEM) or scanning TEM (STEM) has also been employed to fabricate graphene nanostructures [142]–[144]. Although this approach can offer atomic scale patterning resolution but it is very expensive and has major drawbacks. For instance, the technique requires graphene sheets to be transferred onto specific TEM grids which is not

suitable for large scale device fabrication [58], [145]. Moreover, transferring the patterned graphene flakes reliably onto a substrate (e.g. SiO₂) and then fabricating the required metal contacts harmlessly to allow electrical characterization of the devices are both very challenging tasks that have yet to be successfully demonstrated.

Focused Ion Beam (FIB) milling is another technique that is widely used for fabrication of micro and nano electronic devices. Milling and sputtering are achieved through collisions of the energetic Ga⁺ ions with the target atoms, displacing them from their original sites. Unfortunately a minimum probe size of ~4 nm limits the possible feature size. This is compounded by the high number of collision cascades produced by the Ga⁺ ions as they penetrate the sample, resulting in an interaction volume much larger than the probe size [146]. The high sputtering rate, which is due to large mass of the Ga⁺ ions, can be suitable for larger device fabrication, but it becomes problematic for the fabrication of nano devices when removal of small amounts of material is required.

In 2007, Carl Zeiss SMT introduced Helium-Ion Microscopy (HIM) as a new surface imaging technique [28]–[32]. It involves scanning a focused beam of helium ions across a surface to generate an image from the resulting secondary electron (SE) emission. An atomically sharp and extremely bright source, combined with the smaller de Broglie wavelength (and so larger momentum) of helium ions compared to electrons, enables a sub-nm probe size at the sample surface. Additionally, He ions produce far fewer collision cascades (and so low amount of beam divergence) in the first ~100 nm of entering the substrate resulting in a small interaction volume and so high resolution imaging, routinely below 1 nm (edge resolution) and, with the latest versions of the tool, below 0.35 nm [33]–[35].

Figure 4.2 compares beam interaction volume for Ga-ion beam, He-ion beam and electron beam in a Si substrate at an acceleration voltage of 30 keV. It is evident that the interaction volume of the He-ion beam is far more localised upon entering the substrate compare to the Ga-ion beam that is never truly localised and broadens as it enters the substrate. Furthermore, electrons penetrate and scatter far more easily due to their small mass and so their interaction radius is much larger compare to He-ion and Ga-ion beams. At higher acceleration voltages the interaction radius of the He-ion beam becomes even smaller and its penetration depth increases [146], however, current versions of the tool operate at a maximum of 30-40 keV.

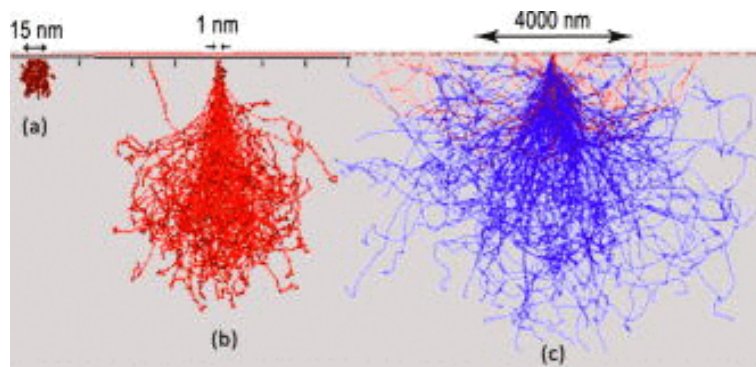


Figure 4.2 – Comparison of beam interaction volume for (a) Ga-ion beam, (b) He-ion beam and (c) electron beam at an acceleration voltage of 30 keV in a Si substrate. Figure from ref. [146].

Helium ion microscopy was primarily developed and introduced as an ultra-high resolution imaging technology, with unique contrast mechanisms and imaging abilities. However, as it produces an intense focused beam of He^+ ions, it is also capable of patterning (milling and lithography) and sputtering that are more commonly associated with a conventional Ga-ion beam. Therefore, shortly after its introduction, it was recognised as potential patterning tool for fabrication of state-of-the-art nano devices. There are three methods of employing the HIM for nanofabrication, resist-free patterning (milling), resist-assisted patterning (lithography) and beam-induced metal deposition.

In this chapter, first, we introduce Carl Zeiss Orion Helium ion microscope as an imaging tool. Furthermore, we discuss the capability of HIM milling for nanofabrication through a literature review, highlighting some of the most interesting recent experimental works. This is followed by introducing our novel hybrid fabrication method which is a combination of conventional e-beam lithography and HIM milling. E-beam lithography is used to form metal contacts onto graphene flakes. Helium ion milling is then used to pattern the flakes with intricate DQD devices, with sub-10 nm resolution and high fidelity, and to isolate the gate electrodes from the source and drain regions of the devices, enabling the fabricated nanoscale devices to be electrically characterized. All the steps involved in the fabrication process of such devices are explained systematically in great detail in order to pave the way for future graphene projects in Southampton Nano Group. Finally, we conclude this chapter by discussing the electrical

characterization of the final fabricated devices, demonstrating the successful fabrication of the first electrically characterized He-ion beam patterned graphene device. This approach could pave the way to a better understanding and more detailed study of graphene quantum devices.

The processing steps for the fabrication of graphene nano devices, e.g. GDQD, by our hybrid method are illustrated in Figure 4.3.

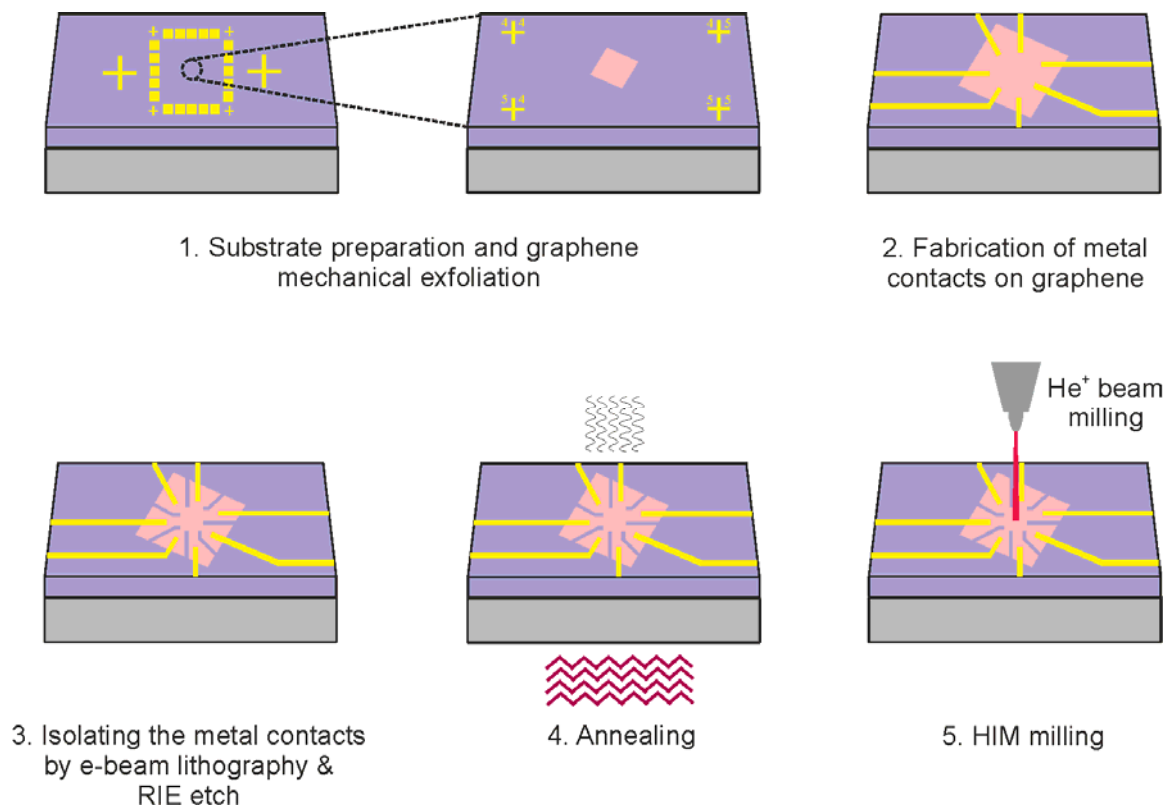


Figure 4.3 – Schematic illustration of the steps involved in the fabrication of GDQD devices by HIM milling.

4.2 Helium-ion microscopy

As mentioned in section 4.1, helium ion microscopy (Figure 4.4(a)) is a new surface imaging technique, similar to scanning electron microscopy (SEM) but with a focused beam of helium ions, enabling sub-nm resolution imaging from secondary electron (SE) emission. The HIM is

described as "the brightest illumination source ever created by man" which offers unprecedented spatial resolution over electronic microscopes [147], [148]. The structure of the HIM is shown in Figure 4.4(b). When the sharp needle (tip) in the source region (see Figure 4.4(b)), which is kept under high vacuum and cryogenic temperatures (~ 74 K), is positively biased, an extremely intense electric field produces at its apex. That is, with modest voltages in range of 5-30 keV, field strengths of 5 V/\AA can be achieved [30]. At field strength of 3 V/\AA , any neutral gas atoms near the vicinity of the tip are ionised. The ionisation region has a disk shape. The resulting positive helium ions are then immediately accelerated away from the needle. However, the most fascinating feature of the ion source manufactured by ALIS Corporation is its atomically sharp three-sided pyramid shaped needle. The needle is the emitting electrode. It is about 5 mm long and 0.25 mm in diameter and terminates in a 30° angle cone. The needle is made of tungsten because it is mechanically strong enough not to stretch or break due to the high electrostatic fields applied and the associated forces that are generated at the tip during the operation of the microscope [149]. The advantage of this pyramid shaped geometry is that the electric field is concentrated at the apex of the pyramid, so field ionization takes place predominantly at the topmost few atoms [28], [30]–[32], [150], [151].

The emission pattern of the ion source, known as trimer (i.e. three He^+ atoms), is shown in Figure 4.4(c) (inset) and can be monitored using scanning field ion microscopy (SFIM). The trimer is formed using high electric fields which can remove weakly bound atoms from the apex of the needle. In fact, since the trimer configuration is inherently stable, it also maximises the He-ion beam current [149]. For usual operating conditions, the emission from a single atom (the brightest atom in the trimer) is selected with an aperture. The available aperture sizes are 50 μm , 20 μm , 10 μm and 5 μm . Another advantage of the ALIS source is that the beam current can be modulated simply by varying helium gas pressure in the source region (see Figure 4.4(b)). The beam current can be controlled over several orders of magnitude without any need to change the extractor field voltage, the beam energy, or beam steering [30]. The He-ion beam current ranges from 1 fA to 100 pA, although a beam current of 1-5 pA is

typically used. The microscope is also equipped with a gas injection system (OmniGISTM unit, see Figure 4.4(b)) for ion beam-induced deposition applications [152].

The atomically sharp source, combined with the smaller de Broglie wavelength (and so larger momentum) of helium ions compared to electrons, enables a sub-nm probe size at the sample surface [33]–[35]. In addition, He-ions produce far fewer collision cascades (and so low amount of beam divergence) in the first ~ 100 nm of entering the substrate resulting in a small interaction volume (see Figure 4.2). That is, as high energy helium ions enter the substrate, they scatter inelastically, exciting SEs and losing energy in the process (i.e. electronic collision). However, since their mass is much larger (7000 times larger) than electron mass, they maintain their initial path (quasi-perfectly) in the substrate. Eventually as they decelerate and lose their kinetic energies (measured in eV per angstrom), nuclear collisions (i.e. elastic scattering without SE generation) become the dominating ions interactions method. This results in scattering at increasingly large angles and broadening of the beam interaction volume but, deep into the substrate [146]. In the case of an e-beam, electrons only collide elastically with target atoms because of their small mass and scatter far easier than helium ions (i.e. much larger interaction volume). In addition, He-ions are much smaller than gallium ions, resulting in negligible sputtering or subsurface sample damage. Therefore, upon entering a substrate, He-ions lead to a slim excitation volume and offer a much higher imaging resolution.

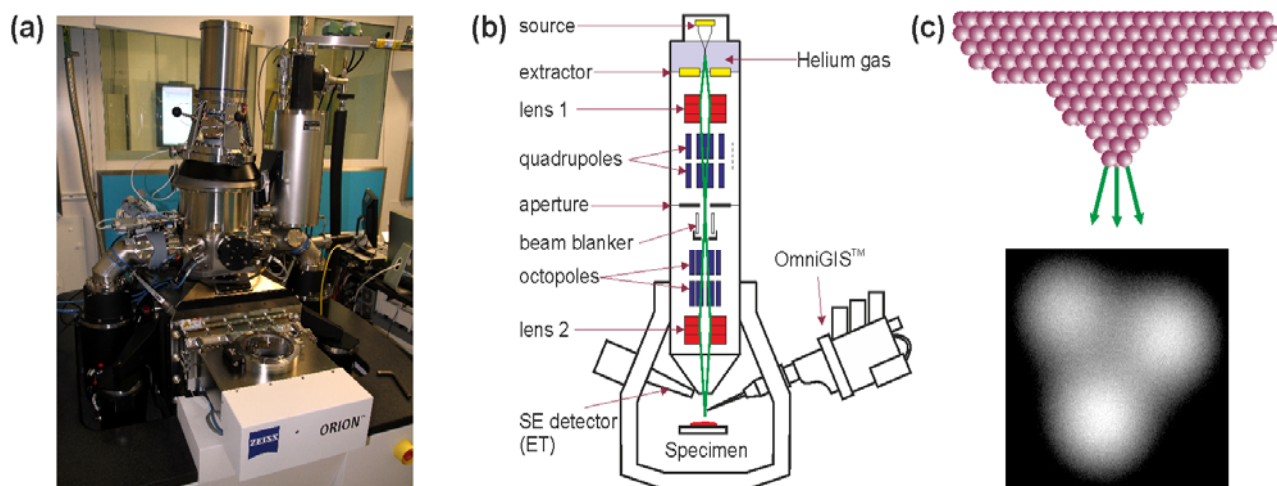


Figure 4.4 – (a) The Zeiss Orion™ Plus HIM at the University of Southampton. (b) Schematic of the HIM column. (c) Atomic structure of the Atomic Level Ion Source (ALIS) with 3 atoms located at the tip (the “trimer”). The inset is a HIM image of the ALIS showing emission from the trimer.

In addition to the properties of the beam source and the incoming beam, another important factor for final imaging quality is the SEs yield (by the primary particles) that exit from the specimen. In fact, SE yield determines the image contrast. That is, the number of SEs generated by the beam determine the brightness at each pixel during imaging (microscopy) [146]. SEs yield is much higher for helium ions than electrons, resulting in a remarkable imaging contrast with very high signal to noise ratio [146], [149]. Consequently, He-ion beam allows imaging with current as low as 1 femtoamp [153]. Furthermore, it is worth mentioning that both generated SEs by the primary ions and backscattered ions are used for imaging in the HIM. The HIM is equipped with a microchannel plate (MCP) detector which intercepts backscattered He-ions and generates grayscale images. Backscattered He-ion images are capable of providing very high elemental contrast (i.e. crystallographic information) on bulk samples such as polycrystalline gold films [154], [155]. That is, energy of the backscattered ions can reveal quantitative information on composition (i.e. scattering probability highly depends on the atomic number of the material).

4.3 An experimental review on nanofabrication by HIM milling

Resist-free patterning (also known as direct patterning or milling) using a focused ion beam (FIB) involves scanning the beam in a defined pattern to selectively remove (sputter) the substrate atoms. Milling by a FIB is widely used as a rapid prototyping tool for fabrication of micro/nano electronic devices and for circuit repair since the technique enables site-specific removal of material. Due to absence of a resist layer, higher patterning resolution than conventional lithography methods is expected. That is, parameters such as proximity effect, resist layer uniformity, undercut (profile) of resist layer and sample development are absent and do not affect the patterning resolution.

The helium-ion microscope with its sub-nm resolution is considered as a versatile-high-resolution-resist-free patterning tool and has found a wide range of applications in the field of nano sciences. In this section, we present a brief experimental review on He-ion beam milling for fabrication of high resolution nano devices.

4.3.1 Plasmonic nano devices

Fabrication of plasmonic devices by He-ion milling is a very recent application for the Carl Zeiss OrionTM Plus HIM, which has made an enormous impact in this field in a short time.

Plasmonic devices such as optical antennas are very attractive devices for different applications, e.g. biosensing. For instance, in a plasmonic dipole antenna, reducing the gap size between the two metallic (gold) islands increases the sensitivity of the antenna for sensing applications. However, to employ this device for single molecule detection a gap size of 3 nm [156] is required. So far, the resolution of the EBL fabricated devices are limited to ~10 nm [157], [158] after pattern transfer on thin silicon nitride membranes. Unfortunately, membranes are very fragile and have limited size and for the case of bulk substrates, due to proximity effect and backscattering of electrons, the resolution of the gap size is 15-20 nm [159]. Ga-FIB milling was also demonstrated to be capable of fabricating gap sizes ~15 nm in single crystalline gold flakes [160]. Recently, using He-ion beam milling, Scholder *et al.* [38] demonstrated a plasmonic antenna with a gap size of ~3.5 nm for the first time, with a

precision of ~ 1 nm. Owing to the resolution achieved for the gap size, a much higher sensitivity for the antenna was reported. Furthermore, He-ion milling was also reported for fabricating sub-5 nm partially loaded plasmonic nano antennas [37]. Using a top-down milling approach, the authors demonstrated removal of the Au layer with precision of 1 nm, achieving a nanometre-sized-thick metallic bridge in the gap and greatly improving the sensitivity of the antenna with this geometry (i.e. smaller thickness to its width).

Perhaps, the most fascinating result was reported by Lawrence Berkeley National laboratory in collaboration with Carl Zeiss (Peabody) for fabrication of coaxial optical antennae with sub-10 nm critical dimension. Remarkably, their He-ion beam fabricated antennae matched the theoretically predicated quality factor for the idealised flawless gold resonators (shown in Figure 4.5(b)) [36].

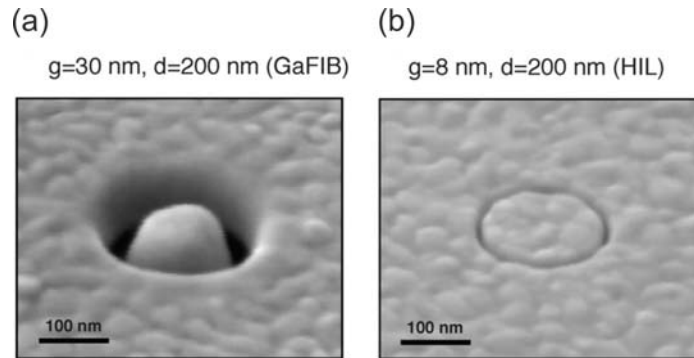


Figure 4.5 – SEM images. Resolution comparison between (a) Ga-FIB milling and (b) HIM milling fabricated plasmonic nanoresonators where g and d are the gap size and the diameter of the coaxial antenna, respectively. Figures from ref. [36].

4.3.2 Graphene nano devices

To date, the nano patterning of graphene flakes into GNRs is most convincingly demonstrated by HIM milling, both for suspended and non-suspended graphene samples. Direct milling of graphene using the HIM has been demonstrated recently [33], [161]–[163] as a high resolution,

resist-free patterning technique. Note that in all the following works the He-ion beam is operated at 30 keV acceleration voltage, unless stated otherwise.

Initially, Bell *et al.* showed the successful milling of a monolayer graphene sheet on a typical SiO₂/Si substrate [33], [34]. By varying the beam dwell time a dose test was conducted, shown in Figure 4.6(a), to ascertain the optimal operation point for He-ion milling. The dose test indicated a suitable dose of 10-15 nC/cm for milling a graphene flake. A detailed AFM analysis measured a depth of 4 nm in the substrate for a dose of 20 nC/cm. It was also found that for very large doses the underlying substrate can swell by at least 50 nm from the effect of ion knock-on damage to the underlying silicon layer. The swelling effect is shown in Figure 4.6(b,c) [33].

Livengood *et al.* discovered that the swelling effect is due to accumulation of helium ions in the underlying substrate, leading to the formation of nano-bubbles which grow and eventually coalesce to form voids as the dose is increased [164]. We discuss the swelling effect extensively in section 4.5, where we address the issues associated with HIM milling.

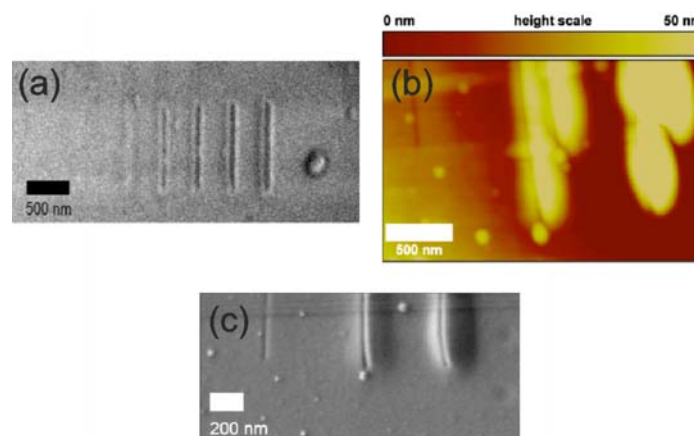


Figure 4.6 – (a) He-ion SE image of a dose test in a monolayer graphene flake on a SiO₂/Si substrate, showing a range of doses from 3 to 15 nC/cm in 3 nC/cm steps (left to right) with the total patterning time varying between 3 and 6 s. (b) AFM and (c) SEM imaging of a pattern milled with 20, 100 and 200 nC/cm dose (left to right) revealed swelling of the underlying substrate by at least 50 nm due to ion knock-on damage. Figures from ref. [33].

Employing the same milling technique, Boden *et al.* demonstrated patterning of monolayer graphene flakes with a variety of QDs device designs [162]. Using the pattern generator integrated into the HIM software, the beam was scanned in a pattern defined by a bitmap to form the device designs into a pristine monolayer graphene flake with minimum feature size of <10 nm (see Figure 4.7).

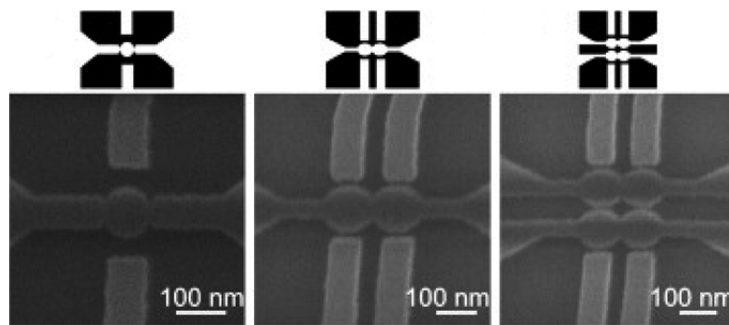


Figure 4.7 – HIM SE images of different QDs device designs fabricated on a monolayer graphene flake. The bitmap designs are shown above each image (black areas indicate the milled regions). Figures from ref. [162].

He-ion beam propagation into graphene on a SiO_2/Si substrate calculated using TRIM software package [165], [166] has demonstrated that moving to suspended graphene samples could reduce backscattered ion damage (see Figure 4.8(a,b)) [33], [34] and ultimately improves pattern resolution, but at the expense of more complicated fabrications procedures.

The superior milling resolution, due to minimisation of backscattered ion damage, in suspended graphene samples was demonstrated experimentally by Pickard *et al.* This included milling on a suspended graphene flake to form a 5 nm wide nano ribbon with a remarkable 60:1 aspect ratio (shown in Figure 4.8(c,d)), for a He-dose of 2.79×10^{18} ions/cm² [161].

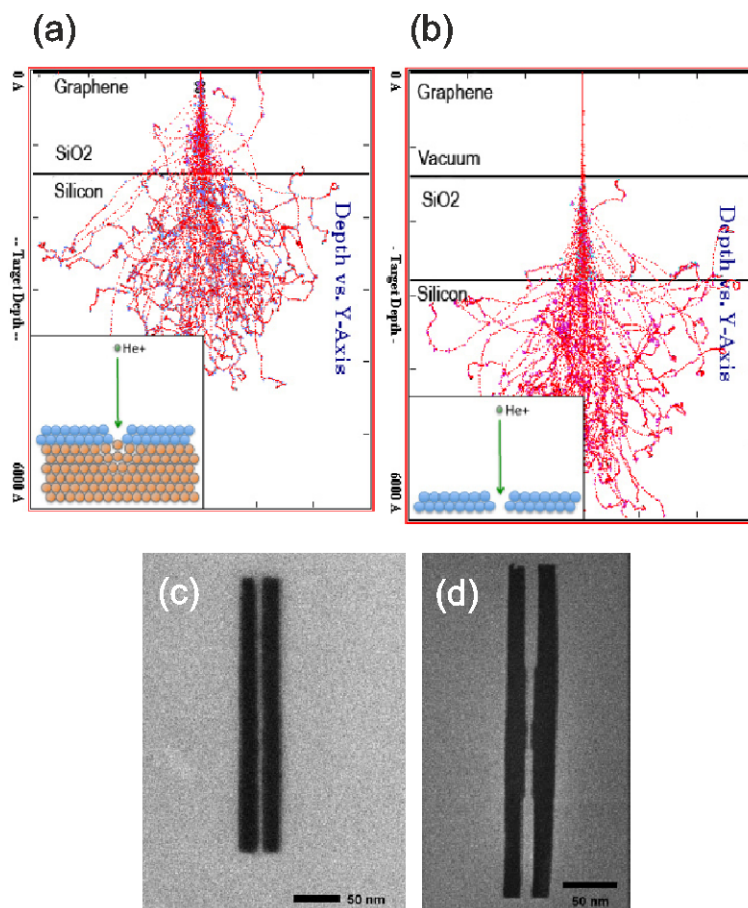


Figure 4.8 – TRIM software [166] simulations comparing He-ion beam propagation into graphene on a SiO₂/Si substrate for (a) non-suspended and (b) suspended graphene flakes [33]. (c) HIM SE image of a 5 nm-wide suspended GNR patterned by He-ion beam milling with a 60:1 aspect ratio. (d) HIM SE image of more complex patterning on a suspended graphene flake, with the GNR width starting at 20 nm and going down to 5 nm. Figures (a,b) and figures (c,d) are from refs. [33] and [161], respectively.

Furthermore, Lemme *et al.* demonstrated the cutting of metal contacted suspended graphene flakes with HIM, with electrical measurements before and after confirming milling through the flake, with a minimum feature size of 10 nm [163]. In this work, etching was achieved by imaging the graphene with a He-ion beam instead of patterning it at a specific He-dose. Once etching of the flake was confirmed by live imaging, the measured current through the device had dropped to about 15 pA from 1 μ A prior to the etching. Since the latter current corresponded to the noise level of the measurement tool, the authors confirmed successful

etching of the graphene sample. The authors also performed an etching attempt on a non-suspended graphene sample on an SiO_2/Si substrate, with a He-dose of 1.5 nC/cm. Here, the residual current through the flake saturated at ~ 4 nA (from an original, pre-milling value of above 0.9 μA), which was attributed to hydrocarbon contamination on the SiO_2 substrate in the milled area [163].

Recently, in a novel attempt, He-ion beam irradiation was employed to create defects for tuning carrier transport in GNRs [39]. In this work, an area of $W_{irr} \times L_{irr}$ (see Figure 4.9(a)) in a GNR (fabricated by HIM milling with 200 nm length and 50 nm width) was exposed to an He-ion beam with different He-doses (ranging from 2.2×10^{15} to 1.3×10^{16} ions/ cm^2), and so resulting in 0.2-1.3% embedded point defects density in the irradiated regions [39]. Note that the defect density in the irradiated region was calculated based on (i) He-dose, (ii) carbon atom density in a graphene sheet of $3.8 \times 10^{15} \text{ cm}^{-2}$, and (iii) the percentage of He-ions that interact with carbon atoms is only 0.4% [39]. The bias current through the irradiated GNRs exponentially decayed with increasing the defect density, which implied the induction of defects by the irradiation (Figure 4.9(c,d)). Interestingly, based on the Raman spectra collected from the irradiated samples (shown in Figure 4.9(b)), the authors revealed that although the D peak enhanced as the defect density was increased but even at high He-dose exposures (i.e. 1.3% defect density in the channel of the device) and the devices almost insulating, the G mode peak is apparent, so suggesting that the honeycomb structure of graphene remains and the exponential decrease in the bias current occurs without essential change in the crystalline structure. Further investigations also indicated that the conductance decays exponentially as the length of the irradiated region (L_{irr}) increases, suggesting that the carrier transport is dominated by strong localization of carriers at the localization sites induced by the defects.

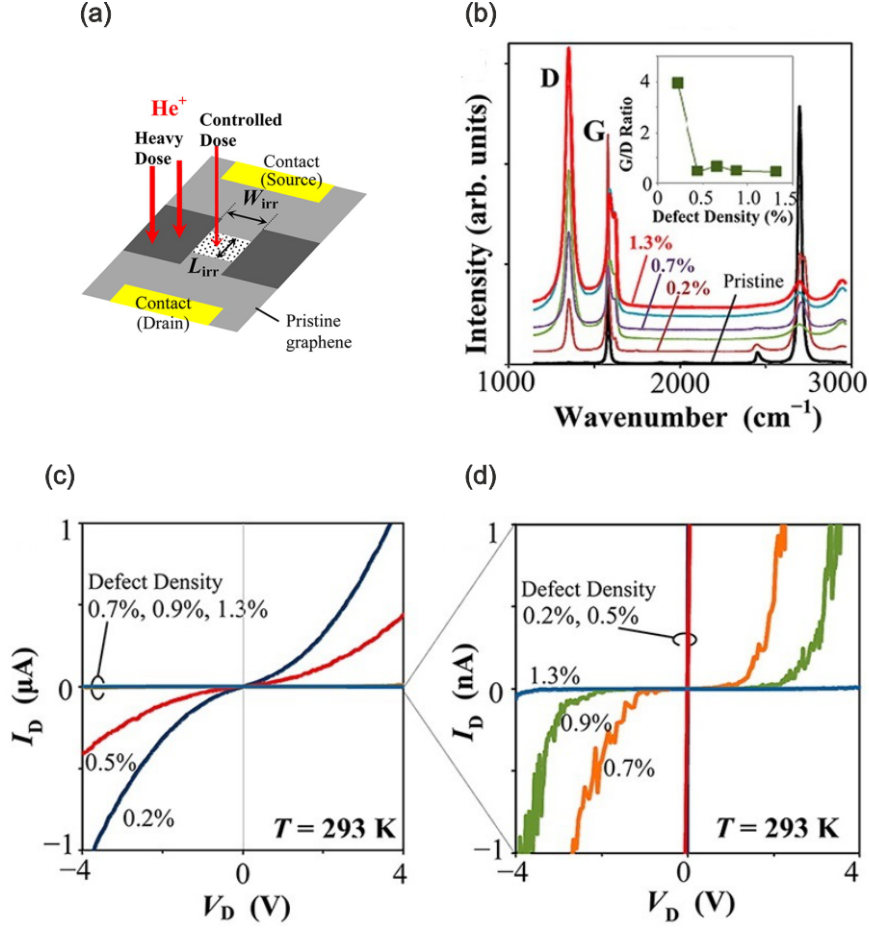


Figure 4.9 – (a) Schematic illustration of the experiment by Nakaharai *et al.*, where W_{irr} and L_{irr} represent the width and the length of the irradiated regions, respectively. (b) Raman spectra collected from the irradiated samples with He-dose ranging from 2.2×10^{15} to 1.3×10^{16} ions/ cm^2 . (c) and (d) Exponential decay in the bias current with increasing the He-dose for an irradiated region of $W_{irr} = 50 nm$ and $L_{irr} = 30 nm$. All figure from ref. [39].

4.3.3 Other applications

In a fascinating experiment on thin SiN membranes, repeatable and reliable fabrication of nanopores with high control on the diameter of the nanopores with minimum diameter of 4 nm was demonstrated [167]. Interestingly, the HIM milling was also found to be faster and offering higher throughput (allowing multiple sample loading) for fabrication of nanopores than Transmission Electron Microscopy (TEM) milling, which has been an established method for fabricating nanopores [167].

Successful fabrication of vias with 5 nm precision and very sharp sidewall angles (ranging from 88°-90°) with a He-ion beam in a 100 nm-thick layer of Au on a silicon substrate as well as a freestanding Au layer (with the same thickness) demonstrated the huge potential of HIM milling for creation of transducers with sensing abilities in nanometre scale [168], [169].

In other attempts, HIM milling was used for fabrication of magnetoresistance spin valve devices with sub-20 nm gap widths [170].

4.4 Fabrication of GDQD by HIM milling

In this section, we discuss our novel hybrid fabrication method that combines conventional e-beam lithography and HIM milling to fabricate GDQD devices.

4.4.1 Sample preparation

Schematic illustration of the steps involved in our fabrication process is demonstrated in Figure 4.3. Since the aim of this chapter is to focus on He-ion beam milling, to avoid inconsistency, the fabrication steps 1-3 will be explained in great detail in Chapter 5. However, before explaining the fabrication step 4 (see Figure 4.3), we would like to point out some information regarding the fabrication steps 2 and 3 (see Figure 4.3).

First, the fine helium ion beam milled features would be damaged during resist spin-coating and lift-off processes and so the fabrication of metal contacts onto graphene flakes had to be carried out prior to HIM milling.

Second, it is desirable to minimise total HIM milling time because drifting of the sample during the milling can jeopardise pattern fidelity for long exposure times. For instance, one can notice that the milled patterns (shown in Figure 4.7) by Boden *et al.* [162] experienced noticeable distortions due to long milling times (i.e. 4-5 minutes). Therefore, to minimise the milling time, we performed a EBL/RIE step (step 3 in Figure 4.3) to introduce isolation lines on the graphene flakes, separating the metal contacts and leaving an area of approximately

500 nm \times 420 nm for the final HIM milling step. HIM secondary electron (SE) images of a graphene flake after fabricating the metal contacts and the isolation lines are shown in Figure 4.10.

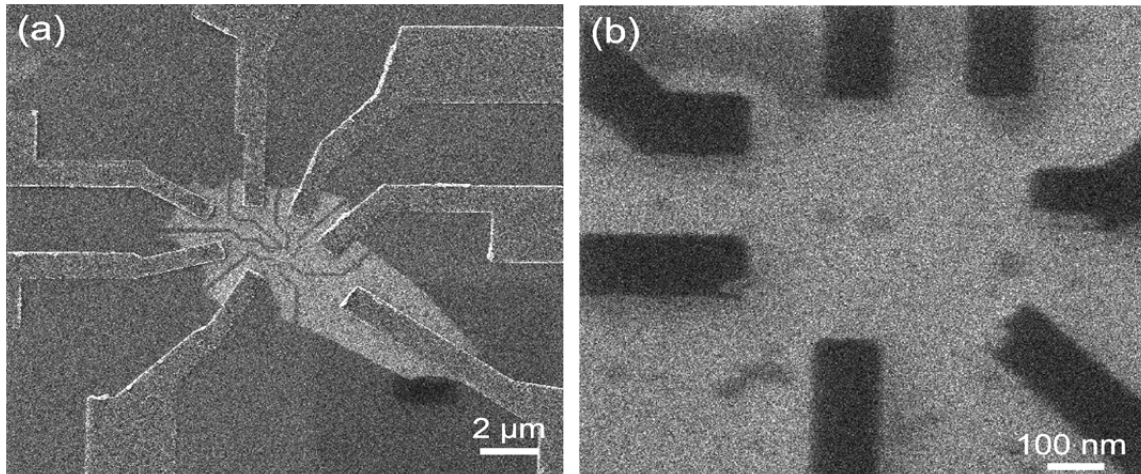


Figure 4.10 – (a) HIM SE image of a monolayer graphene flake with metal contacts and RIE-formed isolation lines. (b) HIM SE image of the etched isolation lines (dark lines in the figure) which are forming an area of ~ 500 nm \times 420 nm on the flake that was left intact for the final HIM patterning step.

Introducing the isolation lines on the flakes by this method greatly reduced the He-ion milling exposure time by reducing the amount of graphene that needed to be milled by the He-ion beam to isolate the pattern. This allowed milling of complex patterns in graphene whilst avoiding the problem of distortion due to drift. Having done this, the next step is to set-up the optimum alignment conditions for the He-ion beam.

4.4.2 Setting-up a He-ion beam

To minimize possible beam-induced hydrocarbon deposition during graphene milling by the He-ion beam, the HIM chamber was cleaned overnight using the integrated Evactron RF plasma cleaner (XEI Scientific, Inc.) at 10 W with at least 10 on/off (15 min/45 min) cycles.

For HIM milling, alignment of the beam to get the best possible image from the surface of the desired substrate (with a beam current suitable for milling) is essential for high resolution patterning. A 10 μm diameter mid-column aperture was selected and the beam was operated with a beam current of 1 pA at an accelerating voltage of 30 keV. The beam current can be tuned by varying the helium pressure at the source (see Figure 4.4(b) for the schematic of the HIM column). Beam optimization was performed whilst imaging a standard resolution test specimen consisting of tin particles on a carbon (Tin on C) substrate (Agar Scientific) to ensure the smallest possible probe size. Figure 4.11 shows HIM SE images of the Tin on C sample, taken under optimum beam conditions.

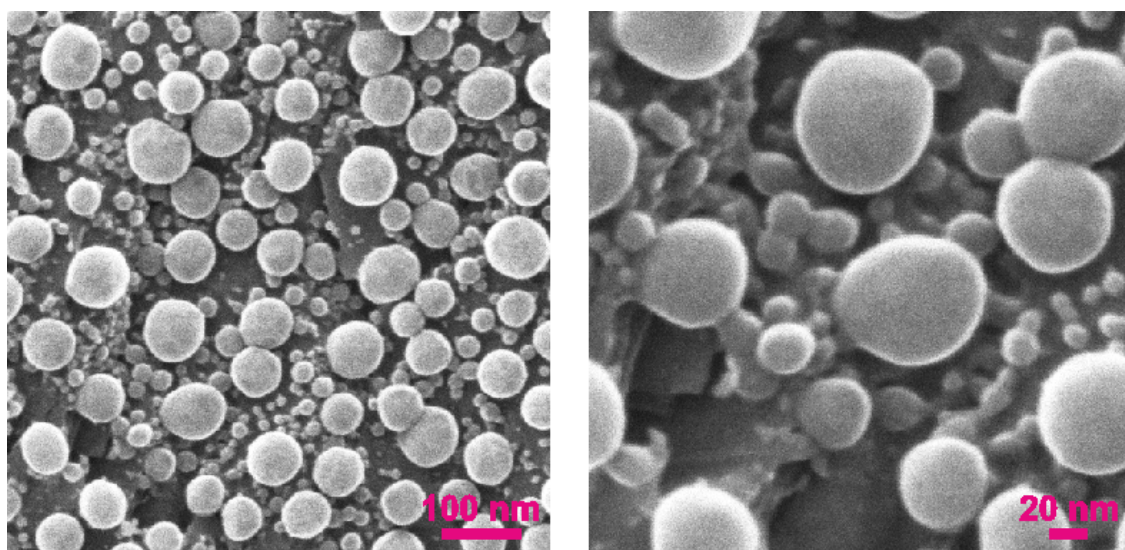


Figure 4.11 – HIM SE images of the Tin on C sample. The images show the staggering resolution of the HIM for feature sizes much smaller than 20 nm.

4.4.3 HIM milling on pristine graphene samples

After obtaining the optimum imaging resolution on the Tin on C sample, the beam was moved to a pristine graphene sample (i.e. a fresh mechanically exfoliated graphene) and the desired flake was manually located. This was achieved using the fabricated alignment marks (see

Figure 5.2(b)), by secondary electron (SE) imaging at low magnifications. The helium beam was then focused onto the graphene surface by imaging an edge of the graphene flake. This provided edge contrast needed for fine focus adjustment and minimized exposure (and so possible damage) to the central area of the flake. Figure 4.12 shows the edge of a monolayer graphene flake imaged with a well-conditioned He-ion beam.

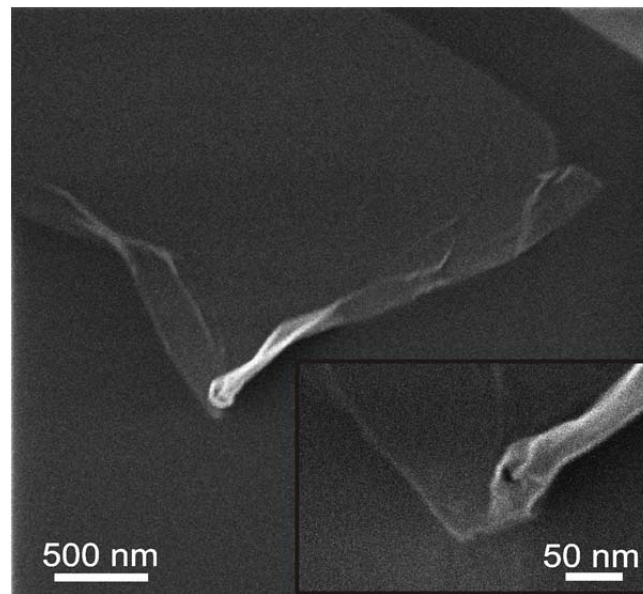


Figure 4.12 – HIM SE images of an edge of a monolayer graphene flake at low magnification and high magnification (inset). The flake edges were imaged at high magnifications to ensure optimum focus.

To ensure optimum focus on a graphene flake, there are two issues that must be considered:

I) We used a high scanning rate of 3 μsec (low imaging resolution). That is, carbon atoms are constantly milled once they are exposed to a beam of high energy helium ions. This step is very challenging for a case of a monolayer graphene flake but is easier as the number of carbon layers is increased (i.e. thicker graphene flakes). Indeed, obtaining optimum focus with such a high scanning rate is very challenging and requires decent user skills with the microscope.

II) In general, as discussed by other works [39]–[44] (also see section 5.5 for a detail discussion), graphene samples are very susceptible to beam irradiation. Beam irradiation results in creation of defects (appearance of the D-peak in the Raman spectrum) and modification of the atomic structure and the electronic properties of graphene samples. Therefore, it is important that an area away from the device region on the flake is chosen for performing the HIM focusing step.

After achieving the optimum focus, the magnification was reduced, the stage was moved to place an area of the flake at the centre of the field of view and the beam was blanked. We employed the internal pattern generator of the microscope to mill our graphene samples. Figure 4.13 shows the control panel for the internal pattern generator of the HIM.

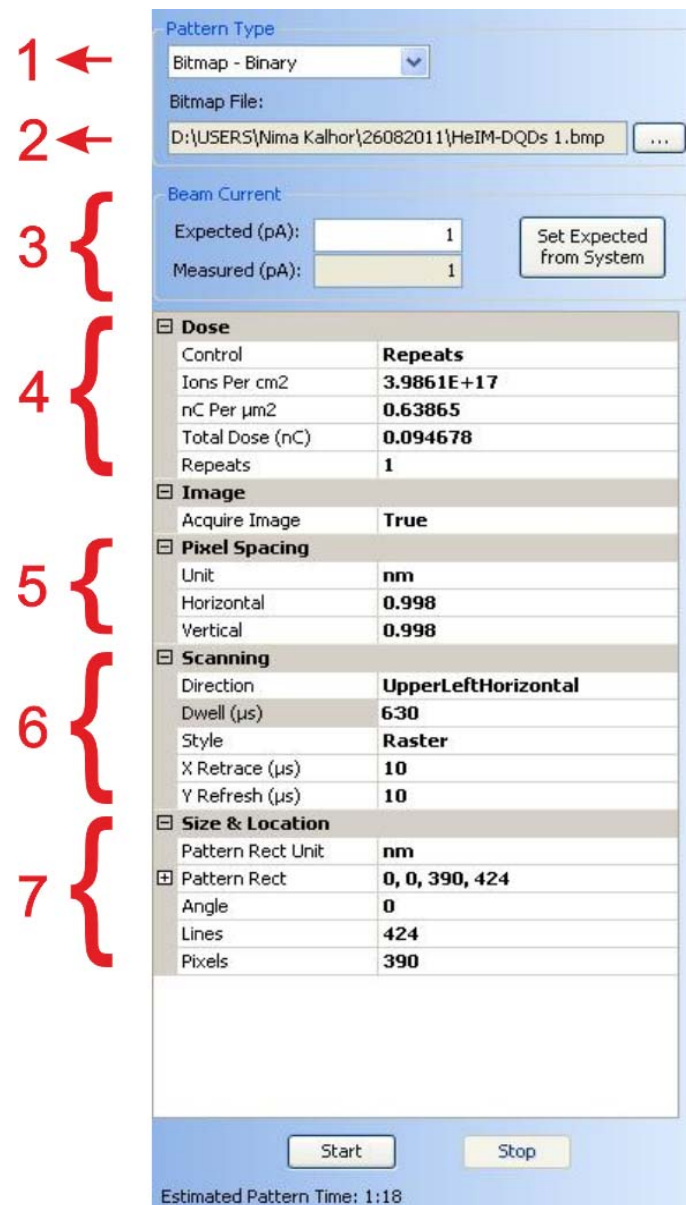


Figure 4.13 – The control panel of the internal pattern generator of the Carl Zeiss Orion™ Plus HIM.

Here, we provide a brief explanation for each set of parameters (labelled by numbers in Figure 4.13) in the internal pattern generator software that should be considered for obtaining optimum milling results.

- 1) There are two pattern types that can be imported into the internal paternal generator, i.e. Bitmap-binary and Dwell map. We used Bitmap-binary. Dwell map can be used when different He-doses are required to be applied to each pixel of a desired pattern.

- 2) The location of the pattern file can be chosen in here.
- 3) By assigning a value to the “Expected” beam current, and based on the values entered in the parameters labelled as 4-7 in Figure 4.13, users are allowed to calculate the He-ion beam dose prior to HIM milling. The “Measured” beam current is the current measured by the microscope.
- 4) This menu shows the He-ion beam dose (calculated in three different units by the pattern generator as shown in Figure 4.13) applied to each pixel of the pattern based on the beam current, the pixel spacing and the beam dwell time. In addition, “Repeat” parameter corresponds to the number of times that the beam scans over a pattern. Therefore, the He-ion beam dose increases with the value of “Repeat” parameter.
- 5) The pixel spacing is identical to shot pitch (also known as shot step) parameter in conventional e-beam lithography and is the beam stepping distance. Here, we have chosen a 1 nm pixel spacing for high resolution milling.
- 6) In this menu, the most important parameter is the dwell time. The dwell time is the time that the beam dwells (exposes) at each pixel of a pattern. Furthermore, “Direction” parameter allows users to choose different milling strategies (i.e. the manner that the beam scans a pattern).
- 7) This menu allows users to define the pattern size (i.e. desired exposure area).

Finally, the pattern generator automatically estimates the milling time (exposure time) based on the values of the above parameters (e.g. 1:18 minutes based on the parameters entered in Figure 4.13).

We conducted extensive series of dose tests to find the optimum value for each of the above parameters for graphene milling. The dose tests were performed on pristine exfoliated graphene flakes.

Initially, the 202×200 pixels binary bitmap image shown in Figure 4.14(a) was imported into the integrated pattern generator for dose tests. A wide range of dose tests were then conducted by varying the dwell time, pixel spacing and beam current. The objective of the dose tests was to find the optimum dose for complete removal of graphene in the exposed areas (black areas in the Figure 4.14(a)) by looking for good contrast of the milled features with respect to the rest of the flake in the post-exposure HIM SE image. Figure 4.14(b) shows the structure

generated during a milling attempt with a dwell time of 540 μs and ~ 1 nm pixel spacing (a total dose of $0.54 \text{ nC}/\mu\text{m}^2$) which resulted in only partial milling of the pattern. The edges of the pattern and the narrow gaps between the side gates and DQD structure are not well defined. However, with a dwell time of 630 μs and ~ 1 nm pixel spacing, which resulted in a total dose of $0.63 \text{ nC}/\mu\text{m}^2$, the resulting pattern was well defined in graphene, with good contrast between exposed and unexposed regions and sharp edge features (Figure 4.14(c)). The diameters of the QD are ~ 26 nm, the constrictions on either side are ~ 12 nm wide and the distances between the side-gates and the QDs are ~ 8 nm.

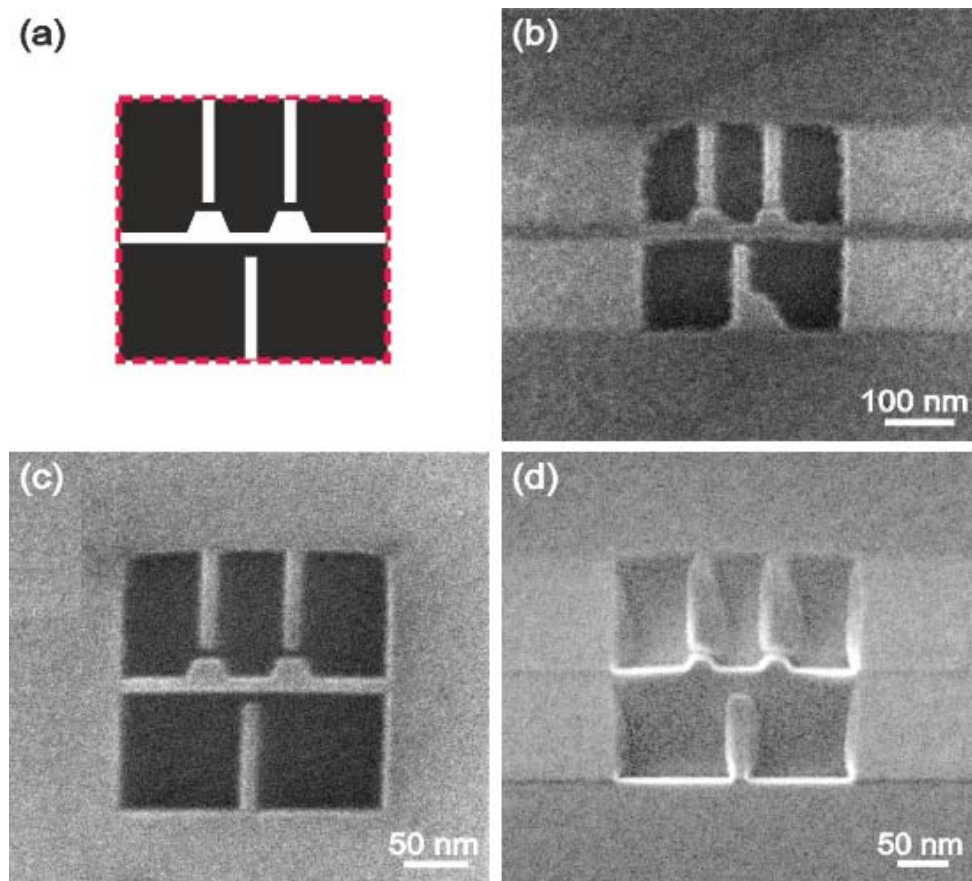


Figure 4.14 – (a) The 202×200 pixel bitmap image of a DQD design. (b) HIM SE image of an area of pristine monolayer graphene flake with a partially milled DQD pattern. (c) HIM SE image of a well-defined DQD pattern milled into a pristine monolayer graphene flake with a He-beam dose of $0.63 \text{ nC}/\mu\text{m}^2$. (d) Surface distortion at high He-doses, due to ion knock-on damage and helium accumulation in the underlying substrate.

These measurements match well to the original pattern design, demonstrating the faithful reproduction of the design with no evidence of the asymmetries that can blight e-beam fabricated devices as shown in Figure 4.1 and in other works [112], [135], [140], [141]. These asymmetries can result from existence of graphite pieces, metallic alignment marks, and roughness of the SiO_2 substrate which may hinder the homogeneous coating of a thin layer of resist onto the sample. Moreover, parameters such as proximity effect, e-beam spot size and sensitivity of the development step of the e-beam exposed patterns can affect the resolution of e-beam lithography. By using a resist-free method such as HIM milling for the final patterning step, these problems are avoided and symmetrical QD designs can be accurately fabricated. Very high He doses can lead to swelling in the underlying substrate due to accumulation of helium, leading to the formation of nano-bubbles which grow and eventually coalesce to form voids as the dose is increased [164]. This causes distortion of the pattern on the surface as is evident in Figure 4.14(d) and in other work [33] and so the applied He dose should be limited to avoid this effect. As we previously mentioned, the detail discussion on the swelling effect due to He-ion bombardment of the substrate is provided in section 4.5, where we address all the issues associated with the HIM milling technique.

4.4.4 HIM milling on e-beam processed graphene samples

Having optimized the exposure parameters on pristine flakes based on HIM inspection of the fabricated pattern, milling was attempted on e-beam processed, metal contacted flakes. Bitmap designs of DQD patterns were prepared based on the arrangement of isolation lines from e-beam processing. An example of a DQD pattern aligned to the isolation lines on a contacted graphene flake, in the integrated HIM pattern generator software, is shown in Figure 4.15.

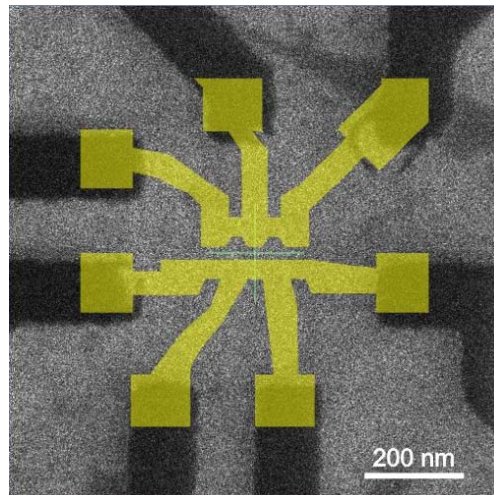


Figure 4.15 – HIM SE image of alignment between the e-beam lithography pattern and the HIM pattern.

Initially, milling using the procedure developed for pristine flakes was not successful when applied to e-beam processed samples, as shown in Figure 4.16. The milled patterns were not so clearly defined compared to those produced on pristine flakes and there was evidence of accumulation, due to hydrocarbon contamination on graphene surface, rather than removal of material in the scanned area. Hydrocarbon contaminations (i.e. organic contamination) can be efficiently cross-linked by the He-ion beam, resulting in build-up of material in beam scanned areas and so preventing successful milling [170], [171].

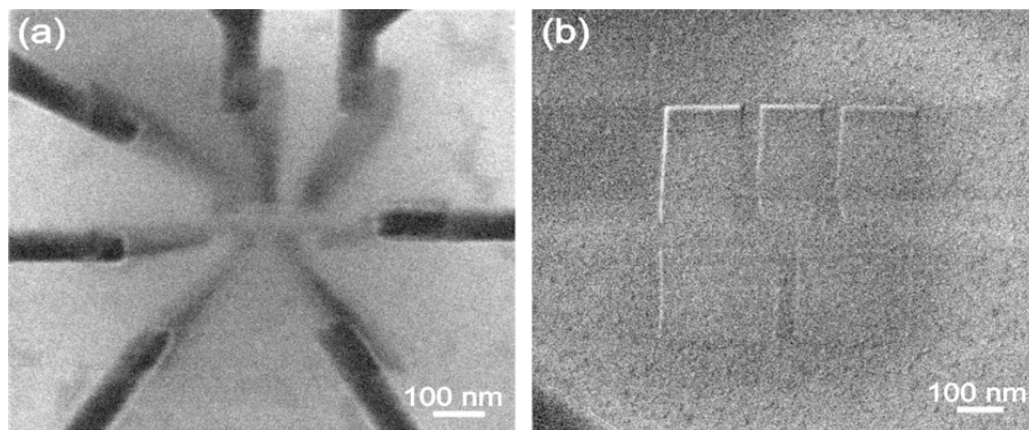


Figure 4.16 – HIM SE images. (a) A poorly defined DQD pattern on one of the prepared monolayer graphene samples after HIM milling with a dose of $0.63 \text{ nC}/\mu\text{m}^2$. (b) A typical milling result for doses ranging from $0.6\text{-}0.7 \text{ nC}/\mu\text{m}^2$.

It was Ishigami *et al.* who initially reported that exposing graphene flakes to solvents and/or resists can lead to production of a continuous film of residues on the surface of the flakes, affecting their thickness and their surface roughness [172]. This was discovered when the authors could not observe triangular and hexagonal lattice patterns by Scanning Tunnelling Microscopy (STM) on graphene samples that had undergone processing with resists. Moreover, they proposed that annealing of processed graphene flakes in forming gas (Ar/H_2) is an effective way to remove these surface contaminants. Since then, although annealing in forming gas is still a popular method for removing the surface contaminants but, other cleaning methods such as wet-chemical cleaning in chloroform [173], annealing in a vacuum chamber [173], rapid thermal annealing (RTA) [174] and current annealing are also proposed [9]. Furthermore, as we will discuss in section 6.2.1, it has been reported that organic contaminants can affect the electrical properties of graphene by spurious doping of graphene flakes [9].

Hence, we conducted extensive series of annealing test runs to develop the required conditions for removing the surface contaminants. This included tuning of the annealing temperature, annealing time and gas flow rate. After each annealing run, the sample was then tested for

HIM milling. The objective was to be able to mill the samples with the optimum He-dose obtained from milling pristine samples, i.e. $0.63 \text{ nC}/\mu\text{m}^2$.

To do this, tens of graphene samples were produced by mechanical exfoliation and were exposed to resists and solvents. The samples were then heat treated at different temperatures (250-400 °C) for different durations (1-3 hours) in forming gas (6% H_2 and 94% N_2) with different gas flow rates (0.5-2.5 Lit/min). After several iterations to optimize the procedure, it was found that annealing the e-beam processed samples at ~ 320 °C in 1.3 L/min forming gas flow (6% H_2 and 94% N_2) for 2 hours in an atmospheric pressure furnace results in removal of surface contaminants sufficient to allow successful HIM milling of DQD patterns, using a dose of $0.63 \text{ nC}/\mu\text{m}^2$ (the dose optimised on pristine monolayer flakes). An HIM SE image, taken immediately after the HIM milling step, of a device that was successfully fabricated on an annealed sample is shown in Figure 4.17. The image shows remarkably well-defined symmetrical features milled on a monolayer graphene flake. Here, the diameter of the dots is ~ 50 nm and the channel width is ~ 30 nm. In addition, the HIM milled isolation lines are shown to connect well to the isolation lines defined by e-beam lithography, demonstrating excellent alignment between the two patterns.

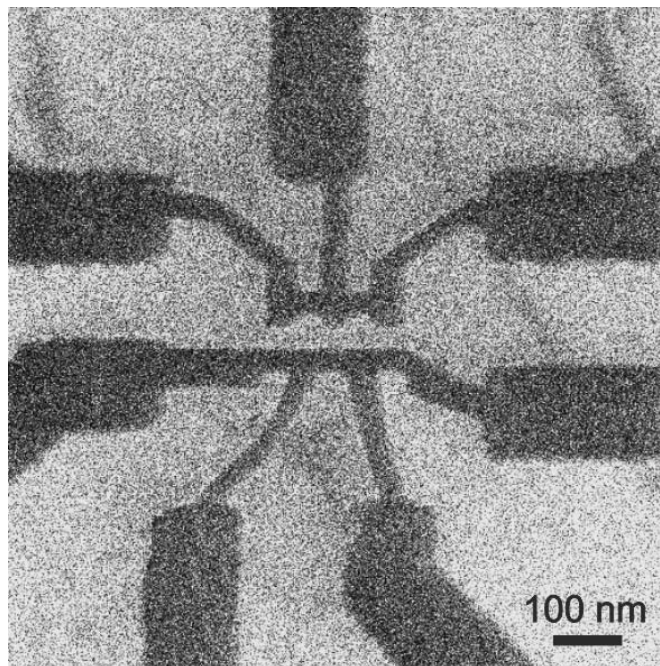


Figure 4.17 – HIM SE image of a well-defined He-ion milled DQD pattern with excellent alignment with the isolation lines defined by e-beam lithography.

However, the Raman spectrum collected from one of the graphene samples after annealing is shown in Figure 4.18(a). Indeed, the spectrum looks very different compare to that of shown for a pristine graphene in Figure 5.4(c). The sharper G peak along with the smaller $I(2D)/I(G)$ ratio in the Raman spectrum after annealing signifies the expected high hole doping density in the samples after the annealing process [175]–[177]. Although the exact nature of the hole doping in graphene after annealing in a forming gas flow is still unknown but, Liu *et al.* [175] suggested that the doping could be due to release of O_2 from the SiO_2 during the annealing, or structural deformation of the flake by the heat which allows it to react with atmospheric O_2 once the samples is taken out of the furnace [175]. The presence of the D peak in the Raman spectrum also indicates some defect generation in the graphene, however, the $I(D)/I(G)$ ratio is still relatively small and so the level of damage induced by the annealing step is considered to be minimal.

Contrary to the report by Liu *et al.* [175], we found that it is possible to prevent the hole doping effect in graphene samples after annealing process. To restore the doping level in the

annealed samples to that of pristine samples, we made two important changes in our annealing recipe. First, we added a 1 hour-long annealing step at ~ 320 °C in 3 L/min Ar gas flow (inert gas environment). Second, the temperature was cooled down to room temperature (i.e. 25 °C) before unloading the samples. The resultant Raman spectrum after annealing is shown in Figure 4.18(b). Remarkably, the spectrum exhibits the characteristics G and 2D peaks of monolayer graphene (high $I(2D)/I(G)$ ratio), with a very small D peak, indicating that the process does not induce many defects and therefore does not adversely affect the quality of the graphene flake. Table 4.1 presents the full details of our optimised annealing process which resulted in the Raman spectrum in Figure 4.18(b).

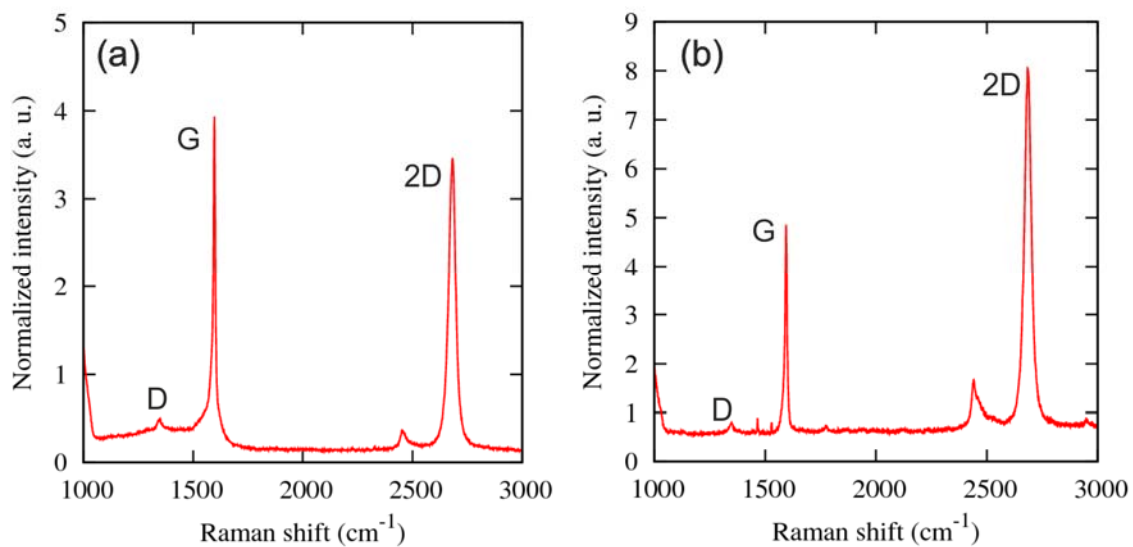


Figure 4.18 – Raman spectra of annealed graphene samples, (a) in 1.3 L/min forming gas flow at ~ 320 °C for 2 hours, (b) in 1.3 L/min forming gas flow at ~ 320 °C for 2 hours and in 3 L/min Ar gas flow for one hour. The Raman spectra were collected using a Renishaw InVia Raman spectrometer with a 532 nm wavelength laser, a laser excitation energy of $E_{\text{laser}} = 2.33$ eV and a $\times 100$ objective lens (numerical aperture of 0.8) which resulted in a laser spot size radius of ~ 400 nm. The graphene flakes were identified at a laser power of 0.2 mW with a 100 seconds exposure time.

TABLE 4.1

A process flow sheet. The steps involved in our annealing process for removing contaminants on the surface of processed graphene samples.

Process description	Temperature	Gas flow	Duration
Forming gas purge	25 °C	N ₂ /H ₂ at a rate of 3 L/min	15 minutes
Temperature ramp-up	25-320 °C	N ₂ /H ₂ at a rate of 1.3 L/min	25 minutes
Annealing in forming gas	320 °C	N ₂ /H ₂ at a rate of 1.3 L/min	2 hours
Annealing in argon	320 °C	Ar at a rate of 3 L/min	1 hour
Temperature cool-down	320-25 °C	Ar at a rate of 3 L/min	7 hours

Note that the details/conditions of all the process steps involved in our HIM fabrication method are presented systematically as a process flow sheet in Appendix B.

4.5 Challenges and issues associated with He-ion milling

Owing to its sub-nm probe size at the sample surface and the fact that, unlike gallium ions, helium ions are non-contaminating, He-ion milling can offer whole new possibilities for high resolution patterning. However, this comes at the expense of number of issues that we address here.

I) Hydrocarbon contamination can impact the milling results considerably. This issue can originate from two sources, i.e. cleanliness of the HIM chamber and the sample contamination. Interaction between the primary ions and contaminant molecules in the chamber can promote the growth of carbonaceous materials on the surface of the sample. Therefore, as we mentioned in section 4.4.2, to minimise possible beam-induced hydrocarbon deposition by the He-ion

beam, the HIM chamber is cleaned using the integrated Evactron RF oxygen plasma cleaner (XEI Scientific, Inc.) in the main chamber at 10-12 W with at least 10 on/off (15 min/45 min) cycles generally prior to milling [33], [34], [169], [178]. In addition, the classic sample contamination concern is even more susceptible for a He-ion beam, due to its high surface sensitivity and the resultant interaction of the primary ions and generated secondary electrons with the contaminant molecules [179], compare to an electron beam. The contaminants can be cross-linked and migrate on the sample surface by the helium beam and build-up in the beam scanned region and so preventing successful milling. In section 4.4.4, we discussed this issue for the case of processed graphene samples and we demonstrated that desired milling results can be achieved by annealing the samples prior to HIM milling.

It is worth mentioning that soaking samples in *N-Methyl-2-Pyrrolidone* (NMP) at room temperature followed by a rinse in *2-Propanol* (IPA) was reported to be a good method for cleaning metallic samples prior to HIM milling [37], [170].

II) Although the lighter mass of He ions compare to Ga ions results in less parasitic sputtering while imaging a sample but, it also offers a lower sputtering yield which hampers the milling of hard/thick substrates or large scale features. In thick substrates, as the milling proceeds, re-deposition on the side walls of the milling area is a competing factor and gradual change of the angle of incidence of the primary ions on the substrate make it increasingly difficult to sputter material and can lead to sloped side walls in final trench and/or vias milled patterns [170]. Indeed, to achieve higher sputtering yields a larger beam current (and so higher He-dose) may offer desirable results for some cases but it can also result in a more complicated outcome, known as swelling effect. In case of a silicon substrate, at He-dose of 1.6×10^{17} ions/cm² the area under the ion propagation path becomes completely amorphous and is accompanied by creation of nanobubbles with diameter ranging from sub-1 to 3 nm in the amorphous region. In the amorphous region, due to its poor solubility of He ions, the ions trap at subsurface and deform the amorphous surface layer to form balloon-shape features at room temperature. Furthermore, higher He-doses result in bigger nanobubbles and bursting of the balloons (and so producing voids in the substrate) due to the build-up of pressure inside them [164].

III) Another issue associated with a He-ion beam is the beam damage during imaging of thin substrates and/or milled patterns on delicate substrates, e.g. graphene. The beam damage on

graphene samples is a complicated subject since even low He-doses can result in induction of different types of defects in graphene lattice [39]. As discussed in section 4.3.2, this was used neatly by Nakaharai *et al.* [180] to tune carrier transport in GNRs. But generally, due to higher mass of helium ions compare to electrons, HIM imaging prior and after milling can cause damage to the substrate as well as fine milled features and therefore, should be avoided. Figure 4.19 shows a good example of the damaged caused on milled features on a graphene sample after HIM imaging where our fine quantum dot features disappeared (milled away). Therefore, alternative imaging methods, e.g. SEM, should be considered to prevent such damages on thin/sensitive samples.

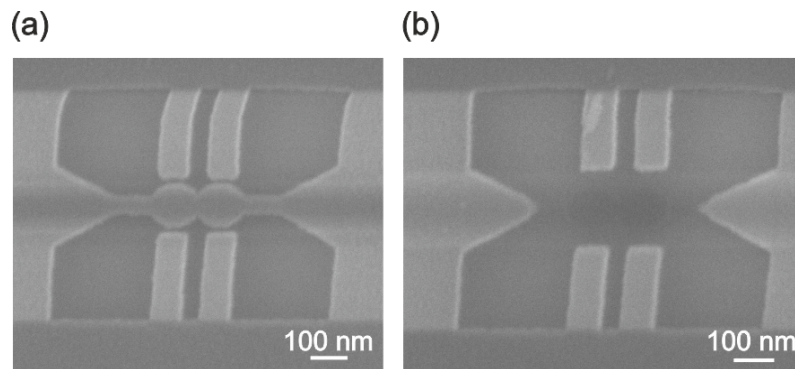


Figure 4.19 – HIM SE images. (a) A DQD structure milled on a monolayer graphene flake. (b) The damage caused on fine milled patterns after HIM imaging, where as a result, the fine double quantum dots structure was milled away.

IV) Possible existence of sub-micrometre features such as wrinkles and rough edges in graphene flakes produced by mechanical exfoliation can hinder the yield of the HIM fabrication process. Due to toughness (strength) of these features, they can interfere with HIM milling and result in not well-defined patterns. An example of HIM milling in presence of wrinkles in a graphene flake is shown in Figure 4.20.

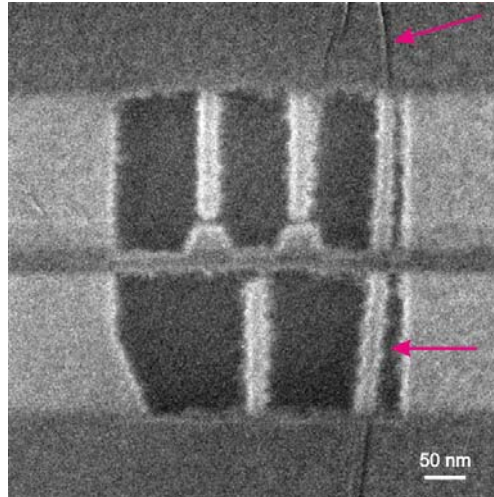


Figure 4.20 – HIM SE image. A not well-defined HIM milled pattern on a monolayer graphene flake due to presence of wrinkles (pointed by the pink arrows) in the flake.

4.6 Electrical characterisations and analysis

The preliminary I-V characterisation of the final fabricated devices by our novel hybrid fabrication method was conducted at room temperature. We employed the similar measurement set-up to that of explained in section 6.1 (also see Figure 6.1).

Results from room temperature measurements of the forward (I_{SD}) and the reverse (I_{DS}) source-drain current through one of our fabricated devices shown in Figure 4.21(a), as a function of the applied source-drain voltage (V_{SD}) are presented in Figure 4.21(c). For a bias voltage of 5 mV, the current through the device with a channel length of ~ 172 nm was 130 pA with almost no measurable current leakage from the channel and the DQD. To confirm complete milling of the graphene exposed to the He beam and therefore successful isolation of all side gates, the device was measured for possible gate leakage between the side-gates. This was achieved by measuring the current through each side-gate by sweeping the bias voltage whilst every individual side-gate was grounded. The currents measured between all side gates lie within the noise levels of the measurement equipment (in fA range) and so can be considered to be negligible, indicating successful isolation of all side gates, as shown in Figure 4.21(d). This proved that accurate alignment between the e-beam pattern and the HIM pattern was

achieved and the developed milling conditions were adequate to completely mill the flake with the desired pattern.

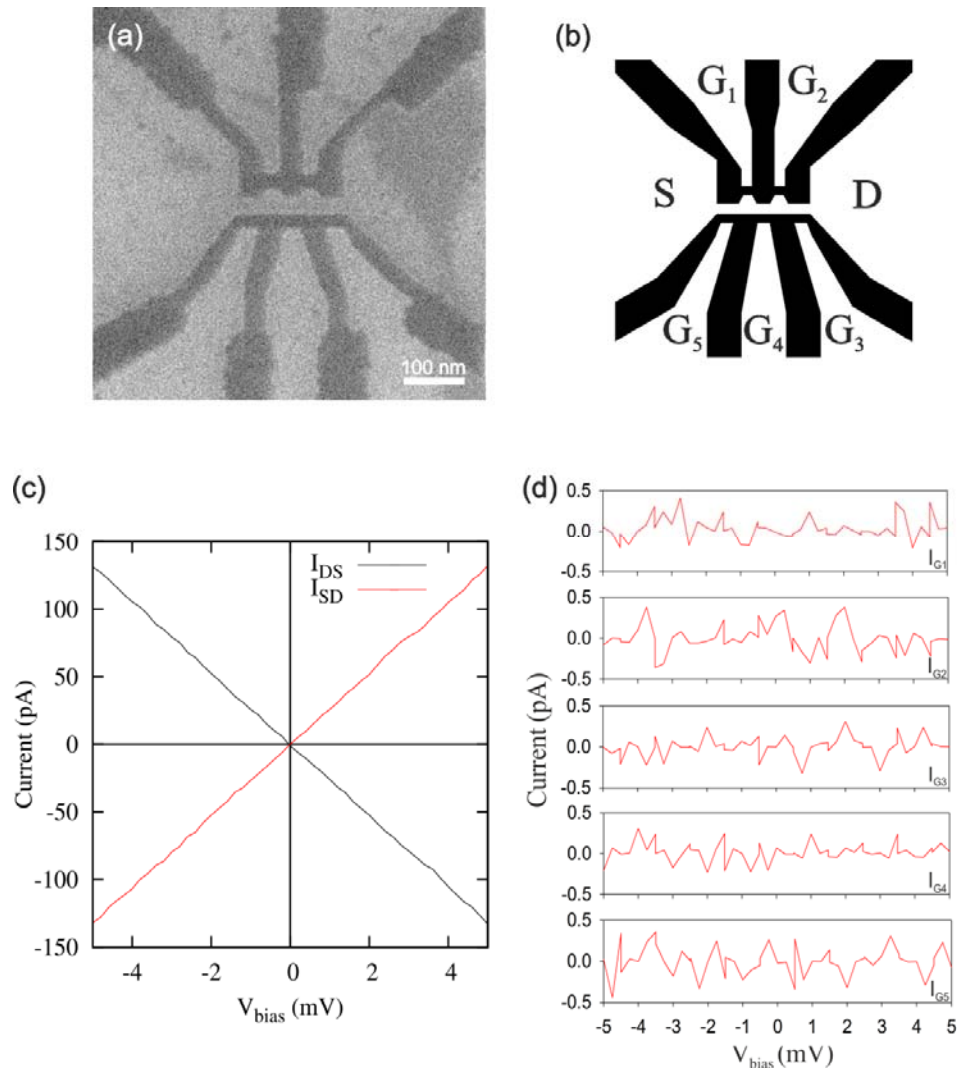


Figure 4.21 – (a) HIM SE image of device milled into a metal-contacted and annealed monolayer graphene flake, with a He-dose of $0.63 \text{ nC}/\mu\text{m}^2$. I-V characterization. (b) The bitmap design of the DQD device with the source, drain and gate contacts labelled. (c) Forward and reverse bias currents as a function of the applied DC bias voltage. (d) Gate-leakage measurements.

The confirmation of complete milling of exposed graphene on SiO₂/Si substrates and successful isolation of contacts is an encouraging step in the development of HIM milling of graphene for nanoelectronic device fabrication. In the study by Lemme *et al.* [17], hydrocarbon contamination on the SiO₂ surface in the HIM exposed regions led to residual conductivity but here it is shown that by employing an annealing step before the final HIM patterning, such contamination can be avoided and regions of a pattern can be fully isolated from other regions. The high resolution and accurate design replication capabilities of the HIM milling technique could pave a way towards more detailed studies of the behaviour of GQD and other graphene QIT devices, both at room and cryogenic temperatures. For instance, in the Figure 4.21(a), the accurate positioning of the side-gates relative to the channels and the DQD (~22 nm) should ensure precise control of the single electron tunnelling through the device.

Interestingly, the collected I-V measurements revealed that the fabricated devices exhibited unusual high resistance. Initially, we attributed the unusual high resistance of the final fabricated device to several factors. For instance, backscattered ions and sputtered atoms from the substrate during the HIM milling can interact with graphene on their way to the surface and induce defects in the graphene flake. In fact, it has been demonstrated theoretically [181] and experimentally [182] that the SiO₂ substrate has a great influence on the final defect creation and could enhance the irradiation damage in supported graphene exposed to energetic particles [183]. Moreover, annealing graphene brings the flake in close contact with the rugged surface of the SiO₂ layer which can lead to degradation of mobility of graphene flakes [173]. Edge scattering mechanisms, edge disorder [184], [185] and edge roughness [55], [56], can also lead to significant degradation in mobility of downscaled graphene nano devices. However, further studies are required to determine the extent of contribution of each of the mentioned factors to the electrical properties of our final fabricated device.

We prepared more samples to investigate further the electrical characteristics of the He-ion beam fabricated devices. However, strangely, upon HIM milling, for the first time, we observed random strange black-dot-shape features on the graphene samples, which are shown in Figure 4.22(a,b). Due to constant milling of graphene during HIM imaging, it was very difficult to obtain high resolution images (with high beam dwell time) and to find out whether the features were physical holes in the graphene lattice or they were deposited particles on the

graphene surface. Interestingly though, we were able to mill the samples successfully with high resolution patterns. Figure 4.22(c) shows a 10 nm-wide GNR milled on an annealed graphene sample in presence of the dot-shape features. The successful milling outcome hinted two important clues. Firstly, the dot-shape features did not interfere or impact the milling outcome and so were not deposited features. Secondly, the milled regions (black lines in Figure 4.22(c)) and the dot-shape features (black dots in Figure 4.22(c)) seemed to exhibit same image contrast. Based on these observations, we speculated that the features might be “etch-pits” which can be created by oxidising graphene samples during an annealing process [175]. Using AFM imaging, Liu *et al.* demonstrated that annealing graphene samples at ~ 300 °C in an oxygen gas flow creates random etch-pits (i.e. O₂ etch) and leads to strong hole doping in graphene samples [175].

We confirmed this by annealing a pristine graphene under the conditions that initially resulted in the Raman spectrum in Figure 4.18(b). The Raman spectrum collected after annealing looked shockingly comparable to that of demonstrated by Liu *et al.* for oxidised graphene samples (see Figure 4.22(d)) [175].

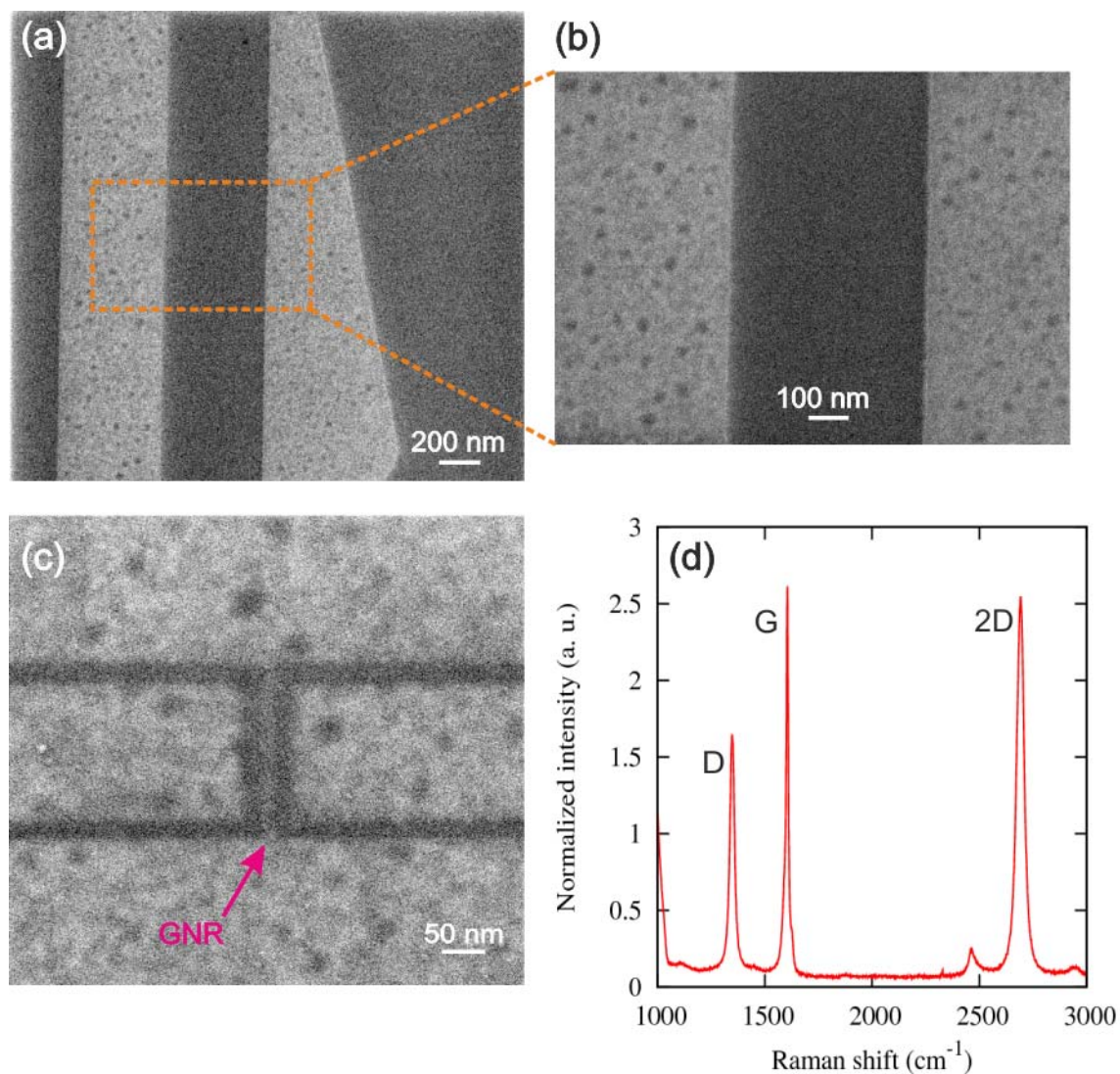


Figure 4.22 – HIM SE images. (a,b) Creation of the black dot-shape features in the graphene samples after annealing. (c) Successful milling of a 10 nm-wide GNR in the presence of the dot-shape features. (d) The Raman spectrum collected from a pristine graphene flake after annealing under the conditions that initially resulted in the Raman spectrum in Figure 4.18(b).

This resulted in extensive amount work to identify the source of oxidation of the graphene samples. Initially, we tried to alter the conditions of the annealing in the hope of solving the issue. Unfortunately, no improvement was observed which suggested a possible fault with the furnace. Therefore, in another approach, we employed a Rapid-Thermal-Annealing (RTA)

process suggested by Jang *et al.* [174] for removing surface contaminants on processed graphene samples. The RTA process suggested by Jang *et al.* [174] is illustrated in Table 4.2.

TABLE 4.2

A process flow sheet. The rapid thermal annealing process suggested by Jang *et al.* [174] for removing surface contaminants on processed graphene samples.

Process description	Temperature	Gas flow	Duration
Temperature ramp-up	25-250 °C at a rate of 5.5 °C/second	N ₂	40 seconds
Annealing	250 °C	N ₂	10 minutes
Temperature cool-down	250-25 °C at a rate of ~10 °C/minute	N ₂	~ 23 minutes

Interestingly, once again, our pristine graphene samples suffered from oxidation. At this point, we considered possibility of contamination in the gas lines. After several discussions, the possibility of water vapour contamination in the cleanroom's gas lines, due to poor quality of the installed gas purifier units, was confirmed by the cleanroom's technical staff.

To confirm that the water vapour contamination in the gas lines was in fact the reason behind the oxidation of our graphene samples, we decided to anneal our samples in a Plasma-enhanced chemical vapour deposition tool (PECVD) which is facilitated with pure hydrogen gas that is provided by a separate gas cylinder and not via the cleanroom's general gas lines. PECVD tools are designed for high quality material deposition and not for annealing applications. However, these tools are equipped with a hotplate which facilitates the energy (heat) required to deposit a material layer onto a desired substrate.

Initially, the samples were annealed at 300 °C in H₂ gas flow (1500 sccm) for 2 hours in a PECVD tool. Remarkably, post annealing HIM imaging showed no sign of etch-pits (oxidation). However, our milling attempts on the annealed sample were not successful.

Therefore, in hope of developing an annealing process with the PECVD tool and achieve desired milling result, extensive amount time and work were spent to optimise the annealing process. Interestingly, a semi-successful milling outcome, with a He-dose of $0.75 \text{ nC}/\mu\text{m}^2$, was achieved after annealing a processed graphene sample at 370°C in H_2 gas flow (1500 sccm) for 2.5 hours. The HIM milling outcome is shown in Figure 4.23.

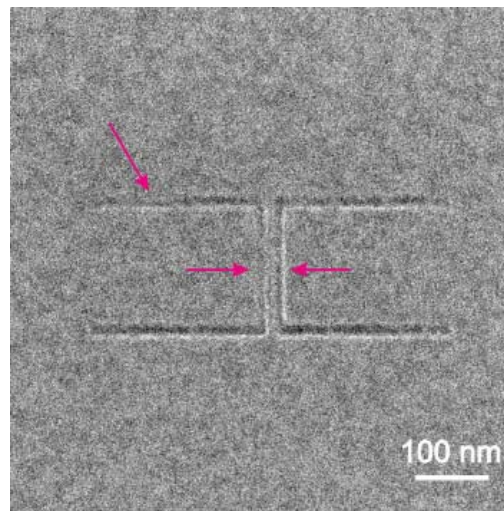


Figure 4.23 – HIM SE image of a semi-successful milling outcome, with a He-dose of $0.75 \text{ nC}/\mu\text{m}^2$, after annealing a process graphene sample at 370°C in H_2 gas flow (1500 sccm) for 2.5 hours in a PECVD tool. The arrows point to some of the regions that the graphene flake was not milled properly.

The temperature and the annealing duration were increased to obtain desired HIM milling result (e.g. similar to that of shown in Figure 4.21(a)) with the optimum He-dose of $0.63 \text{ nC}/\mu\text{m}^2$. However, the milling outcome did not improve. In fact, for temperatures above 400°C , the milling outcome started getting worse. We attributed this to possible re-deposition of contamination in the chamber (of the PECVD tool) onto the samples which becomes more probable with increasing the temperature.

Interestingly, very recently, using a fabrication process very similar to ours (presented in see Figure 4.3), Abbas *et al.* (in collaboration with Hewlett-Packard laboratories) demonstrated

successful fabrication of an array of 5 nm-wide GNRs with HIM milling for chemical sensing applications [186]. The confirmation of successful fabrication of the devices was justified by measuring I-V characteristics of the fabricated devices at room temperature and low temperatures. Interestingly, similar to our analysis, the authors attributed the degradation of the current density in the fabricated devices to edge scattering, increase in defect density in graphene due to backspattered atoms from the substrate during milling, reduced effective transconductance due to creation of charge traps in the SiO₂, and increased electron and hole masses [186]. Furthermore, for an array of 5 nm-wide GNRs (with a length of 200 nm), a $53 \pm 8\%$ change in conductance for 0.4 ppm (parts per million) concentration of NO₂ gas was reported, exhibiting a much higher sensitivity for chemical sensing applications compare to previously reported GNR devices [186].

Figure 4.24 shows an array of high resolution (sub-10 nm) DQD patterns milled on an annealed graphene flake. The minimum defined feature size, which is the gap between the graphene side-gates and channel, is decreased from 9 nm to 3 nm from the first device in the array to the last (left to right), with the other features, i.e. diameter of the DQD and the channel width, scaled down as well. The subsequent HIM image of the fabricated array provides evidence that the small features in the pattern design are faithfully reproduced in the graphene flake, however conclusive proof of this is hard to obtain due to the challenges of imaging such small scale and delicate structures. Slow scanning with the helium beam in an attempt to form a low noise image will cause further milling of the graphene, degrading the fabricated structures. Therefore, low currents and short dwell times must be used when imaging these patterns at high magnifications (e.g. 0.2 pA and 10 μ s were used for the image in Figure 4.24), which inevitably leads to noisy images and difficulties in accurately measuring fine features. Nevertheless, the resolution/size of the DQD patterns shown in Figure 4.24 clearly demonstrates the potential of this technique for fabrication of room temperature-operable quantum devices.

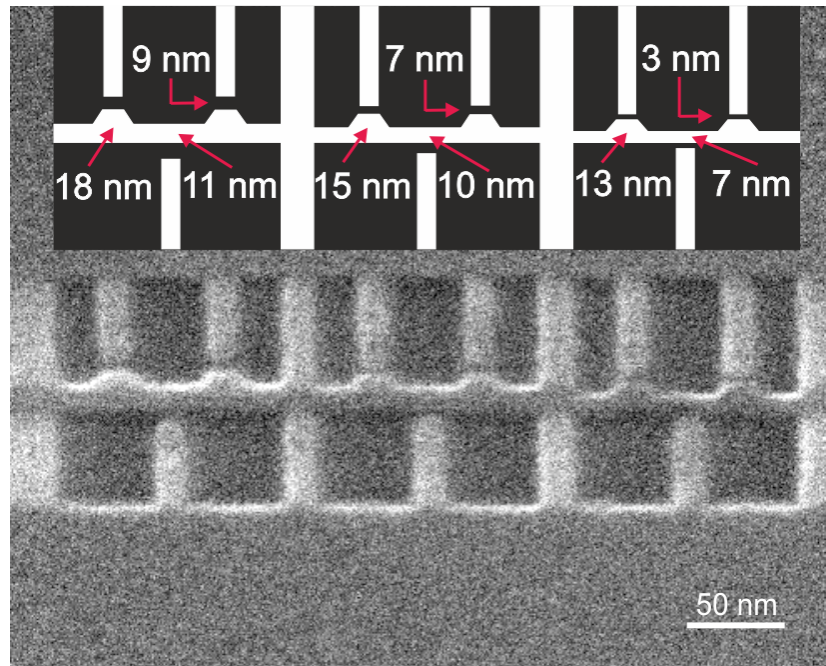


Figure 4.24 – Sub-10 nanometre lithography by HIM milling on a monolayer graphene flake. The bitmap image of the designed patterns (top row) and the HIM image of the consequent milling of each design (bottom row), with a minimum feature size of ~ 3 nm which is the gap between the in-plane graphene side-gates and channel.

4.7 Conclusions

In this chapter, we discussed that there are several parameters that can hinder the resolution of the graphene devices fabricated by the EBL/RIE process. We then introduced helium ion microscopy as an ultra-high resolution imaging tool. We discussed that the atomically sharp source, combined with the smaller de Broglie wavelength (and so larger momentum) of helium ions compared to electrons, enables a sub-nm probe size at the sample surface. Owing to this, HIM has attracted a lot of interest as an alternative nanofabrication tool. We then introduced our novel hybrid fabrication process for extremely downscaled graphene quantum dots by combining conventional e-beam lithography and HIM milling. The helium ion milling is used to pattern graphene flakes with intricate QD devices, with sub-10 nm resolution and high fidelity. We established this novel fabrication approach for the first time. We reported that the unintentional production of hydrocarbon contamination on the surface of graphene flakes after

e-beam lithography can hinder HIM milling. However, by annealing the samples in a H_2/N_2 gas flow, it is possible to reduce this contamination sufficiently to achieve the desired milling results. The electrical characterization of the final device demonstrated the successful fabrication of the first electrically characterized He-ion beam patterned graphene device. This work demonstrates that HIM milling has the potential to enable fabrication of high resolution confinements (<10 nm) and could ultimately pave the way towards observation of Coulomb blockade at room temperature in GQDs devices. Unfortunately though, due to water vapour contamination in our cleanroom's gas lines, fabrication of more devices to investigate their electrical characteristics in greater detail was not achieved. However, the work reported by Abbas *et al.* [186] demonstrated that our fabrication process was well thought out and well-established.

Chapter 5

Fabrication of GQDs devices by electron-beam lithography and RIE etch

One way of fabricating graphene nano devices is by means of conventional electron-beam lithography. This is the most established method of fabricating graphene nano devices and has been widely used by different research groups. This chapter concentrates on the fabrication process that we developed for the first time at Southampton Nanofabrication centre to fabricate graphene nano devices, such as intricate GQDs devices, with high yield of ~80%. All the steps involved in the fabrication process of such devices are explained in detail in order to pave the way for future graphene projects in Southampton Nano Group.

5.1 Introduction

The previous chapter discussed an overview of the operation of quantum dot devices as well as recent studies on the behaviour of GQDs devices. As discussed, despite the short history of graphene, its unique electron-transport characteristics have ensured a rapid growth of interest in the field of electronics. In addition, spin-or-bit coupling and hyperfine interaction with carbon nuclei are both small in graphene, and a very long spin relaxation length has been demonstrated [12], [13], which make graphene a promising candidate material for quantum

information technology and spin qubit embodiment [11]. Therefore, in conjunction with the downscaling trend, it is important to develop a reliable fabrication method to study the behaviour of graphene device at nanometre scale.

Since mid-1960s, by introducing electron microscopy, it has been possible to fabricate and scan structures and features down to tens of nanometres. E-beam lithography (EBL) has been a reliable method for fabrication of nano devices on variety of substrates and is gaining widespread utilisation as the semiconductor industry progresses toward both advanced optical and non-optical lithographic technologies for high resolution patterning. EBL is often used with organic resists which sub-20 nm lithography resolution can be achieved reliably. Currently, using inorganic resists, sub-10 nm lithography resolution is also possible [187], [188]. Electron beam lithography followed by reactive-ion-etch (RIE) is the most common method of fabricating graphene nano devices, e.g. GDQD devices [127], [131], [133], [140], [141]. The method consists of two main fabrication steps, (i) e-beam lithography followed by reactive-ion-etch to pattern graphene flakes (i.e. to define quantum dots) and, (ii) e-beam lithography followed by metal deposition and consequent lift-off to fabricate the metal contacts for the devices. Although the fabrication process may sound simple but, as it was also reported by other research groups, the fabrication of graphene nano devices is technologically very challenging. In addition, depending on the resolution and complexity of a graphene device pattern, the fabrication process yield can vary.

In this chapter, first, we will discuss our fabrication process, which was developed for the first time at the state-of-the-art Southampton Nanofabrication Centre, for graphene nano devices (e.g. GDQD). The chapter is organised in a way to systematically provide a comprehensive study of the steps involved in the fabrication process, challenges/diagnosis and process optimisation. Finally, this chapter is concluded by discussing the electrical characterisation of the final fabricated devices at room temperature and cryogenic temperatures (i.e. observation of Coulomb diamonds).

Our processing steps for the fabrication of GQD devices by e-beam lithography and RIE etch are illustrated in Figure 5.1.

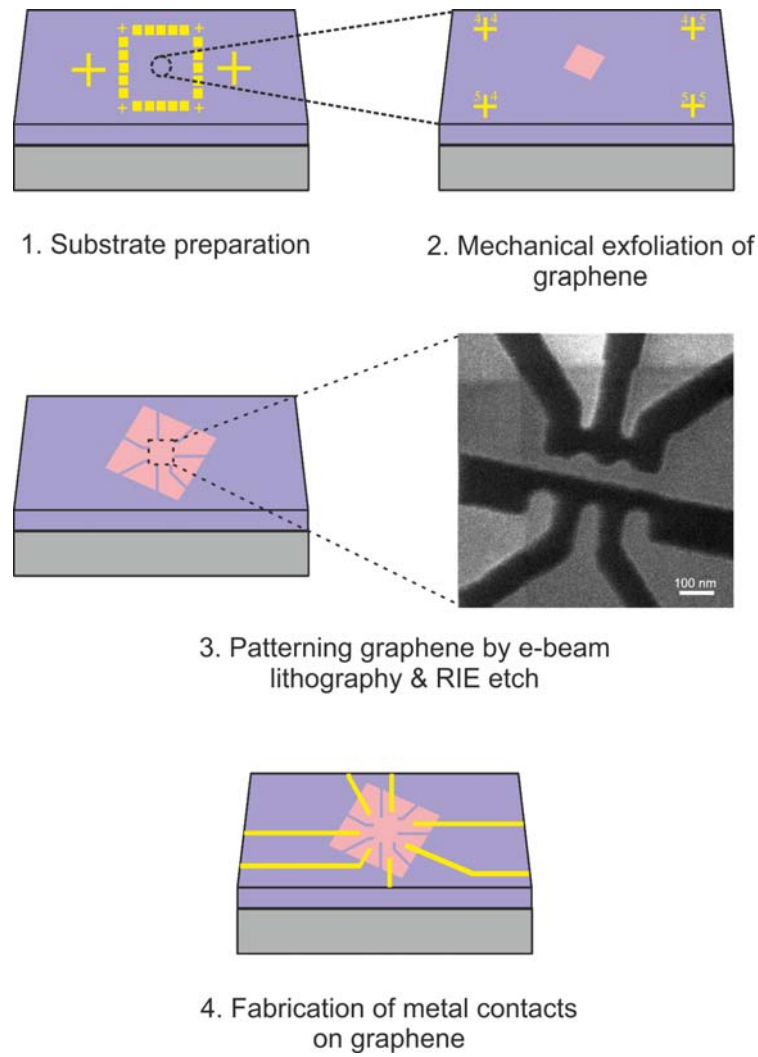


Figure 5.1 – Schematic illustration of the steps involved in the fabrication of GQD devices by e-beam lithography and RIE etch.

5.2 Substrate preparation

The substrates were prepared from highly doped silicon (with low resistivity of $0.001 \, \Omega \cdot \text{cm}$ – $0.01 \, \Omega \cdot \text{cm}$) wafers with 295 nm thermally grown oxide, courtesy of IDB technologies Ltd. To create a decent contact to the highly doped silicon layer for back gate measurements, the oxide layer on one of the sides of the wafer was removed prior to further processing. To this end, one side of the wafer was spin-coated with a $2 \, \mu\text{m}$ -thick layer of S1813 photo-resist (i.e. spun at 1000 rpm), followed by a hard bake at $120 \, ^\circ\text{C}$ for 15 minutes. This hard mask protected the resist-coated side from any damage as we etched the oxide layer on the unprotected side of the

wafer. With the uncoated side of the wafer facing up, the wafers were placed in a reactive-ion-etch (RIE) chamber to etch the oxide layer. The SiO₂ layer was etched in Ar/CHF₃ (38/12 sccm) ambient using a RF power of 200 W, a 14 minutes etch duration and at a vacuum pressure of 30 mTorr. The photo-resist was then removed by leaving the wafer in Fuming-Nitric Acid (FNA) for 5 minutes followed by a rinse in deionised (DI) water. Moreover, to ensure no residues were remained from the wet process on the wafer, an ashing oxygen plasma was employed to clean the wafers thoroughly. This step was performed in a TePla 300E ashing plasma using 600 mL/min O₂ gas flow, RF power of 800 W, for 10 minutes and at a vacuum pressure of 0.15 Torr.

The wafer was then patterned into 3×3 mm small chips with reference alignment marks and bond pads by two e-beam lithography steps. For both lithography steps a bilayer resist layer of *Methyl Methacrylate* (MMA 8.5 EL 9)/*Poly Methyl Methacrylate* (PMMA 495K) was spin-coated. Both MMA resist (spin-coated at 1500 rpm) and PMMA resist (spin-coated at 5000 rpm) were baked for 70 seconds at 150 °C and 180 °C, respectively. Ellipsometry measured a thickness of 425 nm and 125 nm for MMA resist layer and PMMA resist layer, respectively. The advantage of using a bilayer resist is the formation of an undercut after the e-beam exposure in the profile of the resist layer. The formation of the undercut is due to the higher sensitivity of the bottom resist layer, MMA resist in our case, which greatly improves the lift-off process outcomes (see Figure 5.2(a)). Employing a bilayer resist was essential to ensure the fabricated alignment marks (see Figure 5.2(b)) have well-defined edges, and so they are detectable by the e-beam machine for future e-beam lithography steps. Furthermore, the bilayer resist particularly eased the lift-off process for the bond pads features (see blue colour patterns in Figure 5.2(a)) where we deposited a 320 nm-thick layer of Ti/Au (20 nm/300 nm). The e-beam exposure was performed using a state-of-the-art JEOL 9300FS e-beam lithography system, a base e-beam dose of 400 $\mu\text{C}/\text{cm}^2$, with the e-beam operating at an acceleration voltage of 100 keV.

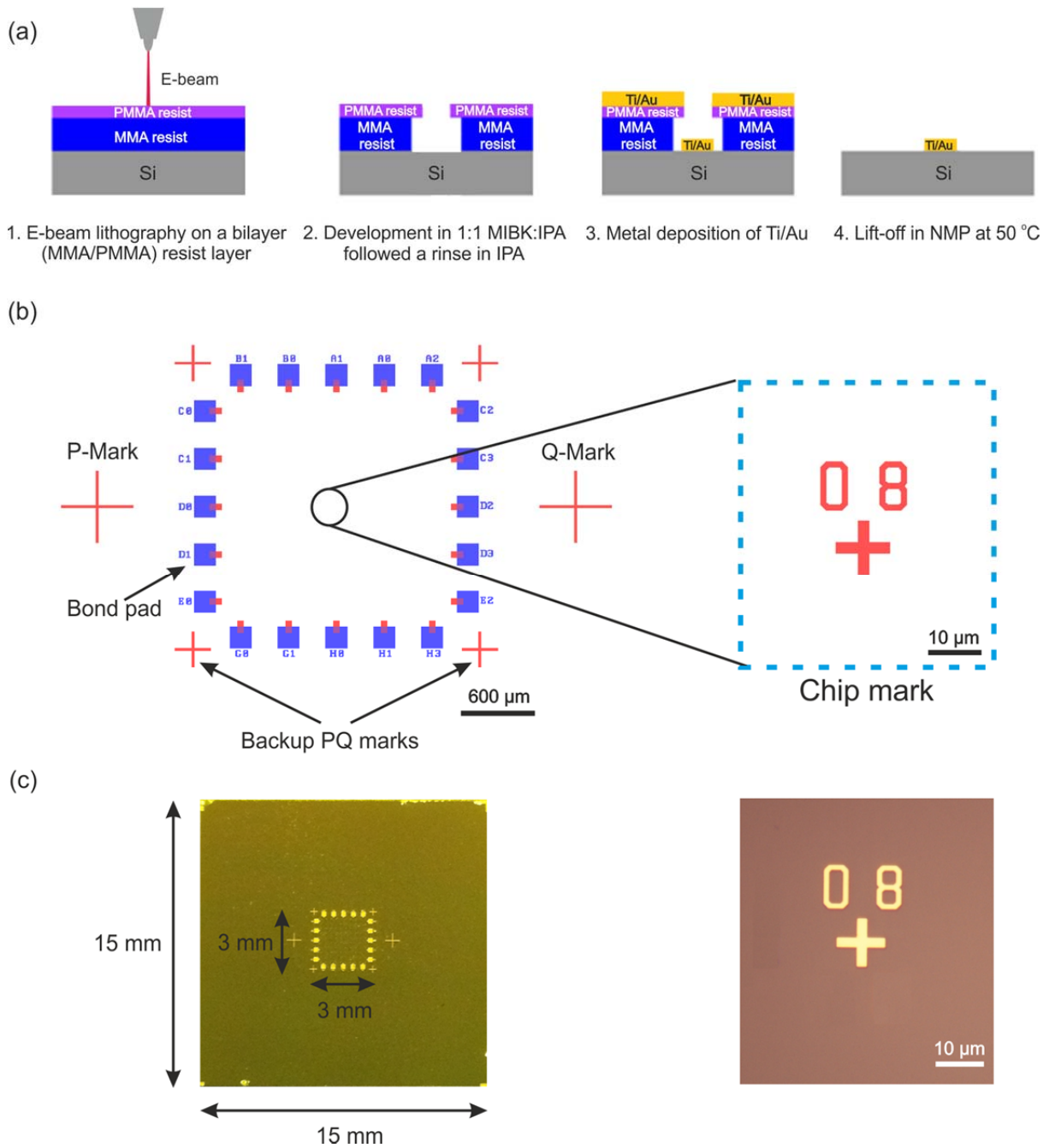


Figure 5.2 – (a) Schematic illustration of the steps involved in the fabrication of the device chips. (b) L-edit design and layout of our device chips. The colour difference (i.e. red and blue) in the L-edit layout distinguishes the exposed patterns in each lithography step. That is, the red-colour layer was exposed and metallised prior to the blue-colour layer. (c) Optical microscopy images of the successful fabrication of the device chips.

The base e-beam dose was obtained after several e-beam exposure dose tests. In addition, to ensure an optimum dose is applied to each pixel (in nanometre) of the designed patterns, proximity effect correction (PEC) was employed using GenISys software (see section 5.4 for a more extensive discussion). This step was particularly important for the fabrication of the chip marks (i.e. PQ and chip marks, see Figure 5.2(b)) to ensure accurate and easy mark detection for future e-beam lithography steps. That is, alignment marks with rough and not well-defined edges often result in mark detection failure during e-beam exposures.

The e-beam exposed wafer was developed in 1:1 mixture of *Methyl isobutyl ketone* (MIBK) and *2-Propanol* (IPA) for 90 seconds followed by a rinse in IPA for 30 seconds. The wafers were then metalized after each lithography step by e-beam evaporation of Ti/Au (5 nm/45 nm for the first step and 15 nm/300 nm for the second step) at a base pressure of 3×10^{-7} mbar, a deposition rate of 0.5 Å/second, with the e-beam operating at 10 keV, in a Leybold LAB700 evaporator. The subsequent lift-off was performed in *N-Methyl-2-Pyrrolidone* (NMP) at 50 °C followed by a rinse in DI water and IPA. The schematic of the fabrication process, the L-edit design layout and the final fabricated chips are shown in Figure 5.2.

Finally the wafer was diced into the fabricated chips (see Figure 5.2(c)). To protect the chips from scratch and/or particles (e.g. silicon dust) during the dicing step, the wafer was spin-coated with the similar S1813 mask layer (as discussed above) again. The samples were dusted off using DI water and N₂ blow gun prior to removing the resist (mask) layer. The resist layer was then removed in NMP at 50 °C followed by a rinse in DI water and IPA.

5.3 Mechanical exfoliation of graphene

Prior to transferring graphene onto the chips by means of mechanical exfoliation, the fabricated chips needed to be cleaned thoroughly from possible organic residues and/or contaminants that might have resided on the surface of the chips during the fabrication process. This step is very crucial. That is, organic residues or contaminants on the SiO₂ layer can weaken the bonding (i.e. adhesion) between the substrate and exfoliated graphene flakes, and so resulting in a low yield of mechanical exfoliation process.

To remove the contaminants, the samples were immersed in acetone followed by IPA for 10 minutes each. The samples were then baked at 200 °C on a hotplate for 5 minutes to remove any alcohol residue(s). Finally, the samples were exposed to UV light by an ozone (O_3) cleaner for 10 minutes. To our experience, this cleaning process guarantees very clean substrates and greatly improves the mechanical exfoliation yield. The cleaned samples were then used for mechanical exfoliation.

By a technique known as mechanical exfoliation, graphite is stripped down to fewer atomic layers of graphite using an adhesive tape. The common choices for the adhesive tapes are scotch tape, blue tape and water-soluble tape. Scotch tape provides very good flakes due to its high adhesion and was also used to isolate graphene for the first time [46]. However, due to its high stickiness, it leaves nasty glue residues on the substrate and/or on the exfoliated flakes. These glue residues are very difficult to remove and require an intensive cleaning process, e.g. thermal annealing, to be cleaned. More importantly, the glue residues have been illustrated to limit the carrier mobility in the produced graphene flake [9], [61], [189]. Furthermore, they can weaken the adhesion of the substrate surface and prevent resist layers to be spin-coated uniformly onto the samples for future lithography steps. Glue residues on graphene can also degrade the quality of electrical contact between the flake and deposited metallic terminals onto the device. Therefore, we chose blue tape (PO non-UV dicing blue tape with 0.095 mm thickness from Pantech tape CO., LTD.) that offers good adhesion strength and, if used properly, does not leave any residue(s) on the sample.

Unfortunately there is no direct reference which explains the mechanical exfoliation method in detail or to suggest how to improve the yield of the process. However, after several iterations of different conditions, here is the way that we came to realise to offer a decent yield. To start the process, cut 6 long blue tape strips. Cut one of the strips into 3 small rectangles. Take one of the strips and place a piece of graphite onto one of its ends. To exfoliate the graphite one needs to make a tape-graphite-tape sandwich. To do so, gently grab and fold the graphite end of the tape and try to transfer the graphite 1-2 cm away from its current location on the tape by making a tape-graphite-tape sandwich. Use your thumb or a pair of tweezers and rub the back of the tape to ensure the two sides of the tape are pressed firmly together. Slowly peel the tape off and now the graphite piece should have transferred to a location 1-2 cm away

from its original location on the tape. After each repeat the outer layers of graphite stick to the tape and so peeled off, resulting in a shinier and thinner graphite piece on the tape (see Figure 5.3(a)). Repeat this step for 10-15 times until you produce a thin and very shiny piece of graphite on the tape. Now transfer the graphite onto one of the small rectangle-shape tape pieces. Pick up another small rectangle-shape tape piece and create a tape-graphite-tape sandwich. However, this time, create the tape-graphite-tape sandwich several times in order to obtain similar graphite density onto both of the tapes. Continue this step until you feel the stickiness of the tapes is gone. Then using a fresh piece of tape and one of the now graphite-covered tape pieces repeat the previous step, until you produce a consistent light grey layer of graphite on one of the tapes, as shown in Figure 5.3(b). Locate an area of the tape with the highest graphite density and place it on a chip. It is very important to use an area of the tape with a high graphite density to avoid leaving glue residues onto the sample after peeling off the tape. Furthermore, thin graphene flakes are more likely to be produced when there is a decent graphite density on the tape. An example of the blue residues is shown in Figure 5.3(c). Using a pair of tweezers gently rub the back of the tape for 3 minutes to transfer the graphene/graphite pieces onto the chip. Then peel off the tape very slowly and immerse the chip in a small beaker filled with IPA. Place the beaker in an ultrasonic bath and sonicate the sample for 1 minute. The sonication step helps significantly to remove a very decent number of bulky (big) graphite pieces off of the sample. The effect of the sonication step is shown in Figure 5.3(e). Finally, blow-dry the sample by a N_2 gun.

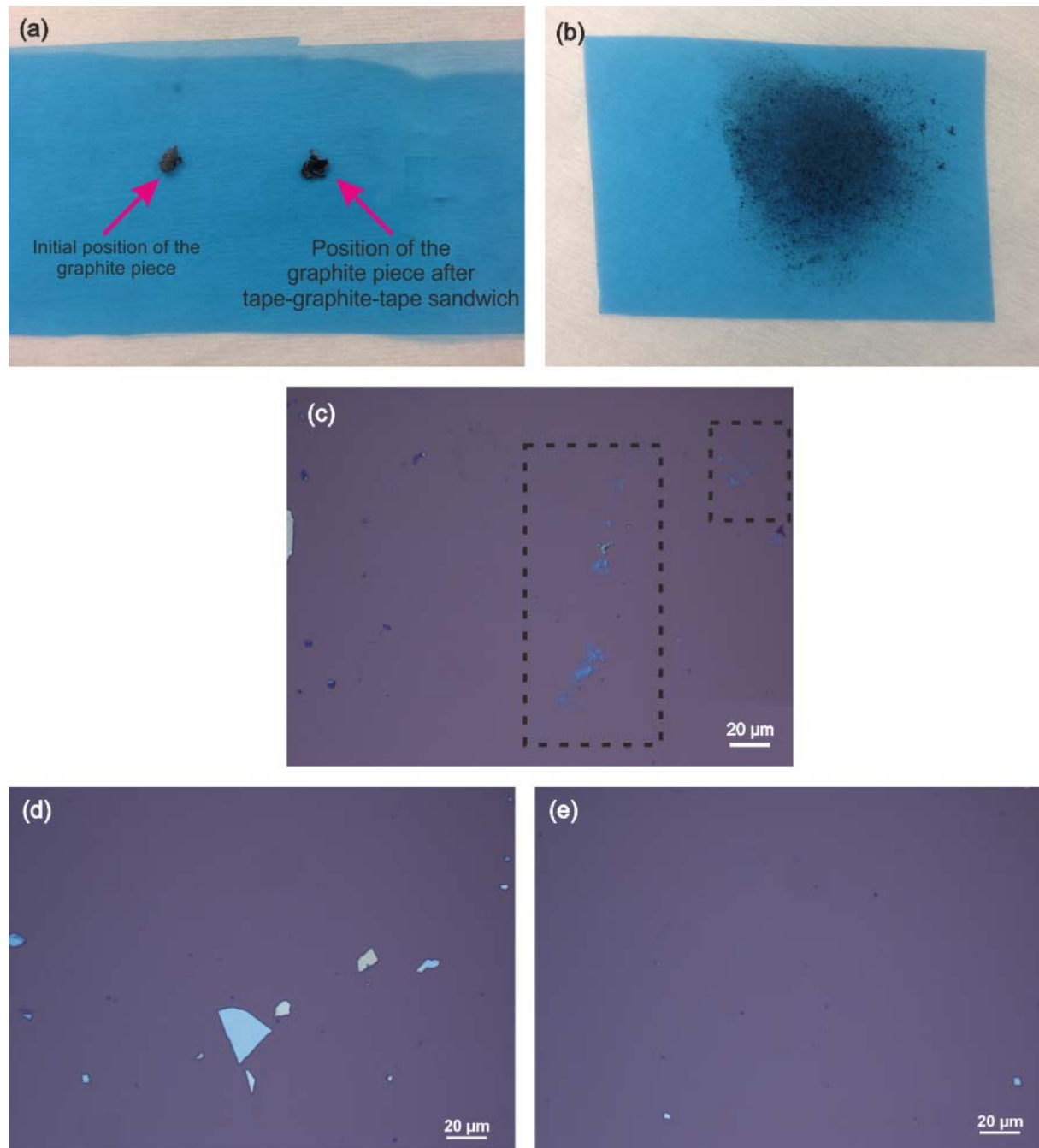


Figure 5.3 – (a) Optical image of a blue tape strip after performing a tape-graphite-tape sandwich. (b) Optical image of a piece of blue tape with sufficient graphite density. (c) Optical microscopy image of produced blue residues (inside the black dashed regions) on a sample due to lack of adequate graphite density on the used blue tape. (d) and (e) are optical microscopy images of a sample before and after sonication, respectively. The images clearly show effectiveness of the sonication step for removing excessive pieces of graphite produced after mechanical exfoliation process on the samples.

Thin flakes were initially located by optical microscopy [46], [75], [190]. In addition, Raman spectroscopy was employed to identify the number of graphene layers more precisely [76]. The Raman spectra were collected using a Renishaw InVia Raman spectrometer with a 532 nm wavelength laser, a laser excitation energy of $E_{laser} = 2.33$ eV and a $\times 100$ objective lens (numerical aperture of 0.8) which resulted in a laser spot size radius of ~ 400 nm. The graphene flakes were identified at a laser power of 0.2 mW with a 100 seconds exposure time. We employed a low laser power to avoid laser-induced damage and/or laser-induced heating on the samples during the measurements [76]. However, we optimised the combination of the laser power and the exposure time to ensure the collected spectra were smooth and informative. Figure 5.4 shows examples of our produced monolayer graphene flakes by mechanical exfoliation as well as a Raman spectrum collected from one of the monolayer graphene samples. The FWHM of the 2D peak shown in Figure 5.4(c), collected under the Raman spectroscopy conditions mentioned above, is 29.9 cm^{-1} which is similar to the value reported for monolayer graphene flakes (i.e. $\sim 30 \text{ cm}^{-1}$ [88]). This indicates that we successfully managed to produce monolayer graphene flakes using our mechanical exfoliation process.

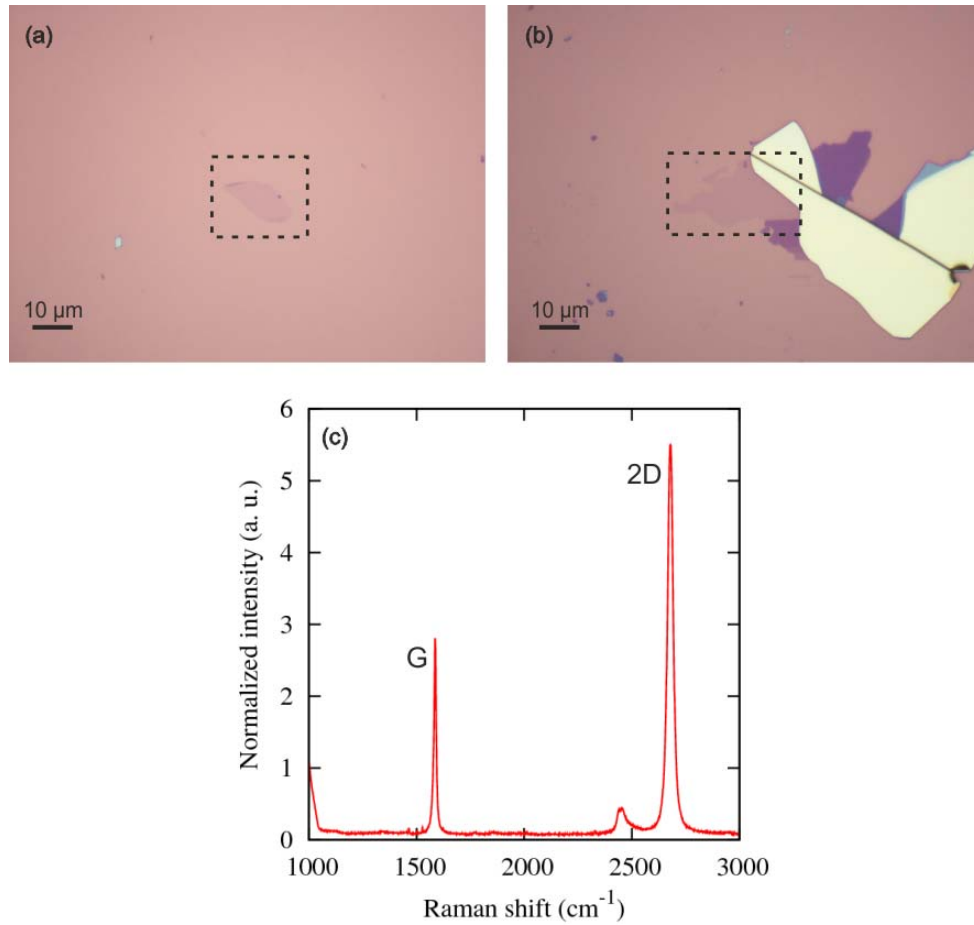


Figure 5.4 – (a) and (b) optical microscopy images of our produced monolayer graphene flakes (inside the black dashed regions) by mechanical exfoliation. (c) A Raman spectrum collected from one of our monolayer graphene flakes.

5.4 Patterning of graphene by e-beam lithography and RIE etch

In this section we explain patterning of the produced graphene flakes with desired designs, e.g. DQD, by means of e-beam lithography and RIE etch. For high resolution lithography PMMA resist (495K A4) was diluted in anisole to prepare a 1:2 (PMMA:anisole) mixture. Using ellipsometry, the resist spin-coating conditions were tuned and a 40 nm-thick layer of the PMMA resist was obtained at 1600 rpm. PMMA is an ultra-high resolution resist with relatively poor sensitivity and poor dry etch resistance. However, as we will discuss later, a very short RIE step is required to transfer e-beam exposed patterns onto graphene flakes.

Ellipsometry measurement indicated that only ~ 6 nm of the total thickness of the resist layer was etched away during our optimised RIE etch step (which we will discuss below). This suggested that the resist layer was thick enough to protect our graphene flakes during the RIE etch process. Although sub-10 nm patterning of graphene with e-beam lithography of inorganic resists, i.e. *hydrogen silsesquioxane* (HSQ) resist, is reported [111], [112] but, as we will discuss later (see section 5.5), the beam-induced damage at high e-beam doses can result in severe damage in graphene samples [44]. Therefore, we decided to use a 40 nm-thick layer of PMMA resist which offers decent lithography resolution at much lower e-beam doses than HSQ resist.

Resist pre-bake conditions, e-beam dose and resist development conditions were identified as the main parameters to affect the resolution of the lithography process. This led to extensive e-beam lithography test exposures to optimise conditions of each of those parameters. Courtesy of the datasheet provided by Microchem Corp. (the supplier of the PMMA resist), a pre-bake time of 60-90 seconds at 180 °C is suggested for PMMA resist. Based on our previous experience with the resist, for our initial dose tests we used a pre-bake time of 70 seconds. However, as we will discuss later in this section, for the final tuning of our lithography process we also studied the effect of the resist pre-bake time in the resolution of our patterns.

High resolution lithography is a complicated subject. In general, fabricated features by lithography can suffer from a finite point-spread function (PSF). PSF profile of a beam (i.e. approximately a Gaussian distribution for an electron beam) is the spatial distribution of energy deposition in a resist as a function of radial distance from primary beam incidence. PSF results in the exposure of unwanted features between patterns with small gaps where neighbouring features can obtain additional dose from the overlapping exposure dose tails, i.e. proximity effect (PE). Therefore, beam interaction radius at the surface of substrate has a great influence in the final resolution of beam-exposed features. The interaction between an electron beam and the substrate results in generation of high energy secondary electrons (SEs). These SEs can exit the substrate (i.e. backscattering effect) away from the primary beam and result in additional exposure of resist molecules. It is worth mentioning that higher beam operation voltages increase the SEs scattering distance. An extensive discussion of beam interaction radius is provided in the next chapter at which, we propose helium ion beam milling for ultra-high resolution patterning of graphene samples.

A common approach to avoid proximity effect is a dose (e.g. shot time, spot size) or pattern correction during exposure based on the energy point spread function at given exposure conditions (i.e. substrate, beam acceleration voltage). To this end, we employed GenISys software which automatically calculates the proximity effect correction (PEC) for a given pattern. The software breaks a pattern into many small sub-patterns and then assigns each sub-pattern a dose increase or decrease, as required to avoid PE. That is, increase (decrease) in the shot time for small isolated (large dense) patterns.

The PEC calculations indicated that a 60% dose increase is required for the successful exposure of our patterns, i.e. total e-beam dose = e-beam base dose + 60%. An example of one of our patterns is shown in Figure 5.5(a). Therefore, from now on, we explain how we obtained the optimum e-beam base dose.

The e-beam base dose was varied from 100-250 $\mu\text{C}/\text{cm}^2$ in 10 $\mu\text{C}/\text{cm}^2$ steps to find the optimum dose for our patterns. It is worth mentioning that the dose range was estimated based on our previous experience with the resist. The exposed samples were then developed in MIBK:IPA (50:50) mix and we avoided agitation of the samples in the developer. The duration of the development step was varied in 10 seconds steps from 30-70 seconds and was followed by a rinse in IPA for 30 seconds. Note that, due to the considerable number of parameters involved in the lithography process and the fact that graphene flakes produced by mechanical exfoliation often have small sizes, the initial e-beam lithography tests were conducted on the fabricated chips (i.e. SiO_2/Si , see Figure 5.2(c)) without any graphene flakes.

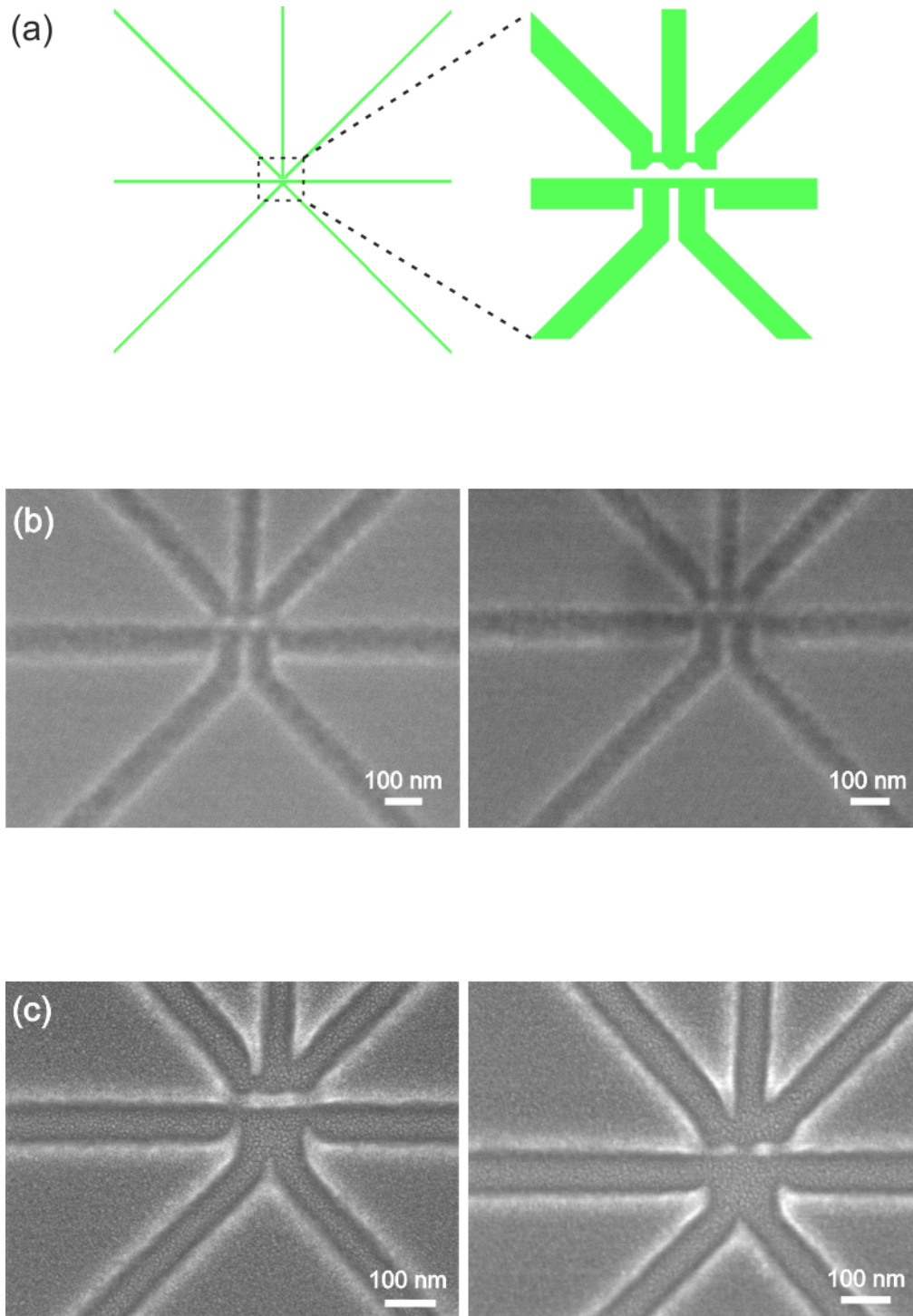


Figure 5.5 – (a) The L-edit design layout of the exposed pattern for the e-beam dose tests. The diameter of the DQD is designed 50 nm, the source and drain channels are 30 nm wide and the distance between the side-gates and the DQD is 25 nm. (b) SEM image of a developed sample after e-beam lithography. (c) SEM image of the same sample after depositing a ~3 nm layer of Au onto the sample which improved the imaging contrast significantly. The grainy texture visible in the image is also due to the Au deposition.

We used a JOEL JSM 7500F FEG-SEM system to image the developed patterns. Although we operated the beam at a low beam voltage of 2 keV but the resist-patterns disappeared fairly quickly (see Figure 5.5(b)), leaving a short time window (i.e. ~ 10 seconds) to take informative images. To overcome this issue, we deposited a very thin layer of Au (~ 3 nm) on the samples. This step improved the contrast of the SEM image significantly (see Figure 5.5(c)). The SEM images revealed that the development time needed to be 50-70 seconds. That is, the patterns that were developed for shorter than 50 seconds looked either blurry or did not even show up under SEM, suggesting the development time was too short. On the other hand, a development time above 70 seconds was found to be too long as the fine features, e.g. DQD features, looked slightly shrunken. Furthermore, although depositing a thin layer of Au improved the contrast of the SEM imaging greatly but, the obtained images did not prove to be conclusive. Because the small features, i.e. DQD and the apex of the side-gates, were still too sensitive to the e-beam and disappeared during high resolution imaging. Therefore, important information about the size of the DQD and the distances between the side-gates and the DQD could not be obtained at this stage. Images taken at lower beam energies, below 2 keV, also were found to be not very informative.

Therefore, based on the obtained results, another set of dose tests with the same e-beam base dose range were conducted but this time, the samples were developed for 50-70 seconds and the development time was varied in steps of 5 seconds. In order to preserve the fine features exposed in the resist for high resolution SEM imaging, we then metallised the samples with a Ti/Au (2 nm/5 nm) layer by manual controlling of the deposition in the Leybold LAB700 evaporator. To do this, the e-beam current was manually increased slowly whilst the samples were covered with a shutter. Once a 0.1 \AA/sec deposition rate was measured by the crystal sensor inside the chamber the shutter was opened manually and was closed when the required thickness was achieved. This avoided possible material spitting issues and/or deposition of a thicker metal layer by the automatic operation mode of the evaporator. Note that, prior to this deposition, we accurately tuned the deposition recipe by performing test depositions to calculate the tooling factor for the deposition of each material, i.e.

$$TF = TF_i \times \left(\frac{T_m}{T_x} \right). \quad (5.1)$$

TF is the final tooling factor, TF_i is the initial tooling factor, T_m is the measured thickness and T_x is the expected thickness. TF_i is usually considered to be equal to 1 to simplify the calculation. The subsequent lift-off was performed in NMP at 50 °C, without applying any agitation to the samples. Remarkably, using this approach, we found it much easier to find the right conditions for our e-beam lithography and development processes. That is, after the lift-off step, the deposited metal layer did not stay on the patterns that were either not exposed with a sufficient e-beam dose or not developed for long enough (see Figure 5.6(b, c)).

Based on the collected images from the samples, a development time of 60 seconds and an e-beam base dose of 180-210 $\mu\text{C}/\text{cm}^2$ were found to be sufficient to fabricate well-defined DQD patterns. As the final process optimisation step and to accurately choose the optimum e-beam base dose, we employed the above conditions to pattern graphene samples. Therefore, tens of graphene samples were prepared and the dose was varied in 5 $\mu\text{C}/\text{cm}^2$ steps. To transfer the lithography pattern onto our graphene samples we employed a Plasmalab System 80 Plus reactive-ion-etch (RIE) plasma etch tool. We always cleaned the RIE chamber prior to etching of our graphene samples with an O_2 plasma run. We included this step to minimise re-deposition of possible contaminants/polymers on the interior walls of the chamber onto our samples during the etching process. The O_2 plasma cleaning step was performed with a 200 sccm O_2 gas flow and a RF power of 200 W for 10 minutes.

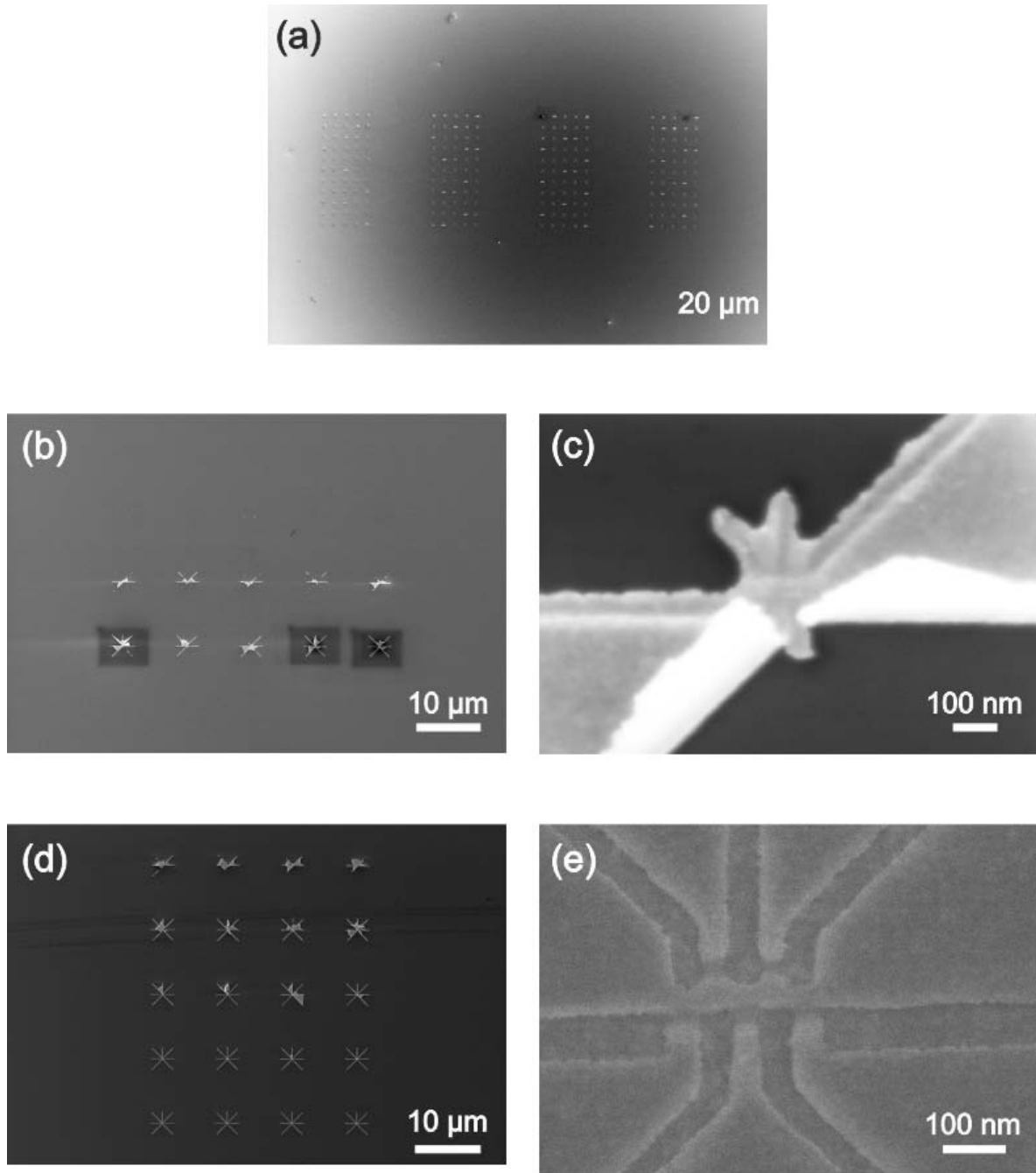


Figure 5.6 – SEM SE images. (a) The e-beam dose tests were conducted in an array of 11×5 and the array was repeated four times. The dose was increased by $10 \mu\text{C}/\text{cm}^2$ by each row. (b) Image of a sample which only two rows remained after the lift-off step, suggesting a wrong combination of e-beam dose and development time. (c) Image of a not well-defined pattern from the array shown on the left. (d) Correct combinations of e-beam dose and development time resulted in better outcomes after the lift-off step. Moreover, it can be observed that the patterns looked better as the e-beam dose was increased. (e) Image of a well-defined DQD structure.

Initially, to develop the RIE recipe, a RF power range of 10-30 W was chosen and was varied in 5 W steps. Moreover, the etching duration was varied between 5-20 seconds. To ignite the plasma a gas flow is required in the chamber. Based on previous works by other groups [130], [133], [134], [191], a Ar/O₂ gas flow was chosen. It is worth mentioning that pure O₂ gas flow can also be used to etch graphene samples [135], [192]. To our experience, an Ar/O₂ gas flow results in a more consistent DC bias voltage values at a given RF power. The ratio of Ar/O₂ gas flow varies in different literatures, e.g. 1:1 [134], 2:1 [133], 9:1 [130], [191]. We varied the Ar/O₂ gas flow ratio from 1:1-9:1. After several test runs we found that a 4:1 (Ar/O₂) ratio results in the most consistent DC bias voltage values at different RF powers but more importantly, gives the best etch results. Finally we obtained that 1-3 layers of graphene can be perfectly etched with a RF power of 15 W, a 15 seconds etch duration and a 4:1 Ar/O₂ gas flow with vacuum pressure of ~25 mTorr. After etching, the resist layer was removed in acetone (for 10 minutes) followed by IPA (for 10 minutes) and the samples were dried by N₂ blow.

However, this time, we found it challenging to find the right combination of e-beam dose and RIE conditions by SEM imaging. That was due to a combination of the beam-induced charging effect and hydrocarbon contamination in the chamber of our SEM tool which limited the resolution and the imaging quality. Examples of SEM imaging of graphene samples are shown in Figure 5.7(a,b).

As we discussed extensively in chapter 4, the Carl Zeiss OrionTM Plus Helium ion microscope (HIM) with a sub-nm resolution is a new surface imaging technique that involves scanning a focused beam of helium ions across a surface to generate an image from the resulting secondary electron (SE) emission. Since He-ions are positively charged particles the charging effect that SEM tool often suffer from is greatly minimised. In addition, the high yield of SEs generation results in remarkable imaging quality [149]. HIM imaging allowed us to take stunning images of the RIE etched patterns in our graphene samples. Examples of the taken images are shown in Figure 5.7(c,d).

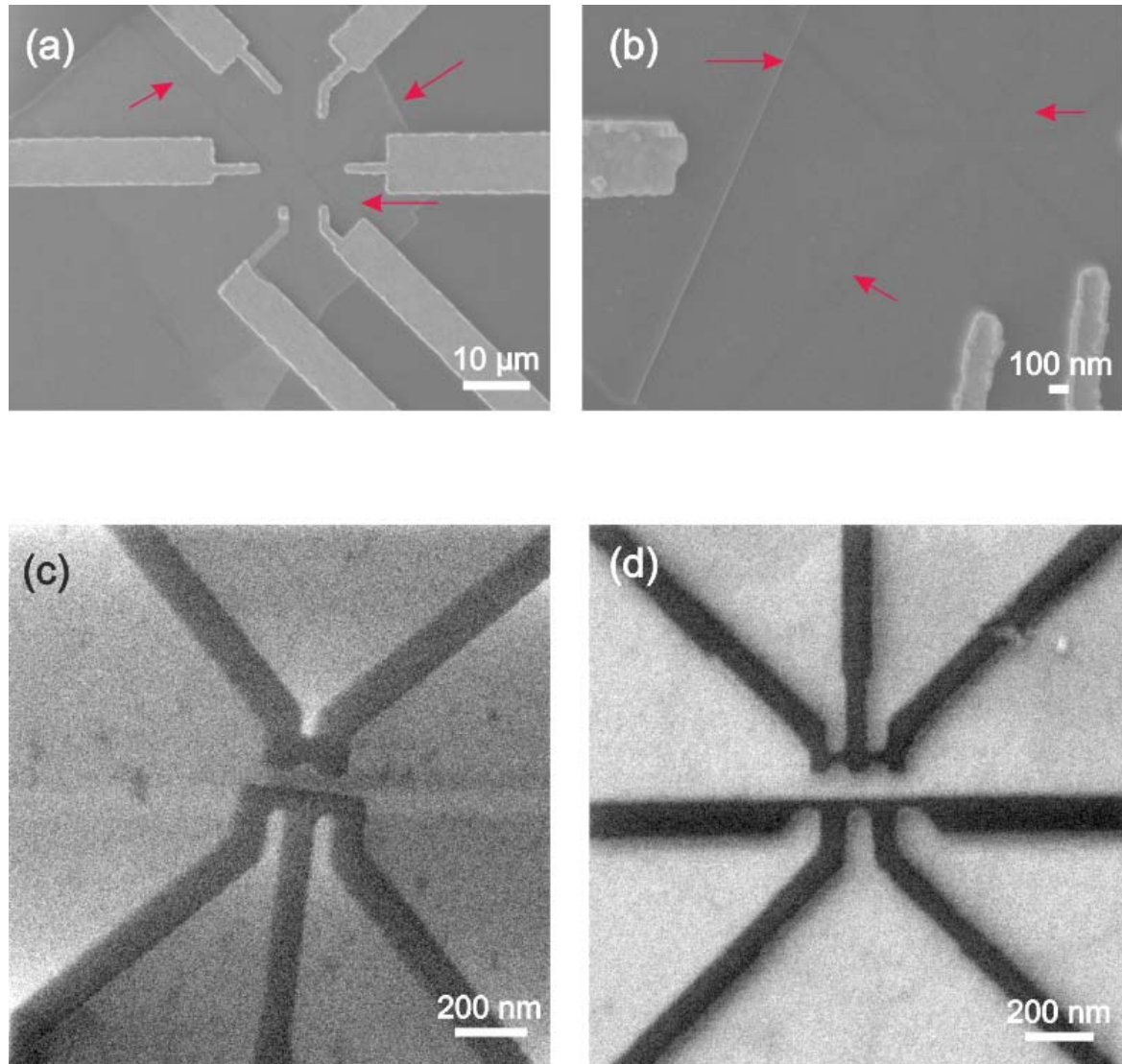


Figure 5.7 – (a) SEM SE image of an etched pattern into a graphene sample. (b) Resolution degradation at high magnification SEM imaging. The red-colour arrows in both images point to the RIE etched patterns that are hardly observable. (c) and (d) demonstrate the superb capability of HIM for high resolution imaging of graphene samples.

Based on the collected HIM images, we found the optimum e-beam dose for our patterns to be $195 \mu\text{C}/\text{cm}^2$. In addition, it is worth mentioning that we did not notice any improvement in the resolution of our patterns by increasing the pre-bake time from 70 seconds. A comparison between our fabricated GDQD patterns and previous works [135], [140], [192] reveals a decent resolution improvement with our fabrication process.

5.5 Fabrication of metal contacts onto graphene samples

The next step was to fabricate metal contacts onto the patterned graphene samples to allow electrical characterization of the devices. Carrier transport from a three-dimensional metal to a two-dimensional graphene sheet that has different density of states and working function is a very interesting subject which has attracted a lot of interest recently. The metal-graphene contact resistance limits the on-state current of graphene Field-Effect-Transistors (FETs), resulting in a compromised performance [193]–[196]. In addition to the contact resistance issue, single atomic layer of carbon is a very sensitive substrate and can be induced with defects during device fabrication very easily. For instance, thermal annealing of graphene flakes leads to heavy hole doping and severe degradation of electron mobility in graphene devices [173]. Exposing graphene flakes with a beam of high-energy particles during device fabrication, e.g. e-beam lithography, is another source which can induce defects into graphene samples, i.e. beam-induced damage.

The required dose for e-beam lithography increases depending on three parameters, (i) the desired resolution and the minimum feature size of the device design, (ii) e-beam sensitivity of the resist layer and (iii) the thickness of the resist layer. Therefore, the required dose for e-beam lithography increases with decreasing the minimum feature size in a device design. Therefore, there is a trade-off between the resolution of the lithography process and the beam-induced damage on graphene. In this regard, PMMA resist is possibly the best choice for patterning graphene samples as it requires a lower (much lower) e-beam dose than other high resolution electron sensitive resists such as ZEP520 resist (HSQ resist). But the exposure time and the exposure area for fine patterns can be short and small, respectively.

However, this is a different scenario for fabrication of metal contacts onto graphene devices. Metal contacts patterns are usually much larger than small device patterns and depending on the complexity of the device design (i.e. the required number of metal contacts for the device) the beam exposed area on a flake can be quite large with respect to the size of the flake, resulting in creation of defects and degradation of electronic properties of graphene devices. It is also worth mentioning that each metallic gate is often fabricated to occupy roughly an area of $300 \times 300 - 500 \times 500 \text{ nm}^2$ on a graphene gate to ensure a good electrical contact.

Furthermore, generally, an aspect ratio of 5:1 for resist thickness to the required metal thickness is recommended to guarantee a successful lift-off process. But the required e-beam dose for lithography increases with the resist thickness. This aspect ratio is perhaps a more critical case in fabrication of graphene devices. That is, as we will discuss later, conventional lift-off aid techniques, e.g. sample sonication, can severely damage etched patterns into graphene flakes. Therefore, sample agitation is avoided during lift-off process on graphene samples.

Electron-beam irradiation of graphene flakes was investigated in several studies [43], [44], [197], [198]. The studies reported that the radiation exposure results in a considerable disorder D peak in the Raman spectrum of graphene samples, indicating damage to the lattice. Moreover, the ratio of $I(D)/I(G)$ Raman peaks increases with the radiation dose and the exposure time [44], [197]. Furthermore, Raman spectroscopy revealed that bilayer flakes are much less sensitive than monolayer flakes to an increase in the e-beam dose [198]. Childres *et al.* [197] demonstrated that e-beam irradiation of graphene FETs shifts the Dirac point towards more negative back gate voltages (i.e. n-doping) and results in significant mobility degradation. The resultant n-doping was attributed to electron-hole generation and accumulation of holes at the SiO_2/Si interface which resulted in attraction of electrons into the graphene channel. This was also confirmed after reporting a substantially reduced shift in the Dirac point of e-beam irradiated suspended graphene devices [197].

Therefore, due to the above reasons, we tried to minimise the e-beam-induced damage during the lithography step for fabrication of the metal contacts. To this end, we chose a single layer of MMA resist. MMA resist exhibits high e-beam sensitivity and can be exposed with relatively low doses. Developing this process was a time consuming task. This was mainly because of the number of parameters involved in the fabrication of the metal contacts. Therefore, extensive effort and time were spent to develop and optimise the conditions for the resist coating (i.e. resist thickness), resist pre-bake, e-beam lithography, post-exposure development, metal deposition and lift-off processes. Each step had to be investigated and optimised several times to achieve the desirable lift-off results. This was similar to the approach we employed to develop the process conditions for patterning graphene flakes. Hence, here, we only mention the optimised conditions and parameters which resulted in successful results.

It is worth mentioning that lift-off is a process that can be tricky and destructive to both graphene flakes and/or the etched patterns. Figure 5.8 shows examples of damages occurred to the etched patterns in graphene flakes after lift-off process. Therefore, our objective was to optimise the process sequence of EBL/metal deposition/lift-off in a way to prevent such damages.

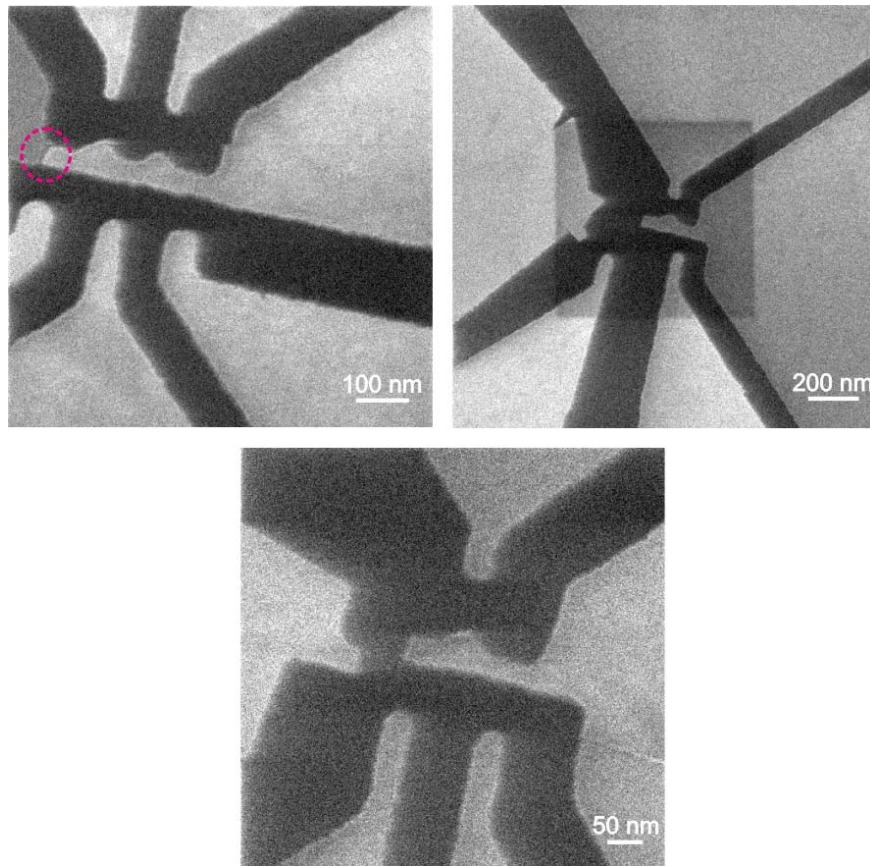


Figure 5.8 – HIM SE images. Examples of caused damages to etched patterns in graphene flakes after lift-off process. Note that in all these cases, we used a pipette to gently help the lift-off. However, evidently, even such a weak pressure (samples agitation) was found to be destructive to the etched patterns.

A single layer of MMA (8.5 EL 9) resist was spin-coated at 2500 rpm to achieve a thickness of ~370 nm (measured by ellipsometry) and was then baked at 150 °C for 70 seconds on a

hotplate. We employed GenISys software again to calculate the PEC for the e-beam lithography of our metal contact patterns. An example of a pattern after PEC calculation is shown in Figure 5.9(a), where each block of colour corresponds to a specific exposure intensity based on the PEC calculation. We found out that a low e-beam base dose of $110 \mu\text{C}/\text{cm}^2$ is sufficient to expose the resist layer, with the e-beam operating at an acceleration voltage of 100 keV. Note that, depending on the minimum feature size of the designed pattern, PEC calculations often assigned an additional exposure intensity of $\sim 30\text{-}45\%$, resulting in a total e-beam dose of $143\text{-}159.5 \mu\text{C}/\text{cm}^2$. This dose increase was assigned to the tails of the metal contacts that were designed and placed on the flakes (i.e. the beam exposed areas on the graphene flakes). This is a significantly lower e-beam dose than a $400 \mu\text{C}/\text{cm}^2$ (without PEC) which is required to expose a bilayer MMA/PMMA resist. We also investigated a bilayer resist layer of PMMA (495K)/PMMA (950K) and found a base dose of $410 \mu\text{C}/\text{cm}^2$. The significant dose reduction for the case of MMA resist can greatly minimise the possible e-beam-induced damage into graphene flakes.

After lithography the samples were developed in a 50:50 mixture of MIBK and IPA for 75 seconds, followed by a rinse in IPA for 30 seconds. Figure 5.9(b) shows an optical image of a well-defined metal contacts pattern after the EBL and development steps. The metal deposition was then performed by e-beam evaporation of Ti/Au (5 nm/60 nm) at a pressure of 3×10^{-7} mbar, a deposition rate of $0.5 \text{ \AA}/\text{second}$, with the e-beam operating at 10 keV, in a Leybold LAB700 evaporator.

Lift-off process can be a relatively simple and straightforward step in fabrication of silicon-based devices. This is mostly due to the fact that patterns etched in a silicon substrate are relatively robust and can survive strong lift-off methods such as sample sonication. However, as we mentioned and showed in Figure 5.8, etched patterns on a single layer of carbon atoms are far more delicate and can easily get damaged during a lift-off process. Hence, it is very important to optimise the conditions of the process sequence of e-beam lithography, metal deposition and lift-off in a way to ensure no sample agitation is required to achieve good lift-off results and avoid damaging etched patterns on graphene flakes.

Therefore, we performed the lift-off in NMP at 50°C followed by a rinse in DI water and IPA (for 5 minutes each). This method proved to be very effective, as often, after 70 minutes,

without applying any force to the samples, the excessive metal was completely detached from the sample and so resulting in perfect lift-off results (see Figure 5.9(c)). Figure 5.9(c) also shows the great ability of our process for fabricating dense metal contacts patterns, where metal contacts for two DQD devices (i.e. 7 metal contacts for each DQD device) on two monolayer graphene flakes in close proximity of each other are fabricated. The SEM image in Figure 5.9(d) shows successful fabrication of metal contacts on a graphene flake with minimum feature size of ~ 150 nm, i.e. the width of the tips of the fabricated metal contacts.

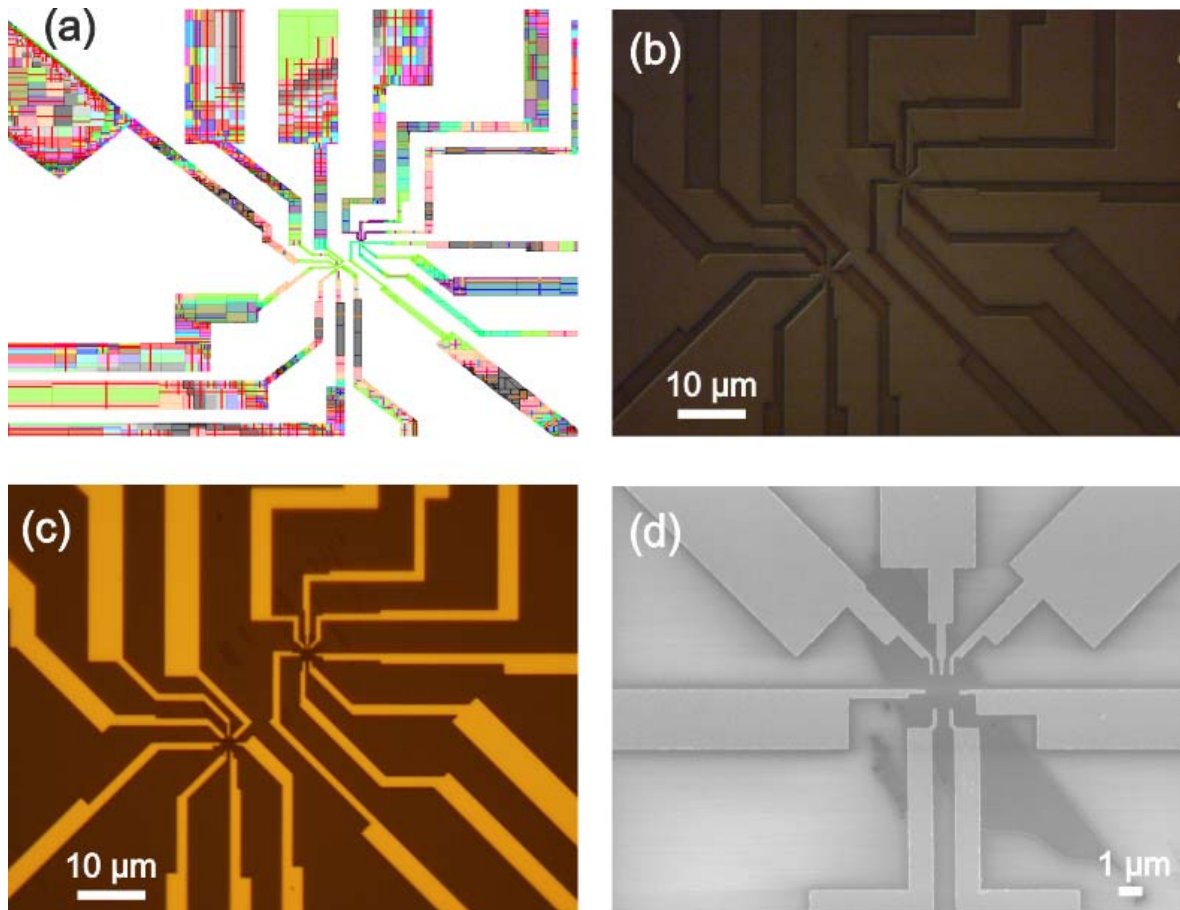


Figure 5.9 – (a) An example of a device layout after PEC calculations by GenISys software. Each block of colour corresponds to a specific exposure intensity. (b) Optical microscopy image of the pattern shown in Fig. 4.9(a) after the EBL and development processes (i.e. prior to metal deposition). (c) Optical microscopy image of successful fabrication of metal contacts onto two graphene flakes after lift-off. (d) SEM image of successful fabrication of metal contacts onto a graphene flake with minimum feature size of ~ 150 nm.

It is also worth mentioning that in our initial attempts we performed lift-off process in acetone at 30-35 °C. However, this method was found not too effective in the areas that the metal contacts were fabricated in close proximity of each other. Although a quick sonication step (10 seconds) removed the excessive metal off of the samples but, it also damaged the graphene flakes severely and in some cases, broke the fine metal contacts. The undesirable lift-off results with acetone are most likely due to its high volatility and consequent cooling effect at the sample surface. These cause a fast drying and re-deposition of stripped resist and/or metal onto the substrate as the lift-off process progresses. On the other hand, NMP is a more powerful solvent and owing to its low volatility and higher boiling temperature, lift-off can be performed at higher temperatures (e.g. NMP can be heated to 80 °C).

Note that the details/conditions of all the process steps involved in our EBL/RIE fabrication method are presented systematically as a process flow sheet in Appendix A.

5.6 Issues associated with the EBL and RIE process

In this section, we would like to address some technological issues which can affect graphene devices fabricated with EBL/RIE method.

5.6.1 Impact of the bulk graphite pieces

Production of monolayer graphene samples with low graphite density (i.e. bulky pieces of graphite) via mechanical exfoliation is a hard task. Typically, the thickness of graphite pieces can range between 10-100 nm. These small objects, which can be as large as a few μm , can impact the EBL/RIE fabrication process in two ways.

First, graphite pieces can result in an uneven resist layer thickness (e.g. in our case PMMA ~ 40 nm) during spin-coating and consequently hinder the lithography resolution. It is worth mentioning that the roughness of the SiO_2 surface layer and the metallic alignment marks (depending on their thickness) on the chip can also affect the uniformity of the resist layer.

Second, graphite pieces can cause discontinuity in the fabricated metal contacts for graphene devices. Therefore, it is crucial to design the metal contacts in such a way to avoid having them going over thick pieces of graphite. To this end, we collected optical microscopy images of the desired areas of our samples at $\times 50$ magnification. The images were then imported to AutoCAD software to locate the accurate position of the sample features relative to the chip marks. We then imported the collected coordinates to L-edit software to design the metal contacts reliably.

5.6.2 Impact of metal contacts in the EBL process

As we discussed, lift-off process can be quite challenging in fabrication of graphene devices. We also demonstrated examples of possible unintentional damage to the etched patterns into graphene samples during this process (see Figure 5.8). To prevent this, we also investigated the possibility of fabricating metal contacts prior to patterning of graphene flakes. However, it did not work. We realised that the resist layer (i.e. 40 nm-thick layer of PMMA) may get trapped/isolated in the area between the fabricated metal contacts during resist spin-coating, and so resulting in different resist layer thicknesses and affecting the lithography outcome severely. An example of such fabrication approach is shown in Figure 5.10. Moreover, for each individual device, due to random shape/size of graphene flakes produced by mechanical exfoliation, the design/arrangement of metal contacts varies. This means different resist layer uniformities (thicknesses) between the metal contacts. Therefore, it is impossible to develop a fabrication process based on this approach for mechanically exfoliated graphene samples.

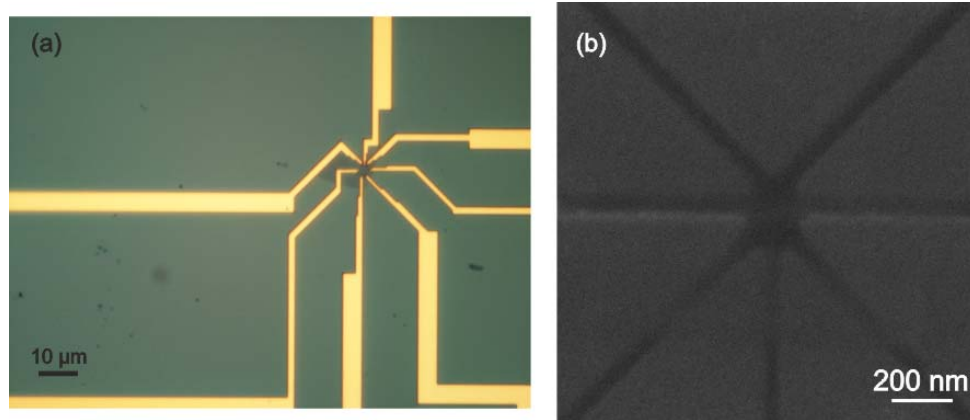


Figure 5.10 – (a) Optical microscopy image of a graphene sample with metal contacts after spin-coating of a 40 nm-thick layer of PMMA resist. Interestingly, the image contrast does not show any noticeable change in the resist layer uniformity. Note that for this fabrication approach we deposited a metal layer of Ti/Au (5 nm/25 nm). (b) HIM SE image of the same sample after EBL and RIE etch. Due to change in the resist layer thickness in the area between the fabricated metal contacts, the fine features, e.g. DQD, were not fabricated successfully.

5.7 Conclusions

In this chapter, we introduced a method for fabricating graphene quantum dots devices by means of conventional e-beam lithography followed by RIE etch. This was achieved by EBL on a ~ 40 nm-thick layer of PMMA resist followed by RIE etch in Ar/O₂ gas flow. All the steps involved in the fabrication process, which were established for the first time at Southampton Nanofabrication Centre, were explained in great detail. In order to minimise e-beam induced damage onto graphene samples during EBL of metal contacts patterns, we used MMA resist for the first time. The high sensitivity of MMA resist allowed us to expose the resist layer with a very low e-beam base dose of $110 \mu\text{C}/\text{cm}^2$. Furthermore, we argued that the graphite pieces produced during mechanical exfoliation as well as metallic features (e.g. metallic marks) on the samples can affect the uniformity (thickness) of the resist layer, and so hindering the resolution of the fabricated devices by this method. Finally, we confirmed the successful development of the fabrication process by means of HIM SE imaging.

Chapter 6

Electrical characterisations and analysis of EBL/RIE fabricated GQDs devices

In order to gain a detail insight of the viability of our fabrication process and device design in realising single electron tunnelling, we performed electrical characterisations on the devices fabricated by our EBL/RIE process. We conducted the electrical measurements at both room temperature and cryogenic temperature to study both device performance from a fabrication process yield point of view as well as the behaviour of the devices at low temperatures. Our graphene quantum dots devices were fabricated on monolayer graphene flake samples produced by mechanical exfoliation as well as CVD grown graphene samples which, to our best of knowledge, we report fabrication of GQDs devices on the latter substrate for the first time.

Furthermore, to determine the feasibility of our DQD device design for single electron tunnelling behaviour (i.e. Coulomb blockade), we present a simulation study by means of COMSOL Multiphysics and Monte Carlo single electron circuit simulations (SETSPICE) to discuss the electrical behaviour of these devices in more detail.

6.1 Room temperature characterisation

The preliminary I-V characterisations of the final fabricated devices were conducted at room temperature using a Polytech MSA-400 micro system analyser and on a Cascade Microtech probe station connected coaxially to an Agilent B1500A parameter analyser. The probe station was set-up on an optics table with intelligent tuneable vibration dampening technology to reduce electrical noise during measurement. Photos of our room temperature set-up are shown in Figure 6.1. Samples were placed in a dark cupboard and 2.4 μm -wide tungsten probe tips were used for measurement to obtain good ohmic contact with each device's Au contact pads.

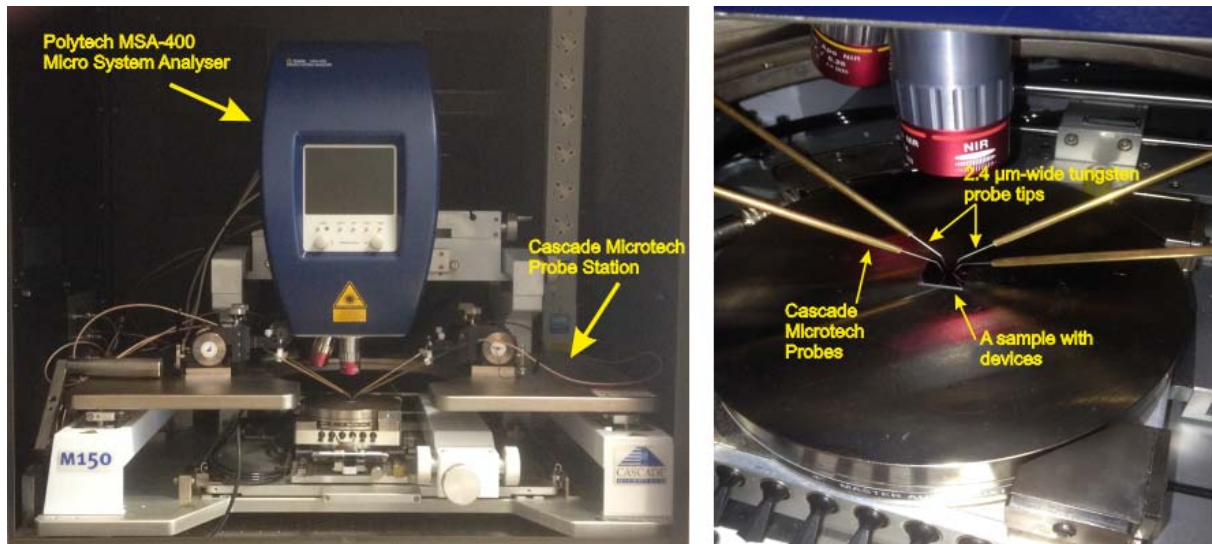


Figure 6.1 – (Right) Photo of our room temperature measurement set-up. (Left) Photo of the set-up during a measurement using tungsten probe tips to connect the device to measurement equipment.

Since the room temperature electrical characterisations for both the devices fabricated on exfoliated graphene flakes and CVD grown graphene (courtesy of Bluestone Global Tech Co.) samples resulted in similar outcomes, in this section, we focus on the electrical measurements collected from our GDQD devices on CVD grown graphene samples. Note that the CVD GDQD devices were fabricated using the same process flow as our graphene samples produced

by mechanical exfoliation (i.e. (i) EBL followed by RIE etch and (ii) EBL followed by metal deposition). Figure 6.2(a) shows successful fabrication of an array of GDQD devices (with different channel widths and dots sizes) on CVD graphene samples which clearly indicates the versatility of our fabrication process. Furthermore, to our best of knowledge, this is the first attempt at obtaining such high density and high resolution graphene quantum dots devices with high reproducibility in such large numbers.

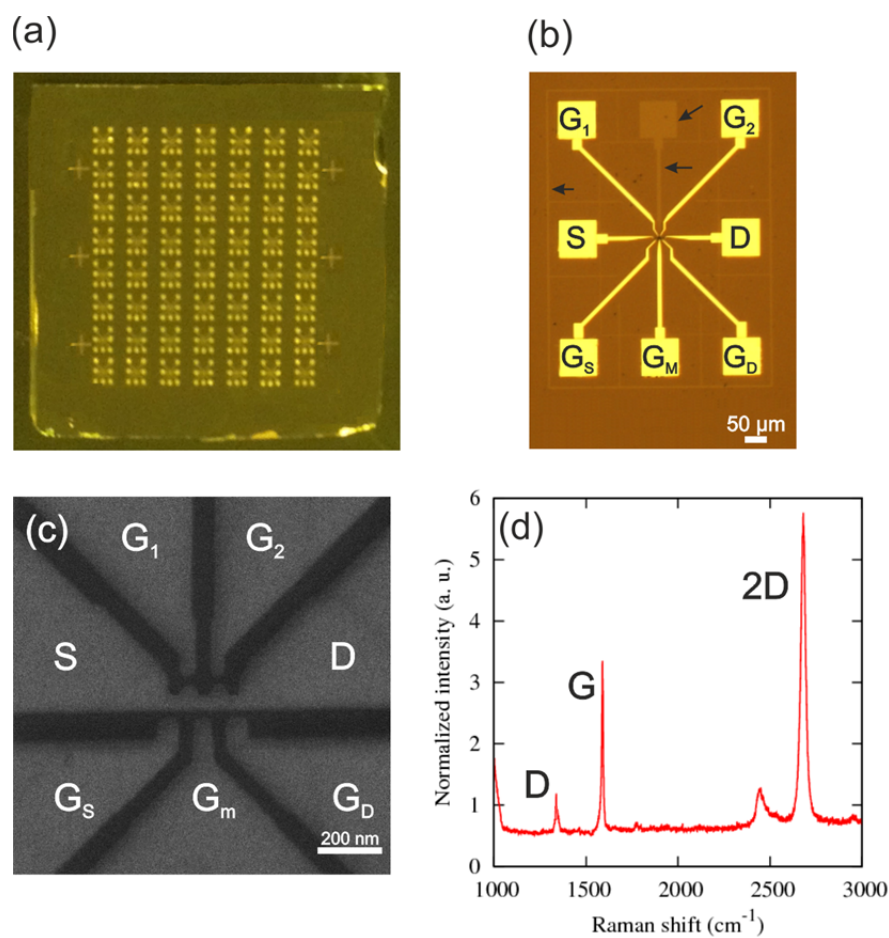


Figure 6.2 – (a) Optical image of an array of GDQD devices successfully fabricated on a CVD graphene sample. (b) Optical microscopy image of a fabricated GDQD device on a CVD graphene sample. The black arrows point to the RIE etched patterns. (c) HIM SE image of a device with similar dimensions as the one electrically characterised in this section, with channel width of $\sim 55\ \text{nm}$ and dots size of $\sim 85\ \text{nm}$. (d) The Raman spectrum of the CVD graphene sample collected using a Renishaw InVia Raman Spectrometer with a $532\ \text{nm}$ wavelength laser (at a power of $0.2\ \text{mW}$), prior to the device fabrication.

Figure 6.2(d) shows the Raman spectrum of the CVD graphene sample, collected using a Renishaw InVia Raman Spectrometer with a 532 nm wavelength laser (and under the laser conditions explained in Chapter 5), prior to the device fabrication. However, in addition to the G and 2D peaks, the spectrum exhibits a noticeable D peak at $\sim 1350 \text{ cm}^{-1}$ [86] which was absent in our graphene samples produced by mechanical exfoliation (see Figure 5.4(c)). As discussed in section 2.4.3, the D peak arises due to existence of defects/disorder in graphene lattice [86], [87]. In CVD graphene, the D peak can originate due to existence of grain boundaries (i.e. poly-crystalline structure), suggesting lower degree of crystalline order to that of graphene samples produced by mechanical exfoliation [199]. In fact, it has been demonstrated that in CVD graphene samples significant intervalley scattering mechanism can occur at the grain boundaries [52].

Using our measurement set-up, Figure 6.3(a) shows a plot of linear (ohmic) $I_{DS} - V_{DS}$ behaviour (with almost no measurable current leakage from the channel and the DQD) for one of our DQD devices, whilst all other side-gates (see Figure 6.2(c)) were grounded. To confirm the desired pattern (see Figure 6.2(c)) was etched successfully in graphene, we also measured the devices for possible gate-leakage between the in-plane graphene side-gates. This was achieved by measuring the current through each side-gate by sweeping the bias voltage whilst every individual side-gate was grounded. The currents measured between all side-gates lay within the noise levels of the measurement equipment (in fA range) and so can be considered to be negligible, indicating the RIE process was developed successfully and the desired pattern (see Figure 6.2(c)) was transferred into the graphene sample faithfully.

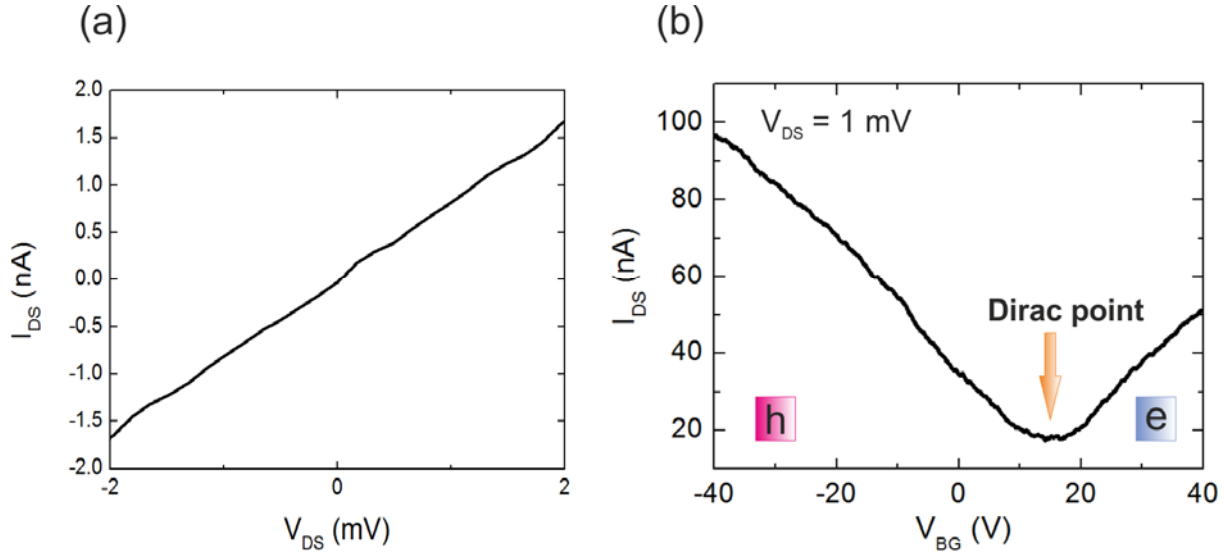


Figure 6.3 – Room temperature I-V characterisations, i.e. $T = 300$ K. (a) Ohmic behaviour of bias current I_{DS} as a function of applied bias voltage V_{DS} . (b) Ambipolar behaviour of the device with $V_{DS} = 1$ mV, where h (e) represents hole (electron) carrier transport regime.

Figure 6.3(b) shows a plot of the measured ambipolar behaviour in the device which clearly shows that the charge carriers can be tuned between electrons and holes in the channel by sweeping the back gate voltage V_{BG} . Based on this measurement, we estimated the Dirac point to be at $V_{BG} \approx 16.5$ V. The shift in the location of the Dirac point (which can be found at $V_{BG} \approx 0$ for an undoped pristine graphene flake) is due to organic contaminants (e.g. resist residues) that can reside on the samples during fabrication process and result in spurious doping in graphene [9], [59].

Based on the room temperature measurements, we also estimated the yield of our fabrication process. Estimation of the statistical yield of our fabrication process at this stage was due to several factors. This was mainly because of our limited access to low temperature measurement facilities which usually led to long-time gaps between the fabrication and the electrical characterisations of the final fabricated devices (and so possible degradation of the electrical properties of the device in time) at cryogenic temperatures. Furthermore, fabricated devices can get damaged during sample preparation (e.g. sample dicing and wire-bonding) for cryogenic temperatures measurement, and so affecting the statistical estimation of our

fabrication process yield. On the other hand, spontaneous death of graphene samples after cool down has also been reported [200].

Therefore, based on the room temperature measurements, we obtained a process yield of $\sim 80\%$ (from 57 fabricated devices) for the devices fabricated in graphene samples produced by mechanical exfoliation and a process yield of $\sim 58\%$ (from 160 fabricated devices) for the devices fabricated in CVD graphene samples. These values represent the percentage of the fabricated QD devices which had to exhibit ambipolar behaviour, no observable current leakage from the channel, no observable current leakage between in-plane graphene gates, and no observable back gate leakage through the SiO_2/Si substrate. We attributed our lower process yield for the devices that were fabricated in CVD graphene samples to the quality (see also the Raman spectrum in Figure 6.2(d)) and consistency of the purchased samples. That is, our CVD graphene samples featured small grain boundaries, areas of removed graphene, cracks (physical damage) and wrinkles.

To our best of knowledge, there is no systematic study on the fabrication yield of graphene QD devices. This may be partly due to the fact that only very few groups are actively working in this very new field. However, recently fabrication of graphene QD devices on mechanically exfoliated graphene samples was claimed to be technologically challenging and a very low fabrication yield of $\approx 10\%$ was reported [201]. In that study, parameters such as non-working metal contacts, leakage to the back gate and side-gate leakage were identified to negatively impact the EBL/RIE process yield [201]. Therefore, in comparison, our estimated process yield values indeed suggest a great improvement in reliability of our EBL/RIE process for fabrication of graphene QD devices to that of developed by others. We achieved our higher fabrication yield by accurately optimising conditions of all the steps involved in the fabrication process, as we explained in chapter 5.

6.2 Cryogenic temperature characterisation

The fabricated GDQD devices behave similar to a graphene nanoribbon (GNR) device at room temperature. That is, as we discussed in section 3.2.1, in order to observe Coulomb blockade

effects, the thermal energy must be suppressed to prevent the electrons entering or exiting the QD freely.

Due to the absence of required characterisation facilities in the University of Southampton, the cryogenic temperature measurements were conducted in our project collaborator's laboratory by Prof Muruganathan Manoharan and Mr Takuya Iwasaki in the Japan Advanced Institute of Science and Technology (JAIST).

These measurements were conducted in a low temperature probe station "Grail10-308-X-4K-LV" from Nagase Techno-Engineering Co., Ltd. The chamber is facilitated with a GM-JT (Gifford McMahon-Joule Thomson) refrigerator which can offer a lowest temperature of 4.5 K on the chamber's stage. However, according to our test results, the temperature at the sample surface is ~ 6 K. Coaxial tungsten needles were used for the measurements to obtain good ohmic contact with each device's Au bond pads. Outside the vacuum chamber, the wire connections to the probes were made by tri-axial low noise cables. We also used Agilent Technologies B1500A device analyser which offers a voltage resolution of $25 \mu\text{V}$ and a current resolution of 1 fA . Figure 6.4 shows our low temperature measurements set-up at JAIST.

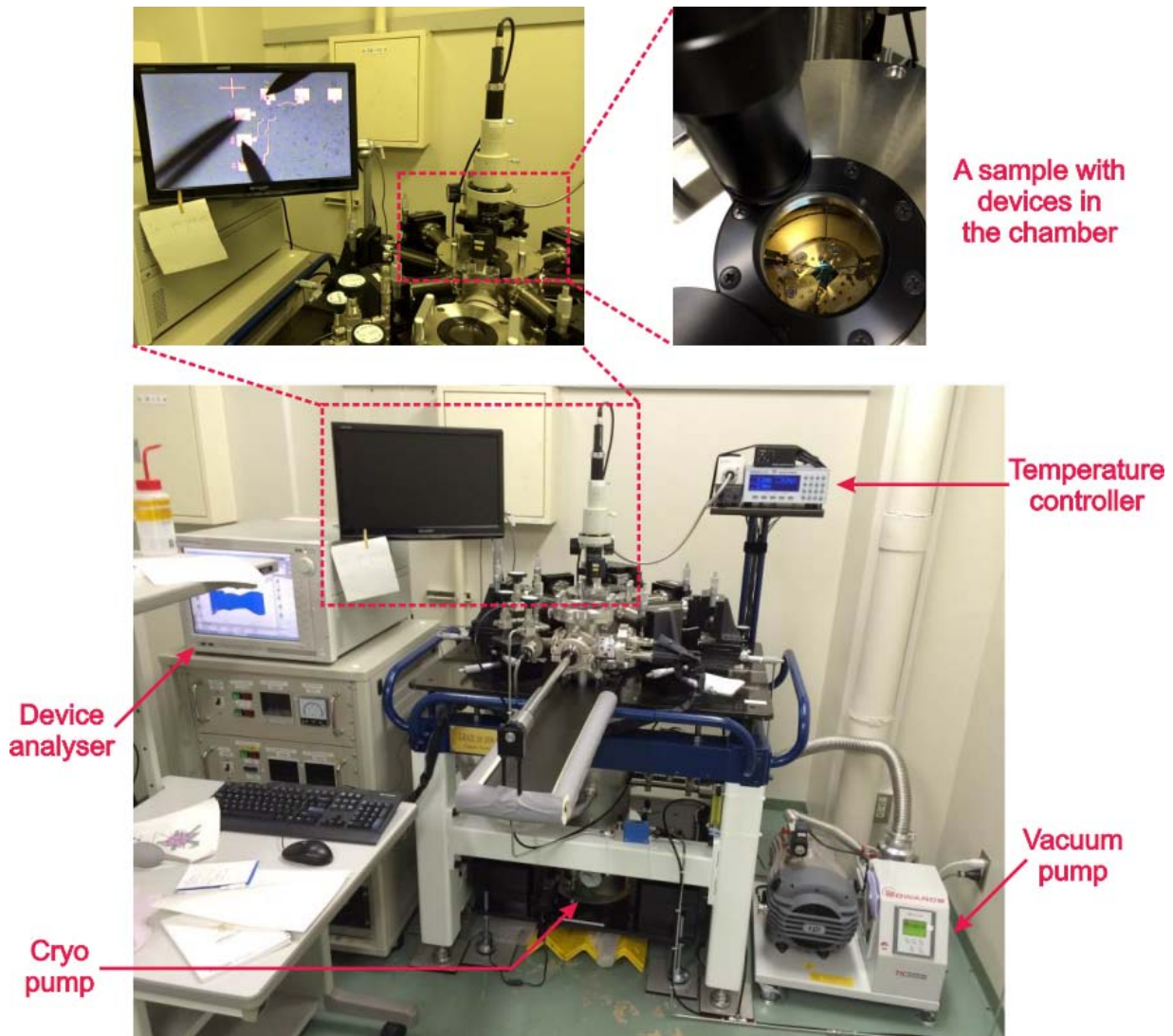


Figure 6.4 – Our low temperature measurement set-up at JAIST.

6.2.1 DQD devices fabricated in CVD grown graphene samples

In the following, we discuss the electrical characterisations of two of the CVD graphene DQD devices, with similar dimensions as the device shown in Figure 6.2(c), measured at cryogenic temperature. We name these two devices as device *A* and device *B*. It is worth mentioning that the two devices had similar geometries and were chosen randomly from the array of devices shown in Figure 6.2(a). Using our measurement set-up at JAIST, the two devices were measured at ~ 6 K (the temperature at the base of the substrate) and at a chamber pressure of $\sim 10^{-4}$ Pa.

Figure 6.5(a) shows the schematic L-edit design of the device A which exhibited a large current leakage across the red-colour arrow-line and small current leakage across the blue-colour arrow-lines. The small current leakage across S-G_s terminals (see Figure 6.5(a)) is weakly observable in Figure 6.5(b) where the measured I_{DS} is slightly smaller for positive V_{DS} voltages than that of for negative V_{DS} voltages. By tuning the back gate voltage at the Dirac point (found at room temperature, see Figure 6.3(b)) and sweeping the bias voltage, $I_{DS} - V_{DS}$ plot exhibited a weak nonlinear behaviour, which is shown in Figure 6.5(b). This nonlinear $I_{DS} - V_{DS}$ behaviour is due to Coulomb blockade (as explained in section 3.2.1 and see also Figure 3.4(a)). However, it is evident that the current was not fully suppressed and the Coulomb blockade region is not well-defined. This can be easily explained based on our discussion in section 3.2.1. That is, one of the two main criteria to observe CB is to ensure the thermal energy is much lower than the charging energy of the dot E_C , i.e. $k_B T \ll E_C$. This condition can be examined for our device by considering the GDQD device as two QDs with diameter of $D = 85$ nm. In the case of graphene, the total capacitance of each dot can be estimated by assuming the self-capacitance of a circular disk of a diameter D which can be calculated as [115], [202], [203]:

$$C_{self} \approx 4\epsilon_0\epsilon D, \quad (6.1)$$

where $\epsilon_0 = 8.85 \times 10^{-12}$ F/m. Following Refs. [115], [123], [140], [202], for the dielectric constant we use $\epsilon = (\epsilon_{ox} + 1)/2 \approx 2.5$ which is an average between the underlying SiO₂ and the vacuum on top of the sample. Therefore, the capacitance between the QD and the back gate can be estimated as $C_{bg} \approx 7.5$ aF and consequently, $E_C = e^2/C_{bg} \approx 21.3$ meV. On the other hand, thermal energy at $T \sim 6$ K is equal to $k_B T = 0.51$ meV, where k_B is Boltzmann constant (i.e. $\sim 8.61 \times 10^{-5}$ eV/K). Indeed, since $E_C > k_B T$ the nonlinearity can be observed in the $I_{DS} - V_{DS}$ plot. However, in our case, E_C is not sufficiently larger to suppress thermal fluctuations [123], [125], [130], [134], [141], and so a well-defined CB region was not observed in Figure 6.5(b).

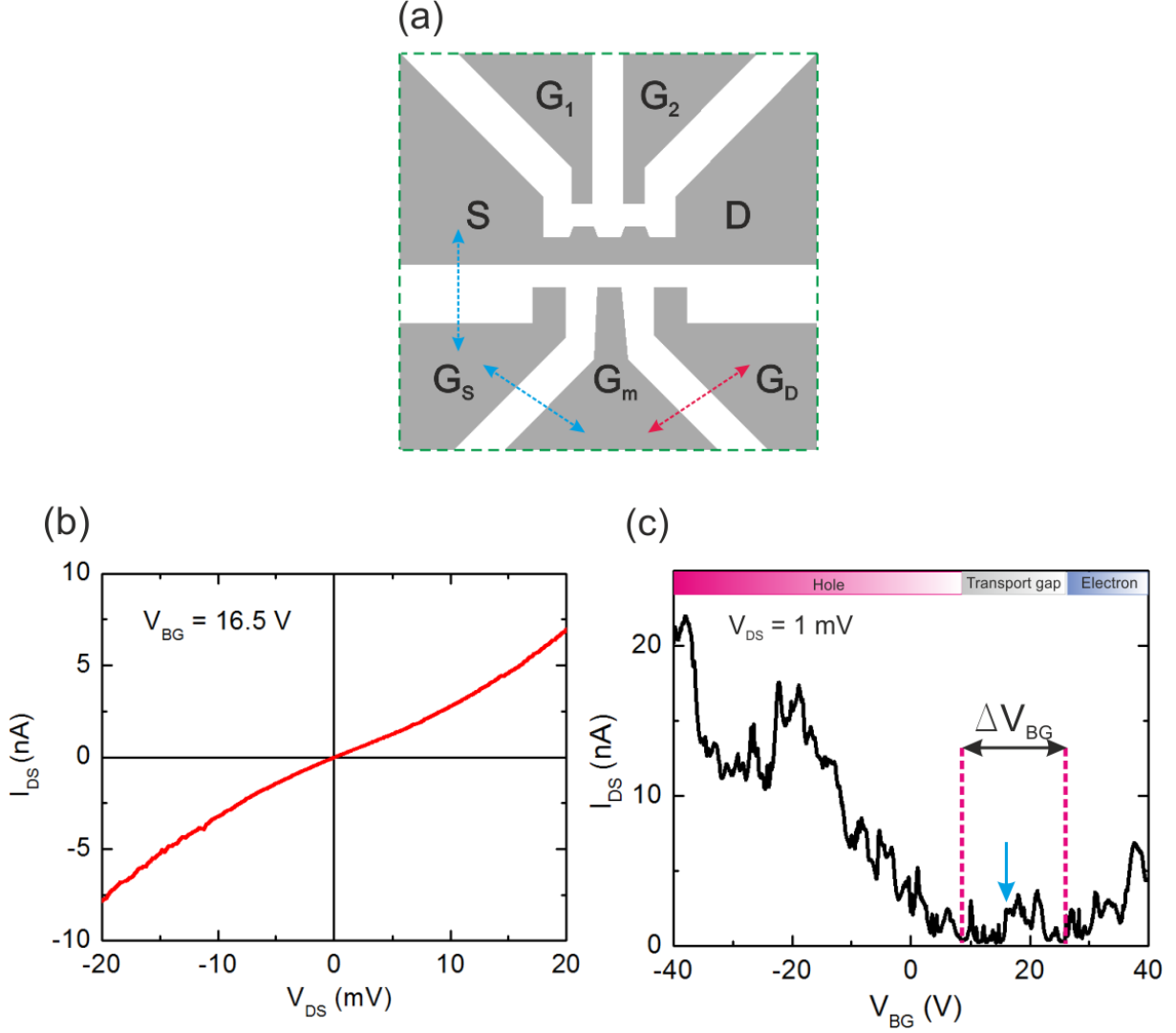


Figure 6.5 – Cryogenic temperature electrical measurements of the device *A* at $T \sim 6$ K and at chamber pressure of $\sim 10^{-4}$ Pa. (a) Schematic L-edit design of the device *A* where the red-colour (blue-colour) arrow-line indicates a large (small) current leakage that was measured in the device. (b) Observation of a nonlinear $I_{DS} - V_{DS}$ behaviour due to Coulomb blockade around $V_{DS} \approx 0$ V, with $V_{BG} = 16.5$ V. (c) A plot of $I_{DS} - V_{BG}$ which clearly shows a region of suppressed current ($\Delta V_{BG} \sim 17$ V) around the Dirac point, with $V_{DS} = 1$ mV. Note that in both measurements all the in-plane graphene gates are grounded.

In addition to the presence of thermal activation energy in our measurements, the high current through the device and absence of a well-defined CB region in the $I_{DS} - V_{DS}$ plot can be also

attributed to the barrier height of the graphene channels (i.e. transparency of the potential barriers) and co-tunnelling effect (i.e. parallel tunnelling events).

As we mentioned in section 3.2.1, in addition to the condition $k_B T \ll E_c$, the tunnel barriers' resistance must be much higher than the quantum resistance ($R_T \gg R_Q$) to ensure localisation of an electron (i.e. the energy uncertainty to be much smaller than the charging energy) on the QDs, and so resulting in Coulomb blockade (CB) effects. A direct consequence of transparent tunnel barriers (i.e. tunnelling resistance is not large compared to the quantum resistance) is a phenomenon known as co-tunnelling. In the case of co-tunnelling, two or more electrons tunnelling events can occur simultaneously, which negatively impacts controllable manipulation of single electron devices and results in higher current flow through a QD device [204], [205]. As we mentioned, the tunnel barrier resistance can be calculated using Eq.(3.8) (i.e. by calculating single electron tunnelling per unit time through a potential barrier). The tunnel barrier height (and so the tunnelling rate) in a GQD device can be tuned electrostatically by applying voltage to the side-gates (i.e. side-gates G_S , G_M , G_D in Figure 6.2(c) and Figure 6.5(a)). However, we were unable to perform this due to the limitation of our measurement tool. On the other hand, using a crude approximation a Coulomb blockade region of ~ 5 mV can be estimated from the $I_{DS} - V_{DS}$ plot. Based on this approximation, it can be argued that outside of the estimated Coulomb blockade region the plot exhibits a linear behaviour, suggesting that the fabricated device has symmetric tunnel barriers [99].

Furthermore, in section 3.3.1 we discussed that the conductance level of graphene nanoribbons (GNRs) is proportional to their width [112], [114]. Ponomarenko *et al.* suggested that GNRs with $W > 40$ nm exhibit too high conductance (i.e. high barrier transparency) and Coulomb blockade effects in GQD devices are weakened and are smeared with increasing the width of the GNRs [123]. In fact, the majority of previously reported GQD devices were constructed with 20-40 nm wide graphene channels [115], [123]–[127].

On the contrary, however, successful observation of single electron tunnelling and even excited states in GQD devices with channel widths of 50-70 nm has been demonstrated [130], [131], [140]. In those cases though, the thermal energy was more effectively suppressed compared to our experiment. That is, the successful observation of single electron tunnelling for a GQD device with ~ 50 nm wide channels was achieved at $T \sim 1.7$ K [130], [131]. More interestingly,

observation of excited states for a GQD device consisting of a ~ 60 nm and a ~ 70 nm wide channels was reported at $T \sim 200$ mK [140]. Therefore, these works may suggest that for our devices with ~ 55 nm wide channels a more pronounced Coulomb blockade effects could have been observable if, (i) the thermal energy was more effectively suppressed, and (ii) by electrostatic tuning of the barriers heights using the fabricated side-gates.

In agreement with other works [81], [82], [106], [113], we observed a region of strongly suppressed current (i.e. transport gap ΔV_{BG}) around the Dirac point in the $I_{DS} - V_{BG}$ plot which separated the hole transport regime (left inset in Figure 6.5(c)) from the electron transport regime (right inset in Figure 6.5(c)). We quantified the size of the transport gap by searching for the smoothened conductance trace over a back gate V_{BG} range [106] (see Figure 6.5(b)). Based on this, we estimated a transport gap of $\Delta V_{BG} \sim 17$ V. The transport gap is expected to be mainly caused by the local tunnel barriers (i.e. the three 55 nm-wide GNR constrictions, see Figure 6.2(c)) [131], [141], which was also reported for GNRs [81], [106], [113].

The exact origin of large number of reproducible sharp current resonances inside the transport gap is an on-going debate. However, it has been demonstrated that observation of these current resonances can be attributed to unintentionally formed localised electronic states or quantum dots during patterning/etching of graphene flakes [81], [106] and/or interaction effects due to edge roughness, disorder or bond contractions at the edges of graphene flakes [106]. It has been demonstrated that the broadening of some of these resonance peaks inside the transport gap is limited by temperature rather than by the lifetime of the resonance [81], [82]. However, as mentioned, the overall hole-doping (referring to the location of the transport gap with respect to the V_{BG}) is most likely due to produced organic contaminants on the graphene during fabrication process [59] and atmospheric O_2 binding (and moisture) [141].

In order to access the DQD regime, we fixed the V_{BG} to a value inside the transport gap (the region pointed by the blue arrow in Figure 6.5(b)), where it seemed I_{DS} was effectively suppressed. Figure 6.6(a) shows a colour plot of $V_{DS} - V_{BG} - I_{DS}$ where regions of suppressed I_{DS} can be observed in the V_{DS} direction inside the transport gap region. The suppression of I_{DS} in V_{DS} direction differs to that of observed in the $I_{DS} - V_{BG}$ plot (see Figure 6.5(c)). The ΔV_{BG} (shown in Figure 6.5(c)) is measured at constant V_{DS} but varying Fermi energy E_F , and so is

related to a change in Fermi energy ΔE_F in the device, i.e. transport gap. On the other hand, varying the V_{DS} value (i.e. bias window) at a fixed E_F leads to an effective energy gap ($E_g = e\Delta V_{DS}$) [81], [115].

At sufficiently low temperatures, I_{DS} (carrier transport) is dominated by well distinguishable diamonds of suppressed current (i.e. Coulomb diamonds) [81], [82], [106]. However, in our case (shown in Figure 6.6), the $V_{DS} - V_{BG} - I_{DS}$ plot appears to exhibit extremely dense arrangements of Coulomb diamonds that are smeared together and have different sizes. Figure 6.6(a) shows a region inside the transport gap ΔV_{BG} where the height of the Coulomb diamonds (the extent in V_{DS} direction) can be used to estimate the energy gap E_g of the fabricated graphene channel. Based on a crudely estimated Coulomb blockade region of ~ 5 mV from the $I_{DS} - V_{DS}$ plot shown in Figure 6.5(b), an $E_g \approx 5$ meV is marked in Figure 6.6(a). The larger E_g values in the $V_{DS} - V_{BG} - I_{DS}$ plot could have originated from smaller unintentional quantum dots (i.e. charged islands) that were formed during the etching/patterning along the edges of the graphene flake. Formation of unintentional QDs along the edges of graphene nanoribbons after etching/patterning was discussed in section 3.3.1 in great detail. Hence, the largest E_g value in the $V_{DS} - V_{BG} - I_{DS}$ plot corresponds to the charging energy of the minimum (the smallest) unintentional island size (QD) formed along the edges of the graphene channel, i.e. the minimum island size corresponds to the maximum charging energy $E_{c,max}$ [81], [106], [115]. Furthermore, the yellow-dashed lines in Figure 6.6(b) highlight the edges of our estimated Coulomb diamonds. However, it is evident that the conductance value changes inside the estimated diamonds, indicating that the estimated Coulomb diamonds may consist of smaller diamonds. These observations can be attributed to four parameters.

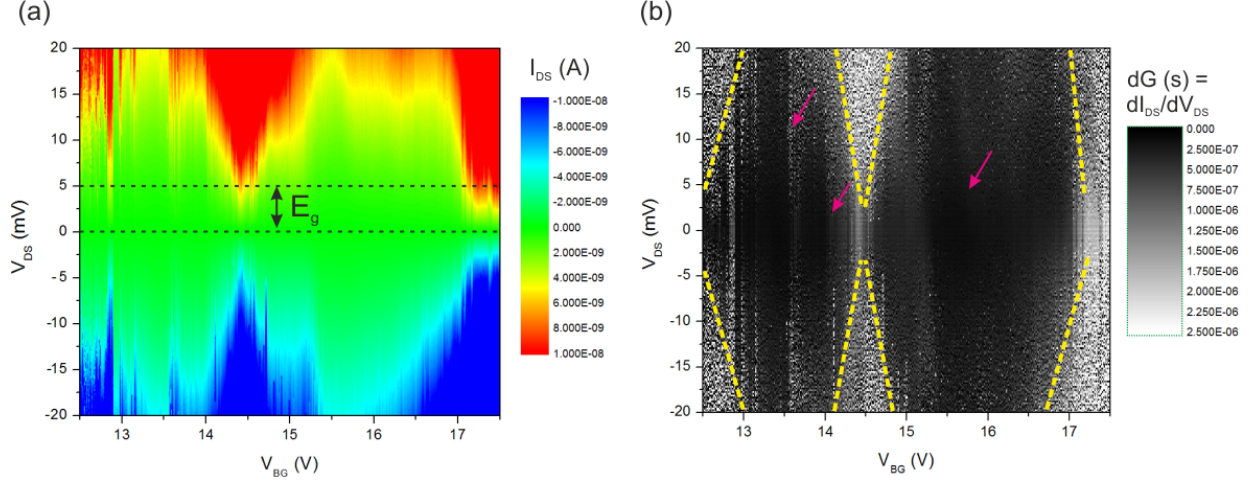


Figure 6.6 – Cryogenic temperature electrical measurements of the device *A* at $T \sim 6$ K and at chamber pressure of $\sim 10^{-4}$ Pa. (a) A colour plot of $V_{DS} - V_{BG} - I_{DS}$, exhibiting an $E_g \approx 5$ meV. (b) A contrast plot of $V_{DS} - V_{BG} - dG$, exhibiting faint Coulomb diamonds as well as change in conductance inside the estimated diamonds.

I) Indeed, one dominant contributing factor is the thermal energy. As we discussed, at $T \sim 6$ K, the thermal energy was not sufficiently suppressed in our experiment to observe pronounced (strong) Coulomb blockade effect in I_{DS} as a function of V_{DS} , and so CB region in $I_{DS} - V_{DS}$ plot (see Figure 6.5(b)). This was also confirmed by estimating the charging energy of the QDs ($E_C \approx 21.3$ meV) which was found not to be adequately larger than the thermal energy to satisfy CB requirement. As a result, the electrons could still travel (quasi-)² freely through the graphene channels and only a weak CB effect was observed (see Figure 6.5(b)). Consequently, we cannot observe well-defined Coulomb diamonds in the $V_{DS} - V_{BG} - I_{DS}$ plot shown in Figure 6.6(a). In fact, observation of well-defined CB behaviours, e.g. Coulomb diamonds or (side) gate modulation of bias current, is achieved by balancing thermal energy and V_{DS} value. Therefore, V_{DS} value is usually applied in agreement with condition $V_{DS} \ll 4k_B T$ [81], [106], [112]. However, in our case, one may suggest that $V_{DS} = 1$ mV was slightly larger than it should have been. This is evident in Figure 6.7 where it can be seen that in the transport gap

² Note that based on figure 2.3, we achieved to observe a nonlinear $I_{DS} - V_{DS}$ behaviour, which suggests that the electron transport in the device was suppressed to some extent at $T \sim 6$ K. Therefore, electrons could not travel through the graphene channel completely free.

region of the device A the conductance level never reaches zero and the conductance resonances are not very distinguishable.

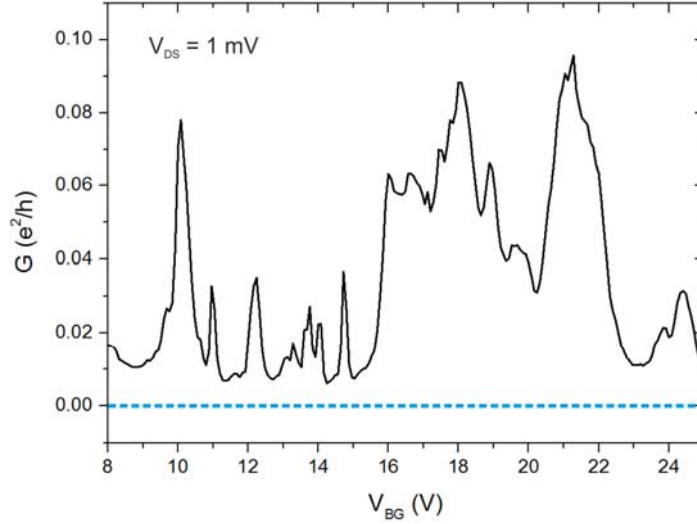


Figure 6.7 – Cryogenic temperature electrical measurements of the device A at $T \sim 6$ K and at chamber pressure of $\sim 10^{-4}$ Pa. Observation of sharp (but not well-distinguishable) conductance resonances in the transport gap region of the device, where the conductance is not fully suppressed for $V_{DS} = 1$ mV. This observation is attributed to the V_{DS} value and the thermal energy.

II) As we discussed in section 3.3.1, generally, observation of many sharp and strong Coulomb diamonds in $V_{DS} - V_{BG} - I_{DS}$ plot inside the transport gap region is attributed to charged islands (or QDs) that can be formed unintentionally during etching/patterning of graphene nano constrictions [81], [82], [106]. The formation of these charged islands can arise in the presence of a quantum confinement energy gap in conjunction with a strong bulk and/or edge-induced disorder potential. These localised states can lead to strong current modulations inside the transport gap region (ΔV_{BG}) which can be seen as Coulomb diamonds of suppressed current by varying the V_{DS} at cryogenic temperatures (see Figure 6.6(a)). Since these unintentional QDs have random sizes, they exhibit different charging energies, and so appear as Coulomb diamonds with different sizes in $V_{DS} - V_{BG} - I_{DS}$ plot at low temperatures. In fact, these

charged islands can affect tunability of graphene QD devices and were found to pose a serious challenge in understanding and further progress in the field of graphene QIP [125], [126]. That is, in a graphene quantum dot device not only the dot can be charged, but also the localised states in the constrictions. As a result, transport resonances in the constrictions were found to lead to non-monotonic modulations of tunnelling between the two dots and between the dots and the leads (i.e. source and drain) in a GDQD device [125], [126]. Furthermore, Molitor *et al.* suggested that these resonances may also result in additional conductance resonances inside bias triangle of GDQD devices [125].

III) As we mentioned, it has been reported that existence of organic contaminants (e.g. chemisorption of oxygen, moisture and resists residues produced during device fabrication) on the surface of a graphene sample can result in hole doping, and so shifting of the position of the Dirac point towards more positive back gate voltages [59], [60], [141]. Chemisorption of oxygen and moisture and consequent hole doping can occur naturally in time even in pristine graphene flakes [177], [206]. In this regard, it has been also reported that the roughness of underlying SiO₂ substrate can greatly increase the level of hole doping by causing structural deformation and regions of curvature in graphene lattice [206]. These curved regions can lead to sp³ C orbital character and π -orbital misalignment (or weakening of the π bonds) and increase chemical reactivity [175], [206]. On the other hand, the uncontrollable surface contamination coverage of resist residues can lead to large variation in properties of graphene devices [173]. Depending on the extent of doping level, the resultant spurious doping could appear as additional features in $I - V$ plots (e.g. bias current oscillations and/or spontaneous change in graphene resistance) of a fabricated device [9], [207]. In fact, we observed similar electrical properties in the device *B*. Figure 6.8(a) shows random spontaneous changes in resistance in $I_{DS} - V_{DS}$ plot of the device *B*, which also exhibits an overall resistance much higher than the device *A*. If such behaviour is attributed to spurious doping of the graphene flake by organic contaminants, then our hypothesis is that perhaps for the device *B* the graphene region was structurally deformed (due to roughness of the underlying SiO₂ substrate) which led to a greater chemical reactivity, and so much higher doping level in the device [175], [206]. However, based on the $V_{DS} - V_{BG} - I_{DS}$ of the device *B* (see Figure 6.8(b)), we estimated $E_g \approx 11.2$ meV which is comparable to that of estimated for device *A* and in other work [83].

This suggests that our fabrication process transferred the desired DQD pattern in the graphene flakes faithfully and possibly, other parameters (i.e. spurious doping, grain boundaries in CVD graphene) resulted in the observed different electrical characteristics of the two devices. It is worth mentioning that we measured no current leakage via the channel, between the side-gates, or via back gate in the device *B* which suggested successful etching of the graphene flake.

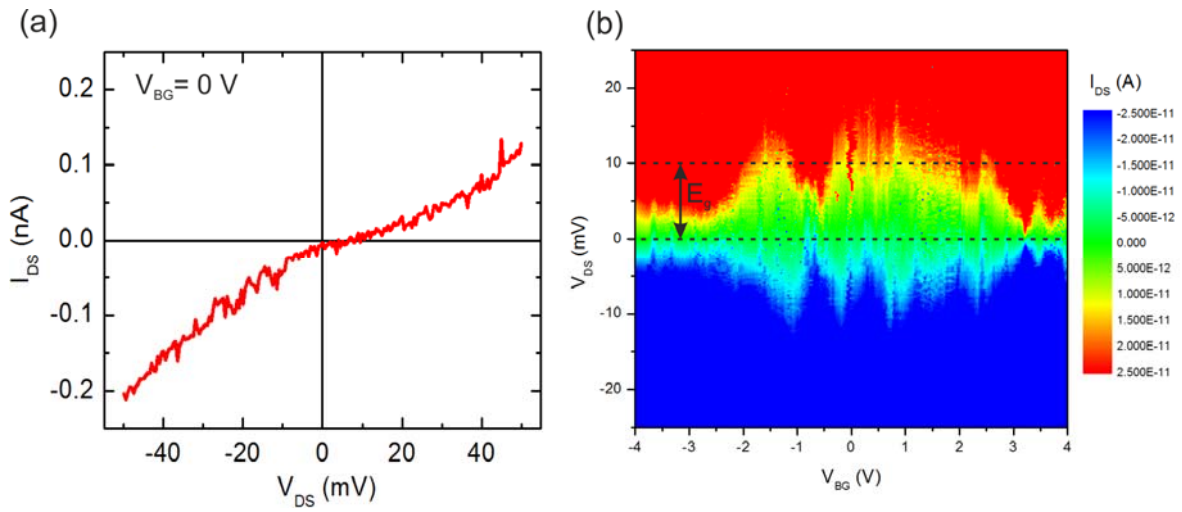


Figure 6.8 – Cryogenic temperature electrical measurements of the device *B* at $T \sim 6$ K and at chamber pressure of $\sim 10^{-4}$ Pa. (a) $I_{DS} - V_{DS}$ plot exhibiting random spontaneous changes in the resistance of the graphene channel which can be attributed to spurious doping by organic contaminants on the sample. (b) $V_{DS} - V_{BG} - I_{DS}$ colour plot which an $E_g \approx 11.2$ meV can be estimated in the direction of the V_{DS} axis due to formation of unintentional charged islands (QDs) after patterning of the graphene flake. Note that we did not measure current leakage in the device *B*.

Furthermore, the overall higher resistance of the device *B* than that of for the device *A* can be explained as follow. The organic contaminants have been also suggested to behave as external carrier scattering sites, and so result in carrier mobility degradation in graphene devices. This was discovered by electrical characterisation of fabricated graphene devices before and after an annealing process (thermal annealing [59] and current annealing [60]) which a considerable

increase in the carrier mobility was measured after annealing [59], [60]. Therefore, we can safely suggest that carrier mobility decreases with increasing the population (density) of organic contaminants on graphene samples. AFM analysis revealed that graphene is more susceptible than the SiO₂ substrate to resist residues produced during fabrication of graphene devices, where the thickness of graphene was increased from 0.6 nm to ~1.5 nm and a root-mean-square surface roughness of 0.54 nm and 0.17 nm were reported for graphene and SiO₂ layer, respectively [173]. Resist residues on graphene and trapped on rugged surface of the underlying SiO₂ layer can contribute to charge trapping, and so carrier injection during capacitive gating in graphene devices. This have been demonstrated to lead to hysteresis in $I_{DS} - V_{BG}$ plot of graphene devices [59], [60]. In fact, we observed similar possible impact of the charge trapping/carrier injection issue in side-gate modulation of the I_{DS} in our DQD devices. Figure 6.9 shows the side-gate modulation (via G_1 gate, see Figure 6.2(c)) of differential conductance as a function of V_{DS} with $V_{BG} = 16.5$ V in the device *A*, exhibiting no sign of Coulomb diamonds. Similar behaviour was observed in the device *B*.

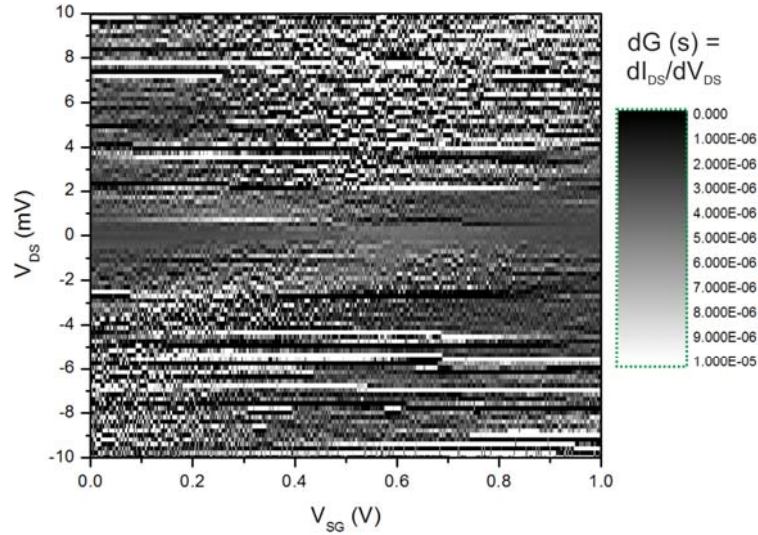


Figure 6.9 – Cryogenic temperature electrical measurements of the device *A* at $T \sim 6$ K and at chamber pressure of $\sim 10^{-4}$ Pa. Side-gate modulation of the I_{DS} with $V_{BG} = 16.5$ V, where no sign of Coulomb diamonds can be observed. Note that V_{SG} is the applied voltage to the G_1 side-gate (see Figure 6.2(c)).

Our hypothesis is that possible coverage of organic contaminants (i.e. trapped charges) on all surfaces of graphene flakes (i.e. the interface between the etched patterned in graphene such as side-gates and the QDs) as well as on the SiO_2 surface hindered the effectiveness of capacitive gating between the QDs and in-plane graphene side-gates. In fact, we noticed a likely hint of this hypothesis during our preliminary measurement of side-gate modulation (via G_1 gate, see Figure 6.2(c)) of I_{DS} . That is, for both devices, after each measurement $I_{DS} - V_{SG}$ plots (not shown here) exhibited different position of conductance peaks as well as different number of conductance peaks, suggesting a plausible contribution of trapped charges in the capacitive gating interface.

IV) Another possible contributing factor in the electrical behaviour of our DQD devices could be attributed to the polycrystalline structure of CVD graphene samples. Recent transmission electron microscopy (TEM) studies have shown that CVD graphene films exhibit polycrystalline structure [208], [209]. In fact, the grain boundaries can be also observed by optical microscopy [210]. CVD graphene consists of a number of different grains and orientations of graphene that are all joined together in a homogenous layer. Figure 6.10 shows HIM SE image of an area of a CVD graphene sample that we purchased from itrix Co., where the pink arrows in the figure point to some of the grain boundaries. In addition, as it can be seen in the figure, the grains have different shapes and can vary in size considerably, ranging from less than $1\text{ }\mu\text{m}$ (highlighted by the purple dashed-squares in Figure 6.10) to several μm in width.

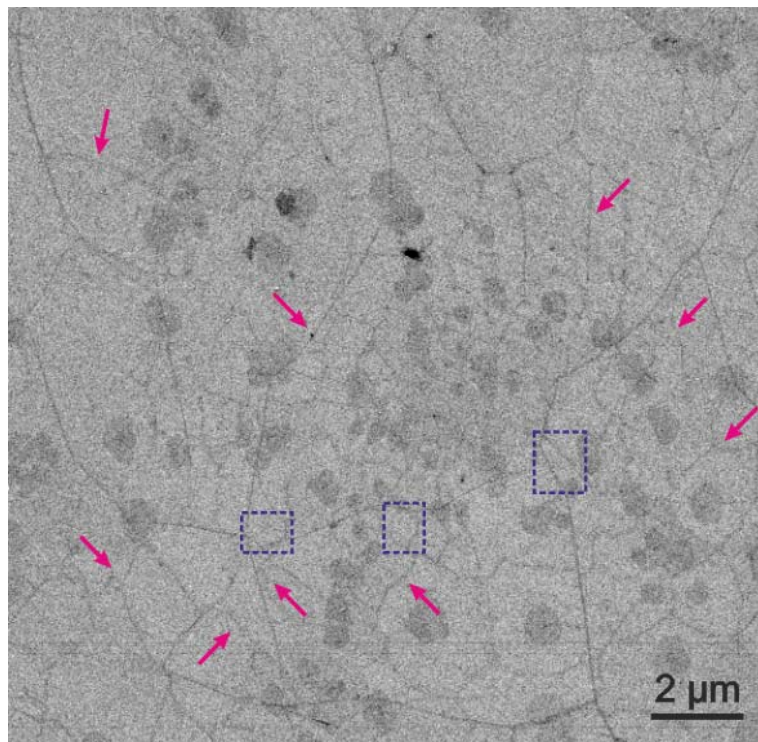


Figure 6.10 – HIM SE image of grain boundaries in a CVD graphene sample purchased from itrix Co. The pink arrows point to some of the grain boundaries in the flake. The purple dashed-squares highlight grains with a width smaller than 1 μm .

Grain boundaries in CVD graphene are considered as defect sites [73], [211]. Raman mapping on CVD graphene samples revealed that the intensity of D peak across grain boundaries increases significantly compare to within graphene grains [52]. The high intensity of D peak suggests a significant intervalley scattering mechanism at the grain boundaries. In addition, electrical transport measurements performed on CVD graphene samples revealed a substantial increase in resistance at grain boundaries, reflecting the effect of grain boundaries to impede electrical transport in CVD graphene samples [52]. Furthermore, in conjunction to the high intensity of the D peak, low temperature (at 4.3 K) magnetoresistance measurements across grain boundaries showed a prominent peak at $B = 0$ T which was associated with weak localisation [52]. The fact that weak localisation was not observed (or was negligible) in single-crystal grains of CVD graphene suggested that grain boundaries are major sources of intervalley scattering. That is, due to chiral nature of carriers in graphene, presence of sharp

lattice defects (which cause intervalley scattering with large momentum transfer) are required to observe weak localisation [52]. It is also worth mentioning that ripples in CVD graphene flakes may also contribute to intervalley scattering [52].

Previously, Khalafalla *et al.* reported observation of inter-grain electrostatic coupling effects in single electron transport through nanocrystalline silicon channels [212]–[214]. The nanometre size grains (~5-40 nm) of crystalline silicon, separated by amorphous silicon or SiO₂ grain boundaries (i.e. tunnel barriers), resulted in electron confinement (and so single electron charging energies), formation of a system of QDs and current paths within the devices. Consequently, the authors investigated complex arrangements of conductance lines and irregular stability region shapes in the stability diagram of the fabricated devices, suggesting a complicated capacitance network and/or change in coupling capacitance between Si grains by varying gate voltages [212]–[214].

In general, although organic contaminants and grain boundaries can potentially pose considerable effects in the electrical properties of our DQD devices but, since our measurement set-up did not satisfy the CB conditions (i.e. thermal energy), we cannot conclusively discuss the contribution of these two parameters based on the collected measurement results. Furthermore, we should highlight another fact regarding this study. That is, as we mentioned, unfortunately due to our limited access to low temperature measurement facilities, there was always a lengthy delay (several months) between the device fabrication and the cryogenic temperature electrical measurements. There are some scattered reports on degradation of the electrical properties of graphene devices in time. Notably, Rumyantsev *et al.* reported that aged (one month old) graphene FET devices can exhibit decrease of the carrier mobility and increase of the contact resistance [215]. Therefore, degradation of the electrical properties of the devices in time is a factor that cannot be ruled out, particularly for sensitive devices such as quantum dots.

6.2.2 QD devices fabricated in mechanically exfoliated graphene samples

We also conducted electrical measurements on one of our quantum dot devices fabricated in a monolayer graphene sample produced by mechanical exfoliation. The measurements were

conducted both at room temperature and cryogenic temperatures (~ 6 K) using same characterisation set-up that we used for the fabricated devices in CVD graphene samples.

Figure 6.11(a) shows an optical image of the mechanically exfoliated monolayer graphene flake we used to fabricate the GQD device. The graphene flake was identified by optical microscopy and Raman spectroscopy. Using our AutoCAD method (see section 5.6.1), the shape (size) and location of the produced graphene flake was imported faithfully to L-edit software (see Figure 6.11(b)). The fabricated device consists of two 60 nm-wide constrictions which connect a QD with diameter of 90 nm to the source (S) and drain (D) terminals. Furthermore, G_1 side-gate controls the electrochemical potential of the QD and G_2 and G_3 side-gates are to tune electron tunnelling via the source and drain channels, respectively (see Figure 6.11(b)). Note that the side-gates (G_1 , G_2 and G_3) are fabricated ~ 50 nm away from their corresponding features. HIM SE image of a similar device design, but with different dimensions, is shown in Figure 5.7(c).

Figure 6.11(c) shows the linear (ohmic) behaviour of bias current I_{DS} as a function of the applied bias current V_{DS} at room temperature. Figure 6.11(d) shows the ambipolar behaviour of I_{DS} as a function of back gate voltage V_{BG} with $V_{DS} = 1$ mV at room temperature. Once again, the shift in the position of the Dirac point ($V_{BG} \sim 18$ V) is due to organic contaminants that resulted in hole doping in the flake as well as the (resistance) oscillations in $I_{DS} - V_{BG}$ plot. Furthermore, we measured no current leakage via channel, between side-gate or via back gate, and so the GQD device was fabricated successfully.

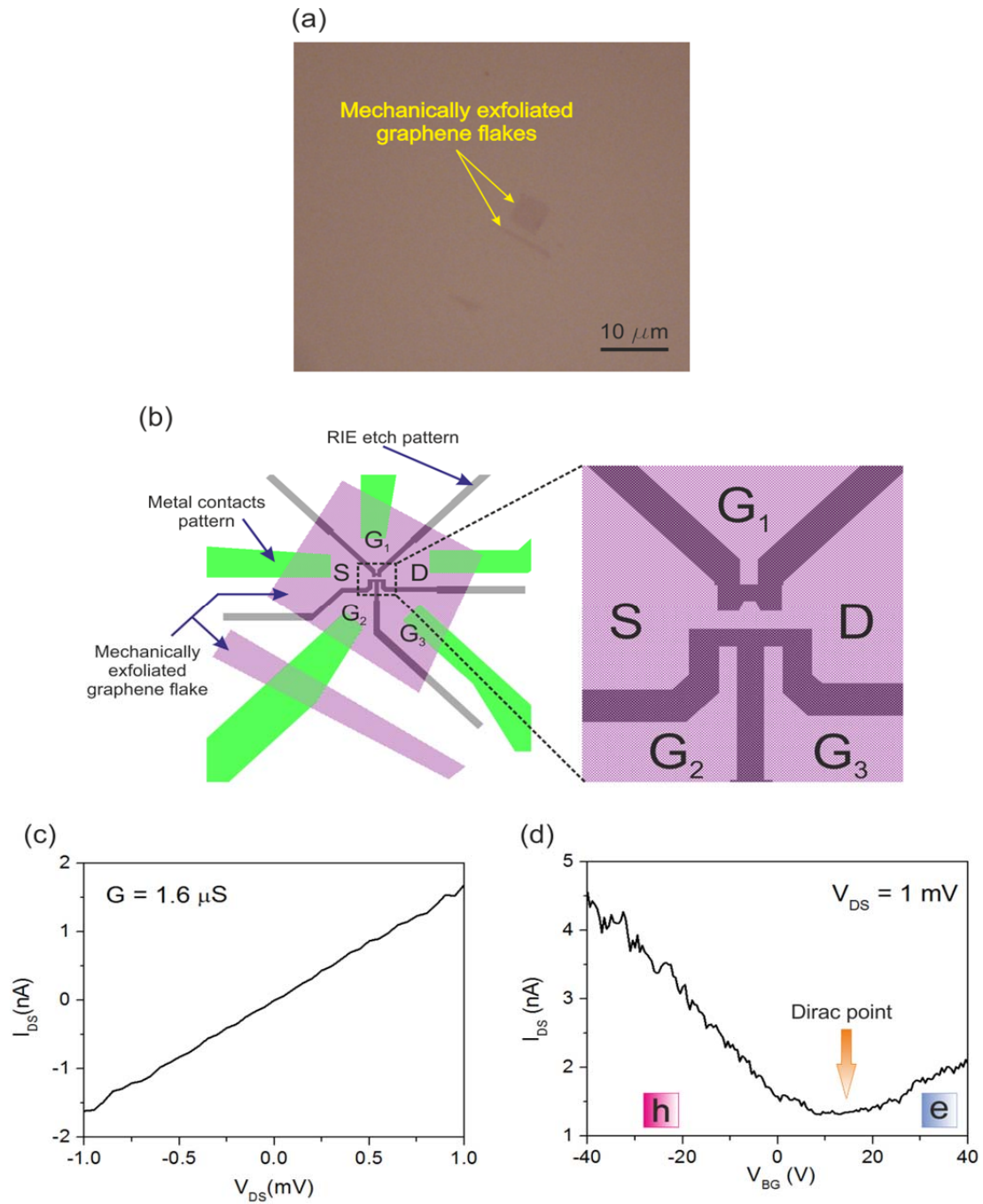


Figure 6.11 – (a) Optical microscopy image of the produced monolayer graphene flake by mechanical exfoliation. (b) L-edit device design of a graphene QD where the position and size of the flake were obtained faithfully by our AutoCAD method. The pink region is the graphene area. The green-colour (grey-colour) features show the metal contacts design (RIE etch pattern) in the graphene flake. (c) The measured $I_{DS} - V_{DS}$ plot (ohmic behaviour) of the GQD device at room temperature. (d) The ambipolar behaviour of I_{DS} as a function of V_{BG} with $V_{DS} = 1$ mV at room temperature. Note that all the other gates are grounded.

Back gate modulation of the bias current with $V_{DS} = 1$ mV at ~ 6 K and at vacuum pressure of 10^{-4} Pa is shown in Figure 6.12(a). A transport gap region of $\Delta V_{BG} \sim 16$ V can be roughly estimated in the figure. Figure 6.12(b) offers a close look inside the transport gap region which reveals that the conductance was never suppressed in the estimated transport gap region, and was still relatively high to study single electron tunnelling in the device. Furthermore, conductance resonances look smeared and no resonance peak could be distinguished in the transport gap region. These observations can be attributed to the thermal energy and the applied V_{DS} value.

The value of applied V_{DS} can be a contributing factor in observation of a not fully suppressed I_{DS} in the transport gap region at ~ 6 K. That is, usually a low bias voltage is applied to observe a well-defined transport gap region, i.e. $V_{DS} \ll 4k_B T$ [81], [106], [112], [113]. As V_{DS} increases, the drain (source) energy level approaches the conduction (valence) band edge and falls into the bias window, and so electrons (holes) are injected from drain (source) and I_{DS} rises [112], [216]. This in turn results in smearing of the transport gap region in $I_{DS} - V_{BG}$ plot, and not well-defined conductance resonances. However, one may suggest that these observations contradict with our electrical measurements on the device *A*, which was also consist of 60-nm wide constrictions but exhibited a more defined transport gap region with $V_{DS} = 1$ mV. This can be simply attributed to the higher carrier mobility (and so with less defective sites) in single-crystalline graphene flakes produced by mechanical exfoliation than that of for poly-crystalline CVD graphene which exhibit grain boundaries and usually a noticeable *D* peak in their Raman spectrum.

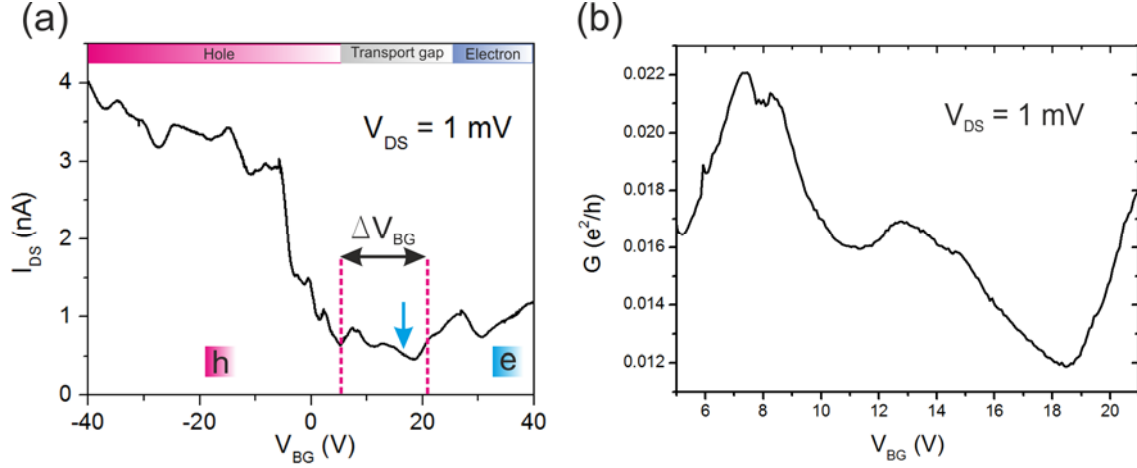


Figure 6.12 – Cryogenic temperature measurements at ~ 6 K and vacuum pressure of 10^{-4} Pa. (a) Back gate modulation of I_{DS} with $V_{DS} = 1$ mV, resulting in a not well-defined transport gap region with an estimated $\Delta V_{BG} \sim 16$ V. The blue arrow points to $V_{BG} = 18$ V which we used for further measurements on the device. (b) Conductance inside the transport gap region where the conductance resonances look smeared since the thermal energy and V_{DS} parameters were not fully optimised.

Figure 6.13(a) shows the $V_{DS} - V_{BG} - \log(G/S^{-1})$ contrast plot with faint signatures of Coulomb diamonds. It is noticeable that conductance level varies (located by the blue arrows in Figure 6.13(a)), suggesting that the plot consists of number of diamonds (blockade regions). This observation and the fact that Coulomb diamonds are not well-defined can be attributed to the thermal energy and the charging energy of the QD, i.e. $E_C \gg k_B T$. That is, the charging energy of a 90 nm dots size can be estimated as $E_C \approx 20.09$ (calculated based on Eq. (6.1)) which is not much greater than the thermal energy ($= 0.51$ meV) at 6 K to fulfil the Coulomb blockade condition.

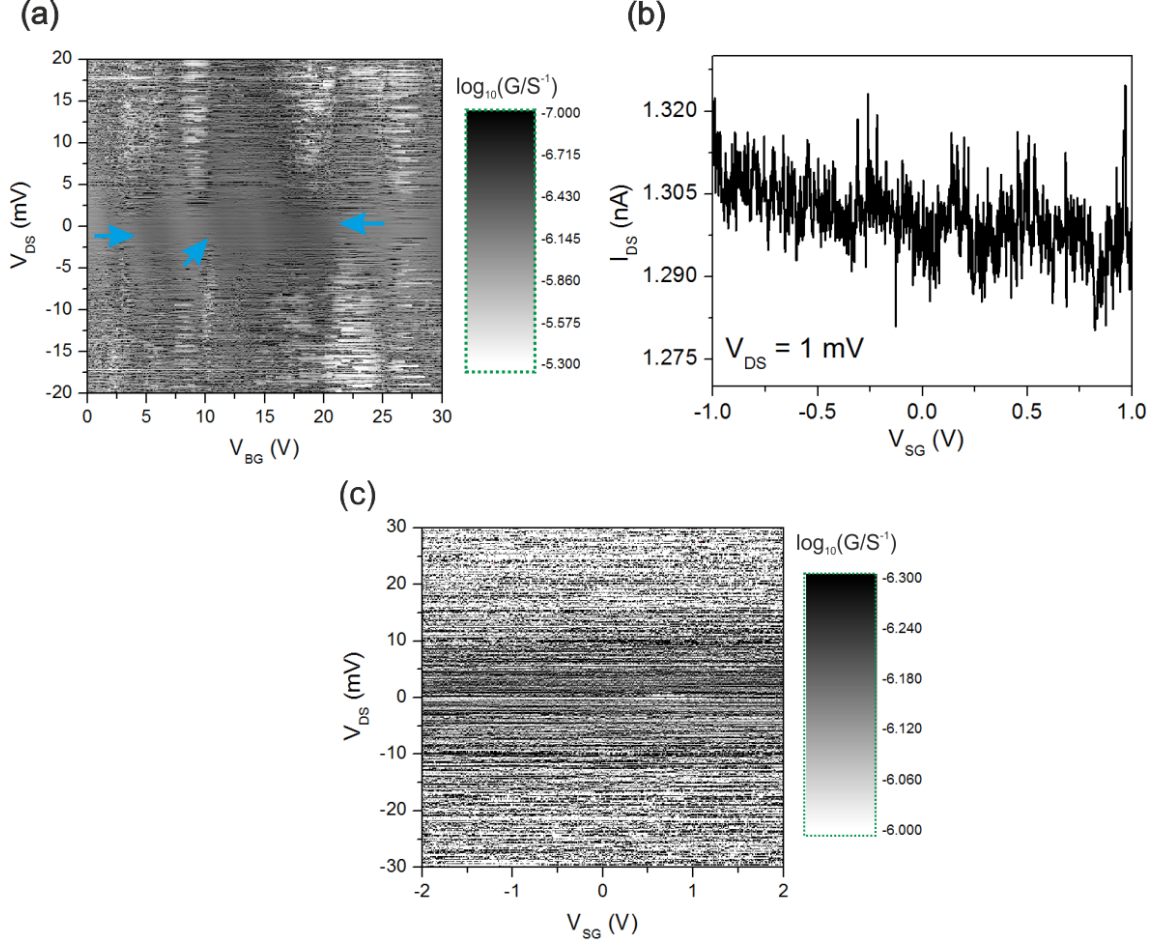


Figure 6.13 – Cryogenic temperature measurements at ~ 6 K and vacuum pressure of 10^{-4} Pa. (a) $V_{DS} - V_{BG} - \log(dG)$ contrast plot, exhibiting faint signature of Coulomb diamonds since the CB requirement, i.e. $E_C \gg k_B T$, is not satisfied. (b) Side gate (G_1 gate in Figure 6.11(b)) modulation of the bias current I_{DS} with $V_{DS} = 1$ mV and $V_{BG} = 18$ V. (c) $V_{DS} - V_{BG} - \log(G/S^{-1})$ contrast plot with $V_{BG} = 18$ V, showing no sign of Coulomb diamonds.

Interestingly, for side-gate modulation of the bias current we observed similar behaviour to that of observed for our DQD devices. For our GQD device, we used the G_1 gate (see Figure 6.11(b)) as the side-gate with $V_{DS} = 1$ mV and $V_{BG} = 18$ V (pointed by the blue arrow in Figure 6.13(b)). Figure 6.13(b) shows no sign of current modulation as a function of the applied side-gate voltage V_{SG} . Consequently, no Coulomb diamonds can be observed in the direction of the V_{DS} axis in the $V_{DS} - V_{BG} - \log(G/S^{-1})$ contrast plot (Figure 6.13(c)). The fact that similar behaviour was observed in all the three measured devices which were fabricated in

two different types of graphene samples (i.e. CVD graphene and exfoliated graphene) with two different device designs (i.e. QD and DQD) makes our hypothesis on the contribution of organic contaminants in side-gate modulation of I_{DS} more plausible. However, one cannot ignore the fact that due to the thermal energy we could only observe weak CB effect in our devices. This was evident in the $I_{DS} - V_{DS}$ plot of all the three devices at ~ 6 K. As a result, it was difficult to expect to observe well-defined CB features, such as Coulomb diamonds and side-gate modulation, in carrier transport characteristics of our devices. Therefore, further electrical measurements at lower cryogenic temperatures are required before discussing the extent of contribution of the organic contaminants and the grain boundaries (in the case of the CVD graphene) in electrical characteristics of our devices.

In order to investigate the side-gate modulation of I_{DS} issue in our devices further, we tried to study the effect of dielectric material. To this end, we deposited ~ 4 nm-thick layer of Al_2O_3 by atomic layer deposition (ALD) directly onto several of our devices. However, due to hydrophobic nature (chemically inert) of graphene surface, this only led to selective growth of Al_2O_3 grains on our graphene samples [217], [218]. Consequently, after the deposition, we observed inconsistent electrical characteristics among the devices. However, we confirmed that the ALD process resulted in degradation of electrical properties of all the devices. In fact, this is in agreement with previous results which reported severe degradation in mobility of graphene samples after deposition of dielectric materials [217]. Furthermore, we did not observe any improvement in the side-gate modulation of I_{DS} after the ALD process, which can be attributed to the uniformity of the Al_2O_3 growth on the graphene sample. For an extended discussion regarding these experiments please see Appendix C.

It is worth mentioning that surface functionalization of graphene has been demonstrated to result in uniform ALD growth [217]. Surface functionalization provides intentional nucleation sites/functionalization layer on graphene surface to initiate ALD growth. Two common methods to achieve this are, (i) *perylene tetracarboxylic* acid coating of graphene [218] and (ii) metal deposition of ~ 1 -2 nm-thick layer of Al followed by natural oxidation in air (i.e. Al_2O_3) as seed layer for ALD growth [219].

To overcome the limitations of our low temperature measurement set-up and to determine the feasibility of our DQD device design for single electron tunnelling behaviour (i.e. Coulomb

blockade), we conducted a simulation study by means of COMSOL Multiphysics and Monte Carlo single electron circuit simulations (SETSPICE).

6.3 Design and dynamic simulation of the fabricated GDQD devices by the EBL/RIE process

In this section, we discuss the electrical behaviour of our DQD devices (the devices A and B) based on the classical capacitance model (see section 3.2.3). This simulation work is conducted by combining COMSOL Multiphysics and SETSPICE Monte Carlo single electron circuit simulations to study the $I - V$ plots as well as the stability diagram of our GDQD devices. It is worth mentioning that SETSPICE (also known as CAMSET) is a Monte Carlo single electron circuit simulator that was developed by Hitachi Cambridge Laboratory [220].

Here, the L-edit design of a fabricated DQD device was input into COMSOL's finite element method-based capacitance simulator in which the capacitance(s) between each component in the device was extracted. These capacitance values were then fed into SETSPICE single electron circuit simulator to calculate the $I - V$ characteristics of the device and discuss its electrical behaviour at cryogenic temperatures, i.e. 1.4 K.

6.3.1 Device design and capacitance simulation methodology

We needed to extract the capacitances between each component in the fabricated DQD device to investigate its electrical behaviour based on the classical capacitance model. To this end, by importing the L-edit design of the measured device (see Figure 6.2(c)) into COMSOL's electrostatics application mode, a 3D structural schematic of our DQD system was designed. The 3D structural schematic of our DQD device simulated by COMSOL is shown in Figure 6.14. Note that only features in close proximity to our DQD are shown in Figure 6.14. This simulation is developed to extract the capacitance values between in-plane graphene features. Therefore, the effects of metal contacts onto the graphene devices as well as the metallic bond-pads (see Figure 6.2(b)) were not taken into account as their contribution would be

approximately the same among all the device components, and so result in negligible discrepancies between these components.

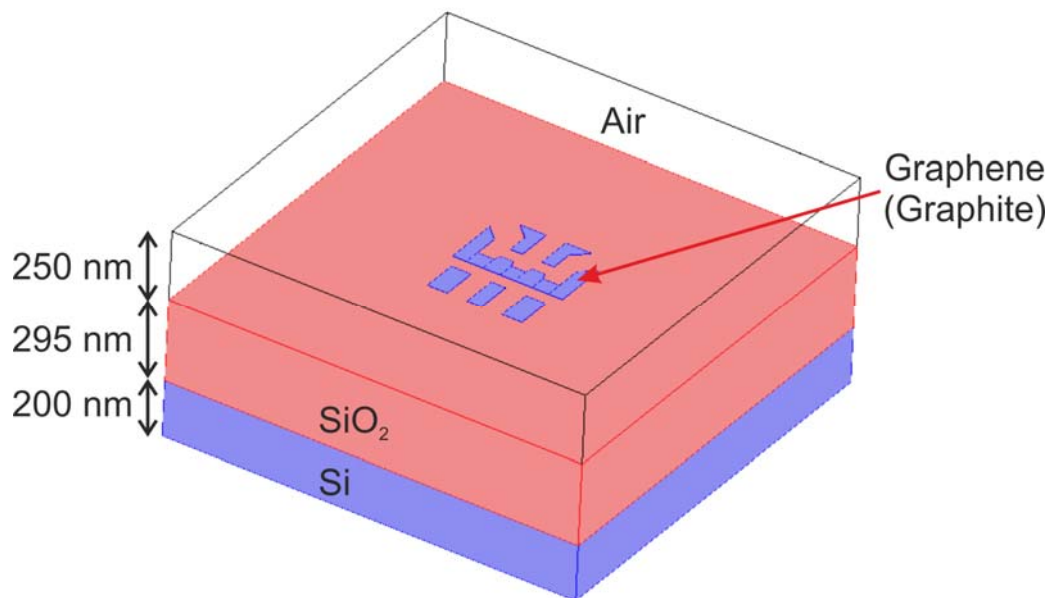


Figure 6.14 – Schematic 3D model of our graphene DQD device design using COMSOL Multiphysics.

The graphene layer is treated as a homogeneous graphite film with thickness of 1 nm, in agreement with previous COMSOL simulation for graphene devices [221]. The graphene layer is placed on top of a SiO₂/Si layer with 295 nm/200 nm thicknesses, respectively. Furthermore, since our device did not have a top gate, air (vacuum) is the dielectric between our in-plane features. Therefore, we assumed a 250 nm-thick layer of air on top of the graphene components.

To calculate the capacitance between any two components, we applied 1 V to one component whilst the other component was grounded. For instance, to obtain the capacitance value between in-plane gates G_1 and G_2 (see Figure 6.2(c)), we applied 1 V to all boundary surfaces in COMSOL which defined G_1 and grounded all the boundary surfaces which defined G_2 . After solving Maxwell's equations (performing “Mesh” on the created 3D DQD system), COMSOL

performs integration over all boundary surfaces of G_2 to calculate the induced charge on the surface of G_2 . Figure 6.15 shows the electrical potential distribution of our DQD system when 1 V was applied to G_1 with G_2 grounded. Finally, via $Q = CV$ with $V = 1$ V, COMSOL obtains the capacitance between in-plane gates G_1 and G_2 . We employed similar procedure to calculate all the inter-part capacitances of our DQD system. Note that all other boundary surfaces of the graphene features were set to have continuity boundary conditions during this calculation. However, the outermost boundaries which defined the DQD system (i.e. air, SiO₂, Si layers) were grounded.

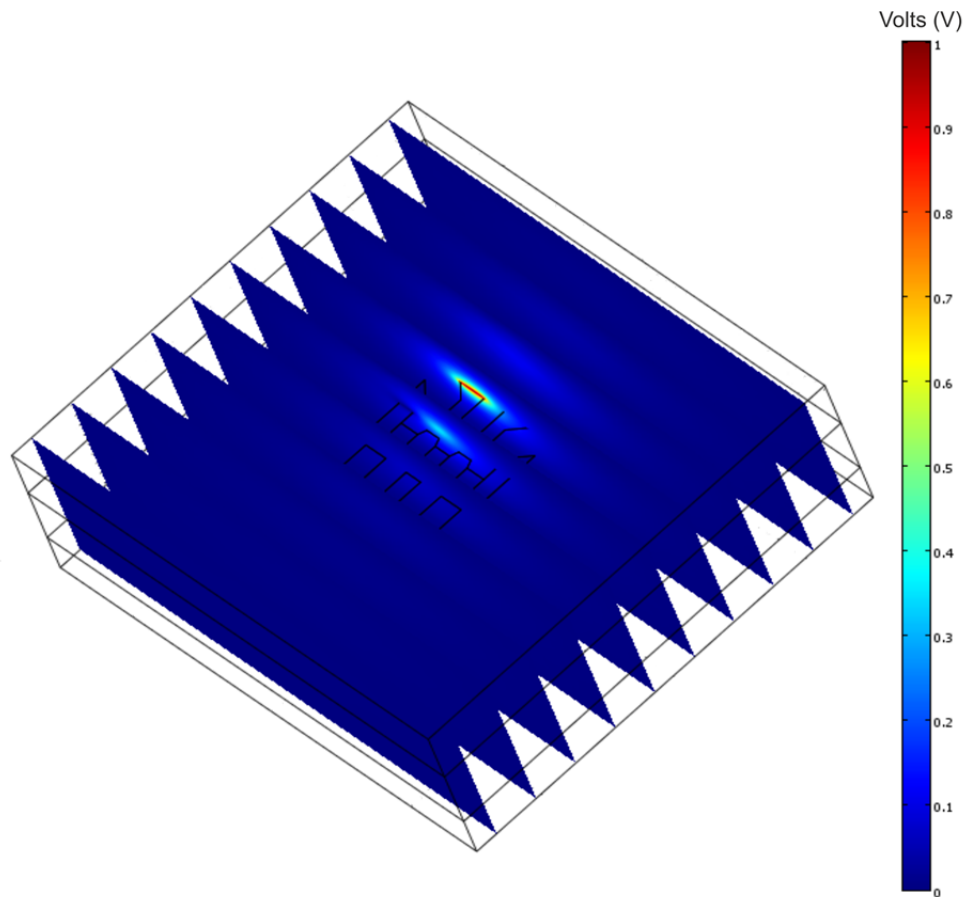


Figure 6.15 – COMSOL Multiphysics simulations. Cross-sectional plots of the electrical potential distribution in our DQD system solved using Maxwell's equations after applying 1 V to G_1 with G_2 grounded.

Table 6.1 summarises all the extracted inter-part capacitances of our DQD device which was shown in Figure 6.2(c).

TABLE 6.1

Table of the extracted inter-part capacitances of our DQD device obtained using COMSOL Multiphysics.

Label	Capacitance/aF
$C_{G1-S} = C_{G2-D}$	9.18
C_{G1-G2}	9.24
$C_{G1-QD1} = C_{G2-QD2}$	9.11
$C_{G1-QD2} = C_{G2-QD1}$	8.98
$C_{GS-S} = C_{GD-D}$	10.15
$C_{GS-GM} = C_{GM-GD}$	10.24
$C_{GS-QD1} = C_{GD-QD2}$	10.09
$C_{GM-QD1} = C_{GM-QD2}$	8.69
$C_{BG-QD1} = C_{BG-QD2}$	7.5

An equivalent circuit diagram of our DQD device based on the classical capacitance model is shown in Figure 6.16. Also note that the coupling capacitances between the graphene components and the back gate are not shown in Figure 6.16 to avoid cluttering the key aspects of the circuit schematic.

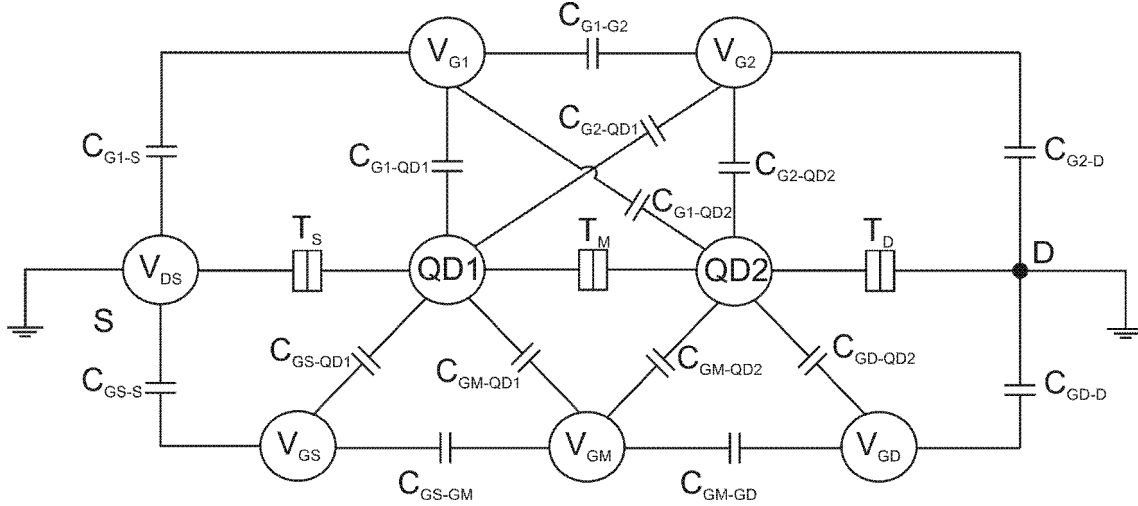


Figure 6.16 – Equivalent circuit diagram of our GDQD device shown in Figure 6.2(c) and the respective capacitance values are presented in Table 6.1.

6.3.2 Equivalent circuit and device simulation methodology

We used Mote Carlo single electron simulator SETSPICE for dynamic circuit simulations [220]. The capacitance values obtained from COMSOL simulations were used to implement the equivalent circuit diagram into SETSPICE simulator. However, since COMSOL cannot simulate tunnel barriers (i.e. T_S , T_M and T_D in Figure 6.16), we assumed symmetric tunnel barriers with capacitance and resistance of 500 k Ω and 5 aF, respectively. Also, we assumed that the device is operating at cryogenic temperature of 1.4 K.

The $I_{DS} - V_{DS}$ plot of our GDQD device calculated as a function of temperature is shown in Figure 6.17.

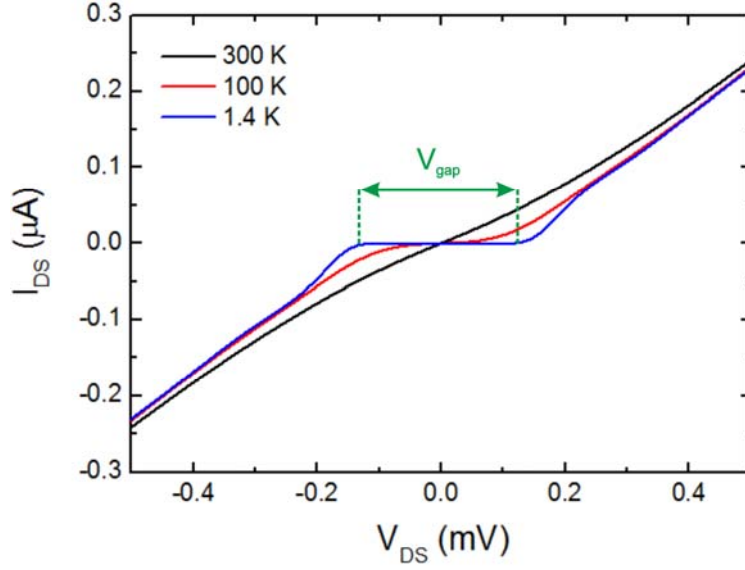


Figure 6.17 – The $I_{DS} - V_{DS}$ plot of our GDQD device as a function of temperature. The region of suppressed current (CB region) due to Coulomb blockade becomes more evident with decreasing the temperature.

At room temperature (i.e. 300 K), the $I_{DS} - V_{DS}$ plot exhibits an ohmic behaviour. However, a region of suppressed current (i.e. CB region) forms with decreasing the temperature in agreement with Coulomb blockade condition $k_B T \ll E_c$. For small bias voltages, there is no current and the tunnelling rate is exponentially low. Eventually, at 1.4 K the thermal energy is much smaller than the charging energy of the dots and the Coulomb blockade region (i.e. V_{gap}) becomes very pronounced in our system. In this system the electron tunnelling through the potential barriers (i.e. T_S , T_M , T_D) via quantum dots only occurs when the condition $eV_{DS} > E_{add}(= eV_{gap})$ is satisfied.

The back gate modulation of I_{DS} as a function of V_{DS} , and so observation of Coulomb diamonds, is shown in Figure 6.18. However, here, the calculated plot looks drastically different to that of we measured for the fabricated devices (for examples, see Figure 6.6(a) and Figure 6.8(b)) where the collected $V_{DS} - V_{BG} - I_{DS}$ plots consisted of complex and dense Coulomb diamonds (with varying in size and shape) arrangements. These discrepancies can be attributed to existence of unintentional QDs along the etched patterns in graphene and grain boundaries in CVD graphene samples in the fabricated devices, which are not considered in

this simulation work. The unintentional QDs and grain boundaries resulted in additional electron confinement, and so single electron charging energies in the fabricated devices.

In this simulation, the two quantum dots are controlled by a same gate (i.e. back gate). Therefore, their respective level spacing cannot be tuned accurately and carrier transport remains blockaded as long as the bias window (i.e. eV_{DS}) equals the electrochemical mismatch between the dots. Furthermore, in addition to controlling the energy levels of the dots, the V_{BG} (back gate potential) also modifies the carrier concentration in the reservoirs, and so affecting the tunnelling rate as well as the coupling between the two dots and their respective leads (i.e. source and drain terminals).

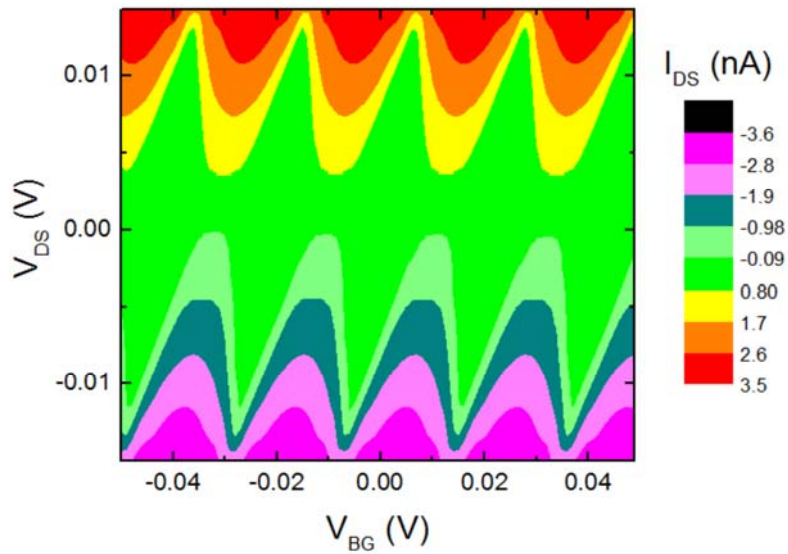


Figure 6.18 – Observation of Coulomb diamonds as a function of the back gate voltage in our DQD device at 1.4 K.

In a real DQD system though, the Coulomb diamonds shrink in size with increasing the V_{BG} until to a point that the system behaves as a single quantum dot, resulting in a single channel of continuous conductance.

From the geometry of the Coulomb diamonds we can estimate an $E_C \approx 13$ meV. Also, the back gate period (see section 3.2.2 for more information) is $\Delta V_g \sim 20$ meV, which is in agreement with the calculated $C_{BG} \approx 7.5$ aF (see section 6.2.1).

A close look at Figure 6.18 indicates a finite slope (i.e. “lever arm”) in the shape of the calculated Coulomb diamonds. The value of this lever arm can be calculated as,

$$\alpha_{bg} = C_{BG}/C_{\Sigma}, \quad (6.2)$$

which in our case is $\alpha_{bg} \sim 0.43$.

By controlling the electrochemical potential of each dot individually using side-gates, we can tune carrier transport in a DQD device more accurately and obtain the stability diagram of the system as a function of the applied side-gate voltages. The calculated stability diagram, and so observation of honeycomb diagram, for our DQD device with $V_{DS} = 500$ μ V is shown in Figure 6.19.

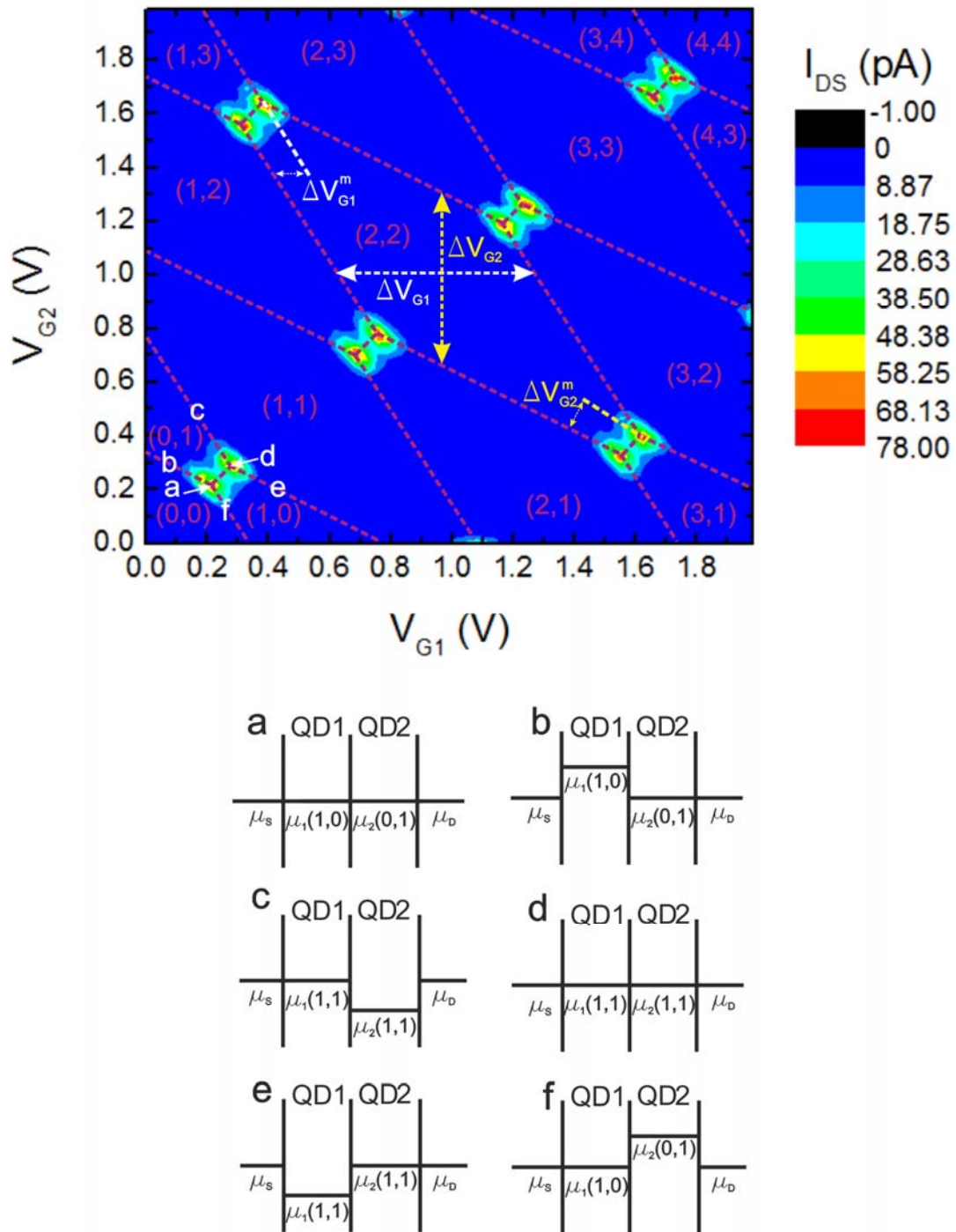


Figure 6.19 – The stability diagram of our DQD device with $V_{DS} = 500$ μ V at 1.4 K. The diagrams on the bottom show the electrochemical potential of the dots on the corresponding positions in the honeycomb diagram.

Since the stability diagram exhibits a honeycomb pattern, we confirm that our DQD system is in intermediate interdot coupling regime. The shiny circle-shape features in the stability diagram are the triple points where a complete single carrier tunnelling from source to drain via both dots occurs. The sequential tunnelling events are only allowed at the triple points where μ_{QD1} , μ_{QD2} , μ_S and μ_D are aligned. The pink dashed-lines show the boundaries of each honeycomb cell where the number of electrons in each dot is presented as (n,m). At the dashed line connecting two triple points, the charge states are degenerated. Furthermore, the inset in Figure 6.19 shows the change in the electrochemical potential of each QD at the corresponding positions in the stability diagram. Based on the equations explained in section 3.2.3, the geometry of each honeycomb cell can be calculated. From the stability diagram we can also estimate $\Delta V_{G1} = \Delta V_{G2} \approx 700$ mV and $\Delta V_{G1}^m = \Delta V_{G2}^m \approx 100$ mV.

By increasing the bias voltage, the triple points grow in size and become triangle-shape, i.e. bias triangles. Figure 6.20(a) shows the stability diagram of our DQD device with $V_{DS} = 2$ mV at 1.4 K.

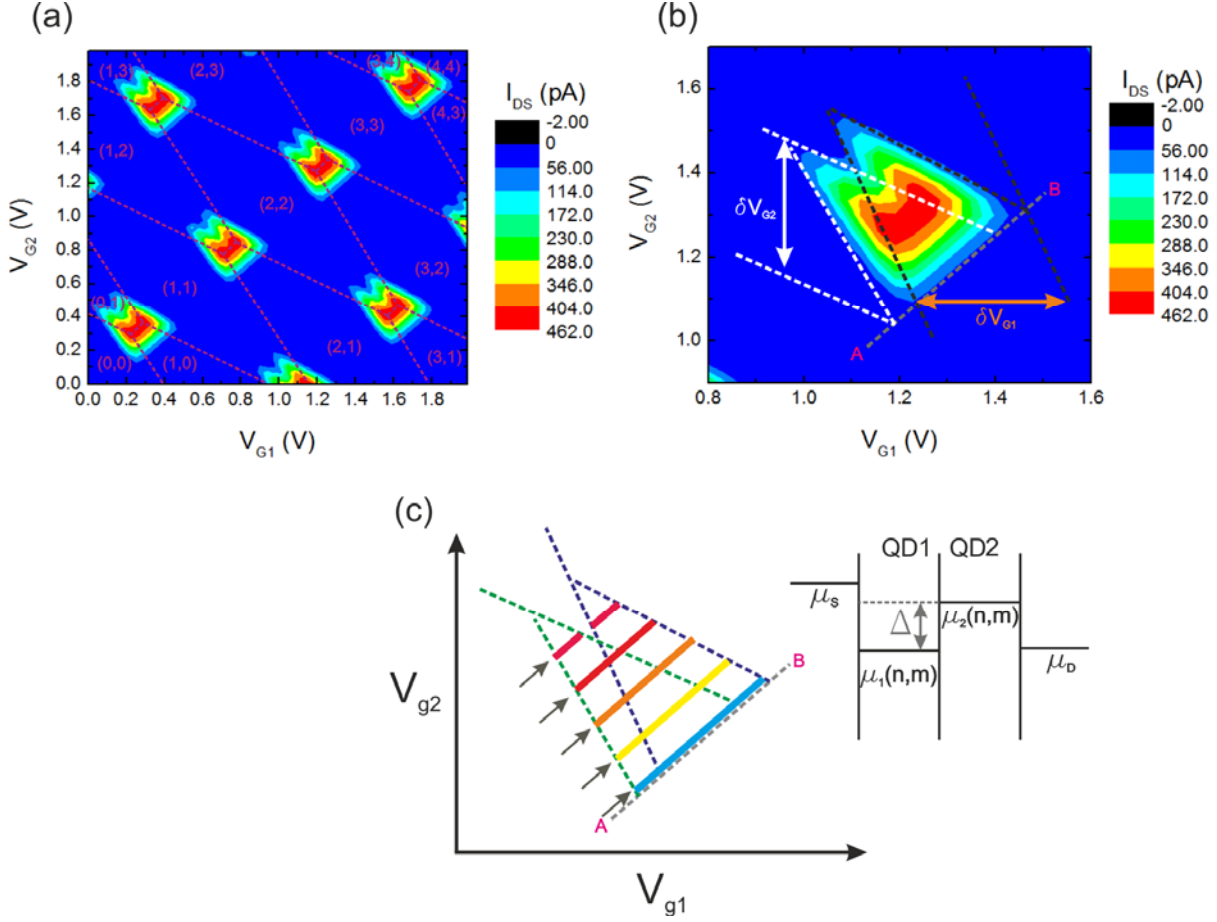


Figure 6.20 – (a) The stability diagram of our DQD device with $V_{DS} = 2$ mV at 1.4 K. (b) The geometry of a pair of bias triangles from the stability diagram in Figure 6.20(a). (c) A schematic diagram of quantized energy states inside a bias triangle. The inset shows the ground states of the DQD system with the possible first excited state of the left dot. The current value increases from the bottom edge towards the apex of the triangles.

The geometry of a pair of bias triangles is shown in Figure 6.20(b) which can be estimated as, $\delta V_{G1} = \delta V_{G2} \approx 300$ mV. As mentioned in section 3.2.3, the bias triangles grow in size with increasing the bias voltage. But, for a sufficiently large V_{DS} , a number of discrete energy levels can appear between the ground states of the dots, known as excited states, which can also contribute to the conductance (e.g. see Figure 3.9). However, observation of these quantized states is beyond capability of the SETSPICE simulator.

Figure 6.20(c) shows a schematic diagram of possible quantized current states in a pair of bias triangles. The current value increases from the bottom edge (blue colour line in Figure 6.20(c))

towards the apex of the triangles (red colour line in Figure 6.20(c)). The level spacing between the quantized states (i.e. single particle level spacing) in a disk-like monolayer graphene QDs can be calculated by,

$$\Delta(N) = \hbar v_F / (d\sqrt{N}), \quad (6.3)$$

where N is the number of charge carriers in the dot ($N \gg 1$), $v_F \approx 10^6$ m/s is the Fermi velocity and d is the diameter of the dot [140], [141]. This is in contrast to other two-dimensional (e.g. bilayer graphene) and three-dimensional systems where the single-particle level spacing is independent of the charge carrier number N [141]. That is, as we mentioned in section 2.2, graphene exhibits a linear density of states around the energy of the K point which can be calculated by [115], [140],

$$\mathcal{D}(E) = 2E / \pi^2 \hbar^2 v_F. \quad (6.4)$$

Consequently, the single particle level spacing in a monolayer graphene flake is dependent on the value of N .

6.4 Conclusions

In this chapter, we discussed the electrical characterisations results on the graphene quantum dots devices fabricated by our EBL/RIE process at both room temperature and cryogenic temperatures (i.e. ~ 6 K). Two different types of devices were discussed in this chapter. These were graphene DQD devices fabricated on CVD grown graphene samples and a GQD device fabricated on a mechanically exfoliated graphene sample. Room temperature measurements were used to justify the successful development of our EBL/RIE process and to calculate the statistical yield of our process. Based on the room temperature electrical characterisations, we calculated a statistical fabrication yield of 80% (from 57 fabricated devices) for our DQD devices fabricated on graphene samples produced by mechanical exfoliated and a statistical fabrication yield of 58% (from 160 fabricated devices) for the devices fabricated on CVD graphene samples. These values represent the percentage of fabricated QDs devices which had

to exhibit ambipolar behaviour, no observable current leakage from the channel, no observable current leakage between in-plane graphene side-gates, and no observable back gate leakage through the SiO_2/Si substrate. The lower fabrication yield on the purchased CVD grown graphene samples was attributed to the quality and consistency of the flakes.

Cryogenic temperature measurements resulted in observation of complex and dense Coulomb diamonds arrangements in the collected $V_{DS} - V_{BG} - I_{DS}$ plots. We attributed this to formation of unintentional QDs along the etched patterns in graphene and grain boundaries in CVD graphene samples. The estimated E_g values from $V_{DS} - V_{BG} - I_{DS}$ plots showed good agreement with published results, indicating faithful transfer of the desired patterns into the graphene samples. However, due to temperature limit of our low temperature measurement set-up which did not satisfy the condition $E_C \ll k_B T$, we did not manage to observe pronounced Coulomb blockade effects. This in turn affected the resolution (clarity) of the obtained measurement results, e.g. Coulomb diamonds. We also reported on a plausible impact of the organic contaminants, which can reside on graphene samples during fabrication of the devices, on the effectiveness of the side-gate modulation of the bias current. Furthermore, to determine the feasibility of our DQD device design for single electron tunnelling behaviour (i.e. Coulomb blockade), we presented a simulation study by means of COMSOL Multiphysics and Monte Carlo single electron circuit simulations (SETSPICE) to discuss the electrical behaviour of these devices in more detail at 1.4 K. This resulted in successful calculation of the $I - V$ characteristics of the device including the corresponding stability diagram, observation of triple points and bias triangles. The simulation results confirmed that our devices are well designed and are capable of exhibiting single electron tunnelling characteristics for quantum information processing studies.

Chapter 7

Conclusions and future work

7.1 Conclusions

In this thesis, we studied graphene as an alternative host material for fabricating quantum dot devices. We discussed that due to (i) the absence of hyperfine interaction and (ii) extremely weak spin-orbit coupling, graphene is considered as an exotic material, if not ideal, for fabrication of quantum dots devices and spin qubit embodiment. We discussed initial attempts in studying behaviour of graphene quantum dots through a literature review which highlighted promising potential of graphene for quantum information processing. However, more detail investigations are required to fully exploit single electron tunnelling in graphene quantum dots. That is, currently, disorder-induced potential seems to pose a major challenge for future device applications in the field of quantum information processing and further improvement is required to suppress the influence of disorder on the tenability of the device.

We successfully developed and established two methods for fabricating graphene nano devices such as intricate QD devices.

We argued that there are several parameters (e.g. proximity effect, resist undercut during etching, uneven thickness of the resist layer) that can hinder the resolution of the fabricated graphene devices by EBL/RIE method. Therefore, we proposed our novel hybrid fabrication

process for extremely downscaled graphene quantum dots by combining conventional e-beam lithography and direct milling with the sub-nm focused helium ion beam generated by a helium ion microscope. The helium ion milling is used to pattern graphene flakes with intricate QD devices, with sub-10 nm resolution and high fidelity. We established this novel fabrication approach for the first time. We found that the unintentional production of hydrocarbon contamination on the surface of graphene flakes after e-beam lithography can hinder HIM milling. However, by annealing the samples in a H_2/N_2 gas flow, it is possible to reduce this contamination sufficiently to achieve the desired milling results. The electrical characterization of the final device demonstrates the successful fabrication of the first electrically characterized He-ion beam patterned graphene device. Unfortunately though, due to water vapour contamination in our cleanroom's gas lines, we were not able to investigate the electrical characteristics of these devices in detail. However, through a recent study, we confirmed that our fabrication process was well thought out and well-established. The highly controllable, fine scale fabrication capabilities (<10 nm) offered by this approach could lead to a more detailed understanding of the electrical characteristics of graphene nano devices and could ultimately pave the way towards room-temperature operable graphene quantum dot devices.

We also demonstrated the successful development of our EBL/RIE fabrication process for the first time at the Southampton Nanofabrication Centre. All the process steps involved in the fabrication of such devices were discussed extensively. To minimise e-beam induced damage on our graphene samples during e-beam lithography, we employ a single layer of *Methyl Methacrylate* (MMA) resist for the first time as a radical method for fabrication of metal contacts onto graphene devices. The high electron beam sensitivity of MMA resist allows the use of a dramatically lower e-beam dose to that of required for a bilayer resist layer (and so less beam induced damage onto the graphene samples) which, using our optimised process, also ensures consistent and successful lift-off outcome with minimum feature size of ~ 150 nm. This was achieved by simultaneous tuning of the resist thickness (i.e. MMA), e-beam lithography process, metal deposition conditions (i.e. metal deposition at a rate of $0.5 \text{ \AA}/\text{second}$), thickness of the deposited metal layer (i.e. Ti/Au 5 nm/ 60 nm), and performing the lift-off process in warm *N-Methyl-2-Pyrrolidone* (NMP). We also demonstrated that our fabricated devices by

this method exhibit better resolution than majority of previous studies. We achieved successful fabrication of QD devices on graphene samples produced by mechanical exfoliation and CVD grown graphene. To our best of knowledge, this is the first attempt at obtaining such high density and high resolution graphene quantum dots devices with high reproducibility in such large numbers on CVD grown graphene, which clearly indicates the versatility of our fabrication process.

We discussed the electrical characterisations of the fabricated quantum dots devices by our EBL/RIE process on CVD grown graphene and on mechanically exfoliated graphene samples at room temperature and cryogenic temperature. Room temperature measurements were used to justify the successful development of our EBL/RIE process and to calculate the statistical yield of our process. Based on the room temperature electrical characterisations, we calculated a statistical fabrication yield of 80% (from 57 fabricated devices) for our DQD devices fabricated on graphene samples produced by mechanical exfoliated and a statistical fabrication yield of 58% (from 160 fabricated devices) for the devices fabricated on CVD graphene samples. These values represent the percentage of fabricated QDs devices which had to exhibit ambipolar behaviour, no observable current leakage from the channel, no observable current leakage between in-plane graphene side-gates, and no observable back gate leakage through the SiO_2/Si substrate. The lower fabrication yield in CVD graphene samples was attributed to the quality and consistency of the flakes on the purchased samples. We also justified considerable improvement in reliability of our EBL/RIE process for fabrication of GQD devices, and so successful optimisation of the steps involved in the fabrication process, by comparing our process yield values with previous works by others.

Cryogenic temperature measurements resulted in observation of complex and dense Coulomb diamonds arrangements in the collected $V_{DS} - V_{BG} - I_{DS}$ plots. We attributed this to formation of unintentional QDs along the etched patterns in graphene and grain boundaries in CVD graphene samples. We estimated the energy gaps values from collected $V_{DS} - V_{BG} - I_{DS}$ plots which showed good agreement with published results, indicating faithful transfer of the desired patterns into the graphene samples. However, due to temperature limit of our low temperature measurement set-up which did not satisfy the condition $E_C \ll k_B T$, we did not manage to

observe pronounced Coulomb blockade effects. This in turn affected the resolution (clarity) of the obtained measurement results, e.g. Coulomb diamonds. We also reported the plausible impact of the organic contaminants, which can reside on graphene samples during fabrication of the devices, on the effectiveness of the side-gate modulation of the bias current. However, based on our present measurement results, the extent of the contribution of the organic contaminants cannot be accurately discussed at this stage. Furthermore, to determine the feasibility of our DQD device design for single electron tunnelling behaviour (i.e. Coulomb blockade), we presented a simulation study by means of COMSOL Multiphysics and Monte Carlo single electron circuit simulations (SETSPICE) to discuss the electrical behaviour of these devices in more detail at 1.4 K. This resulted in successful calculation of the $I - V$ characteristics of the device including the corresponding stability diagram, observation of triple points and bias triangles. The simulation results confirmed that our devices are well designed and are capable of exhibiting single electron tunnelling characteristics for quantum information processing studies.

7.2 Future works

The sole focus of this work was to fabricate graphene quantum dot devices. However, the two fabrication methods which we successfully developed and established can be used for fabricating variety of graphene nano devices. Here, based on our achievements, we discuss a few possible future directions.

7.2.1 EBL/RIE fabrication method

The cryogenic temperature measurements that we discussed in chapter 5 are very encouraging to continue investigating the single electron tunnelling in the devices at lower temperatures, using a cryostat. Particularly, given the fact that there are very few reported studies on graphene quantum dots, there are many exciting experiments that can be conducted to investigate the behaviour of these devices.

For future studies, to avoid possible undesirable effects of organic contaminants in electrical properties of fabricated graphene quantum dots devices, an annealing step should be carried out prior to cryogenic temperature measurements. This was also suggested in other works [106], [130], [131], [133], [140]. This can be achieved using a similar process to that of we developed for HIM milling.

Furthermore, an interesting study would be to replicate the original work by Fujisawa *et al.* on inelastic tunnelling in GaAs/AlGaAs double quantum dot devices for GDQD devices [104]. That is, when the electrochemical potentials of the dots are aligned, an electron can elastically tunnel through the DQD from source to drain. However, an electron can also inelastically tunnel through the dots by an emission or absorption of a phonon with the same energy as the potential difference between the two dots. The inelastic tunnelling rate (Γ_C) depends on the phonon spectral density $J(\omega)$ and the electrochemical potential difference (ΔE) of the dots, and is equal to:

$$\Gamma_C \propto \left(\frac{T_c}{\Delta E} \right)^2 J(\Delta E), \quad (7.1)$$

where T_c is the tunnel coupling between the dots. Based on this, one can investigate the electron-phonon interactions and their contribution in single electron tunnelling in GDQD devices. Indeed, this study can be extended further to investigate the decoherence (time) for charge qubits.

7.2.2 HIM milling fabrication method

The high resolution and accurate design replication capabilities of the HIM milling technique could pave a way towards more detailed studies of the behaviour of graphene nano devices (particularly GQDs and other graphene QIT devices), both at room and cryogenic temperatures. For instance, in the Figure 4.21(a), the accurate positioning of the side-gates relative to the channels and the DQD (~ 22 nm) should ensure precise control of the single electron tunnelling through the device. Moreover, as shown in Figure 4.24, it is possible to achieve even higher milling resolution on graphene flakes compared to that demonstrated for the device characterized in this report.

The effect of HIM milling on the roughness of graphene edges and the extent of atomic level defects induced in the unexposed regions as a result of He ions backscattering from the substrate are currently unknown and require further investigation. These factors are particularly important for nanoscale devices, where the edges form a significant proportion of the overall device material. Moreover, as mentioned in section 4.3.2, moving to suspended devices could reduce backscattered ion damage and improve pattern resolution, but at the expense of more complicated fabrication procedures.

Scanning transmission electron microscopy (STEM) analysis could be a very decent method to investigate the edge roughness and beam induced damage in He-ion beam patterned graphene devices. STEM has been demonstrated as a promising method to study patterned graphene samples with atomic resolution [143], [144]. Indeed, electrical characterisations are also required to fully investigate the quality of the final fabricated devices by this method.

Furthermore, for future attempts, we think it would be interesting to use chloroform treatment instead of heat treatment to remove the surface contaminants on processed graphene samples. That is, annealing graphene samples can bring them in closer contact with rugged surface of SiO₂ layer, and so degrading the electrical properties of graphene samples [173].

Apart from promising potential of HIM milling for fabricating graphene quantum dot devices, there are other device designs (applications) that could be very interesting to employ HIM milling. One very interesting possibility is to fabricate graphene interband tunnel transistors, also known as Tunnel Field-Effect-Transistors (TEFTs), with ultrathin GNR channel. Graphene is fast becoming a very popular substrate for TFETs for two reasons,

- i) To enhance the ON-state tunnelling current, narrower bandgap materials with smaller effective masses are more preferable [222]. One-dimensional TFETs exhibit superior gate control and reduction of transverse energy component in their tunnelling transport [223], [224].
- ii) Graphene nanoribbons (GNRs) have a width-tunable bandgap and monolayer-thin body, which is especially favourable for TFETs applications, and more amenable to planar processing and large-scale integration than CNTs.

To our best of knowledge, however, there are no reports on experimental results on the behaviour of GTFETs and so far all the studies are limited to theoretical and computational

studies. Therefore, the GTFETs research is still very young and there are a lot to be explored experimentally. This can be an interesting device design to employ HIM milling to fabricate the narrow GNR channel.

Appendix A

Fabrication process flow sheet of graphene nano device by EBL/RIE method

TABLE A.1

A process flow sheet. Fabrication of graphene nano devices by the EBL/RIE method.

Process	Description of process steps	
Substrate preparation	1) S1813 photo-resist coating	a) Spin-coating at 1000 rpm (~2 μm -thick resist layer) b) Hard bake at 120 $^{\circ}\text{C}$ for 15 minutes
	2) SiO_2 etch using RIE	a) Ar/CHF_3 (38/12 sccm) gas flow b) RF power = 200 W c) Vacuum pressure = 30 mTorr d) Etch duration = 14 minutes
	3) S1813 photo-resist strip	a) Fuming nitric acid (FNA) soak for 5 minutes followed by DI water rinse for 5 minutes b) N_2 blow dry
	4) Ashing oxygen plasma	a) 600 ml/min O_2 gas flow b) RF power = 800 W c) Chamber pressure = 0.15 Torr d) Ashing duration = 10 minutes
Sample fabrication based on the designs shown in Figure 5.2(b,c)	1) MMA (8.5 EL9) coating	a) Spin-coating at 1500 rpm (~425 nm-thick resist layer) b) Bake at 150 $^{\circ}\text{C}$ for 70 seconds
	2) PMMA (495K) coating	a) Spin-coating at 5000 rpm (~125 nm thick resist layer) b) Bake at 180 $^{\circ}\text{C}$ for 70 seconds
	3) E-beam lithography	a) E-beam base dose = 400 $\mu\text{C}/\text{cm}^2$ b) E-beam operating (acceleration) voltage = 100 keV
	4) Development	a) MIBK:IPA (1:1) for 90 seconds b) IPA rinse for 30 seconds c) N_2 blow dry
	5) E-beam metal deposition	a) Ti/Au (5 nm/45 nm) for red-colour patterns and Ti/Au (15 nm/300 nm) for blue-colour patterns in Figure 5.2(b) b) Deposition rate = 0.5 $\text{\AA}/\text{sec}$ c) E-beam operating voltage = 10 keV

		d) Chamber pressure = 3×10^7
	6) Lift-off	a) NMP at 50 °C for 2 hours followed by DI water rinse and IPA rinse for 5 minutes each b) N ₂ blow dry
	7) Dicing	a) Spin-coating of S1813 photo-resist at 1000 rpm (~2 µm-thick resist layer) b) Hard bake at 120 °C for 15 minutes c) Dicing d) Striping of S1813 photo-resist in NMP at 50 °C for 1.5 hours followed by a rinse in DI water and IPA for 5 minutes each e) N ₂ blow dry
Graphene production	1) Sample/chip cleaning	a) Acetone and IPA cleaning for 10 minutes each b) Hotplate bake at 200 °C for 5 minutes c) UV light exposure for 10 minutes
	2) Graphene production	a) By means of mechanical exfoliation as explained in section 5.3 b) Sample sonication in IPA for 1 minute c) N ₂ blow dry
Patterning of graphene flakes by EBL/RIE	1) PMMA (1:2 anisole mix) coating	a) Spin-coating at 1600 rpm (~40 nm thick resist layer) b) Bake at 180 °C for 70 seconds
	2) EBL	a) E-beam base dose = 195 µC/cm ² b) PEC value = 60% c) E-beam operating (acceleration) voltage = 100 keV
	3) Development	a) MIBK:IPA (50:50) mix for 60 seconds b) IPA rinse for 30 seconds c) N ₂ blow dry
	4) RIE etch	a) Ar/O ₂ (4:1) gas flow b) RF power = 15 W c) Etch duration = 15 seconds d) Chamber pressure ~25 mTorr
	5) Resist strip	a) Rinse in acetone for 10 minutes b) Rinse in IPA for 10 minutes c) N ₂ blow dry
Fabrication of metal contacts onto graphene flakes	1) MMA (8.5 EL9) coating	a) Spin-coating at 2500 rpm (~370 nm thick resist layer) b) Bake at 150 °C for 70 seconds
	2) EBL	a) E-beam base dose = 110 µC/cm ² b) E-beam operating (acceleration) voltage = 100 keV
	3) Development	a) MIBK:IPA (50:50) for 75 seconds b) Rinse in IPA for 30 seconds c) N ₂ blow dry

	4) E-beam metal deposition	a) Ti/Au (5 nm/60 nm) b) Deposition rate = 0.5 Å/sec c) E-beam operating voltage = 10 keV
	5) Lift-off	a) NMP at 50 °C for 70 minutes b) DI water and IPA rinse for 5 minutes each c) N ₂ blow dry

Appendix B

Fabrication of graphene nano devices by HIM milling

Note that due to similarity of the sample preparation procedure (i.e. substrate preparation, fabrication of the chips and production of graphene) for both EBL/RIE and HIM milling methods, we have excluded the associated fabrication steps in this process flow sheet. Please refer to the process flow sheet presented in Appendix B for the fabrication steps involved in the sample preparation procedure.

TABLE B.2

A process flow sheet. Fabrication of graphene nano devices by the HIM milling method.

Process	Description of process steps	
Fabrication of metal contacts onto graphene flakes	1) MMA (8.5 EL9) coating	a) Spin-coating at 2500 rpm (~370 nm thick resist layer) b) Bake at 150 °C for 70 seconds
	2) EBL	a) E-beam base dose = 110 $\mu\text{C}/\text{cm}^2$ b) E-beam operating (acceleration) voltage = 100 keV
	3) Development	a) MIBK:IPA (50:50) for 75 seconds b) Rinse in IPA for 30 seconds c) N ₂ blow dry
	4) E-beam metal deposition	a) Ti/Au (5 nm/60 nm) b) Deposition rate = 0.5 Å/sec c) E-beam operating voltage = 10 keV
	5) Lift-off	a) NMP at 50 °C for 70 minutes b) DI water and IPA rinse for 5 minutes each c) N ₂ blow dry
Patterning of graphene flakes by EBL/RIE	1) PMMA (1:2 anisole mix) coating	a) Spin-coating at 1600 rpm (~40 nm thick resist layer) b) Bake at 180 °C for 70 seconds
	2) EBL	a) E-beam base dose = 195 $\mu\text{C}/\text{cm}^2$ b) PEC value = 60% c) E-beam operating (acceleration) voltage = 100 keV
	3) Development	a) MIBK:IPA (50:50) mix for 60 seconds b) IPA rinse for 30 seconds c) N ₂ blow dry
	4) RIE etch	a) Ar/O ₂ (4:1) gas flow b) RF power = 15 W c) Etch duration = 15 seconds d) Chamber pressure ~25 mTorr
	5) Resist strip	a) Rinse in acetone for 10 minutes b) Rinse in IPA for 10 minutes c) N ₂ blow dry
Removal of organic contaminants	1) Annealing in forming gas	a) H ₂ /N ₂ (6%/94%) gas flow b) Gas flow rate = 1.3 L/min c) Temperature ramp up (25-320 °C) in 25 minutes d) Temperature ~320 °C e) Duration = 2 hours
	2) Annealing in argon	a) Ar gas flow b) Gas flow rate = 3 L/min

		c) Temperature ~ 320 °C d) Duration = 45 minutes e) Cooling down to ~ 25 °C
He-ion beam patterning	1) HIM milling	a) He-ion beam dose = $0.63 \text{ nC}/\mu\text{m}^2$ b) He-ion beam current = 1 pA c) He-ion beam operating (acceleration) voltage = 30 keV

Appendix C

Atomic layer deposition of Al_2O_3 on a GQD device for improving side gate modulations

In order to investigate the side-gate modulation of I_{DS} issue in our devices further, we decided to study the effect of dielectric material. To this end, we deposited ~ 4 nm-thick layer of Al_2O_3 by atomic layer deposition (ALD) onto the GQD device we discussed in the section 6.2.2. This was achieved in an ALD tool by using pulses of pure water (0.015 seconds) and Trimethylaluminum (0.015 seconds) at 160 °C under a vacuum pressure of 10^{-3} Pa. Based on our previous practices, each cycle (~ 30 seconds long) results in ~ 1.1 Å of Al_2O_3 . After the ALD deposition, in order to guarantee ohmic contact to the device for electrical measurements, the bond pads on the sample (see Figure 5.2(b,c)) associated with the device were scratched with probes needles to remove the Al_2O_3 layer on the gold bond pads. To ensure Al_2O_3 layer was successfully removed, we then measured the electrical characteristics of each bond pad to confirm their linear $I - V$ behaviour.

Figure A1 shows the electrical characterisation of the device at room temperature after Al_2O_3 deposition. Strangely though, the $I_{DS} - V_{DS}$ plot no longer showed a linear behaviour but rather exhibited a Schottky-like behaviour with a very weak bias current (Figure A1(a)). This resulted in speculation that the graphene flake was undergone a type of damage (i.e. production of defects) during the ALD process. In fact, deposition of dielectric materials onto graphene flakes have reported to result in severe degradation in mobility but, in those cases, graphene still exhibited its usual $I - V$ behaviour (i.e. linear $I_{DS} - V_{DS}$, ambipolar behaviour) [217]. In addition, we did not observe any improvement in the side-gate modulation of the I_{DS} even after the Al_2O_3 deposition (Figure A1(b)). However, we observed very small I_{DS} modulations by varying the back gate voltage V_{BG} (Figure A1(c)).

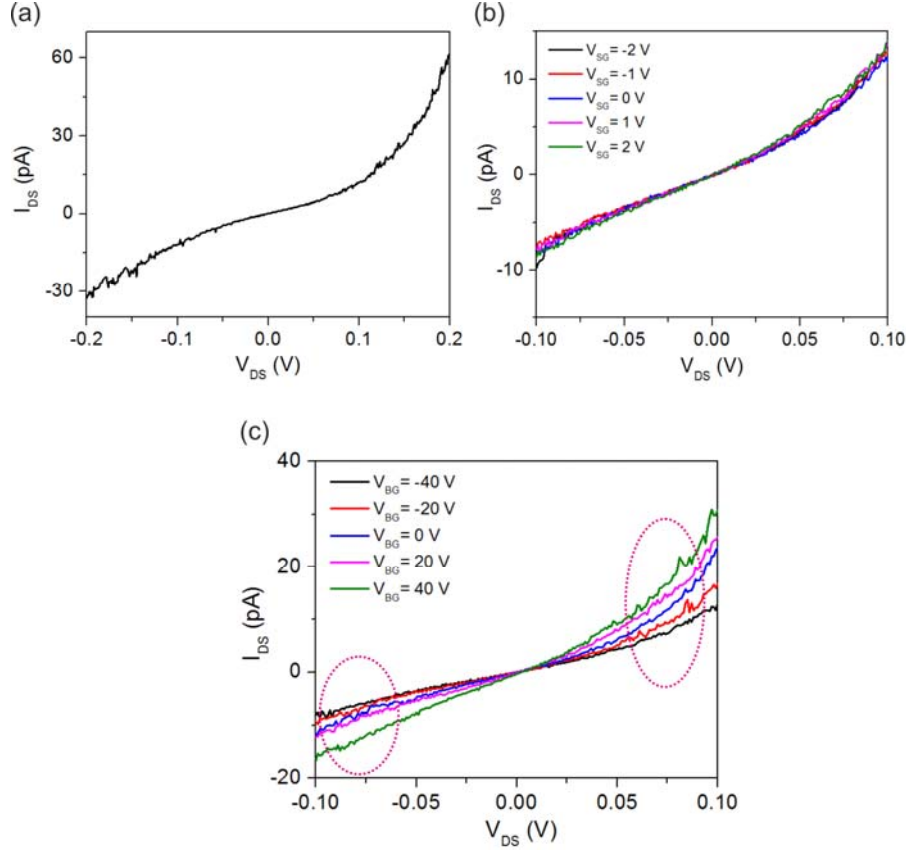


Figure A1 – Room temperature electrical measurements after ALD deposition of Al_2O_3 onto the GQD device in the section 6.2.2. (a) The measured $I_{DS} - V_{DS}$ plot which exhibits a Schottky-like behaviour instead of an ohmic (linear) behaviour. (b) No side-gate modulation (G_1 gate in Figure 6.11(b)) of I_{DS} as a function of V_{DS} was observed. (c) Observation of small back gate modulation of I_{DS} as a function of V_{DS} .

Electrical characteristics of the device at cryogenic temperatures (i.e. ~ 6 K) are shown in Figure A.2. Figure A.2(b) shows a weak ambipolar behaviour in $I_{DS} - V_{BG}$ plot for $V_{DS} = 700$ mV which strangely, exhibits current quantization subbands. We also found these subbands to be reproducible for different V_{DS} values (Figure A.2(c)). Moreover, contrary to electrical behaviour of the device pre-ALD deposition, we did not observe any sign of Coulomb diamonds in the $V_{DS} - V_{BG} - \log(G)$ contrast plot (Figure A.2(d)).

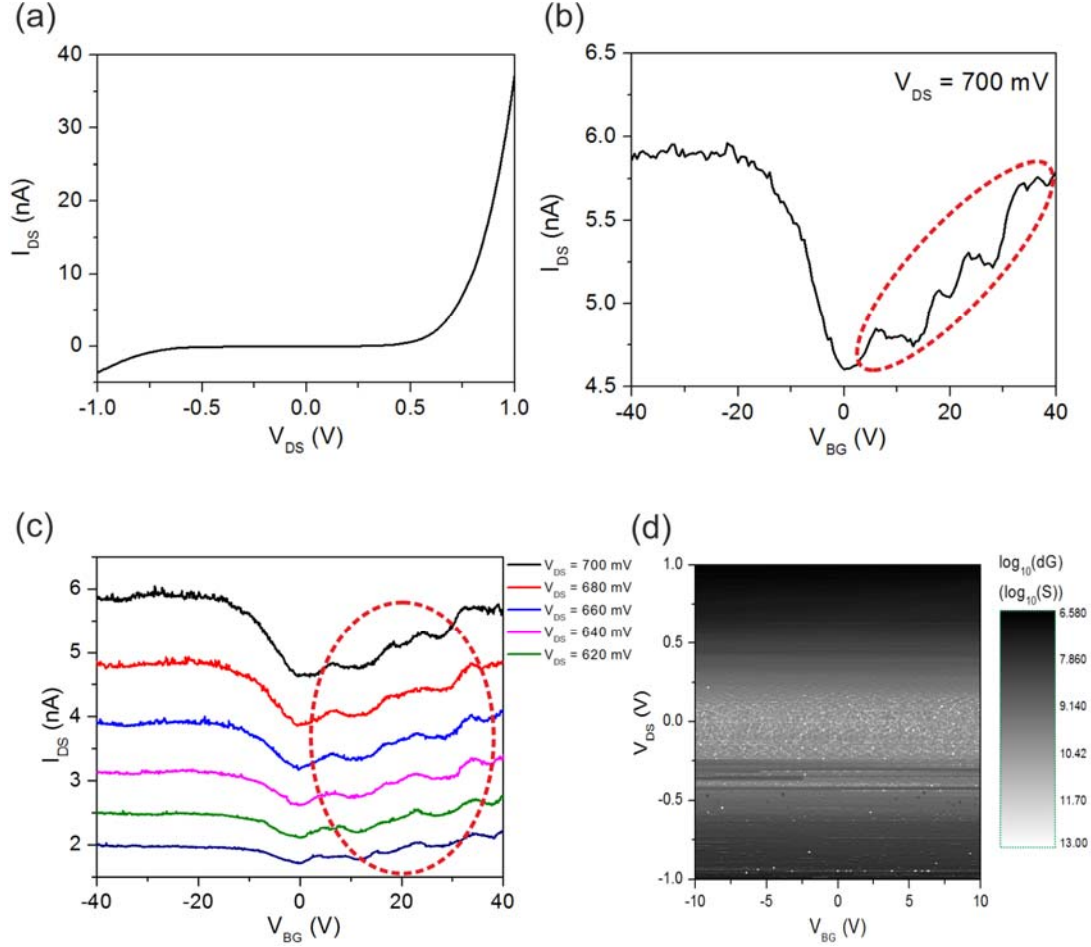


Figure A2 – Cryogenic temperature electrical measurements at ~ 6 K and at vacuum pressure of 10^{-4} Pa. (a) $I_{DS} - V_{DS}$ plot exhibiting a pronounced Schottky-like behaviour. (b) Back gate modulation of I_{DS} with $V_{DS} = 700$ mV, exhibiting quantized current subbands. (c) Observation of repeatable current quantization subbands in $I_{DS} - V_{BG}$ plot for different V_{DS} values. (d) $V_{DS} - V_{BG} - \log(dG)$ contrast plot of the device which shows no sign of Coulomb diamonds after ALD deposition.

Observation of current quantization subbands in GNRs has been reported before [216]. The subbands, which decreased in height with increasing the length of the GNRs, were attributed to low electron transmission probabilities through a GNR device mainly due to scattering by defects [216]. However, in our case, subbands were observed only on one side of the ambipolar transition (see Figure A2(b)). Furthermore, quantum transport calculations also confirmed that observation of subbands are due to enhanced electron backscattering by defects at

energies near subband edges [225]. These suggested possible influence of major defects in electrical behaviour of our GQD device after the ALD deposition.

To investigate this further, we employed atomic force microscope (AFM) scanning to image the sample. AFM images of the GQD device are shown in Figure A3.

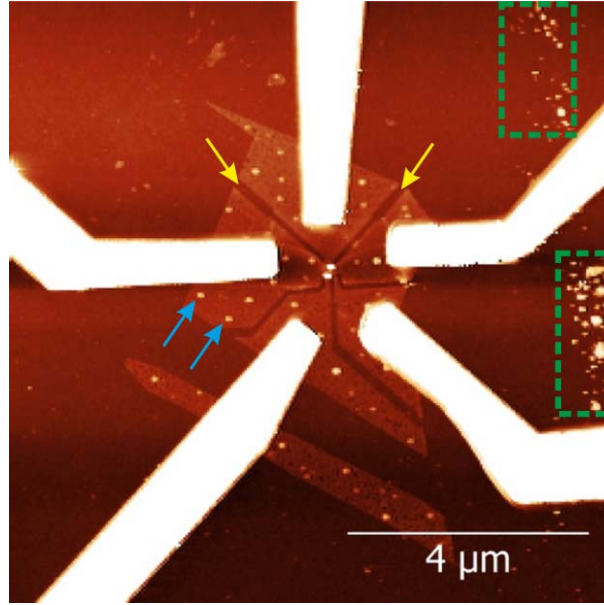


Figure A3 – Atomic force microscopy imaging of the GQD device after ALD deposition of Al₂O₃. The yellow arrows point to the RIE-etch patterns in the flake. The blue arrows point to the selective Al₂O₃ growth at defective sites. The green-dashed-rectangles highlight the regions of possible Al₂O₃ growth on the SiO₂ substrate.

In fact, AFM scanning revealed some interesting information about the sample. First, AFM imaging confirmed the reliability of our AutoCAD method for locating graphene flakes as well as our process for fabricating graphene QD devices. Figure A3 shows perfect alignment between the RIE etched patterns and the metal contacts on the graphene flake, and so faithful positioning of the flake was achieved by our AutoCAD method. Furthermore, the RIE etched patterns and the metal contacts are clearly very well-defined, and so confirmed the reliability of our fabrication process. However, we also observed random-size dot-shape features on the

graphene flake (pointed by the blue arrows in Figure A3) and in the some regions of SiO₂ substrate (the regions enclosed in the green-dashed-rectangles in Figure A3).

It has been reported that due to hydrophobic (chemically inert) nature of graphene surface, direct deposition of metal oxides on graphene fails to produce continuous layer of dielectrics and instead, results in selective growth. That is, ALD depends on chemisorption and rapid reaction of precursor molecules with surface functional groups. Consequently, no ALD can happen on pristine graphene flakes since they do not have any dangling bonds or surface functional groups to react with precursor. However, Wang *et al.* demonstrated that ALD can occur on the edges of graphene flakes, suggesting dangling bonds or possible termination of reactive species on the edges [218]. Also, the authors reported the possibility of random dot-shape ALD growth in the middle of graphene flakes due to likely existence of defects (e.g. pentagon-hexagon pairs or vacancies) [218]. Therefore, surface functionalization is required to provide an intentional nucleation sites/functionalization layer (e.g. *perylene tetracarboxylic acid* coating of graphene [218]) on the inert surface of graphene to achieve uniform ALD growth [217], [218].

In contrary, although we also observed random ALD growth on our graphene flake (pointed by blue arrows in see Figure A3) but no growth occurred on the edges of the flake. Furthermore, we observed regions with relatively high density of ALD growth (highlighted in the green-dashed-rectangles in Figure A3) on the SiO₂ substrate. This may suggest a possible fault in our ALD process, e.g. contamination deposition. Indeed, existence of organic contaminants or hydrocarbons (i.e. resist contaminants such as CH₃ or CH₂) on the sample can also hinder ALD growth on a substrate. Therefore, high resolution XPS analysis is required to truly identify the deposited features on the samples after the ALD process.

We then used same deposition process on more samples to investigate the consistency of defect creation and device degradation after our ALD process. Interestingly, it resulted in different outcomes. For instance, Figure A4(a) shows $I_{DS} - V_{BG}$ plot of the device *A* (see section 6.2.1) after Al₂O₃ deposition, where transition from hole regime to electron regime is no more clear. This is in contrast to the measurement results collected pre-ALD deposition (see Figure 6.5(c)).

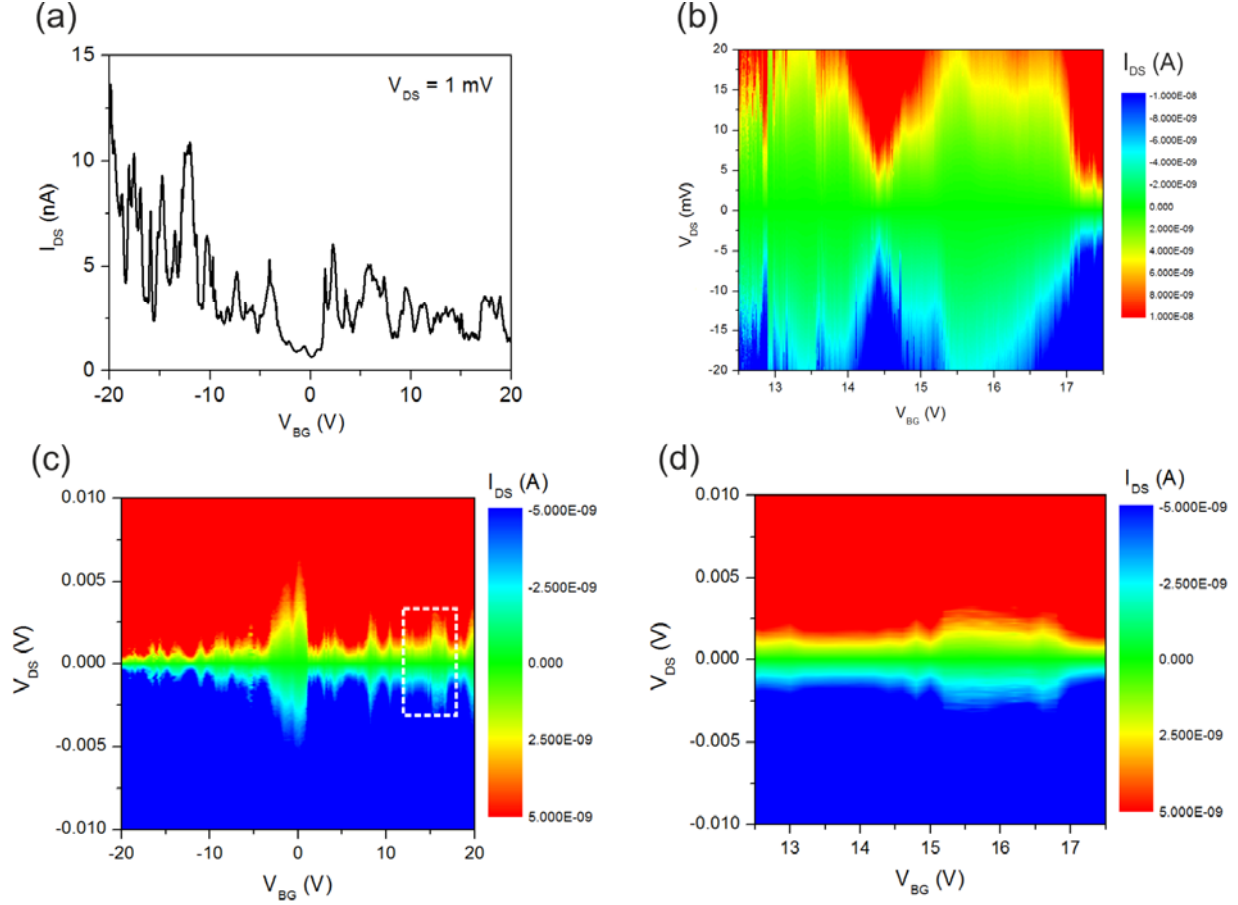


Figure A4 – Cryogenic temperature electrical measurements at ~ 6 K and at vacuum pressure of 10^{-4} Pa of the device *B*. (a) $I_{DS} - V_{BG}$ plot does not exhibit a clear transition between hole and electron regimes. (b) $V_{DS} - V_{BG} - I_{DS}$ colour plot of the device pre-ALD deposition. (c) $V_{DS} - V_{BG} - I_{DS}$ colour plot of the device after the ALD deposition, exhibiting a wider (smaller) ΔV_{BG} (E_g). (d) $V_{DS} - V_{BG} - I_{DS}$ colour plot of the white-dashed-rectangle region in Figure A4(c).

However, in contrast to the GQD device, we could still observe Coulomb diamonds in the $V_{DS} - V_{BG} - I_{DS}$ colour plot of the device *A*, shown in Figure A4(c). The figure also suggests a wider transport gap ΔV_{BG} and a much smaller $E_g \approx 1.25$ meV compare to those of observed pre-ALD deposition in the device (see section 6.2.1 and Figure A4(b)). Furthermore, Figure A4(b) and Figure A4(d) show same region of $V_{DS} - V_{BG} - I_{DS}$ colour plot before and after the ALD deposition, respectively. A comparison between these two figures suggests a considerable change in the size of the Coulomb diamonds after the ALD deposition.

Al_2O_3 deposition on the device B (see section 6.2.1) resulted in death of the device. Furthermore, $V_{DS} - V_{BG} - \log_{10}(dG/S^{-1})$ contrast plot collected after the ALD process on a DQD device fabricated in CVD graphene, with similar device design to that of for device A and B but with 80 nm-wide constrictions and dots size of 105 nm, also showed very weak (noisy) Coulomb diamond-shaped current blockaded regions (Figure A5(a)). On the other hand, a DQD device with similar device dimensions fabricated in the same CVD graphene sample as the previous device exhibited a much more pronounced Coulomb diamonds in its $V_{DS} - V_{BG} - I_{DS}$ contrast plot where a $E_g \approx 8$ meV can be extracted (Figure A5(b)). However, this E_g value is not comparable to the energy gap value ($E_g \approx 2\text{-}5$ meV) expected for a 80 nm-wide and 300 nm-long GNR [83].

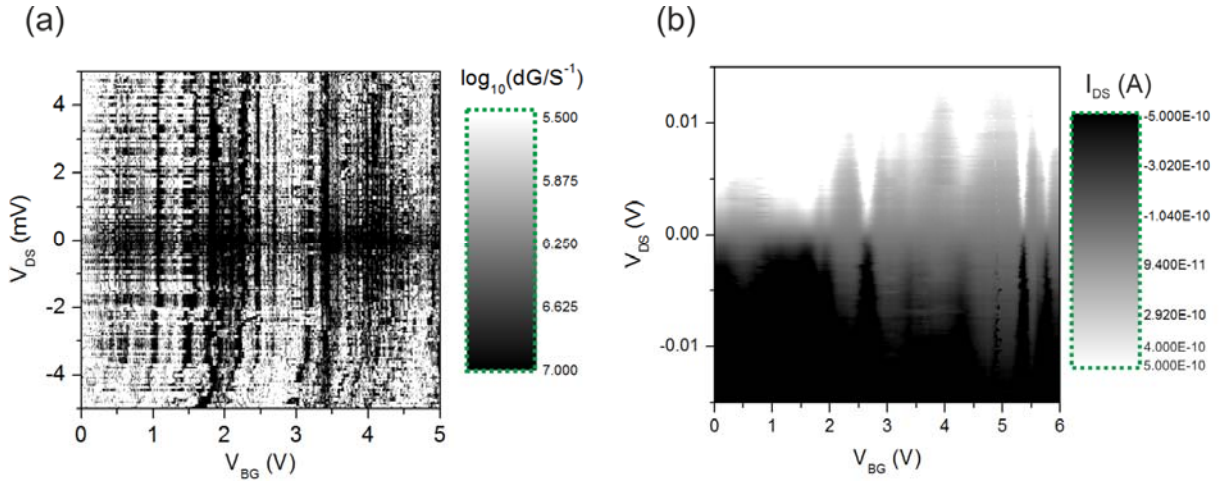


Figure A5 – Cryogenic temperature electrical measurements at ~ 6 K and at vacuum pressure of 10^{-4} Pa of two DQD devices fabricated in a same CVD graphene sample with 80 nm-wide constrictions and dots size of 105 nm after the ALD deposition. (a) A $V_{DS} - V_{BG} - \log_{10}(dG/S^{-1})$ contrast plot exhibiting very weak (noisy) Coulomb diamond-shaped current blockaded regions. (b) A $V_{DS} - V_{BG} - I_{DS}$ contrast plot where a $E_g \approx 8$ meV can be extracted.

Given the fact that all the DQD devices discussed in this Appendix were fabricated in the same CVD graphene sample and each exhibited a different electrical characteristic after the

Al_2O_3 deposition suggests the strong randomness of the impact of the ALD process. This can be attributed to hydrophobic nature of graphene which results in selective Al_2O_3 growth on the sample. Furthermore, we did not observe any improvement for side-gate modulation of I_{DS} after the Al_2O_3 deposition.

Currently, these results show that there is no systematic defect creation and/or consistency in the electrical behaviour of the devices after the ALD deposition. Therefore, surface functionalization of the graphene samples should be considered for future experiments to ensure uniform Al_2O_3 growth.

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