

Configurable Analogue Design

Conquering Variability in an Uncertain World

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Abstract—An increasing issue for analogue integrated circuit designers is the demand to not only provide cutting edge performance, but also to adjust to the demands of smaller process nodes, with the increased variability and other design demands as a result. While digital circuits have the basic advantage of being able to cope with some level of degradation in devices (as long as it does not fundamentally affect the logical behavior of the circuit), in contrast, analogue and mixed signal circuits are generally highly susceptible to those variations. This paper will describe some techniques that can mitigate the intrinsic variability of devices and therefore reduce the subsequent impact on the circuit designs themselves.

Keywords—analogue and mixed signal, integrated circuit design, configurable devices

I. INTRODUCTION

It has been well known for many years that as the technology nodes decrease in size, there will be a corresponding degradation in the device repeatability, mainly due to variation effects. Bernstein, et al [1] provide a seminal work evaluating different nodes and analyzing the reduction in yield as a result of the increased basic variability of the devices. For many years analogue designers lagged behind the significant advances in technology node reduction of the digital design community so this was not a major issue, but with the digital nodes being 40nm and lower, the analogue and mixed signal (AMS) community is now pushing into sub 100nm processes to enable easy integration. This is the point where device variability becomes a significant issue, especially when attempting to achieve high performance.

The challenge for circuit designers then is which approach to take to combat the issue of intrinsic device variability to achieve acceptable yield and performance. Initial efforts to combat these effects fell into two main approaches. The first was to use circuit design techniques to attempt to mitigate the variability of devices, using arrays of devices, such as Field Programmable Analog Arrays (FPAA) by Hall, et al in [2] to design specific operational amplifier based circuits. A variation of this type of approach was to use a network of transistors that could be configured in a completely arbitrary manner using a network of switches to achieve the desired performance, as described by Zebulum, et al [3], where the

idea was to use a network of switches to configure a transistor amplifier using evolutionary algorithms. With a network of devices to work with, it becomes possible to implement algorithms, such as evolutionary (or Genetic Algorithms) to find an optimal solution, one of the first examples of this type of application demonstrated by Lee and Gulak [4].

The alternative approach to dealing with the issue of device variability is to use device level techniques including device calibration. Trimming was commonly used in early devices, however this is obviously expensive and time consuming, therefore not a practical option for modern day high-density systems. Direct calibration of devices is therefore the preferred route when this type of approach is required. One of the techniques applied for this is substrate biasing, where the substrate of the entire chip or circuit is biased. For analogue circuits, this method can be scaled down to be applied to individual transistors, where it is commonly referred to as Dynamic Threshold MOS (DTMOS), as introduced in [5]. While this type of biasing technique is useful, especially in some specific SOI processes, where it is relatively straightforward to isolate sections of a circuit, in most cases it is complex and difficult to implement. As a result, the idea of configurable analogue devices [6] has become interesting from a circuit designer's perspective in that individual devices can be tailored to meet a specific performance requirement. This has a specific application in extreme environments where the impact of temperature can have a massive effect in addition to the intrinsic device characteristics on the overall circuit performance [7].

II. CIRCUITS IN EXTREME ENVIRONMENTS

Extreme environments lead to different issues for circuit designers to deal with, and can have a dramatic effect on the longevity and performance of the circuits [8-10]. Dealing with high temperature used to be a difficult issue for conventional CMOS design, however the development of Silicon Carbide (SiC) devices have a much higher tolerance to temperature, however as this is a relatively new technology, the variability is still an issue [12]. Radiation tolerance which has conventionally been the province of SiGe devices has also been investigated using advanced packaging [13],[14]. Other

techniques have been to use arrays of devices [11] to combat the variations of temperature and hence device behavior.

The extension of the use of calibration for both analogue and digital devices has also been used, however these have a significant limitation, that will be addressed later in this paper [15],[16].

III. CONFIGURABLE ANALOGUE TRANSISTORS

With the problem of extreme environments and external variations driving the circuit designer from trimming (static) solutions, to a more dynamic approach, particularly one that could be deployed in remote locations (such as Space), an electronic form of calibration becomes attractive. To achieve this the basic approach of the configurable analogue transistor was developed, where a device is partitioned into a main section, and increasingly small “slices” to enable multiple size options to be achieved, with minimal overhead. The basic device structure was described in [6] and is reproduced in figure 1.

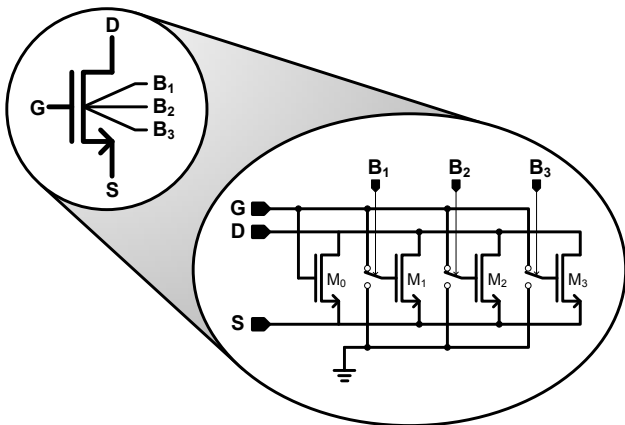


Figure 1: Configurable Analogue Transistor (from [6])

While this provides a configurable device, this is only the start of the process, as the device needs to be sized correctly, placed in the most appropriate place in the design, and then calibrated in operation. In order to identify the critical devices (to maintain the most efficient ratio of configurable devices to standard devices), it is essential to find those devices where configuration will affect the correction the most. This is a subtle difference from those devices which cause the variation, and therefore the circuit must be analyzed to not only find the devices causing a problem, but also those which are the most effective at correcting the problem. Rudolf et al [18] provide an approach where the circuit is simulated and the analysis is designed to identify the most critical devices and then minimize the overhead of the additional devices. Modeling and Simulation can be used to understand the nature of specific failures and how they affect the circuit performance [19].

The second step having identified the critical devices in the circuit, the next step is to size the devices in such a way that the right number of slices and size of slices can be obtained.

Wilson et al [17] discussed the mathematical process by which the intrinsic device variation can be used to calculate the ability of multiple slices to compensate for variation, and then to size the configurable device to achieve the optimal ability to compensate for predicted variation due to device tolerances.

IV. EXTREME ENVIRONMENTS AND CAT

The other application of the technique is to allow compensation for temperature changes across a wide range, and this is a suitable way to demonstrate the ability of the CAT to improve the performance of an operational amplifier based circuit, where accuracy and stability are crucial, such as an instrumentation amplifier as shown in figure 2. The devices that have CAT transistors are highlighted in red, and the resistor R7 is also configurable with a simple switching arrangement.

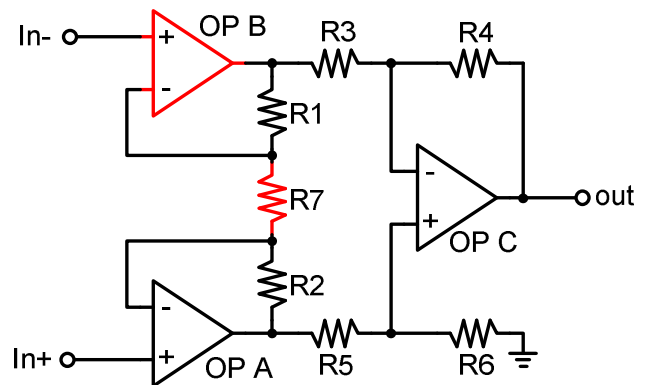


Figure 2: Instrumentation Amplifier

When the basic gain performance of the amplifier is compared with and without the CAT implemented, the difference can be seen with a dramatic difference due to temperature effects without CAT and a very stable result with the CAT – as shown in figure 3.

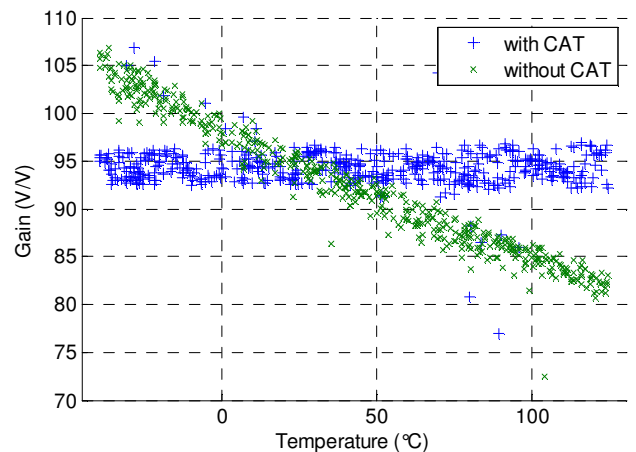


Figure 3: Gain versus temperature

To put this in context, the operational amplifier has only two CAT devices and therefore only three devices (2 transistors

and one resistor) were required to completely compensate for the thermal change.

When process and mismatch variation are considered, similar improvements are also seen. Mismatch variation is the most common issue within a single circuit and the effect of adding a CAT can be clearly seen in figure 4, where the inclusion of the CAT provides a much more tightly controlled gain response

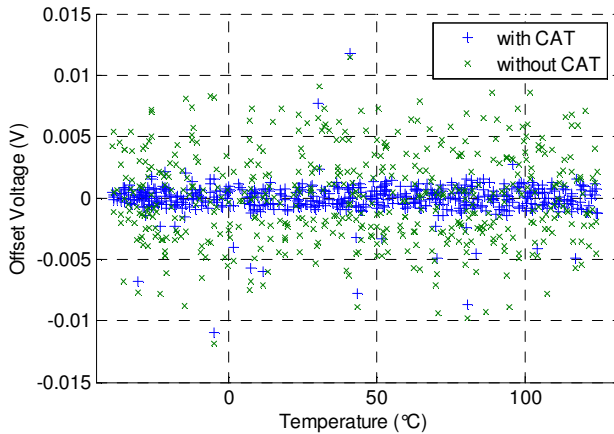


Figure 4: Gain versus temperature (with mismatch)

V. CONCLUSION

This paper provides a brief overview of some of the common techniques that can be applied to mitigate the effects of process variation and environmental effects (such as temperature). A specific technique (Configurable Analogue Transistors) is shown to be effective in combating both approaches, and with sensible selection of devices, can be at a very minimal overhead to the circuit designer.

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