

Silicon Diffusion Engineering in Rapid Melt Growth of Silicon-Germanium on Insulator

C. G. Littlejohns, F.Y. Gardes, M. Nedeljkovic, G. Mashanovich, G.T. Reed

Optoelectronics Research Centre, University of Southampton, Southampton, SO17 1BJ, UK

In this paper we focus on developing an efficient method to obtain a crystalline SiGe layer on top of an insulator. The method is aimed at enabling the fabrication of different concentration of crystalline SiGe alloy through structure engineering. This technique could enable the alloy composition to be different by design across a single wafer by using a single Germanium deposition step.

Introduction

Ge or GeSi-on-insulator (SGOI) is a desirable system with applications in electronic and photonic devices such as photodetectors, mid-infrared waveguides and high mobility Ge complementary metal oxide semiconductors (CMOS). A number of methods have been proposed to produce blanket SGOI films on Si wafers, including layer transfer [1, 2] and Ge condensation [2, 3]. A complementary technique to fabricate localized SGOI regions on a Si wafer is rapid melt growth (RMG) in micro-crucibles [4].

Results and discussion

In order to realize RMG a thin insulating layer is deposited onto a silicon wafer and patterned to expose seed areas. A blanket Ge layer is then deposited using a non-selective technique such as chemical vapour deposition (CVD) and patterned into strips protruding from the exposed Si seeds. These strips are then encapsulated with an insulating layer in order to form micro-crucibles which contain the Ge during the RMG. The wafers are heated using a rapid thermal annealer (RTA) at approximately 80 °C/s to a temperature above the melting point of Ge, in order to initiate the RMG process, and cooled naturally. All dislocation defects formed as a result of the lattice mismatch between Si and Ge are contained in the seed area due to defect necking, resulting in localized single crystal SiGe-on-insulator formation.

Control of the Si concentration in the SiGe strips is extremely challenging. As the samples are heated Si diffuses from the seed into the Ge strips forming SiGe alloys with a solidification temperature dependent on the Si concentration. Therefore at any given temperature, once the Si concentration reaches a certain concentration recrystallization commences in the seed area and propagates along the SiGe strips during cooling. However, since there is a large separation between the solidus and liquidus phase of a SiGe alloy [5], and the Si diffusivity is high in the liquidus phase, at the regrowth front a Si rich solid phase and a Ge rich liquid phase is apparent. This leads to a lateral gradation of the Si concentration along the strips with approximately 100% Ge at the end of the strips.

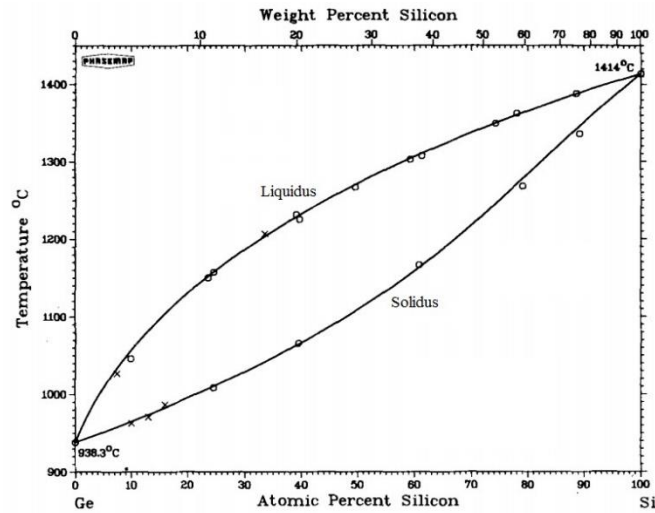


Figure 1 – Phase diagram of SiGe alloys showing separation of the solidus and liquidus phases – modified from [5]

Here we present a method of engineering the SiGe interdiffusion using tailored structures in order to modify the RMG kinetics resulting in a more consistent Si concentration along a SiGe strip. The approximate Si concentration in the SiGe strips has been characterised using 532 nm Raman Spectroscopy by taking the ratio of the SiGe peak (seen at approximately 380-400 cm^{-1}) and the GeGe peak (seen at approximately 300 cm^{-1}), as shown in Figure 2.

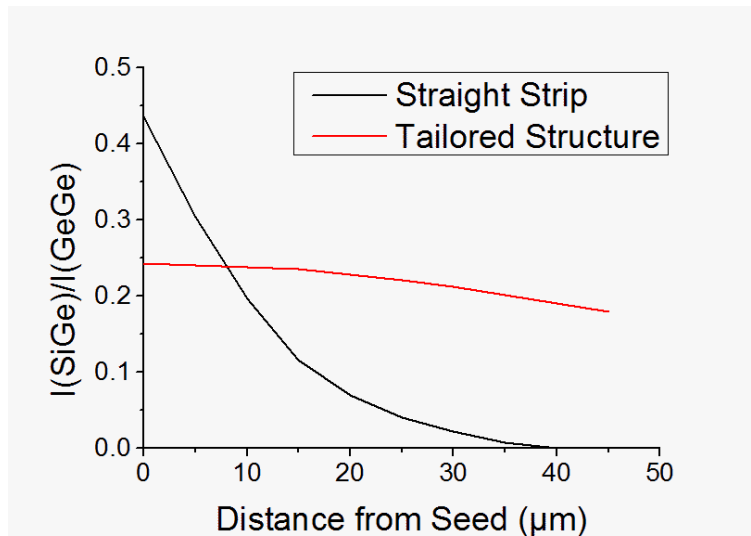


Figure 2 – Ratio of SiGe:GeGe Raman peaks showing more consistent Si concentration in the tailored structure when compared with a straight strip

This improved control of the Si concentration in single crystal SGOI could lead to a new breed of photonic and electronic devices on insulator.

Acknowledgments

This work was supported by the EPSRC through the HERMES and UKSP projects.

References

References:

- [1] A. J. Pitera et al. "Coplanar Integration of Lattice-Mismatched Semiconductors with Silicon by Wafer Bonding Ge / Si $1 - x$ Ge x / Si Virtual Substrates," *Journal of The Electrochemical Society*, vol. 151, pp. G443-G447, July 1, 2004 2004.
- [2] G. Taraschi, A. J. Pitera, and E. A. Fitzgerald, "Strained Si, SiGe, and Ge on-insulator: review of wafer bonding fabrication techniques," *Solid-State Electronics*, vol. 48, pp. 1297-1305, 8// 2004.
- [3] S. Nakaharai et al. "Characterization of 7-nm-thick strained Ge-on-insulator layer fabricated by Ge-condensation technique," *Applied Physics Letters*, vol. 83, pp. 3516-3518, 2003.
- [4] Y. Liu, M. D. Deal, and J. D. Plummer, "High-quality single-crystal Ge on insulator by liquid-phase epitaxy on Si substrates," *Applied Physics Letters*, vol. 84, pp. 2563-2565, 2004.
- [5] R. W. Olesinski and G. J. Abbaschian, "The Ge-Si (Germanium-Silicon) system," *Bulletin of Alloy Phase Diagrams*, vol. 5, pp. 180-183, 1984/04/01 1984.