Silicon-germanium composition engineering for next generation multilayer devices and systems

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Abstract: We report a method of engineering constant composition, single crystal, defect free SiGe-on-insulator grown by a rapid melt growth technique using tailored tree-like structures. Branches emanating from the main SiGe strip act as Silicon "reservoirs" to prevent the usual gradation of the alloy composition. This technique enables multiple SiGe strips to be grown using the same single generic Ge deposition step, each with a different composition determined by the structural design. Using this technique, we envisage a silicon photonics platform for on-chip optical communications whereby both modulators and detectors can be fabricated with the same device design and therefore the same simple fabrication steps. This can be realised by exploiting the rapid melt growth SiGe composition engineering detailed in this paper to tune the bandgap of electro-absorption modulators for multi-channel links using wavelength division multiplexing, whilst simultaneously forming pure Ge photodetectors. This technology could open the way for a new multilayer photonic architecture or for extremely low power density, multi-channel on-chip optical communications by integrating the concept with the cascaded photonic crystal architecture demonstrated by Debnath *et al.* [1].

1. Introduction

High quality Ge or silicon-germanium-on-insulator (SGOI) has many attractive properties for numerous applications in electronics and photonics such as electro-absorption modulators [2] and high mobility complementary metal-oxide semiconductor (CMOS) devices [3]. A number of methods have been proposed to produce SGOI films on Si wafers, including layer transfer and Ge condensation [4]. An alternative technique known as rapid melt growth (RMG) offers the potential for formation of localized single crystal, defect free layers at a low cost using only a single Ge deposition step and a single anneal step. However, until now this technique has resulted in a graded SiGe composition [5, 6], rendering it unsuitable for most devices and applications. Here, for the first time we report a method of engineering the SiGe composition to a near constant value with the use of tailored tree-like structures, which will revolutionise deployment of SiGe in circuit architectures.

2. Process Description

A thin SiO_2 layer is first deposited onto a Si wafer and patterned to open seed areas which act as the crystal template for the Ge during epitaxial regrowth. A blanket Ge layer is then deposited using a non-selective growth method and etched into the desired patterns. A top capping SiO_2 layer is deposited to form micro-crucibles within which the Ge is contained during the subsequent rapid thermal annealing (RTA) process. During this process the temperature is ramped up above the Ge melting point at a rate of 100 °C/s before being allowed to cool naturally. Whilst the Ge is in the liquid phase, Si diffuses from the substrate to form a liquid SiGe pool which is contained within the micro-crucible. During cooling epitaxial regrowth commences in the seed area and propagates along the SiGe strips.

3. Material Characterization

The SiGe layers were characterized using 532 nm Raman Spectroscopy by taking the ratio of the integrated intensity of the SiGe peak and GeGe peak (at approximately 380 cm^{-1} and 300 cm^{-1} respectively). This ratio can be correlated to Ge concentration using the Mooney equation [7] ($k = 1.2$). In a conventional straight SiGe wire there is a gradation of the Ge concentration as a result of the preferential Si rich solid formation at the epitaxial regrowth front, with rejection of the Ge into the liquid, according to the phase diagram in Fig. 1. However, by introducing Si "reservoirs" along the strip by forming a tree-like structure (Fig. 2) a liquid phase Si pool remains as the growth front propagates along the strip resulting in a near constant composition as shown in Fig. 3. The branches exhibit the expected straight strip characteristics with a gradation of the SiGe composition resulting in pure single crystal Ge at the tips. We have also shown that the composition along the centre strip can be controlled by the anneal temperature with a higher temperature resulting in a more Si rich alloy.

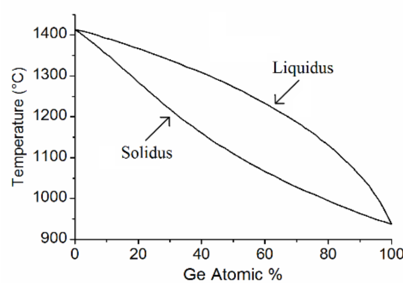

Fig. 1 *- SiGe phase diagram showing separation of the solidus and liquidus - adapted from [8].*

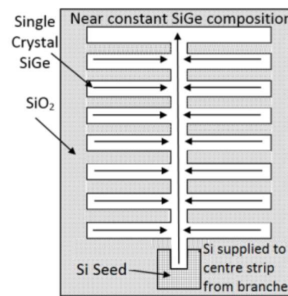

Fig. 2 *– SiGe composition engineering using tailored tree-like structures.*

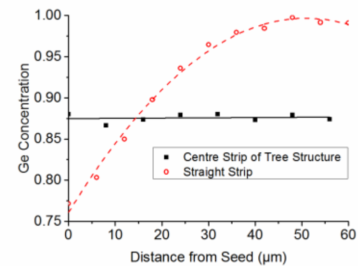

Fig. 3 *- Ge concentration in centre strip of tree structure compared to a straight strip. Anneal temp. = 955 °C.*

Threading dislocations caused by the lattice mismatch between the Si substrate and the Ge layer are confirmed by transmission electron microscope (TEM) imaging, to be confined to the seed area as a result of a dislocation necking mechanism. Electron back-scatter diffraction (EBSD) measurements confirm that the entire SiGe layer is of the same crystal orientation as the Si substrate.

4. Summary and Conclusion

This RMG method using tailored tree-like structures enables the fabrication of multiple single crystal SGOI layers of different compositions, on the same wafer, using only a single Ge deposition process and a single anneal process, by engineering the structure of the Ge layer to provide Si "reservoirs" along the strip. This facilitates a host of device designs, within a relatively simple growth environment, as compared to the complexities of other methods, and also offers flexibility in device designs within that growth environment, providing a path for the seamless integration of electronics and photonics at a low cost. Furthermore, for the first time, constant SiGe compositions can be regrown in situ.

References

[1] K. Debnath, L. O'Faolain, F. Y. Gardes, A. G. Steffan, G. T. Reed, and T. F. Krauss, "Cascaded modulator architecture for WDM applications," *Optics Express,* vol. 20, pp. 27420-27428, 2012.

[2] J. Liu, *et al.*, "Waveguide-integrated, ultralow-energy GeSi electro-absorption modulators," *Nat Photon,* vol. 2, pp. 433-437, 2008.

[3] R. Pillarisetty, "Academic and industry research progress in germanium nanodevices," *Nature,* vol. 479, pp. 324-328, 2011.

[4] G. Taraschi, A. J. Pitera, and E. A. Fitzgerald, "Strained Si, SiGe, and Ge on-insulator: review of wafer bonding fabrication techniques," *Solid-State Electronics,* vol. 48, pp. 1297-1305, 2004.

[5] H. Y. S. Koh, "Rapid melt growth of silicon germanium for heterogeneous integration on silicon," PhD, Department of Electrical Engineering, Stanford University, 2011.

[6] R. Matsumura, Y. Tojo, M. Kurosawa, T. Sadoh, I. Mizushima, and M. Miyao, "Growth-rate-dependent laterally graded SiGe profiles on insulator by cooling-rate controlled rapid-melting-growth," *Applied Physics Letters,* vol. 101, 2012.

[7] P. M. Mooney, F. H. Dacol, J. C. Tsang, and J. O. Chu, "Raman scattering analysis of relaxed Ge_xSi_{1-x} alloy layers," *Applied Physics Letters,* vol. 62, pp. 2069-2071, 1993.

[8] R. W. Olesinski and G. J. Abbaschian, "The Ge−Si system," *Bulletin of Alloy Phase Diagrams,* vol. 5, pp. 180-183, 1984.