# UNIVERSITY OF SOUTHAMPTON

FACULTY OF PHYSICAL AND APPLIED SCIENCES

Optoelectronics Research Centre


## Silicon-germanium for photonic applications

by


**Callum George Littlejohns**


Thesis for the degree of Doctor of Philosophy

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# ABSTRACT

FACULTY OF PHYSICAL AND APPLIED SCIENCES

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Germanium and silicon-germanium have become crucial materials in the silicon photonics field, enabling devices such as high speed photodetectors and high speed modulators to be realised.

In order to fabricate efficient and cost effective silicon photonic devices, high quality epitaxial germanium and silicon-germanium growth on silicon, or silicon-on-insulator, is of the utmost importance.

In this project, localised single crystal, defect free silicon-germanium on insulator islands have been grown using a rapid melt growth technique. Tailored tree-like structures have been used to modify the cooling rate of the structures during re-growth from the liquid phase. The resulting silicon-germanium composition profiles have been characterised using Raman spectroscopy.

Using these tailored tree-like structures, uniform composition silicon-germanium strips have been grown, which is the first time this has been demonstrated using a rapid melt growth technique. Additionally, the ability to locally tune the composition of adjacent silicon-germanium strips has been shown. This enables the possibility of growing a whole range of uniform composition strips, using only a single growth step and a single anneal step, for, amongst others, wavelength division multiplexing applications.

Epitaxial growth of germanium on silicon by plasma enhanced chemical vapour deposition has also been studied. Single crystal layers with a defect density of approximately $3.3 \times 10^8$ $cm^{-2}$ and root mean square surface roughness of 3.5 nm have been demonstrated. It has also been shown that the defect density, surface roughness and crystallinity are all improved with a two minutes, 600 °C anneal.

This material has been used to fabricate 12.5 Gbit/s, 0.1 A/W waveguide integrated, zero bias photodetectors for 1550 nm silicon photonics applications, and also, germanium-on-silicon waveguides for mid-infrared silicon photonics applications.

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# DECLARATION OF AUTHORSHIP

I, CALLUM GEORGE LITTLEJOHNS
declare that this thesis and the work presented in it are my own and has been generated by me as the result of my own original research.

SILICON-GERMANIUM FOR PHOTONIC APPLICATIONS

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;

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**Patents**

1. **C. G. Littlejohns**, F. Y. Gardes, G. T. Reed, "Melt-growth of single crystal alloy semiconductor structures and semiconductor assemblies incorporating such structures", 2014 (filed).

**Journal Papers**

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2. G. Z. Mashanovich, F. Y. Gardes, D. J. Thomson, Y. Hu, K. Li, M. Nedeljkovic, J. Soler Penades, A. Z. Khokhar, C. J. Mitchell, S. Stankovic, R. Topley, S. A. Reynolds, Y. Wang, B. Troia, V. M. N. Passaro, **C. G. Littlejohns**, T. Dominguez Bucio, P. R. Wilson, G. T. Reed, "Silicon photonic waveguides and devices for near- and mid-IR applications", *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 21, pp. 1-12, 2015.
3. M. Nedeljkovic, C. J. Mitchell, A. Z. Khokhar, S. A. Reynolds, D. J. Thomson, F. Y. Gardes, **C. G. Littlejohns**, G. T. Reed, G. Z. Mashanovich, "Mid-infrared thermo-optic modulators in SOI", *Photonics Technology Letters*, vol. 26, pp. 1352-1355, 2014.

4. **C. G. Littlejohns**, Y. Hu, F. Y. Gardes, D. J. Thomson, S. A. Reynolds, G. Z. Mashanovich, G. T. Reed, "50 Gb/s silicon photonics receiver with low insertion loss", *Photonics Technology Letters*, vol. 26, pp. 714-717, 2014.

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1. **C. G. Littlejohns**, M. Nedeljkovic, G. Z. Mashanovich, G. T. Reed, F. Y. Gardes, "Silicon-germanium composition engineering for next generation multilayer devices and systems", *IEEE Group IV Photonics*, Paris, France, 27-29 August 2014.

**Invited Conference Papers**

1. G. T. Reed, Y. Hu, G. Z. Mashanovich, F. Y. Gardes, D. J. Thomson, J. Soler-Penades, M. Nedeljkovic, A. Khokar, P. Thomas, **C. G. Littlejohns**, A. Ahmad, S. Reynolds, R. Topley, C. Mitchell, S. Stankovic, D. J. Richardson, P. Petropoulos, P. Thomas, P. R. Wilson, L. Ke, T. M. Ben Masaud, A. Tarazona, H. Chong, "Near infrared and the mid infrared silicon photonic devices", *Nano Korea 2014 Symposium*, Seoul, South Korea, 2-4 July 2014.
2. G. T. Reed, G. Z. Mashanovich, F. Y. Gardes, D. J. Thomson, Y. Hu, J. Soler-Penades, M. Nedeljkovic, A. Khokar, P. Thomas, **C. G. Littlejohns**, A. Ahmad, S. Reynolds, R. Topley, C. Mitchell, S. Stankovic, X. Chen, P. R. Wilson, L. Ke, T. M. Ben Masaud, A. Tarazona, H. Chong, "Silicon photonics", *7th ISTDM*, Singapore, 2-4 June 2014.
3. Y. Hu, **C. G. Littlejohns**, J. Soler Penades, A. Z. Khokhar, S. Stankovic, S. A. Reynolds, C. J. Mitchell, F. Y. Gardes, D. J. Thomson, "Multichannel silicon photonic devices based on angled multimode interferometers", *Photonics North*, Montreal, Canada, 28-30 May 2014.
4. G. T. Reed, G. Z. Mashanovich, F. Y. Gardes, D. J. Thomson, Y. Hu, J. Soler-Penades, M. Nedeljkovic, A. Z. Khokhar, P. Thomas, **C. G. Littlejohns**, A. Ahmed, S. Reynolds, R. Topley, C. Mitchell, S. Stankovic, P. R. Wilson, L. Ke, T. M. Ben Masaud, A. Tarazona, H. M. H. Chong, "Silicon photonic devices for the near and mid-infrared wavelength ranges", *Mediterranean Photonics Conference*, Trani, Italy, 7-9 May 2014.
5. G. T. Reed, G. Z. Mashanovich, F. Y. Gardes, D. J. Thomson, Y. Hu, J. Soler-Penades, M. Nedeljkovic, A. Khokhar, P. Thomas, **C. G. Littlejohns**, A. Ahmad, S. Reynolds, R. Topley, C. Mitchell, S. Stankovic, N. Owens , X. Chen, P. R. Wilson, L. Ke, T. Ben Masaud, A. Tarazona, H. M. H. Chong, "Recent results in silicon photonics at the University of Southampton", *Photonics West*, San Francisco, USA, 1-6 February 2014.

**Conference Papers**

1. **C. G. Littlejohns**, F. Y. Gardes, M. Nedeljkovic, G. Z. Mashanovich, G. T. Reed, "Silicon diffusion engineering in rapid melt growth of silicon-germanium-on-insulator", *ECS and SMEQ Joint International Meeting,* Cancun, Mexico, 5-9 October 2014.
2. F. Y. Gardes, **C. G. Littlejohns**, T. Dominguez Bucio, J. Soler Penades, C. J. Mitchell, A. Z. Khokhar, G. T. Reed, G. Z. Mashanovich "Ge-on-Si and SiGeOI for future photonic integrated systems", *EMRS Fall Meeting*, Warsaw, Poland, 15-18 September 2014.

3. F. Y. Gardes, **C. G. Littlejohns**, J. Soler Penades, C. J. Mitchell, A. Z. Khokhar, G. T. Reed, G. Z. Mashanovich, "Germanium for photonic applications", *7th ISTDM*, Singapore, 2-4 June 2014.
4. F. Y. Gardes, T. Dominguez Bucio, **C. G. Littlejohns**, G. T. Reed, K. Debnath, L. O'Faolain, "Group IV functionalization of low index waveguides", *Photonics North*, Montreal, Canada, 28-30 May 2014.

**Conference Posters**

1. **C. G. Littlejohns**, M. Nedeljkovic, G. Z. Mashanovich, G. T. Reed, F. Y. Gardes, "Single crystal silicon-germanium-on-insulator growth for next generation devices and systems", *Zepler Institute Photonics Day,* Southampton, UK, 19 September 2014 (best poster runner-up prize).
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3. **C. G. Littlejohns**, F. Y. Gardes, G. Z. Mashanovich, G. T. Reed, "Germanium growth by liquid phase epitaxy", *Japanese Silicon Photonics International School*, Tokyo, Japan, 26-28 January 2013.

Signed:…… Date:……

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# Chapter 1: Introduction

The demand for increasing bandwidth and data rates in the communication and computing industries has led to the migration from electronic signals to optical signals at certain system levels. High data rates require high signal frequencies at which the skin effect becomes detrimental to the performance of copper interconnects. Optical signals are not susceptible to this effect, and because they use semiconductor or dielectric waveguides, they do not suffer from the resistive loss that dominates propagation loss in electrical lines [1]. High frequency, low loss signals, transmitted using optical fibres, revolutionised long distance communications in the 1990's, and have since become an integral part of the World Wide Web. However, optical signals have yet to replace electrical signals for short distance connections because of the higher costs of conventional optical systems. Nevertheless, the future need for on-chip optical interconnects has been discussed by Intel as early as 2004 [2].

This project is concerned with the development of low-cost, low thermal budget, epitaxial growth of germanium and silicon-germanium (SiGe) on silicon, and silicon-on-insulator (SOI) substrates, for use in the silicon photonics industry for, amongst other applications, high speed modulation and photodetection.

## 1.1 Silicon photonics

Silicon has dominated the electronics industry for decades, and is now also becoming the material of choice for parts of the photonics industry; an area that has traditionally been dominated by III-V semiconductors [3, 4]. One of the main advantages of silicon photonics is its compatibility with complementary metal oxide semiconductor (CMOS) technologies, therefore facilitating electronic and optical integration on the same wafer, in the same fabrication facility. This also enables the transfer of decades of knowledge of silicon processing techniques. Silicon is also an abundant material, and therefore available at low cost when compared with other semiconductor substrates. The challenge lies in reducing

the fabrication costs associated with silicon photonics circuits, which will only be achieved through mass production.

Another potential benefit of migrating to optical systems is the reduction in power consumption. In electronic systems, the dominant energy dissipation is charging and discharging the capacitances of the interconnect wires. Furthermore, as the electronic interconnects become smaller to accommodate more transistors, their resistance is raised, further increasing the energy dissipation of the system. In optical interconnect systems these issues are not prevalent [5].

The refractive index (RI) of crystalline silicon at 1.55 μm, the most commonly used communications wavelength, which corresponds to the minimum propagation loss in optical fibres, is 3.476 (see Fig. 1-1), compared with a refractive index of 1.443 for its native oxide ($SiO_2$) [6]. This large refractive index contrast allows for high confinement of light and device miniaturisation, and is utilised by the most commonly used silicon photonics substrate: silicon-on-insulator.

The field has already yielded its first commercial products. In 2000, Bookham Technology (now Oclaro) commercially pioneered the first integrated silicon photonics product. They offered an arrayed waveguide grating (AWG) multiplexer, integrated with variable optical attenuators (VOA) [7]. In 2007, Luxtera released a CMOS photonics product [8] that contained 4 separate transceiver channels, each capable of transmitting 10 Gbit/s over 300 m. In 2012, Luxtera announced that this product had reached 1 million sales [9]. Luxtera have since developed an improved version of the product that is capable of transmitting 4 channels at 28 Gbit/s, powered by a single co-packaged laser [10]. These products offer a fully integrated solution, with on-chip waveguide level modulation and photodetection, along with associated electronics.

In 2012, IBM announced their first fully integrated CMOS silicon photonics transceiver [11]. Using 90 nm standard CMOS fabrication techniques, they were able to achieve 4 channels at 25 Gbit/s each, with an external light source.

In early 2013, Intel announced that it was shipping engineering samples of a 100 Gbit/s silicon photonics module, intended for links inside and between racks in data centres [12].

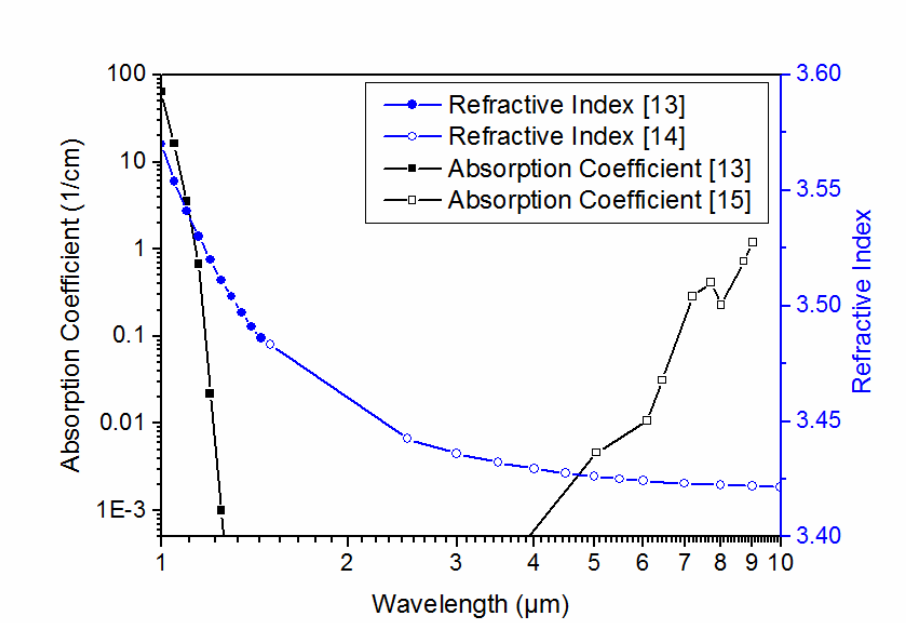


*Fig. 1-1. Refractive index and absorption coefficient in silicon as a function of wavelength.*
*Data gathered from [13-15].*

Further development looks set to accelerate with, in addition to the above, companies such as Kotura (recently acquired by Mellanox Technologies Ltd.), Genalyte, Oracle and HP all actively involved with silicon photonics research.

### 1.1.1 Applications of silicon photonics

The current mainstream target application for silicon photonics is short reach interconnects, for example from server to server in datacentres. Other envisioned applications include implantable medical chips, sensing, and fibre-to-the-home internet.

## 1.2 Silicon-germanium and germanium epitaxial growth

In order to achieve a complete library of silicon photonics circuit building blocks, it is necessary to incorporate germanium onto the substrate to fabricate the receiving element of the circuit. This therefore demands epitaxial germanium growth on silicon.

The most challenging obstacle for high quality germanium and silicon-germanium epitaxial growth on silicon is caused by the 4.2% mismatch in lattice

constants of the two materials. This mismatch leads to the formation of performance inhibiting defects in the epitaxial layer.

High quality germanium and silicon-germanium on silicon has been grown using a variety of techniques [16]. The majority of these techniques require high temperatures during the growth phase (> 600 °C), and are costly and complex. However, plasma enhanced chemical vapour deposition (PECVD) offers a low cost, low temperature growth method. In addition, rapid melt growth (RMG) offers the potential to grow localised high quality, single crystal germanium and silicon-germanium on insulator [17], using only a simple, non-critical growth step, and a single anneal step.

## 1.3 Germanium photodetectors

Silicon is transparent at 1.55 μm and therefore, as described above, germanium is often used for photodetection. Germanium, along with silicon, is a group IV material, and therefore avoids the contamination issues relating to III-V materials. It has the same diamond face centred cubic crystalline structure as silicon, but has a smaller bandgap, allowing it to absorb light at the communications wavelengths. Germanium also offers both higher electron mobility and higher hole mobility when compared with silicon, which ultimately allows for faster electronic devices. These properties make germanium the dominant material for silicon photonics integrated photodetectors [18-20].

## 1.4 Thesis outline

This thesis begins with a background discussion of germanium and silicon-germanium epitaxial growth on silicon, followed by a summary of the principles of photodetection, as well as the important photodetector performance characteristics. The subsequent chapter reviews the current state-of-the-art in these fields.

There are then three chapters discussing the main areas of research carried out in this thesis. The first is a study of low cost, low temperature, germanium-on-silicon growth by plasma enhanced chemical vapour deposition. Using this technique, single crystal germanium is epitaxially grown on silicon at a

temperature of 400 ˚C, resulting in a defect density of approximately $3.3x10^8$ $cm^{-2}$ after an anneal at 600 °C for two minutes.

The second, and main area of research, is rapid melt growth of germanium and silicon-germanium on localised insulator islands. The main aim of this section is to develop a high quality localised silicon-germanium-on-insulator platform that will potentially enable the migration from conventional photonics silicon-on-insulator substrates, to silicon substrates typically used in the electronics industry. The use of the same substrate will greatly enhance the prospects of monolithic electronic-photonic integration. This can be achieved through the growth of localised silicon-germanium for modulation [21] and detection [22], connected by dielectric waveguides deposited on top of the active layer [23]. The challenge lies in developing a growth method that enables multiple silicon-germanium compositions to be grown for the realisation of multi-channel links, with the use of wavelength division multiplexing (WDM). In this chapter, single crystal, high quality, silicon-germanium-on-insulator is fabricated with a uniform composition using novel tailored tree-like structures.

The results gathered in these previous two chapters are subsequently utilised in the third and final research area: high speed germanium photodetectors. Zero bias, 12.5 Gbit/s waveguide integrated photodetectors are fabricated, with a responsivity, at a wavelength of 1550 nm, of approximately 0.1 A/W.

Finally the conclusions and potential future work are discussed

# Chapter 2: Background and theory

## 2.1 Properties of germanium and silicon-germanium

Si, Ge and $Si_{1-x}Ge_x$ alloys are all semiconducting materials with a diamond lattice structure based on that of a face-centred cubic unit cell. This enables epitaxial growth of one material onto the other for a plethora of applications in both photonics and electronics.

SiGe possesses full miscibility over its entire composition range which allows for the tuning of properties such as the bandgap and the lattice constant between those of bulk Si and bulk Ge.

Both Ge and SiGe have a higher hole and electron mobility than Si, meaning that they will ultimately lead to faster electronic devices, e.g. transistors [1]. In fact, Ge has the highest hole mobility of any known semiconductor [2]. It also has a major advantage over its III-V competitors in that it is a CMOS compatible material, and is in fact already part of the CMOS production line. This means that monolithic integration of Si, SiGe and Ge based electronics and photonics on the same substrate is possible. Table 2-1 compares some key properties of Si and Ge. The lower bandgap of Ge, when compared to Si, is critical for the fabrication of photodetectors as it results in an optically absorbing material at wavelengths where Si is transparent. The lattice constant is a key property for epitaxial growth as it determines the physical size of the crystal structure.

*Table 2-1. Some key properties of Si and Ge, gathered from [3].*

| Property | Silicon | Germanium |
|---|---|---|
| Bandgap (eV) | 1.11 | 0.66 |
| Electron mobility ($cm^2V^{-1}s^{-1}$) | 1400 | 3900 |
| Hole mobility ($cm^2V^{-1}s^{-1}$) | 450 | 1900 |
| Lattice constant (nm) | 0.5431 | 0.5658 |

## 2.2 Germanium energy band structure

A semiconductor, such as Ge, can be defined as either a direct bandgap material or an indirect bandgap material. In a direct bandgap material, an electron can move from the valance band to the conduction band if it gains sufficient energy to cross the bandgap. However, in an indirect bandgap material, in order for an electron to move from the valence band to the conduction band it needs to not only gain sufficient energy, but it also requires a change in momentum.

Ge is defined as an indirect bandgap material because its lowest energy bandgap, $E_g$ = 0.66 eV, is indirect. However, Ge also has a direct bandgap, $E_{\Gamma 1}$, only 140 meV above at 0.8 eV, as shown in Fig. 2-1. For comparison the bandgap of Si is 1.11 eV (also indirect).

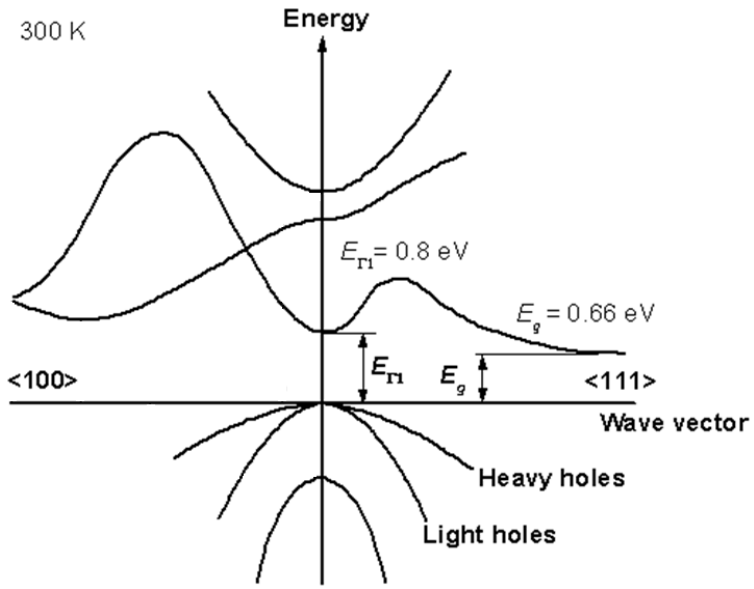


*Fig. 2-1. Energy band diagram of Ge at 300 K, modified from [4].*

## 2.3 Germanium and silicon-germanium epitaxial growth

Epitaxial growth of Ge and SiGe, on Si, is of vital importance for silicon photonics to enable fully integrated optical systems. A brief overview of epitaxial growth techniques and applications of Ge and SiGe on Si is given in Chapter 3.

If the lattice constants of two materials are the same, and both materials have the same crystal structure, then one material can be epitaxially grown on the other material without strain or dislocations. However, if there is a lattice constant mismatch between the two materials, as with Si and Ge, the epitaxial

layer will become strained as its lattice constant adapts to that of the seed crystal. Equation 2-1 calculates the 4.2 % lattice constant mismatch between Si and Ge from the parameters listed in Table 2-1:

$$\frac{5.65791\ \text{Å} - 5.4311\ \text{Å}}{5.4311\ \text{Å}} \times 100 = 4.2\ \% \qquad \text{Equation 2-1}$$

As first discovered by Van Der Merwe in 1963 [5], if the epitaxial layer reaches a critical thickness, determined by the lattice mismatch, amongst other properties, the excess in strain energy leads to the formation of misfit dislocations. The elastic strain energy, $E_{strain}$, can be calculated using Equation 2-2:

$$E_{strain} = \lambda \left(\frac{\Delta a}{a}\right)^2 At \qquad \text{Equation 2-2}$$

Where $\lambda$ is the biaxial elastic modulus, $\Delta a$ is the forced change in lattice constant, $a$ is the unstrained lattice constant, $A$ is the epitaxial film surface area and $t$ is the film thickness. The critical thickness for defect free, compressively strained Ge-on-Si has been shown to be around 4-10 nm [6]. Once this critical thickness has been reached it is energetically favourable to form misfit dislocations to reduce the elastic strain energy. The growth evolution of Ge-on-Si is demonstrated in Fig. 2-2 through to Fig. 2-4.

Fig. 2-2 shows the initial wetting layer formed when Ge is grown on Si. As the Ge lattice is 4.2% bigger than the Si lattice the Ge is compressively strained.

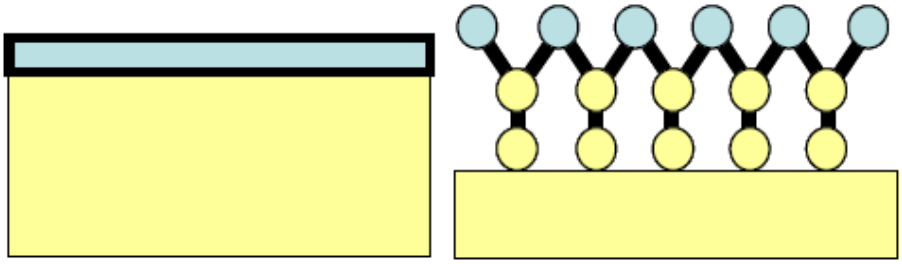

*Fig. 2-2. Cross-section and atomic view of Ge-on-Si growth, showing the wetting layer, reproduced from [7].*

Fig. 2-3 shows the addition of a few more Ge monolayers. Total strain energy increases linearly with film thickness, as per Equation 2-2.

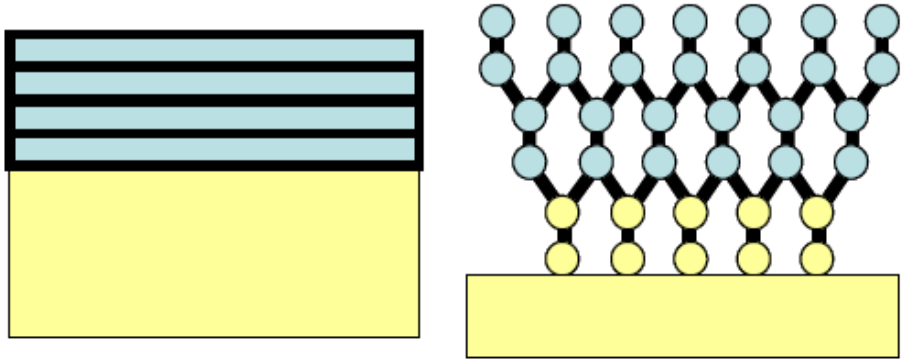

*Fig. 2-3. Cross section and atomic view of Ge-on-Si growth, below the critical thickness, reproduced from [7].*

Fig. 2-4 shows Ge-on-Si growth after the critical thickness has been reached. A misfit dislocation is formed that reduces the total elastic strain energy and allows a relaxed layer to be formed.

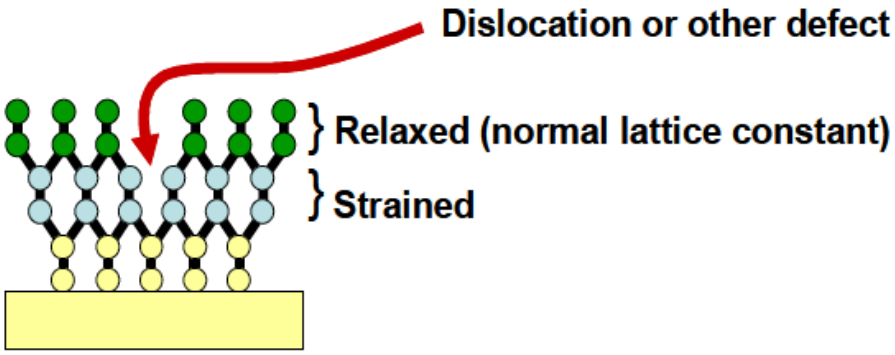


*Fig. 2-4. Atomic view of Ge-on-Si growth above the critical thickness, showing a misfit dislocation, reproduced from [7].*

Any subsequent layers grown on top of a film containing misfit dislocations will contain threading dislocations that propagate through the film. These dislocations can only terminate either at the surface, at high angle grain boundaries, at some material interfaces, or by annihilation with dislocations with an antiparallel Burgers vector (the Burgers vector represents the magnitude and direction of a lattice distortion) [8]. The density of these dislocations in the Ge layer, defined as the threading dislocation density (TDD) is an important measure of Ge-on-Si film quality. It is of vital importance to minimise the TDD of Ge-on-Si layers because these defects can degrade physical, optical, and electrical properties of the device material, which can lead to premature device failure and poor performance.

## 2.4 Epitaxial defect necking

Threading dislocations are terminated at the interface with an insulating material such as $SiO_2$. This fact can be exploited for TDD reduction using a process called epitaxial defect necking, as shown in Fig. 2-5.

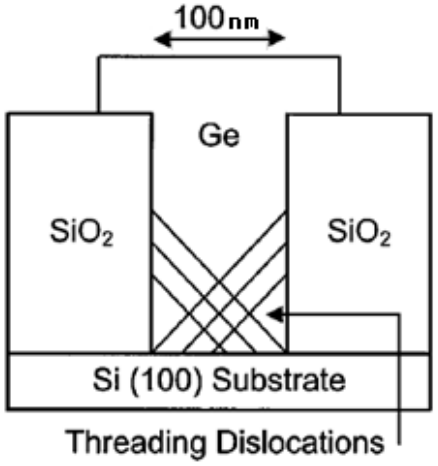


*Fig. 2-5. Cross-section diagram demonstrating the principles of epitaxial defect necking, reproduced from [9].*

In the (111) <110> diamond cubic slip system, misfit dislocations lie along the <110> directions and the slip plane is (111). Threading dislocations in the <110> directions make a 45° angle to the underlying Si (100) substrate. Therefore if the aspect ratio of the wells in the mask is greater than 1, crystallography dictates that threading dislocations will be blocked by the side-walls, resulting in a defect free Ge top surface. This is very similar to bulk Si Czochralski crystal growth [10].

The principles of epitaxial defect necking are used in the rapid melt growth work described in Chapter 5.

## 2.5 Light detection

When incident light falls upon the surface of a semiconductor, electrons are promoted from the valence band to the conduction band, providing the photons are of higher energy than the bandgap energy of the semiconductor, as shown in Fig. 2-6.

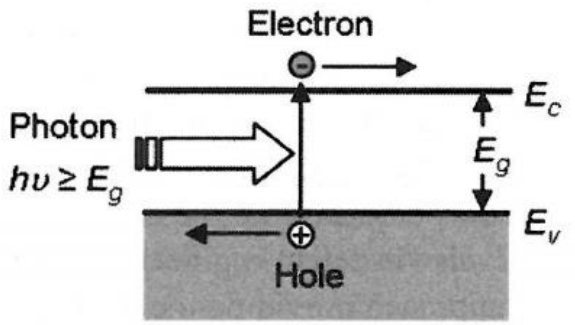


*Fig. 2-6. Optical absorption of a photon and consequent electron-hole pair generation, reproduced from [11].*
*$E_C$ is the conduction band energy, $E_V$ is the valence band energy and $E_g$ is the bandgap energy.*

The photon energy, *E*, can be calculated using Planck's equation:

$$E = h\nu = \frac{hc}{\lambda} \qquad \text{Equation 2-3}$$

Where *h* is Planck's constant ($6.6262\times10^{-34}$ Js), $\nu$ is the frequency, *c* is the speed of light in a vacuum ($2.9979\times10^{8}$ m/s) and $\lambda$ is the wavelength. Once the electrons are promoted to the conduction band they become mobile and can drift around the semiconductor under the influence of an electric field to produce a measurable current.

### 2.5.1 Absorption coefficient

The absorption coefficient, $\alpha$, describes a materials ability to absorb light at different wavelengths and can be calculated using the Beer-Lambert Law:

$$I = I_0 e^{-\alpha x} \qquad \text{Equation 2-4}$$

Where *I* is the transmitted intensity, $I_0$ is the incident intensity and *x* is the path length. Fig. 2-7 displays the absorption coefficient for both Si and Ge as a function of wavelength.

The inflection point on the Ge absorption spectrum, at a wavelength of approximately 1.55 μm, is due to the shift from direct to indirect absorption.

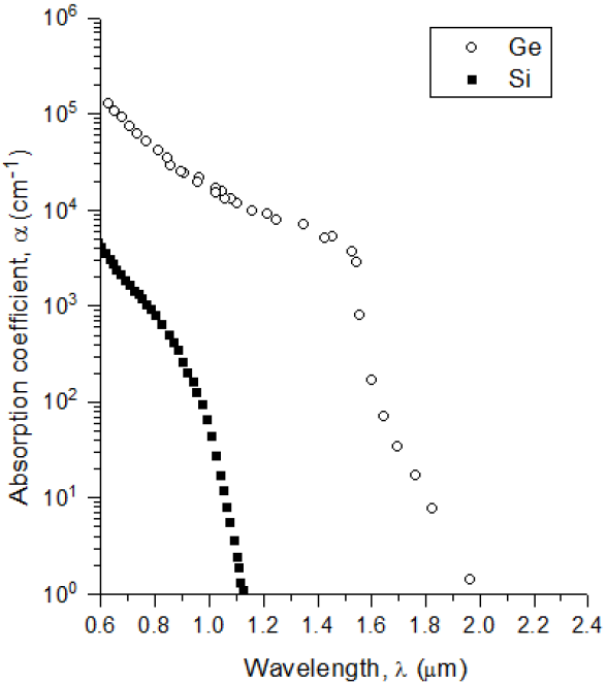


*Fig. 2-7. Absorption spectra of Si and Ge at 300 K, modified from [12].*

### 2.5.2 *p-n* junctions

The properties of a semiconductor can be altered with the introduction of a dopant, such as boron (B) or phosphorous (P). In an *n*-type region the dopants contribute mobile electrons that shift the Fermi level, $E_F$, (the energy level where the probability of occupation by an electron is 0.5) closer to the conduction band. Hence, there is a resultant surplus of electrons in the conduction band. Likewise, in a *p*-type region the dopants contribute mobile holes that shift the Fermi level closer to the valence band, resulting in surplus holes in the valence band.

When a *p*-type region and an *n*-type region are in contact with each other, the excess electrons in the *n*-type region diffuse across to the *p*-type region where they recombine with the abundant holes, and leave a positively charged impurity within the crystal structure of the *n*-type region. The opposite is true for holes in the *p*-type region. This results in a carrier depletion region, and a built in electric field which opposes the diffusion of carriers, causing equilibrium to be established. This is demonstrated in Fig. 2-8.

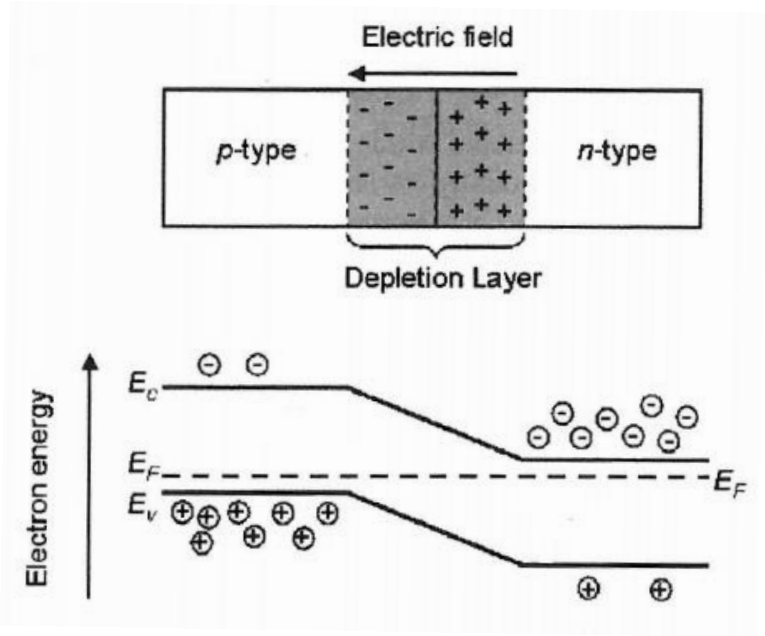


*Fig. 2-8. A p-n junction in equilibrium, reproduced from [11].*
*a) Electric field across depletion layer caused by ionised donors, b) electron energy band diagram.*

If a reverse bias is applied to the *p-n* junction then the depletion layer is extended as the potential barrier is increased, leading to reduced minority carrier diffusion.

Compared with an ordinary *p-n* junction, a *p–i–n* junction has an undoped layer in the centre of the device, leading to a bigger depletion region which enables more efficient collection of the photogenerated carriers in a detector. The introduction of an intrinsic region therefore generally leads to an improved photodetector.

### 2.5.3 Photodetector performance characteristics

In order to determine the relative performance of a photodetector, a number of important characteristics must be considered. This section defines these characteristics.

### 2.5.3.1 Quantum efficiency

The quantum efficiency, $\eta$, is defined as the number of electron-hole pairs generated per incident photon, as per Equation 2-5. It is dependent on the absorption coefficient of the material and is therefore wavelength dependent.

$$\eta = \frac{electrons/sec}{photons/sec} = \frac{I_p}{q}.\frac{h\nu}{P_{opt}} \qquad \text{Equation 2-5}$$

Where $I_p$ is the photogenerated current, $q$ is the charge of an electron ($1.6\times10^{-19}$ C) and $P_{opt}$ is the incident optical power.

### 2.5.3.2 Responsivity

The responsivity, $R$, of a photodetector relates the incident optical power to the amount of generated photocurrent in units of A/W, as per Equation 2-6. Again, this is wavelength dependent and will be significantly higher at energies high enough to make direct band-band transitions possible.

$$R = \frac{\mathrm{I}_p}{P_{opt}} = \eta\frac{q}{h\nu} \qquad \text{Equation 2-6}$$

The responsivity is a much more useful characteristic than the quantum efficiency when comparing photodetectors, as it is dependent on the whole device rather than just the absorbing layer.

### 2.5.3.3 Optical bandwidth

The optical bandwidth is measured by illuminating the device with monochromatic light, intensity modulated at increasing frequency, and measuring the voltage drop across a 50 Ω load connected to the output. The optical bandwidth is then defined as the frequency at which the output voltage drops below half the maximum voltage (DC voltage). The bandwidth of a device is limited by a combination of four factors [13]:

1. Drift time of carriers across the depletion region.
2. Diffusion of carriers generated outside of the depletion region.
3. Capacitance of the junction.

4. Access resistance and contact resistance.

The diffusion process is relatively slow so care must be taken to ensure that all the electron-hole pairs are generated in the depletion region. The drift time/velocity is related to the carrier mobility and the applied electric field. The carrier saturation velocity of Ge is of the order ~$10^7$ cm/s [14]. Therefore, if the depletion region is approximately 1 μm wide, and there is a strong electric field, the drift time will be picoseconds. This means that the drift time will be significantly shorter than the recombination time (the recombination time is expected to be of the order of tens of μs [15]), so the majority of carriers will be collected and contribute to the output current.

The capacitance, *C*, of a device can be approximated by its dimensions, as per Equation 2-7:

$$C = \frac{\varepsilon A}{d} \qquad \text{Equation 2-7}$$

Where $\varepsilon$ is the permittivity of the dielectric material, *A* is the cross sectional area of the doped regions acting as the plates and *d* is the depletion region width. It can be seen that increasing the width of the depletion region decreases the capacitance; however, this will also increase the drift time in the depletion region so a trade-off must occur in order to maximise the device speed.

The overall RC time constant is determined by the junction capacitance, the access resistance and contact resistance, and any load resistance applied to the device.

It is important to note that the electrical bandwidth of the photodetector is the frequency at which the optical power drops below half the maximum power. Electrical power is proportional to the square of the voltage, so in the decibel scale this appears as a factor of two difference between optical bandwidth and electrical bandwidth. Therefore, the 3 dB optical bandwidth is equivalent to the 6 dB point on the electrical response curve.

### 2.5.3.4 Dark current

The dark current, $I_d$, is the current flowing through the device when there is no input light source. Dark currents at room temperature have been shown by Ang

*et al.* [16] to be generated by Shockley-Read-Hall processes [17, 18]. In this mechanism, electron-hole pairs are generated via defect induced trap levels in the Ge forbidden gap, and then swept out of the device by the built-in electric field. It is therefore imperative to keep the number of defects in the Ge at a minimum to reduce the dark current of the resultant photodetector.

#### 2.5.3.5 Other important characteristics

Another important characteristic that must always be considered is the overall cost for both the raw materials and fabrication of the device. This must be kept to a minimum by using simple fabrication techniques and low cost materials. Other important characteristics that cannot be measured quantitatively include CMOS compatibility and ease of integration with existing technology.

## 2.6 Techniques used

This section will briefly describe and explain the important physics behind the fabrication and characterisation tools used in this thesis.

### 2.6.1 Chemical vapour deposition

In chemical vapour deposition (CVD), a film is produced by chemical reactions that take place on the substrate surface. The input gases react to form solid by-products, which are deposited on the surface of the substrate, and volatile gases that flow out of the reactor. In plasma enhanced chemical vapour deposition (PECVD), radio frequency (RF) power is applied across two electrodes inside the reaction chamber, which causes the input gases to dissociate and become ionised, forming a plasma. This allows deposition to take place at lower temperatures than more conventional CVD techniques. As described in "Silicon VLSI Technology" by Plummer *et al.* [19] there are 7 steps involved with PECVD:

1. Transport of the reactant gases into the chamber.
2. Dissociation of gases in the plasma.
3. Diffusion of the reactants from the plasma to the wafer surface.
4. Adsorption of the reactants on the wafer surface.
5. Surface processes, including migration to attachment sites and surface reaction.

6. Desorption of by-products from the surface.
7. Transport of by-products away from the surface.

A PECVD reaction chamber is shown in Fig. 2-9.

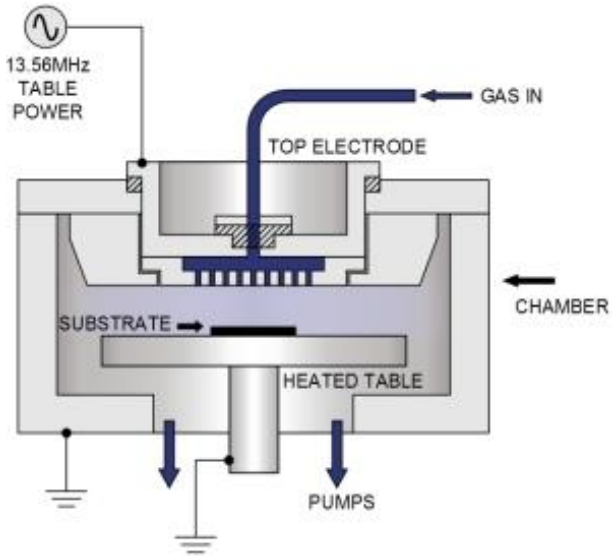


*Fig. 2-9. Schematic diagram of a PECVD reaction chamber, reproduced from [20].*

Ge is formed by the decomposition of $GeH_4$ gas by the following reaction:

$$GeH_4 \rightarrow Ge + 2H_2$$

$SiO_2$ is formed by the reaction of $SiH_4$ with $N_2O$, as per the following reaction:

$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2$$

Often, in the above reactions, the gaseous by-products are incorporated into the deposited film. This is usually undesirable and can be rectified by a densification process whereby the substrate is heated to a few hundred degrees to allow the gases to diffuse from the film.

The major variables that affect PECVD growth are temperature, pressure, and gas flow rates. The temperature must be high enough for the chemical reactions to take place, but a temperature that is too high may have detrimental effects on features already developed on the substrate. As a general rule, a higher temperature leads to a higher growth rate. A higher growth rate can also typically be achieved by increasing the gas flow of the input gases. However, high growth rate usually leads to lower quality films with higher surface roughness [21]. A

low pressure is usually desirable since it leads to fewer contaminants in the film, but it must be kept high enough to allow the plasma to form.

### 2.6.2 Inductively coupled plasma etching

In inductively coupled plasma (ICP) etching, an RF (usually 13.56 MHz) current is delivered through a coil which is wrapped around the reaction chamber. This current induces a strong alternating magnetic field in the chamber, which in turn induces an alternating electric current which dissociates the input gases into a plasma, leaving reactive neutral chemical species and ions. RF power is also often applied across the electrodes in the reaction chamber, as shown in Fig. 2-10. The reactive neutral elements in the plasma are responsible for chemical etching and the ions are responsible for physical etching.

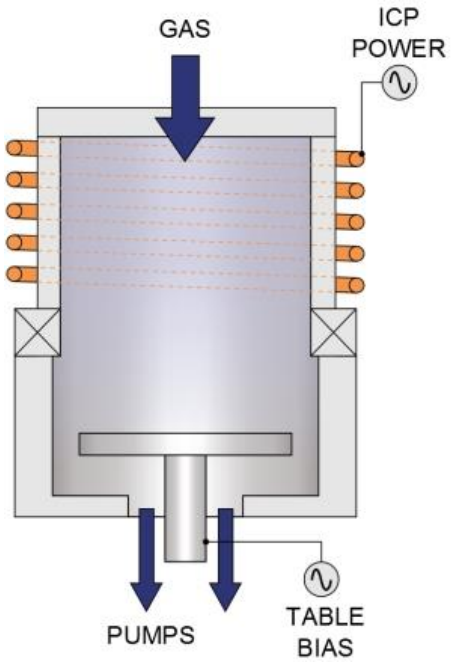


*Fig. 2-10. Schematic diagram of ICP etch system, reproduced from [20].*

Chemical etching is usually done by free radicals; that is chemical species that have incomplete bonding i.e. unpaired electrons. Typical free radicals used for chemical etching include F and $CF_3$, both of which can be formed by the reaction of free electrons in the plasma and $CF_4$, as per the reaction below:

$$e^- + CF_4 \rightarrow CF_3 + F + e^-$$

The unpaired electrons cause these free radicals to be highly reactive. As they are adsorbed onto the surface of the substrate, they react and form volatile products, which evaporate away from the surface as shown in Fig. 2-11.

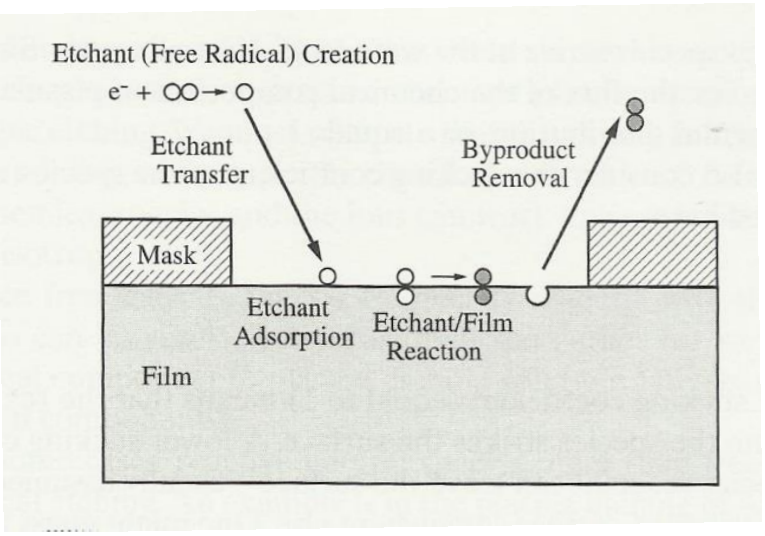


*Fig. 2-11. Processes involved in chemical etching during a plasma etch process, reproduced from [19].*

Chemical etching is an isotropic process; that is, it etches in all directions, mainly due to an isotropic arrival angle, and the low sticking coefficient between the free radical and the substrate. However, it can also be a very selective process since certain free radicals only react with particular substrates.

Physical etching is caused by the acceleration of the positive ions in the plasma towards the table, which holds the substrate. This accumulates charge on the substrate by absorbing the fast moving electrons that are accelerated towards it by the RF table power. When the ions strike the substrate, some atoms are etched from the surface. Since the ions tend to arrive normal to the surface of the substrate the etch profile is anisotropic; that is, it etches in one direction. However, this also means that there is no selectivity between materials that are etched. Fig. 2-12 shows a summary of chemical and physical etching.

The advantage of ICP etching over reactive ion etching (RIE) is that the plasma density, which is determined by the ICP power, can be controlled independently to the ion bombardment, which is determined by the table RF power. The high density plasma allows for a high ion flux, and therefore high etch rates at low pressure. This low pressure is advantageous in that there are less collisions between the ions that are bombarding the wafer, which results in an etch profile

that becomes more anisotropic because the majority of the ions are perpendicularly approaching the wafer.

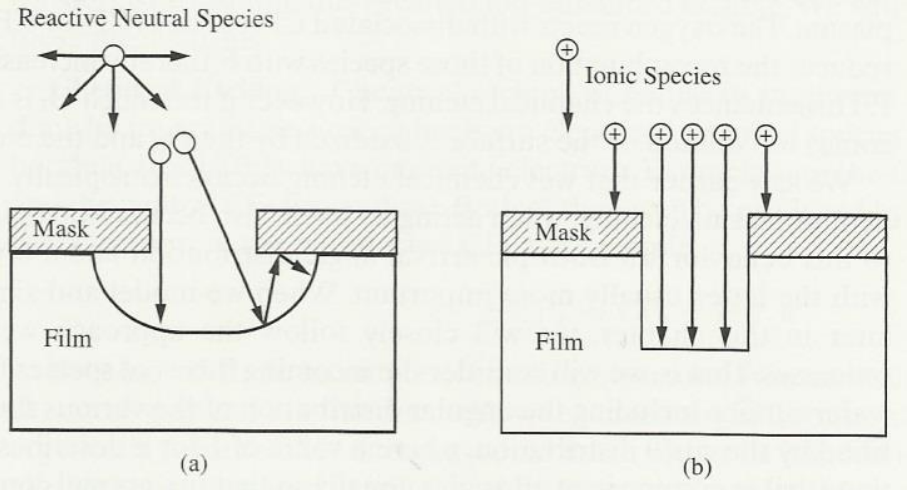


*Fig. 2-12. Fluxes of species in plasma etching, reproduced from [19]. a) Chemical, selective, isotropic etching, b) physical, non-selective anisotropic etching.*

### 2.6.3 Ion implantation

Ion implantation is a commonly used technique to introduce impurities into a semiconductor in order to alter its properties. The main advantages of ion implantation, over dopant diffusion and in-situ doped growth, are its more precise control, which leads to improved reproducibility, and lower processing temperatures [3]. An ion implantation system is shown in Fig. 2-13. The ion source contains a filament which heats a source gas to break it up into charged ions, which are subsequently accelerated by the applied extraction voltage. The analysing magnet is adjusted so that only the ions with the desired mass-charge ratio are not filtered out (e.g. $B^+$ ions). These selected ions are then accelerated in the acceleration tube to the implantation energy, and collimated with the use of apertures. The beam is then scanned over the wafer with the use of electrostatic deflection plates. The whole process happens under low pressure to avoid ion scattering caused by collisions with gas molecules.

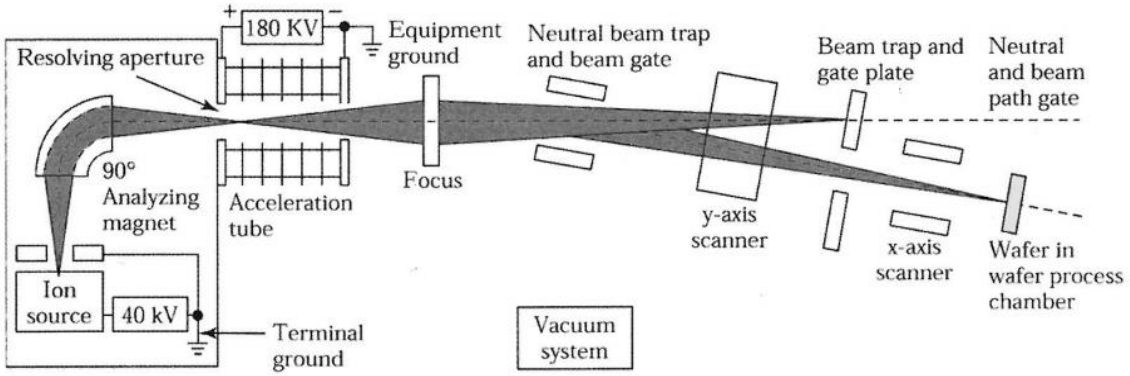


*Fig. 2-13. An ion implantation system, reproduced from [3].*

The energetic ions then lose their energy through collisions with the substrate electrons and nuclei, and come to rest within the substrate. The substrate can be selectively implanted with the use of a mask, as shown in Fig. 2-14. The average depth of the implant is controlled by the implantation energy.

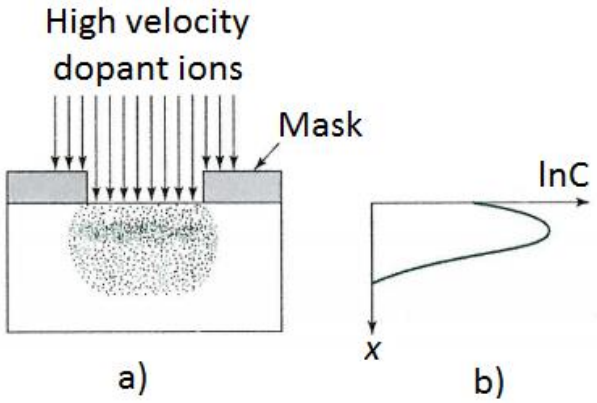


*Fig. 2-14. Diagram showing ion implantation, adapted from [3].*
*a) Ion implantation for selective introduction of dopants using a mask,*
*b) doping concentration profile as a function of depth.*

Ion implantation inevitably causes lattice damage within the substrate due to the ion collisions. Therefore, this damage should be repaired with the use of a high temperature anneal, which simultaneously activates the implanted ions. Dopant activation is a process that locates the dopants in substitutional lattice sites so that they become electrically active. Interstitial dopant atoms are not electrically active.

### 2.6.4 Rapid thermal annealing

Dopant activation is typically carried out by rapid thermal annealing (RTA). This rapid heating and cooling process electrically activates the implanted ions with minimal diffusion. The system consists of a chamber with tungsten filament lamps, which are capable of heating at a rate of approximately 100 °C/s. The cold walls of the chamber assist in rapid cooling of the wafer. The temperature is controlled either by direct thermocouple contact with the backside of the wafer, or through measuring the infra-red emission from the wafer with a pyrometer.

### 2.6.5 Metal sputtering

Metal deposition for CMOS fabrication is typically carried out by a sputtering process. Sputtering is usually preferred to evaporation, which was extensively used for earlier generations of integrated circuits (IC), for a number of reasons. These reasons include the generation of higher energy atoms, which leads to denser films with smaller grain size and better adhesion, better layer thickness uniformity, and better step coverage [22].

There are two basic types of metal sputtering; direct current (DC) and radio frequency (RF) current. DC sputtering is used only for metals, due to their electrical conductivity, and RF sputtering is typically used for dielectrics, although metals can be RF sputtered as well.

In a DC sputtering system, a negative bias is applied to the metal electrode, which then causes stray electrons to be accelerated towards the anode. If these electrons strike the argon atoms in the chamber with sufficiently high energy (greater than the argon ionisation energy, 15.7 eV), then the Ar is ionised and a plasma is created. The positively charged Ar ions are then accelerated towards the negatively biased metal target. Upon impact with the metal target the Ar ions sputter metal atoms from the surface of the target. These ejected metal atoms are then transported to the surface of the substrate where they condense to form a thin film.

RF sputtering works on the same principles but instead of a applying a negative bias to the metal target an RF bias is applied to generate the plasma.

### 2.6.6 Raman spectroscopy

When light is incident upon a molecule or crystal, it can be elastically or inelastically scattered. Elastic scattering, or Rayleigh scattering, occurs when the scattered photon has the same energy, and therefore wavelength, as the incident photon. Inelastic scattering, or Raman scattering, occurs when the scattered photon has a different energy, and therefore wavelength, to the incident photon.

This inelastic scattering process, termed the Raman effect, occurs when an incident photon interacts with the electric dipole of a material, causing a change in vibrational energy of the material, and a change in energy of the photon. This process only occurs in approximately 1 in $10^7$ photons. The normal modes of vibration of a molecule are quantised depending on the masses of the atoms in the molecule, the strength of their chemical bonds, and the atomic arrangement. Consequently, molecules have characteristic Raman spectra that can be analysed to determine many important characteristics.

The interaction between an incident photon and the electric dipole of the material excites the material to a virtual state, higher in energy than the initial state. From this virtual state, the material de-excites and emits a photon with a different energy from the incident photon. The difference in photon energy is equal, and opposite, to the difference in vibrational energy of the material.

There are two types of Raman scattering; Stokes scattering and anti-Stokes scattering. Stokes scattering occurs when the scattered photon has lower energy, and therefore longer wavelength (according to Equation 2-3), than the incident photon. Anti-Stokes scattering occurs when the scattered photon has higher energy, and therefore shorter wavelength, than the incident photon. This is shown in Fig. 2-15.

The Stokes-shifted spectrum is usually much stronger than the anti-Stokes-shifted spectrum, since at room temperature the thermal population of vibrationally excited states is low; therefore it is impossible for the majority of interactions to de-excite to a lower vibrational energy, since the initial energy level is the ground state.

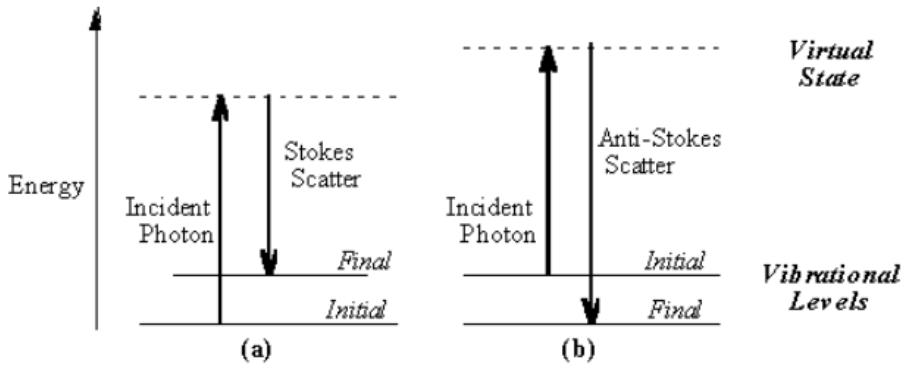


*Fig. 2-15. Energy level diagram for Raman scattering, reproduced from [23].*

*a) Stokes scattering, b) anti-Stokes scattering.*

The Raman shift, $\Delta\omega$, given in wavenumbers, can be calculated using Equation 2-8:

$$\Delta\omega = \left(\frac{1}{\lambda_0} - \frac{1}{\lambda_1}\right) \qquad \text{Equation 2-8}$$

Where $\lambda_0$ is the incident wavelength and $\lambda_1$ is the scattered wavelength. The Raman shifts of single crystal Ge and single crystal Si are 300.7 $cm^{-1}$ and 520.2 $cm^{-1}$ respectively, with a full width at half maximum (FWHM) of 5.3 $cm^{-1}$ for Ge and 4.6 $cm^{-1}$ for Si [24].

A Raman microscope, as shown in Fig. 2-16, consists of a laser with beam shaping components, an optical microscope to focus the beam on the sample, a notch filter to remove Rayleigh scattered photons, focusing optics and a grating to separate the different scattered wavelengths, and a charge coupled device (CCD) detector to detect the Raman scattered photons.

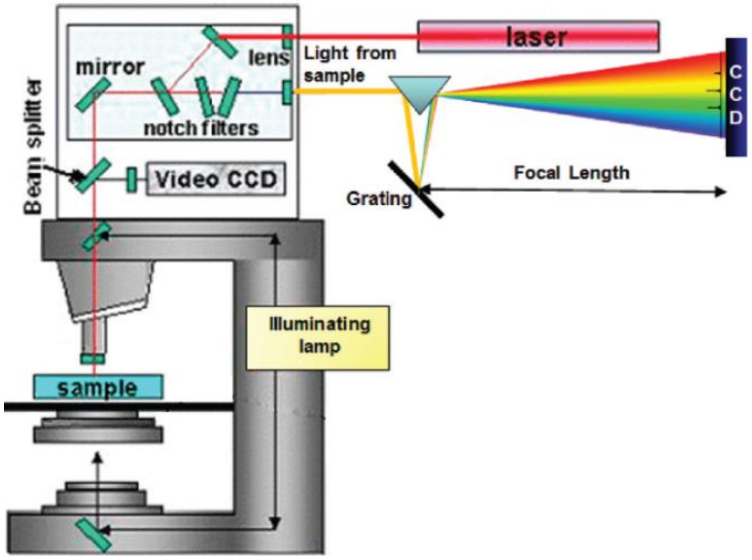


*Fig. 2-16. A Raman microscope, reproduced from [25].*

A number of different parameters can be varied in a Raman microscope. Lasers with wavelengths of 532 nm, 633 nm, and 785 nm can be used to probe varying depths of material. The penetration depth of the laser, $\delta_p$, is determined by Equation 2-9:

$$\delta_p = \frac{1}{\alpha} \qquad \text{Equation 2-9}$$

Where $\alpha$ is the absorption coefficient of the material, at the particular laser wavelength in question. The penetration depths for Si and Ge are given for various laser wavelengths in Table 2-2.

*Table 2-2. Laser penetration depths in Si and Ge at different wavelengths, calculated from data in [26].*

| | **Laser wavelength (nm)** | | |
|---|---|---|---|
| | **532** | **633** | **785** |
| Penetration depth in Ge (nm) | 17 | 53 | 179 |
| Penetration depth in Si (nm) | 980 | 2650 | 8930 |

The magnification of the optical microscope can also be varied in order to probe varying surface areas of the material. The numerical aperture, *NA*, of the lens describes the 'acceptance cone' of light that can enter or exit the lens, and is calculated by Equation 2-10:

$$NA = \mathrm{nsin}\theta \qquad \text{Equation 2-10}$$

Where $n$ is the refractive index of the medium that the lens is in and $\vartheta$ is the half-angle of the maximum cone of light that can enter or exit the lens. The minimum laser focused spot size, $d_l$, can be calculated using Equation 2-11:

$$d_l = \frac{1.22\lambda}{NA} \qquad \text{Equation 2-11}$$

Where the constant '1.22' is determined by the Rayleigh criteria to spatially resolve two adjacent objects. Table 2-3 details the minimum spot size diameter for various laser wavelengths and magnifications.

*Table 2-3. Spot size diameter for various laser wavelengths and magnifications.*
*Specifications from Leica Microsystems [27].*

| Magnification | Numerical aperture | Laser wavelength: 532 nm | Laser wavelength: 633 nm | Laser wavelength: 785 nm |
|---|---|---|---|---|
| | | Spot size diameter (µm) | | |
| x5 | 0.12 | 2.71 | 3.22 | 4.00 |
| x20 | 0.4 | 0.81 | 0.97 | 1.20 |
| x50 | 0.75 | 0.43 | 0.51 | 0.64 |

For the purposes of SiGe composition measurements using Raman spectroscopy, it is important to have a high spectral resolution in order to accurately measure sharp Ge-Ge and Si-Ge peaks. This can only be achieved with the use of a high density grating (3000 lines/mm), since the focal length of the system is fixed. This grating is only suitable for the lowest available wavelength, 532 nm. Therefore, this is the only wavelength that is utilised in this project.

### 2.6.7 Auger electron spectroscopy

Auger electron spectroscopy (AES) is a spatially resolved surface chemistry analytical technique, which can be used to gather compositional information about a sample. It measures the energy of emitted electrons which arise by the auger effect, whereby the filling of an inner-shell vacancy of an atom is accompanied by the emission of an electron from the same atom. When an electron falls from a higher energy level to a vacancy formed by the removal of a core electron, the excess energy is usually released in the form of a photon. However, sometimes this energy is transferred to another electron, which is then

emitted from the atom; this is the Auger effect. The kinetic energy of the emitted electron corresponds to the difference in energy of the initial electronic transition and the ionisation energy for the electron shell from which the electron was emitted. In this way, the auger spectrum can be used to quantify the elements present in the sample. However, the escape depth is limited to only a few nanometres due to the low energy of emitted electrons, so only surface information is gathered using this technique.

### 2.6.8 X-ray diffraction spectroscopy

X-ray diffraction spectroscopy (XRD) is a crystallographic characterisation technique that can be used to quantify, amongst other parameters, interatomic spacing, crystal orientation and crystallite size. An x-ray incident upon a sample will either be transmitted or scattered by the electrons of the atoms in the sample. If the x-rays are scattered they will constructively interfere when Bragg's law is satisfied (Equation 2-12):

$$n\lambda = 2\mathrm{d}\sin\theta \qquad \text{Equation 2-12}$$

Where $n$ is an integer, $\lambda$ is the wavelength of the x-rays, $d$ is the interatomic spacing and $\vartheta$ is the incident angle. As the incident angle and/or the detector angle is scanned, a series of characteristic peaks will emerge when Bragg's law is satisfied. These peaks correspond to different crystal orientations of the sample. The peak width, often measured by the full width at half maximum (FWHM), is a measure of the mosaicity of the sample, i.e. the degree of crystal orientation deviation from the perfect single crystal.

### 2.6.9 Atomic force microscopy

Atomic force microscopy (AFM) is a surface morphology characterisation technique, capable of measuring surface roughness on the nanometre scale. The AFM consists of a cantilever with a sharp tip that is scanned over a surface using a piezoelectric scanner. A laser, directed at the back of the cantilever, and photodetector are used to measure the deflection of the cantilever caused by the surface morphology of the sample. A simplified diagram of AFM operation is shown in Fig. 2-17.

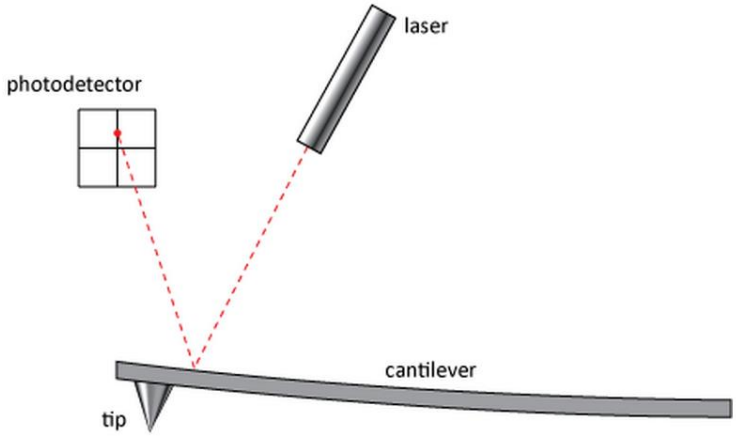


*Fig. 2-17. Simplified diagram of AFM, reproduced from [28].*

The AFM is conventionally operated in either contact or tapping mode. In contact mode, the detector monitors the changing cantilever deflection and calculates the force on the cantilever using Hooke's law. The feedback circuit then attempts to maintain a constant force and deflection point. In tapping mode, the cantilever oscillates at its resonant frequency just above the surface of the sample. The oscillation is damped when the cantilever comes close to the sample, and therefore the surface morphology can be determined by changes in the oscillation amplitude.

# Chapter 3: Literature review

This chapter will review the current state of the art in Ge/SiGe-on-Si epitaxial growth, Ge/SiGe-on-insulator (GOI/SGOI) formation, and light detection technologies at the communications wavelengths of 1.3 μm and 1.55 μm. These wavelengths have become an industry standard because 1.3 μm is the point of zero optical dispersion and 1.55 μm has the lowest optical propagation loss.

## 3.1 SiGe/Ge-on-silicon growth techniques

This section provides a brief overview of current Ge-on-Si and SiGe-on-Si growth techniques for a whole host of applications including integrated photodetectors (see section 3.3), Ge waveguides for mid-infrared (MIR) wavelengths [1-3] and sensing [4]. The difficulty in growing Ge-on-Si stems from the 4.2% mismatch in the lattice constants of the two elements (given in Appendix F of reference [5]). This means that the epitaxial Ge becomes highly strained, leading to high misfit dislocation densities at the interface of the two materials. These dislocations then propagate through the epitaxial layer as threading dislocations. Stransky-Krastanov growth of Ge-on-Si, as shown in Fig. 3-1, also causes high surface roughness which hinders planar CMOS integration [6].

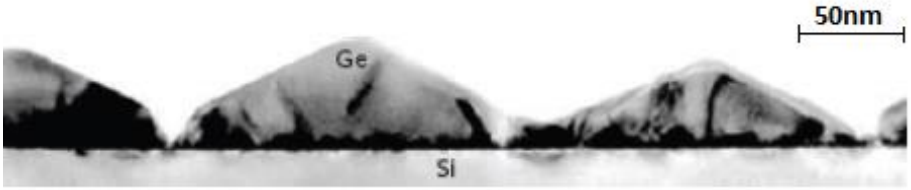


*Fig. 3-1. Stransky-Krastanov growth of Ge-on-Si at 550 °C in an ultrahigh vacuum chemical vapour deposition reactor, reproduced from [6].*

### 3.1.1 Molecular beam epitaxy

The first successful attempt at growing Ge-on-Si for use as a photodetector was demonstrated by Luryi *et al.* [7] in 1984. Their approach was to move the active detector structure away from the SiGe interface, to reduce the effects of the

dislocations, by growing a graded SiGe buffer at the interface using molecular beam epitaxy (MBE). MBE is a technique that epitaxially grows thin films by heating a solid source until it sublimates to form a gas, which is then condensed on a substrate. This process is fairly slow and requires an ultra-high vacuum to produce successful results.

The MBE growth method was further developed by Liu *et al.* [8] in 2004. They used a temperature of 370 °C to grow Ge-on-Si as this was compatible with the back-end thermal budget of CMOS semiconductor technology (restricted to less than 450 °C). This low temperature growth is an advantage of MBE, as most of the alternative approaches discussed below require temperatures of greater than 450 °C. However, using these low temperatures hinder the formation of a Ge wetting layer and idealises Stransky-Krastanov growth, which in turn leads to very high dislocation densities of approximately $4\times10^{10}$ $cm^{-2}$, some three orders of magnitude greater than some of the techniques discussed below.

In 2011, Kaschel *et al.* [9] demonstrated MBE growth of Ge in Si wells with the aim of reducing the strain in the epitaxial Ge layer. One advantage of growing Ge in wells that was cited in this paper, is that it becomes possible to melt the Ge buffer layer to reduce the dislocation density and form a smooth, relaxed Ge virtual substrate, from which the remaining Ge layer can be grown, as shown in Fig. 3-2. This is possible since the Ge is contained within the well once it has melted.

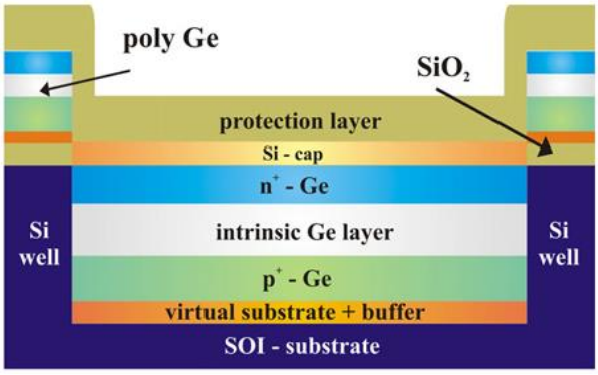


*Fig. 3-2. Schematic showing growth of Ge by MBE in Si wells, reproduced from [9].*

### 3.1.2 Chemical vapour deposition

Another method of semiconductor growth is chemical vapour deposition (CVD). In this process, a substrate is exposed to a volatile gas, or combination of gases, which react and are deposited on the surface of the substrate, usually in a raised temperature and low pressure environment. In 1981, Kuech *et al.* [10] successfully grew Ge-on-Si for the first time using this method. They obtained varying levels of crystal and surface quality from the decomposition of $GeH_4$ in a $H_2$ ambient environment, at substrate temperatures of 500-900 °C. At low temperatures (500-600 °C) they showed that at thicknesses of greater than 1-2 μm a smooth surface was formed. However, at lower thicknesses islands were formed.

In 1998, Samavedam *et al.* [11] used ultra-high vacuum chemical vapour deposition (UHVCVD) to grow graded SiGe layers to reduce the dislocation density of the pure Ge at the top of the structure. A schematic is shown in Fig. 3-3.

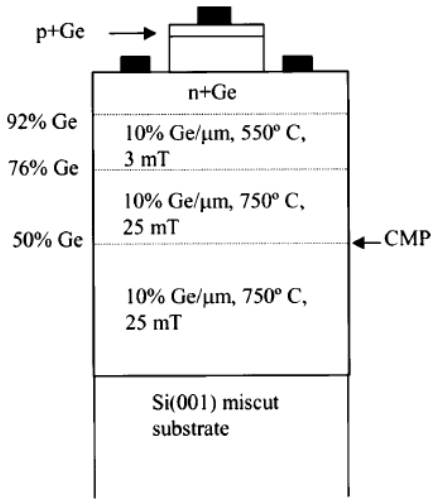


*Fig. 3-3. Schematic showing relaxed, graded SiGe buffer growth, reproduced from [11].*

They added a chemical mechanical polishing (CMP) step at the 50% Ge point to liberate dislocations, and optimise the relaxation of the graded structure. In fact, they managed to reduce the dislocation density by an order of magnitude from approximately $10^7$ per $cm^2$ to $10^6$ per $cm^2$ with this step.

It was demonstrated in 1999 by Luan *et al.* [12] and in 2000 by Colace *et al.* [13], that the threading dislocation density (TDD) could be reduced by a post

growth cyclic thermal annealing treatment. Their samples were grown using UHVCVD. With the additional thermal annealing processing step the TDD within the Ge was reduced, as shown in Table 3-1.

*Table 3-1. Dislocation densities in Ge grown on Si after cyclic thermal annealing, reproduced from [13].*

| Sample ID | A | B | C |
|---|---|---|---|
| Cyclic annealing temperatures (°C) | NA | 900/780 | 900/780 |
| Number of annealing cycles | 0 | 5 | 20 |
| Threading-dislocation density ($cm^{-2}$) | $9.5\pm0.4\times10^{8}$ | $2.7\pm0.1\times10^{7}$ | $1.6\pm0.1\times10^{7}$ |
| Mobility-lifetime product ($cm^2/V$) | $7\times10^{-8}$ | $2\times10^{-7}$ | $3\times10^{-6}$ |

All samples detailed in Table 3-1 were grown by a two-step UHVCVD process, and subsequently treated by cyclic thermal annealing. The threading dislocation densities were measured by both plan-view transmission electron microscope (TEM) and etch pit density (EPD) techniques. The mobility-lifetime products were estimated from the measured photocurrent response of metal-semiconductor-metal (MSM) photodetectors.

Another route which was initially proposed by Fama *et al.* [14] in 2002, and closely followed by Hernandez *et al.* [15] in 2003, relies on the deposition of a low temperature Ge layer followed by a high temperature Ge layer. In 2004, Hartmann *et al.* [16] further developed this method. They grew a 25 nm layer at 400 °C, followed by a layer of up to 1600 nm at temperatures between 400 °C and 750 °C, using reduced pressure chemical vapour deposition (RPCVD). The low temperature adopted for the first layer relaxes the strain in the Ge without the nucleation of any islands, and the higher temperature second step improves the layer quality and leads to a faster growth rate. They produced samples with a TDD of $9\times10^{8}$ $cm^{-2}$ and surface roughness of 0.6 nm.

One of the possible drawbacks of a high temperature annealing step, as cited by Morse *et al.* [17], is that it causes Si and Ge interdiffusion, which is particularly significant with thinner Ge films. This can cause dramatic reduction in the absorption coefficient of the material, as demonstrated by a reduction in responsivity at 1.3 μm from an expected value of 0.59 A/W to a measured value of 0.45 A/W. Nevertheless, this step does reduce the TDD to approximately

$10^7$ $cm^{-2}$, some two orders of magnitude lower than the TDD quoted by Hartmann *et al.* [16], without the annealing step.

In 2007, Loh *et al.* [18] combined the above techniques of a SiGe buffer layer with the low temperature followed by high temperature Ge growth. Using UHVCVD, they first grew a 30 nm SiGe buffer at 350 °C, followed by a 30 nm Ge layer at 350 °C and a 100 nm Ge layer at 550 °C. It was found that it was necessary for the low temperature Ge layer to be at least 30 nm in order to get a continuous and fully coalesced layer. Below this thickness, three dimensional islands formed due to the surfactant action of the atmospheric H, and the low mobility of the injected $GeH_4$ adatoms. Using this process, they measured a TDD of $6\times10^6$ $cm^{-2}$ and a surface roughness of 1.2 nm. In 2012, Chen *et al.* [19] attempted to further improve the Ge quality by adding a strained layer superlattice (SLS) into the stack as shown in Fig. 3-4.

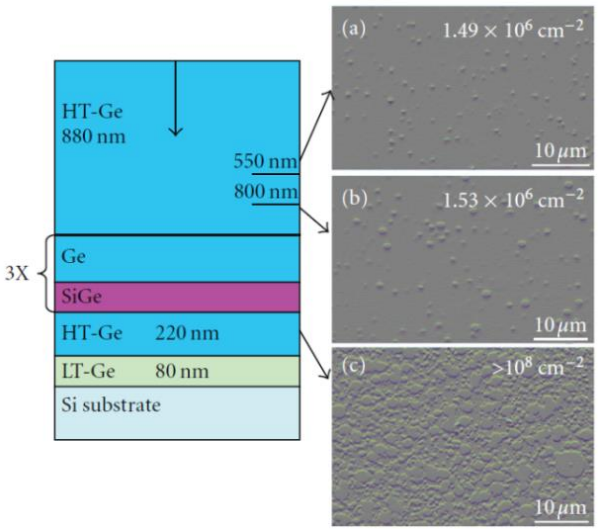


*Fig. 3-4. Schematic and optical images of a Ge-on-Si strained layer superlattice structure, reproduced from [19].*

The strained layer superlattice was engineered to reduce the strain in the top most Ge layer, which can be seen in the optical images on the right hand side of Fig. 3-4. Using this method, Chen *et al.* measured a surface roughness of less than 1 nm, and a TDD of $1.5\times10^6$ $cm^{-2}$.

Another method for reducing the TDD of epitaxial Ge-on-Si is multiple hydrogen annealing for heteroepitaxy (MHAH). This method uses multiple high temperature anneals, in an H atmosphere, throughout the growth process. In

2006, Nayfeh [20] demonstrated a TDD of $5\times10^{7}$ $cm^{-2}$, and a surface roughness of 2.5 nm using this technique.

In 2009, Osmond *et al.* [21] demonstrated extremely low dark current density values of $4.1\times10^{-2}$ $mA/cm^2$ for photodetectors grown using low energy plasma enhanced chemical vapour deposition (LEPECVD). Their process used only one growth step at a constant temperature, giving high growth rates of approximately 4 nm/sec, and a TDD of $10^{9}$ $cm^{-2}$ without thermal annealing, and $2\times10^{7}$ $cm^{-2}$ with thermal annealing. This high growth rate has the advantage of increasing the throughput, making structures grown in this way more manufacturable. They propose that roughening is suppressed by a high concentration of atomic H, acting as a surfactant.

A further possible method of epitaxial growth of Ge-on-Si is hot wire chemical vapour deposition (HWCVD). In this technique, a filament is heated to approximately 1250 °C and ultrahigh purity $GeH_4$ is introduced into the chamber. The high temperature causes the Ge and H to dissociate, resulting in Ge deposition on the substrate surface. In 2001, Mukherjee *et al.* [22] reported 98% crystalline fraction using this method, with the 2% amorphous regions confined only to the SiGe interface. Their results showed the top surface of the Ge to be atomically flat, with little or no diffusion of Si into the Ge layer.

### 3.1.3 Substrate patterning

In 2000, Langdo *et al.* [23] proposed that the TDD of Ge grown on Si could be reduced by blocking the defects using epitaxial necking.

They coated Si wafers with 120 nm of thermal $SiO_2$ before patterning with reactive ion etching (RIE), to achieve 100 nm wide wells, spaced approximately 100 nm apart. Using UHVCVD, a 25 nm Si buffer was then grown at 650 °C, followed by a Ge layer which was grown until coalescence from the neighbouring epitaxial layer overgrowth (ELO) fronts occurred. Using this technique, the Ge lacked propagating defects. However, dislocation defects did occur at the coalescing points, as shown in Fig. 3-5.

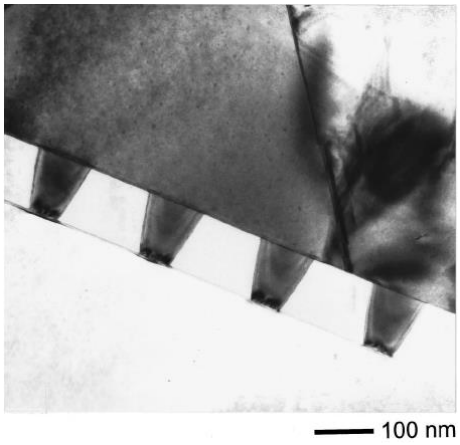


*Fig. 3-5. Thick interfacial dislocation at coalescence point of ELO growth, reproduced from [23].*

In 2006, Vanamu *et al.* [24] followed a similar path; however, they directly patterned the Si rather than an $SiO_2$ layer, as shown in Fig. 3-6. This was done using reactive ion etching (RIE) to pattern the Si, followed by CVD deposition of Ge at 600 °C.

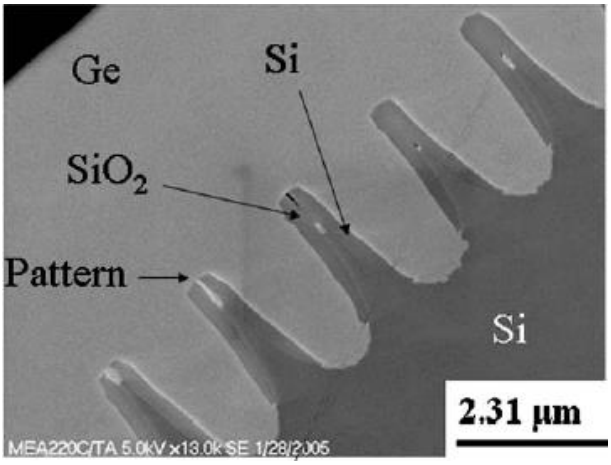


*Fig. 3-6. Cross-section SEM image of Ge on nanostructured Si substrate, reproduced from [24].*

Using this technique, they were able to grow 100% relaxed Ge with a surface roughness of approximately 2 nm, and an extremely low TDD of $5\times10^5$ $cm^{-2}$.

## 3.2 SiGe/Ge-on-insulator fabrication techniques

This section briefly describes a variety of methods for producing Ge-on-insulator (GOI) and SiGe-on-insulator (SGOI) substrates, for applications in photonics (e.g. photodetectors), electronics (e.g. MOSFETS), and lattice matching for epitaxial III-V growth [25-27].

### 3.2.1 Layer transfer using a donor wafer

The most commonly used method for producing GOI and SGOI wafers is layer transfer using a donor wafer [28-30]. This process is summarised in Fig. 3-7.

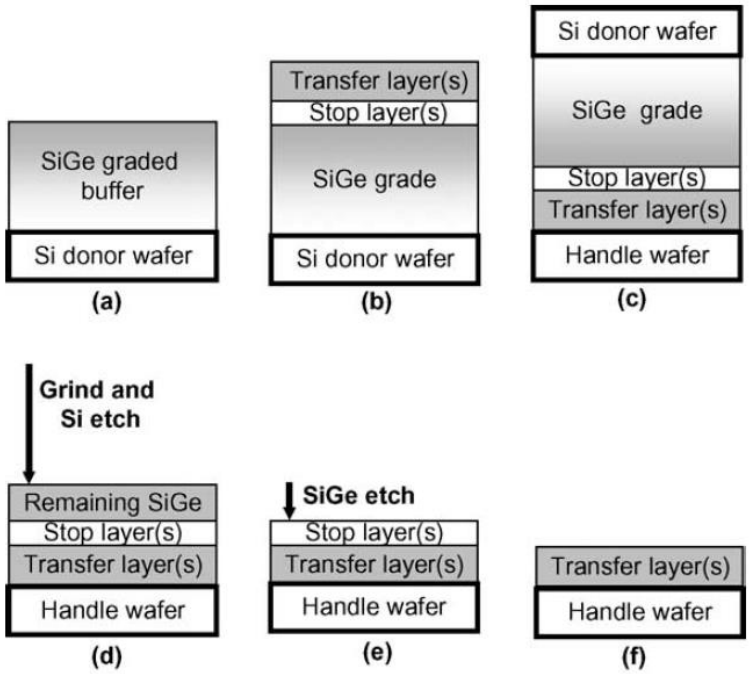


*Fig. 3-7. Layer transfer process using a donor wafer, reproduced from [28].*
*a) Growth of SiGe graded buffer layer on donor wafer, b) growth of stop and transfer layers, c) wafer bonding to wafer handle, d) backside grinding by CMP, e) selective SiGe etching to stop layer, f) removal of stop layer.*

This is similar to the SmartCut$^{TM}$ process [31], whereby an H implant at a very controlled depth is used, which acts as a splitting surface within the transfer layer on the donor wafer. The transfer layer is bonded to a handle wafer with a top $SiO_2$ layer (which becomes the buried oxide), and using a high temperature anneal, the donor wafer is removed at the splitting surface, resulting in a GOI or SGOI substrate.

This is a very well controlled process, but it is only possible to transfer a layer containing a single SiGe composition.

### 3.2.2 Ge condensation

Ge condensation is a method first proposed by King-Jien *et al.* [32] in 2005, and further investigated by Park and Choi [33] in 2007. In order to obtain high percentage Ge, Park and Choi first grew a SiGe layer with a graded Ge concentration by UHVCVD. Next, they carried out thermal oxidation in an $O_2$ atmosphere at temperatures lower than the SiGe melting point. In this oxidation process, the Ge atoms are rejected from the $SiO_2$ layers, suppressing the out-diffusion of Ge atoms, whereas the Si atoms are oxidised in the $O_2$ atmosphere. This causes the SiGe layers to merge into a uniform layer, by interdiffusion of Si and Ge atoms, until at the end of the process, nearly all of the Si atoms are oxidised, and a Ge layer remains. This process results in a very low surface roughness of 0.85 nm, and is described in Fig. 3-8.

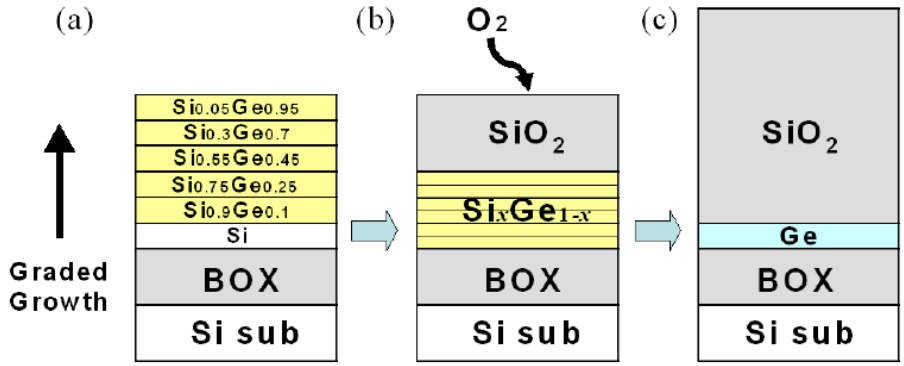


*Fig. 3-8. Graded Ge condensation growth method, reproduced from [33].*
*a) Growth of SiGe layer on SOI wafer, b) oxidation of SGOI layer, c) complete Ge condensation.*

The top $SiO_2$ layer can be easily removed with an HF etch. In order to analyse this Ge condensation process, they measured the atomic compositions of the sample before and after the condensation process, using secondary ion mass spectroscopy (SIMS), as shown in Fig. 3-9.

It can clearly be seen that after the condensation process, close to 100% Ge is achieved. The SiGe composition can be tuned by adjusting the oxidation time, but again, only a single composition per wafer can be achieved [34].

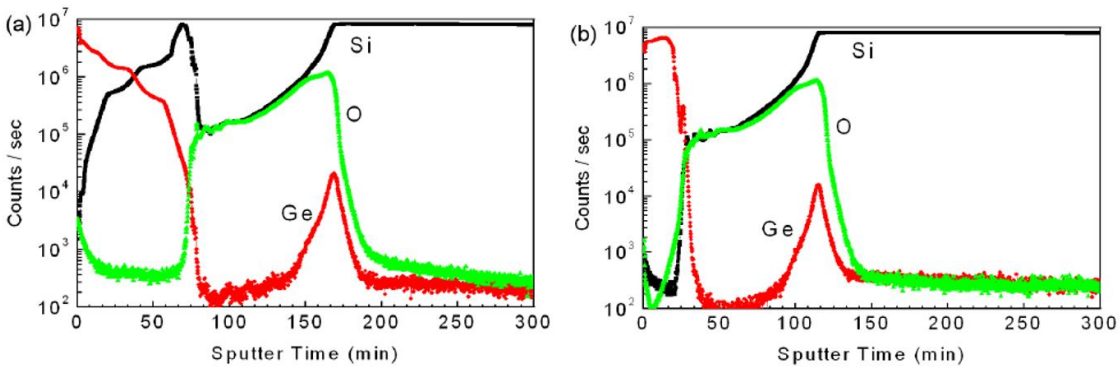


*Fig. 3-9. SIMS depth profiles of Ge condensation process, reproduced from [33].*

*a) Before oxidation of the SGOI layer, b) after oxidation of the SGOI layer.*

### 3.2.3 Lateral Ge-on-insulator growth

In 2014, Yamamoto *et al.* [35] demonstrated localised GOI fabrication using lateral growth confined within two insulating layers, as shown by the cross-section scanning electron microscope (SEM) image in Fig. 3-10a.

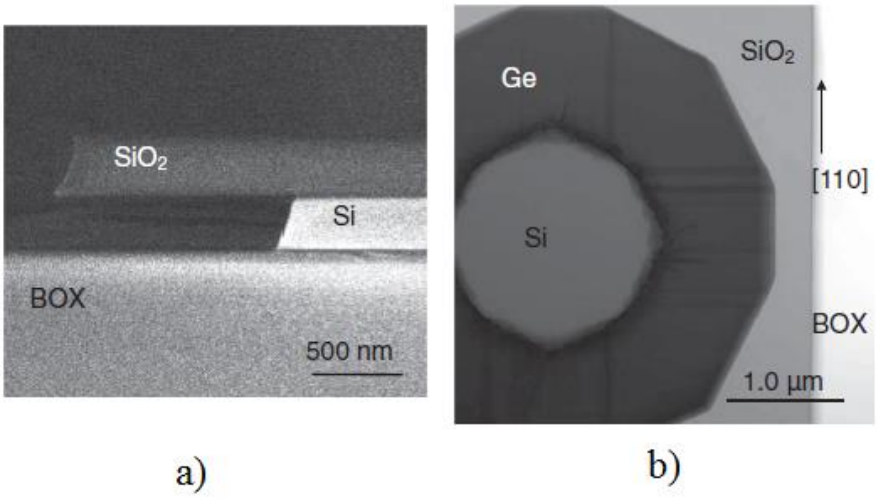


*Fig. 3-10. Lateral GOI growth, reproduced from [35].*

*a) Cross-section SEM image of the growth region prior to Ge growth, b) plan view TEM image after growth.*

They observed that most of the defects were confined to the first 150 nm from the Si core. After the initial 150 nm, defects were only observed in the [110] and [1-10] directions, as shown in Fig. 3-10b, meaning that areas of defect free Ge were realised.

### 3.2.4 Rapid melt growth

Rapid melt growth (RMG), also referred to as liquid phase epitaxy (LPE), is a technique that was invented in the 1960s [36], and further developed in the 1970s, for the fabrication of detectors [37], LEDs [38] and laser diodes [39]. The technique, originally used for III-V crystal growth, was pioneered by Liu *et al.* [40] for localised GOI growth in 2004, and has since been studied by various groups [41-45] and adapted for SGOI growth [46-52].

In this technique, a thin insulating layer is deposited on a Si substrate and patterned to open up seed windows, which will initiate the Ge recrystallisation. Next, Ge is deposited using a non-selective method, and patterned to form the desired features. This is then encapsulated using an insulating layer, and subsequently heated in a rapid thermal annealer (RTA) in order to melt the Ge. As the Ge cools down after melting it recrystallises from the Si seed, and the growth front propagates along the Ge feature. This method is plausible because Si (1414 °C) has a much higher melting point than Ge (938 °C) [5], so the Si crystal lattice remains solid at the point where the Ge becomes liquid. The defects in the Ge are blocked by the insulating layers by epitaxial necking.

In 2004, Liu *et al.* [40] first proposed RMG growth of Ge-on-Si. They sputtered Ge onto the substrate, after the first $SiO_2$ deposition, as this is a non-selective deposition process. However, as a more readily available alternative, they did also propose depositing a thin 4 nm Si layer using UHVCVD over the entire sample, before performing Ge UHVCVD. This proposed technique would avoid selective Ge growth in the Si seed windows occurring. They heated their samples to a temperature of 940 °C for 2 seconds, and allowed the chamber to cool naturally, creating single crystalline Ge films with no defects away from the Si seeds.

In 2009, Miyao *et al.* [42, 43] investigated different width strips of Ge, as shown in Fig. 3-11. They deposited 100 nm of Ge using MBE, and then heated their samples to 1000 °C for 1 second, before characterising them with an optical microscope.

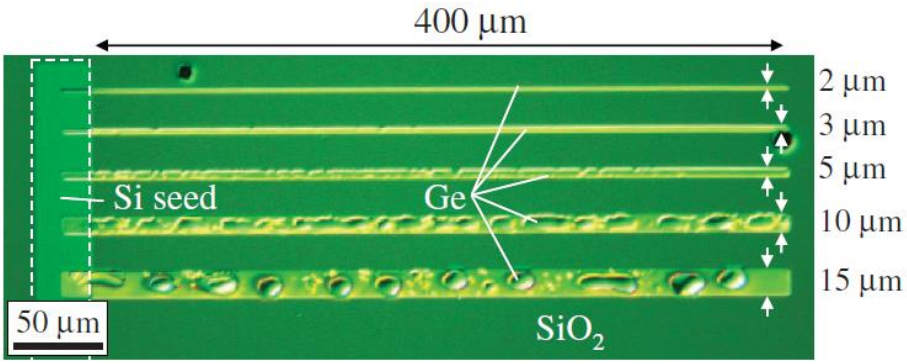


*Fig. 3-11. Optical micrograph of different width Ge strips grown by RMG, reproduced from [42].*

They discovered that up to 400 µm long single crystal Ge was formed using a strip width of 3 µm or less, but beyond 3 µm Ge agglomeration occurred and balls were formed, which the authors attribute to the high interface energy between the liquid Ge region and the oxide underlayer. They also investigated the Si fraction in the Ge strips using micro-probe Raman spectroscopy and were able to plot the Si fraction as a function of the distance from the Si seed, as shown in Fig. 3-12.

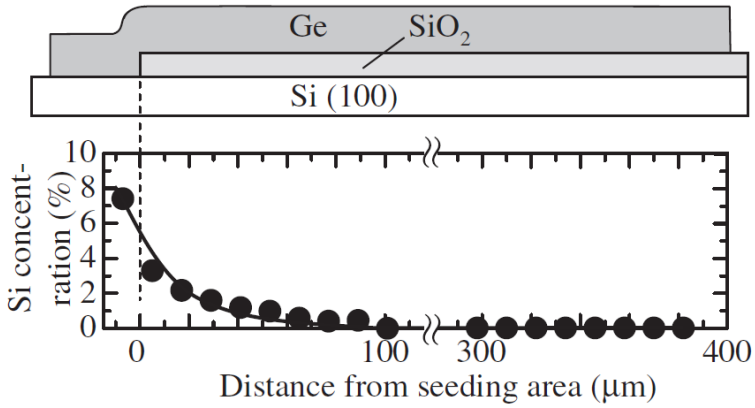


*Fig. 3-12. Si fraction obtained from Raman spectra as a function of distance from seeding area, for RMG Ge strips, reproduced from [42].*

This clearly demonstrates Si diffusion from the seed area into the Ge strips during the melting process; however, the diffusion length is limited to 70 µm for the experimental conditions they used. In another paper [43], they also investigated the growth mechanism of the Ge after melting, suggesting two possibilities. The first possibility is that the driving force to initiate the RMG is the thermal flow from the liquid Ge, through the Si substrate. The second possibility is that the spatial gradient of the Si fraction, existing near the seeding

area, is the driving force of the RMG. As the solidification temperature of the SiGe is increased with increasing Si fraction, this mechanism suggests that the melt back will be initiated in the Si rich seed area and propagate along the Ge strip, where the solidification temperature will be lower. In order to distinguish between the two mechanisms, an additional experiment with quartz substrates was carried out. In this experiment a poly-Si seed, deposited on an $SiO_2$ layer was used, as shown in Fig. 3-13.

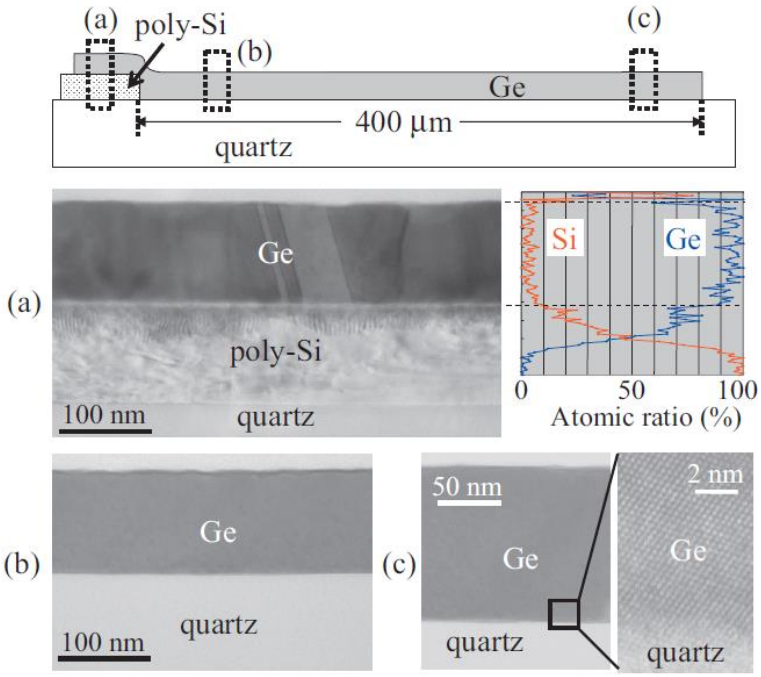


*Fig. 3-13. Ge RMG from a poly-Si seed, reproduced from [43].*
*a) Cross-section TEM image and depth distribution of Si and Ge concentrations in the seeding area, and cross-section TEM images in the region over b) 50 µm, and c) 350 µm, from the seeding area, respectively.*

Their results indicate that the single crystal Ge growth is initiated from the poly-Si seed, and propagates laterally, with the Ge having the same crystal orientation as the poly-Si seeds. Since in this case there is no substrate to allow thermal flow away from the Ge, it suggests that the SiGe mixing near the seeding area is the important force to trigger RMG. This means that beyond 70 µm, where there is no Si composition gradient, another solidification driving force should be considered. The authors propose that the latent heat of solidification at the solid-liquid interface is a key factor in explaining the melt back beyond 70 µm. In the cooling process the temperature of the solid Ge falls with time; however,

the molten Ge tends to keep a constant temperature due to the latent heat from the solidification process. Consequently, a thermal gradient is automatically formed at the growth front, which realises the continuous RMG even without a composition gradient.

In 2009, Hashimoto *et al.* [44] experimented with different insulating materials, with the aim of reducing the interface energy between the Ge and the insulating material, so that wider strips could be formed without Ge agglomeration. They discovered that when using $La_2O_3$ as the insulating material, they were able to grow 5 µm wide Ge strips, an improvement on the previously recorded 3 µm strips. However, since La is metallic it is not suitable for semiconductor devices.

More recently, Koh [46] has grown SGOI using the RMG method. Koh deposited a variety of initial SiGe compositions, but found that after the RMG process a graded composition profile was achieved, independent of the initial SiGe composition, as shown in Fig. 3-14.

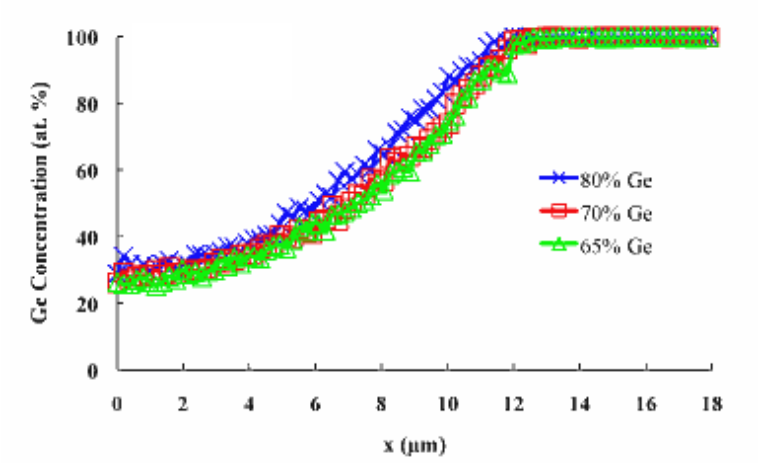


*Fig. 3-14. SiGe composition profiles, after RMG, of strips with different initial SiGe compositions, reproduced from [46].*

The graded profile is a result of preferential Si rich solid formation, with rejection of Ge into the liquid ahead of the growth front, as shown by the SiGe phase diagram in Fig. 3-15. The author proposed that once solidification commences in the seed area, the diffusion of Si from the seed is blocked, and therefore a finite amount of Si is available in the strip. The result of this is complete depletion of the Si before the end of the strip, meaning that pure Ge can be achieved.

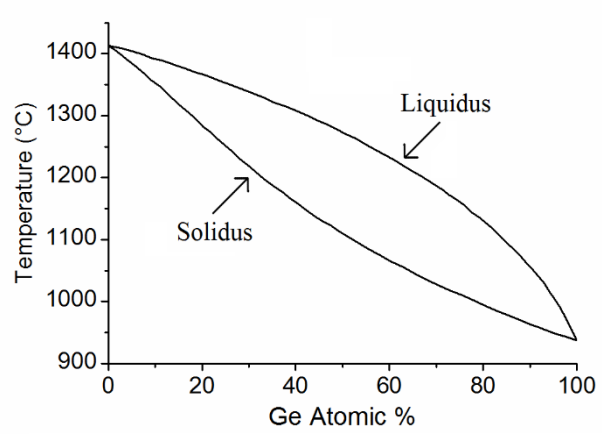


*Fig. 3-15. SiGe phase diagram – adapted from [53].*

Koh attributed the independence of initial SiGe composition to the final composition profile to the high diffusivity of both Si [54] and Ge [55] in liquid SiGe. This essentially means that for such short strip lengths (20 μm), and at a high anneal temperature (1172 °C), the Si diffusion from the seed is the significant factor.

Matsumara and Tojo *et al.* [47, 49] investigated different cooling rates and discovered that the composition profile is affected by the cooling rate (CR), and the strip length. They suggest this is due to a modification in the regrowth front propagation speed, which affects the diffusion in the liquid ahead of the regrowth front. Their data is shown in Fig. 3-16.

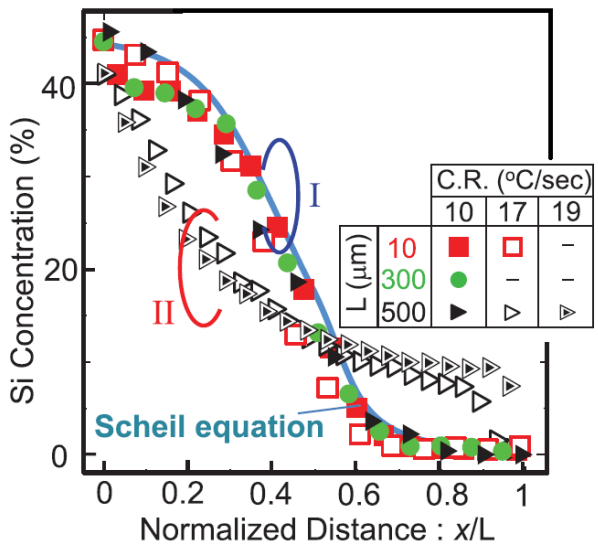


*Fig. 3-16. SiGe composition profiles for a variety of cooling rates and strip lengths, reproduced from [47].*

They also demonstrated multilayer SiGe strips using RMG.

In 2014, Bai *et al.* [50] discovered that the composition profile is independent of peak temperature anneal time, as shown in Fig. 3-17, which confirms the theory that Si diffusion from the seed is dramatically reduced once solidification has commenced, and that the initial composition is controlled by the peak anneal temperature, not the anneal time.

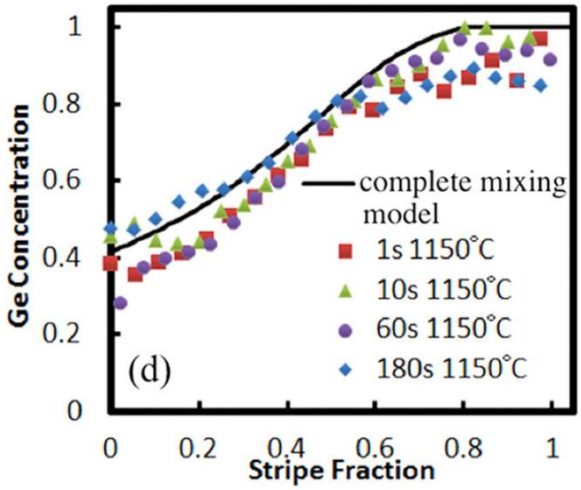


*Fig. 3-17. SiGe composition profiles after RMG at a range of anneal times, reproduced from [50].*

To date, RMG of SiGe or Ge has been demonstrated for gate all around P-MOSFETs [56, 57], P-channel finFETs [58], and waveguide integrated heterojunction photodetectors [59, 60]. These devices demonstrate the possibility of using RMG to obtain high quality, single crystal Ge layers on localised insulator islands, located on top of Si substrates or SOI substrates. This enables a bridge between electronic components and photonic components; the latter group IV based components being predominantly confined to the SOI platform [61-67]. This vision is clearly demonstrated by Going *et al.* [68] in a gate photoMOSFET, where a Ge gated NMOS phototransistor is integrated on a SOI photonics platform.

RMG demonstrates the ability to fabricate localised SGOI islands with a range of compositions. However, in order for this material to be suitable for SiGe device fabrication it is necessary to produce uniform SiGe composition profiles, which has not yet been demonstrated. This is due to the large separation between the solidus and liquidus curves of the SiGe phase diagram, which leads to the formation of graded composition profiles.

### 3.2.4.1 Summary of Ge-on-Si growth techniques

Many different Ge-on-Si growth techniques have been discussed in this section. Table 3-2 briefly summarises each of the techniques.

*Table 3-2. Summary of different Ge-on-Si growth techniques. * Substrate related defects are 0 $cm^{-2}$, but overall defect density is much higher due to dislocations at coalescence points. LT = low temperature, HT = high temperature.*

| Growth technique | Buffer layer thick. (μm) | Ge layer thick. (μm) | Growth rate (nm/s) | TDD ($cm^{-2}$) | Surface roughness (nm) | Growth temp. (°C) | Post-growth anneal | Ref. |
|---|---|---|---|---|---|---|---|---|
| LT MBE | / | 0.2 | 0.02 | $4\times10^{10}$ | 1.5 | 450 | / | [8, 69] |
| MBE with annealing | / | 1.1 | 0.5 | $1\times10^{7}$ | 3.9 | 500 | 700 °C 30 mins | [70] |
| Graded buffer UHVCVD with CMP | 10 | 1.5 | 0.8/0.24 | $2.1\times10^{6}$ | 24 | 750/550 | / | [11, 71] |
| Two step LT/HT UHVCVD with cyclic annealing | 0.03 | 1.0 | No info. | $1.6\times10^{7}$ | No info. | 350/600 | 780 °C/ 900 °C 20 cycles | [12, 72] |
| Two step LT/HT UHVCVD with SiGe buffer | 0.027 | 0.1 | 0.17 | $6\times10^{6}$ | 1.2 | 350/550 | / | [18] |
| Two step LT/HT RPCVD | 0.025 | 0.73 | 0.36 | $9\times10^{8}$ | 0.6 | 400/750 | / | [16] |
| Two step LT/HT RPCVD with annealing | 0.1 | 1.2 | No info. | $\sim10^{7}$ | No info. | 400/670 | 900 °C 100 mins | [17] |
| Two step LT/HT UHVCVD with SLS | 0.3 + SLS | 0.55 | No info. | $1.5\times10^{6}$ | 1 | 350/630 | / | [19] |
| MHAH | / | 4.5 | No info. | $5\times10^{7}$ | 2.5 | 400 | 825 °C 60 mins | [20] |
| LEPECVD | / | 1.0 | 4.8 | $\sim10^{9}$ | 0.5 | 500 | / | [21] |
| LEPECVD with cyclic annealing | / | 1.0 | 4.8 | $2\times10^{7}$ | 0.5 | 500 | 600 °C/ 780 °C 3 cycles | [21] |
| Hot Wire CVD | / | 0.17 | 0.3 | No info. | Atomically flat | 350 | / | [22] |
| UHVCVD with epitaxial necking | 0.025 | No info. | No info. | 0* | No info. | 650 | / | [23] |
| CVD with substrate patterning | / | 10 | No info. | $5\times10^{5}$ | 2 | 600 | / | [24] |
| Ge condensation | / | 0.03 | No info. | No info. | 0.84 | No info. | / | [33] |
| RMG | / | 0.1 | No info. | 0 | No info. | 940 | / | [40] |

The growth techniques detailed in this section provide a multitude of solutions for Ge-on-Si epitaxial growth. The majority of the growth techniques utilise a post growth annealing step to reduce the TDD of the Ge. One of these techniques, rapid melt growth, takes the annealing step further and actually melts the Ge in order to initiate regrowth, from a Si seed, from the liquid phase. This solution offers the lowest TDD, as shown in Table 3-2, and also demonstrates the ability to grow a range of SiGe compositions from a single initial growth step. This has the potential to be extremely useful for applications that require a range of SiGe compositions, e.g. SiGe electro-absorption modulators for wavelength division multiplexing (WDM) systems. However, to date, RMG of SiGe on Si substrates has not yielded device grade material, due to the graded composition profiles achieved. In order for the material to become suitable for device fabrication, uniform, and tuneable, SiGe composition profiles are required. A novel solution to this problem is detailed in Chapter 5.

## 3.3 Ge *p-i-n* photodetectors

The photodetector is a key component of a silicon photonics fully integrated system. Ge has become the industry material of choice for photodetector applications due to its compatibility with current CMOS fabrication techniques. It is in fact already part of the CMOS production line [73].

Historically, Ge based photodetectors had to be cooled to approximately 77 K to reduce the dark current. This however, made them very expensive and of limited use. In the past decade or so, the ability to epitaxially grow high quality Ge-on-Si, as described above, has dramatically changed this. The ability to use Si as a substrate has enabled completely new applications for Ge photodetectors that had typically been covered by compound materials such as InGaAs [6].

Many different photodetector designs have been researched to date including, but not limited to; normal incidence Ge photodetectors [7-9, 11, 13, 14, 17, 21, 69, 72, 74-78], waveguide integrated Ge vertical *p-i-n* photodetectors [60, 79-94], waveguide integrated Ge lateral *p-i-n* photodetectors [93, 95-99], waveguide integrated Ge metal-semiconductor-metal (MSM) photodetectors [100-102], Ge avalanche photodetectors [103-105] and Si defect photodetectors [106-108].

### 3.3.1 Normal incidence photodetectors

The first application for Ge-on-Si photodetectors was normal incidence (NI) photodetectors for free-space or fibre optic coupling. A typical device design is shown in Fig. 3-18; the device is illuminated from the top.

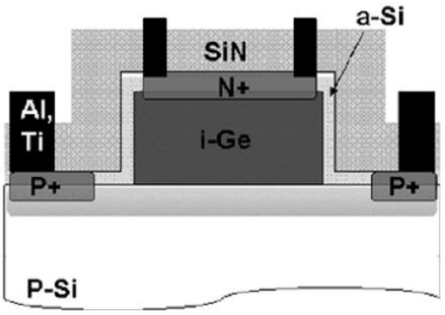


*Fig. 3-18. Cross-sectional schematic of a typical normal incidence Ge photodetector, reproduced from [17].*

The ideal photodetector characteristics are high responsivity, low dark current, and high bandwidth. However, for normal incidence photodetectors there are a number of trade-offs that make this difficult to achieve. For example, the photodetectors must have a large surface area for efficient coupling of light from an optical fibre. However, this large surface area increases the capacitance and dark current, and therefore reduces the speed and sensitivity of the device. In addition, the large distance between the anode and cathode of the device increases the carrier drift times, which also limits the speed. Therefore, in order to increase the speed of the device, it is intuitive to decrease the Ge thickness; however, this reduces the absorption efficiency of the Ge layer and results in a reduced responsivity. Devices with this design are conventionally fabricated using InGaAs due to a faster response time and a higher quantum efficiency.

Nevertheless, many different groups [7-9, 11, 13, 14, 17, 21, 69, 72, 74-78] have fabricated normal incidence Ge photodetectors with various designs and various growth techniques. The speeds of the reported devices are typically between 1 GHz and 8 GHz, with the responsivity typically between 0.2 and 0.75 A/W, and the dark current density typically in the tens of milliamps per $cm^2$.

In 2005, Liu *et al.* [76] discovered that their *p-i-n* Ge photodetectors exhibited a responsivity at 0 V that was more than 98 % of the responsivity at 2 V reverse bias, as shown in Fig. 3-19.

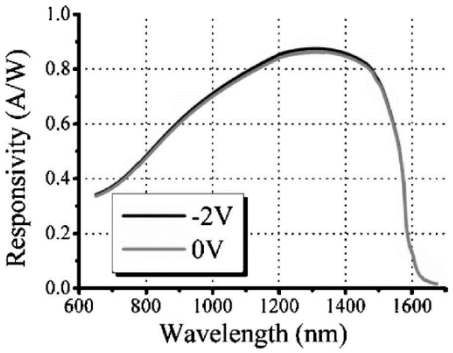


*Fig. 3-19. Responsivity of a Ge p-i-n photodetector at 0 V and 2 V reverse bias, reproduced from [76].*

This implied a large built in electric field within the intrinsic region, which was measured to be approximately 2 kV/cm. The drift velocity of electrons and holes in Ge at an electric field of 2 kV/cm are $5.1\times10^6$ cm/s and $3.0\times10^6$ cm/s respectively [109, 110]. Therefore, if the intrinsic region is sufficiently narrow, the drift transit times can be a few tens of picoseconds. Even if some carrier diffusion due to the incomplete depletion of the intrinsic region at 0 V is considered, the transit times will still be approximately 150 ps. As the minority carrier lifetime is approximately 1 ns for a Ge film with a $1.7\times10^7$ $cm^{-2}$ dislocation density, an order of magnitude larger than the carrier transit time [13], then all of the carriers will be collected before they recombine, even at 0 V, due to the high built-in electric field. Operation at zero bias is especially beneficial for achieving energy efficiency in large scale electronic-photonic integration, since the photodetectors consume almost no power at all.

A further benefit of operating a zero bias is the reduction in the dark current density (and absolute dark current), as shown in Fig. 3-20.

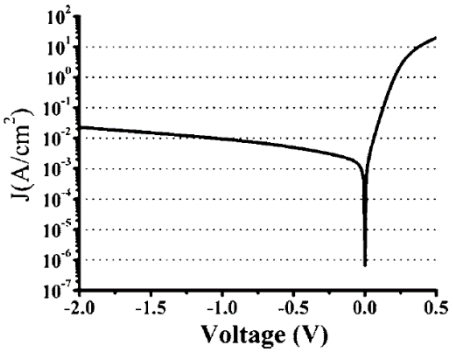


*Fig. 3-20. IV characteristics of a Ge p-i-n photodetector, reproduced from [76].*

As there is only a 2% reduction in responsivity between 2 V reverse bias and 0 V bias, but a four orders of magnitude reduction in dark current density, the signal to noise ratio is clearly going to be vastly improved at 0 V. However, one of the disadvantages of operating at 0 V is the reduction in speed, as shown in Fig. 3-21.

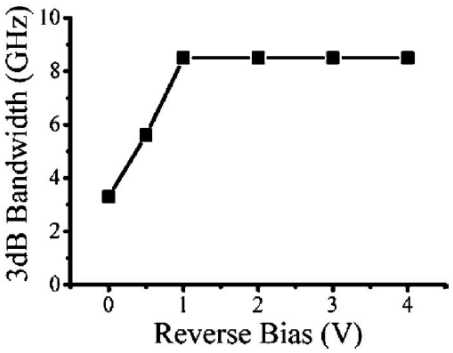


*Fig. 3-21. 3dB bandwidth of a p-i-n photodetector as a function of reverse bias, reproduced from [76].*

### 3.3.2 Waveguide integrated photodetectors

Of much greater interest for silicon photonics applications are waveguide integrated photodetectors, whereby the light is coupled into the device from a waveguide. This type of device design enables integration with other optical devices, the result of which could be very densely packed, high-bandwidth transceivers. Light is typically coupled from an external laser, through an optical fibre, onto a chip, using a grating coupler [111].

One of the main advantages of waveguide integrated designs is the improved responsivity. In normal incidence designs, the absorption length is limited by the Ge thickness, which also defines the path length and transit time for the generated carriers. With a waveguide integrated design, the absorption length can be defined independently of the Ge thickness, therefore allowing enhanced responsivity and bandwidth at low Ge thicknesses. Another major advantage of waveguide integrated designs is that the overall size can be dramatically reduced, therefore reducing the absolute dark current, for the same dark current density. Since noise is determined by the absolute dark current and not the dark current density, waveguide integrated designs also improve the detection limit or noise equivalent power (NEP) of the device.

### 3.3.2.1 Vertical devices

A vertical device has the junction defined in the vertical direction, perpendicular to the substrate surface. The bottom contact is typically formed in the Si substrate, with an intrinsic Ge absorbing region and a top contact either formed in the Ge, or in an epitaxial Si layer. If the top contact is formed in the Ge, the device is termed a heterojunction device, since the junction contacts are formed in different materials. If the top contact is formed in a Si layer, then the device is termed a dual heterojunction device, since the junction contacts are both in Si, but the junction is formed across a Ge layer. A typical waveguide integrated vertical device is shown in Fig. 3-22.

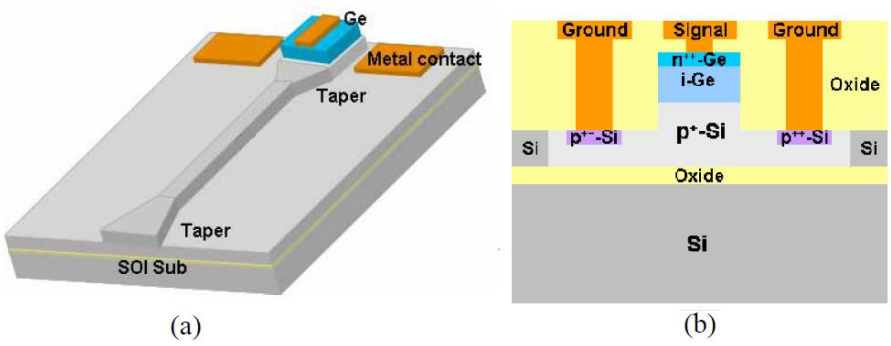


*Fig. 3-22. A typical waveguide integrated vertical Ge photodetector, reproduced from [81].*
*a) Schematic layout, b) cross-section of the Ge p-i-n photodetector.*

The first group to demonstrate waveguide coupling at 1.55 μm were Liu *et al.* [79] in 2006, with several other groups [60, 79-94] publishing data soon after. As expected, the reported devices show improved responsivity (Fig. 3-23) and larger bandwidth (Fig. 3-24) when compared to the normal incidence devices (Fig. 3-19 and Fig. 3-21 respectively).

Liao *et al.* [86, 88] observed high optical absorption in the top metal contact, which was reducing the responsivity of their devices. In order to compensate for this, they grew a thicker Ge layer and improved the responsivity of their devices from 0.6 A/W [86], to 0.95 A/W [88].

The doped regions are typically formed by ion implantation, but with this type of device design they can also be formed in-situ with Ge growth.

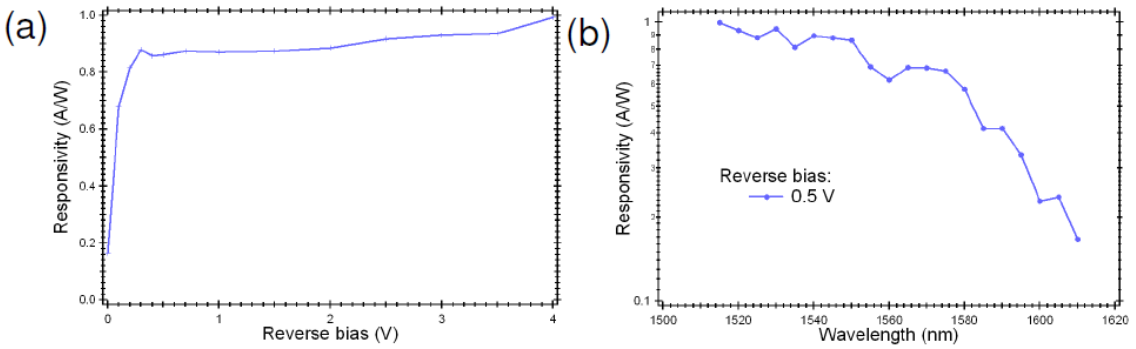


*Fig. 3-23. Responsivity of a waveguide coupled vertical Ge photodetector, reproduced from [84].*
*a) vs. reverse bias, b) vs. wavelength.*

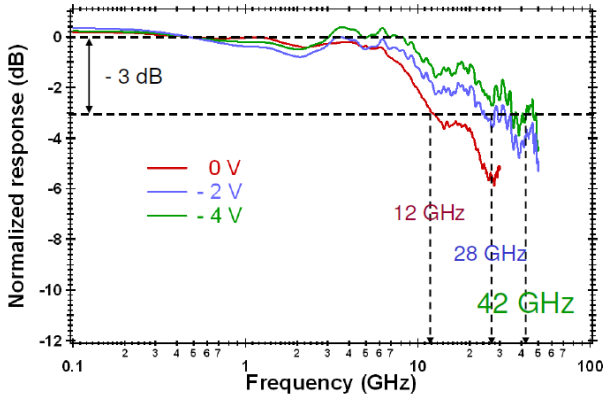


*Fig. 3-24. Normalised optical responses of a waveguide coupled vertical Ge photodetector, reproduced from [84].*

### 3.3.2.2 Lateral devices

A lateral device has the junction defined in the lateral direction, parallel to the substrate surface. Lateral device structures can be defined as homojunction structures (i.e. junction formed across a single material, e.g. Ge, with both of the metal contacts formed to Ge) [95-98], or dual heterojunction (i.e. junction formed across two materials, e.g. Ge and Si, with both of the metal contacts formed to Si) [93, 99].

Lateral device structures, as shown in Fig. 3-25, offer the added advantage over vertical device structures of being able to define the carrier path length independently to the Ge thickness, therefore making the thickness of the grown Ge less critical, and enabling planar devices to be formed without limiting control over the device design. Junction widths can be defined by ion implantation and varied, depending on the application, to prioritise either responsivity or speed

(reducing the junction width will typically increase device speed but reduce responsivity).

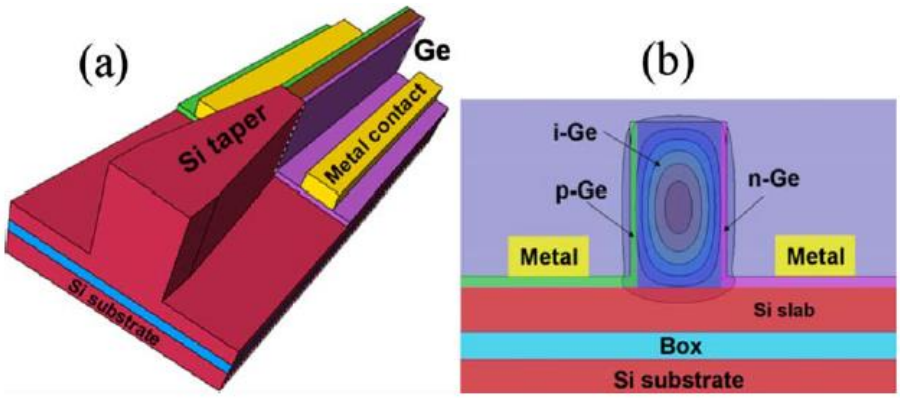


*Fig. 3-25. A typical waveguide integrated lateral Ge photodetector, reproduced from [95].*
*a) Schematic view, b) cross-section of the Ge p-i-n region.*

The first lateral device design at 1.55 μm was reported by Feng *et al.* [95] in 2009, with a responsivity as high as 1.1 A/W. In 2012, Vivien *et al.* [96] published excellent results showing open eye diagrams at 40 Gbit/s with 0 V bias, as shown in Fig. 3-26. This demonstrates the high built-in electric fields that can be achieved with these device designs.

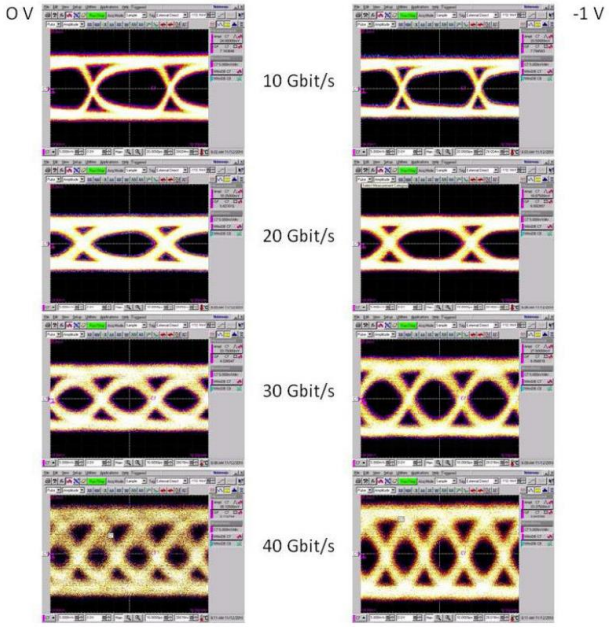


*Fig. 3-26. Eye diagrams of lateral Ge photodetectors at 10 Gbit/s, 20 Gbit/s, 30 Gbit/s and 40 Gbit/s, under 0 V bias and 1 V reverse bias, reproduced from [96].*

They estimated the optical bandwidth to be 120 GHz, with a responsivity of 0.8 A/W, but a very high dark current density of 80 A/cm$^2$. The authors propose that the bandwidth is so high due to dopant diffusion during thermal annealing, which reduces the width of the intrinsic region. A possible reason for the large dark current density can be found by considering an energy band diagram for a vertical heterojunction device structure, shown in Fig. 3-27, and a lateral homojunction device structure, shown in Fig. 3-28.

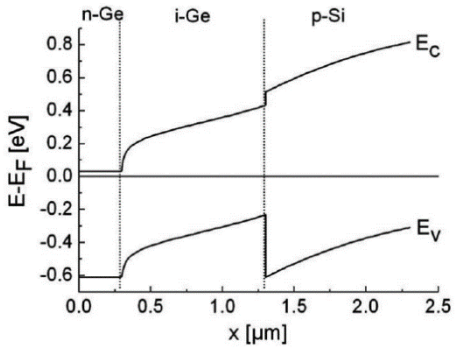


*Fig. 3-27. Band diagram for vertical heterojunction p-i-n Ge photodetector, reproduced from [21].*

In the vertical heterojunction device, it can be seen that there is a 0.36 eV barrier in the valence band between the intrinsic Ge and the *p*-type Si, which limits the minority hole current in the device.

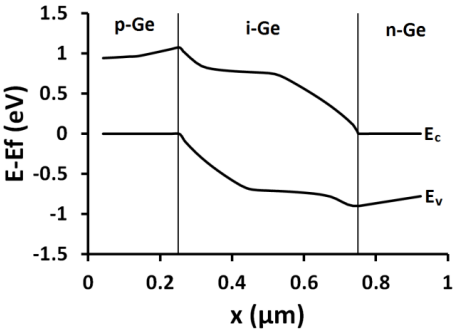


*Fig. 3-28. Band diagram for lateral homojunction p-i-n Ge photodetector.*

By comparison, there is no such barrier in the lateral homojunction device, since there is no Si/Ge heterojunction. Consequently, there is a larger dark current for the lateral homojunction devices. This is confirmed by the much lower dark currents measured for lateral dual heterojunction devices [93, 99].

### 3.3.3 Light coupling methods

In order to get light from a Si waveguide into a Ge photodetector, there are two types of coupling available: vertical coupling and butt coupling, as shown in Fig. 3-29. It is convention in the literature to refer to vertical coupling as evanescent coupling. An evanescent wave decays exponentially, without absorption, as a function of the distance from a boundary. This is not actually the case with vertical coupling since the mode couples from the Si into the Ge, due to the higher refractive index of Ge. However, in order to maintain convention, vertical coupling will be referred to as evanescent coupling throughout this thesis.

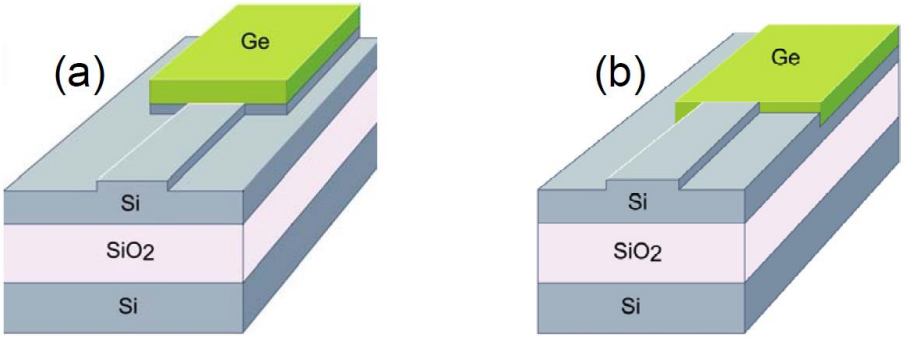


*Fig. 3-29. Methods of coupling light from a Si waveguide into a Ge photodetector, reproduced from [112].*
***a)** Evanescent coupling, b) butt coupling.*

Efficient butt coupling requires mode-matching conditions for the waveguide and detector modes, and precautions must be taken to reduce reflections from the Si-Ge interface. Evanescent coupling exploits the fact that light can be easily transferred between materials of similar refractive indices. Fig. 3-30 and Fig. 3-31 show finite difference time domain (FDTD) simulations of butt coupling and evanescent coupling respectively, carried out by Brouckaert *et al.* [112].

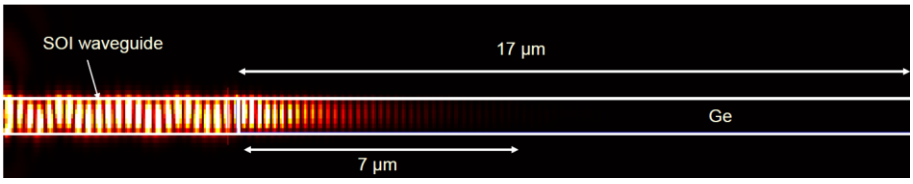


*Fig. 3-30. FDTD simulation of butt coupling into a Ge photodetector at 1.55 µm, reproduced from [112].*

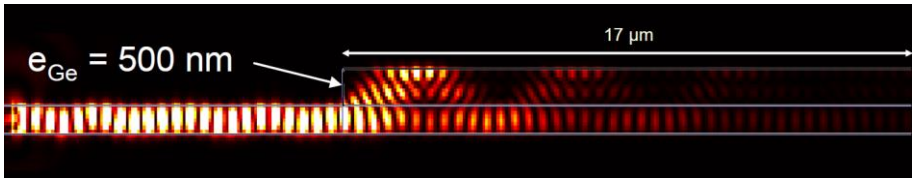


*Fig. 3-31. FDTD simulation of evanescent coupling into a Ge photodetector at 1.55 µm, reproduced from [112].*

From these simulations it can be seen that butt coupling method only requires approximately 7 µm to absorb 95% of the light, whereas evanescent coupling, with a 500 nm thick Ge layer, requires approximately 17 µm to absorb 95% of the light. The absorption length of an evanescent coupled design could be decreased with the use of a thicker Ge layer.

Although the evanescent coupling method is easier to fabricate due to the lack of an additional etch, which is required for butt coupling, the larger dimensions typically lead to a larger capacitance, and therefore, a slower device.

## 3.4 Other photodetector designs

A number of other CMOS compatible photodetector designs have been demonstrated, some of which will briefly be detailed in this section.

### 3.4.1 Metal-semiconductor-metal photodetectors

A metal-semiconductor-metal (MSM) photodetector is a photoconductive device whose conductivity is altered as it is illuminated, meaning it cannot work under zero bias. One major issue with early MSM photodetector devices was the high dark current densities. This leads to high stand-by power consumption, making them unfavourable and impractical to use.

### 3.4.2 Avalanche photodetectors

Avalanche photodetectors (APD's) can offer approximately a 5-10 dB improvement in sensitivity when compared to *p-i-n* devices, due to their internal multiplication gain [113]. Ge/Si APDs combine the optical absorption properties of Ge at 1.55 µm with the carrier multiplication properties of Si. Photogenerated electrons from the Ge layer undergo a series of impact ionisation processes in

the high electric field Si region, which consequently amplifies the photocurrent and improves the sensitivity.

APD's tend to be used for detection of low power signals with high sensitivity requirements. However, in order to achieve amplification, high, non CMOS compatible voltages, close to the diode breakdown are required, typically about 25 V reverse bias. At low voltages of less than 5 V reverse bias the photocurrent is small since the generated electrons in the Ge layer are blocked by the energy barrier at the Ge/Si hetero-interface [74].

### 3.4.3 Si defect photodetectors

When Si is bombarded with ionising radiation, defects such as interstitials and vacancies are produced in the Si crystal structure. Most of these defects rapidly reincorporate into the crystal structure, but some combine to form complex stable defects, which alter the normal band structure of the Si, and introduce mid-bandgap levels, causing a shift in absorption characteristics [114]. This can enable photodetection at wavelengths beyond the normal limit of Si photodetectors.

As with the APD's, the high bias voltages required for this type of photodetector make them unfavourable for CMOS integration.

## 3.5 Photodetectors summary

Table 3-3 compares the various photodetector designs that have been discussed in this chapter.

*Table 3-3. Performance comparison of different photodetector designs. All data is for 1 V reverse bias, unless otherwise stated. Data marked with † has been simulated by the authors. Data marked with †† indicates gain bandwidth product. LT = low temperature, HT = high temperature.*

| Responsivity (A/W) at 1.55 μm | 3 dB bandwidth (GHz) | Dark current density ($mA/cm^2$) | Dark current (nA) at 20 °C | Ge growth technique | Year | Ref. |
|---|---|---|---|---|---|---|
| **Normal incidence Ge photodetectors** | | | | | | |
| $13.3\times10^{-2}$ (1.3 μm) | 2.35 (-3 V) | 0.15 | No info. | UHVCVD with graded SiGe buffer | 1998 | [11] |
| 0.25 | 1 (-4 V) | 30 | $12\times10^{3}$ | LT/HT UHVCVD with annealing | 2000 | [13] |
| 0.2 | 1 | 20 | No info. | LT/HT UHVCVD with annealing | 2001 | [74] |
| 0.75 | 2.5 | 15 | 1200 | LT/HT UHVCVD with annealing | 2002 | [14] |
| 0.75 | 5 | No info. | No info. | LT/HT UHVCVD with annealing | 2003 | [75] |
| 0.56 | 8.5 (1.04 μm) | 10 | $2.2\times10^{3}$ | LT/HT UHVCVD with annealing | 2005 | [76] |
| 0.45 (1.31 μm) | 8.8 (-2 V) | 6.4 | 100 | LT/HT RPCVD with annealing | 2006 | [17] |
| 0.13 | 5.2 | 0.3 | 0.4 | LT/HT UHVCVD with buffer | 2007 | [77] |
| 0.4 | No info. | $4.1\times10^{-2}$ | 320 | LEPECVD with annealing | 2009 | [21] |
| 0.1 | 1.3 | 60 | No info. | LT/HT MBE with SiGe buffer | 2011 | [9] |
| 0.4 | 45.2 | 2.4 | 30 | LT/HT RPCVD | 2013 | [78] |
| **Waveguide coupled vertical device Ge photodetectors** | | | | | | |
| 1 (1.52 μm) | 4.5 | No info. | No info. | No info. | 2006 | [79] |
| 1.08 | 7.2 | 410 (-0.5 V) | 60 | LT/HT UHVCVD with annealing | 2007 | [80] |
| 0.89 (-2 V) | 31.3 (-2 V) | 51 (-2 V) | 169 (-2 V) | LT/HT growth with annealing | 2007 | [81] |
| 1 | 8.5 | No info. | 0.2 | UHVCVD with graded SiGe buffer | 2008 | [82] |
| 0.9 | 28 (-2 V) | 60 | 18 | LT/HT RPCVD with annealing | 2009 | [84] |
| 0.05 (-2 V) | 49 (-2 V) | 130 | No info. | MBE | 2009 | [85] |
| 0.56 | 24 | 625 | 120 | LT/HT UHVCVD with annealing | 2010 | [86] |
| 0.7 | 12 | 28 | 600 | LT/HT UHVCVD with annealing | 2010 | [87] |
| 0.95 | 36 | 11 | 11 | LT/HT growth with annealing | 2011 | [88] |
| 0.8 | 45 | 40 | 3 | LT/HT growth | 2011 | [89] |

| Responsivity (A/W) at 1.55 µm | 3 dB bandwidth (GHz) | Dark current density (mA/cm$^2$) | Dark current (nA) at 20 °C | Ge growth technique | Year | Ref. |
|---|---|---|---|---|---|---|
| 1 (-2 V) | 20 (-2 V) | 49 | 245 | No info. | 2013 | [90] |
| 0.75 | 30 | No info. | 3000 | No info. | 2013 | [91] |
| 0.65 | 15 | 340 | 170 | LT/HT UHVCVD with SiGe buffer | 2013 | [92] |
| 0.45 | 50 | 100 | 11 | No info. | 2014 | [93] |
| 0.4 (1.3 µm) | 15 | 250 | 100 | RMG | 2014 | [60] |
| 1 | 33 | 40 | No info. | RPCVD | 2014 | [94] |
| **Waveguide coupled lateral device Ge photodetectors** | | | | | | |
| 1.1 | 33 | $16\times10^3$ | 1300 | LT/HT growth with annealing | 2009 | [95] |
| 0.8 | 120 | $80\times10^3$ | 4000 | LT/HT RPCVD with annealing | 2012 | [96] |
| 0.9 (1.5 µm) | 10 | $10\times10^3$ | 2000 | RPCVD with annealing | 2012 | [97] |
| 0.4 | 50 | 714 | 25 | LT/HT RPCVD with annealing | 2013 | [98] |
| 1 | 20 | 43 | 3 | No info. | 2014 | [93] |
| 1.07 | 30 | No info. | 4000 | No info. | 2014 | [99] |
| **Waveguide coupled lateral device MSM photodetectors** | | | | | | |
| 1† | 14.7 (-2 V) | $394\times10^3$ | $130\times10^3$ | LT/HT RPCVD | 2007 | [100] |
| 0.3 | 25 | 400 | 100 | Bulk Ge wafer bonding | 2008 | [101] |
| No info. | 40 | $171\times10^3$ | $4\times10^3$ | Bulk Ge wafer bonding | 2009 | [102] |
| **Ge avalanche photodetectors** | | | | | | |
| 16.8 (-23 V) | 105†† (-23 V) | No info. | $20\times10^4$ (-23 V) | UHVCVD | 2010 | [103] |
| 12 (-28 V) | 310†† (-28 V) | $1.4\times10^3$ (-28 V) | $1\times10^4$ (-28 V) | LT/HT UHVCVD with graded SiGe buffer | 2012 | [104] |
| 8 (-7 V) | 190†† (-7 V) | $12.2\times10^6$ (-7 V) | $610\times10^3$ (-7 V) | LT/HT RPCVD with annealing | 2014 | [105] |
| **Si defect photodetectors** | | | | | | |
| $3\times10^{-3}$ | No info. | $2\times10^{-3}$ | 1 | / | 2005 | [106] |
| 0.8 (-21 V) | 2 | No info. | $10\times10^3$ (-21 V) | / | 2007 | [107] |
| 0.1 (-2V) | 7 (-2 V) | 1.3 (-2 V) | 0.1 | / | 2010 | [108] |

These various parameters are compared graphically in Fig. 3-32 and Fig. 3-33.

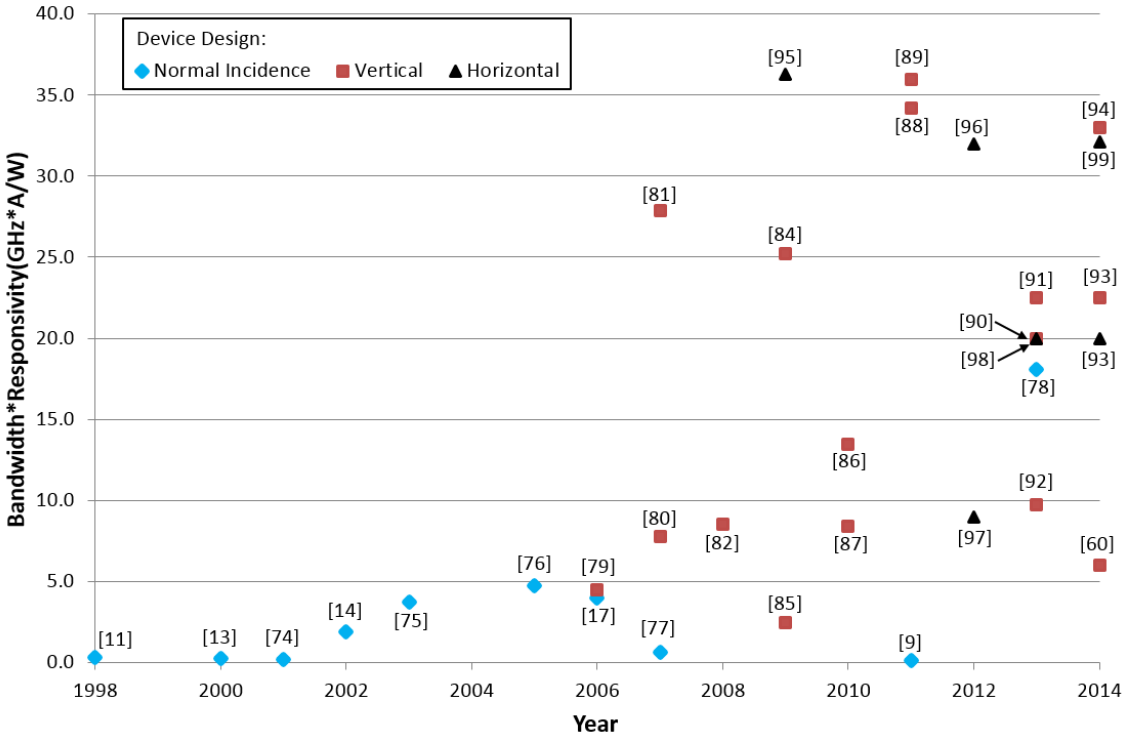


*Fig. 3-32. Ge photodetector performance comparison: Responsivity bandwidth product vs. year.*

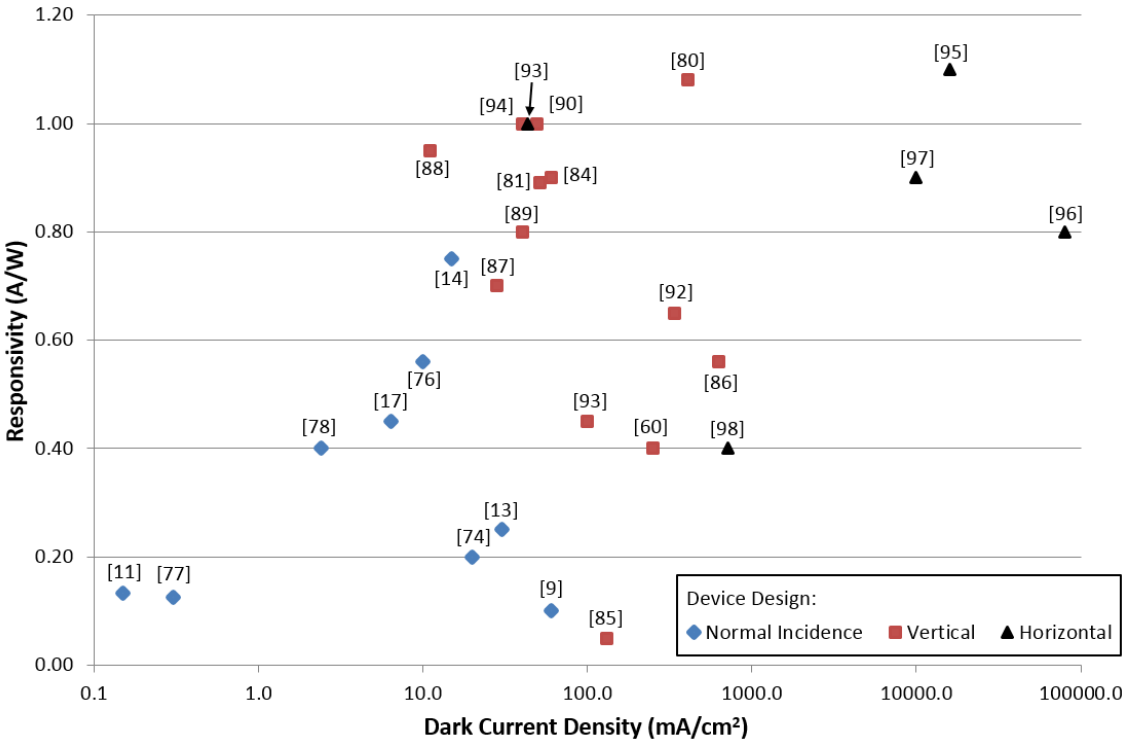


*Fig. 3-33. Ge photodetector performance comparison: Responsivity vs. dark current density.*

Normal incidence photodetectors generally have poor responsivity due to reflections at the air to Ge interface and due to the dependence on the Ge thickness. They also typically have a poor 3 dB bandwidth, due to the large dimensions of the device.

MSM photodetectors typically have undesirably high dark current densities. Avalanche photodetectors offer excellent gain bandwidth properties, but the voltages required are too high for integration with high speed, low power CMOS technology. Si defect photodetectors offer extremely low dark current, but generally a poor responsivity. The responsivity can be improved at the expense of dark current with high reverse bias voltages, but this is undesirable for power saving purposes.

Consequently, waveguide integrated *p-i-n* photodetectors are crucial for fully integrated, low power systems, because they offer excellent performance at low bias voltages.

## 3.6 Literature review conclusions

In this chapter, a number of Ge and SiGe growth methods have been discussed, with the TDD and surface roughness identified as the key figure of merit for the material quality. For SiGe growth, there is a clear need for a method that will enable multiple uniform SiGe compositions to be realised on the same substrate, for applications in areas such as WDM systems. None of the methods discussed above are able to achieve this.

RMG offers both the potential for the lowest TDD of all the growth methods discussed, and also the ability to grow a range of SiGe compositions, on insulator, using the same growth step. Therefore, this is the growth method that will be investigated in this thesis. The challenge lies in forming large areas of uniform composition SiGe, which are suitable for device fabrication.

There has been a large number of high quality Ge photodetectors reported in the literature, with a responsivity of 1.1 A/W, and a speed of 33 GHz amongst the best reported. However, there is a need for a low cost, low temperature alternative to these state-of-the-art devices. PECVD has been identified as a potential growth method that satisfies these criteria.

# Chapter 4: Ge-on-Si plasma enhanced chemical vapour deposition

## 4.1 Motivation and applications

In this chapter, a brief experimental study of hetero-epitaxial Ge-on-Si growth using plasma-enhanced chemical vapour deposition (PECVD) is reported. The main intention of this study was to identify a layer suitable for rapid melt growth (RMG) (see Chapter 5), but as an aside Ge waveguides for mid-IR wavelengths have also been fabricated. The quality of grown layers using various recipes has been examined using a range of characterisation techniques.

Crystalline and poly-crystalline Ge-on-Si has many applications in the fields of complementary metal oxide semiconductor (CMOS) electronics [1], micro-electromechanical systems (MEMS) [2], and photonics [3]. Ge has both a higher electron mobility and hole mobility than Si [1], and can therefore enable faster electronic devices, such as transistors for example [4]. Ge is aggressively etched by $H_2O_2$, or by a conventional RCA-one solution ($H_2O$:$H_2O_2$:$NH_4OH$), making it ideal for a sacrificial layer in MEMS applications. It has also become the preferred system for some near-infrared and mid-infrared photonic devices. For near infrared, Ge is crucial for the fabrication of photodetectors [5-7], quantum confined stark effect (QCSE) modulators and detectors [8-10], and Franz-Keldysh modulators [11]. When extended to mid-infrared wavelengths, Ge-on-Si becomes one of the structures of choice for waveguides [12-14] and other passive devices [15], with optical transmission all the way up to 14.7 μm [16]. In order to optimise device performance, high quality Ge growth is desirable.

A number of Ge-on-Si growth methods have been demonstrated, a summary of which can be found in Chapter 3.

The biggest challenge faced by all of these growth methods stems from the 4.2% difference between the lattice constants of Ge and Si. During epitaxial growth, this mismatch leads to the formation of stress relieving lattice dislocations that propagate to the Ge surface as threading dislocations. Such dislocations

inevitably inhibit the performance of the resulting devices. It is therefore desirable to minimise the threading dislocation density (TDD) of the epitaxial Ge-on-Si layer. Other important Ge layer characteristics which affect device performance include crystallinity (the degree to which the layer is in a preferred crystal orientation), surface roughness, and grain size.

## 4.2 Ge-on-Si growth process

Ge growth was performed in an Oxford Instruments System 100 PECVD tool on 6 inch (100) Si wafers.

### 4.2.1 Pre-growth cleaning

The pre-growth cleaning process is of the utmost importance if a high quality Ge layer is to be achieved. It is vital that the substrate has a clean surface, free from both contamination and native $SiO_2$, for the epitaxial layer to seed correctly. There are two main methods of pre-growth cleaning; an HF dip, or a high temperature bake at approximately 850 °C [17]. The HF dip removes the native $SiO_2$ from the substrate surface, and forms a passivation layer with H terminated surface bonds so that the wafer can be wet cleaned and handled in air. This enables the wafer to be transferred to the reaction chamber without the formation of a new native $SiO_2$. This passivation layer reduces the substrates reactivity with air by 13 orders of magnitude [17]. Alternatively, a high temperature bake (typically > 850 °C) desorbs the native $SiO_2$ from the substrate surface.

In this project, a dilute 20:1 ($H_2O$:HF) HF dip for 10 seconds was performed at room temperature prior to growth, because the substrate table of the PECVD tool was restricted to a maximum temperature of 400 °C.

### 4.2.2 Ge growth

An Ar diluted $GeH_4$ (10%) precursor gas is used for all experiments. Once the wafers are loaded into the chamber, there is 5 minutes stabilisation period where the wafer is heated up to the table temperature, and the gas flows and chamber pressure are stabilised, prior to plasma strike. The chamber pressure is set to 500 mT for all experiments, with an $H_2$ gas flow of 100 standard cubic

centimetres per minute (sccm), and a radio frequency (RF) power of 20 W. The temperature is varied between 250 °C and 400 °C, and the $GeH_4$ gas flow is varied between 1.5 sccm and 50 sccm, as described in Table 4-1.

*Table 4-1. Summary of process variables for the Ge PECVD growth study. For all samples the pressure is 500 mT, the RF power is 20 W, and the $H_2$ flow is 100 sccm.*

| Sample | $GeH_4$ flow (sccm) | Temperature (°C) | Thickness (nm) | Growth rate (nm/min) |
|---|---|---|---|---|
| A | 50 | 250 | 700 | 26.67 |
| B | 10 | 250 | 1250 | 4.17 |
| C | 2.5 | 250 | 980 | 1.09 |
| D | 2.5 | 400 | 922 | 1.01 |
| E | 1.5 | 400 | 625 | 0.52 |
| F – step 1 | 2.5 | 250 | ~15 | ~1.09 |
| F – step 2 | 2.5 | 400 | 960 | 1.07 |
| G – step 1 | 2.5 | 250 | ~15 | ~1.09 |
| G – step 2 | 1.5 | 400 | 690 | 0.52 |

When 20 W of RF power is applied across the two electrodes in the CVD chamber, the $GeH_4$ gas is broken down into Ge and H radicals. This has the benefit that the liberated H scavenges any oxygen in the chamber, therefore reducing oxide inclusions in the Ge film [18]. The 20 W of RF power was selected as a compromise between high growth rate and low void fraction. Poulsen *et al.* [19] observed that increasing the RF power increased the growth rate, but also increased the void fraction.

After growth was complete and the wafers had been removed from the PECVD chamber, they were cleaved to enable a sample from each wafer to be annealed. This was carried out using a rapid thermal annealer (RTA) at 600 °C, in an inert $N_2$ atmosphere, for 2 minutes, in order to realise solid phase epitaxy (SPE) if the original growth had resulted in an amorphous Ge layer [20]. Alternatively, if the original growth had resulted in a polycrystalline or single crystal layer, then the anneal step is performed with the intention of reducing the TDD of the layer, and decreasing the surface roughness. Ideally, this would be performed in a $H_2$ atmosphere as it exhibits better surface roughness reduction than $N_2$ [21], but the RTA system used in this project does not have $H_2$ as a supply gas.

## 4.3 Characterisation

The grown Ge layers have been characterised using scanning electron microscopy (SEM) imaging, transmission electron microscopy (TEM) imaging, x-ray diffraction (XRD), electron backscatter diffraction (EBSD), and atomic force microscopy (AFM) for surface roughness measurements. A summary of the results is displayed in Table 4-2 at the end of this section.

### 4.3.1 Layer imaging

The Ge-on-Si layers were firstly characterised using cross-section and plan view SEM images in order to determine if there were any voids in the layers, and to visually investigate the surfaces. Some example images are shown in Fig. 4-1.

As observed by Poulsen *et al.* [19], a high growth rate resulted in voids in the Ge layer (Fig. 4-1a). In order to remove these voids, it was necessary to decrease the growth rate below 4 nm/min. This was achieved by increasing the dilution of the $GeH_4$ precursor gas by reducing its flow firstly to 10 sccm (sample B), and then to 2.5 sccm (sample C). Fig. 4-1b, Fig. 4-1c, and Fig. 4-1d all have a growth rate of less than 1.1 nm/min, and exhibit no voids in the Ge layers.

Once a void free layer had been realised, the temperature was increased to 400 °C (sample D) in an attempt to improve the layer quality by increasing the surface adatom mobility, similar to observed with Si epitaxial growth [22]. However, it was found that at this higher temperature a large number of stress relieving pyramidal hillocks (Fig. 4-1c) were present on the layer surface. It is predicted that this higher temperature favours Stransky-Krastanov growth, resulting in the initial formation of 3D islands at the Ge-Si interface [3]. The growth rate at this temperature was reduced by a further decrease in the $GeH_4$ flow to 1.5 sccm (sample E), but this resulted in more hillocks on the sample surface.

In an attempt to reduce the number of hillocks on the layer surface, inspiration was drawn from the 2-step reduced pressure chemical vapour deposition (RPCVD) recipes developed by a number of groups [23-25]. A 2-step growth process, comprising a low temperature step followed by a high temperature step, was therefore attempted with a $GeH_4$ flow of 2.5 sccm (sample F), which

resulted in a dramatic reduction in the number of hillocks observed (Fig. 4-1d). In order to further improve the layer quality, the second growth step flow rate was again reduced to 1.5 sccm (sample G). This time the number of hillocks was reduced, which is probably due to the presence of the initial low temperature wetting layer.

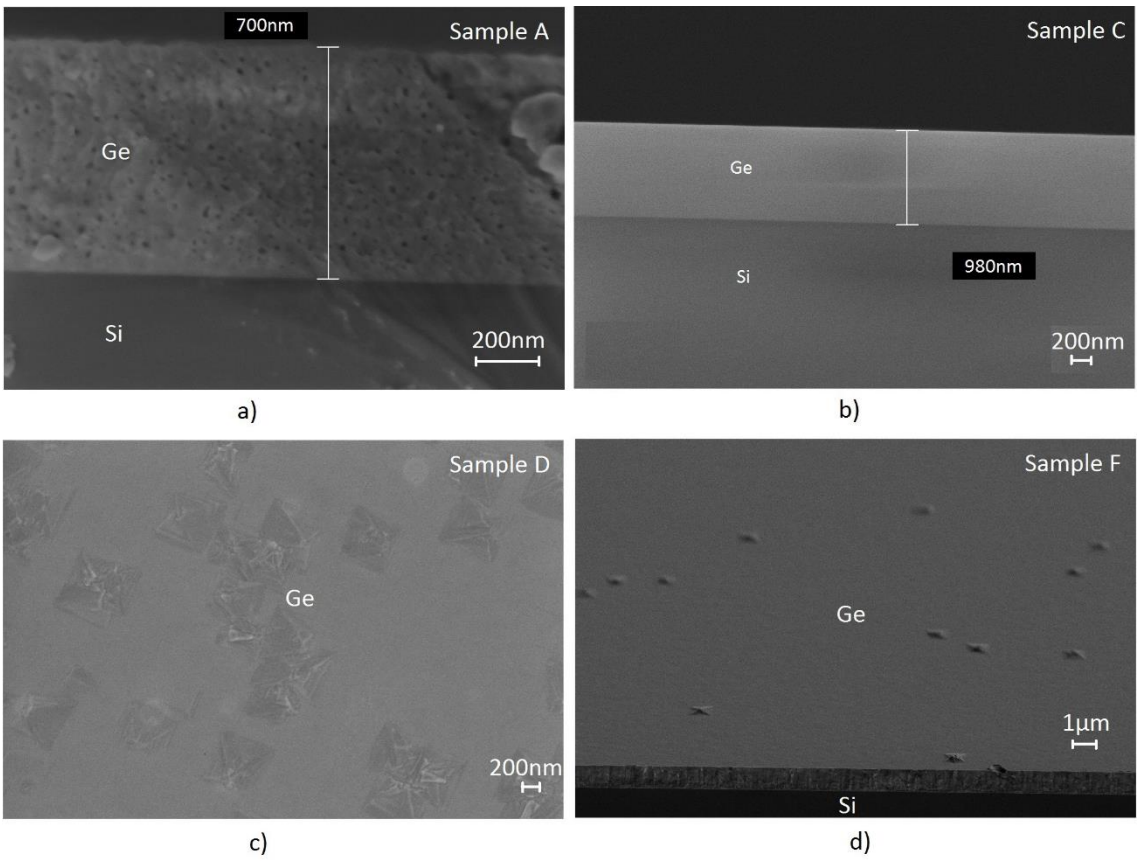


*Fig. 4-1. SEM images of PECVD Ge-on-Si.*
*a) Cross-section of sample A, showing voids in layer, b) cross-section of sample C, showing no voids in layer due to lower growth rate, c) plan view of sample D, showing high density of stress relieving pyramidal hillocks on the Ge surface, d) angled cross-section of sample F, showing a reduction in the number of stress relieving hillocks by using a 2-step growth recipe.*

#### 4.3.1.1 Transmission electron microscopy

TEM can be used to produce high resolution, atomic scale cross-section images. In order to do this, a sample has to be prepared that is transparent to electrons. This is typically a thickness of a few tens of nanometres.

In this project, TEM-ready samples were prepared by EAG Labs using an in-situ focused ion beam (FIB) lift-out technique. The samples were coated with carbon prior to milling for protection, and then imaged at 200 kV in bright-field TEM mode. Only sample G was imaged, due to the costly and laborious nature of this procedure. A few images are shown in Fig. 4-2 and Fig. 4-3.

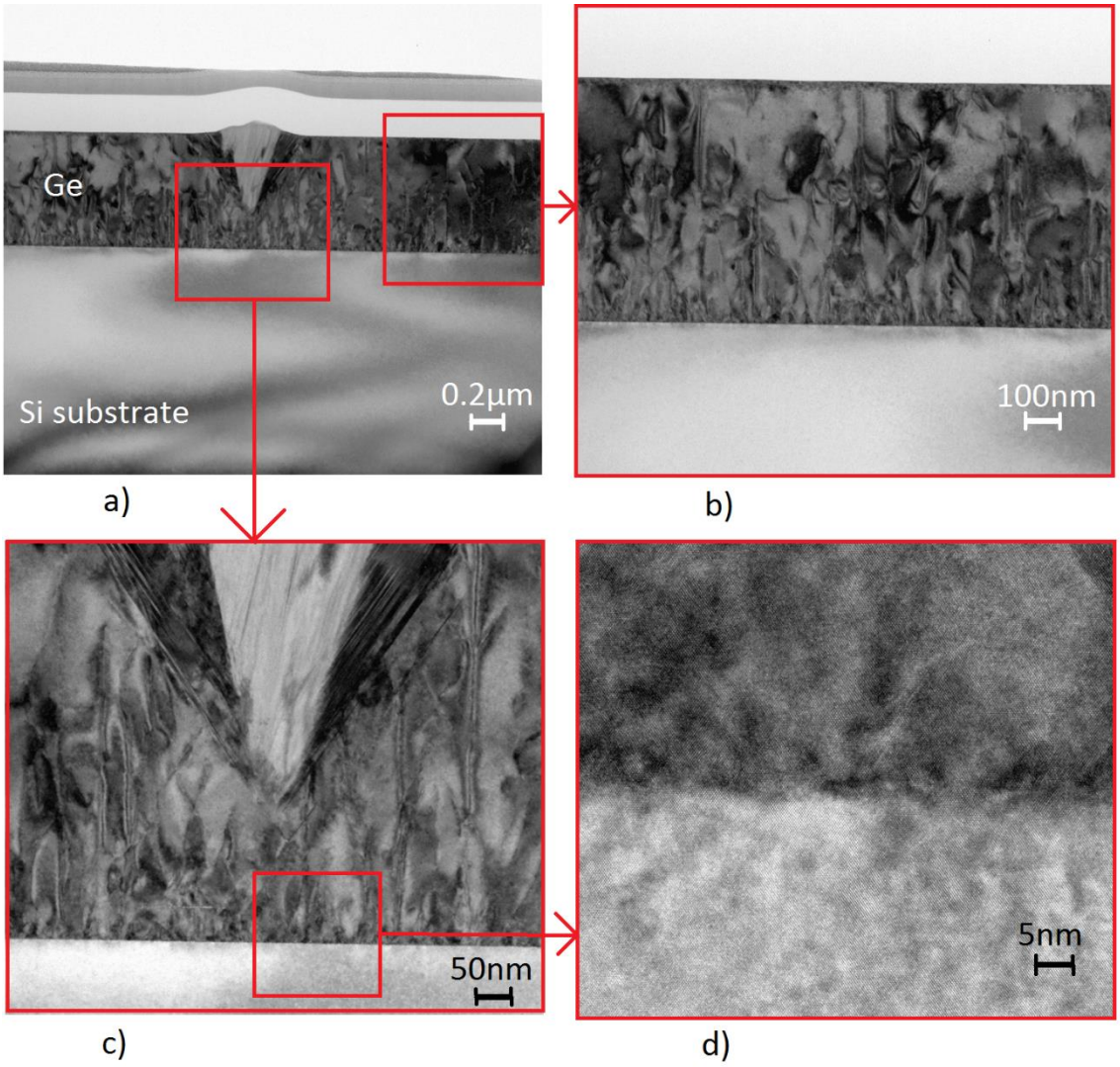


*Fig. 4-2. TEM images of sample G - as grown.*
*a) Cross-section TEM showing a stress relieving hillock, b) cross-section TEM of entire Ge layer, showing high defect density, c) cross-section TEM showing the formation of a defective area, d) high resolution cross-section TEM of the Si-Ge interface.*

These TEM images show a very high TDD, which can be calculated from Fig. 4-2b to be approximately $2x10^9$ $cm^{-2}$. Fig. 4-2a and Fig. 4-2c show a stress relieving hillock evolving from a point defect in the Ge. The resulting lighter coloured area

is polycrystalline (see Fig. 4-7), which grows at a faster rate than the bulk of the layer, thus producing a hillock on the surface. Fig. 4-2d shows a high resolution image at the Si-Ge interface, which displays a higher TDD than the bulk of the layer.

Fig. 4-3 compares the as grown sample to the annealed sample (600 °C for 2 minutes in $N_2$, at atmospheric pressure), showing a dramatic reduction in the TDD.

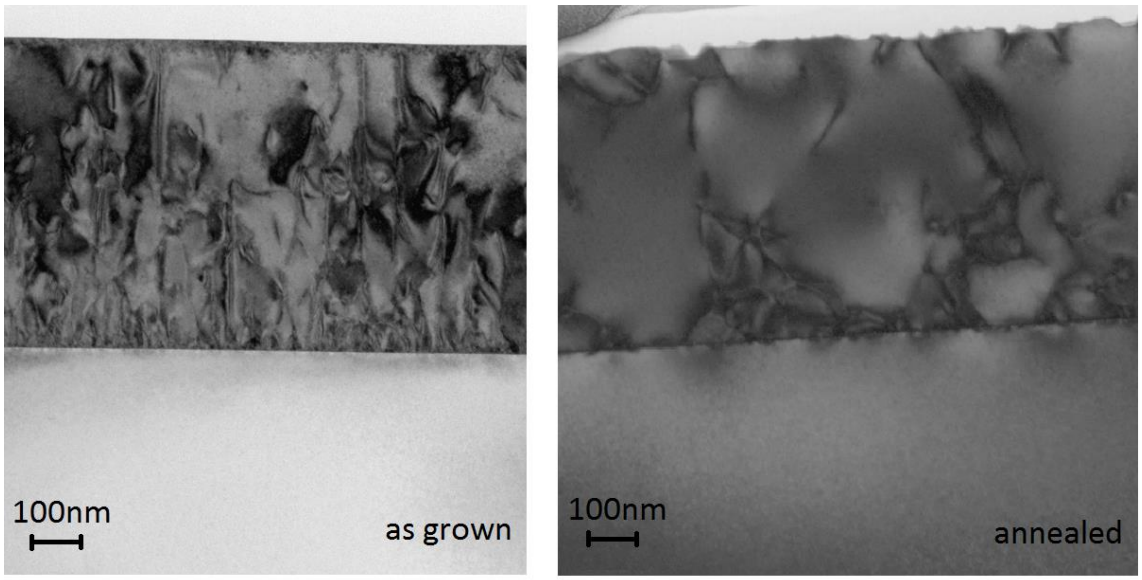


*Fig. 4-3. TEM images of sample G showing the effects of annealing. a) As grown, b) after annealing at 600 °C for 2 minutes in an $N_2$ atmosphere.*

From the image in Fig. 4-3b it can be estimated that the TDD is approximately $3.3 \times 10^8$ $cm^{-2}$. This is a reduction in TDD of approximately one order of magnitude. It is proposed that the mechanism for defect reduction is thermal-stress induced dislocation glide and annihilation [26].

### 4.3.2 Crystal properties

The crystal structure of an epitaxial layer is also very important for device performance, since features like grain boundaries affect properties such as electron mobility and hole mobility [27]. A number of different characterisation techniques have been used in order to investigate the crystal properties of the epitaxial Ge-on-Si layers.

### 4.3.2.1 X-ray diffraction

XRD is used to determine the crystal orientations of the Ge layers, and therefore establish if the grown layer is amorphous, polycrystalline or single crystal. Fig. 4-4 shows some example XRD spectra.

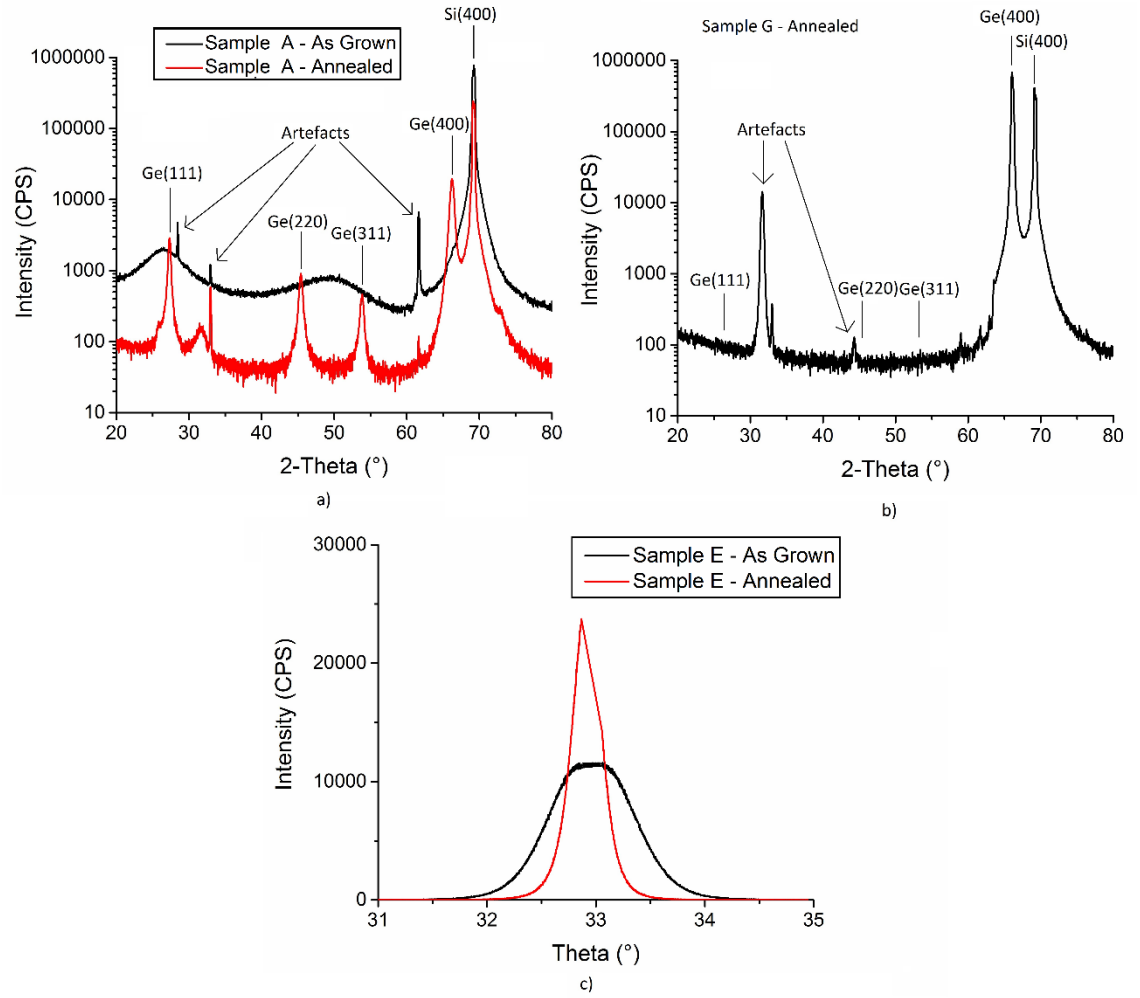


*Fig. 4-4. Theta:2-theta and rocking curve XRD spectra for various samples.*
*a) Theta:2-theta scan of sample A showing initial amorphous layer, and polycrystalline layer after annealing, b) theta:2-theta scan of sample G after annealing, showing single crystal growth, c) rocking curve measurement of sample E, showing improvement in mosaicity after annealing.*

Only sample A was found to be amorphous after initial growth (Fig. 4-4a), which is established due to the lack of any characteristic peaks at the expected 2-theta angles that satisfy Bragg's Law. Due to the various peaks of the annealed sample,

it can be concluded that SPE was realised after annealing, which resulted in a polycrystalline layer [20]. The large peak at approximately 69° is the (400) Si substrate peak that is present in all spectra.

Sample B was found to be polycrystalline, both as grown and after annealing, and samples C-G were found to be single crystal, which can be concluded due to the presence of only a single peak at approximately 66° (e.g. in Fig. 4-4b).

Rocking curve measurements can also be used as a measure of crystal quality [28]. Theta is set to the characteristic Ge (400) angle of 33°, and the sample is then rocked in very small increments. The full width at half maximum (FWHM) of the resulting peak is a measure of the mosaicity of the layer, i.e. the degree of misorientation from the perfect single crystal. As shown in Fig. 4-4c, the mosaicity is improved by thermal annealing. Values for the FWHM of the rocking curves for all samples are given in Table 4-2.

In Fig. 4-4a and Fig. 4-4b, artefacts have been marked on the graphs. It was concluded that these peaks were artefacts because upon comparison with a database of materials, no corresponding peaks could be found.

Matsuda [29] proposed that the film crystal structure is primarily governed by the diffusion length of the precursors on the growing surface. He suggested that crystallisation is promoted by high H dilutions, such as those used for samples B-G, because H adsorption on the growing surface increases the diffusion length of the adsorbed Ge, resulting in the formation of crystallites. Two other mechanisms have also been proposed for Si epitaxial growth to explain why crystallite formation is favoured by H dilution. These mechanisms may also be relevant to Ge-on-Si epitaxial growth. Tsuo *et al.* [30] proposed that H acts as an etchant that preferentially eliminates the energetically weakest configurations associated with the amorphous phase, therefore leaving only the energetically stronger crystalline phases. Shibata *et al.* [31] proposed that H atoms diffuse several layers into the growing film, which relaxes the Si–Si (or Ge-Ge) network, thereby enhancing the possibility of crystallite formation.

#### 4.3.2.2 Electron backscatter diffraction

EBSD measurements were also carried out in order to confirm the single crystal nature of the Ge layers grown using recipes C-G. Due to the nature of the

measurement, EBSD only gives information for the first few tens of nanometres of material.

An EBSD map is formed from a series of individual point measurements. At each point, if the material is crystalline, a Kikuchi pattern is formed that is characteristic, not only of the material, but also of the crystal orientation at that particular point. Fig. 4-5a shows an example Kikuchi pattern, along with a representation of the associated crystal structure (Fig. 4-5b). Each band in the Kikuchi pattern is associated with Bragg diffraction from one side of a single set of lattice planes.

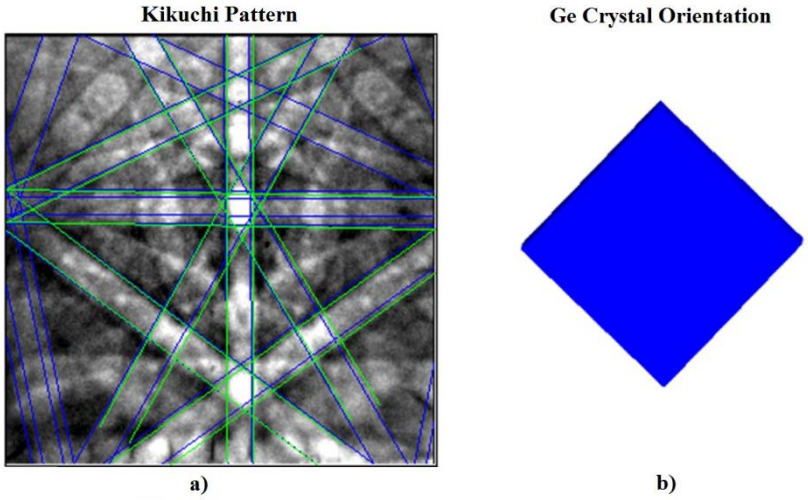


*Fig. 4-5. EBSD Kikuchi pattern of a single point, and equivalent crystal orientation – sample G, annealed.*
*a) Example Kikuchi pattern, b) equivalent crystal orientation.*

The EBSD map can be converted into a pole figure, as shown in Fig. 4-6, that illustrates stereographic projections of the orientation distribution of crystallographic lattice planes. Each pole figure illustrates a flattened semi-sphere, with each peak indicating a lattice orientation at that particular rotation and tilt. In Fig. 4-6, the pole figures are viewed at various orientations.

These pole figures confirm that the material is single crystal, due to the presence of only single points on each cubic face (i.e. the peaks are separated by a 90° rotation of the projected semi-sphere). A polycrystalline layer would result in characteristic rings that correspond to a whole range of crystal rotations.

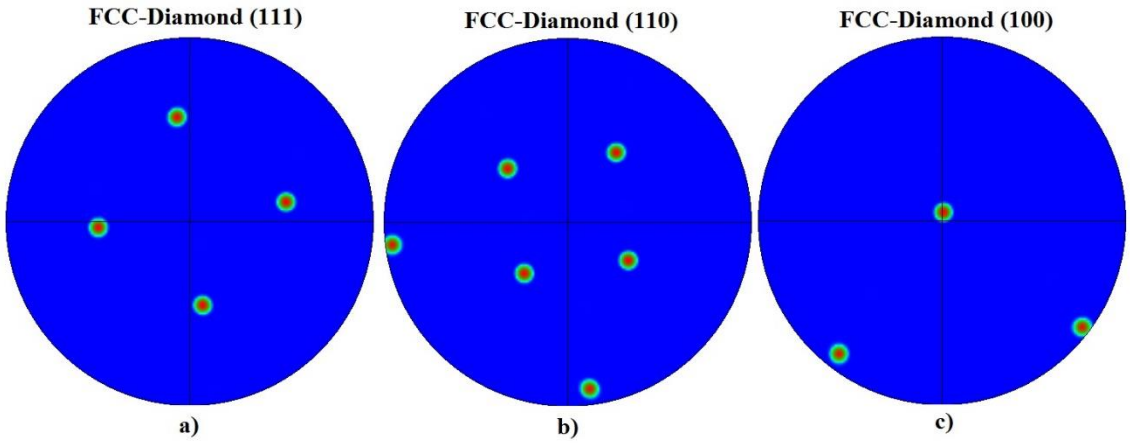


*Fig. 4-6. Pole figures in various orientations – sample G, annealed. a) Viewed from the (111) direction, b) viewed from the (110) direction, c) viewed from the (100) direction.*

#### 4.3.2.3 Transmission electron microscopy diffraction patterns

Further confirmation of the single crystal nature of the Ge layers can be gained from the TEM electron diffraction patterns shown in Fig. 4-7.

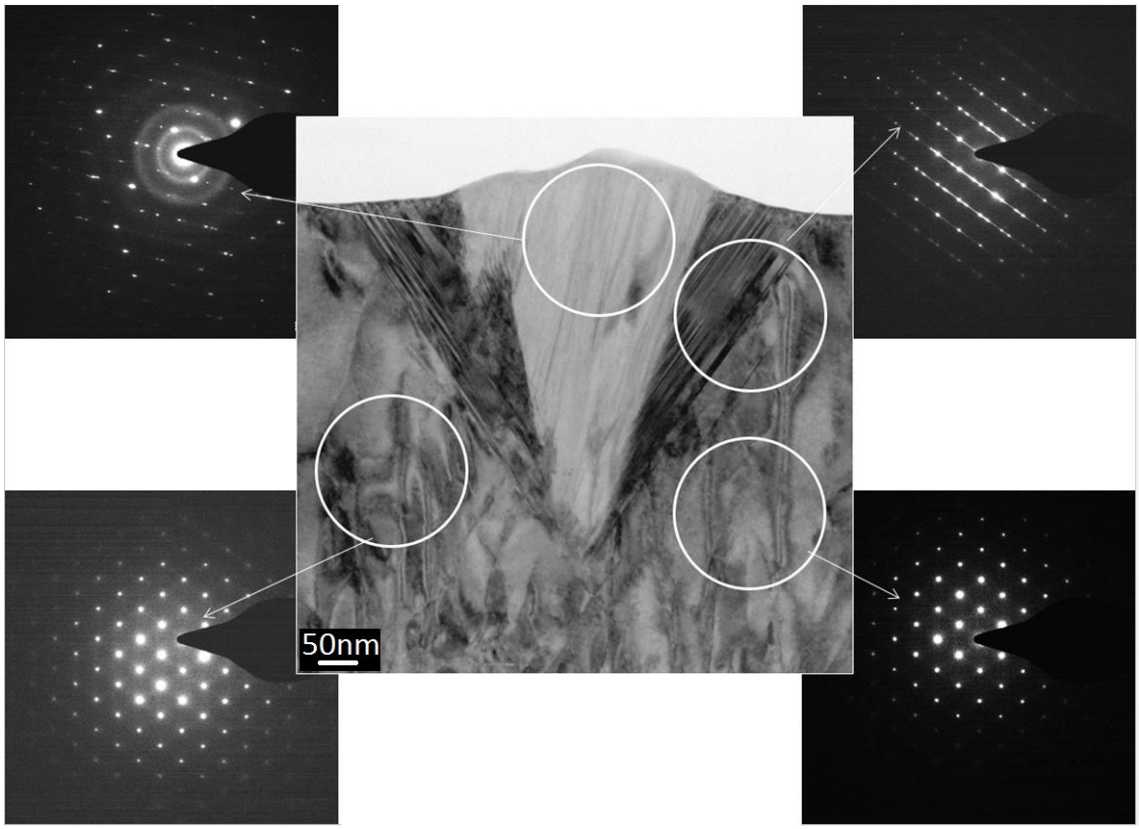


*Fig. 4-7. Electron diffraction patterns from sample G, as grown.*

The clear single electron diffraction points establish that the material is single crystal in the bulk of the material. On the contrary, the rings observed within the defective hillock establish that this region is polycrystalline.

### 4.3.3 Surface roughness

The surface roughness is another important parameter for epitaxial layers. High surface roughness is undesirable since in the majority of applications it will hinder device performance. The surface roughness was measured by AFM. The root mean square (RMS) roughness is given in Table 4-2 for all samples, and some example 3D images are shown in Fig. 4-8.

Fig. 4-8a shows a high peak surface roughness for sample C. The higher temperature growth (Fig. 4-8b) shows the formation of stress relieving pyramidal hillocks on the surface of the layer. The 2-step growth used for sample G (Fig. 4-8c) shows a dramatic reduction in the surface roughness, along with significantly fewer stress relieving hillocks. The maximum tolerable surface roughness depends on the application. For example, for waveguide applications a roughness of only a few nanometres is desirable, in order to reduce scattering losses over waveguide lengths of a few centimetres. However, for photodetector applications, the device length is only a few microns so the surface roughness tolerance becomes more relaxed.

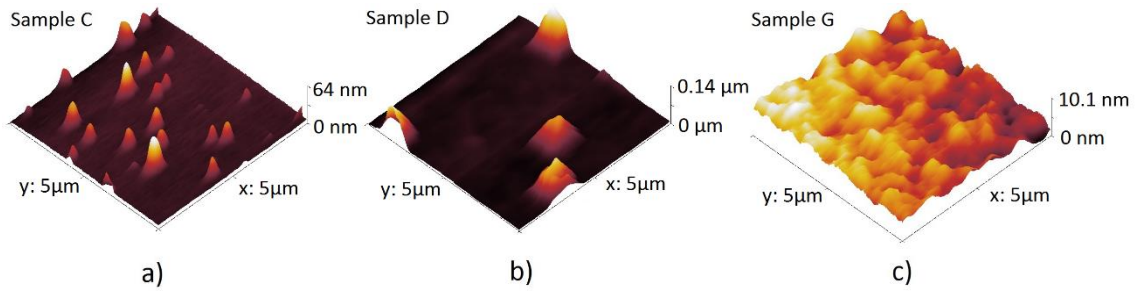


*Fig. 4-8. AFM surface roughness measurements.*
*a) Sample C (64 nm peak), b) sample D (140 nm peak), c) sample G (10.1 nm peak). All samples are annealed.*

## 4.4 Ge on patterned $SiO_2$ growth

In order to produce high quality Ge by RMG (see Chapter 5), it is necessary for the initial Ge growth to be non-selective to an $SiO_2$ surface. Therefore, growth

recipes C, F, and G (see Table 4-1) were repeated on a Si wafer with a 50 nm $SiO_2$ surface layer, which was patterned by photolithography and a 20:1 HF etch, to test for growth selectivity. After patterning the $SiO_2$ layer, the photoresist was removed by $O_2$ plasma ashing. In order to ensure a clean surface prior to epitaxial Ge growth, the wafers were subsequently cleaned in 20:1 HF for 5 seconds. A short HF dip of only 5 seconds is performed to ensure that the $SiO_2$ surface layer is not totally removed (the approximate etch rate of PECVD $SiO_2$ in 20:1 HF is 1.5 nm/s). $SiO_2$ is often used as a mask for selective Ge growth in RPCVD [32], but it is expected that in this case the presence of Ar will limit the Ge adatom surface mobility [33], so that nucleation occurs on the $SiO_2$ surface as well as the Si surface. Fig. 4-9 shows a cross-section SEM image of Ge growth on a patterned $SiO_2$ surface, using recipe C.

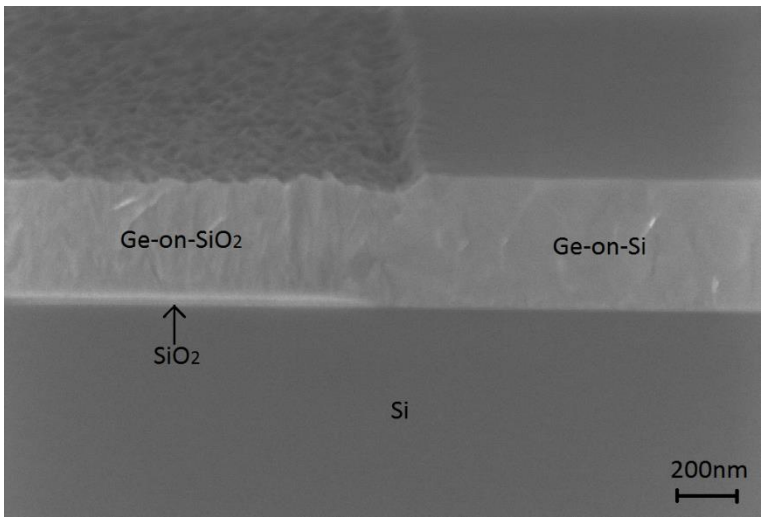


*Fig. 4-9. Cross-section SEM image of Ge grown on a patterned $SiO_2$ surface, using recipe C.*

It can clearly be seen that this is a non-selective growth recipe, therefore ensuring it is suitable for RMG. However, the Ge-on-$SiO_2$ is quite rough, but as it will be melted as part of the RMG process this may not be a problem.

It was also observed that the number of stress relieving hillocks on the Ge-on-Si surface was dramatically reduced when using a patterned $SiO_2$ layer on the Si substrate. This may be because the stress is relieved in the Ge-on-$SiO_2$ layer as an alternative relief mechanism to the formation of hillocks. In light of this observation, a patterned substrate is used for the Ge waveguides fabricated in section 4.6, below. Recipes F and G were also non-selective.

## 4.5 Ge PECVD growth summary

Table 4-2 summarises the results of the Ge PECVD growth study.

*Table 4-2. Summary of Ge PECVD characterisation results.*

| Sample | % Thickness with voids | RMS surface roughness (nm) | Ge (400) FWHM (arcsec) | TDD ($cm^{-2}$) |
|---|---|---|---|---|
| A – as grown | 98 | 5.2 | amorphous | / |
| A - annealed | 96 | 4.7 | 3175 | / |
| B – as grown | 80 | 14.0 | 2620 | / |
| B - annealed | 60 | 13.7 | 2150 | / |
| C – as grown | 0 | 10.5 | 2545 | / |
| C - annealed | 0 | 5.6 | 1115 | / |
| D – as grown | 0 | 36.6 | 2538 | / |
| D - annealed | 0 | 32.2 | 1109 | / |
| E – as grown | 0 | 26.9 | 2513 | / |
| E - annealed | 0 | 22.3 | 1089 | / |
| F – as grown | 0 | 25.4 | 2606 | / |
| F – annealed | 0 | 19.4 | 1116 | / |
| G – as grown | 0 | 4.1 | 2480 | $2.0 \times 10^{9}$ |
| G – annealed | 0 | 3.5 | 1012 | $3.3 \times 10^{8}$ |

It is clear from this table that annealing after growth is extremely beneficial for layer quality. Adequate $GeH_4$ dilution is required in order to realise a void free layer, demonstrated by the high percentage of voids observed in sample A and sample B. A 2-step low temperature, followed by high temperature growth (sample G) results in the lowest TDD and surface roughness, as well as the highest degree of crystallinity, confirmed by the lowest XRD (400) FWHM. Table 4-3, which is repeated from Chapter 3, compares this work with other Ge-on-Si growth techniques.

*Table 4-3. Comparison of Ge-on-Si growth techniques with this work. All acronyms are defined in Chapter 3. Underlined data represents this work.*

| Growth technique | Buffer layer thick. (μm) | Ge layer thick. (μm) | Growth rate (nm/s) | TDD ($cm^{-2}$) | Surface roughness (nm) | Growth temp. (°C) | Post-growth anneal | Ref. |
|---|---|---|---|---|---|---|---|---|
| Two step LT/HT PECVD (this work) | / | 0.69 | 0.009 | $3.3\times10^{8}$ | 3.5 | 250/400 | 600 °C 2 mins | / |
| LT MBE | / | 0.2 | 0.02 | $4\times10^{10}$ | 1.5 | 450 | / | [34, 35] |
| MBE with annealing | / | 1.1 | 0.5 | $1\times10^{7}$ | 3.9 | 500 | 700 °C 30 mins | [36] |
| Graded buffer UHVCVD with CMP | 10 | 1.5 | 0.8/0.24 | $2.1\times10^{6}$ | 24 | 750/550 | / | [37, 38] |
| Two step LT/HT UHVCVD with cyclic annealing | 0.03 | 1.0 | No info. | $1.6\times10^{7}$ | No info. | 350/600 | 780 °C/ 900 °C 20 cycles | [39, 40] |
| Two step LT/HT UHVCVD with SiGe buffer | 0.027 | 0.1 | 0.17 | $6\times10^{6}$ | 1.2 | 350/550 | / | [41] |
| Two step LT/HT RPCVD | 0.025 | 0.73 | 0.36 | $9\times10^{8}$ | 0.6 | 400/750 | / | [25] |
| Two step LT/HT RPCVD with annealing | 0.1 | 1.2 | No info. | $\sim10^{7}$ | No info. | 400/670 | 900 °C 100 mins | [42] |
| Two step LT/HT UHVCVD with SLS | 0.3 + SLS | 0.55 | No info. | $1.5\times10^{6}$ | 1 | 350/630 | / | [43] |
| MHAH | / | 4.5 | No info. | $5\times10^{7}$ | 2.5 | 400 | 825 °C 60 mins | [44] |
| LEPECVD | / | 1.0 | 4.8 | $\sim10^{9}$ | 0.5 | 500 | / | [45] |
| LEPECVD with cyclic annealing | / | 1.0 | 4.8 | $2\times10^{7}$ | 0.5 | 500 | 600 °C/ 780 °C 3 cycles | [45] |
| Hot Wire CVD | / | 0.17 | 0.3 | No info. | Atomically flat | 350 | / | [46] |
| CVD with substrate patterning | / | 10 | No info. | $5\times10^{5}$ | 2 | 600 | / | [47] |
| Ge condensation | / | 0.03 | No info. | No info. | 0.84 | No info. | / | [48] |
| RMG | / | 0.1 | No info. | 0 | No info. | 940 | / | [49] |

## 4.6 Ge-on-Si waveguides for mid-IR wavelengths

As described above, Ge-on-Si is an ideal candidate for mid-IR silicon photonics applications as it is transparent in the wavelength range 1.9 μm to 14.7 μm [16]. In order to fabricate Ge-on-Si waveguides, a Ge etch study was firstly carried out in order to obtain straight and smooth sidewalls for the waveguides, to minimise optical losses.

### 4.6.1 Ge etch study

The first attempts at a Ge etch were carried out using reactive ion etching (RIE) with $SF_6$ and $O_2$ as the etching gases [50]. The $SF_6$ gas flow was fixed at 36 sccm and the temperature was fixed at 15 °C. The RF power, pressure and $O_2$ gas flow were varied, as per the parameters in Table 4-4. Minitab software [51] was used to generate a box-behnken [52] design of 15 samples. This type of design avoids the need to study all 27 possible variations of the 3 parameters. The resist used was S1813. The Ge was grown on a thin $SiO_2$ layer, which acts as an etch stop.

*Table 4-4. RIE Ge etch study parameters and results.*

| Wafer no. | Pressure (mT) | RF power (W) | % $O_2$ flow | Undercut (nm) | Sidewall angle (°) |
|---|---|---|---|---|---|
| 1 | 45 | 100 | 25 | 275 | 86 |
| 2 | 30 | 100 | 18 | 215 | 104 |
| 3 | 30 | 100 | 18 | 215 | 104 |
| 4 | 30 | 100 | 18 | 215 | 104 |
| 5 | 45 | 150 | 18 | 416 | 130 |
| 6 | 30 | 150 | 10 | 231 | 109 |
| 7 | 30 | 150 | 25 | 346 | 106 |
| 8 | 15 | 50 | 18 | 130 | 65 |
| 9 | 30 | 50 | 25 | 205 | 55 |
| 10 | 45 | 50 | 18 | 220 | 73 |
| 11 | 30 | 50 | 10 | 165 | 76 |
| 12 | 15 | 100 | 10 | 144 | 68 |
| 13 | 15 | 100 | 25 | 120 | 72 |
| 14 | 15 | 150 | 18 | 100 | 77 |
| 15 | 45 | 100 | 10 | 225 | 123 |

Fig. 4-10 shows an example SEM, and demonstrates the undercut and sidewall angle measurements. The ideal case is 90° sidewall angle, and 0 nm undercut. This way the etched Ge dimensions will match the lithography.

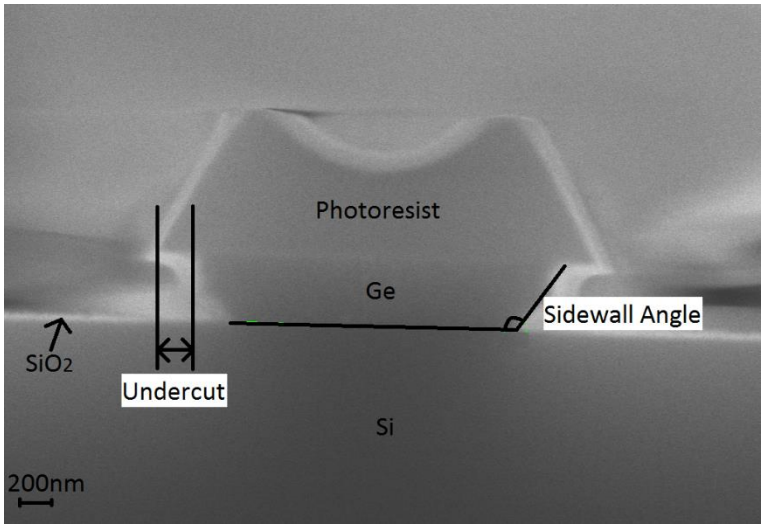


*Fig. 4-10. SEM image of Ge etch, showing undercut and sidewall angle measurements.*

The results of the etch study detailed in Table 4-4 are displayed in graphical form in Fig. 4-11 and Fig. 4-12.

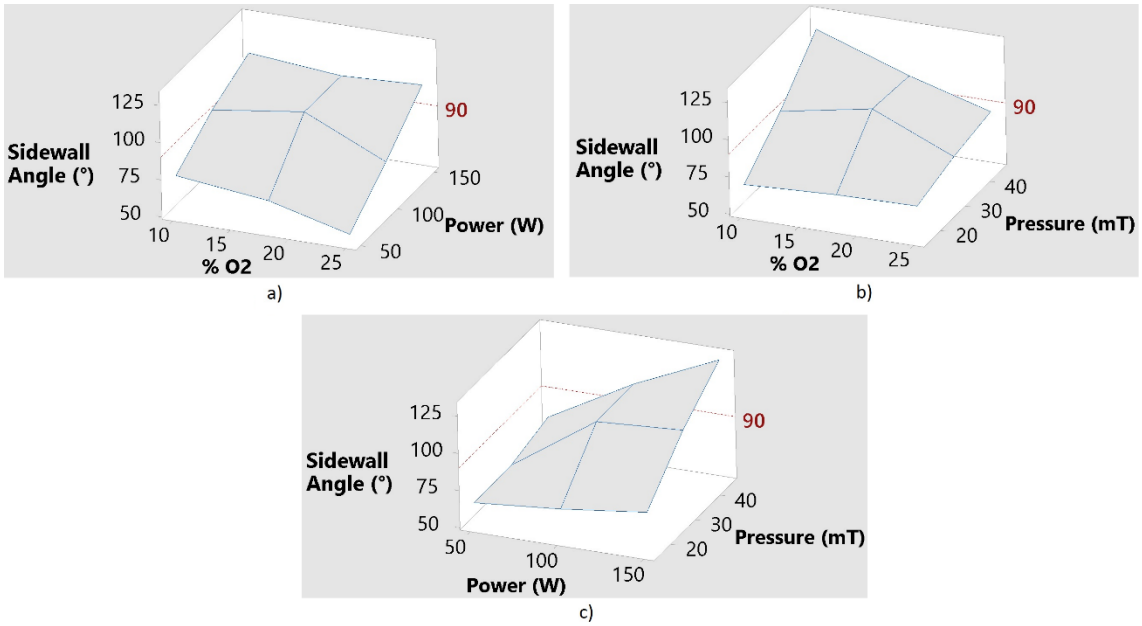


*Fig. 4-11. Surface plots of sidewall angle vs. process parameters. a) Sidewall angle vs. % $O_2$ and power, b) sidewall angle vs. % $O_2$ and pressure, c) sidewall angle vs. power and pressure.*

From Fig. 4-11 it is possible to observe trends in the etch profile as the process parameters are changed. It can be clearly seen that increasing the RF power increases the sidewall angle. This is due to a more anisotropic physical etch, as a result of a higher DC bias, which leads to greater ion bombardment of the sample. It can also be seen that increasing the pressure also results in an increased sidewall angle. The higher pressure leads to increased ion bombardment in the chamber, meaning that the energetic ions approach the surface at angles that are not perpendicular to the substrate surface, which therefore leads to an increased sidewall angle. The $O_2$ flow effects the passivation layer formation on the sidewalls. $O_2$ reacts with Ge to form $GeO_2$, which is only physically etched using this chemistry. Therefore, upon formation of $GeO_2$ on the sidewalls, it inhibits chemical etching in the lateral direction, resulting in a decreased sidewall angle with increased $O_2$ flow. This is similar to the results presented in the literature [50]. It is possible that in this study the over-etched Ge could have skewed the results. The Ge was purposely over-etched in order to assess the effectiveness of the $SiO_2$ etch stop layer.

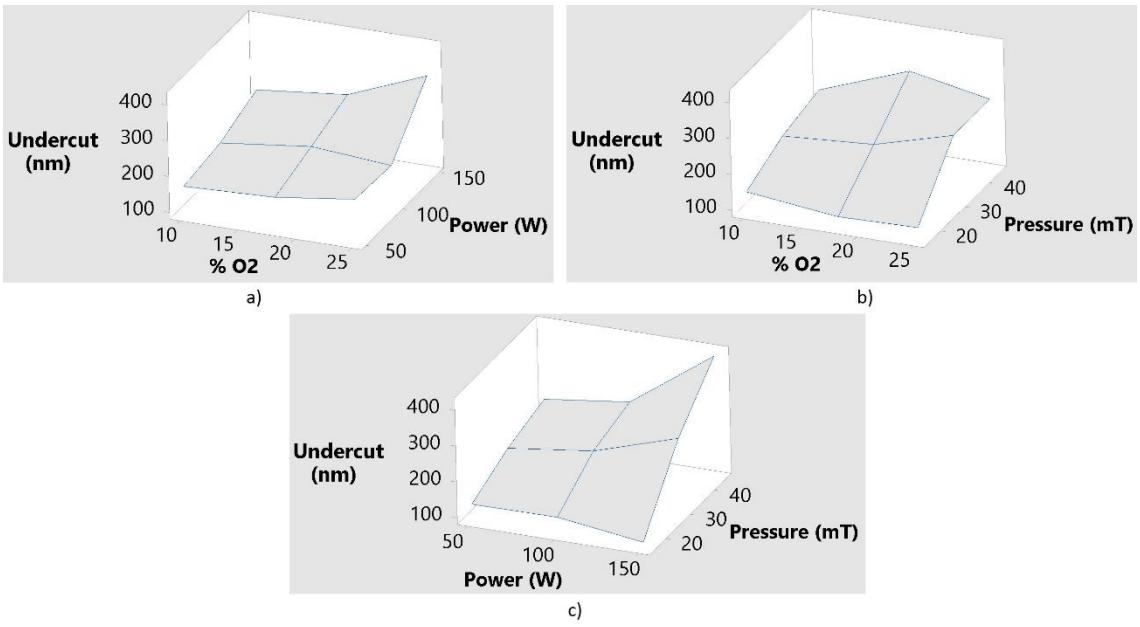


*Fig. 4-12. Surface plots of undercut vs. process parameters.*
*a) Undercut vs. % $O_2$ and power, b) undercut vs. % $O_2$ and pressure, c) undercut vs. power and pressure.*

From Fig. 4-12 it can be seen that the undercut is mostly a function of the chamber pressure, and that the RF power and $O_2$ flow have little effect. At higher

pressures the undercut is increased, due to the reduced directionality of the ion bombardment as a result of a greater number of ion collisions in the gas.

From the plots shown in Fig. 4-11 and Fig. 4-12 it is possible to predict an etch recipe that would yield 90° sidewalls. However, the minimum undercut achieved was 100 nm. This is not ideal, but not catastrophic as the original mask can be adjusted to account for this undercut so that the resulting profile does not differ from the design. The main problem with this etch was that when it was scaled up to wafer scale, the etch depth uniformity across the wafer was poor. The etch profile also changed when ZEP e-beam resist was used instead of S1813. In light of this, it was decided to use the knowledge gained from this etch study to design an inductively coupled plasma (ICP) etch. One advantage of ICP etching, over RIE etching, is that the plasma density can be independently controlled to the DC bias (controlled by the RF power) by adjusting the ICP power. This typically results in better etch depth uniformity across the wafer. Unfortunately, $O_2$ was unavailable in the ICP etching tool so $C_4F_8$ was used instead to produce a carbon based passivation layer on the sidewalls [53], as an alternative to the previous oxygen based passivation layer. The initial etch, based on a Si etch investigated in [53], produced an acute sidewall angle so, as demonstrated in Fig. 4-11a and Fig. 4-11c, both the RF power and ICP power were increased in order to increase the sidewall angle. The final etch recipe produced near 90° sidewall angles, as shown in Fig. 4-13.

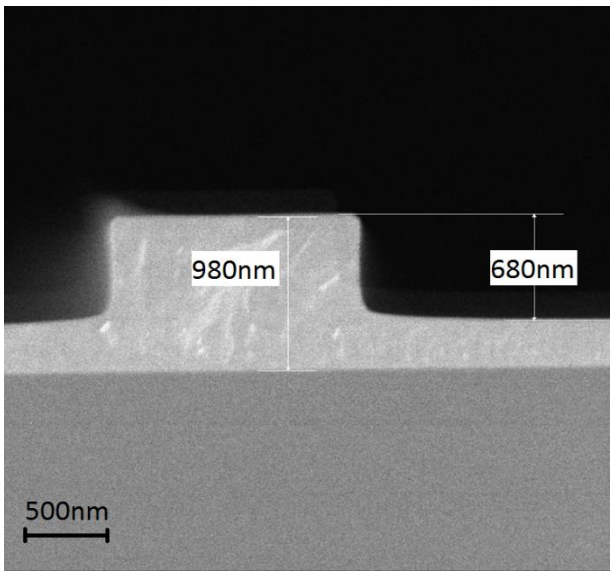


*Fig. 4-13. SEM image of Ge ICP etch.*
*Etch recipe: RF power: 50 W, ICP power: 700 W, pressure: 15 mT, temperature: 15 °C, $SF_6$ flow: 25 sccm, $C_4F_8$: 45 sccm.*

### 4.6.2 Device design

In order to assess the suitability of the Ge-on-Si layers studied above for mid-IR waveguides, some simple rib waveguides were designed by Jordi Soler Penades, with a Ge thickness of 2 μm, and an etch depth of 1.3 μm, as shown in Fig. 4-14. Grating couplers were used to couple light into, and out of, the waveguides. The grating period was 2.11 μm, with a fill factor of 0.5.

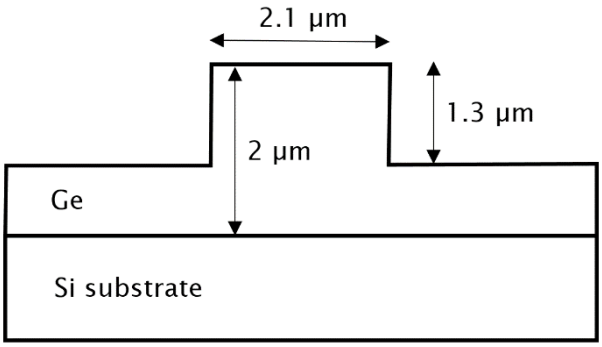


*Fig. 4-14. Schematic of Ge-on-Si mid-IR rib waveguide.*

It is desirable to reduce the number of hillocks on the surface of the Ge since they will cause high degrees of optical scattering losses, and result in low waveguide transmission efficiency. Therefore, the waveguides were fabricated on a patterned $SiO_2$ surface because, as described above, the number of hillocks in the Ge-on-Si region was greatly reduced using this method. However, it was also observed that when using this method, large areas of Ge delaminated from the $SiO_2$ surface as a result of the compressive stress in both the $SiO_2$ and Ge layers, and also the high interface energy between Ge and $SiO_2$ [54]. This can be observed in the optical microscope image in Fig. 4-15. However, these delaminated areas were always confined to the Ge-on-$SiO_2$ layers, and therefore would not affect the Ge-on-Si waveguides. This delamination effect was only observed for the higher growth temperature recipes, recipe F and recipe G (see Table 4-1), suggesting that the stress is greater in these layers (only recipes C, F, and G were grown on patterned $SiO_2$). Nevertheless, recipe F was selected for the purposes of the waveguides, ahead of the higher quality recipe G, simply because the growth rate of recipe G was too slow for 2 μm growth.

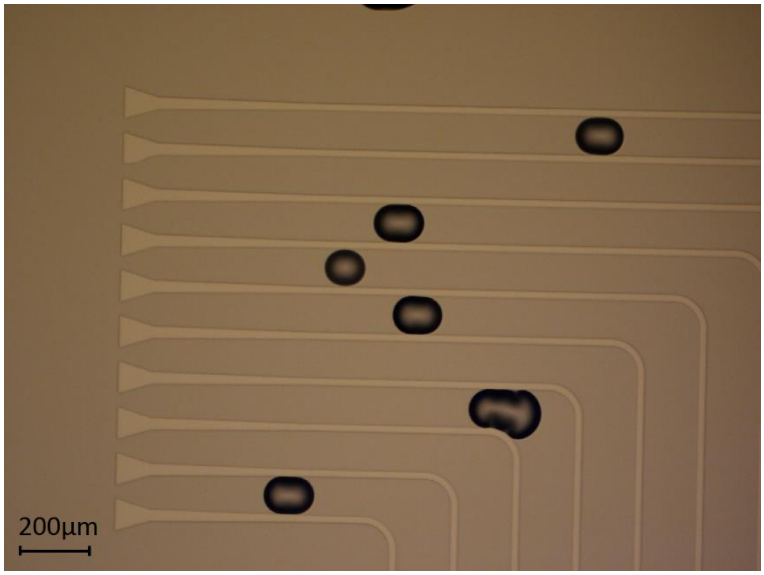


*Fig. 4-15. Optical microscope image of Ge growth on patterned $SiO_2$ surface, showing Ge delamination on some $SiO_2$ surfaces.*

After Ge growth on the patterned $SiO_2$ layer, waveguides were etched into the Ge-on-Si regions using e-beam lithography, and ICP etching using the recipe developed in section 4.6.1, above. ZEP e-beam resist was used to define the features. Grating couplers were used to couple the light into, and out of, the waveguides, as shown in Fig. 4-16. The waveguides were tapered out from the single mode width of 2.1 µm in order to improve the coupling efficiency of the gratings. This is necessary since the mid-IR fibre core diameter is approximately 9 µm [55].

After etching, the ZEP resist was removed in an $O_2$ plasma asher. However, a residue was unintentionally left on the surface of the waveguides (Fig. 4-16b), but this is not expected to hinder performance since simulations show that the light is well confined within the rib waveguide.

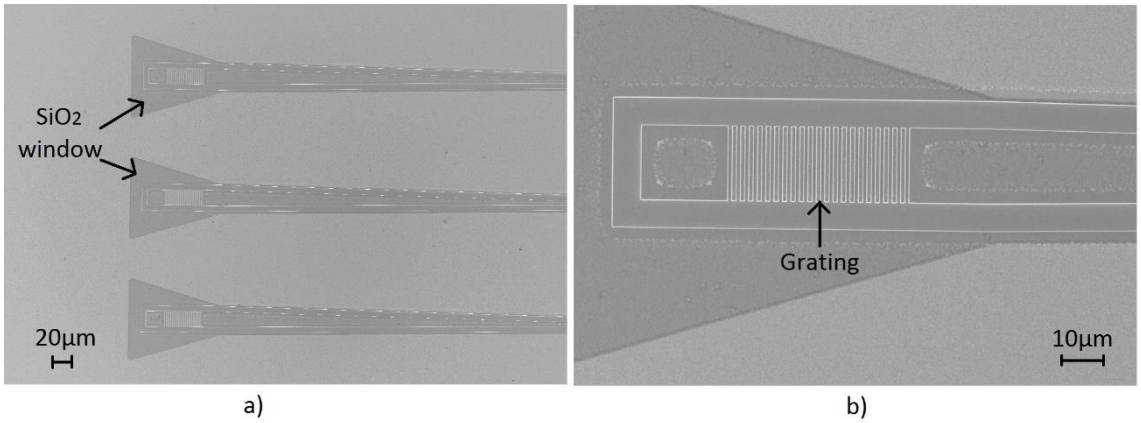


*Fig. 4-16. SEM image of Ge waveguides grown in windows defined in an $SiO_2$ layer.*
*a) Overview showing waveguides positioned in $SiO_2$ windows, b) gratings to couple light into, and out of, the waveguides. Resist residue can be seen in the centre of the waveguides but this is not expected to interact with the propagating light.*

### 4.6.3 Measurement setup

In order to characterise the Ge waveguides, the setup shown in Fig. 4-17 was used.

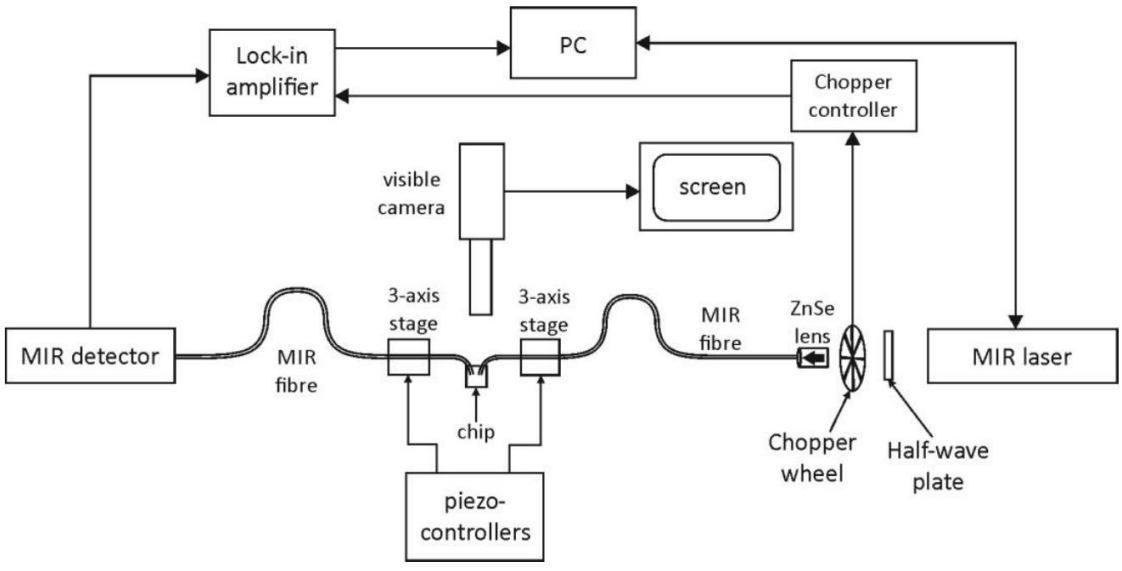


*Fig. 4-17. Measurement setup for mid-IR waveguide characterisation, reproduced from [56].*

The mid-IR setup is more complex than the equivalent near infra-red setup due to the noise reducing signal processing that is required to filter out the

background infra-red radiation (i.e. thermal blackbody emission). This is the purpose of the chopper wheel, chopper controller and lock-in amplifier. The chopper wheel is a rotating mechanical wheel with regular apertures that is placed in the path of the light beam to effectively produce an optical square wave. The frequency of this optical square wave, which can be adjusted by the chopper controller, is passed to the lock-in amplifier which measures only the amplitude of the square wave at the desired frequency, thus filtering out the majority of the background noise.

The light beam produced by the laser firstly passes through a half-wave plate, which can be used to adjust the polarisation, and then through the chopper wheel. The beam is then coupled into a mid-IR optical fibre using a ZnSe focusing lens. This optical fibre guides the light to the chip, which is placed on a stage in the centre of the setup. The fibre is orientated at approximately 10° to the normal to the chip surface by a fibre holder, which is positioned using a 3-axis stage. The fibre can be approximately aligned to the grating using micrometres on the 3-axis stage, and fine adjusted to achieve optimum coupling using a piezo-controller. A camera positioned above the sample allows the position of the fibres to be viewed on a screen. The output fibre is similarly configured to the input fibre, and guides the light onto the mid-IR detector. The whole system is controlled by a PC. This setup is described in more detail in [56].

### 4.6.4 Loss measurements

The transmission was measured through a series of straight waveguides, of varying lengths, in the wavelength range 3.725 μm to 3.815 μm. The results are plotted in Fig. 4-18.

The measured loss of 42 dB/cm is very high compared to the state-of-the-art of 2.5 dB/cm (2 μm Ge thickness at λ=5.8 μm) [57], and 0.58 dB/cm (3 μm Ge thickness at λ=3.8 μm) [58]. This could be due to the high TDD of the Ge layer (Fig. 4-2b), which would cause high degrees of scattering. TDD reduction by thermal annealing was attempted but this caused Ge delamination as most of the layer is grown on $SiO_2$. This delamination was observed even at anneal temperatures as low as 600 °C. In future experiments, the Ge grown on $SiO_2$ could be removed prior to waveguide formation by etching using a negative

resist such as AZ2070. In this way, TDD reduction by thermal annealing will be plausible, as only Ge-on-Si will remain.

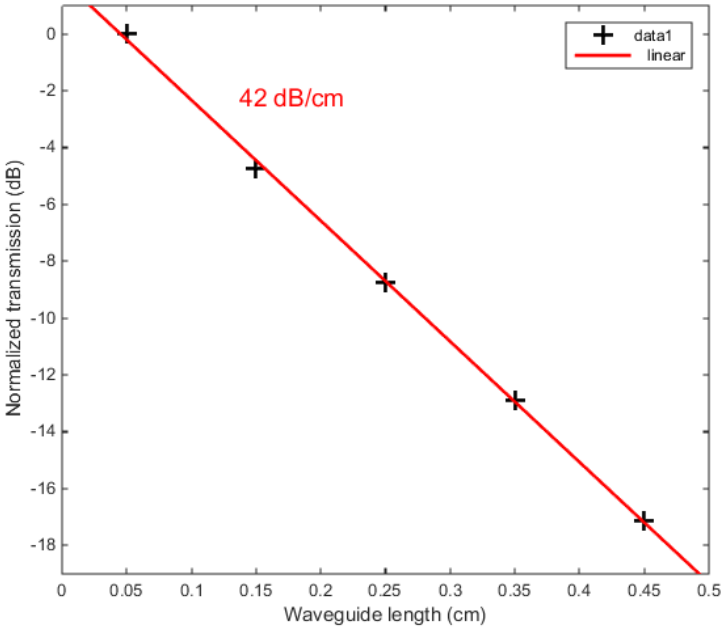


*Fig. 4-18. Propagation loss measurements for 2.1 µm wide PECVD Ge-on-Si waveguides.*

## 4.7 Ge-on-Si PECVD conclusions

Ge-on-Si growth using PECVD is a low cost, low temperature method that is capable of forming single crystal Ge material. It is therefore suitable for the fabrication of low cost devices, where the material quality is not of the utmost importance. For example, it is suitable for the formation of a Ge layer for RMG, as discussed in Chapter 5, and the fabrication of low cost photodetectors, as discussed in Chapter 6.

Using a 2-step PECVD growth method, with an initial growth at 250 °C, followed by a subsequent growth at 400 °C, a TDD of $3.3 \times 10^8$ $cm^{-2}$ and a surface roughness of 3.5 nm has been demonstrated. These properties were measured after a 600 °C anneal in an $N_2$ atmosphere for 2 minutes. This anneal step improved the TDD by an order of magnitude.

# Chapter 5: SiGe rapid melt growth

## 5.1 Motivation and applications

Silicon-germanium ($Si_{1-x}Ge_x$) has become a well-established material in both the electronics and photonics industries. It possesses full miscibility across its entire composition range, which allows for the tuning of properties such as the band gap and lattice constant, between those of bulk Si and bulk Ge. This means that depending on the composition, SiGe alloys can be either optically absorbing or transparent at the most common telecommunication wavelengths (1550 nm or 1310 nm), which enables the fabrication of active optical devices for both modulation [1, 2] and detection [3, 4]. It also has both a higher electron mobility, and hole mobility relative to Si [5], which will ultimately lead to faster electronic devices, e.g. bipolar complementary metal-oxide semiconductor (BiCMOS) transistors [6, 7]. Another potential application for SiGe is lattice matching for epitaxial III-V growth [8-10].

SiGe can be epitaxially grown directly on Si substrates using conventional methods such as molecular beam epitaxy (MBE) [11], low energy plasma enhanced chemical vapour deposition (LEPECVD) [12], and reduced pressure chemical vapour deposition (RPCVD) [13]. However, these growth methods inevitably introduce a high defect density into the SiGe layer due to the lattice mismatch between the SiGe and the Si substrate. These growth methods are briefly summarised in Chapter 3.

Another method of growing SiGe, this time on a localised insulator, is rapid melt growth (RMG). RMG, also referred to as liquid phase epitaxy (LPE), is a technique that was invented in the 1960's [14], and further developed in the 1970s for the fabrication of detectors [15], LEDs [16], and laser diodes [17]. The technique, originally used for III-V crystal growth, was pioneered by Liu *et al.* [18] for localized germanium-on-insulator (GOI) growth in 2004, and has since been studied by various groups [19-23], and adapted for silicon-germanium-on-insulator (SGOI) growth [24-30].

One particular motivation for a localised SGOI platform is the monolithic integration of photonic devices with electronic devices on Si substrates, providing a complementary solution to the more standard silicon-on-insulator (SOI) substrates typically used for photonic devices. The migration to Si substrates is of major interest for cost, process flexibility, and compatibility reasons. An electro-photonics integrated platform can be achieved with the use of dielectric optical waveguides [31], with localised buried $SiO_2$ layers for optical confinement. Other techniques for producing localised SGOI include layer transfer using a donor wafer [32] and Ge condensation [33]. However, using these techniques, only a single SiGe composition can be achieved.

RMG is enabled by the fact that Si has a much higher melting point than Ge (1414 °C and 938 °C respectively [34]), meaning that the Ge can be melted whilst the Si, acting as a template, maintains its crystal structure. One of the main benefits of growing SiGe using RMG is the extremely low threading dislocation density (TDD) that can be achieved. This has the potential to lead to improvements in device characteristics, such as dark current and quantum efficiency, when compared to devices fabricated by other growth methods.

This chapter begins with a description of the RMG fabrication process, and subsequently presents a novel method for realising tuneable, uniform composition, localised SGOI layers, using tailored tree-like structures.

## 5.2 Fabrication process

All fabrication has been carried out on 6 inch (100) Si wafers. Prior to fabrication, a standard RCA clean was carried out on all process wafers. This consisted of a 5 minutes dip in 5:1:1 $H_2O$:$H_2O_2$:$NH_4OH$ (RCA-1), at a temperature of 40 °C, to remove any organic contaminants, followed by a 1 minute dip in 20:1 HF to remove the surface $SiO_2$ formed during the RCA-1 clean, and finally a 5 minutes dip in 6:1:1 $H_2O$:$H_2O_2$:HCl (RCA-2), at a temperature of 40 °C, to remove any metallic contaminants.

The first step following cleaning was to deposit an insulating layer onto the Si substrate for the lateral regrowth to propagate along. This can be any insulating material such as $SiO_2$ or $Si_3N_4$. In this project, a 50 nm $SiO_2$ layer was deposited by plasma enhanced chemical vapour deposition (PECVD). $SiO_2$ was selected for

the simplicity of the HF wet etch, as opposed to the hot $H_3O_4P$ wet etch for $Si_3N_4$, which requires specialised equipment. The thickness of this insulating layer can be varied to suit the design requirements. A standard $SiO_2$ deposition recipe was used, with the process gases being $SiH_4$ (4.2 sccm), $N_2O$ (350 sccm) and $N_2$ (80 sccm), which react as follows:

$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2$$

The additional nitrogen is recommended by the tool manufacturer as it improves the film thickness uniformity over the wafer.

$SiO_2$ densification was then carried out using a rapid thermal annealer (RTA) in order to reduce the amount of H trapped in the $SiO_2$ film. This is important because trapped gas in the $SiO_2$ film could be released during the RMG annealing process, causing voids to form in the SiGe as it recrystallises. Zhang *et al.* [35] used secondary ion mass spectroscopy (SIMS) to measure the H content in $SiH_4$ based $SiO_2$ films deposited using PECVD, after annealing at different temperatures, as shown in Fig. 5-1.

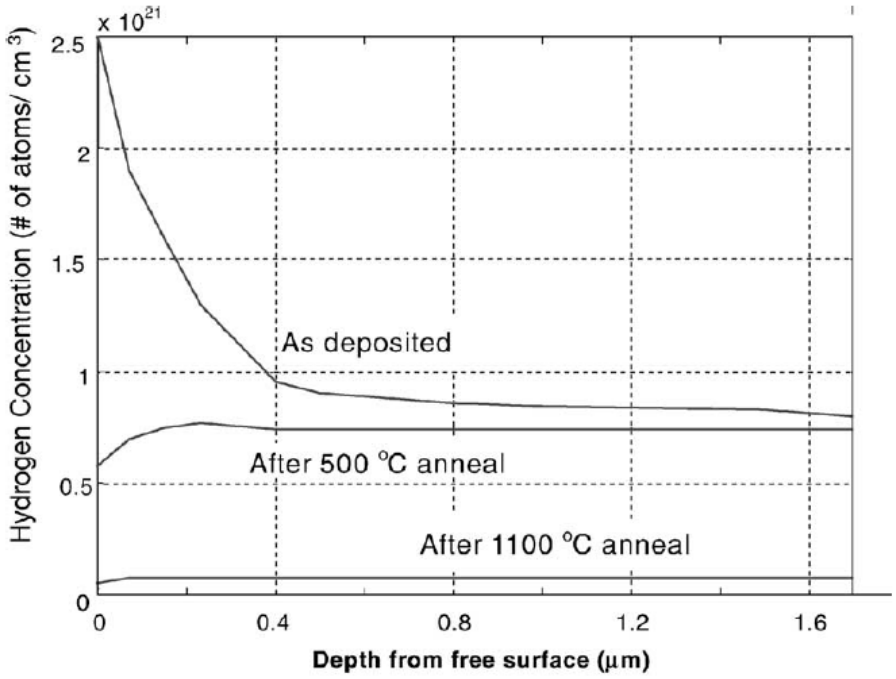


*Fig. 5-1. SIMS H composition analysis of $SiH_4$ based PECVD of $SiO_2$, reproduced from [35].*

They discovered that annealing significantly reduced H concentration close to the free surface, with higher temperature anneals resulting in lower H

concentrations. However, high temperature annealing led to high levels of stress in the wafer, which led to wafer bowing. Therefore, an intermediate temperature of 700 °C was chosen for this 30 minutes densification process.

Ellipsometry measurements confirmed that after the 30 minutes anneal the thickness of the 50 nm $SiO_2$ decreased by approximately 2.5 nm or 5%. This is a result of the rejection of H from the $SiO_2$ film.

The $SiO_2$ layer was then patterned using standard ultra-violet (UV) photolithography, and a dilute (20:1) HF wet etch, in order to expose the underlying Si to act as a seed for the SiGe recrystallisation process. An HF etch was selected firstly because of its simplicity and batch etching capabilities, and secondly because Vu *et al.* [36] observed that a plasma etch damaged the Si surface, which proved to hinder SiGe regrowth. A plasma etch also tends to leave polymer on the surface of the Si, which subsequently requires an HF clean to remove. HF etches $SiO_2$ by the following reaction:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

The etch rate at room temperature of densified $SiO_2$ in 20:1 HF is approximately 70 nm/min.

The photoresist was removed in an $O_2$ plasma using a plasma asher, which inevitably leads to the formation of a thin native $SiO_2$ on the Si surface. Consequently, an HF dip (5 seconds) must be performed prior to Ge growth, firstly to remove the native $SiO_2$ formed during ashing, and secondly to ensure that the dangling bonds at the surface of the Si substrate are terminated with H to prevent the formation of a native $SiO_2$ in the atmosphere during transfer to the Ge growth chamber. Harame *et al.* [37] observed that this HF last approach eliminated the need for a high temperature pre-bake (to remove the native $SiO_2$) prior to epitaxial Ge growth, by reducing the Si reactivity to air by more than 13 orders of magnitude.

Ge growth was then performed by PECVD using $GeH_4$ diluted in Ar (10%) (2.5 sccm) and $H_2$ (100 sccm), at a temperature of 250 °C (recipe C). More details of the Ge growth can be found in Chapter 4. This particular recipe was selected, ahead of the higher quality recipe F and recipe G, due to the Ge delamination observed for these recipes on $SiO_2$ surfaces. A thickness of 400 nm was grown

in order to match the 400 nm Si overlayer typically used in SOI wafers for Si photonics applications, therefore enabling a planar surface if a butt coupling architecture is employed. Fig. 5-2 shows a cross section scanning electron microscope (SEM) image at the seed edge after the Ge growth. Non-selective growth is achieved (i.e. growth on both Si and $SiO_2$), which is necessary for RMG to be realised. The surface roughness is visibly higher when grown on $SiO_2$, when compared to growth on Si. This could be reduced by chemical mechanical polishing (CMP).

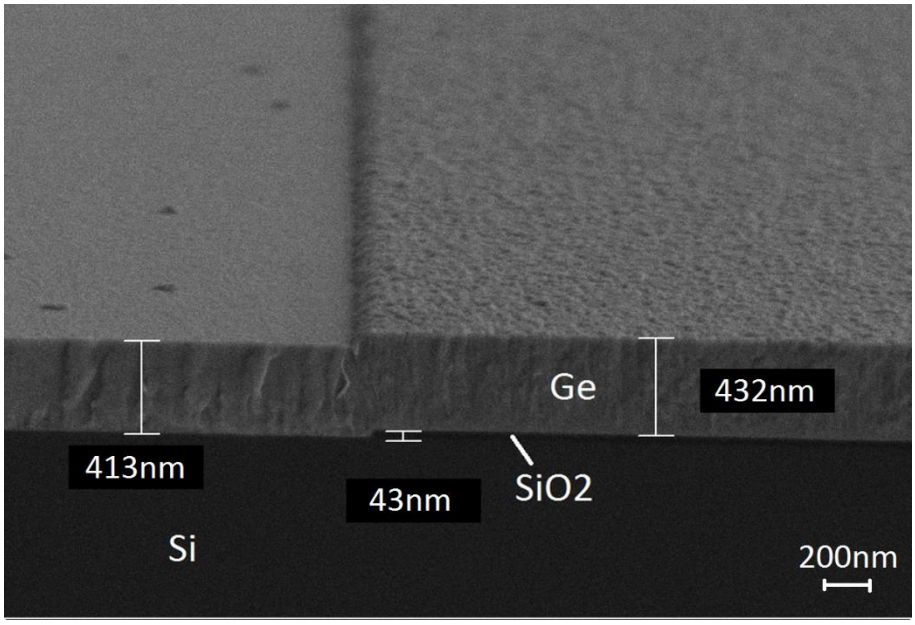


*Fig. 5-2. Cross-section SEM image of Ge growth at the seed edge.*

The Ge was then patterned into the desired structures via an inductively coupled plasma (ICP) etch, using $SF_6$ and $C_4F_8$, with one end of the Ge pattern overlapping the Si seed area, as defined using standard UV photolithography. $SiO_2$ bonds are extremely strong and are difficult to break with fluorine alone; therefore, the $SiO_2$ acts as an etch stop due to the high selectivity of this etch process (9:1 selectivity of Ge:$SiO_2$). The photoresist was removed after etching by $O_2$ plasma ashing.

A 1 μm $SiO_2$ layer was then deposited by PECVD in order to encapsulate the Ge structures, forming micro-crucibles, within which the liquid Ge is contained during subsequent melting in an RTA. During this melting step, the temperature of the RTA is stabilised at 500 °C before ramping up to the peak temperature, above the melting point of Ge (938 °C), at a rate of approximately 100 °C/s. The

temperature is then held at its peak for 1 second, before cooling naturally (i.e. switching off the RTA lamps). It is important to note here that, whilst the measured peak anneal temperatures are accurate relative to one another, they should be considered arbitrary temperatures in the absolute sense, because they are recorded using a pyrometer measuring the infra-red radiation from the back of the Si substrate during annealing. This recorded temperature does not match the SiGe temperature since the optical absorption coefficients of the SiGe and Si substrate are different, and will vary depending on the alloy composition [38]. The temperature can also vary across each wafer. Therefore, in most cases, an estimated temperature is used, based on the SiGe phase diagram, which is explained in section 5.3.1.1, below.

This fabrication process is summarised in Fig. 5-3.

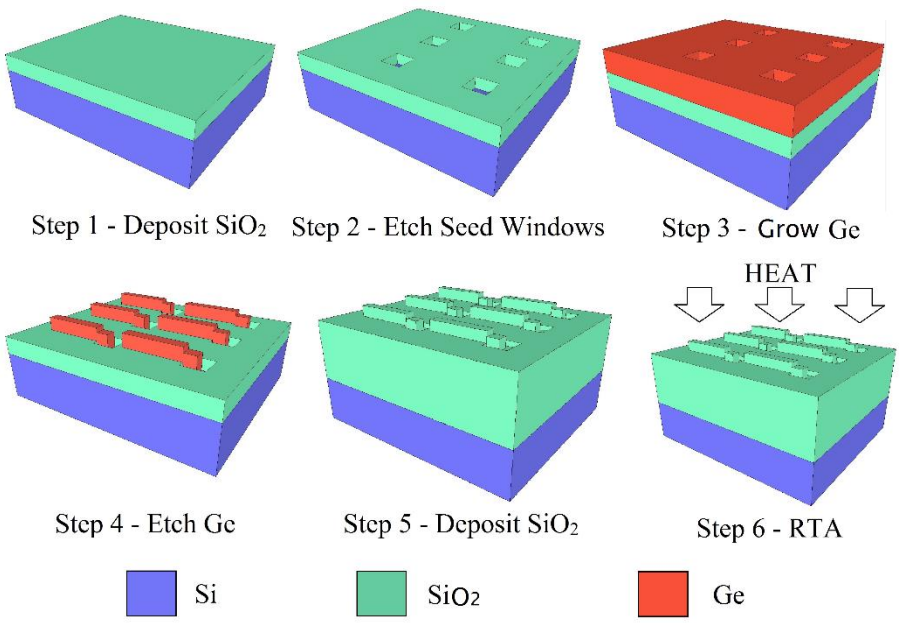


*Fig. 5-3. Summary of the SiGe RMG fabrication process.*
*Step 1: an insulating layer is deposited onto a Si substrate, step 2: the insulating layer is etched to open up seed windows, from which the Ge will regrow, step 3: Ge is grown using a non-selective method, step 4: the Ge is etched into the desired patterns, emanating from the Si seed windows, step 5: an insulating capping layer is deposited to encapsulate the Ge, step 6: RMG is performed in an RTA by raising the temperature above the Ge melting point and subsequently cooling.*

### 5.2.1 Regrowth mechanism

The purpose of the RMG process, as the name suggests, is to melt a material and initiate recrystallisation from the liquid phase, using a seed, by subsequent cooling. One of the big advantages of this is that the initial Ge growth is non-critical, and can therefore be carried out using any non-selective method such as evaporation, sputtering, or, in this case, PECVD. Fig. 5-4 shows a cross-section schematic of the recrystallisation process during cooling.

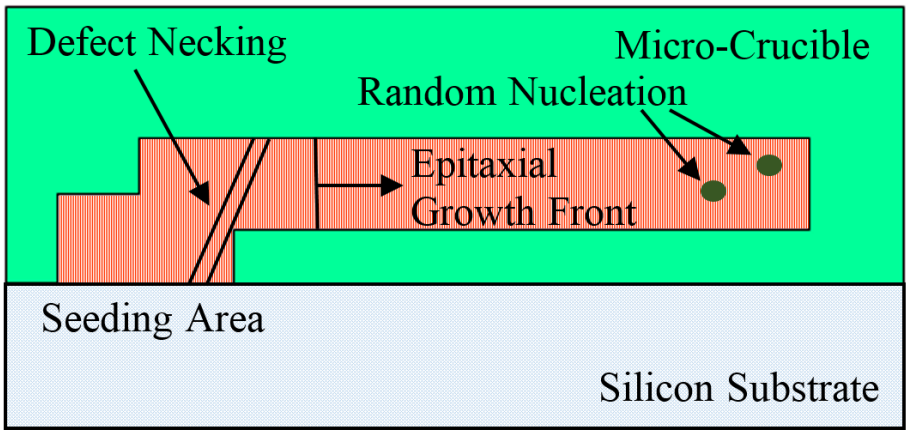


*Fig. 5-4. A cross-section schematic of the recrystallisation process during cooling.*

As the temperature is raised above the melting point of Ge, Si diffusion from the seed is greatly enhanced [39]. This leads to the formation of a SiGe liquid, which then recrystallises from the Si seed upon cooling. It is essential that regrowth is initiated at the Si seed in order to ensure single crystal, epitaxial growth, with the SiGe solidifying with the same crystal structure as the underlying Si. Growth is initiated at the seed for two reasons: firstly, the Si substrate acts as a heat sink, ensuring more rapid cooling in the seed area; secondly, Si diffusion into the Ge structure increases the solidification temperature so that material with a slightly higher Si composition solidifies first (i.e. areas nearer the Si seed). The solidification temperature of a SiGe alloy, as a function of composition, can be determined by the solidus curve on the SiGe phase diagram, shown in Fig. 5-5.

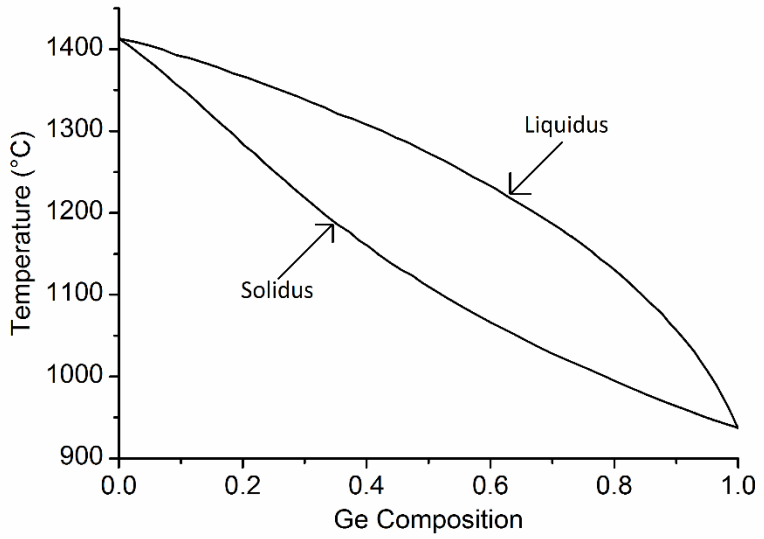


*Fig. 5-5. SiGe phase diagram - adapted from [40].*

After solidification has commenced in the seed, epitaxial growth then propagates laterally along the SiGe structure. Another advantage of using this method is that all the defects caused by the lattice mismatch between Si and Ge are confined to the seed area by a defect necking mechanism [41].

Undercooled SiGe liquid can also recrystallise through random nucleation ahead of the regrowth front [42]. It is critical to avoid this in order to ensure single crystal epitaxial growth. However, it is only likely to occur if the growth front propagation speed is extremely slow, especially during binary alloy regrowth, where solidification occurs over a range of temperatures. Random nucleation is driven by the Gibbs free energy change, $\Delta G$, in the liquid to solid phase transition, and is a result of random fluctuations. As a random solid nucleus forms, the Gibbs free energy change is proportional to the volume of the solid. However, because the nucleus has a crystalline structure that is different from the liquid, energy is needed to form the nucleus-liquid interface, which is proportional to the surface area of the nucleus. Therefore, in order for the solid nucleus to become energetically stable, a critical radius, $r^*$, must be reached in order for the Gibbs free energy change due to solid formation (driving energy) to be greater than the interface energy (retarding energy). An arbitrary solid nucleus that randomly forms tends to diminish, rather than grow, because the interface energy is greater than the Gibbs free energy change. This is demonstrated in Fig. 5-6.

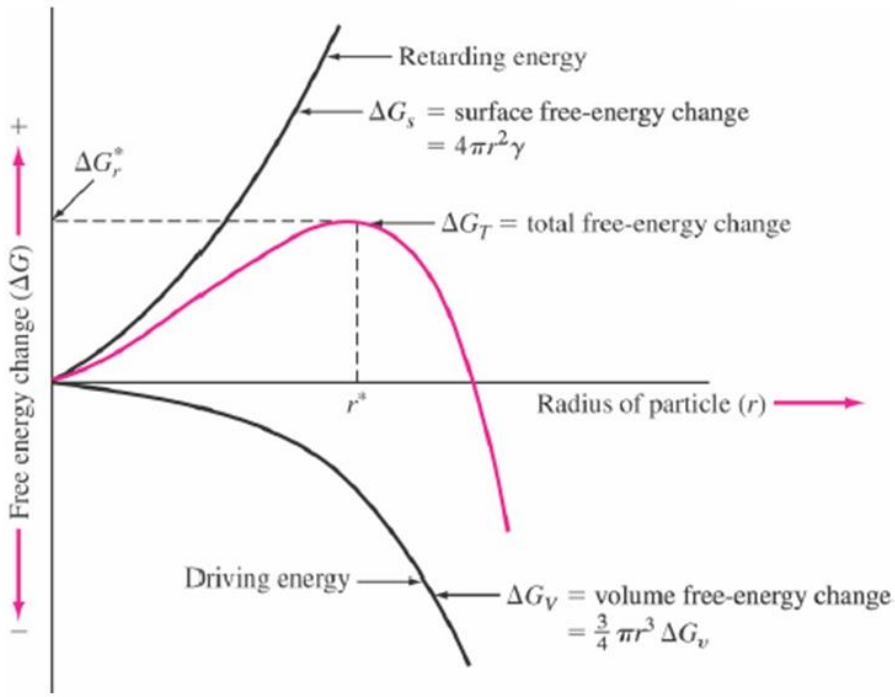


*Fig. 5-6. Energy change in random nucleation as a function of nucleus radius, reproduced from [43].*

Homogeneous nucleation occurs in the SiGe melt; heterogeneous nucleation occurs on the micro-crucible walls, or on contaminants in the melt. Heterogeneous nucleation forms a lower energy barrier than homogenous nucleation because the heterogeneous nucleation site lowers the energy cost of forming a nucleus.

## 5.3 Characterisation

After RMG has been performed, the SiGe material was characterised to determine its composition. The crystal quality was also analysed using electron backscatter diffraction (EBSD) and transmission electron microscopy (TEM).

The primary method of SiGe composition characterisation used in this project is Raman spectroscopy. This method has been selected because it is a micro-scale, non-destructive technique, which does not require any sample preparation, and is commonly used for this type of analysis [20, 44-46]. Auger electron spectroscopy (AES) was also carried out by Christopher Mallinson at the Surface Analysis Laboratory, at the University of Surrey, as a method of confirming the results obtained by Raman spectroscopy.

### 5.3.1 Raman spectroscopy

The SiGe composition profile in all structures has been characterised using 532 nm Raman spectroscopy. A 50x objective lens was used, resulting in a laser spot size of approximately 0.5 μm. A description of Raman spectroscopy can be found in Chapter 2. It is important to recognise that the data gathered relates to the near-surface information only. This is because a 532 nm laser has a penetration depth, which is dependent on the composition [38], of several tens of nanometers in high Ge percentage SiGe. Therefore, it is possible that there is a non-uniform vertical distribution of Ge, but this is predicted to be negligible [28], particularly in areas away from the seed, since the epitaxial regrowth front propagates laterally, and not vertically.

A lateral scan was performed along each structure, resulting in a series of Raman spectra, each of which can be analysed to determine the SiGe composition at that particular point. An example Raman spectrum is shown in Fig. 5-7.

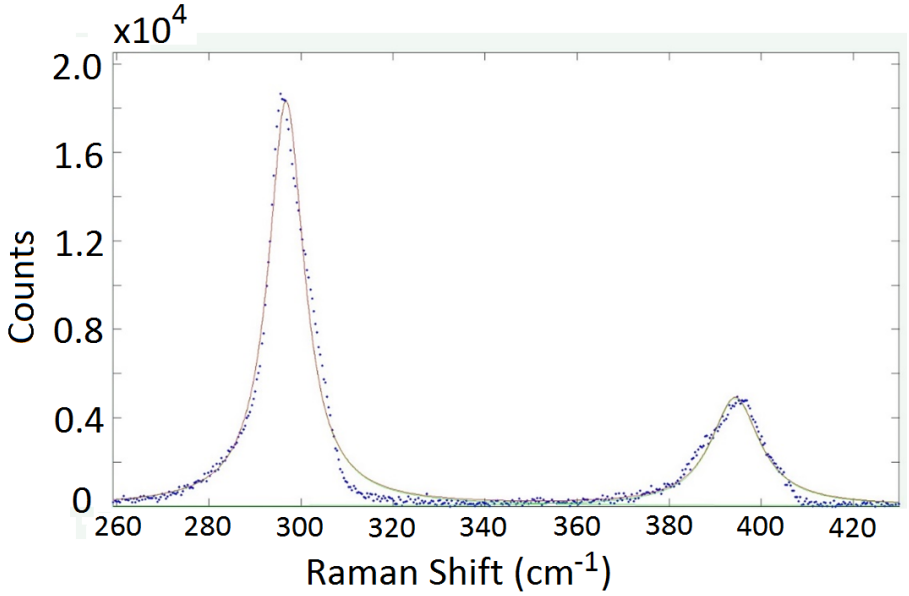


*Fig. 5-7. Example Raman spectrum showing fitted Lorentzian curves.*

Each spectrum has 2 characteristic peaks; the first, at a wavenumber in the range of 280 $cm^{-1}$ to 300 $cm^{-1}$, corresponds to the Ge-Ge mode vibrations, and the second, in the range of 390 $cm^{-1}$ to 410 $cm^{-1}$, corresponds to the Si-Ge mode vibrations. The wavenumber of each mode depends on the composition of the measured material, which therefore enables the composition to be determined

using the peak location [45, 47]. Shin *et al.* [47] showed that the unstrained Ge-Ge Raman peak location, $\omega_{GeGe}$, can be calculated by Equation 5-1:

$$\omega_{GeGe} = 280.8 + 19.37x \qquad \text{Equation 5-1}$$

Where $x$ is the Ge concentration. The spectral resolution of the Raman spectrometer used in this project is only 0.4 $cm^{-1}$, which corresponds to a Ge concentration uncertainty of approximately 0.02. However, this type of measurement is complicated by the fact that the peak location also depends on strain [48-50]. In fact, an in-plane strain of 1% will induce a peak shift of approximately 3.85 $cm^{-1}$ [48]. Therefore, an alternative method of determining the composition at each point was used.

By considering the relative intensites of the Si-Ge and Ge-Ge peaks, as proposed by Mooney *et al.* [44], the composition can also be determined. In order to perform this analysis, a Lorentzian curve is fitted to each peak using the MATLAB peakfit function (shown in Fig. 5-7 as solid lines) [51]. The ratio of the integrated intensities can then be related to SiGe composition by Equation 5-2:

$$\frac{I(SiGe)}{I(GeGe)} = \frac{2(1-x)}{kx} \qquad \text{Equation 5-2}$$

Where, *I(SiGe)* and *I(GeGe)* are the integrated intensities of the Si-Ge and Ge-Ge modes respectively, $x$ is the Ge concentration and $k$, which is dependent on the excitation wavelength, is an experimental setup specific constant that can be determined from samples of known composition.

Three SiGe layers, with a variety of compositions, which were grown using reduced pressure chemical vapour deposition (RPCVD) on Si wafers, were provided by IHP, Frankfurt, Germany. The composition of each of these layers was measured by SIMS. An example is shown in Fig. 5-8. SIMS is a destructive technique that requires large areas to be etched, which deems it unsuitable for strip composition profile analysis, but the accuracy of the technique is critical for calibration purposes.

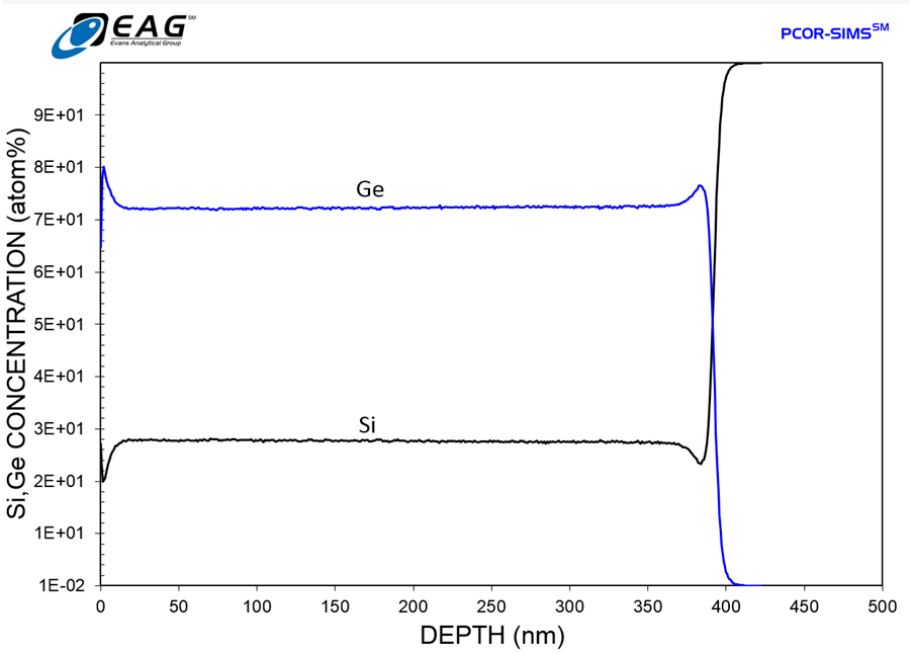


*Fig. 5-8. SIMS composition analysis of SiGe calibration sample.*

The top 50 nm of the samples were etched to remove the graded composition material at the surface. The samples were then measured using the Raman spectrometer, from which *k* was determined to be 1.2, as shown in Fig. 5-9.

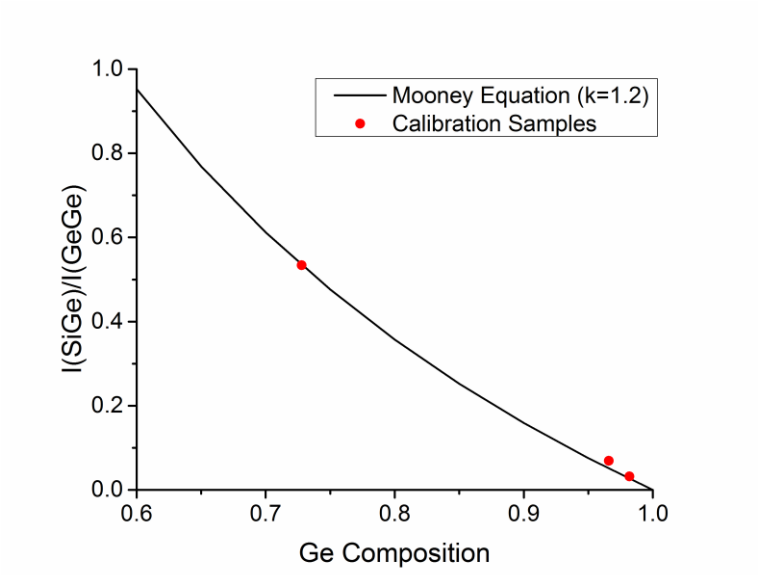


*Fig. 5-9. Calculation of the Mooney equation constant, k.*

Ideally, Fig. 5-9 would have more data points, but given that only 3 compositions of SiGe were available for measurement, k=1.2 is the best fit to the data. This value of *k* is in close agreement with the value quoted by another group in the literature [20]. Based on repeat Raman measurements, the error in the Ge composition is predicted to be approximately ±0.02.

#### 5.3.1.1 Composition profiles of straight strips

After RMG was carried out, the top encapsulating $SiO_2$ was removed in 20:1 HF to enable SEM viewing of the SiGe structures. Fig. 5-10 shows an array of strip widths, with a fixed length of 200 μm.

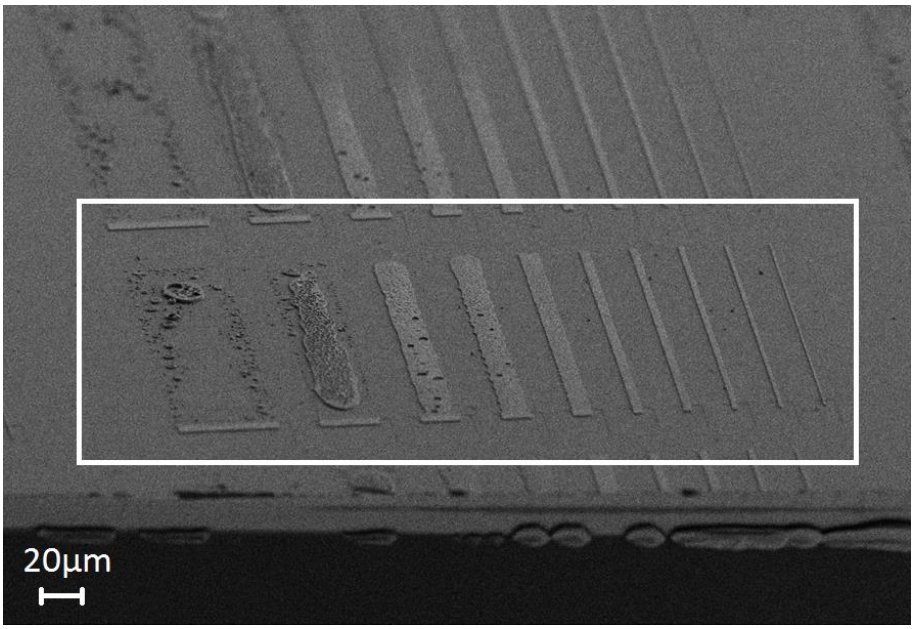


*Fig. 5-10. SEM image of RMG straight strips showing agglomeration at large strip widths.*

It is immediately clear from this image that there is a maximum strip width, below which RMG remains stable. Closer inspection reveals this maximum width to be of the order of 5 μm, using the fabrication process described above. At widths greater than 5 μm, the liquid SiGe agglomerates. This is possibly due to the high interface energy between $SiO_2$ and SiGe [22], which results in de-wetting of the $SiO_2$ surface whilst the SiGe is in the liquid phase. At strip widths less than 5 μm, agglomeration is suppressed, possibly because of a reduction in the effective pressure of the liquid SiGe on the top $SiO_2$. Consequently, only strips with a width of 5 μm or less are investigated in detail.

Fig. 5-11 shows the composition profile as a function of distance from the Si seed for a variety of strip lengths. The actual anneal temperature of the SiGe has been estimated to be 1008 °C ± 8 °C from the phase diagram (Fig. 5-5), by considering the lowest measured Ge concentration. As discussed earlier, as the structures are raised above the melting point of Ge, Si diffusion into the Ge dramatically increases, leading to the formation of a SiGe liquid. The diffusivity

of Si in liquid Ge, $D_S$, is approximately $3x10^{-4}$ $cm^2/s$ [39]. Therefore, the diffusion length is $\sqrt{(D_S t)}$, or approximately 200 µm, assuming the Ge is melted for 1 second. It is therefore valid to assume the liquid to be at a uniform composition before solidification commences, and that this peak temperature estimation is accurate.

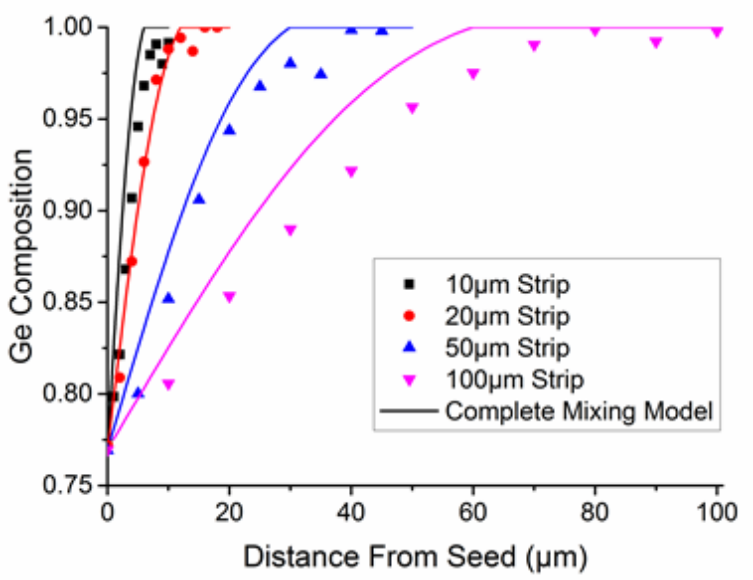


*Fig. 5-11. SiGe composition profiles for a range of straight strip lengths. Strip width = 5 µm. Estimated maximum SiGe temperature = 1008 °C. The strips have been fitted with the complete mixing model [28].*

It can be seen in Fig. 5-11 that the composition varies in the straight strips, from lower Ge concentration SiGe at the seed, to pure Ge at the far end of the strip. The composition profile is independent of length for the range of lengths shown. This can be seen in Fig. 5-12, where the strip length has been normalised by dividing each point by the total length of each respective strip. The complete mixing model [28], based on analysis originally carried out by Scheil [52], has been added to each curve. A complete explanation and derivation of the complete mixing model is given in section 5.3.1.4, below.

This observed graded composition profile is a result of the large separation between the solidus and liquidus curves of the SiGe phase diagram (Fig. 5-5), which results in preferential Si rich solid formation at the regrowth front, with rejection of Ge into the liquid.

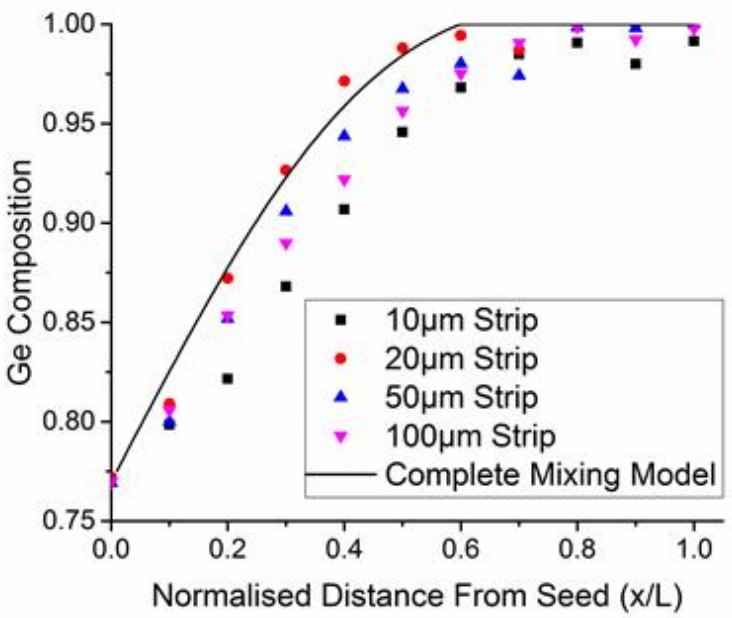


*Fig. 5-12. Normalised SiGe composition profiles of straight strips. Strip width = 5 µm. Estimated maximum SiGe temperature = 1008 °C. The strips have been fitted with the complete mixing model [28].*

Since the diffusivity of both Si and Ge in solid SiGe is many orders of magnitude lower than in liquid SiGe, it can be approximated that there is no diffusion in the solid phase. This assumption is validated by the fact that no diffusion (within experimental error) was observed for a sample annealed at a measured temperature of 854 °C (Fig. 5-13).

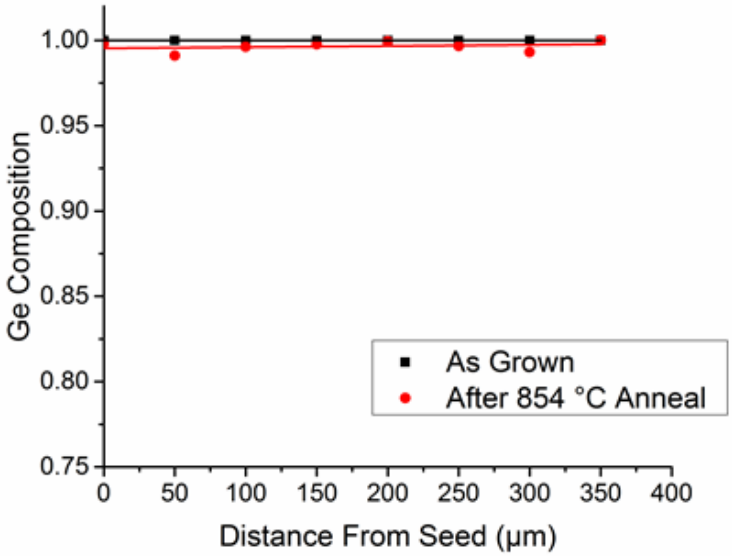


*Fig. 5-13. SiGe composition profile in a straight strip annealed below the Ge melting point.*

However, because the sample was heated from the top surface via optical radiation, but measured from the backside surface using a pyrometer, it is expected that the Ge temperature was in fact closer to its melting point.

Due to the lack of diffusion in the solid, once the SiGe in the seed area has solidified, Si diffusion from the substrate is blocked, leading to a finite Si 'pool' available in the SiGe melt. As described above, the SiGe phase diagram shows that there is a preferential growth of Si rich solid, which results in complete depletion of the Si 'pool' before the end of a straight strip. This graded profile is shown visually in Fig. 5-14, where straight SiGe strips have been etched in RCA-1 solution, both before annealing (Fig. 5-14a), and after annealing (Fig. 5-14b). RCA-1 solution will selectively etch Ge over Si due to the fact that $GeO_2$ is soluble in water. The $H_2O_2$ in RCA-1 solution oxidises the surface of both Si and Ge, but only the oxidised Ge will dissolve in the water used for dilution. In this figure, it can be seen that the etch is uniform in all directions before annealing, due to the 100% Ge, and that after annealing the etch rate is slower, close to the seed area, where the Si composition is higher.

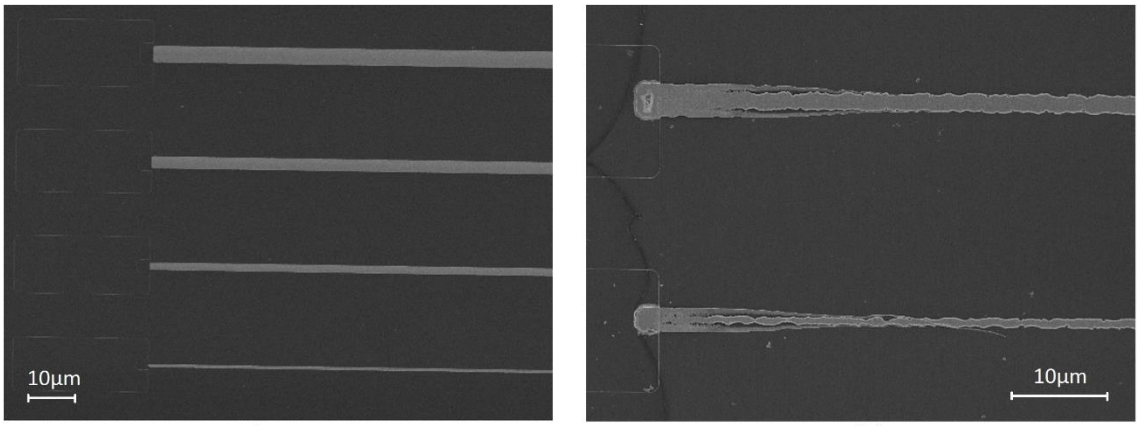


*Fig. 5-14. SEM images of straight SiGe strips after RCA-1 etching. a) Before annealing, showing uniform etch rate along length of strip, b) after annealing, showing lower etch rate near the seeds due to higher Si composition.*

### 5.3.1.2 Segregation coefficient

It is useful to define the segregation coefficient, *k*, of a SiGe alloy. *k* is a variable that defines the degree of segregation between Si and Ge at the regrowth front.

It is simply the ratio of the Ge solid composition, $C_S$, to the Ge liquid composition, $C_L$, at any given temperature:

$$k = \frac{C_S}{C_L}$$ Equation 5-3

This can be calculated from the phase diagram, as shown in Fig. 5-15.

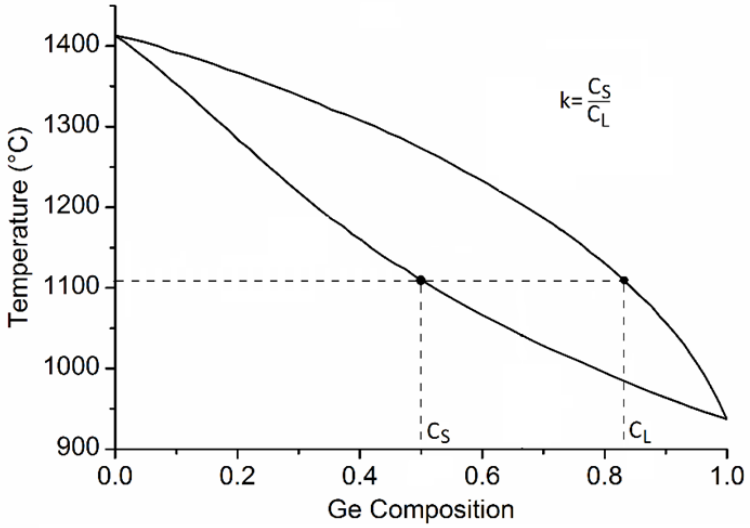


*Fig. 5-15. Calculating the segregation coefficient from the phase diagram.*

$C_0$ is defined as the average composition in the liquid when solidification commences, and is a function of anneal temperature, due to the increased Si diffusion into the strips at higher anneal temperatures.

The segregation coefficient can be plotted as a function of the solid Ge composition, as shown in Fig. 5-16, by gathering the $C_L$ and $C_S$ values from the SiGe phase diagram.

It can be seen that as the Ge composition approaches that of pure Ge, the segregation coefficient approaches unity. Conversely, there is a higher degree of segregation at lower Ge compositions. A linear fit has been applied between Ge compositions of 0.4 and 1.0, resulting in Equation 5-4 for the segregation coefficient as a function of the Ge solid composition, $C_S$.

$$k = \frac{C_S}{C_L} = 0.78C_S + 0.21$$ Equation 5-4

This simplified fit is applicable to all of the measurements carried out in this project, because no Ge compositions less than 0.4 were measured.

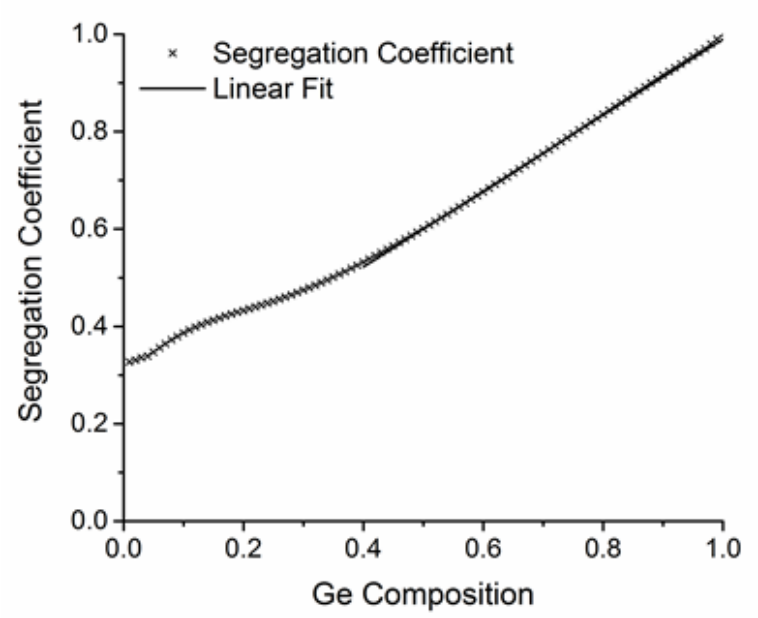


*Fig. 5-16. Segregation coefficient as a function of solid Ge composition. A linear fit has been applied between Ge compositions of 0.4 and 1.0.*

### 5.3.1.3 Scheil equation

The simplest model of binary alloy solidification is perhaps the Scheil equation [52]. This equations makes 3 assumptions:

1. There is no diffusion in the solid.
2. There is complete mixing of Si and Ge in the liquid, resulting in a uniform composition.
3. The segregation coefficient, $k$, is a constant. This is true if the phase diagram is simplified to straight lines for small composition ranges.

Solidification will commence in the seed area when the composition is $kC_0$. This is because the liquid is at a uniform composition of $C_0$, and therefore the solid composition can be calculated from the segregation coefficient (Equation 5-3). As the regrowth front propagates along the strip, the liquid is enriched with the rejected Ge, resulting in an increase in the Ge composition of the solidified alloy, as shown in Fig. 5-17.

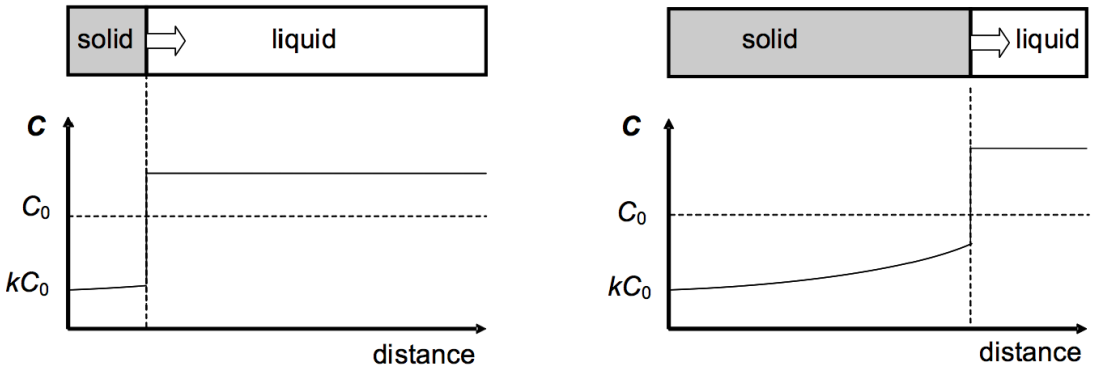


*Fig. 5-17. Composition profile evolution according to the Scheil equation, reproduced from [53].*
*This diagram assumes a constant value of k.*

The full derivation of the Scheil equation is given in Appendix C, so the equation is simply stated here:

$$C_S = kC_0(1 - f_S)^{k-1} \qquad \text{Equation 5-5}$$

Where $f_S$ is the fraction of the strip that has solidified. This equation predicts that the solid concentration tends towards infinity, but of course it will only reach 100% Ge.

Since this equation assumes complete mixing in the liquid, it is only accurate when the regrowth speed is low, allowing enough time for the rejected Ge at the regrowth front to diffuse into the bulk melt.

### 5.3.1.4 Complete mixing model

A more accurate version of the Scheil equation is the complete mixing model [28], because this model does not assume a constant value of *k*. The other two assumptions still remain valid. For the purposes of this project, the simplified linear equation for the segregation coefficient (Equation 5-4) has been used.

In order to derive the complete mixing model we consider a small advancement of the growth front, as shown in Fig. 5-18.

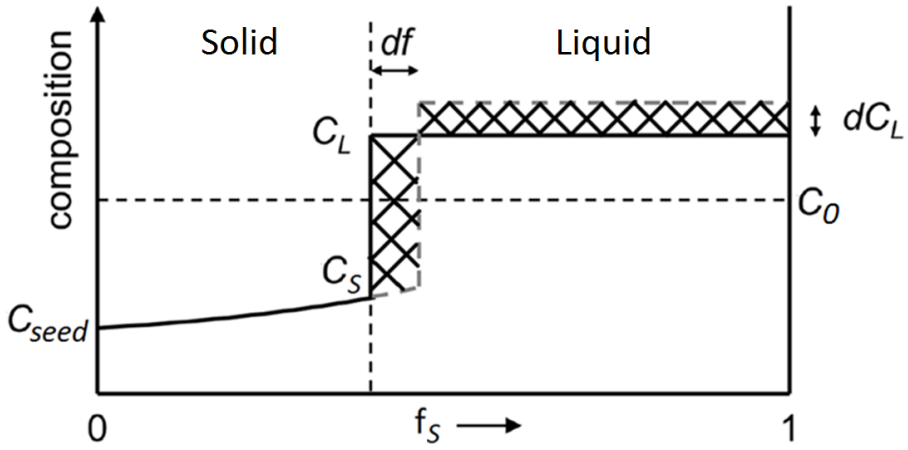


*Fig. 5-18. Derivation of the complete mixing model.*

In Fig. 5-18, the solid line represents the original composition profile at a given point in time. The dashed line represents the composition profile after a small advancement of the growth front, *df*. At the growth front, Ge is rejected from the solid, into the liquid. Therefore, conservation of mass allows equating of the amount of Ge in the two hashed areas:

$$(C_L - C_S)\, df = (1 - f_S) dC_L \qquad \text{Equation 5-6}$$

The segregation coefficient can be used to substitute in for $C_S$. Therefore, rearranging the linear approximation of the segregation coefficient (Equation 5-4) gives:

$$C_S = \frac{0.21 C_L}{1 - 0.78 C_L} \qquad \text{Equation 5-7}$$

Substituting Equation 5-7 into Equation 5-6, and integrating both sides results in Equation 5-8:

$$1 - f_S = \left(\frac{C_{seed}}{C_S}\right)^{\frac{1}{0.79}} \left(\frac{0.79 - 0.78 C_S}{0.79 - 0.78 C_{Seed}}\right)^{\frac{0.21}{0.79}} \left(\frac{0.78 C_S + 0.21}{0.78 C_{seed} + 0.21}\right) \qquad \text{Equation 5-8}$$

Where $C_{seed}$ is the solid composition at the edge of the seed. This is the complete mixing model, which in this case is valid for Ge compositions between 0.4 and 1.0, due to the linear simplification of the segregation coefficient (Equation 5-4). Appendix D details the full derivation of this equation.

Due to the assumption that the liquid has a uniform composition (i.e. complete mixing of the rejected Ge into the melt), this equation is also only valid when the regrowth propagation speed is low, or the strip length is small.

This model has been fitted to the straight strip data in Fig. 5-11 and Fig. 5-12. It can be seen that the model is a close match to the data, and within the tolerance of the Raman measurements. This suggests that for straight strips of this length, the regrowth propagation speed is low enough to allow complete mixing of the rejected Ge into the melt.

However, in order to grow device grade SGOI, it is desirable to achieve a uniform SiGe composition, to enable simpler fabrication to match device specifications. To date, this has not been demonstrated in the literature [24-28]. It is proposed that a uniform composition can be achieved by steady-state solidification, whereby there is limited diffusion in the liquid as a result of a higher regrowth front propagation speed.

#### 5.3.1.5 Steady-state solidification

In steady-state solidification there is only limited diffusion in the liquid, which is a more accurate model than either the Scheil equation, or the complete mixing model, when the regrowth speed is non-negligible. In steady-state solidification, diffusion of the rejected Ge at the regrowth front is balanced by the propagation of the regrowth front, therefore resulting in a uniform composition profile. Diffusion of Ge is given by Fick's second law:

$$\frac{dC_S}{dt} = D_L \frac{d^2C_S}{dx^2}$$

Also:

$$\frac{dC_S}{dt} = \frac{dC_S}{dx}\frac{dx}{dt} = v\frac{dC_S}{dx}$$

Where $D_L$ is the diffusivity of Ge in liquid SiGe, $v$ is the regrowth front propagation speed, and $x$ is the distance in the liquid with a non-uniform composition. This equation assumes a constant regrowth propagation speed. These equations combine to give Equation 5-9:

$$D_L\left(\frac{d^2C_S}{dx^2}\right) - v\left(\frac{dC_S}{dx}\right) = 0 \qquad \text{Equation 5-9}$$

This is a second order differential equation. Therefore, the solution is of the form:

$$C_S = \alpha e^{\beta x} + \gamma$$

The first and second order differentials of this equation are:

$$\frac{dC_S}{dx} = \beta\alpha e^{\beta x}$$

And

$$\frac{d^2C_S}{dx^2} = \beta^2\alpha e^{\beta x}$$

Substituting these two equations into Equation 5-9 gives (note the change in sign since Ge diffusion and regrowth are in the same direction):

$$D_L\beta^2\alpha e^{\beta x} + v\beta\alpha e^{\beta x} = 0$$

Which simplifies to:

$$\beta = \frac{-v}{D_L}$$

Substituting this into the general solution to a second order differential equation results in Equation 5-10:

$$C_S = \alpha e^{\left(\frac{-x}{D_L/v}\right)} + \gamma \qquad \text{Equation 5-10}$$

The boundary conditions for this equation are $C_S = C_0$ when $x = \infty$, and $C_S = C_L$ when $x = 0$. Substituting the boundary conditions into Equation 5-10 results in:

$$\gamma = C_0$$

And therefore:

$$\alpha = C_L - C_0$$

Substituting these back into Equation 5-10:

$$C_S = C_0 + (C_L - C_0)\, e^{\left(\frac{-x}{D_L/v}\right)}$$

Which becomes:

$$C_S = C_0 + \frac{C_0(1-k)}{k} e^{\left(\frac{-x}{D_L/v}\right)} \qquad \text{Equation 5-11}$$

This is the steady-state equation for alloy solidification, which is explained in Fig. 5-19.

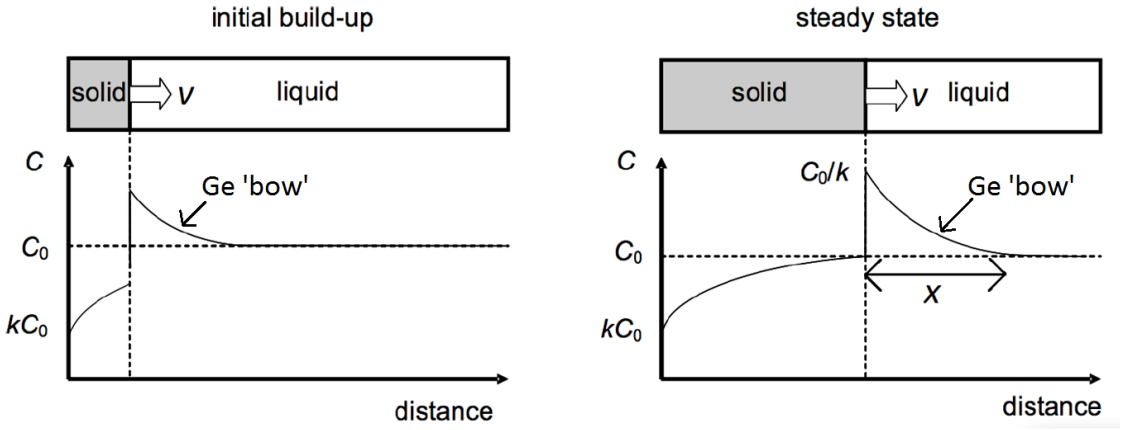


*Fig. 5-19. Steady-state solidification – adapted from [53].*

There is an initial transient period where the Ge 'bow' builds up at the regrowth front. This is formed because the Ge is rejected from the regrowth front, but not completely diffused into the bulk liquid, due to a faster regrowth propagation speed when compared to the complete mixing model. This results in a higher Ge composition at the regrowth front than in the bulk liquid. Once the solid composition reaches $C_0$, steady-state solidification is reached. This continues until near the end of the structure where $x$ becomes small, so that complete diffusion in the liquid is realised. At this point the composition profile becomes more like that predicted by the complete mixing model (Equation 5-8).

In order to predict the composition profiles using the steady-state equation, the simulation software on the University of Cambridge website "Dissemination of IT for the Promotion of Materials Science" [54] was used. This software enabled trends in the composition profile as the regrowth front propagation speed was increased to be observed, as shown in Fig. 5-20.

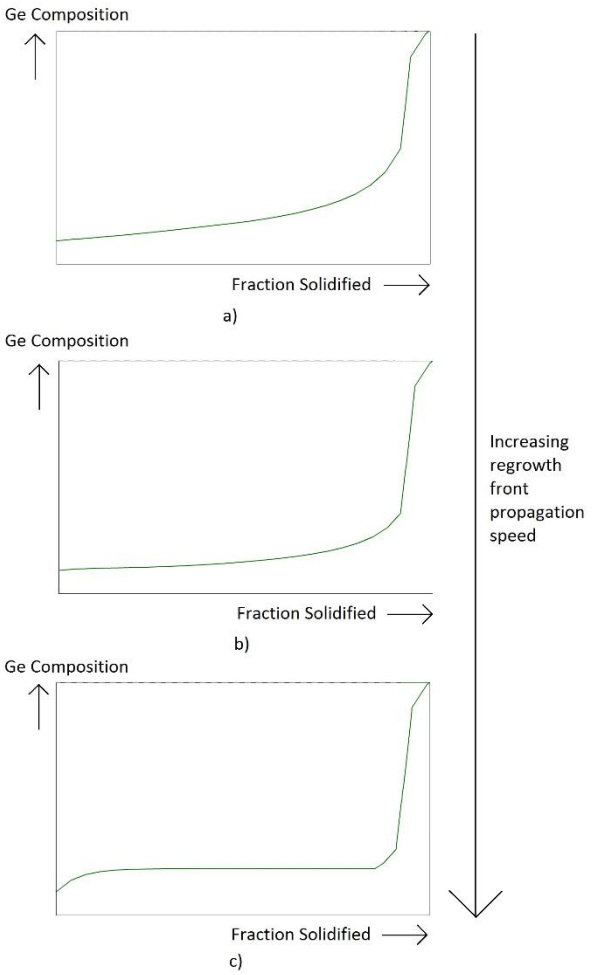


*Fig. 5-20. Simulations of Ge composition profiles using steady-state solidification [54].*
*Showing increasing regrowth front propagation speed from a) to c).*

From these simulations, it can be seen that as the regrowth front propagation speed increases, the composition profile becomes flatter. The quantitative speeds are not shown in Fig. 5-20 because they are extremely difficult to determine. This is because in Equation 5-11 the exponential term is:

$$e^{\left(\frac{-x}{D_L/v}\right)}$$

$D_L$ is a known constant, but *x* and *v* are dependent on one another. For example, if the regrowth speed is increased, the distance in the liquid with a non-uniform composition (i.e. *x*) will invariably decrease. Therefore *v* cannot be accurately quantified.

The composition profile becomes flatter at high regrowth front propagation speeds because the diffusion of the rejected Ge into the melt at the regrowth front, is balanced by the propagation of the regrowth front itself. This results in a 'bow' wave of rejected Ge being pushed along the strip, without diffusing into the bulk melt, until near the end of the strip, as shown in Fig. 5-19. Therefore, in order to achieve a uniform composition, it is necessary to maximise the regrowth front propagation speed. It follows that in order to maximise the regrowth front propagation speed, it is necessary to maximise the cooling rate of the SiGe structures after melting [55]. Since the cooling rate of the system used for RMG of straight strips is already at its maximum (after reaching the peak temperature the RTA lamps are switched off), it is necessary to increase the cooling rate by other means.

#### 5.3.1.6 Composition profiles of tailored structures

The graded composition profiles described above are of very limited use for the fabrication of electronic and photonic devices, where a uniform composition is usually required. Therefore, it is desirable to use the RMG technique in order to reap the benefits of the localised, single crystal SGOI platform, but to engineer a uniform composition.

In order to achieve a uniform composition, it can be seen from the above discussions that steady-state solidification must be realised, with a fast regrowth front propagation speed. In light of this, a tailored tree-like structure was designed, as shown in Fig. 5-21. The branches were added to the main central strip to act as radiating elements designed to increase the cooling rate of the structure, and therefore increase the regrowth front propagation speed along the central strip.

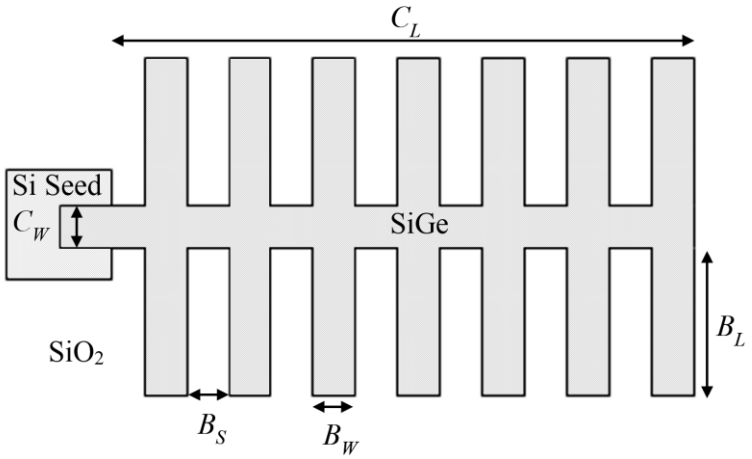


*Fig. 5-21. Schematic of a tailored tree-like structure. Dimensions are defined as: centre strip width = $C_W$, centre strip length = $C_L$, branch width = $B_W$, branch length = $B_L$, branch separation = $B_S$, and number of branches = n.*

An SEM image of a tailored tree-like structure is shown in Fig. 5-22.

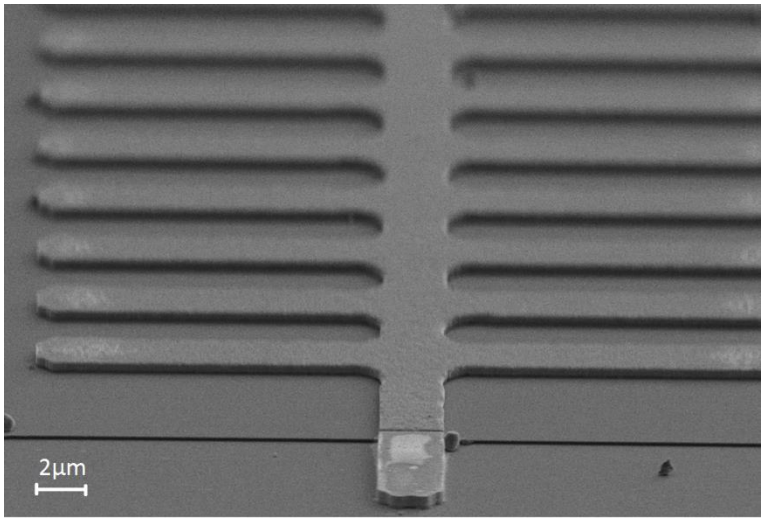


*Fig. 5-22. SEM image of a tailored tree-like structure.*

The structural parameters of the tree-like structure were varied, and the composition profiles in the central strips were measured by Raman spectroscopy.

Fig. 5-23 shows the composition profiles in the central strips of tree-like structures with a range of branch separations, and a fixed branch width and branch length. The main central strip is 100 µm long in all cases. The branch separation is reduced by adding additional branches ranging from $n = 4$ ($B_S = 25$ µm) to $n = 10$ ($B_S = 5$ µm).

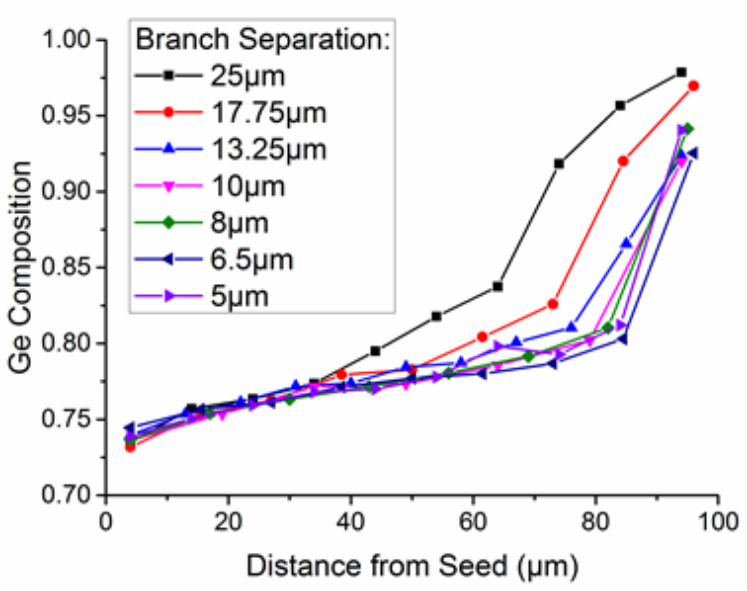


*Fig. 5-23. Ge composition as a function of distance from the seed for the central strip of tree-like structures with a range of branch separations. $C_W$ = 5 μm, $B_W$ = 5 μm, $B_L$ = 20 μm and $C_L$ = 100 μm. The total number of branches increases from 4 ($B_S$ = 25 μm) to 10 ($B_S$ = 5 μm). Estimated maximum SiGe temperature = 1030 °C.*

There is a clear change in the composition profile of these structures when compared with the straight strips in Fig. 5-11. This is attributed to the cooling effects of the branches, which means that there is no longer complete mixing in the liquid ahead of the regrowth front. Therefore, a flatter composition profile is achieved, until the end of the strip where the remaining distance left to solidify is short enough that complete mixing in the liquid occurs. It can be seen that there is negligible change in the composition profile when $B_S$ < 10 μm, meaning that the cooling rate capability of the branches must saturate at this point.

Fig. 5-24 shows the composition profiles in the central strip of tree-like structures with a range of branch lengths, and a fixed branch width and branch separation. As $B_L$ is extended, the composition profile in the central strip becomes flatter. This shows that increasing the branch length increases the cooling rate, which is expected due to the larger branch surface area leading to greater heat dissipation during cooling.

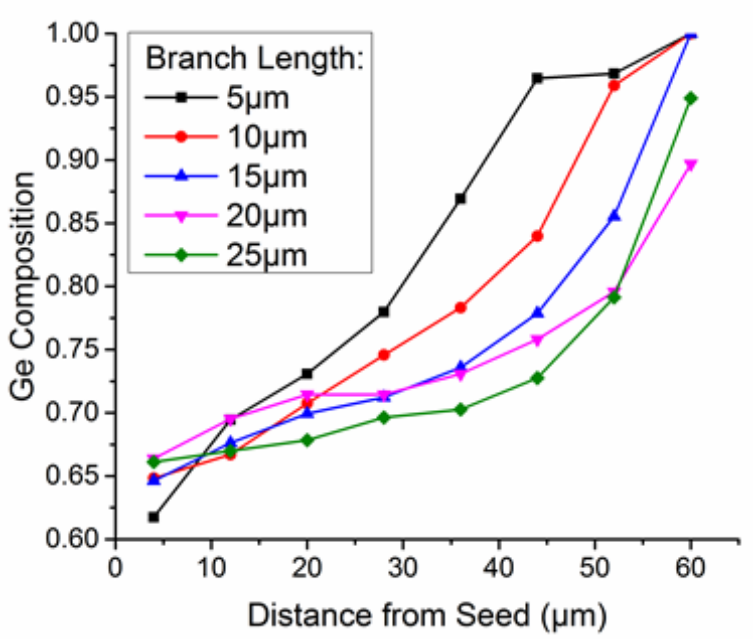


*Fig. 5-24. Ge composition as a function of distance from the seed for the central strip of tree-like structures with a range of branch lengths. $C_W$ = 5 μm, $B_W$ = 5 μm, $B_S$ = 3 μm and $C_L$ = 65 μm. Estimated maximum SiGe temperature = 1055 °C.*

Fig. 5-25 shows the composition profiles in the central strip of tree-like structures with a range of branch widths, and a fixed branch length. The branch separation varies between 3 μm for the widest branch ($B_W$ = 5 μm), to 7 μm for the narrowest branch ($B_W$ = 1 μm), in order to keep the total length of the tree-like structure constant ($C_L$ = 65 μm). This small variation in $B_S$ has been shown in Fig. 5-23 to have very little effect on the composition profile, so for the purposes of this discussion it will be neglected.

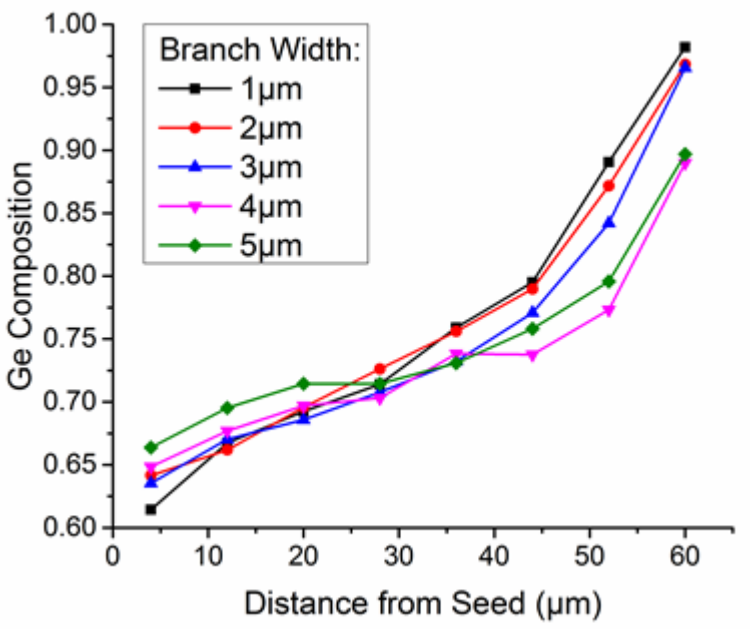


*Fig. 5-25. Ge composition as a function of distance from the seed for the central strip of tree-like structures with a range of branch widths. $C_W$ = 5 µm, $C_L$ = 65 µm and $B_L$ = 20 µm. $B_S$ = 3 µm to 7 µm so that there are the same number of branches on each structure (n = 8). Estimated maximum SiGe temperature = 1055 °C.*

It can be seen that whilst increasing $B_W$ leads to a slight flattening of the composition profile in the central strip, the effect is much less profound than increasing $B_L$ by the same proportion (i.e. $B_L$ = 5 µm to 25 µm and $B_W$ = 1 µm to 5 µm). This shows that the branch width is not the limiting factor to the cooling rate, but rather the branch length is.

In order to demonstrate the importance of the branch length over the branch width, Fig. 5-26 plots three different branch dimensions, each with the same total volume.

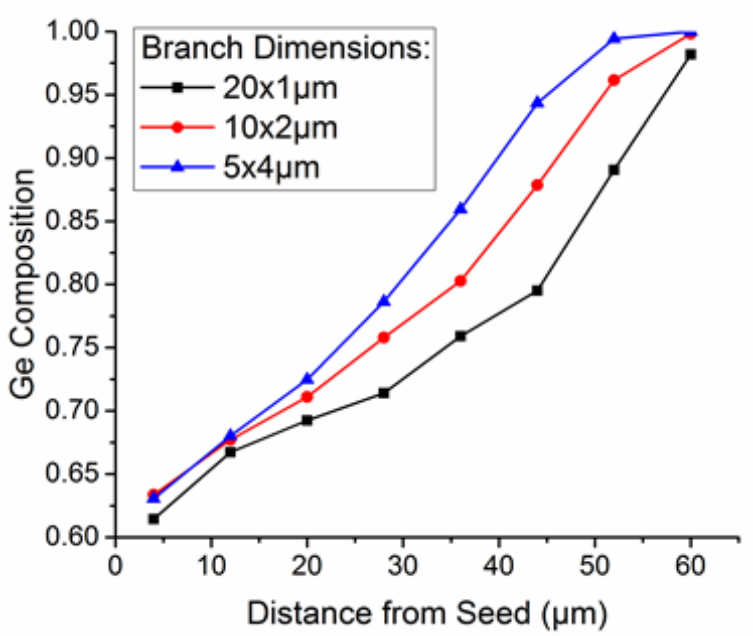


*Fig. 5-26. Ge composition as a function of distance from the seed for the central strip of tree-like structures with a fixed branch volume but different branch dimensions.*
*$C_W$ = 5 μm and $C_L$ = 65 μm. Estimated maximum SiGe temperature = 1055 °C.*

From Fig. 5-26, it can be concluded that the long, thin branches dissipate heat through thermal radiation much more efficiently than short, wide branches, due to the flatter composition profile. The long, thin branches have an increased surface area to volume ratio when compared with the short, wide branches. This means that a larger surface area is exposed to the cooler surroundings, which leads to increased heat dissipation (the surface area to volume ratios are 7.1, 6.1, and 5.7 for the 20x1 μm branches, 10x2 μm branches, and 5x4 μm branches, respectively). This increased heat dissipation leads to a larger cooling rate, and therefore a faster regrowth front propagation speed and flatter composition profile.

In the experiments detailed above, the composition profiles have been changed from that predicted by the complete mixing model observed with straight strips, to a flatter composition profile predicted by the steady-state solidification model. However, as shown in Fig. 5-20, in order to achieve a completely flat composition profile, it is necessary to further increase the cooling rate. In order to achieve this, the central strip width, $C_W$, was decreased from 5 μm to 3 μm. The composition profile of the complete tree-like structure is shown in Fig. 5-27.

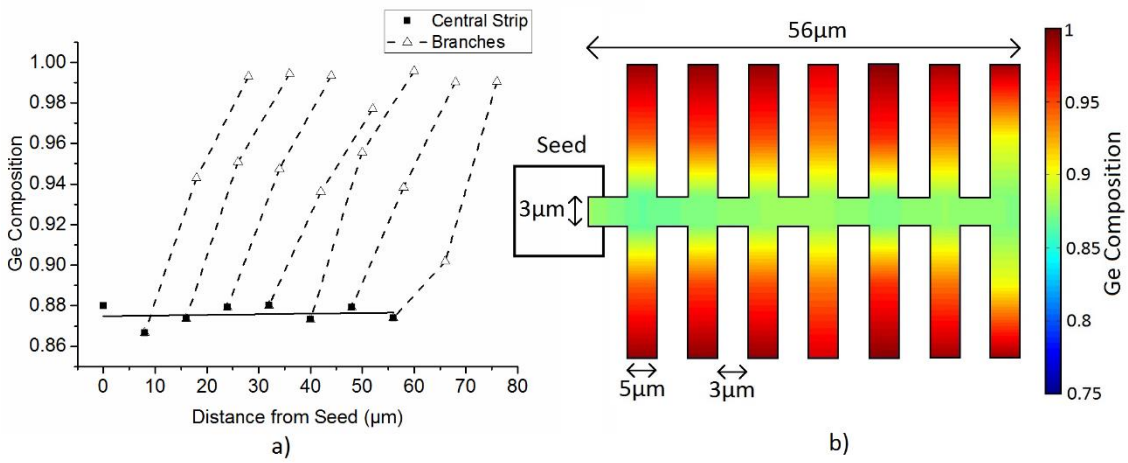


*Fig. 5-27. Composition profile of a tailored tree-like structure. a) Graph, b) schematic. $C_W$ = 3 μm, $C_L$ = 65 μm, $B_L$ = 20 μm, $B_W$ = 5 μm and $B_S$ = 3 μm. Estimated maximum SiGe temperature = 975 °C. The final set of branches have been omitted to display only the uniform composition region.*

Fig. 5-27 shows that a uniform composition can be achieved in the central strip of a tree-like structure, when the central strip width is reduced to 3 μm. Only the first 56 μm of the central strip of the tree-like structure has been plotted, as this is the uniform composition region. The SiGe becomes Ge rich after this length because solidification has passed the penultimate set of branches, and therefore the cooling effects of the branches are diminished. Additionally, the remaining length of the strip left to solidify becomes small, so complete mixing in the melt ahead of the regrowth front is realised. The branches display a graded composition profile, similar to that of a straight strip, which suggests that the central strip solidifies first, and then subsequently acts as a seed for the regrowth of the branches. The composition profiles in the branches does not match the complete mixing model, which suggests that the regrowth front propagation speed is too fast for complete mixing of the rejected Ge ahead of the regrowth front to occur. This could be due to an increased cooling rate of the entire structure when compared with a straight strip.

Fig. 5-28 plots the composition profile of both a straight strip, and the central strip of a tree-like structure with the same dimensions, in order to emphasise the change in composition profile with the addition of the branches.

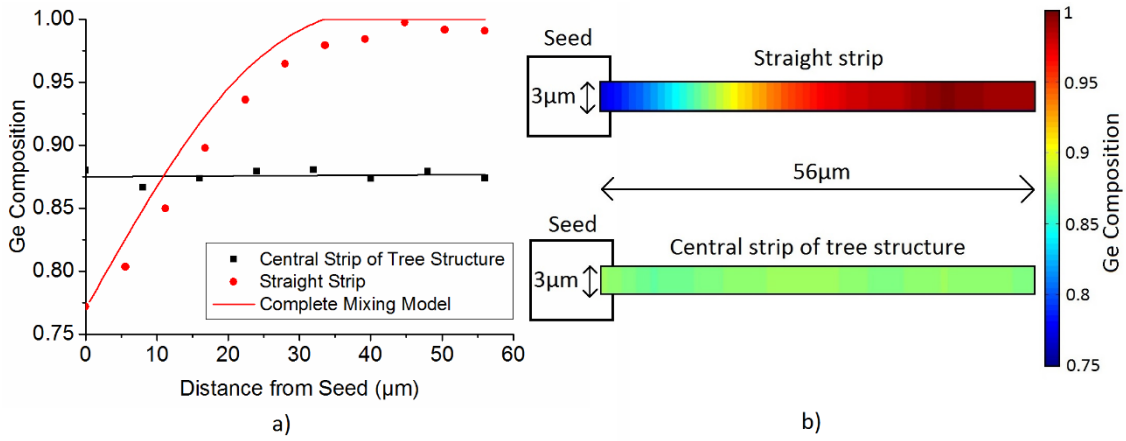


*Fig. 5-28. Comparison of composition profiles of straight strip and central strip of tailored tree-like structure.*
*a) Graph, b) schematic. The final set of branches have been omitted from the central strip of the tailored tree-like structure to display only the uniform composition region. The straight strip data has been standardised using data from the 10 μm, 20 μm, 50 μm, and 100 μm length strips in order to match the length of the tailored tree-like structure. The complete mixing model has been fitted to the straight strip data [28]. A linear fit has been added to the tailored tree-like structure data.*

### 5.3.1.7 Composition tuning by anneal temperature

After demonstrating a uniform composition profile through the use of tailored tree-like structures, it is desirable to be able to tune the composition in the central strip. This is to enable the RMG method to be used for a host of device designs, with a range of SiGe compositions.

One method of tuning the composition is to modify the anneal temperature during the RMG process. A higher anneal temperature leads to greater Si diffusion into the SiGe structure before solidification commences, as per the phase diagram shown in Fig. 5-5. This is demonstrated in Fig. 5-29.

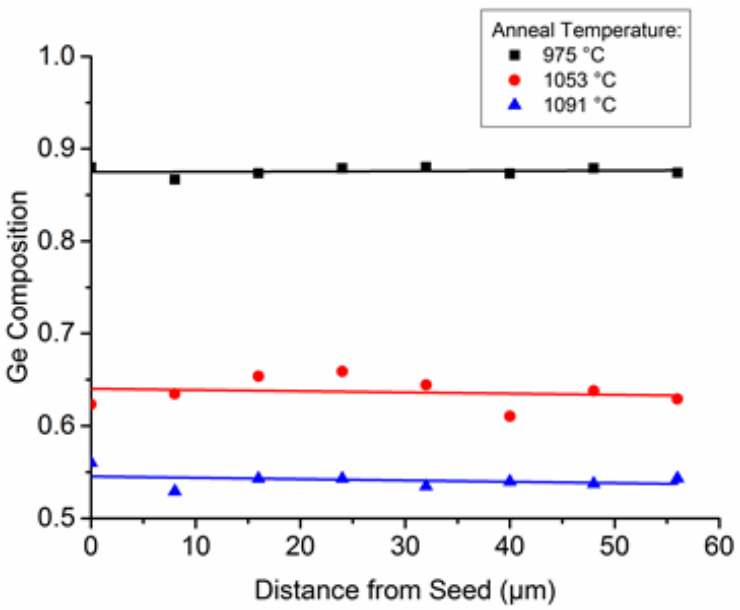


*Fig. 5-29. Composition profiles in the central strips of tailored tree-like structures annealed at a range of temperatures.*
*$C_W$ = 3 μm, $C_L$ = 65 μm, $B_L$ = 20 μm, $B_W$ = 5 μm and $B_S$ = 3 μm. Only the first 56 μm of each tree-like structure has been considered to display only the uniform composition region. A linear fit has been added to each data set.*

Fig. 5-29 shows that a uniform composition is achieved at all three of the anneal temperatures. As expected, a higher anneal temperature leads to a lower Ge composition, therefore enabling composition tuning by anneal temperature modification. This is further demonstrated in Fig. 5-30, where the average Ge composition over the first 56 μm of the central strip of the tree-like structures has been plotted as a function of anneal temperature.

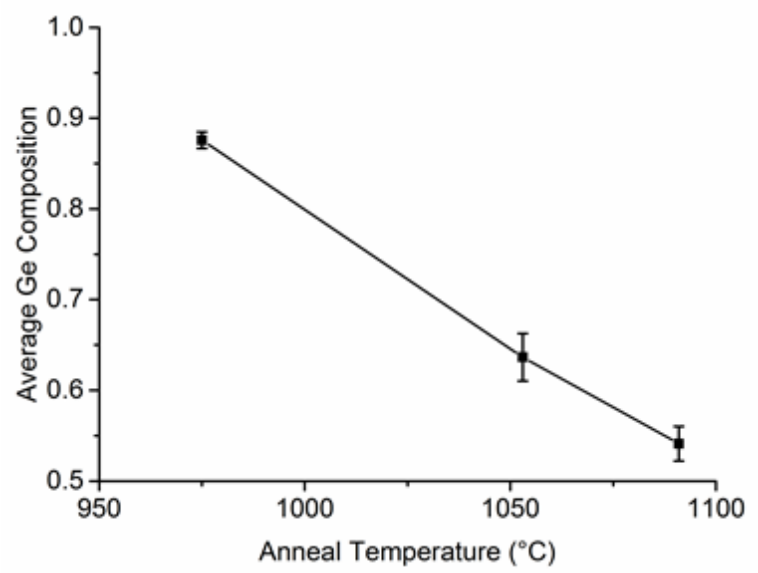


*Fig. 5-30. Average Ge composition along the central strip of a tailored tree-like structure as a function of anneal temperature.*
*Only the uniform region up to 56 µm has been considered for the average composition calculations. The error bars show the maximum and minimum values observed along each strip.*

### 5.3.1.8 Composition tuning by structural design

The ability to tune the composition by modifying the anneal temperature during the RMG growth is very useful. However, it does not enable multiple SiGe compositions to be achieved on the same wafer, since only a single anneal temperature per wafer can be used. It is desirable to be able to tune the uniform composition across a single wafer, so that each SiGe region can be adjusted to the specific design requirements determined by the device under fabrication.

It has already been shown in section 5.3.1.6 that the composition profile in the central strip of a tailored tree-like structure can be adjusted by modifying the structural design of the branches. Therefore, in order to grow multiple uniform SiGe compositions on the same wafer, the tailored tree-like structures described above have been combined with a straight strip, to incorporate the graded composition profile of the straight strip with the uniform composition profile of the central strip of the tree-like structures. This novel tailored structure results in a range of tuneable uniform compositions, as shown in Fig. 5-31.

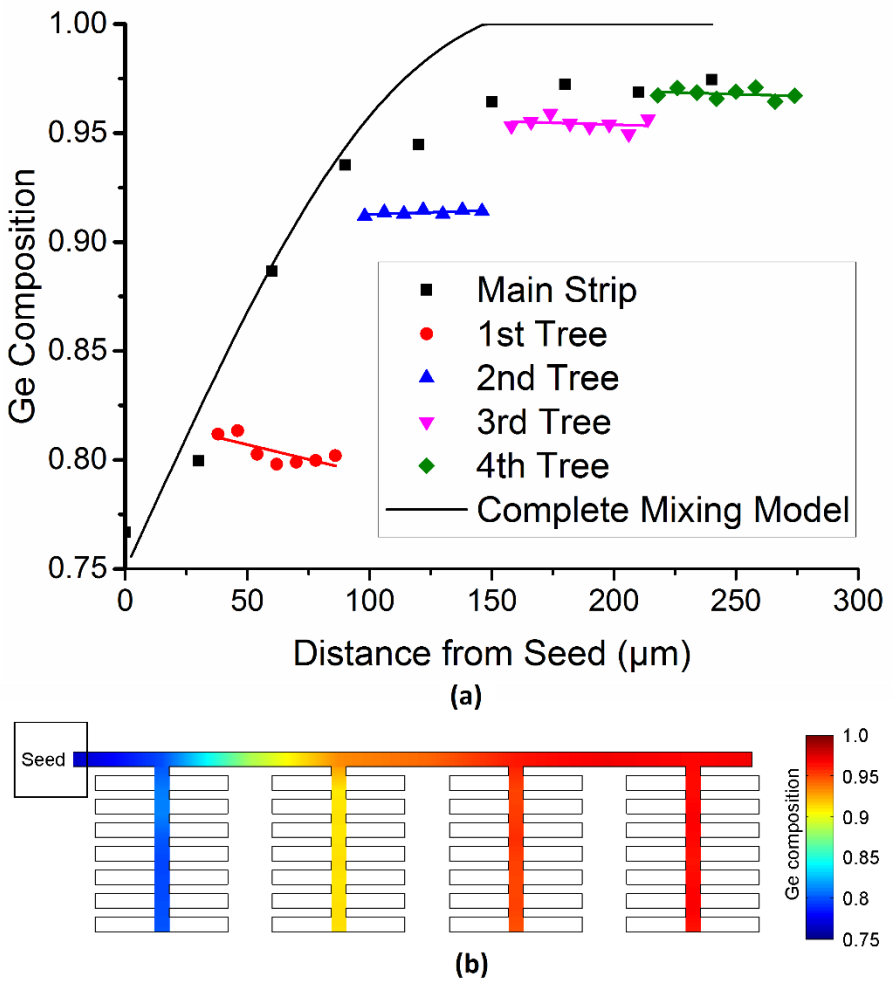


*Fig. 5-31. Ge composition as a function of distance from the seed for a straight strip with a series of attached tree-like structures.*
*Tree dimensions: $C_W$ = 3 μm, $B_W$ = 5 μm, $B_L$ = 20 μm, $B_S$ = 3 μm, $C_L$ = 65 μm. Main strip dimensions: width = 5 μm and length = 230 μm. Trees are located at positions 30 μm, 90 μm, 150 μm, and 210 μm along the main strip. The final set of branches on each tree have been omitted to display only the uniform composition regions. The white regions in b) have not been measured as in practice they would be etched away, leaving only the uniform composition SiGe. Estimated maximum SiGe temperature = 1017 °C. The main strip has been fitted with the complete mixing model [28]. The central strip of each tree-like structure has a linear fit.*

This structure demonstrates a Ge composition of 81%, 92%, 95%, and 97% in the central strip of the first, second, third, and fourth tree-like structures, respectively. The standard deviations of the 7 measured points in each tree-like structure are 0.006, 0.008, 0.004, and 0.002, respectively, showing that the

composition can be controlled to within 1% of the mean (which is within the measurement error), over a 56 μm length, using this method.

The main strip does not adhere to the complete mixing model, which could be due to incomplete mixing of the Ge into the melt ahead of the regrowth front, as a result of the increased SiGe volume caused by the addition of the tree-like structures. It could also be due to the slightly increased cooling rate with the addition of the tree-like structures (which act as radiating branches).

This design has the potential to be extremely powerful for SGOI growth as it enables a multitude of uniform compositions to be achieved using a single growth step, therefore allowing a large degree of design freedom across a single wafer.

### 5.3.2 Auger electron spectroscopy

In order to confirm the integrity of the data gathered by Raman spectroscopy, Auger electron spectroscopy (AES) was also performed. Firstly, the top capping $SiO_2$ layer was removed using a 20:1 HF wet etch. AES was then performed using a Thermo Scientific Microlab 350 Scanning Auger Microscope, with a spot size of 20 nm. High resolution Ge and Si spectra were collected from 650-1205 eV and 1300-1650 eV, respectively. The air formed surface oxide and surface C contamination were removed with 20 seconds of Ar ion sputtering. A linear background subtraction is performed over the peak ranges, which is necessary as the large background distorts the true peak intensity. Fig. 5-32 shows an example AES spectrum, with the Si and Ge peaks marked.

The exact composition was not determined using this characterisation technique. Instead, the Si:Ge peak ratios (peaks found at approximately 1615 eV and 1145 eV respectively) were used because it is expected that this ratio closely relates to the SiGe composition [56]. The Si:Ge peak ratio profiles for a straight strip and the central strip of a tree-like structure have been plotted, with the SiGe:GeGe Raman integrated mode intensities for ease of comparison, in Fig. 5-33. The profiles shown are indicative of the Si concentration, as opposed to the Ge concentration in all of the other figures thus far. The reason for this is that the AES Si peak at low Si concentrations is very close to the noise floor, and

therefore a plot indicative of Ge concentration (i.e. Ge:Si peak ratio) is extremely noisy.

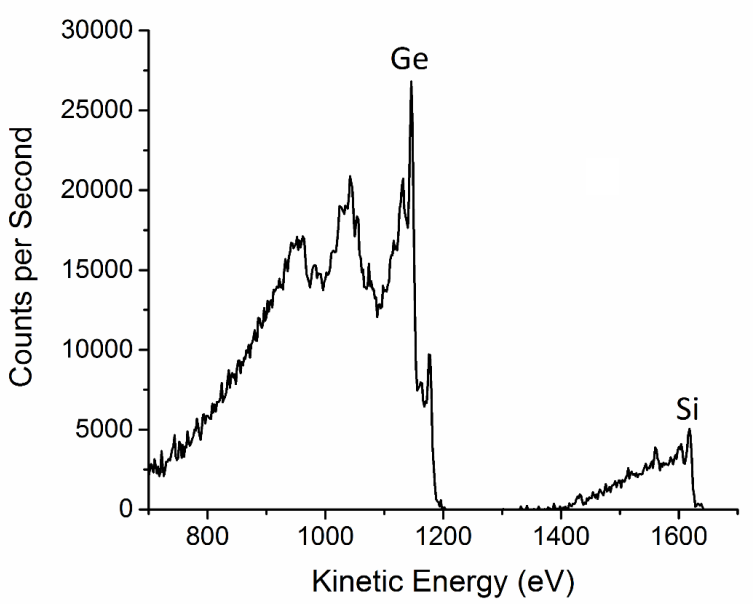


*Fig. 5-32. Example AES spectrum.*

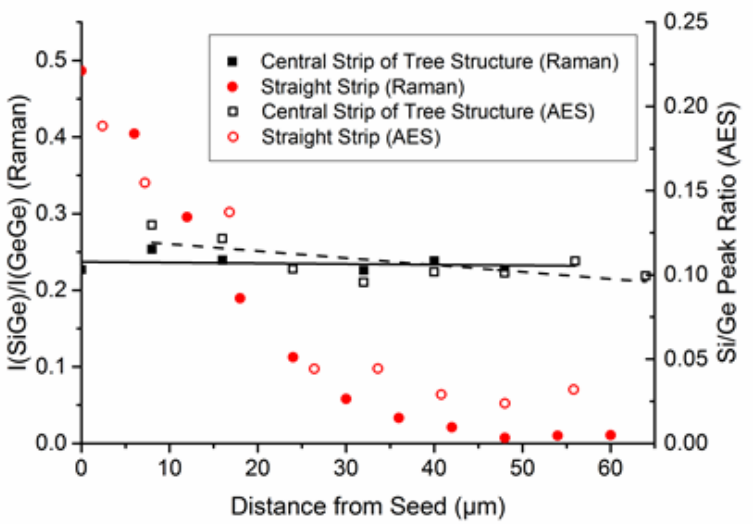


*Fig. 5-33. Comparison of Raman and AES data for a straight strip and the central strip of a tree-like structure.*
*A linear fit has been applied to the central strip data sets for both the AES and Raman. The solid symbols relate to the Raman measurements on the left hand scale, and the hollow symbols relate to the AES measurements on the right hand scale.*

This figure establishes that the AES data is in close agreement with the Raman data. The small discrepencies between the Raman and AES measurements can be attributed to the difficulty in extracting the Si peak from the AES

measurements for high Ge compositions, because the signal is very close to the noise floor. It may also be due to the difference in spot size (approximately 500 nm for Raman and approximately 20 nm for AES) or penetration depth (several tens of nm for Raman and several nm for AES) of the two characterisation techniques.

### 5.3.3 Transmission electron microscopy

Transmission electron microscopy (TEM) has been performed to image a cross section of a SiGe tree-like structure, both within the seed area, and also along one of the branches. The locations of the TEM cross-sections are shown in the plan view SEM image in Fig. 5-34a. The cross section TEM lamellae were prepared by EAG Labs using an in-situ focused ion beam (FIB) lift out technique. For protection, the samples were coated with local e-beam and ion-beam platinum prior to FIB milling.

Threading dislocations, caused by the lattice constant mismatch between Si and Ge, are clearly observed in the TEM images but are confined to the seed area (Fig. 5-34b), and do not propagate along the SiGe structure (Fig. 5-34c to Fig. 5-34f). The high resolution cross-section images (Fig. 5-34d and Fig. 5-34f) confirm single crystal, defect free SGOI fabrication using this RMG method. Ge diffusion into the Si substrate can also be observed in Fig. 5-34b.

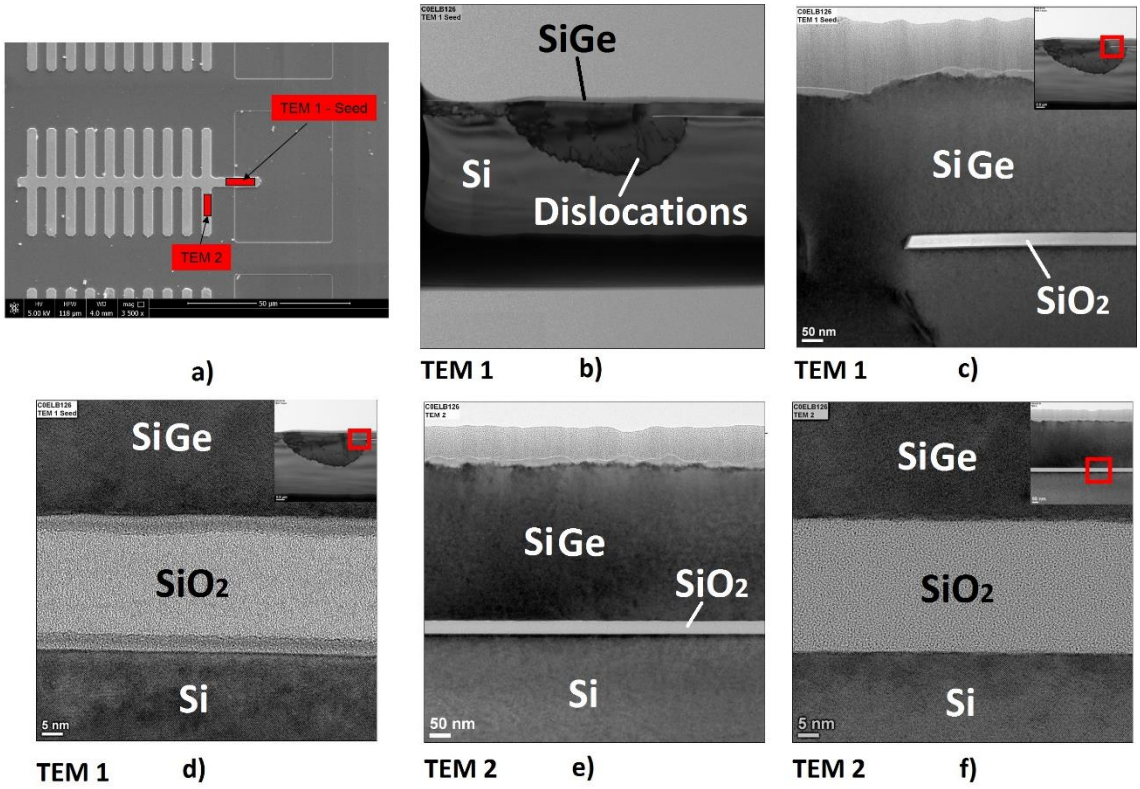


*Fig. 5-34. **C**ross-section TEM images of RMG SiGe in both the seed area and along a branch.*

*a) Plan view SEM image showing the 2 locations from which the TEM-ready lamella were prepared, b) cross-section TEM in the seed area showing Ge diffusion into the Si, and threading dislocations confined to the seed area, c) high resolution cross-section TEM at the seed edge, showing no dislocations propagating along the SiGe strip, d) ultra-high resolution cross-section TEM image at the seed edge, showing single crystal SiGe formation, e) high resolution cross-section TEM image along the first branch, with no dislocations apparent, f) ultra-high resolution cross-section TEM image along the first branch, showing single crystal SiGe formation. The layer on top of the SiGe in all images is e-beam platinum, which has been added for protection during FIB milling.*

### 5.3.4 Electron backscatter diffraction

Electron back-scatter diffraction (EBSD) measurements have also been performed in order to confirm the crystal orientation of the RMG tailored tree-like structures, as shown in Fig. 5-35. These measurements were also performed by

EAG Labs. The sample surface was etched with a gallium ion beam, prior to EBSD imaging, to remove any surface contamination.

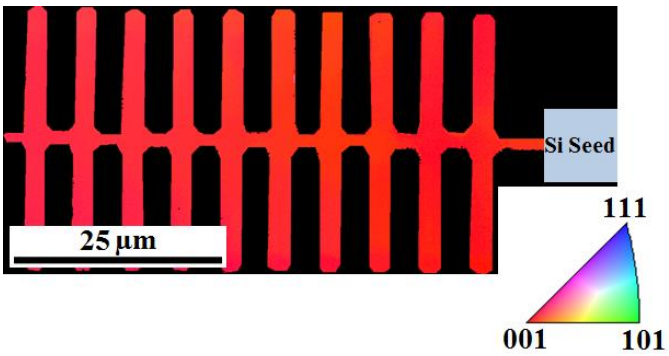


*Fig. 5-35. EBSD scan of a tailored tree-like structure.*

Fig. 5-35 displays a plan view crystal orientation map of a tree-like structure. The colour is representative of the measured crystal orientation, as shown by the inset scale diagram. Therefore, as the tree-like structure contains only a single colour, it can be concluded that the entire structure is single crystal. The crystal orientation matches that of the Si substrate. This confirms that continuous lateral regrowth has been realised because the Ge was initially grown on $SiO_2$, and therefore is not expected to have only a single crystal orientation, since it had no crystal template during initial growth.

## 5.4 Rapid melt growth from polycrystalline Si seeds

It is also possible to perform RMG from polycrystalline Si (poly-Si) seeds, rather than bulk Si seeds. In order to do this, the fabrication steps detailed above were repeated with a slight modification to the seed formation steps. A thick 2 µm $SiO_2$ layer was first deposited onto a bulk Si wafer using PECVD. A 100 nm poly-Si layer was then deposited onto this $SiO_2$ layer by hot-wire chemical vapour deposition (HWCVD). This poly-Si layer was then patterned using standard UV photolithography and ICP etching. The remaining RMG fabrications steps were then carried out as described above in section 5.2. This process is summarised in Fig. 5-36.

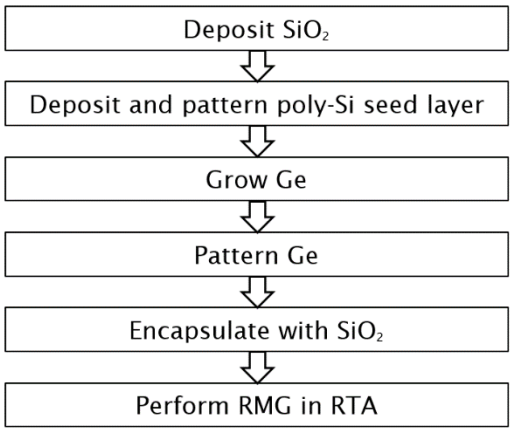


*Fig. 5-36. Poly-Si seed RMG fabrication summary.*

Miyao *et al.* [20, 21] note that the resultant structure is still single crystal, most commonly (100). This is possibly due to a faster regrowth speed of this crystal orientation compared to other crystal orientations. Fig. 5-37 shows an SEM image of a straight strip grown from a poly-Si seed. The polycrystalline nature of the SiGe is clearly visible within the seed area, after which no grains are visible.

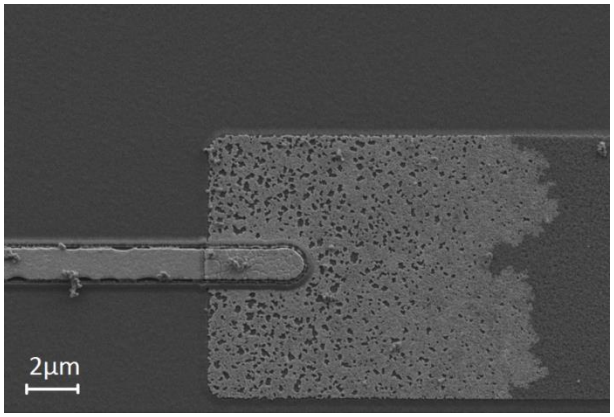


*Fig. 5-37. SEM image of a RMG SiGe straight strip from a poly-Si seed.*

Ge diffusion from the strip into the seed area is also clearly visible. This then agglomerates upon melting, due to the high interface energy with the encapsulating $SiO_2$ layer. The remainder of the poly-Si seed retains its structure as it is not melted in the RMG process.

Closer inspection of a tree-like structure reveals an insight into the regrowth of these structures. An SEM image is shown in Fig. 5-38.

The poly-Si seed deposited on a thick (2 µm) $SiO_2$ layer does not have the heat sinking capabilities of a bulk Si seed, resulting in a slower regrowth front propagation speed in the SiGe structure. The result is that random nucleation

occurs in the liquid SiGe ahead of the regrowth front. Fig. 5-38 suggests that the central strip of the structure regrows first, due to the low nucleation count, and only then the branches regrow, due to the high nucleation count in the branches. This backs up the same conclusion made earlier from the composition profiles. The nucleation count also increases in branches that are further away from the seed. These observations also support the hypothesis that the branches act as cooling elements, since it is apparent that they regrow after the central strip.

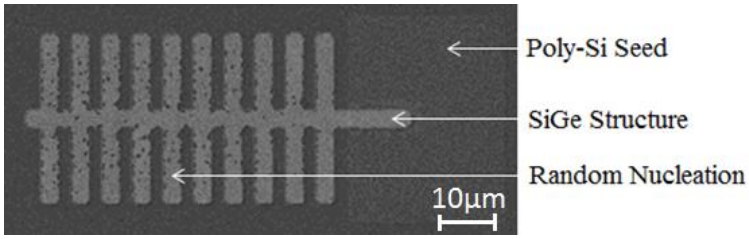


*Fig. 5-38. SEM image of RMG SiGe tree-like structure from a poly-Si seed.*

The SiGe composition profiles in these structures are not displayed here, since there is limited Si diffusion from the seed due to its relatively small volume. This makes RMG from poly-Si seeds suitable for pure Ge growth for multilayer applications. However, it is beneficial to have a bulk Si seed, for both SiGe growth and pure Ge growth, if possible since the crystal orientation can be controlled with the use of a bulk Si seed.

## 5.5 Rapid melt growth conclusions

In conclusion, the simple method described here for the fabrication of localised SGOI structures could act as the blueprint for the coexistence of next generation SiGe electronic and photonic devices on the same wafer, using a variety of substrates such as bulk Si or SOI. The SiGe composition engineering that produces single crystal, high quality, SiGe layers could enable the fabrication of a multitude of devices requiring different compositions of SiGe, such as wavelength division multiplexing (WDM) applications, on the same wafer, in a single deposition step and a single anneal step. Thanks to this methodology, the composition of SiGe can now be varied according to the anneal temperature and/or the material structure, enabling SiGe composition engineering dictated by structural design, and not by the deposition or growth mechanism. This method leads to a simplified (single deposition) fabrication process, providing a path for the seamless integration of electronics and photonics at a low cost.

# Chapter 6: Ge photodetectors

## 6.1 Motivation and applications

One of the essential building blocks of any Si photonics circuit is a photodetector; a device that converts the received optical signal into an electronic signal for computational processing. A discussion of the theory behind photodetection and the important performance characteristics is provided in Chapter 2, and an in depth review of the state-of-the-art in Ge photodetector technology can be found in Chapter 3.

Ge is an ideal candidate for photodetector applications in Si photonics systems as it is already part of the CMOS production line [1]. It has a direct band gap of 0.8 eV, enabling detection at both of the most commonly used telecommunications wavelengths, i.e. 1.3 μm (zero dispersion) and 1.55 μm (low loss). Ge photodetectors can be utilised not only in telecommunications but also, amongst others, for applications in sensing and medical lab on a chip devices [2].

The fabrication of photodetectors grown by plasma enhanced chemical vapour deposition (PECVD) (see Chapter 4) offers a low cost, low temperature option. Rapid melt growth (RMG) is also an attractive growth method for photodetectors, because the high quality layers (see Chapter 5) have the potential to improve device characteristics such as dark current and quantum efficiency. This chapter discusses the fabrication of waveguide integrated photodetectors using both PECVD and RMG Ge growth techniques.

## 6.2 Device design

All photodetectors were fabricated on 6 inch silicon-on-insulator (SOI) wafers, with a 400 nm Si overlayer and 2 μm buried oxide (BOX) layer. Throughout this chapter, all Ge growth is performed using recipe C (details in Chapter 4). This recipe was selected, ahead of the higher quality recipe F and recipe G, due to the Ge delamination observed for these recipes on $SiO_2$ surfaces. Ge

delamination from $SiO_2$ surfaces renders the material unsuitable for RMG. In order to make a direct performance comparison between the as grown PECVD photodetectors and the RMG photodetectors, the same growth recipe was used for all devices.

In an attempt to simplify fabrication, the PECVD and RMG photodetectors were also designed with the same masks. This meant that due to the nature of the RMG technique, along with other fabrication limitations, some restrictions on the photodetector device design are enforced:

1. When performing RMG the Ge is laterally grown on a thin $SiO_2$ layer, therefore eliminating the ability to use a vertical heterogeneous device design. A homogeneous lateral device with an ion implanted junction is therefore required.
2. The maximum Ge strip width achievable with RMG is 5 μm in order to avoid Ge agglomeration during the melting process. Therefore, the total photodetector device width is limited to 5 μm.
3. The minimum intrinsic region width, *W,* is 0.5 μm due to fabrication limitations and alignment tolerances.

A butt coupled design has been selected firstly because the thin $SiO_2$ layer in between the Si and Ge layers could reduce the evanescent coupling efficiency in alternative designs, and secondly because it enables shorter, and therefore lower capacitance devices. In order to achieve a butt coupled design, a trench is etched into the Si overlayer. After Ge growth, the majority of the Ge is etched leaving Ge only in the Si trenches. A range of device widths (*W*) and lengths (*L*) have been fabricated, as detailed in Table 6-1. Fig. 6-1 shows a simplified schematic of the butt coupled photodetector.

*Table 6-1. Photodetector design variations.*

| | Minimum (μm) | No. of intermediate values (non-uniform step size) | Maximum (μm) |
|---|---|---|---|
| Intrinsic width (*W*) | 0.5 | 4 | 1.5 |
| Intrinsic length (*L*) | 3 | 3 | 15 |

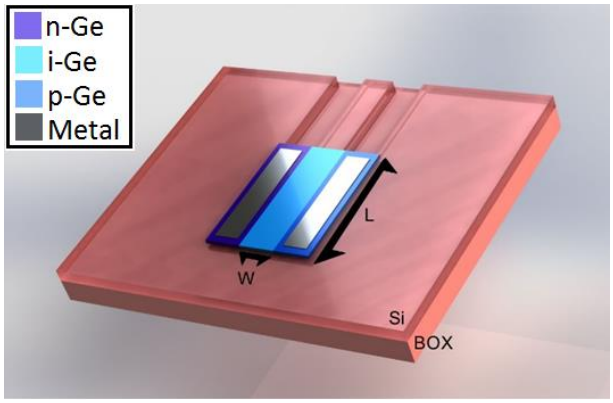


*Fig. 6-1. Schematic of photodetector design.*

A complete listing of the fabrication steps for the PECVD photodetectors is detailed in Appendix A. The RMG photodetectors process flow can be found in Appendix B.

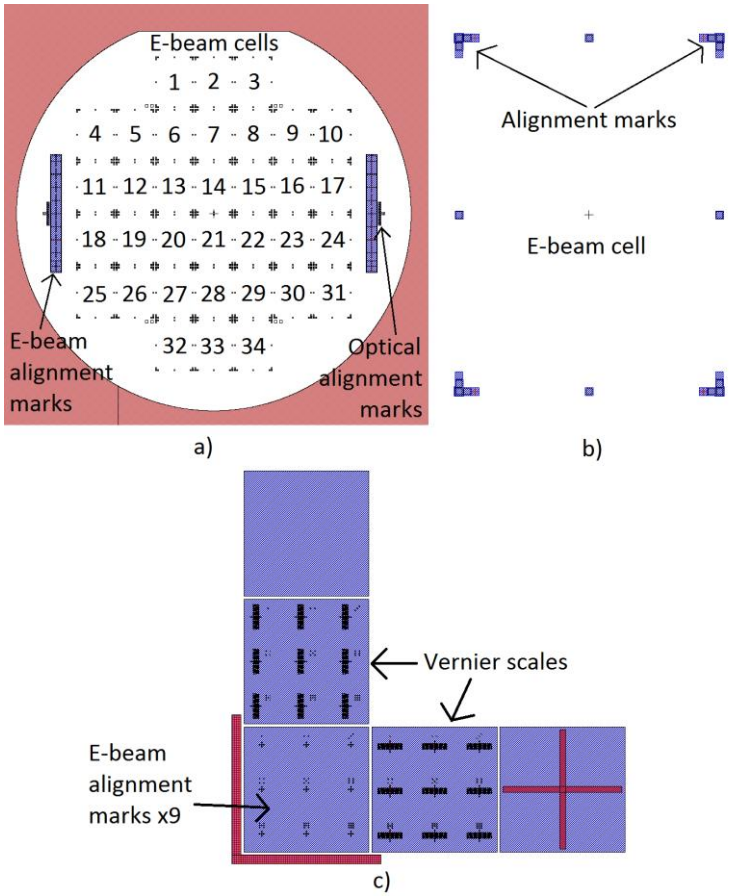


*Fig. 6-2. Photodetector wafer layout.*
*a) 6 inch wafer layout showing 34 individual cells, as well as e-beam lithography and photolithography wafer scale alignment marks, b) layout of each individual cell with 6x e-beam alignment mark groups, c) 9x e-beam alignment marks on each cell for multiple mask layers, as well as Vernier scales for both x and y misalignment measurements.*

The complete process required 3 (PECVD photodetectors) or 4 (RMG photodetectors) photolithography masks, and 6 e-beam lithography masks. The alignment errors for photolithography masks and e-beam lithography masks are approximately 1 μm and <100 nm, respectively. Therefore photolithography is only used for the non-critical layers, where a small alignment error is tolerable, such as the seed etch for the RMG and the metal lift-off for electrode pads (which are subsequently defined to ground-signal-ground (GSG) electrodes by e-beam lithography). Photolithography is also used to define the alignment marks, as shown in Fig. 6-2. A total of 34 individual 20x15 mm cells can be included on each wafer (Fig. 6-2a).

## 6.3 Process development

Prior to device fabrication, the majority of the fabrication steps had to be developed to meet the required specification. This section briefly describes the process development that was carried out. As a result of the time constraints of this project, the process development was generally carried out a few steps ahead of the process flow of the device wafers.

### 6.3.1 Ge etch

More details of the Ge etch development process can be found in Chapter 4. Nevertheless, the etch recipe had to be tested for AZ2070 negative resist, which was found to have better adhesion to Ge than AZ5214E negative resist. The 4 μm thick AZ2070 was written by e-beam lithography. The etch profile is shown in Fig. 6-3, displaying near vertical sidewalls and no undercut.

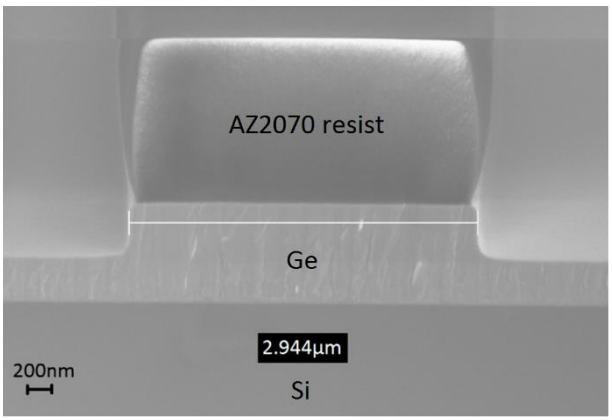


*Fig. 6-3. SEM image of Ge etch using 4 μm thick AZ2070 resist, written by e-beam lithography.*

### 6.3.2 Rapid melt growth

A study of RMG is carried out in Chapter 5. However, the process had to be tested on SOI wafers. The presence of the insulating 2 μm $SiO_2$ layer changes the thermal properties of the substrate, and therefore affects the cooling rate. A range of temperatures between 927 °C and 1090 °C were tested and subsequently observed using an optical microscope, as shown in Fig. 6-4.

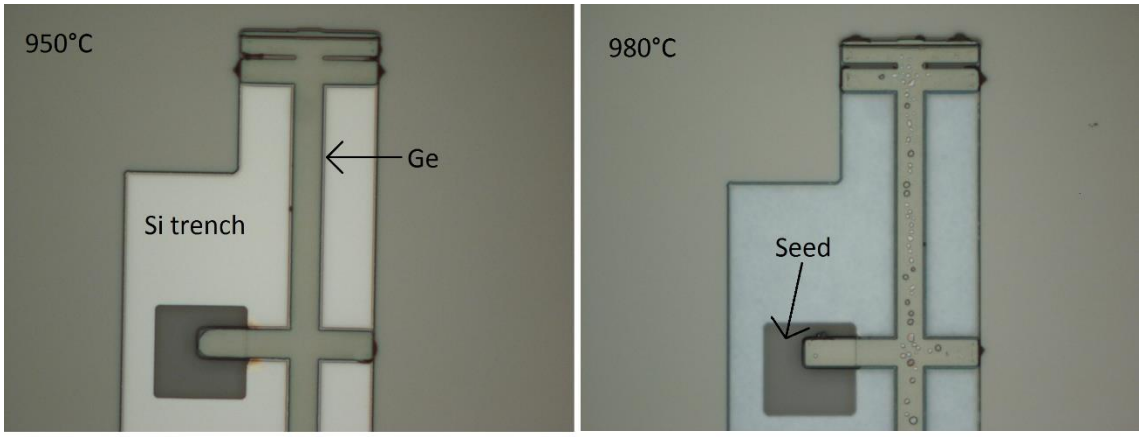


*Fig. 6-4. Optical microscope images of RMG Ge for photodetector device fabrication.*
*a) x20 image after 950 °C (measured temperature) anneal, showing no Ge agglomeration, b) x20 image after 980 °C (measured temperature) anneal showing, Ge agglomeration.*

It was found that the optimum anneal temperature was 950 °C (measured temperature). Above this temperature, Ge agglomeration became apparent and voids began to form in the Ge layer (Fig. 6-4b). This is different behaviour to the RMG performed on bulk Si wafers in Chapter 5, which can be attributed to the insulating effects of the BOX layer. This is concluded because the Ge layer in Fig. 6-4 is very similar in appearance to those grown using polycrystalline Si seeds on a thick $SiO_2$ layer.

Raman spectroscopy measurements of the Ge layer show very low Si concentrations, even in areas close to the seed. This may be due to the very thin (approximately 40 nm) Si layer from which the Ge is regrown, as shown in Fig. 6-5. The Si seed is only 40 nm thick because RMG is performed in an etched trench in order to enable butt coupling from a Si waveguide into the Ge photodetector.

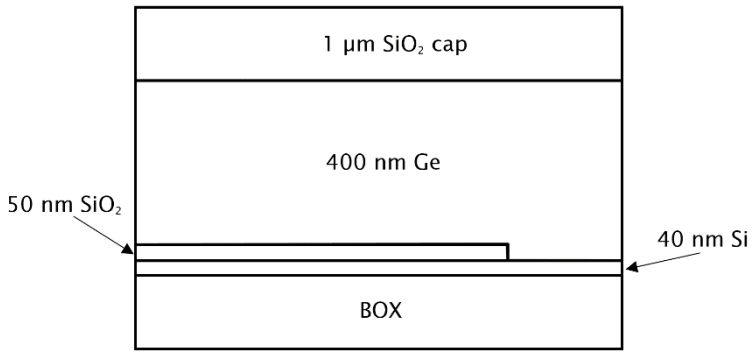


*Fig. 6-5. Schematic of RMG in thinned SOI trenches.*

### 6.3.3 Si etch

A Si etch was required to form the waveguides which couple the light into the photodetectors, as well as to form the Si trenches and alignment marks in the first fabrication steps. Due to the similarities in chemistry between Si and Ge, the same etch recipe was used with very similar results. The waveguide and grating layers were written by e-beam lithography using ZEP resist. The Si etch depth was 220 nm for optimal grating coupler performance. The Si trenches and alignment marks were defined using S1813 photoresist and ultra-violet (UV) photolithography.

### 6.3.4 $SiO_2$ etch

An $SiO_2$ etch was required to etch vias in the passivation layer to enable metal contacts to the Ge. In this case it is desirable to have slightly angled (approximately 70-80°) sidewalls to achieve better step coverage when the metal is sputtered onto the wafer. Fig. 6-6 compares an $SiO_2$ etch using a Plasmatherm Versaline deep etching tool and a standard inductively couple plasma (ICP) etching tool. After completion of the $SiO_2$ etch, a metal layer (50 nm Ti + 450 nm Al) has been sputtered onto the surface to observe the step coverage.

The etch in Fig. 6-6a uses $CF_4$ as the precursor gas, and the etch in Fig. 6-6b uses $CHF_3$ and Ar as the precursor gases. It can be seen that the step coverage of the metal is much better when the $SiO_2$ etch angle is decreased from 90° (Fig. 6-6a) to 80° (Fig. 6-6b). Therefore, the ICP etch was selected for photodetector fabrication. However, a problem that was discovered with this etch was that the etch rate was dependent on the feature size (via size).

A 1x1 mm opening was used to measure the etch depth using ellipsometry, but upon inspection by cross-section scanning electron microscope (SEM) it was found that the smaller vias (the smallest being approximately 3x1.5 μm) were not fully etched, whereas the large 1x1 mm openings were. In light of this, a 1 minute 20:1 HF etch was used after ICP etching to remove the remaining $SiO_2$ from the small vias, and ensure a smooth Ge surface for metal contact.

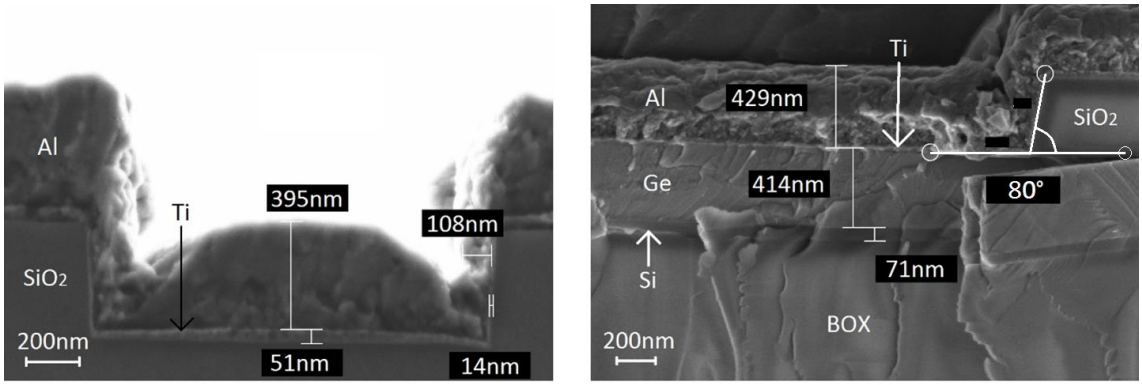


*Fig. 6-6. Cross-section SEM images of $SiO_2$ etch using Plasmatherm deep etching tool and ICP etching tool.*
*a) $SiO_2$ etch using Plasmatherm tool showing vertical sidewalls, which leads to poor metal step coverage, b) $SiO_2$ etch using ICP tool showing improved metal step coverage due to the increased angle of the $SiO_2$ etch.*

### 6.3.5 Metal sputtering

A Ti/Al metal stack was selected for the formation of electrodes, similar to that used by the ePIXfab service [3]. The Ti acts as an adhesion layer, onto which Al is sputtered due to its lower resistivity [4]. A Leybold Optics HELIOS sputtering tool was used to deposit 50 nm Ti, followed by 450 nm Al. The Ti was sputtered by applying 8000 W radio frequency (RF) power with an Ar flow of 30 sccm. For the Al, it is desirable to have small grain size, and low surface roughness, to enable simpler etching of narrow trenches to define the electrodes. A simple sputtering study was carried out by varying the DC power (Fig. 6-7) and the Ar flow (Fig. 6-8), and characterising the surface roughness and grain size by atomic force microscopy (AFM).

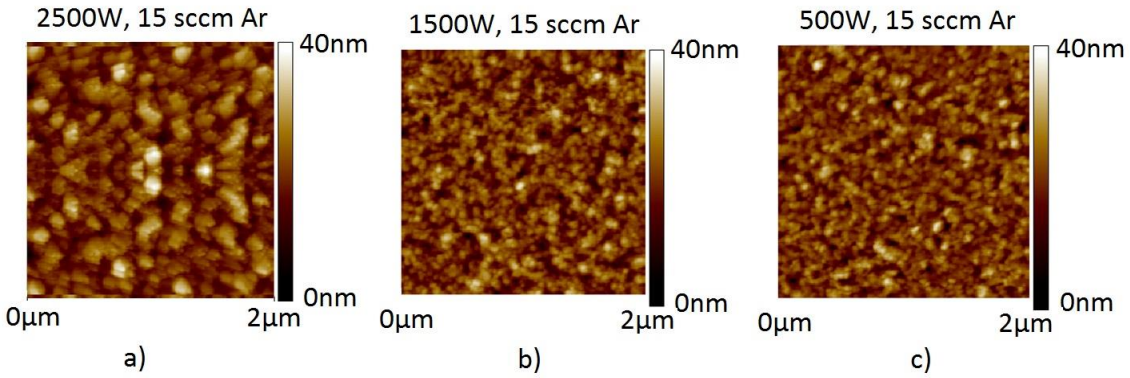


*Fig. 6-7. AFM surface roughness plots of sputtered Al for various DC powers.*
*a) 2500 W, b) 1500 W, c) 500 W, all depositions have 15 sccm Ar flow.*

These AFM images show that decreasing the DC power from 2500 W to 500 W decreased both the grain size, and the surface roughness, with an Ar flow of 15 sccm.

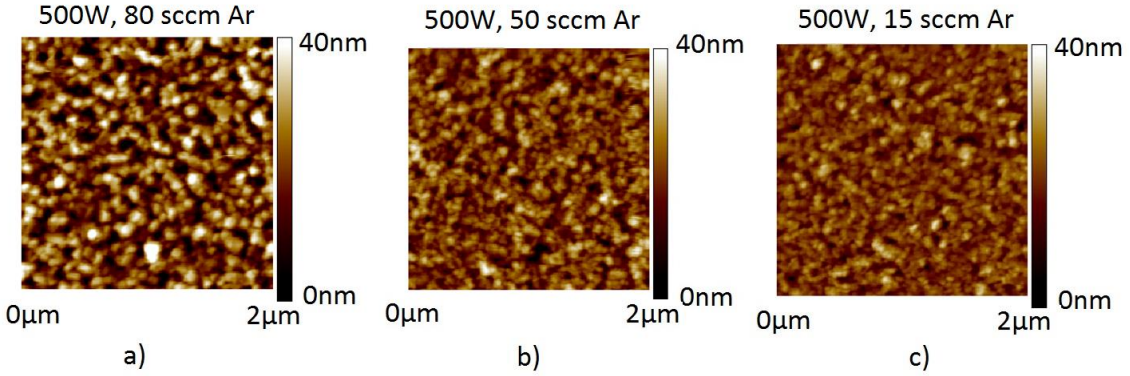


*Fig. 6-8. AFM surface roughness plots of sputtered Al for various Ar flows.*
*a) 80 sccm, b) 50 sccm, c) 15 sccm, all depositions have 500 W DC power.*

These AFM images show that a smoother layer with smaller grain size is achieved at the lowest Ar flow. Therefore, an Al sputter with 500 W DC power and 15 sccm Ar flow was selected for electrode fabrication. Although both of the trends suggest a lower power and lower gas flow would be beneficial, below these values the plasma becomes unstable and the process becomes unreliable.

### 6.3.6 Metal etch

Another process that required developing was a metal etch that is used to define the electrodes. An ICP etch study using S1813 photoresist was performed by varying the precursor gases as follows (based on recipes on the Oxford Plasma Technology website [5]): etch recipe 1: 10 sccm Ar, 20 sccm $Cl_2$, etch recipe 2: 10 sccm Ar, 20 sccm HBr, etch recipe 3: 10 sccm Ar, 10 sccm $Cl_2$, 10 sccm HBr. It was found that the recipe with the steepest sidewalls was etch recipe 2 (10 sccm Ar, 20 sccm HBr), as shown in Fig. 6-9. Steep sidewalls are desirable for the metal etch to ensure the metal conducting path is broken for very narrow trenches, such as that between the two terminals of the photodetectors.

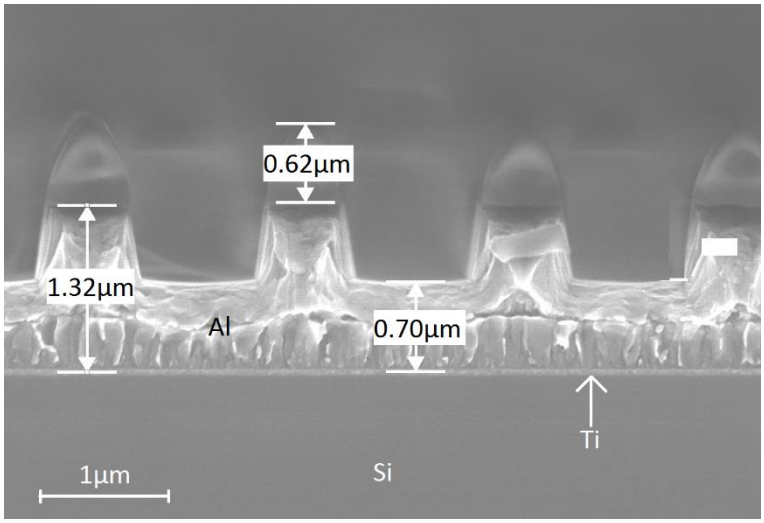


*Fig. 6-9. Al ICP etch using S1813 photoresist.*

However, as the alignment for the metal etch was critical, e-beam lithography was required. When this recipe was repeated with PMMA e-beam resist (which was selected due to its greater thickness than ZEP), large quantities of polymer build-up was apparent on the sidewalls. This resulted in the electrode etch that separates the signal pad from the ground pad being unsuccessful, as shown in Fig. 6-10.

In light of this difficulty, it was necessary to use ZEP e-beam resist, instead of PMMA. In order to achieve the required thickness of resist for etching 500 nm of metal, a double layer of ZEP was successfully used.

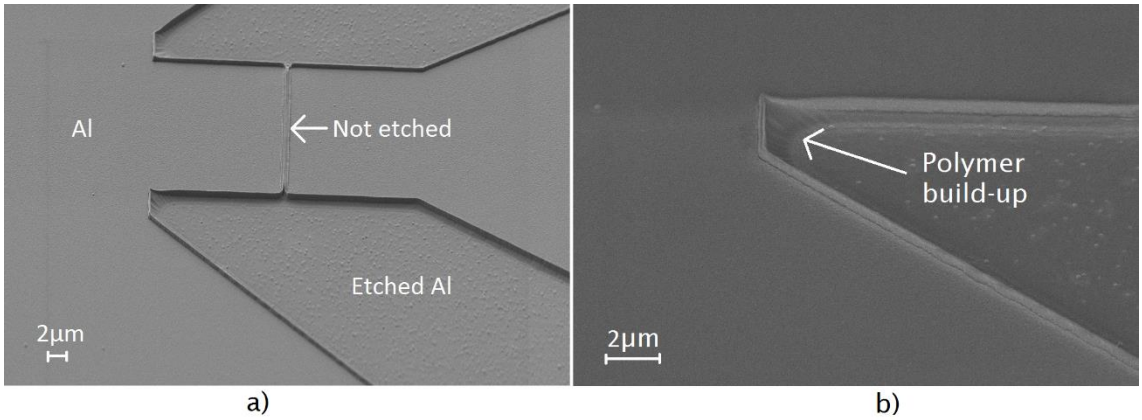


*Fig. 6-10. Al ICP etch using PMMA e-beam resist.*
*a) Centre of electrode etch showing failure to break contact between signal and ground pads, b) polymer build-up at the edge of mask features.*

### 6.3.7 Transmission line measurements

In addition to the photodetector devices, some transmission line measurement (TLM) wafers were fabricated in unison in order to characterise the metal contacts and doping profiles.

All fabrication was carried out on 400 nm Si overlayer, 2 µm BOX SOI wafers. The Si overlayer was thinned down to 50 nm by ICP etching to ensure a direct correlation with the photodetector wafers. The process flow then mirrored the photodetector wafers, as summarised in Fig. 6-11.

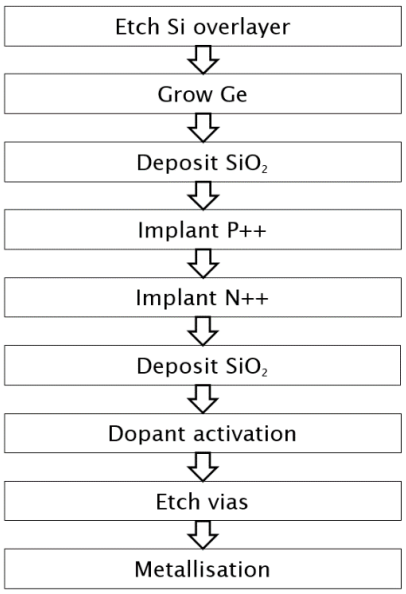


*Fig. 6-11. Process flow for TLM test wafers.*

As alignment was not critical for these wafers optical masks were used for all layers.

### 6.3.7.1 Implant simulations and characterisation

In order to define the *p-i-n* junction in the Ge layer, ion implantation through a mask is performed. Boron is used for the P++ regions and phosphorus is used for the N++ regions. Implantation simulations were carried out using the Silvaco Athena process simulation software [6]. Athena provides a convenient platform for the simulation of many common processes used within the semiconductor industry, such as lithography, etching, and oxidation. It is also regularly used for the modelling of implantation profiles, particularly in Si, but also in Ge.

The two main variables in the simulations are the acceleration energy and the dose. The acceleration energy controls the depth of the implant at the expense of lattice damage to the substrate. The dose controls the quantity of ions incident upon the surface. For both the P++ and N++ regions, a shallow implant is desired in order to limit Ge lattice damage, and limit the lateral deflection of energetic implanted ions. The simulation results are shown in Fig. 6-12 (P++) and Fig. 6-13 (N++). The thin $SiO_2$ layer on top of the Ge is to help removal of the resist after implantation (after both implants have been carried out an HF etch is performed to strip the $SiO_2$ layer, along with any resist residue).

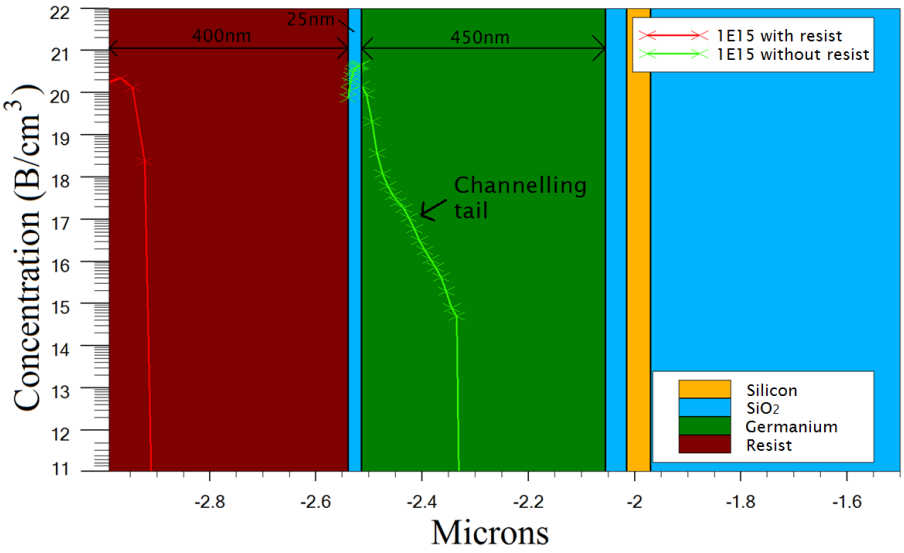


*Fig. 6-12. Silvaco Athena simulation of boron P++ implant.*

The red line indicates the implant profile with resist, and the green line represents the implant profile without resist. It can be seen that a resist thickness of 400 nm is sufficient to act as a mask. A maximum boron concentration of $3x10^{20}$ $cm^{-3}$ is achieved at the Ge surface. From this simulation, it appears that the implant depth is greater in the Ge than in the resist. This effect is unexpected due to the higher density of Ge when compared with resist. However, it can be explained by a channelling effect in the Ge, as a result of its crystal structure. This is confirmed by simulating the same implant conditions with amorphous Ge in order to remove the channelling effect. The resultant implant depth in amorphous Ge was found to be lower than resist.

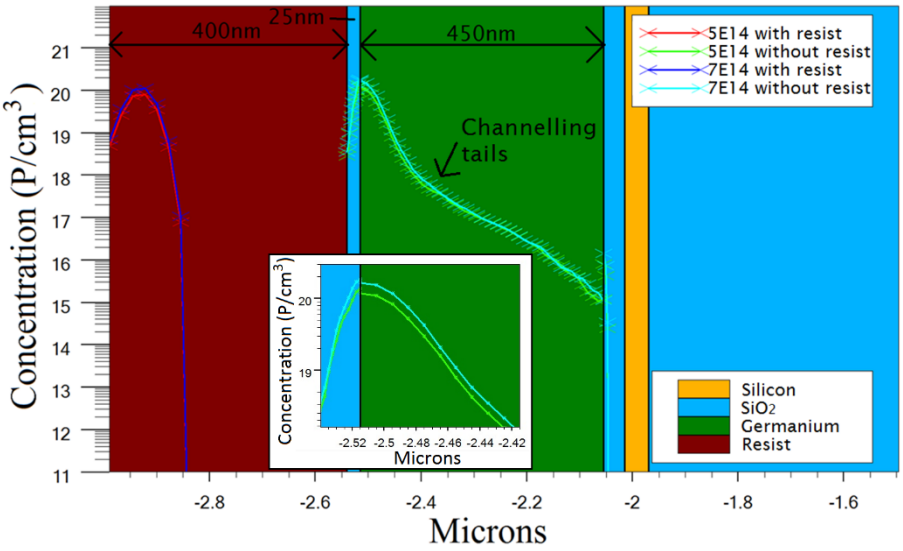


*Fig. 6-13. Silvaco Athena simulation of phosphorus N++ implant with different doses.*
*Inset is a zoomed graph of the Ge surface to show the profiles of the different implants.*

The phosphorus N++ implant achieves a maximum concentration of $2x10^{20}$ $cm^{-3}$ at the Ge surface with an implant dose of $7x10^{14}$ $cm^{-2}$, and a concentration of $1.5x10^{20}$ $cm^{-3}$ with an implant dose of $5x10^{14}$ $cm^{-2}$. As with the P++ implant, a channelling tail is observed in the Ge.

For the TLM wafers the dose of $5x10^{14}$ $cm^{-2}$ was used. However, for the photodetectors both doses were used, as per the variations described below in Table 6-2.

After implantation the wafers were annealed in a rapid thermal annealer (RTA) in order to activate the dopants, and repair some of the damage caused to the Ge lattice by the energetic ion collisions. One wafer was annealed at 580 °C, and the other at 600 °C, both for 39s. The dopants are expected to diffuse a few tens of nanometres with this anneal [7].

After activation, the dopant depth profiles in the 600 °C anneal temperature wafer were analysed by secondary mass ion spectroscopy (SIMS), as shown in Fig. 6-14 (P++) and Fig. 6-15 (N++). Only the 600 °C anneal temperature wafer was analysed due to the improved dopant activation at this temperature, when compared with 580 °C, as described in section 6.3.7.2, below.

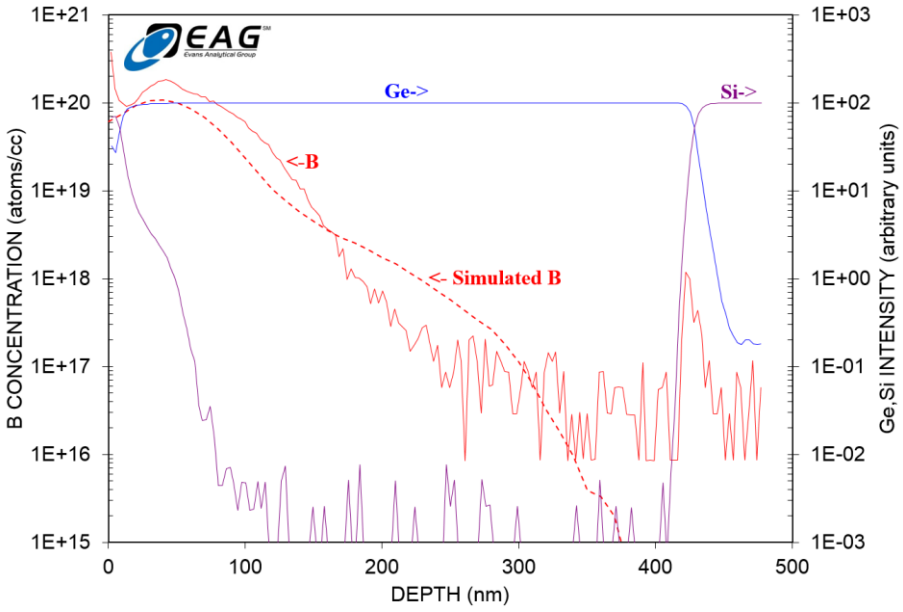


*Fig. 6-14. SIMS doping profile of boron P++ region after annealing at 600 °C.*

The maximum boron concentration achieved was approximately $2x10^{20}$ $cm^{-3}$ within the first 50 nm of the Ge. The dopant depth profile agrees well with the simulations (Fig. 6-12).

The maximum phosphorus concentration achieved with a dose of $5x10^{14}$ $cm^{-2}$ was approximately $1x10^{20}$ $cm^{-3}$. Again, the doping profile agrees well with the simulations (Fig. 6-13). Any minor differences between the measured implant profiles and the simulated implant profiles can be attributed to two small discrepancies in the simulations, and also dopant diffusion during the subsequent 600 °C anneal. Firstly, the simulated implant was performed through

a 25 nm thermal $SiO_2$, whereas the actual implants were performed through a 25 nm PECVD $SiO_2$. A PECVD $SiO_2$ layer is less dense than a thermal $SiO_2$ layer, and therefore the actual implants are expected to be slightly deeper. Secondly, the simulated implants assumed a perfect single crystal Ge layer, whereas in reality the Ge layer is defective. As a result of this, the ion collisions in the Ge layer will differ, and the resultant profiles will not be the same.

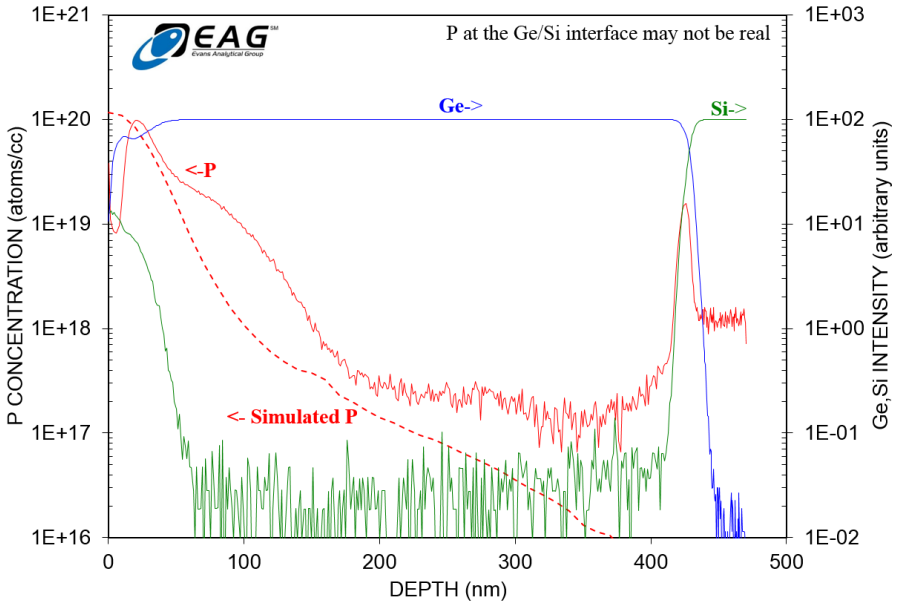


*Fig. 6-15. SIMS doping profile of phosphorus N++ region after annealing at 600 °C.*

### 6.3.7.2 Resistance characterisation

The sheet resistance of the doped regions and the contact resistance can be calculated by measuring the IV characteristics of a number of conducting tracks, with a range of lengths, as shown in Fig. 6-16a (P++) and Fig. 6-17a (N++). From these IV plots, the resistance of each length of track can be calculated by taking the reciprocal of the gradient. The track length can then be plotted against resistance, as shown in Fig. 6-16b (P++) and Fig. 6-17b (N++).

A linear fit has been added to both the N++ and P++ track length against resistance graphs, because it is expected that the resistance, *R*, would increase linearly with length, as per Equation 6-1:

$$R = \frac{\rho L}{A} \qquad \text{Equation 6-1}$$

Where $\rho$ is the resistivity of the doped Ge layer, $L$ is the track length, and $A$ is the cross-sectional area. However, this is clearly not the case, as shown by the exponential fit to the data. This suggests that surface leakage current, possibly in the form of trap assisted tunnelling current caused by the unterminated dangling bonds at the Ge-$SiO_2$ interface [8], is prevalent. Therefore, it is not possible to extract the sheet resistance or the contact resistance from these graphs, as it is expected that the surface acts as the main conducting path between contacts, and not the bulk of the doped layer.

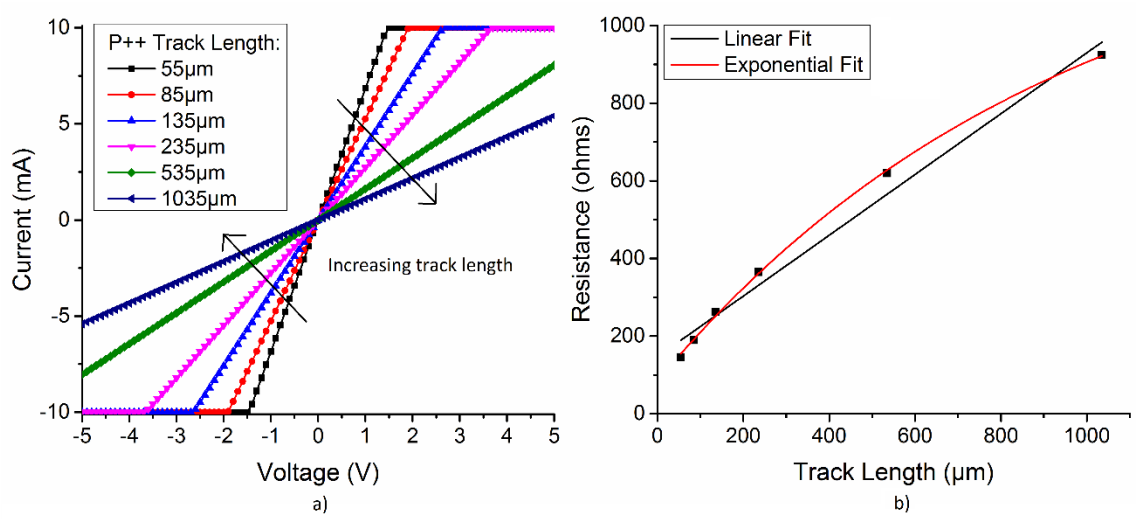


*Fig. 6-16. P++ TLM measurements.*
*a) IV plots for various track lengths, b) resistance as a function of track length showing expected linear fit, as well as exponential fit.*

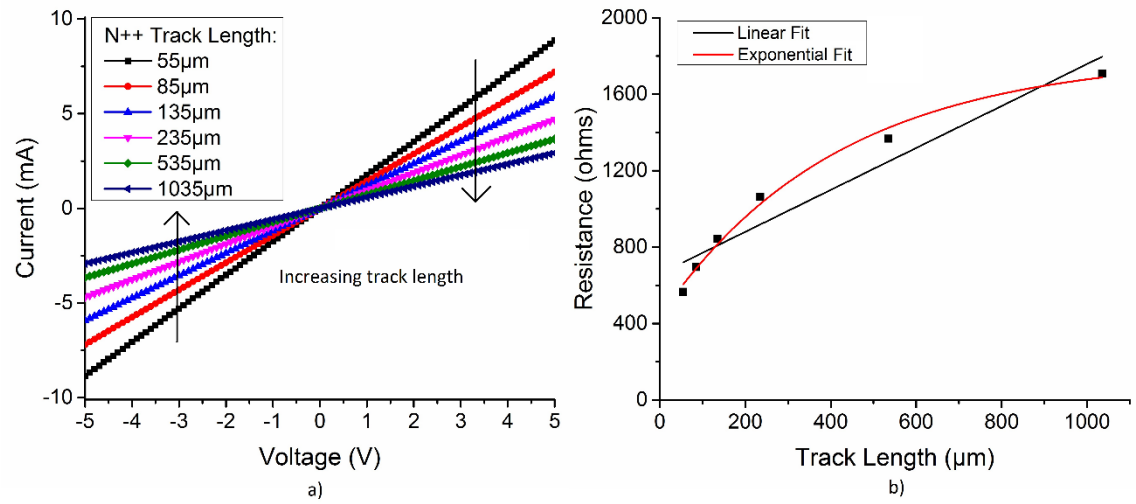


*Fig. 6-17. N++ TLM measurements.*
*a) IV plots for various track lengths, b) resistance as a function of track length showing expected linear fit, as well as exponential fit.*

In light of this, Ge thermal oxidation at 500 °C for 10 minutes using an RTA in an oxygen environment [9] was carried out on some of the photodetector wafers, after ion implantation had been performed. The aim of this was to reduce the surface leakage current, as demonstrated in [8, 10, 11]. This temperature was selected as it was sufficient to grow a thin (approximately 10 nm) $GeO_2$ layer that is predicted to significantly reduce dark current [8, 12], but also induce negligible dopant diffusion [7].

As a result of this study, it was also discovered that the resistance of the N++ tracks decreased by a factor of 5 when the dopants were activated at 600 °C when compared with 580 °C. However, there was a negligible difference between the P++ tracks at the two anneal temperatures. Therefore, an anneal temperature of 600 °C was selected for the photodetector dopant activation.

## 6.4 Photodetector fabrication process

In total, 5 wafers for RMG photodetectors and 3 wafers for PECVD photodetectors were processed. Small variations in processing were implemented, as summarised in Table 6-2. The full process flows can be found in Appendix A and Appendix B.

*Table 6-2. Summary of photodetector wafer process variations. For full process flows refer to Appendix A and Appendix B. Wafer 2 does not have the process variations listed due to Ge growth failure.*

| Wafer number | Wafer designation | Backside $Si_3N_4$ deposition | N++ implant dose ($P/cm^2$) | Ge thermal oxidation | Implant activation anneal time (s) | Cell isolation etching |
|---|---|---|---|---|---|---|
| 1 | RMG 1 | Yes | $5x10^{14}$ | No | 15 | No |
| 2 | RMG 2 | / | / | / | / | / |
| 3 | RMG 3 | No | $5x10^{14}$ | No | 15 | No |
| 4 | RMG 4 | Yes | $7x10^{14}$ | Yes | 15 | Yes |
| 5 | RMG 5 | Yes | $7x10^{14}$ | Yes | 15 | Yes |
| 6 | PECVD 1 | No | $5x10^{14}$ | No | 15 | No |
| 7 | PECVD 2 | No | $5x10^{14}$ | No | 39 | No |
| 8 | PECVD 3 | No | $7x10^{14}$ | Yes | 15 | No |

As described earlier, as a result of the limited timescale of this project, the photodetector fabrication was carried out simultaneously with the process development. In other words, the process development was always a few steps ahead of the photodetector wafers in the process flow (see Appendix A and Appendix B). The one major exception to this was the ion implantation step, for which the TLM wafers and the photodetector wafers were processed in one batch to keep the costs down.

### 6.4.1 Wafer bowing

A major problem that was discovered as fabrication was carried out, was the wafer bowing induced by the stress in the various deposited layers. Table 6-3 summarises the wafer bowing measurements carried out at various points in the process flow.

All bowing measurements in Table 6-3 are a result of compressive strain i.e. convex wafer. For the step numbers and full process flows, refer to Appendix A and Appendix B.

*Table 6-3. Wafer bowing measurements throughout photodetector fabrication process.*
*These measurements were only carried out on certain wafers.*

| Step number (RMG photodetectors) | Step number (PECVD photodetectors) | Step description | Wafer bow (μm) | | |
|---|---|---|---|---|---|
| | | | RMG wafer 4 | RMG wafer 5 | PECVD wafer 3 |
| 9 | 7 | Before Ge growth | / | 45 | 38 |
| 11 | 8 | After Ge growth | 58 | 63 | 60 |
| 13 | 10 | After Ge etch | / | / | 31 |
| 15 | / | After $SiO_2$ deposition (RMG capping layer) | 58 | 61 | / |
| 16 | / | After RMG anneal | / | 72 | / |
| 17 | / | After HF etch ($SiO_2$ cap removal) | 82 | 82 | / |
| 18 | / | After backside $Si_3N_4$ deposition | 43 | 48 | / |
| 33 | 30 | After $SiO_2$ deposition (passivation layer) | 96 | 91 | 57 |
| 41 | / | After cell isolation etching | 90 | 100 | / |

The major problem caused by the wafer bowing was that the e-beam lithography tool was unable to focus the electron beam to write the patterns in the resist, if the wafer was bowed by more than 60 μm. This enforced various attempts at reducing the bowing of the wafers, as described below.

#### 6.4.1.1 Backside $Si_3N_4$ deposition

In order to reduce the bowing of the wafers caused by compressive strain in the various deposited layers, a compressively strained $Si_3N_4$ layer was deposited on the backside of some of the process wafers (see Table 6-2) by PECVD.

In a $Si_3N_4$ stress study conducted by Dr Owain Clarke, using a low frequency (<1 MHz)/RF frequency (13.56 MHz) plasma cycling deposition technique, the stress in the $Si_3N_4$ layer was characterised as a function of the percentage of low frequency plasma to RF frequency plasma. It was found that increasing the percentage of low frequency, during 20s cycles, increased the compressive stress in the $Si_3N_4$ layer, similar to that observed by other groups [13]. The results are shown in Fig. 6-18.

As a result of this study a 100% low frequency $Si_3N_4$ PECVD deposition was performed on the backside of some of the wafers. This was carried out in an attempt to reduce the bowing by applying an opposing force to the compressive stress on the topside of the wafer. The backside $Si_3N_4$ deposition performed after the RMG step successfully flattened the wafer, as shown by the bowing measurements in Table 6-3. However, upon addition of the $SiO_2$ layer for passivation and vias, the stress once again induced a wafer bow that was incompatible with the e-beam lithography tool. Backside $Si_3N_4$ deposition was again performed in an attempt to reduce the bowing of the wafer. However, in this case, the stress induced catastrophic wafer twisting, probably due to the non-uniform stress on the topside of the wafer, as a result of the patterned layers. Therefore this wafer had to be scrapped, and another method of stress reduction was sought.

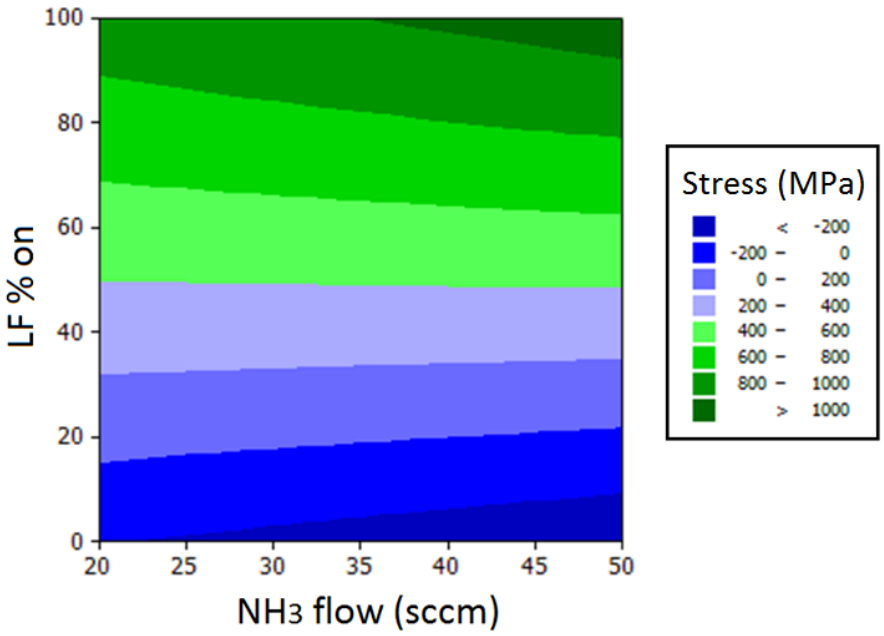


*Fig. 6-18. Contour plot of $Si_3N_4$ stress as a function of low frequency plasma percentage and $NH_3$ flow.*
*By convention, a negative stress value corresponds to tensile stress, and conversely, a positive stress value corresponds to compressive stress.*

### 6.4.1.2 Deep etch for cell isolation

It was hypothesised that by performing an etch through each of the stress inducing layers deposited on the SOI wafer, and therefore isolating each of the individual e-beam cells on the wafer (see Fig. 6-2), the stress in the wafer would be reduced so that the wafers were once again compatible with the e-beam lithography tool. To test this, a mask was designed to etch around the perimeter of each e-beam cell, as shown in Fig. 6-19a. This was performed, using S1813 photoresist, after the passivating $SiO_2$ layer was deposited, as this layer bowed the wafers beyond the specification of the e-beam lithography tool. Firstly, the top $SiO_2$ passivation layer was removed by 20:1 HF etching. Secondly, the SOI Si overlayer was removed by ICP etching. At this stage there was found to be no reduction in wafer bowing, so the BOX layer was etched using 20:1 HF.

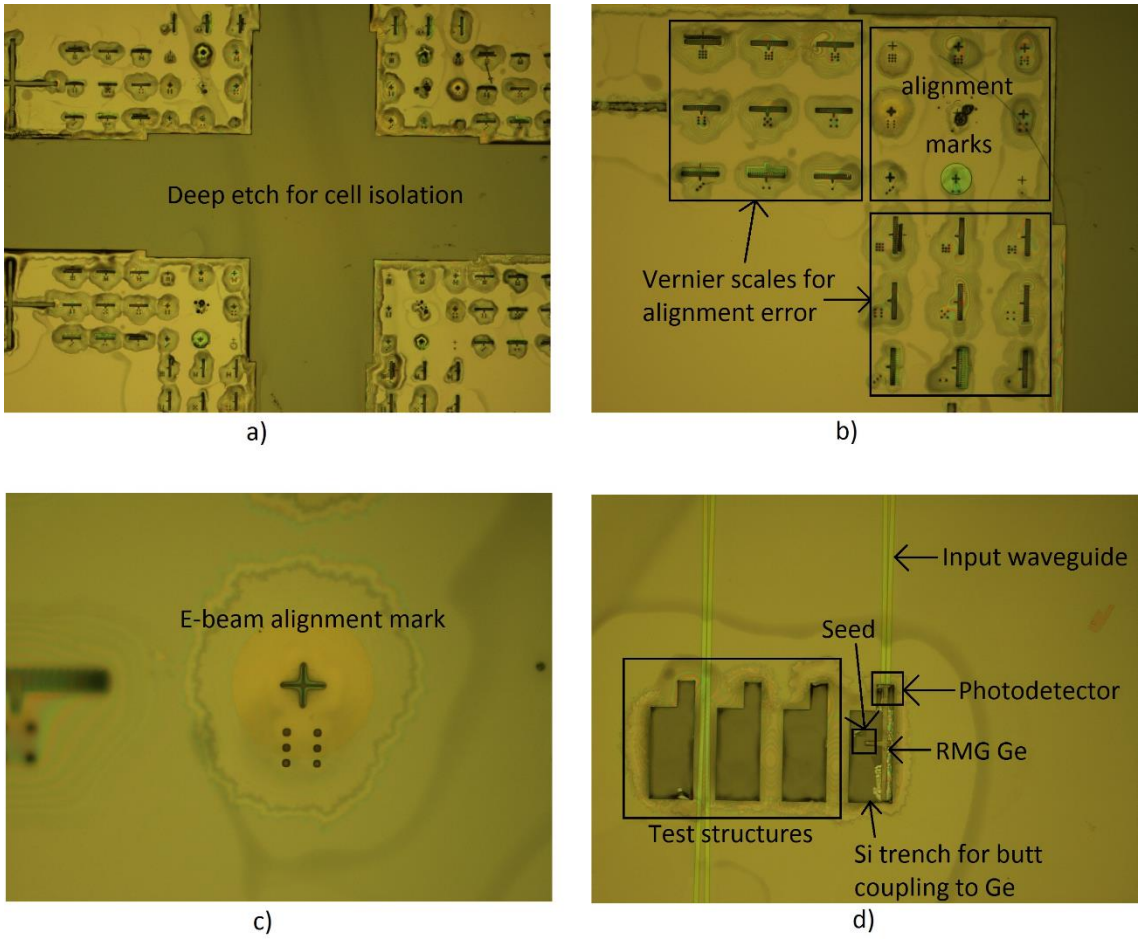


*Fig. 6-19. Microscope images of alignment mark damage after performing a deep etch to isolate each of the e-beam cells. a) Deep etch around the perimeter of each e-beam cell, b) e-beam alignment marks and Vernier scales for x and y alignment error measurements, c) single e-beam alignment mark, d) RMG photodetector. All images show HF under-etching.*

However, as the 2 µm BOX layer required 1 hour in 20:1 HF to be totally etched, it was found that the S1813 photoresist was not sufficient to mask the rest of the wafer. As a result of this, the HF penetrated into the features, possibly due to a thinner resist on the sidewalls of etched features. This damaged the alignment marks so that they were no longer detected by the e-beam lithography tool, and therefore the vias could not be written (see Fig. 6-19b and Fig. 6-19c). The HF had also penetrated into the Si trenches containing the RMG photodetectors, and consequently etched the $SiO_2$ underneath the Ge. This caused most of the RMG structures to delaminate. Unfortunately, as a result of this damage, no RMG photodetectors were fabricated.

Nevertheless, the wafer bowing was measured after etching through all of the layers, including the BOX, down to the bulk Si wafer. It was discovered that the bowing had not been reduced by any significant amount.

### 6.4.2 Summary of photodetector fabrication process

Table 6-4 summarises the photodetector fabrication results. In total, 3 PECVD photodetector wafers were successfully completed. All 5 RMG wafers were unsuccessful, as a result of wafer bowing.

*Table 6-4. Summary of photodetector fabrication results.*

| Wafer number | Wafer designation | Fabrication result |
|---|---|---|
| 1 | RMG 1 | Wafer bowing after $SiO_2$ passivation layer deposition incompatible with e-beam. Backside $Si_3N_4$ deposition twisted the wafer, which enforced e-beam manual alignment of vias mask. Alignment was out of tolerance. Wafer scrapped. |
| 2 | RMG 2 | Error during Ge growth caused by a problem with the $GeH_4$ gas mass flow controller. Wafer scrapped. |
| 3 | RMG 3 | Wafer bowing after $SiO_2$ passivation layer deposition enforced e-beam manual alignment of vias. Alignment was out of tolerance, but nevertheless the wafer was diced in order to inspect the $SiO_2$ etch rate in small vias by cross-section SEM. Wafer subsequently scrapped. |
| 4 | RMG 4 | Wafer bowing after $SiO_2$ passivation layer deposition incompatible with e-beam. E-beam cell isolation by deep etching through stress layers caused Ge delamination as a result of insufficient masking during HF etching. Wafer scrapped. |
| 5 | RMG 5 | Wafer bowing after $SiO_2$ passivation layer deposition incompatible with e-beam. E-beam cell isolation by deep etching through stress layers caused Ge delamination as a result of insufficient masking during HF etching. Wafer scrapped. |
| 6 | PECVD 1 | Fabrication successfully completed. |
| 7 | PECVD 2 | Fabrication successfully completed. |
| 8 | PECVD 3 | Fabrication successfully completed. |

Fig. 6-20 shows a few microscope images of the PECVD photodetectors after fabrication was completed.

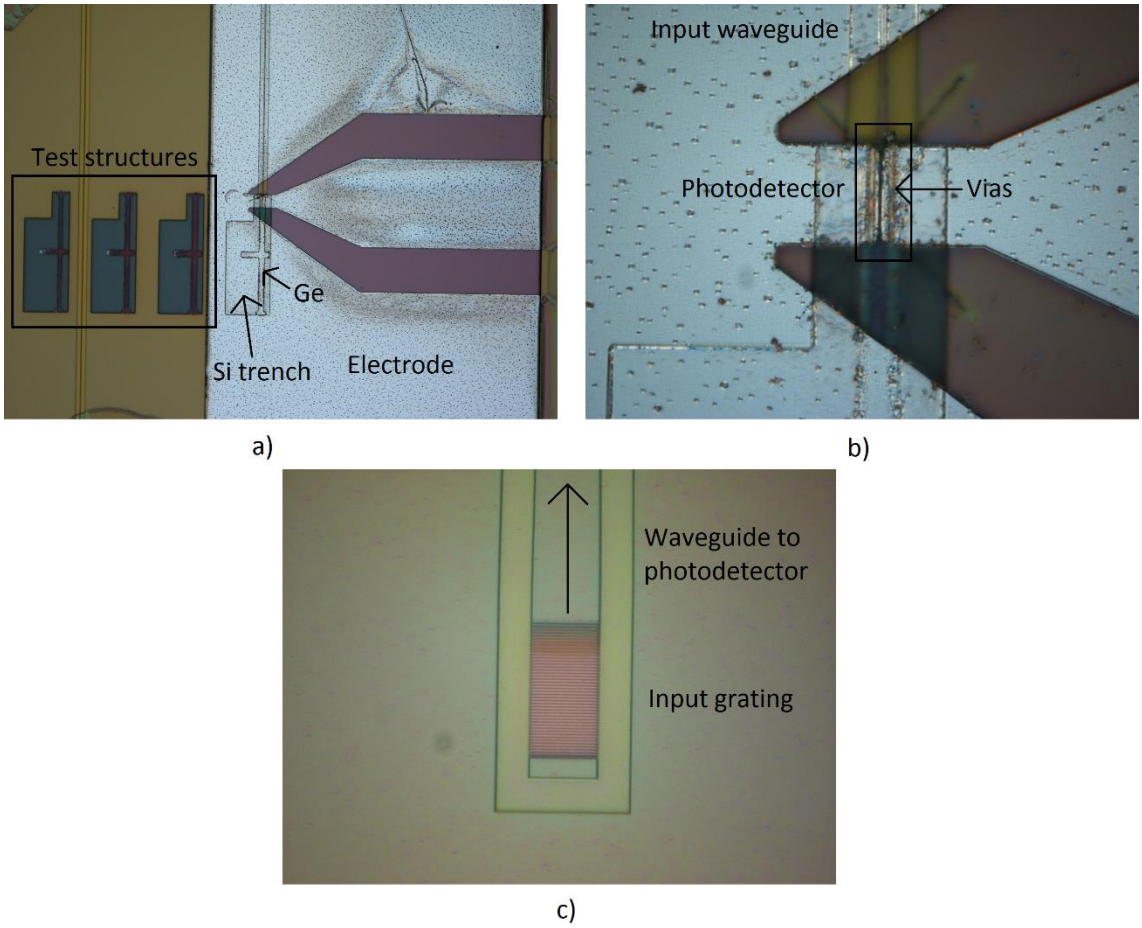


*Fig. 6-20. Microscope images of PECVD photodetectors. a) x20 image showing the entire device, b) x100 image showing the active region, c) x150 image showing the input grating coupler.*

In addition, cross-section images of the device were gathered by cross-sectional SEM, after focused ion beam (FIB) milling of the device through the active region. Fig. 6-21 shows a labelled cross-section of the completed device, and Fig. 6-22 shows the measured dimensions.

It can be seen that this device was successfully fabricated within the planned dimensional specification.

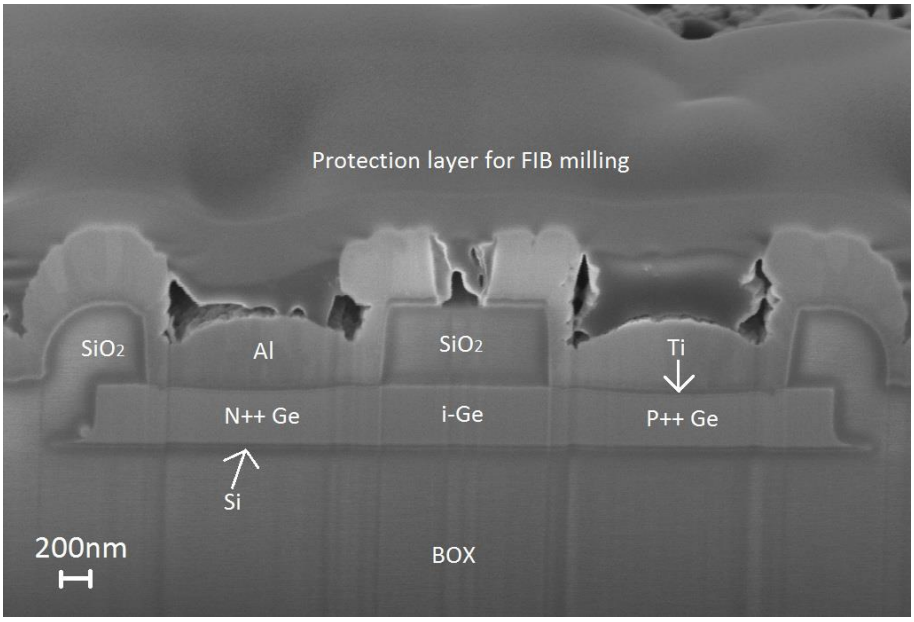


*Fig. 6-21. Cross-section SEM of a completed PECVD photodetector.*

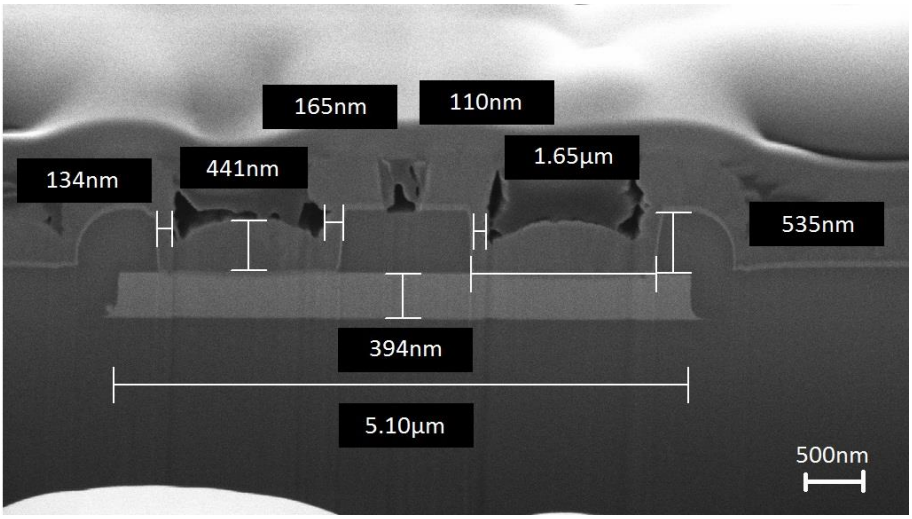


*Fig. 6-22. Cross-section SEM of a completed PECVD photodetector, showing device dimensions.*

## 6.5 Photodetector characterisation

The DC and AC performance of the PECVD photodetectors has been characterised in this section.

### 6.5.1 Measurement setup

The measurement setup for both DC and AC characterisation is shown schematically in Fig. 6-23.

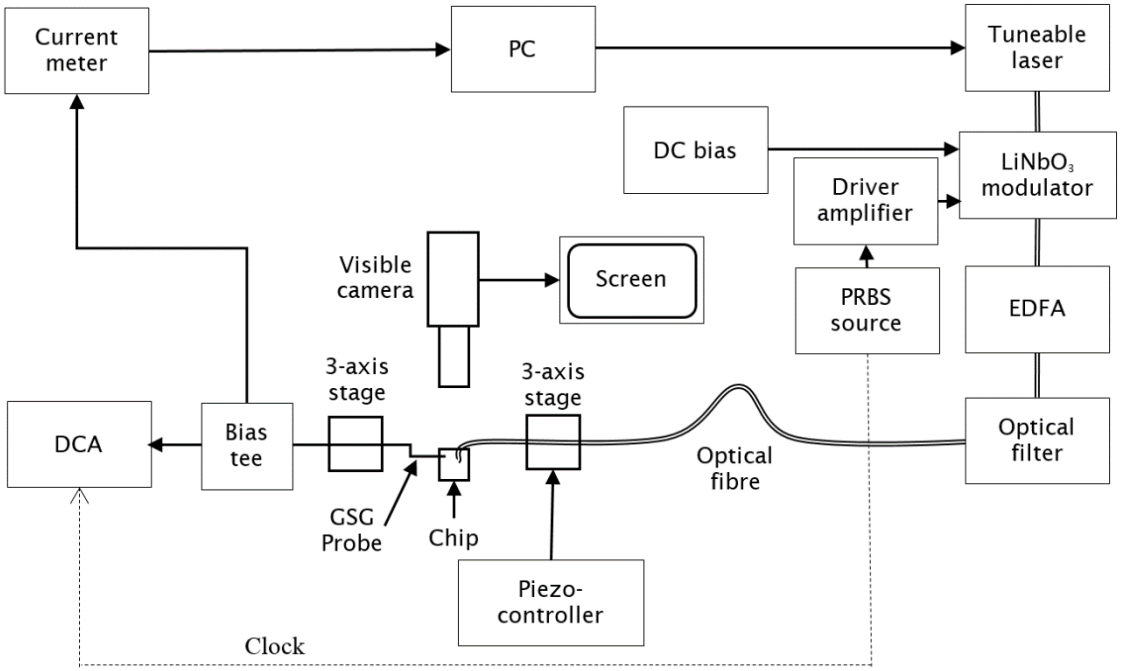


*Fig. 6-23. 1.55 μm photodetector device measurement setup.*

The chip under measurement is placed on a stage, with a visible camera mounted above it so that it can be viewed on a screen. The optical signal is coupled into, and out of, the chip using optical fibres mounted on 3-axis stages (the optical output arrangement is not shown in Fig. 6-23 since it is only required for normalisation purposes). The position of the optical fibres can be adjusted by eye, using micrometers, and then finely adjusted using piezo-controllers. A ground-signal-ground (GSG) probe is used to provide an electrical contact to the photodetectors. This is connected to a current meter for DC measurements, and a digital communications analyser (DCA) for AC measurements. A bias tee separates the DC and AC components to avoid equipment damage.

In order to measure the DC characteristics, light from a tuneable wavelength laser is coupled directly into the photodetectors via an optical fibre and grating coupler.

In order to measure the high-speed performance of the PECVD photodetectors, a modulated optical signal is generated using an electrical pseudo-random binary sequence (PRBS) source, driver amplifier and commercial $LiNbO_3$ modulator (in the range of 1 Gbit/s to 12.5 Gb/s). This signal is amplified using an erbium doped fibre amplifier (EDFA), and subsequently coupled to the device using an optical fibre and a grating coupler.

### 6.5.2 DC performance

In order to calculate the responsivity of the photodetectors, it is necessary to know the optical power reaching the photodetector. In order to evaluate this, the input circuit loss is firstly calculated by measuring the power exiting the input optical fibre using a free-space detector (not shown in Fig. 6-23). This is repeated for the output circuit loss by connecting the output fibre to the laser. Finally, the total optical loss through a simple tapered straight normalisation waveguide, with a grating coupler on both the input and output, is measured. The coupling (grating) loss plus the waveguide loss is then calculated by subtracting the input circuit loss and output circuit loss from the total loss. The power entering the photodetector can then be calculated using the input circuit loss, and half of the coupling loss plus waveguide loss. This is because there is only a single grating loss to be considered, and half the waveguide length, when compared with the normalisation structure, when coupling the light into a photodetector.

Using the technique described above, the responsivity of a device with an intrinsic region with dimensions of 1.5 μm width and 5 μm length was measured to be 0.1 A/W, with no applied bias. There are a number of potential reasons why the responsivity is fairly low. Firstly, it was observed during fabrication that there was a slight misalignment between the input waveguide and the central, intrinsic section of the photodetector. Therefore, some of the optical signal may be leaking into the doped regions, where any photogenerated carriers are likely to recombine before they are swept out of the device. This is because they are generated outside of the high electric field region (i.e. the intrinsic region). Secondly, the high defect density of the PECVD Ge material (see Chapter 4) could lead to a small recombination time, even in the high electric field, intrinsic region. As a result, it is possible that not all of the photogenerated carriers are swept out of the device before they recombine, and therefore they do not contribute to the measured current.

The measured dark current of the same device at 0 V was 2.21 μA, from which the dark current density can be calculated to be $2.9 \times 10^4$ mA/cm$^2$. As described above for the TLM measurements, the suspected cause of this high dark current is high surface leakage current, possibly in the form of trap assisted tunnelling current caused by the unterminated dangling bonds at the Ge-$SiO_2$ interface [8]. There was no significant difference in dark current between equivalent devices

on wafer 6 (no Ge thermal oxidation) and wafer 8 (Ge thermal oxidation). This suggests that the thin $GeO_2$ layer did not lead to successful surface passivation. The difficulty encountered here was that the surface leakage issues were not discovered until after ion implantation had been performed on all wafers. Therefore, in order to grow a thermal $GeO_2$ layer, a low temperature (500 °C) was used to limit the dopant diffusion prior to dopant activation. This temperature was assumed to grow only a few nanometres of $GeO_2$ [9]. The actual thickness was not measured due to the complexity of the ellipsometer model and the small layer thickness.

Unfortunately, due to the high dark current discussed above, the majority of the fabricated devices were not performing as predicted. Therefore, a comparison of the different device dimensions was not possible.

### 6.5.3 AC performance

A convenient way of analysing the high speed performance of photodetectors is with the use of eye-diagrams. These diagrams show the transitions from '1' to '0' and vice versa on a voltage (y-axis) against time (x-axis) plot. The more open the eye at any given bit rate, the faster the device since this shows a faster transition between states.

The PECVD photodetector open eye-diagrams for data rates in the range 1 Gbit/s to 12.5 Gbit/s at 0 V are shown in Fig. 6-24.

These diagrams show that the device is capable of working up to 12.5 Gbit/s, with no applied bias. This demonstrates the strong built-in electric field is sufficient to collect the generated carriers. If a reverse bias is applied, the speed is typically improved [14] due to the increased electric field, which enhances the carrier drift velocity. However, due to the high surface leakage current of the PECVD photodetectors, if a reverse bias is applied the leakage current becomes too large for the photocurrent to be measured.

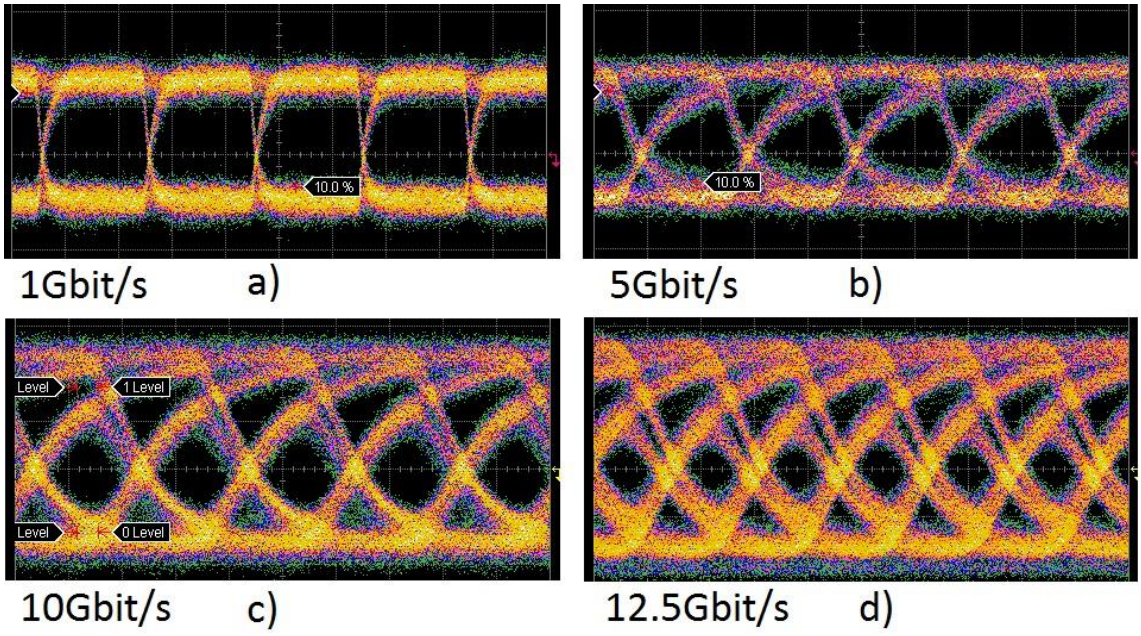


*Fig. 6-24. PECVD photodetector eye diagrams.*
*a) 1 Gbit/s, b) 5 Gbit/s, c) 10 Gbit/s, 12.5 Gbit/s. All eye diagrams are measured at 0 V. Device intrinsic dimensions W = 1.5 μm, L = 5 μm.*
*λ = 1550 nm.*

## 6.6 4-channel photodetectors

In addition to the PECVD photodetectors described above, 4-channel Ge photodetectors fabricated using the ePIXfab service [3] were characterised [15]. The multi-channel devices were based on angled multimode interferometers (AMMI) designed by Dr Youfang Hu [16, 17], and Ge photodetectors designed by Dr Frederic Gardes. The Ge photodetectors, grown by reduced pressure chemical vapour deposition (RPCVD), have a very similar design to the PECVD photodetectors described above. The intrinsic absorbing region has dimensions of 1.4x14 μm. The 4-channel receivers were fabricated on 220 nm Si overlayer, 2 μm BOX SOI wafers.

The AMMI based design offers a convenient way to build a silicon wavelength division multiplexing (WDM) optical transceiver. They could have the distinct advantages of both low insertion loss (hence, low input power for transmitter, and high responsivity for receiver), and ease of fabrication (single etch step on the WDM part) at the same time. A schematic drawing of the device is shown in Fig. 6-25.

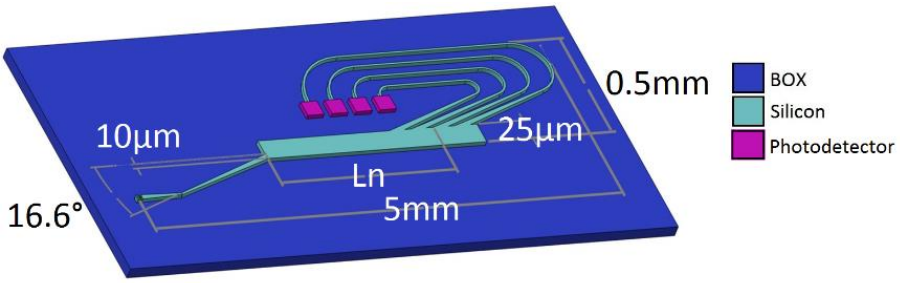


*Fig. 6-25. Schematic of the AMMI receiver, reproduced from [15].*

The AMMI has a channel spacing of 10 nm, centred at 1560 nm. Simulation shows this structure has an insertion loss of -0.3 dB, and a cross talk of -25 dB [15].

Light from a tuneable wavelength laser was coupled into the receiver device via an optical fibre and grating coupler, using the setup shown in Fig. 6-23. The resulting current from each of the 4 channels, with no applied bias, was measured and plotted in Fig. 6-26. After removing the external losses such as coupling loss and waveguide loss by measuring the transmission through a straight normalisation waveguide, the responsivity of the photodetectors at 1550 nm, with no applied bias, is calculated to be approximately 0.5 A/W. It was found that the current had no dependence on the applied bias, which implies that all of the photogenerated carriers are collected by the strong built-in electric field.

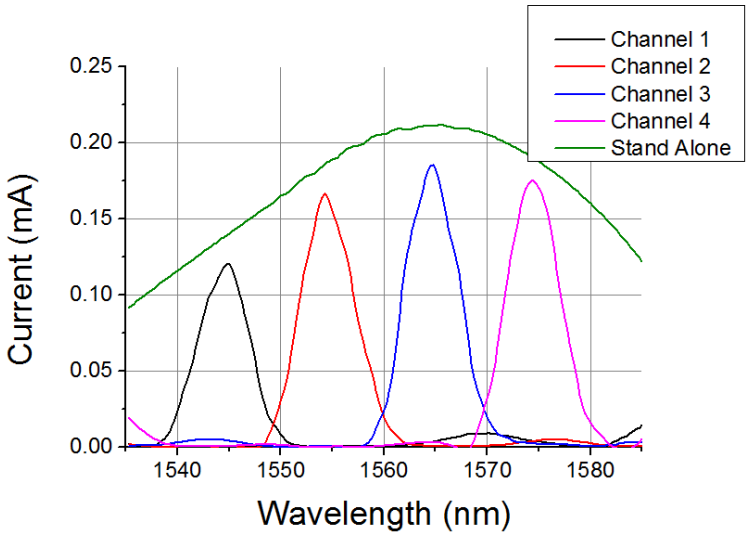


*Fig. 6-26. Measured current from the 4 photodetector channels and a standalone photodetector with the same configuration, reproduced from [3].*

By comparing the current from a standalone photodetector with the same configuration with the current from each channel of the AMMI receiver device, the transmission through the AMMI can be calculated and plotted, as shown in Fig. 6-27.

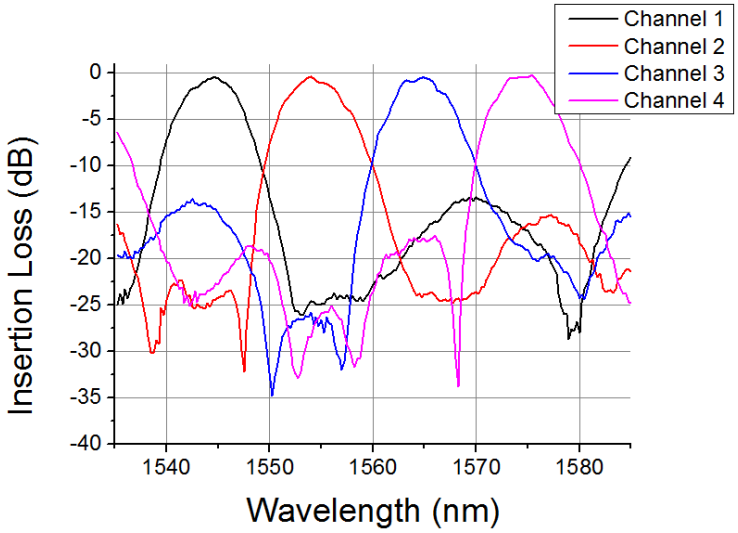


*Fig. 6-27. Measured insertion loss of the 4-channel WDM device, reproduced from [3].*

From this plot, it can be seen that a single AMMI has an insertion loss of < -0.5 dB and a cross-talk of approximately < -15 dB across the 4 channels. The channel spacing is 10 nm. The experimental results match reasonably well with the simulation data, except that the cross talk at channels 1, 3 and 4 is higher. It is shown that the main peaks of these channels coincide with the side peaks of the non-neighbouring channels, which is not seen in the simulation [15].

The dark current of the photodetectors is measured to be 60 pA, with no applied bias, and 10-20 nA at -1 V. IV curves for a 4 channel receiver and stand-alone photodetector are shown in Fig. 6-28, where a current limit of 250 μA has been set in order to prevent damage to the devices.

The reason for the lack of significant surface leakage current with these devices is unknown because the complete fabrication process is confidential. Based on the summary of the fabrication process given on the ePIXfab website [3], it can be speculated that the chemical mechanical polishing (CMP) step after Ge growth leads to a better quality interface between the Ge and $SiO_2$ that results in successful surface passivation.

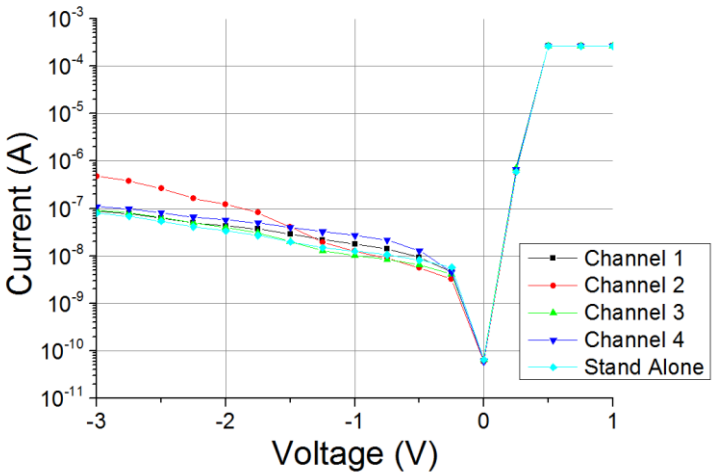


*Fig. 6-28. IV curves for the 4-channel photodetectors and standalone photodetector, showing a dark current of 60 pA at 0 V, and 10-20 nA at -1 V, reproduced from [3].*

The high-speed performance was also characterised using the setup described in Fig. 6-23. The resulting open eye-diagrams for each channel at its peak wavelength are shown in Fig. 6-29, giving an aggregate data rate of 50 Gbit/s.

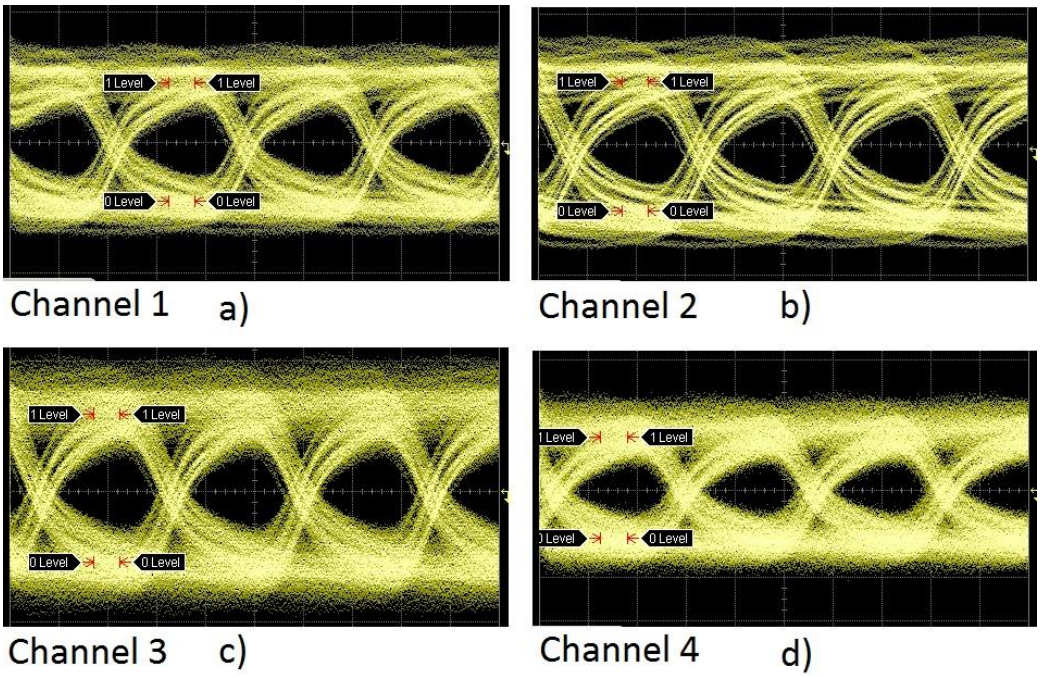


*Fig. 6-29. 12.5 Gb/s eye diagrams of 4-channel photodetectors operating at -1 V, reproduced from [3].*
*a) Channel 1 at 1545 nm, b) channel 2 at 1555 nm, c) channel 3 at 1565 nm, d) channel 4 at 1575 nm.*

## 6.7 Ge photodetectors conclusions

In order to successfully fabricate photodetectors, a multitude of process development was required. Two major problems were encountered during fabrication: wafer bowing and high surface leakage current. Unfortunately, the wafer bowing problems with the RMG photodetectors could not be resolved within the timeframe of this project, and therefore no devices were measured. However, even with the high surface leakage current associated with dangling bonds at the Ge-$SiO_2$ interface, the PECVD photodetectors were able to operate at a speed of 12.5 Gbit/s, with no applied bias. The PECVD photodetectors fabricated in this project were comparable in speed with the RPCVD photodetectors fabricated as part of the ePIXfab service. The responsivity of the PECVD photodetectors was lower than the RPCVD photodetectors. This may be due to the lower material quality of the PECVD photodetectors, the misaligned input waveguides for the PECVD photodetectors, the shorter length of the PECVD photodetectors, or a combination of the above. The major advantages of the PECVD photodetectors over the RPCVD photodetectors, are the low cost Ge growth method, and also the low temperature required for Ge growth.

Table 6-5, repeated from chapter 3, compares the photodetectors detailed in this project with those in the literature.

*Table 6-5. Photodetectors performance comparison with published data.*
*All data is for 1 V reverse bias unless otherwise stated. All acronyms are defined in Chapter 3. Underlined data indicates this work.*

| Responsivity (A/W) at 1.55 μm | 3 dB bandwidth (GHz) | Dark current density (mA/cm$^2$) | Dark current (nA) at 20 °C | Ge growth technique | Year | Ref. |
|---|---|---|---|---|---|---|
| **Waveguide coupled vertical device Ge photodetectors** | | | | | | |
| 1 (1.52 μm) | 4.5 | No info. | No info. | No info. | 2006 | [18] |
| 1.08 | 7.2 | 410 (-0.5 V) | 60 | LT/HT UHVCVD with annealing | 2007 | [19] |
| 0.89 (-2 V) | 31.3 (-2 V) | 51 (-2 V) | 169 (-2 V) | LT/HT growth with annealing | 2007 | [20] |
| 1 | 8.5 | No info. | 0.2 | UHVCVD with graded SiGe buffer | 2008 | [21] |
| 0.9 | 28 (-2 V) | 60 | 18 | LT/HT RPCVD with annealing | 2009 | [22] |
| 0.05 (-2 V) | 49 (-2 V) | 130 | No info. | MBE | 2009 | [23] |
| 0.56 | 24 | 625 | 120 | LT/HT UHVCVD with annealing | 2010 | [24] |
| 0.7 | 12 | 28 | 600 | LT/HT UHVCVD with annealing | 2010 | [25] |
| 0.95 | 36 | 11 | 11 | LT/HT growth with annealing | 2011 | [26] |
| 0.8 | 45 | 40 | 3 | LT/HT growth | 2011 | [27] |
| 1 (-2 V) | 20 (-2 V) | 49 | 245 | No info. | 2013 | [28] |
| 0.75 | 30 | No info. | 3000 | No info. | 2013 | [29] |
| 0.65 | 15 | 340 | 170 | LT/HT UHVCVD with SiGe buffer | 2013 | [30] |
| 0.45 | 50 | 100 | 11 | No info. | 2014 | [31] |
| 0.4 (1.3 μm) | 15 | 250 | 100 | RMG | 2014 | [32] |
| 1 | 33 | 40 | No info. | RPCVD | 2014 | [33] |
| **Waveguide coupled lateral device Ge photodetectors** | | | | | | |
| 0.1 (0 V) | 12.5 (0 V) | $2.9\times10^4$ (0 V) | $2.1\times10^3$ ( 0 V) | LT PECVD (this work) | 2015 | / |
| 0.5 | 12.5 | 51 | 10 | RPCVD (this work) | 2014 | / |
| 1.1 | 33 | $16\times10^3$ | $1.3\times10^3$ | LT/HT growth with annealing | 2009 | [34] |
| 0.8 | 120 | $80\times10^3$ | $4\times10^3$ | LT/HT RPCVD with annealing | 2012 | [14] |
| 0.9 (1.5 μm) | 10 | $10\times10^3$ | $2\times10^3$ | RPCVD with annealing | 2012 | [35] |
| 0.4 | 50 | 714 | 25 | LT/HT RPCVD with annealing | 2013 | [36] |
| 1 | 20 | 43 | 3 | No info. | 2014 | [31] |
| 1.07 | 30 | No info. | 4000 | No info. | 2014 | [37] |

# Chapter 7: Conclusions and future work

## 7.1 Conclusions

Ge and SiGe will play a key role in the future of silicon photonics, at both near-infrared and mid-infrared wavelengths. Applications include high speed electro-absorption modulators, high speed photodetectors, and mid-infrared waveguides. In the literature review, a number of epitaxial Ge/SiGe-on-Si growth techniques are discussed. It was concluded that there was a need for a growth technique that could simultaneously attain a range of SiGe compositions, in a single growth step. Such a growth technique would enable fabrication of multiple SiGe compositions, to suit the design requirements for applications such as wavelength division multiplexing (WDM) systems. None of the growth techniques identified in the literature review were able to achieve this, on the same wafer.

In this project, a rapid melt growth (RMG) technique has been used to grow high quality, device grade, single crystal localised SiGe-on-insulator (SGOI) structures. RMG is a technique that realises lateral overgrowth of SiGe, onto an insulating layer, from a Si seed. In order to perform RMG, a blanket layer of Ge is grown on a patterned $SiO_2$ layer, on a Si substrate. The Ge is then etched into structures, encapsulated with an additional $SiO_2$ layer, and subsequently melted by rapid thermal annealing (RTA). Whilst the Ge is in the liquid phase, diffusion from the Si seed is apparent, forming a SiGe melt. Upon cooling, the Si seed acts as a crystal template from which the SiGe regrowth commences, and subsequently, the epitaxial growth front propagates laterally along the SiGe structure. This facilitates a range of SiGe compositions within a single growth step as desired, and therefore opens up a host of low cost applications.

One of the major advantages of RMG is that the defects, caused by the lattice mismatch between Si and Ge, are confined to the seed area by a defect necking mechanism. All dislocations are terminated at the top Ge-$SiO_2$ interface, and do not propagate laterally along the SiGe structures. Additionally, since the Ge will be subsequently melted, the initial Ge growth is non-critical. Therefore, any non-selective deposition method can be used, e.g. e-beam evaporation or plasma

enhanced chemical vapour deposition (PECVD). However, a potential drawback is that a high temperature anneal (> 938 °C) is required to melt the Ge, albeit for a very short length of time (approximately 1 second). This enables low cost Ge growth methods to be used, with a very low thermal budget, without compromising the final material quality.

After RMG was performed, the SiGe composition profiles were characterised using Raman spectroscopy. This is a non-destructive technique, which enables the SiGe composition to be calculated from the ratio of the Ge-Ge and Si-Ge peak intensities. This facilitates post-growth characterisation without damage to the sample, meaning that it could be used in a commercial environment for error testing and quality control.

In this project, straight strips of up to 100 μm in length and 5 μm in width were shown to have graded composition profiles, with the lowest Ge concentration near the seed, and pure Ge at the distal end of the strips. This has also been shown in the literature. A maximum width of 5 μm was identified, beyond which SiGe agglomeration occurred, possibly due to the high interface energy between SiGe and $SiO_2$. The graded composition profiles can be attributed to the separation between the solidus and liquidus curves on the SiGe phase diagram. This means that at any given temperature, the composition of the solid and the liquid are different. As a result, a Si rich solid is formed as regrowth commences, with rejection of Ge into the liquid ahead of the regrowth front. Due to minimal diffusion of Si and Ge in the solid phase it is assumed that once solidification commences in the seed area, Si diffusion from the substrate is blocked, and therefore a limited quantity of Si is available in the SiGe melt. Consequently, the available Si is consumed in the solid, within approximately the first 70% of the strip, and pure Ge is realised for approximately the last 30% of the strip. Whilst this is ideal for the formation of high quality pure Ge, the graded composition profile renders fabricating SiGe devices extremely difficult.

This graded composition profile can be modelled using the complete mixing model, which assumes no diffusion in the solid phase, and complete mixing of Si and Ge in the liquid phase. These assumptions can only be met under conditions of slow regrowth, or when the remaining distance left to solidify is small. Since the measured composition profiles of strips up to 100 μm in length approximately match the complete mixing model, it can be concluded that the

regrowth speed is slow enough for complete mixing to occur in the liquid. This enables the composition profiles of such structures to be predicted. Therefore, this offers a graded composition profile, if required for novel designs.

However, in order for this SGOI material to be suitable for device fabrication, it is necessary to develop a method of achieving a uniform SiGe composition. In order to achieve this, it was identified that steady-state solidification was required. In this model, uniform composition profiles are achieved when the regrowth front propagation speed is high enough so that the diffusion of rejected Ge at the regrowth front is balanced by the propagation of the regrowth front itself, in the same direction. It follows that in order to maximise the regrowth front propagation speed, the cooling rate needed to be maximised. Therefore, radiating branches were added to the SiGe strips, forming tree-like structures, in order to increase the cooling rate of the main central strip. Consequently, for the first time, we can vary the composition profile of the SiGe simply by changing the physical design of the structure, without the need to modify the fabrication process.

A number of different composition profiles were achieved by varying the structural parameters of the branches. It was concluded that in order to achieve the flattest composition profile (i.e. the fastest cooling rate), long, thin branches were preferable to short, wide branches. This is due to the increased surface area to volume ratio, leading to more efficient cooling, through thermal radiation.

Most importantly, uniform composition profiles were achieved with a central strip width of 3 μm, branch length of 20 μm, and branch width of 5 μm. The composition variation over a 56 μm length was less than 2%, which is within the measurement tolerance. The final 8 μm (after the penultimate set of branches) of the central strip of the tree-like structure were excluded from this measurement. This is because a graded composition profile was demonstrated at the end of the central strip, firstly due to the diminished cooling effects of the branches, and secondly because the remaining distance left to solidify became small enough to realise complete mixing of the SiGe liquid. In practice, the non-uniform composition regions, i.e. the branches and the final 8 μm of the central strip, would be etched away to leave only the uniform composition material for device fabrication. Therefore, for the first time, device grade, uniform

composition SGOI has been demonstrated using an RMG technique. The small variation in measured composition, over a large length, enables many devices to be designed without dimensional restrictions in both length and width.

Composition tuning has also been demonstrated, simply by changing the anneal temperature during the rapid melt growth phase. Higher anneal temperatures lead to increased Si diffusion from the seed, and therefore decrease the Ge concentration of the uniform SiGe strips. The significance of this method of composition tuning is that the initial growth parameters do not need to be finely tuned to achieve the desired composition. Instead, only the anneal temperature needs to be modified, which means that batches of initial Ge growth can be carried out without the need to consider the composition requirements.

The graded composition profile of a straight strip was then combined with the uniform composition profiles of tree-like structures to demonstrate composition tuning by structural design, as opposed to growth conditions. Using this method, uniform compositions (within 1% of the mean) of 81%, 92%, 95%, and 97% are achieved. To the best of the authors knowledge, this is the first time that multiple, uniform SiGe compositions have been grown on a single wafer using only a single growth step. As discussed earlier, this enables a range of SiGe compositions to be realised on a single wafer, with a low thermal budget, and at a low cost. This allows the SiGe composition of each device to be optimised, rather than having to compromise on a fixed SiGe composition across the wafer.

The uniform composition SiGe material grown in this project was demonstrated to be suitable for state-of-the-art device fabrication by electron backscatter diffraction (EBSD) measurements and transmission electron microscope (TEM) imaging. The EBSD measurements showed a single crystal SiGe layer had been fabricated and the TEM imaging demonstrated that all defects were confined to the seed area. This high material quality was realised with a low temperature, low cost, initial Ge growth (250 °C) and a short high temperature anneal (approximately 1000 °C for 1 second). When employing other Ge-on-Si growth techniques, such as molecular beam epitaxy (MBE) and reduced pressure chemical vapour deposition (RPCVD), the initial growth is often followed by cyclic thermal annealing, in order to reduce the defect density of the epitaxial Ge layer. This annealing process is typically carried out for a period of a few hours at

temperatures greater than 700 °C. In this project, using a RMG technique, SiGe layers of comparable or improved quality, when compared to other growth methods, are fabricated with a vastly decreased thermal budget. This confirms that this technique is viable for commercial device fabrication.

In order to realise electronic-photonic monolithic integration, one potential solution is to utilise a bulk Si substrate, with localised buried $SiO_2$ regions for optical confinement for photonic devices. The bulk Si substrate is essential for cooling of electronic devices. The ability to locally tune the SiGe composition to suit the design requirements is a highly desirable capability. Therefore, the RMG technique demonstrated in this project could be of vital importance to the realisation of this long term goal of electronic-photonic monolithic integration. Not only does it enable the fabrication of a plethora of photonic devices, but it is also achieved using low cost methods.

In this project, the initial growth of Ge was carried out by PECVD, because this was identified as a low-cost, low temperature growth technique. Although the initial growth of Ge is non-critical for RMG, a growth study was nevertheless carried out, in order to fabricate a high quality layer for other applications, including mid-infrared waveguides. Additionally, the aim was to directly compare photodetectors fabricated by both PECVD and RMG to gain an insight into the importance of the material quality in device fabrication.

The PECVD study was carried out under constant pressure (500 mT), constant radio frequency (RF) power (20 W) and constant $H_2$ flow (100 sccm) conditions. Only the $GeH_4$ flow and the temperature were modified. It was found that at a low temperature (250 °C), with low $GeH_4$ dilutions (> 10 sccm), voids were present in the Ge layer. In order to remove these voids, the growth rate was decreased by decreasing the $GeH_4$ flow to 2.5 sccm. In an attempt increase the layer quality, the temperature was increased to 400 °C in order to increase the surface adatom mobility. However, it was found that at this temperature a large number of stress relieving hillocks were present on the surface of the epitaxial Ge. This is consistent with this higher temperature favouring Stransky-Krastanov growth, resulting in the initial formation of 3D islands at the Ge-Si interface. Subsequently, with the aim of reducing the number of these stress relieving hillocks, a two-step growth was performed. The first growth step was performed at 250 °C to form a wetting layer approximately 15 nm thick; the second growth

step was performed at 400 °C in order to improve the layer quality. Using this growth technique a layer with an approximate defect density of $2x10^9$ $cm^{-2}$ was realised. However, it was shown that after a 600 °C anneal for 2 minutes in an $N_2$ atmosphere, the defect density was improved by an order of magnitude, to approximately $3.3x10^8$ $cm^{-2}$. Equally, the surface roughness, crystallinity (determined by the sharpness of the Ge (400) x-ray diffraction peak) and defect density of all recipes were improved by this short anneal. The 600 °C anneal was selected because this is the temperature at which the Ge dopant activation was performed for the formation of *p-i-n* junctions for high speed photodetectors. Although the results gathered in this study are not comparable with the state-of-the-art for Ge-on-Si epitaxial growth it should be stressed that the temperatures used were significantly lower than the majority of the growth methods identified in the literature review. Therefore, the PECVD Ge grown in this project is suitable for back-end CMOS integration, where the temperature is limited to 450 °C.

Finally, the fabrication of waveguide integrated Ge photodetectors grown by both RMG and PECVD was performed. The PECVD photodetectors operated at 12.5 Gbit/s with no applied bias, which demonstrates the strong built-in electric field. However, high surface leakage currents meant that the devices could not operate under reverse bias since the leakage current dominated the photocurrent. Nevertheless, the devices exhibited a responsivity of 0.1 A/W at 0 V, and are suitable for low-cost applications where dark current is not an overriding concern. The fabrication of photodetectors by RMG highlighted wafer bowing issues related to the stress in the $SiO_2$ and Ge layers, the result of which was the scrapping of these wafers. However, the fabrication of photodetectors by this technique is seen as a promising concept, due to the high quality of the Ge layer, if the wafer bowing issues can be resolved. Some potential solutions to this problem are discussed in section 7.2, below.

In this thesis, the growth of SiGe by RMG has been advanced by developing a method of achieving device grade material with a tuneable SiGe composition. The composition is tuned by the structural design, and not by the growth recipe, which enables a multitude of compositions to be grown using only a single growth step, and a single anneal step. In addition, a low cost, low temperature epitaxial Ge growth, on Si, using PECVD has been demonstrated. This material

was used to fabricate low-cost, zero bias, 12.5 Gbit/s waveguide integrated photodetectors with a responsivity at 1550 nm of 0.1 A.W.

## 7.2 Future work

The high quality of the SGOI layers grown by rapid melt growth offers plenty of scope for future work. Some potential future research is listed here:

- *Realisation of larger areas of SGOI:* In this project the maximum width of SGOI achieved was 5 μm with the use of a $SiO_2$ underlayer and $SiO_2$ capping layer. An investigation into the insulating material choice may yield wider strips, either due to a reduction in surface interface energy, or by stress engineering the capping layer to prevent SiGe agglomeration at larger widths.
- *Expand the tuneability of the SGOI strips:* The tuneability of the SGOI strips could be expanded to produce a larger variation in SiGe compositions by extending the tailored structure to incorporate a larger number of tree-like structures. Additionally, using a higher temperature anneal (i.e. > 1100 °C) could also broaden the range of compositions achievable.
- *Fabricate SiGe devices e.g. electro-absorption modulators:* This project has demonstrated the ability to grow high quality material that is suitable for the fabrication of state-of-the-art SiGe devices. The extremely low levels of defects (none observed on TEM images) suggest that devices will not be limited by material quality.
- *Fabricate a wavelength division multiplexed (WDM) optical link:* The ability to achieve a range of SiGe compositions, from the same single growth step, could enable the fabrication of a multitude of electro-absorption modulators to be fabricated, each with a slightly different SiGe composition, for WDM applications. Simultaneous fabrication of pure Ge photodetectors can be achieved, with the same growth method, enabling a full link to be realised, with the use of dielectric waveguides deposited on top of the active devices [1] for optical coupling.
- *Fabricate multilayer devices using poly-Si seeds:* The ability to use a poly-Si seed to realise RMG has been demonstrated in this project. This could enable the fabrication of multilayer devices and systems, which means

that the space on the substrate can be maximised for the electronic components, with photonic components on additional layers.

Additionally the low-cost photodetectors developed in Chapter 6 show a lot of promise, but require additional work to optimise the devices. Some potential areas of future research are listed below:

- *Develop low stress $SiO_2$ layers:* The need for low stress layers in order to reduce the wafer bowing is clear. This is not only required for e-beam lithography, but also for compatibility with planar CMOS applications.
- *Develop photodetectors on a bulk Si platform:* The wafer bowing issues encountered with the RMG photodetectors on SOI wafers could also be alleviated with the use of a bulk Si substrate. It was found that the SOI wafers were typically bowed by up to 40 μm prior to any processing. On a bulk Si platform the photodetectors can be developed as normal incidence devices, or dielectric waveguide coupled devices. This would enable a direct comparison between the RMG and PECVD photodetector devices to be made in order to assess the importance of the material quality to the efficiency of the device.
- *Reduce surface leakage current:* This project highlighted surface leakage current issues related to improper passivation of the Ge layer. Research into improved surface passivation is therefore required. This could potentially be realised by the deposition of a thin amorphous Si layer, on the Ge surface, after growth [2].
- *Investigate gas phase doping:* Gas phase doping has been shown to reduce the dark current density of photodetectors by up to two orders of magnitude [3]. This is due to the reduction in lattice damage when compared with the more conventional ion implantation technique. Therefore the feasibility of implementing gas phase doping instead of ion implantation would be an interesting study.

# Appendix A: PECVD photodetector process flow

Table A-1. PECVD photodetector process flow.

| Step Number | Process Name | Process Description | Comments |
|---|---|---|---|
| 1 | $SiO_2$ Deposition #1 | PECVD 40 nm | |
| 2 | Anneal #1 | RTA 600 °C $SiO_2$ Densification | |
| 3 | Photolithography #1 | Alignment Marks & Ge Growth Windows Masks | S1813 (1.3 μm) Resist |
| 4 | $SiO_2$ Etch #1 | HF Etch 40 nm | |
| 5 | Si Etch #1 | ICP 350 nm Etch | |
| 6 | Plasma Clean #1 | $O_2$ Plasma Clean | |
| 7 | HF Dip #1 | HF Dip 5 seconds | |
| 8 | Ge Growth #1 | PECVD 400 nm Ge | Growth Recipe C |
| 9 | E-Beam Lithography #1 | Ge Etch Mask | AZ2070 (4 μm) Resist |
| 10 | Ge Etch #1 | ICP Etch 400 nm | |
| 11 | Plasma Clean #2 | $O_2$ Plasma Clean | |
| 12 | $SiO_2$ Etch #2 | HF Etch 40 nm | |
| 13 | E-Beam Lithography #2 | Waveguide & Gratings Masks | ZEP (250 nm) Resist |
| 14 | Si Etch #2 | ICP 220 nm Etch | |
| 15 | Plasma Clean #3 | $O_2$ Plasma Clean | |
| 16 | $SiO_2$ Deposition #2 | PECVD 20 nm | |
| 17 | E-Beam Lithography #3 | P++ Mask | ZEP (450 nm) Resist |
| 18 | Boron Implantation #1 | B ($BF_3$), 20 keV, $1x10^{15}$ B/cm$^2$ | |
| 19 | Plasma Clean #4 | $O_2$ Plasma Clean | |
| 20 | E-Beam Lithography #4 | N++ Mask | ZEP (450 nm) Resist |
| 21 | Phosphorous Implantation #1 | P (Ar+P), 30 keV, $5x10^{14}$ P/cm$^2$ or $7x10^{14}$ P/cm$^2$ | |
| 22 | Plasma Clean #5 | $O_2$ Plasma Clean | |
| 23 | $SiO_2$ Etch #3 | HF Etch 20 nm | |
| 24 | Thermal Oxidation #1 | RTA Thermal Ge Oxidation 5 nm | Wafers: PECVD 3 |
| 25 | $SiO_2$ Deposition #3 | PECVD 20 nm | |
| 26 | Anneal #2 | RTA Dopant Activation 600 °C | |
| 27 | $SiO_2$ Deposition #3 | PECVD 480 nm | |
| 28 | Photolithography #2 | Alignment Mark Openings Mask | S1813 (1.3 μm) Resist |
| 29 | $SiO_2$ Etch #4 | HF Etch 500 nm | |
| 30 | Plasma Clean #6 | $O_2$ Plasma Clean | |
| 31 | E-Beam Lithography #5 | Ge Contact Holes Mask | PMMA (1.6 μm) Resist |
| 32 | $SiO_2$ Etch #5 | ICP Etch 450 nm | |

Appendix A: PECVD photodetector process flow

| Step Number | Process Name | Process Description | Comments |
|---|---|---|---|
| 33 | $SiO_2$ Etch #6 | HF Etch 50 nm | |
| 34 | Plasma Clean #7 | $O_2$ Plasma Clean | |
| 35 | Photolithography #3 | Electrodes Mask | AZ2070 (4 μm) Resist |
| 36 | De-Scum #1 | $O_2$ RIE De-Scum | |
| 37 | Water Dip #1 | DI Water Dip | |
| 38 | Metal Stack Sputter #1 | 500 nm Metal Sputter | 50 nm Ti/450 nm Al |
| 39 | Lift Off #1 | 500 nm Metal Lift Off | |
| 40 | Anneal #3 | RTA Metal Anneal 350 °C | |
| 41 | E-Beam Lithography #6 | Electrode Definition Mask | ZEP (1.4 μm) Resist |
| 42 | Metal Etch #1 | 500 nm ICP Metal Etch | |
| 43 | Plasma Clean #8 | $O_2$ Plasma Clean | |
| 44 | Dicing #1 | Dicing Saw | 15x20 mm Pitch |

# Appendix B: RMG photodetector process flow

Table B-1. RMG photodetector process flow.

| Step Number | Process Name | Process Description | Comments |
|---|---|---|---|
| 1 | Photolithography #1 | Alignment Marks & Ge Growth Windows Masks | S1813 (1.3 μm) Resist |
| 2 | Si Etch #1 | ICP 350 nm Etch | |
| 3 | Plasma Clean #1 | $O_2$ Plasma Clean | |
| 4 | Thermal Oxidation #1 | RTA Thermal Si Oxidation 20 nm | |
| 5 | $SiO_2$ Deposition #1 | PECVD 20 nm | |
| 6 | Anneal #1 | RTA 600 °C $SiO_2$ Densification | |
| 7 | Photolithography #2 | Seed Windows Mask | S1813 (1.3 μm) Resist |
| 8 | $SiO_2$ Etch #1 | HF Etch 40 nm | |
| 9 | Plasma Clean #2 | $O_2$ Plasma Clean | |
| 10 | HF Dip #1 | HF Dip 5 seconds | |
| 11 | Ge Growth #1 | PECVD 400 nm Ge | Growth Recipe C |
| 12 | E-Beam Lithography #1 | Ge Etch Mask | AZ2070 (4 μm) Resist |
| 13 | Ge Etch #1 | ICP Etch 400 nm | |
| 14 | Plasma Clean #3 | $O_2$ Plasma Clean | |
| 15 | $SiO_2$ Deposition #2 | PECVD 1000 nm | |
| 16 | Anneal #2 | RTA RMG 950 °C | |
| 17 | $SiO_2$ Etch #2 | HF Etch 1040 nm | |
| 18 | $Si_3N_4$ Backside Deposition #1 | PECVD 300 nm | Wafers: RMG 4 & RMG 5 |
| 19 | E-Beam Lithography #2 | Waveguide & Gratings Masks | ZEP (250 nm) Resist |
| 20 | Si Etch #2 | ICP 220 nm Etch | |
| 21 | Plasma Clean #4 | $O_2$ Plasma Clean | |
| 22 | $SiO_2$ Deposition #3 | PECVD 20 nm | |
| 23 | E-Beam Lithography #3 | P++ Mask | ZEP (450 nm) Resist |
| 24 | Boron Implantation #1 | B ($BF_3$), 20 keV, $1x10^{15}$ B/cm$^2$ | |
| 25 | Plasma Clean #5 | $O_2$ Plasma Clean | |
| 26 | E-Beam Lithography #4 | N++ Mask | ZEP (450 nm) Resist |
| 27 | Phosphorous Implantation #1 | P (Ar+P), 30 keV, $5x10^{14}$ P/cm$^2$ or $7x10^{14}$ P/cm$^2$ | |
| 28 | Plasma Clean #6 | $O_2$ Plasma Clean | |
| 29 | $SiO_2$ Etch #3 | HF Etch 20 nm | |
| 30 | Thermal Oxidation #2 | RTA Thermal Ge Oxidation 5 nm | Wafers: RMG 4 & RMG 5 |
| 31 | $SiO_2$ Deposition #4 | PECVD 20 nm | |

Appendix B: RMG photodetector process flow

| Step Number | Process Name | Process Description | Comments |
|---|---|---|---|
| 32 | Anneal #3 | RTA Dopant Activation 600 °C | |
| 33 | $SiO_2$ Deposition #5 | PECVD 480 nm | |
| 34 | Photolithography #3 | E-Beam Cells Isolation Mask | S1813 (1.3 μm) Resist |
| 35 | $SiO_2$ Etch #4 | HF Etch 500 nm | |
| 36 | Si Etch #3 | ICP 400 nm Etch | |
| 37 | $SiO_2$ Etch #5 | HF Etch 2000 nm | Unsuccessful |
| 38 | Plasma Clean #7 | $O_2$ Plasma Clean | |
| 39* | Photolithography #3 | Alignment Mark Openings Mask | S1813 (1.3 μm) Resist |
| 40* | $SiO_2$ Etch #6 | HF Etch 500 nm | |
| 41* | Plasma Clean #8 | $O_2$ Plasma Clean | |
| 42* | E-Beam Lithography #5 | Ge Contact Holes Mask | PMMA (1.6 μm) Resist |
| 43* | $SiO_2$ Etch #7 | ICP Etch 450 nm | |
| 44* | $SiO_2$ Etch #8 | HF Etch 50 nm | |
| 45* | Plasma Clean #9 | $O_2$ Plasma Clean | |
| 46* | Photolithography #4 | Electrodes Mask | AZ2070 (4 μm) Resist |
| 47* | De-Scum #1 | $O_2$ RIE De-Scum | |
| 48* | Water Dip #1 | DI Water Dip | |
| 49* | Metal Stack Sputter #1 | 500 nm Metal Sputter | 50 nm Ti/450 nm Al |
| 50* | Lift Off #1 | 500 nm Metal Lift Off | |
| 51* | Anneal #4 | RTA Metal Anneal 350 °C | |
| 52* | E-Beam Lithography #6 | Electrode Definition Mask | ZEP (1.4 μm) Resist |
| 53* | Metal Etch #1 | 500 nm ICP Metal Etch | |
| 54* | Plasma Clean #10 | $O_2$ Plasma Clean | |
| 55* | Dicing #1 | Dicing Saw | 15x20 mm Pitch |

*Steps 39-55 were not completed due to wafer bowing issues, as described in Chapter 6.

# Appendix C: Scheil equation derivation

In order to derive the Scheil equation, we consider a small advancement of the growth front, as shown in Fig. C-1. Here, $C_L$ is the Ge composition of the liquid, $C_0$ is the average Ge composition, $k$ is the segregation coefficient, and $f$ is the fraction solidified.

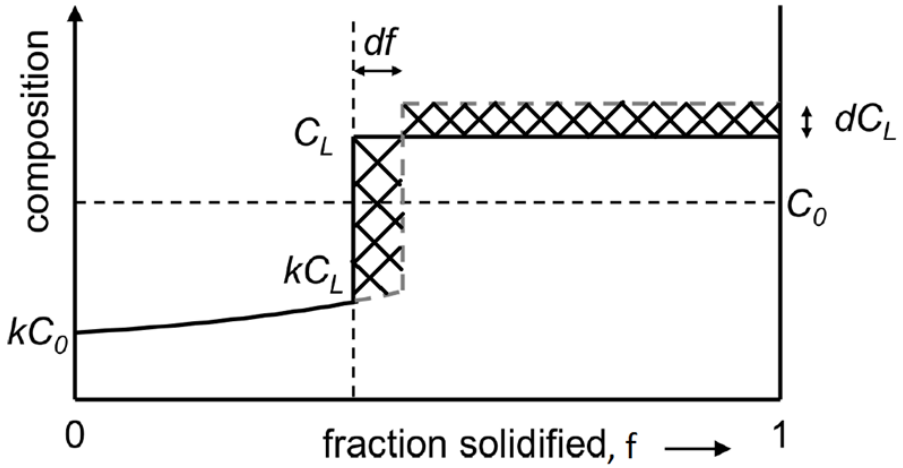


*Fig. C-1. Derivation of the Scheil equation.*

In Fig. C-1, the solid line represents the original composition profile at a given point in time. The dashed line represents the composition profile after a small advancement of the growth front, *df*. At the growth front, Ge is rejected from the solid, into the liquid. Therefore, conservation of mass allows equating of the amount of Ge in the two hashed areas:

$$(C_L - kC_L)\, df = (1-f) dC_L$$

$$C_L(1-k)\, df = (1-f) dC_L$$

Integrating from zero to $f_S$ on the left hand side, and from $C_0$ to $C_L$ on the right hand side, since when $f_S = 0$, $C_L = C_0$:

$$\int_0^{f_S} \frac{1}{(1-f)}\, df = \int_{C_0}^{C_L} \frac{1}{C_L(1-k)}\, dC_L$$

Appendix C: Scheil equation derivation

$$-\ln(1-f_S) = \frac{1}{1-k}\ln\frac{C_L}{C_0}$$

Taking exponentials and rearranging gives:

$$C_L = C_0(1-f_S)^{k-1}$$

Or in terms of the solid composition:

$$C_S = kC_0(1-f_S)^{k-1}$$

This is the Scheil equation. This equation predicts that the solid concentration tends towards infinity, but of course it will only reach 100% Ge.

# Appendix D: Complete mixing model derivation

In order to derive the complete mixing model, we consider a small advancement of the growth front, as shown in Fig. D-1. Here $C_L$ is the Ge composition of the liquid, $C_0$ is the average Ge composition, $C_S$ is the Ge composition of the solid, $C_{seed}$ is the solid Ge composition at the edge of the seed, and $f_S$ is the fraction solidified.

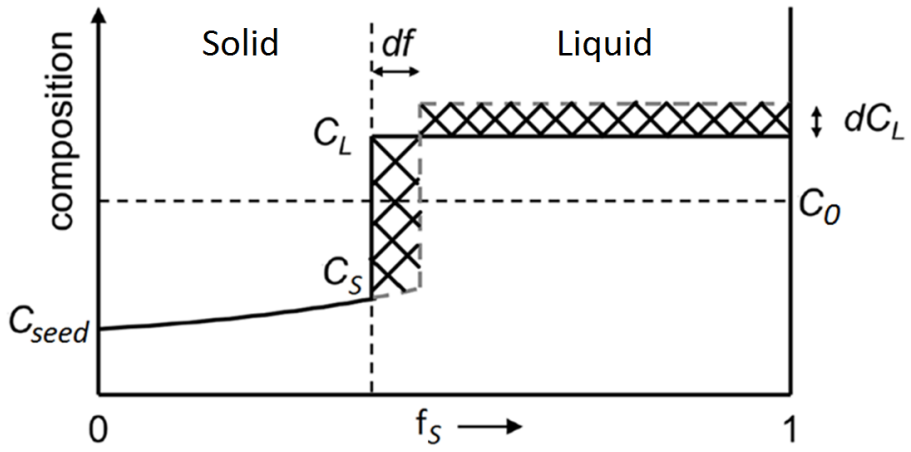


*Fig. D-1. Derivation of the complete mixing model.*

In Fig. D-1, the solid line represents the original composition profile at a given point in time. The dashed line represents the composition profile after a small advancement of the growth front, *df*. At the growth front, Ge is rejected from the solid, into the liquid. Therefore, conservation of mass allows equating of the amount of Ge in the two hashed areas:

$$(C_L - C_S)\, df = (1 - f_S) dC_L$$

$$\frac{1}{(1 - f_S)} df_S = \frac{1}{(C_L - C_S)} dC_L \qquad \text{Equation D-1}$$

Appendix D: Complete mixing model derivation

The segregation coefficient, *k*, is given by:

$$k = \frac{C_S}{C_L} = 0.78C_S + 0.21$$

$$C_L = \frac{C_S}{0.78C_S + 0.21} \qquad \text{Equation D-2}$$

Equation D-2 implies that:

$$C_S = \frac{0.21C_L}{1 - 0.78C_L} \qquad \text{Equation D-3}$$

Substituting Equation D-3 into Equation D-1:

$$\int \frac{1}{(1 - f_S)} df_S = \int \frac{1}{(C_L - C_S)} dC_L = \int \frac{1}{C_L\left(1 - \frac{0.21}{1 - 0.78C_L}\right)} dC_L$$

$$\int \frac{1}{(1 - f_S)} df_S = \int \frac{1 - 0.78C_L}{C_L(0.79 - 0.78C_L)} dC_L \qquad \text{Equation D-4}$$

Using partial fractions to simplify the right hand side:

$$\int \frac{1}{(1 - f_S)} df_S = \int \frac{1}{0.79C_L} + \frac{0.78(\frac{1}{0.79} - 1)}{0.79 - 0.78C_L} dC_L$$

Integrating both sides:

$$-\ln(1 - f_S) = \frac{1}{0.79}\ln C_L - \left(\frac{1}{0.79} - 1\right)\ln(0.79 - 0.78C_L) + \ln c$$

Where ln(c) is a constant. Simplifying the right hand side:

$$-\ln(1 - f_S) = \frac{1}{0.79}[\ln C_L - \ln(0.79 - 0.78C_L)] + \ln(0.79 - 0.78C_L) + \ln c$$

$$= \frac{1}{0.79}\ln\left(\frac{C_L}{0.79 - 0.78C_L}\right) + \ln(0.79 - 0.78C_L) + \ln c$$

If the coefficient of the second term on the right hand side is rewritten as $\frac{1}{0.79} - \frac{0.21}{0.79} = 1$ then:

$$-\ln(1-f_S) = \frac{1}{0.79}\ln\left(\frac{C_L}{0.79-0.78C_L}\right) + \left(\frac{1}{0.79} - \frac{0.21}{0.79}\right)\ln(0.79-0.78C_L) + \ln c$$

$$= \frac{1}{0.79}\left[\ln\left(\frac{C_L}{0.79-0.78C_L}\right) + \ln(0.79-0.78C_L)\right] - \frac{0.21}{0.79}\ln(0.79-0.78C_L) + \ln c$$

$$= \frac{1}{0.79}\ln\left(\frac{C_L(0.79-0.78C_L)}{0.79-0.78C_L}\right) - \frac{0.21}{0.79}\ln(0.79-0.78C_L) + \ln c$$

$$= \frac{1}{0.79}\ln C_L - \frac{0.21}{0.79}\ln(0.79-0.78C_L) + \ln c$$

$$= \ln\left(C_L^{\frac{1}{0.79}}\right) + \ln\left[(0.79-0.78C_L)^{-\frac{0.21}{0.79}}\right] + \ln c$$

$$= \ln\left(C_L^{\frac{1}{0.79}}\right) + \ln\left[\left(\frac{1}{0.79-0.78C_L}\right)^{\frac{0.21}{0.79}}\right] + \ln c$$

$$= \ln\left[C_L^{\frac{1}{0.79}}\left(\frac{1}{0.79-0.78C_L}\right)^{\frac{0.21}{0.79}} c\right]$$

Multiplying both sides by -1:

$$\ln(1-f_S) = -\ln\left[C_L^{\frac{1}{0.79}}\left(\frac{1}{0.79-0.78C_L}\right)^{\frac{0.21}{0.79}} c\right]$$

$$= \ln\left[C_L^{-\frac{1}{0.79}}\left(\frac{1}{0.79-0.78C_L}\right)^{-\frac{0.21}{0.79}} c^{-1}\right]$$

$$= \ln\left[\left(\frac{1}{C_L}\right)^{\frac{1}{0.79}}(0.79-0.78C_L)^{\frac{0.21}{0.79}}c^{-1}\right]$$

Taking exponentials of both sides:

$$1-f_S = \left(\frac{1}{C_L}\right)^{\frac{1}{0.79}}(0.79-0.78C_L)^{\frac{0.21}{0.79}}c^{-1} \qquad \text{Equation D-5}$$

Appendix D: Complete mixing model derivation

Using the fact that $C_S = C_{seed}$ when $f_S = 0$ and calculating $c$:

$$c = \left(\frac{1}{\widehat{C_L}}\right)^{\frac{1}{0.79}} \left(0.79 - 0.78\widehat{C_L}\right)^{\frac{0.21}{0.79}}$$

Where $\widehat{C_L}$ is $C_L$ when $C_S = C_{seed}$, i.e. $\widehat{C_L} = \frac{C_{seed}}{0.78C_{seed}+0.21}$. Substituting c back into Equation D-5:

$$1 - f_S = \left(\frac{\widehat{C_L}}{C_L}\right)^{\frac{1}{0.79}} \left(\frac{0.79 - 0.78C_L}{0.79 - 0.78\widehat{C_L}}\right)^{\frac{0.21}{0.79}} \qquad \text{Equation D-6}$$

Substituting Equation D-2 and $\widehat{C_L}$ into the first term on the right hand side of Equation D-6:

$$1 - f_S = \left(\frac{\frac{C_{seed}}{0.78C_{seed} + 0.21}}{\frac{C_S}{0.78C_S + 0.21}}\right)^{\frac{1}{0.79}} \left(\frac{0.79 - 0.78C_L}{0.79 - 0.78\widehat{C_L}}\right)^{\frac{0.21}{0.79}}$$

$$= \left(\frac{C_{seed}}{C_S}\right)^{\frac{1}{0.79}} \left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right)^{\frac{1}{0.79}} \left(\frac{0.79 - 0.78C_L}{0.79 - 0.78\widehat{C_L}}\right)^{\frac{0.21}{0.79}}$$

Considering the second term on the right hand side of Equation D-6, and substituting in both Equation D-2 and $\widehat{C_L}$:

$$\frac{0.79 - 0.78C_L}{0.79 - 0.78\widehat{C_L}} = \frac{0.79 - \frac{0.78C_S}{0.78C_S + 0.21}}{0.79 - \frac{0.78C_{seed}}{0.78C_{seed} + 0.21}}$$

$$= \left(\frac{\frac{1}{0.78C_S + 0.21}}{\frac{1}{0.78C_{seed} + 0.21}}\right)\left(\frac{0.79(0.78C_S + 0.21) - 0.78C_S}{0.79(0.78C_{seed} + 0.21) - 0.78C_{seed}}\right)$$

$$= \left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right)^{-1}\left(\frac{0.79(0.78C_S + 0.21) - 0.78C_S}{0.79(0.78C_{seed} + 0.21) - 0.78C_{seed}}\right)$$

$$= \left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right)^{-1}\left(\frac{0.78C_S(0.79 - 1) + 0.79(0.21)}{0.78C_{Seed}(0.79 - 1) + 0.79(0.21)}\right)$$

$$= \left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right)^{-1}\left(\frac{0.78C_S(-0.21) + 0.79(0.21)}{0.78C_{Seed}(-0.21) + 0.79(0.21)}\right)$$

$$= \left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right)^{-1} \left(\frac{0.21(0.79 - 0.78C_S)}{0.21(0.79 - 0.78C_{Seed})}\right)$$

$$= \left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right)^{-1} \left(\frac{0.79 - 0.78C_S}{0.79 - 0.78C_{Seed}}\right)$$

Substituting this into Equation D-6:

$$1 - f_S = \left(\frac{C_{seed}}{C_S}\right)^{\frac{1}{0.79}} \left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right)^{\frac{1}{0.79}} \left(\left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right)^{-1} \left(\frac{0.79 - 0.78C_S}{0.79 - 0.78C_{Seed}}\right)\right)^{\frac{0.21}{0.79}}$$

$$= \left(\frac{C_{seed}}{C_S}\right)^{\frac{1}{0.79}} \left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right)^{\frac{1}{0.79}} \left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right)^{-\frac{0.21}{0.79}} \left(\frac{0.79 - 0.78C_S}{0.79 - 0.78C_{Seed}}\right)^{\frac{0.21}{0.79}}$$

$$1 - f_S = \left(\frac{C_{seed}}{C_S}\right)^{\frac{1}{0.79}} \left(\frac{0.79 - 0.78C_S}{0.79 - 0.78C_{Seed}}\right)^{\frac{0.21}{0.79}} \left(\frac{0.78C_S + 0.21}{0.78C_{seed} + 0.21}\right) \quad \text{Equation D-7}$$

This is the complete mixing model, which is valid for Ge compositions between 0.4 and 1.0, due to the simplified linear fit to the segregation coefficient that was used (Equation D-2).

# Appendix D: Complete mixing model derivation

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